IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.	)	
	)	
Plaintiff,	)	
	)	
v.	)	
	)	
SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.	)	Civil Action No. 2:21-CV-463-JRG
	)	
	)	JURY TRIAL DEMANDED
Defendants.	)	

FIRST AMENDED COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its First Amended Complaint against defendants Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. Netlist filed its initial complaint against Defendants on December 20, 2021. Dkt. 1 ("Initial Complaint"). In its Initial Complaint, Netlist presented allegations regarding Defendants' infringement of three of Netlist's patents: U.S. Patent Nos. 10,860,506 (the "'506 Patent," Ex. 1), 10,949,339 (the "'339 Patent," Ex. 2), and 11,016,918 (the "'918 Patent," Ex. 3). Netlist also indicated its intent to assert then pending U.S. Pat. No. 11,232,054 (the "'054 Patent," Ex. 4) upon issuance. On December 28, 2021, Defendants filed an unopposed motion confirming

the parties' agreement to waive service for SEC, and set the deadline for Defendants' answer to the Initial Complaint as April 12, 2022. Dkt. 10. Defendants collectively filed an answer on April 12, 2022 (Dkt. 16) without moving to dismiss the Initial Complaint. Netlist now enters its First Amended Complaint as a matter of course pursuant to Fed. R. Civ. Proc., Rule 15(a)(1)(B).

3. Upon the entry of this First Amended Complaint, this action now involves six of Netlist's patents: the '506 Patent, the '339 Patent, the '918 Patent, the '054 Patent, and U.S. Patent Nos. 8,787,060 (the "'060 Patent," Ex. 5), and 9,318,160 (the "'160 Patent," Ex. 6) (collectively, the "Patents-in-Suit").

I. THE PARTIES

4. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

5. On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi, 16677, Republic of Korea. On information and belief, SEC is the worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this First Amended Complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

6. On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale

and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201. SEA is a wholly owned subsidiary of SEC.

7. On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, Defendant SSI maintains facilities at 6625 Excellence Way, Plano, Texas 75023. Defendant SSI may be served with process through its registered agent National Registered Agents, Inc., 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136. On information and belief, SSI is a wholly owned subsidiary of SEA.

8. On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

9. Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

10. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

11. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through

subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

12. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). For example, SEC maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. As another example, SEA maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. Venue is also proper for SSI because it maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district.

13. Defendants have not contested proper venue in this District. *See, e.g.*, Answer at ¶ 10, *Arbor Global Strategies LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-333, Dkt. 43 (E.D. Tex. Apr. 27, 2020); Answer at ¶ 29, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-347, Dkt. 14 (E.D. Tex. Feb. 12, 2020).

III. FACTUAL ALLEGATIONS

Background

14. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast

amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

15. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LR-DIMM"), HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

16. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

17. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications. The structure, function, and operation of memory modules is defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), the standard-setting body for the microelectronics industry. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

The Asserted Netlist Patents

The '506 Patent

18. The '506 Patent is entitled "Memory Module With Timing-Controlled Data Buffering." Netlist owns the '506 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '506 Patent was filed as Application No. 16/391,151 on April 22, 2019, issued as a patent on December 8, 2020, and claims priority to, among others, a utility application filed on July 27, 2013 (No. 13/952,599) and a provisional application filed on July 27, 2012 (No. 61/676,883).

19. Samsung had knowledge of the '506 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket. Samsung has also gained knowledge of the '506 Patent via the Initial Complaint filed on December 20, 2021.

20. As described in the '506 Patent, in conventional memory modules, the "distribution of control signals and a control clock signal in the memory module is subject to strict constraints" to ensure that memory devices on the memory module can be properly accessed. Ex. 1 at 2:16-17. For example, in some conventional memory modules, "control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules." *Id.* at 2:20-24. But as noted in the '506 Patent, "[t]he balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections." *Id.* at 2:24-27. In yet other conventional memory systems, the memory controller includes mechanisms such as read or write leveling for compensating for unbalanced wire lengths on the memory module. *Id.* at 2:30-32. However, with increasing memory operating speed and memory density "such leveling mechanisms are also insufficient to

ensure proper timing of the control and/or data signals received and/or transmitted by the memory modules." *Id.* at 2:32-36.

21. The '506 Patent discloses a memory module operable in a memory system with a memory controller that includes memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data signal lines in a data bus and respective sets of the memory devices. As summarized in the Abstract, "[e]ach respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals." *Id.*, Abstract.

22. The buffer circuits (118, highlighted below) are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices as illustrated in the exemplary configuration of Figure 2A.

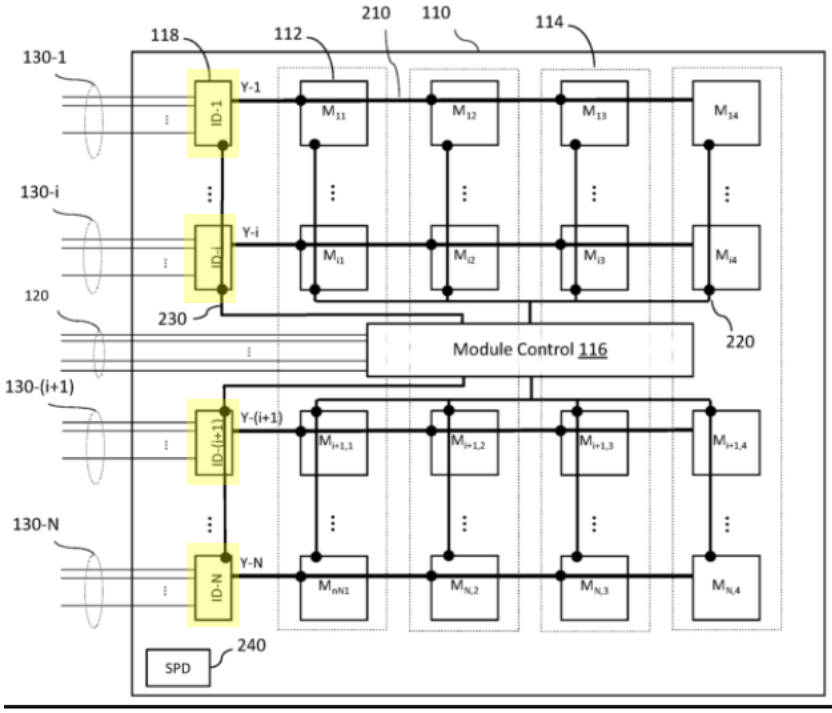


FIG. 2A

23. However, because the buffer circuits—or "isolation devices"—are distributed across the memory module, at high speeds of operation, the same set of module control signals sent by the module control circuit in the module may reach different buffer circuits at different times across one cycle of the system clock. *Id.* at 9:51-62 ("Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n−1) in the exemplary configuration shown in FIG. 2."). The '506 Patent discloses an embodiment wherein "each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100." *Id.* at 10:11-21.

<u>The '339 Patent</u>

24. The '339 Patent is entitled "Memory Module With Controlled Byte-Wise Buffers." Netlist owns the '339 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '339 Patent was filed as Application No. 15/470,856 on March 27, 2017, issued as a patent on March 16, 2021, and claims priority to U.S. Patent Application No. 12/504,131 filed on July 16, 2009, U.S. Patent Application No. 12/761,179 filed on April 15, 2010 and U.S. Application No. 13/970,606 filed on August 20, 2013.

25. Samsung had knowledge of the ’339 Patent no later than August 2, 2021 via its access to Netlist’s patent portfolio docket. Samsung has also gained knowledge of the ’339 Patent via the Initial Complaint filed on December 20, 2021.

26. As described in the ’339 Patent, in optimizing performance of memory subsystems (e.g. memory modules) “consideration is always given to memory density, power dissipation (or thermal dissipation, speed, and cost.” Ex. 2 at 2:5-7. The ’339 Patent further explains that “[g]enerally, these attributes are not orthogonal to each other, meaning that optimizing one attribute may detrimentally affect another attribute. For example, increasing memory density typically causes higher power dissipation, slower operational speed, and higher costs.” *Id.* at 2:7-12. The ’339 Patent is generally directed to a memory module optimized to reduce the load experienced by a system memory controller via the use of configurable data transmission circuits.

27. The ’339 Patent discloses a memory module configured to communicate with a memory controller that includes DDR DRAM devices arranged in multiple ranks each of the same width as the memory module, and a module controller configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals. As summarized in the Abstract, “[t]he registered address and control signals selects one of the multiple ranks to perform the read or write operation. The module controller further outputs a set of module control signals in response to the input address and control signals. The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank.” *Id.*, Abstract.

28. Figure 3A illustrates an example of a memory subsystem consistent with embodiments disclosed in the ’339 Patent.

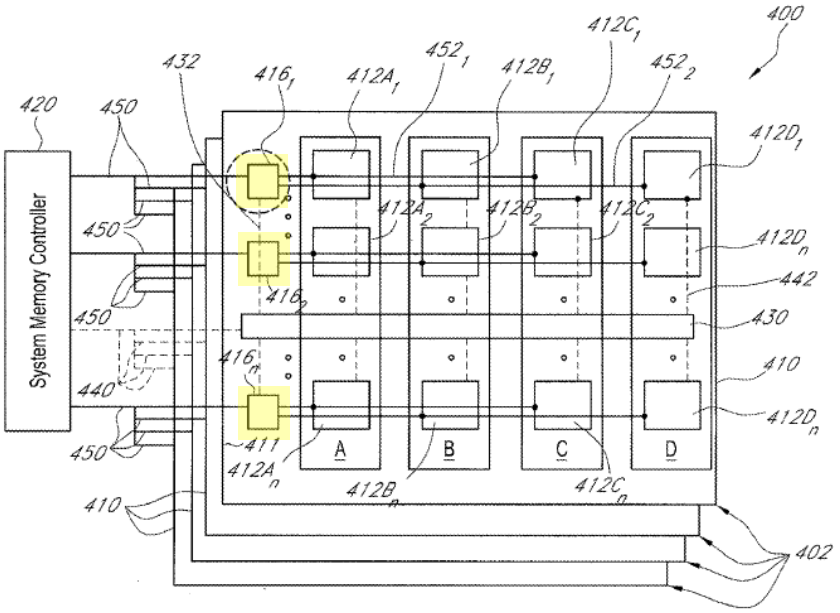


FIG. 3A

29. As shown above, Figure 3A depicts a memory subsystem 400 including memory modules 402 comprising memory devices 412, data transmission circuits 416 (highlighted above), and module control circuits 430. The data transmission circuits 416 operate to reduce the load experienced by the memory controller 420 to improve performance of a read or write operation. *Id.* at 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. . . . Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system . . . ."). In certain embodiments, "the data

transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively coupled." *Id.* at 13:31-36.

The '918 Patent

30. The '918 Patent is entitled "Flash-DRAM Hybrid Memory Module." Netlist owns the '918 Patent by assignment from the listed inventors Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta. The '918 Patent was filed as Application No. 17/138,766 on December 30, 2020, issued as a patent on May 25, 2021, and claims priority to, among others, U.S. Application No. 13,559,476 filed on July 26, 2012; U.S. Application No. 12/240,916 filed on September 29, 2008; U.S. Application No. 12/131,873 filed on June 2, 2008; as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

31. Samsung had knowledge of the '918 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket via notice of U.S. Patent Application No. 12/240,916 and U.S. Patent Application No. 12/131,873 on August 2, 2021. Samsung has also gained knowledge of the '918 Patent via the Initial Complaint filed on December 20, 2021.

32. As summarized in the Abstract, the '918 Patent discloses a memory module that includes a printed circuit board with an interface that couples it to a host system for provision of power, data, address and control signals, and additionally features "[f]irst, second, and third buck converters [that] receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage

monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." Ex. 3, Abstract.

33. The '918 Patent discloses, *inter alia*, a power module that provides power to various components of the memory system as depicted in Figure 16, shown below.

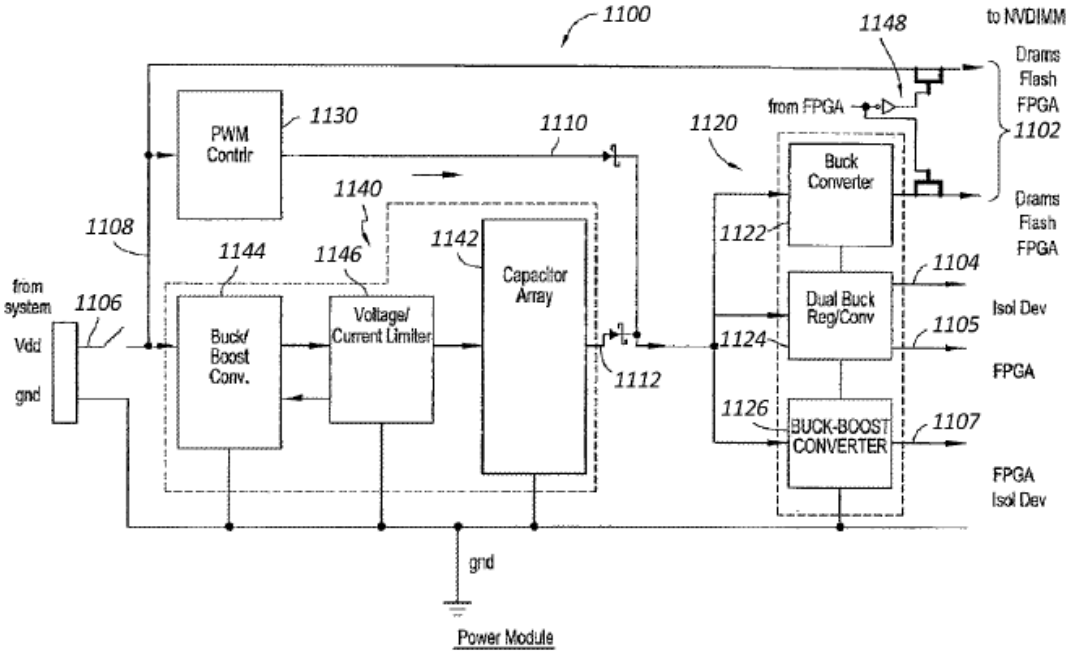


FIG. 16

34. The '918 Patent explains that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller." *Id.* at 28:3-15. "The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters." *Id.* at 29:18-19.

35. This design represents a fundamental departure from prior generations of DDR modules for which the voltage regulation was provided by power management units located on motherboards, external to the DDR modules. In contrast, the ’918 Patent (as well as its continuation, the ’054 Patent, discussed below), moves the voltage regulation and many other power management functions into the DDR modules themselves, therefore allowing for more precise and accurate regulation of voltages and more efficient power management.

36. The inventions of the ’918 Patent provide for the effective operation of DDR5 memory modules, by enabling, among other benefits, greater power efficiency than previous generations of DDR technology. The DDR5 standard is characterized by the use of an on-module power management system. Samsung itself notes “[t]he on-DIMM PMIC further boosts power management efficiency and power supply stability.” Ex. 12 at 5.

The ’054 Patent

37. The ’054 Patent is entitled “Flash-DRAM Hybrid Memory Module.” Netlist owns the ’054 Patent by assignment from the listed inventors Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta. The ’054 Patent was filed as Application No. 17/328,019 on May 24, 2021, issued as a patent on January 25, 2022, and claims priority to, among others, U.S. Application No. 13,559,476 filed on July 26, 2012; U.S. Application No. 12/240,916 filed on September 29, 2008; U.S. Application No. 12/131,873 filed on June 2, 2008; as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

38. Samsung has had knowledge of the application leading to the ’054 Patent no later than December 20, 2021, and the patent itself no later than January 25, 2022.

39. As summarized in the Abstract, the ’054 Patent discloses a memory module that includes a printed circuit board with an interface that couples it to a host system for provision of

power, data, address and control signals, and additionally features "[f]irst, second, and third buck converters [that] receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." Ex. 4, Abstract.

40. The '054 Patent discloses, *inter alia*, a power module that provides power to various components of the memory system as depicted in Figure 16, shown below.

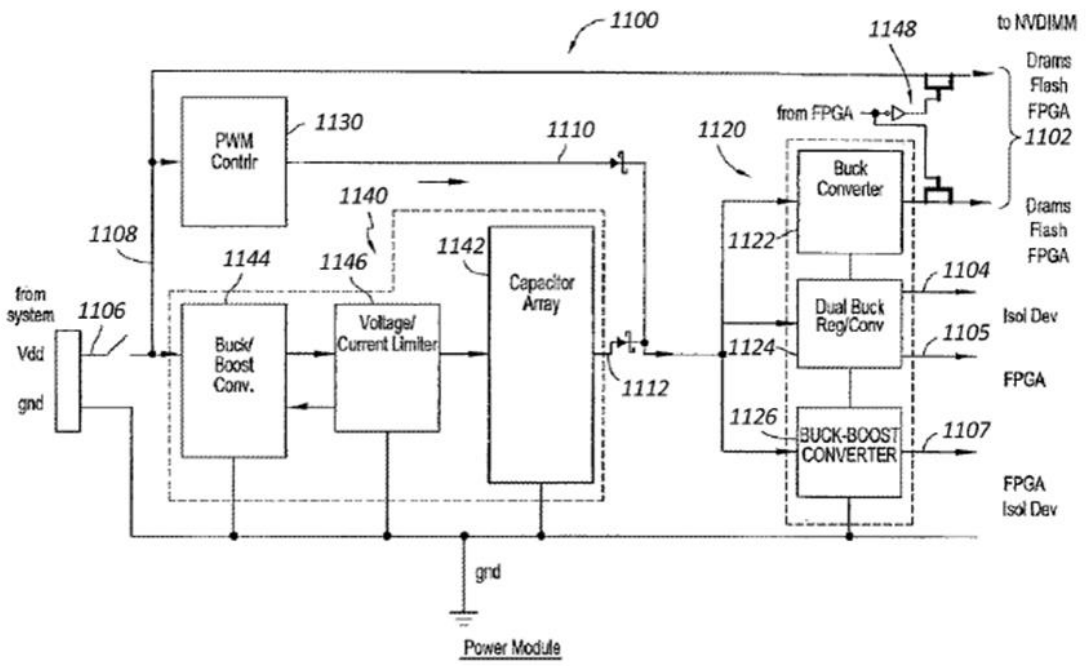


FIG. 16

41. Like the inventions of the '918 Patent, the inventions of the '054 Patent provide for the effective operation of DDR5 memory modules, by enabling, among other benefits, greater power efficiency than previous generations of DDR technology. *See supra* ¶¶ 35-36.

The ’060 and ’160 Patents

42. The ’060 Patent is entitled “Method and Apparatus for Optimizing Driver Load in a Memory Package.” Netlist owns the ’060 Patent by assignment from listed inventor Hyun Lee. The ’060 Patent was filed as Application No. 13/288,850 on November 3, 2011, issued as a patent on July 22, 2014, and claims priority to a provisional application filed on November 3, 2010 (No. 61/409,893).

43. The ’160 Patent is a continuation of the ‘060 patent and is entitled “Memory Package with Optimized Driver Load and Method of Operation.” Netlist owns the ’160 Patent by assignment from listed inventor Hyun Lee. The ’160 Patent was filed as Application No. 14/337,168 on July 21, 2014, issued as a patent on April 19, 2016, and claims priority to, among others, a utility application filed on November 3, 2011 (No. 13/288,850, which issued as the ‘060 patent) and a provisional application filed on November 3, 2010 (No. 61/409,893).

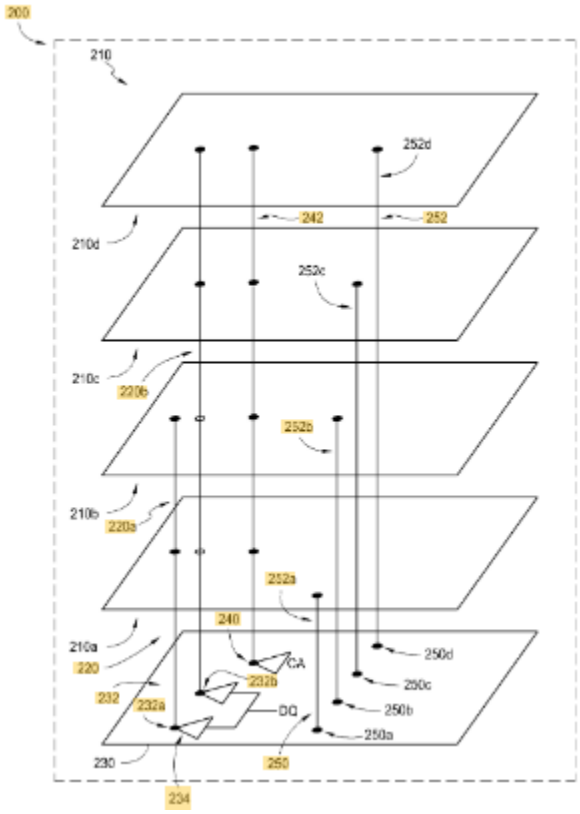
44. Samsung had knowledge of the ’060 and ’160 Patents no later than August 2, 2021 via its access to Netlist’s patent portfolio docket. Samsung also has knowledge of the two patents as of the filing of this First Amended Complaint.

45. The ’060 and ’160 Patents disclose systems and methods for optimizing a load in a memory package featuring a control die, array dies, and numerous die interconnects. In contrast to traditional DDR modules in which different DRAM devices are packaged individually and then assembled on a common printed circuit boards, the inventions of the ’060 and ’160 Patents are directed to DDR modules each having multiple vertically stacked DRAM devices interconnected to a common control circuit, all packaged in a same package.

46. For example, as summarized in the Abstract, the memory package features at least two die interconnects, where “[t]he first die interconnect is in electrical communication with a data port of a first array die and a data port of a second array die and not in electrical communication

with data ports of a third array die. The second die interconnect is in electrical communication with a data port of the third array die and not in electrical communication with data ports of the first array die and the second array die." Ex. 5, Abstract; Ex. 6, Abstract. The memory package's control die includes "a first data conduit configured to transmit a data signal to the first die interconnect and not to the second die interconnect, and at least a second data conduit configured to transmit the data signal to the second die interconnect and not to the first die interconnect." *Id.*

47. The '060 and '160 Patents explain that in conventional memory packages, the die interconnects are in communication with ***each*** of the array dies, which disadvantageously increases the load on the data conduit. Ex. 5, at 11:32-40. To address this problem, the '060 and '160 Patents disclose memory packages with multiple die interconnects in electrical communication with ***some***, but not all of the array dies, as illustrated below. *Id.* at 5:46-6:36.



48. As the '060 and '160 Patents explain, in the disclosed memory packages "[e]ach of these die interconnects 320 may be coupled to, or in electrical communication with at least one

port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 ***without being in electrical communication with a port from at least one array die 310***, which may be in electrical communication with a different die interconnect 320. *Id.* at 5:54-62 (emphasis added). This enables the memory packages to be designed with smaller form factor in mind, and lowers power consumption. *See id.* at 7:22-8:62.

Samsung's Infringing Activities

49. Samsung is a global technology company and one of the largest manufacturers of semiconductor memory products such as DRAM, NAND Flash, and MCP (Multi-Chip Package) such as high-bandwidth memories ("HBM"). Samsung develops, manufactures, sells, offers to sell, and imports into the United States memory components and memory modules designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications.

50. Samsung and Netlist were initially partners under a 2015 Joint Development and License Agreement ("JDLA"), which granted Samsung a 5-year paid-up license to Netlist's patents "having an effective first filing date on or prior to" November 12, 2020. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 20-cv-993, Dkt. 186 at 20-21 (C.D. Cal. Oct. 14, 2021). On information and belief, Samsung used Netlist's technologies to develop products both in the mature markets such as DDR4 memory modules and the emerging market for new generations of DRAM technologies, including DDR5 and HBMs. Under the JDLA, Samsung was obligated to supply Netlist certain memory products at competitive prices. Samsung, however, did not honor its promises and repeatedly failed to fulfill Netlist's product orders. As a result, Netlist terminated the JDLA on July 15, 2020, which termination was found effective by a federal district court in the Central District of California on October 14, 2021. *Id.*

51. On February 15, 2022 the Central District Court entered judgement in favor of Netlist on all three of its contract claims. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 20-cv-993, Dkt. 306 (C.D. Cal. Feb. 15, 2022).

52. In entering judgement in favor of Netlist on all its claims, Judge Scarsi stated explicitly that "Netlist terminated the JDLA pursuant to JDLA § 13.2, and Samsung's licenses and rights under the JDLA have ceased." *Id.* at 2.

53. Following the entry of Judgment in the Central District, Defendants responded to Netlist's Initial Complaint in this action by submitting themselves to the jurisdiction of this Court via answer. *See* Dkt. 16.

DDR4 Memory Modules

54. On information and belief, Samsung makes, uses, sells, offers to sell, and/or imports within this District and elsewhere in the United States, without authority, infringing DDR4 LRDIMMs, DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, HBM2 and HBM2E products, and other products that have materially the same structures and designs in relevant parts (the "Accused Instrumentalities").

55. The accused DDR4 LRDIMMs include, without limitation, any Samsung DDR4 LRDIMM products made, sold, offered for sale, used and/or imported into the United States by Samsung. By way of non-limiting example, the accused DDR4 LRDIMMs products include Samsung products having the following part numbers: M386A4K40BB0-CRC, M386A8K40BM1-CRC, M386A8K40BM2-CTD, M386A8K40BMB-CRC, M386A8K40CM2-CRC, M386A8K40CM2-CTD, M386A8K40CM2-CVF, M386A8K40DM2-CTD, M386A8K40DM2-CVF, M386A8K40DM2-CWE, M386AAG40AM3-CWE, M386AAG40MM2-CVF, M386AAG40MMB-CVF, M386AAK40B40-CUC, M386AAK40B40-CWD, M386ABG40M50-CYF, M386ABG40M51-CAE, M386ABG40M5B-CYF. Further

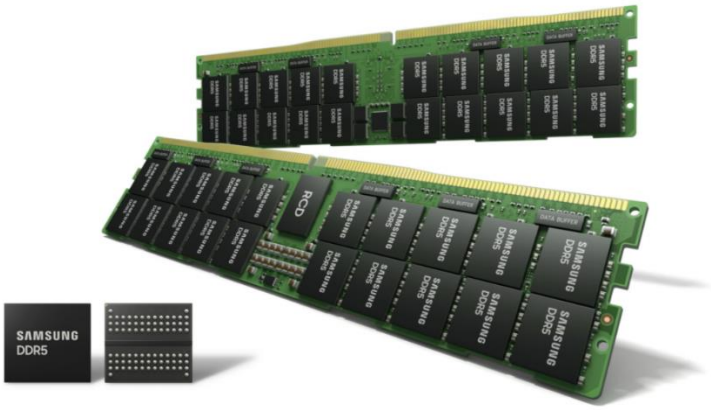
examples of Samsung's DDR4 LRDIMM products can be found via Samsung's module-selector web page. *See Module: Memory Modules For Extensive Use*, Samsung, *available at* https://www.samsung.com/semiconductor/dram/module.

DDR5 Memory Modules

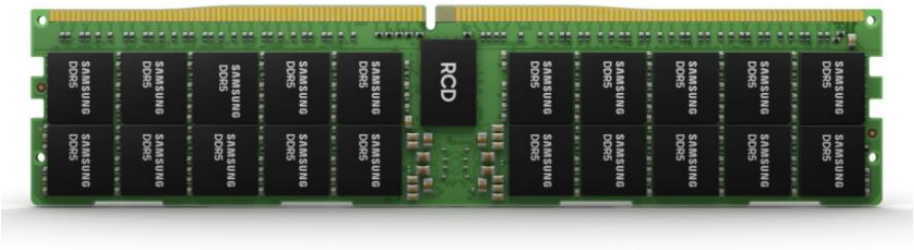
56. The accused DDR5 products include, without limitation, any Samsung DDR5 products made, sold, offered for sale, used and/or imported into the United States by Samsung. By way of non-limiting example, the accused DDR5 products include Samsung products having the following part numbers: M323R2GA3BB0-CQK0D, M321R8GA0BB0-CQK, M321R4GA0BB0-CQKEG, and M323R2GA3BB0-CQK0D.

57. As further example, the Accused Instrumentalities include, without limitation, any DDR5 products made, sold, offered for sale, used and/or imported into the United States by Samsung, including those modules utilizing Samsung's own power management IC (including at least PMIC components having part numbers: S2FPC01, S2FPD01, and S2FPD02) that Samsung confirms "fully support JEDEC standards." Ex. 17 (S2FPC01); Ex. 18 (S2FPD01).

58. By way of non-limiting example, the accused DDR5 products also include products marketed and publicized in an October 12, 2021 Samsung Press release, as shown below.

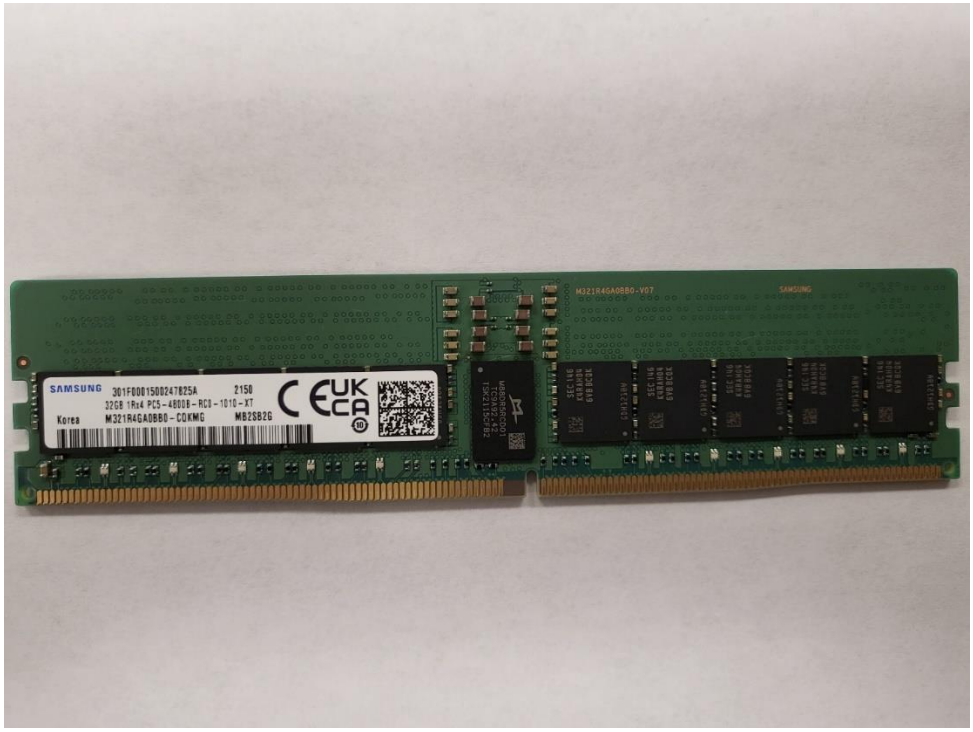


Ex. 8 at 1 (depiction of a Samsung DDR5 LRDIMM).



Id. at 2 (depiction of a Samsung DDR5 RDIMM).

59. An example of a Samsung DDR5 RDIMM obtainable in the U.S. is shown below:

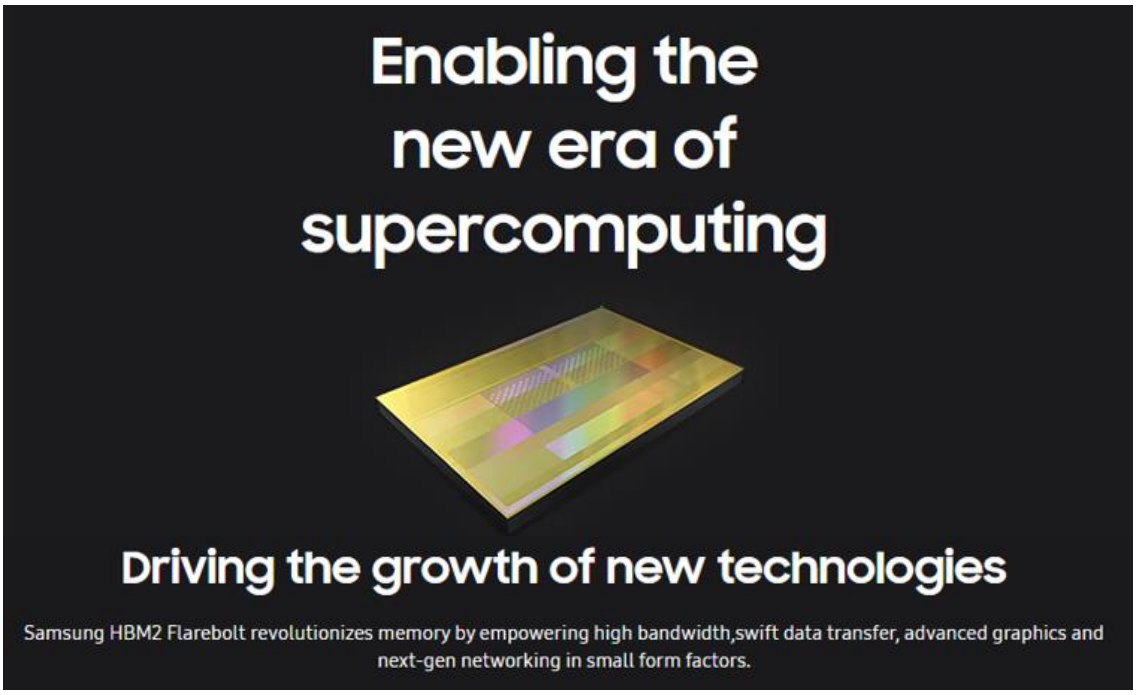


60. As further example, the Accused Instrumentalities include, without limitation, any Samsung DDR5 UDIMM and DDR5 SODIMMs products made, sold, offered for sale, used and/or imported into the United States by Samsung. An example of a Samsung DDR5 UDIMM obtainable in the U.S. is shown below:

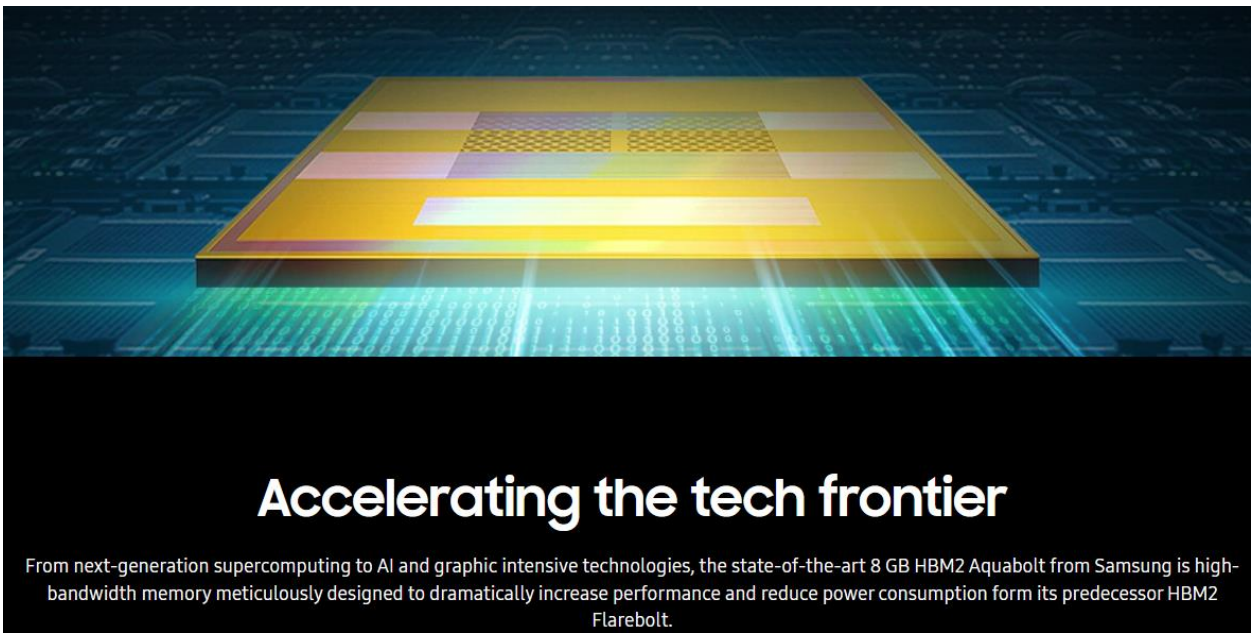
High Bandwidth Memory ("HBM")

61. HBM is a type of high-speed computer memory technology that relies in part on vertically-stacked memory dies and differs from the DDR4 or DDR5 DIMM formats described in the paragraphs above. Samsung is a major supplier of HBM. Samsung itself confirms that its HBM products are "optimized for high-performance computing (HPC), and offer the performance needed to power next-generation technologies, such as artificial intelligence (AI)." Ex. 20 at 2.

62. The Accused HBM Products include, without limitation, any Samsung HBM2, HBM2E and newer products with 8 or more stacked DRAM dies made, sold, used, offered for sale, and/or imported into the United States by Samsung. By way of non-limiting example, the Accused HBM Products include Samsung's HBM2 Flarebolt, including, without limitation, the following product: KHA883901B-MC12. *See HBM2 Flarebolt*, Samsung, *available at* https://semiconductor.samsung.com/dram/hbm/hbm2-flarebolt/.



63. The Accused HBM Products further include Samsung's HBM2 Aquabolt, including, without limitation, products having the following part numbers: KHA884901X-MC12, KHA884901X-MC13, KHA884901X-MN12, KHA884901X-MN13. *See* HBM2 Aquabolt, Samsung, *available at* https://semiconductor.samsung.com/dram/hbm/hbm2-aquabolt/.

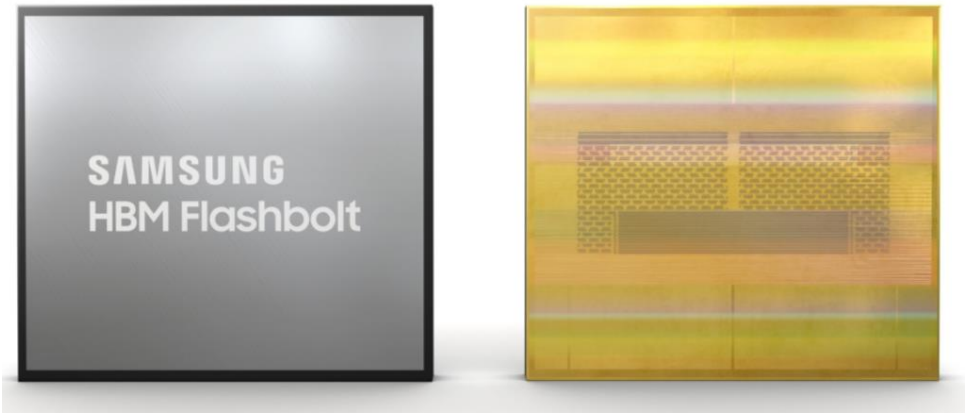


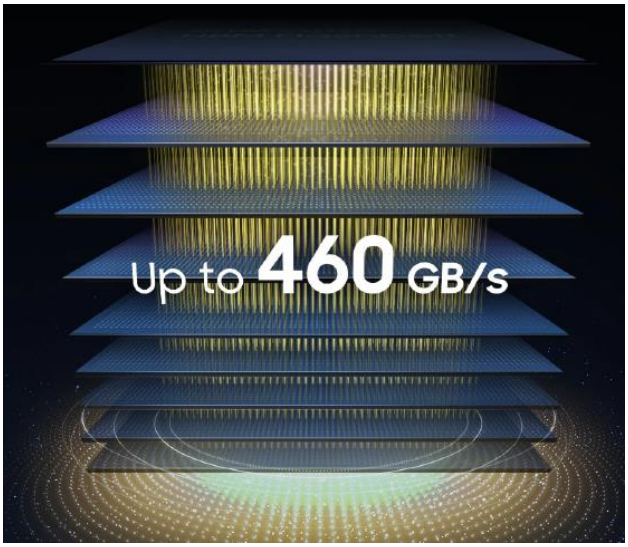
See also, e.g., Ex. 21 at 2-3:

> To achieve HBM2 Aquabolt's unprecedented performance, Samsung has applied new technologies related to TSV design and thermal control. A single 8GB HBM2 package consists of eight 8Gb HBM2 dies, which are vertically interconnected using over 5,000 TSVs (Through Silicon Via's) per die. While using so many TSVs can cause collateral clock skew, Samsung succeeded in minimizing the skew to a very modest level and significantly enhancing chip performance in the process.

64. The Accused HBM Products further include Samsung's HBM2E Flashbolt, including, without limitation, products having the following part numbers: KHAA44801B-MC17, KHAA84901B-MC17, KHAA44801B-MC16, KHAA84901B-JC16, KHAA84901B-JC17, KHAA84901B-MC16. Further examples of Samsung's HBM2E products can be found via Samsung's part-selector web page. *See HBM2E Flashbolt*, Samsung, *available at* https://semiconductor.samsung.com/dram/hbm/hbm2e-flashbolt/ (representative product depicted below); *see also, e.g.*,

New HBM2E stacks eight 16Gb DRAM dies to achieve 16GB package capacity and ensures a stable data transfer speed at 3.2Gbps





HBM2E Flashbolt offers about twice the capacity of the previous generation HBM solution by stacking eight layers of 10nm-class 16 Gb DRAM dies. A larger capacity allows the development of deeper neural networks that greatly improves the speed of acquiring results for Big Data analytics.

※ Source from Samsung Datasheet (Available upon request)

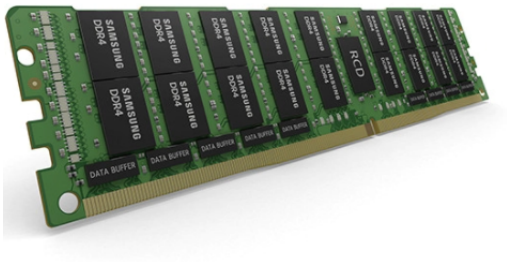
IV. FIRST CLAIM FOR RELIEF – '506 PATENT

65. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

66. On information and belief, Samsung directly infringed and is currently infringing at least one claim of the '506 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '506 Patent.[1]

[1] The theories set forth herein are based on Netlist's present understanding of the Samsung Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, Netlist's contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

67. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs.



LRDIMM

Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

Ex. 19 at 2 (depiction of a Samsung DDR4 LRDIMM).

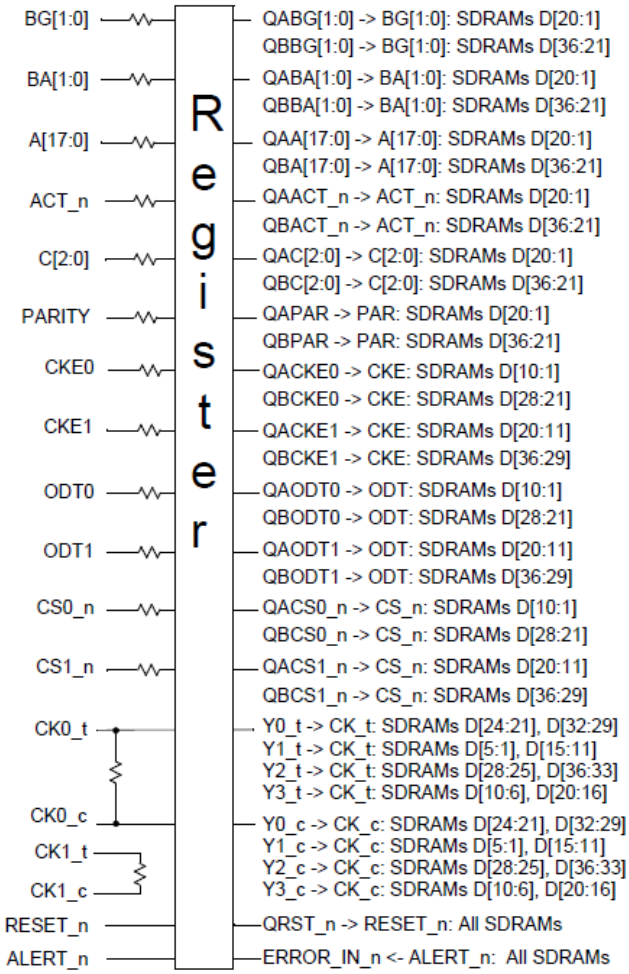
68. Each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced data signal." *Id.* It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus. For example:

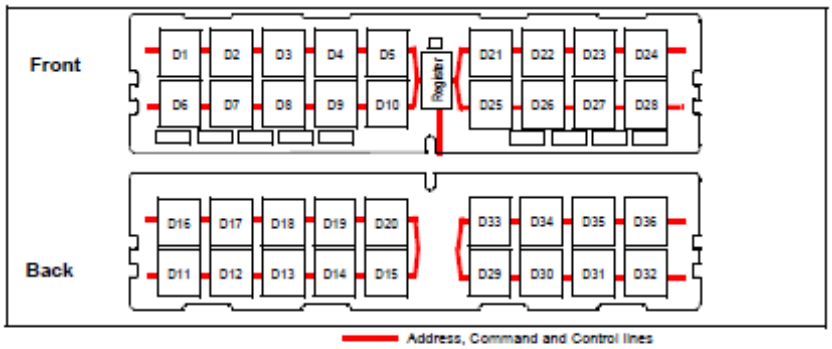
5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address input	SCL	I2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PAR	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM core power supply
WE_n[4]	SDRAM write enable	C0, C1, C2	Chip ID lines for 3DS SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines	VDDSPD	Serial SPD-TSE positive power supply
ACT_n	Register input for activate	ALERT_n	SDRAM ALERT_n
DQ0–DQ63	DIMM memory data bus	VPP	SDRAM Supply
CB0–CB7	DIMM ECC check bits	RESET_n	Set DRAMs to a Known State
DQS0_t–DQS17_t	SDRAM data strobes (positive line of differential pair)	EVENT_n	SPD-TSE signals a thermal event has occurred.
DQS0_c–DQS17_c	SDRAM data strobes (negative line of differential pair)	VTT	SDRAM I/O termination supply
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	RFU	Reserved for future use
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Ex. 7 (M386AAK40B40 Datasheet) at 6.





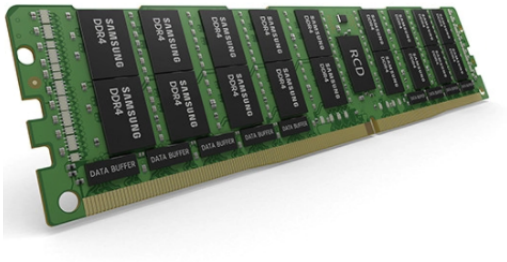
NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

- 10 -

SAMSUNG

Id. at 10 (red lines in original).

69. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.



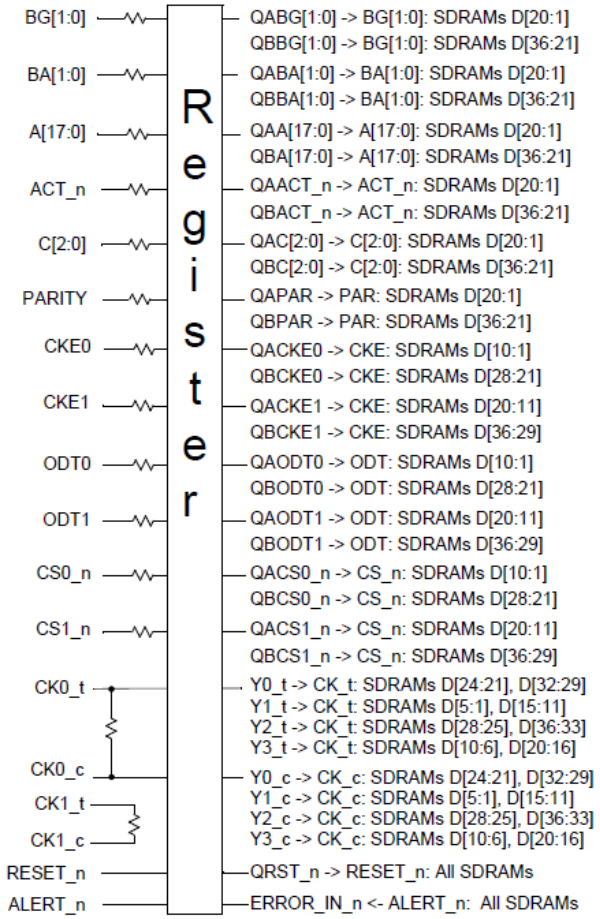
LRDIMM

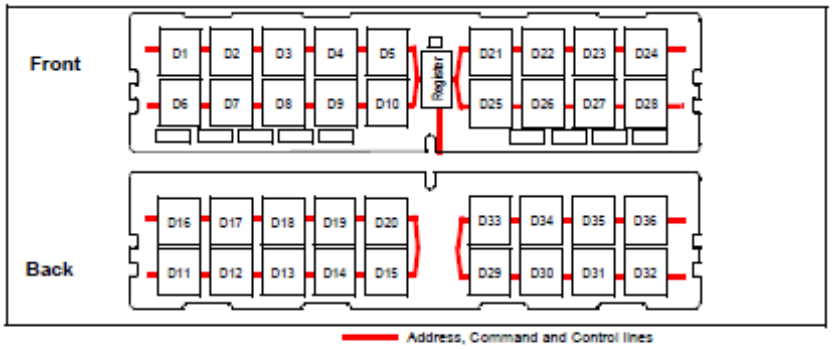
Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

Ex. 19 at 2 (depiction of a Samsung DDR4 LRDIMM); *see also* Ex. 7 (M386AAK40B40 Datasheet) at 42.

70. The accused DDR4 LRDIMMs further each comprise a module control device (*e.g.*, a registering clock driver, or "RCD") on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals, as illustrated in the example below.



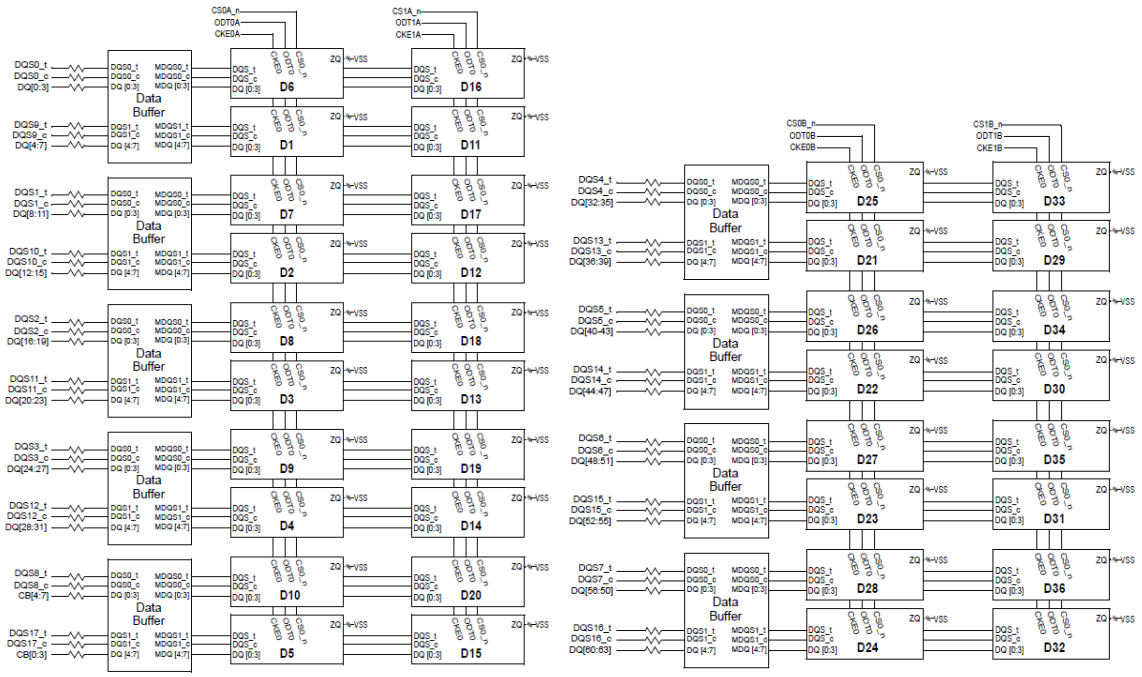


NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

- 10 -

SAMSUNG

Ex. 7 (M386AAK40B40 Datasheet) at 10 (red lines in original); *see also id.* at 42.

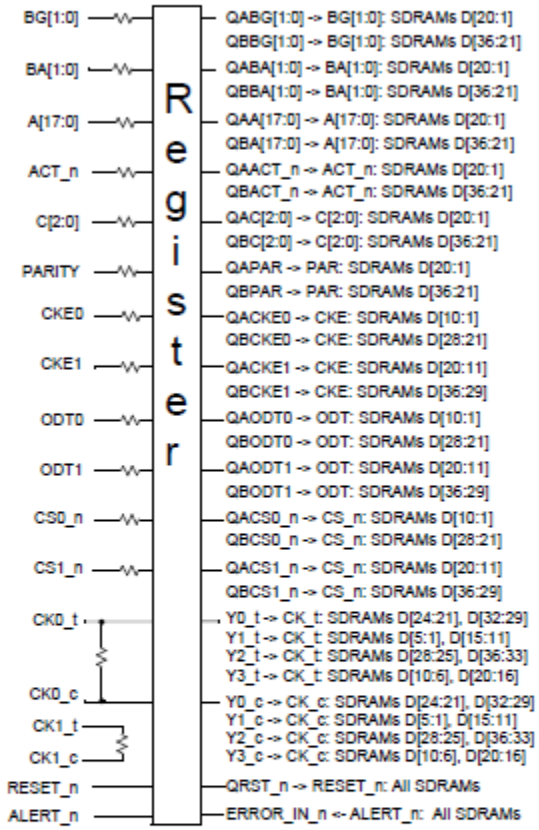


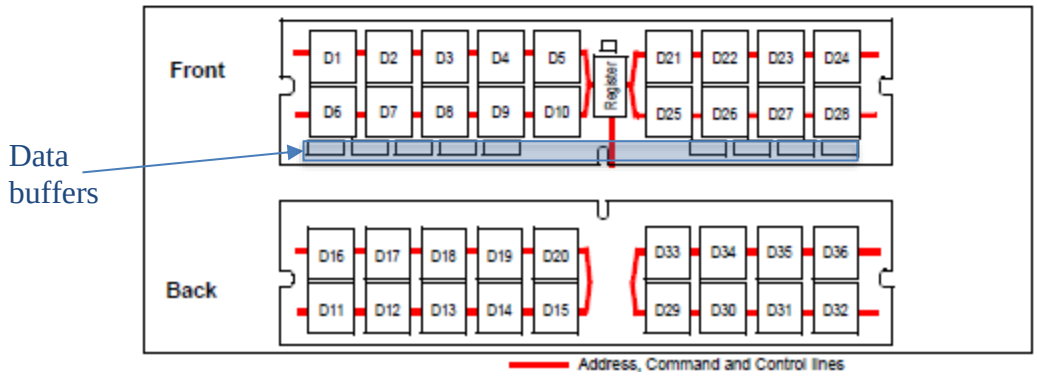
Id. at 11-12.

71. The accused DDR4 LRDIMMs also each include memory devices arranged in multiple ranks on the module board and coupled to the module control device (*e.g.*, RCD) via module C/A signal lines that conduct the registered C/A signals, as illustrated in the examples below.

9.1 128GB, 16Gx72 Module

(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM



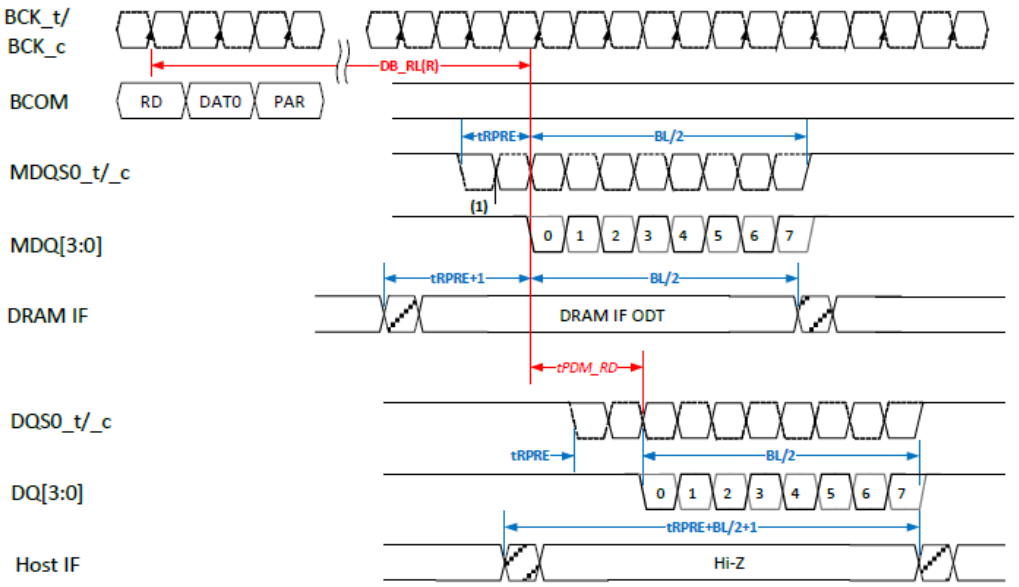


Id. at 10 (red lines in original); *see also id.* at 42.

72. In each accused DDR4 LRDIMM's memory devices, the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a

first read strobe. For example, each accused DDR4 LRDIMM follows the timing sequence for a READ command shown below.

Figure 3 shows the timing sequence for a Read command.



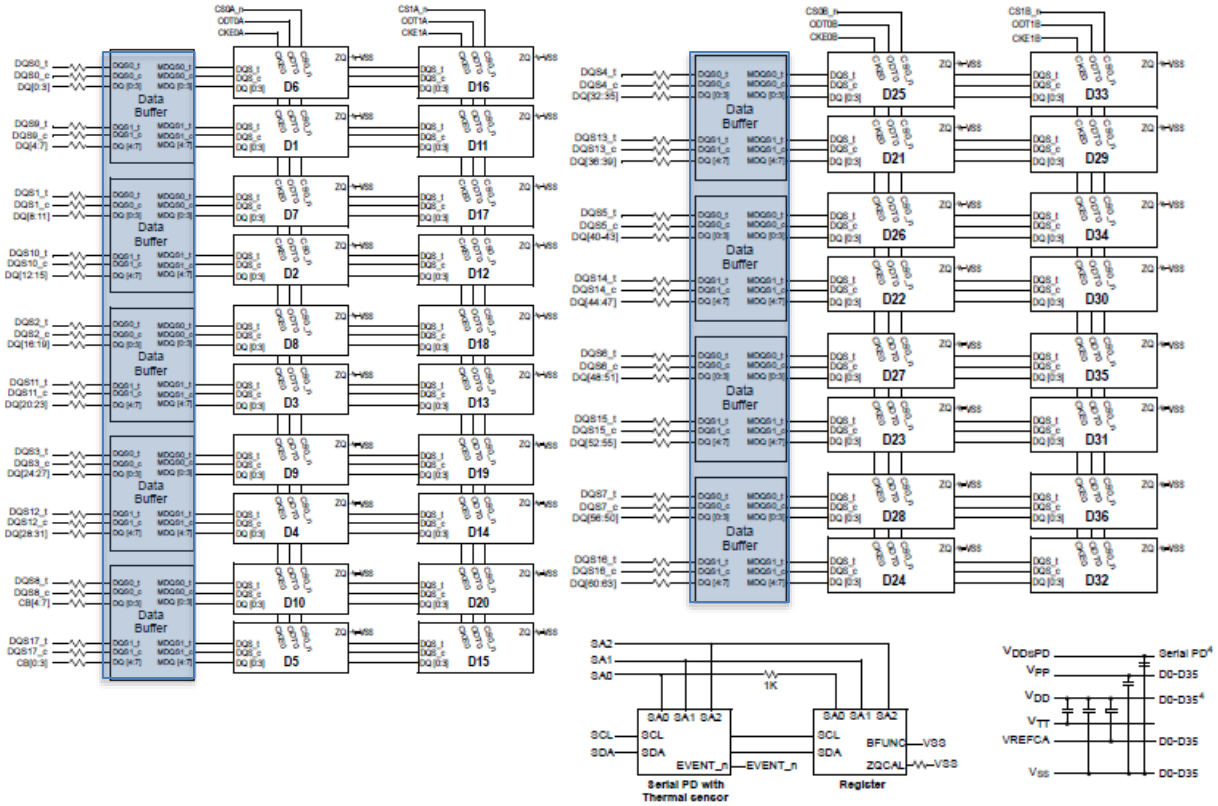
(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 3 — READ Timing

Ex. 9 (JEDEC JESD82-32A Standard), at 14 (annotated); *see also*, *e.g.*, Ex. 7 (M386AAK40B40 Datasheet) at 11-12 (functional block for a representative product, depicted above).

73. The accused DDR4 LRDIMMs further each include data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, as illustrated below.

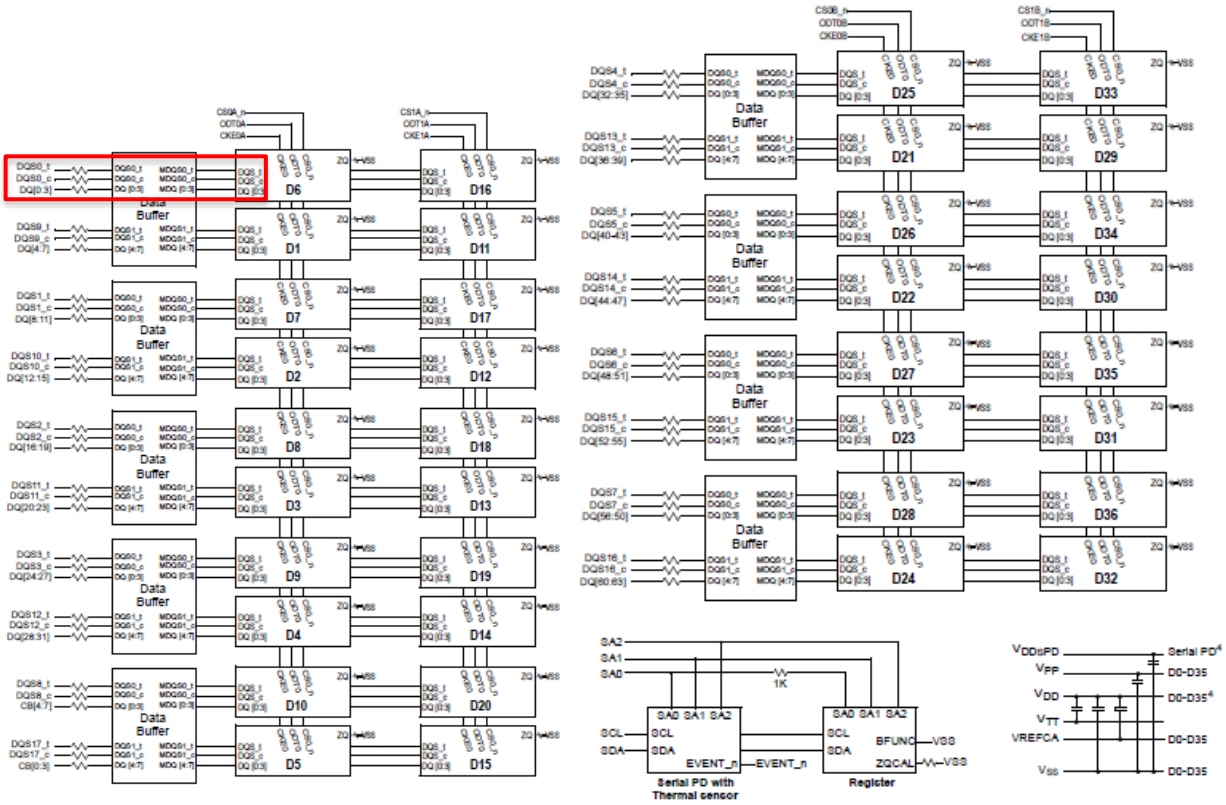
Ex. 19 at 2 (depiction of a Samsung DDR4 LRDIMM).



Ex. 7 (M386AAK40B40 Datasheet) at 11-12 (annotated to illustrate data buffers coupled between at least one respective memory device in each of the multiple ranks).

74. In each accused DDR4 LRDIMM, a first data buffer on the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read

strobe; sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus; wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations. For example, the strobes MDQS0_t and MDQS0_c are delayed by a variable delay circuitry and produce a first delayed read strobe. The data buffer determines the predetermined amount of delay based on, for example, BCOM signals received from the memory controller of the host in one or more previous operations, which signals in turn are in response to information sent by the memory module as part of MRD training.



Ex. 7 (M386AAK40B40 Datasheet) at 11-12.

75. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '506 Patent

through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

76. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '506 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, the accused DDR4 LRDIMM products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM and other materially similar products would be covered by one or more claims of the '506 Patents. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM and other materially similar products infringes at least one claim of the '506 Patent.

77. Samsung's infringement of the '506 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '506 Patent since at least August 2, 2021. Samsung's infringement of the '506 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement,

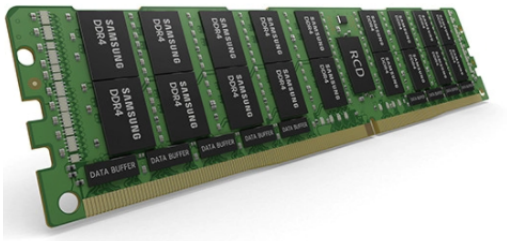
and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

V. SECOND CLAIM FOR RELIEF – '339 PATENT

78. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

79. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '339 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '339 Patent.

80. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a N-bit-wide memory module *(e.g.*, 64-bit-wide) mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide. For instance, each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced data signal." Ex. 19 at 2. It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus.



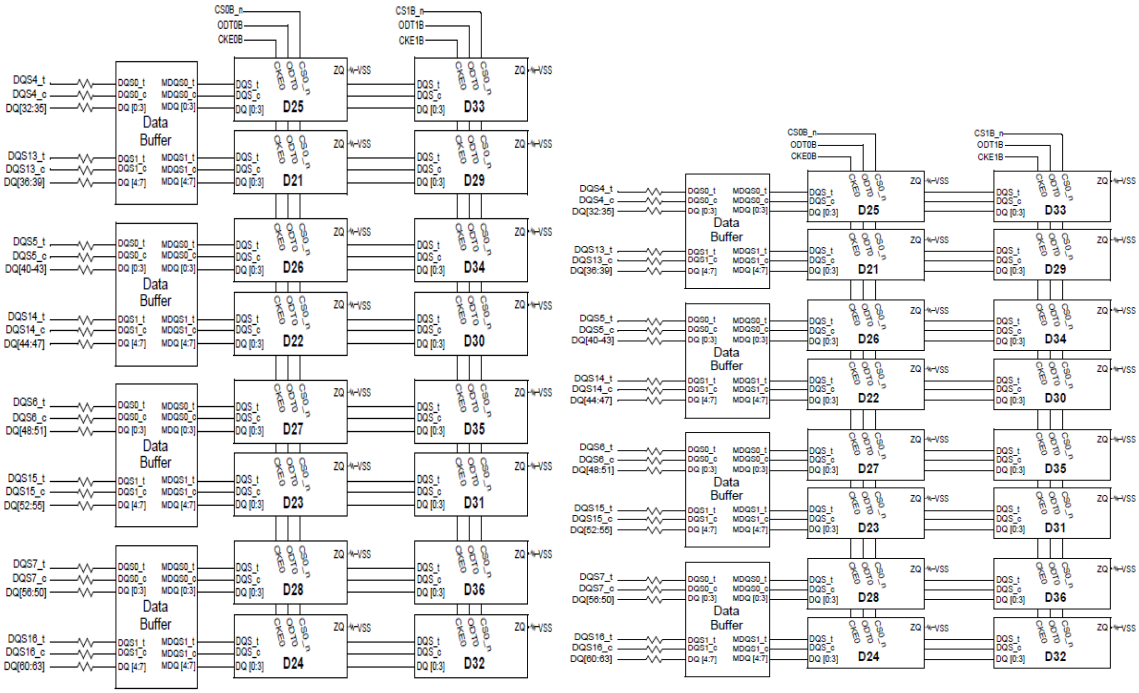
LRDIMM

Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

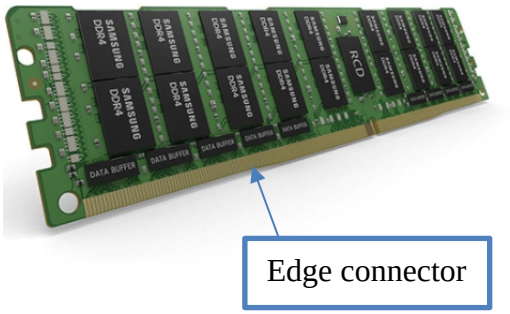
Id. at 2 (depiction of a Samsung DDR4 LRDIMM).

81. In the configuration above, there are 9 sets of byte-wide signal lines including 64-bit wide data signal lines (DQ0-DQ63) and 8-bit wide check bits signal lines (CB0-CB7). For example:



Ex. 7 (M386AAK40B40 Datasheet) at 11-12.

82. The accused DDR4 LRDIMMs each comprise a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket. For example:



LRDIMM

Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

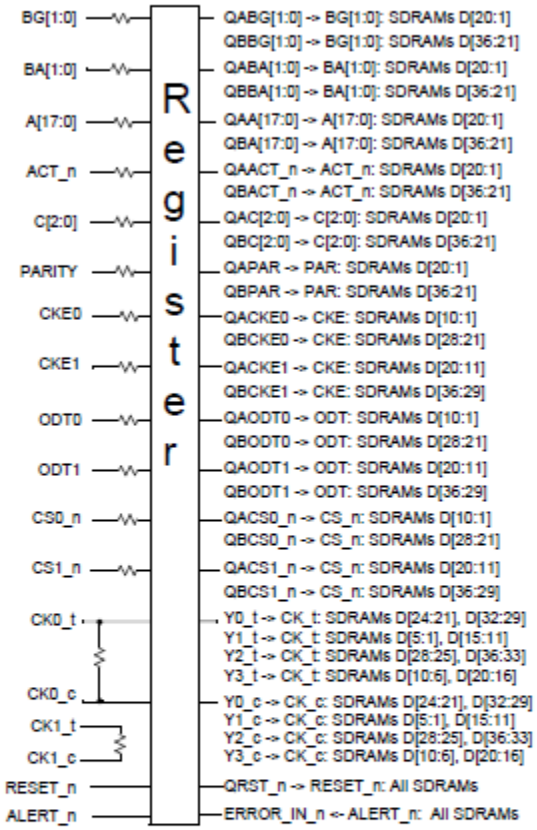
Ex. 19 at 2 (depiction of a Samsung DDR4 LRDIMM).

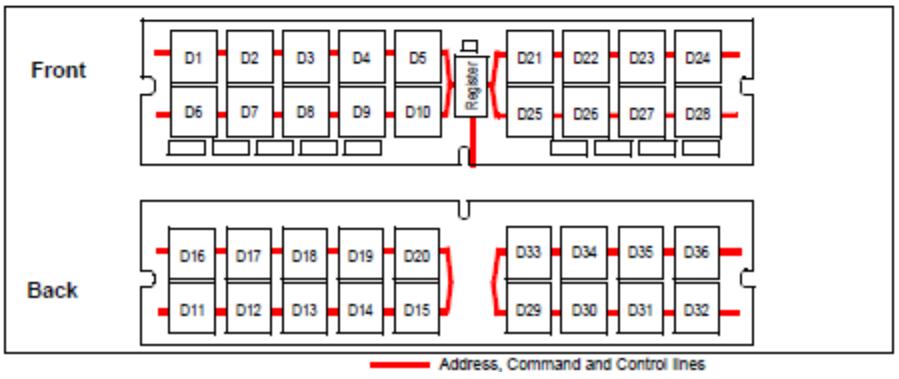
83. The accused DDR4 LRDIMMs each include double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks. As shown above, each DDR4 LRDIMM module includes multiple ranks of memory devices.

84. The accused DDR4 LRDIMMs further comprise a module controller (*e.g.*, RCD) coupled to the PCB and operatively coupled to the DDR DRAM devices. For example:

9.1 128GB, 16Gx72 Module

(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM





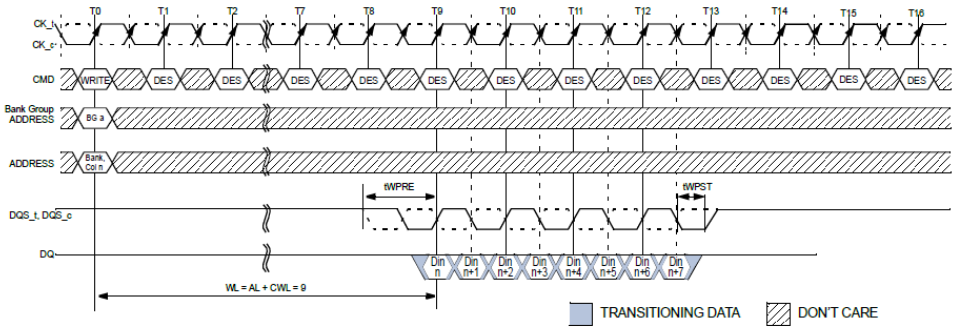
Ex. 7 (M386AAK40B40 Datasheet) at 10 (red lines in original); *see also id.* at 42.

85. The module controller (*e.g.*, RCD) is configurable to receive from the memory controller via the address and control signal lines (*e.g.*, red lines above) input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and

control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data (*e.g.*, by using a registered chip-select signal to select a target rank for performing the memory write operation), wherein the module controller is further configurable to output module control signals (*e.g.*, during a first clock cycle when BCOM [3:0] is 1000, the module control signals would correspond to a write WR command) in response to at least some of the input address and control signals. For example, a Write burst operation results in a burst of data and data strobes received by the DDR4 LRDIMM via the DQS/DQ pins of the memory bus, and to write the data via data buffers into a memory device as determined by input address and control signal (*e.g.*, CS signal). *See*, *e.g.*, Ex. 10 (JESD79-4C DDR4 SDRAM Standard), at 122.

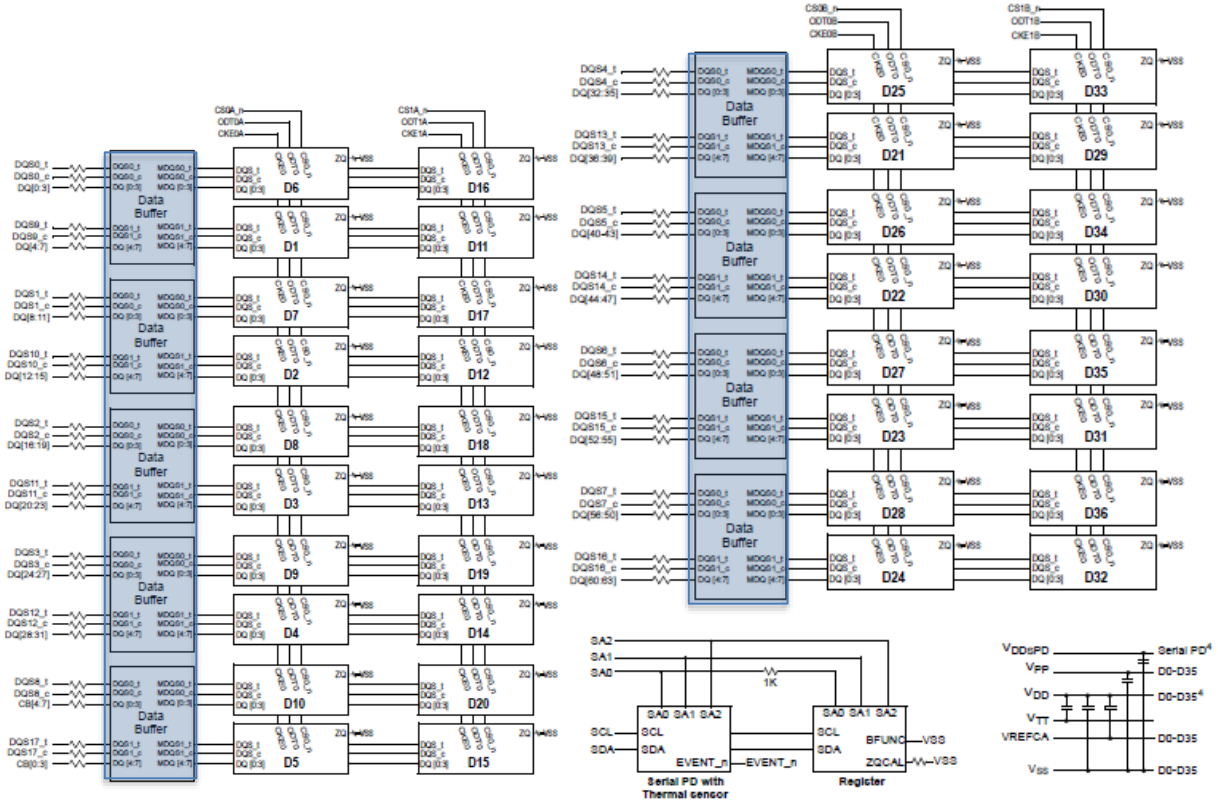
4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

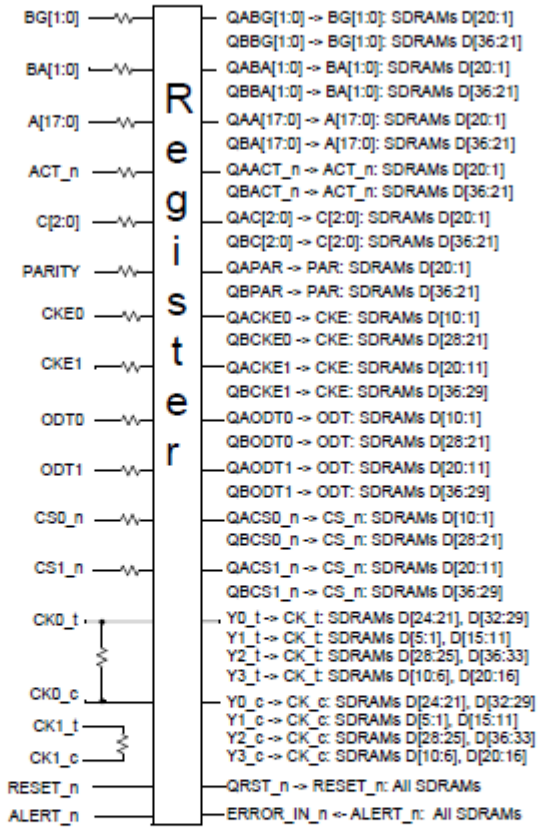
Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)

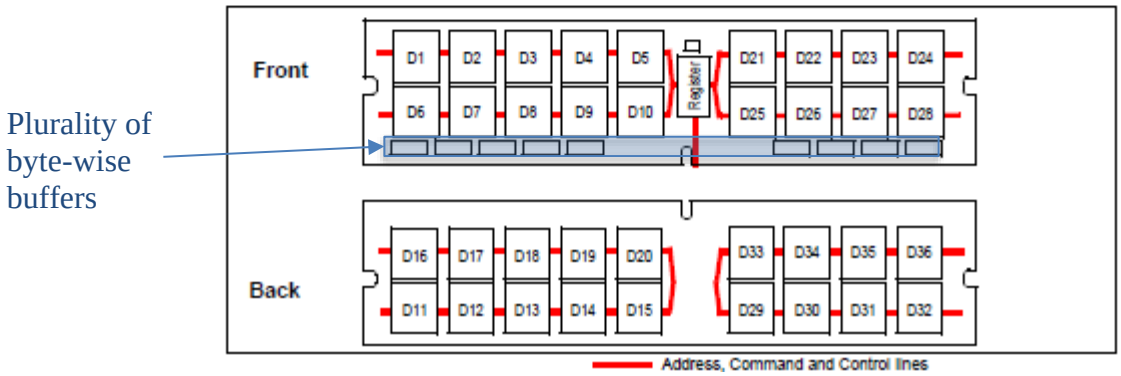


Ex. 7 (M386AAK40B40 Datasheet) at 11-12 (annotated to illustrate plurality of byte-wise buffers).

9.1 128GB, 16Gx72 Module

(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM





Ex. 7 (M386AAK40B40 Datasheet) at 10 (red lines in original); *see also id.* at 42.

86. Further, as illustrated above and below, the accused DDR4 LRDIMMs also each comprise a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second

side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines.

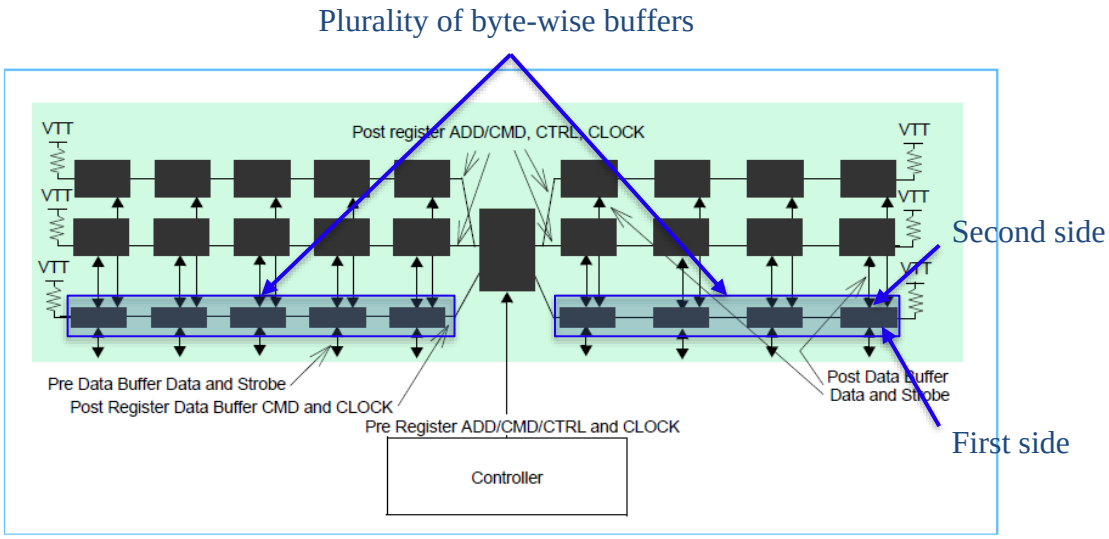


Figure 3 — LRDIMM Topologies

Ex. 11 (JEDEC 21C Standard), at 4.20.27-17.

87. In each of the accused DDR4 LRDIMMs, the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals and the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers, *e.g.*, via the MDQ_OE signal associated with a particular TX for a particular MDQ bit, to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period. For example:

4.61 Logic Diagram

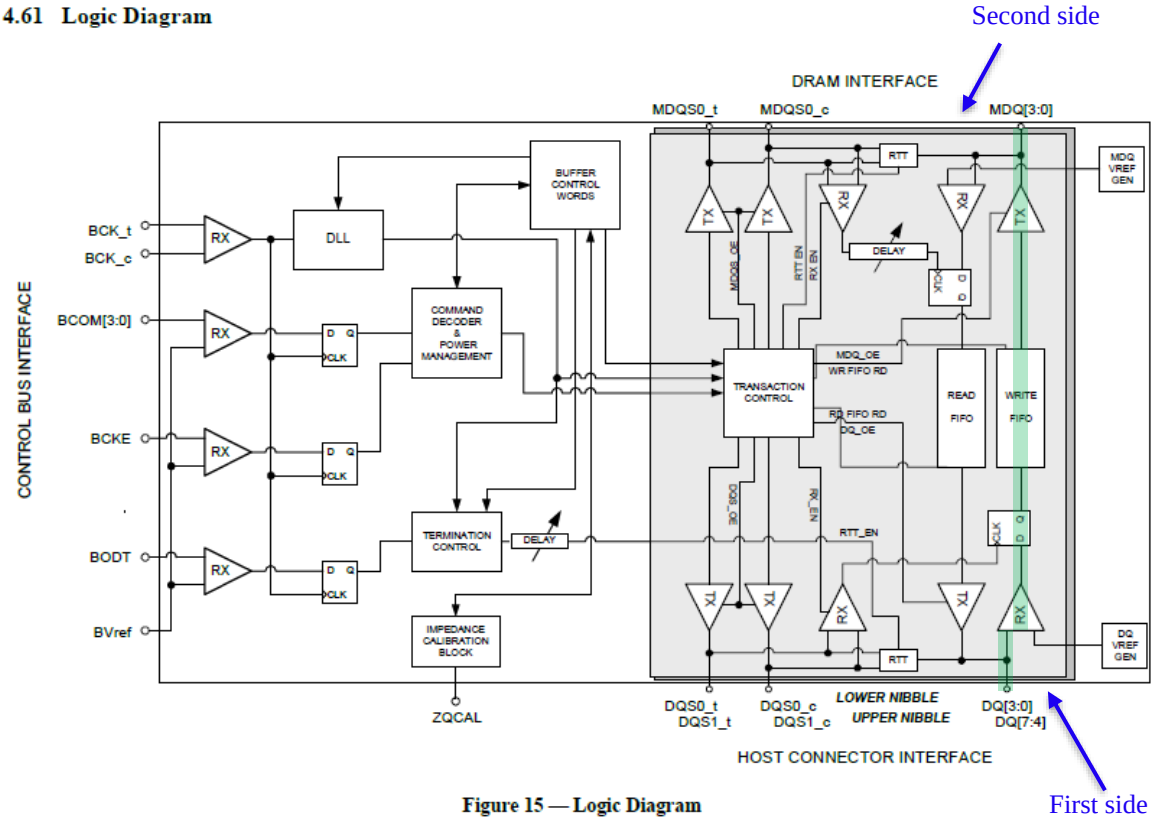


Figure 15 — Logic Diagram

Ex. 9 (JESD82-32A Standard), at 95 (showing an example of a byte-wise data path (upper nibble and lower nibble), highlighted in green, between the first side at DQ and the second side at MDQ).

88. In each of the accused DDR4 LRDIMMs, the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period. For example:

Figure 2 shows the timing sequence for a Write command.

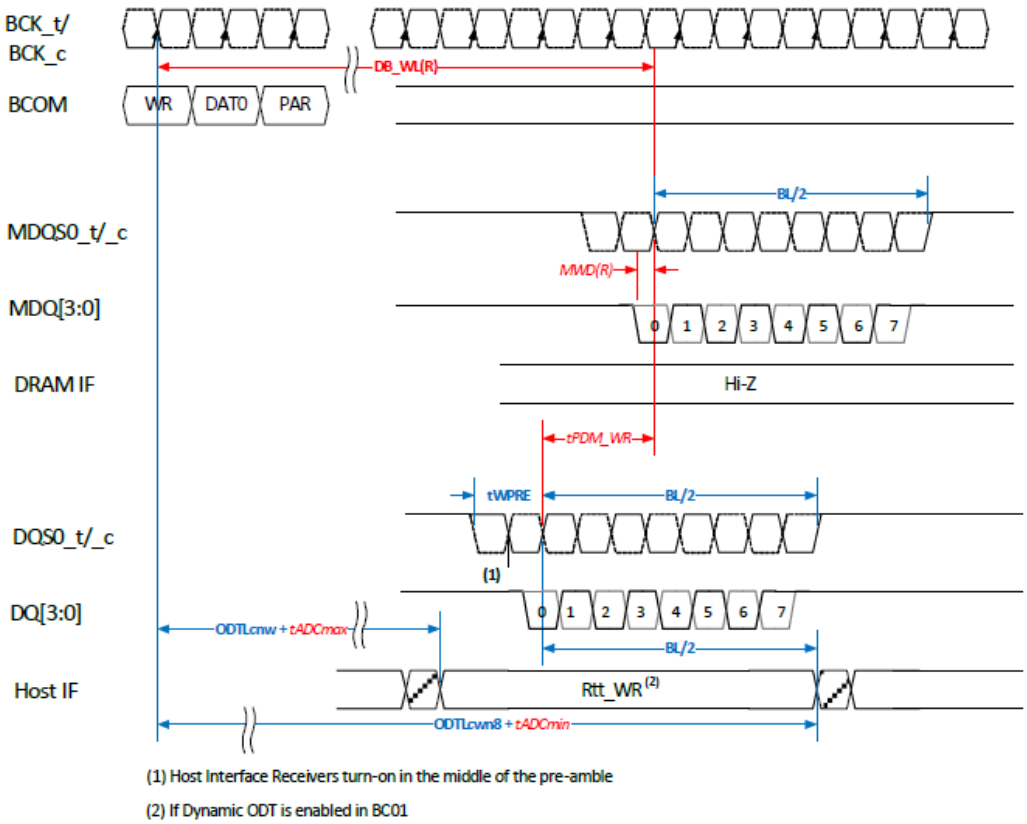


Figure 2 — WRITE Timing

Id. at 13.

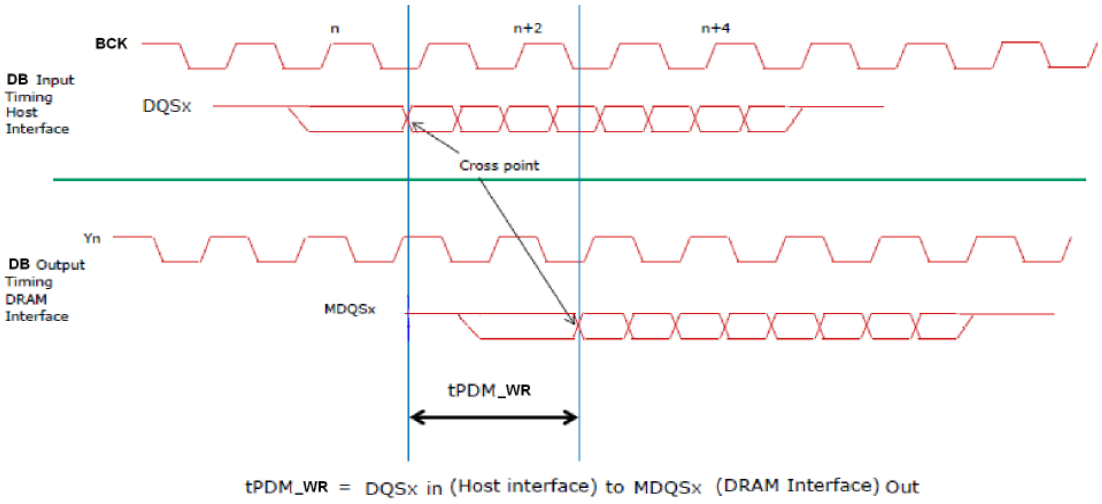


Figure 56 — tPDM_WR Latency Measurement

Id. at 165.

Table 146 — WRITE Output Timings

		DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4- 2933		DDR4-3200		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
tDVB	Data valid before MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
tDVA	Data valid after MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
Data Strobe Timing											
MDQS_t - MDQS_c differential output low time	tMQSL	0.46	-	0.46	-	0.46	-	0.46	-	tCK	1, 3
MDQS_t - MDQS_c differential output high time	tMQSH	0.46	-	0.46	-	0.46	-	0.46	-	tCK	2, 3

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

Id. at 169.

89. On information and belief, Samsung also indirectly infringes the ’339 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung’s customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the ’339 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the ’339 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

90. On information and belief, Samsung also indirectly infringes the ’339 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on

information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '339 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '339 Patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '339 Patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '339 Patent.

91. Samsung's infringement of the '339 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '339 Patent since at least August 2, 2021. Samsung's infringement of the '339 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VI. THIRD CLAIM FOR RELIEF – '918 PATENT

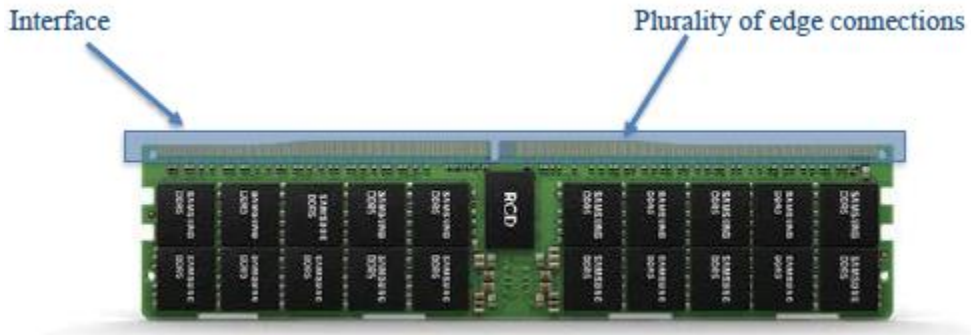
92. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

93. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '918 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products with materially the same structures in relevant parts. For example, and as

shown below, the accused DDR5 memory modules and other products with materially the same structures in relevant parts infringe at least one claim of the ’918 Patent.

94. For example, the accused DDR5 products comprise a memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system, as illustrated below.

Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).



Id. at 2 (depiction of a Samsung DDR5 RDIMM).

(Image of a Samsung DDR5 RDIMM obtained in the U.S.).

(Image of a Samsung DDR5 UDIMM obtained in the U.S.).

95. The accused DDR5 products further comprise a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; and a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude. For example, Samsung notes on its web site that its DDR5 modules include an "on-DIMM PMIC" that "further boosts power management efficiency and power supply stability." Ex. 12 at 5; *see also* Ex. 13 at 2 ("One major design improvement to the newest generation DRAM solution involves integrating the PMIC into the memory module — previous generations placed

the PMIC on the motherboard — offering increased compatibility and signal integrity, and providing a more reliable and sustained performance.”).

96. Samsung’s PMIC for DDR5 includes a high-efficiency hybrid gate driver and an asynchronous-based dual-phase buck control scheme. *Id.* The dual-phase buck control scheme “allows the DC voltage to step down from high to low with a fast transient response to changes in the output load current and adapts the conversion accordingly to efficiently regulate its output voltage at near-constant levels.” *Id.*

97. The PMIC provides the required regulated voltages, in accordance with the latest DDR5 standards. For example:

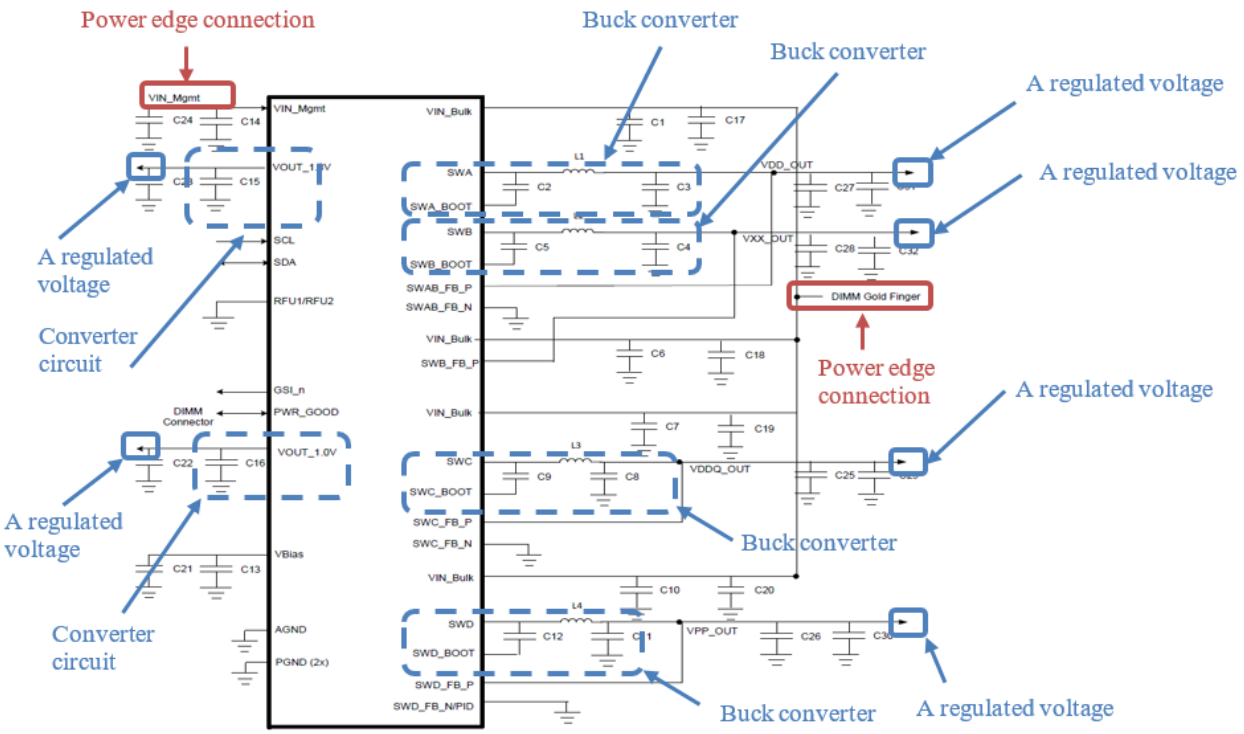


Figure 10 — Single Phase Regulator Example Schematic

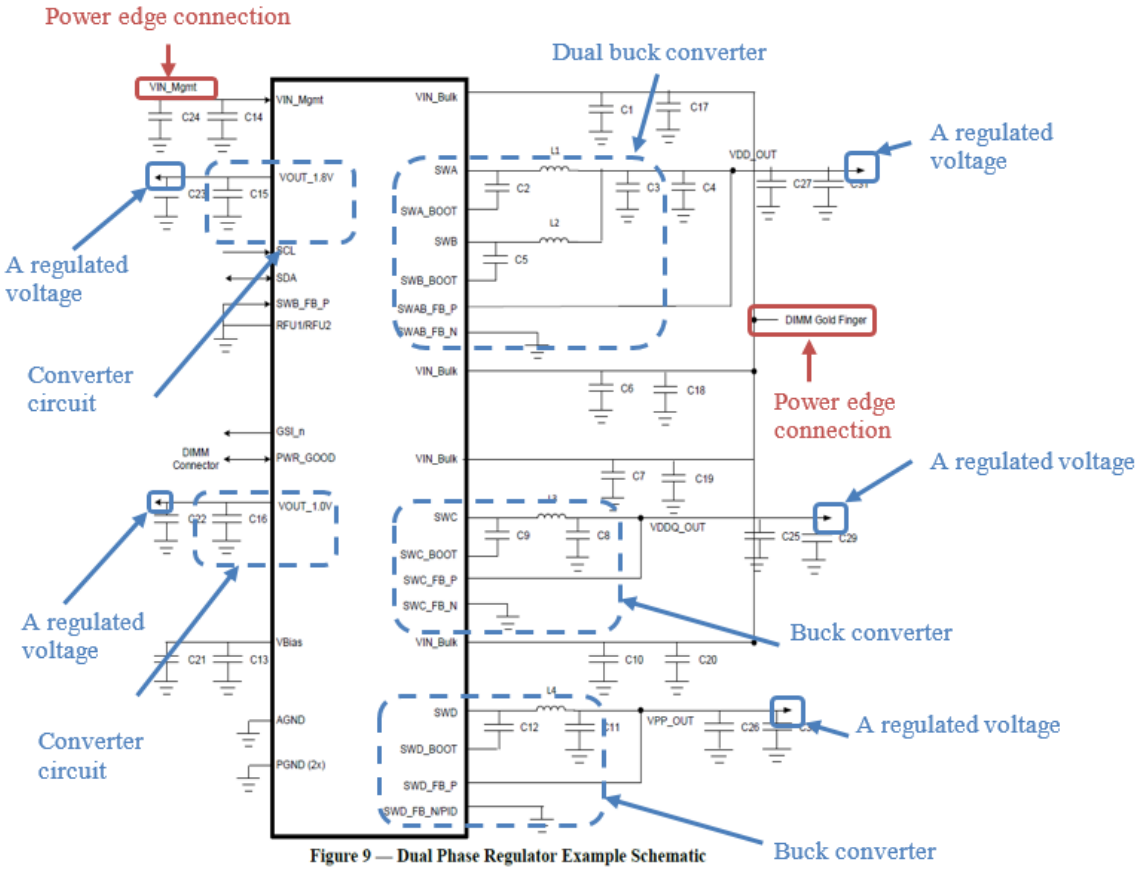
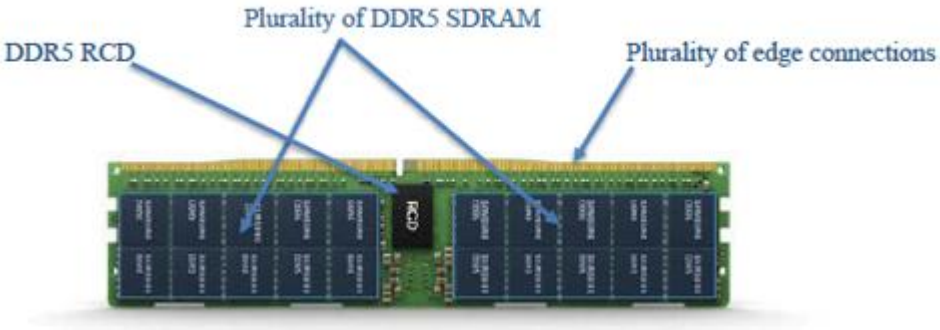


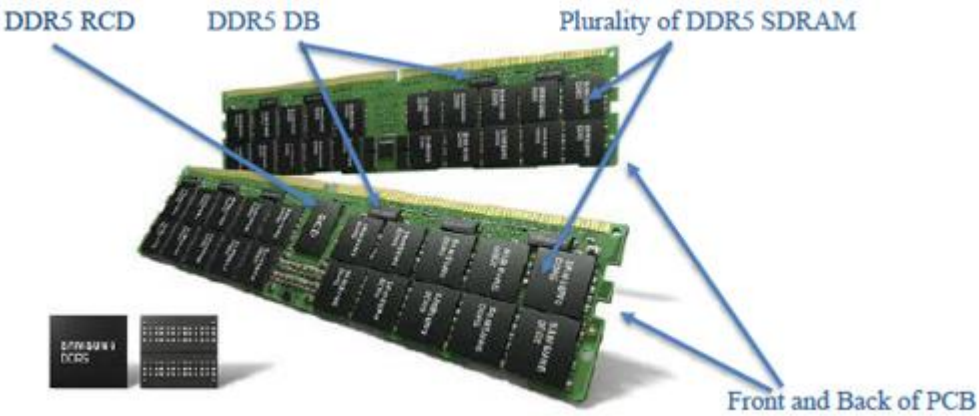
Figure 9 — Dual Phase Regulator Example Schematic

Ex. 14 (JEDEC Power Management Specification for DDR5) (annotated), at 19-20.

98. The accused DDR5 products further comprise a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit (*e.g.*, RCD) coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, as illustrated below.



Ex. 8 at 2 (depiction of a Samsung DDR5 RDIMM).



Id. at 1 (depiction of a Samsung DDR5 LRDIMM).

2.4 DDR5 SDRAM X4/8 Ballout using MO-210

Table 1 provides the ballout for DDR5 SDRAM X4/8 using MO-210.

Table 1 — DDR5 SDRAM X4/8 Ballout Using MO-210

AN	1	2	3	4	5	6	7	8	9	10	11	
AL		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD		B
C		VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS		C
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ		D
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD		E
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS		F
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		G
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		H
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ		J
K		VDD	CA6	CA2				CA3	CA7	VDD		K
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ		L
M		CAI	CA10	CA12				CA13	CA11	RESET_n		M
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	N

Ex. 15 (JEDEC 79-5 DDR5 SDRAM Standard), at 3.

Table 3 — Pinout Description (Continued)

Symbol	Type	Function
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V
ZQ	Reference	Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to V_{SS}.

Id. at 5.

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V

Ex. 16 (JEDEC DDR5 RCD Standard, JESD 82-511), at 176.

99. The at least one circuit (*e.g.*, RCD) is operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. For example:

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

Id. at 5.

100. The at least one circuit is coupled to both the second regulated voltage and the fourth regulated voltage. For example, the RCD receives both VDDIO and VDD or VDDQ input,

with the amplitude of VDDIO (*e.g.*, 1.0V) being less than the amplitude of VDD (*e.g.*, 1.1V) or VDDQ (*e.g.*, 1.1V).

Fourth regulated voltage VDDIO

Second regulated voltage VDD or VDDQ

Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	A
B	QB CA1_A	V_{SS}	QB CA9_A	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	QB CA9_B	V_{SS}	QB CA1_B	B
C	QB CA6_A	V_{SS}	QB CA8_A	V_{DD}	ZQ CAL	SCL	DERROR _IN_A_n	DERROR _IN_B_n	SDA	V_{DDIO}	V_{DD}	QB CA8_B	V_{SS}	QB CA6_B	C
D	QB CA5_A	V_{SS}	QB CA2_A	V_{DD}	V_{DD}	V_{DD}			V_{DD}	V_{DD}	V_{DD}	QB CA2_B	V_{SS}	QB CA5_B	D
E	QB CA0_A	V_{SS}	QB CA4_A	V_{DD}	QBCK _A_c	QBCK _A_t	V_{SS}	V_{SS}	QBCK _B_t	QBCK _B_c	V_{DD}	QB CA4_B	V_{SS}	QB CA0_B	E

Id. at 3.

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V

Id. at 176.

101. Testing confirms the relative amplitude. For example, voltmeters connected to VDD, VDDQ, and VDDIO (VIO) of a Samsung RDIMM recorded 1.1V, 1.1V, and 1.0V respectively.

102. On information and belief, Samsung also indirectly infringes the '918 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers

and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the ’918 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR5 products and other materially similar products that infringe the ’918 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR5 memory modules and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

103. On information and belief, Samsung also indirectly infringes the ’918 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers and end-users infringement of the ’918 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR5 memory modules and other materially similar products that infringe the ’918 Patent. On information and belief, the accused DDR5 products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR5 products and other materially similar products may be covered by one or more claims of the ’918 Patent. On information and belief, the use of the product or process that includes the accused DDR5 products and other materially similar products infringes at least one claim of the ’918 Patent.

104. Samsung’s infringement of the ’918 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the ’918 Patent since at least August 2, 2021. Samsung’s infringement of the ’918 Patent has been continuing and willful. Samsung continues

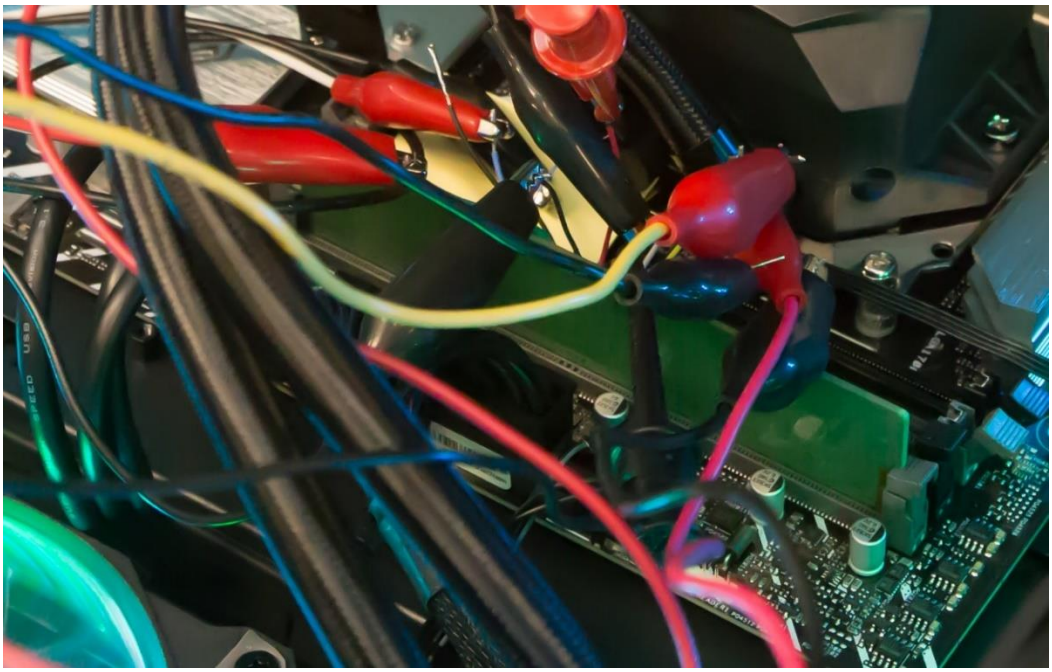
to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VII. FOURTH CLAIM FOR RELIEF – '054 PATENT

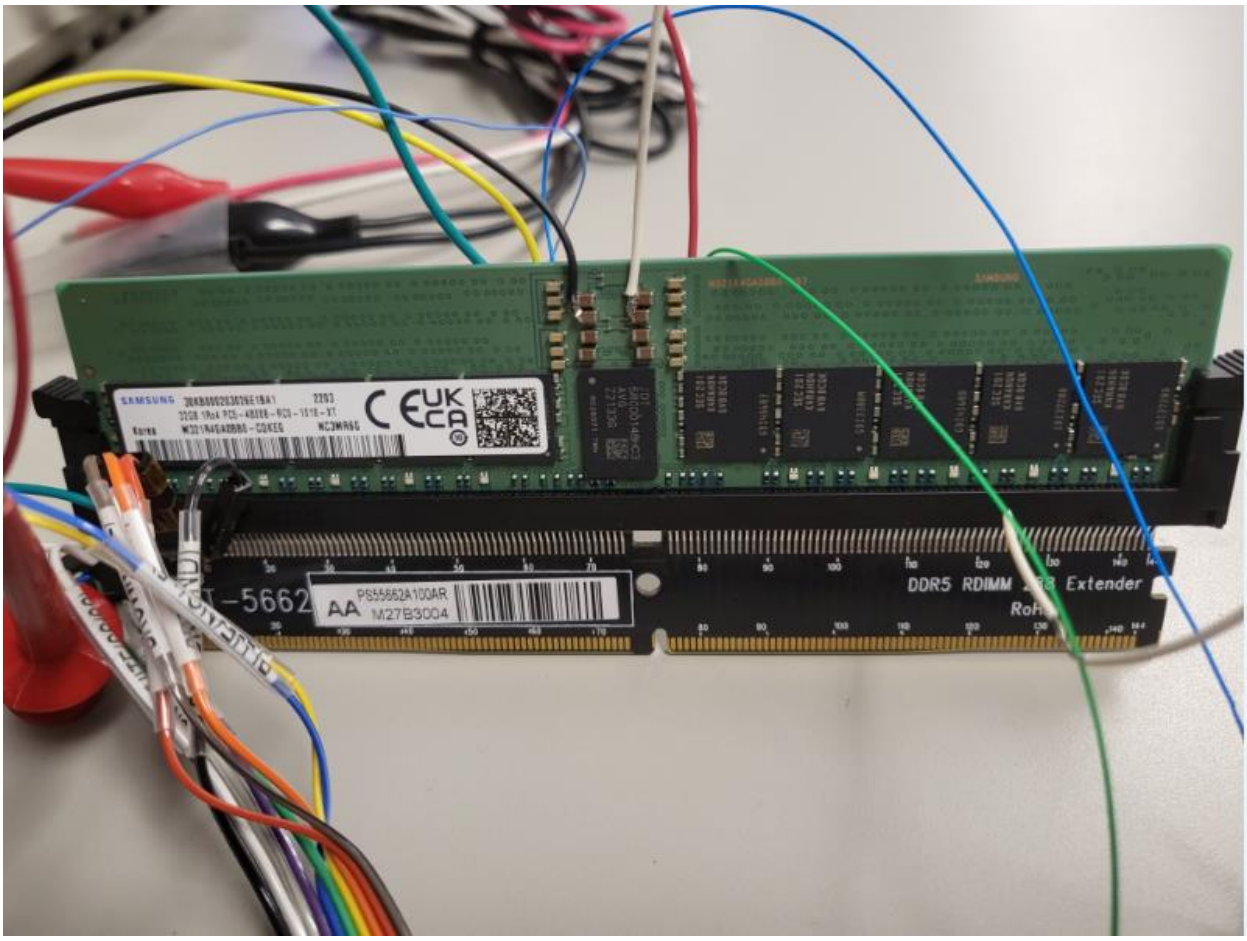
105. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

106. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '054 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR5 memory modules and other products with materially the same structures in relevant parts infringe at least one claim of the '054 Patent.

107. For example, the accused DDR5 products comprise a memory module comprising a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, as illustrated below using a representative UDIMM and RDIMM.



(Images of a Samsung DDR5 UDIMM obtained in the U.S. and inserted into a host system).

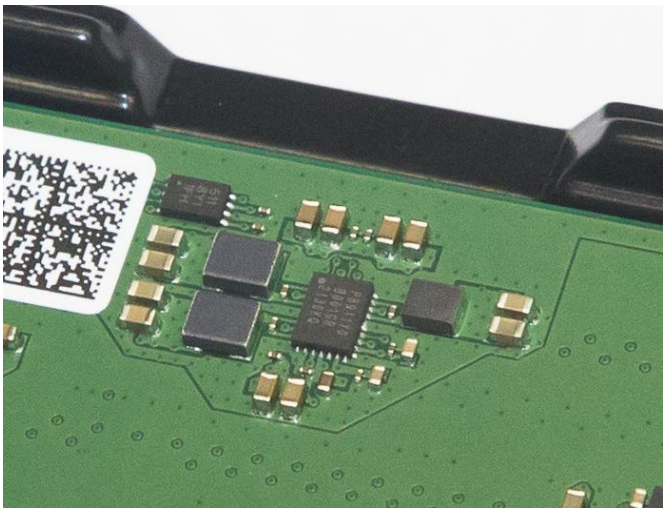


(Images of a Samsung DDR5 RDIMM obtained in the U.S. for testing).

108. The accused DDR5 products further comprise a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages. For example, Samsung notes on its website

that its DDR5 modules include an "on-DIMM PMIC" that "further boosts power management efficiency and power supply stability." Ex. 12 at 5; *see also* Ex. 13 at 2 ("One major design improvement to the newest generation DRAM solution involves integrating the PMIC into the memory module — previous generations placed the PMIC on the motherboard — offering increased compatibility and signal integrity, and providing a more reliable and sustained performance.").

109. Samsung's PMIC for DDR5 includes a high-efficiency hybrid gate driver and an asynchronous-based dual-phase buck control scheme. *Id.* The dual-phase buck control scheme "allows the DC voltage to step down from high to low with a fast transient response to changes in the output load current and adapts the conversion accordingly to efficiently regulate its output voltage at near-constant levels." *Id.* *See also, e.g.*,



(Zoomed-in view of Samsung voltage conversion and power control circuits on the above Samsung DDR5 UDIMM).

(View of Samsung voltage conversion and power control circuits on the above Samsung DDR5 RDIMM).

110. The voltage conversion circuit, which includes the relevant parts of PMIC, *e.g.*, the inductors, capacitors, and other necessary elements that comprise at least three buck converters, provides the at least three required regulated voltages. The regulated voltages include VDD, VDDQ, VPP, among others. On information and belief, the magnitude of these regulated voltages are programmable. For example, VDD and VDDQ can be programmed to have an amplitude of 1.1V. As another example, VPP can be a regulated voltage at 1.8V. DRAMs on the PCB are each coupled to the VDD, VDDQ and VPP regulated voltages. The voltage conversion circuit can also have other voltage regulators, including linear voltage regulators. Outputs from these other voltage regulators include, *e.g.*, a 1.8V output for powering components such as SPD, and where applicable, a 1.0V output for powering components such as RCD that is present in RDIMMs and

LRDIMMs. The observed voltages and behavior are consistent with the latest DDR5 standards, within error tolerance. *See supra* ¶¶ 97-100.

(Input and output voltages for a Samsung UDIMM)

(Input and output voltages for a Samsung RDIMM)

111. The accused DDR5 products further comprise a plurality of components (such as DRAM devices, thermal sensors, SPD and, where applicable, RCD and data buffers) coupled to the PCB, each component of which is coupled to at least one regulated voltage of the plurality of regulated voltages, including a plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages. *See*, *e.g.*, *supra* ¶ 98.

112. The accused DDR5 products further comprise a controller coupled to the PCB, which includes a voltage monitor circuit coupled to an input voltage, such as VIN_BULK or where applicable, VIN_MGMT, received from the host system via the interface. The controller and the voltage monitoring circuit may be part of the PMIC. In response to the voltage monitor detecting an amplitude change in the input voltage (*e.g.*, an over- or under-voltage condition on the input

power pins), the memory module transitions from a first operable state (*e.g.*, with all components operating normally) to a second operable state (*e.g.*, with the PMIC, thermal sensors, and/or SPD still operating, but not necessarily all components operating).

113. Furthermore, in response to the detected over- or under- voltage, the controller is configured to perform operations such as a write operation that records predefined bit value(s) in a register. The register is a non-volatile memory because the information written to the register by the controller is retained even after power-off.

114. On information and belief, Samsung also indirectly infringes the ’054 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung’s customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the ’054 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR5 products and other materially similar products that infringe the ’054 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR5 memory modules and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

115. On information and belief, Samsung also indirectly infringes the ’054 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers and end-users infringement of the ’054 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR5 memory modules and other materially similar products that infringe the ’054 Patent. On information and

belief, the accused DDR5 products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR5 products and other materially similar products may be covered by one or more claims of the ’054 Patent. On information and belief, the use of the product or process that includes the accused DDR5 products and other materially similar products infringes at least one claim of the ’054 Patent.

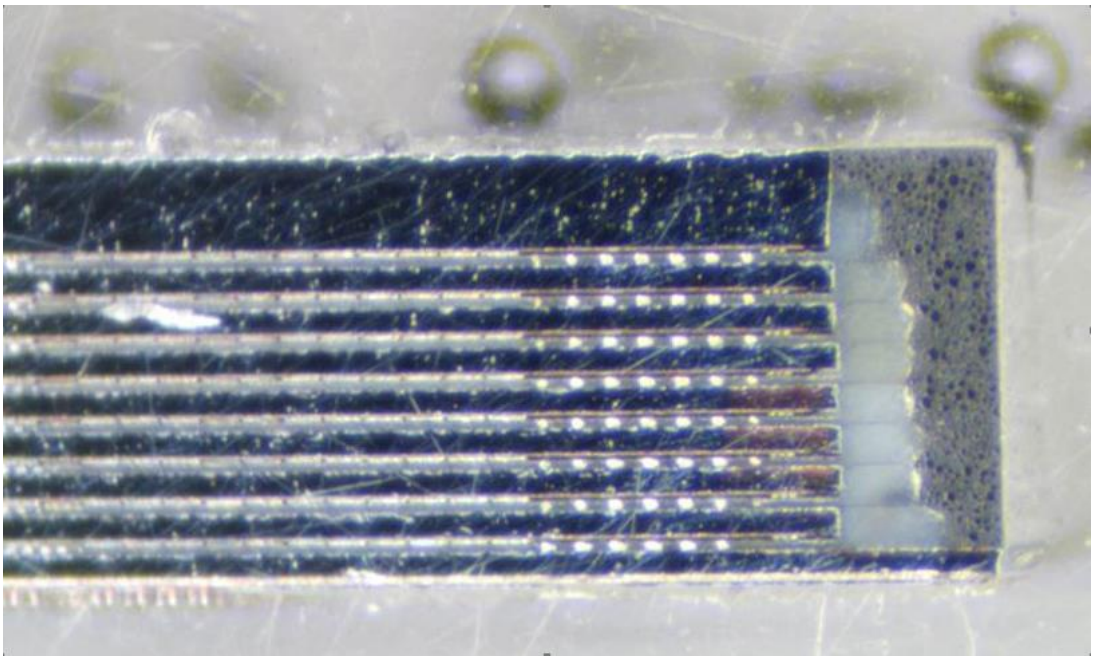
116. Samsung’s infringement of the ’054 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the ’054 Patent since at least August 2, 2021. Samsung’s infringement of the ’054 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VIII. FIFTH CLAIM FOR RELIEF – ’060 PATENT

117. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

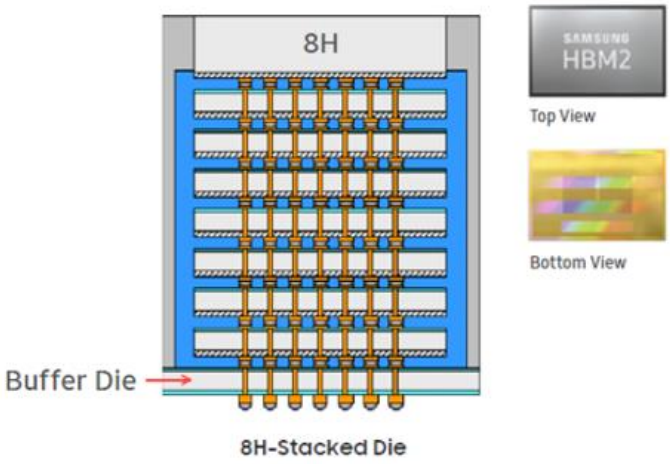
118. On information and belief, Defendants directly infringed and are currently infringing at least claim 20 of the ’060 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure and operating mechanisms in relevant part infringe at least one claim of the ’060 Patent.

119. The Accused HBM Products also each include a plurality of array dies arranged in a stack (*e.g.*, 8 stacked DRAM dies). The plurality of array dies can be divided into at least two groups of array dies. The dies are interconnected via TSVs and associated bumps and bond pads.



120. The Accused HBM Products have also at least two die interconnects. For example, some TSVs only electrically interconnect some of the DRAM dies (first group of array die(s), selected from the group of DRAM dies that Samsung annotates each individually as a "Core Die"), while others may electrically bypass this first group of array dies and electrically connect with the active transceiver logic of at least one of the other DRAM dies (second group of array die(s)).

121. The Accused HBM Products also includes a control die (*e.g.*, the bottom die in the image below, labeled by Samsung as a "Buffer Die"), with a plurality of input/output terminals, such as terminals for data and control/address signals via which the memory die stack communicates data and control/address signals with a CPU, GPU, FPGA, or other external dies. The control die also includes a first driver that drives data signal via the first die interconnects and a second driver that drives data signal via the second die interconnects.



Ex. 22 at 4 (Samsung White Paper).

122. The operation of the Accused HBM Products includes a step of receiving a data signal at a first terminal (*e.g.*, a data terminal) of the input/output terminals and a step of receiving a control signal at second terminals (*e.g.*, control/address terminals) of the input/output terminals.

123. Chip select signals, which may be encoded in the received stack ID ("SID") signals, each select an array die to which data signals are to be driven by the corresponding data driver via the corresponding die interconnects. The Accused HBM Products select one of the first driver and the second driver in accordance with the chip select signal(s) to drive the data signal to the selected array die via the corresponding first or second die interconnect.

124. On information and belief, Samsung also indirectly infringes the '060 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '060 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the Accused HBM Products and other materially similar products that infringe the '060 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the Accused HBM

Products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

125. On information and belief, Samsung also indirectly infringes the ’060 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers and end-users infringement of the ‘060 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the Accused HBM Products and other materially similar products that infringe the ’060 Patent. On information and belief, the Accused HBM Products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the Accused HBM Products and other materially similar products may be covered by one or more claims of the ’060 Patent. On information and belief, the use of the product or process that includes the Accused HBM Products and other materially similar products infringes at least one claim of the ‘060 Patent.

126. Samsung’s infringement of the ’060 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the ’060 Patent since at least August 2, 2021. Samsung’s infringement of the ’060 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

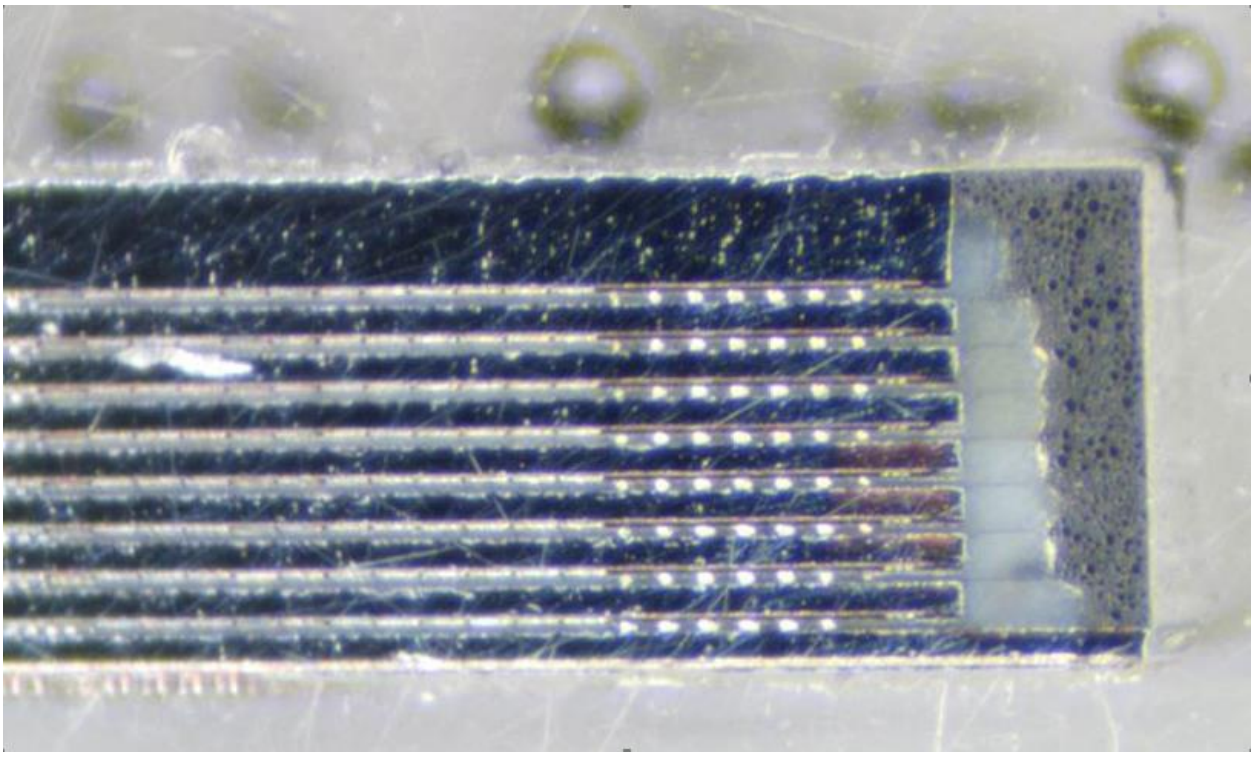
IX. SIXTH CLAIM FOR RELIEF – ’160 PATENT

127. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

128. On information and belief, Defendants directly infringed and are currently infringing at least claim 1 of the ’160 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure in relevant part infringe at least one claim of the ’160 Patent.

129. For example, the Accused HBM Products include terminals for data and terminals for control signals (*e.g.*, command and address signals).

130. The Accused HBM Products also each include stacked array dies (*e.g.*, 8 stacked DRAM dies) including at least two groups of array dies. The dies are interconnected via TSVs and associated bumps and bond pads.



131. The Accused HBM Products have also at least two interconnects, each in electrical communication with one group of array dies but not in communication with a second group of array dies. For example, first die interconnects are in electrical communication with a first group

of array dies and not in electrical communication with a second group of at least one array die; and second die interconnects are in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. This may be achieved by electrically coupling certain TSVs with active transceiver logic for only a subset of the dies. For example, some TSVs may only interconnect some of the DRAM dies (first group of array dies) and some may bypass this first group of DRAM dies and electrically connect with the active transceiver logic of at least some of the other DRAM dies (second group of array dies).

132. The Accused HBM Products also each include a control die (*e.g.*, the bottom "Buffer Die" in the image above, *supra* ¶ 121). The control die includes first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals. The data conduit includes first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies; and the second data conduit include second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die. The second driver size is different from the first driver size, for example, to account for the different distances data signals have to travel to reach the respective array dies in the stack.

133. On information and belief, Samsung also indirectly infringes the '160 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '160 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the Accused HBM Products and other materially similar products that infringe the '160 Patent. On information and belief, Samsung provides specifications, datasheets, instruction

manuals, and/or other materials that encourage and facilitate infringing use of the Accused HBM Products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

134. On information and belief, Samsung also indirectly infringes the ’160 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers and end-users infringement of the ‘160 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the Accused HBM Products and other materially similar products that infringe the ’160 Patent. On information and belief, the Accused HBM Products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the Accused HBM Products and other materially similar products may be covered by one or more claims of the ’160 Patent. On information and belief, the use of the product or process that includes the Accused HBM Products and other materially similar products infringes at least one claim of the ‘160 Patent.

135. Samsung’s infringement of the ’160 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the ’160 Patent since at least August 2, 2021. Samsung’s infringement of the ’160 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

X. DEMAND FOR JURY TRIAL

136. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

XI. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Samsung infringes the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Samsung's infringement;

C. an award of damages resulting from Samsung's acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung's infringement of the Patents-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: May 3, 2022

Respectfully submitted,

/s/ Jason Sheasby

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