UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., Defendants.	)	Civil Action No. 2:21-CV-463-JRG **JURY TRIAL DEMANDED**

JOINT CLAIM CONSTRUCTION CHART PURSUANT TO P.R. 4-5(d)

Pursuant to P.R. 4-5(d) and the Court's Docket Control Order (Dkt. 34), Plaintiff Netlist, Inc. ("Netlist") and Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively "Samsung") submit this Joint Claim Construction Chart. The exhibits to this pleading contain Netlist's and Samsung's proposed constructions for disputed terms and agreed-to terms for the patents-in-suit as follows:

- Exhibit A1: U.S. Pat. No 11,016,918 (the "'918 patent") and U.S. Pat. No 11,232,054 (the "'054 patent");
- Exhibit A2: U.S. Pat. No 8,787,060 (the "'060 patent") and U.S. Pat. No 9,318,160 (the "'160 patent");
- Exhibit A3: U.S. Pat. No 10,860,506 (the "'506 patent"); and
- Exhibit A4: U.S. Pat. No 10,949,339 (the "'339 patent").

The parties note that since the filing of the P.R. 4-3 Joint Claim Construction Statement (Dkt. 70), Samsung has agreed to withdraw claim 7 of the ’060 patent from construction.

Dated: September 30, 2022

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that, on September 30, 2022 a copy of the foregoing was served to all counsel of record.

/s/ Sam Baxter
Sam Baxter

Exhibit A

Exhibit A1: Proposed Constructions for the ’918 and ’054 Patents

Exhibit A2: Proposed Constructions for the ’060 and ’160 Patents

Exhibit A3: Proposed Constructions for the ’506 Patent

Exhibit A4: Proposed Constructions for the ’339 Patent

Exhibit A1: Proposed Constructions for the '918 and '054 Patents[1]

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**first**" / "**second**" / "**third**" / "**fourth**" "**regulated voltages**" '918: all claims	Plain and ordinary meaning (that is, first, second, third and fourth voltages that are adjusted, within tolerance, to a particular voltage level)[2]	"first regulated voltage that is distinct from the second, third, and fourth regulated voltages" / "second regulated voltage that is distinct from the first, third, and fourth regulated voltages" / "third regulated voltage that is distinct from the first, second, and fourth regulated voltages" / "fourth regulated voltage that is distinct from the first, second, and third regulated voltages"	
"**first**" / "**second**" / "**third**" / "**fourth**" "**voltage amplitude**" '918: all claims	Plain and ordinary meaning (that is, first/ second/ third/ fourth amplitude of voltage which need not all be different)	"first voltage amplitude that is distinct from the second, third, and fourth voltage amplitudes" / "second voltage amplitude that is distinct from the first, third, and fourth voltage amplitudes" / "third voltage amplitude that is distinct from the first, second, and fourth voltage amplitude" / "fourth voltage amplitude that is distinct from the first, second, and third voltage amplitude"	

[1] Phrases in square brackets provide context and require no construction.

[2] Netlist does not believe the term "regulated voltage" needs to be construed; but if necessary, Netlist proposes construing it as a "voltage that is maintained, within tolerance, at a particular voltage level."

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**at least three regulated voltages**" '054: claims 1-15	Plain and ordinary meaning (that is, three or more regulated voltages)	"at least three distinct regulated voltages"	
"**plurality of regulated voltages**" '054: claims 16, 24	Plain and ordinary meaning (that is, multiple regulated voltages)	"plurality of distinct regulated voltages"	
"**a second plurality of address and control signals**" '918: claims 1-3, 5-7, 9-13, 15, 21	Plain and ordinary meaning (that is, a second set of address and control signals)	"a second plurality of address and control signals that are distinct from a first plurality of address and control signals"	
"**dual buck converter**" / "**dual-buck converter**" '918: claims 2, 17, 28 '054: claim 15	Plain and ordinary meaning (that is, a buck converter with two regulated voltage outputs whose amplitude may be the same or different)	"buck converter with two outputs outputting two distinct regulated voltages"	
"**pre-regulated input voltage**" '918: claims 16, 22, 30	Plain and ordinary meaning (that is,	"regulated voltage generated on the memory module from an input voltage"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
	modulated input voltage)[3]		
"A **memory module**" '918 and '054: all claims	The preamble is limiting	The preamble is non-limiting	
"**operable state**" '054: claims 4-7, 11-12, 16-17, 23, 25-26	[Agreed]	[Agreed]	"state in which the memory module is operated"
"**first operable state**" '054: claims 4-7, 11-12, 16-17, 23, 25-26	[Agreed]	[Agreed]	"state in which the memory module is operated before transition"
"**second operable state**" '054: claims 4-7, 11-12, 16-17, 23, 25-26	[Agreed]	[Agreed]	"state in which the memory module is operated after transition"

[3] Netlist believes that the term "input voltage" in "pre-regulated input voltage," if construed, should receive its plain and ordinary meaning: voltage that is provided to the earlier mentioned converters or converter circuit.

Exhibit A2: Proposed Constructions for the ’060 and ’160 Patents

Term (Patent/Claim)	Netlist’s Proposed Construction	Samsung’s Proposed Construction	Court’s Construction
“**array die**” ’060 and ’160: all asserted claims	Plain and ordinary meaning (that is, a die including memory cells)	“array die that is different from a DRAM circuit”	
“**chip select signal**” ’060: claims 11-14, 16-19, 20, 21, 23-28	“signal for enabling or selecting one or more array dies for data transfer”	Plain and ordinary meaning	
“**chip select conduits**” ’060: claims 6, 11-14, 16-19	“conduits for transmitting” “chip select signals,” as construed above	Plain and ordinary meaning	
“**A memory package**” ’060 and ’160: all asserted claims	[Agreed]	[Agreed]	The preamble is limiting.

Exhibit A3: Proposed Constructions for the '506 Patent

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"[the method further comprising,] **before receiving the input C/A signals corresponding to the memory read operation, determining the first predetermined amount based at least on signals received by the first data buffer**" '506: claim 14	the step of determining the first predetermined amount based at least on signals received by the first data buffer occurs before the earlier recited step of "receiving, at the module device, input C/A signals corresponding to a memory read operation via the C/A signal lines."	"during one or more previous memory operations"[4]	
"**one or more previous operations**" '506: claims 1-3, 11, 15, 16	[Agreed][5]	[Agreed]	"one or more previous memory operations"

[4] Samsung does not believe that the additional phrase "determining the first predetermined amount based at least on signals received by the first data buffer," which Netlist has added to this term, needs to be construed. If Netlist insists on including this phrase in the term being construed, the construction of the combined term should be: "determining the first predetermined amount based at least on signals received by the first data buffer during one or more previous memory operations."

[5] Note: Netlist's proposed construction is not intended to limit the recited "operations" to ones involving writing to or reading from a DRAM. Dkt. 73 at 46. Samsung believes that "one or more previous memory operations" should be given its plain and ordinary meaning. Dkt. 70-2 at 23 n.1.

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising**" '506: claim 1	[Agreed]	[Agreed]	The preamble is limiting.

Exhibit A4: Proposed Constructions for the '339 Patent

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**time period in accordance with a latency parameter**" '339: claims 1, 11, 34, 35	"a time period wherein both the start of the time period and duration of the time period depends on at least a latency parameter"	Plain and ordinary meaning	
"**each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period**"[6] '339: claim 1	"time period in accordance with a latency parameter" as construed above. The remaining term requires no additional construction at this time (i.e., plain and ordinary meaning).	"each respective byte-wise buffer further includes logic configurable to, in response to the module control signals, activate the byte-wise data path connected to a first DDR DRAM device (in a first N-bit-wide rank), and disable the byte-wise data path connected to a second DDR DRAM device (in a second N-bit-wide rank), to cause a respective byte-wise section of the N-bit wide write data associated with the memory operation to be sent from the first side to the first DDR DRAM device along the activated byte-wise data path and not sent to the second DDR DRAM device along the disabled byte-wise data path during the first time period in accordance with a latency parameter"	

[6] This clause combines two of Samsung's identified terms, per its suggestion. Dkt. 70-2 at 32 n.3.

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period**" '339: claim 1	No construction is necessary (i.e., plain and ordinary meaning).	"logic in response to the module control signals is configured to enable the first tristate buffers to activate the byte-wise data path connected to a first DDR DRAM device (in a first N-bit-wide rank) and disable the byte-wise data path connected to a second DDR DRAM device (in a second N-bit-wide rank), to cause the respective byte-wise section of the N-bit wide write data to be sent from the first side to the module data lines coupled to the first DDR DRAM device along the activated byte-wise data path and not sent to the module data lines coupled to the second DDR DRAM device along the disabled byte-wise data path during the first time period"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**each respective data transmission circuit is configurable to enable the data paths for a first <u>time period in accordance with a latency parameter</u> to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period**" '339: claim 11	"<u>time period in accordance with a latency parameter</u>" as construed above. The remaining term requires no additional construction at this time (i.e., plain and ordinary meaning).	"each respective data transmission circuit is configurable to, during the first time period in accordance with a latency parameter, activate the data paths connected to a first respective pair of DDR DRAM devices (in a first N-bit-wide rank), and disable the data paths connected to another respective pair of DDR DRAM devices (in another N-bit-wide rank), to cause a respective section of the N-bit wide write data associated with the memory operation to be sent from the first side to the first respective pair of DDR DRAM devices along the activated data paths and not sent to the other respective pair of DDR DRAM devices along the disabled data paths"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, and to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks**" '339: claim 11	No construction is necessary (i.e., plain and ordinary meaning).	"the respective data transmission circuit, in response to the module control signals, is configured to enable a first subset and a second subset of the first tristate buffers to activate the data paths connected to a first respective pair of DDR DRAM devices (in a first N-bit-wide rank), and disable the data paths connected to another respective pair of DDR DRAM devices (in another N-bit-wide rank), to cause the first subsection of the respective section of the N-bit wide write data to be sent from the first side to a first subset of the respective module data lines coupled to a first one of the first respective pair of DDR DRAM devices along one of the activated data paths, and a second subsection of the respective section of the N-bit wide write data to be sent to a second subset of the respective module data lines coupled to a second one of the first respective pair of DDR DRAM devices along another one of the activated data paths, and the respective section of the N-bit wide write data to not be sent to the other respective pair of DDR DRAM devices along the disabled data paths"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period**" '339: claim 19	No construction is necessary (i.e., plain and ordinary meaning).	"each respective buffer further includes logic configurable to, during a first time period, activate the data path connected to a first DDR DRAM device (in a first N-bit-wide rank), and disable the data path connected to a second DDR DRAM device (in a second N-bit-wide rank), to cause a respective section of the first N-bit wide data associated with the first memory operation to be sent from the first DDR DRAM device to the first side along the activated data path and not sent from the second DDR DRAM device along the disabled data path, and further configurable to, during a second time period subsequent to the first time period, activate the data path connected to the second DDR DRAM device and disable the data path connected to the first DDR DRAM device, to cause a respective section of the second N-bit wide data associated with the second memory operation to be sent from the second DDR DRAM device to the first side along the activated data path and not sent from the first DDR DRAM device along the disabled data path"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**each respective n-bit-wide data buffer includes** … **a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, . . . a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers**" '339: claim 27	No construction is necessary (i.e., plain and ordinary meaning)	"each respective n-bit-wide data buffer includes logic configurable to enable a first set of tristate buffers to activate a data path connected to one DDR DRAM device (in a rank), and disable a data path connected to a different DDR DRAM device (in a different rank), to cause the respective n-bit section of the write data to be sent from the data signal lines to the module data lines coupled to the DDR DRAM device along the activated data path and not sent to the different DDR DRAM device along the disabled data path, and further configurable to enable a second set of tristate buffers to activate a data path connected to a DDR DRAM device (in a rank), and disable a data path connected to a different DDR DRAM device (in a different rank), to cause the respective n-bit section of the read data to be sent to the data signal lines from the module data lines coupled to the DDR DRAM device along the activated data path and not sent from the different DDR DRAM device along the disabled data path"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**a module controller** … **configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N- bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals**" '339: claim 1	No construction is necessary (i.e., plain and ordinary meaning)	"a control circuit configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks and corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and in response to receiving the input address and control signals, to output registered address and control signals corresponding to the number of physical ranks of memory devices on the module, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**a module controller** … **configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N- bit-wide rank among the multiple N-bit-wide ranks, and to output registered address and control signals in response to the input address and control signal, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals**" '339: claim 11	No construction is necessary (i.e., plain and ordinary meaning)	"a control circuit configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank among the multiple N-bit-wide ranks and corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and in response to the input address and control signals, to output registered address and control signals corresponding to the number of physical ranks of memory devices on the module, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**a module controller** … **configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit- wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals, wherein the first**	No construction is necessary (i.e., plain and ordinary meaning)	"a control circuit configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks and corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and in response to receiving the first address and control signals, to output first registered address and control signals for the first memory operation corresponding to the number of physical ranks of memory devices on the module, and in response to receiving the second address and control signals, to output second registered address and control signals for the second memory operation	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N- bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals" '339: claim 19		corresponding to the number of physical ranks of memory devices on the module, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**a module controller** … **configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals**" '339: claim 27	No construction is necessary (i.e., plain and ordinary meaning)	"a control circuit configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and to subsequently receive second address and control signals for a memory read operation corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and in response to the first address and control signals, to output for the memory write operation first module control signals and first registered address and control signals corresponding to the number of physical ranks of memory devices on the module, and in response to the second address and control signals, to output for the memory read operation second module control signals and second registered address and control signals corresponding to the number of physical ranks of memory devices on the module"	

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**N-bit wide write data**" '339: claims 1-3, 11, 14	[Agreed]	[Agreed]	"write data that is N bits in width"
"**A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising**" '339: claim 1	[Agreed]	[Agreed]	The preamble is limiting.

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising**" '339: claims 11, 19	[Agreed]	[Agreed]	The preamble is limiting.

Term (Patent/Claim)	Netlist's Proposed Construction	Samsung's Proposed Construction	Court's Construction
"**A memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and data signal lines, the data signal lines including a plurality of sets of data signal lines, each set of data signal lines is n bit wide, the memory module comprising**" '339: claim 27	[Agreed]	[Agreed]	The preamble is limiting.