

UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR § 1.53(b))</i>		Attorney Docket No. 129980-5049-US01	
		First Inventor	Hyun Lee
		Title	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
		Electronically filed	April 22, 2019
APPLICATION ELEMENTS <i>See MPEP Chapter 600 concerning utility patent application contents.</i>		Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	
1. ☐ Fee Transmittal Form <i>(with duplicate for fee processing)</i> 2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27 3. ☒ Specification [Total Pages 32] 4. ☒ Drawing(s) (35 USC § 113) [Total Sheets 26] 5. ☒ Oath or Declaration [Total Pages 2] a. ☐ Newly executed <i>(original or copy)</i> b. ☒ Copy from a prior application (37 CFR § 1.63(d)) 6. ☒ Application Data Sheet, see 37 C.F.R. § 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program <i>(Appendix)</i> ☐ Landscape Table on CD 8. ☐ Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statement verifying identity of above copies		ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers <i>(cover sheet & document(s))</i> Name of Assignee: 10. ☒ 37 CFR § 3.73(c) Statement a. ☒ Power of Attorney 11. ☐ English Translation Document <i>(if applicable)</i> 12. ☐ Information Disclosure Statement and PTO-1449 a. ☐ Copies of citations attached 13. ☐ Preliminary Amendment 14. ☐ Return Receipt Postcard <i>(MPEP 503)</i> 15. ☐ Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> 16. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i) 17. ☐ Other:	
Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 MUST be included in an Application Data Sheet (ADS). (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).			
19. CORRESPONDENCE ADDRESS: Customer Number 79141			
Signature	/Jamie J. Zheng/	Date	April 22, 2019
Name (Print/Type)	Jamie J. Zheng	Registration No. (Attorney/Agent)	51,167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	To be assigned
Serial No.:	To be assigned	Art Unit	To be assigned
Filed:	Filed herewith	Examiner:	To be assigned
For:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING	Attorney Docket No.:	129980-5049-US01

STATEMENT UNDER 37 C.F.R. § 3.73(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Netlist, Inc., a corporation, states that it is the assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventor(s) of the parent of the patent application/patent identified above.

The assignment was recorded in the United States Patent and Trademark Office on November 21, 2017 at Reel 044194, Frame 0965, or for which a copy thereof is attached.

The undersigned is authorized to act on behalf of the assignee.

Date: April 22, 2019

/Jamie J. Zheng/	51,167
Jamie J. Zheng	(Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP	
1400 Page Mill Road	
Palo Alto, CA 94304	
(650) 843-4000	

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number
:

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

- ☐ Inventor or Joint Inventor
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature

Date: January 9, 2013

Name

Gail Sasaki

Title

Vice President and Chief Financial Officer

Company

Netlist, Inc.

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature

Total of ___ forms are submitted.

**COMBINED DECLARATION AND ASSIGNMENT
FOR UTILITY OR DESIGN APPLICATION**

**Title of
Invention**

MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

DECLARATION

As a below named inventor, I hereby declare that:

This declaration
is directed to:

☐

The attached application, or

☒

United States application or PCT international application
number 13/952,599 filed on July 27, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) and other good and valuable consideration paid, I hereby sell and assign to

Netlist, Inc.

(Name of Assignee)

of 51 Discovery, Suite #150, Irvine, CA 92618

(Address of Assignee)

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

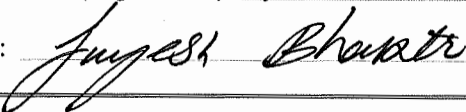
I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: 

Date: 10/9/2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: 

Date: 10/14/2013

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor	1				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Hyun		Lee		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Ladera Ranch	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	175 Technology, Suite 150				
Address 2					
City	Irvine	State/Province	CA		
Postal Code	92618	Country	US		

Inventor	2				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jayesh	R.	Bhakta		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	175 Technology, Suite 150				
Address 2					
City	Irvine	State/Province	CA		
Postal Code	92618	Country	US		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

Micron Technology Inc. et al.

Ex. 1052, p. 6

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

☐ An Address is being provided for the correspondence information of this application.

Customer Number	79141		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		
Attorney Docket Number	129980-5049-US01	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	26	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	15/820076	2017-11-21		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/820076	Continuation of	15/426064	2017-02-07	9824035	2017-11-21
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/426064	Continuation of	14/846993	2015-09-07	9563587	2017-02-07
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/846993	Continuation of	13/952599	2013-07-27	9128632	2015-09-08
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
13/952599	Claims benefit of provisional	61/676883	2012-07-27		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					
Add					

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
		Micron Technology Inc. et al.	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant	1	Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear		
☒ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
Name of the Deceased or Legally Incapacitated Inventor:		
If the Applicant is an Organization check here. ☒		
Organization Name	Netlist, Inc.	
Mailing Address Information For Applicant:		
Address 1	175 Technology, Suite 150	
Address 2		
City	Irvine	State/Province CA
Country	US	Postal Code 92618
Phone Number		Fax Number
Email Address		
Additional Applicant Data may be generated within this form by selecting the Add button. Add		

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

Assignee	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				Remove
If the Assignee or Non-Applicant Assignee is an Organization check here.				☐
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				Add

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jamie J. Zheng/		Date (YYYY-MM-DD)	2019-04-22
First Name	Jamie J.	Last Name	Zheng	Registration Number
				51167
Additional Signature may be generated within this form by selecting the Add button.				Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	129980-5049-US01
		Application Number	
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- 1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
- 2 A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
- 3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
- 4 A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
- 5 A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
- 6 A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7 A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
- 8 A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
- 9 A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

CLAIM OF PRIORITY

[0001] The present application is a continuation of U.S. Pat. App. No. 15/820,076, filed November 21, 2017, which is a continuation of U.S. Pat. App. No. 15/426,064, filed February 7, 2017 (U.S. Pat. No. 9,824,035), which is a continuation of U.S. Pat. App. No. 14/846,993, filed September 7, 2015 (U.S. Pat. No. 9,563,587), which is a continuation of U.S. Pat. App. No. 13/952,599, filed July 27, 2013, (U.S. Pat. No. 9,128,632), which claims priority to U.S. Provisional Pat. Appl. No. 61/676,883, filed on July 27, 2012. Each of the above applications is incorporated herein by reference in its entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] The present application is related to commonly-owned U.S. Pat. App. No. 14/715,486, filed on May 18, 2015; U.S. Pat. App. No. 13/970,606, filed on August 20, 2013, now U.S. Pat. No. 9,606,907; U.S. Pat. App. No. 12/504,131, filed on July 16, 2009, now U.S. Pat. No. 8,417,870; U.S. Pat. App. No. 12/761,179, filed on April 15, 2010, now U.S. Pat. No. 8,516,185; U.S. Pat. App. No. 13/287,042, filed on November 1, 2011, now U.S. Pat. No. 8,756,364; and U.S. Pat. App. No. 13/287,081, filed on November 1, 2011, now U.S. Pat. No. 8,516,188; each of which is incorporated herein by reference in its entirety.

FIELD

[0003] The disclosure herein is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

BACKGROUND

[0004] With recent advancement of information technology and widespread use of the

Internet to store and process information, more and more demands are placed on the acquisition, processing, storage and dissemination of vocal, pictorial, textual and numerical information by microelectronics-based combination of computing and communication means. In a typical computer or server system, memory modules are used to store data or information. A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB). A processor or a memory controller accesses the memory module via a memory bus, which, for a single-in-line memory module (SIMM), can have a 32-bit wide data path, or for a dual-in-line memory module (DIMM), can have a 64-bit wide data path.

[0005] The memory devices of a memory module are generally organized in ranks, with each rank of memory devices generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" or "by 72" organization.

[0006] The memory capacity or memory density of a memory module increases with the number of memory devices on the memory module. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.

[0007] In certain conventional memory modules, the ranks are selected or activated by control signals from a processor or memory controller during operation. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density of the memory modules that can be used in these computer and server systems.

[0008] For memory devices in such as a memory module to be properly accessed,

distribution of control signals and a control clock signal in the memory module is subject to strict constraints. In some conventional memory modules, control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules. The balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections.

[0009] In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a diagram illustrating a memory system including at least one memory module according to one embodiment.

[0011] FIGS. 2A-2D are each a diagrams illustrating interactions among components in a memory module according to certain embodiments.

[0012] FIG. 3 is a diagram illustrating one of a plurality of data buffers in a memory module according to one embodiment.

[0013] FIGS. 4A-4B are each a diagram illustrating data and data strobe signal lines coupled to memory devices in a memory module according to certain embodiments.

[0014] FIGS. 5A-5B are diagrams illustrating different numbers of memory devices that can be coupled to each data buffer in a memory module according to certain embodiments.

[0015] FIG. 6 is a diagram illustrating a control circuit in a data buffer according to

certain embodiments.

[0016] FIG. 7 is a diagram illustrating control signals from a module control device to a plurality of data buffers in a memory module according to certain embodiments.

[0017] FIG. 8 is a timing diagram illustrating alignment of module control signals with respect to module clock signals.

[0018] FIG. 9 is a diagram illustrating a metastability detection circuit and signal adjustment circuit in a data buffer according to certain embodiments.

[0019] FIGS. 10A-10C are diagrams illustrating a metastability detection circuit according to certain embodiments.

[0020] FIGS. 10D is a diagram illustrating a signal adjustment circuit according to certain embodiments.

[0021] FIGS. 11A-11B are diagrams illustrating a metastability detection circuit and signal adjustment circuit, respectively, according to certain embodiments.

[0022] FIGS. 12A-12B are a timing diagrams illustrating a write operation and a read operation, respectively, performed by a memory module according to one embodiment.

[0023] FIG. 13 is a diagram illustrating a delay control circuit in a data buffer according to certain embodiments.

[0024] FIG. 14 is a diagram illustrating a DQ or DQS routing circuit in a data buffer according to an embodiment.

[0025] FIG. 15 a diagram illustrating a DQS routing circuit having a delay circuit in a data buffer according to an embodiment.

[0026] FIG. 16 a diagram illustrating a DQ routing circuit having a delay circuit in a data buffer according to an embodiment.

[0027] FIG. 17 is a diagram illustrating a delay circuit in a DQ or DQS routing circuit according to an embodiment.

[0028] FIG. 18 is a flowchart illustrating a method for data edge alignment according to embodiments.

[0029] FIG. 19 is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

DESCRIPTION OF EMBODIMENTS

[0030] A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines.

[0031] The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective

groups of memory devices. Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock. Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller. Thus, the memory controller does not have direct control of the memory devices. In one embodiment, each group of memory devices include at least two subgroups, each subgroup including at least one memory device. Each buffer circuit is configured to select a subgroup in the respective group of memory devices to communicate data with the memory controller in response to the module control signals. Thus, the memory module can have more ranks of memory devices than what is supported by the memory controller.

[0032] In one embodiment, each buffer circuit includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or a module clock signal to mitigate any metastability condition in the module control signals.

[0033] Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

[0034] FIG. 1 shows a system 100 including a memory controller (MCH) 101 and one or more memory modules 110 coupled to the MCH by a memory bus 105, according to one embodiment. As shown, the memory bus includes C/A signal lines 120 and groups of system data/strobe signal lines 130. Also as shown, each memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114. Each memory module 110 further includes a module control circuit (module controller or module control

device) 116 coupled to the MCH 101 via the C/A signal lines 120, and a plurality of buffer circuits or isolation devices 118 coupled to the MCH 101 via respective groups of system data/strobe signal lines 130. In one embodiment, the memory devices 112, the module control circuit 116 and the isolation devices 118 can be mounted on a same side or different sides of a printed circuit board (module board) 119.

[0035] In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module 110 may vary. For example, as shown, each memory module 110 may include four ranks of memory devices 112. In another embodiment, the memory module 110 may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices 112.

[0036] In the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices 112. Additionally, in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller. For example, in various embodiments, the memory bus 105 may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.

[0037] Furthermore, the memory devices 112 may include any type of memory devices. For example, in one embodiment, the memory devices 112 may include dynamic random access memory (DRAM) devices. Additionally, in one embodiment, each memory module 110 may include a dual in-line memory module (DIMM).

[0038] Referring to FIG. 2A, which illustrates one memory module 110 according to an embodiment, the module control device 116 receives system memory commands represented by a set of system control/address (C/A) signals from the MCH 101 via signal

lines 120 and generates module command signals and module control signals based on memory commands from the system. The module control device 116 also received a system clock MCK and generates a module clock signal CK in response to the system clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and $\overline{\text{MCK}}$, and the module clock signal may include a pair of complementary clock signals CK and $\overline{\text{CK}}$.

[0039] Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strobe (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals, which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK.

[0040] Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.

[0041] Examples of module control signals include, but are not limited to a mode signal

(MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices 118 via respective module control signal lines 230. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices 118 via the module control signal lines and decoded/processed at the isolation devices.

[0042] Module control device 116 transmits the module command signals to the memory devices 112 via module C/A signal lines 220. The memory devices 112 operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller. The module control device transmits the module control signals together with the module clock signal CK to the isolation devices 118 via module control signal lines 230. As shown in FIG. 2, at least some of the memory devices in a same rank share a same set of module C/A signal lines 220, and at least some of the isolation devices 118 share a same set of module control signal lines 230.

[0043] As shown in FIGS. 2A and 2B, each rank 114 includes N memory devices, where N is an integer larger than one. For example, a first rank includes memory devices M_{11} , ..., M_{i1} , $M_{i+1,1}$, ..., M_N , a second rank includes memory devices M_{12} , ..., M_{i2} , $M_{i+1,2}$, ..., $M_{N,2}$, and so on. In one embodiment, the memory devices 112 are also organized in groups or sets, with each group corresponding to a respective group of system data/strobe signal lines 130 and including at least one memory device from each rank. For example, memory devices M_{11} , M_{12} , M_{13} , and M_{14} form a first group of memory devices, memory devices M_{i1} , M_{i2} , M_{i3} , and M_{i4} form an i^{th} group of memory devices, and so on.

[0044] As shown, the isolation devices 118 are associated with respective groups of memory devices and are coupled between respective groups of system data/strobe signal lines 130 and the respective groups of memory devices. For example, isolation device ID-1

among the isolation devices 118 is associated with the first group of memory devices M_{11} , M_{12} , M_{13} , and M_{14} and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices, isolation devices ID- i among the isolation devices 118 is associated with the i^{th} group of memory devices M_{i1} , M_{i2} , M_{i3} , and M_{i4} and is coupled between the group of system data/strobe signal lines 130- i and the i^{th} group of memory devices, and so on.

[0045] In one embodiment, each group or sets of memory devices are coupled to the associated isolation device 118 via a set of module data/strobe lines 210. Each group or set of memory devices is organized in subgroups or subsets, with each subgroup or subset including at least one memory device. The subgroups in a group of memory devices may be coupled to the associated isolation device 118 via a same set of module data/strobe lines 210 (as shown in FIG. 2A) or via respective subsets of module data/strobe lines 210 (as shown in FIG. 2B). For example, as shown in FIG. 2B, in the first group of memory devices, memory devices M_{11} and/or M_{13} form a first subgroup, and memory devices M_{12} and/or M_{14} form a second subgroup; in the i^{th} group of memory devices, memory devices M_{i1} and/or M_{i3} form a first subgroup, and memory devices M_{i2} and/or M_{i4} form a second subgroup; and so on. The first subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device 118 via an associated first subset of module data/strobe lines YA, and the second subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device via an associated second subset of module data/strobe lines YB, as shown. For example, memory devices M_{11} and/or M_{13} form the first subgroup are/is coupled to the isolation device ID-1 via the corresponding first subset of module data/strobe lines YA-1, and memory devices M_{12} and/or M_{14} form the second subgroup are/is coupled to the isolation device ID-1 via the corresponding second subset of module data/strobe lines YA-2.

[0046] In one embodiment, the isolation devices 118 are in the data paths between the MCH 101 and the memory module 110 and include data buffers between the MCH 101 and the respective groups of memory devices. In one embodiment, each isolation device 118 is

configured to select a subgroup in the respective group of memory devices to communicate data with the MCH 101 in response to the module control signals, such that the memory module can include more ranks than what is supported by the MCH 101. Further, each isolation devices 118 is configured to isolate unselected subgroup(s) of memory devices from the MCH 101 during write operations, so that the MCH sees a load on each data line that is less than a load associated with the respective group of memory devices. In one embodiment, the MCH sees only a load associated with one memory device on each data/strobe signal line during write operations.

[0047] In one embodiment, the isolation devices 118 are distributed across the memory module 110 or the module board 119 in positions corresponding to the respective groups of memory devices. For example, isolation device ID-1 is disposed in a first position corresponding to the first group of memory devices M_{i1} , M_{i2} , M_{i3} , and M_{i4} , and isolation device ID- i is disposed in an i^{th} position separate from the first position and corresponding to the i^{th} group of memory devices M_{i1} , M_{i2} , M_{i3} , and M_{i4} . In one embodiment, the first position is between the first group of memory devices and an edge 201 of the module board 119 where connections (not shown) to the data/strobe signal lines 130 are placed, and i^{th} position is between the i^{th} group of memory devices and the edge 201 of the module board 119. In one embodiment, the isolation devices 118 are distributed along the edge 201 of the memory module 110. In one embodiment, each isolation device 118 is a separate integrated circuit device packaged either by itself or together with at least some of the respective group of memory devices. In one embodiment, the module data/strobe signal lines 210, the module C/A signal lines 220, and the module control signal lines 230 include signal traces formed on and/or in the module board 119.

[0048] As an option, memory module 110 may further include a serial-presence detect (SPD) device 240, which may include electrically erasable programmable read-only memory (EEPROM) for storing data that characterize various attributes of the memory module 110. Examples of such data include a number of row addresses, a number of column addresses, a data width of the memory devices, a number of ranks on the memory

module 110, a memory density per rank, a number of memory device on the memory module 110, and a memory density per memory device, etc. A basic input/output system (BIOS) of system 100 can be informed of these attributes of the memory module 110 by reading from the SPD 240 and can use such data to configure the MCH 101 properly for maximum reliability and performance.

[0049] In certain embodiments, the SPD 240 and/or the control circuit 116 store module configuration information, such as: memory space translation code, memory address mapping function code, input and output signals timing control information for the control circuit 116, input and output signals electrical and logical level control information for the control circuit 116, etc. In certain embodiments, the SPD 240 contains a system view of the module 110 which can be different from an actual physical construction of the module 110. For example, the SPD 240 stores at least one memory operation parameter that is different from a corresponding memory operation parameter in a system memory controller setting. The SPD 240 may also store at least one data buffer operation parameter that is different from a corresponding parameter in the system memory controller setting.

[0050] Thus, in certain embodiment, in the memory module 110, C/A signals representing a memory command are received and buffered by the module control circuit 116, so that the MCH sees only the module control circuit 116 as far as the C/A signals are concerned. Write data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118. On the other hand, read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130. Thus, MCH 101 does not directly operate or control the memory devices 112. As far as data/strobe signals are concerned, the MCH 101 mainly sees the isolation devices 118, and the system 100 depends on the isolation devices 118 to properly time the transmission of the read data and strobe signals to the MCH 101.

[0051] In certain embodiments, the memory module 110 is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access

memory devices (DRAM). In certain embodiments, the control circuit 116 includes a DDR register, and logic for memory space translation between a system memory domain and a module level physical memory domain. Such translation may produce address mapping, proper interface timing for the control signals to the module level physical memory domain, and a proper interface electrical and logical level for the control signals to the module level physical memory domain.

[0052] As shown in FIG. 2C, in certain embodiments, the control circuit 116 transmits registered C/A and clock signals to the memory devices 112, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices 118, in a fly-by configuration. As the speed of memory operations increase, issues can arise with respect to signal alignment for input, output delay variation due process, voltage and temperature (PVT) variations, synchronization with system memory controller interface, and phase drift accumulation during operation, etc. Electrical interface calibration drift during operation due to charge build up and timing interface calibration drift during operation due to environment change can also create issues.

[0053] For example, load reduction mechanism in the isolation devices 118 would provide a single data bus interface to the respective set of memory devices, which is hidden from the system memory controller 101. Thus, a long sequence of interface timing training may be required due to limited controllability of the system memory controller 101 over the interface between the memory devices 112 and the associated isolation devices 118. Furthermore, interface signal alignment-drift after the initial training would not be easily detected by the system memory controller 101, which may cause silent system failure.

[0054] Moreover, clock skew amongst the memory devices 112 and the associated isolation devices 118 due to the distributed architecture of the memory module 110 can cause synchronization issues. As the speed of memory operation increase, data period can become very close to the signal propagation delay time. Thus, such issues cannot simply be addressed by pipelining the data paths, as variation of the signal propagation time through I/Os becomes a very significant portion of a data period.

[0055] To address at least some of the above issues, in certain embodiments, as shown in FIG. 2D, the control circuit 116 transmits registered C/A signals to the memory devices 112, and transmits the module control signals and the module clock signal to the data buffers 118, in a fly-by arrangement. The memory devices 112 do not receive the module clock signal from the control circuit 116. Instead, each data buffer 118 regenerates the clock that is used by the respective set of memory devices 112. Each Data buffer 118 is thus responsible for providing a correct data timing interface between the respective set of memory devices 112 and the system memory controller 101. Each data buffer 118 is also responsible for providing the correct control signal timing between the control circuit 116 and the respective set of memory devices 112.

[0056] Thus, the memory module 110 in FIG. 2D allows a locally synchronized operation for each respective set of memory devices 112, which can correspond to a nibble or a byte of a DDR data bus between the memory module 110 and the system memory controller 101. Also, signal interface between each data buffer 118 and the respective set of memory devices 112 can be synchronized. In one embodiment, each data buffer 118 has a set of configurable operations, including, for example: programmable phase relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices 112, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller 101, programmable phase adjustment related to at least one control signal that is coupled to the control circuit 116. The locally synchronized operation also makes it easier for each data buffer 118 to perform self-testing of the associated set of memory devices 112, independent of the self-testing of other sets of memory devices performed by the other data buffers, as disclosed in commonly-owned U.S. Patent 8,001,434, entitled "Memory Board with Self-Testing Capability," which is incorporated herein by reference in its entirety.

[0057] In certain embodiments, operations of the isolation devices 118 are controlled by the module control signals from the module control circuit 116, which generates the module control signals according to the C/A signals received from the MCH. Thus, the

module control signals need to be properly received by the isolation devices 118 to insure their proper operation. In one embodiment, the module control signals are transmitted together with the module clock signal CK, which is also generated by the module control circuit 116 based on the system clock signal MCK. The isolation circuits 118 buffers the module clock signal, which is used to time the sampling of the module control signals. Since the isolation devices 118 are distributed across the memory module, the module control signal lines 230 can stretch across the memory module 110, over a distance of several centimeters. As the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals. Therefore, in one embodiment, the isolation circuits 118 includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or the module clock signal to mitigate any metastability condition in the module control signals, as explained in further detail below.

[0058] Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-($n-1$) in the exemplary configuration shown in FIG. 2. In other words, a same set of module control signals may reach different isolation devices 118 at different times across more than one clock cycle of the system clock. For example, when the clock frequency of the system clock is higher than 800 MHz, the clock cycle time is less than about 1.2 ns. With a signal travel speed of about 70ps per centimeter of signal line, a module control signal would travel about 15 cm during one clock cycle. When the clock frequency increases to 1600 MHz, a module control signal would travel less than 8 cm during one clock cycle. Thus, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appear on the signal line.

[0059] With the isolation devices 118 receiving module control signals at different times across more than one clock cycle, the module control signals alone are not sufficient to time the transmission of read data signals to the MCH 101 from the isolation devices 118. In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100, as explained in more detail below.

[0060] More illustrative information will now be set forth regarding various optional configurations, architectures, and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0061] In one embodiment, as shown in FIG. 3, each group of signal lines 130 include a set of n data (DQ) signal lines 322 each for transmitting one of a set of data signals $DQ_0, DQ_1, \dots, DQ_{n-1}$, and at least one strobe (DQS) signal line 324 for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of n module data signal lines $Y_0, Y_1, \dots, Y_{n-1}$ and at least one module strobe signal line Y_{DQS} . When the subsets of memory devices are coupled to the associated isolation device 118 via respective subsets of memory devices, each set of module data/strobe lines Y may include multiple subsets of module data/strobe lines, such as the subsets of module data/strobe lines YA and YB shown in FIG. 2B. Each subset of module data/strobe lines YA include a set of n first module data lines $YA_0, YA_1, \dots, YA_n$ and at least one first module strobe signal line YA_{DQS} ; and each subset of module data/strobe lines YB include a set of n second module data lines $YB_0, YB_1, \dots, YB_n$ and at least one second module strobe signal line YB_{DQS} .

[0062] Each isolation device 118 includes a set of DQ routing circuits 320 coupled on one side to respective ones of the set of n DQ signal lines 322, and on another side to respective ones of the respective set of n module data lines, or respective ones of the respective subsets of module data lines, such as the first module data lines $YA_0, YA_1, \dots, YA_n$ and the second module data lines $YB_0, YB_1, \dots, YB_n$. Each isolation device 118 further includes an ID control circuit 310 coupled on one side to the at least one DQS signal line 324, on another side to the one or more module strobe signal lines Y_{DQS} , or the first module strobe signal line YA_{DQS} and second module strobe signal line YB_{DQS} . The ID control circuit 310 also receives the module clock signal CK and the module control signals via the module control signal lines 230, and outputs ID control signals 330 to the DQ routing circuits 320, including, for example, one or more enable signals ENA and/or ENB, and some or all of the other received, decoded, and/or otherwise processed module control signals, a delay signal DS, a read DQS signal RDQS, a write DQS signal WDQS, and a buffer clock signal CK0. Each DQ routing circuit 320 is configured to enable data communication between the respective DQ signal line 322 with a selected subgroup of one or more memory devices in response to the module control signals, as explained in more detail below.

[0063] In certain embodiments, the ID control circuit 310 also provides a delay signal DS, which is used by the DQ routing circuits 320 to align read data output by the isolation device 118 with read data output by the other isolation devices 118, as explained in further detail below. In certain embodiments, the ID control circuit 310 regenerates a clock signal from the module clock signal CK, which can have a programmable delay from the module clock signal. The regenerated clock signal is used as the clock signal CK0 and a clock signal CKM that is provided to the corresponding set of memory devices, as explained in more detail below.

[0064] The memory devices 112 are coupled to the isolation devices 118 via a same set of module data/strobe signal lines or different subsets of module data/strobe signal lines. For example, as shown in FIG. 4A, memory devices M_{11}, M_{12}, M_{13} , and M_{14} in the first group of memory devices can be coupled to the isolation device ID-1 via a same set of module

data lines Y-1₀, Y-1₁, ..., Y-1_{n-1} and module strobe line Y-1_{DQS}. In such embodiment, a subgroup in the group of memory devices can be selected by the isolation devices to communicated data with the MCH based on the phases of the data/strobe signals, which can be different with respect to different subgroups of memory devices.

[0065] Alternatively, as shown in FIG. 4B, memory devices M₁₁ and M₁₃, which form a subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines YA-1₀, YA-1₁, ..., YA-1_n and module strobe line YA-1_{DQS} and memory devices M₁₂ and M₁₄, which form another subgroup in the first group of memory devices, are coupled to the isolation device ID-1 via the module data lines YB-1₀, YB-1₁, ..., YB-1_n and module strobe line YB-1_{DQS}. Memory devices coupled to the same isolation devices can be disposed on a same side or different sides of the memory board 119. Memory devices coupled to the same isolation devices may be placed side by side, on opposite sides of the module boards 119, or stacked over each other, and/or over the associated isolation device.

[0066] Multiple memory devices having a data width that is less than a data width of the isolation devices 118 may be used in place of one of the memory devices 112, which has the same data width as that of the isolation devices. For example, as shown in FIG. 5A, two memory devices M₁₁₋₁ and M₁₁₋₂ may be used in place of the memory device M₁₁. Each of the two memory devices M₁₁₋₁ and M₁₁₋₂ has a data width of 4, and together they act like a memory device M₁₁ of a data width of 8. Thus, memory device M₁₁₋₁ is coupled to the isolation device ID-1 via module data lines YA-1₀, ..., YA-1₃ and module strobe line YA-1_{DQS-1} while memory circuit M₁₁₋₂ is coupled to the isolation device ID-1 via module data lines YA-1₄, ..., YA-1₇ and module strobe line YA-1_{DQS-2}.

[0067] In another embodiment, as shown in FIG. 5B, four memory devices M₁₁₋₁ to M₁₁₋₄ may be used as the memory device M₁₁. Each of the four memory devices M₁₁₋₁ to M₁₁₋₄ has a data width of 4, and together they act like a memory device M₁₁ of a data width of 16. Thus, memory device M₁₁₋₁ is coupled to the isolation device ID-1 via module data lines YA-1₀, ..., YA-1₃ and module strobe line YA-1_{DQS-1} while memory device M₁₁₋₂ is coupled

to the isolation device ID-1 via module data lines YA-14, ..., YA-17 and module strobe line YA-1_{DQS-2}, and so on.

[0068] FIG. 6 illustrates the ID control circuit 310 in an isolation device 118. As shown, the ID control circuit 310 includes a clock buffer 610 to receive the module clock signal CK from the module control device 116, and to output a module clock signal CK0. The ID control circuit 310 further includes a strobe routing circuit 620 that are coupled on one side to the corresponding system DQS signal line 324 and on another side to the corresponding module DQS signal lines YA_{DQS} and YB_{DQS}. The ID control circuit 310 further includes a receiver circuit 630 with respect to each of at least some of the module control signals (MCS) to receive a respective one of the module control signals. The ID control circuit 310 further includes a command processing circuit 640 that provides the received, decoded, and/or otherwise processed module control signals 330 to the DQ routing circuits 320 and the strobe routing circuit 620 either directly or after further processing, if needed. The received/decoded/processed module control signals may include, for example, one or more enable signals ENA and/or ENB that are used by the DQ routing circuits 320 and the strobe routing circuit 620 to selectively enabling data communication between the MCH 101 and one of the subgroups in the respective group of memory devices, with which the isolation device is associated.

[0069] The strobe routing circuit 620 also buffers strobe signals received from either the MCH 101 or the memory devices 112, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits 320. In one embodiment, the ID control circuit 310 further includes a delay control circuit 650 that receives one of the module control signals and either a data signal or a strobe signal and determines a delay amount to be used by the DQ routing circuit 320 and the strobe routing circuit 620. The delay amount is provided to the DQ routing circuit 320 and the strobe routing circuit in a delay signal DS.

[0070] In a receiver circuit 630, the respective MCS is received in accordance with the module clock signal CK0. In one embodiment, receiver circuit 630 samples the respective MCS using rising (or falling) edges of the module clock CK0. Since the isolation devices

118 are distributed across the memory module 110 at positions corresponding to the respective groups of memory devices, the module control signal lines 230 that carry the MCS to the isolation devices can stretch over a distance of more than 10 centimeters, as shown in FIG. 7. As the MCS and CK0 travel along their respective module control signal lines 710 and 720, they can become misaligned with each other when they reach the input pins 730 of an isolation device 118.

[0071] For example, a module control signal, like the MCS 810 shown in FIG. 8, can be perfectly aligned with the module clock signal CK, with a rising edge 801 of the module clock signal CK being at a center of a data eye 802, when the MCS signal and the clock signal leave the module control circuit 116. When the module control signal and the module clock signal reach an isolation device, however, their alignment can become shifted like the MCS 820 with respect to the CK signal, i.e., the rising edge 801 of the clock signal is near a left edge of a data eye of the MCS 820, barely providing enough set up time for proper sampling of the module control signal. Or, the module control signal, like the MCS 830, can be shifted with respect to the module clock signal such that a rising edge 801 of the clock signal is near a right edge of a data eye of the MCS, barely providing enough hold time for proper sampling of the module control signal. Or, ever worse, the module control signal, like the MCS 840, can be so shifted with respect to the module clock signal such that a rising edge 801 of the clock signal falls in the glitches 803 at the edge of a data eye of the MCS, meaning that the sampled results could be metastable.

[0072] In one embodiment, as shown in FIG. 9, a receiver circuit 630 includes a metastability detection circuit (MDC) 910 to determine a metastability condition in a corresponding module control signal MCS0. In one embodiment, the MDC 910 generates at least one delayed version of the module clock signal CK and at least one delayed version of the corresponding MCS0. The MDC 910 also generates one or more metastability indicators and outputs the one or more metastability indicators via lines 912 and/or 914.

[0073] The receiver circuit 630 further includes a signal selection circuit 920 that receives the module clock CK and the at least one delayed version of the module clock via signal

lines 916. The signal selection circuit 920 also receives the corresponding MCS and the at least one delayed version of the corresponding MCS via signal lines 918. The signal selection circuit 920 selects a clock signal CK_i from among the module clock CK and the at least one delayed version of the module clock based on one or more of the metastability indicators. The signal selection circuit 920 may also select an MCS signal MCS_i from among the corresponding MCS and the at least one delayed version of the corresponding MCS based on at least one other metastability indicator.

[0074] The receiver circuit 630 further includes a sampler or register circuit 930 that samples the selected module control signal MCS_i according to the selected clock signal CK_i and outputs the sampled signal as the received module control signal, which is provided to the command processing circuit 640 for further processing (if needed) before being provided to the DQ routing circuits 320 and DQS routing circuit 620.

[0075] FIG. 10A illustrates an MDC 910 according to one embodiment. As shown, the MDC 910 includes a delay circuit 1012 that generates a delayed version MCS_1 of the corresponding MCS_0 by adding a predetermined amount of delay (e.g., 10ps) to MCS_0 . MDC 910 also includes a delay circuit 1016 that generates a delayed version CK_1 of the clock signal CK_0 by adding a predetermined amount of delay to CK_0 . In one embodiment, CK_1 is delayed from CK_0 by about 1/10th of a clock cycle, e.g., 50-70 ps for an operating frequency of about 1600 MHz. The MDC 910 further includes a sampler circuit 1042 that samples MCS_1 according to CK_0 and outputs a sampled result A, a sampler circuit 1044 that samples MCS_0 according to CK_0 and outputs a sampled result B, and a sampler circuit 1046 that samples MCS_0 according to CK_1 and outputs a sampled result C. The MDC 910 further includes a logic circuit (e.g., a majority decision circuit) that generates metastability indicators Z1 and Z2 based on the sampled results A, B, and C.

[0076] In one embodiment, Z1 is the result of a logic operation (e.g., an XNOR operation) on the sampled result, e.g., $Z1 = \overline{A \oplus B}$, and Z2 is the result of another logic operation on the sampled results, e.g., $Z2 = \overline{B \oplus C}$. Thus, as shown in FIG. 10B and Table 1 below, when a metastability condition of insufficient hold time occurs, i.e., a rising clock edge

1061 of CK0 is close to the right side of a data eye where glitches at the edges of the data eyes can make C unpredictable, A and B can be in agreement (i.e., Z1 is true) while B and C are likely not in agreement (i.e., Z2 is false). FIG. 10 C illustrates a metastability condition when there is insufficient set-up time. As shown in FIG. 10C and Table 1 below, a rising clock edge 1061 of CK0 is close to the left side of a data eye where glitches at the edges of the data eyes can make A unpredictable. Thus, A and B can be in disagreement so Z1 is false while B and C can be in agreement so Z2 is true. Not shown in the figures is the situation that all A, B, and C are in agreement, meaning that both the rising clock edge 1061 of CK0 and the rising clock edge 1062 of CK1 are near the middle of an MCS0 data eye so there is no metastability issues and both Z1 and Z2 are true, as shown in Table 1.

[0077] FIG. 10D illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1071 that selects between CK0 and CK1 based on the metastability indicator Z1, and a second multiplexor 1072 that selects between MCS0 and MCS1 based on the metastability indicator Z2. Thus, as shown in Table 1, where a metastability condition of insufficient hold time occurs, $Z1=1$ and $Z2=0$, and MCS1 is output from multiplexor 1071 while CK0 is output from multiplexor 1072. Sampler 930 thus samples MCS1 according to the rising edges of CK0. Thus, more hold time is provided to mitigate the metastability condition since MCS1 is shifted from MCS0 toward the right.

[0078] On the other hand, where a metastability condition of insufficient set-up time occurs, $Z1=0$ and $Z2=1$, and CK1 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. Sampler 930 thus samples MCS0 according to the rising edges of CK1. Since CK1 is shifted from CK0 toward the right, more set-up time is provided to mitigate the metastability condition.

Table 1 Metastability Detection and Signal Selection

Sampler Output			MS Indicators		MS Condition	Signal Selection	
A	B	C	Z1	Z2		CK	MCS
D1	D1	D2	1	0	insufficient hold time	CK0	MCS1
D1	D2	D2	0	1	insufficient set-up time	CK1	MCS0
D1	D1	D1	1	1	no metastability	CK0	MCS0

[0079] In the case when no metastability is detected, Z1=1 and Z2=1, and CK0 is output from multiplexor 1071 while MCS0 is output from multiplexor 1072. So, the unshifted module control signal is sampled according to the unshifted module clock signal.

[0080] FIGS. 10A-10D illustrate a relatively simple implementation of the metastability detection circuit (MDC) 910 where only three different sample points are provided to detect metastability condition in the module control signal. In general, the MDC 910 may generate more delayed versions of the module clock signal CK0 and/or the corresponding module control signal MCS0, and may include more sampler circuits to sample any additional delayed versions of the module control signal according to either the module clock signal or one of the delayed versions of the module clock signal. For example, as shown in FIG. 11A, the MDC 910 can include a plurality of delay circuits 1102 that generate m delayed versions of MCS0, e.g., MCS1, MCS2, ... MCS m , and m delayed versions of CK0, e.g., CK1, CK2, ..., CK m . The MDC 910 can include sampler circuits 1104 that sample MCS0 according to CK0, CK1, ..., CK m , respectively, and sampler circuits 1104 that sample MCS0, MCS1, MCS2, ... MCS m according to CK0, respectively. The outputs of the samplers 1104 are provided to a logic circuit 1120, which determines a metastability condition in MCK0 based on the sampler outputs using, for example, a majority decision logic. The logic circuit 1120 outputs a first metastability indicator on line(s) 912 and a second metastability indicator on line(s) 914.

[0081] FIG. 11B illustrates a signal selection circuit 920 according to an embodiment. As shown, in one embodiment, the signal selection circuit 920 includes a first multiplexor 1171 that selects between CK0, CK1, ..., CK m based on the metastability indicator

provided on line(s) 912, and a second multiplexor 1172 that selects between MCS₀, MCS₁, ..., MCS_{*m*} based on the metastability indicator provided on line(s) 914, such that the rising edges of the selected clock signal, e.g., Ck_{*i*}, are close to the middle of the respective data eyes in the selected module control signal, e.g., MCS_{*i*}. The selected signals MCS_{*i*} and Ck_{*i*} are provided to the sampler 930, which samples MCS_{*i*} according to the rising edges of CK_{*i*}.

[0082] As stated above, in certain embodiments, since the isolation devices 118 are in the data paths between the MCH 101 and the respective groups of memory devices 112, the MCH 101 does not have direct control of the memory devices 112. Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing. In one embodiment, the isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation, as discussed further below.

[0083] FIG. 12A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit 116 at time t₁, the module control circuit 116 outputs one or more enable signals EN at time t₂ in response to the write commands. The one or more enable signals are received by an isolation device 118 at time t₃, which afterwards receives one or more strobe signal DQS from the MCH 101 at time t₄. Note that the same enable signal may be received by another isolation device 118 at time t₃', which can be in a different cycle of the system clock MCK from the cycle which t₃ is in. The time interval between t₄ and t₁ is consistent with a write latency W.L. associated with the system 100, and is controllable by the MCH 101 and knowable to the isolation device 118. The time interval between t₄ and t₃, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device 118 since both these signals are received by the isolation device. Based on such determination, the isolation device 118 can have knowledge of the time interval between t₃ and t₁, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device 118 to properly

time transmission of read data to the MCH, as explained further below.

[0084] FIG. 12B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit 116 at time t5, the module control circuit 116 outputs one or more enable signals EN at time t6 in response to the read commands. The one or more enable signals are received by an isolation device 118 at time t7, which afterwards receives at time t8 read data signals (not shown) and one or more strobe signal DQS from the respective group of memory devices. Note that the same enable signal may be received by another isolation device 118 at time t3', which can be in a different cycle of the system clock MCK from the cycle which t3 is in. Thus, the enable signals alone cannot be used to time the transmission of the read signals by the isolation devices 118.

[0085] With knowledge of the time interval between t7 and t5, which should be about the same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH 101 via the respective group of data/strobe signal lines 130, with the time interval between t9 and t5 being consistent with a read latency R.L. associated with the system 100.

[0086] The time interval between t4 and t3, i.e., the enable to write data delay EWD, is determined by the delay control circuit 650 in the ID control circuit 310, as shown in FIG. 6. According to one embodiment, as shown in FIG. 13, the delay control circuit 650 includes a preamble detector 1310 to detect a write preamble in the DQS, a flip-flop circuit 1320 having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK0, and a counter circuit 1330 having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit 1320. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when the one of the module control signal is received.

[0087] FIG. 14 illustrates a DQ or DQS routing circuit 320 or 620 according to an embodiment. As shown, the DQ/DQS routing circuit 320/620 includes a DQ/DQS pin 1401 that is coupled to the corresponding DQ/DQS signal line 322/324, a set of one or more DQS pins 1402 that is coupled to a corresponding module DQ/DQS line(s) Y/Y_{DQS}, or YA/YA_{DQS} and YB/YB_{DQS}. The DQ/DQS routing circuit 320/620 further includes a write strobe buffer 1410 that buffers write data/strobe, and a write data/strobe receiver 1420 that samples the write data/strobe. The DQ/DQS routing circuit 320/620 further includes a plurality of write paths 1430 that are selectable or can be selectively enabled by one or more of the module control signals, such as the enable signals ENA and ENB.

[0088] The DQS routing circuit further includes a plurality of read paths 1450 that are selectable by the one or more of the module control signals. Output from the selected read path is delayed in a delay circuit 1460 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1470. The sampled read data/strobe is transmitted by transmitter 1480 onto the corresponding data/strobe signal line 322/324 via the DQ/DQS pin 1401.

[0089] FIG. 15 illustrates a DQS routing circuit 620 according to an embodiment. As shown, the DQS routing circuit 620 includes a first DQS pin 1501 that is coupled to a corresponding DQS signal line 324, a second DQS pin 1502A that is coupled to a corresponding module DQS line YA_{DQS}, a third DQS pin 1502B that is coupled to a corresponding module DQS line YB_{DQS}. The DQS routing circuit 620 further includes a first write strobe path coupled between the first DQS pin 1501 and the second DQS pin 1502A and a second write strobe path coupled between the first DQS pin 1501 and the third DQS pin 1502B. The first write strobe path includes a write strobe buffer 1510 that buffers a write strobe, a write strobe receiver 1520 that samples the write strobe according to the buffered module signal CK0. The sampled write strobe is provided to the DQ routing circuits 320 as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter 1530A that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YA_{DQS}. The second write strobe path

includes the write strobe buffer 1510, the write strobe receiver 1520, and a second write strobe transmitter 1530B that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YB_{DQS} . The first and second write strobe transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0090] The DQS routing circuit further includes a read strobe path coupled between the first DQS pin 1501 and a selected one of the second and third DQS pins 1502A and 1502B. In the read strobe path, a select circuit 1550 (e.g., a multiplexor) selects either a read strobe signal received via DQS pin 1502A or a read strobe signal received via DQS pin 1502B based on one or both of the enable signals ENA or ENB. The selected read strobe signal is delayed in a delay circuit 1560 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1570 according to the buffered module clock signal CK0. The sampled read strobe is provided to the DQ routing circuits 320 as the read strobe RDQS and is transmitted by transmitter 1580 onto the corresponding strobe signal line 324 via the first DQS pin 1501.

[0091] FIG. 16 illustrates a DQ routing circuit 320 according to an embodiment. As shown, the DQ routing circuit 320 includes a first DQ pin 1601 that is coupled to a corresponding DQ signal line 130, a second DQ pin 1602A that is coupled to a corresponding module DQ line YA_{DQ} , a third DQ pin 1602B that is coupled to a corresponding module DQ line YB_{DQ} . The DQ routing circuit 320 further includes a first write data path coupled between the first DQ pin 1601 and the second DQ pin 1602A and a second write data path coupled between the first DQ pin 1601 and the third DQ pin 1602B. The first write data path includes a write data buffer 1610, a write data receiver 1620 that samples write data according to the write strobe WDQS from the DQS routing circuit 620, and a first write data transmitter 1630A that transmits the write data to one or more memory devices 112 coupled to the module data line YA_{DQ} . The second write data path includes the write data buffer 1610, the write data receiver 1620, and a second write data

transmitter 1630B that transmits the write data to one or more memory devices 112 coupled to the module data line YB_{DQ}. The first and second write data transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

[0092] The DQ routing circuit further includes a read data path coupled between the first DQ pin 1601 and a selected one of the second and third DQ pins 1602A and 1602B. In the read data path, a select circuit 1650 (e.g., a multiplexor) selects either a read data signal received via DQ pin 1602A or a read data signal received via DQ pin 1602B based on one or both of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit 1660 by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit 1670 according to the read strobe RDQS from the DQS routing circuit 620, and transmitted by transmitter 1680 onto the corresponding data signal line 130 via the first DQ pin 1601.

[0093] FIG. 17 illustrate a delay circuit 1560 or 1660 according to an embodiment. As shown, the delay circuit 1560 or 1660 includes a plurality of delay stages, such as delay stages 1710, 1720, and 1730, each delaying a read data or read strobe signal from the select circuit 1550/1650 by a predetermined amount. The delay circuit 1560 or 1660 further includes a select circuit 1740 (e.g., a multiplexor) that selects from among the read data or read strobe signal and the outputs from the delay stages according to the delay signal DS. The output of the select circuit 1740, is provided to the sampler circuit 1570 or 1670, either directly or after being buffered by a buffer circuit 1750.

[0094] Thus, as shown in FIG. 18, in one embodiment, a memory module 110 operates in the memory system 100 according to a method 1800. In the method, during a write operation, one or more module control signals are received by an isolation device 118 from a module control circuit or module controller 116 (1810). The module controller 116 generates the one or more module control signals in response to C/A signals representing a write command from the MCH 101. The one or more module control signals are used to

control the isolation device 118. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device 118. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device 118 from the MCH 101 (1820). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.

[0095] Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.

[0096] As shown in FIG. 18, a delay signal DS is generated according to the time interval EWD (1830). Concurrent to receiving the write strobe signal DQS, the isolation device 118 also receives a set of write data signals DQ (1840). The received write data signals are transmitted to the subgroup of memory devices (1850), which are selected from the group of memory devices coupled to the isolation device 118 by the one or more first enable signals.

[0097] During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device 118 from the module controller 116 (1860). The one or more second enable signals are generated by the module controller 116 in response to read command signals received from the MCH 101, and are used by the isolation device 118 to select a subgroup of memory devices from

which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (1870). To properly time the transmission of the DQS and DQ signals to the MCH 101, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system 100.

[0098] In certain embodiments, especially the embodiments shown in FIG. 2D, the delay circuits 1560 and 1660 shown in FIGS. 15 and 16 are not needed to provide alignment of the read data. As shown in FIG. 19, the ID control circuit 310 includes a clock regeneration circuit 1920 that regenerates the clock signal CK received from the control circuit 116, according to the delay signal DS. The regenerated clock signals CK0 and CKM each includes a proper amount of delay as compared to the clock signal CK. The clock CK0 is provided to the strobe routing circuit 620 so that the strobe signals are properly timed to result in proper data alignment. The regenerated clock signal CKM is provided to the respective set of memory devices so that the respective data buffer 118 and the respective set of memory devices are locally synchronized.

WE CLAIM:

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.

MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

ABSTRACT OF THE DISCLOSURE

A memory module is operable in a memory system with a memory controller. The memory module comprises memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data signal lines in a data bus and respective sets of the memory devices. Each respective buffer circuit is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices. Each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.

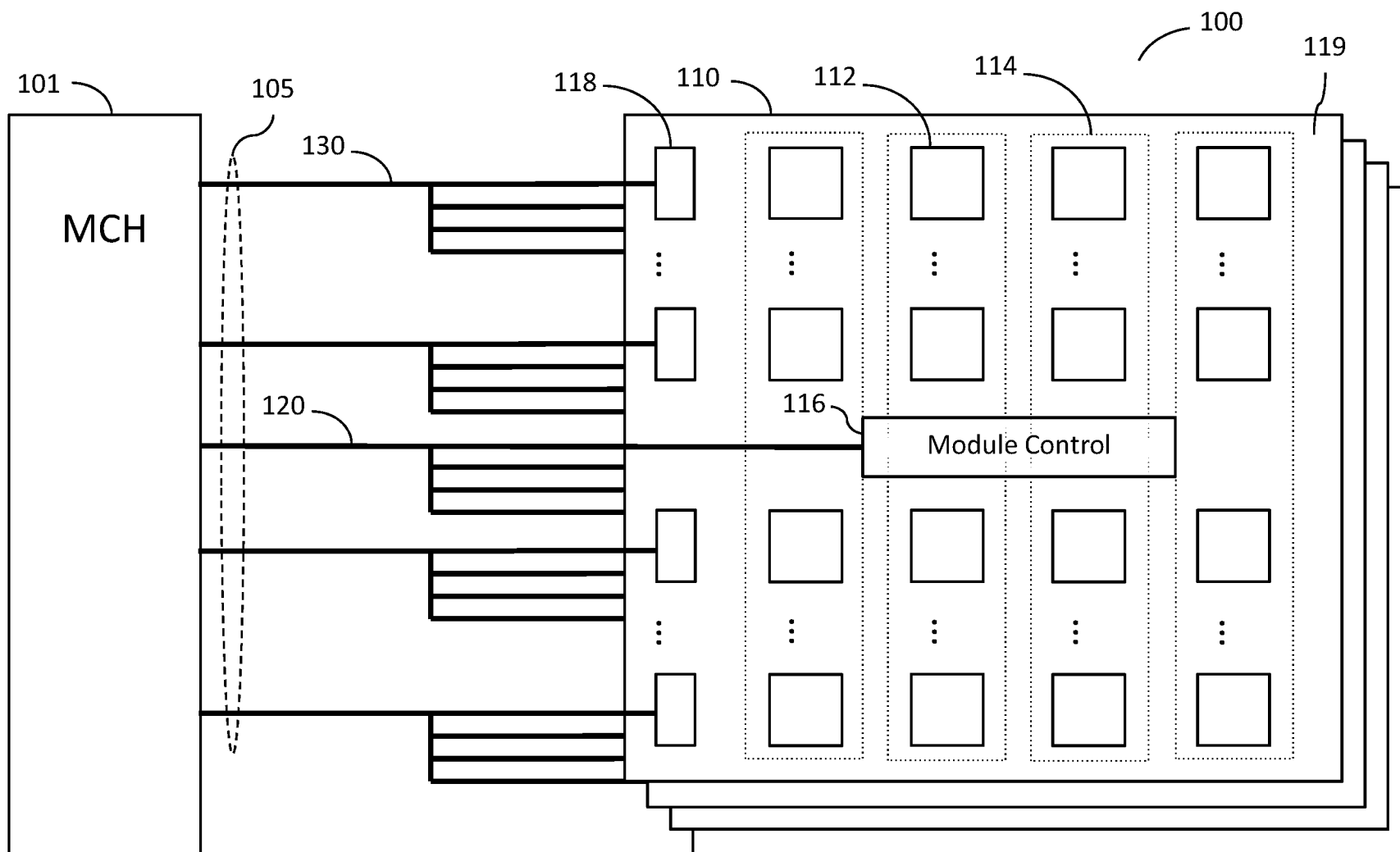
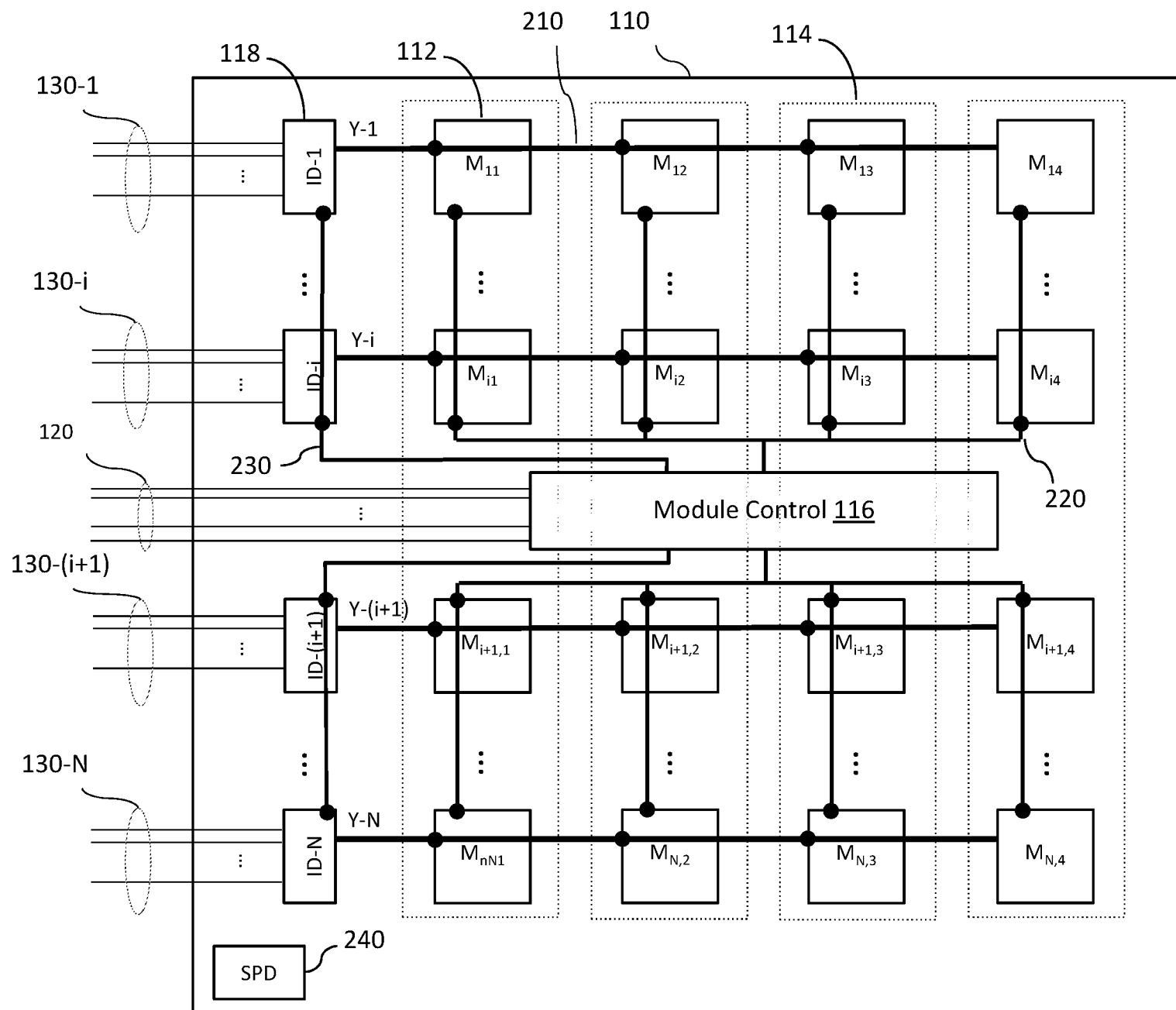


FIG. 1



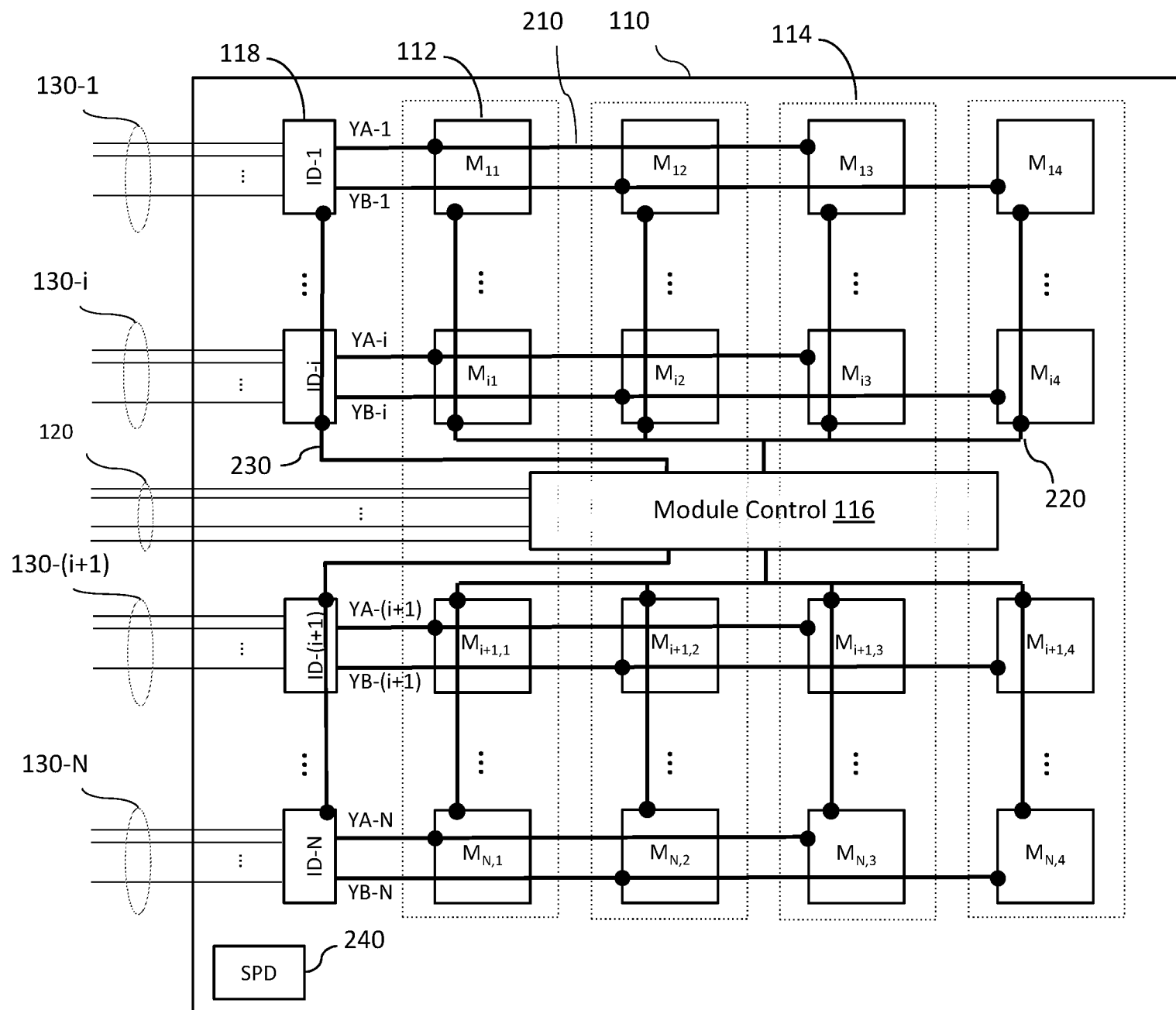
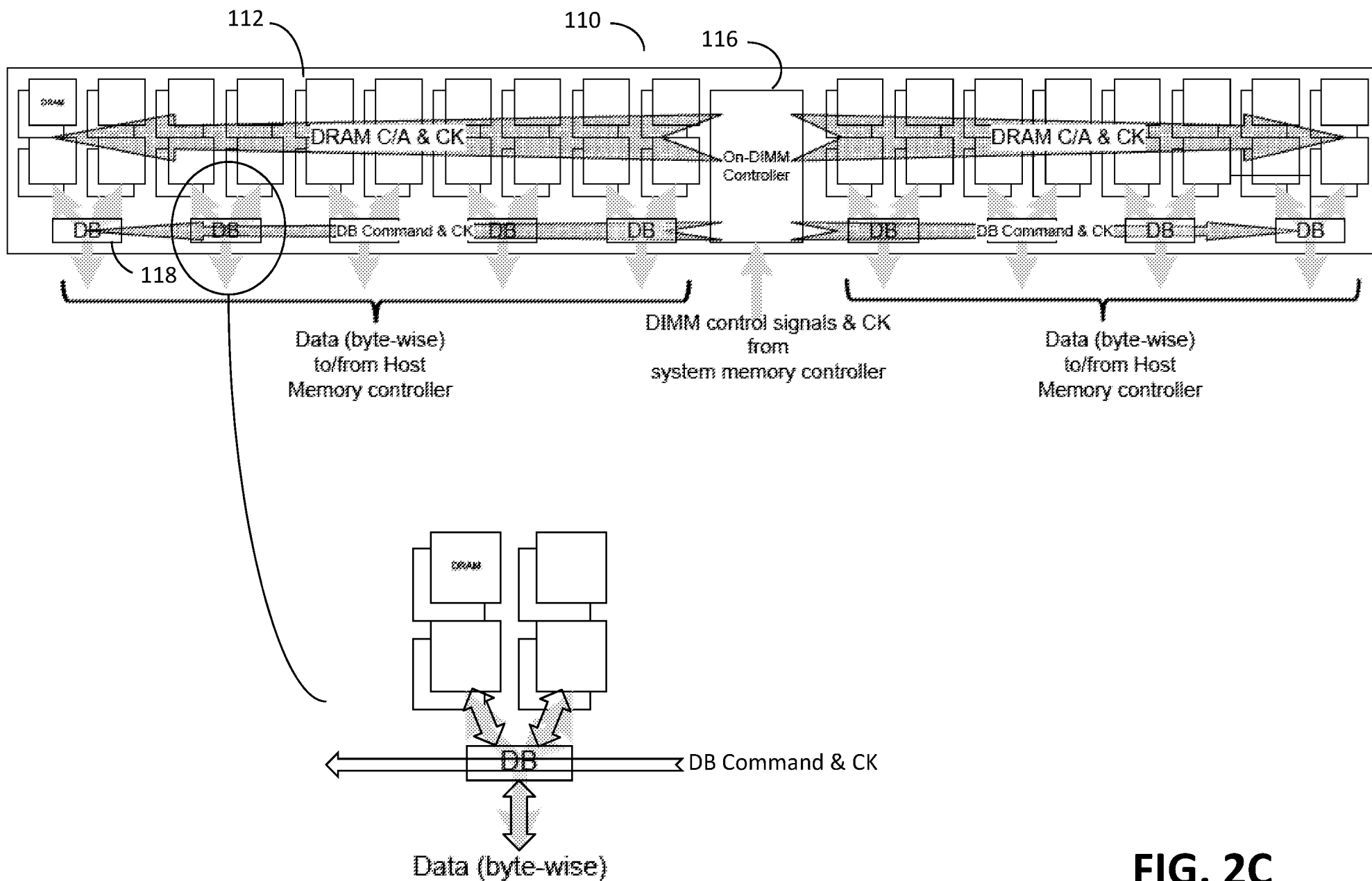
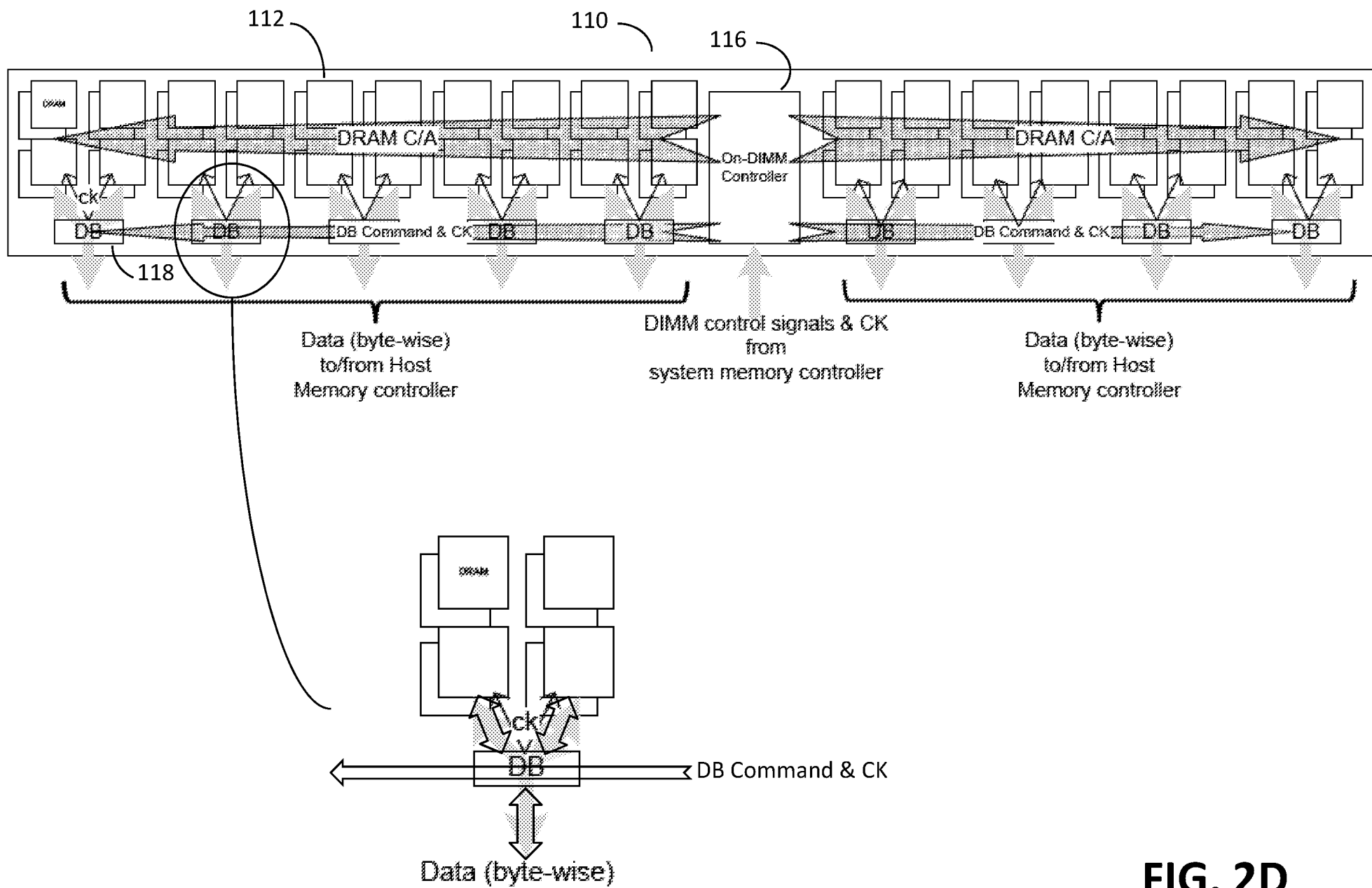
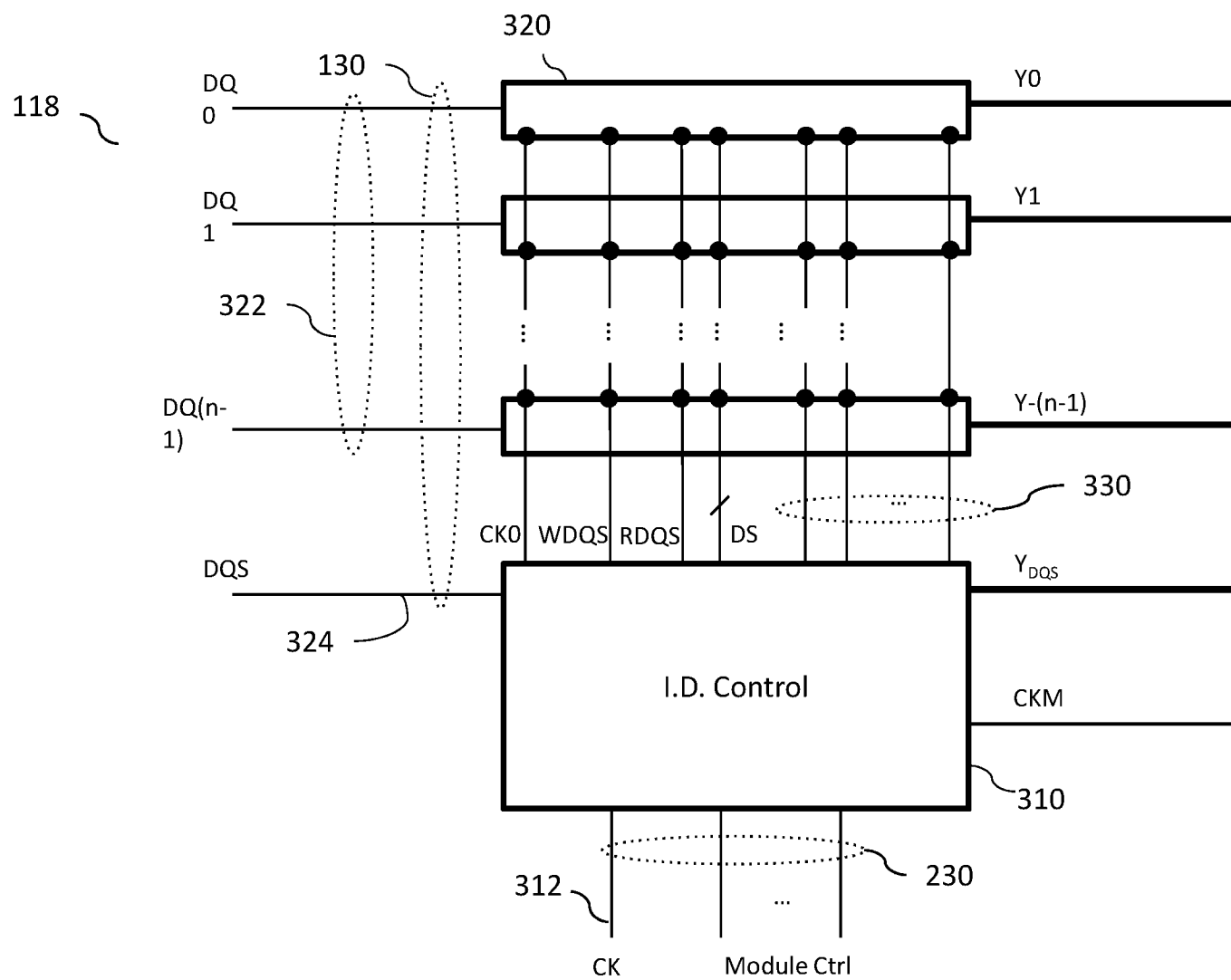
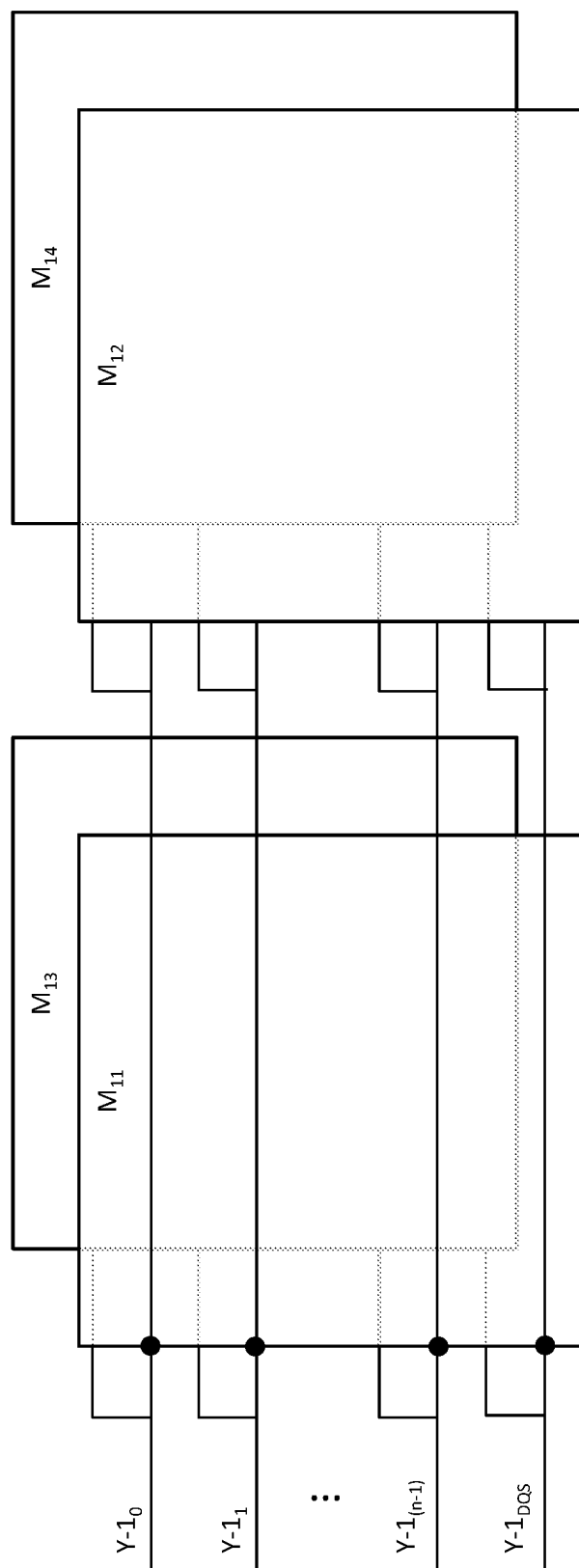


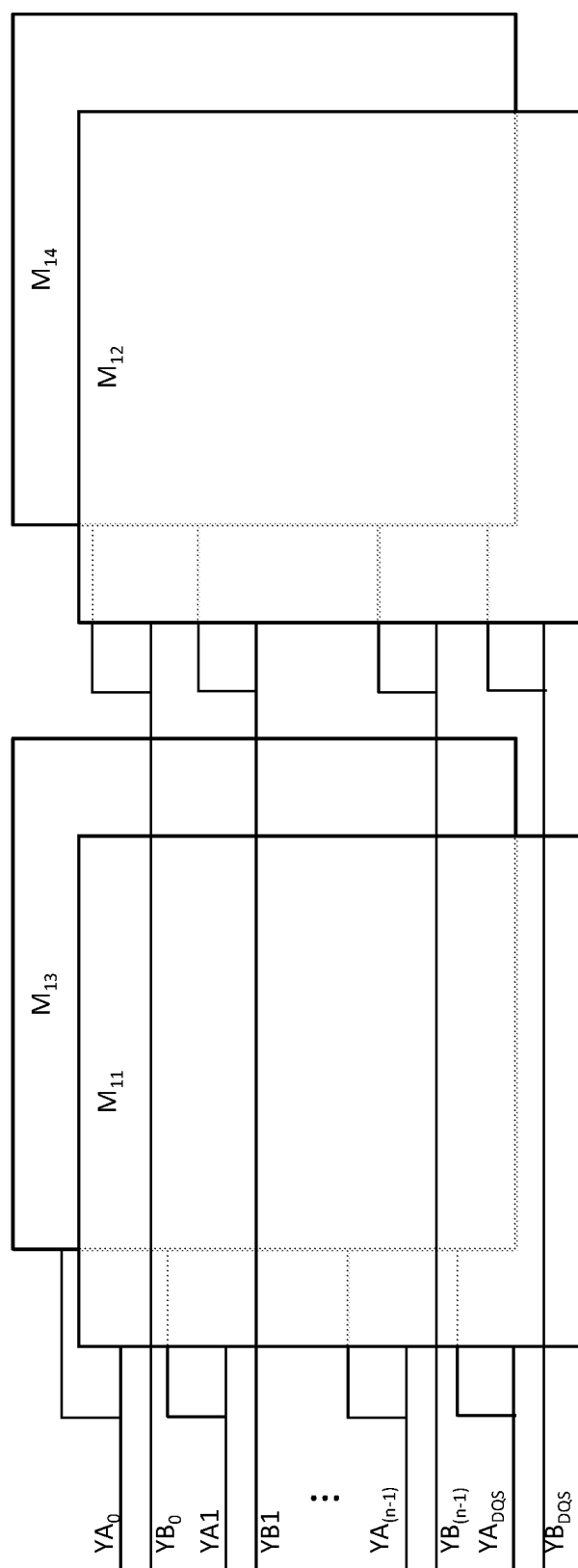
FIG. 2B

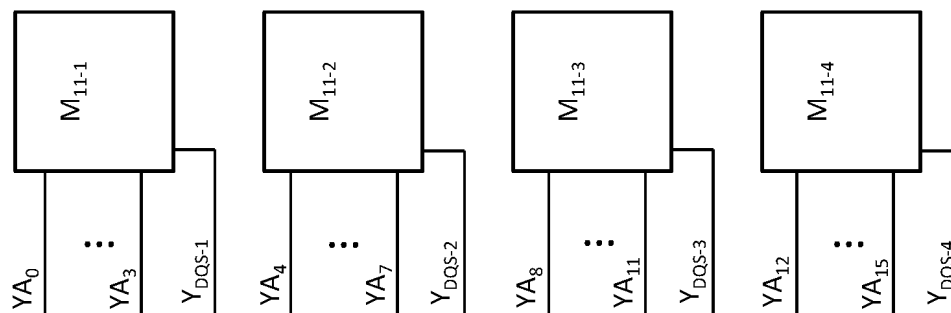
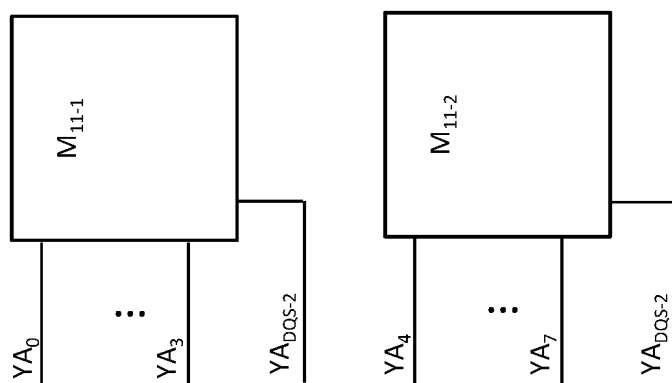
**FIG. 2C**

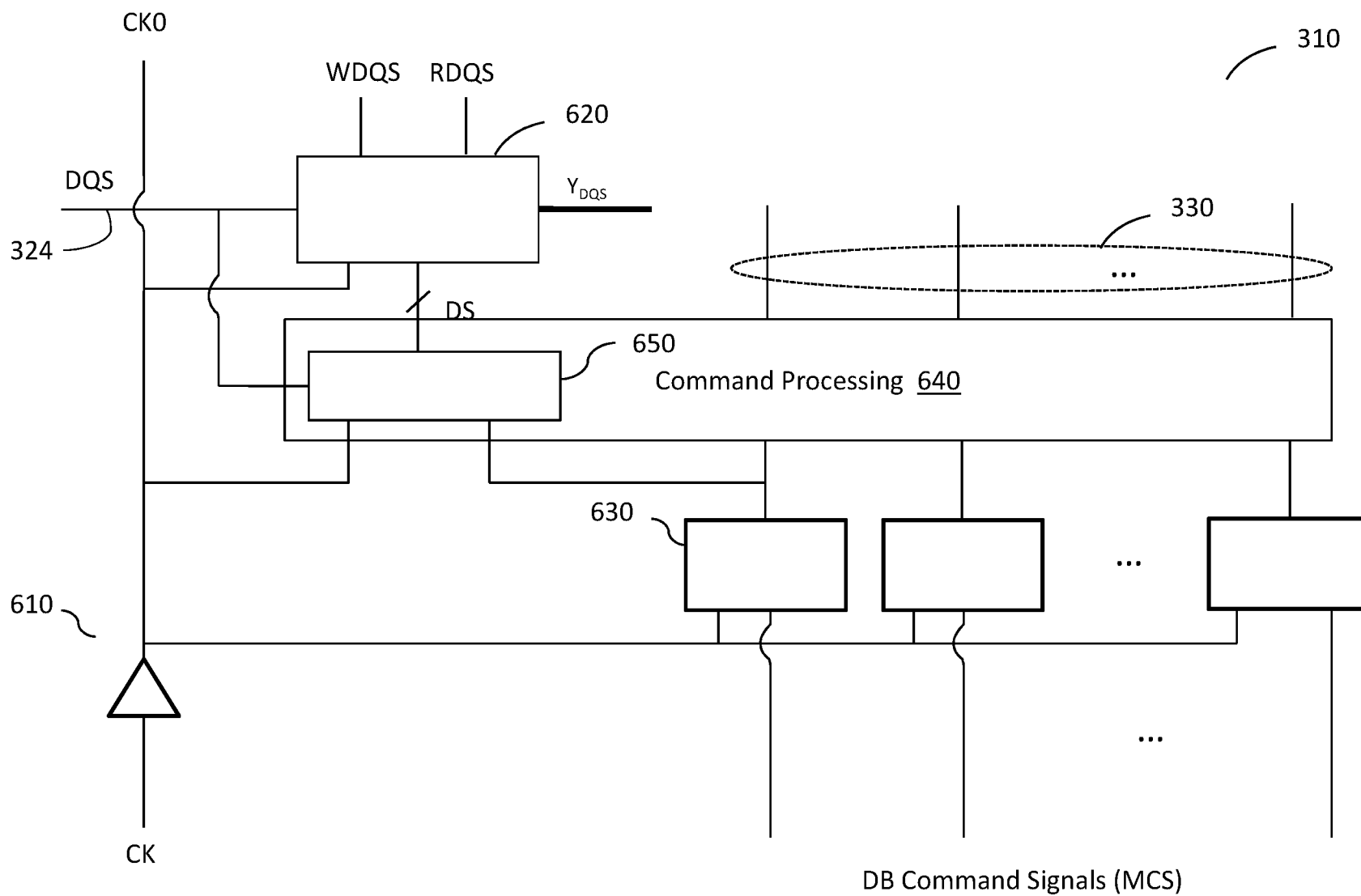
**FIG. 2D**

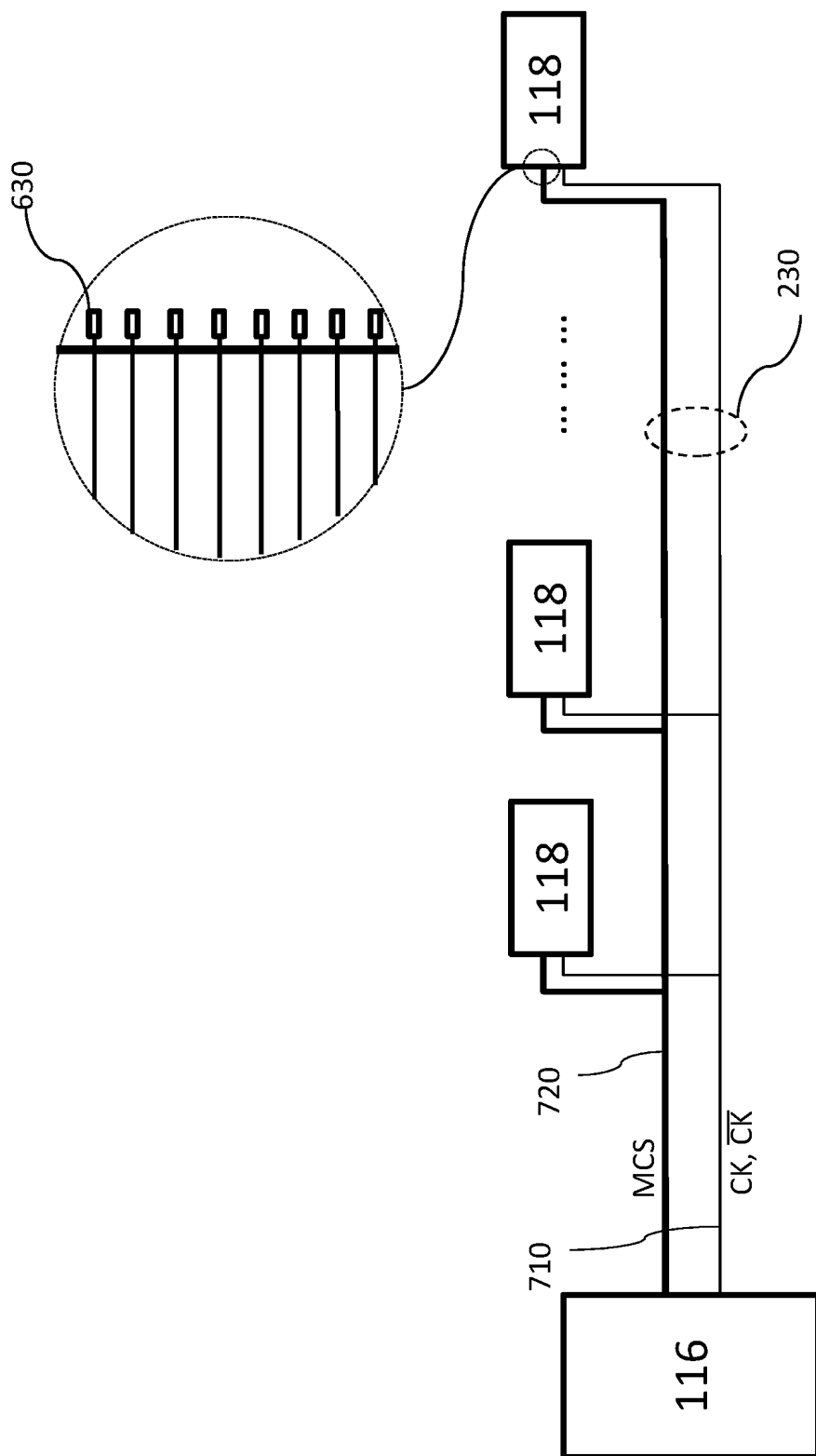
**FIG. 3**

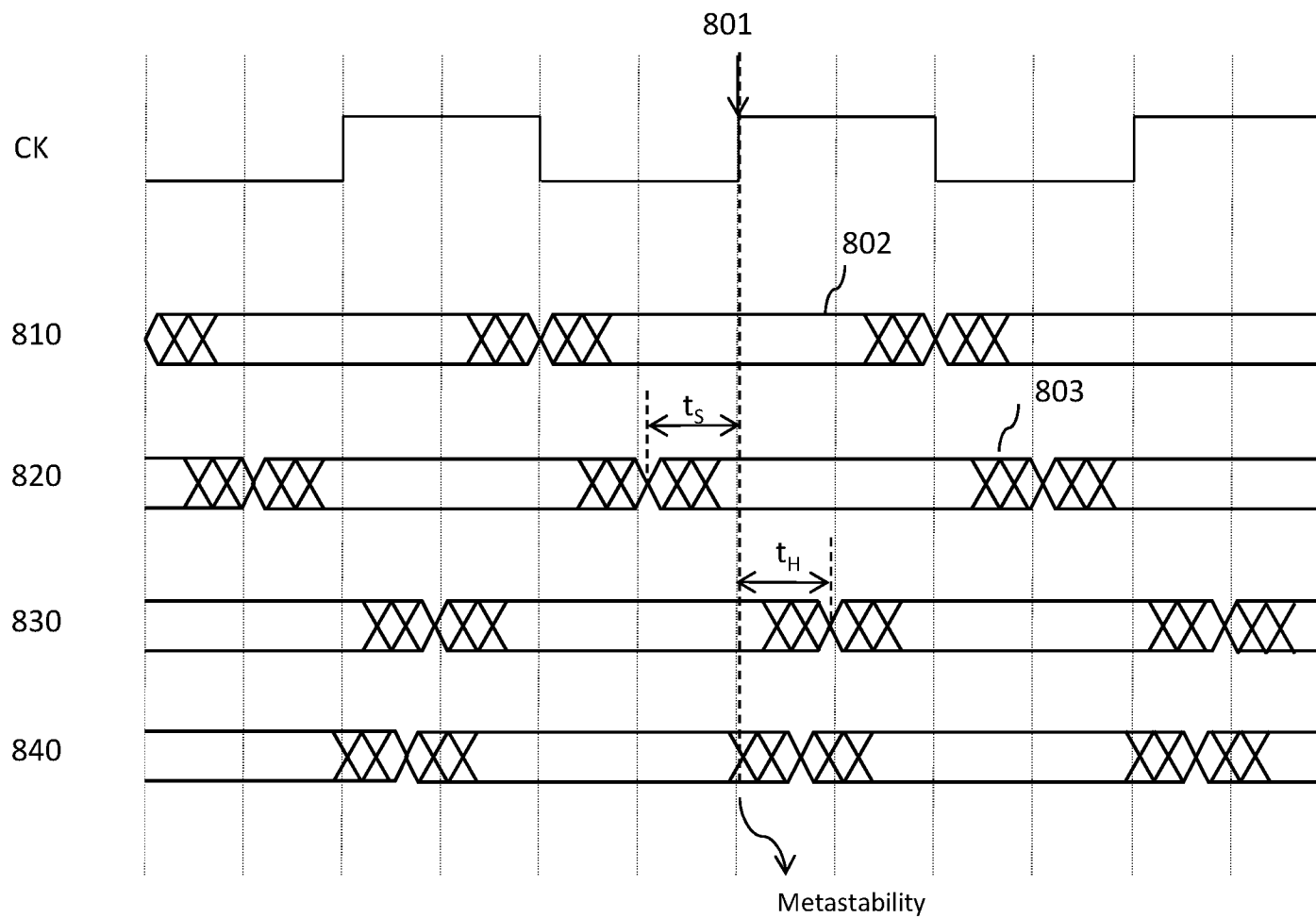
**FIG. 4A**

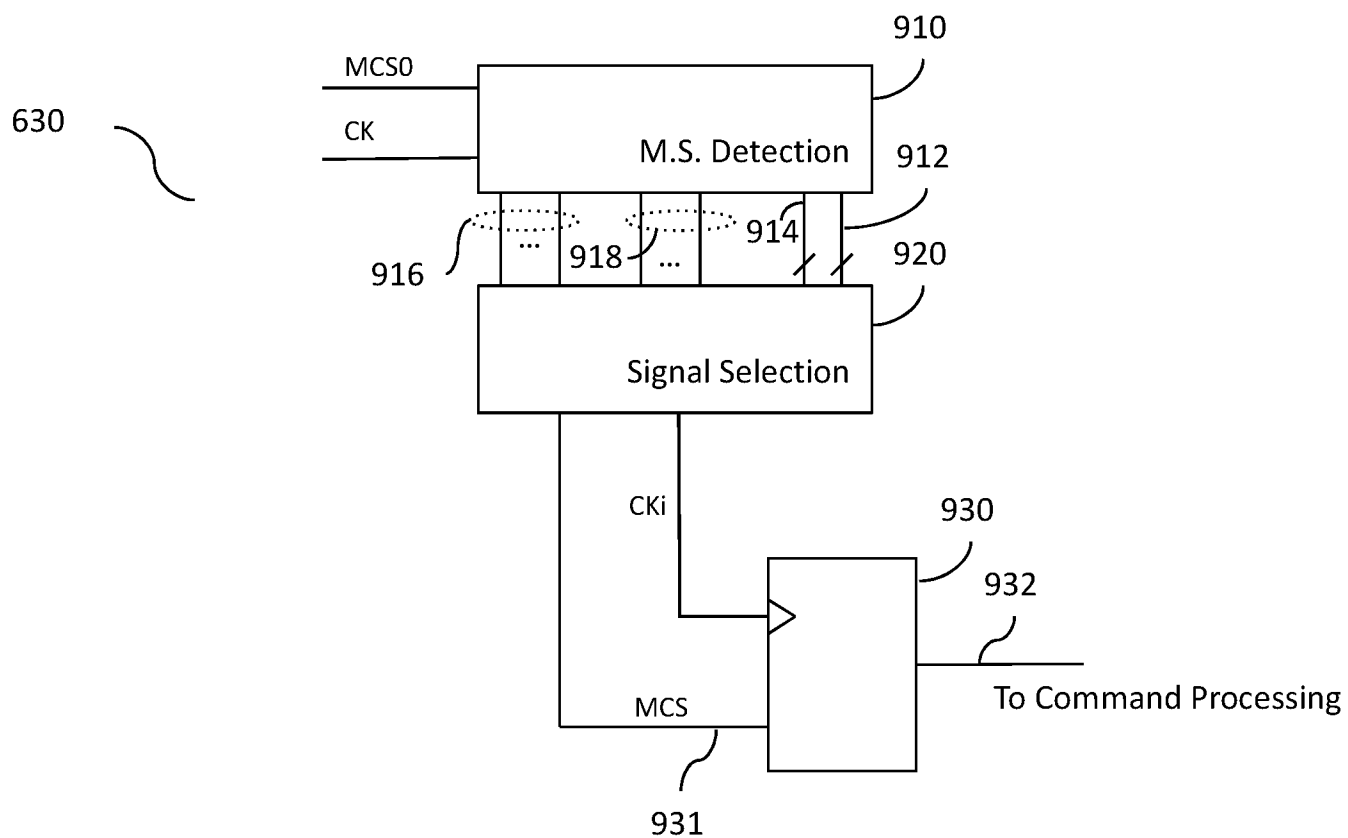
**FIG. 4B**

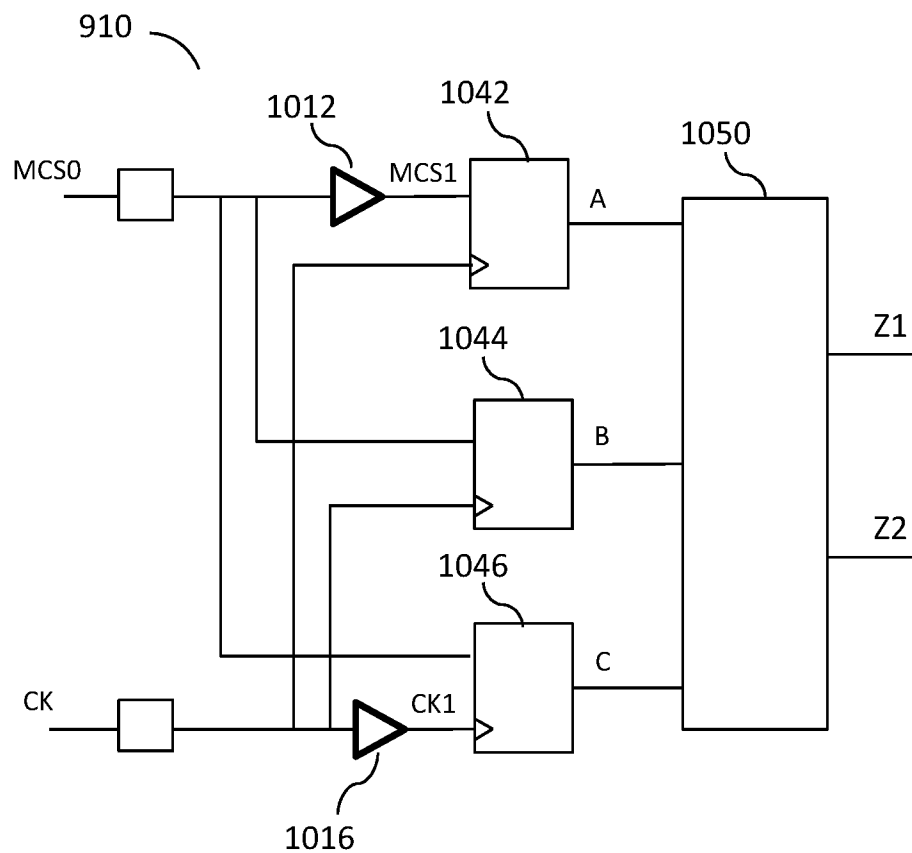
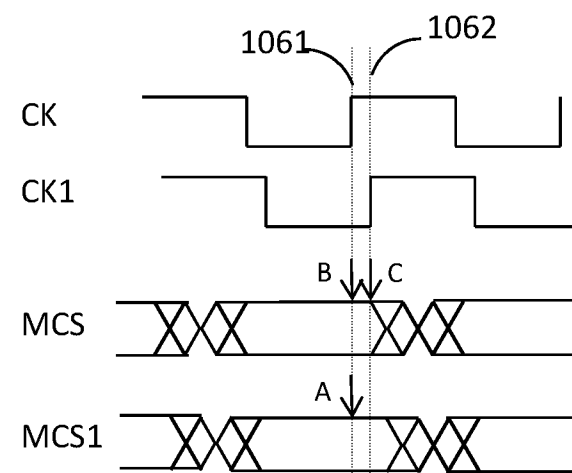
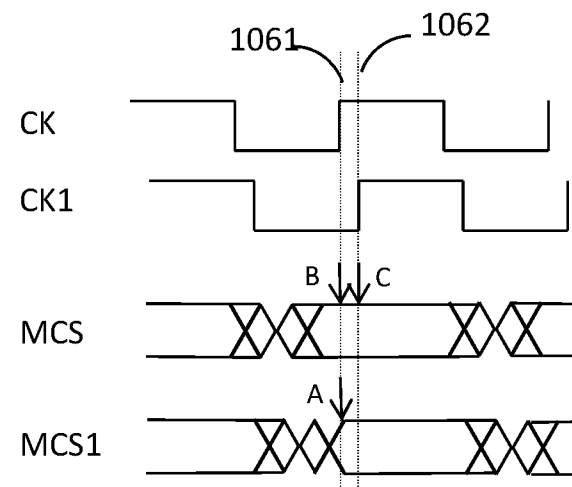
**FIG. 5B****FIG. 5A**

**FIG. 6**

**FIG. 7**

**FIG. 8**

**FIG. 9**

**FIG. 10A****FIG. 10B****FIG. 10C**

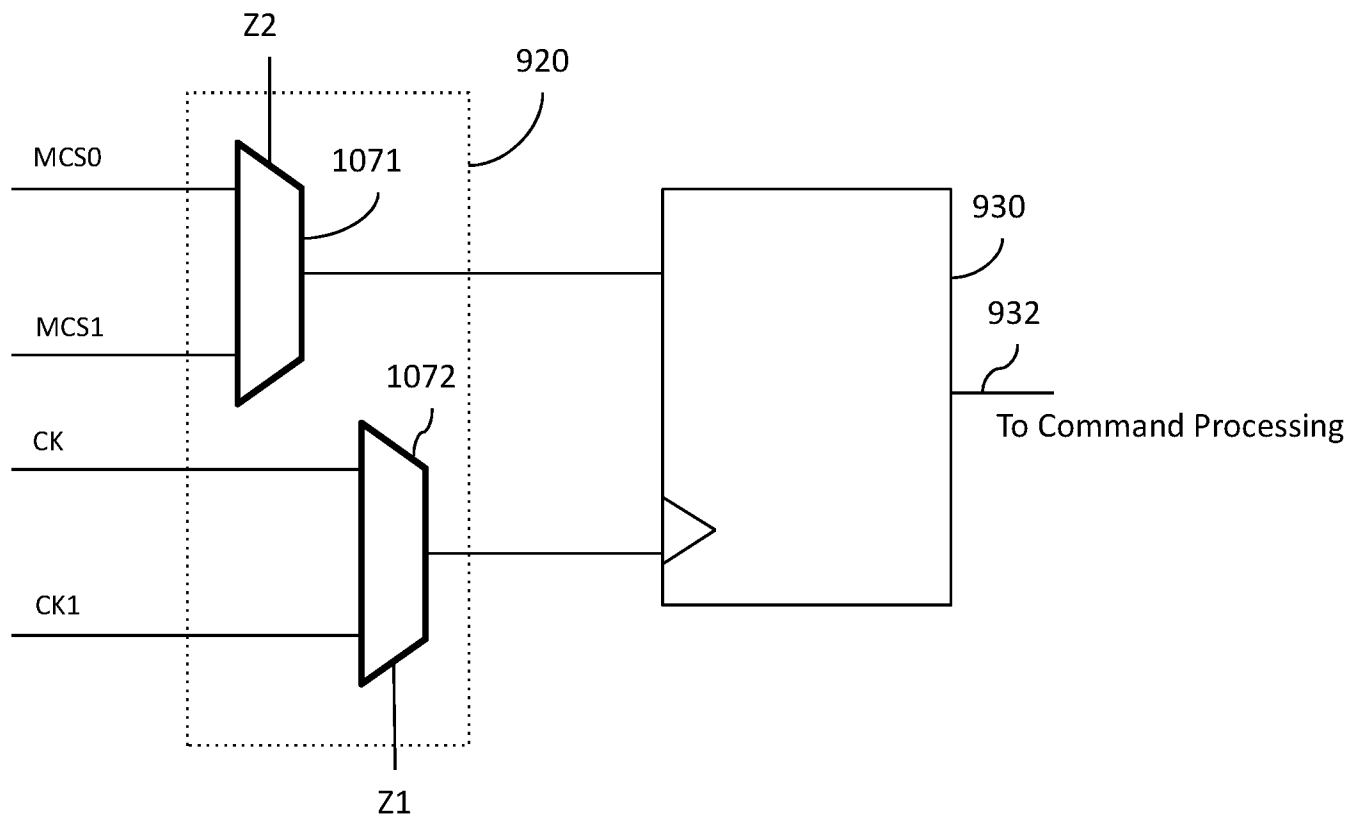


FIG. 10D

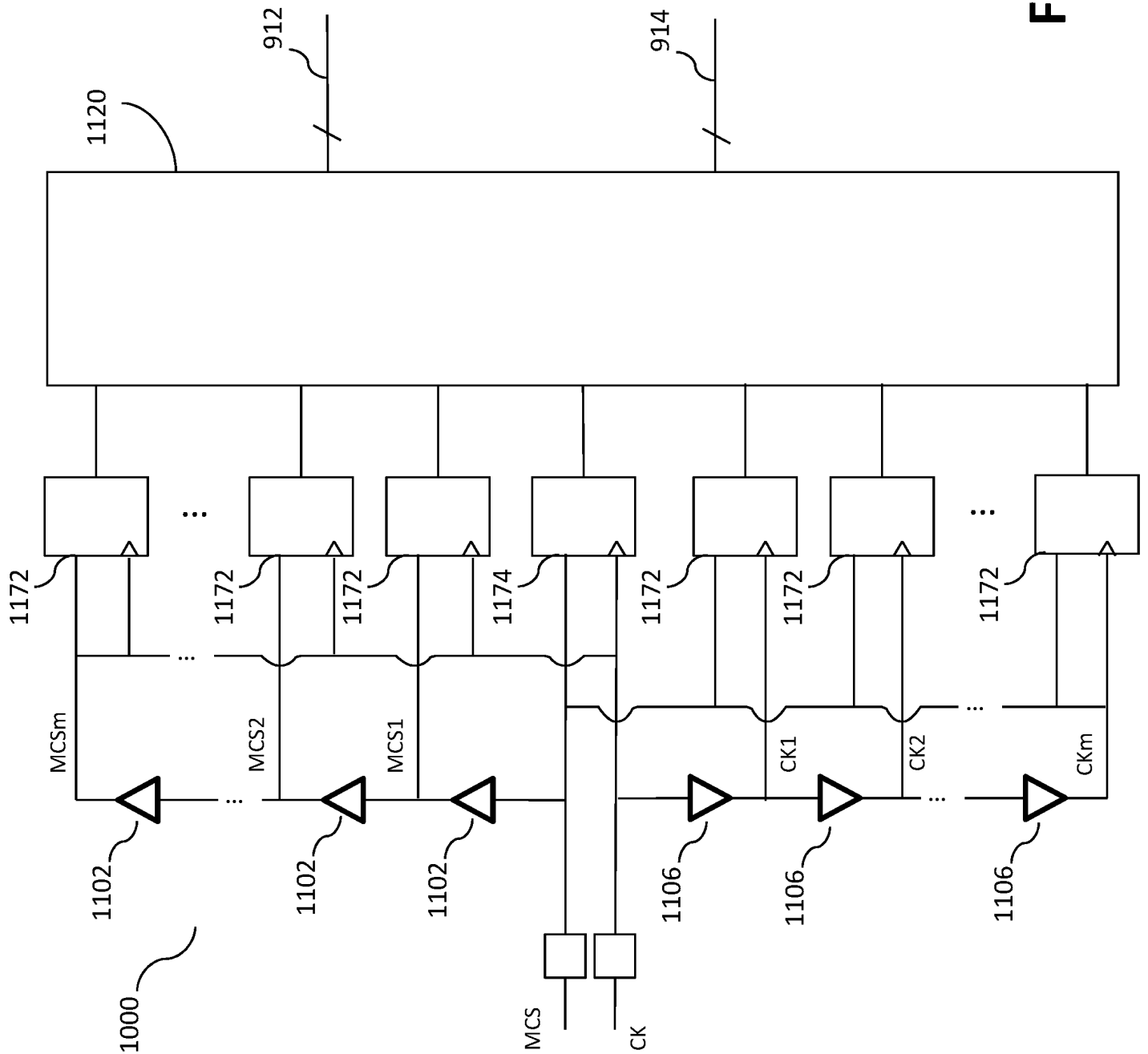
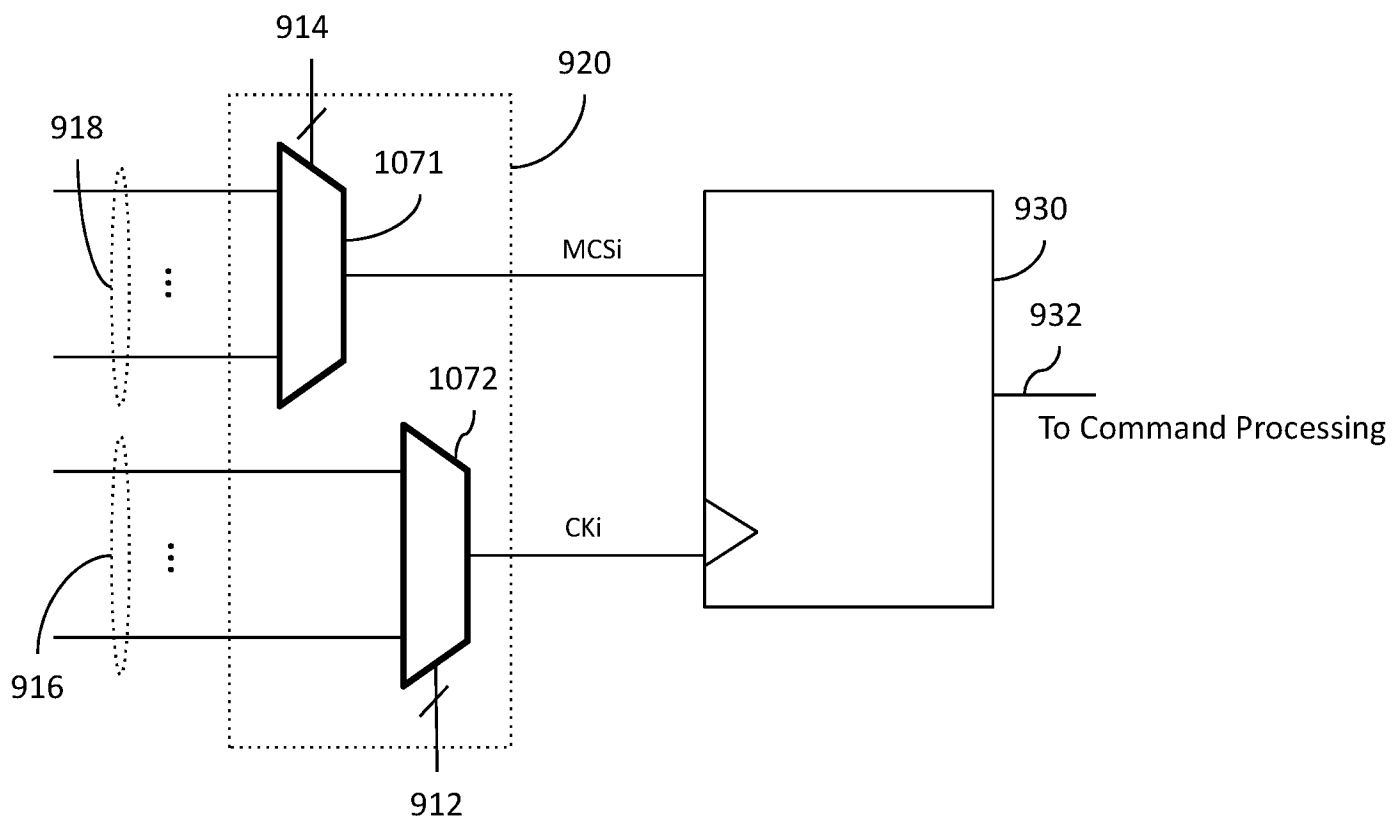
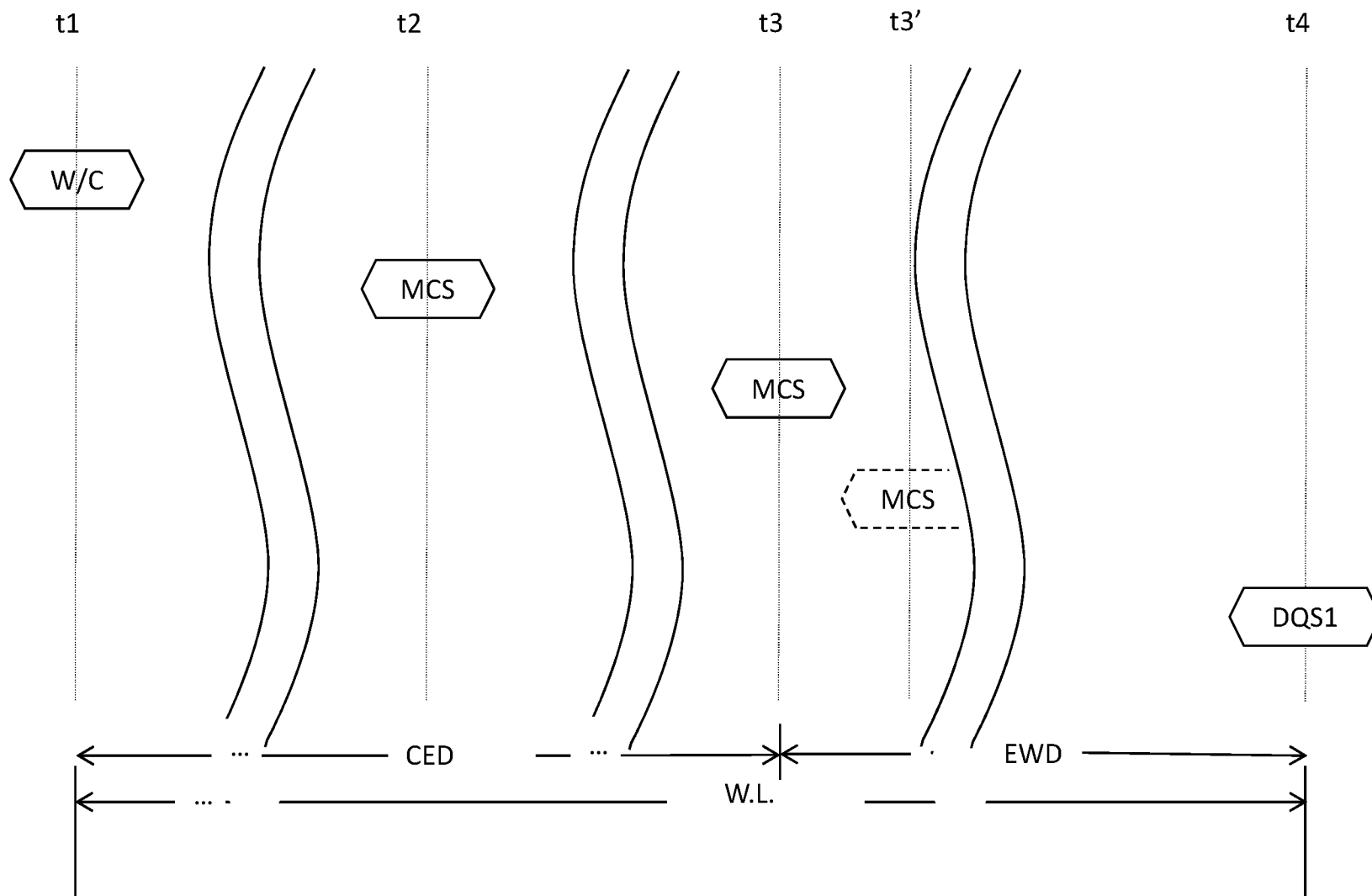
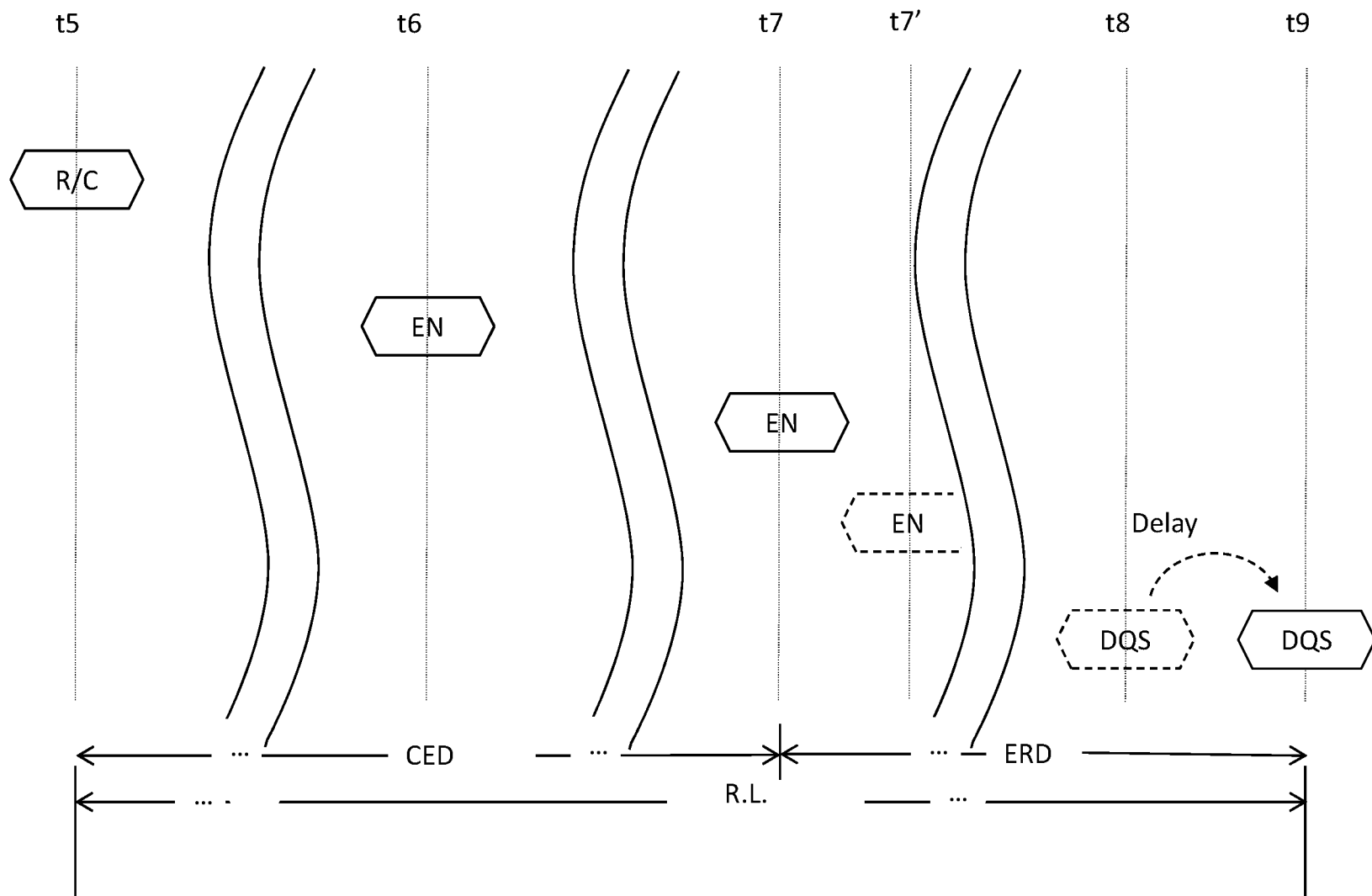
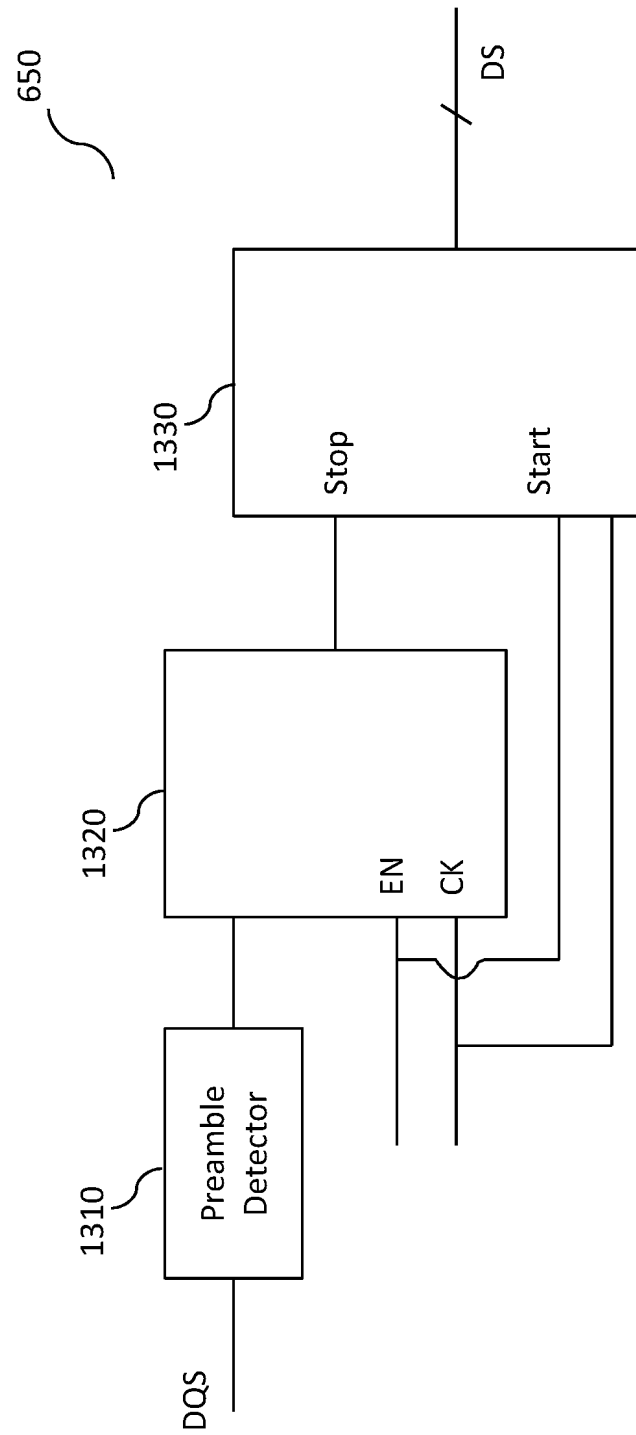


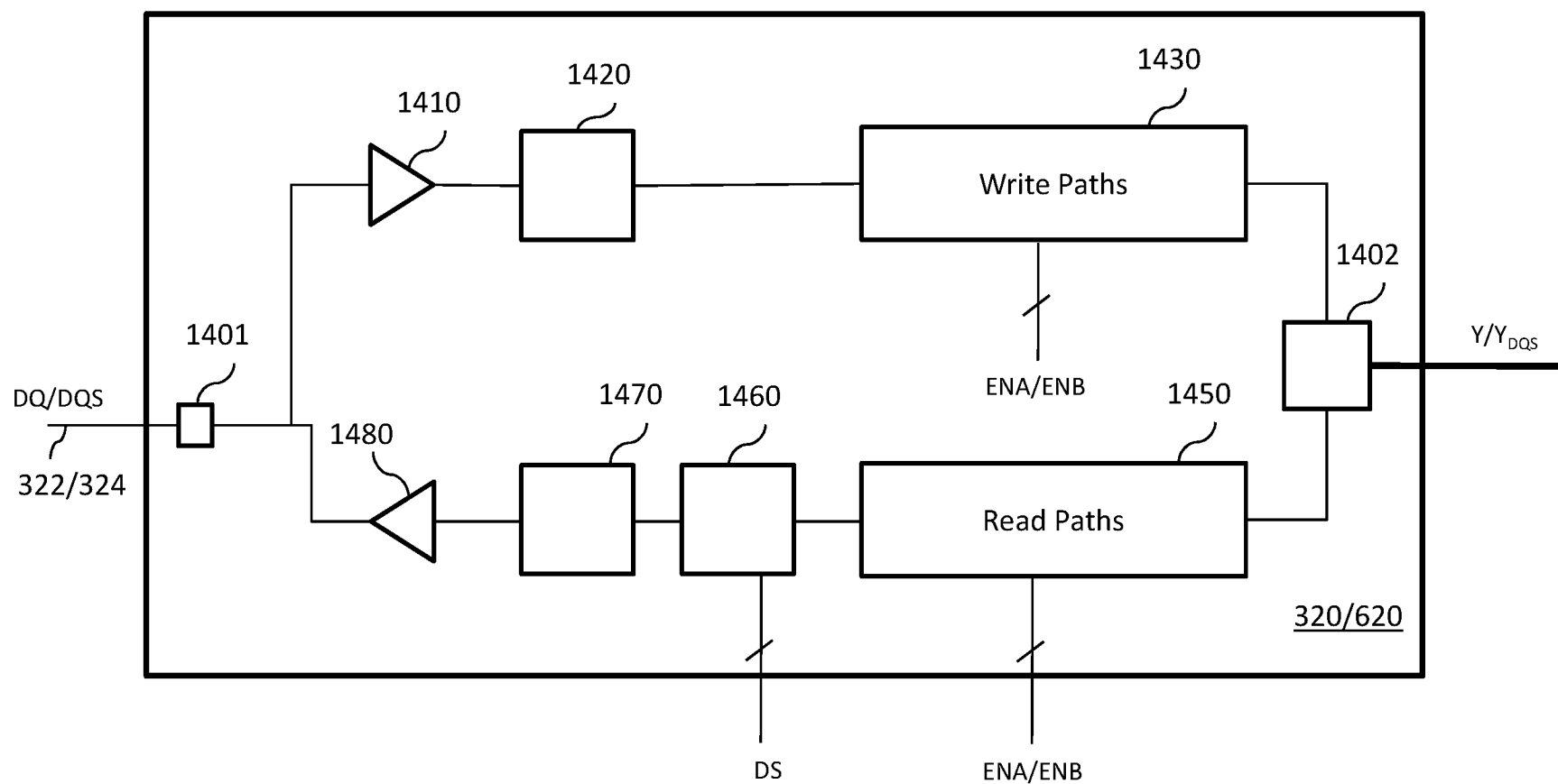
FIG. 11A

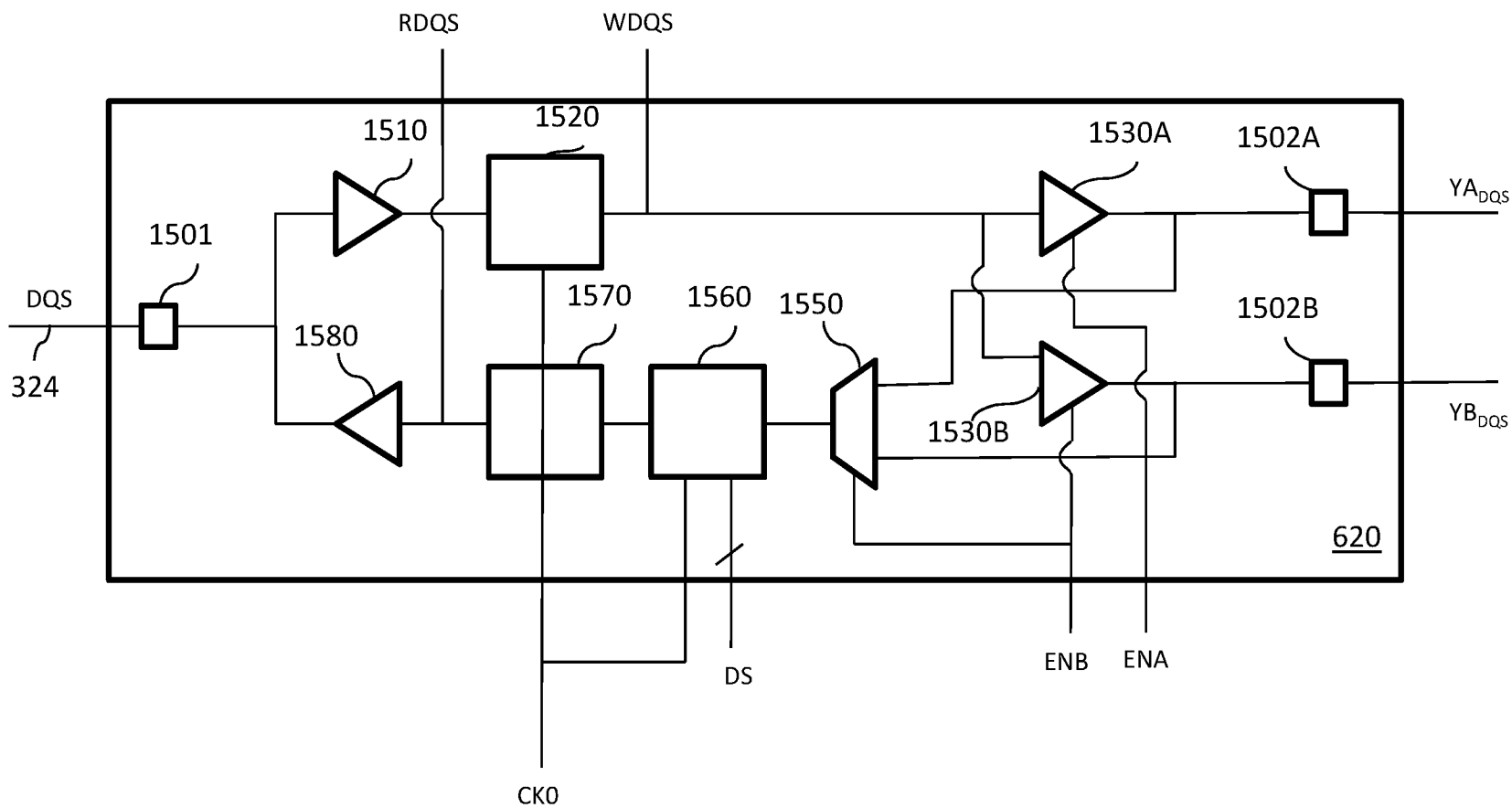
**FIG. 11B**

**FIG. 12A**

**FIG. 12B**

**FIG. 13**

**FIG. 14**

**FIG. 15**

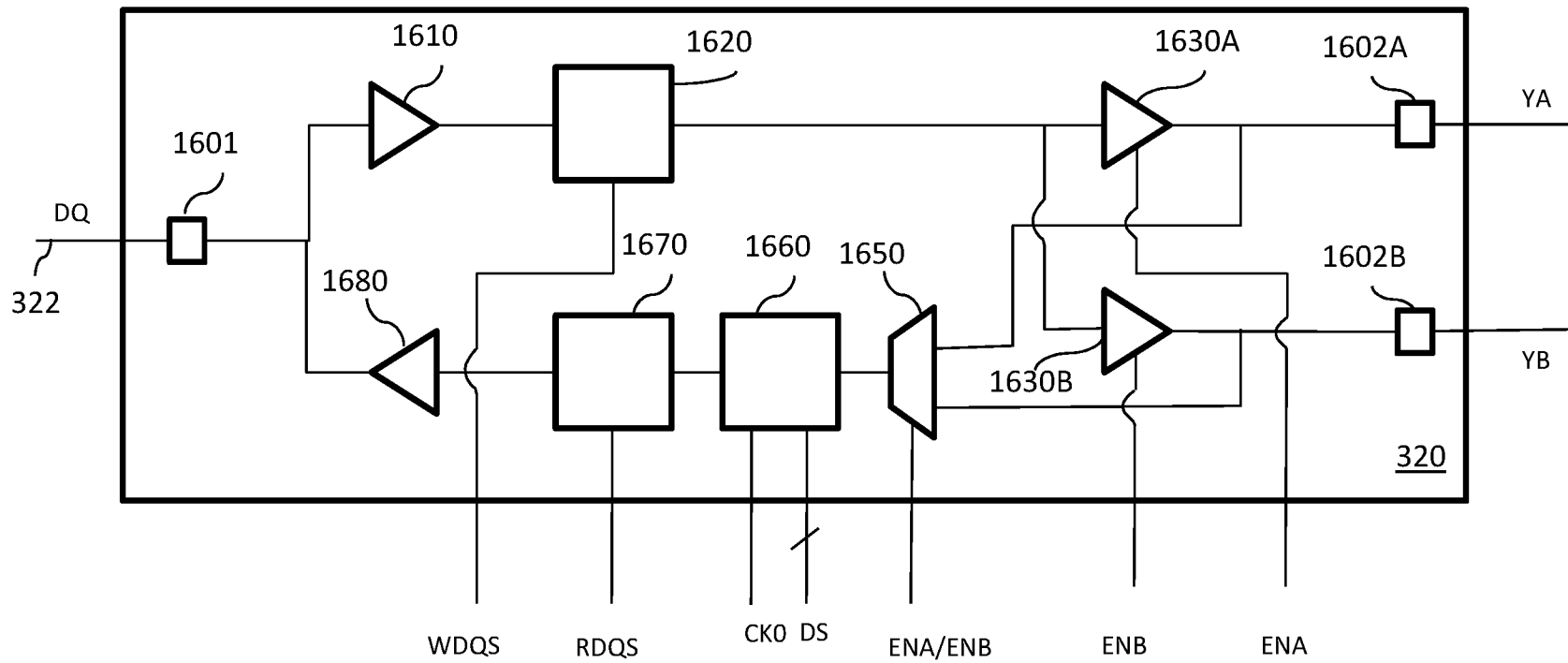
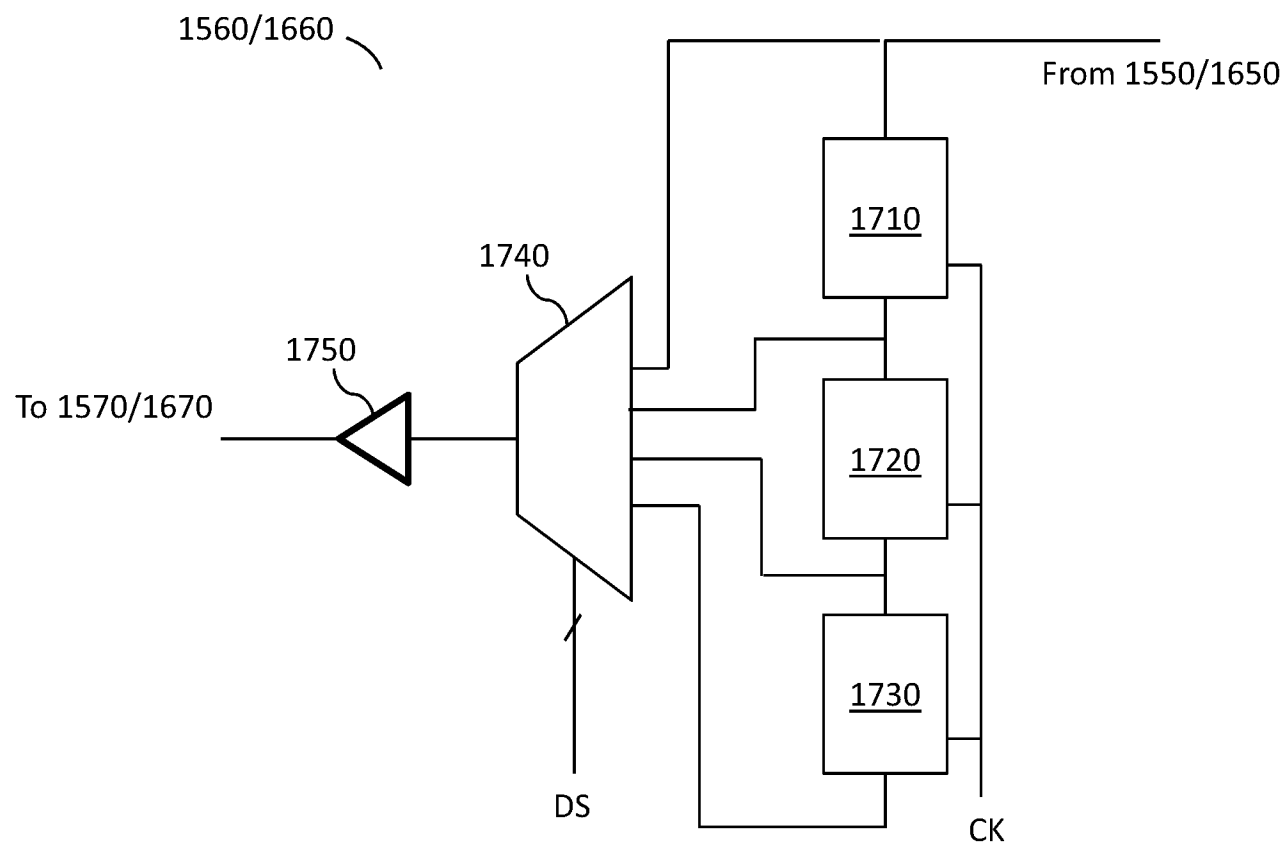
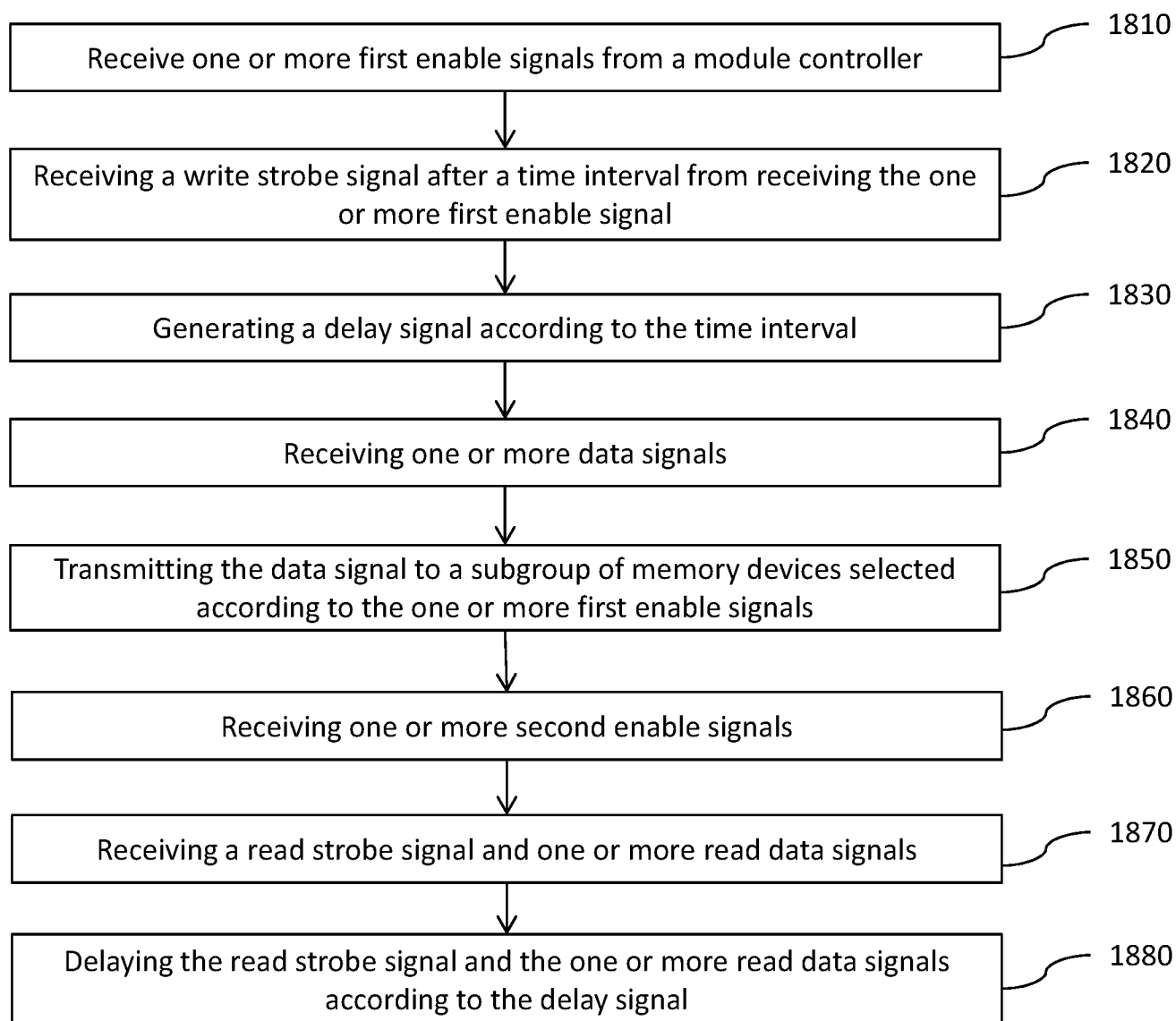
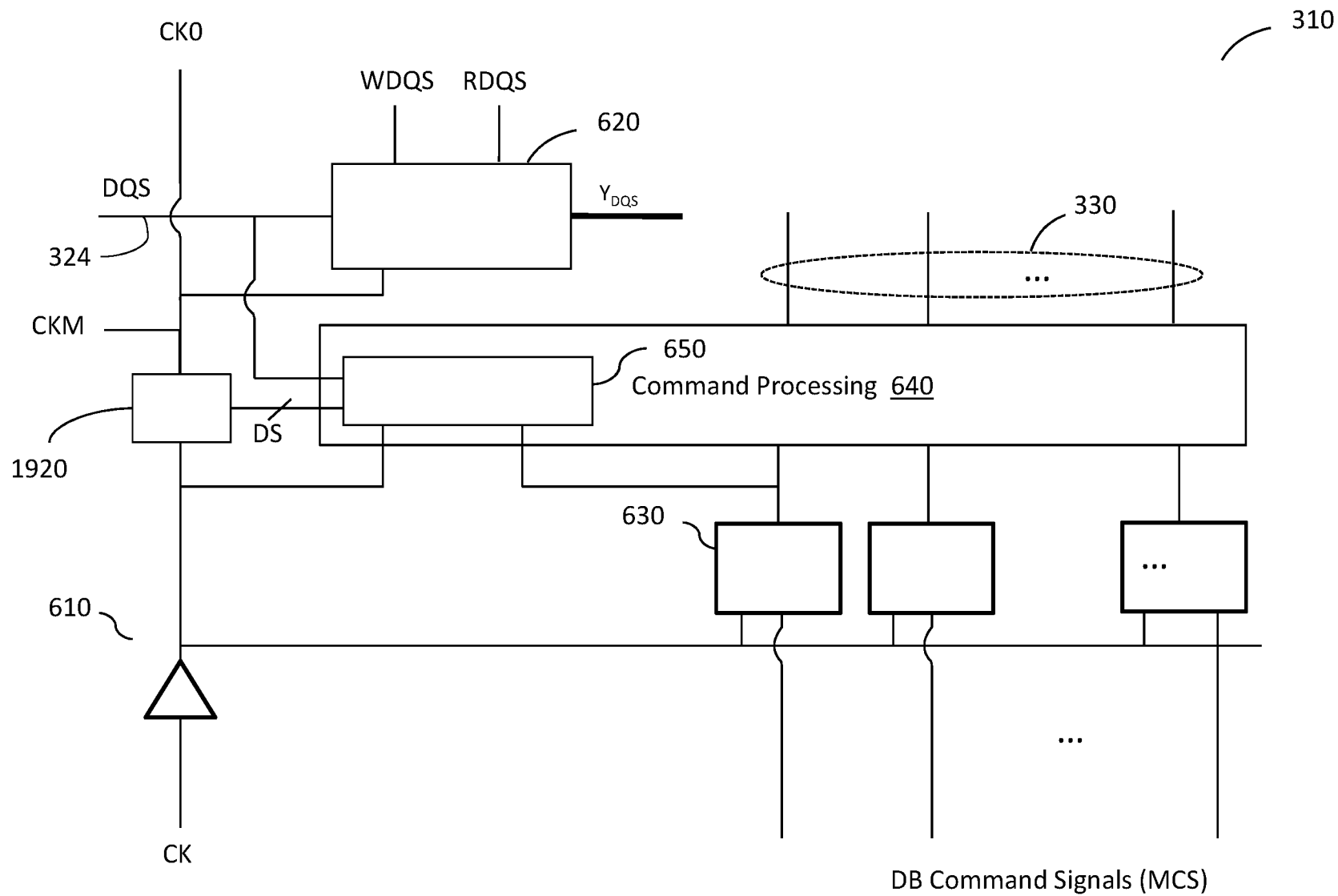


FIG. 16

**FIG. 17**

**FIG. 18**

**FIG. 19**

Electronic Acknowledgement Receipt

EFS ID:	35796399
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	22-APR-2019
Filing Date:	
Time Stamp:	19:48:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	129980_5049US01_Transmittal.pdf	146751 b07378eaaee50fe0cd8049d9c983bdba0057773	no	1

Warnings:

Micron Technology Inc. et al.

Ex. 1052, p. 73

Information:					
2		129980_5049US01_STMT_POA.pdf	122625	yes	2
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Assignee showing of ownership per 37 CFR 3.73		1	1	
	Power of Attorney		2	2	
Warnings:					
Information:					
3	Oath or Declaration filed	129980_5049US01_Decl.pdf	100992	no	2
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Warnings:					
Information:					
4	Application Data Sheet	129980_5049US01_ADS.pdf	1823366	no	9
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Warnings:					
Information:					
5		129980_5049US01_APPLN.pdf	246874	yes	32
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	30	
	Claims		31	31	
	Abstract		32	32	
Warnings:					
Information:					
6	Drawings-only black and white line drawings	129980_5049US01_DRWGS.pdf	629318	no	26
			b49f146ecd420958233792a59c3d860df4239ebf		
Micron Technology Inc. et al.					

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Information:**Total Files Size (in bytes):**

3069926

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01

CONFIRMATION NO. 3694

FORMALITIES LETTER



OC000000107883732

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Date Mailed: 05/06/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ 300 basic filing fee.
- \$ 160 surcharge.
- \$ 660 search fee.
- \$ 760 examination fee.
- \$(0) previous unapplied payment amount.
- \$ 1880 TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ytdemisse/

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/391,151				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(j))	1	minus 20 = *			OR	x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/391,151	04/22/2019	2139	0.00	129980-5049-US01	1	1

CONFIRMATION NO. 3694

79141

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FILING RECEIPT



0000000107883731

Date Mailed: 05/06/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/820,076 11/21/2017 PAT 10268608
which is a CON of 15/426,064 02/07/2017 PAT 9824035
which is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/02/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/391,151**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
Title

MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2139
Filed:	April 22, 2019	Examiner:	TBD
For:	Memory Module With Timing- Controlled Data Buffering	Attorney Docket No:	129980-5049-US01

**RESPONSE TO THE NOTICE TO FILE MISSING PARTS
OF NONPROVISIONAL APPLICATION**

Mail Stop: MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts mailed May 6, 2019, enclosed is the Notice to File Missing Parts of Nonprovisional Application for the above-identified application. The fee for the late filing fee surcharge is estimated to be \$160.

Also enclosed please find a Fee Transmittal Form setting forth the calculation for the statutory basic filing, search and examination fees, together with the excess claim fees due in this matter. The fees calculated for the statutory basic filing, search and examination fees together with the excess claim fees and application size fee (if applicable) are estimated to be \$1720.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

Respectfully submitted,

Date: August 6, 2019

/ Jamie J. Zheng / 51,167
Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01

CONFIRMATION NO. 3694

FORMALITIES LETTER



OC000000107883732

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Date Mailed: 05/06/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ 300 basic filing fee.
- \$ 160 surcharge.
- \$ 660 search fee.
- \$ 760 examination fee.
- \$(0) previous unapplied payment amount.
- \$ 1880 TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ytdemisse/

UTILITY PATENT APPLICATION FEE TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR § 1.53(b))</i>	Attorney Docket No.		129980-5094-US01
	First Inventor		Hyun Lee
	Title		Memory Module With Timing-Controlled Data Buffering
	Electronically filed		August 6, 2019

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BASIC FILING, SEARCH AND EXAMINATION FEES

Application Type	Filing Fees	Search Fees	Examination Fees	Fees Paid (\$)
Utility	\$ 300	\$ 660	\$ 760	\$ 1720

EXCESS CLAIM FEES

Type	No. Filed	Less	Extra	Extra Rate (\$)	Fee (\$)
Total Claims	1	- 20	0	\$ 100 each	0
Independent	1	- 3	0	\$ 460 each	0
Surcharge for late filing fee					160

APPLICATION SIZE FEE (Specification and Drawings)

Total Sheets	Extra Sheets	No. of each add'l 50 or fraction thereof	Fee (\$)
58 x .75- 100	0 / 50	0 (round up to whole no.) x \$400	0

Sub Total	1880
Applicant qualifies for the 50% Reduction for Independent Inventor, Nonprofit Organization or Small Business Concern minus electronic filing discount of \$75	
TOTAL FILING FEE	1880

Please charge the total filing fee and any other additional fees to Morgan, Lewis & Bockius LLP Deposit Account 50-0310 (order no. 129980-5049-US01).

Respectfully submitted,

Date: August 6, 2019

/ Jamie J. Zheng /

Jamie J. Zheng
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

51,167
(Reg. No.)

Electronic Patent Application Fee Transmittal

Application Number:	16391151			
Filing Date:	22-Apr-2019			
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING			
First Named Inventor/Applicant Name:	Hyun Lee			
Filer:	Jamie Jie Zheng/S. Olivier			
Attorney Docket Number:	129980-5049-US01			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Micron Technology Inc. et al.

Ex. 1052, p. 87

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	1251	1	200	200
Miscellaneous:				
Total in USD (\$)				2080

Electronic Acknowledgement Receipt

EFS ID:	36802308
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	06-AUG-2019
Filing Date:	22-APR-2019
Time Stamp:	19:43:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$2080
RAM confirmation Number	E201986J44069487
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Micron Technology Inc. et al.

Ex. 1052, p. 89

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5049US01_RESPONSE.pdf	251554	yes	4
			c30d21ef7b142b4662261e5a9ccd50093bb1b5f0		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Response to Pre-Exam Formalities Notice		1	3	
	Fee Worksheet (SB06)		4	4	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	39317	no	2
			7c7cc0d63f0cbda19e3301cc78578129352c12bb		
Warnings:					
Information:					
Total Files Size (in bytes):			290871		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/391,151	04/22/2019	2139	1880	129980-5049-US01	1	1

CONFIRMATION NO. 3694

UPDATED FILING RECEIPT

79141

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304



Date Mailed: 08/09/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/820,076 11/21/2017 PAT 10268608
which is a CON of 15/426,064 02/07/2017 PAT 9824035
which is a CON of 14/846,993 09/07/2015 PAT 9563587
which is a CON of 13/952,599 07/27/2013 PAT 9128632
which claims benefit of 61/676,883 07/27/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/02/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/391,151**

Projected Publication Date: 11/14/2019

Non-Publication Request: No

Early Publication Request: No
Title

MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/391,151				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(j))	1	minus 20 = *			OR	x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2184	
				Examiner Name	To be assigned	
Sheet	1	of	7	Attorney Docket Number		129980-5049US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,381,140 B1	04-30-2002	Liao	
		6,754,746 B1	06-22-2004	Leung et al.	
		6,799,252 B1	09-28-2004	Bauman	
		7,254,036 B2	08-07-2007	Pauley et al.	
		7,464,225 B2	12-09-2008	Tsern	
		7,884,619 B1	02-08-2011	Chong et al.	
		8,214,616 B2	07-03-2012	Ware et al.	
		8,565,033 B1	10-22-2013	Manochararajah et al.	
		8,949,519 B2	02-03-2015	Rajan et al.	
		2002/0038405 A1	03-28-2002	Leddige et al.	
		2002/0039323 A1	04-04-2002	Tokutome et al.	
		2004/0105292 A1	06-03-2004	Matsui	
		2006/0077731 A1	04-13-2006	Ware et al.	
		2007/0064462 A1	03-22-2007	Matsui	
		2007/0217559 A1	09-20-2007	Stott et al.	
		2008/0037412 A1	02-14-2008	Geile et al.	
		2008/0162790 A1	07-03-2008	IM	
		2009/0198924 A1	08-06-2009	Shaeffer et al.	
		2009/0248969 A1	10-01-2009	Wu et al.	
		2009/0296503 A1	12-03-2009	Chu et al.	
		2010/0125681 A1	05-20-2010	Patel	
		2010/0228891 A1	09-09-2010	Talbot	
		2010/0271092 A1	10-28-2010	Zerbe et al.	
		2011/0085408 A1	04-14-2011	Neubauer	
		2012/0256639 A1	10-11-2012	Pausini et al.	
		2014/0029370 A1	01-30-2014	Koshizuka	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code - Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		CN102576565B	09-30-2015	Netlist, Inc.		
		WO 99/30240	06-17-1999	Intel Corporation		

NON PATENT LITERATURE DOCUMENTS

Examiner Signature		Date Considered	
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DB2/ 37149841.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2184	
				Examiner Name	To be assigned	
Sheet	2	of	7	Attorney Docket Number		129980-5049US01

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Lee, Office Action, US15/426,064, 02JUN2017, 11 pgs.
		Lee, Notice of Allowance, US15/426,064, 21SEP2017, 9 pgs.
		Lee, Notice of Allowance, US14/846,993, 23SEP2016, 8 pgs.
		Lee, Office Action, US13/952,599, 31JUL2014, 12 pgs.
		Lee, Notice of Allowance, US13/952,599, 23APR2015, 8 pgs.
		Lee, Notice of Allowance, US15/820,076, 03JUL2018, 9 pgs.
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Objections to Evidence, filed February 29, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Reply, filed May 19, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Response to Motion for Observations, filed June 10, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Response to Netlist1s Submission, filed June 13, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s Objections to Petitioner1s Demonstrative Exhibits, filed June 23, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s Demonstrative Exhibits, filed June 24, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Updated Exhibit List, filed June 24, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016

Examiner Signature		Date Considered	
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DB2/ 37149841.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	To be assigned
Sheet	3	of	7	Attorney Docket Number	129980-5049US01

		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Demonstrative Exhibits, filed June 24, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.Don February 12, 2016," filed February 22, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.Don April 20, 2015," filed February 22, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Objections to Evidence, filed February 29, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Reply, filed May 19, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner1s SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Response to Motion for Observations, filed June 10, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Response to Patent Owner1s Submission, filed June 13, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner1s Objections to Petitioner1s Demonstrative Exhibits, filed June 23, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner1s Demonstrative Exhibits, filed June 24, 2016

Examiner Signature		Date Considered	
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DB2/ 37149841.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2184	
				Examiner Name	To be assigned	
Sheet	4	of	7	Attorney Docket Number		129980-5049US01

		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
		International Search Report and Written Opinion, International Application No. PCT/US14/48517, filed July 28, 2014, dated October 27, 2014
		Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.
		Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.
		Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.
		Examination Report, European Patent Application No. 10730021.2, dated April 14, 2014.
		Response to Examination Report, European Patent Application No. 10730021.2, dated June 4, 2014.
		Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015.
		Response to Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015, filed November 4, 2015.
		English Translation of the Notice of Grounds for Rejection, Korean Patent Application No. 2012-7004038, dated May 11, 2016
		Notice of Allowance, U.S. Pat. Appl. No. 13/970,606, filed August 20, 2013, dated June 27, 2016
		Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated November 23, 2015
		Response to Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated March 23, 2016
		Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015

Examiner Signature		Date Considered	
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DB2/ 37149841.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2184
Sheet	5	of	7	Examiner Name	To be assigned
				Attorney Docket Number	129980-5049US01

		Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015
		Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
		Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8, 2015
		Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8, 2015
		Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002
		Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10
		U.S. District Court Northern District of California, Case No. 4:13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages
		Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411
		Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265
		Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid
		Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&searchBin=Search
		Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015

Examiner Signature		Date Considered	
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DB2/ 37149841.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2184	
				Examiner Name	To be assigned	
Sheet	6	of	7	Attorney Docket Number		129980-5049US01

		Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015
		Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.

Examiner Signature		Date Considered	
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DB2/ 37149841.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	To be assigned
Sheet	7	of	7	Attorney Docket Number	129980-5049US01

		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, Conduct of the Proceedings, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed August 6, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018

Examiner Signature		Date Considered	
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Electronic Acknowledgement Receipt

EFS ID:	36931637
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lamesha Robertson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	20-AUG-2019
Filing Date:	22-APR-2019
Time Stamp:	21:00:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5049US01_IDS.pdf	992807	yes	11
			0a102c4d5bd400830280e542059c0301589203da		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	4
	Information Disclosure Statement (IDS) Form (SB08)	5	11
Warnings:			
Information:			
Total Files Size (in bytes):		992807	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2184
Filed:	April 22, 2019	Examiner:	To be assigned
For:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING	Attorney Docket No.:	129980-5049US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:
 - 1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.
 - 1b. A legible copy of:
 - ☐ Each foreign patent;
 - ☐ Each publication or that portion which caused it to be listed on the PTO-1449;
 - ☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;
 - ☐ all other information or portion which caused it to be listed on the PTO-1449.
 - 1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.
 - 1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):
- ☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);
 - ☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;
 - ☒ Before the mailing of the first Office action on the merits;
 - ☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.
3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

- 3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.
- 3b. ☐ The \$240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 3c. ☐ The \$120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 3d. ☐ The \$60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

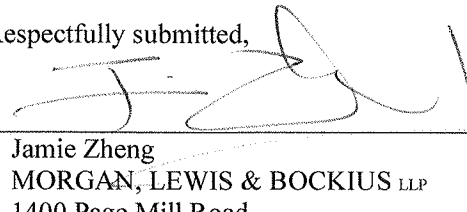
- 4a. ☐ The Certification Statement in Item 5 below is applicable.
- 4b. ☐ The \$240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 4c. ☐ The \$120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 4d. ☐ The \$60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)
- (Check either Item 5a, 5b, 5c or 5d)*
- 5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.
- 5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.
- 5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.
- 5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.
6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.
7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).
- (Check appropriate Items 7a, 7b and/or 7c)*
- 7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.
- 7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/820,076, filed on November 21, 2017, 15/426,064, filed on February 7, 2017, 14/846,993, filed on September 7, 2015, and 13/952,599, filed on July 27, 2013, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).
- 7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.
8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

- 8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .
9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:
- (Check Item 9a, 9b, or 9c)*
- 9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.
- 9b. ☐ set forth in the application.
- 9c. ☐ enclosed as an attachment hereto.
10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049US01).
11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 20, 2019



Jamie Zheng
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

51,167
(Reg. No.)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01

CONFIRMATION NO. 3694

PUBLICATION NOTICE



OC000000112625372

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Title:MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

Publication No.US-2019-0347220-A1

Publication Date:11/14/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020		
				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2183	
				Examiner Name	Sun, Michael	
Sheet	1	of	22	Attorney Docket Number		129980-5049US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code			
		RE36,229	1999-06-01	Cady	
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DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	2	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	3	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	4	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	5	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	6	of	22	Attorney Docket Number	129980-5049US01

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DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	7	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	8	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2183	
				Examiner Name	Sun, Michael	
Sheet	9	of	22	Attorney Docket Number		129980-5049US01

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				Application Number	16/391,151
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				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	10	of	22	Attorney Docket Number	129980-5049US01

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				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	11	of	22	Attorney Docket Number	129980-5049US01

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DB2/ 22684197.4

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				Examiner Name	Sun, Michael
Sheet	12	of	22	Attorney Docket Number	129980-5049US01

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				Examiner Name	Sun, Michael
Sheet	13	of	22	Attorney Docket Number	129980-5049US01

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				Art Unit	2183
Sheet	14	of	22	Examiner Name	Sun, Michael
				Attorney Docket Number	129980-5049US01

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Sheet	15	of	22	Attorney Docket Number	129980-5049US01

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Sheet	16	of	22	Attorney Docket Number	129980-5049US01

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Sheet	17	of	22	Attorney Docket Number	129980-5049US01

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Examiner Signature		Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	18	of	22	Attorney Docket Number	129980-5049US01

		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Complaint For Patent Infringement, filed Sept. 22, 2009 in 10 pages.
		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages.
		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's First Amended Complaint for Patent Infringement, filed Feb. 11, 2010 in 9 pages.
		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Notice of Motion and Motion for Stay Pending Reexaminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages.
		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages.
		U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Plaintiff Netlist, Inc's First Amended Complaint For Patent Infringement, filed Dec. 23, 2009 in 8 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Claim Construction Reply Brief, filed Sept. 22, 2009 in 19 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Opening Claim Construction Brief, filed July 28, 2009 in 21 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, Inc.'s Opposition to Google Inc's Motion for Summary Judgment of Invalidity, filed July 6, 2010 in 13 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit A To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 2 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit B to Joint Claim Construction and Prehearing Statement, filed June 12, 2009 in 36 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Joint Claim Construction and Prehearing Statement, filed June 12, 2009 in 5 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Netlist, Inc.'s Answer to Complaint and Counterclaims, filed Nov. 18, 2008 in 9 pages.

Examiner Signature		Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
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				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	19	of	22	Attorney Docket Number	129980-5049US01

		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Order Re Claim Construction, filed Nov. 16, 2009 in 1 page.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Plaintiff Google's Reply to Counterclaims, filed Dec. 8, 2008 in 4 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Stipulation Re: Additional Agreed-Upon Claim Constructions, filed Oct. 28, 2009 in 3 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., [Redacted] Google Inc.'s Responsive Claim Construction Brief, filed Aug. 25, 2009 in 30 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Amended Exhibit A To Joint Claim Construction And Prehearing Statement, filed Oct. 28, 2009 in 1 page.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Appendix 1 To Google's Responsive Claim Construction Brief, filed Nov. 12, 2009 in 4 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 1 to Exhibit B To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 7 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 2 To Exhibit B To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 12 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Complaint for Declaratory Relief, filed Aug. 29, 2008 in 49 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Complaint For Patent Infringement, filed Dec. 4, 2009 in 47 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, NETLIST, INC. vs. GOOGLE, INC., Defendant Google Inc's Responsive Claim Construction Brief, filed Aug. 4, 2010 in 108 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Exhibit A to Joint Claim Construction and Prehearing Statement under Patent L. R. 4-3, filed June 25, 2010 in 2 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Exhibit B to Joint Claim Construction and Prehearing Statement under Patent L. R. 4-3, filed Jun. 25, 2010 in 23 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Google's Answer to Plaintiff's Complaint for Patent Infringement; and Assertion of Counterclaims, filed Feb. 12, 2010 in 13 pages.

Examiner Signature		Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020		
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				First Named Inventor	Hyun Lee	
				Art Unit	2183	
				Examiner Name	Sun, Michael	
Sheet	20	of	22	Attorney Docket Number		129980-5049US01

		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Joint Claim Construction And Prehearing Statement Under Patent Local Rule 4-3, filed June 25, 2010 in 5 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc.'s Reply Claim Construction Brief, filed Aug. 16, 2010 in 17 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc.'s Reply to Defendant Google Inc.'s Counterclaim, filed March 8, 2010 in 11 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc.'s Opening Claim Construction Brief, filed Jul. 16, 2010 in 162 pages.
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		Vogt, Pete, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity," Intel, Feb. 18, 2004, 33 pages.
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, Conduct of the Proceedings, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed August 6, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	21	of	22	Attorney Docket Number	129980-5049US01

		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 14, 'Patent Owner's Response,' filed October,19,2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February,11,2019
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 19, 'Petitioners' Request for Oral Argument,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 21, 'Patent Owner Objections To Reply Evidence,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 20, 'Patent Owner Request For Oral Argument,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 22, 'Patent Owner Motion To Exclude,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 23, 'Corrected Petitioners' Reply to Patent Owner's Response,' filed February,20,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 28, 'Order - Trial Hearing,' filed March,22,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June,27,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June,27,2019
		Response, Article 94 3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs
		Observations by third parties, EP 18179414.0, 22FEB2019, 1 pg
		Patent Document filed by a third party, 20FEB2019, 10 pgs
		Netlist, Inc., Observations by third parties, EP 3404660, 20FEB2019, 46 pgs
		Reply to Written Opinion prepared by the EPO, EP 18179414.0, 17JAN2019, 20 pgs
		Netlist, Inc., Information on Search Strategy, EP 18179414, 23OCT2018, 1 pg
		European Search Report, EP 18179414, 23OCT2018, 3 pgs

Examiner Signature		Date Considered	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	22	of	22	Attorney Docket Number	129980-5049US01

		European Search Opinion, EP 18179414, 23OCT2018, 3 pgs
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, Conduct of the Proceedings, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed August 6, 2018
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		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING	Attorney Docket No.:	129980-5049US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:
 - 1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.
 - 1b. A legible copy of:
 - ☐ Each foreign patent;
 - ☐ Each publication or that portion which caused it to be listed on the PTO-1449;
 - ☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;
 - ☐ all other information or portion which caused it to be listed on the PTO-1449.
 - 1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.
 - 1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):
- ☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);
 - ☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;
 - ☒ Before the mailing of the first Office action on the merits;
 - ☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.
3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.
- (Check either Item 3a, 3b, 3c or 3d)*
- 3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.
- 3b. ☐ The \$240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 3c. ☐ The \$120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 3d. ☐ The \$60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.
- (Check Item 4a, and 4b, 4c or 4d)*
- 4a. ☐ The Certification Statement in Item 5 below is applicable.
- 4b. ☐ The \$240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 4c. ☐ The \$120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).
- 4d. ☐ The \$60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

- 5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.
- 5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.
- 5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.
- 5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.
6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.
7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

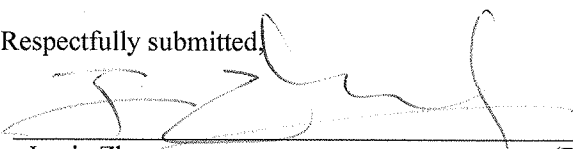
(Check appropriate Items 7a, 7b and/or 7c)

- 7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.
- 7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/820,076, filed on November 21, 2017, 15/426,064, filed on February 7, 2017, 14/846,993, filed on September 7, 2015, 13/952,599, filed on July 27, 2013, and 15/470,856, filed on March 27, 2017, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).
- 7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)
- 8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .
9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:
- (Check Item 9a, 9b, or 9c)
- 9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.
- 9b. ☐ set forth in the application.
- 9c. ☐ enclosed as an attachment hereto.
10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049US01).
11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: January 8, 2020



Jamie Zheng
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

51,167
(Reg. No.)

Electronic Acknowledgement Receipt

EFS ID:	38243637
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lamesha Robertson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	08-JAN-2020
Filing Date:	22-APR-2019
Time Stamp:	19:12:04
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5049US01_IDS.pdf	2660427	yes	26
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694
79141	7590	01/10/2020	EXAMINER	
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)			SUN, MICHAEL	
1400 Page Mill Road			ART UNIT	PAPER NUMBER
Palo Alto, CA 94304			2183	
			NOTIFICATION DATE	DELIVERY MODE
			01/10/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Continuation filed on 4/22/2019.

Claim 1 is pending for this examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 8/20/2019 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Obvious-Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van*

Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-12 of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-12 of

copending Application No. 15/820,076, now U.S. Patent No. 10,268,608, as listed below, and as such anticipate the claims of the copending application:

Claims	Instant Application	Claims	copending Application No. 15/820,076, now U.S. Patent No. 10,268,608
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal and to

	the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.		perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command
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			processing circuit in response to at least one of the module control signals.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608, and as such would be rendered obvious over the already allowed claims of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608.		

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035.

Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-22 of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035, as listed below, and as such anticipate the claims of the copending application:

Claims	Instant Application	Claims	copending Application No. 15/426,064, now U.S. Patent No. 9,824,035
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus;	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus;

	a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive		a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and memory devices mounted on the module board and configured to perform the first memory' operation in response to the module command signals, the memory devices including a plurality of sets of memory' devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the
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	the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.		module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035, and as such would be rendered obvious over the already allowed claims of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035.		

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-20 of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587, as listed below, and as such anticipate the claims of the copending application:

Claims	Instant Application	Claims	copending Application No. 14/846,993, now U.S. Patent No. 9,563,587
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of

control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of	control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board including edge connections for connecting to respective ones of the signal lines in the memory bus; memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to control the memory devices and the buffer circuits in response to the memory command signals; wherein the each respective buffer circuit is configured to respond to one or more first
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	data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.	control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation; wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing information derived from receiving the one or more first control signals and the write data/strobe signals during the write operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587, and as such would be rendered obvious over the already allowed claims of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587.	

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632.

Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-20 of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632, as listed below, and as such anticipate the claims of the copending application:

Claims	Instant Application	Claims	copending Application No. 13/952,599, now U.S. Patent No. 9,128,632
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to	Independent claim 1	A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals; memory devices organized in groups, each group including at

	the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the		least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and a plurality of buffer circuits to receive the module control signals, each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and wherein the each respective buffer circuit is configured to determine a respective time interval based on signals
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	respective set of data signals by an amount determined based on at least one of the module control signals.		received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632, and as such would be rendered obvious over the already allowed claims of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632.		

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Manohararajah et al. (US 8,565,033), herein referred to as Manohararajah ‘033.

Referring to **claim 1**, Manohararajah ‘033 teaches a memory module operable to communicate with a memory controller via a memory bus (see Fig. 2, wherein memory module 22 communicates with programmable integrated circuit 10 across buses 34 and 36 through memory interface circuitry 24 that includes a memory controller 28), the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines (see Fig. 2, wherein bus 34 is used for data / data strobe signals and bus 36 is

used for clock / address / commands), the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus (see Fig. 3, wherein the memory modules 22 includes a plurality of memory groups 52 each with respective buss 34 and 36 to connect to programmable integrated circuit 10); a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal (see Fig. 3, wherein memory interface circuitry 24 is used to connect to memory modules 22 and would include circuitry for issuing data / data strobe signals on buses 34 and clock / address / command signals across buses 36); and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines (see Figs. 3-5, wherein memory module 22 includes multiple memory groups 52 that connect to memory interface circuit 26 through buses for data / data strobe signals 34 and clock / address / command signals 36, use to perform memory operations utilizing the memory groups 52); and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each

respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals (see Figs. 4-5, I/O circuit 54, read-sync buffers 60, read-valid buffers 62; see Col. 1, lines 57-67, Col. 2, lines 1-5, wherein during read and write operations, buffering can be done to synchronize / tune / calibrate reads and writes, also see Col. 2, lines 37-47; see Col. 2, lines 52-64, wherein delays can be introduced using programmable delay chains to provide additional latency to calibrate operations to a desired tuning accuracy; also see Figs. 14-15, wherein read operations and write operations are calibrated by increasing / reducing latency).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724. The examiner can normally be reached on Monday-Friday 8am-4pm EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aimee Li can be reached on 571-272-4169. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

Art Unit:2183

applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/

Primary Examiner, Art Unit 2183

<i>Notice of References Cited</i>	Application/Control No. 16/391,151		Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner MICHAEL SUN		Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8565033-B1	10-2013	Manohararajah; Valavan	G11C29/028	365/129
*	B	US-20140029370-A1	01-2014	KOSHIZUKA; Atsuo	G11C7/1051	365/233.13
*	C	US-20060077731-A1	04-2006	Ware; Frederick A.	G11C5/04	365/194
*	D	US-20070217559-A1	09-2007	Stott; Bret G.	H04L7/0037	375/355
*	E	US-20100271092-A1	10-2010	Zerbe; Jared L.	G06F13/4243	327/161
*	F	US-8214616-B2	07-2012	Ware; Frederick A.	G06F1/06	711/167
*	G	US-8949519-B2	02-2015	Rajan; Suresh Natarajan	G11C5/02	365/189.2
*	H	US-20020039323-A1	04-2002	Tokutome, Hiroto	G11C7/1066	365/233.12
*	I	US-20080037412-A1	02-2008	Geile; Michael J.	G06F17/14	370/208
*	J	US-7884619-B1	02-2011	Chong; Yan	G01R31/3016	324/601
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.
	Examiner MICHAEL SUN	Art Unit 2183

CPC - Searched*		
Symbol	Date	Examiner
limited search of G06F 1/12	01/04/2020	MS
limited search of G06F 13/1689	01/04/2020	MS
limited search of G06F 12/0246	01/04/2020	MS
limited search of G06F 13/1694	01/04/2020	MS

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST Search - see attached	01/04/2020	MS
Inventor Search - see attached EAST Search	01/04/2020	MS
limited EAST Search of class/subclasses 710/5, 6, and 7	01/04/2020	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	01/04/2020	MS
Google Scholar Search - search terms used: (memory module and memory controller and address and control signals and data signals and clock signal and buffer and delay); (memory module and memory controller and address and control signal and data signal and clock signal and buffer and delay and delaying by amount determined by control signal)	01/04/2020	MS

/MICHAEL SUN/ Primary Examiner, Art Unit 2183	
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<i>Search Notes</i> 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.
	Examiner MICHAEL SUN	Art Unit 2183

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/MICHAEL SUN/ Primary Examiner, Art Unit 2183	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S348	5791	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S349	2417	S348 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S350	220	S349 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S351	81	S350 AND ((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) OR (710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S352	81	S351 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S353	81	S352 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S354	81	S353 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S355	47	S354 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S356	10	S355 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S357	5462	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2020/01/04 13:39

			IBM_TDB			
S358	124	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:39
S359	681480	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:40
S360	68428	S359 and ((determin\$5 or calculat\$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:40
S361	181	S359 and ((determin\$5 or calculat\$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:40
S362	82	S361 and (transmi\$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:40
S363	874	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:43
S364	2	S363 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:43
S365	8223	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:44
S366	1076	S365 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:44
S367	55	S366 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:44
S368	13	S367 and (align\$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:44
S369	197351	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2020/01/04 13:45

			IBM_TDB			
S370	2409	S369 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:45
S371	1959	S370 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:45
S372	1921	S371 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:45
S373	403	S372 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:45
S374	91	S373 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:45
S375	9548	memory module and buffer and tim\$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:46
S376	1912	S375 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:46
S377	1416	S376 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:46
S378	407	S377 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:46
S379	10	S378 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:46
S380	10	S379 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/01/04 13:46
S381	7	S380 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	ON	2020/01/04 13:46

			IBM_TDB			
S382	498	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:47
S383	365	S382 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:47
S384	175	S383 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:47
S385	156	S384 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:47
S386	56	S385 and tim\$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:47
S387	14	S386 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/01/04 13:47

EAST Search History (Interference)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
				Application Number	16/391,151	
				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2184	
Examiner Name	To be assigned					
Sheet	1	of	7	Attorney Docket Number	129980-5049US01	

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Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Signature	/MICHAEL SUN/	Date Considered	01/04/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
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				First Named Inventor	Hyun Lee	
				Art Unit	2184	
Examiner Name	To be assigned					
Sheet	2	of	7	Attorney Docket Number		129980-5049US01

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
/M.S./		Lee, Office Action, US15/426,064, 02JUN2017, 11 pgs.
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/M.S./		Lee, Notice of Allowance, US14/846,993, 23SEP2016, 8 pgs.
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		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016
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		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016
		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016
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		Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016

Examiner Signature	/MICHAEL SUN/	Date Considered	01/04/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019		
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				Filing Date	April 22, 2019	
				First Named Inventor	Hyun Lee	
				Art Unit	2184	
				Examiner Name	To be assigned	
Sheet	3	of	7	Attorney Docket Number		129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	01/04/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 20, 2019	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2184
				Examiner Name	To be assigned
Sheet	4	of	7	Attorney Docket Number	129980-5049US01

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				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2184
Examiner Name	To be assigned				
Sheet	5	of	7	Attorney Docket Number	129980-5049US01

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				Art Unit	2184
				Examiner Name	To be assigned
Sheet	6	of	7	Attorney Docket Number	129980-5049US01

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		February 10, 2016
		Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl
		Sechen Deposition Transcript,' filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan
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				Examiner Name	To be assigned
Sheet	7	of	7	Attorney Docket Number	129980-5049US01

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		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed June 29, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018

Examiner Signature	/MICHAEL SUN/	Date Considered	01/04/2020
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DB2/ 37149841.1

Electronically filed April 10, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	<i>MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING</i>	Attorney Docket No.:	129980-5049-US01

RESPONSE TO OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Office Action dated January 10, 2020 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

Electronic Acknowledgement Receipt

EFS ID:	39130538
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	10-APR-2020
Filing Date:	22-APR-2019
Time Stamp:	18:25:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5049US01_AMEND.pdf	177364	yes	13
			7ce7cf2b5614a88c12c2a72ef8f13338874f7f48		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Applicant Arguments/Remarks Made in an Amendment	10	13
	Claims	2	9
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Warnings:			
Information:			
Total Files Size (in bytes):		177364	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

REMARKS

This amendment responds to the office action mailed January 10, 2020. In the office action, the Examiner:

- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-12 of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-22 of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-20 of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-20 of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632; and
- rejected claim 1 as being anticipated by Manohararajah et al. (US 8,565,033).

REMARKS CONCERNING CLAIMS

Claim 1 has been canceled.

Claims 2-21 have been added.

Support for the amendments can be found in at least paragraphs [0034], [0047], [0050], [0052], [0061]-[0074], and [0083]-[0097], and the Figures referenced to in these paragraphs of the application as filed. No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2 - 21.

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

I. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-12 OF COPENDING APPLICATION NO. 15/820,076, NOW U.S. PATENT NO. 10,268,608

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

II. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-22 OF COPENDING APPLICATION NO. 15/426,064, NOW U.S. PATENT NO. 9,824,035

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

III. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-20 OF COPENDING APPLICATION NO. 14/846,993, NOW U.S. PATENT NO. 9,563,587

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

IV. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-20 OF COPENDING APPLICATION NO. 13/952,599, NOW U.S. PATENT NO. 9,128,632

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 102

V. REJECTION OF CLAIM 1 AS BEING ANTICIPATED BY MANOHARARAJAH

Claim 1 has been cancelled. New claims 2-21 are patentable over Manohararajah.

With respect to claim 2, Manohararajah does not disclose or teach all of the elements arranged as claimed. For example, claim 2 recites:

“a module control device on the module board configurable to *receive* input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals.”

Emphasis added.

Manohararajah does not teach a memory module including such a module control device. In Manohararajah, the memory module 22 is shown to include memory groups 52-1 to 52-N but no module control device. The memory interface circuitry 24 in Manohararajah, which is on the other side of the buses 34/36, *outputs* instead of *receiving* input C/A signals corresponding to a memory read operation via the C/A signal lines. Therefore, the memory interface circuitry 24 in Manohararajah cannot be likened to the module control device in claim 2.

As another example, claim 2 further recites:

“a module board having edge connections to be coupled to respective signal lines in the memory bus” and “data buffers on the module board and coupled *between* the edge connections and the memory devices.”

Emphasis added.

Again, Manohararajah does not teach these claimed features. In Manohararajah, the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62, which the Office Action refers to when discussing data buffers, are not coupled between the memory device groups 52-1 to 52-N and any edge connections to be coupled to buses 34/36. Instead, the memory device groups 52-1 to 52-3 are shown in FIGS. 4-5 as coupled directed to one side of the buses 34/36 and the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62 are on the other side of the buses 34/36. Thus, Manohararajah does not disclose or teach “data buffers on the module board and coupled *between* the edge connections and the memory devices,” as recited in claim 2.

As a further example, claim 2 further recites:

“a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to the module control signals, ... *transmit* the first section of the read data to a first section of the data bus.”

Emphasis added.

In contract, the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62 in Manohararajah *receive* read data and read strobes from bus 34 instead of transmitting read data and read strobe to bus 34.

Therefore, Manohararajah does not teach each and every element of claim 2, and claim 2 is patentable over Manohararajah.

Claims 3-14 depend from claim 2 and include further limitations in addition to the limitation in claim 2. Therefore, claims 3-14 are patentable for at least the same reasons claim 2 is patentable.

The arguments regarding claim 2 apply to claim 15. Therefore, claim 15 is also patentable over Manohararajah.

Claims 16-21 depend from claim 15 and include further limitations in addition to the limitation in claim 15. Therefore, claims 16-21 are patentable for at least the same reasons claim 15 is patentable.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 10, 2020

/Jamie J. Zheng/

51,167

Jamie J. Zheng

(Reg. No.)

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)
2. (New) A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:
 - a module board having edge connections to be coupled to respective signal lines in the memory bus;
 - a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
 - memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and
 - data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
 - delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
 - sample the first section of the read data using the first delayed read strobe; and
 - transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer before the memory read operation.

3. (New) The memory module of claim 2, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:

delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sample the second section of the read data using the second delayed read strobe; and

transmit the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based at least on signals received by the second data buffer before the memory read operation.

4. (New) The memory module of claim 3, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and

transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based at least on signals received by the first data buffer before the memory read operation.

5. (New) The memory module of claim 3, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer before the

memory read operation includes at least another strobe signal associated with the previous operation.

6. (New) The memory module claim 3, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

7. (New) The memory module of claim 2, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation.

8. (New) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:

- receive the module clock signal;
- generate a local clock signal having a programmable phase relationship with the module clock signal; and
- output the local clock signal;

wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

9. (New) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

10. (New) The memory module of claim 9, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

11. (New) The memory module of claim 10, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

12. (New) The memory module of claim 2, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer before the memory read operation.

13. (New) The memory module of claim 2, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

14. (New) The memory module of claim 2, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.

15. (New) A method, comprising:

at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer, wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;

receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sampling the first section of the read data using the first delayed read strobe; and

transmitting the first section of the read data to a first section of the data bus; and

the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

16. (New) The method of claim 15, wherein the data buffers further include a second data buffer, and wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe, the method further comprising, at the second data buffer, in response to the one or more of the module control signals:

delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sampling the second section of the read data using the second delayed read strobe; and

transmitting the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based on signals received by the second data buffer before the memory read operation.

17. (New) The method of claim 16, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe, the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and

transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based on the signals received by the first data buffer before the memory read operation.

18. (New) The method of claim 16, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation, and the signals received by the second data buffer before the memory read operation includes at least another strobe signal associated with the previous operation.

19. (New) The method of claim 15, further comprising:
- receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;
 - outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
 - receiving, at the first data buffer, the module clock signal;
 - generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and
 - outputting, at the first data buffer, the local clock signal;
 - receiving, at the first memory device, the local clock signal; and
 - outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.
20. (New) The method of claim 15, further comprising:
- receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;
 - outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
 - generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.
21. (New) The method of claim 20, further comprising, at the first data buffer:
- generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;
 - selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;
 - selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and

sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed		PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce	
Electronic Petition Request	TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT		
Application Number	16391151		
Filing Date	22-Apr-2019		
First Named Inventor	Hyun Lee		
Attorney Docket Number	129980-5049-US01		
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING		
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.			
Owner		Percent Interest	
Netlist, Inc.		100%	
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s) 10268608 9824035 9563587 9128632			

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- ☐ Small Entity
- ☐ Micro Entity
- ☒ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 51167

☐ A sole inventor

☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

☐ A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng/
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16391151			
Filing Date:	22-Apr-2019			
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING			
First Named Inventor/Applicant Name:	Hyun Lee			
Filer:	Jamie Jie Zheng/S. Olivier			
Attorney Docket Number:	129980-5049-US01			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				160

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Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16391151

Filing Date: 22-Apr-2019

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on April 10, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	39126263
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
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Filing Date:	22-APR-2019
Time Stamp:	18:30:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	E202040I30444621
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Micron Technology Inc. et al.

Ex. 1052, p. 191

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	34941	no	3
			44159a3c60102b2f57ccaa9e136a94656136a557		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30632	no	2
			bff60b5196fd414426c50c6a2010a8a9169a03ea5		
Warnings:					
Information:					
Total Files Size (in bytes):			65573		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/391,151		Filing Date 04/22/2019		☐ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED - PART I										
		(Column 1)	(Column 2)							
FOR		NUMBER FILED	NUMBER EXTRA	RATE (\$)		FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	N/A						
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A	N/A						
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	N/A						
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*	x \$100 =						
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*	x \$460 =						
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL						
APPLICATION AS AMENDED - PART II										
		(Column 1)	(Column 2)	(Column 3)						
AMENDMENT	04/10/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =		0		
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	x \$460 =		0		
	☒ Application Size Fee (37 CFR 1.16(s))							400		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		400		
		(Column 1)	(Column 2)	(Column 3)						
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =				
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =				
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE				
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/ROSS W BROWN/				
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/391,151		Filing Date 04/22/2019		☐ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED - PART I										
		(Column 1)	(Column 2)							
FOR		NUMBER FILED	NUMBER EXTRA	RATE (\$)		FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	N/A						
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A	N/A						
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	N/A						
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*	x \$100 =						
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*	x \$460 =						
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL						
APPLICATION AS AMENDED - PART II										
		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT	04/10/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =		0		
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	x \$460 =		0		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		0		
		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =				
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =				
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE				
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/ROSS W BROWN/				
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 07/23/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER

SUN, MICHAEL

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 07/23/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	10/23/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

79141 7590 07/23/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	10/23/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, MICHAEL	2183	710-310000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694
79141	7590	07/23/2020	EXAMINER	
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)			SUN, MICHAEL	
1400 Page Mill Road			ART UNIT	
Palo Alto, CA 94304			PAPER NUMBER	
			2183	
DATE MAILED: 07/23/2020				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/391,151	Applicant(s) Lee et al.	
	Examiner MICHAEL SUN	Art Unit 2183	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Applicant's Amendment filed 4/10/2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-21. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>1/08/2020</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

/MICHAEL SUN/
Primary Examiner, Art Unit 2183

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Amendment filed 4/10/2020.

Claims 2-21 are pending for this examination.

Claim 1 was cancelled.

Claims 2-21 were added.

Terminal Disclaimer

The terminal disclaimer filed on 4/10/2020 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 10,268,608; US Patent No. 9,824,035; US Patent No. 9,563,587; and US Patent No. 9,128,632 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/08/2020 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Examiner notes that in the IDS filed 1/08/2020 there were many Non-Patent Literature Documents and Foreign Patent Documents that were listed throughout without any corresponding copy of these documents attached to review in this instant application or any of

the parent applications. As such, these listings were not considered as Examiner had no copy of these documents to review.

Allowable Subject Matter

Claims 2-21 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory controller systems with memory arranged into memory ranks and memory modules including a buffer provided for buffering signals / data to and from memory chips on the memory modules; and memory systems that implement delays for transmitting signals to and from memory devices of a memory module including delaying strobe signals, however, the prior art does not fairly teach or suggest, individually or in combination, a memory controller system with memory modules having control and address signal lines implemented to be used corresponding to memory read operations to and from memory devices of the memory module that are arranged in multiple ranks with data buffers coupled to the memory devices, where memory read operations output read data and read strobes associated with the memory read operations, and where the data buffer implemented delaying of a first read strobe by a predetermined amount, i.e. generating a delayed read strobe, sampling the first section of read data using the delayed read strobe, and transmitting the section of read data to a data bus, where the predetermined amount of delay is determined based at least on signals received by the data buffer before the memory read operation as claimed. Applicant argues these limitations on Pages 11-13 of Applicant's Remarks filed 4/10/2020. These limitations find

support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Related / Relevant Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kizer et al. (US 2012/0170389) teaches a memory controller that implements read strobes and delaying of such read strobes based on synchronization signals.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724.

The examiner can normally be reached on Monday-Friday 8am-4pm EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aimee Li can be reached on 571-272-4169. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/
Primary Examiner, Art Unit 2183

Notice of References Cited	Application/Control No. 16/391,151		Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner MICHAEL SUN		Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

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*	B	US-20140036607-A1	02-2014	Koshizuka; Atsuo	G11C11/4096	365/193
*	C	US-20140029370-A1	01-2014	KOSHIZUKA; Atsuo	G11C15/00	365/233.13
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner MICHAEL SUN	Art Unit 2183	

CPC						
Symbol					Type	Version
G06F	/	13	/	1673	F	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G11C	/	5	/	04	I	2013-01-01
G11C	/	7	/	1006	I	2013-01-01
G11C	/	7	/	1066	I	2013-01-01
G11C	/	7	/	1093	I	2013-01-01
G11C	/	29	/	023	I	2013-01-01
G11C	/	29	/	028	I	2013-01-01
G11C	/	16	/	00	I	2013-01-01
G06F	/	1	/	10	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0647	I	2013-01-01
G06F	/	3	/	0683	I	2013-01-01
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H05K	/	999	/	99	I	2013-01-01
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G11C	/	2029	/	0407	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MICHAEL SUN/ Primary Examiner, Art Unit 2183	16 July 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Issue Classification 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.
	Examiner MICHAEL SUN	Art Unit 2183

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G06F	/	3	/ 00
G06F	/	12	/ 00
G06F	/	13	/ 00
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
710	310

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
710	5	6	7			
711	1	2	3	4	154	155

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MICHAEL SUN/ Primary Examiner, Art Unit 2183 (Primary Examiner)	16 July 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.
	Examiner MICHAEL SUN	Art Unit 2183

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	9	10	18	19										
1	2	10	11	19	20										
2	3	11	12	20	21										
3	4	12	13												
4	5	13	14												
5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9	17	18												

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 20	
/MICHAEL SUN/ Primary Examiner, Art Unit 2183 (Primary Examiner) _____ (Date) 16 July 2020		O.G. Print Claim(s) 1	O.G. Print Figure 1

<i>Search Notes</i> 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.
	Examiner MICHAEL SUN	Art Unit 2183

CPC - Searched*		
Symbol	Date	Examiner
limited search of G06F 1/12	07/08/2020	MS
limited search of G06F 13/1689	07/08/2020	MS
limited search of G06F 12/0246	07/08/2020	MS
limited search of G06F 13/1694	07/08/2020	MS

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Updated EAST Search - see attached	07/16/2020	MS
Inventor Search - see attached EAST Search	07/08/2020	MS
limited EAST Search of class/subclasses 710/5, 6, and 7	07/08/2020	MS
limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155	07/08/2020	MS
Google Scholar Search - search attached	07/16/2020	MS

/MICHAEL SUN/ Primary Examiner, Art Unit 2183	
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<i>Search Notes</i> 	Application/Control No. 16/391,151	Applicant(s)/Patent Under Reexamination Lee et al.
	Examiner MICHAEL SUN	Art Unit 2183

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
710	limited search of subclasses 5, 6, and 7	07/16/2020	MS
711	limited search of subclasses 1, 2, 3, 4, 154, and 155	07/16/2020	MS

/MICHAEL SUN/ Primary Examiner, Art Unit 2183	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020		
				Application Number		16/391,151
				Filing Date		April 22, 2019
				First Named Inventor		Hyun Lee
				Art Unit		2183
Examiner Name		Sun, Michael				
Sheet	1	of	22	Attorney Docket Number		129980-5049US01

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DB2/ 22684197.4

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				First Named Inventor		Hyun Lee
				Art Unit		2183
				Examiner Name		Sun, Michael
Sheet	2	of	22	Attorney Docket Number		129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	3	of	22	Attorney Docket Number	129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	4	of	22	Attorney Docket Number	129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
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				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	5	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
				Attorney Docket Number	129980-5049US01
Sheet	6	of	22		

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				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	7	of	22	Attorney Docket Number	129980-5049US01

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				Examiner Name	Sun, Michael
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				Art Unit	2183	
				Examiner Name	Sun, Michael	
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				First Named Inventor	Hyun Lee	
				Art Unit	2183	
				Examiner Name	Sun, Michael	
Sheet	10	of	22	Attorney Docket Number		129980-5049US01

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				First Named Inventor	Hyun Lee
				Art Unit	2183
Examiner Name	Sun, Michael				
Sheet	11	of	22	Attorney Docket Number	129980-5049US01

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				Application Number	16/391,151
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				Examiner Name	Sun, Michael
Sheet	12	of	22	Attorney Docket Number	129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020		
				Application Number		16/391,151
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				First Named Inventor		Hyun Lee
				Art Unit		2183
				Examiner Name		Sun, Michael
Sheet	13	of	22	Attorney Docket Number		129980-5049US01

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Sheet	14	of	22	Examiner Name	Sun, Michael
				Attorney Docket Number	129980-5049US01

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				Examiner Name	Sun, Michael
Sheet	15	of	22	Attorney Docket Number	129980-5049US01

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DB2/ 22684197.4

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				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	16	of	22	Attorney Docket Number	129980-5049US01

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Sheet	17	of	22	Attorney Docket Number	129980-5049US01

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Sheet	18	of	22	Attorney Docket Number	129980-5049US01

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Sheet	19	of	22	Attorney Docket Number		129980-5049US01	

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DB2/ 22684197.4

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Sheet	20	of	22	Attorney Docket Number	129980-5049US01

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		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, Conduct of the Proceedings, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed August 6, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018

Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
Examiner Name	Sun, Michael				
Sheet	21	of	22	Attorney Docket Number	129980-5049US01

		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 14, 'Patent Owner's Response,' filed October,19,2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February,11,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February,11,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 19, 'Petitioners' Request for Oral Argument,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 21, 'Patent Owner Objections To Reply Evidence,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 20, 'Patent Owner Request For Oral Argument,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 22, 'Patent Owner Motion To Exclude,' filed February,19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 23, 'Corrected Petitioners' Reply to Patent Owner's Response,' filed February,20,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 28, 'Order - Trial Hearing,' filed March,22,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June,27,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June,27,2019
		Response, Article 94.3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs
		Observations by third parties, EP 18179414.0, 22FEB2019, 1 pg
		Patent Document filed by a third party, 20FEB2019, 10 pgs
		Netlist, Inc., Observations by third parties, EP 3404660, 20FEB2019, 46 pgs
		Reply to Written Opinion prepared by the EPO, EP 18179414.0, 17JAN2019, 20 pgs
		Netlist, Inc., Information on Search Strategy, EP 18179414, 23OCT2018, 1 pg
		European Search Report, EP 18179414, 23OCT2018, 3 pgs

Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	22	of	22	Attorney Docket Number	129980-5049US01

		European Search Opinion, EP 18170414, 23OCT2018, 3 pgs
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, Conduct of the Proceedings, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed August 6, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed June 29, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018

Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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DB2/ 22684197.4

Web Search History

date, time	web site	search string
7/16/2020 9:59:11 AM	Google Scholar	memory controller control signal address signal buffer read strobe
7/16/2020 9:59:11 AM	Google Patents	Keyword Group 1 [memory controller control signal address signal buffer read strobe]
7/16/2020 9:59:21 AM	Google Scholar	memory controller control signal address signal buffer read strobe delaying read strobe
7/16/2020 9:59:21 AM	Google Patents	Keyword Group 1 [memory controller control signal address signal buffer read strobe delaying read strobe]

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S388	6,028	memory module and timing signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S389	2,531	S388 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S390	222	S389 and operating speed	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S391	81	S390 AND ((G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) OR (710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS.)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S392	81	S391 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S393	81	S392 and ((data or strobe) near2 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S394	81	S393 and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S395	47	S394 and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45

S396	10	S395 and command signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S397	5,637	(lee, hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S398	126	(bhakta, jayesh).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:45
S399	710,725	buffer and memory and (data or strobe) and (read or write)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:47
S400	71,581	S399 and ((determin\$5 or calculat\$3) with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:47
S401	202	S399 and ((determin\$5 or calculat\$3) with (time interval or delay) with (first signal) with (second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:48
S402	90	S401 and (transmi\$5 with (time interval or delay))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:48
S403	910	(determining or calculating) with (time interval or delay) with (first signal) with (second signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:50
S404	3	S403 and memory controller and buffer and memory bus	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 14:50
S405	9,030	memory module and buffer and memory device and memory controller and control signal and command	US-PGPUB; USPAT; USOCR; EPO;	ADJ	ON	2020/07/08 15:02

			DERWENT; IBM_TDB			
S406	1,109	S405 and system clock	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:02
S407	55	S406 and (write with (different near4 time))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:02
S408	13	S407 and (align\$4 with read)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:02
S409	203,309	(deriving or timing or calculating) with (delay or latency)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:04
S410	2,498	S409 and read and write and strobe and memory module and controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:04
S411	2,026	S410 and buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:04
S412	1,987	S411 and ((data or strobe) near4 signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:04
S413	414	S412 and (timing with transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:04
S414	95	S413 and (timing with transmission with read) with write	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:04

S415	10,019	memory module and buffer and tim\$3 and (control signal or address signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/07/08 15:06
S416	1,984	S415 and time interval	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:06
S417	1,463	S416 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:06
S418	418	S417 and (strobe signal and data signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:06
S419	10	S418 and (time interval with (first signal and second signal))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:06
S420	10	S419 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:06
S421	7	S420 and time transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/08 15:06
S422	512	memory module and buffer and (control signal and address signal and data signal and strobe signal)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/07/08 15:08
S423	376	S422 and delay	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/07/08 15:08
S424	180	S423 and time interval	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2020/07/08 15:08

			DERWENT; IBM_TDB			
S425	161	S424 and memory controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/07/08 15:08
S426	56	S425 and tim\$3 transmission	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/07/08 15:08
S427	14	S426 and first signal and second signal	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2020/07/08 15:08
S428	492	control signal and address signal and signal lines and memory controller and strobe and (rank with memory) and buffer and delay\$3	US-PGPUB; USPAT; USOCR; EPO; JPO	ADJ	ON	2020/07/16 09:49
S429	0	S428 and (delay\$3 near4 read strobe)	US-PGPUB; USPAT; USOCR; EPO; JPO	ADJ	ON	2020/07/16 09:50
S430	14	S428 and (delay\$3 with read strobe)	US-PGPUB; USPAT; USOCR; EPO; JPO	ADJ	ON	2020/07/16 09:50

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S431	8	((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC.) and (memory controller).clm. and (buffer).clm. and (read strobe).clm.	US-PGPUB; USPAT	ADJ	ON	2020/07/16 09:55
S432	5	S431 and (delay\$3).clm.	US-PGPUB; USPAT	ADJ	ON	2020/07/16 09:56
S433	19	(memory controller).clm. and (buffer).clm. and (read strobe).clm.	US-PGPUB; USPAT	ADJ	ON	2020/07/16 09:56

S434	2	S433 and (delay\$3 near5 read strobe).clm.	US- PGPUB; USPAT	ADJ	ON	2020/07/16 09:57
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7/16/2020 10:18:57 AM

C:\Users\msun\Documents\EAST\Workspaces\16391151.wsp



UNITED STATES PATENT AND TRADEMARK OFFICE

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BIB DATA SHEET

CONFIRMATION NO. 3694

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
16/391,151	04/22/2019	710	2183	129980-5049-US01		
APPLICANTS Netlist, Inc., Irvine, CA; INVENTORS Hyun Lee, Ladera Ranch, CA; Jayesh R. Bhakta, Cerritos, CA; ** CONTINUING DATA ***** This application is a CON of 15/820,076 11/21/2017 PAT 10268608 which is a CON of 15/426,064 02/07/2017 PAT 9824035 which is a CON of 14/846,993 09/07/2015 PAT 9563587 which is a CON of 13/952,599 07/27/2013 PAT 9128632 which claims benefit of 61/676,883 07/27/2012 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/02/2019						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/MICHAEL SUN/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 26	TOTAL CLAIMS ~~1~~ 20	INDEPENDENT CLAIMS ~~1~~ 2
ADDRESS Morgan, Lewis & Bockius LLP (PA)(J. Zheng) 1400 Page Mill Road Palo Alto, CA 94304 UNITED STATES						
TITLE MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING						
FILING FEE RECEIVED 1880	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Electronic Acknowledgement Receipt

EFS ID:	40871572
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5049-US01
Receipt Date:	16-OCT-2020
Filing Date:	22-APR-2019
Time Stamp:	23:29:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	129980-5049- US01_312_AMEND.pdf	124106	no	11
			d053362e94b42ef41ae42a9c9ab77388b925b827		

Warnings:

Micron Technology Inc. et al.

Ex. 1052, p. 240

Information:	
Total Files Size (in bytes):	124106
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

Electronically filed October 16, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	<i>MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING</i>	Attorney Docket No.:	129980-5049-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The enclosed Amendment is filed after a Notice of Allowance dated July 23, 2020, and is filed under 37 C.F.R. § 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)
2. (Currently Amended) A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:
 - a module board having edge connections to be coupled to respective signal lines in the memory bus;
 - a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
 - memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and
 - data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
 - delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
 - sample the first section of the read data using the first delayed read strobe; and
 - transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations ~~before the memory read operation.~~

3. (Currently Amended) The memory module of claim 2, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:

delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sample the second section of the read data using the second delayed read strobe; and

transmit the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations ~~before the memory read operation.~~

4. (Currently Amended) The memory module of claim 3, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and

transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations ~~before the memory read operation.~~

5. (Currently Amended) The memory module of claim 3, wherein the signals received by the first data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least another strobe signal associated with the previous operation.

6. (Previously Presented) The memory module claim 3, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

7. (Currently Amended) The memory module of claim 2, wherein the signals received by the first data buffer ~~before the memory read operation includes~~ during one or more previous operations include at least a strobe signal associated with a previous operation.

8. (Previously Presented) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:

- receive the module clock signal;
- generate a local clock signal having a programmable phase relationship with the module clock signal; and
- output the local clock signal;

wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

9. (Previously Presented) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals,

a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

10. (Previously Presented) The memory module of claim 9, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

11. (Previously Presented) The memory module of claim 10, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

12. (Currently Amended) The memory module of claim 2, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations ~~before the memory read operation~~.

13. (Previously Presented) The memory module of claim 2, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the

multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

14. (Previously Presented) The memory module of claim 2, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.

15. (Previously Presented) A method, comprising:

at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer, wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;

receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;
sampling the first section of the read data using the first delayed read strobe; and
transmitting the first section of the read data to a first section of the data bus; and
the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

16. (Currently Amended) The method of claim 15, wherein the data buffers further include a second data buffer, and wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe, the method further comprising, at the second data buffer, in response to the one or more of the module control signals:

delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;
sampling the second section of the read data using the second delayed read strobe; and
transmitting the second section of the read data to a second section of the data bus;
wherein the second predetermined amount is determined based on signals received by the second data buffer during one or more previous operations ~~before the memory read operation~~.

17. (Currently Amended) The method of claim 16, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe, the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;
sampling the third section of the read data using the third delayed read strobe
concurrently with receiving the first section of the read data using the first delayed read strobe;
and
transmitting the third section of the read data to a third section of the data bus
concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based on the signals received by the first data buffer during one or more previous operations~~before the memory read operation~~.

18. (Currently Amended) The method of claim 16, wherein the signals received by the first data buffer ~~before the memory read operation~~ includes during one or more previous operations include at least a strobe signal associated with a previous operation, and the signals received by the second data buffer ~~before the memory read operation~~ includes during one or more previous operations include at least another strobe signal associated with the previous operation.

19. (Previously Presented) The method of claim 15, further comprising:
receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;
outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
receiving, at the first data buffer, the module clock signal;
generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and
outputting, at the first data buffer, the local clock signal;
receiving, at the first memory device, the local clock signal; and
outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.

20. (Previously Presented) The method of claim 15, further comprising:
receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;
outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.

21. (Previously Presented) The method of claim 20, further comprising, at the first data buffer:

generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;

selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;

selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and

sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

REMARKS

This amendment is filed under 37 C.F.R. § 1.312 after the Notice of Allowance dated July 23, 2020.

REMARKS CONCERNING INFORMATION DISCLOSURE STATEMENT

Applicant appreciates Examiner's diligent review of the Information Disclosure Statement submitted on January 8, 2020 (IDS). In the Notice of Allowance, the Examiner notes that "in the IDS filed 1/08/2020 there were many Non-Patent Literature Documents and Foreign Patent Documents that were listed throughout without any corresponding copy of these documents attached." Applicant would like to point out that the IDS identified several related applications in which the references have been submitted, including applications to which the present application claims priority under 35 U.S.C. §120 ("the parent applications"), and a co-pending U.S. Patent Applications No. 15/470,856, filed on March 27, 2017 ("the co-pending application").

Applicant apologizes for mistakenly grouping the co-pending application in the IDS as one of the applications to which the present application claims priority under 35 U.S.C. §120. The co-pending application is instead an application that claims priority to a related application cross-referenced in the present application (i.e., U.S. Pat. App. No. 13/970,606, filed on August 20). The references in the IDS that are crossed out in the Notice of Allowance were listed in the IDS mainly due to the reason that they had been listed in Information Disclosure Statements in the co-pending application.

REMARKS CONCERNING CLAIMS

Claims 2-5, 7, 12, and 16-18 have been amended to address minor issues of clarity and to correct grammatical errors.

No new matter has been added, and the amendment should not necessitate additional search or examination. Therefore, entry of the amendment is respectfully requested.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover,

the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2 - 21.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: October 16, 2020

/Jamie J. Zheng/

51,167

Jamie J. Zheng

(Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP

1400 Page Mill Road

Palo Alto, CA 94304

Phone: (650) 843-4000

PART B - FEE(S) TRANSMITTAL

Electronically filed October 22, 2020

Complete and send this form with applicable fee(s), to: Mail

Mail Stop ISSUE FEE
 Commissioner of Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 (571) 273-2885

or Fax

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advanced orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS

MORGAN, LEWIS & BOCKIUS LLP
 1400 Page Mill Road
 Palo Alto, CA 94304

Note: A certificate of mailing below can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTY'S DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694

TITLE OF INVENTION MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	1000	10/23/2020

EXAMINER	ART UNIT	CLASS-SUB CLASS
SUN, MICHAEL	2183	710-310000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed

1. **Morgan, Lewis & Bockius LLP**

2. _____

3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE:

NETLIST, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee☐ Advanced Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above.)

☐ A check in the amount of the fee(s) enclosed☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-0310 (order no. 129980-5049-US01).

5. Change in Small Entity Status (from status indicated above)☐ a. Applicant certifying micro entity status. See 37 CFR 1.29.

NOTE: Absent a valid certification of Micro Entity (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be sign in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature: / Jamie J. Zheng /

Date: October 22, 2020

Printed Name: Jamie J. Zheng

Registration No. 51,167

Electronic Patent Application Fee Transmittal

Application Number:	16391151			
Filing Date:	22-Apr-2019			
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING			
First Named Inventor/Applicant Name:	Hyun Lee			
Filer:	Jamie Jie Zheng/Jacqueline Yu			
Attorney Docket Number:	129980-5049-US01			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt

EFS ID:	40901756
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5049-US01
Receipt Date:	22-OCT-2020
Filing Date:	22-APR-2019
Time Stamp:	20:00:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	E20200LK00462012
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Micron Technology Inc. et al.

Ex. 1052, p. 256

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	129980-5049- US01_Issue_Fee_Transmittal. pdf	160173	no	1
			271f10ce90ec8b720e5bd9c5acb0513249d f31a		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30664	no	2
			5cb3bef0f5f828b9fa7d69b210093f9e7d0c 9e17		
Warnings:					
Information:					
Total Files Size (in bytes):			190837		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694
79141	7590	11/04/2020	EXAMINER	
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)			SUN, MICHAEL	
1400 Page Mill Road			ART UNIT	PAPER NUMBER
Palo Alto, CA 94304			2183	
			NOTIFICATION DATE	DELIVERY MODE
			11/04/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Response to Rule 312 Communication	Application No.		Applicant(s)		
	16/391,151		Lee et al.		
	Examiner		Art Unit	AIA (FITF) Status	
	MICHAEL SUN		2183	No	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 16 October 2020 under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/MICHAEL SUN/ Primary Examiner, Art Unit 2183	
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Electronically filed October 16, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	<i>MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING</i>	Attorney Docket No.:	129980-5049-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The enclosed Amendment is filed after a Notice of Allowance dated July 23, 2020, and is filed under 37 C.F.R. § 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

OK TO ENTER: /M.S/ 10/30/2020

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Electronically filed January 8, 2020	
				Application Number	16/391,151
Substitute for Form 1449-PTO				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	7	of	22	Attorney Docket Number	129980-5049US01

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Examiner Initials	Cite No.	Foreign Patent Document Country Code - Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
Examiner Name	Sun, Michael				
Sheet	6	of	22	Attorney Docket Number	129980-5049US01

Change(s) applied
to document,
/D.M./
9/8/2020

/M.S./		7,464,225	2008-12-02	Tsern	
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/M.S./		20050010737	2005-01-13	Fred Ware	
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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
				Filing Date	April 22, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	4	of	22	Attorney Docket Number	129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 8, 2020	
				Application Number	16/391,151
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				Art Unit	2183
				Examiner Name	Sun, Michael
Sheet	5	of	22	Attorney Docket Number	129980-5049US01

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Examiner Signature	/MICHAEL SUN/	Date Considered	07/10/2020
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	12/08/2020	10860506	129980-5049-US01	3694

79141 7590 11/18/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Netlist, Inc., Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court EASTERN DISTRICT OF TEXAS MARSHALL DIVISION on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:21-cv-463	DATE FILED 12/20/2021	U.S. DISTRICT COURT EASTERN DISTRICT OF TEXAS MARSHALL DIVISION
PLAINTIFF NETLIST, INC.		DEFENDANT Samsung Electronics Co., Ltd., Samsung Electronics America, Inc. Samsung Semiconductor, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 10,860,506	12/8/2020	Netlist, Inc.
2 10,949,339	3/16/2021	Netlist, Inc.
3 11,016,918	5/25/2021	Netlist Inc.
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Micron Technology Inc. et al.
Ex. 1052, p. 266