Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2024-00370

Patent 10,268,608

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,268,608

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 10,268,608
1002	File History of U.S. Patent No. 10,268,608
1003	Declaration of Dr. Robert Wedig
1004	Curriculum Vitae of Dr. Robert Wedig
1005	U.S. Patent Pub. No. US2010/0312956 to Hiraishi
1006	U.S. Patent No. 8,020,022 to Tokuhiro
1007	U.S. Patent Pub. No. 2006/0277355 by Ellsberry
1008	U.S. Patent No. 6,184,701 to Kim
1009	U.S. Patent No. 8,566,516 to Schakel
1010	File History of U.S. Patent No. 9,128,632
1011	File History of U.S. Patent No. 9,563,587
1012	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition)
1013	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response)
1014	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution)
1015	*SK Hynix Inc. et al. v. Netlist, Inc*., IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision)
1016	U.S. Patent Pub. No. 2011/0062999 to Nimaiyar
1017	Declaration of Julie Carlson for JEDEC Standard 21-C

Exhibit #	Description
1018	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1019	Declaration of Julie Carlson for JESD79-3C
1020	JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008)
1021	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) (excerpts)
1022	Harold S. Stone, Microcomputer Interfacing (1982)
1023	Microsoft Computer Dictionary (5th ed. 2002)
1024	U.S. Patent No. 9,263,103 to Giovannini
1025	U.S. App. No. 61/676,883 (provisional application to '632 Patent)
1026	U.S. Patent No. 8,565,033 to Manohararajah
1027	U.S. Patent No. 7,808,849 to Swain
1028	U.S. Patent No. 6,906,555 to Ma
1029	U.S. Patent Pub. No. 2007/0008791 to Butt
1030	U.S. Patent No. 7,036,053 to Zumkehr
1031	U.S. Patent No. 9,824,035
1032	File History of U.S. Patent No. 9,824,035
1033	U.S. Patent No. 5,036,221 to Brucculeri
1034	U.S. Patent No. 9,536,579 to Iijima
1035	Complaint, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021) (asserting U.S. Patent No. 10,268,608)

Exhibit #	Description
1036	Order Transferring Cases to the Austin Division, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. Feb. 14, 2022)
1037	Joint Claim Construction Statement, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. Apr. 14, 2022)
1038	Order on Motion to Stay, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. May 11, 2022), Dkt. 69.
1039	[intentionally omitted]
1040	Final Written Decision in *Inter Partes* Review, *Micron Tech, Inc. et al. v. Netlist, Inc.*, IPR2022-00236, Paper 34 (PTAB June 20, 2023) (U.S. Patent No. 9,824,035)
1041	Decision Denying Institution of *Inter Partes* Review, *Micron Tech, Inc. et al. v. Netlist, Inc.*, IPR2022-00237, Paper 15 (PTAB July 19, 2022) (U.S. Patent No. 10,268,608)
1042	Decision Granting Petitioner's Request on Rehearing of Final Written Decision, *Micron Tech, Inc. et al. v. Netlist, Inc.*, IPR2022-00236, Paper 36 (PTAB August 16, 2023) (U.S. Patent No. 9,824,035)
1043	[intentionally omitted]
1044	Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021) (asserting U.S. Patent No. 10,860,506)
1045	First Amended Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. May 3, 2022)
1046	U.S. Patent No. 10,860,506
1047	Final Written Decision in *Inter Partes* Review, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, IPR2022-00711, Paper 42 (PTAB Oct. 17, 2023) (U.S. Patent No. 10,860,506)

Exhibit #	Description
1048	Joint 4-3 Claim Construction and Prehearing Statement, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Aug. 19, 2022 and Aug. 23, 2022)
1049	Joint Claim Construction Chart Pursuant to P.R. 4-5(d), *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Sept. 30, 2022)
1050	Claim Construction Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Dec. 14, 2022)
1051	Defendants' Objections to Claim Construction Memorandum Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. Dec. 29, 2022)
1052	File History of U.S. Patent No. 10,860,506
1053	Complaint, *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (asserting U.S. Patent No. 10,860,506)
1054	Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Aug. 1, 2022)
1055	First Amended Complaint, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Aug. 15, 2022)
1056	Netlist's motion to amend its complaint to assert U.S. Patent No. 10,268,608, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023)
1057	Netlist's proposed Second Amended Complaint asserting U.S. Patent No. 10,268,608 in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. Jan. 20, 2023)
1058	JEDEC DDR4DB02 Data Buffer Definition Standard, JESD82-32A (Aug. 2019)
1059	[intentionally omitted]

Exhibit #	Description
1060	[intentionally omitted]
1061	[intentionally omitted]
1062	[intentionally omitted]
1063	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1064	Federal Court Management Statistics (June 30, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/06/30-2>
1067	Samsung Petition, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00847, Paper 1 (PTAB April 27, 2023) (U.S. Patent No. 10,268,608)
1068	Decision Granting Institution of *Inter Partes* Review, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00847, Paper 13 (PTAB December 12, 2023) (U.S. Patent No. 10,268,608)
1069	Micron Petition, *Micron Tech, Inc. et al. v. Netlist, Inc.*, IPR2022-00237, Paper 1 (PTAB July December 23, 2021) (U.S. Patent No. 10,268,608)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1[pre]	1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
1[a]	a module board having edge connections for coupling to respective signal lines in the memory bus;
1[b]	a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
1[c]	memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
1[d]	a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,
1[e]	wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,
1[f]	wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ref. #	Listing of Challenged Claims
2[a]	2. The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation,
2[b]	wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation,
2[c]	wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals,
2[d]	wherein the at least one of the module control signals include at least one of the first set of module control signals, and
2[e]	wherein the signal through the data path is a signal associated with the second memory operation.
3[a]	3. The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks,
3[b]	wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and
3[c]	wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.
4	4. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
5	5. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

Ref. #	Listing of Challenged Claims
6	6. The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.
7	7. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
8	8. The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.
9[a]	9. The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,
9[b]	wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.
10[a]	10. The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation,
10[b]	the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.
11	11. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
12	12. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

I. PETITIONERS' MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest of this Petition are the Petitioners Micron Technology, Inc.; Micron Semiconductor Products, Inc., and Micron Technology Texas LLC.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 10,268,608 ("'608 Patent").

- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2023-00847 ("Samsung IPR")
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed August 1, 2022); *Netlist, Inc. v. Micron Technology, Inc. et al.*, 2:22-cv-00294 (E.D. Tex. filed August 1, 2022)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)

- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00237
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236
- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2022-00711
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2023-00205
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00730

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Petitioners consent to service of all documents via electronic mail to Winston-IPR-NetList@winston.com.

II. INTRODUCTION

Petitioners respectfully request trial on claims 1-12 of U.S. Patent 10,268,608 ("'608 Patent") (EX1001) based on Hiraishi (EX1005) in combination with various secondary references, none considered during prosecution.

III. COMPLIANCE WITH IPR REQUIREMENTS

A. Grounds for Standing (§42.104(a))

Petitioners certify that the '608 Patent is available for IPR and that Petitioners are not barred or estopped from requesting an IPR on the grounds below.

B. Identification of Challenge (§42.104(b))

Petitioners challenge claims 1-12 of the '608 Patent under §103(a) as follows:

	Ground	Claims
1	Hiraishi + Butt	1-12
2	Ground 1 + Tokuhiro	1-12
3	(Ground 1 or 2) + Ellsberry	5, 12
4	(Ground 1 or 2) + Kim	6-8
5	(Ground 1 or 2) + Kim and Ellsberry	8

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date

The '608 Patent claims priority to a provisional application filed July 27, 2012, EX1001; EX1025, which is after Petitioners' prior art. For IPR purposes only, Petitioners assume this date as the effective filing date.

B. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the '608 Patent's field in July 2012 would have been someone with an advanced electrical or computer engineering degree and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of field work experience. EX1003, ¶37. A POSITA would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including standard-compliant DRAM and SDRAM devices, and their interaction with computer components, such as memory controllers. *Id.* A POSITA would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other memory components. *Id.*

C. The '608 Patent

1. Overview

The '608 Patent discloses a memory module (110) including memory devices (112, green) organized in groups, each group with an associated data buffer (118, blue) and one module control device (116, red). EX1003, ¶38; EX1001, 3:25-27, 3:51-54, FIG.2C (below).[1]

[1] All emphasis and color highlighting has been added unless otherwise noted.

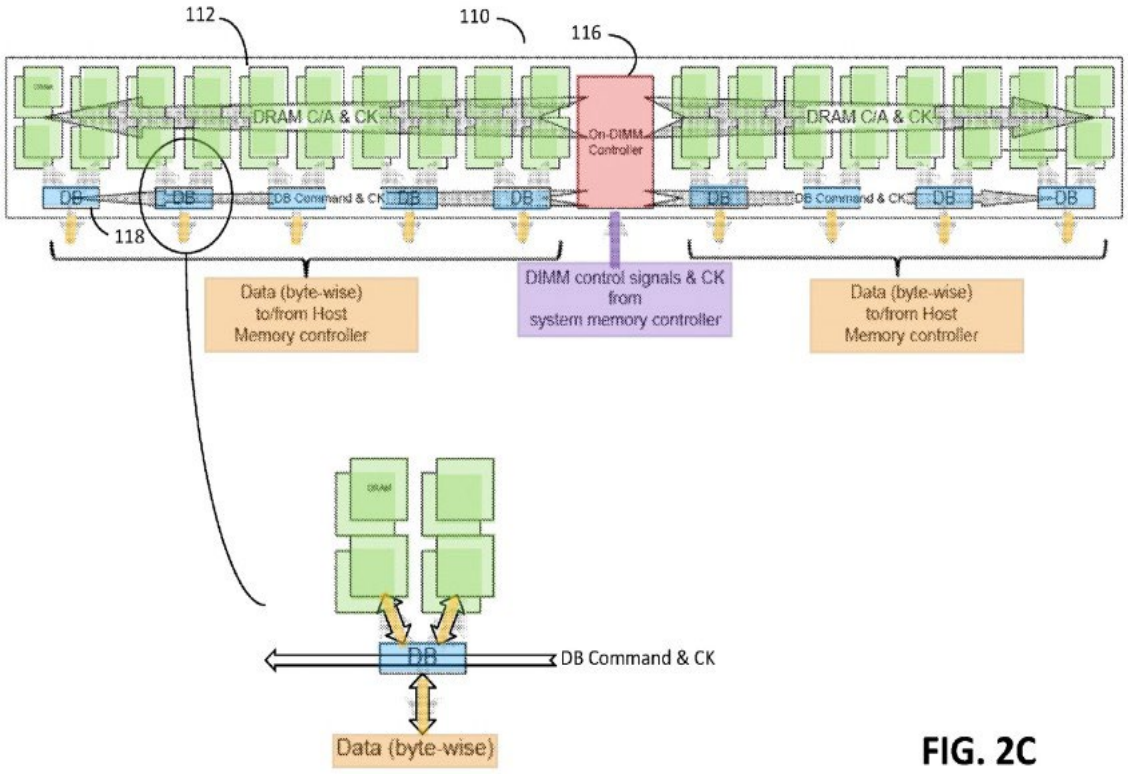

112
110
116
DRAM C/A & CK
On-DIMM Controller
DRAM C/A & CK
DB
DB
DB Command & CK
DB
DB
DB
DB Command & CK
DB
DB
118
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
DRAM
DB
DB Command & CK
Data (byte-wise)

FIG. 2C

As shown below, the memory module (110) is connected to a memory controller (MCH) (101) with a bus including control/address (C/A) signal lines (120, purple) to the module controller (116, red) and data/strobe signal lines (130, orange) to the data buffers (118, blue) which communicate data with respective groups of memory devices 112 (green). EX1003, ¶¶39-40; EX1001, 3:29-34, 4:20-32, FIG.1 (below).

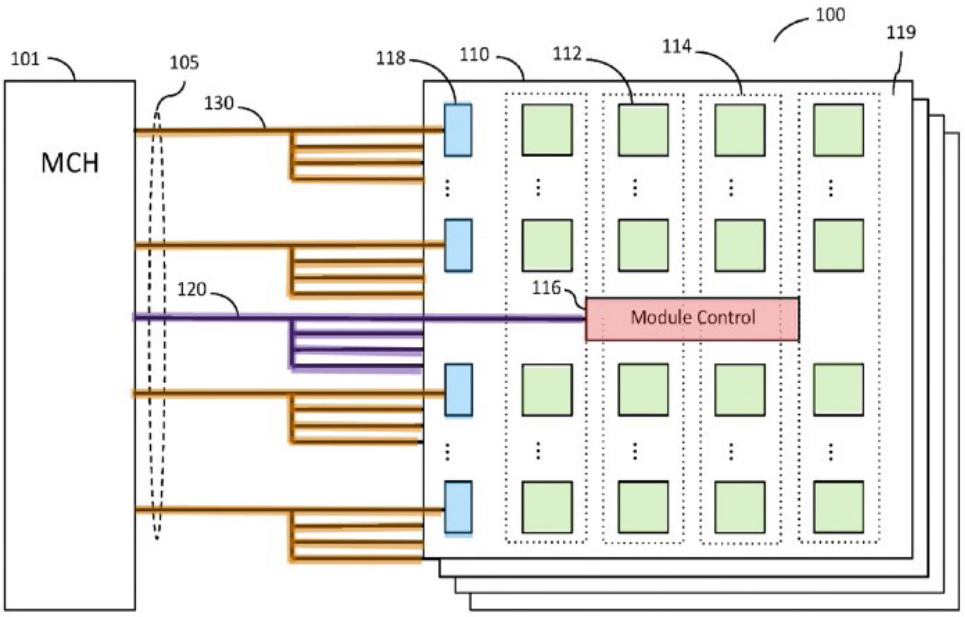


FIG. 1

The module controller (116, red) receives system commands from the memory controller (101) and generates from them module command signals for the memory devices and module control signals for the data buffers. EX1003, ¶¶41- 42; EX1001, 4:27-30, 4:65-5:7, 5:57-65, *see also id.* FIGS. 2A-2B, 6:12-29, 4:60-64.

Because the data buffers (blue) and associated memory devices (green) are distributed across the memory module, "a same set of module control signals may reach different [data buffers (blue)] at different times across more than one clock cycle of the system clock." EX1003, ¶43; EX1001, 9:52-10:6, 10:7-21. The '608 Patent purports to solve this "fly-by" problem by each data buffer determining a time interval based on signal timing during a write operation—in particular, the difference (EWD) between reception of a ***write command*** (W/C) and reception of the corresponding data strobe (DQS1) (FIG.12A, below)—which is then used to adjust signal timing during memory ***read operations*** (FIG.12B, below). EX1003, ¶44; EX1001, 15:27-50, 15:66-16:9, FIGS. 12A-12B.

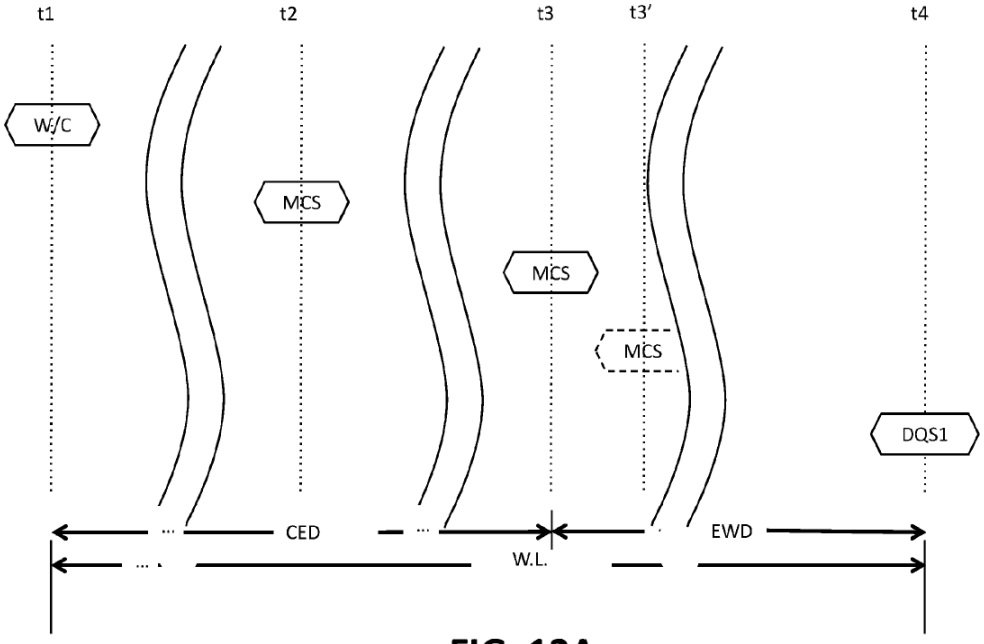


FIG. 12A

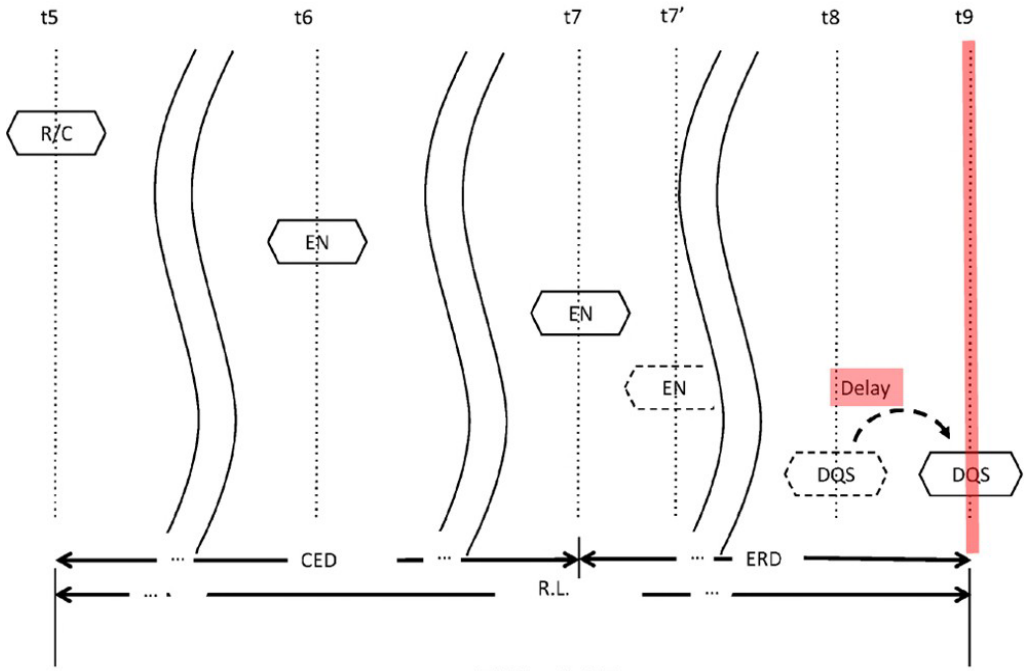


FIG. 12B

2. Prosecution History

The ’608 Patent claims are not patentably distinct from the claims of parent U.S. Patent No. 9,824,035 (“the ’035 Patent”) and child U.S. Patent No. 10,860,506 (“the ‘506 Patent”). EX1003, ¶¶54-64, 67-69; EX1031; EX1046; EX1052, pp.140-51, 185-86; EX1002, pp.83-91, 102-03. The Board found all ’506 claims and most ’035 claims unpatentable in final written decisions involving Petitioners. EX1040; EX1042; EX1047. While the Board denied Petitioners’ earlier ’608 petition based on different grounds than here, EX1041, the Board found all ’608 claims unpatentable by final written decision in the IPR that this petition seeks to join, EX1041.

The ’608 Patent has the same written description as grandparent U.S. Patent No. 9,128,632 (“the ’632 Patent”). EX1003, ¶¶45-47; EX1002, p.36; EX1010. The

Board denied instituting an IPR on the '632 Patent (IPR2017-00730) based on specific claim language not found in the '608 Patent. EX1003, ¶¶50-53; EX1014, pp.10-14. Netlist disclosed nothing about the '632 IPR or cited art during prosecution. EX1003, ¶53; EX1002.

D. Construction of Claim Terms

The Board need not expressly construe any claim term because the prior art invalidates the claims under any plausible construction, in accordance with 37 C.F.R. §42.100(b). Examples of how the '608 Patent uses these terms is shown below:

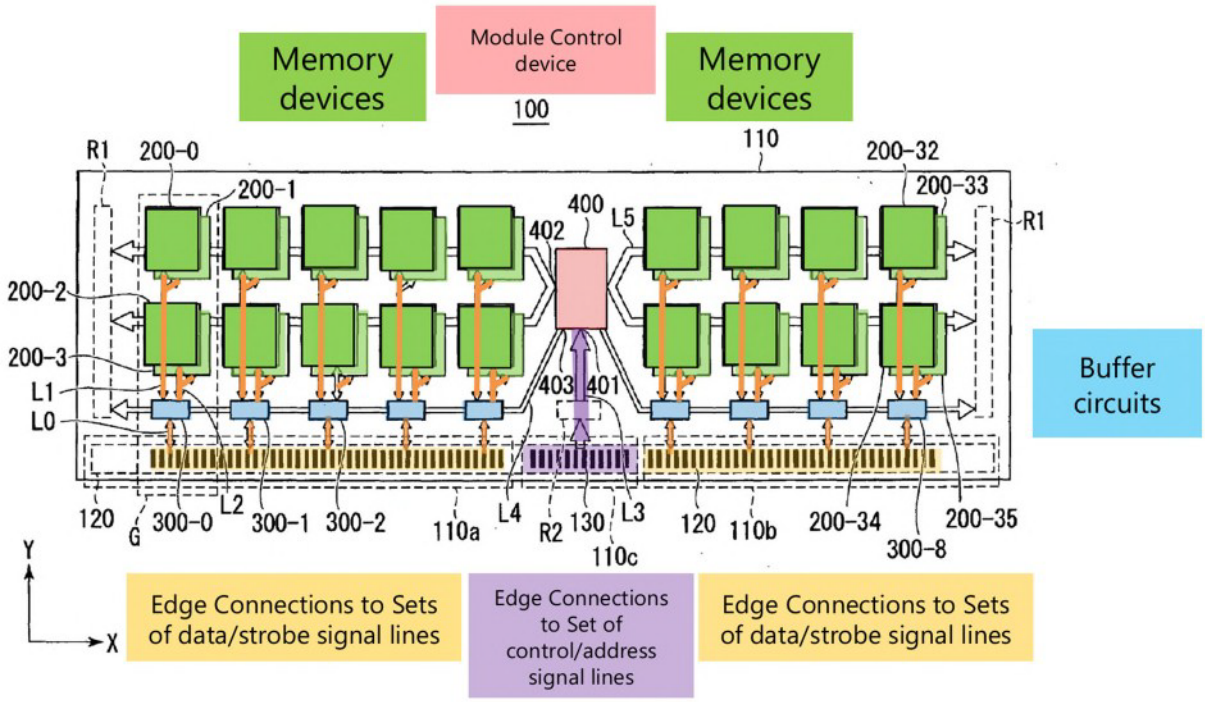
Term	EX1001	EX1003
"memory operation"	3:29-34, 5:58-63	¶76
"memory module"	1:50-55; *see also* EX1023, p.334	¶¶77-78
"memory controller"	4:47-49	¶79
"memory bus"	4:50-58	¶80
"system command signals"	3:29-38, 4:65-5:4	¶¶81-82
"module command signals"	3:41-46, 5:58-63, 5:27-42	¶¶83-84
"module control signals"	3:41-50, 4:27-30, 5:43-51	¶¶85-86
"metastability"	9:42-45	¶¶87-88

V. PRIOR ART OVERVIEW

A. Hiraishi (EX1005)

US2010/0312956 ("Hiraishi"), published in 2010, is §102(b) art. Hiraishi was not cited or discussed during prosecution. EX1002; EX1003, ¶¶89-97.

Figures 1 and 7 of Hiraishi, below illustrate that Hiraishi's memory module includes a central "command/address/control register buffer" (red) and a fly-by configuration of "memory chips" (green) and "data register buffers" (blue). EX1005, ¶¶[0045-49], [0051-52], [0055-56], [0059-61], [0103], [0107].


Memory devices
Module Control device
100
Memory devices
R1
200-0
200-1
110
200-32
200-33
R1
400
L5
402
200-2
200-3
L1
L0
403
401
Buffer circuits
120
G
300-0
L2
300-1
300-2
110a
L4
R2
130
L3
110c
120
110b
200-34
300-8
200-35
Y
X
Edge Connections to Sets of data/strobe signal lines
Edge Connections to Set of control/address signal lines
Edge Connections to Sets of data/strobe signal lines

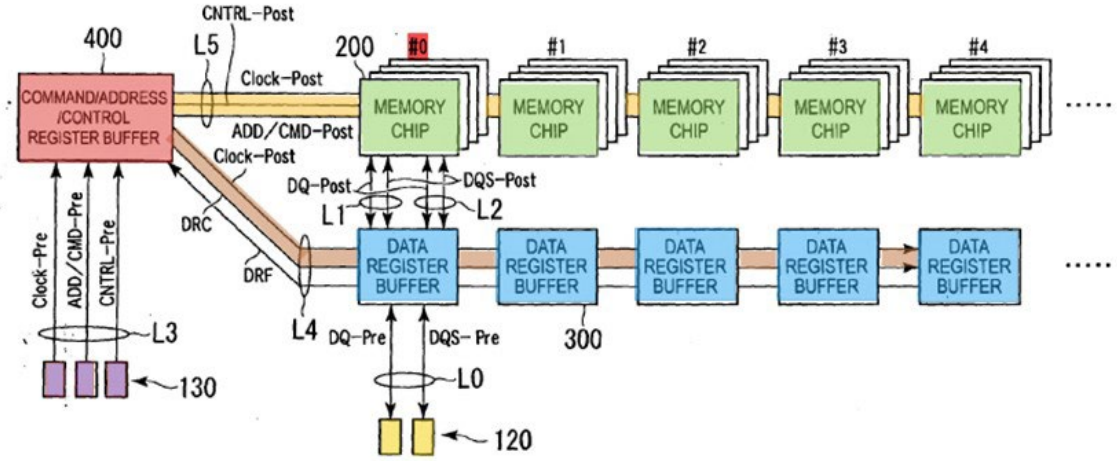

400
CNTRL-Post
L5
200
#0
#1
#2
#3
#4
COMMAND/ADDRESS /CONTROL REGISTER BUFFER
Clock-Post
MEMORY CHIP
ADD/CMD-Post
Clock-Post
DQ-Post
DQS-Post
L1
L2
DRC
DRF
DATA REGISTER BUFFER
Clock-Pre
ADD/CMD-Pre
CNTRL-Pre
L3
130
L4
DQ-Pre
DQS-Pre
300
L0
120

FIG.7

Hiraishi's data register buffers make timing adjustments to account for signal timing discrepancies by performing write and read leveling operations using leveling circuits 322 and 323. Figure 5 (below); EX1005, ¶¶[0084], [0087], [0090], [0104],

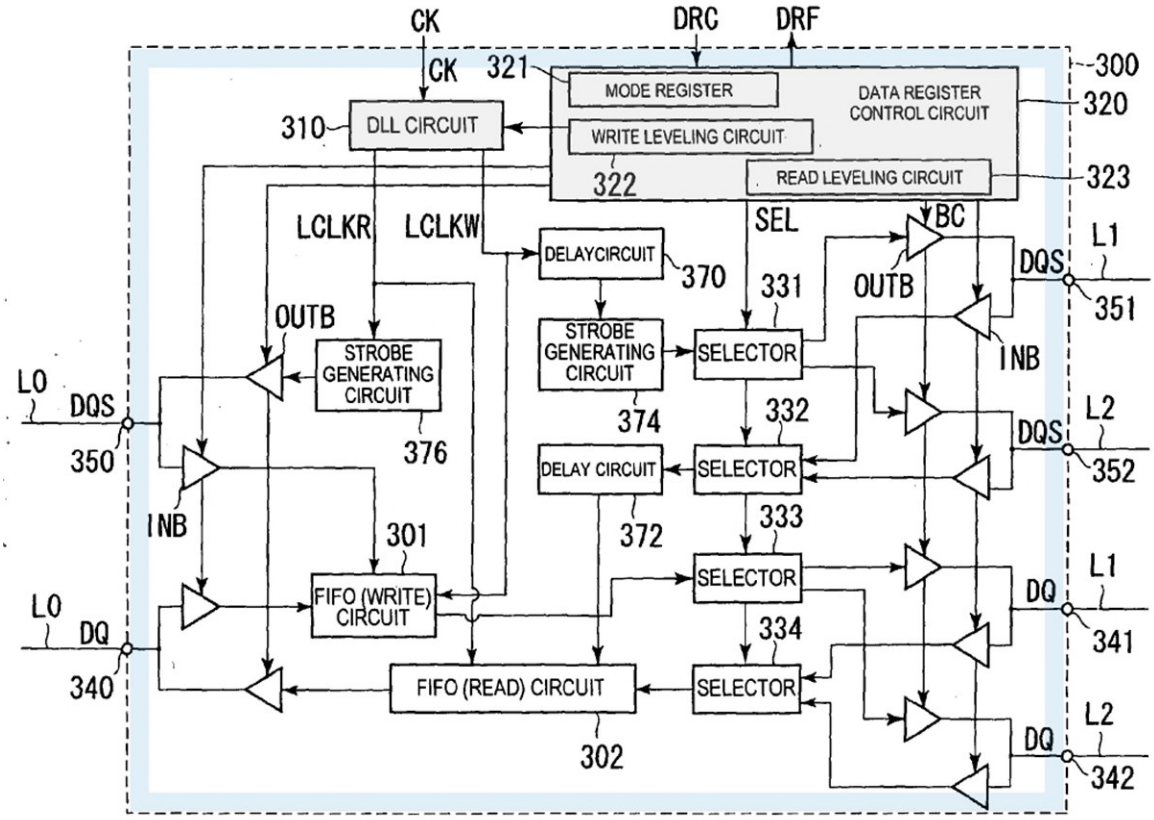


FIG.5

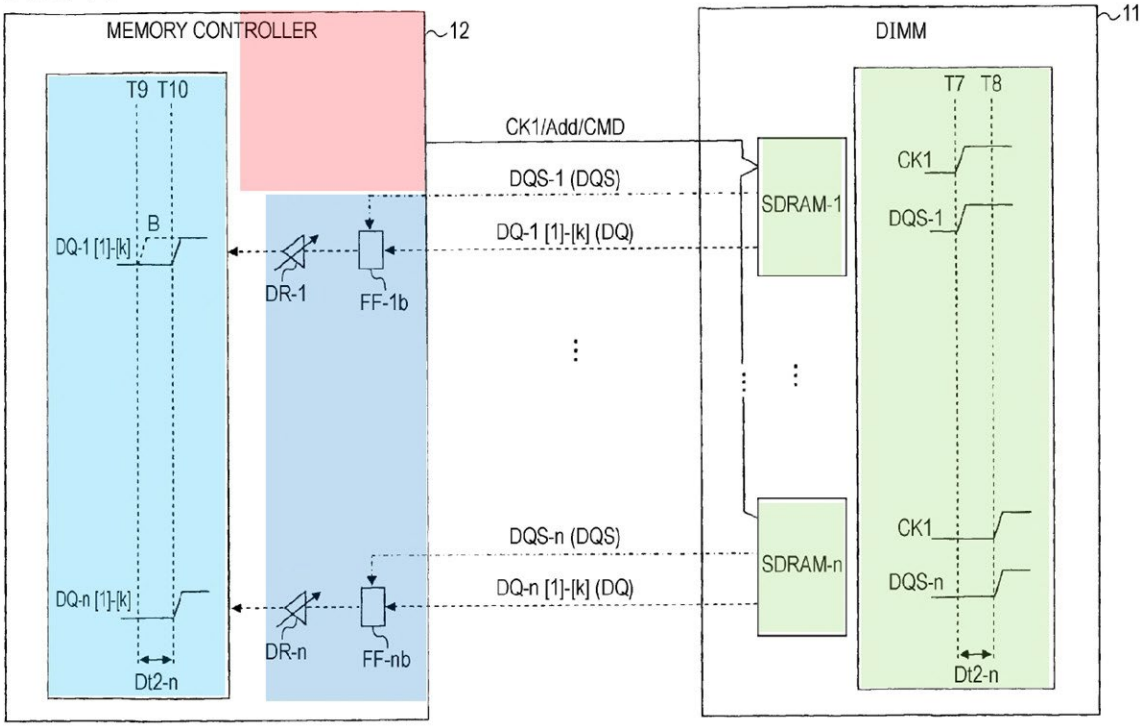
[0140-42], [0147].

B. Tokuhiro (EX1006)

U.S. Patent No. 8,020,022 to Tokuhiro ("Tokuhiro"), issued in 2011, is §102(a), (e) art. Tokuhiro was not cited or discussed during prosecution. EX1002; EX1003, ¶¶98-102.

Tokuhiro recognizes the problems of fly-by delays, and proposes using a ***write*** delay to compensate for delays during ***read*** operations. EX1003, ¶¶101-102; EX1006, 1:63-2:9, 2:10-12, 2:54-59, 3:1-12, 3:16-26, FIG.11 (below).

FIG. 11



C. Ellsberry (EX1007)

US2006/0277355 to Ellsberry ("Ellsberry"), published in 2006, is §102(b) art. Ellsberry was cited among hundreds of references but not discussed during prosecution. EX1002, p.151; EX1003, ¶¶103-104. Ellsberry discloses using either 8-bit wide memory devices, EX1007, FIG.13 (below left, green), or pairs of 4-bit wide memory devices, *id.* FIG.11 (below right, green), in alternative implementations.

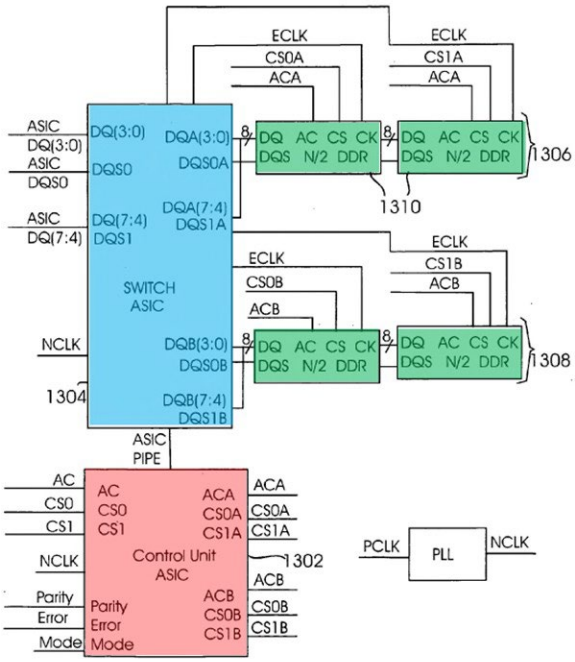


Fig. 13

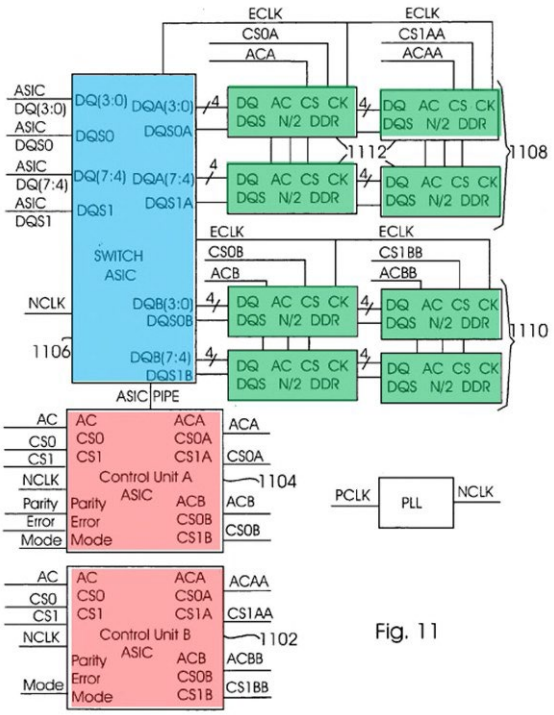


Fig. 11

D. Butt (EX1029)

US2007/0008791 ("Butt"), published in 2007, is §102(b) art. Butt was not cited or discussed during prosecution. EX1002; EX1003, ¶¶105-109. Butt discloses the details of buffering and adjusting DQ/DQS signals in the data paths (104). EX1029, FIG.2 (below).

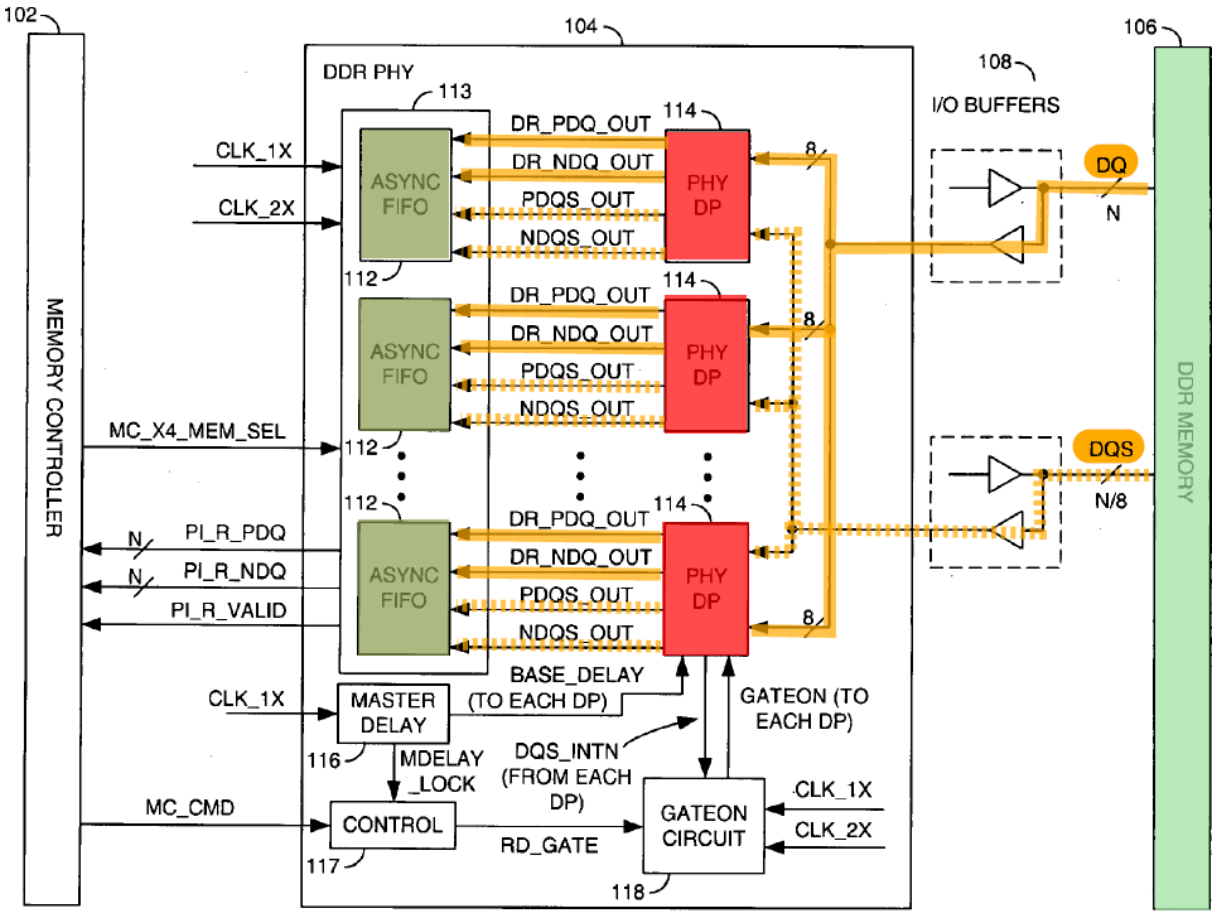


FIG. 2

E. Kim (EX1008)

U.S. Patent No. 6,184,701 to Kim ("Kim"), issued in 2001, is §102(a), (b) art. Kim was not cited or discussed during prosecution. EX1002; EX1003, ¶¶110-111. Kim discloses "a metastability detection/prevention circuit" to be incorporated with any "main active circuit" in need thereof. EX1008, 2:21-22.

VI. PRECISE REASONS FOR RELIEF REQUESTED

Regardless of a broad or narrow interpretation, the '608 Patent claims are invalid. In litigation, Netlist has broadly interpreted "*memory operations*" to include

read leveling and subsequent read operations, and a "*delay…determined by the command processing circuit*" to include programming by the system memory controller. EX1003, ¶113; *see also* EX1035, ¶¶90-91, 121; EX1048, 54; EX1057, 59-62. The '035 and '608 Patents, however, teach that the buffer circuit determines a delay in the direction of a write operation and applies the delay to read data in subsequent read operations. EX1001, 2:28-36, 15:23-16:9, FIGS. 12A-B. The '608 Patent claims are invalid under both Netlist's broader interpretation, *infra* pp.14-71, and narrower interpretation more consistent with the specification and the file history, *infra* pp.72-107.

Netlist has also interpreted the claims broadly to include a single bi-directional "data path" between the buffer circuit and memory devices. EX1003, ¶114; EX1035, ¶¶118-19. The '608 Patent, in contrast, discloses a "fork in the road" layout (e.g., two bi-directional data paths, going to memory devices in two ranks, totaling four ranks). *Id.* The prior art invalidates the claims under either interpretation. *Id*.; *infra* pp.56-58, 66-71.

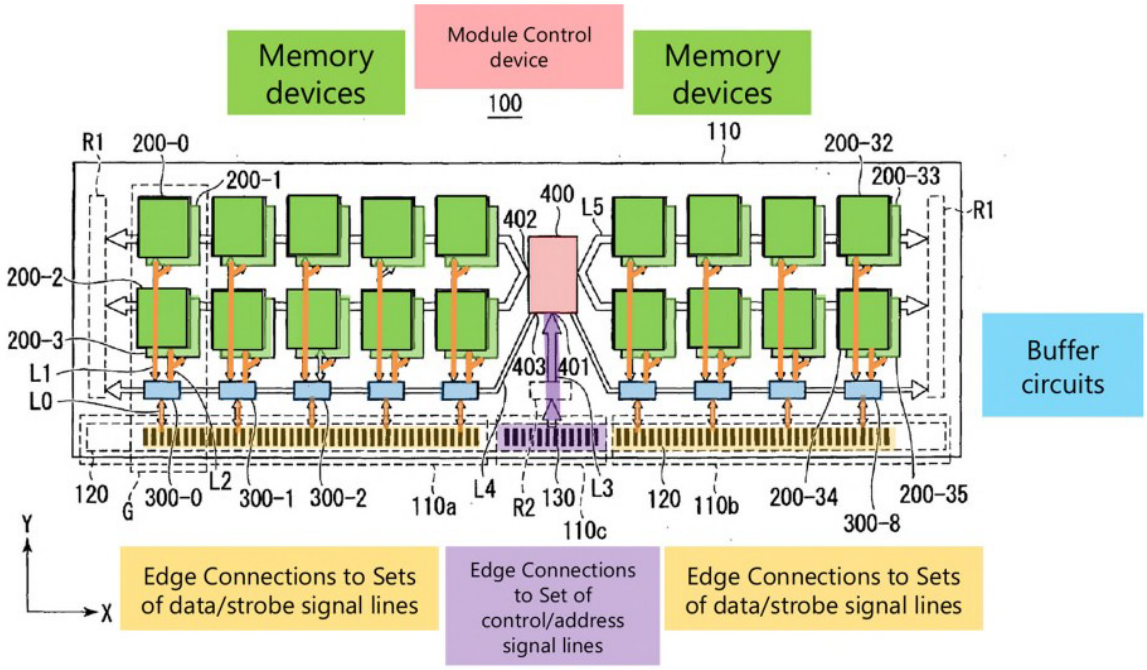
A. Ground 1: Hiraishi + Butt (claims 1-12)

1. Claim 1

a) 1[pre]

Hiraishi discloses "a memory module [e.g., memory module 100] operable to communicate with a memory controller [MCH 12 in FIGS. 2-3] via a memory bus [line 23 in FIG.3], the memory bus including signal lines, the signal lines including

a set of control/address signal lines [to couple to command/address/control line L3 on the module, purple] and a plurality of sets of data/strobe signal lines [to couple to data line L0 on the module, orange]":



EX1003, ¶115; EX1005, FIG.1.

Memory module 100 is operable to communicate with the memory controller (MCH 12) via a memory bus (line 23) coupled to data line L0 and the command/address/control line L3 (above) on the memory module 100.

EX1003, ¶116; EX1005, ¶¶[0065], [0069], FIGS.2-3 (below).

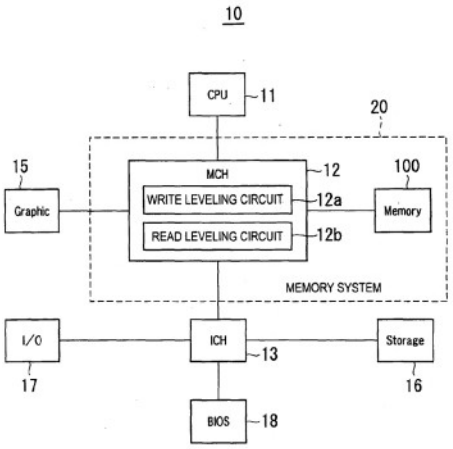


FIG.2

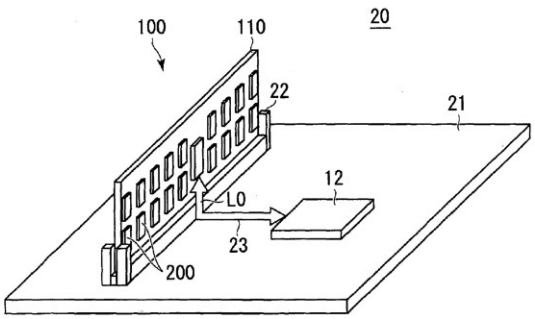


FIG.3

The memory bus (line 23) includes a set of control/address signal lines coupling, through connectors 130 (purple), to command/address/control line L3, and multiple sets of data/strobe signal lines, each set coupling, through connectors 120 (orange), to data line L0. EX1003, ¶117; EX1005, ¶¶[0047], [0049], [0069], [0102]-[0103], FIGS.1&7.

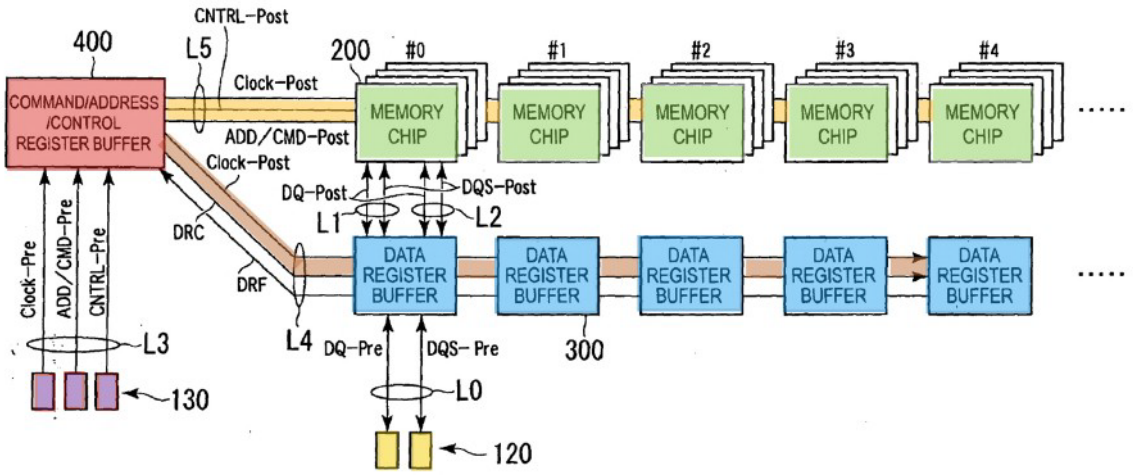
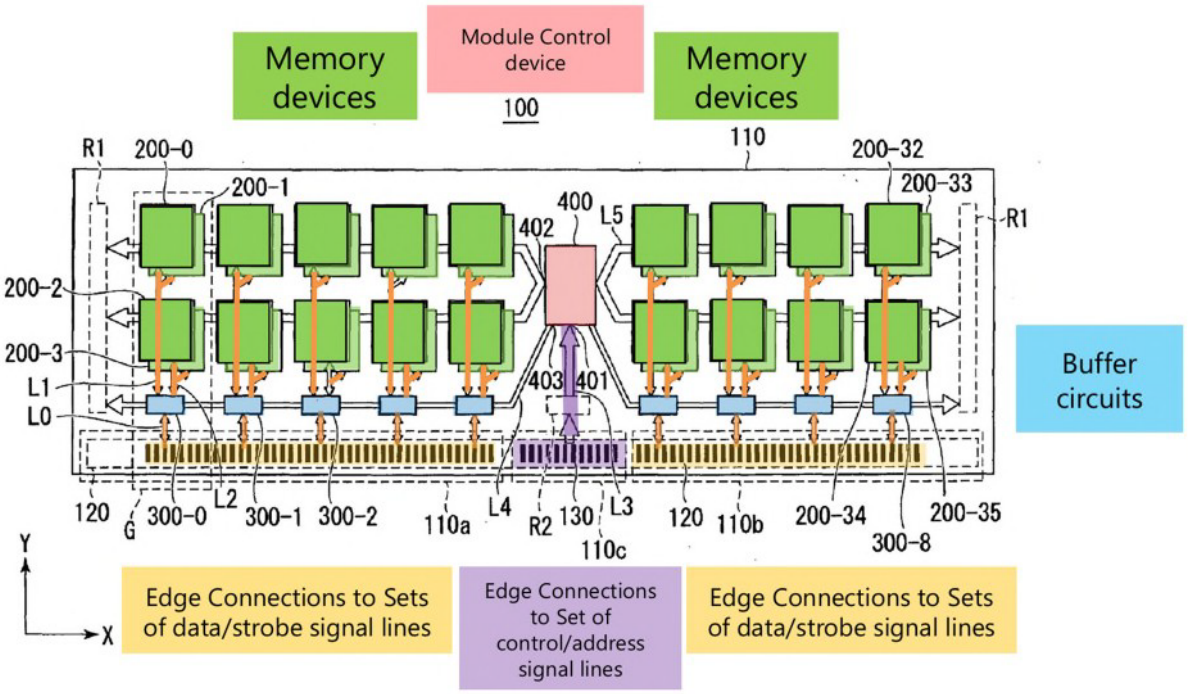


FIG.7

b) 1[a]: module board

Hiraishi discloses "*a module board* [module substrate 110] *having edge connections* [including command/address/control connectors 130 (purple) and data connectors 120 (orange)] *for coupling to respective signal lines in the memory bus* [line 23, above in FIG.3]":



EX1003, ¶118; EX1005, FIG.1.

Memory module 100 includes a "module substrate 110 [which] is a printed circuit board" (PCB) having "*edge connections*" 120 and 130 at its edge for coupling to respective signal lines in the memory bus connected to the memory controller (MCH 12 in FIGS. 2-3 above). EX1003, ¶¶119-121; EX1005, ¶¶[0045- 49]; *compare* EX1005, FIG.1 (above), *with* EX1001, FIG.2C (below).

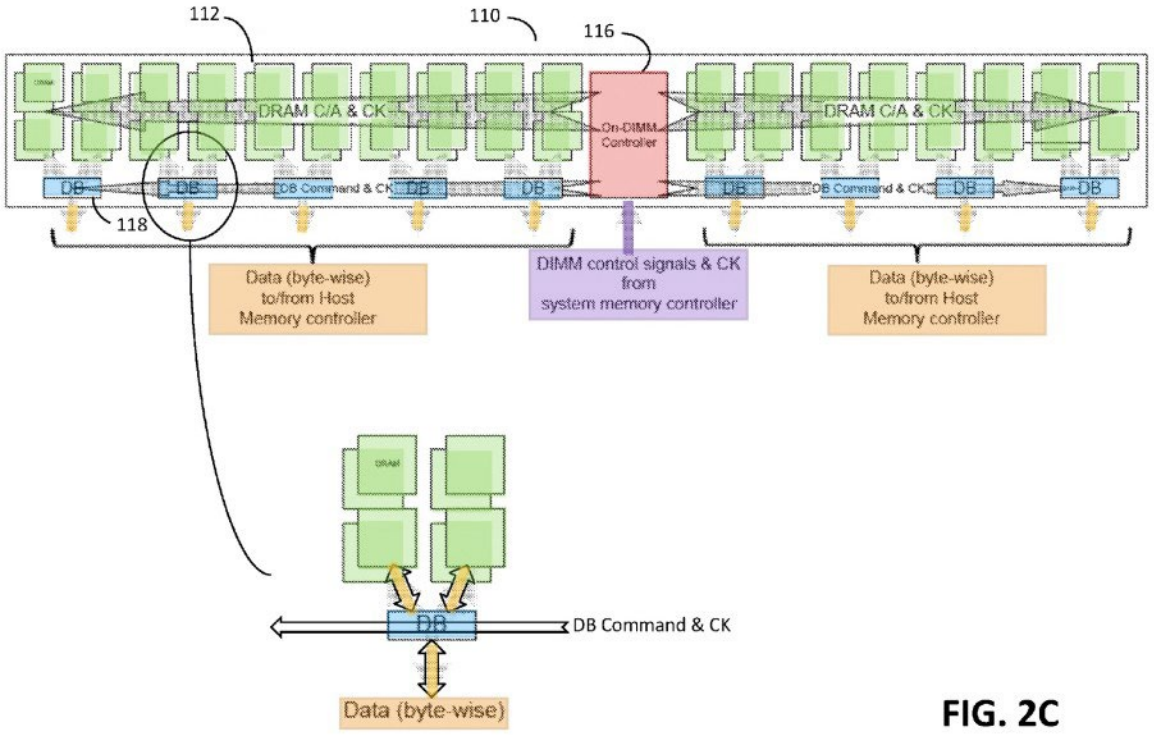
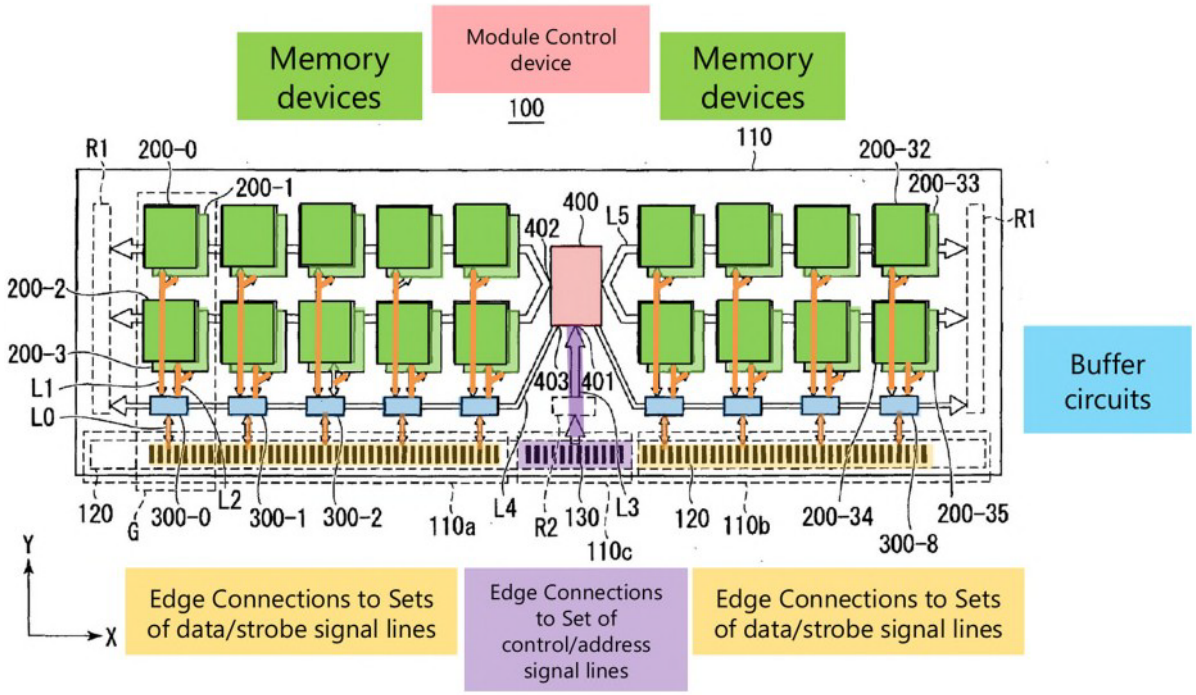


FIG. 2C

c) 1[b]: module control device

Hiraishi discloses "*a module control device* [command/address/control register buffer 400, red] *mounted on the module board* [substrate 110]":



EX1003, ¶¶122-123; EX1005, ¶[0059], FIG.1.

The "module control device" (400, red, FIGS. 1, 6-7) is "configured to receive system command signals for memory operations [e.g., read or write operations] via the set of control/address signal lines [through command/address/control connectors 130 and command/address/control line L3 (FIG.7) at input terminal 401 (FIG.6, purple)] and to output module command signals [ADD/CMD-Post in module command/address/control line L5 (FIG.7) at output terminal 402 (FIG.6, orange)] and module control signals [including DRC, brown, on control line L4 (FIG.7) at output terminal 403 (FIG.6)] in response to the system command signals [received on command/address/control connectors 130 (FIG.7, purple)], the module control

device being further configured to receive a system clock signal [Clock-Pre in L3] and output a module clock signal [Clock-Post in L4 and L5]."

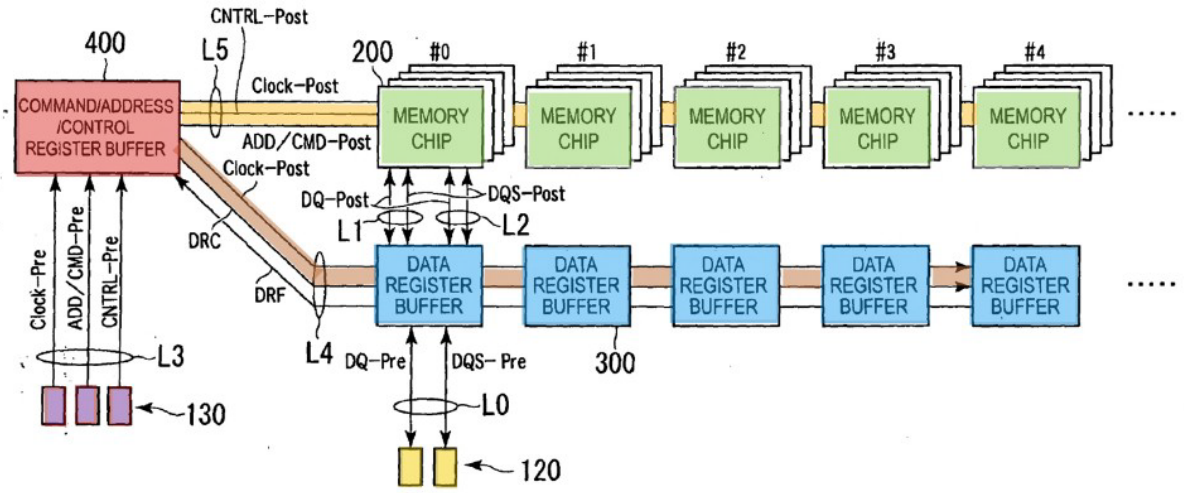


FIG.7

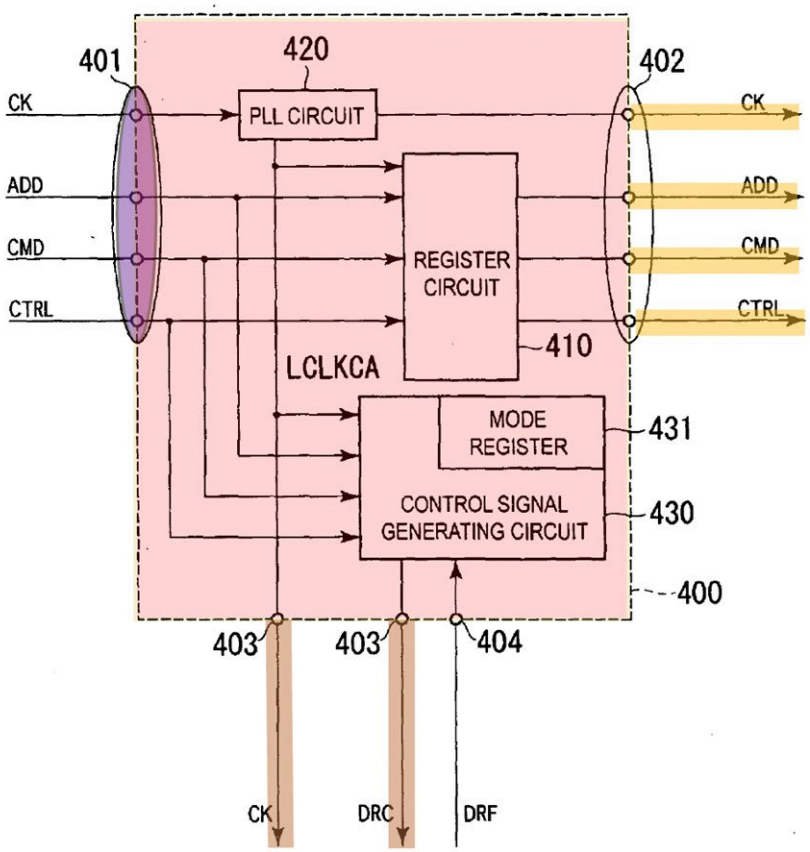


FIG.6

EX1003, ¶124; EX1005, ¶¶[0018]-[0019], FIGS.6-7.

Hiraishi teaches that the module control device (400, red) is configured to receive system command signals for memory operations from the memory controller via the set of control/address signal lines (EX1003, ¶125; EX1005, ¶¶[0047], [0060], [0097]) and output module command signals and module control signals in response to the system command signals (EX1003, ¶¶126-127; EX1005, ¶¶[0060], [0097], [0099]). Hiraishi further teaches that the module control device (400) is configured

to receive a system clock signal (Clock-Pre) and output a module clock signal (Clock-Post). EX1003, ¶128; EX1005, ¶[0108], FIGS. 6-7.

Hiraishi discloses that memory operations can include read or write operations. EX1005, ¶¶[0122]-[0136]. Figures 11 and 12 (below) show the timing of a read and write operation, including the Command/Address/Control Register Buffer (red) receiving a read or write command (red box) on line CMD(IN) (orange), and outputting corresponding signals on line CMD(OUT) (orange) to the memory chips (green) and on line CONTROL SIGNAL(OUT) (brown) to the Data Register Buffer (blue). As also shown in these figures, the command and control signals are accompanied by corresponding clock signals (yellow).

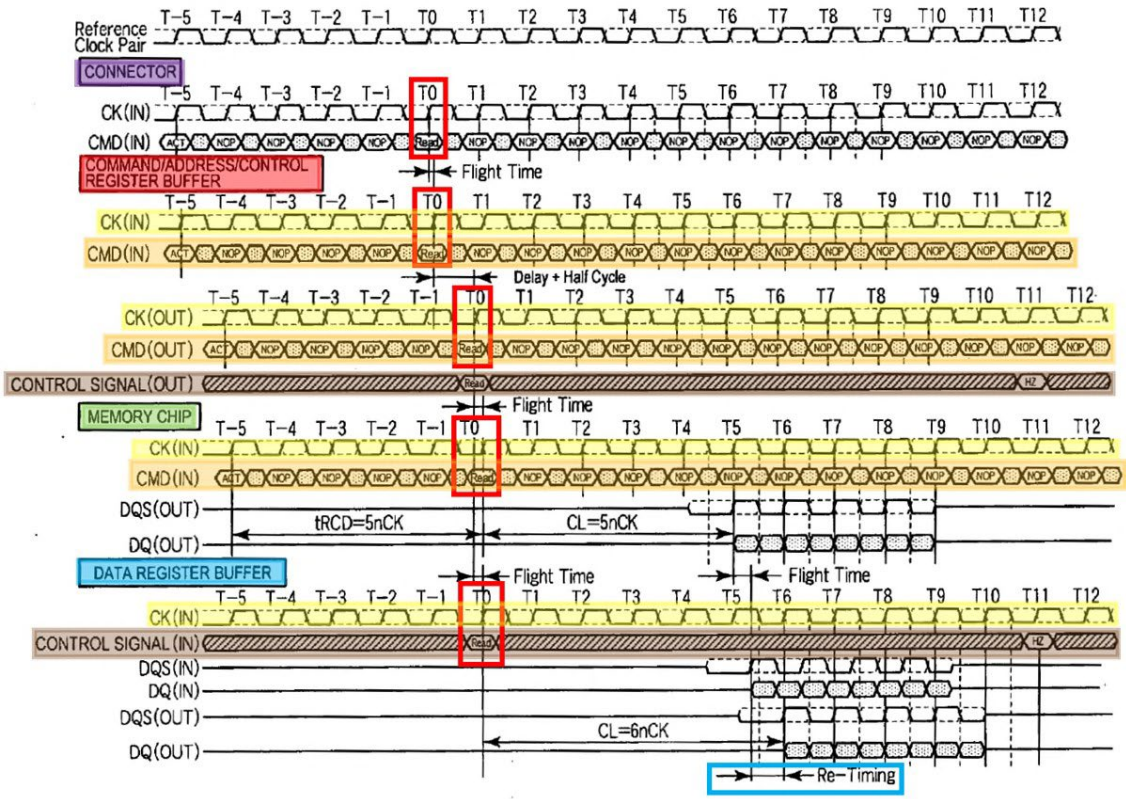

Reference Clock Pair
CONNECTOR
CK(IN)
CMD(IN)
COMMAND/ADDRESS/CONTROL REGISTER BUFFER
Flight Time
Delay + Half Cycle
CK(OUT)
CMD(OUT)
CONTROL SIGNAL(OUT)
MEMORY CHIP
DQS(OUT)
DQ(OUT)
tRCD=5nCK
CL=5nCK
DATA REGISTER BUFFER
CONTROL SIGNAL(IN)
DQS(IN)
DQ(IN)
CL=6nCK
Re-Timing

FIG.11

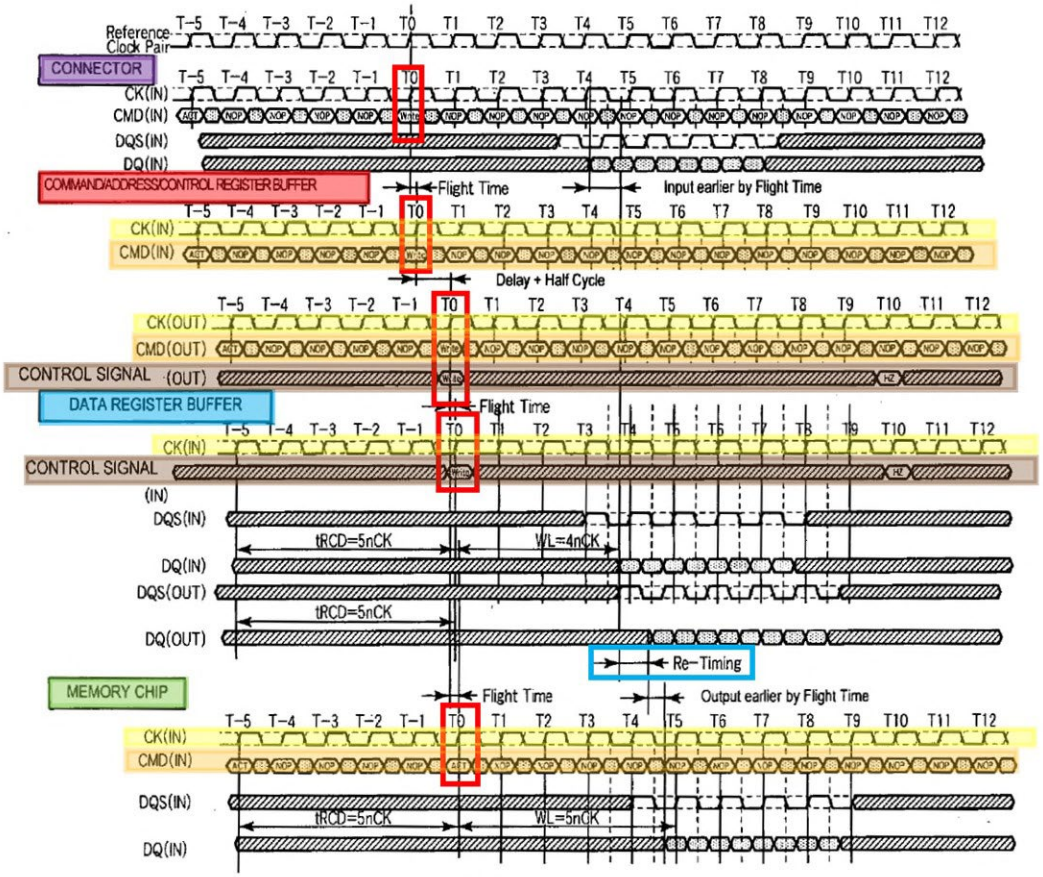


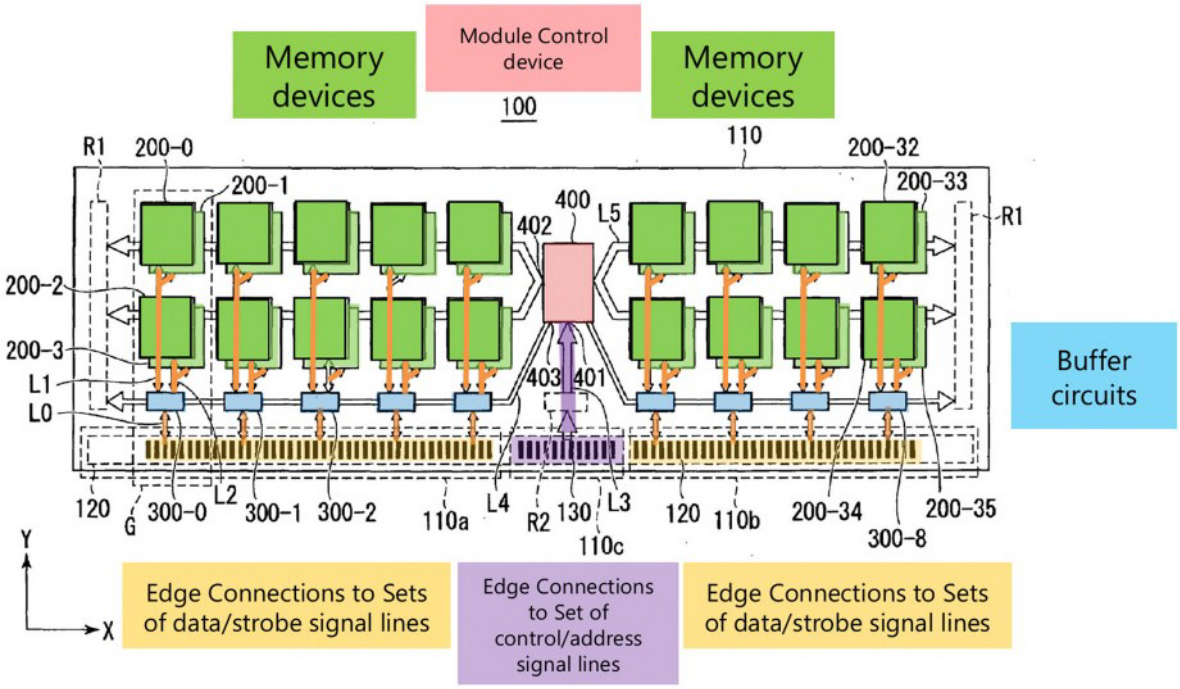
FIG.12

EX1003, ¶129; EX1005, FIGS. 11-12.

d) 1[c]: memory devices

Hiraishi discloses "memory devices [200-0 to 200-35 (green)] mounted on the module board and configured to receive the module command signals [on module command/address/control line L5 (FIG.7)] and the module clock signal [Clock-Post, L5], and to perform the memory operations [e.g., a write or read operation] in response to the module command signals [on line L5], the memory devices including a plurality of sets of memory devices [e.g., a set including memory devices 200-0 to

200-3] corresponding to respective sets of the plurality of sets of data/strobe signal lines [the data/strobe lines coupled to L0]."



EX1003, ¶130; EX1005, FIG.1.

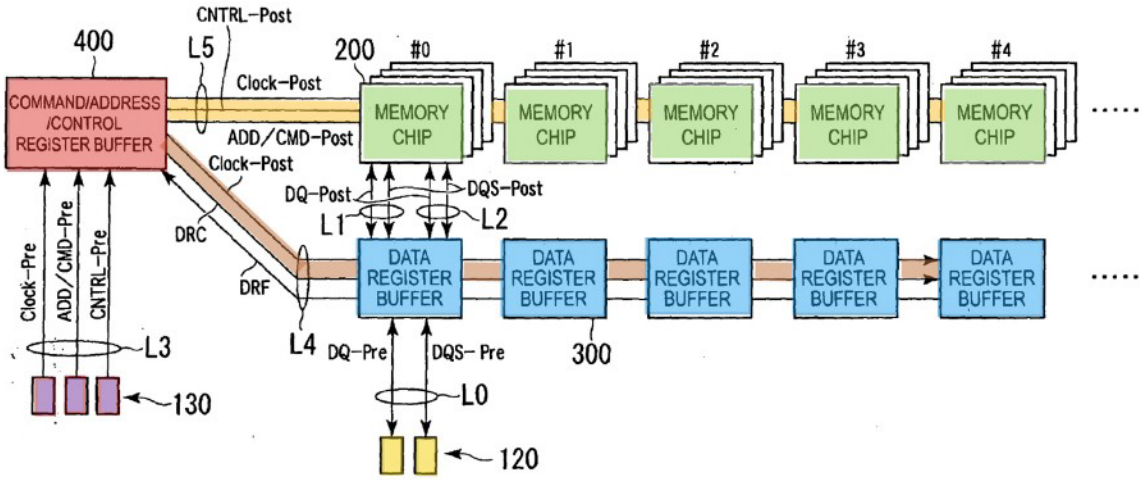


FIG.7

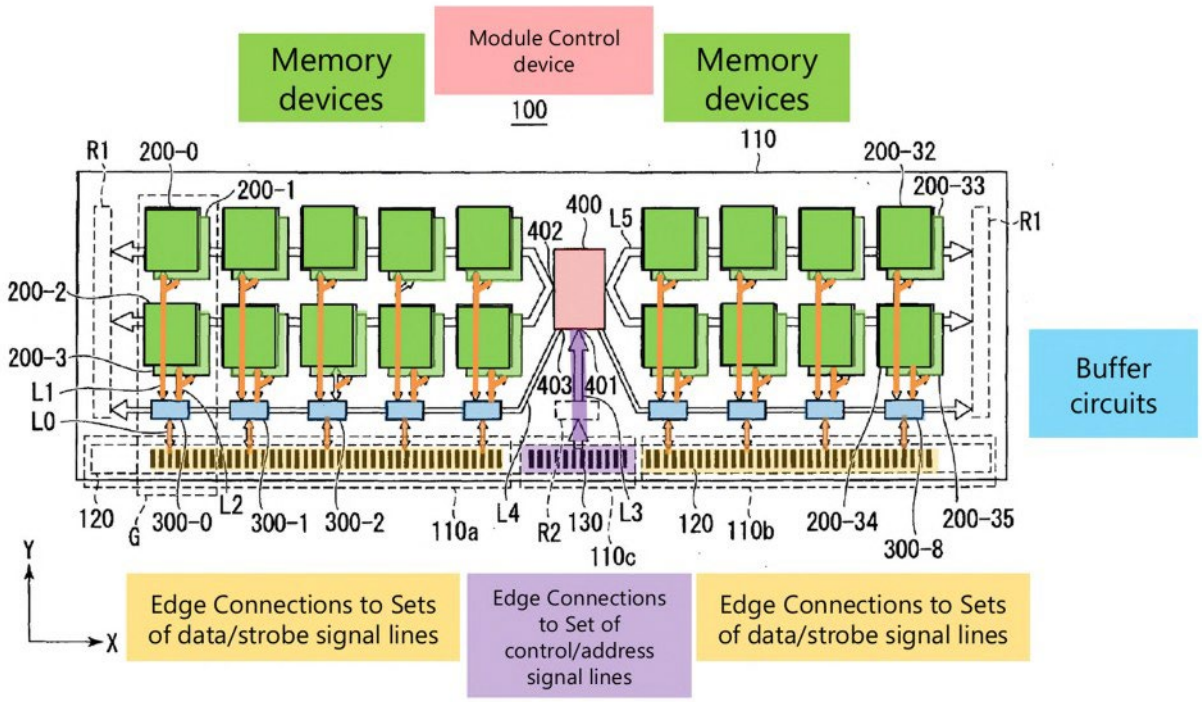
EX1003, ¶130; EX1005, FIG.7.

Hiraishi's module 100 includes memory chips 200 mounted on the module substrate 110 (EX1003, ¶131; EX1005, ¶[0045]) which are configured to receive the module command signals and the module clock signal on L5, and to perform memory operations in response to the module command signals. EX1003, ¶132; EX1005, ¶[0054]. For example, "clock signal CK … to the memory chip 200 … is supplied from … register buffer 400." EX1005, ¶[0108]. The memory operation, e.g., a read or write operation, is performed in response to "ACT" and "Read" or "Write" commands issued by command/address/control register buffer 400. EX1003, ¶132; EX1005, ¶¶[0122]-[0136], FIGS. 11-12; *see also* EX1005, ¶¶[0163], [0170]; EX1020, 33, 56-76.

Hiraishi's memory devices include multiple sets of memory devices (*e.g.*, 200-0 to 200-3), each corresponding to a respective set of data/strobe signal lines. EX1003, ¶133. For example, memory devices 200-0 and 200-1 are connected to data register buffer 300-0 by line L1, memory devices 200-2 and 200-3 connected by line L2, and data register buffer 300-0 is associated with line L0 from the edge connectors 120. EX1003, ¶133; EX1005, ¶¶[0053], [0056], [0103]. Thus, a POSITA would have understood that one set of memory devices (200-0 to 200-3) corresponds to one of the sets of data/strobe signal lines (L0, which comprises DQ- pre and DQS-pre) and that each other set of memory devices corresponds to other respective sets of data/strobe lines (*e.g.*, in FIG.1, a set for each buffer 300-0 through 300-8). EX1003, ¶133.

e) 1[d]: buffer circuits

As shown below, Hiraishi discloses "*a plurality of buffer circuits* [data register buffer circuits 300-0 to 300-8 (blue)] *corresponding to respective sets of the plurality of sets of data/strobe signal lines* [*e.g.*, respective data/strobe signal DQ-Pre and DQS-Pre in L0]":



EX1003, ¶134; EX1005, FIG.1.

Figure 1 above shows nine data register buffers, each corresponding to a group of four memory chips, and each buffering read and write data transferred via line L0 to data lines L1 and L2 and *vice versa*. EX1003, ¶¶135-136; EX1005, ¶¶[0045], [0055-56], [0084], [0017], FIG.5 (below, showing data register buffer 300 being coupled to data(DQ)/strobe(DQS) signal lines L0 on one side and L1/L2 on the other).

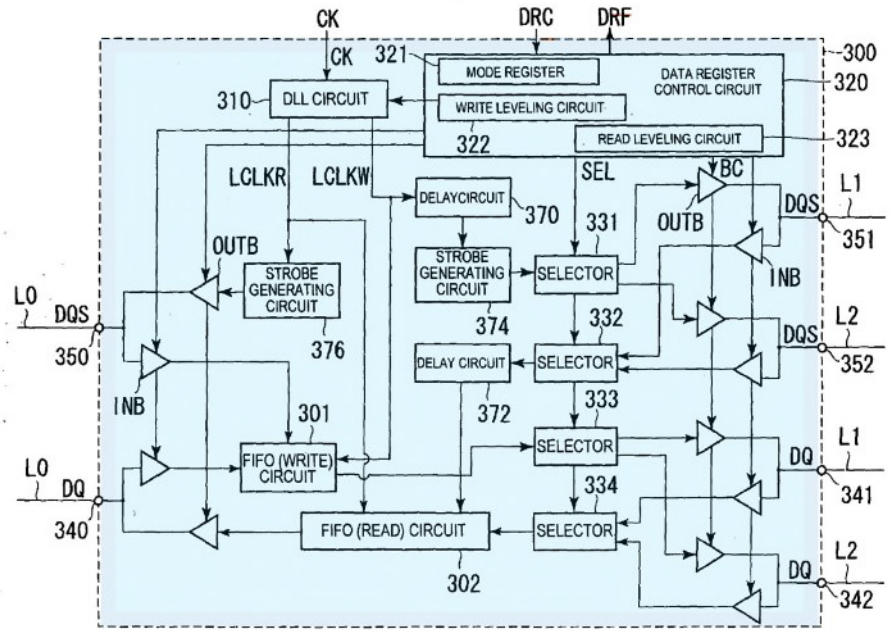


FIG.5

Figure 7 below also confirms coupling of data register buffer 300 to DQ-Pre and DQS-Pre lines in L0. EX1003, ¶137; EX1005, ¶[0103], FIG.7.

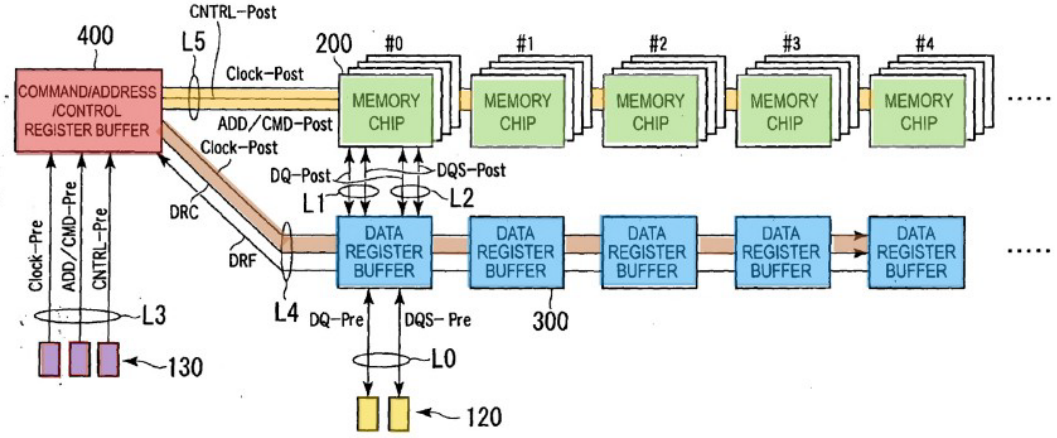
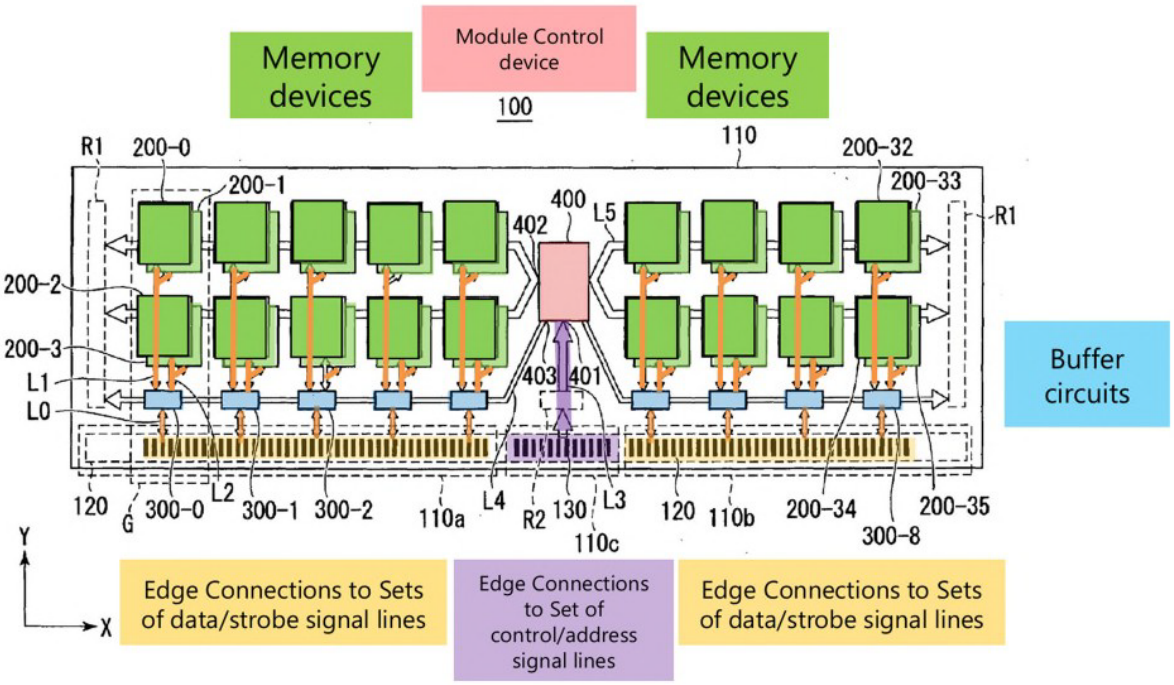


FIG.7

f) 1[e]: first wherein clause; module control signals

As shown below and discussed in 1[d] above, Hiraishi discloses that "each respective buffer circuit of the plurality of buffer circuits is mounted on the module board [data register buffer circuits 300-0 to 300-8, blue], coupled between a respective set of data/strobe signal lines [L0, including lines DQ-Pre and DQS- Pre] and a respective set of memory devices [e.g., memory chips 200-0 to 200-3, connected by data lines L1 and L2, including lines DQ-Post and DQS-Post, to the respective buffer circuit 300]":



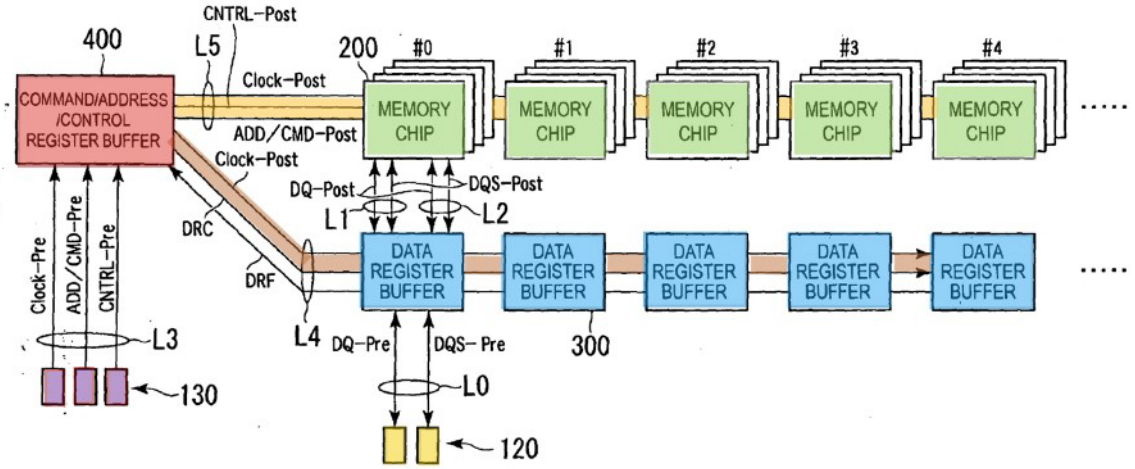


FIG.7

EX1003, ¶¶138-139; EX1005, ¶¶[0045], [0055]-[0056], [0084]-[0085], [0103], FIGS. 1, 7.

As shown by Figures 7 (above) and 5 (below), Hiraishi also discloses that each respective buffer circuit is "*configured to receive the module control signals* [including DRC] *and the module clock signal* [CK (Clock-Post in FIG.7)]."

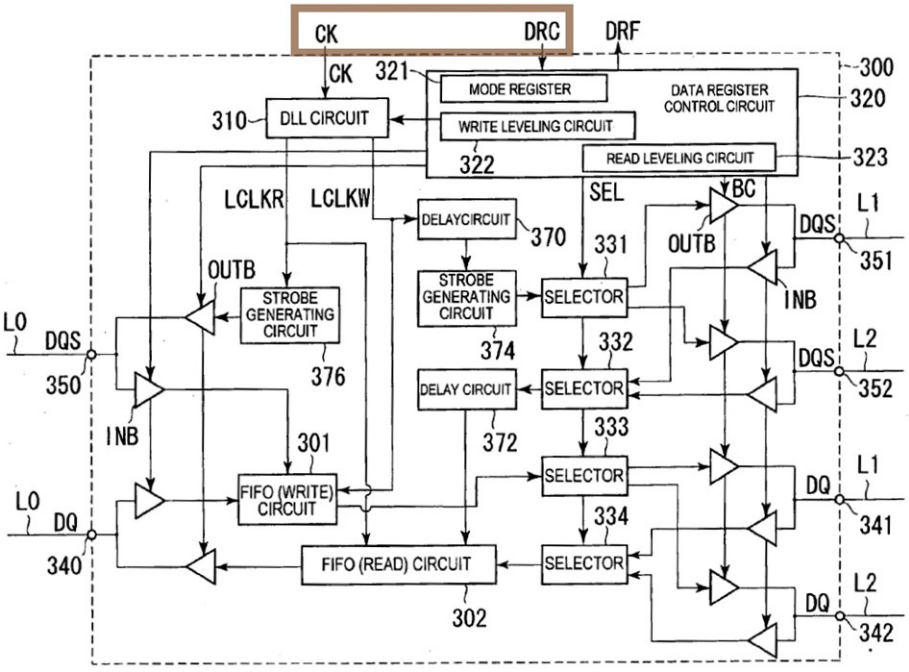


FIG.5

EX1003, ¶¶140-141; EX1005, ¶¶[0058], [0087]-[0088], FIG.5.

Hiraishi in view of Butt (Ground 1) also discloses "*the each respective buffer circuit* [300] *including a data path* [orange in FIG.5 below for read and write operations, respectively] *corresponding to each data signal line in the respective set of data/strobe signal lines* [L0, including lines DQ (data) and DQS (strobe) in FIG.7)]." EX1003, ¶¶142-143; EX1005, ¶[0084], FIG.5.

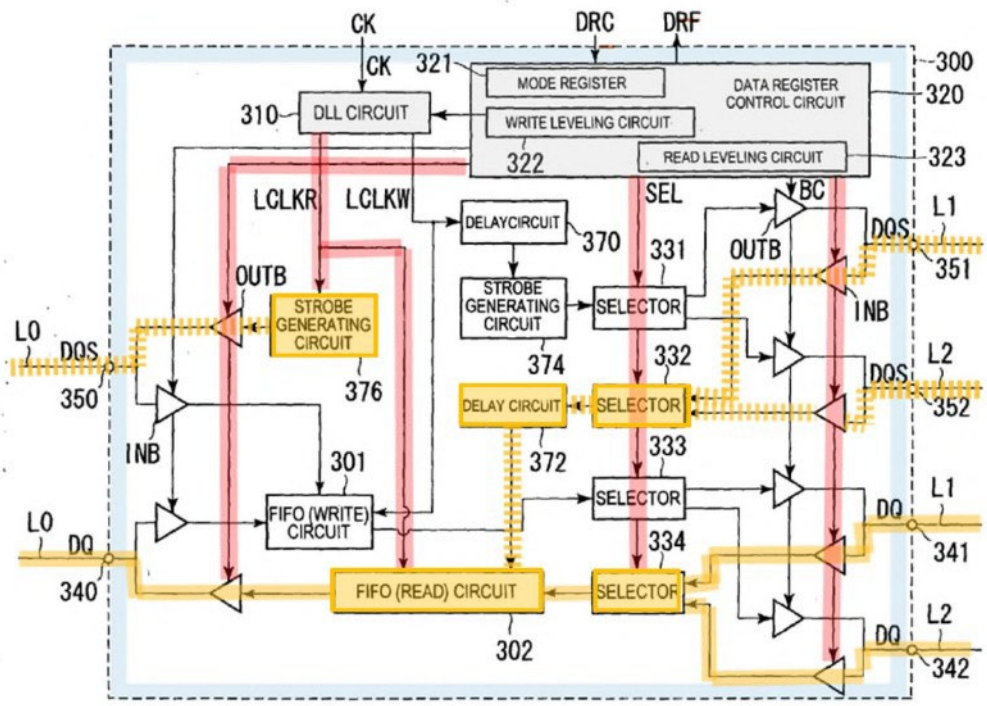

CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
OUTB
331
OUTB
STROBE GENERATING CIRCUIT
376
STROBE GENERATING CIRCUIT
374
SELECTOR
INB
L0
DQS
350
332
L2
DQS
352
DELAY CIRCUIT
372
SELECTOR
INB
301
333
SELECTOR
L1
DQ
341
L0
DQ
340
FIFO (WRITE) CIRCUIT
334
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
342
302

FIG.5

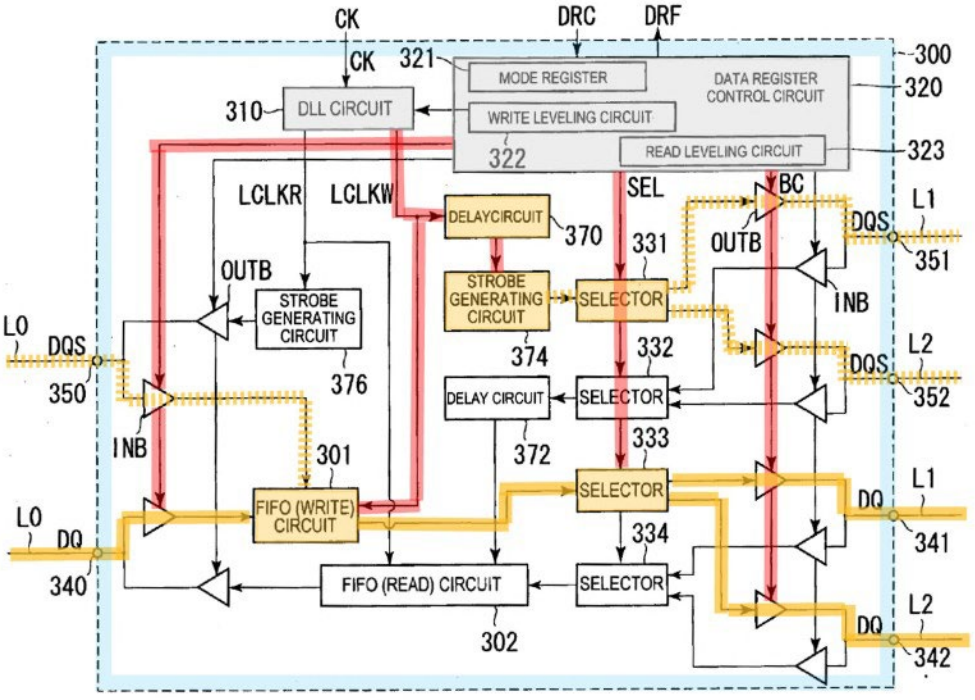

CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
OUTB
331
OUTB
STROBE GENERATING CIRCUIT
376
STROBE GENERATING CIRCUIT
374
SELECTOR
INB
L0
DQS
350
332
L2
DQS
352
DELAY CIRCUIT
372
SELECTOR
INB
301
333
SELECTOR
L1
DQ
341
L0
DQ
340
FIFO (WRITE) CIRCUIT
334
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
342
302

FIG.5

Hirashi explains that, during memory read or write operations, each respective buffer circuit buffers the data in respective FIFO Read or Write circuits between the data/strobe terminals 340/350 on the left of Figure 5 and the data/strobe terminals 341/342 and 351/352 on the right. EX1003, ¶143; EX1005, ¶[0084].

Similarly, Butt discloses that a circuit between a memory controller and DDR memory devices uses strobe signals to sample the data signals and buffer in FIFOs. EX1003, ¶144; EX1029, FIGS. 2, 3A (below).

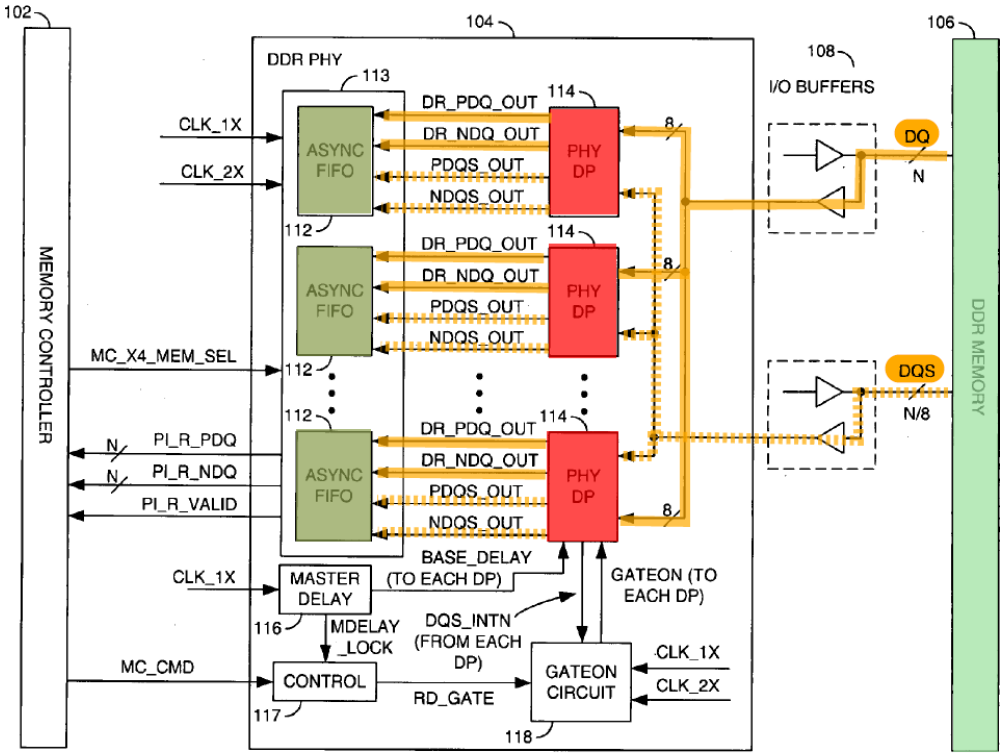


FIG. 2

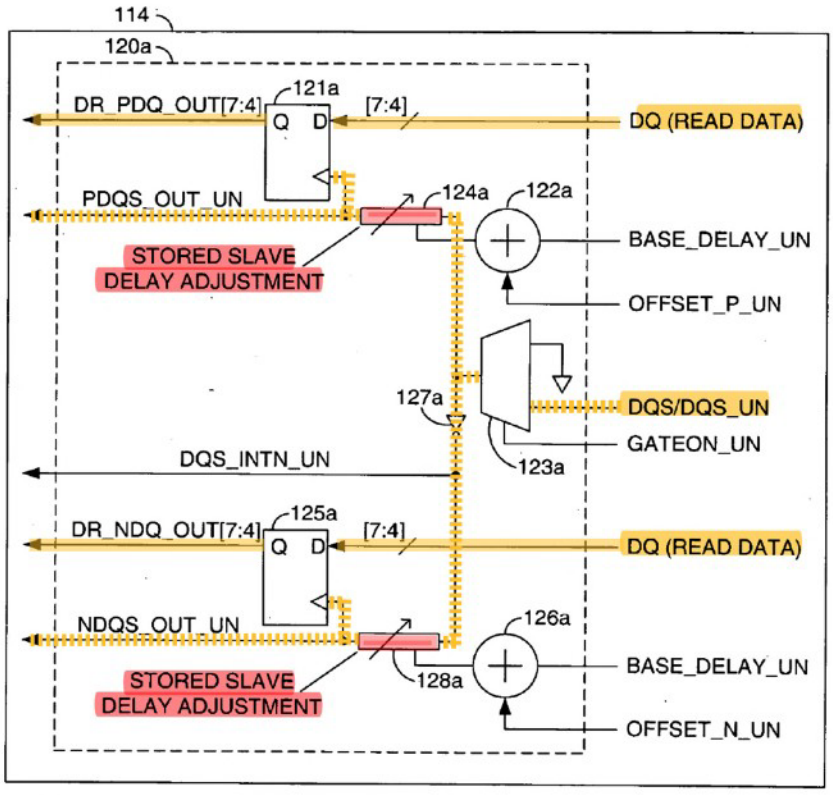


FIG. 3A

Butt explains that this circuit is an implementation of a "data path." EX1003, ¶144; EX1029, ¶[0017]. Therefore, a POSITA would have understood from the disclosure of Butt that Hiraishi's data register buffer 300 includes "data paths" (orange) where data strobe signals sample the data and the data samples are buffered in respective FIFO circuits. *Id.*

Hiraishi and Butt are analogous art to the '608 Patent, as each is directed to solving the problem of accurate timing of data transmissions for memory transactions. EX1003, ¶145; EX1001, Title; EX1005, ¶[0140]; EX1029, ¶[0005]. A POSITA would have understood and been motivated to implement the techniques

used in the data paths of Butt in Hiraishi's data register buffer. For example, both Hiraishi's data register buffer and Butt's interface circuit communicate data and strobe signals to and from the memory devices, sample the data signals using the strobe signal, and buffer the data in a FIFO. Thus, she would have been motivated to determine an optimum offset delay for the data sampling and buffering in the data paths and to control the data path accordingly as taught by Butt in order to optimize Hiraishi's data register buffer. EX1003, ¶146; EX1029, Abstract, ¶[0034]. Thus, Hiraishi in view of Butt discloses to a POSITA that each respective buffer circuit includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines. EX1003, ¶147.

Ground 1 further discloses that each respective buffer circuit includes "*a command processing circuit* [including Data Register Control Circuit 320 and logic in DLL Circuit 310] *configured to decode the module control signals* [including DRC] *and to control the data path in accordance with the module control signals* [e.g., DRC, received by Data Register Control Circuit 320] *and the module clock signal* [CK, received by DLL circuit 310]." EX1003, ¶148.

Hiraishi's data register buffer 300 is controlled by the command/address/control register buffer 400 using module control signals (e.g., DRC) and a module clock signal (CK). EX1003, ¶149; EX1005, ¶[0058]. The Data Register Control Circuit 320 receives and decodes the module control signal (DRC)

and controls the data path accordingly, e.g., by setting selectors 331-334, activating selected buffer circuits INB and OUTB, and selectively controlling FIFO Write and Read Circuits 301/302, delay circuits 370/372, and Strobe Generating Circuits 374/376. EX1003, ¶¶144-149; EX1005, ¶¶[0088]-[0091]. DLL circuit 310 generates local clock signals such as LCLKR and LCLKW from the module clock signal CK to control the data path accordingly, including timing of the FIFO Write and Read circuits, delay circuits 370/372, and strobe generating circuits 374/376. EX1003, ¶149; EX1005, ¶[0087]. For example, a POSITA would have understood that delay circuit 372 can be controlled to optimize capturing read data as taught by Butt. *Id*.

Thus, the data register buffer includes a command processing circuit (including Data Register Control Circuit 320 and DLL Circuit 310) that decodes the module control signals and controls the data path (e.g., for transmitting data and strobe signals associated with a read operation from a memory on data line L1) in accordance with the module control signals (DRC) and the module clock signal (CK). EX1003, ¶150. For example, when reading from memory on data line L1, the input buffers on terminals 351 and 341 are activated and selected by the selectors 332 and 334, and the output buffers to terminals 350 and 340 are also activated. The process is similar for a read operation from memory devices on data line L2 (using terminals 352/342, and avoiding bus conflicts). *Id.*; EX1022, 89-90. Ground 1 also

discloses to a POSITA controlling the data path for a write operation to memory devices on data line L1 or L2. EX1003, ¶151.

This Hiraishi-Butt combination is consistent with the Hiraishi-Butt combination which the Board found has a reasonable likelihood of invalidating the related 506 patent. EX1047, 10-26; EX1003, ¶¶67-69.

g) 1[f]: second wherein clause: tristate buffer and delay circuit configured to delay a signal

Ground 1 discloses that "the data path [orange] corresponding to the each data signal line includes at least one tristate buffer [e.g., output buffers OUTB and input buffers INB] controlled by the command processing circuit [including Data Register Control Circuit 320 and logic in DLL Circuit 310] and a delay circuit [including DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376] configured to delay a signal through the data path [e.g., during a read or write operation] by an amount determined by the command processing circuit [e.g., during the Read/Write Leveling step S4 between the memory devices and the data buffer] in response to at least one of the module control signals [e.g., DRC]." As discussed above (pp.33-37), a POSITA would have understood from the disclosure of Butt that Hiraishi's data register buffer includes data paths and would have been motivated to implement Butt's data path controlling techniques in Hiraishi's data register buffer. EX1003,

¶152; EX1005, FIG.5 (below, showing data paths, orange, for read and write operations).

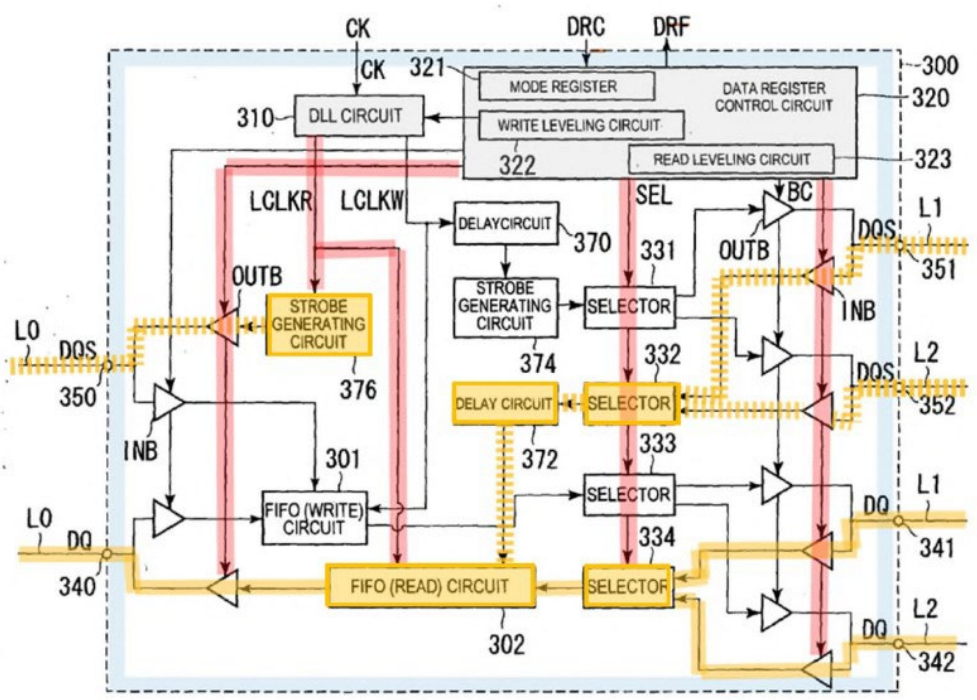


FIG.5

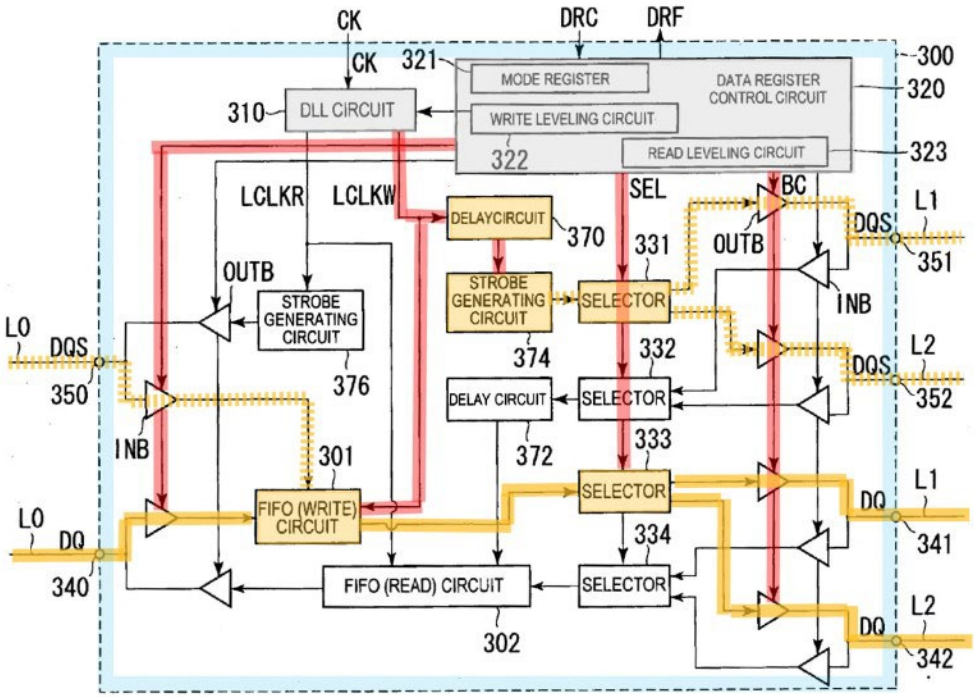

CK
DRC
DRF
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
300
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
331
OUTB
OUTB
STROBE GENERATING CIRCUIT
STROBE GENERATING CIRCUIT
SELECTOR
INB
L0
DQS
350
374
332
L2
DQS
352
376
DELAY CIRCUIT
SELECTOR
INB
372
333
301
SELECTOR
L1
DQ
341
L0
DQ
340
FIFO (WRITE) CIRCUIT
334
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
342
302

FIG.5

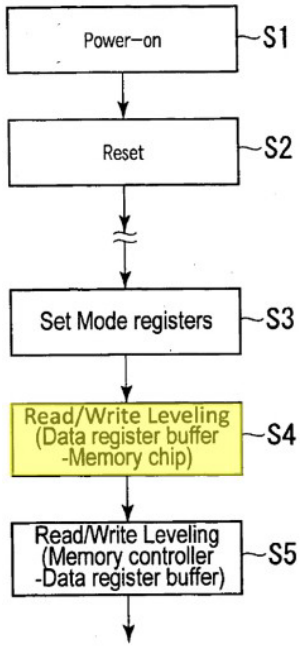

Power-on
S1
Reset
S2
Set Mode registers
S3
Read/Write Leveling (Data register buffer -Memory chip)
S4
Read/Write Leveling (Memory controller -Data register buffer)
S5

FIG.13

Hiraishi also discloses S4 Read/Write leveling to determine the delay through the data path. *Id*.; EX1005, FIG.13.

Regarding "the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit," Hiraishi discloses that the "data register control circuit 320" controls several tri-state buffers in the data path, including, e.g., buffers OUTB and INB shown in Figure 5, thus teaching that these buffers are "controlled by the command processing circuit" (i.e., including data register control circuit 320). EX1003, ¶153; EX1005, ¶[0088]. Hiraishi teaches that these OUTB and INB buffers are tri-state buffers. EX1003, ¶154; EX1022, p.68, FIG.2.23, p.74, FIG.2.28 (below, showing tri-state buffers).

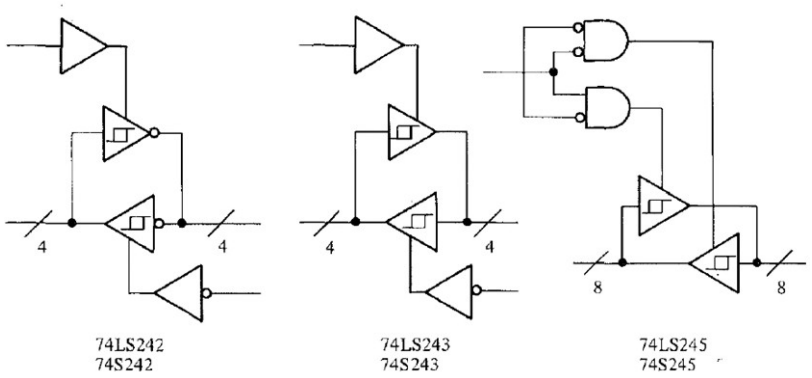


FIGURE 2.28 Drivers and receivers (continued on next page).

Using tristate buffers to drive bidirectional DQ and DQS lines was common practice at the time. EX1003, ¶154; EX1005, ¶¶[0088], [0151]; EX1022, pp.68, 117, 133, FIG.4.7 (below, showing tristate buffers for bidirectional data lines).

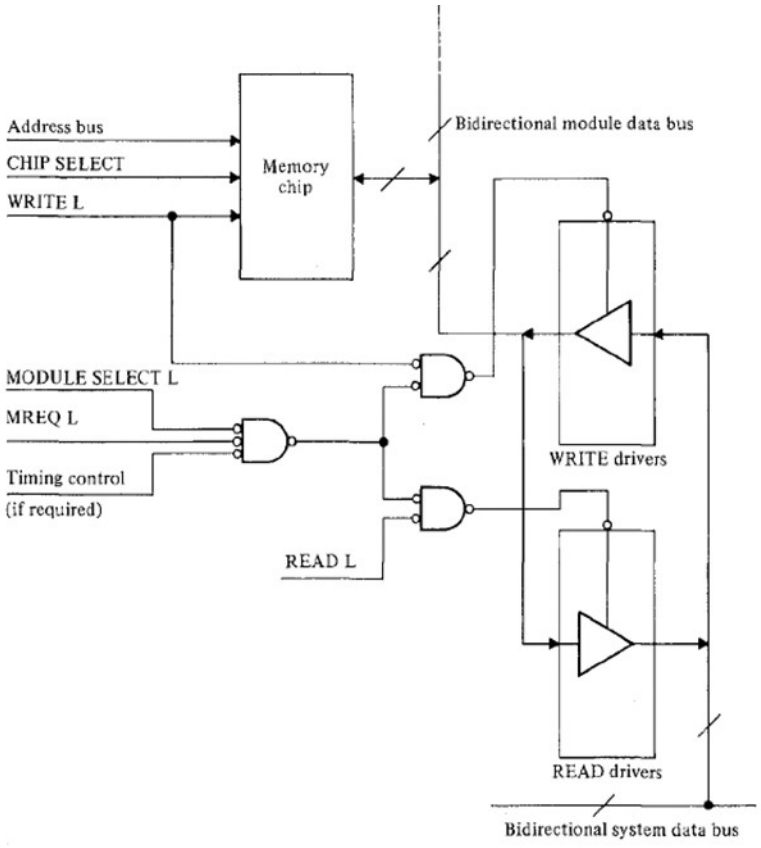


FIGURE 4.7 Tri-state driver control for interfacing memory chips to bidirectional data lines.

Regarding the "delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals," the claim language is ambiguous as to whether "in response to at least one of the module control signals" modifies the term "to delay" or "determined," but Ground 1 discloses both interpretations. EX1003, ¶155. Hiraishi's data register buffer 300 determines delays through the data path for read and write operations by respective read and write leveling operations during initialization in response to control signals from the command/address/control register 400, and applies those delays on the data/strobe signals for read and write

operations during normal operation in response to read and write commands received from the command/address/control register 400, as discussed below.

Hiraishi discloses that the timing is off between the DQ-pre/DQS-pre and DQ-post/DQS-post signals through the data register buffer, requiring separate timing adjustments between the memory chips and data register buffer (step S-4 in FIG.13) and between the data register buffer and memory controller (step S-5 in FIG.13). EX1003, ¶156; EX1005, ¶[0104]. Furthermore, Ground 1 discloses to a POSITA that the data buffers adjust the timing of both the data (DQ) and strobe (DQS) signals through the data path such that "the appropriate DQ-DQS relationship" is maintained. *Id.*, EX1029, ¶[0003].

Hiraishi's S-4 step includes both read and write leveling between the data register buffer and the memory chips, such that a "delay circuit [is] configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals," as explained below. EX1003, ¶¶157-158; EX1005, ¶¶[0090], [0140].

Hiraishi's S-4 write leveling operation is performed during initialization responsive to module control signals (e.g., DRC conveying "mode switching" or "mode register set" commands) by a write leveling circuit 322 "to adjust a write timing…in consideration of a propagation time of a signal." EX1003, ¶159; EX1005, ¶¶[0088], [0090], [0100], [0140], [0142], FIG.5. In response to a write leveling mode

register set command, the memory devices provide feedback of a local clock sampled by the strobe signal, and the write leveling circuit 322 is activated by corresponding DRC signals to process that feedback. *Id*., EX1020 (JESD79-3C), 42-43. Figures 14A and 14B of Hiraishi explain the S-4 write leveling operation. EX1003, ¶160; EX1005, ¶¶[0142-46], FIGS. 14A-14B (below).

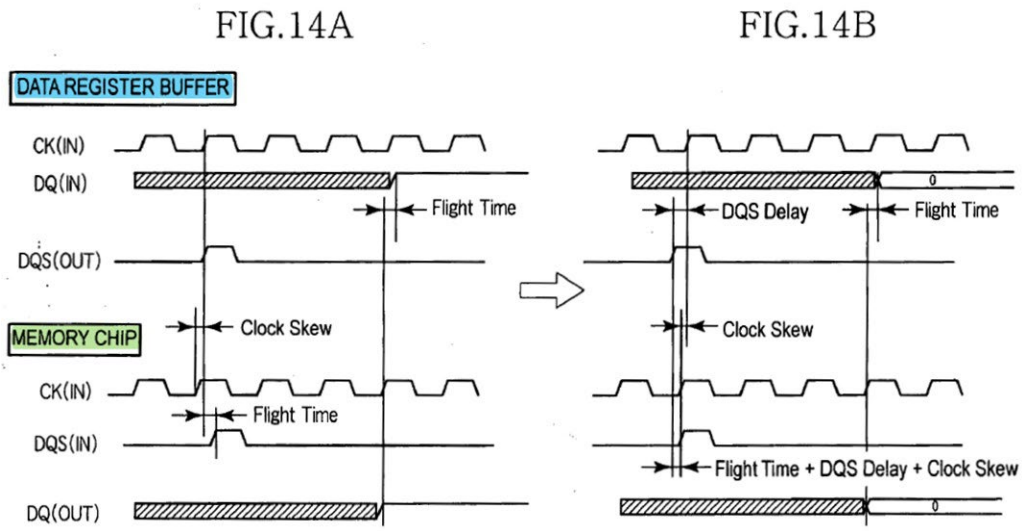


Figure 14A shows that, before write leveling, the strobe signal DQS is off from the memory's local clock. "The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW" such that "the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other" as shown in Figure 14B. EX1005, ¶¶[0145-46]. The delays determined during write leveling are stored in the data register buffer 300 and applied by the control circuit 320 to delay both the data and data strobe signals during subsequent write

operations to ensure that the standard data to strobe timing requirements are met at the memory devices. *Id*., FIG.12 (below, showing "Re-timing" (blue box) of both data and strobe to arrive at the memory with WL=5); EX1003, ¶160; EX1020, 68.

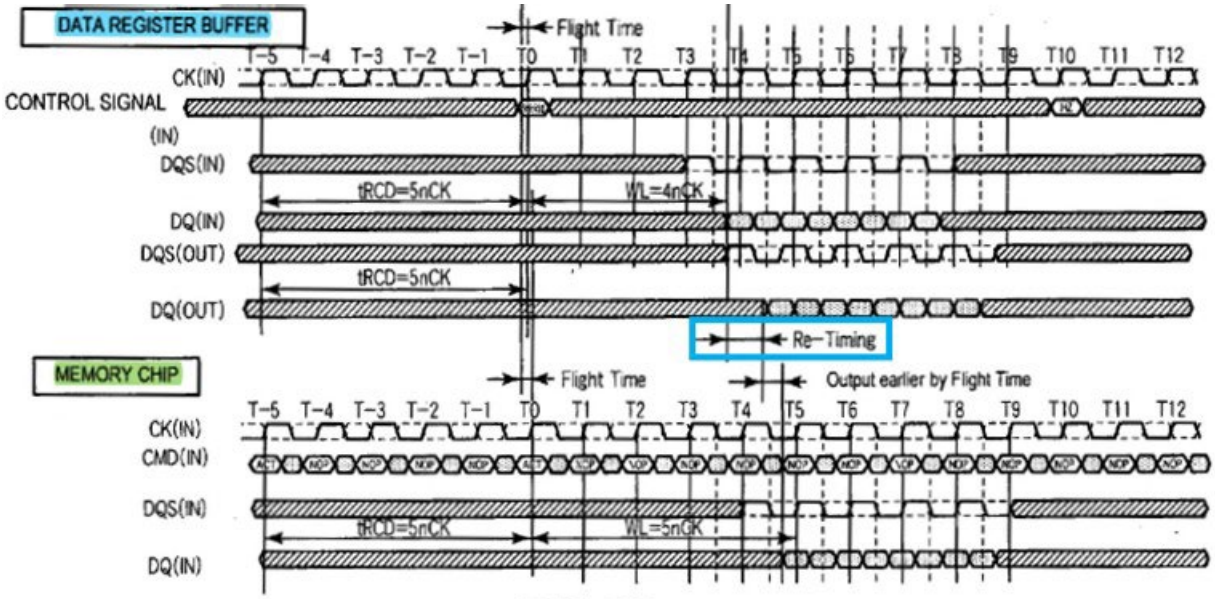


FIG.12

Hiraishi's data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 and performs a re-timing in synchronization with the phase-adjusted internal clock LCLKW which is used to read the FIFO circuit 301 to output the write data DQ and to generate the corresponding strobe DQS with Delay and Strobe Generating Circuits 370 and 374. EX1003, ¶161; EX1005, ¶¶[0135], [0087], [0084], [0091], FIG.5 (below, showing write data paths, orange).

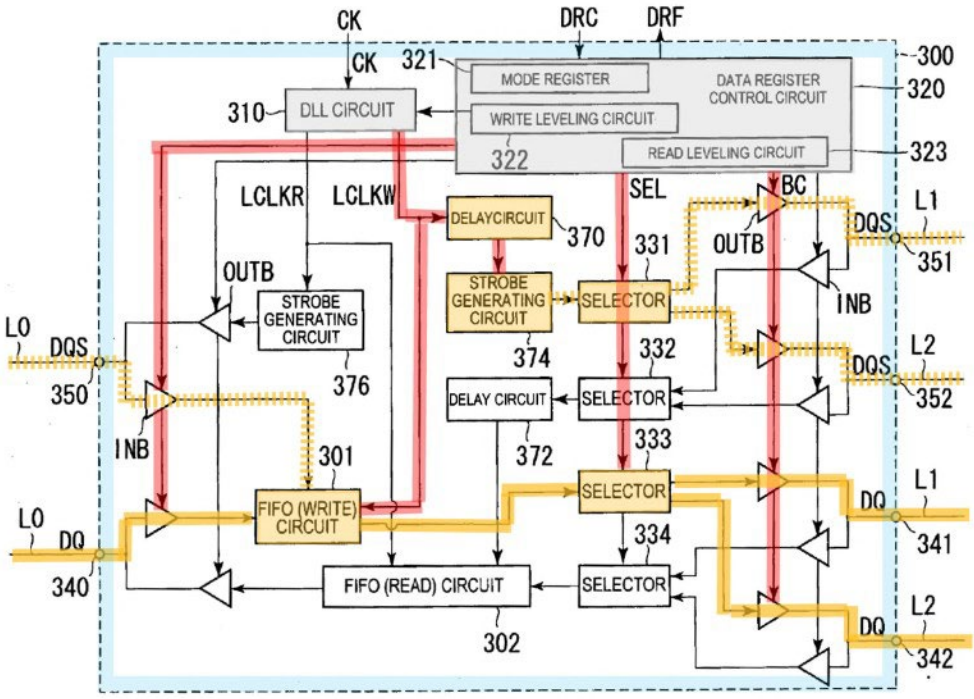


FIG.5

Therefore, Ground 1's delay circuit for write operations includes the Write FIFO 301 delaying the write data signal, delay circuit 370 delaying the LCLKW signal, the strobe generating circuit 374 generating a delayed strobe signal that is in synch with the delayed write data, and DLL circuit 310 generating the LCLKW signal for timing the output of the delayed data and strobe signals. EX1003, ¶161. The result of Ground 1's delay circuit is a variable delay for the DQ/DQS signals ("*a delay circuit configured to delay a signal through the data path*"), whose amount is determined by Data Register Control Circuit 320 and logic in DLL Circuit 310 based on the result of the write leveling operation ("*by an amount determined by the command processing circuit*.").

Similarly, Hiraishi discloses that S-4 read leveling is "to adjust…a read timing in consideration of a propagation time of a signal." EX1005, ¶[0140]. For example, Hiraishi discloses that read data arrives at the data buffer from different memories at different times A. EX1005, FIG.15, ¶¶[150-151].

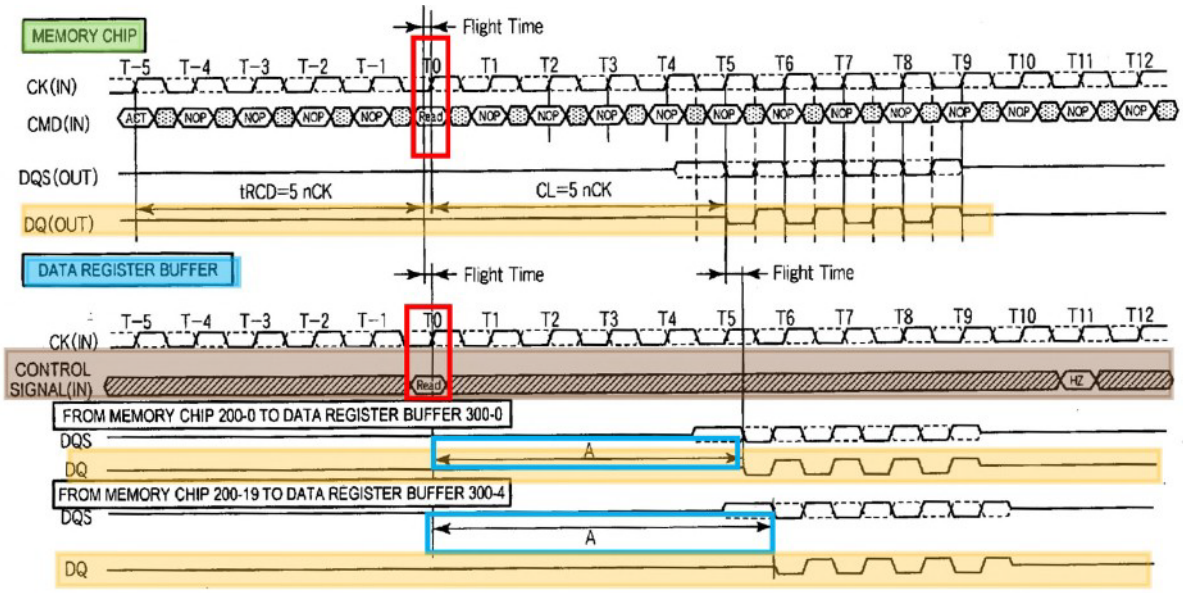


FIG.15

Read leveling determines delays ("Re-Timing") for the read data (DQ) and strobe (DQS) signals received at different times A such that the delayed data and strobe signals are output CL=6 clock cycles after the read command is received by the data buffer. EX1003, ¶¶162-163; EX1005, ¶¶[0163], [0147]-[0151], FIG.11.

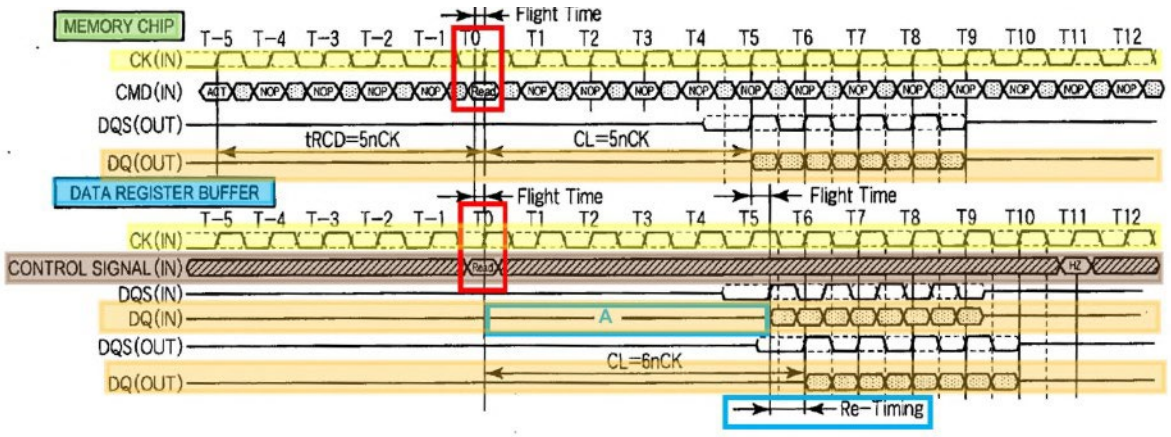


FIG.11

Therefore, the DQ/DQS read delays are determined as the difference between the time of data output at CL=6 and time A of data arrival. *Id.* These delays are based on the timing of the control and clock signals (DRC, CK) carrying the read command (T0), the measured read data arrival time A from the memory, and a latency parameter (CL=6). EX1003, ¶163. Ground 1's delay circuitry delays the data and strobe signals (DQ/DQS) through the read data paths for subsequent read operations by an amount determined by the read leveling operation. *Id.* This read leveling operation is performed by the read leveling circuit 323 (in FIG.5), which a POSITA would have understood to be activated by a module control signal DRC. *Id.*; EX1005, ¶¶[0147]-[0151]. Such a read leveling operation was well known and supported by standards at the time. EX1003, ¶164; EX1005, ¶¶[0150], [0160], [0163], FIGS. 5, 13; EX1020, pp.31, 48, 51.

Ground 1 further teaches that the measured "time A" is also used by the data register control circuit 320 to activate the input buffers INB and other parts of the

read data path to clock the data properly into the FIFO (read) circuit 302. EX1003, ¶165; EX1005, ¶¶[0084-85], [0151], FIG.5 (below, showing read data paths, orange).

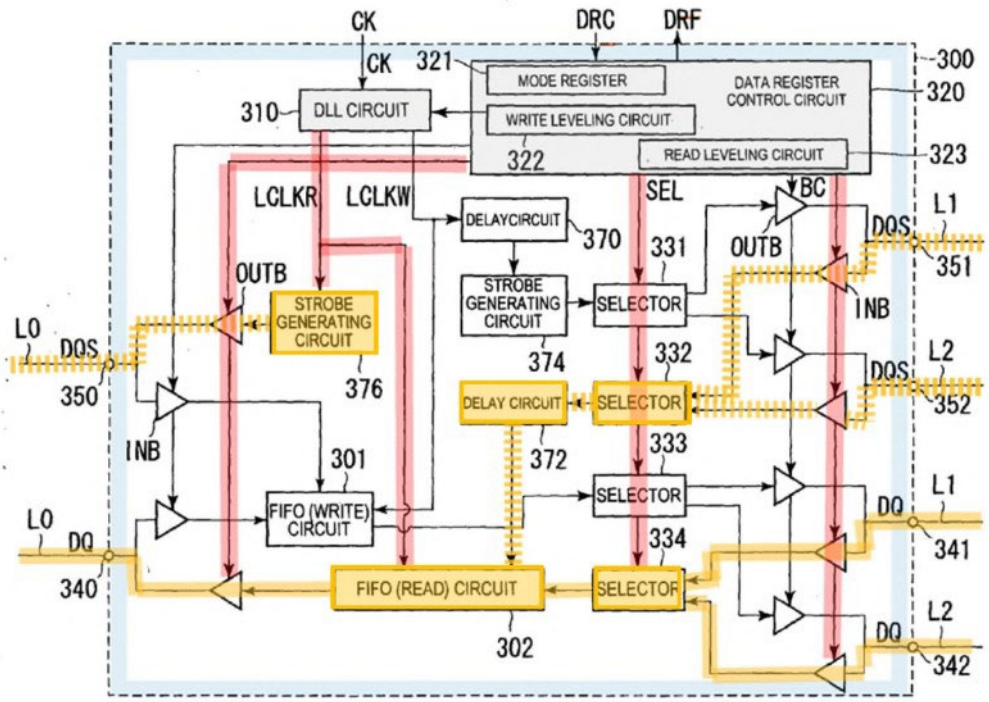


FIG.5

Ground 1 also discloses that "[a]n output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310." EX1005, ¶[0087]; *see also* ¶[0084] (strobe generating circuit 376 generates DQS in synchronization with LCLKR).

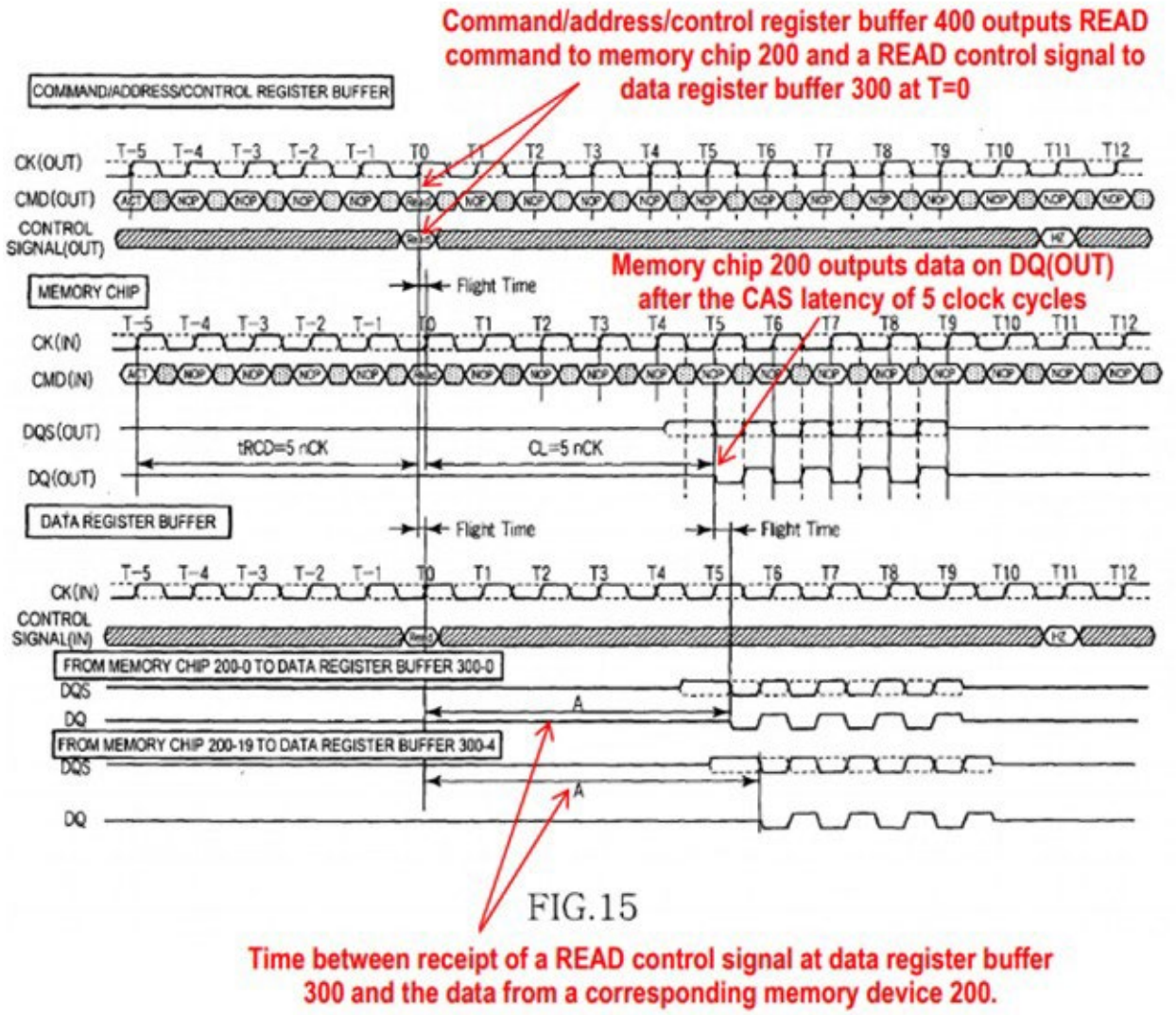
The result of these operations is a variable delay adjusting the timing of the read data and strobe signals on the data path. As shown above, the read data and strobe signals received at "time A" from the memory devices are delayed by a

variable amount such that they are output on the data bus in synchronization with the local clock of the data register buffer. EX1003, ¶165.

Therefore, Ground 1 discloses the claimed "*delay circuit*" for read operations, including the FIFO (read) circuit 302 delaying the read data signal, delay circuit 372 delaying the input strobe signal, the strobe generating circuit 376 generating a delayed strobe signal that is in synch with the delayed read data, and DLL circuit 310 generating the LCLKR signal for timing the output of the delayed read data and strobe signals. EX1003, ¶166. In response to module control signals indicating a read operation, the input of the Read FIFO 302 and selected input buffers INB are activated in accordance with time A, and the data is read into the Read FIFO 302 according to a strobe signal delayed by delay circuit 372. EX1005, ¶[0091]; EX1003, ¶166. The strobe output from strobe generating circuit 376 and data from the Read FIFO 302 are timed by LCLKR generated by the DLL circuit 310. The result is a delay of the DQ/DQS signals ("*a delay circuit configured to delay a signal through the data path*") by an amount determined by Data Register Control Circuit 320 and logic in DLL Circuit 310 based on the result of the read leveling operation ("*by an amount determined by the command processing circuit*"). EX1005, ¶¶[0084], [0087], [0130], FIG.11; EX1003, ¶¶166-167.

In a prior proceeding involving a related patent, Netlist made several admissions confirming the points above. EX1003, ¶¶168-171; EX1013, pp.38-40,

42. For example, below is Netlist's annotation of Saito's Figure 15 (identical to Hiraishi's):



EX1013, p.39; EX1003, ¶¶168-169. As shown above, Netlist conceded that Hiraishi, in connection with S4 read leveling, discloses a "*delay circuit configured to delay a signal through the data path by an amount* [e.g., the difference between CL=6 when the data is output and time A when it arrived by activating the INB/OUTB buffers

and adjusting their timing (e.g., using DLL circuit 310, strobe generating circuit 376, and FIFO (Read) circuit 302) to align with the local clock signal when they are output] *determined by the command processing circuit in response to at least one of the module control signals* [e.g., READ control signal]." EX1003, ¶¶169-170; EX1013, pp.39-40, 42.

2. Claim 2

a) 2[a]: first and second memory operations

As discussed for 1[f] above, Hiraishi's S-4 read/write leveling operation comprises a "*first memory operation*" (as interpreted by Netlist for infringement purposes), and a subsequent normal read/write operation is a "*second memory operation subsequent to the first memory operation*." EX1003, ¶172. The memory devices perform the read/write leveling operations and read/write operations in response to commands, including mode register set commands and read/write commands. EX1003, ¶¶172-173; EX1020, 29, 31, 33, 43, 48-54.

b) 2[b]: first and second set of command[2] signals

Hiraishi teaches that a set of command signals is necessary for both the S-4 read or write leveling operation ("*first memory operation*" under Netlist's

[2] The term "*the command signal*" lacks proper antecedent basis because claim 1 recites both "*system command signals*" and "*module command signals*."

interpretation) and for a subsequent read or write operation ("*second memory operation*"). EX1003, ¶174; EX1020, pp.31, 33, 48-54.

For example, Hiraishi discloses that read and write command signals ("*second set of command signals*") from the system memory controller are received by command/address/control register 400. EX1003, ¶175; EX1005, FIGS. 11-12, ¶¶[0124-25], [0133-34]. A POSITA would have understood that a "*first set of command signals*" from the memory controller is also necessary for the S4 read/write leveling operation. EX1005, ¶¶[0139-40]; EX1003, ¶¶176, 159-160; EX1020, 31, 33, 48-54, 43.

c) 2[c]: first and second set of control signals

As explained above for 1[b], Hiraishi discloses that the control signal generating circuit 430 (part of the command/address/control register buffer 400) generates control signals in response to command signals. EX1003, ¶178; EX1005, ¶¶[0060], [0099].

Hiraishi discloses that for a S-4 read leveling operation, the command/address/control register buffer 400 ("*module control device*") generates "*a first set of module control signals*" [e.g., DRC] in response "*the first set of command signals*" (e.g., command initiating the read leveling operation) and supplies the module control signals to the data register buffers 300. EX1003, ¶¶179, 181; EX1005, ¶[0148]. Similarly for write leveling operations, a POSITA would

have understood that, during initialization, the command/address/control register buffer 400 outputs corresponding mode switching and mode register setting commands to the data register buffers 300. EX1003, ¶¶179, 159-160.

Likewise, for a subsequent read operation ["*second set of command signals*"], Hiraishi discloses that command/address/control register buffer 400 registers the received command "ACT and Read," and in response "supplies a read command Read to the data register buffer 300 as part of the control signal DRC ["*second set of module control signals*"]." EX1003, ¶¶180-181; EX1005, ¶[0126]. For a write operation, "a flow of the command is similar to that in the read operation." *Id*.; EX1005, ¶[0134].

d) 2[d]: signal associated with the second memory operation

The terms "*the at least one of the module control signals*" and "*the signal through the data path*" find antecedent basis in 1[f], which recites "a delay circuit configured to delay ***a signal through the data path*** by an amount determined by the command processing circuit in response to ***at least one of the module control signals***." EX1003, ¶182.

As explained above for 2[c], where the "*first memory operation*" includes a read/write leveling operation, "*the at least one of the module control signals*" includes at least control signal DRC. EX1003, ¶183. Hiraishi discloses that the delay

amount is determined by the command processing circuit, as explained above in 1[f], in response to this control signal. EX1003, ¶183; EX1005, ¶[0148].

Hiraishi discloses that subsequent to read/write leveling, the signals through the data path for read operations are delayed by an amount determined by read/write leveling, as explained above in 1[f]. EX1003, ¶184. Thus, where the "*second memory operation*" is a read/write operation, Hiraishi discloses that "*the signal through the data path is a signal associated with the second memory operation*," and this signal is delayed by an amount determined by the command processing circuit in response to at least one of the module control signals during the read/write leveling procedure which is "*at least one of the module control signals…of the first set of module control signals*." EX1003, ¶184.

3. Claim 3

a) 3[a]: different ranks

Hiraishi expressly discloses a "four-Rank configuration" with four memory devices in a group ("*the respective set of memory devices*"), each memory device in the group in a different rank. EX1003, ¶185; EX1005, ¶¶[0051]-[0052].

b) 3[b]: module command signals

As explained above for 1[b], Hiraishi discloses that the command/address/control register buffer 400 generates module command signals output to memory devices 200 in response to the first and second set of command signals (e.g., corresponding to initiating a read/write leveling operation and a

subsequent read/write operation). EX1003, ¶¶186-190; EX1005, ¶¶[0060], [0097], [0126], [0134], [0148].

c) 3[c]: chip select

Hiraishi also discloses that the second set of module command signals (corresponding to a subsequent read/write operation) include chip select signals that select at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation. EX1003, ¶191. For example, Hiraishi discloses that each rank is selected by a respective chip select signal. *Id.*; EX1005, ¶[0051]; EX1021, pp.319, 413; EX1018, pp.6, 10-16. A POSITA would have understood that, because the "*respective set of memory devices*" includes one memory device from each rank, the chip select signals also select one memory device in that "*respective set*." EX1003, ¶191. Hiraishi also discloses that the chip select signals are part of the command signals, consistent with a POSITA's understanding. *Id.*; EX1005, ¶[0076]; EX1020, pp.33, 13, 34 & n.1. Hiraishi further discloses that the selected memory device performs the "*second memory operation*" as it inputs or outputs respective data (DQ) and strobe (DQS) signals on terminals 204 and 205. EX1003, ¶191; EX1005, ¶¶[0078]-[0081], FIG.4.

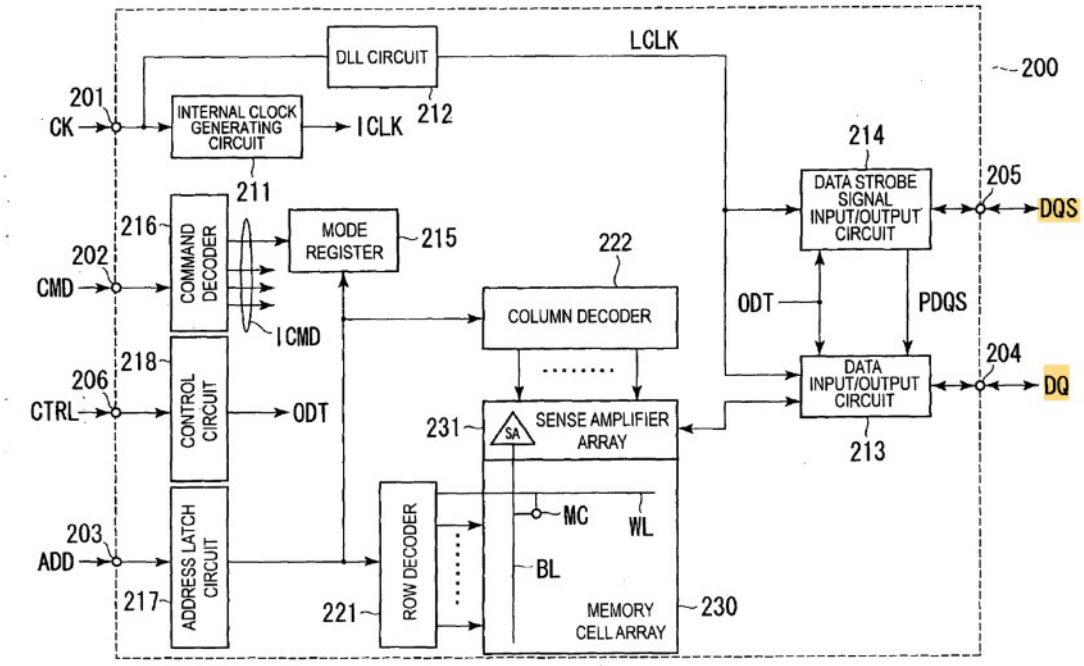
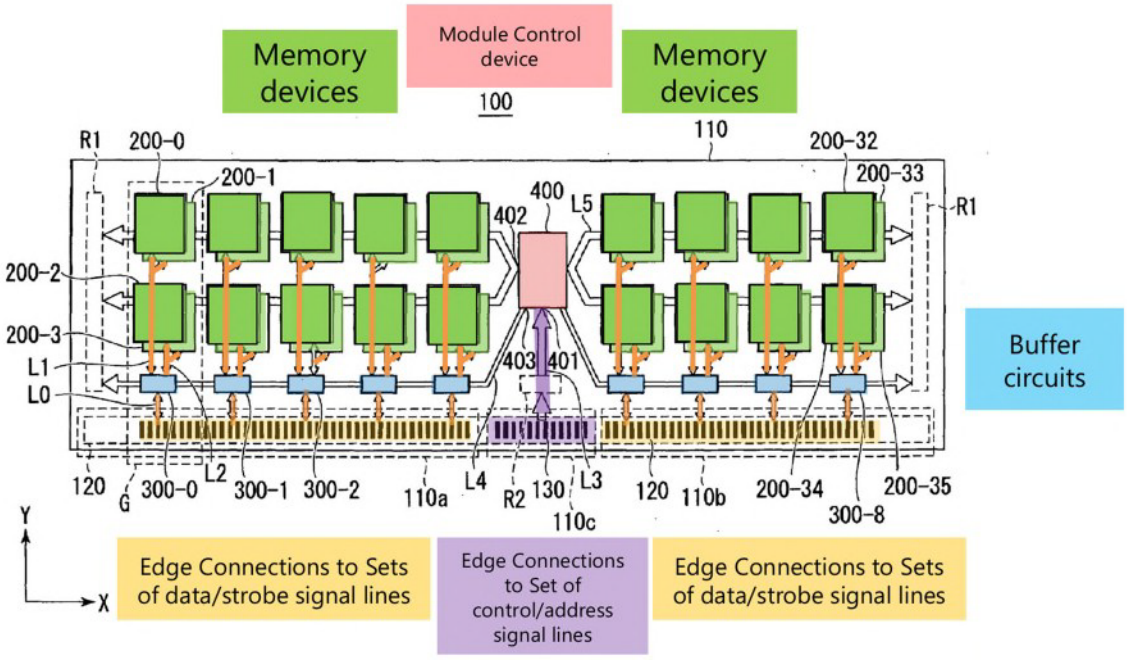


FIG.4

4. Claim 4: x8 buffers and memory devices

Hiraishi discloses "wherein each of the plurality of buffer circuits [blue] has a data width of 1 byte, and wherein each of the memory devices [green] has a data width of 1 byte." EX1003, ¶¶192-193; EX1005, ¶¶[0053] ("**An arrow of each of the data lines L1 and L2** [(orange)] **shown in FIG. 1 indicates a line of 1 byte** (8 bits)."), [0085] ("**a single data register buffer** 300 **inputs and outputs 1-byte data.**"), FIG.1 (below).



5. Claim 5: x8 buffer; x4 memory devices

As explained above for claim 4, Hiraishi discloses that "*each of the plurality of buffer circuits has a data width of 1 byte*." Although Hiraishi also discloses that each of the memory devices has a data width of 1 byte, a POSITA would have understood that this is just one implementation, and that a single 8-bit memory device could be replaced with a pair of 4-bit wide memory devices, as was a standard option at the time. EX1003, ¶¶194-195; EX1005, ¶[0073]; EX1020, 3-12 (describing standard DDR3 memory devices with x4, x8, and x16 data widths); EX1018, 4.20.4-25 to -27 (showing either x8, or pairs of x4, memory devices can be used on a DIMM); EX1021, 370-71, tbl.8.1.

6. Claim 6: metastability detection circuit

As shown below, Hiraishi discloses that "*each respective buffer further includes a receiver circuit* [in DLL circuit 310 and Data Register Control circuit 320] *for each of the module control signals* [*e.g.*, DRC]," and at least renders obvious that "*the receiver circuit includes a metastability detection circuit configured to determine a metastability condition* [such as a metastability condition in capturing signal values] *in the each of the module control signals* [*e.g.*, DRC] *with respect to the module clock signal* [CK]."

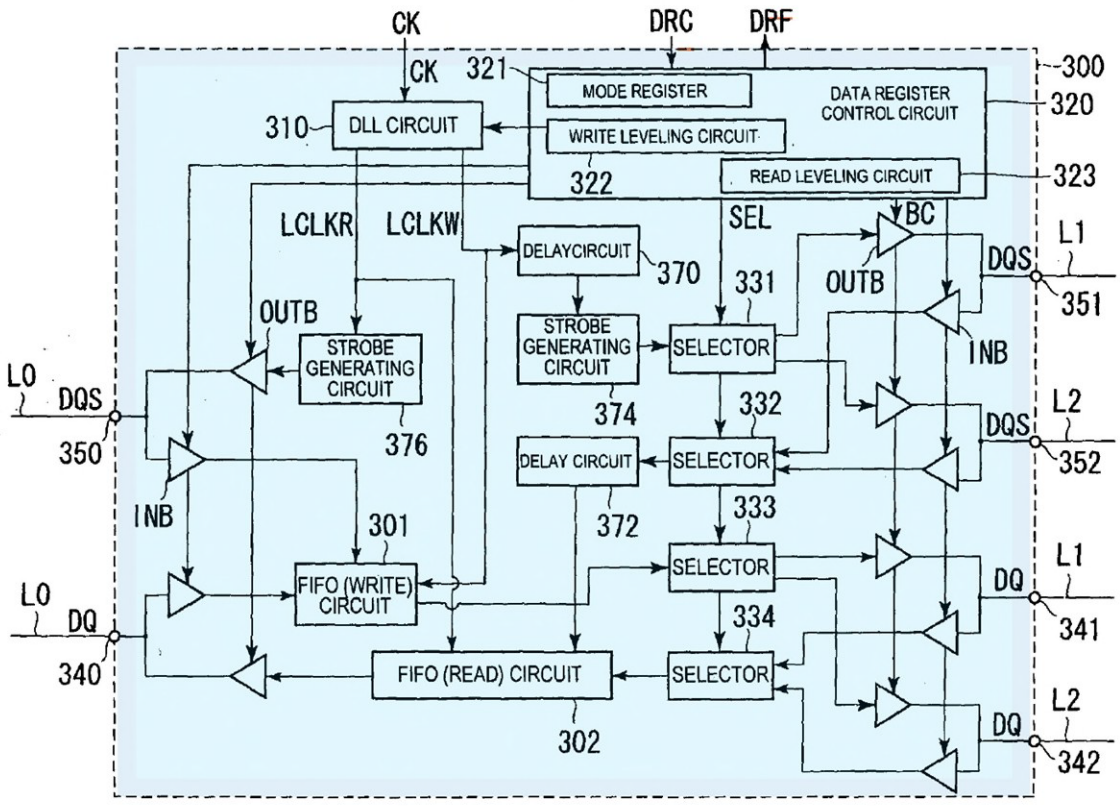


FIG.5

EX1003, ¶¶199-201; EX1005, FIG.5.

For example, Hiraishi discloses that the control signal DRC and corresponding clock CK are transmitted on control line L4 to multiple Data Register Buffers. EX1003, ¶202; EX1005, FIG.7:

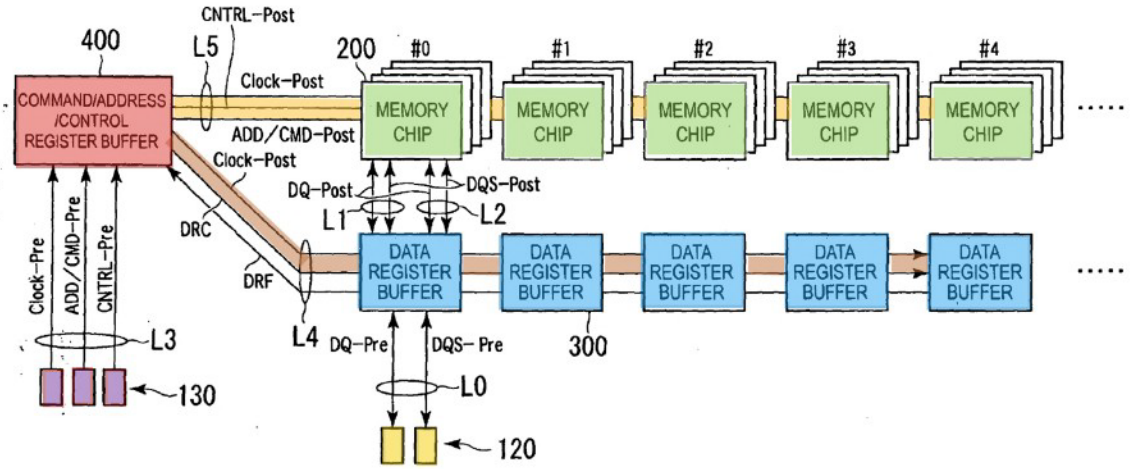


FIG.7

Hiraishi also discloses that the DLL circuit 310 in the data buffer receives the module clock signal CK and generates from this CK a number of internal clocks, including LCLKR and LCLKW, with fine phase adjustments used for the data buffer's internal operation (*see, e.g.*, EX1005, FIG.5) and that the DRC signal is captured by the Data Register Control unit 320. EX1003, ¶202. A POSITA would have understood from this disclosure that DLL circuit 310 generates, based on the received clock signal CK, the internal clock used to capture the DRC signal, EX1003, ¶203, and that the internal clock is generated with a specific phase selected to avoid metastability

because the control information conveyed by the DRC signal may not be correctly captured if there is a metastability condition at the input of the DRC signal. *Id.* (citing EX1008, 1:21- 31). Due to the high speed at which the memory devices operated at the time, Hiraishi teaches that the "use of the DLL circuit is substantially essential." EX1005, ¶[0163]; EX1003, ¶203.

Given the possibility of erroneous DRC signal reading, it also would have been obvious to a POSITA to have the Data Register Control Circuit 320 include a known metastability condition detector and implement the DLL circuit 310 to avoid metastability by adjusting the phase of the internal clock signal used to capture the DRC signal (like how Hiraishi's DLL circuit adjusts the LCLKW signal's phase). EX1003, ¶204. A POSITA would have understood that such a metastability condition detector can be used, e.g., during initialization to indicate the presence of a metastability condition to allow adjustment of the internal clock's phase to avoid the metastability condition. *Id.*

7. Claims 7-8

The limitations of claims 7-8 are substantially identical to earlier limitations, as shown in the following table:

Claim…	…is substantially similar to claim…	…and obvious for at least the same reasons above and in EX1003:

7	4	¶¶208-209 (¶¶192-193)
8	5	¶¶210-211 (¶¶194-198)

8. Claim 9:

a) 9[a]: clock regeneration circuit

Hiraishi discloses that "the each respective buffer circuit further includes a clock regeneration circuit [including DLL circuit 310] configured to generate a local clock signal [for internal operations] having a programmable phase relationship with the module clock signal [CK]," e.g., the local clocks LCLKW and LCLKR have a programmable phase relationship with the module clock signal CK. EX1003, ¶213; EX1005, FIG.5 (below).

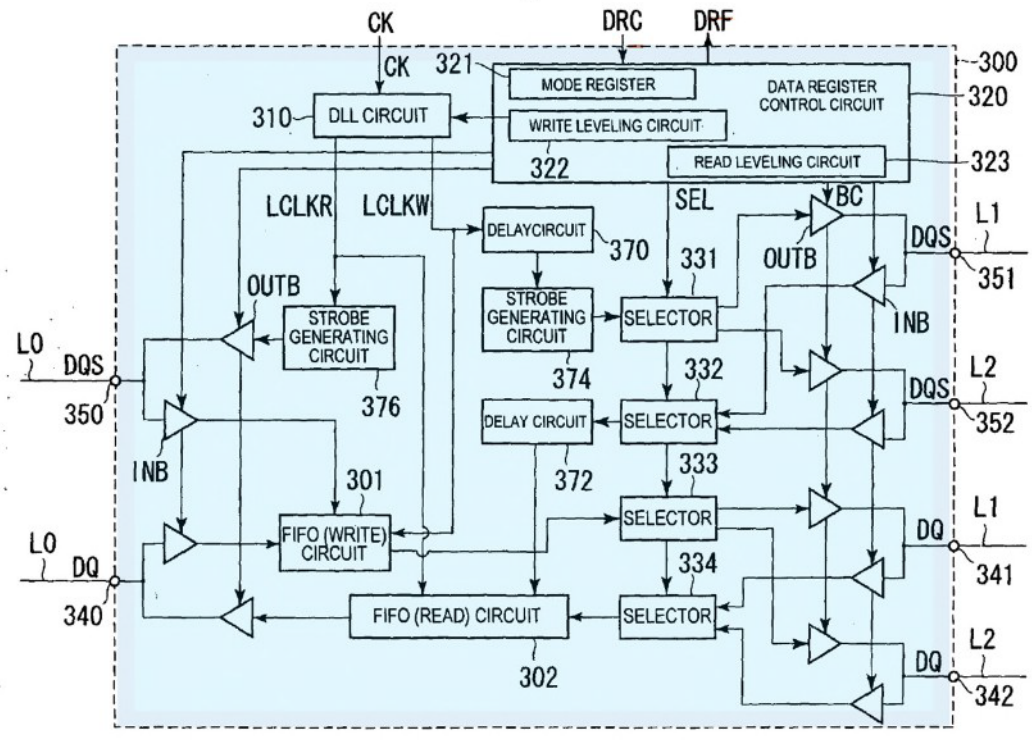


FIG.5

For example, Hiraishi teaches that the DLL circuit 310 generates local clock signals LCLKR and LCLKW based on the module clock signal CK, EX1003, ¶214; EX1005, ¶[0087], and further teaches that DLL circuit 310 is a clock regeneration circuit configured to generate local clock signals (for the data register buffer's 300 internal operation) which have a programmable phase relationship relative to the module clock signal CK. EX1003, ¶214; EX1005, ¶¶[0074], [0145], [0163].

b) 9[b]: output local clock to memory devices

Although Hiraishi discloses embodiments where the buffer circuits 300 and memory devices 200 have independent DLL circuits (resulting in no need for the buffer circuits' local clock to be output to the memory devices), Hiraishi also discloses that when the memory devices do not include a DLL circuit, the DLL circuit in the buffer circuit 300 is used to adjust the input/output timing in the memory devices as well, and a local clock signal of the buffer circuits would be output to the respective set of memory devices to synchronize operations of those memory devices with the buffer circuit. EX1003, ¶216; EX1005, ¶[0200].

A POSITA would have known that sharing circuitry between buffer circuits and memory devices, including circuits that generate a local clock, was a well-known design choice, and that one common technique was to output the buffer circuit's local clock to the memory devices. EX1003, ¶217. For example, the disclosure of US 8,566,516 ("Schakel," filed October 30, 2007) (EX1009) is

consistent with Hiraishi and the knowledge of a POSITA at the time, and confirms it would have been obvious to output the buffer circuit's local clock signal to the memory devices. EX1003, ¶¶217-218; EX1009, 4:5-14, 4:31-41, FIG.1B.

Specifically, Schakel discloses several configurations of memory modules, one of which involves a plurality of memory devices (DRAM modules) electrically interconnected together, and a single buffer circuit ("intelligent buffer 133"), which includes the functionality of an interface circuit ("interface circuit 102").

EX1009, 4:5-14; FIG.1B:

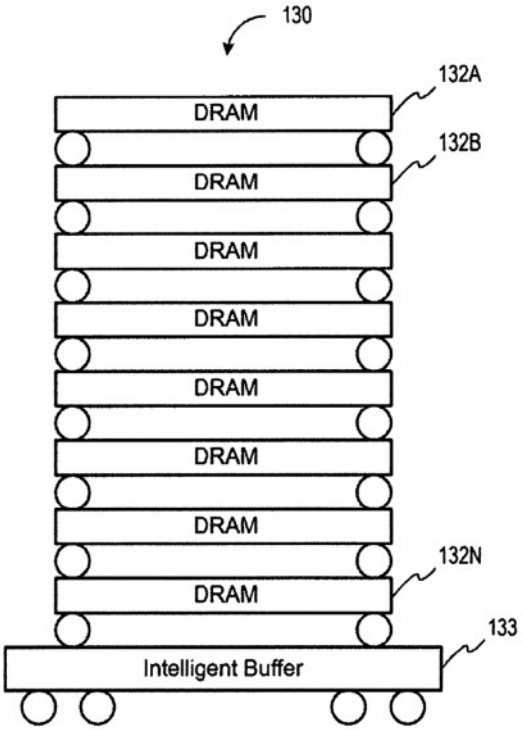


FIG. 1B

Schakel discloses that as an alternative to each DRAM module having its own clock generating circuitry, they could be associated with a single buffer circuit outputting

a clock signal to the memory devices, consistent with Hiraishi's disclosure above. EX1003, ¶¶217-218; EX1009, 4:31-41.

9. Claim 10: claim 9 + sampler

As shown below, Ground 1 discloses that the data paths for read operations ("*second memory operation*")[3] include a "*first data path*" for transmitting a "*strobe signal*," such as the data path coupled to the line L1 at the input/output terminal 351 for transmitting data strobe signals (DQS, dashed orange line), and a "*second data path*" for transmitting a "*data signal*," such as the data path coupled to the data line L1 at the input/output terminal 341 for transmitting a data signal (DQ, solid orange line):

[3] The term "*the second memory operation*" lacks antecedent basis

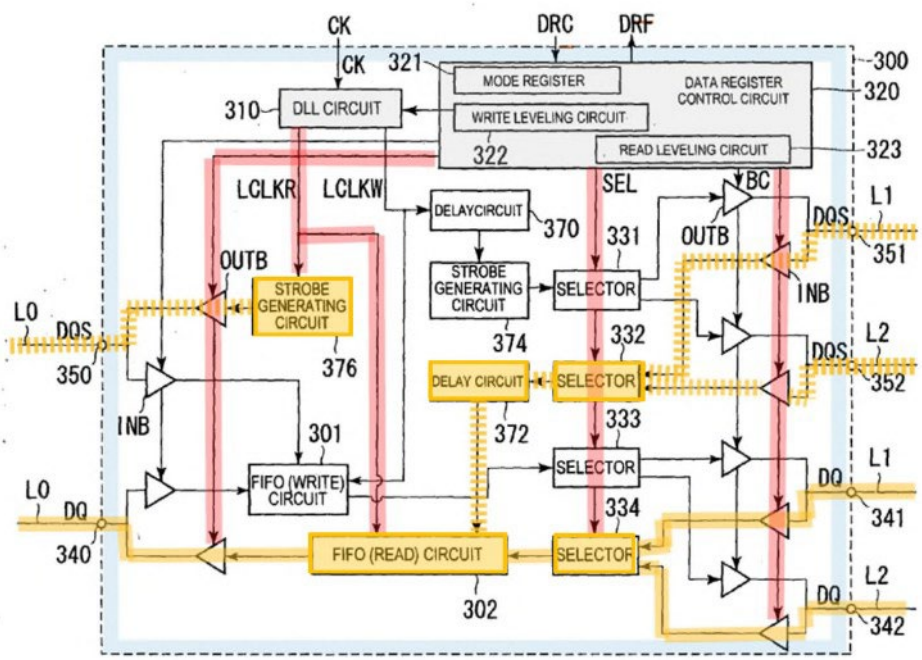


FIG.5

EX1003, ¶¶222, 144-147; EX1005, FIG.5. As shown above, the data paths for read operations include another data path for transmitting a strobe signal, e.g., the data path coupled to the line L2 at the input/output terminal 352 for transmitting data strobe signals (DQS, dashed orange line), as well as for transmitting a data signal, e.g., the data path coupled to the line L2 at the input/output terminal 342 for transmitting data signals (DQ, solid orange line). *Id.* Either L1 or L2 could be considered a "*first data path*," but only one would be used at a given time, to avoid conflicts. *Id.* In other words, like Figures 15-16 of the '608 Patent (below), Hiraishi's data paths have a "fork in the road" arrangement for routing data and strobe signals from either one (L1) or the other (L2) branch to the same output (terminal 350,

coupled to line L0 for strobe signals; terminal 340, coupled to line L0 for data signals) during read operations. *Id.*; *compare* EX1005, FIG.5, *with* EX1001, FIGS. 15-16 (below, with solid orange lines added to indicate paths for data signals during read operations, and dashed orange lines added to indicate the sampled strobe signal—the gap in the dashed orange lines includes circuitry that provides the required delays of strobe signals through the data buffer).

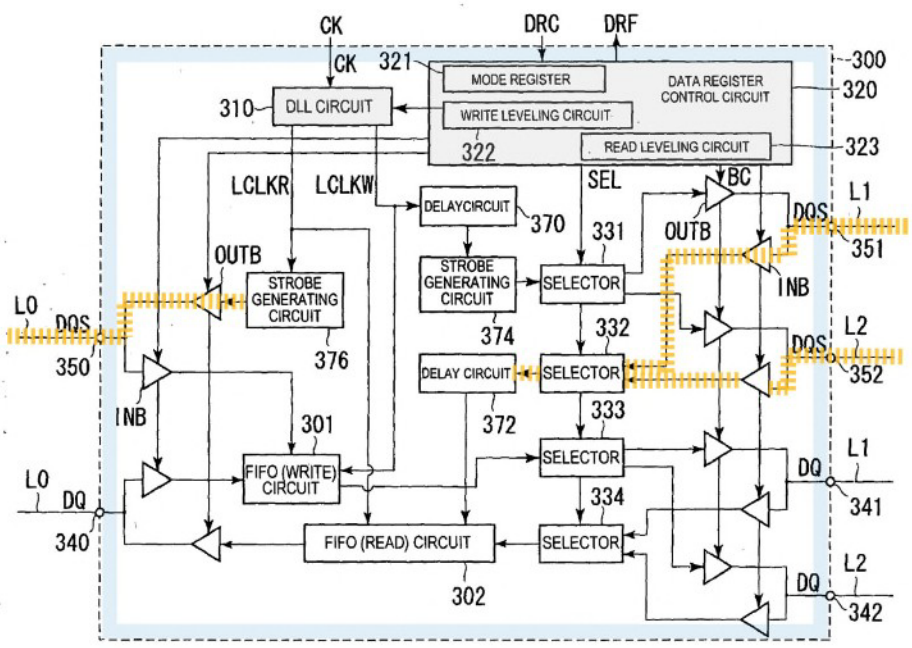


FIG.5

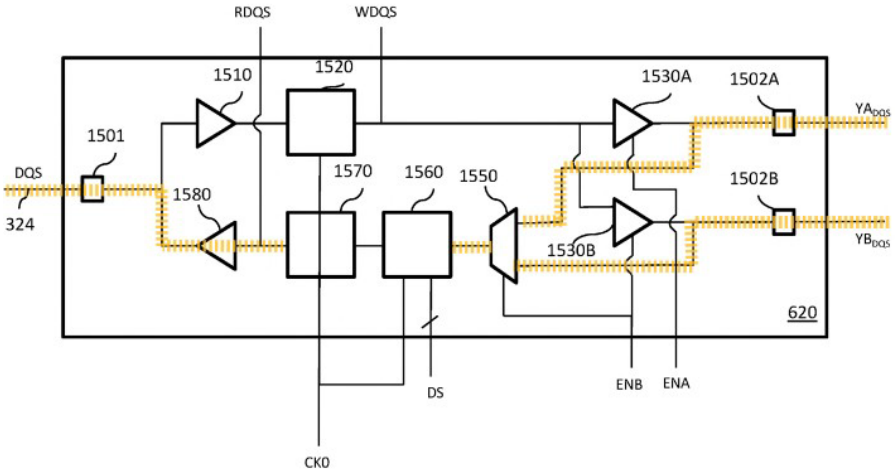

RDQS
WDQS
1510
1520
1530A
1502A
YA_DQS
1501
DQS
324
1580
1570
1560
1550
1502B
1530B
YB_DQS
620
DS
ENB
ENA
CK0

FIG. 15

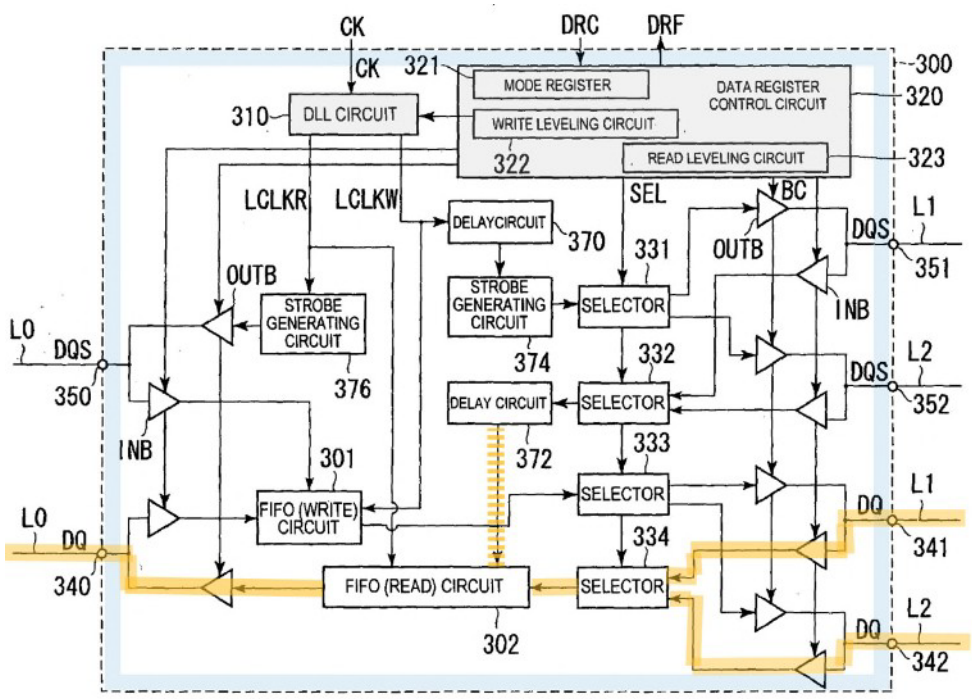

CK
DRC
DRF
CK
321
300
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
READ LEVELING CIRCUIT
322
323
LCLKR
LCLKW
DELAYCIRCUIT
370
SEL
BC
L1
DQS
351
OUTB
331
OUTB
STROBE GENERATING CIRCUIT
STROBE GENERATING CIRCUIT
SELECTOR
INB
L0
DQS
350
376
374
332
L2
DQS
352
DELAY CIRCUIT
SELECTOR
INB
301
372
333
SELECTOR
L1
L0
DQ
FIFO (WRITE) CIRCUIT
DQ
341
334
340
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
302
342

FIG.5

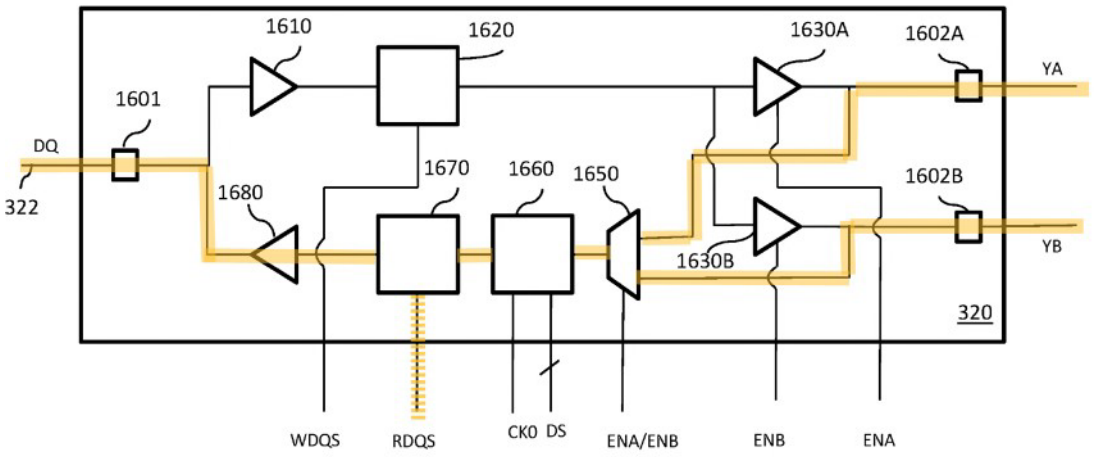


FIG. 16

EX1003, ¶222.

Additionally, the first and second data paths in Hiraishi include a sampler, e.g., a register circuit, that samples the strobe signal in accordance with the local clock signal, and samples the data signal in accordance with the sampled strobe signal, just like in Figures 15-16 of the '608 Patent (above). EX1003, ¶223; EX1001, 13:23-27, 17:10-13. For a read operation, Hiraishi teaches that sampling happens at delay circuit 372 to delay the DQS signal by about 90 degrees, and that sampling happens in accordance with the Data Register Buffer's local clock (e.g., to detect the phase of the DQS signal). EX1003, ¶223; EX1005, ¶[0091]; EX1028, FIGS. 2-4 (showing phase comparator 35 sampling the strobe signal DQS in accordance with a local clock CLKb to delay the strobe signal by 90 degrees). Thus, a POSITA would have

understood that Hiraishi's delay circuit "*samples the strobe signal* [DQS] *in accordance with the local clock signal.*"

As shown above in Figure 5, Ground 1 teaches that sampling the data signal in accordance with the sampled strobe signals happens at the FIFO (Read) circuit (302). EX1003, ¶224; EX1029, ¶[0020]. A POSITA would understand that this process requires a latch: the delay circuit 372 provides the sampled strobe signal that determines the timing for how the FIFO clocks in the data, and when the data signal is latched in the FIFO, it necessarily is sampled (registered), and because the delayed DQS strobe signal acts "as an input trigger signal" to latch the data in the FIFO (Read) circuit 302, the data is necessarily sampled in accordance with the sampled strobe signal. EX1003, ¶224; EX1005, ¶[0091]; EX1021, 331-35.

10. Claims 11-12

The limitations of claims 11-12 are substantially identical to earlier limitations, as shown in the following table:

Claim…	…is substantially similar to claim…	…and obvious for at least the same reasons above and in EX1003:
11	4	¶¶225-226 (¶¶192-193)
12	5	¶¶227-228 (¶¶194-198)

B. Ground 2: Ground 1 + Tokuhiro (claims 1-12)

To the extent the '608 Patent's claims are interpreted to require that "*a second memory operation*" is a read operation where the read data is delayed by an amount determined in the direction of a write operation, Ground 1 in further view of Tokuhiro renders obvious claims 1-12.

1. Motivations to Combine

Tokuhiro teaches that a DDR3 memory interface employs fly-by topology for connections between a memory controller and a DIMM (Dual Inline Memory Module). EX1003, ¶230; EX1006, 1:22-33, 2:54-59. Tokuhiro teaches that fly-by delays need to be compensated for both write *and* read data, and problems arise if the fly-by delay in read operations exceeds one clock period. EX1006, 3:9-12; EX1003, ¶230.

Tokuhiro solves this problem of large fly-by delays by delaying the transmission of read data before it enters the receiver's common clock domain, without the need for special mechanisms like FIFO. EX1003, ¶¶230-231; EX1006, 3:16-26, 18:66-19:7, FIGS. 5-7, 11. To do this, Tokuhiro discloses "a ***second variable delay unit*** for delaying, in the ***read operation***, a data signal input from the memory ***by a second delay time***." EX1003, ¶231; EX1006, 3:16-26. Tokuhiro also teaches that, for the ***read*** operation, the "***second delay time ... is set based on the first delay time***" which is determined in the direction of a ***write*** operation. *Id*. Thus,

Tokuhiro discloses a similar technique to the '608 Patent's disclosure. *See* EX1003, ¶¶232-236.

Tokuhiro and Hiraishi are analogous art to the '608 Patent since each is directed to improving memory modules in which the memory chips are arranged in a fly-by configuration—e.g., DDR3. EX1003, ¶237. A POSITA would have been motivated to combine Tokuhiro and Hiraishi for at least three reasons, discussed below. *Id*.

a) First motivation: Tokuhiro teaches calculating read delays based on delays for write operations, which is more efficient than Hiraishi's technique of read leveling independent of write delays

Hiraishi recognizes that "because the data DQ is buffered by the data register buffer 300," the timing is off between DQ/DQS-Pre and DQ/DQS-Post, thus recognizing the necessity of timing adjustments. EX1003, ¶238; EX1005, ¶[0104], FIG.7 (below).

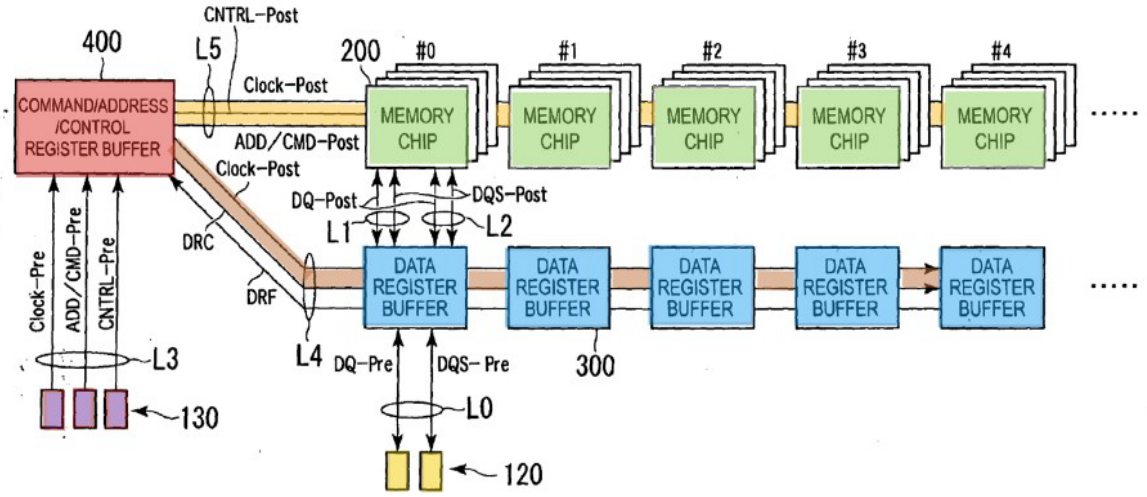


FIG.7

In Hiraishi, these timing adjustments include write and read leveling operations, which are performed independently. EX1003, ¶¶239-241; EX1005, ¶¶[0140], [0151], [0161], FIGS. 14-17 (with FIG.15 ("S4" read leveling) and FIG.17 ("S5" read leveling) below).

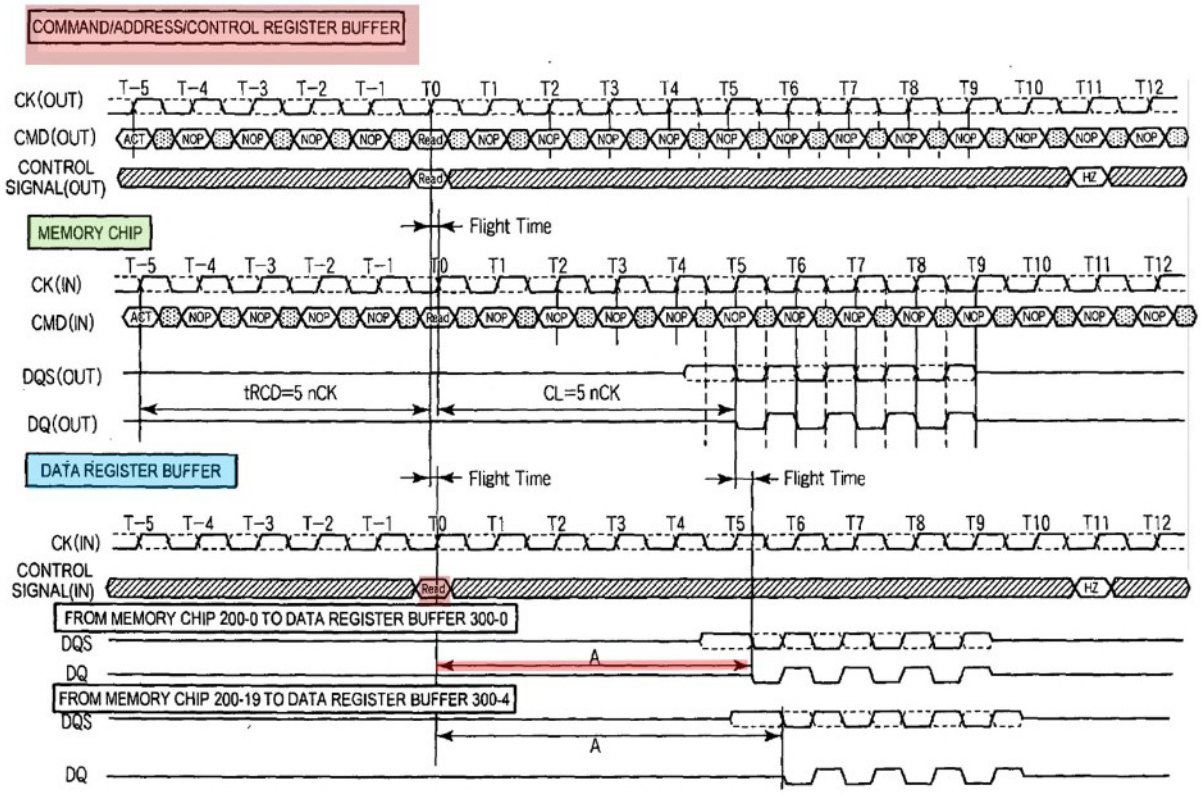
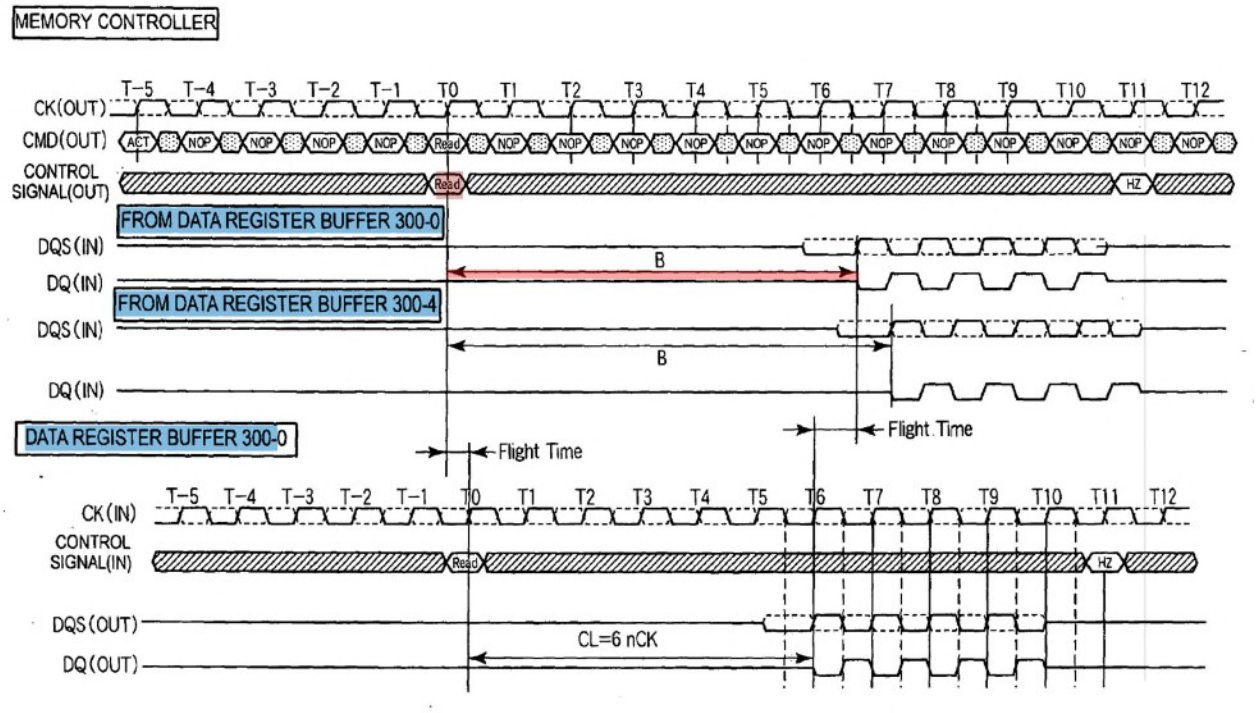


FIG.15

For example, Hiraishi's S4 read leveling delays the read data and strobe signals to output at the same time despite the data arriving from different memory devices at different times A (FIG.15, above). *Id.*; EX1005, FIG.11, ¶[0130].

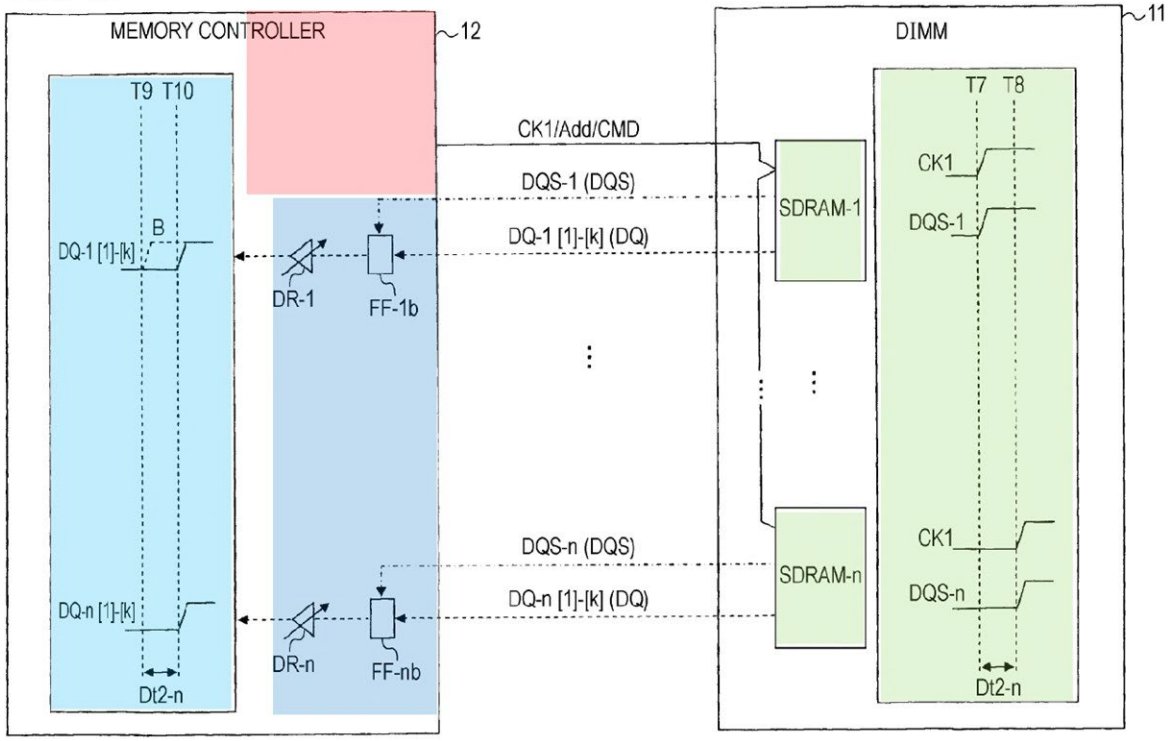


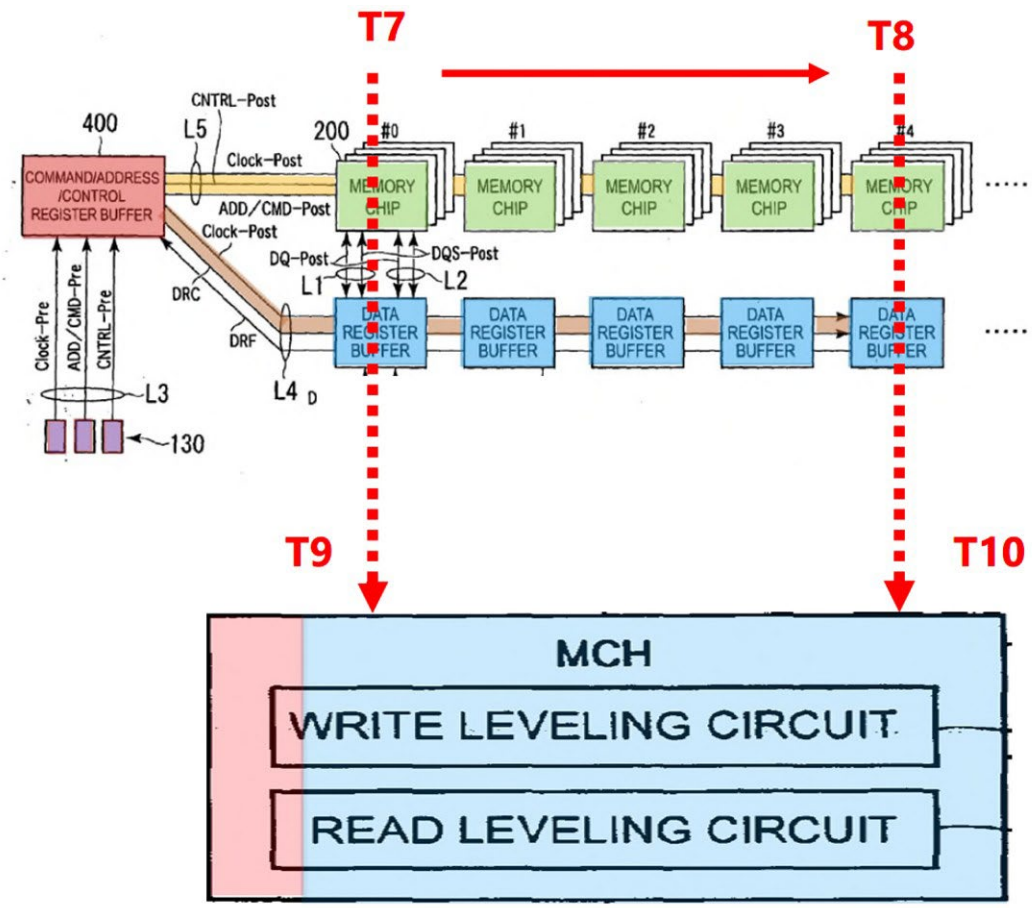
Similarly, Hiraishi's S5 read leveling needs to handle the different arrival times B (FIG.17, above) of read data to the memory controller from different data buffers due to fly-by delays. EX1003, ¶241.

A POSITA would have understood that performing these read leveling operations independently from write leveling, as in Hiraishi, requires time and corresponding circuitry, thus motivating her to simplify these operations, e.g., by using Tokuhiro's technique of setting read delays based on write delays. EX1003, ¶¶242-245, 247; EX1006, Abstract, 18:66-19:7, FIG.11 (below, showing read delay elements DR-1 to DR-n in Tokuhiro so all read data arrives at T10, rather

than between T9 and T10 due to fly-by delays); EX1005, ¶¶[0129-30], FIGS. 11, 7 (below, adding MCH and timing T7 to T10 to show similar fly-by delays in Hiraishi).

FIG. 11

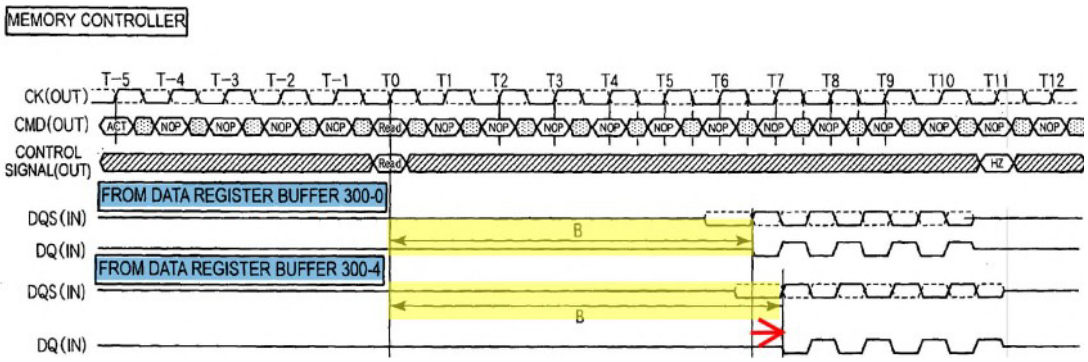




This combination would have been well known within the skill at the time, since Tokuhiro details how to calculate read delays based on write delays, expectedly providing a memory system with a simplified read leveling operation. EX1003, ¶247. Write and read leveling techniques were well known at the time, EX1020, 26-27, 31, 33, 42-45, 48-54, and can be the claimed "operations" according to Netlist, EX1035, 39, 42-43, 49-52; EX1048, 54; EX1057, 62; EX1003, ¶246.

b) Second motivation: Tokuhiro provides simple techniques for removing fly-by delays, while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays

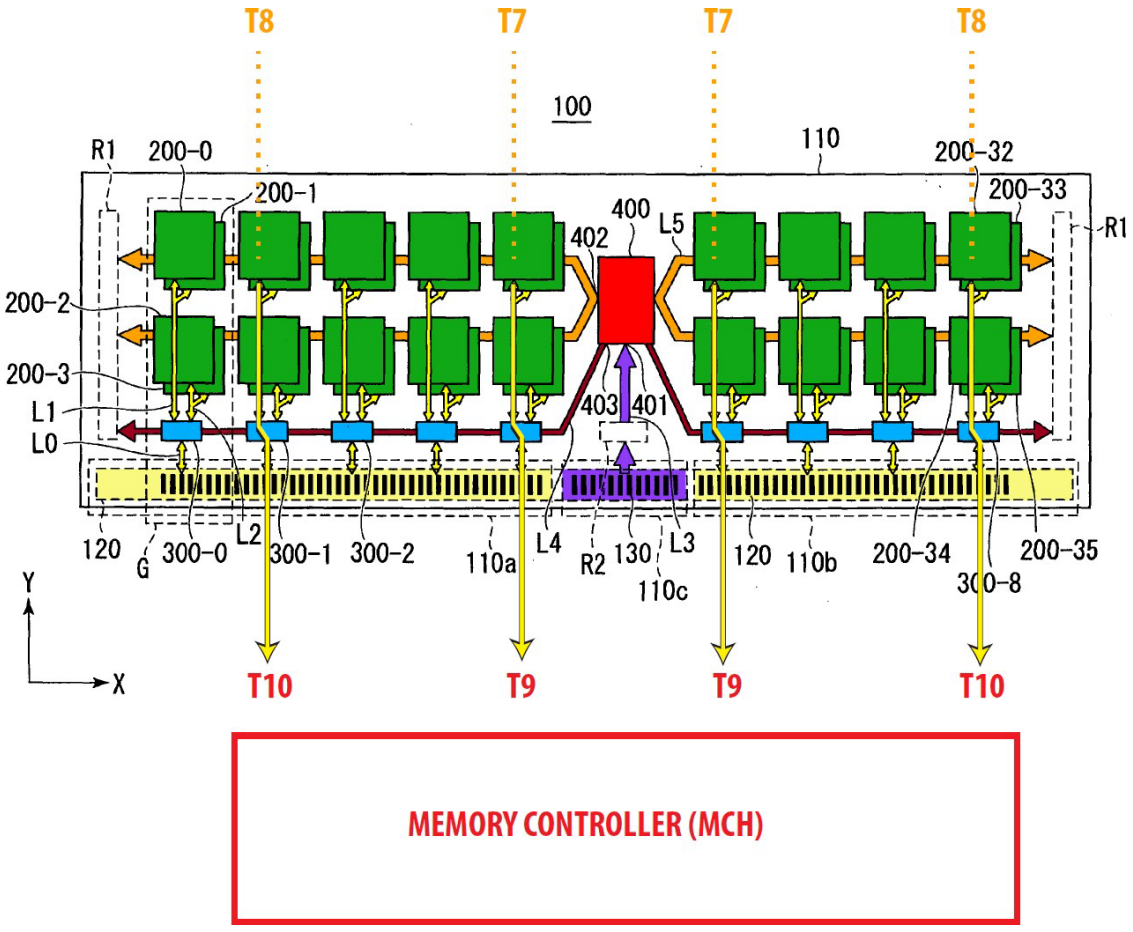
Hiraishi discloses both "S4" and "S5" read leveling. EX1003, ¶¶248-249; EX1005, ¶¶[0151], [0130], [0161], FIGS. 15, 17. Even after "S5" read leveling, however, the read data arrives at the memory controller from different data buffers with different "time B" delays, so Hiraishi's memory controller must remove the fly-by delay (red arrow) between the different data buffers. EX1003, ¶249; EX1005, FIG.17:

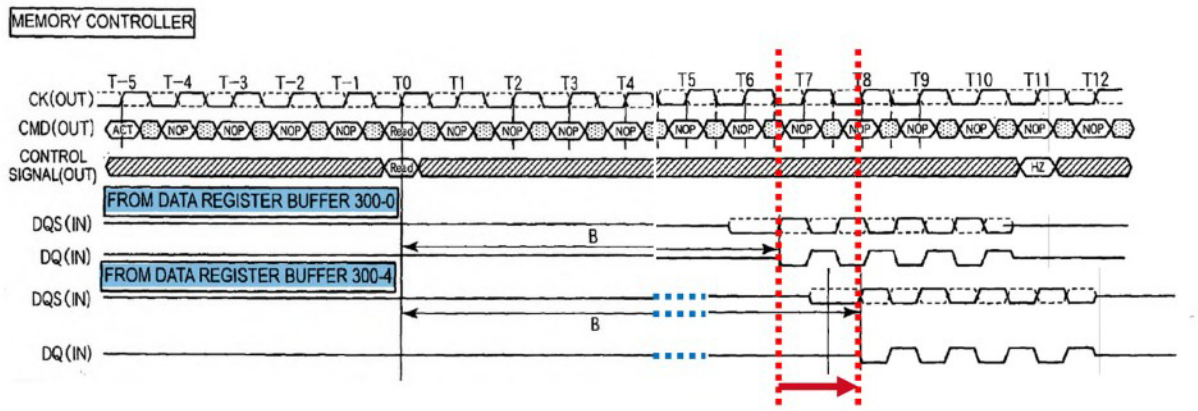


A POSITA would have understood that Tokuhiro's "DR" delay circuits, which remove fly-by delays without the need for a special FIFO, could be used in connection with Hiraishi to compensate for the remaining fly-by delays, making the read data arrive at the memory controller at substantially the same time. EX1006, 18:66-19:7; EX1003, ¶250. A POSITA would have thus been motivated to use Tokuhiro's simple technique of delay circuits DR with Hiraishi's memory module. EX1003, ¶251.

c) Third motivation: Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not

A POSITA would have understood that Hiraishi suffers from the same problem identified by Tokuhiro: fly-by delays greater than one clock cycle. EX1003, ¶¶252-255; EX1005, ¶[0005], FIG.1 (Hiraishi's module annotated below to show times T7 to T10 from Tokuhiro FIG.11 where the delays T7 to T8, and T9 to T10, can be greater than one clock cycle), FIG.17 (Hiraishi's timing modified below to show a fly-by delay greater than one clock cycle); EX1006, FIG.11, 2:54-59, 3:9-12, 3:16-26, 18:43-53. Delays greater than one clock cycle were a known problem that had been solved with special FIFO circuitry. EX1024, 5:25-31, 6:56-7:2.





Hiraishi is silent about handling delays greater than one clock cycle (see modified Hiraishi's FIG.17 above). EX1003, ¶256; EX1005, ¶[0160], FIG.17. A POSITA would have known about the problem of fly-by delays greater than one clock cycle, motivating her to look for solutions such as Tokuhiro's technique of using simple "DR" delay circuits. EX1003, ¶¶256-258; EX1006, 18:66-19:7.

2. The combination of Ground 1 in further view of Tokuhiro relied upon here

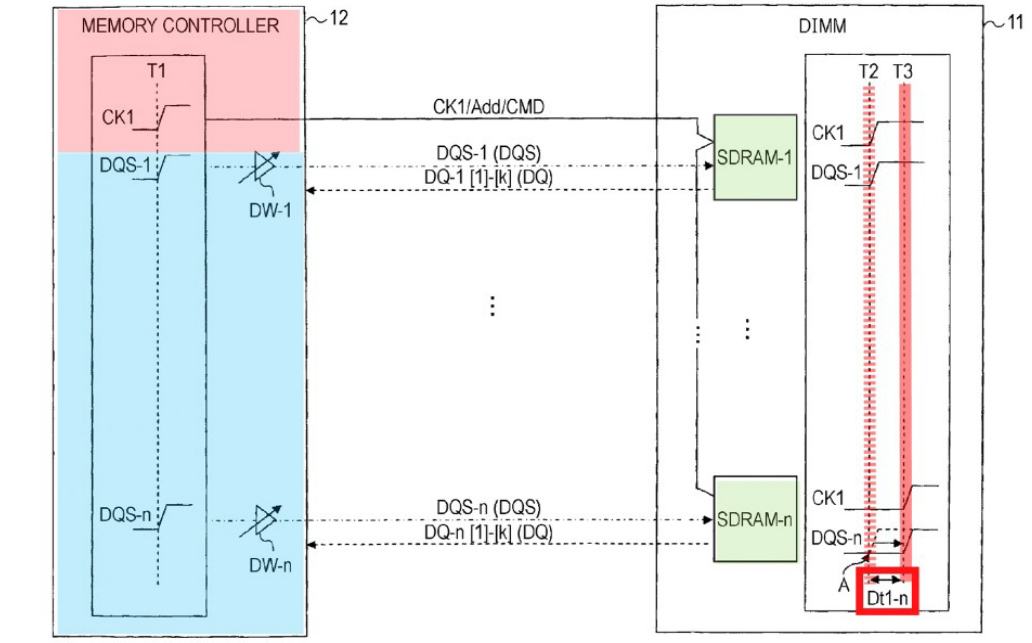
a) It would have been obvious to implement Tokuhiro's delay elements in Hiraishi's data register buffers

It would have been obvious to a POSITA to implement Tokuhiro's delay functionality in Hiraishi's data register buffers, and a POSITA would have had a reasonable expectation of success in doing so. EX1003, ¶¶259-261. A POSITA would have understood from Tokuhiro's teaching that delay elements DR1 and DR2 (purple, FIGS. 5-6, below) can compensate for fly-by delays of read data (e.g., Dt2 in FIG.11, below) using the delays for write operations (e.g., Dt1 in FIG.7, below),

even if the fly-by delay between two memory devices is larger than one clock cycle (e.g., between SDRAM-1 and SDRAM-n). EX1003, ¶233; EX1006, FIG.7; EX1003, ¶234; EX1006, FIG.11 (below, showing delay elements so all read data arrives at T10); EX1003, ¶236; EX1006, 18:66-19:7, FIGS. 5-6. The memory devices in Hiraishi interface with the data register buffers, not directly with the memory controller (MCH). EX1003, ¶263. A POSITA would have understood that Tokuhiro's delay functionality can be implemented in Hiraishi's data buffers or memory controller—a finite number of predictable solutions to the same problem—rendering both solutions obvious. And since Hiraishi already teaches read (and write) leveling circuitry in the data register buffers, a POSITA would have been motivated to implement Tokuhiro's delay elements (DR) in Hirashi's data buffers (shown below). *Id.*

For example, Tokuhiro recognizes the problem that the clock CK1 (and corresponding address and command signals) arrive with different delays (e.g., at times T2 (dashed red line) and T3 (solid red line)) to different memory devices (SDRAM-1,…,SDRAM-n; green) due to the "fly-by" arrangement of those memories).

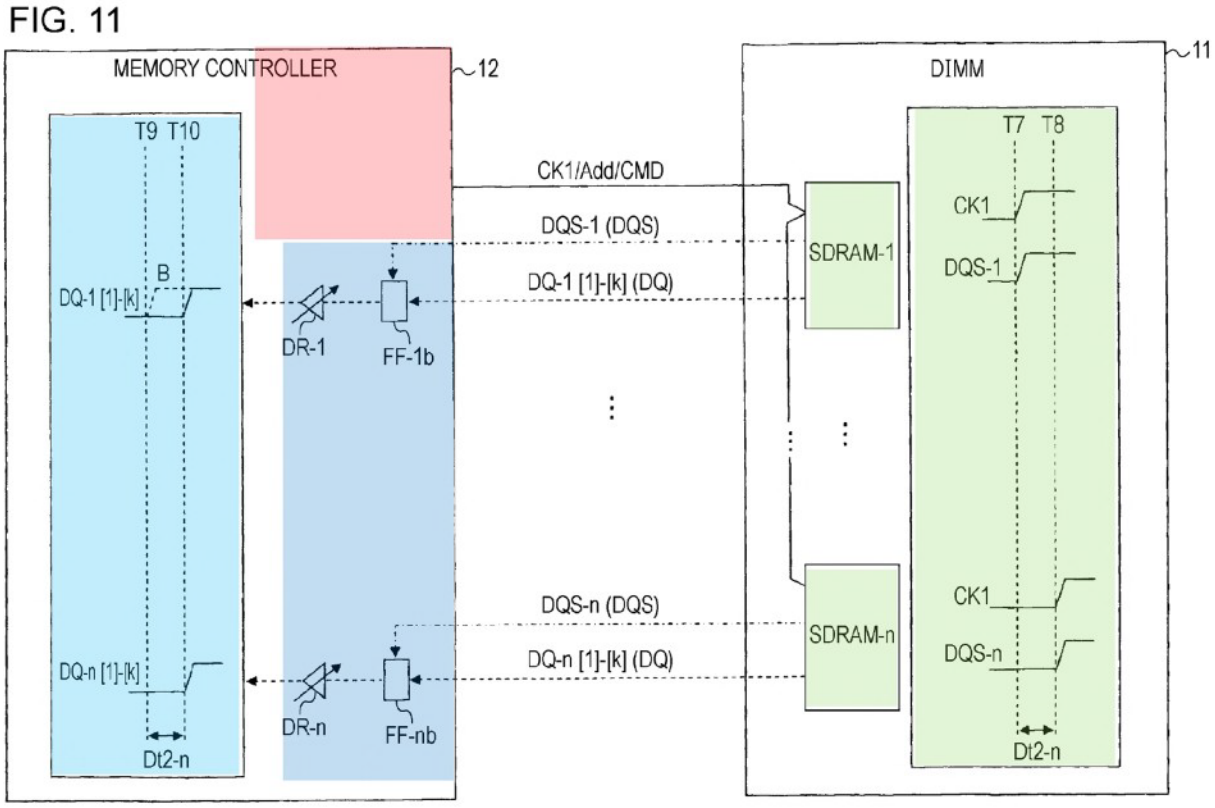
FIG. 7



EX1003, ¶233. Tokuhiro compensates those fly-by delays for read operations.

EX1003, ¶234; EX1006, FIG.11 (below).

FIG. 11



The details of delaying the data signals (solid orange) by delay elements DR1 and DR2 (purple) before those signals are captured by flip-flops FF6 and FF8 (olive green) in the clock domain (yellow) of the memory controller are illustrated by Tokuhiro's Figure 5 (for SDRAM-1) and Figure 6 (for SDRAM-n):

FIG. 5

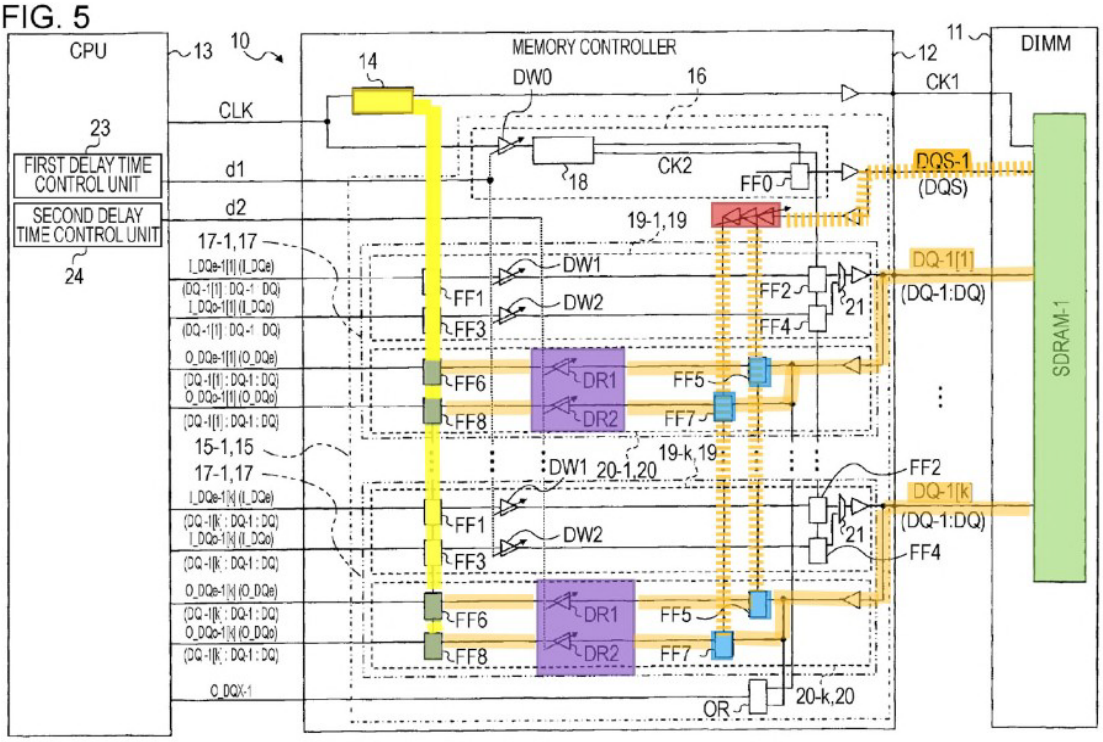
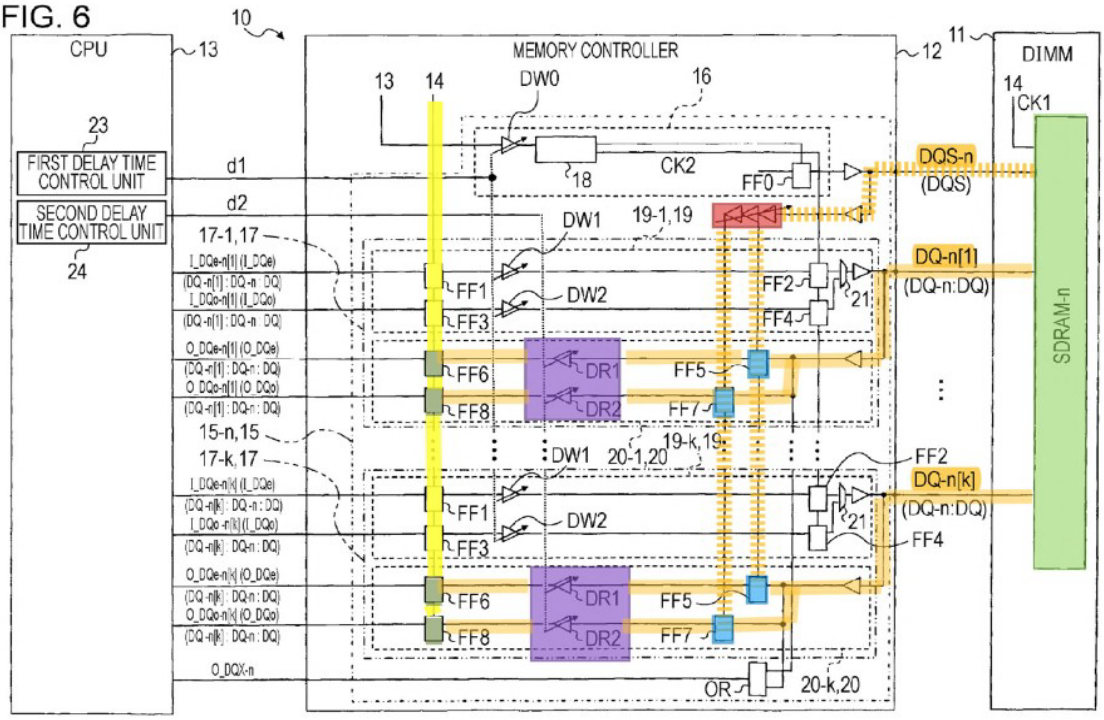


FIG. 6



EX1003, ¶235, EX1006, 10:63-12:5, FIGS. 5-6.

Tokuhiro teaches to apply the read delay (e.g., DR-1, purple) immediately after the corresponding read data from the memory (e.g., SDRAM-1, green) has been latched (e.g., by flip-flop FF5, blue, in red box, below), as illustrated in Tokuhiro's Figure 5 annotated below (upper left). EX1003, ¶261. Hiraishi teaches that the read data from the memory (DRAM, green added) is latched into FIFO (Read) Circuit 302 (blue, in red box, below). *Id.*; EX1005, FIG.5 (reproduced below, lower right, with annotations). Accordingly, a POSITA would have been motivated to add Tokuhiro's read delay elements (e.g., DR-1) to Hiraishi's data register buffer immediately after the read data from the memory is latched (red box), as shown below. *Id.*

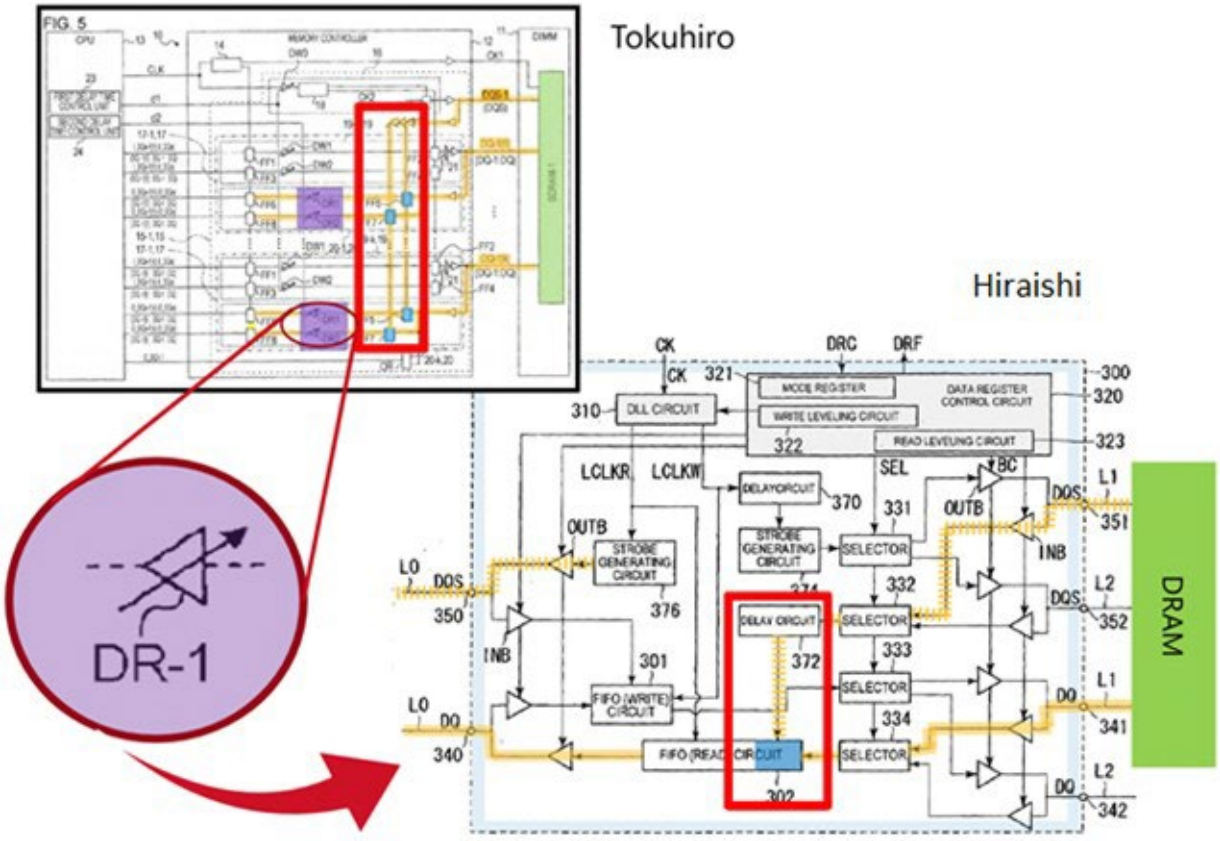


FIG.5

EX1003, ¶261.

In this combination, a POSITA would have understood that in a read operation, the data signal (DQ, 340) is transmitted from the data buffer to the memory controller with a corresponding strobe signal (DQS, 350) which is in sync with the data signal, and thus the strobe and data signals have to be in sync after Tokuhiro's read delay has been added to Hiraishi's data buffer. EX1003, ¶262; EX1005, FIG.5. Delaying both data and strobe signals was well known in the art, and disclosed by Tokuhiro for write operations. *Id*.; EX1006, FIGS. 5-6, 9:33-40. A POSITA would have understood that the same functionality could be implemented

in the data buffer of Hiraishi to delay the transmission of read data along with its strobe signal to the memory controller, such as illustrated in Hiraishi's Figure 5 (modified to show combination with Tokuhiro) below:

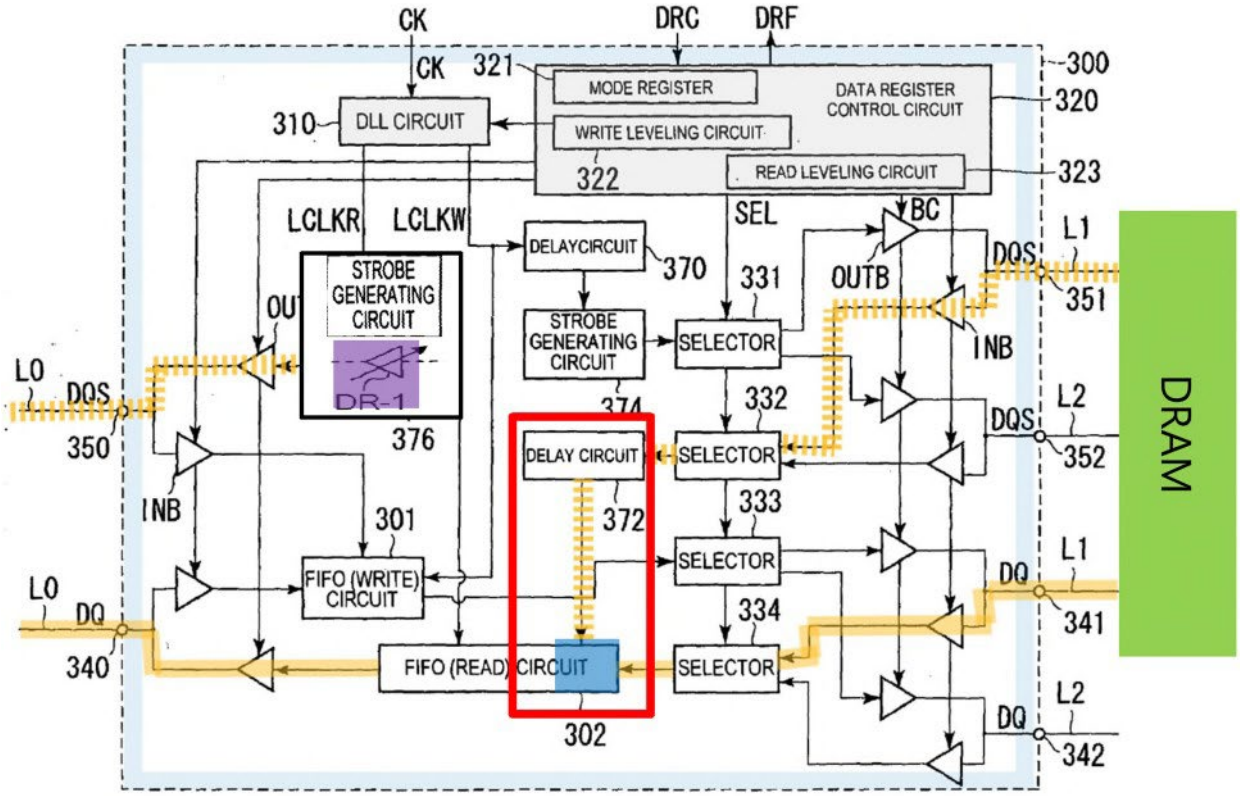
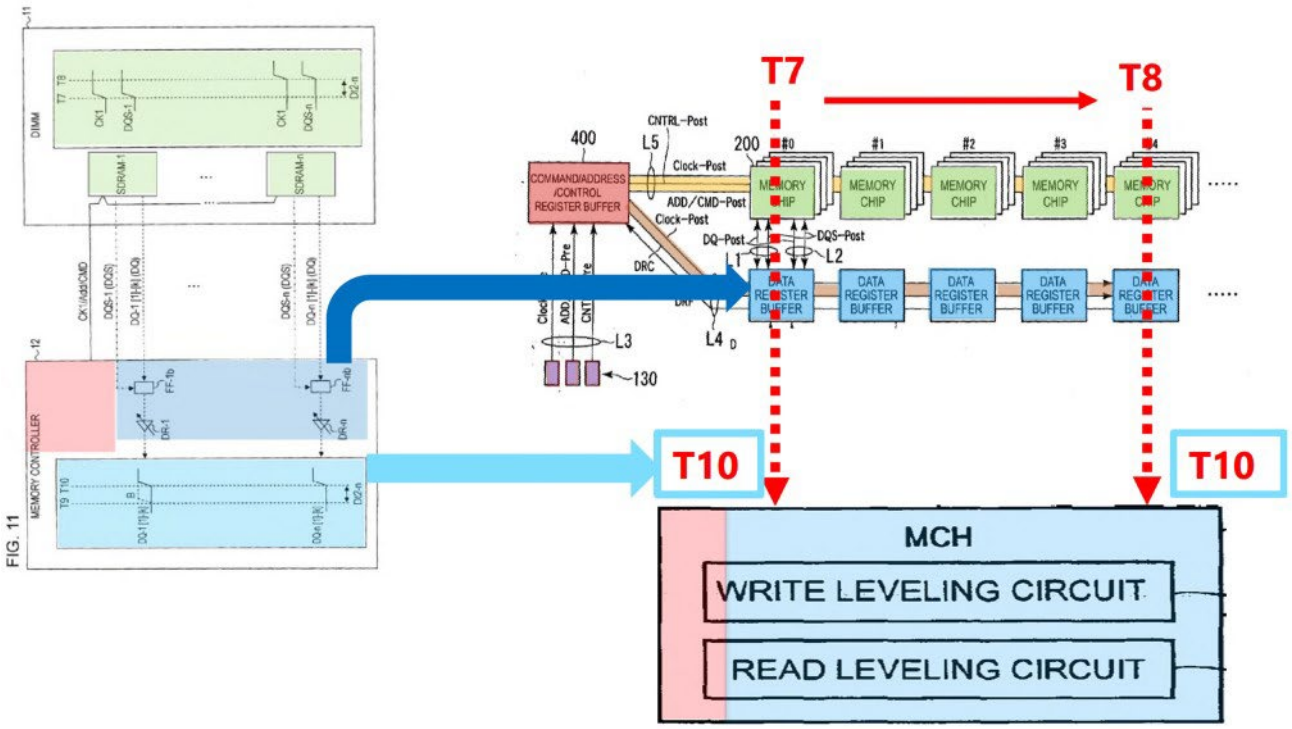


FIG.5

EX1003, ¶262.

In this combination, Tokuhiro's read delay functionality (DR-1, purple) is added to Hiraishi's data buffer to remove the large fly-by delays. Based on Tokuhiro's teachings, the read delay circuit DR-1 (purple) is added to the Strobe Generating Circuit 376 to delay both the strobe signal DQS 350 and the signal clocking out data from FIFO (Read) Circuit 302 so that the delayed data DQ 340 from the Read FIFO is in sync with the delayed strobe 350. EX1003, ¶262; EX1020,

p.56; EX1006, 18:53-64. Alternatively, delay elements similar to Tokuhiro's DR elements can be used instead of (or in addition to) Hiraishi's FIFO circuit for delaying the read data. EX1003, ¶262.



As illustrated above in Tokuhiro's Figure 11 (left) and Hiraishi's Figure 7 (right), the combination advantageously implements the functionality of the additional read delay of Tokuhiro in the data register buffers of Hiraishi (illustrated by the dark blue arrow), such that the read data arrives to the MCH at substantially the same time (T10) despite the fly-by delay (from T7 to T8), so the read data from all memories can be captured in one clock cycle, despite fly-by delays larger than one clock cycle. EX1003, ¶264.

A POSITA would have understood that this combination avoids the memory controller managing large fly-by delays, thus requiring less circuity and functionality for implementation, such as extra logic and circuitry to re-order read data captured in different clock cycles. EX1003, ¶265. Another advantage is that large fly-by delays are removed on the module at the first practically available location (the data buffers, since JEDEC-compliant memory devices would not have such delay elements), preventing these delays in the rest of the system. EX1003, ¶266; EX1006, 2:45- 59.

b) It would have been obvious for either Hiraishi's memory controller or module controller to program Tokuhiro's delay elements in Hiraishi's data buffers

A POSITA would have understood that there are two potential ways to implement Tokuhiro's technique of adding read delay elements to Hiraishi's data buffer to solve the problem of large fly-by delays: (1) the ***system memory controller*** could determine the read delays based on the timing for a write operation *during* write leveling and program the read delay elements in the data buffers accordingly, or (2) the ***module controller*** could determine the read delays based on the delays measured by the data buffers during a write operation *before* write leveling (when the memory controller issues a write command to the memory module) and program the read delay elements in the data buffers accordingly. EX1003, ¶¶268, 271;

EX1006, 16:18. Either way, the result is that the memory controller does not have to manage large fly-by delays when capturing read data. EX1003, ¶271.

(1) First implementation of the combination (system memory controller determines the read delay)

A POSITA would have understood that the system memory controller in Hiraishi can determine the fly-by delays on the module during write leveling as taught by Tokuhiro. EX1003, ¶272; EX1006, FIG.7. Tokuhiro explains that the Dt1 delay times obtained from write leveling are used to set the delays Dt2 for the read data. *Id.*; EX1006, 16:43-46, FIGS. 7, 11. Thus, in this implementation of the combination, a POSITA would implement Tokuhiro's calculation of the fly-by delays based on write leveling in Hiraishi's system memory controller and, based on these fly-by delays, the system memory controller would program the additional read delay elements in the data buffers. EX1003, ¶273. A POSITA would implement Hiraishi's "S5" leveling operations (between the system memory controller and data buffers) so that the system memory controller performs write leveling, then programs the read delay elements in the data buffers (based on the write delays) to remove fly-by delays, and then performs any necessary read leveling (without fly-by delays) for any fine tuning of DQ/DQS alignment. *Id.*; EX1005, ¶¶[0091], [0141], [0161], [0163], FIG.13 (below with annotations in accordance with the first implementation).

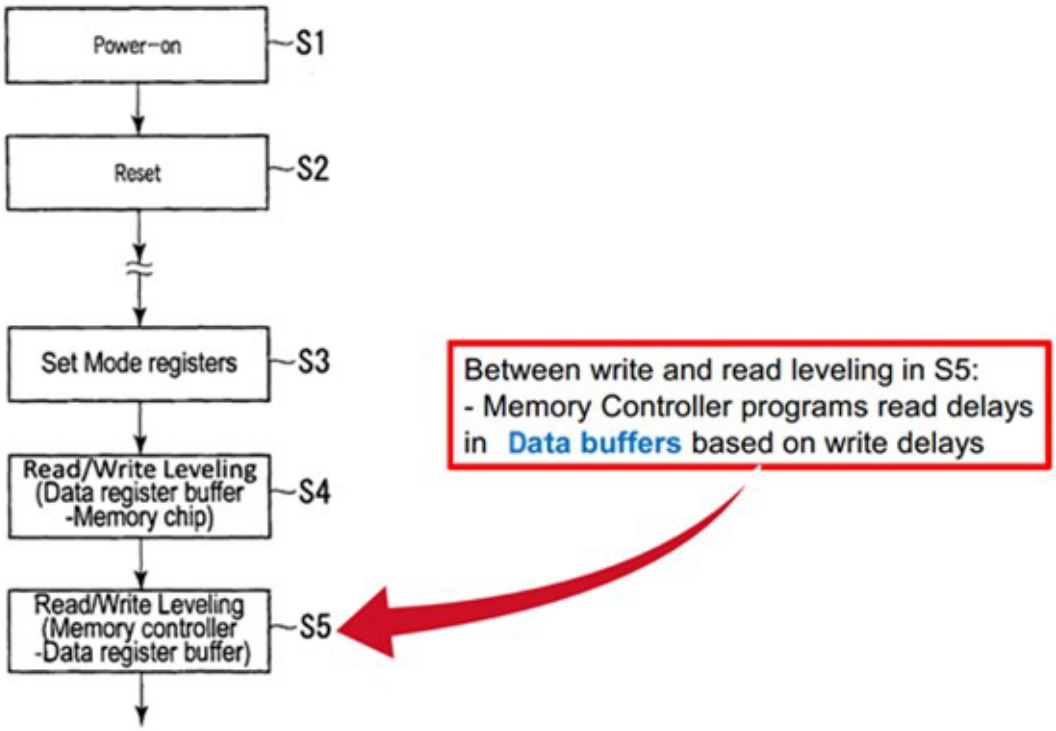


FIG.13

As taught by Tokuhiro, this results in the read data arriving at the memory controller without substantial fly-by delays, simplifying the memory controller's job and circuitry. EX1003, ¶273.

This implementation was well within the level of ordinary skill and provided nothing more than what was expected from the combination. EX1003, ¶274. For example, implementing Tokuhiro's read delay functionality in Hiraishi's data buffers comprises adding a known function (delaying read data as taught by Tokuhiro) to a known data buffer of Hiraishi, where the data buffer already had similar functionalities, including read and write leveling functions. *Id.* Similarly, since

Tokuhiro taught how to calculate and set those read delays, a POSITA would have understood how to modify Hiraishi's system memory controller to add the same functionalities and the result is as expected: the MCH does not have to manage delays larger than one clock cycle when trying to capture the correct values of read data. *Id.*

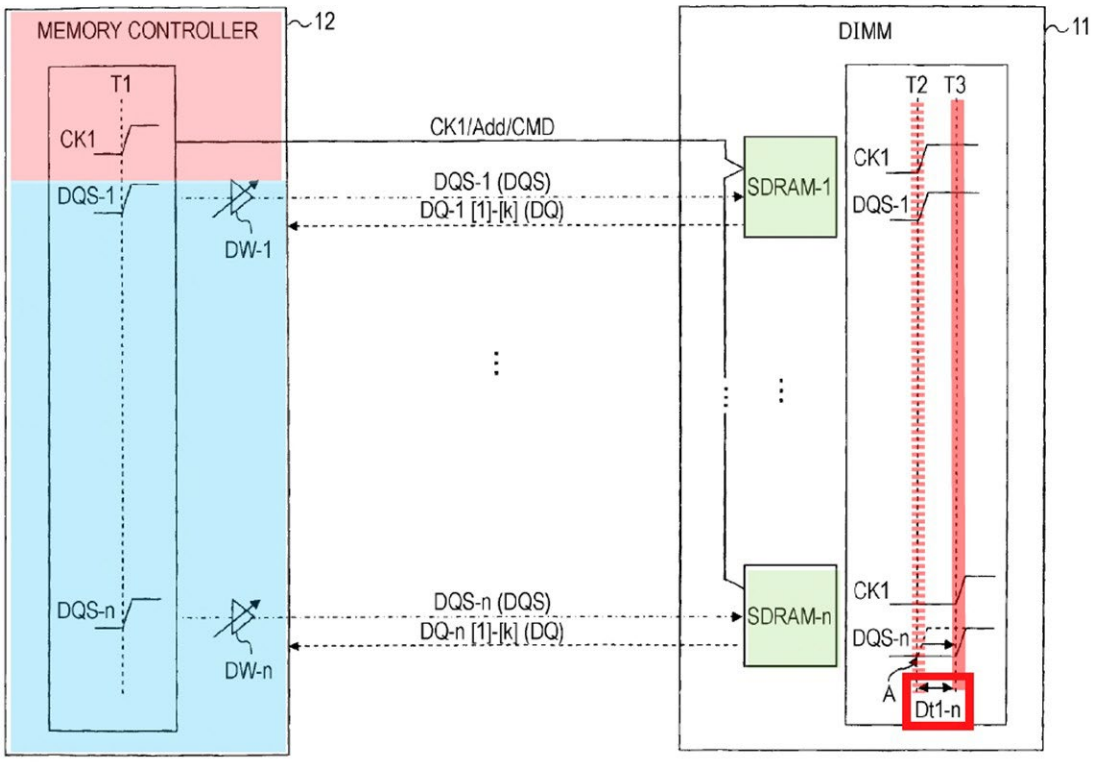
(2) Second implementation of the combination (module controller determines the read delay)

Additionally, a POSITA would have understood (and had a reasonable expectation of success) that Tokuhiro's technique can also be implemented in Hiraishi's memory module such that the ***data buffer circuits*** measure timing information to determine the fly-by delays during a write operation, and Hiraishi's ***module controller*** programs the corresponding read delays in the data buffers. EX1003, ¶275.

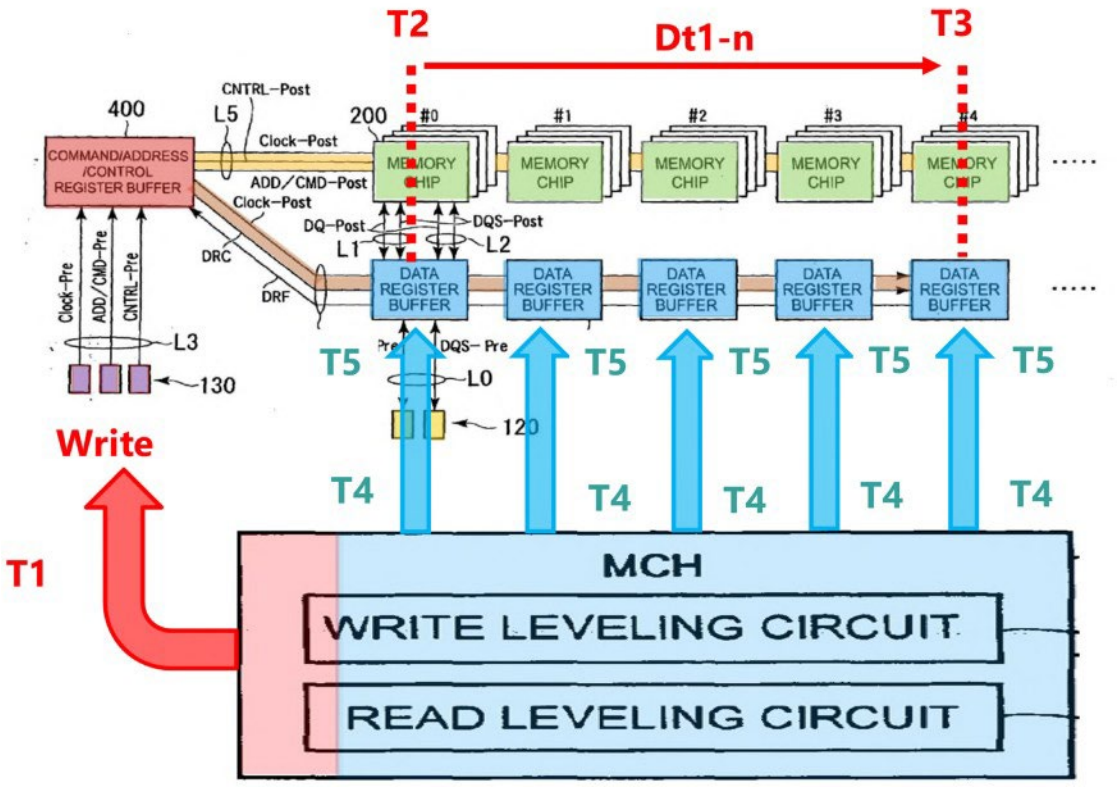
A POSITA would have been motivated to implement Tokuhiro's technique in Hiraishi's module, as opposed to the memory controller, because Hiraishi teaches that functionalities of the memory controller—including interfacing with the memory chips and performing read and write leveling—can be performed by the module controller and data buffers. EX1003, ¶276; EX1005, FIG.5, ¶[0151]. Tokuhiro explains that, before the write leveling, the write strobe signals arrive to the module at substantially the same time (T2), but the corresponding

clock/address/command signals have respective fly-by-delays in the chain (such as a delay Dt1-n for the n-th device). EX1006, FIG.7 (below), FIG.10, 13:30-37.

FIG. 7



Accordingly, a POSITA would have been motivated to use Hiraishi's time measuring technique in the data buffer to determine the fly-by delays during a *write* operation and set the *read* delays as taught by Tokuhiro and shown below. EX1003, ¶¶276-277; EX1006, FIGS. 7, 10; EX1005, FIG.7 (annotated below).



In this implementation, the write command arrives at each data buffer with respective fly-by delays (Dt1) dependent on the distance from the module controller. EX1003, ¶278. The write data (blue arrows), however, would arrive at each data buffer substantially at the same time T5, since the write leveling delays have not yet been applied by the memory controller. Thus, each data buffer can measure the time difference between when the write command is received (between T2 and T3, depending on the buffer) and when the data arrives (T5). *Id.*

A POSITA would have understood that those time differences for a write operation can be measured using the technique that Hiraishi's data buffer already uses to determine a time delay between receiving a read command and arrival of the

corresponding read data. EX1003, ¶279; EX1005, ¶[0151], FIG.15. Thus, a POSITA would have understood that the functionality of measuring the time difference between receipt of a read command and arrival of corresponding read data can also be implemented to measure the time difference between receipt of a write command and arrival of corresponding write data. EX1003, ¶279. Accordingly, a POSITA would have been motivated to use Hiraishi's time measuring technique to measure a time interval between the arrival of a write command (e.g., T3) and the respective strobe signal (DQS) travelling with the corresponding write data (DQ) (e.g., T5) to determine the corresponding fly-by delays (e.g., Dt1-n). *Id.*

A POSITA would have understood that Hiraishi's memory buffers can use the feed-back channel DRF to communicate the measured time intervals to the module controller which can then use those time intervals to determine the corresponding fly-by delays for a read operation as taught by Tokuhiro, and program the read delay elements in the data buffers for transmitting the read data accordingly. EX1003, ¶280; EX1005, ¶¶[0089], [0099]. Alternatively, the module controller can send information, such as a maximum delay time, to the memory buffers and the memory buffers can determine and program the read delays. *Id.*; EX1006, 16:15-42.

In this implementation, Tokuhiro's read delay functionality is added to the data register buffers of Hiraishi's module such that, advantageously, no changes to the circuitry of the memory controller are necessary. EX1003, ¶281. Tokuhiro's

functionality of determining the fly-by delays from write operation delays and setting the read delays accordingly is implemented in Hiraishi's memory module, as shown in modified FIG.13 below. *Id.*

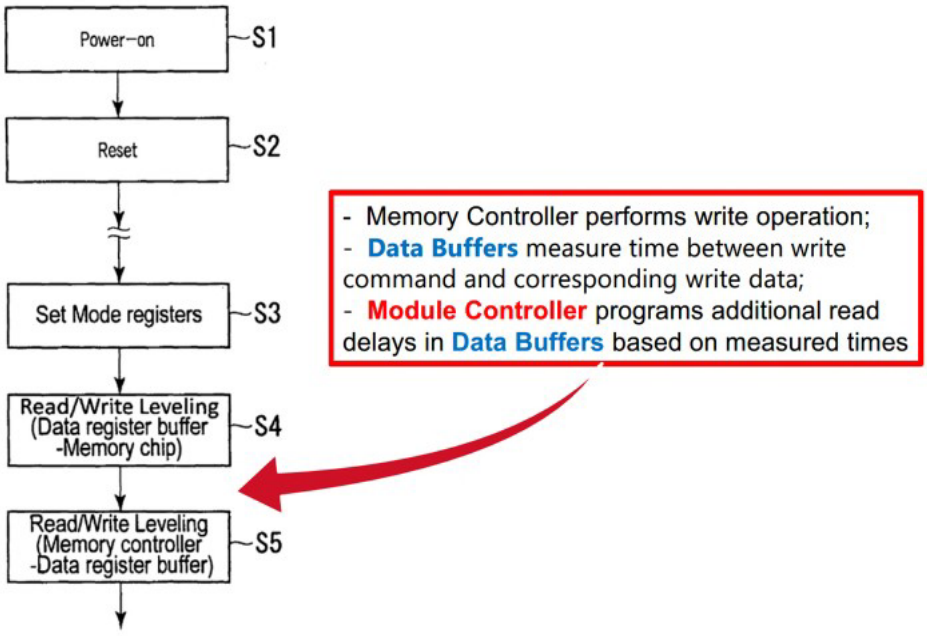


FIG.13

EX1003, ¶281.

3. Claim 1

Claim limitations 1[pre] through 1[e] are disclosed by Ground 1 as explained above. *Supra*, pp.14-39. Claim limitation 1[f] is satisfied by the combination of Ground 1+Tokuhiro (Ground 2) as explained above, *supra* pp.72-97, and shown below:

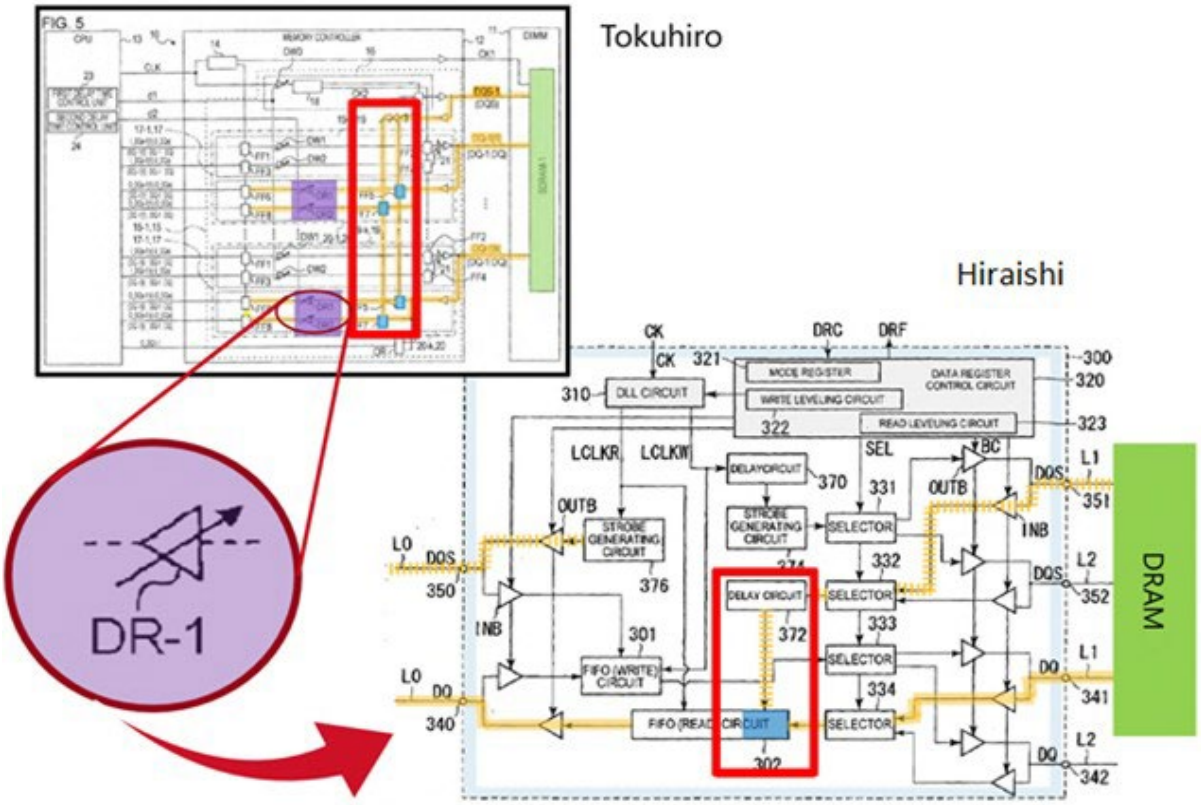


FIG.5

The first implementation of Ground 2, *supra* pp.91-93 (where the delay element is added to Hiraishi's buffer circuits, and the ***system memory controller determines the fly-by delays*** during write leveling) satisfies limitation 1[f] under Netlist's apparent claim interpretation. EX1003, ¶¶282-285. In this combination, "*the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path* [*i.e.*, using delay elements, as taught by Tokuhiro to delay DQ and DQS signals on data path L0 (see Tokuhiro FIG.5 and Hiraishi FIG.5 annotated above)] *by an amount determined by the*

command processing circuit in response to at least one of the module control signals [e.g., the memory controller performs write leveling and programs the read delay elements in Hiraishi's data buffers (similar to Netlist's infringement allegations)]." EX1003, ¶285; EX1005, FIG.13:

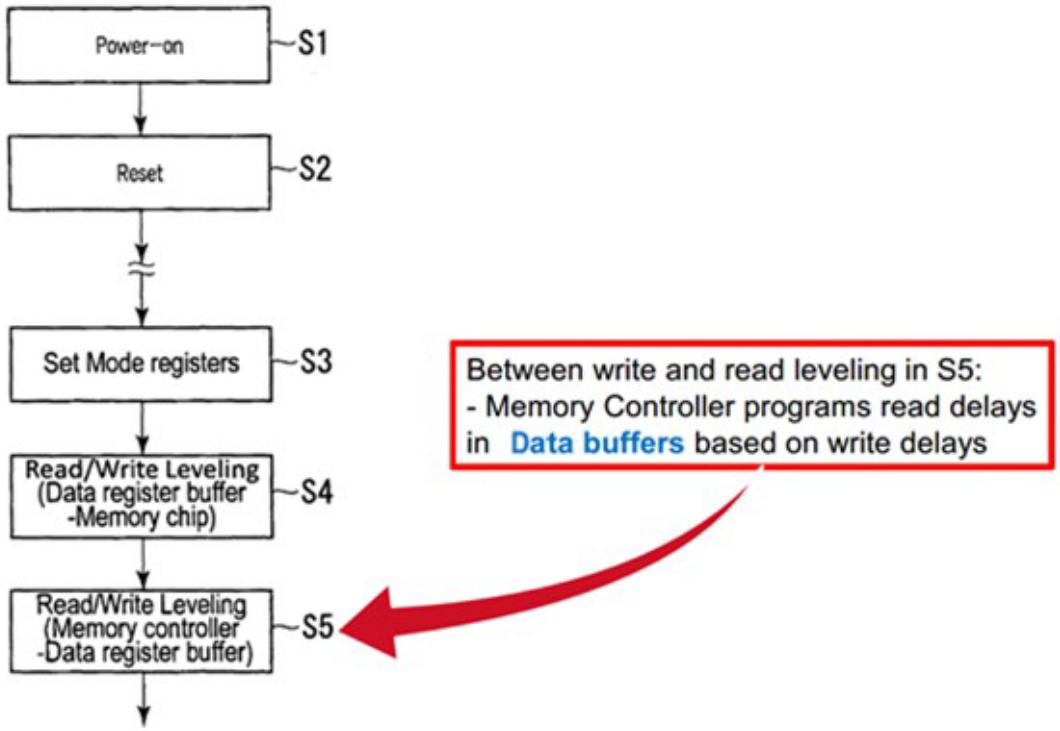


FIG.13

The second implementation of Ground 2, *supra* pp.93-97 (where the ***module controller and data buffers on the module determine the fly-by delays*** during a write operation) also satisfies limitation 1[f] under a narrower construction. EX1003, ¶286. In this combination, "*the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing*

circuit and a delay circuit configured to delay a signal through the data path [e.g., using delay elements, as taught by Tokuhiro to delay DQ and DQS signals on data path L0 (see Tokuhiro FIG.5 and Hiraishi FIG.5 annotated above)] *by an amount determined by the command processing circuit in response to at least one of the module control signals* [e.g., by comparing the timing of DQ/DQS signals (from the memory controller) and a corresponding Write command (supplied by the memory controller and transmitted to the buffer circuits via the module controller)]." EX1003, ¶286; EX1005, FIG.13:

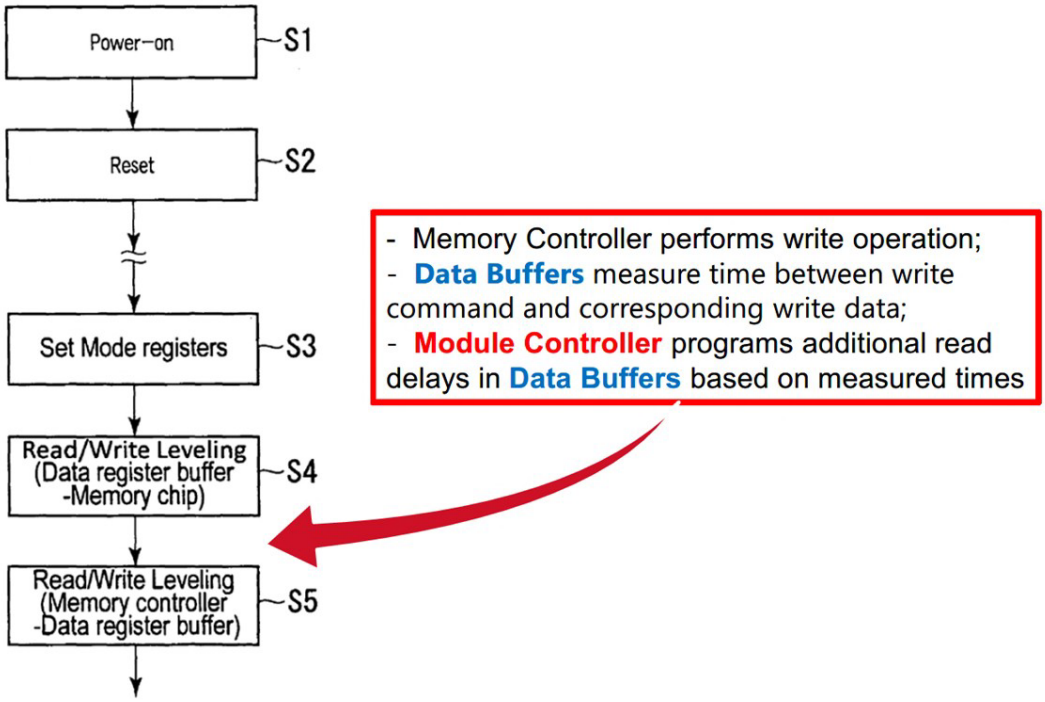


FIG.13

4. Claim 2

a) 2[a]: first and second memory operations

In the first implementation of Ground 2, *supra* pp.91-93, the "*first memory operation*" is an S5 write leveling operation, which is a "*memory operation*" according to Netlist, EX1003, ¶246, and is used in order to obtain delay timing information for the read delay elements in Hiraishi's data buffer for subsequent read operations. EX1003, ¶288.

In the second implementation of Ground 2, *supra* pp.93-97, the delay element is added to Hiraishi's buffer circuits and a time interval is measured by the data buffers during a write operation. EX1003, ¶288. In this combination, "*the memory operations include a first memory operation* [*e.g.*, a write operation initiated after S4 leveling but prior to S5 leveling (*see* modified Hiraishi FIG.13 below)] *and a second memory operation subsequent to the first memory operation* [*e.g.,* a subsequent read operation]." EX1003, ¶288; EX1005, FIG.13:

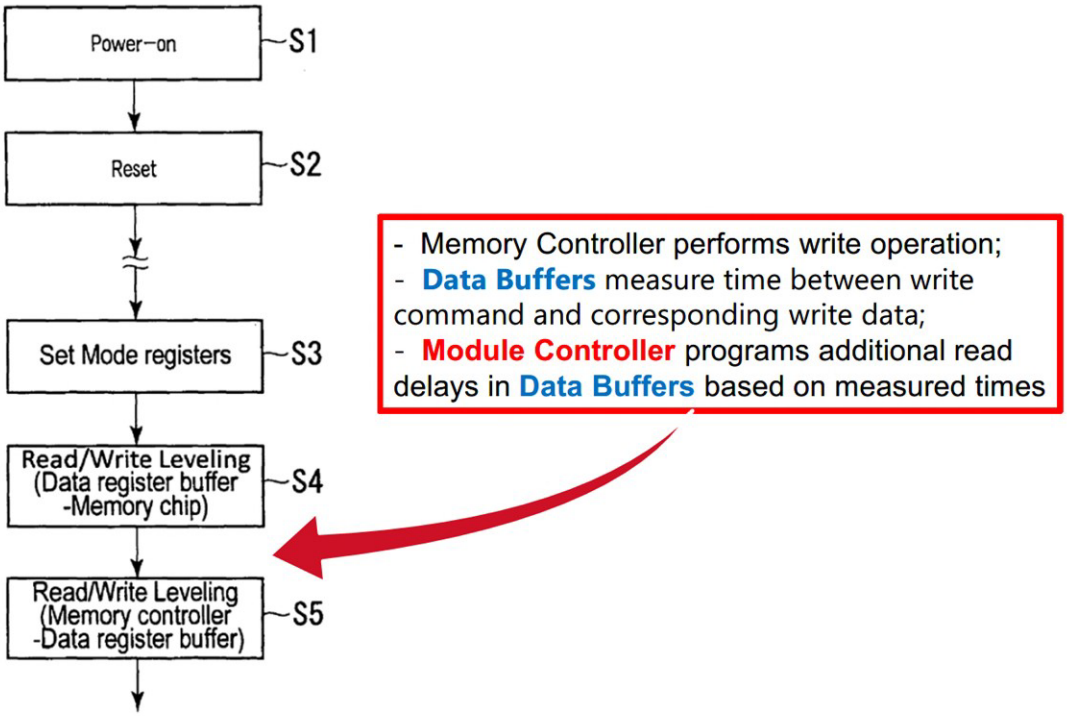


FIG.13

b) 2[b]: first and second set of command signals

In the first implementation, *supra* pp.91-93, "*the first memory operation*" is an S5 write leveling operation, and the memory controller issues commands ("*system command signals*") to the module to initiate the write leveling. EX1003, ¶290; EX1020, p.43. Since the S5 write leveling is between the memory controller and the data buffers, a POSITA would have understood that the module controller sends no-operation (NOP) commands ("*module command signals*") to the memory devices. EX1003, ¶290; EX1020, p.33.

In the second implementation, *supra* pp.93-97, the "*first memory operation*" is a write operation that is initiated after S4 leveling but before S5 leveling:

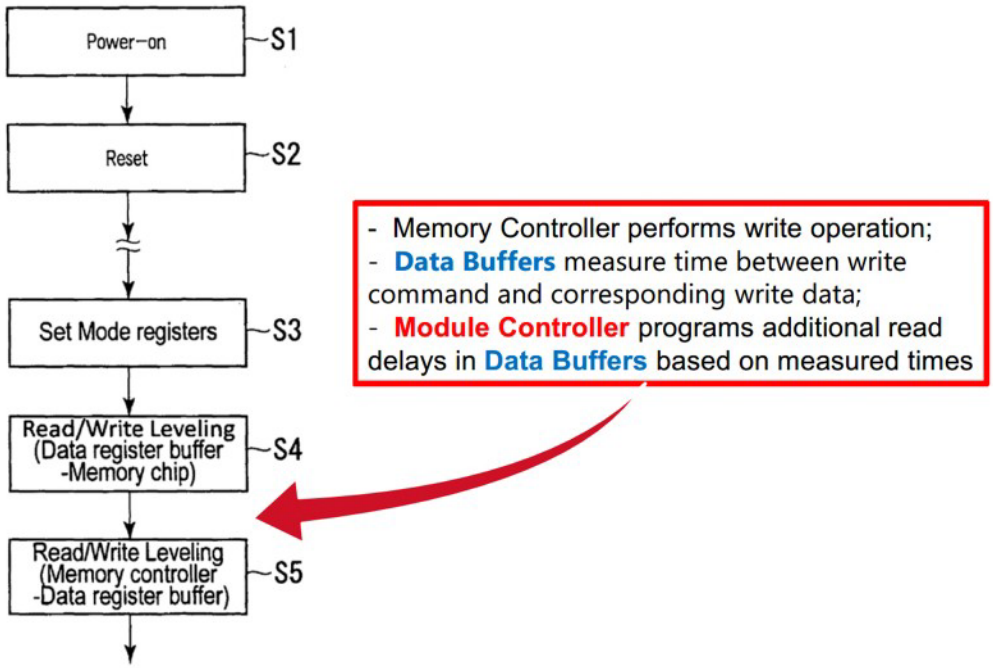


FIG.13

EX1003, ¶291; EX1005, FIG.13. During this operation, a Write command is transmitted from the memory controller to the module controller (command/address/control register buffer 400 receiving "*system command signals*") which either forwards the write command or sends no-operation commands to the memory devices ("*module command signals*"). EX1003, ¶291. After a write latency, the write DQ and DQS signals are sent from the memory controller (MCH 12) to each buffer circuit (300). *Id.* The command/address/control register buffer 400 also transmits the Write command to each buffer circuit. *Id.* Each buffer circuit calculates

the respective time interval based on the arrival timing of the DQ and DQS signals as compared to the arrival timing of the Write command signal. *Id.* In this combination, the "*second memory operation*" is a subsequent read operation, for which the memory controller transmits at least a read command ("*system command signals*") and the module controller forwards the read command to the memory devices ("*module command signals*"). *Id.*; EX1005, ¶[0124], FIG.11. Thus, "*the command signals include a first set of command signals* [e.g., write command] *for the first memory operation* [write operation after S4 but before S5 leveling] *and a second set of command signals* [e.g., read command] *for the second memory operation* [subsequent read operation]." EX1003, ¶291.

c) 2[c]: first and second set of control signals

In the first implementation, *supra* pp.91-93, the S5 write leveling is a "*first*" operation which is performed when the module control device sends module control signals to Hiraishi's data buffers to initiate the write leveling operation, and the "*second*" operation is a read operation when the module control device uses the module control signals to send the read command to the data buffers. EX1003, ¶293.

In the second implementation, *supra* pp.93-97, the "*first memory operation*" is a write operation, initiated after S4 leveling but before S5 leveling and the first set of command signals includes a write command:

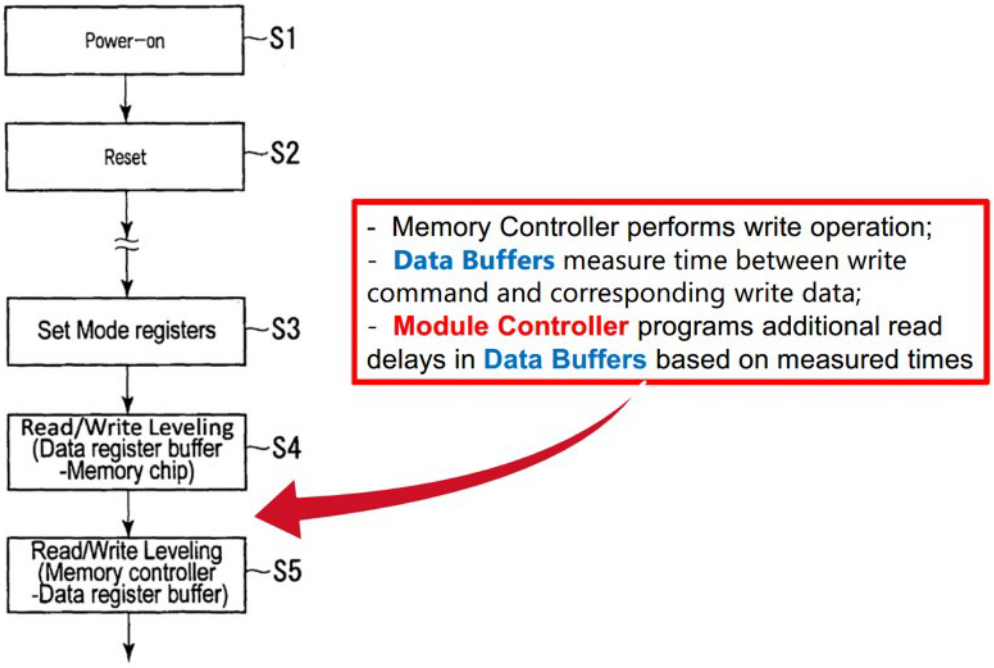


FIG.13

EX1003, ¶293; EX1005, FIG.13. The command/address/control register buffer 400 transmits the Write command to each buffer circuit as part of the control signal DRC. EX1003, ¶¶293, 277. In this combination, the "*second memory operation*" is a subsequent read operation, for which the memory controller transmits at least a read command. EX1003, ¶293. This read command is also transmitted to each buffer circuit as part of the control signal DRC. *Id.*; EX1005, ¶[0126]. Thus, "*the module control signals include a first set of module control signals* [control signal DRC

transmitting Write command] *output by the module control device* [command/address/control register buffer 400] *in response to the first set of command signals* [Write command issued after S4 but before S5 leveling] *and a second set of module control signals* [control signal DRC transmitting Read command] *output by the module control device in response to the second set of command signals* [subsequent read command]." EX1003, ¶293.

d) 2[d]: signal associated with the second memory operation

In the first implementation, *supra* pp.91-93, the S5 write leveling is a "*first*" operation, performed when the module control device sends module control signals to Hiraishi's data buffers to initiate the write leveling operation, and the "*second*" operation is a read operation when the read data signals pass through the data buffers. EX1003, ¶295.

In the second implementation, *supra* pp.93-97, the "*first set of module control signals*" comprises the control signal DRC used to transmit the Write command to data register buffers 300. EX1003, ¶296. In response to this write command, each buffer circuit calculates the respective time interval based on arrival timing of the DQ and DQS signals compared to arrival timing of the Write command signal. EX1003, ¶¶296, 277-281. The delay amount is determined by the command processing circuit, as recited in limitation 1[f], in response to this control signal. *Id.* The signal through the data path for subsequent read operations is delayed by the

determined delay amount. *Id.* Thus, in the combination, "*the at least one of the module control signals include at least one of the first set of module control signals* [the control signal DRC used to transmit the Write command to data register buffers 300]*, and wherein the signal through the data path is a signal* [DQ or DQS] *associated with the second memory operation* [subsequent read operation]." EX1003, ¶296.

5. Claims 3-12

Claims 3-12 are obvious over Ground 1 (and thus also the combination of Ground 1+Tokuhiro) for the same reasons. EX1003, ¶297.

C. Ground 3: Ground 1 or Ground 2 + Ellsberry (claims 5 and 12)

To the extent it is found that Ground 1 or 2 does not disclose or render obvious memory devices with "*a data width of 4 bits*" as recited in claims 5 and 12, those claims are rendered obvious in further view of Ellsberry (EX1007).

EX1003, ¶¶196-198, 228, 298.

Ellsberry discloses a memory module with four ranks of memories and the same distributed buffer architecture as Hiraishi to reduce load, and expressly describes modules with 8-bit wide data buffers (SWITCH ASIC, blue, with DQ[3:0] and DQ[7:4]) coupled to either 8-bit wide memory chips or pairs of 4-bit wide memory chips (green). EX1003, ¶196; EX1007, FIG.11 (pairs of 4-bit wide memories) and FIG.13 (8-bit wide memories):

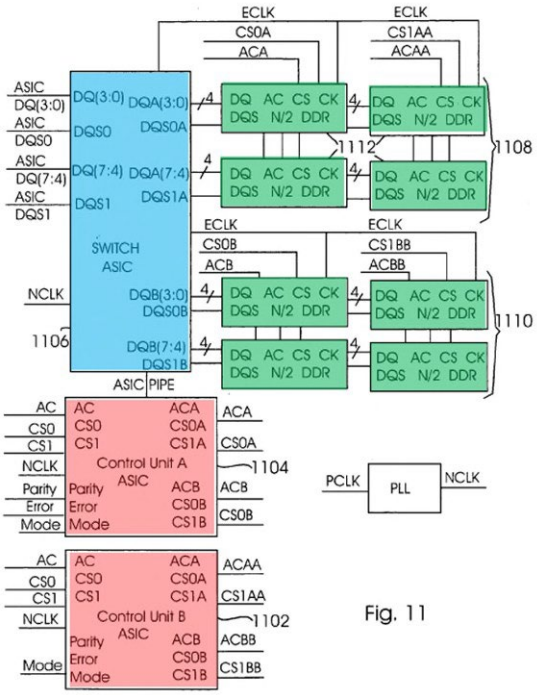


Fig. 11

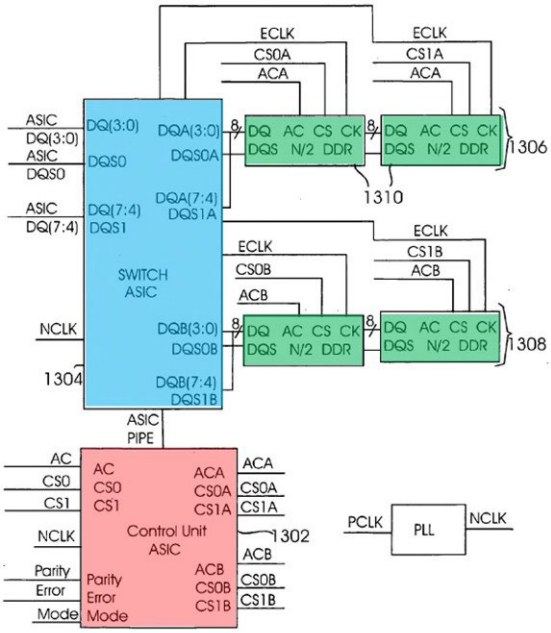


Fig. 13

EX1003, ¶196.

A POSITA would understand that Ellsberry's Figures 2, 5, and 13 correspond to an embodiment utilizing 8-bit memory devices, while Ellsberry's Figures 2, 6, and 11 correspond to another embodiment utilizing pairs of 4-bit memory devices. EX1003, ¶¶197-198; EX1007, FIGS. 2, 5-6, 11, 13. Indeed, the Board made that finding in a Final Written Decision against Netlist, EX1015, pp.77-78, which is now binding against Netlist, *MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1377-78 (Fed. Cir. 2018). Using 4-bit memory devices was one of a finite number of well-known solutions. EX1003, ¶195. Ground 3 thus renders obvious claims 5 and 12.

D. Ground 4: Ground 1 or Ground 2 + Kim (claims 6-8)

To the extent Ground 1 or Ground 2 is found not to disclose or render obvious a metastability detection circuit and/or signal adjustment circuit as claimed, claim 6

is rendered obvious in light of Grounds 1 or 2 in further view of Kim (EX1008). EX1003, ¶¶205-207, 209, 211. Both Kim and Hiraishi are directed to solving the problem of reliable communication between integrated circuits, including between Hiraishi's command/address/control register buffer 400 and data buffers 300. EX1003, ¶205; EX1008, 1:12-14, 1:21-31. To solve the identified metastability problem, Kim discloses "a metastability detection/prevention circuit 20" to be incorporated with any "main active circuit 10" in need thereof, including "a data input buffer." EX1003, ¶205; EX1008, 2:23-37.

It would have been obvious to a POSITA to combine the functionality of Kim's metastability detection circuitry with the DRC inputs in Hiraishi's data register buffers. EX1003, ¶206. A POSITA would have been motivated to make the combination to obtain more reliable communication by avoiding metastability at the input of the DRC signals, e.g., because DRC signals carry important control information and metastability can be avoided by the DLL adjusting the phase of the internal clock used by the input buffer. EX1003, ¶¶206-207; EX1005, ¶[0100]. Making the combination would have been well within the level of skill at the time and provided nothing more than expected from the prior art: detecting metastability at the DRC input and removing the metastability by adjusting the phase of the corresponding internal clock. EX1003, ¶207.

Claims 7-8 depend from claim 6, and are rendered obvious for the same reasons as stated above in Ground 1 and 2.

E. Ground 5: Ground 1 or 2 + Kim and Ellsberry (claim 8)

Claim 8 depends on claim 6, which is rendered obvious by Ground 1 or 2 in view of Kim as explained in Ground 4. To the extent it is found that Ground 4's combination does not disclose or render obvious memory devices with "*a data width of 4 bits*" as recited in claim 8, it is rendered obvious in further view of Ellsberry (EX1007) for the same reasons as discussed in Ground 3 for claims 5 and 12. EX1003, ¶211.

VII. DISCRETIONARY DENIAL IS INAPPROPRIATE

A. 35 U.S.C. § 325(d)

The Board instituted *inter partes* review of claims 1-12 of the '608 Patent in the Samsung IPR. EX1068. Petitioners move to join the Samsung IPR, using a substantively identical petition. *See* EX1067. The Board should not discretionarily deny institution under *Advanced Bionics* and §325(d) for the reasons identified in the Samsung IPR institution decision. *See* EX1068, pp.8-14.

B. 35 U.S.C. § 314(a)

1. *Fintiv*

Fintiv factors strongly favor institution. The first *Fintiv* factor favors institution because the Court granted a stay in the co-pending litigation—which is currently in force—pending PTAB resolution of IPRs related to several patents

including the '608 patent. EX1038. The second, third, and fourth *Fintiv* factors favor institution because "[t]he court has not yet rendered a scheduling order or set a trial date, and the parties have conducted discovery only with respect to the issue of venue." *Id.*, p.4. The Court characterized the case as "still at its infancy." *Id*. Further, the Board already instituted the Samsung IPR, allowing the Board to address the asserted prior art and narrow issues in the co-pending litigation. The fifth *Fintiv* factor is neutral or inapplicable because nothing in *Fintiv* suggests that the same party between proceedings weighs in favor of discretionary denial.

2. *General Plastic*

Discretionary denial under *General Plastic* is not warranted. The Board in *General Plastic* noted that "[t]here is no *per se* rule precluding the filing of follow-on petitions after the Board's denial of one or more first-filed petitions on the same patent." *General Plastic*, p.15. The Board "recognize[d] that there may be circumstances where multiple petitions by the same petitioner against the same claims of a patent should be permitted, and that such a determination is dependent on the facts at issue in the case." *Id.*, p.18.

Addressing *General Plastic* factors 1, 2, and 3, these factors should be considered together. *CODE200, UAB et al. v. Bright Data LTD.*, IPR2022-00861, Paper 18 (Aug. 23, 2022) ("*CODE200*"), p.5. Specifically, the Board should consider whether there is any evidence of "road-mapping" concerns. *Id.*; *General*

Plastic, p.17. Here, there is no evidence of "road-mapping." Specifically, there is no evidence that Petitioners modified this petition from their earlier IPR petition on the '608 patent—EX1069—based on information in the subsequent preliminary response and denial of institution and rehearing. Rather, Petitioners simply adopted the Samsung IPR petition essentially verbatim—using all the same arguments, evidence, and expert declaration—and agreed to act as an "understudy." There is no evidence that Petitioners "strategically stage[d] their prior art and arguments in multiple petitions, using [the Board's] decisions as a roadmap," a primary concern in *General Plastic. General Plastic*, p.17. Rather, this "Petition makes no changes from the instituted [Samsung] petition" and "[t]hus, the roadmapping concerns addressed in *General Plastic* . . . are not present here." *Intel Corporation v. VLSI Technology LLC*, IPR2022-00366, Paper 14 (June 8, 2022), p.11. Thus, these factors weigh against discretionary denial.

Addressing *General Plastic* factor 4, Petitioners were not aware of the critical prior art used in Samsung's '608 IPR, which this petition seeks to join, when filing its original petition. The Board denied instituting Petitioners' original IPR, finding that its primary reference Osanai did not disclose a "data path" with a "delay circuit." EX1041, pp. 17-21. Samsung's '608 petition introduced a new reference, Butt, to address this exact concern. *See, e.g.*, EX1067, pp.113-14, 39-42; EX1068, p.10, 12-13. Petitioners represent that it had no knowledge of Butt when filing its original

petition. This reference never showed up in any of Petitioners' prior art searches, and Petitioners did not disclose Butt in its invalidity contentions. Thus, this factor weighs against discretionary denial.

Addressing *General Plastic* factor 5, Petitioners were time barred from filing an IPR petition on the '608 patent after April 28, 2022 under 35 U.S.C. § 315(b). *See* EX1035. The Samsung IPR petition was not filed until April 27, 2023, and only instituted on December 12, 2023, after which a one-month window opened to join the Samsung IPR if accompanied by a motion for joinder. *See* 37 CFR § 42.122(b). Because the present petition is filed within the one-month allowed window, and Petitioners could not have joined the Samsung IPR petition earlier than this window, this factor weighs against discretionary denial.

Addressing *General Plastic* factor 6, instituting Petitioners' review would require expending minimal additional Board resources, given this petition presents the same grounds and arguments as the already instituted Samsung IPR, and Petitioners agreed to take an understudy role. Therefore, this factors weigh against discretionary denial.

Finally, *General Plastic* factor 7 "ha[s] limited relevance [here], as the Board noted that the one year statutory time period may be adjusted for a joined case under 35 U.S.C. § 316(a)(11)." *CODE200, p.*6 (internal quotation marks omitted).

Further, this case is distinguishable from *Apple Inc. v. Uniloc 2017 LLC*, IPR2020-00854 ("*Apple*"), because in *Apple*, the petitioner's underlying argument was that "*General Plastic* does not apply" to serial petitions where the petitioner seeks to join as an understudy, and that "a joinder petition 'effectively neutralizes' a *General Plastic* analysis." *Apple*, Paper 8 (June 22, 2020), p.4. In *Apple*, the petitioner failed to address a majority of the *General Plastic* factors, claiming they were simply irrelevant or inapplicable. *Id.*, pp.4-5. In its decision, the Court repeatedly stated that it was not persuaded by petitioner's arguments that that the *General Plastic* factors were not applicable or irrelevant. *Apple*, Paper 9 (October 28, 2020). Here, however, Petitioners do not argue that *General Plastic* does not apply, and alternatively applies each factor.

Additionally, as highlighted by the Board in *Google LLC v. Express Mobile Inc.*, IPR2022-00791, Paper 15 (October 7, 2022), a "[p]etitioner's representation about its lack of knowledge of the prior art at issue in [its] [serial] IPR" when filing its first petition is sufficient to distinguish a case from *Apple*; because in *Apple*, the petitioner "failed to set forth facts … concerning its knowledge, at the time it filed the first petition, of the prior asserted in the [second petition]." *Id,* pp.7-8 (internal quotation marks omitted). The petitioner in *Apple* completely dodged this issue, simply stating "these factors are inapplicable." *Apple*, Paper 8, p.5. Because

Petitioners represent that it was not aware of the relevant prior art—Butt—when filing its first petition, this further distinguishes the present case from *Apple*.

On balance, these factors weigh against discretionary denial, and any prejudice to Netlist is minimal. Petitioners simply seek to join an already-instituted IPR, using a substantively identical petition, and taking on an "understudy" role. *See also General Plastic*, p.17 ("[The Board's] intent in formulating these factors was to take undue inequities and prejudices to Patent Owner into account.").

VIII. CONCLUSION

Petitioners respectfully request that Trial be instituted and claims 1-12 be canceled as unpatentable.

Dated: January 10, 2024

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,948 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

Dated: January 10, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), I hereby certify that on January 10, 2024, a true and correct copy of the foregoing IPR petition including all attachments, appendices and exhibits, has been served in its entirety by FedEx Express on the following counsel of record for patent owner of 10,268,608 at the correspondence address of record:

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A courtesy copy of this Motion was also served upon litigation counsel for Patent Owner via email, as follows:

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