IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00237
U.S. Patent No. 10,268,608

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,268,608

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PETITIONERS' EXHIBIT LIST

Ex. No.	Brief Description
1001	U.S. Patent No. 10,268,608
1002	File History of U.S. Patent No. 10,268,608
1003	Declaration of Dr. Don Alpert
1004	Dr. Don Alpert CV
1005	U.S. Patent Application No. 2010/0312925 A1 to Osanai et al. ("Osanai")
1006	U.S. Patent No. 8,020,022 to Tokuhiro ("Tokuhiro")
1007	U.S. Patent No. 8,713,379 to Takefman et al. ("Takefman")
1008	U.S. Patent No. 9,824,035 to Lee et al.
1009	RESERVED
1010	File History of U.S. Patent No. 9,128,632
1011	U.S. Patent No. 8,565,033 to Manohararajah et al. ("Manohararajah")
1012	Excerpt of DDR4 SDRAM Load Reduced DIMM Specification, JEDEC Standard No. 21C, Rev. 1.00 (August 2015)
1013	Excerpt of DDR3 SDRAM, JEDEC Standard, JESD79-3C (November 2008)
1014	Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.,* Case No. 6:21-cv-00431 (W.D. Tex.)
1015	Graf, Rudolph F., Modern Dictionary of Electronics, 7th ed. (1999), p. 804
1016	Filed Stipulations of Petitioners for U.S. Patent No. 10,268,608 in *Netlist, Inc. v. Micron Technology, Inc. et al., Case No. 6:21-cv-00431 (W.D. Tex.)*
1017	Scheduling Order in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)

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1018	Proof of Service of Summons and Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)
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1020	Micron's Proposed Claim Construction in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)

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I. Introduction

Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioners") request *inter partes* review (IPR) of claims 1–5 (the "challenged claims") of U.S. Patent No. 10,268,608 (the "'608 patent"

The '608 patent and its parent applications are directed toward memory modules that include multiple memory chips. All were allowed over the prior art because of one feature—inclusion of buffer delay circuit on a memory module that (i) obtains timing information from received signals for one memory operation and (ii) uses that timing information to determine transmission timing for its connected memory chips for a second operation. The patents recite this feature to overcome a problem of having to balance the "length of the wires to" multiple memory devices "to eliminate variation of the timing of the control signals" (e.g., relating to read/write operations). *See, e.g.,* Ex. 1001, 2:20-25. The patents narrowly overcame prior art that included buffers as part of a memory controller that "implements delay for transmitting signals to the memory devices." *See infra*, Section III.D.

The '608 patent's claims 1-2 collectively recite features that most closely track the supposed novel feature that overcame the prior art. Claim 1 defines "a delay circuit [in a buffer] configured to delay a signal through the data path by an

amount determined by the command processing circuit in response to at least one of the module control signals." Ex. 1001, claim 1. Claim 2 further requires determining this amount requires using module control signals from *a first* operation. *Id.*, claim 2. Claims 1-2 further recite use of this delay amount to "to delay a signal through a data path" for the *second*, subsequent operation. *Id.*, claims 1 and 2. Together, claims 1-2 recite limitations that most closely track the limitations that the notice of allowance stated the cited prior art did not teach: "*obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information*." Ex. 1002, p. 206.

Tokuhiro, however, taught this supposed novel feature almost four years earlier. More specifically, Tokuhiro recognized that propagation delays could be different for varying locations of memory devices. *See infra*, § V.A.2. Tokuhiro disclosed solving this problem by use of "variable delay" circuits, a "first" of which obtains timing information from a write operation, and a "second" of which uses that timing information to determine timing of read operations. *Id.* Tokuhiro, in combination with the buffers disclosed in Osanai, renders the supposed novel features of claim 2 as well as other features in claims 1–5 of the '608 patent obvious.

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The remaining '608 patent claim limitations encompass well-known components that have been included in commonplace memory devices before the critical time. Osanai evidences these base components and features. Without the limitations emphasized in the notice of allowance that cover the supposed novel feature, claim 1 fails to overcome what the examiner acknowledged the prior art taught. Ground 1 demonstrates this by showing Osanai anticipates claims 1 and 4. Likewise, Ground 3 demonstrates this by showing that Takefman also renders claimed components obvious to the extent they are not found expressly disclosed in Osanai. Both Grounds 1 and 3 show that the remaining claimed components were well-known components and commonplace in memory devices before the critical time.

None of these references were considered during prosecution. For the foregoing reasons, the challenged claims are unpatentable and should be cancelled.

II. Requirements for *Inter Partes* Review

This Petition complies with all statutory requirements, as well as 37 C.F.R. §§ 42.104-105 and 42.15, and should be accorded a filing date pursuant to 37 C.F.R. § 42.106. The required fee is being paid electronically through PTAB E2E.

A. Petitioners' Certification

As required by 37 C.F.R. § 42.104(a), Petitioners certify that the '608 patent "is available for *inter partes* review and that the Petitioners are not barred or

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estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition." Petitioners certify that this Petition is filed within one year of the date of service of the complaint—June 15, 2021. No Petitioner, nor any party in privity with Petitioner, has filed a civil action challenging the validity of any claim of this patent. Accordingly, Petitioners therefore certify that the '608 patent is available for *inter partes* review.

B. Identification of Challenge

Under 37 C.F.R. §§ 42.104(b) and 42.22, Petitioners request that the Board institute this IPR on the '608 patent's claims 1–5 and cancel those claims as unpatentable for obviousness under pre-AIA 35 U.S.C. §§ 102 and 103 on the following grounds:

Ground	Claims	Basis for Unpatentability
1	1 and 4	Anticipated by Osanai (Ex. 1005)
2	1–5	Obvious over Osanai (Ex. 1005) in view of Tokuhiro (Ex. 1006)
3	1–5	Obvious over Osanai (Ex. 1005) in view of Tokuhiro (Ex. 1006), in further view of Takefman

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III. U.S. Patent No. 10,268,608 (Ex. 1001)

A. Earliest Effective Filing Date

The ’608 patent claims earliest priority to provisional application No. 61/676,833 filed on July 27, 2012. For purposes of this Petition, Petitioners assume that the challenged claims are entitled to an effective filing date of July 27, 2012.

B. Level of Ordinary Skill in the Art

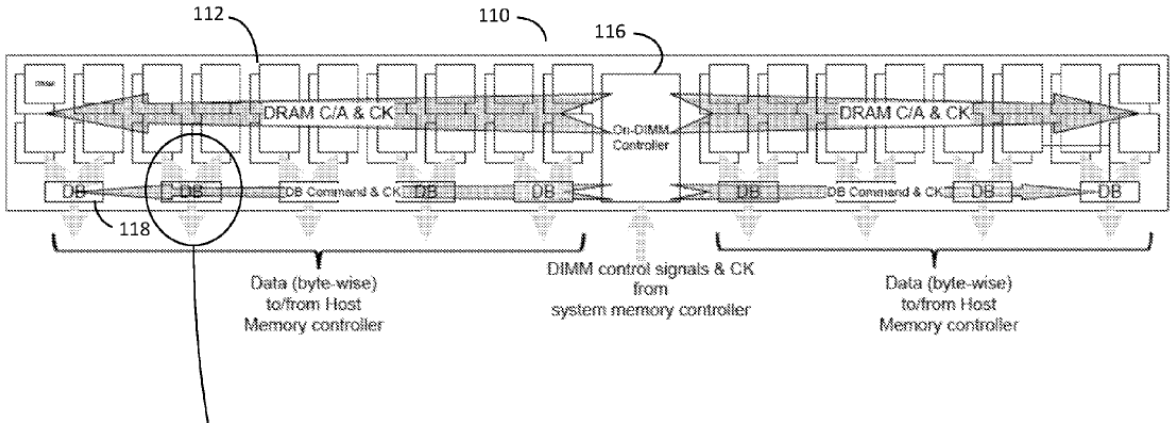
As of July 2012, a person of ordinary skill in the art (“POSITA”) would have been a person with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor’s degree in such engineering disciplines and at least three years working in the field. Ex. 1003, ¶ 42. Such a person would have been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers. Ex. 1003, ¶ 42. Standards for DRAM and SDRAM devices would have included, for example, DDR3 standards. *See*, *e.g.,* Ex. 1013. The references cited in this Petition and the experience of Dr. Donald Alpert as described in his expert declaration (Ex. 1003) reflect this level of skill in the art.

C. Technology Overview

The ’608 patent relates to computer memory modules. Ex. 1001, 1:37–39. It discloses a memory module that includes multiple memory devices 112, data buffers

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118, and a module control device 116. Ex. 1001, Abstract. Figure 2C depicts these components:



Ex. 1001, Fig. 2C.

As shown above, module control device 116 is located at the center of memory module 110. *See id.*; Ex. 1003, ¶ 46. Several memory devices 112 share a respective data buffer 118. Ex. 1001, 8:36–39; Ex. 1003, ¶ 46. Both memory devices 112 and their respective data buffers 118 are distributed lengthwise across the memory module. *See* Ex. 1001, Fig. 2C; Ex. 1003, ¶ 46.

Memory module 110 has a memory bus to receive commands from a memory controller (not shown). Ex. 1001, Abstract; Ex. 1003, ¶ 47. This bus includes both control/address (C/A) and data/strobe signal lines that connect the memory controller to the module control device 116 and to each memory device 112 via its shared data buffer 118, respectively. Ex. 1001, 4:29–44. To command the memory module 110, the memory controller issues command signals across C/A signal lines.

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As one command signal, C/A signals are sent to the module control device 116 that instruct the memory module to perform operations, such as read or write operations. *Id.*, 3:29–38. For another, the memory controller sends and receives data/strobe signals to/from the memory devices 112 via the data buffers 118 to convey data (and timing information) for the read and write commands. *Id.*, 7:63–8:3; *see also id.*, 10:31–11:7; Ex. 1003, ¶ 47.

Figure 2C, shown above, illustrates that data buffers 118 and their associated memory devices 112 are distributed at varying distances from the module control device 116. These varying distances result in "unbalanced wire lengths" and varying propagation delays—stated otherwise, control signals may take longer to reach memory devices that are farther away. Ex. 1001, 2:28–32; Ex. 1003, ¶ 48. Conventional systems used "leveling mechanisms for write and/or read operations" in the memory controllers (not shown) to compensate for such propagation delays. Ex. 1001, 2:28–32; Ex. 1003, ¶ 48. The '608 patent alleges, however, that these leveling mechanisms cannot accurately ensure "proper timing of the control and/or data signals received and/or transmitted by the memory modules." *Id.*, 2:32–36; Ex. 1003, ¶ 48.

To solve this problem, the '608 patent discloses use of a signal alignment circuit in each data buffer to determine transmission timing. *See id.*, 10:7–21, 15:17–26; *see also* Ex. 1003, ¶ 49. Transmission timing is determined based on time

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interval information obtained from a prior write operation. Ex. 1001, 10:11–21; *see id.*, 10:7–11, 15:17–26; Ex. 1003, ¶ 49. Using the obtained timing interval, the signal alignment circuit calculates the time interval for subsequent read operations. Ex. 1001, 10:11–21; *see id.*, 10:7–11, 15:17–26; Ex. 1003, ¶ 49.

D. Relevant Prosecution History

An examination of the prosecution for the parent application that resulted in U.S. Patent No. 9,128,632 (the "'632 patent application") illustrates why the Examiner allowed the challenged claims. The '632 patent's initial claims were rejected as anticipated by U.S. Patent No. 8,565,033 to Manohararajah ("Manohararajah"). Ex. 1010, 100–108; Ex. 1011. The applicant responded with arguments and claim amendments to overcome that rejection. Ex. 1010, 134–35.

More specifically, the applicant first argued that Manohararajah disclosed buffer circuits as part of the memory controller instead of the claimed memory module as amended. *Id.*, 139–140. Specifically, the claims were amended to recite that each data buffer both:

- "determine[s] a respective time interval based on signals received by the each respective buffer circuit during a memory *write operation*," and

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- "time transmission of a respective set of *read data signals* received from the respective group of memory devices in accordance with the time interval and a read latency parameter . . . ."

Id., 134 (emphasis added). Manohararajah, the applicant argued, was different and only disclosed delaying "DQ/DQS" control signals for optimal phase alignment. *Id.*, 140–141 ("[n]owhere in Manohararajah it is described the transmission of read data signal from each respective buffer is timed in accordance with a time interval determined based signals [sic] received by the each respective buffer").

The Examiner allowed the claims in the '632 patent application, stating:

> [The p]rior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to memory devices of each module.
>
> [T]he prior art does not fairly teach or suggest … a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to ***determine a respective time interval based on signals received by each buffer circuit during an operation to configure the timing of transmission of signals to the memory devices,*** wherein the buffers are located in such a way that they receive

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> control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read/ write signals to their respective groups of memory devices as claimed in the independent claims.

Ex. 1010, 1078 (emphasis added). Stated otherwise, the prior art used buffered memory modules to delay signal transmissions, but there was no finding of buffers that determine a time interval *from a write operation* and use that information to determine a delay for *a read operation* to time accordingly. Ex. 1010, pp. 100–108, 134–143, 1078.

The Examiner made a similar statement in allowing the challenged claims. Ex. 1002, pp. 205–206; Ex 1003, ¶¶ 52–55. Notably, the Examiner acknowledged that the prior art taught most components in the challenged claims—namely, "memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implements delays for transmitting signals to the memory devices of each module." *Id.* The Examiner also focused the reason for allowance on how each buffer includes logic that obtains timing information based on signals received by the buffers during a write (second) memory operation prior to a read (first) memory operation:

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> [T]he prior art does not fairly teach or suggest … a memory module system with a plurality of buffers…including logic that… is configured to ***obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information*** ....

Ex. 1002, 206 (emphasis added); *see id.*, 127–128. These limitations, however, do not appear[1] in the '608 patent's claims. *See* Ex. 1008, Claim 1. At best, this supposedly novel feature appears in claim 2 that further requires both (i) a "*first memory operation*," a subsequent "*second memory operation*," and (ii) the delayed "*signal*" is "*associated with the second memory operation*" and delayed by an amount determined using signals belonging to the "*first memory operation*." Ex. 1003, ¶ 56, *see* Ex. 1001, 19:36–20:4. As discussed herein, however, this supposedly novel feature was taught by Tokuhiro years prior. Ex. 1003, ¶ 56; *See, e.g.*, Ex. 1006, Abstract.

IV. Claim Construction

The Board construes claims under the same standard used in civil actions in federal district court. The district court for the related litigations has not yet

[1] These limitations are from related U.S. Patent No. 9,824,035. Ex. 1008, Claim 1.

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construed the claim terms. The parties' proposed constructions from the related litigations are set forth in Exs. 1019-1020. As stated therein, Petitioners are asserting that certain terms are subject to means-plus-function treatment under 35 U.S.C. §112, ¶6, and are indefinite for failure to provide structural support in the specification. Petitioners are not asking the Board to find any claim indefinite for the purposes of this Petition, and instead use Patent Owner's proposed constructions and interpretation herein. The Board and Federal Circuit have approved of this procedure in several matters. See, e.g., *Micron Technology, Inc. et al. v. Unification Technologies LLC*, IPR2021-00344, Paper 9 at 10-11 (P.T.A.B. July 9, 2021); *Spherix Inc. v. Matal*, 703 F. App'x 982, 983 (Fed. Cir. 2017) (approving petitioner's proposal of patent owner's claim interpretations); *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12 (P.T.A.B. Nov. 10, 2020) ("Petitioner's alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review."); *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp*., 948 F.3d 1342, 1355 (Fed. Cir. 2020) (indefinite claims may also be found invalid as anticipated or obvious); *Vibrant Media v. Gen. Elec. Co*., No. IPR2013-00172, Paper 50, 10 (P.T.A.B. July 28, 2014) ("an indefiniteness determination in this proceeding would not have prevented us from deciding whether the claims would have been obvious over the cited prior art.").

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V. Detailed Discussion of the Grounds for Unpatentability

The challenged claims are unpatentable based on three different grounds. Ground 1 establishes that claims 1 and 4 are anticipated by Osanai. Ground 2 establishes that claims 1–5 are obvious over Osanai in view of Tokuhiro. Ground 3 establishes that claims 1–5 are obvious over Osanai in view of Tokuhiro, in further view of Takefman.

A. Prior Art Overviews

1. Osanai (Ex. 1005)

U.S. Patent Application Publication No. 2010/0312925 to Osanai ("Osanai") is titled "Load Reduced Memory Module." Osanai published on December 9, 2010 and qualifies as prior art under pre-AIA 35 U.S.C. § 102(b).

Osanai discloses a memory module 100 that mirrors LRDIMM described in the Joint Electron Device Engineering Council (JEDEC) standards for Double Data Rate 4 (DDR4) memory, which Netlist alleges infringes the '608 patent claims. Ex. 1003, ¶ 59; Ex. 1012, p. 2, Ex. 1014, ¶¶ 110, *see id.*, 111–125. Such a memory module 100 is depicted in Osanai's Figure 1 shown below as including multiple memory chips 200, data buffers 300, and a command/address/control register buffer 400:

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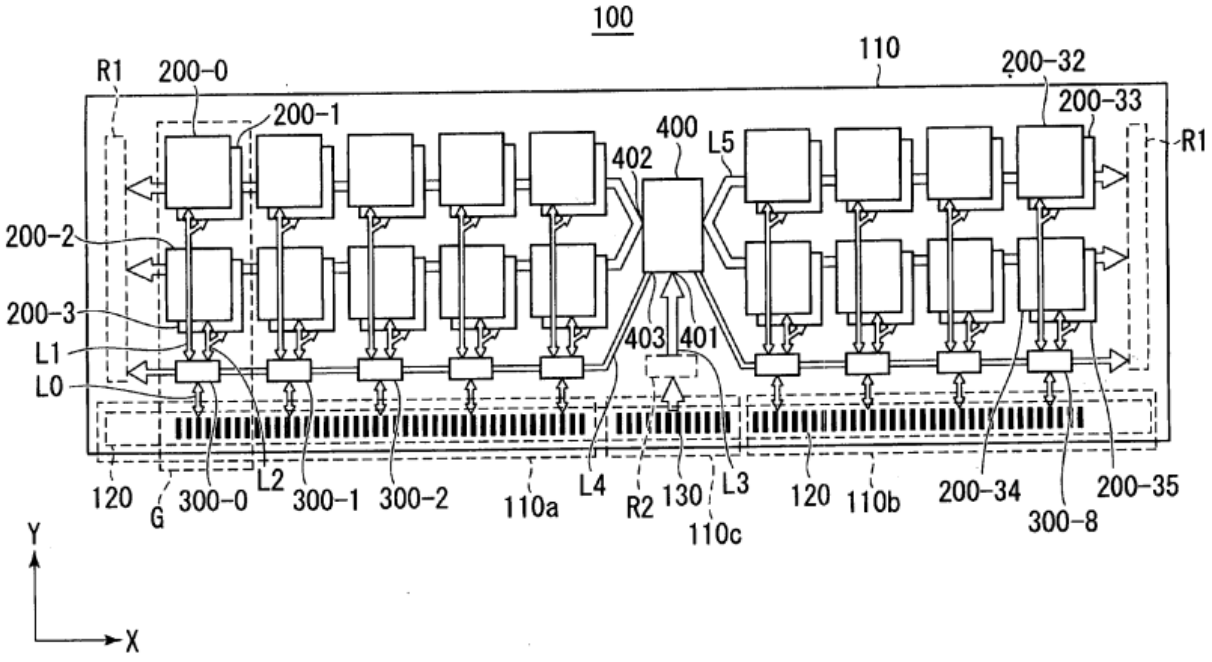


FIG.1

Ex. 1005, Fig. 1, [0051]–[0052]; Ex. 1003, ¶ 58. Command/address/control register buffer 400 is located at the center of the memory module 100. *See* Ex. 1005, Fig. 1. Memory chips 200 are organized into sets that share a buffer 300. *See* Ex. 1005, Fig. 1, [0051]–[0052]; Ex. 1003, ¶ 58; *see also* Ex. 1005, [0057]–[0058]. The same chips are also organized into ranks, which include one chip from each set. *Id.*, [0111]; Ex. 1003, ¶ 58. Both memory chips 200 and their respective buffers 300 are distributed lengthwise across the memory module. *See* Ex. 1005, Fig. 1, [0052]–[0054]; Ex. 1003, ¶ 58.

Memory module 100 receives commands from memory controller 12, shown in Figure 3 below:

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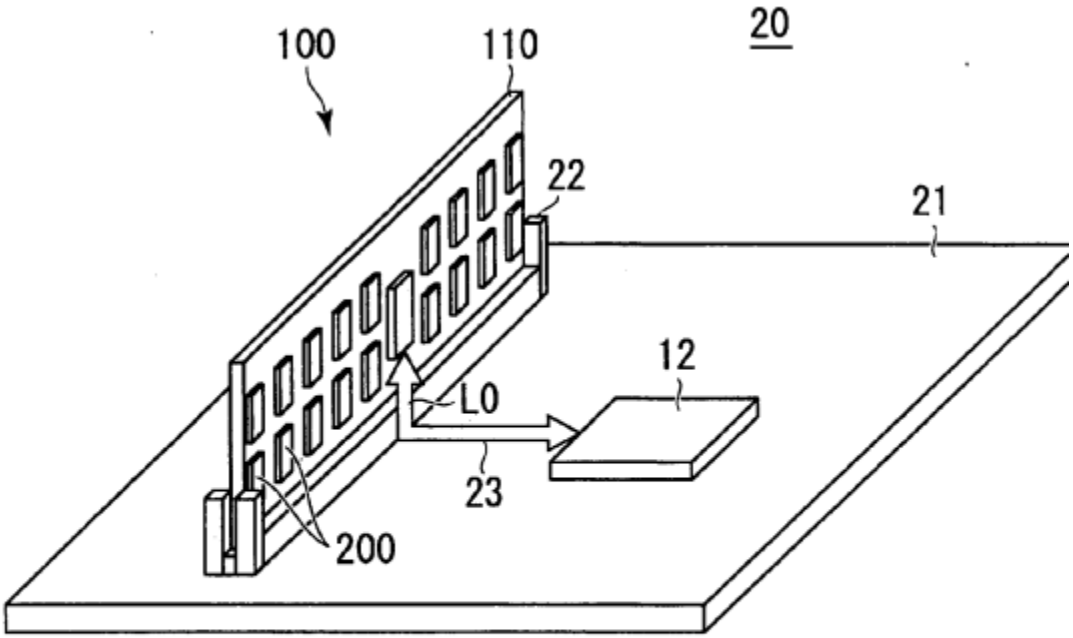


FIG.3

Ex. 1005, Fig. 3, [0074]–[0075]; Ex. 1003, ¶ 60. To do so, memory module 100 receives commands across control/address (C/A) signal lines that connect the memory controller 12 and the command/address/control register buffer 400 (Ex. 1005, Fig. 3 (line 23), [0075],). A POSITA would have understood that these commands are sent over Osanai's line 23, which connects to data lines L0 and command/address/control line L3. Ex. 1005, [0075]; Ex. 1003, ¶ 60. Memory controller 12 issues command signals across C/A signal lines to the command/address/control register buffer 400. Ex. 1005, [0054]–[0055]. Register

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buffer 400 then sends C/A signals to instruct the memory chips 200 to perform operations, such as read or write operations. *Id.* Memory controller 12 also sends and receives data/strobe signals to/from the memory chips 200 via the buffers 300 used to convey data for the read and write commands. Ex. 1005, [0054]–[0055].

Osanai recognized that, because these memory chips 200 and their respective buffers 300 are located at different distances from register buffer 400, signals arrive at memory chips 200 later when those chips are located farther away. *See id.*, [0146]–[0149]; Ex. 1003, ¶ 61. To compensate for this propagation delay, Osanai discloses both read and write leveling circuitry 322 and 323 located in the data register control circuit 320 inside data buffer 300. *Id.*, Fig. 5, [0096]; *see also id*., [0146]–[0164], Figs. 14A–17. These read and write leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a signal." *Id.* [0146]. These techniques make timing adjustments so that signals between "the memory chips 200 and the data register buffer 300" are sent at the appropriate time. Ex. 1005, [0110]; *see also id*., [0096], [0146].

2. Tokuhiro (Ex. 1006)

U.S Patent No. 8,020,022 to Tokuhiro ("Tokuhiro") is titled "Delay time control of memory controller." Tokuhiro was filed on September 12, 2008 and qualifies as prior art under pre-AIA 35 U.S.C. § 102(e).

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Tokuhiro relates to computer memory and discloses a timing "technique for controlling read/write operations for a plurality of memories …." Ex. 1006, 1:15–20. Tokuhiro recognized that memory modules designed according to JEDEC standards have SDRAMs placed in a "lengthwise direction" away from the memory controller, resulting in differing propagation delays where each memory will not receive the clock signal at the same time. *Id.* 1:63–2:1 ("Thus, in the DDR3 memory interface, because the clock signal line for the clock signal CK is wired to the plurality of SDRAMs 92-1 to 92-*n* through the daisy chain connection and a propagation delay is generated, the clock signal CK output from the memory controller 90 cannot reach all the SDRAMs 92-1 to 92-*n* at the same time."); Ex. 1003, ¶ 63; *see also* Ex. 1006, 2:1–23. Notably, Tokuhiro and the '608 patent describe the same problem. *Compare* Ex. 1006, 1:63–2:1 *with* Ex. 1001, 2:28–36; Ex. 1003, ¶ 64.

Both Tokuhiro and the '608 patent propose the same solution, as well. First, Tokuhiro recognizes that the JEDEC standard specifies a "write leveling function" where variable delay circuits are used to sample the clock signal from the memory controller output during write operations "and adjusting (compensating) a delay time of the data strobe signal." Ex. 1006, 2:10-23; Ex. 1003, ¶ 64. Tokuhiro also recognizes, however, that the JEDEC standard does not provide for a corresponding delay compensation for read operations. Ex. 1006, 2:54-59 ("compensations of the

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signal arrival time in read operations are not provided with the JEDEC standards"). Tokuhiro then proposes a solution of calculating a delay time for read operations based on timing information obtained from prior write operations. Ex. 1006, Abstract ("For each of the plurality of memories, a first variable delay unit delaying, in the write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time."), 15:14–23, 15:54–58; Ex. 1003, ¶ 65. The '608 patent calculates its read operation delay the same way. *See* Ex. 1001, 4:14–19 ("[t]his time interval [determined during the write operation] is used during a subsequent read operation to time transmission of read data to the memory controller …."). Accordingly, both Tokuhiro and the '608 patent describe the same solution—the supposed inventive concept that the Examiner focused on in the notice of allowance. *See supra,* Section III.D.

Tokuhiro and the '608 patent thus describe the same propagation delay problem caused by memory chips being located at different distances lengthwise across a memory module. Ex. 1003, ¶ 66. Both propose the same solution: for each memory, calculate the delay for the read operation using the delay determined during a write operation. *Id.* The primary difference between Tokuhiro and the '608 patent is that Tokuhiro was filed years earlier. *Id.*

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3. Takefman (Ex. 1007)

U.S. Patent No. 8,713,379 to Takefman ("Takefman") is titled "System and Method of Interfacing Co-processors and Input/Output Devices via a Main Memory System." Takefman was filed on November 22, 2011 and qualifies as prior art under pre-AIA 35 U.S.C. § 102(e).

Takefman discloses a TeraDIMM architecture that includes DRAM 302, "data buffer devices" (called Bolt devices) 303, and a Rush 301 control circuitry, shown in Figure 3 below:

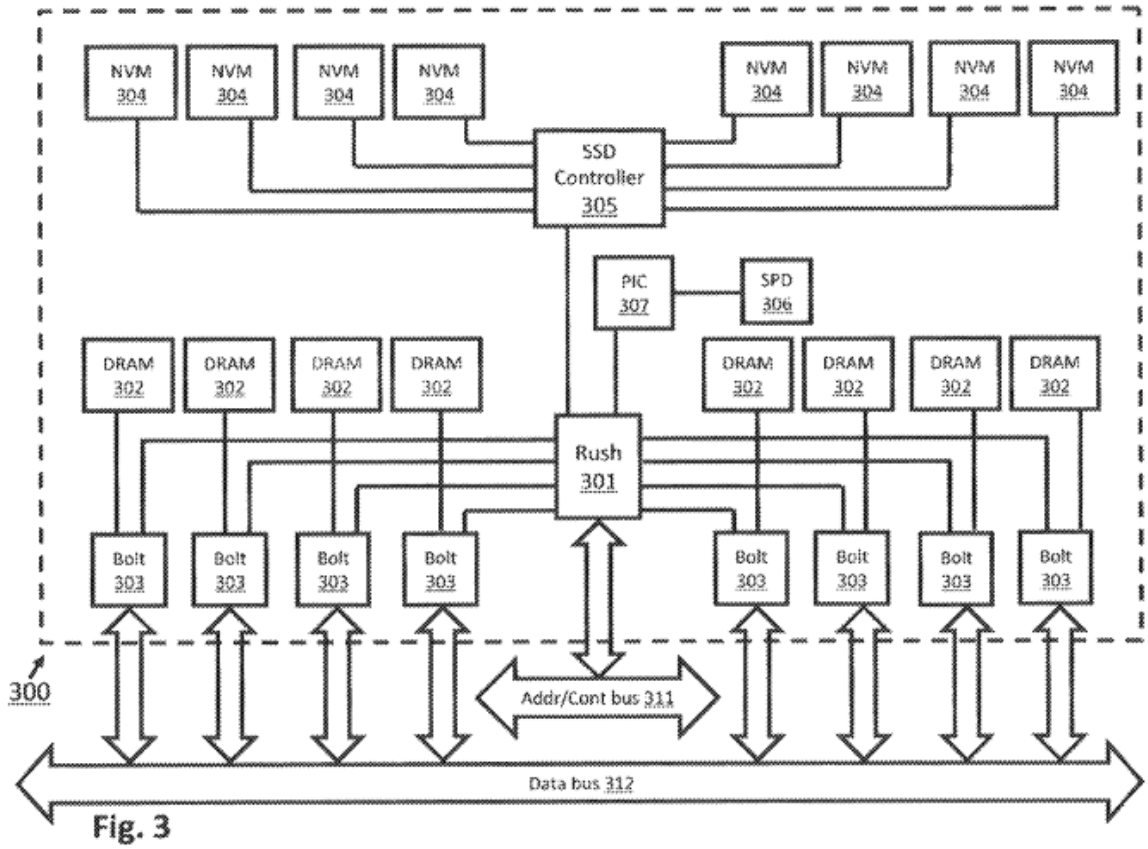


Fig. 3

Ex. 1007, Fig. 3; 5:53–63; Ex. 1003, ¶ 68. As shown above, the Rush 301 control circuitry is located centrally to the DRAM 302 of the memory module 300. *See id.*,

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Fig. 3. DRAM 302 can be organized into groups called ranks. *See id.*, 5:2–10. Each DRAM 302 also connects to a corresponding Bolt device 303. Ex. 1007, Fig. 3; 5:53–63. Both DRAM and their respective Bolt devices are distributed lengthwise across TeraDIMM 300. Ex. 1007, Fig. 3; 5:53–63.

"Because of the difference in the distances between the Bolt devices 303 and the Rush 301 and the Bolt devices 303 and the DRAM devices 302, the TeraDIMM may arrange its launch time" so that "its data arrives at an appropriate time." Ex. 1007, 6:17–20. To do so, Rush 301 includes per-lane delay compensation circuits that provide "programmable launch times and lane de-skew." Ex. 1007, 6:14–17. Stated otherwise, these compensation circuits delay signal transmission so that signals arrive at the appropriate time. Ex. 1003, ¶ 69.

B. Ground 1: Osanai Anticipates Claims 1 and 4

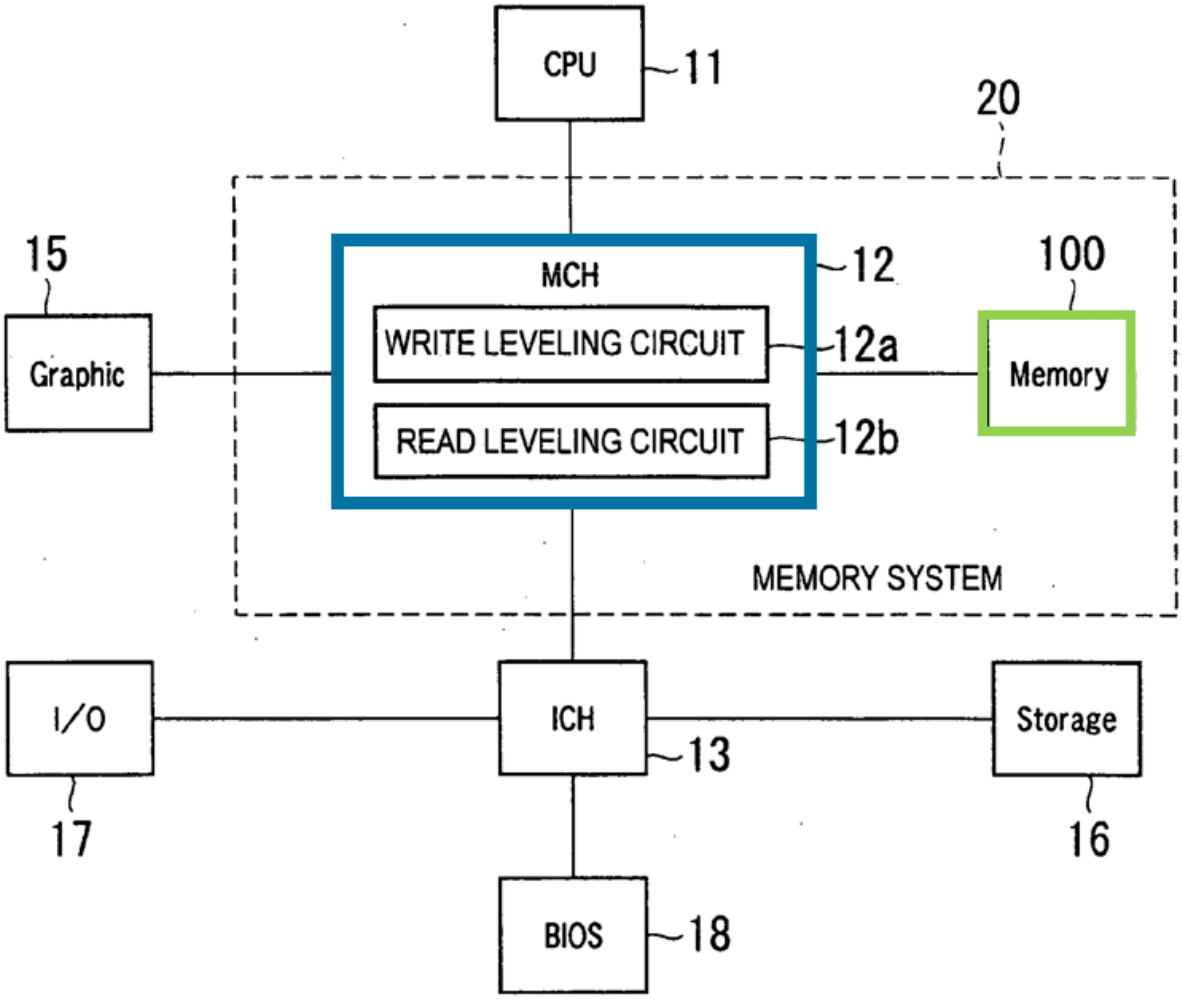
1. Claim 1

a. Preamble

To the extent the preamble is limiting, Osanai discloses this limitation.

First, Osanai discloses "[*a*] *memory module operable to communicate with a memory controller via a memory bus.*" Osanai discloses a memory module 100 that operates in a memory system 20 with a memory control hub (or MCH) 12. Ex. 1005, [0069–71], Fig. 2. Figure 2 of Osanai illustrates that this memory module 100 is connected to memory control hub 12 (a "*memory controller*"), shown below:

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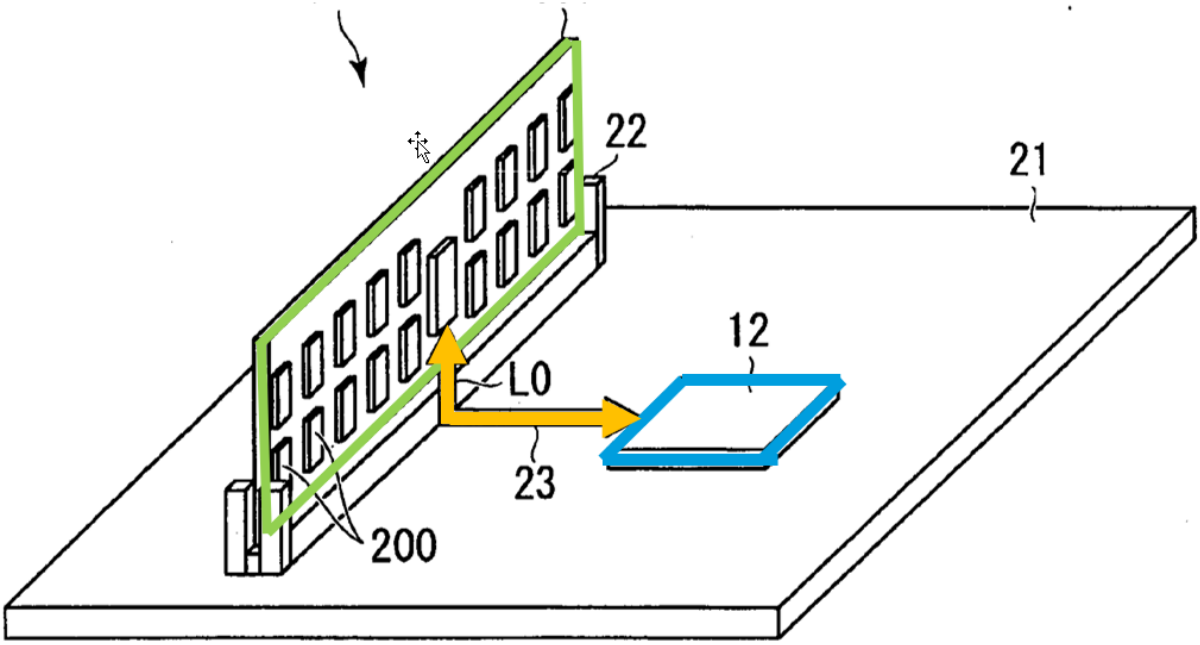


Ex. 1005, Fig. 2 (annotated); Ex. 1003, ¶ 75. Memory control hub 12 "functions as a memory controller for the memory module" (Ex. 1005, [0071]) and meets the '608 patent's broad description of a memory controller. *See* Ex. 1001, 4:46–49 ("[A] memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices").

Memory module 100 and control hub 12 communicate using communication line 23, which is part of a "*bus*." Ex. 1003, ¶¶ 76–78. As Dr. Alpert explains, a

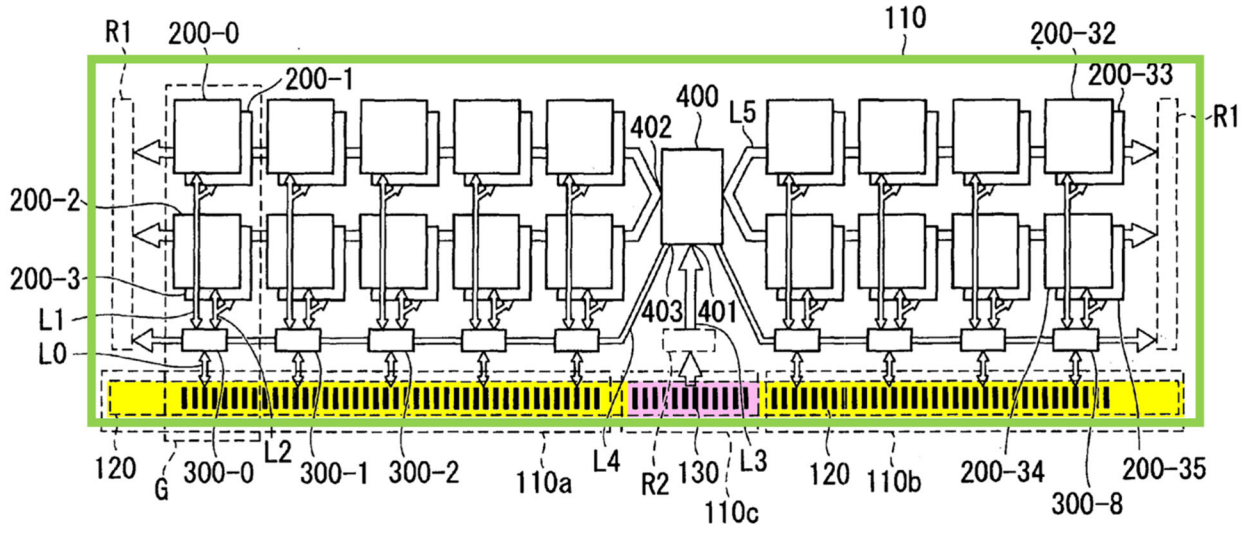
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POSITA would have understood that Osanai's line 23 connects to data lines L0 and command/address/control line L3. Ex. 1003, ¶ 76; Ex. 1005, [0075]. First, those components communicate over line 23:



Ex. 1005, Fig. 3, [0075] ("On a signal path between the memory controller 12 and the memory chips 200 [of memory module 100], there exists a line 23 formed on the motherboard 21 and the data line L0 and the command/address/control line L3 formed on the module [PCB] 110."). Second, memory module 100 communicates with the memory controller using data connectors 120 (shown in yellow) and command/address/control connectors 130 (shown in pink), shown in annotated Figure 1 below:

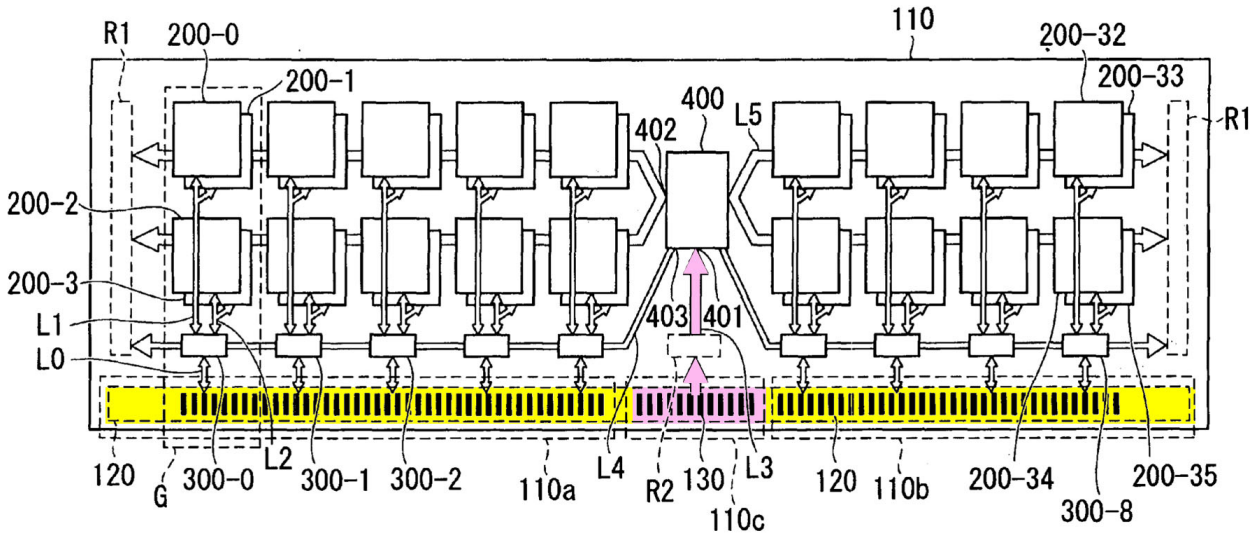
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Ex. 1005, Fig. 1, [0054]–[0055]; Ex. 1003, ¶ 77. To communicate, memory module 12 and controller 100 use line 23 via data connectors 120 and command/address/control connectors 130. Ex. 1003, ¶ 78; *see* Ex. 1005, [0126]. As Dr. Alpert explains, a POSITA would have understood that L0 and L3 lines and communication line 23, collectively, are a "*memory bus*." Ex. 1003, ¶ 78; *see* Ex. 1005, [0054]–[0055], [0126], Figs. 1 and 2C. The '608 patent refers to a "*memory bus*" broadly. Ex. 1001, 4:49–53 ("[A] memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller"). Accordingly, Osanai discloses a "*memory module* [100] *operable to communicate with a memory controller* [12] *via a memory bus*." Ex. 1003, ¶ 78.

Osanai further discloses a "*memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe*

signal lines." Osanai's Figure 1, as explained above, depicts data connectors 120 (shown in yellow) and command/address/control connectors 130 (shown in pink):



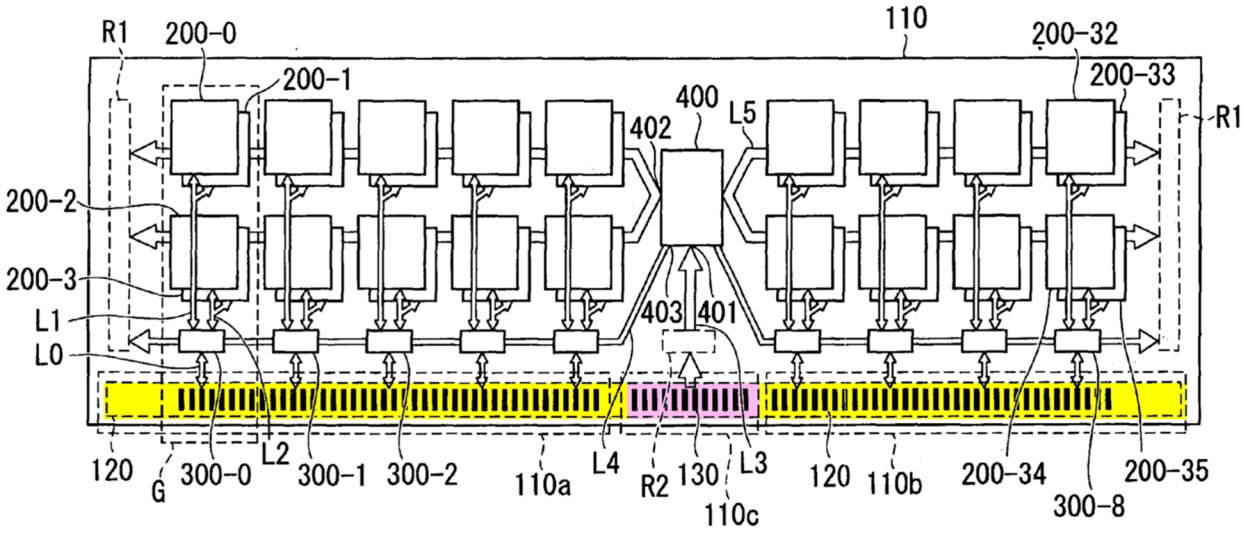
Ex. 1005, Fig. 1 (annotated), [0054]–[0055]; Ex. 1003, ¶ 80. Line 23 (part of the claimed "*memory bus*") of Figure 3 uses these connectors to connect "*signal lines*" shown above as L0 and L3. Ex. 1005, [0054]–[0055], [0075]; Ex. 1003, ¶ 80. As Dr. Alpert explains, a POSITA would recognize that the L3 signal line represents the "*control/address signal line*" and the L0 signal lines represent the "*data/strobe signal lines*." Ex. 1005, [0054]–[0055], [0075]; Ex. 1003, ¶ 80.

b. A Module Board

Osanai also discloses "*a module board having edge connections for coupling to respective signal lines in the memory bus*." Figure 1 of Osanai shows that memory module 100 includes data connectors 120 and 130 (the "*edge connections*"). As

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shown in Figure 1 below, these connectors are located on the edge and connect the signal lines L0 and L3 to line 23 of the memory bus:



Ex, 1005, [0054] ("The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between memory module 100 and the controller [12]."); Ex. 1003, ¶ 83. Accordingly, the connectors 120 and 130 satisfy the claimed "*edge connections*." *Id.*

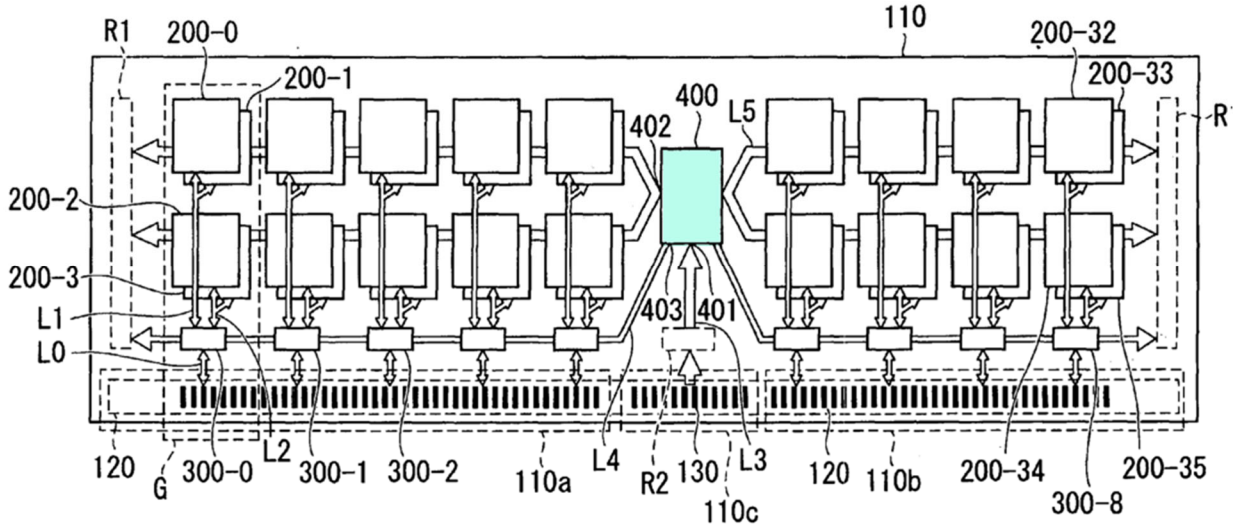
c. A Module Control Device

Osanai also discloses "*a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module*

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control device being further configured to receive a system clock signal and output a module clock signal."

Figure 1 of Osanai shows a command/address/control register buffer 400 ("*module control device*") mounted on memory module 100, shown below:



Ex. 1005, [0066] ("The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200"); *see also id*. Fig. 6 (path 401 to 402), [0101]–[0103]; Ex. 1003, ¶ 86. The memory controller 12 sends command/address/control signals to buffer 400, which are "*system command signals*." Ex. 1005, [0053], [0102]; Ex. 1003, ¶ 87.

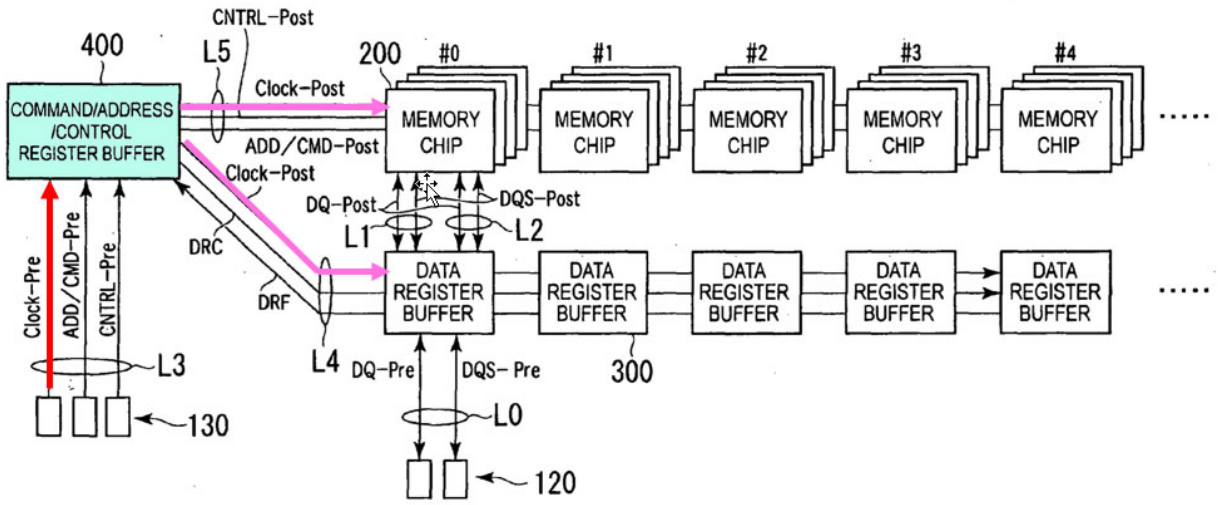
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In response, Osanai's command/address/control register buffer 400 ("*module control device*") outputs "*module command*" and "*control signals*," such as address (ADD), Command (CMD), Control (CTRL), and Clock (CK) (each being a "*module command signal*") as well as control signal DRC (a "*module control signal*"). Ex. 1005, Fig. 6, [0103]; Ex. 1003, ¶ 87. Register buffer 400 also outputs DRC (Data Register Control) (including both "*module control*" and "*command signals*") to the DRC circuit 320 in buffer 300 (*see* Ex. 1005, Fig. 5), which controls operation of the input and output buffers of the data register buffer 300, *e.g.*, adjustment of output impedance and/or control of ODT operations signals. Ex. 1005, [0066], [0105], [0132]; Ex. 1003, ¶ 87; *see* Ex. 1005, Figs. 4 and 6, [0078]–[0084], [0093], [0103], [0106]. These interpretations are consistent with how the '608 patent describes "*module command signals*" and "*control signals*." Ex. 1001, 4:65-5:54, 7:59-63 (explaining what constitutes command signals). Osanai's command/address/control register buffer 400 is configured to receive these signals for read or write operations (the claimed "*memory operations*"). *See id.* Figs. 11, 15, and 17 (read operations), [0080] and [0085]. As Dr. Alpert explains, a POSITA would have recognized that the '608 patent confirms that Osanai's signals are the claimed "*module control*" and "*command signals*" for the "*memory operations*," such as a read operation. Ex. 1003, ¶ 88; *see* Ex. 1001, 3:27-38, 5:11–57. Such a person would thus have understood

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that Osanai discloses the claimed "*module control*" and "*command signals*." Ex. 1003, ¶ 88.

Osanai further discloses "*the module control device being further configured to receive a system clock signal and output a module clock signal*." As shown in annotated Figure 7, Osanai's command/address/control register buffer 400 ("*module control device*") also receives a Clock-Pre Signal ("*system clock signal*") (shown as red arrow) and outputs a Clock-Post signal ("*a module clock signal*") (shown as pink arrow):



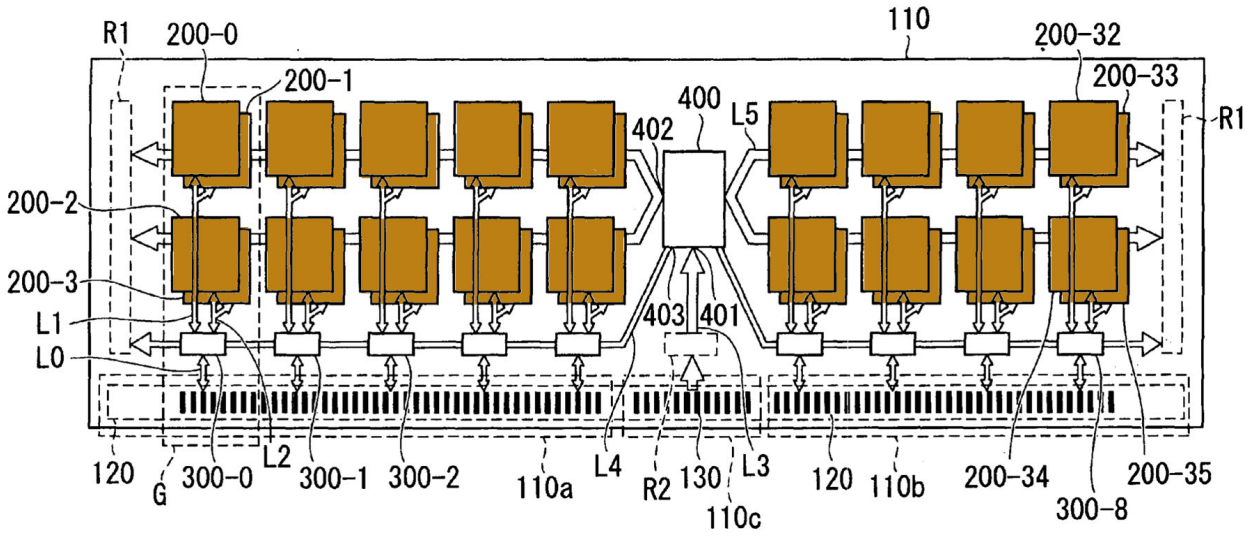
Ex. 1005, Fig. 7 (annotated), [0114]; Ex. 1003, ¶¶ 89–90; *see* Ex. 1005, Figs. 6–7, [0104], [0112]–[0113]. A POSITA would have recognized that Osanai's command/address/control register buffer 400 outputs the same clock signals to the data buffers and memory chips. Ex. 1003, ¶ 90; *see* Ex. 1005, Figs. 4–6 and 7, [0104], [0112]–[0113], [0154]. Such a person would have recognized that these

Clock-Post signals have the same timing. Ex. 1003, ¶ 90; *see* Ex. 1005, Figs. 12, 15, 17, [0154].

d. Memory Devices

Osanai also discloses "*memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals*."

Figure 1 of Osanai discloses multiple memory chips 200 ("*memory devices*") mounted on the memory module 100, shown below:



Ex. 1005, Fig. 1 (annotated); Ex. 1003, ¶ 93. These memory chips 200 perform memory operations as instructed. Ex. 1003, ¶ 93; Ex. 1005, [0060] ("An operation of the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the

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command/address/control register buffer 400. Details on the memory chip 200 will be described later."). To do so, Osanai's memory chips receive both CNTRL-Post signals ("*module command signals*") and Clock-post signals ("*clock signals*") to instruct them to perform operations. Ex. 1005, [0112] ("The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips **200** are supplied from the command/address/control register buffer **400**."); *see id.* Figs. 6 and 7, [0104], [0101]–[0111], [0113]–[0114]. Such memory operations include both read and write operations. Ex. 1005, [0060], [0085], [0090], Ex. 1003, ¶ 93.

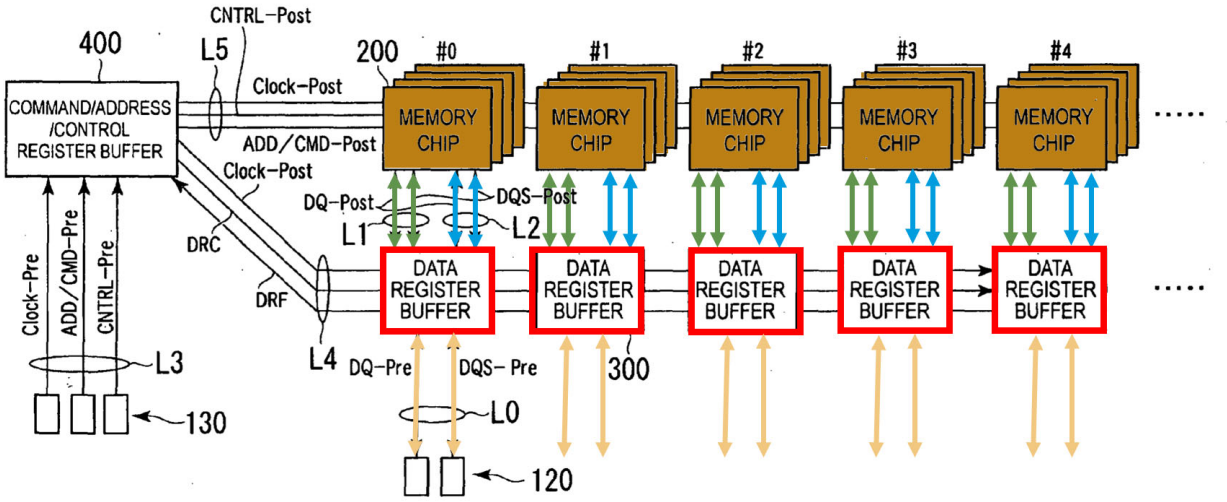
e. Sets of Memory Devices

Osanai also discloses "*the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines*."

Osanai's memory chips 200 are grouped into sets making "*a plurality of sets of memory devices*," which share a data buffer. Ex. 1005, [0058] ("In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other."). Each group has its own respective set of data/strobe signal lines, L0 data lines. Ex.

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1003, ¶ 96. Lines L1 and L2 are coupled to the memory bus via their data buffer and respective connector in Line L0. *See* Ex. 1005, Figs. 5 and 7. Annotated Figure 7 of Osanai illustrates these lines:

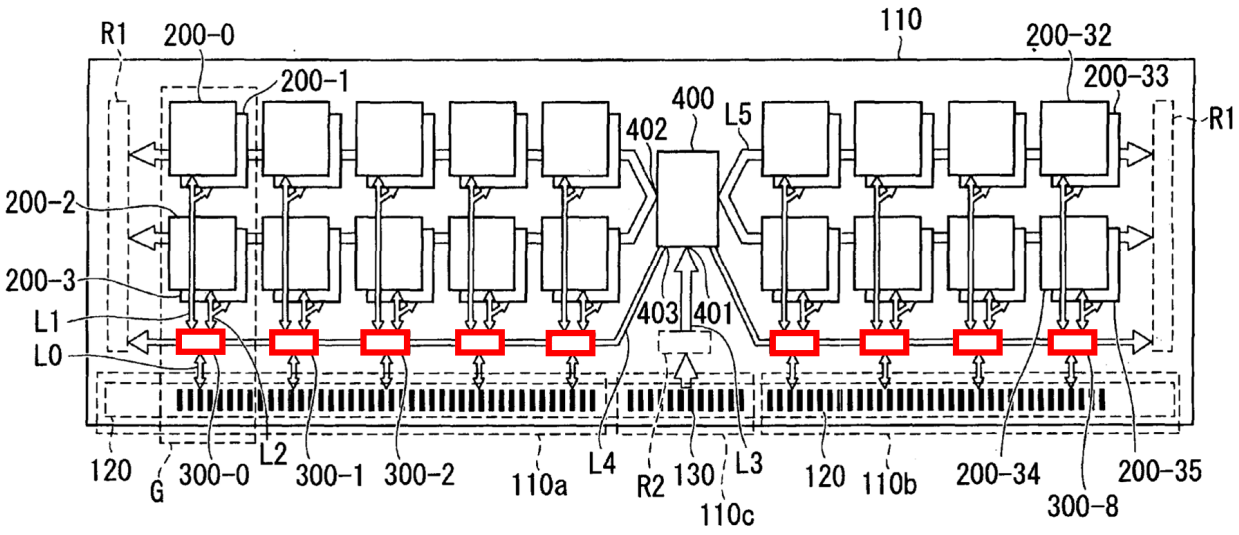


Ex. 1005, Fig. 7, [0109]. Accordingly, memory chip sets communicate with their respective data register buffer and have a corresponding set of L0 data lines (a "*plurality of sets of data/strobe signal lines*"). Ex. 1003, ¶ 97.

f. Buffer Circuits

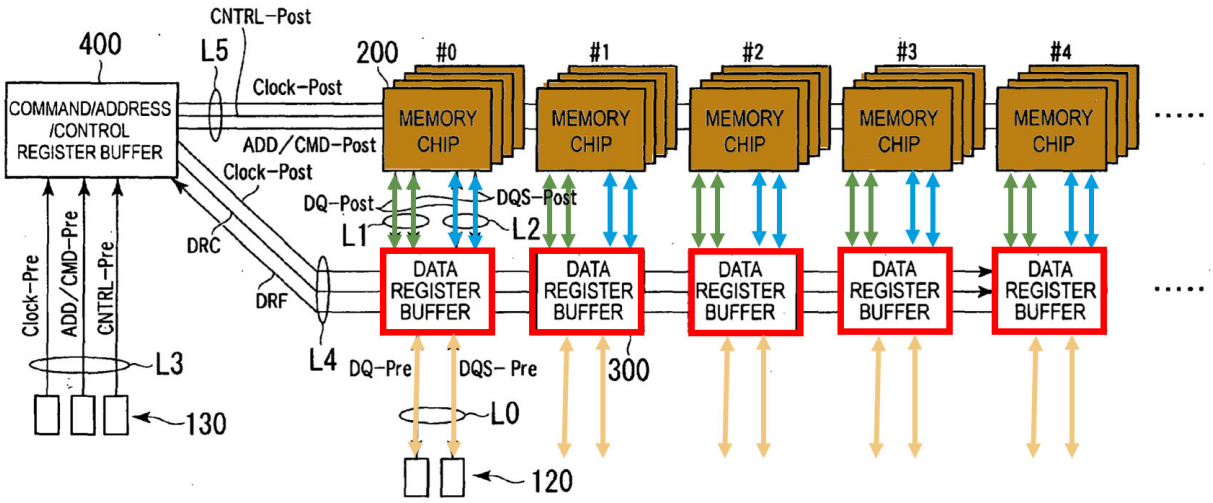
Osanai also discloses "*a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board*."

Figure 1 of Osanai discloses data register buffers 300 that are mounted on the memory module 100 ("*wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board*"), shown below:



Ex. 1005, Fig. 1 (annotated), [0052] ("Furthermore, in the present embodiment, the memory module 100 includes nine data register buffers 300. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers 300-0 to 300-8."); Ex. 1003, ¶ 100. Likewise, annotated Figure 7 shows how each data register buffer 300 is paired with a set of memory chips and L0 data lines ("*respective sets of the plurality of sets of data/strobe signal lines*"):

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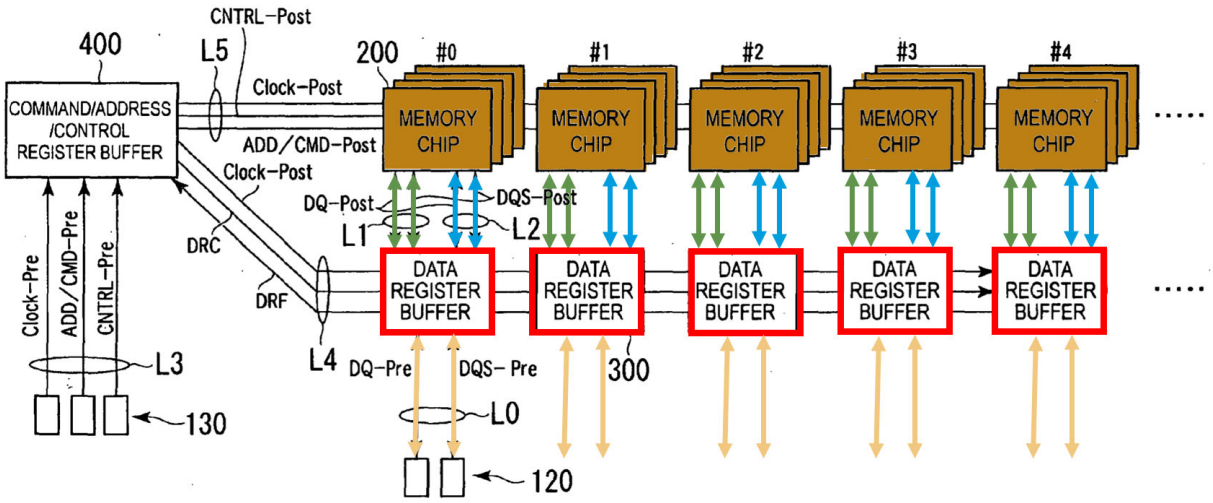


Ex. 1005, Fig. 7 (annotated), [0061]–[0062], [0109]; Ex. 1003, ¶ 101; *see* Ex. 1005, Fig. 1.

g. Data/Strobe Lines

Osanai also discloses "[*wherein each respective buffer circuit is mounted on the module board*] *coupled between a respective set of data/strobe signal lines and a respective set of memory devices and configured to receive the module control signals and the module clock signal*."

Figures 1 and 7 show that each data register buffer 300 (a "*buffer circuit*") is mounted on the module between L0 data lines ("*respective set*[] *of the plurality of set of data/strobe signal lines*") and its respective memory chip group (#0 through #4) (each being a "*respective set of memory devices*"), shown below:

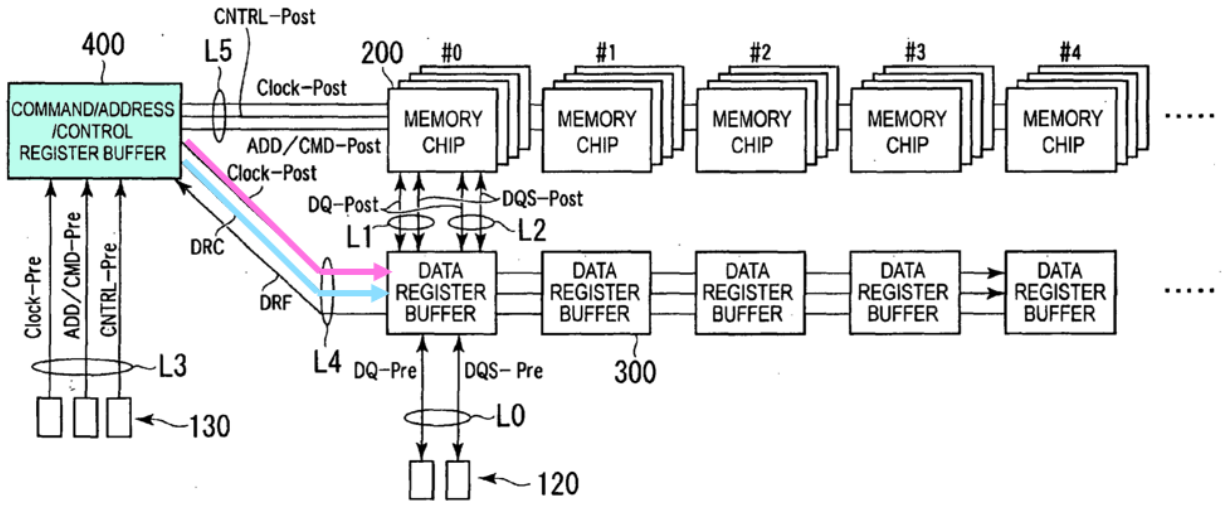


Id. at Fig. 7 (annotated), [0109]; *see id.*, Fig. 1, Claim 8. As shown in annotated Figure 7 above, memory chips are organized into groups, thereby making a "*respective set of memory devices*." Ex. 1005, [0057]–[0058]; Ex. 1003, ¶ 104. In describing Figure 7, Osanai states that "the data register buffer 300 and [each group of] the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005, [0109]; Ex. 1003, ¶ 105; *see also* Fig. 1. Lines L1 and L2 are coupled to the memory bus via their respective connectors for the L0 data lines, which are "*respective sets of the plurality of set of data/strobe signal lines*." Ex. 1003, ¶ 105; *see* Ex. 1005, Figs. 5 and 7, [0109]. Thus, Osanai discloses this limitation.

Osanai further discloses "*wherein each respective buffer circuit of the plurality of buffer circuits is… configured to receive the module control signals and the module clock signal*."

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As shown in annotated Figure 7, Osanai's command/address/control register buffer 400 ("*module control device*") outputs a Clock-Post signal ("*a module clock signal*") (shown as pink arrow) and DRC ("*module control signals*") (shown as blue arrow) to buffers 300:

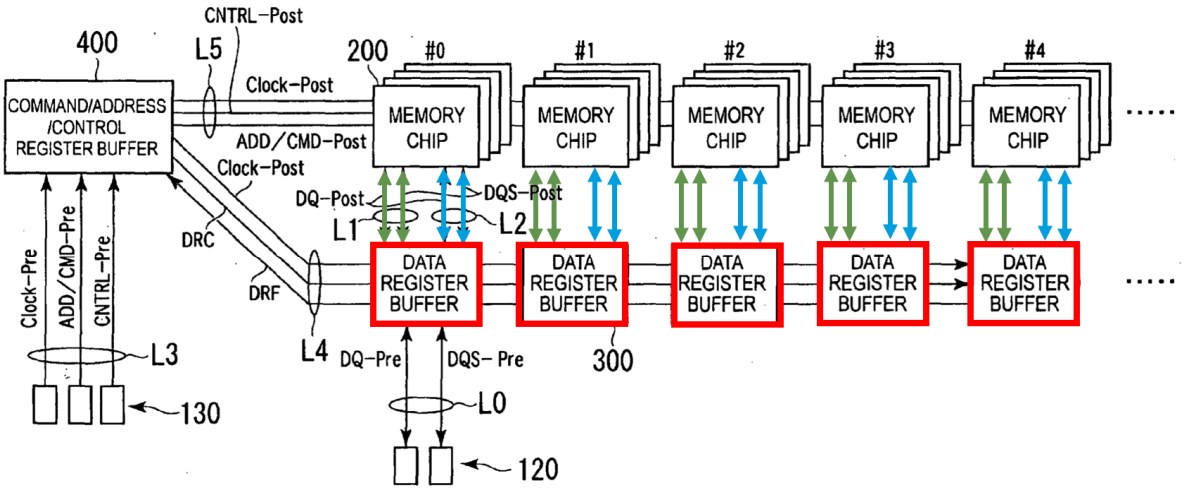


Ex. 1005, Fig. 7 (annotated), [0114]; Ex. 1003, ¶ 107; *see* Ex. 1005, Fig. 1 (showing the buffers 300 are mounted on the memory module), Figs. 6–7, [0104], [0112]–[0113]. A POSITA would have recognized that Osanai's command/address/control register buffer 400 outputs clock signals to the data buffer. Ex. 1003, ¶ 107; *see* Ex. 1005, Figs. 6 and 7, [0093], [0104], [0112]–[0113]. Such a person would have recognized that the command/address/control register buffer 400 also outputs "*module control signals*," such as Read commands, to the data register 300 as part of the control signal DRC. Ex. 1003, ¶ 107; *see* Ex. 1005, [0154], [0157], [0164].

h. A Data Path

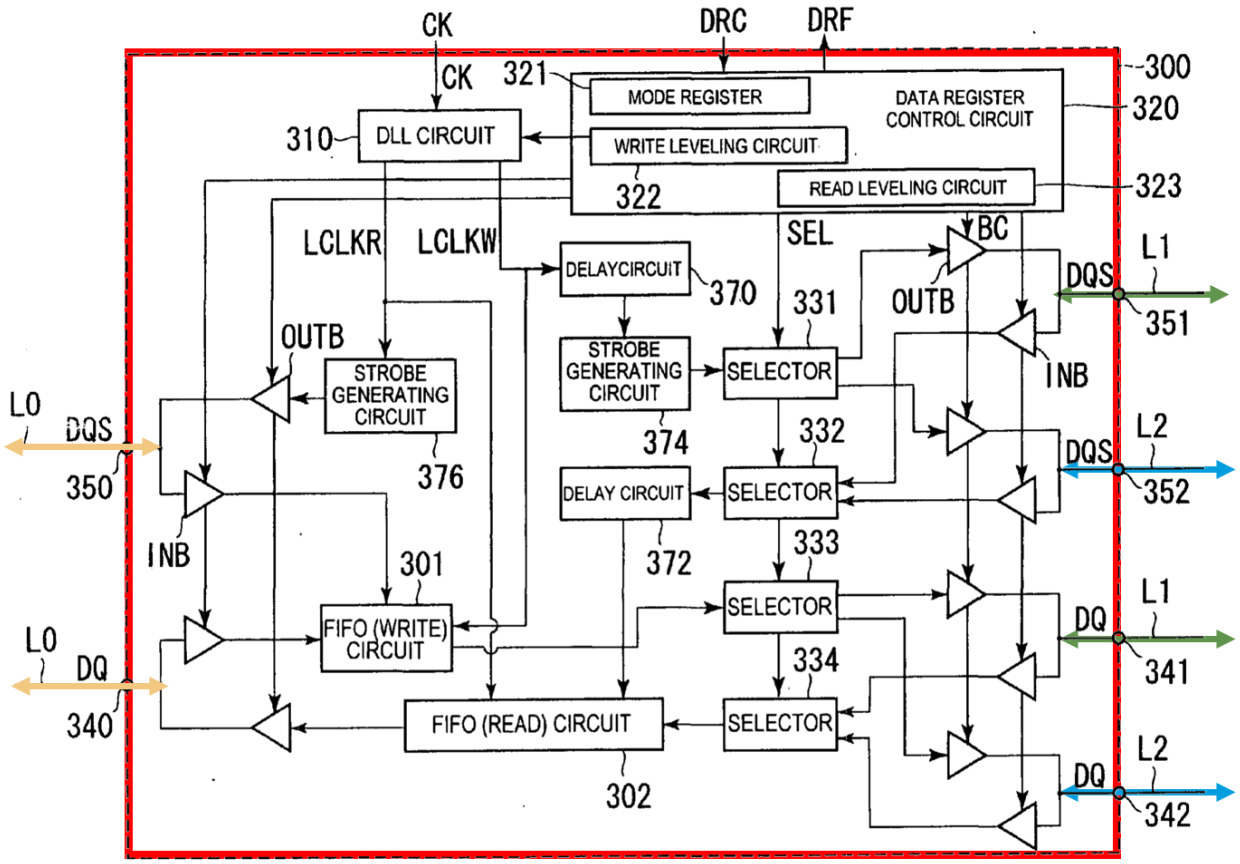
Osanai also discloses that "*each respective buffer circuit includ*[*es*] *a data path corresponding to each data signal line in the respective set of data/strobe signal lines*."

Figure 7 shows that each data register buffer 300 has "*data paths*" that correspond to each data signal line, L1 and L2 data lines, connected to each memory chip group (#0 through #4…), shown below:



Id. at Fig. 7 (annotated), [0109] ("The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line[s] L1 or L2."); Ex. 1003, ¶ 110; *see also* Ex. 1005, Fig. 1. A POSITA would have understood these data paths include circuitry components in the data register

buffer 300 that connect each L0 data lines ("*respective set of data/strobe signal lines*") at terminals 340 and 350, shown in Figure 5 below:



Ex. 1005, Fig. 5 (annotated), [0109], Ex. 1003, ¶ 110.

Using L1 or L2, the data register buffer 300 transmits "*data and strobe signals*." Ex. 1005, Fig. 5, [0109] ("In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and *a data strobe signal transferred through the data line L1 or L2*

is represented by a data strobe signal DQS-Post.") (emphasis added); Ex. 1003, ¶ 111. Specifically, data buffer 300 receives DQS-Pre signals from data line L0 and outputs DQS-Post over data line L1 or L2. Ex. 1005, Fig. 5, [0109], Ex. 1003, ¶ 111. Using the same data lines, data register buffer 300 sends DQ-Post after processing DQ-Pre received over data line L0. Ex. 1005, Fig. 5, [0109], Ex. 1003, ¶ 112. These two signals, DQ-Post and DQS-Post, are "*data and strobe signals*." *Id.*

i. Command Processing Circuit

Osanai also discloses that buffer circuits 300 include "*a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit*."

Figure 5 of Osanai illustrates a data register buffer 300 that includes a data register control circuit 320 and DLL Circuit 310 (collectively, the "*command processing circuit*") that uses received DRC signals and clock signals to select the appropriate data path, shown below:

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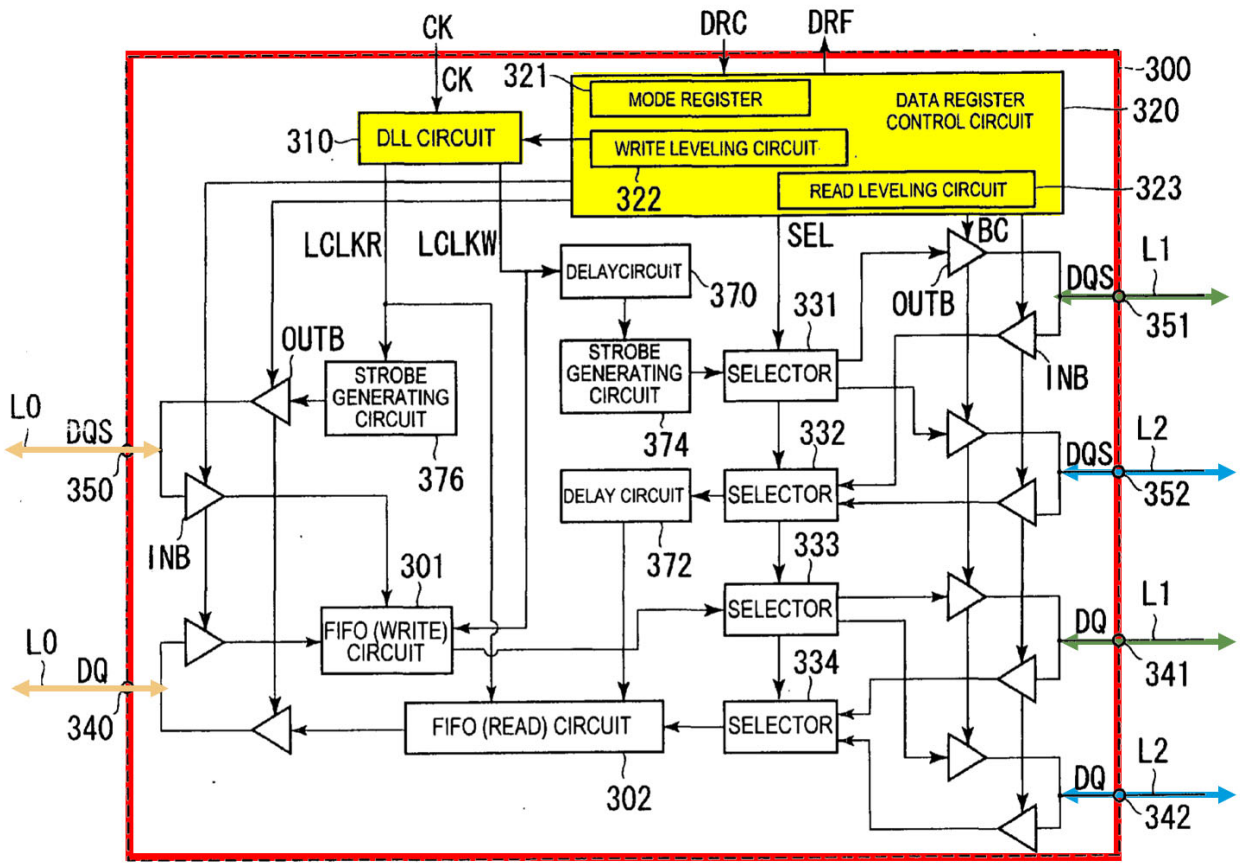


FIG.5

Id., Fig. 5 (annotated), [0094]; *see id.*, Fig. 2, [0094], [0096]; *see also id.*, [0158], [0163]. Using decoded DRC ("*module control signals*") signals, the data register control circuit 320 enables different data paths for reading and writing operations ("*control the data path*"). Ex. 1003, ¶ 115; *see* Ex. 1005, [0106] ("The control signal DRC includes … a signal indicating a direction of transmitting and receiving data …"); *see also id*., [0094], [0097], [0105], [0132]. For example, and as Dr. Alpert explains, a POSITA would have understood these disclosures to teach that the data register control circuit 320 selects (or "*controls*") certain paths using SEL, INB, and OUTB signals as well as selectors 331–334, which supplies data DQ to input or

output terminals, 341 and 342, to certain memory chips 200. Ex. 1003, ¶ 115; Ex. 1005, [0094], [0097]. This interpretation is consistent with how the '608 patent describes "*control*[*ling*] *a data path*." *See* Ex. 1001, 5:43–45, 12:10–20, 18:10–15. In addition, Osanai's DLL circuit 310 receives this module (CK) signal and uses that signal to generates two local clocks: one for read operations (LCLKR) and another for write operations (LCLKW). Ex. 1005, [0090]. A POSITA would have recognized the data path would have used the appropriate clocks in their respective read/write operation data paths. Ex. 1003, ¶ 115; *see* Ex. 1005, Fig. 5. Consequently, a POSITA would have recognized that Osanai's data register buffer 300 selects data paths "*in accordance with the module control signals and the module clock signal*." *Id.*

Any data path selected by Osanai's data register control circuit 320 includes a "*tristate buffer*." Ex. 1003, ¶ 116. For example, Osanai discloses tristate buffers, such as the OUTB buffers. Ex. 1005, [0094], Figure 5. As Dr. Alpert explains, a POSITA would have recognized that Osanai's buffers necessarily operate in a third, high-impedance state so that they would not overload or interfere with the other buffer operations. Ex. 1003, ¶ 116; *see* Ex. 1005, Fig. 5, OUTB buffer. Such a person would have recognized that, in addition to its on/off states, the buffers used for read operations over line 340 would necessarily need to be in a high-impedance state during write operations. *See* Figs. 5 and 11, [0129]–[0136]; Ex. 1003, ¶ 116;

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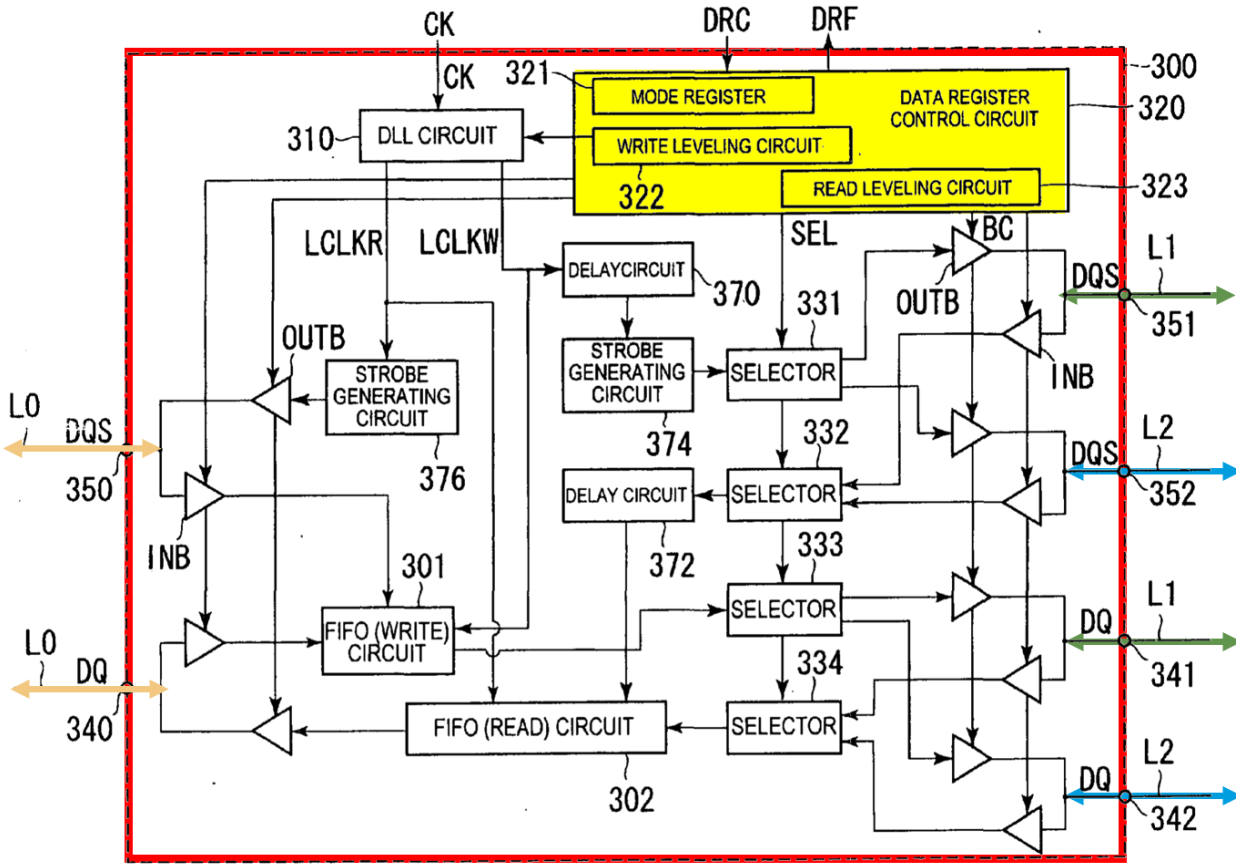
see also Ex. 1005, [0090]–[0094], [0097]–[0098], [0105]–[0106]. Such a person would have understood that these buffers are "*tristate buffers*" because each has three states—namely, on, off, or electrically disconnected. Ex. 1015, p. 6. Further, and as Dr. Alpert explains, a POSITA would have also recognized that these buffers are part of data paths controlled by data register control circuit 320, *see* Ex. 1005, [0090]–[0094], [0097]–[0098], [0105]–[0106]), and connected to L1 and L2 data lines that connect to memory chips 200 (*see* Ex. 1005, Fig. 1). Ex. 1003, ¶ 116. Accordingly, data register buffer 300 includes "*data path(s) corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit*." Ex. 1003, ¶ 116.

j. Delay Circuit

Osanai also discloses that buffer circuits 300 include "*a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals*."

Osanai's control circuit 320 further includes read leveling and write leveling circuits 322 and 323, shown below:

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Id., Fig. 5 (annotated), Ex. 1003, ¶ 120. As Dr. Alpert explains, a POSITA would have recognized that this data register control circuit 320 (part of the claimed "*command processing circuit*") also includes the read leveling and write leveling circuits 322 and 323. Ex. 1003, ¶ 121. Such a person would have recognized that both read and write leveling circuitries compensate for propagation delays caused by some memory chips being placed farther away from their respective data register buffers. *Id.*; Ex. 1005, [0146] ("The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal.").

To make these adjustments, the read/write leveling circuitry and DLL Circuit 310 (part of the claimed "*command processing circuit*") use the module clock (CK) signal sent from the command/address/control register buffer 400. Ex. 1003, ¶ 122; *see* Ex. 1005, Fig. 5, CK, Fig. 7, Clock-Post. Based on this clock signal, a "timing adjustment"—that is, an added time delay—is then used to compensate for propagation delays. Ex. 1005, [0110]; *see id.*, [0149]–[0157]. For example, during the write leveling operation, Osanai's "data register buffer 300 outputs a data strobe signal DQS that is synchronized with the clock signal CK," which is supplied by command/address/control register buffer 400. *Id.* [0149]. Because of differing propagation delays, however, "input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip **200** side." *Id.* To correct this timing error, the write leveling circuitry 322 delays the output timing of the DQS sent from data register buffer 300, thus creating DQS-Post ("*delay*[*ing*] *a signal through the data path by an amount determined by the command processing circuit*"). *Id.* [0151]–[0152]; Ex. 1003, ¶ 123. A similar read leveling process results in signals being delayed. Ex. 1005, [0153]–[0157]; Ex. 1003, ¶ 123. Using these leveling techniques, the leveling circuitry "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal." Ex. 1005, [0146]; *see id.*, [0149]–[0157]; Ex. 1003, ¶ 123.

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A POSITA would have recognized that specific delays were chosen "*in response to at least one of the module control signals*." Ex. 1003, ¶ 124. For example, the specific delay chosen depends on whether the DRC mode that represents a read operation or write operations, which use different "*module control signals*." Ex. 1005, [0132] ("In addition, the command/address/control register buffer 400 supplies *a read command Read to the data register buffer 300 as a part of the control signal DRC*.") (emphasis added); *see id.*, Fig. 7, [0094], [0154]–[0157], [0164]; Ex. 1003, ¶ 124. Alternatively, read and write leveling circuitry uses the module clock (CK) signal (another type of "*module control signal*"). Ex. 1003, ¶ 124; *see* Ex. 1005, Fig. 5, CK, Fig. 7, Clock-Post. Consequently, a POSITA would have understood that Osanai's control circuit 320 determines the delay "*amount… in response to at least one of the module control signals*." Ex. 1003, ¶ 125.

2. Claim 4

Claim 4 depends on claim 1 and recites "*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte*." Osanai discloses this limitation.

Osanai data register buffer 300 has a data width of "*1-byte.*" Ex. 1005, [0091]. Osanai expressly discloses that "a single data register buffer 300 inputs and outputs 1-byte data…." *Id.*; Ex. 1003, ¶ 127. Each of Osanai's memory devices also has a

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data width of 1 byte ("*each of the memory devices has a data width of 1 byte*"). Ex. 1005, [0059] ("An arrow of each of the data lines L1 and L2 shown in Fig. 1 indicates a line of 1 byte (8 bits)"); Ex. 1003, ¶ 127.

C. Ground 2: Osanai in View of Tokuhiro Renders Claims 1–5 Obvious

Claims 1-5 are also obvious over Osanai in view of Tokuhiro. Petitioners rely upon the Osanai disclosures set forth in Ground 1 and show how the challenged claims are obvious in further view of Tokuhiro below

1. Claim 1: "delay[ing] a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals."

To the extent that Netlist argues Osanai does not explicitly disclose to "*delay a signal through the data path by an amount determined… in response to at least one of the module control signals*," this feature is rendered obvious by Tokuhiro.

a. Tokuhiro discloses "delay[ing] a signal through the data path by an amount determined… in response to… control signals."

Like Osanai, Tokuhiro discloses read and write leveling techniques. Ex. 1003, ¶ 130. Tokuhiro explains that such leveling techniques are necessary to compensate for different propagation delays. Ex. 1006, 1:63–2:9. Specifically, Tokuhiro states that propagation delays differ because memory units have different wiring lengths. *Id*. To compensate for these different delays, "the difference in the delay time caused in the write operations between the memory controller 90 and the plurality of

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SDRAMs 92 is adjusted by employing the write leveling function." *Id.*, 2:46–49. Tokuhiro recognizes that the "delay [determined from the write leveling function] may affect [] reading data from the SDRAM 92," as well. *Id.* 3:9–12.

Consequently, Tokuhiro teaches a delay unit that calculates a first delay time from a write operation to use in its calculation of a second delay time used for a read operation ("*delaying a signal…by an amount determined*"). Ex. 1003, ¶ 131; Ex. 1006, 3:16–26 ("[A] first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time."). Specifically, Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the write level operation:

> Because the wirings for connection between the memory controller 12 and the DIMM 11 are formed in the same length, … ***In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling.*** Accordingly, in the second delay time control unit **24**, ***the second delay time Dt2-x corresponding to one SDRAM-x is set by using the above-mentioned formula (3-5) so that the sum of the first delay time Dt1-x and the second delay time Dt2-x both corresponding to the relevant SDRAM-x is equal to a preset value.***

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Id., at 16:1–23 (emphases added), Abstract. Because Tokuhiro uses "*timing information*" determined during the write operation for a subsequent read operation, it follows that the write operation necessarily occurred before the read operation. Ex. 1003, ¶ 131.

A POSITA would have recognized that Tokuhiro's delay technique obtains delay times for read and write operations using "*control signals*." *See* Ex. 1006, 9:1–32, 11:5–46, 12:42–58, 14:59–15:15, 16:47–17:11, 23:23–40, 26:21–46; Ex. 1003, ¶ 132. Tokuhiro explains as much:

> Further, the first delay time control unit *23 outputs the* ***respective first control signals d1*** to the first variable delay circuits DW-**1** to DW-n so that the set first delay times Dt**1**-**1** to Dt**1**-*n* are obtained. ***In accordance with the first control signals d1***, the first variable delay circuits DW-**1** to DW-n delay the data strobe signals DQS-**1** to DQS-n by the first delay times Dt**1**-**1** to Dt**1**-*n*, respectively.…
>
> Further, the second delay time control unit 24 ***outputs the respective second control signals d2*** to the second variable delay circuits DR-1 to DR-n so that the set second delay times Dt2-1 to Dt2-n are obtained***. In accordance with the second control signals d2***, the second variable delay circuits DR-1 to DR-n delay the data signals DQ-1 to DQ-n by the second delay times Dt2-1 to Dt2-n, respectively.

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Ex. 1006, 14:59–15:15; *see id.* 9:1–32, 11:5–46, 12:42–58, 16:47–17:11, 23:23–40, 26:21–46; Ex. 1003, ¶ 132. Accordingly, a POSITA would have recognized that Tokuhiro's technique "*delay*[*s*] *a signal…by an amount determined… in response to at least one of the… control signals*." Ex. 1003, ¶ 132.

The challenged claims encompass Tokuhiro's technique, which mirrors the '608 patent's description of how the delay amount is determined. Ex. 1003, ¶ 133. Specifically, the '608 patent explains that the delay amount for a read operation is determined using a timing interval determined during a prior write operation:

> Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, *during a write operation*, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. *This time interval is used during a subsequent read operation* to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

Ex. 1001, 4:9–19 (emphasis added); *see also id.*, Claim 2. As explained above, Tokuhiro also discloses that timing information determined during a write operation is used in determining a delay for subsequent read operations. Ex. 1003, ¶ 133; Ex.

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1006, 3:16–26, 16:14–23. Consequently, Tokuhiro discloses the same technique that is described by the ’608 patent—but years earlier.

b. It would have been obvious to use Tokuhiro’s technique in Osanai’s buffer leveling circuitries.

Osanai and Tokuhiro are analogous art to the ’608 patent. Ex. 1003, ¶135. Both are analogous art because they are directed toward the same field of endeavor—namely, memory modules. *Id.*; Ex. 1001, 1:37–39; Ex. 1005, [0001], Ex. 1006, 1:15–20. Moreover, both are analogous art because they are reasonably pertinent to a problem described by the ’608 patent: “[a]s memory operating speed and memory density continue to increase, however, such [read and write] leveling mechanisms are also insufficient to [ensure] proper timing of the control and/or data signals….” Ex. 1001, 2:32–36; Ex. 1005, [0110]; Ex. 1006, 1:15–20.

A POSITA would have been motivated to incorporate Tokuhiro’s leveling technique in Osanai’s data register control circuit 320 for at least three primary reasons. Each reason alone satisfies the requisite rationale according to *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007).

First, and as Dr. Alpert explains, it would have been obvious to use Tokuhiro’s teaching in Osanai’s data register control circuit 320 to achieve the same benefit achieved by Tokuhiro’s device, i.e., reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling. Ex. 1003, ¶ 137. Incorporating Tokuhiro’s

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technique would have provided the same efficiency to Osanai's memory module. Ex. 1003, ¶ 137. Such a modification to Osanai's data register buffer would not be beyond the skill of a POSITA. Ex. 1003, ¶ 137. Thus, such a modification would have been obvious. *KSR*, 550 U.S. at 417 ("For the same reason, if a technique has been used to improve one device, and a [POSITA] would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.").

Second, and as Dr. Alpert explains, a POSITA would have been motivated to modify Osanai's data register buffer to incorporate Tokuhiro's technique based on the express teaching found in Tokuhiro—namely, reduced power consumption and circuit area. Ex. 1006, 24:26–29 ("Accordingly, the delay times Dt1 and Dt2 from the input of the two signals to the output thereof ***can be efficiently set without increasing the power consumption and the area*** occupied by the apparatus.") (emphasis added); *see* Ex. 1006, Figs. 16-17, 21:15-24:42, Ex. 1003, ¶ 138. Such a person would have recognized that Tokuhiro's technique of using a common structure for implementing write and read delays would improve power consumption for Osanai's memory module. Ex. 1003, ¶ 138. That person would also have recognized that, by reducing the circuit area, this modification would have necessarily reduced costs by increasing manufacturing yield. Ex. 1003, ¶ 138. By compensating for such a delay, a POSITA would have recognized that the delay

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calculated using Tokuhiro's leveling technique would be more energy-efficient than a conventional read/write leveling technique that did not account for a write operation's delay. Ex. 1003, ¶ 138; *see also* Ex. 1006, Figs. 16-17, 21:15-24:42. A POSITA would have thus been motivated to use Tokuhiro's technique in Osanai's data register control circuit 320. Ex. 1003, ¶ 138.

Third, and as Dr. Alpert explains, a POSITA would have been motivated to modify Osanai's data register control circuit 320 to incorporate Tokuhiro's teaching to improve signal fidelity, decrease timing skew among components, and/or lower the load perceived by the memory controller. Ex. 1003, ¶ 139. Osanai and Tokuhiro recognize these are problems in the prior art. Ex. 1005, [0004]–[0005], [0075]–[0076], [0117]–[0119], [0176], [0194]; Ex. 1006, 1:63–2:28, 3:1–13. Based on these disclosures, a POSITA would have sought ways to mitigate these problems and Tokuhiro's technique would have provided a way to do so. Ex. 1003, ¶ 139; Ex. 1006, 3:16–26, 19:8–13, 19:25–33. Accordingly, a POSITA would be motivated to modify Osanai's data register control circuit 320 to incorporate Tokuhiro's teaching. Ex. 1003, ¶ 139.

For any of these reasons, a POSITA would have been motivated to modify Osanai's data register control circuit 320 to include Tokuhiro's leveling technique. Ex. 1003, ¶ 140. By doing so, the combination of Osanai and Tokuhiro render obvious "*delaying a signal through the data path by an amount determined …in*

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response to at least one of the module control signals." *Id.* The combination of Osanai and Tokuhiro thus render claim 1 obvious.

2. Claim 2

Claim 2 depends on claim 1 and further recites "*wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.*" Osanai, as modified by Tokuhiro, discloses this limitation.

The combination of Osanai and Tokuhiro render obvious "*a first memory operation and a second memory operation subsequent to the first memory operation*." Osanai's data register buffer 300 has logic that calculates the timing information used in both read (the "*second memory operation*") and write operations (the "*first memory operation*"). Ex. 1005, Fig. 2, [0096] ("Furthermore, the data

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register control circuit **320** includes a write leveling circuit **322** and a read leveling circuit **323**. The write leveling circuit **322** is a circuit for *performing a write leveling operation*, and the read leveling circuit **323** is a circuit for *performing a read leveling operation*.") (emphases added). Combined with Tokuhiro, Osanai's data register buffer must necessarily obtain timing information during a "*first*" (write) "*memory operation*" prior to the read *("second*") "*memory operation*" because Tokuhiro's technique uses the timing information from the writing operation to determine the time delay for the read operation. Ex. 1003, ¶ 142; Ex. 1006, 3:16–26, 16:14–23 Accordingly, the combination of Osanai and Tokuhiro render obvious "*a first memory operation and a second memory operation subsequent to the first memory operation*."

Osanai, as modified, also discloses "*wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals*." As explained above, *see* § V.B.1.c, Osanai discloses a command/address/control register buffer 400 that receives "*system command signals*" and outputs "*module command*" and "*control signals.*" Ex. 1003, ¶ 143.

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Osanai also explains that these "*signals*" are different for each memory operation, such as a write operation ("*first memory operation*") and read operation ("*second memory operation*"). Ex. 1005, [0060] (states that "[a]n operation of the memory chip 200 is controlled based on the command signals"); Ex. 1003, ¶ 143; *see* Ex. 1005, [0090], [0097], [0109]–[0110]. A POSITA would have understood these disclosures to mean that read or write operations have a different "*set of command signals*" that result in a different "*set of module control signals output by the module control device in response to the first set of command signals*." Ex. 1005, Fig. 11, Fig. 12 [0129]-[0132], [0138]-[0140]; Ex. 1003, ¶ 143. Such a person would thus have recognized that Osanai discloses that a write operation (the "*first memory operation*") "*includes a first set of command signals*" that is received by command/address/control register buffer 400 (*"module control device*"), which then outputs "*a first set of module control signals*." Ex. 1003, ¶ 143. Likewise, such a person would have recognized that Osanai discloses that a read operation (the "*second memory operation*") "*includes a second set of command signals*" that, when received by command/address/control register buffer 400 (*"module control device*"), output "*a second set of module control signals*." Ex. 1003, ¶ 143. Thus, Osanai, as modified, discloses this limitation.

Claim 2 also requires "*wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal*

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through the data path is a signal associated with the second memory operation." A POSITA would have understood that this limitation, stated otherwise, requires that the data register buffer use the "*first set of module control signals*" for one memory operation to determine the delay and that delay would be applied to "*a signal associated with the second memory operation*." *See* Ex. 1001, Claim 1 and 2; Ex. 1003, ¶ 144. According to the prosecution history, *see* § III.D above, this limitation most closely resembles the supposed claimed feature that overcame the prior art: having a buffer that "obtains timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information." Ex. 1002, p. 206; *see* Ex. 1008, Claim 1.

Osanai, as modified, discloses this limitation as well. As explained above, *see* § 145, Tokuhiro's delay technique obtains delay times for read and write operations using "*control signals*" and that it calculates a first delay time from a write operation to use in its calculation of a second delay time used for a read operation. A POSITA would have understood that, by incorporating Tokuhiro's technique into Osanai's data register control circuit 320, the modified circuit would use "*module control signals*" to determine delay time for the write (or "*first*") memory operation ("*wherein the at least one of the module control signals include at least one of the first set of module control signals*"). Ex. 1003, ¶ 145. Such a person would have

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also recognized that this delay time for the write operation would be used to determine the delay for the subsequent read (or "*second*") operation, which is applied to "*a signal associated with the second memory operation*." Ex. 1003, ¶ 145.

3. Claim 3

Claim 3 depends on claim 2 and recites "*wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.*" Osanai discloses this limitation.

Osanai discloses a memory module with memory chips organized into multiple ranks. For example, Osanai discloses how the memory module organizes four memory chips 200 into a single group (or set), with one memory chip from each set belonging to a rank ("*the respective set of memory devices includes one memory device from each of the plurality of ranks*."). Ex. 1005, [0057]–[0058], [0111]. As

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explained above, *see* § V.C.2, a POSITA would thus have recognized that Osanai discloses that write and read memory operations "*include a first*" and "*second set of command signals*" that, when received by command/address/control register buffer 400 (*"module control device*"), output "*a first*" and "*second set of module control signals*," respectively. Ex. 1003, ¶ 148. These "*module control signals*" include, for example, (CS) signal or a clock enable (CKE) signal, both of which are "*chip select signal[s]*." Ex. 1005, [0057]; Ex. 1003, ¶ 148. These "chip select signal[s]" select "[t]he number of Ranks, [which] indicates the number of memory spaces that can be selected in an exclusive manner." Ex. 1005, [0057]; *see id.* [0058]; Ex. 1003, ¶ 148. Using these signals, memory chips are chosen for memory operations, such as the read operation ("*perform the second memory operation*"). Ex. 1003, ¶ 148.

As Dr. Alpert explains, a POSITA would also have recognized that such operations include "*module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals*." Ex. 1003, ¶ 149. As explained above, *see* § V.C.2, a POSITA would have understood these disclosures to mean that read or write operations have a different "*set of command signals*" that result in different "*module command signals*." Ex. 1005,

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Fig. 11, Fig. 12 [0129]–[0132], [0138]–[0140]. Ex. 1003, ¶ 149. Such a person would thus have recognized that Osanai discloses that a write operation (the "*first memory operation*") "includes a first set of command signals" that is received by command/address/control register buffer 400 ("*module control device*"), which then outputs "*a first set of module command signals*." Ex. 1003, ¶ 149. Likewise, such a person would have recognized that Osanai discloses that a read operation (the "*second memory operation*") "includes a second set of command signals" that is received by command/address/control register buffer 400 ("*module control device*"), which then outputs "*a second set of module command signals*." Ex. 1003, ¶ 149.

Osanai also discloses "*wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation*." Ex. 1003, ¶ 150. In read operations, and as Dr. Alpert explains, a POSITA would have understood that the second set of module command signals would include chip select (CS) or the clock enable (CKE) signals. Ex. 1005, [0057]–[0058], [0111]; Ex. 1003, ¶ 150. Such a person would have further understood that these signals select "*the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform*" the memory operation. *See* Ex. 1005, [0057]–[0058], [0111]; Ex. 1003, ¶ 150.

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4. Claim 4

Claim 4 depends on claim 3 and recites "*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte*." Osanai renders this limitation obvious in combination with the knowledge of a POSITA.

As explained above, *see* § V.B.2, Osanai data register buffer 300 has a data width of 1 byte ("*each of the plurality of buffer circuits has a data width of 1 byte*."). Ex. 1005, [0091]. To the extent that Netlist argues that Osanai does not disclose "*wherein each of the memory devices has a data width of 1 byte,"* such a data width is obvious over the knowledge of a POSITA. Ex. 1003, ¶ 154. Osanai explains, however, that the number of "memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number"—that is, different data widths were envisioned by Osanai. Ex. 1005, [0196].

As Dr. Alpert explains, a POSITA would have been motivated to modify Osanai's memory devices to use eight bits for at least four primary reasons. *First*, such a person would have used four bits to comply with the commercial standardization of the DDR3 standard, which specified 8 bits. Ex. 1003, ¶ 154; Ex. 1013, p. 4 (showing x8 DRAM with four data lines). *Second*, such a person would have been motivated to reduce packaging costs, thereby realizing cost savings on the module. Ex. 1003, ¶ 154; Ex. 1013, p. 3. *Third*, using a data width of eight bits would

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have been a common design tradeoff; for example, implementing a data width of eight bits would simplify routing, allow for increased memory density, and potentially improve speed by having fewer devices connected to each data line and reduce the load on each line. Ex. 1003, ¶ 154. A POSITA would also recognize the design benefits of selecting a data width compliant with the JEDEC standard: eight bits. Ex. 1003, ¶ 154; Ex. 1013, p. 4 (showing x8 DRAM with four data lines). *Fourth,* finally, modifying Osanai's memory devices to implement a data width of eight bits would simply arrange old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, and would therefore have been obvious.

5. Claim 5

Claim 5 depends on claim 1 and recites "*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits*." Osanai renders this limitation obvious based on the teachings of Tokuhiro.

As explained above, *see* § V.B.2, Osanai's buffer circuits have a data width of eight bits (Ex. 1005, [0059]), but Osanai's memory devices also have a data width of eight bits (Ex. 1005, [0059]). Osanai explains, however, that the number of "memory chips 200 allocated to a single data register buffer 300 is not limited to a

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particular number"—that is, different data widths were envisioned by Osanai. Ex. 1005, [0196]; Ex. 1003, ¶ 157.

As Dr. Alpert explains, a POSITA would have been motivated to modify Osanai's memory devices to use four bits instead of eight bits for at least four primary reasons. *First*, such a person would have used four bits to comply with the commercial standardization of the DDR3 standard, which specified four bits. Ex. 1003, ¶ 158; Ex. 1013, p. 3 (showing x4 DRAM with four data lines). *Second*, such a person would have been motivated to reduce packaging costs, thereby realizing cost savings on the module. Ex. 1003, ¶ 158; Ex. 1013, p. 3. *Third*, using a data width of four bits would have been a common design tradeoff; for example, implementing a data width of four bits instead of eight bits would simplify routing, allow for increased memory density, and potentially improve speed by having fewer devices connected to each data line and reduce the load on each line. Ex. 1003, ¶ 158. A POSITA would also recognize the design benefits of selecting a data width compliant with the JEDEC standard: four bits. Ex. 1003, ¶ 158; Ex. 1013, p. 3 (showing x4 DRAM with four data lines). *Finally*, modifying Osanai's memory module to implement a data width of four bits would simply arrange old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement, and would therefore have been obvious.

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D. Ground 3: Osanai, Tokuhiro, and Takefman Render Claims 1–5 Obvious

As explained above, *see* §§ V.B and V.C, claim 1 is anticipated by Osanai or rendered obvious over Osanai in view of Tokuhiro. To the extent that Netlist argues that Osanai does not disclose a "tristate buffer," such a feature would have been obvious in view of Takefman. In addition, claims 4-5 are also obvious over Osanai in view of Takefman, with or without Tokuhiro.

1. Claim 1: "Tristate buffer"

To the extent that Netlist argues that Osanai does not disclose a "*tristate buffer*," such a feature would have been obvious. Takefman discloses such a buffer. And a POSITA would have been motivated to incorporate Takefman's buffer into Osanai's "*data paths*."

Takefman's buffer circuits—called Bolt devices 303—include DDR-3 ports that "can be tri-stated" and can signal using "DDR-3 DQ/DQS signaling." Ex. 1007, 6:4–9. Takefman describes the tri-stated Bolt device 303 as follows:

> Each of the Bolt devices include three DDR-3 ports with… each port of the DDR-3 ports can be ***tri-stated*** and can signal using DDR-3 DQ/DQS signaling.

Id. (emphasis added); Ex. 1003. ¶ 162. Accordingly, a POSITA would have understood that Takefman discloses a "*tristate buffer*." *Id.*

Such a person would have been motivated to include Takefman's "*tristate buffers*" in the Osanai's "*data paths*" for three reasons. *First*, modifying Osanai's

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data signal lines to include tristate buffers would mitigate any interference caused by one buffer used in read operations during write operations. Ex. 1003, ¶ 164. *Second*, a POSITA would have understood that tristate buffers allow the output to be sent at a specific time, which is especially important to leveling techniques. *Id*. *Third*, and as Dr. Alpert explains, such a modification would have been a simple substitution for Osanai's buffers. Ex. 1003, ¶ 164; *see* Ex. 1005, [0094]. A POSITA would have recognized that both Osanai's buffers and Takefman's DDR-3 ports operate similarly: both use DDR-3 DQ/DQS signaling for write/read operations. Ex. 1003, ¶ 164; Ex. 1005, [0169], [0176]; Ex. 1007, 6:4–9. Such a modification would not be beyond the skill of a POSITA and would have no unexpected results. Ex. 1003, ¶ 164.

2. Claim 4

Claim 4 depends on claim 1 and recites "*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte*." Osanai renders this limitation obvious in combination based on the teachings of Takefman.

As explained above, Osanai's buffer circuits and memory devices have a data width of eight bits (or 1 byte), (Ex. 1005, [0059]). To the extent that Netlist argues that Osanai's memory devices do not have a data width of eight bits, such a data width would be obvious. Osanai's explains that the number of "memory chips 200

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allocated to a single data register buffer 300 is not limited to a particular number"—that is, different data widths were envisioned by Osanai. Ex. 1005, [0196]; Ex. 1003, ¶ 166.

Takefman discloses multiple memory devices, each having "*a data width of 1 byte*." Ex. 1007, 7:30–40 ("DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8)."). Specifically, Takefman discloses that each DIMM can use DRAMs with "x8" width, which means the DRAM has "*data width of the 1 byte*" or 8 bits. Ex. 1007, 7:30–40 ("DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8)."). A POSITA would have been motivated to modify the data width of Osanai's memory chips 200 to be four bits for the same reasons discussed in Ground 2 above. *See* § V.C.4; Ex. 1003, ¶ 167.

3. Claim 5

Claim 5 depends on claim 1 and recites "*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits*." Osanai renders this limitation obvious based on the teachings of Takefman.

As explained above, Osanai's buffer circuits have a data width of eight bits, but Osanai's memory devices also have a data width of eight bits. Ex. 1005, [0059]. Osanai explains, however, that the number of "memory chips 200 allocated to a

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single data register buffer 300 is not limited to a particular number"—that is, different data widths were envisioned by Osanai. Ex. 1005, [0196]; Ex. 1003, ¶ 169.

One such data width—four bits—is disclosed by Takefman. Ex. 1003, ¶ 170. Specifically, Takefman discloses multiple memory devices, each having "*a data width of 1 byte*." Ex. 1007, 7:30–40 ("DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8)."). Takefman also discloses that each DIMM can use DRAMs with "x4" width, which means the DRAM has a "*data width of 4 bits*." Ex. 1007, 7:30–40 ("DIMM configuration data including the number of ranks of DRAM present and the organization of the DRAM (x4/x8)."). A POSITA would have been motivated to modify the data width of Osanai's memory chips 200 to be four bits for the same reasons discussed in Ground 2 above. *See* § V.C.5; Ex. 1003, ¶ 170.

VI. No Secondary Considerations Exist

As described above, Osanai alone, or in combination with Tokuhiro and/or Takefman, renders the challenged claims obvious. No secondary indicia of non-obviousness exist having a nexus to the putative "invention" of these claims contrary to that conclusion. Petitioners reserves the right to respond to any assertion of secondary indicia of nonobviousness advanced by Patent Owner.

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VII. The Parallel District Court Case Does Not Warrant Denying Institution

When considering a parallel proceeding, the PTAB "balances considerations such as "system efficiency, fairness, and patent quality" using the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). These factors "overlap," and a "holistic view" should be taken. *Id.*, p. 6.

The fourth factor (overlap) strongly favors institution. Petitioners have stipulated that they will not pursue invalidity on the same grounds—or even the same references—if the Board institutes trial in this proceeding. Ex. 1016. Petitioners modeled this stipulation on the stipulation that the Board found to "mitigate any concerns" in *VMware, Inc. v. Intellectual Ventures I LLC*, IPR2020-00470, Paper 13 at 20 (P.T.A.B. August 18, 2020). This fourth factor favors institution here even more so than in *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 (P.T.A.B. June 15, 2020). There, the petitioner provided no stipulation. *Id.* pp. 16-19. Furthermore, this Petition challenges claims 2–4, which are not at issue in the parallel litigation. The claims-at-issue in both proceedings do not overlap and thus another reason that the fourth factor favors institution.

The third factor (investment in parallel proceeding) also favors institution. The district court has not issued any substantive opinions regarding the scope or

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validity of the challenged claims, and given Petitioners' stipulations, the Court is unlikely to invest any resources on the grounds raised in this petition, either before or after the scheduled institution date. In addition, the parallel proceeding is in an early stage and no trial date has been set. Only initial contentions have been exchanged. Ex. 1017, pp. 1-2.

Regarding the sixth factor (merits, other circumstances), the merits strongly favor institution as shown through the strength of the grounds in this petition. Other circumstances also favor institution. Like in *Apple v. SEVEN*, the parallel litigation is complex, involving three patents, 37 asserted claims, and many accused products, and the district court requires reduction of claims pre-trial. *SEVEN*, 21-22; Ex. 1031, 10 (weighing claim reductions). An IPR trial, in contrast, allows a focus on resolving all challenged claims in a single patent, thus "enhanc[ing] the integrity of the patent system." *SEVEN*, 22.

Fintiv factors 1 (stay) and 2 (proximity of trial dates) also favor institution. Petitioners do not know if the district court will stay the case if trial is instituted and the Court has not yet set the trial date. The scheduling order in the related litigation only lists dates up to the *Markman* hearing stage, which is scheduled for March 31, 2021. Ex. 1017, pp. 1-2; *compare Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01007, Paper 15 at 10-13 (P.T.A.B. December 7, 2020) (the "proximity factor in *Fintiv*, on its face, asks us to evaluate our discretion in light of trial dates

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that have been set in parallel litigations, not to speculate as to trial dates that are still to-be-determined"). Without a scheduled trial date, the Board should consider these two factors "weigh[ing] strongly against exercising [PTAB's] discretion to deny [institution]." *See Shure Inc. v. Clearone, Inc.*, PGR2020-00079, Paper 14 at 15–16 (February 16, 2021) ("In any case, unlike in the NHK and Fintiv cases, there is no trial date set in the Illinois case. Thus, this factor weighs strongly against exercising our discretion to deny the Petition."); *Sand Revolution II, LLC v. Cont'l Intermodal Grp–Trucking LLC*, IPR2019-01393, Paper 24 at 8-10 (June 16, 2020) ("Sand") (informative).

For these reasons, the Board should not exercise its discretion to deny institution of this petition.

VIII. The Past IPR Against a Related Patent Does Not Warrant Denying Institution

To the extent Netlist argues the Board should exercise its discretion to deny institution based on the prior *inter partes* review challenge to the '632 parent patent in IPR2017-00730, such a denial would be unwarranted. When considering whether to exercise its discretion under 35 U.S.C. § 314(a), the PTAB may consider seven factors set forth by the Board in *General Plastic Industrial Co., LTD. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2017) (precedential). All factors favor institution or are neutral, as explained below.

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Factor 1 strongly favors institution because IPR2017-00730 involved a different petitioner (SK hynix), a different patent (the '632 patent), and different claims. Moreover, this Petition involves different prior art (*e.g.,* Osanai, Tokuhiro, and Takefman) and a different expert's testimony that were not at issue in IPR2017-00730.

Factors 5 and 6 also favor institution. Factor 5 considers whether Petitioners have an adequate explanation for the time elapsed. That explanation is easily provided here: Petitioners were not involved in IPR2017-00730, nor had Petitioners received notice of the '608 patent until recently in connection with the parallel district court litigation. *See* Ex. 1018. Factor 5 also considers whether the petition is "directed to the same claims of the same patent." This Petition, however, involves a different patent with different claims. For factor 6, the Board has not previously spent any resources considering the issues raised in this petition because this Petition challenges different claims using different prior art. Factor 6 thus favors institution because the Board would not waste its finite resources on arguments previously considered. Therefore, both factors 5 and 6 favor institution.

The remaining factors 2 through 4 and 7 are neutral because Netlist sued Petitioners over three years after the Board issued its final decision in IPR2017-00730. Specifically, Netlist waited until June 15, 2021, to serve its complaint on Petitioners. *See* Ex. 1018. This delay renders factors 2 through 4 neutral because

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any prejudice arose from Netlist's delay in filing suit. Petitioners should not be penalized for such a delay resulting from Netlist waiting years to file suit. Factor 7 is neutral because this Petition would not seem to affect the Board's ability to timely issue a final determination. Accordingly, no remaining factor weighs in favor of denying institution.

For these reasons, the Board should not exercise its discretion to deny institution of this Petition.

IX. Mandatory Notices

A. Real Parties-in-Interest

The named Petitioners are the only entities who are funding and controlling this Petition and are therefore all named as real parties-in-interest. No other entity is funding, controlling, or otherwise has an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

B. Related Proceedings

Netlist asserted the '608 patent against Petitioners in the Western District of Texas, Case No. 6:21-cv-00431. A related patent to the '608 parent, U.S. Patent No. 9,128,632, was at issue in IPR2017-00730. For that IPR, the petitioners were SK hynix Inc., SK hynix America, Inc., and SK hynix Memory Solutions Inc.

This Petition is being filed concurrently with IPR2022-00236, which challenges a parent of the '608 patent which was also asserted in Western District of Texas, Case No. 6:21-cv-00431.

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C. Lead and Backup Counsel

Petitioners' lead and backup counsel are:

Lead Counsel for Petitioner	Backup Counsel for Petitioner
Matthew Hopkins Winston & Strawn LLP 1901 L Street NW Washington, DC 20036 mhopkins@winston.com T: 202.282.5862, F: 202.282.5100 USPTO Reg. No. 76,273	Michael Rueckheim Winston & Strawn LLP 255 Shoreline Dr., Suite 520 Redwood Shores, CA 94065 mrueckheim@winston.com T: 650.858.6500, F: 650.858.6550 (*pro hac vice* to be filed)

D. Electronic Service

Petitioners consent to electronic service at:

Winston-IPR-NetList@winston.com.

X. Fees

The required fee is being paid electronically through PTAB E2E.

XI. Conclusion

Petitioners respectfully request that the Board institute IPR and enter a final written decision finding the challenged claims unpatentable.

Dated: December 23, 2021

Respectfully submitted,

/ *Matthew Hopkins* /
Matthew Hopkins
Winston & Strawn LLP
1901 L Street NW
Washington, DC 20036

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mhopkins@winston.com
T: 202.282.5862, F: 202.282.5100
USPTO Reg. No. 76,273

Lead Counsel for Petition

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CERTIFICATE OF COMPLIANCE

This Petition complies with the word count limits set forth in 37 C.F.R. § 42.24(a)(1)(i), because this Petition contains 13,936 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a)(1) and determined using the word count provided by Microsoft Word, which was used to prepare this Petition.

Dated: December 23, 2021

Respectfully submitted,

/ *Matthew Hopkins* /
Matthew Hopkins
Winston & Strawn LLP
1901 L Street NW
Washington, DC 20036
mhopkins@winston.com
T: 202.282.5862, F: 202.282.5100
USPTO Reg. No. 76,273

Lead Counsel for Petition

CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.105(a), this is to certify that on December 23, 2021, I caused to be served a true and correct copy of the foregoing "**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,268,608**" and Exhibits 1001-1020 by Federal Express on the Patent Owner at the correspondence address of record for U.S. Patent No. 10,268,608:

USCH Law, PC
3790 El Camino Real #1147
Palo Alto CA 94304

A courtesy copy of this Petition and supporting material was also served on litigation counsel for Patent Owner via email:

Paul J. Skiermont
SKIERMONT DERBY LLP
pskiermont@skiermontderby.com

/ *Matthew Hopkins* /
Matthew Hopkins
Winston & Strawn LLP
1901 L Street NW
Washington, DC 20036
mhopkins@winston.com
T: 202.282.5862, F: 202.282.5100
USPTO Reg. No. 76,273

Lead Counsel for Petition