UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC, Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC Defendants.	Civil Case No. 2:22-cv-00203-JRG-RSP **JURY TRIAL DEMANDED**

DEFENDANTS' P.R. 3-3 INVALIDITY CONTENTIONS

Pursuant to Docket Control Order (Dkt. No. 40) and Local Patent Rule 3-3, Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively, "Micron" or "Defendants") hereby provide their Invalidity Contentions, which include the accompanying claim charts concerning U.S. Patent Nos. 10,860,506 ("the '506 patent"), 10,949,339 ("the '339 patent"), 11,016,918 ("the '918 patent"), 11,232,054 ("the '054 patent"), 9,318,160 ("the '160 patent"), and 8,787,060 ("the '060 patent") (collectively, the "Asserted Patents") to Plaintiff Netlist, Inc. ("Plaintiff" or "Netlist").

The citation of prior art herein and the accompanying exhibits are not intended to reflect Defendants' claim construction contentions, which will be disclosed in due course in accordance with the Docket Control Order and may instead reflect Plaintiff's apparent (and potentially erroneous) claim constructions based on its Infringement Contentions.

I. Introduction

As disclosed in its P.R. 3-1 Infringement Contentions served on Defendants, Plaintiff

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asserts the following patents and claims:

Patent	Claims
U.S. Patent No. 10,860,506	**1**, 2, 3, 5, 11, 12, 13, **14**, 15, 16
U.S. Patent No. 10,949,339	**1**, 2, 3, 4, 6, 7, 8, 9, 10, **11**, 12, 13, 14, 15, 16, 17, 18, **19**, 20, 21, 22, 23, 26, **27**, 28, 29, 30, 32, 33, 34, 35
U.S. Patent No. 11,016,918	**1**, 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 15, **16**, 17, 18, 19, 20, 21, 22, **23**, 24, 25, 26, 27, 28, 29, 30
U.S. Patent No. 11,232,054	**1**, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, **16**, 17, 23, **24**, 25, 29, 30
U.S. Patent No. 9,318,160	**1**, 2, 3, 4, 5, 6, 7, 8, 9, 10, **11**, 12, 13, 14, 16, 17, 18, 19, **20**, 21, 23, 24, 25, 26, 27, 28
U.S. Patent No. 8,787,060	**1**, 2, 4, 5

The claims identified above are referenced to as "the Asserted Claims" unless reference is made specifically with respect to particularly identified one or more of the Asserted Patents and/or one or more of the Asserted Claims.

As further detailed in and supported by these Invalidity Contentions, Defendants contend that each of the Asserted Claims is invalid under at least 35 U.S.C. §§ 101, 102, 103, and 112.[1] Defendants reserve the right to prove the invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures pursuant to P.R. 3-3.

II. Amendment / Supplementation

Defendants' Invalidity Contentions pertain to the Asserted Claims as identified in Plaintiff's Infringement Contentions. To the extent the Court later allows Plaintiff to amend its infringement contentions and/or assert one or more claims other than the Asserted Claims, Defendants reserve the right to modify, amend, or supplement these Invalidity Contentions accordingly to, for example, show the invalidity of any such newly Asserted Claims.

[1] References to Title 35 of the United States Code are to statutes prior to amendments under the America Invents Act ("AIA").

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These Invalidity Contentions are based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. A *Markman* Order in this case has not yet been issued, and in no way shall these Invalidity Contentions be taken as any admission or acquiescence by Defendants as to the proper scope of the Asserted Claims and/or proper claim constructions of terms and phrases recited in those claims. By identifying prior art that anticipates and/or renders obvious the Asserted Claims, Defendants do not admit that the claim limitations are capable of construction, do not admit that any claim limitations are supported with an appropriate written description and enabling disclosure in the applicable patent specifications, and do not adopt Plaintiff's apparent claim constructions or admit the accuracy of any particular claim construction.[2] Defendants reserve all rights to later challenge or oppose any claim constructions advanced by Plaintiff and to present their own claim construction positions.

Defendants further reserve the right to revise these Invalidity Contentions in view of the Court's construction of terms and phrases recited in one or more of the Asserted Claims, additional information obtained during discovery, additional infringement theories put forth by Plaintiff during fact and/or expert discovery, any findings as to the priority date(s) of the Asserted Claims, and/or positions that Plaintiff, its fact witnesses, or its expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

Defendants further reserve the right to supplement their accompanying P.R. 3-4(b)

[2] Defendants do not concede that Plaintiff's apparent interpretation of the claims is correct, but rather assert the well-established principle that whatever infringes a claim if later in time anticipates if earlier in time. *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001). Thus, where Plaintiff for purposes of its infringement case alleges that a feature of an accused product meets a particular limitation recited in one or more of the Asserted Claims, then that feature, should it be found in the prior art, would also cause that limitation to be met for invalidity purposes.

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document production should they later discover additional prior art documents, information, testimony, prior art systems and related documentation, and/or software or hardware code, including information provided by third parties after the date of service of these Invalidity Contentions.

Defendants may further rely on inventor admissions concerning the scope or state of the prior art relevant to the Asserted Claims, the patent prosecution histories of the Asserted Patents, related patents and/or patent applications, any deposition or trial testimony of the named inventors on the Asserted Patents, and the papers filed and any evidence produced or submitted by Plaintiff in connection with these cases or other related litigation. Defendants reserve the right to contend that one or more of the Asserted Claims are invalid under 35 U.S.C. § 102(f) in the event Defendants obtain evidence that one or more of the named inventors did not invent the subject matter in the Asserted Claims.

Prior art not included in these Invalidity Contentions, whether known or not known to Defendants, may become relevant. In particular, Defendants are currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified in these Invalidity Contentions. Accordingly, Defendants reserve the right to identify other references that would disclose the allegedly missing limitation(s) of the claimed method, device, or system.

The references identified in these Invalidity Contentions, which include the attached claim charts, may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame.

References identified in these Invalidity Contentions, as well as the "References Cited" on the face of the Asserted Patents and the patents cited within the body of the Asserted Patents,

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may be used to illustrate, but not limit the scope of, the state of the art to which the Asserted Patents pertain (i.e., at a time prior to the date of alleged inventions of the Asserted Claims of the Asserted Patents). Moreover, Defendants reserve the ability to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the Asserted Patents.

Because discovery has just recently begun, Defendants anticipate that additional prior art and invalidity bases may be found. Defendants' investigation and analysis of the prior art is continuing, and thus Defendants reserve the right to supplement, amend, and/or revise the information provided herein as Defendants conduct further investigation and/or analysis, including identifying, charting, and relying on additional references.

Additionally, in view of likely third-party discovery that will be taken, Defendants reserve the right to present additional items of prior art under 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and/or § 103 located during discovery or further investigation, and to assert contentions of invalidity under 35 U.S.C. §§ 102(c), (d), or (f). For example, Defendants expect to issue subpoenas to third parties believed to have knowledge, documents, and/or other evidence concerning invalidity of one or more of the Asserted Claims.

In addition to the positions and prior art identified in these Invalidity Contentions (including the accompanying invalidity claim charts), Defendants also incorporate by reference all invalidity contentions, prior art,[3] and invalidity claim charts (including, without limitation, all anticipation positions, obviousness positions (including all prior art combinations and motivations to combine), indefiniteness positions, written description positions, and non-enablement positions) concerning one or more of the Asserted Patents, as disclosed at any time.

[3] Prior art appearing in the file histories of the Asserted Patents is not required to be separately produced by Defendants under P.R. 3-4(b).

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This includes without limitation disclosures in previous or related litigation, in United States Patent & Trademark Office ("USPTO") proceedings, by the Plaintiff, or by the named inventors or any individuals associated with the prosecution and/or post-grant review of the Asserted Patents.

Specifically, for example, Defendants identify, as prior art upon which they may rely to show the invalidity of the Asserted Claims, the prior art references disclosed by parties in any other litigation involving one or more of the Asserted Patents, any patent related to any of the Asserted Patents, and/or any other patent allegedly assigned to Netlist claiming priority to the Asserted Patents (collectively, "Other Netlist Proceedings").

Plaintiff has a duty to produce to Defendants all relevant documents from the Other Netlist Proceedings including but not limited to all prior art, invalidity contentions, and expert reports on invalidity (among other relevant items).

Defendants reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any relevant discovery provided by third parties, Plaintiff, opening or rebuttal expert reports, fact or expert depositions, or in response to any claim construction ruling(s) issued by this Court (regardless of how and when such ruling is made). Defendants also reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any rebuttal evidence disclosed by Plaintiff or as otherwise may be necessary or appropriate under the circumstances.

III. P.R. 3-3(a) – Identification of Prior Art

Pursuant to P.R. 3-3(a), and subject to Defendants' reservation of rights, Defendants identify each item of prior art that anticipates or renders obvious the Asserted Claims below.[4] In

[4] Defendants' disclosure of prior art is premised on the alleged priority dates of the Asserted

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addition to the prior art identified below and in the attached exhibits, Defendants incorporate by reference all prior art, exhibits, and detailed explanation in the petitions of how the Asserted Claims are obvious or anticipated by prior artas described in at least the following *inter partes* review proceedings pending before the United States Patent and Trademark Office: IPR2022-00639, IPR2022-00711, IPR2022-00999, IPR2022-00996, IPR2022-01428, IPR2022-01427, IPR2023-00203, IPR2023-00204, and IPR2023-00205.

A. U.S. Patent No. 10,860,506

Invalidity claim charts identifying disclosures in the references identified in Tables 1-A, 2-A, 3-A, and 4-A as to the Asserted Claims of the '506 patent are provided in attached Exhibits A1 through A23.

Table 1-A: Prior Art Patents and Printed Publications for the '506 patent

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RA-1	Asserted Patent's Admitted Prior Art (APA)		
RA-2	U.S. Patent App. Pub. No. 2010/0312956 (Hirashi)	Dec. 9, 2010	June 3, 2010
RA-3	U.S. Patent App. Pub. No. 2007/0008791 (Butt)	Jan. 11, 2007	July 7, 2005
RA-4	U.S. Patent No. 8,020,022 (Tokuhiro)	Sept. 13, 2011	Sept. 12, 2008
RA-5	U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry)	Dec. 7, 2006	June 1, 2005
RA-6	U.S. Patent No. 7,024,518 (Halbert)	April 4, 2006	Mar. 13, 2002

Patents as identified in Plaintiff's infringement contentions. Defendants contend Plaintiff is not entitled to the alleged priority dates and reserve the right to modify, amend, or supplement their invalidity contentions with additional prior art references if any Asserted Claim is shown to not be entitled to the respective alleged priority date or if Plaintiff alleges any other priority date for any of the Asserted Claims. Notwithstanding that reservation of rights, Defendants also reserve the right to argue that they have been unduly prejudiced should Plaintiff allege a different priority date for any of the Asserted Claims, and that accordingly Plaintiff should not be allowed to do so.

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Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RA-7	U.S. Patent No. 7,289,386 (Bhakta)	Oct. 30, 2007	July 1, 2005
RA-8	U.S. Patent No. 8,391,089 (Chen)	March 5, 2013	Mar. 5, 2010
RA-9	U.S. Patent No. 8,111,565 (Kuroki)	Feb. 7, 2012	Sept. 29, 2009
RA-10	JEDEC FBDIMM Standards	March 2007	
RA-11	JEDEC SDRAM/DIMM Standards	January 2022, November 2008	
RA-12	U.S. Patent No. 8,001,434 (Lee)	Aug. 16, 2011	Apr. 13, 2009
RA-30	Shabana Aqueel & Kavita Khare, "A High Performance DDR3 SDRAM Controller," Vol. 1, Issue 1, International Journal of Electronics and Electrical Engineering (Aqueel)	July 2012	
RA-31	Young-Chan Jang, "A Self-Calibrating Per-Pin Phase Adjuster for Source Synchronous Double Data Rate Signaling in Parallel Interface," Vol. E94-A, No. 2, IEICE Trans. Fundamentals (Jang)	February 2011	
RA-32	Jang-Woo Lee et al., "Inter-Pin Skew Compensation Scheme for 3.2-Gb/s/pin Parallel Interface," Vol. 10, No. 1, Journal of Semiconductor Technology and Science (Jang-Woo Lee)	March 2010	
RA-33	A. Alexandropoulos et al., "A novel 1.8 V, 1066 Mbps, DDR2, DFI-compatible, Memory Interface," 2010 IEEE Annual Symposium on VLSI, 387 (Alexandropoulos)	2010	
RA-34	Moon-Sang Hwang et al., "27.3: 1.2 Gbps GDDR3 Physical Layer for 3D AMOLED Panel," SID 11 DIGEST (Hwang)	2011	
RA-35	U.S. Patent No. 7,562,271 (Shaeffer)	July 14, 2009	Apr. 6, 2007
RA-36	U.S. Patent No. 9,361,955 (Muralimanohar)		Jan. 27, 2011/ Jan. 28, 2010 (prov)
RA-37	U.S. Patent No. 8,806,116 (Karamcheti)	Aug. 20, 2009	Feb. 11, 2009/ Feb. 12, 2008 (prov)
RA-38	U.S. Patent no. 7,181,584 (LaBerge)	Feb. 20, 2007	Feb. 5, 2004
RA-39	U.S. Patent no. 7,861,043 (Uchida)	Dec. 28, 2010	Feb. 9, 2006

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RA-40	U.S. Patent no. 9,195,602 (Hampel)	May 6, 2010	Mar. 19, 2008/ Mar. 30, 2007 (prov.)

Table 2-A: Prior Art Systems and Inventions for the ’506 patent

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RA-13	SK hynix 178ball FBGA System (SK Hynix FBGA)	At least as early as July 2012
RA-14	Elpida DDR3 SDRAM System (Elpida DDR3 SDRAM)	At least as early as March 2009
RA-15	JEDEC Proposals and Minutes regarding FBDIMM (JEDEC FBDIMM Proposals)	At least as early as October 2004, May 2006, June 2006, August 2007, March 2008
RA-16	JEDEC Proposals and Minutes regarding SDRAM/DIMM (JEDEC SDRAM/DIMM Proposals)	At least as early as November 2010, March 2011, June 2011, August 2011, September 2011, March 2012
RA-17	Lattice Semiconductor DDR3 System (Lattice DDR3)	At least as early as March 2010
RA-18	NXP DDR System (NXP DDR)	At least as early as June 2010
RA-19	Kentron’s Quad Band Memory System (QBM)	At least as early as 1999-2005
RA-20	SDRAM Controller for the MORPHEUS Reconfigurable Architecture (MORPHEUS SDRAM Controller)	At least as early as April 2008
RA-21	Altera External Memory Interface System, as described in "ALTDLL and ALTDQ_DQS Megafunctions User Guide" (Altera 1)	At least as early as February 2012
RA-22	Altera External Memory Interface System, as described in "External Memory Interface Handbook, Volume 4: Simulation, Timing Analysis, and Debugging" (Altera 2)	At least as early as June 2011
RA-23	Altera External Memory Interface System, as described	At least as early as March

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Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
	in "External Memory Interfaces in HardCopy IV Devices" (Altera 3)	2012
RA-24	Altera External Memory Interface System, as described in "Challenges in Implementing DDR3 Memory Interface on PCB Systems - A Methodology for Interfacing DDR3 SDRAM DIMM to an FPGA" (Altera 4)	At least as early as 2008
RA-25	DFi DDR PHY Interface System, as described in "DDR PHY Interface (DFI) Specification" (DFi DDR PHY 1)	At least as early as January 2009
RA-26	DFi DDR PHY Interface System, as described in "DFI 3.0 Specification" (DFi DDR PHY 2)	At least as early as May 2012
RA-27	NXP MSC8152 System, as described in "MSC8152 Reference Manual" (NXP MSC8152)	At least as early as June 2011
RA-28	Xilinx Processing System, as described in "Zynq-7000 Extensible Processing Platform: Technical Reference Manual" (Xilinx 1)	At least as early as May 2012
RA-29	Xilinx Processing System, "Implementing High-Performance Interfaces with Virtex-4 FPGAs" (Xilinx 2)	At least as early as January 2006

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- SK hynix America Inc.'s 178ball FBGA System
- Micron Technology, Inc.'s Elpida DDR3 SDRAM System

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- Lattice Semiconductor Corp.'s DDR3 System
- NXP Semiconductors's Freescale Semiconductor DDR System
- Kentron's Quad Band Memory System
- Institut für Technik der Informationsverarbeitung (ITIV), University of Karlsruhe's SDRAM Controller for the MORPHEUS Reconfigurable Architecture

Discovery is ongoing, and Defendants may serve other third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to memory modules:

- U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) at Fig. 1, [0010], and [0011].
- U.S. Patent App. Pub. No. 2007/0008791 (Butt) at Fig. 1, Fig. 2, [0003], [0005], [0015], and [0017].
- U.S. Patent No. 8,020,022 (Tokuhiro) at Fig. 4, 3:16-43, and 4:62-5:30.
- U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) at Fig. 2, [0002], [0010], [0011], and [0012].
- U.S. Patent No. 7,024,518 (Halbert) at Fig. 4., 3:42-4:8, and 4:36-5:65.
- U.S. Patent No. 7,289,386 (Bhakta) at Fig.1, Fig. 2, Fig. 3, and 2:46-3:30.
- U.S. Patent No. 8,391,089 (Chen) at Fig. 4, 1:22-2:6, 4:3-30, and 5:4-52.
- U.S. Patent No. 8,111,565 (Kuroki) at Fig. 4B, 1:4-33, and 2:52-3:48.
- SK Hynix 178ball FBGA System at page 11 and page 128.
- Elpida DDR3 SDRAM System at page 12, page 13, and page 15.

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- Lattice Semiconductor DDR3 System at Fig. 1, Fig. 2, page 2, and page 4.
- NXP DDR System at page 33, page 35, and page 36.
- Kentron Technologies Inc.'s Quad Band Memory System, QBM Specification Rev. 0.93 at page 6 and page 9.
- SDRAM Controller for the MORPHEUS Reconfigurable Architecture at Fig. 1, Fig. 3, page 1, and page 5.
- U.S. Patent No. 7,562,271 B2 (Shaeffer) at Fig. 5, 3:26–39, 4:18–42, 5:11–20, 9:29–51.
- U.S. Patent No. 9,361,955 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 24:23–44.
- U.S. Patent No. 8,806,116 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.

Each of these references show that the concept of implementing delays in memory modules is not novel and was well-known for many years. In light of the references discussed herein, the Asserted Claims of the '506 patent cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needed to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '506 patent. Defendants'

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investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '506 patent. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '506 patent. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants' possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 3-A provides additional bases for invalidity of the '506 patent under pre-AIA 35

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U.S.C. § 102(f), on the grounds that the inventors of the '506 patent did not themselves invent the subject matter claimed in the '506 patent. The prior art under § 102(f) is identified in Table 3 by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 3-A: Prior Art under pre-AIA § 102(f) for the '506 patent

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RA-19	Quad Band Memory (QBM) System ("*QBM*")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RA-15	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology Corporation • One or more employees of Staktek Corporation
RA-16	Proposals and disclosures made at JEDEC committee meetings during the time period 2010-2012 ("*JEDEC SDRAM/DIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc. • One or more employees of Inphi Corporation

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and

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developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the July 27, 2012 alleged priority date of the '506 patent. During this time period, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873.[5] The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47; SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and derived the claimed subject matter of the '506 patent from the QBM features. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM-NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '506 patent is provided in attached Exhibit A18.

JEDEC Proposals

Hyun Lee – an inventor of the '506 patent – regularly attended JEDEC meetings for at least the JC-40 committee and the JC-45 committee in 2011 and 2012, as well as before and after that timeframe, and before the alleged July 27, 2012 priority date of the '506 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those committees,

[5] Defendants, via subpoena, obtained the infringement contentions and prior art used in Samsung's invalidity contentions against the same Asserted Claims involved *in Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, 2:21-cv-00463-JRG (E.D. Tex.). These contentions refer to the Bates number for documents that Samsung has already produced to Netlist in that case.

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including JESD82-32, dated November 2016, as well as prior drafts of it. For example, Intel presented and discussed Committee Item Number 158.01 ("DDR4 LRDIMM Proposal") at the December 8, 2011 meeting of JC-40, Committee Item Number 0311.14 ("Proposed DDR4 DB Training Modes") at the March 25, 2012 meeting of JC-40, and Committee Item Number 0311.12 ("Proposed DDR DB Buffer Control Words") at the June 4, 2012 meeting of JC-40, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, each of the draft DDR4 LRDIMM drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '506 patent.

After attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and drafted the provisional application to which the '506 patent claims priority, and which Micron has reason to believe contained a significant amount of material Hyun Lee and Netlist learned at JEDEC. Hyun Lee filed the provisional application on July 27, 2012, naming himself as the inventor.

Table 4 below provides additional bases for invalidity of the '506 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the '506 patent was made in this country before the alleged invention date of the '506 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 4 by the name of the person(s) or entities involved in the making of the invention before the applicants of the '506 patent. The circumstances surrounding the making of the invention before

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the applicants of the '506 patent are explained below.

Table 4-A: Prior Art under pre-AIA § 102(g)(2) for the '506 patent

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RA-19	Quad Band Memory (QBM) System ("*QBM*")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RA-15	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology Corporation • One or more employees of Staktek Corporation
RA-16	Proposals and disclosures made at JEDEC committee meetings during the time period 2010-2012 ("*JEDEC SDRAM/DIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc. • One or more employees of Inphi Corporation

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the

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July 27, 2012 alleged priority date of the '506 patent. During this time, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47, SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and used the technical features of the QBM system to draft the provisional application to which the '506 patent claims priority as well as the claims of the '506 patent. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM-NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '506 patent is provided in attached Exhibit A18. Kentron did not abandon, suppress, or conceal its invention of QBM. Kentron presented the technical features of QBM to JEDEC, described the features in newsletters to its QBM Alliance members, and filed patents covering the technology. *See, e.g.*, SAM-NET00313593-615, SAM-NET00315870- 900, SAM-NET00315171-87, SAM-NET00313434.

JEDEC Proposals

Hyun Lee – an inventor of the '506 patent – regularly attended JEDEC meetings for at least the JC-40 committee and the JC-45 committee in 2011 and 2012, as well as before and after that timeframe, and before the alleged July 27, 2012 priority date of the '506 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those committees, including JESD82-32, dated November 2016,

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as well as prior drafts of it. For example, Intel presented and discussed Committee Item Number 158.01 ("DDR4 LRDIMM Proposal") at the December 8, 2011 meeting of JC-40, Committee Item Number 0311.14 ("Proposed DDR4 DB Training Modes") at the March 25, 2012 meeting of JC-40, and Committee Item Number 0311.12 ("Proposed DDR DB Buffer Control Words") at the June 4, 2012 meeting of JC-40, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Therefore, they were not abandoned, suppressed, or concealed. Based on Netlist's apparent view of the scope of the alleged invention, each of the draft DDR4 LRDIMM drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '506 patent.

After attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and drafted the provisional application to which the '506 patent claims priority, and which Micron has reason to believe contained a significant amount of material Hyun Lee and Netlist learned at JEDEC. Hyun Lee filed the provisional application on July 27, 2012, naming himself as the inventor.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

B. U.S. Patent No. 10,949,339

Invalidity claim charts identifying disclosures in the references identified in Tables 1-B, 2-B, 3-B, and 4-B to the Asserted Claims of the '339 patent are provided in attached Exhibits B1 through B25.

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Table 1-B: Prior Art Patents and Printed Publications for the '339 patent

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RB-1	Asserted Patent's Admitted Prior Art (APA)		
RB-2	U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry)	Dec. 7, 2006	June 1, 2005
RB-3	U.S. Patent No. 7,024,518 (Halbert)	April 4, 2006	Mar. 13, 2002
RB-4	U.S. Patent No. 7,532,537 (Solomon)	May 12, 2009	June 19, 2006
RB-5	U.S. Patent No. 6,530,033 (Raynham)	March 4, 2003	Oct. 28, 1999
RB-6	U.S. Patent No. 6,947,304 (Yen)	Sept. 20, 2005	May 12, 2003
RB-7	U.S. Patent App. Pub. No. 2008/0028135 (Rajan)	Jan. 31, 2008	Jan. 31, 2008
RB-8	U.S. Patent No. 6,972,981 (Ruckerbauer)	Dec. 6, 2005	July 30, 2004
RB-9	U.S. Patent No. 7,389,375 (Gower 375)	June 17, 2008	July 30, 2004
RB-10	U.S. Patent No. 7,512,762 (Gower 762)	March 31, 2009	Oct. 29, 2004
RB-11	U.S. Patent No. 7,395,476 (Cowell)	July 1, 2008	Oct. 29, 2004
RB-12	U.S. Patent No. 6,714,433 (Doblar)	March 30, 2004	June 15, 2001
RB-13	U.S. Patent No. 7,289,386 (Bhakta)	Oct. 30, 2007	Oct. 30, 2007
RB-14	JEDEC SDRAM/DIMM Standards	June 2000, January 2002, January 2004, January 2005, November 2008	
RB-15	JEDEC FBDIMM Standards	March 2007	

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Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RB-16	U.S. Patent No. 8,001,434 (Lee)	Aug. 16, 2011	Apr. 13, 2009
RB-25	Hongzhong Zheng et al., "Mini-Rank: Adaptive DRAM Architecture for Improving Memory Power Efficiency," IEEE (Hongzhong Zheng)	2008	
RB-26	U.S. Patent App. Pub. No. 2009/0210616 (Karamcheti)	Aug. 20, 2009	Feb. 11, 2009
RB-27	U.S. Patent App. Pub. No. 2008/0080261 (Shaeffer)	Apr. 3, 2008	Apr. 6, 2007

Table 2-B: Prior Art Systems and Inventions for the '339 patent

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RB-17	JEDEC Proposals and Minutes regarding SDRAM/DIMM (JEDEC SDRAM/DIMM Proposals)	At least as early as May 2008, December 2008, February 2009
RB-18	JEDEC Proposals and Minutes regarding FBDIMM (JEDEC FBDIMM Proposals)	At least as early as October 2004, May 2006, June 2006, August 2007, March 2008
RB-19	Micron DDR2 SDRAM FBDIMM	At least as early as December 2009
RB-20	IBM Z990 eServer	At least as early as May-July 2004
RB-21	Kentron's Quad Band Memory System (QBM)	At least as early as 1999-2005
RB-22	Samsung DDR3 SDRAM	At least as early as April 2009
RB-23	Samsung DDR2 FBDIMM	At least as early as January 2008
RB-24	Kingston Fully Buffered DIMM System, as described in "Fully Buffered DIMM FAQ" (Kingston FBDIMM)	At least as early as 2006

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user

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manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- International Business Machines Corp. (IBM)'s Z990 eServer
- Kentron Technologies Inc.'s Quad Band Memory System (QBM)

Discovery is ongoing, and Defendants may serve third parties with document subpoenas.

One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to memory modules:

- U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) at Fig. 2, [0002], [0010], [0011], and [0012].
- U.S. Patent No. 7,024,518 (Halbert) at Fig. 4, 3:43-4:8, and 4:36-5:65.
- U.S. Patent No. 7,532,537 (Solomon) at Fig. 1, Fig. 9A, 2:62-3:34, and 4:56- 5:2.
- U.S. Patent No. 6,530,033 (Raynham) at Fig. 4A 5:37-6:24, and 7:33-8:11.
- U.S. Patent No. 6,947,304 (Yen) at Fig. 5, 3:22-42, and 4:37-64.
- U.S. Patent App. Pub. No. 2008/0028135 (Rajan) at Fig. 2B, Fig. 3, [0017], [0074], and [0075].
- U.S. Patent No. 6,972,981 (Ruckerbauer) at Fig. 2, 3:50-66, and 4:45-57.

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- U.S. Patent No. 7,389,375 (Gower 375) at Fig. 10, Fig. 11, Fig 12, 2:40-3:13, and 5:38-58.
- U.S. Patent No. 7,512,762 (Gower 762) at Fig. 10, 2:59-3:26, and 5:41-6:22.
- U.S. Patent No. 7,395,476 (Cowell) at Fig. 10, Fig. 11, 3:3-38, and 6:21-54.
- U.S. Patent No. 6,714,433 (Doblar) at Fig. 2, 2:66-3:17, and 6:12-34.
- U.S. Patent No. 7,289,386 (Bhakta) at at Fig.1, Fig. 2, Fig. 3, and 2:46-3:30.
- Micron DDR2 SDRAM FBDIMM at Fig. 2, Fig. 3, Fig. 4, page 1, and page 7.
- IBM's Z990 eServer at Fig. 3, Fig. 4, Fig 11, page 370, and page 372.
- Kentron's Quad Band Memory System (QBM), QBM Specification Rev. 0.93 at page 6 and page 9.
- Samsung Electronics Co., Ltd.'s DDR3 SDRAM.
- Samsung Electronics Co., Ltd.'s DDR2 FBDIMM.
- Micron Technology, Inc.'s DDR2 FBDIMM.
- U.S. Patent App. Pub. No. 2008/0080261 at FIGS. 5-8, 9A-C, 10, 16, 17, 18, 27-30, 36-39 and related disclosures.
- U.S. Patent App. Pub. No. 2009/0210616 at FIGS. 1-5 and related disclosures.

Each of these references show that the concept of controlling the transmission of data signals is not novel. In light of the references discussed herein, the Asserted Claims of the '339 patent cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needed to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these

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contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '339 patent. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '339 patent. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '339 patent. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants' possession, custody, or control available for inspection by Plaintiff.

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Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 3-A provides additional bases for invalidity of the '339 patent under pre-AIA 35 U.S.C. § 102(f), on the grounds that the inventors of the '339 patent did not themselves invent the subject matter claimed in the '339 patent. The prior art under § 102(f) is identified in Table 3 by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 3-B: Prior Art under pre-AIA § 102(f) for the '339 patent

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RB-21	Quad Band Memory (QBM) System ("*QBM*")	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RB-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 ("*JEDEC FBDIMM Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology Corporation • One or more employees of Staktek Corporation
RB-17	Proposals and disclosures made at JEDEC committee meetings during the time period 2008-2009 ("JEDEC SDRAM/DIMM Proposals")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc.

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Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
		• One or more employees of Inphi Corporation • One or more employees of Qimonda • One or more employees of FormFactor Inc.

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the July 16, 2009 alleged priority date of the '339 patent. During this time period, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47; SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and derived the claimed subject matter of the '339 patent from the QBM features. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM-NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '339 patent is provided in attached Exhibit B20.

JEDEC Proposals

During the time period from at least 2005 to 2012, Netlist regularly attended JEDEC meetings for at least the JC-40 and JC-45 committees, including meetings that occurred before

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the July 16, 2009 alleged priority date of the '339 patent. See, e.g., SAM-NET00005551-75; SAM-NET00008503-51; SAM-NET00008664-8700; SAM-NET00008847-67; SAM-NET00019805-18; SAM-NET00020197-98; SAM-NET00023999-24003; SAM-NET00026641-95; SAM-NET00026696-715; SAM-NET00040933-87; SAM-NET00040988-41007; SAM-NET00048535-608; SAM-NET00052084-131; SAM-NET00052132-50; SAM-NET00052917-20; SAM-NET00060465-532; SAM-NET00071314-88; SAM-NET00092148-53; SAM-NET00113524-54; SAM-NET00113555-67.

By virtue of Netlist's attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Netlist was aware of the proposals and drafts being considered and voted upon by those committees. The proposals, drafts, ballots and presentations distributed to the members of the JEDEC committees were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, the proposals, drafts, and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '339 patent.

After attending these meetings and listening to these ideas from other members of JEDEC, Netlist drafted the application to which the '339 patent claims priority, which Micron has reason to believe contained a significant amount of material Netlist learned at JEDEC.

Table 4 below provides additional bases for invalidity of the '339 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the '339 patent was made in this country before the alleged invention date of the '339 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 4 by the name of the person(s) or entities involved in the making of the invention before the

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applicants of the ’339 patent. The circumstances surrounding the making of the invention before the applicants of the ’506 patent are explained below.

Table 4-B: Prior Art under pre-AIA § 102(g)(2) for the ’339 patent

Ex.	Prior Art Disclosing Technical Features	Person(s)/Entity(ies) Involved
RB-21	Quad Band Memory (QBM) System (“QBM”)	Kentron Technologies Inc. employee(s) (*e.g.*, Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
RB-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2004-2008 (“*JEDEC FBDIMM Proposals*”)	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Qimonda • One or more employees of Nanya Technology • One or more employees of Staktek Corp
RB-17	Proposals and disclosures made at JEDEC committee meetings during the time period 2008-2009 (“JEDEC SDRAM/DIMM Proposals”)	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-40 and JC-45 committee meetings). For example: • One or more employees of Intel Corp. • One or more employees of Elpida Memory, Inc. • One or more employees of Inphi Corporation • One or more employees of Qimonda • One or more employees of FormFactor Inc.
RB-16	U.S. Patent No. 8,001,434 to Lee et al. (Lee), filed on Apr. 13, 2009, and issued on Aug. 16, 2011	Hyun Lee, Jayesh R. Bhakta, Soonju Choi

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QBM

Between at least 1999 and 2005, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory (*QBM*) technology, well before the July 16, 2009 alleged priority date of the '339 patent. During this time, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See*, *e.g.*, SAM-NET00315873. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, SAM-NET00315870-900, SAM-NET00315912. Netlist became a QBM Alliance member in February 2002. *See*, *e.g.*, SAM-NET00315845-47; SAM-NET00315874-81. Because Netlist was a QBM Alliance member, Micron has reason to believe that Netlist knew about the technical features of the QBM system and used the technical features of the QBM system to draft the claims of the '506 patent. The technical features of QBM are shown in the following documents: SAM-NET00314833 - SAM- NET00315913. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '506 patent is provided in attached Exhibit B20. Kentron did not abandon, suppress, or conceal its invention of QBM. Kentron presented the technical features of QBM to JEDEC, described the features in newsletters to its QBM Alliance members, and filed patents covering the technology. *See, e.g.*, SAM-NET00313593-615, SAM- NET00315870-900, SAM-NET00315171-87, SAM-NET00313434.

JEDEC Proposals

During the time period from at least 2005 to 2012, Netlist regularly attended JEDEC meetings for at least the JC-40 and JC-45 committees, including meetings that occurred before the July 16, 2009 alleged priority date of the '339 patent. *See, e.g.,* SAM-NET00005551-75; SAM-NET00008503-51; SAM-NET00008664-8700; SAM-NET00008847-67; SAM-

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NET00019805-18; SAM-NET00020197-98; SAM-NET00023999-24003; SAM-NET00026641-95; SAM-NET00026696-715; SAM-NET00040933-87; SAM-NET00040988-41007; SAM-NET00048535-608; SAM-NET00052084-131; SAM-NET00052132-50; SAM-NET00052917-20; SAM-NET00060465-532; SAM-NET00071314-88; SAM-NET00092148-53; SAM-NET00113524-54; SAM-NET00113555-67.

By virtue of Netlist's attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Micron has reason to believe that Netlist was aware of the proposals and drafts being considered and voted upon by those committees. The proposals, drafts, ballots and presentations distributed to the members of the JEDEC committees were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, the proposals, drafts, and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '339 patent.

After attending these meetings and listening to these ideas from other members of JEDEC, Netlist drafted the application, which Micron has reason to believe contained a significant amount of material Netlist learned at JEDEC.

Lee

Netlist alleges that the '339 patent is entitled to a July 16, 2009 priority date. And yet, three months prior, on April 13, 2009, U.S. Patent No. 8,001,434 to Lee et al. (*Lee*) was filed, disclosing the claimed elements of the '339 patent. While the '339 patent lists Hyun Lee and Jayesh R. Bhakta as inventors, the *Lee* patent lists Hyun Lee, Jayesh R. Bhakta, and Soonju Choi. As such, the inventive entity of the '339 patent differs from the *Lee* patent, therefore the alleged invention of the '339 patent was "made in this country" by "another inventor" under 35

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U.S.C. § 102(g)(2). Given that the inventors of *Lee* filed a patent, they did not abandon, suppress, or conceal their invention.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

C. U.S. Patent Nos. 11,016,918 and 11,232,054

Invalidity claim charts identifying disclosures in the references identified in Tables 1-C and 2-C as to the Asserted Claims of the '918 and '054 patents are provided in attached Exhibits C1 through C13 ('918 Patent) and Exhibits D1 through D13 ('054 Patent).

Table 1-C: Prior Art Patents and Printed Publications for the '918 and '054 patents

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RC-1	Asserted Patents Admitted Prior Art (APA)		
RC-2	U.S. Patent Publication No. 2006/0174140 (Harris)	8/3/2006	1/31/2005
RC-3	U.S. Patent Publication No. 2006/0080515 (Spiers)	4/13/2006	10/12/2004
RC-4	U.S. Patent No. 8,189,328 (Kanapathippillai)	5/28/2012	10/22/2007
RC-5	U.S. Patent No. 6,707,724 (Kim)	3/16/2004	2/6/2002
RC-6	JP11-073762 (Okimoto)	3/16/1999	8/28/1997
RC-7	JEDEC Standards	At least as early as June 2000	
RC-8	JP2006-156814 (Ootani)	6/15/2006	11/30/2004
RC-9	Samsung DDR2 Fully Buffered DIMM	11/2006	
RC-10	*A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi)	09/2006	
RC-11	Maxim MAX1917 Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies (MAX1917)	06/2002	
RC-12	*Central Power Management Unit as Portable Power Management Architecture Based on True Digital*	2004	

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Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
	Control (Byoun)		
RC-13	JP2002083872A (Ito)	01/29/2004	
RC-14	U.S. Patent No. 7,724,604 (Amidi)	05/25/2010	10/25/2006
RC-15	U.S. Patent No. 6,856,556 (Hajeck)	02/15/2005	04/03/2003
RC-16	U.S. Patent No. 6,670,234 (Hsu)	12/30/2003	06/22/2001
RC-17	U.S. Patent No. 8,316,074 (McManis)	11/20/2012	03/11/2005
RC-20	*The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller)	2006	
RC-21	SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT)	2006	

Table 2-C: Prior Art Systems and Inventions for the '918 and '054 patents

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RC-7	JEDEC Standards	At least as early as June 2000
RC-18	TPS65023	At least as early as June 2006
RC-19	IRU3048	At least as early as September 2002

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- JEDEC Standards

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- Samsung DDR2 Fully Buffered DIMM
- Infineon Technology Americas Corporation's Rectifier (e.g., IRU3048)
- Micron Technology, Inc.'s DDR2 SDRAM FBDIMM (e.g., MT36HTS51272F, 2006)
- Micron Technology, Inc.'s Elpida 512MB Fully Buffered DIMM (e.g., EBE51FD8AGFD/EBE51FD8AGFN, 2006)
- SK hynix America Inc.'s 240pin Fully Buffered DDR2 SDRAM DIMMs
- Texas Instruments Inc.'s TPS65023

Discovery is ongoing, and Defendants may serve these and other third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as examples of evidence of the state of the art as it relates to memory module devices:

- U.S. Patent Publication No. 2006/0174140 (Harris) at [0002] and [0009].
- U.S. Patent Publication No. 2006/0080515 (Spiers) at Fig. 5 and [0037].
- U.S. Patent No. 8,189,328 (Kanapathippillai) at Fig. 1a and 2:55-3:38.
- U.S. Patent No. 6,707,724 (Kim) at Fig 1, Fig. 9, 1:21-45, and 5:56-6:19.
- JP11-073762 (Okimoto) at Fig., 1, [0002], [0021], and [0022].
- JP2006-156814 (Ootani) at Fig. 1, Fig. 9, [0001], [0011], [0021], and [0024].
- Samsung DDR2 Fully Buffered DIMM.
- TPS65023 at page 1.
- IRU3048 at Fig. 2 and page 5.

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- Keller at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2.
- SUMMIT at pages 1-3 and at figures 1-3.

Each of these references show that the concept of incorporating different types of chips into a single module is not novel. Indeed, combining electrical components for enhanced space and data transfer efficiencies and/or power management has been well known for many years. In light of the references discussed herein, the asserted claims of the asserted patents cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needing to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '918 and '054 patents. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '918 and '054 patents. As such, Defendants reserve all rights to supplement their invalidity contentions.

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Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the ’918 and ’054 patents. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third-party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants’ possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery. Defendants also reserve the right to assert that the ’918 and ’054 patents are invalid under 35 U.S.C. §102(f) and/or (g) in the event Defendants obtain evidence that the named inventors of the ’918 and ’054 patents did not invent (either alone or in conjunction with other parties) the subject matter claimed in the ’918 and ’054 patents. Should Defendants obtain such evidence, they will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived, and/or the circumstances surrounding the making of the invention before the patent application.

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For example, Defendants have reason to believe that individuals substantively involved in the prosecution of the ’506 patent knew about material and non-cumulative prior art by virtue of their participation in JEDEC standards meetings. Defendants also assert invalidity of the ’918 and ’054 patents based on JEDEC documents disclosed and/or publicly available prior to the filing of the ’918 and ’054 patents. *See* Exhibit C10; *see also* Exhibit D10. With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

D. U.S. Patent Nos. 8,787,060 and 9,318,160

Invalidity claim charts identifying disclosures in the references identified in Tables 1-D and 2-D as to the Asserted Claims of the ’060 and ’160 patents are provided in attached Exhibits E1 through E21 (’060 Patent) and Exhibits F1 through F21 (’160 Patent).

Table 1-D: Prior Art Patents and Printed Publications for the ’060 and ’160 patents

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
RD-1	Asserted Patents Admitted Prior Art (APA)		
RD-2	U.S. Patent Application Publication No. 2008/0025137 (Rajan 137)	1/31/2008	7/31/2006
RD-3	U.S. Patent Application Publication No. 2011/0103156 (Kim)	5/5/2011	12/29/2009
RD-4	U.S. Patent No. 9,142,262 (Ware)	4/28/2011	9/24/2010
RD-5	U.S. Patent Application Publication No. 2011/0026293 (Riho 293)	2/3/2011	7/16/2010
RD-6	U.S. Patent Application Publication No. 2010/0195364 (Riho 364)	8/5/2010	2/1/2010
RD-7	U.S. Patent Application Publication No. 2010/0091537 (Best)	4/15/2010	12/13/2007
RD-8	U.S. Patent No. 8,258,619 (Foster)	5/12/2011	11/12/2009
RD-9	U.S. Patent Application Publication No.	5/6/2010	10/30/2008

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Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
	2010/0110745 (Jeddeloh)[6]		
RD-10	U.S. Patent Application Publication No. 2011/0208906 (Gillingham)	8/25/2011	12/14/2010
RD-11	U.S. Patent No. 8,120,958 (Bilger)	6/25/2009	12/24/2007
RD-12	U.S. Patent No. 9,123,552 (Keeth)	10/6/2011	3/30/2010
RD-13	U.S. Patent No. 7,969,192 (Wyman)	7/15/2010	3/26/2010
RD-14	U.S. Patent No. 9,160,349 (Ma)	3/3/2011	8/27/2009
RD-15	U.S. Patent No. 7,796,446 (Ruckerbauer)	3/25/2010	9/19/2008
RD-16	Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh)	June 2008	
RD-17	U.S. Patent No. 8,041,881 (Rajan 881)	10/18/2011	6/12/2007

Table 2-D: Prior Art Systems and Inventions for the '060 and '160 patents

Ex.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
RD-18	JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals)	At least as early as September 2009, December 2009, March 2010, June 2010, September 2010, April 2011, June 2011, September 2011
RD-19	Micron Hybrid Memory Cube	At least as early as August 2010
RD-20	U.S. Patent No. 8,471,362 (Lee)	At least as early as April 5, 2011
RD-21	Micron LRDIMM System	At least as early as 2010

Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also

[6] *See also*, for further background and explanation, U.S. Patent No. 7,623,365 also to Joe M. Jeddeloh ("Jeddeloh 365"), which was filed on August 29, 2007, and issued on November 24, 2009.

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separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Micron Hybrid Memory Cube System ("Micron HMC System") was offered for sale or publicly used or the information known at least as early as August 2010. Micron employees gave presentations about the Micron HMC Systems at conferences (e.g., Hot Chips) and to other companies, including one or more employees of IBM, Cisco, Juniper, and Sony during the relevant time frame. Micron also filed a patent relating to the research involved with the Micron HMC System, referenced herein as Keeth (RD-12).

Micron LRDIMM System was offered for sale or publicly used or the information known at least as early as 2010. Various Micron LRDIMM Systems were publicly sold on variety of websites and Micron even made at least one data sheet available for public dissemination during the relevant time frame.

Discovery is ongoing, and Defendants may serve other third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as examples of evidence of the state of the art as it relates to memory module devices:

Ex.	Patent No. or Title (Primary Inventor/Author)
RD-1	Asserted Patents Admitted Prior Art (APA)
RD-2	U.S. Patent Application Publication No. 2008/0025137 (Rajan 137)
RD-3	U.S. Patent Application Publication No. 2011/0103156 (Kim)
RD-4	U.S. Patent No. 9,142,262 (Ware)
RD-5	U.S. Patent Application Publication No. 2011/0026293 (Riho 293)
RD-6	U.S. Patent Application Publication No. 2010/0195364 (Riho 364)

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Ex.	Patent No. or Title (Primary Inventor/Author)
RD-7	U.S. Patent Application Publication No. 2010/0091537 (Best)
RD-8	U.S. Patent No. 8,258,619 (Foster)
RD-9	U.S. Patent Application Publ. No. 2010/0110745 (Jeddeloh); *see also* Jeddeloh 365
RD-10	U.S. Patent Application Publication No. 2011/0208906 (Gillingham)
RD-11	U.S. Patent No. 8,120,958 (Bilger)
RD-12	U.S. Patent No. 9,123,552 (Keeth)
RD-13	U.S. Patent No. 7,969,192 (Wyman)
RD-14	U.S. Patent No. 9,160,349 (Ma)
RD-15	U.S. Patent No. 7,796,446 (Ruckerbauer)
RD-16	Gabriel H. Loh, *3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture* (2008) (Loh)
RD-17	U.S. Patent No. 8,041,881 (Rajan 881)
RD-18	JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals)
RD-19	Micron Hybrid Memory Cube
RD-20	U.S. Patent No. 8,471,362 (Lee)
RD-21	Micron LRDIMM System

Each of these references show that the concept of reducing the load of drivers in a memory package on a memory module is not novel. Indeed, reducing the load of drivers on the memory module for enhanced data transfer efficiencies and/or power management has been well known for many years. In light of the references discussed herein, the Asserted Claims of the ’060 and ’160 patents cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needing to be obtained via third party subpoenas, or from Plaintiff, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants’ reference to a particular product, device, or software program in these

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contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '060 and '160 patents. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '060 and '160 patents. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '060 and '160 patents. Defendants are in the process of obtaining additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other

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products in Defendants' possession, custody, or control available for inspection by Plaintiff. Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 4-D provides additional bases for invalidity of the '060 and '160 patents under pre-AIA 35 U.S.C. § 102(f), on the grounds that the inventors of the '060 and '160 patents did not themselves invent the subject matter claimed in the '060 patent. The prior art under § 102(f) is identified in Table 4-D by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 4-D: Prior Art under pre-AIA § 102(f) for the '060 and '160 patents

Ex.	Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
RD-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2009-2011 ("*JEDEC HBM and Low Power Proposals*")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-42 committee meetings). For example: • One or more employees of ST Ericsson • One or more employees of the Industrial Technology Research Institute • One or more employees of Hynix • One or more employees of Elpida • One or more employees of Intel • One or more employees of Nokia • One or more employees of Samsung • One or more employees of LSI • One or more employees of AMD • One or more employees of Advantest • One or more employees of Avago Technologies • One or more employees of Samsung • One or more employees of Fusion • One or more employees of NVIDIA • One or more employees of Nanya

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Hyun Lee – an inventor of the ’060 and ’160 patents – regularly attended JEDEC meetings for at least the JC-42 committee in the 2009 to 2011 timeframe, as well as before and after that timeframe

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Hyun Lee was aware of the proposals and draft and final specifications for memory packages being considered and voted upon by those committees. Micron has reason to believe: for example, ST Ericsson presented and discussed Committee Item Number 1776.10 (“MIPI M-PHY Future Mobile PHY Proposal”) at the September 2009 meeting of JC-42; Samsung presented and discussed Committee Item Number 1777.00 (“Wide-IO TG Report”) at the December 2009 meeting of JC- 42; the Industrial Technology Research Institute presented and discussed Committee Item Number 1782.01 (“Advanced Memory Package Proposal”) at the March 2010 meeting of JC-42; and NVIDIA presented and discussed Committee Item Number 1797.00 (“Future High Bandwidth Memory TG”) at the September 2011 meeting of JC-42, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-42 committee of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. Based on Netlist’s apparent view of the scope of the alleged invention, each of the memory package-related drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of ’060 and ’160 patents.

Before November 3, 2010, after attending the above-referenced meetings and observing those ideas from other members of JEDEC, Micron has reason to believe that Hyun Lee returned to Netlist and drafted the provisional application to which the ’060 and ’160 patents claim

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priority, deriving the alleged inventions of the ’060 and ’160 patents from what he learned at JEDEC. He filed the provisional on November 3, 2010, naming himself as the inventor. On November 3, 2011, Hyun Lee filed the application leading to the ’060 patent, which Micron has reason to believe contained a significant amount of new material learned at JEDEC and again named himself as inventor.

Table 5-D below provides additional bases for invalidity of the ’060 and ’160 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the ’060 patent was made in this country before the alleged invention date of the ’060 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 5-D by the name of the person(s) or entities involved in the making of the invention before the applicants of the ’060 patent. The circumstances surrounding the making of the invention before the applicants of the ’060 patent are explained below.

Table 5-D: Prior Art under pre-AIA § 102(g)(2) for the ’060 and ’160 patents

Ex.	Prior Art Disclosing Technical Features	Name of Person(s)
RD-18	Proposals and disclosures made at JEDEC committee meetings during the time period 2009-2011 (“*JEDEC HBM and Low Power Proposals*”)	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-42 committee meetings). For example: • One or more employees of ST Ericsson • One or more employees of the Industrial Technology Research Institute • One or more employees of Hynix • One or more employees of Elpida • One or more employees of Intel • One or more employees of Nokia • One or more employees of Samsung • One or more employees of LSI • One or more employees of AMD

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Ex.	Prior Art Disclosing Technical Features	Name of Person(s)
		• One or more employees of Advantest • One or more employees of Avago Technologies • One or more employees of Samsung • One or more employees of Fusion • One or more employees of NVIDIA • One or more employees of Nanya
RD-19	Micron Hybrid Memory Cube	One or more employees of Micron. Circumstances of development discussed above regarding public availability.

Hyun Lee – an inventor of the '060 and '160 patents – regularly attended JEDEC meetings for at least the JC-42 committee in the 2009 to 2011 timeframe, as well as before and after that timeframe

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Micron has reason to believe that Hyun Lee was aware of the proposals and draft and final specifications for memory packages being considered and voted upon by those committees. Micron has reason to believe: for example, ST Ericsson presented and discussed Committee Item Number 1776.10 ("MIPI M-PHY Future Mobile PHY Proposal") at the September 2009 meeting of JC-42; Samsung presented and discussed Committee Item Number 1777.00 ("Wide-IO TG Report") at the December 2009 meeting of JC- 42; the Industrial Technology Research Institute presented and discussed Committee Item Number 1782.01 ("Advanced Memory Package Proposal") at the March 2010 meeting of JC-42; and NVIDIA presented and discussed Committee Item Number 1797.00 ("Future High Bandwidth Memory TG") at the September 2011 meeting of JC-42, all of which Hyun Lee attended.

Draft specifications, ballots and presentations distributed to the members of the JC-42 committee of JEDEC were distributed to many (20+) key members of the interested public with

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the expectation they would be freely disclosed to and discussed with others. Based on Netlist's apparent view of the scope of the alleged invention, each of the memory package-related drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '060 and '160 patents.

Before November 3, 2010, after attending the above-referenced meetings and observing those ideas from other members of JEDEC, Micron has reason to believe that Hyun Lee returned to Netlist and drafted the provisional application to which the '060 and '160 patents claim priority, and which Micron has reason to believe contained a significant amount of material Hyun Lee and Netlist learned at JEDEC. He filed the provisional on November 3, 2010, naming himself as the inventor. On November 3, 2011, Hyun Lee filed the application leading to the '060 patent, which Micron has reason to believe contained a significant amount of new material learned at JEDEC and again named himself as inventor.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with 35 U.S.C. § 102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

IV. P.R. 3-3(b) – Invalidity Grounds

Pursuant to P.R. 3-3(b), Defendants contend that certain prior art references below anticipate one or more Asserted Claims and that to the extent the identified prior art references do not anticipate the Asserted Claims, those claims are invalid as obvious under 35 U.S.C. §103. Each anticipatory prior art reference, either alone or in combination with other prior art, also renders the Asserted Claims invalid as obvious. In particular, each anticipatory prior art reference may be combined with (1) information generally known to persons skilled in the art at the time of the alleged invention, and/or (2) any of the other anticipatory prior art references. To the extent that Plaintiff contends that any of the anticipatory prior art fails to disclose one or

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more limitations of the Asserted Claims, Defendants contend that any difference between the reference and the corresponding patent claims would have been obvious to one of ordinary skill in the art. Thus, all anticipation charts should be interpreted as both reflecting anticipation by the reference as well as invalidity due to single reference obviousness, to the extent that Plaintiff contends that any limitation is missing.

A. Anticipation

As stated above, Defendants incorporate by reference all other invalidity contentions related to the Asserted Patents served on or otherwise provided to Plaintiff, whether past or future. In accordance with P.R. 3-3(a), prior art references anticipating the Asserted Claims are provided below. The prior art listed below anticipates the Asserted Claims under the proper construction of the claims and/or under Plaintiff's apparent interpretation of the claims as set forth by Plaintiff in its Complaint and Infringement Contentions.

1. U.S. Patent No. 10,860,506

The Asserted Claims of the '506 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '506 patent Asserted Claims in the claim charts of Exhibits A1 through A23 (collectively "Appendix A") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix A provide an explanation showing how these prior art references teach or suggest each and every element of the '506 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3-3(b).

In addition to contending that the '506 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix A, Defendants further contend that the '506 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a)

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and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

Defendants' reference to a particular memory module, circuit, software program, device, or product in the claim charts of Appendix A should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix A that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '506 patent, all prior art as described in any pending or future *inter partes* review proceedings of the '506 patent, and all prior art disclosed during previous litigation proceedings.

Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '506 patent, its foreign counterparts, or any parent or child patent of the '506 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and

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systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix A.

2. U.S. Patent No. 10,949,339

The Asserted Claims of the ’339 patent are anticipated and/or rendered obvious by prior

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art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '339 patent Asserted Claims in the claim charts of Exhibits B1 through B25 (collectively "Appendix B") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix B provide an explanation showing how these prior art references teach or suggest each and every element of the '339 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3- 3(b).

In addition to contending that the '339 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix B, Defendants further contend that the '339 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix B should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix B that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during

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the prosecution of the ’339 patent, all prior art as described in any pending or future *inter partes* review proceedings of the ’339 patent, and all prior art disclosed during previous litigation proceedings. Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the ’339 patent, its foreign counterparts, or any parent or child patent of the ’339 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references,

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other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix B.

3. U.S. Patent No. 11,016,918

The Asserted Claims of the '918 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '918 patent Asserted Claims in the claim charts of Exhibits C1 through C13 (collectively "Appendix C") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix C provide an explanation showing how these prior art references teach or suggest each and every element of the '918 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3- 3(b).

In addition to contending that the '918 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix C, Defendants further contend that the '918 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or

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systems.

Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix C should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix C that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '918 patent, all prior art as described in any pending or future *inter partes* review proceedings of the '918 patent, and all prior art disclosed during previous litigation proceedings. Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '918 patent, its foreign counterparts, or any parent or child patent of the '918 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the

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referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix C.

4. U.S. Patent No. 11,232,054

The Asserted Claims of the ’054 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the ’054 patent Asserted Claims in the claim charts of Exhibits D1 through D13 (collectively “Appendix D”) which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix D provide an explanation showing how these prior art references teach or suggest each and every element of the ’054 patent Asserted Claims. For each

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reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3- 3(b).

In addition to contending that the '054 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix D, Defendants further contend that the '054 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix D should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix D that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '054 patent, all prior art as described in any future *inter partes* review proceedings of the '054 patent, and all prior art disclosed during previous litigation proceedings. Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '054 patent, its

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foreign counterparts, or any parent or child patent of the ’054 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in

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view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix D.

5. U.S. Patent No. 8,787,060

The Asserted Claims of the '060 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '060 patent Asserted Claims in the claim charts of Exhibits E1 through E21 (collectively "Appendix E") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix E provide an explanation showing how these prior art references teach or suggest each and every element of the '060 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3-3(b).

In addition to contending that the '060 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix E, Defendants further contend that the '060 patent Asserted Claims are invalid as anticipated and/or obvious under 35 U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix E should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix E that relates to the cited memory module, circuit, software program, device, or product. In addition,

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Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '060 patent, all prior art as described in any pending and future *inter partes* review proceedings of the '060 patent, and all prior art disclosed during previous litigation proceedings.

Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '060 patent, its foreign counterparts, or any parent or child patent of the '060 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would

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rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix E.

6. U.S. Patent No. 9,318,160

The Asserted Claims of the ’160 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the ’160 patent Asserted Claims in the claim charts of Exhibits F1 through F21 (collectively “Appendix F”) which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix F provide an explanation showing how these prior art references teach or suggest each and every element of the ’160 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3- 3(b).

In addition to contending that the ’160 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix F, Defendants further contend that the

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’160 patent Asserted Claims are invalid as anticipated and/or obvious under 35 U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

Defendants’ reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix F should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix F that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the ’160 patent, all prior art as described in any pending and future *inter partes* review proceedings of the ’160 patent, and all prior art disclosed during previous litigation proceedings.

Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the ’160 patent, its foreign counterparts, or any parent or child patent of the ’160 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to

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demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix F.

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B. Obviousness

As stated above, Defendants incorporate by reference all other invalidity contentions related to the Asserted Patents served on or otherwise provided to Plaintiff, whether past or in the future. In addition to certain claims being anticipated at least under Plaintiff's apparent claim constructions as indicated above, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation. Further, the Asserted Claims are obvious over various combinations of the references shown in the claim charts accompanying or incorporated by reference into this disclosure. No Asserted Claim goes beyond combining known elements to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Thus, to the extent that an Asserted Claim is not anticipated, it is nevertheless invalid as obvious. Specifically, Defendants assert that any charted or incorporated reference in combination with one or more other charted or incorporated references renders the Asserted Claims obvious.

Motivations to combine, as well as the general state of the art, may be found in a variety of places including in the references defined above, and the specification of the Asserted Patents. For example, each piece of prior art relates to the design and/or structure and/or function of memory related devices, such as DIMMs. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein so as to practice the Asserted Claims and there is a motivation in the art to make such a combination.

Motivations to combine various prior art references are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or

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the nature of the problems allegedly addressed by the Asserted Patents. Further reasons to combine the references identified in these charts include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of memory related devices (*e.g.,* DIMMs) that such combinations would have yielded predictable results, and that such combinations would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 127 S. Ct. 1727, 1739 (2007); *see also id.* at 1731 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id.* at 1745–46. The Supreme Court found that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 1731.

Moreover, the Supreme Court recognizes that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. Id. at 1732 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified,

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predictable solution to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id.*

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. Id. at 1740. If a person of ordinary skill can implement a predictable variation, U.S.C. § 103 bars its patentability. Id. The rationale to combine or modify prior art references is significantly stronger when references seek to solve similar problems, come from the same field, and correspond well. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001).

Although the law does not require evidence of motivation to combine, motivation exists to combine one or more of the references disclosed herein with each other. In addition to the specific motivations identified herein, motivation to modify a particular reference or to combine any two or more of the identified references comes from (a) the nature of the problem being solved, (b) the teachings of the prior art, (c) the knowledge of persons of ordinary skill in the art, (d) the fact that all of the references teach systems, apparatuses, and methods related to the subject matter and address the same technical issues described in the Asserted Patents, and (e) one would be motivated by considerations of efficiency, effectiveness, convenience, cost-savings, and accessibility, to combine the various teachings. Additionally, one would be motivated to address the alleged problems or achieve the purported objectives identified in the Background sections of the Asserted Patents.

To the extent not anticipated, the Asserted Claims represent no more than the result of ordinary innovation over the prior art. Moreover, no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known

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alternative to one of skill in the art. *See KSR*, 127 S.Ct. at 1739-40 (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 1742. Nevertheless, in keeping with the Local Patent Rules, and in addition to the information contained in the section immediately above and elsewhere in these contentions, additional motivation and reason to combine the cited art are identified. A person having ordinary skill in any or all of these fields would be aware of all prior art in those fields, including but not limited to the identified prior art references and systems, and would have been motivated to combine the teachings of prior art with the field.

In sum, motivations to modify or combine the identified references including the references listed above can be found via, for example, discussions in the cited references, the state of the art discussed in the references, and the knowledge of one of ordinary skill in the art. One of ordinary skill in the art would have been motivated to combine these references, because these references relate to common objectives and subject matter. The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of skill in the art to combine them. These references are within the field of the Asserted Patents and are directed to similar subject matter within the field. Additionally, the references, and any

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products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination. These disclosures were provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any invalidity contentions.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Plaintiff may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Defendants reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the Asserted Patents.

While Defendants reserve the right to rely on any combination of the references reflected in their charts or incorporated herein by reference, Defendants provide the following exemplary and non-exhaustive references and/or combinations evidencing invalidity of the claims of the Asserted Patents. The combinations of prior art listed below render obvious the Asserted Claims under the proper construction of the claims and/or under Plaintiff's apparent interpretation of the claims as set forth by Plaintiff in its Complaint and Infringement Contentions.

1. U.S. Patent No. 10,860,506

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix A the prior art references that render obvious the Asserted Claims of the '506 patent and include below exemplary combinations showing the obviousness of the '506 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix A, the limitation would have been

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obvious in light of the disclosures within the reference and the knowledge of one of skill in the art at the time of the '506 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix A, such reference may be combined with any other references listed in Appendix A for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '506 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '506 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

a) *Obviousness Rationale*

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix A along with the knowledge of one of ordinary skill in the art to meet the limitations of the '506 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '506 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a

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specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix A would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix A would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references;

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common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the ’506 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix A is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of skill in the art to consult and/or combine any of the prior art listed in Appendix A because all of these references relate to the same area of technology and/or are from analogous art. The ’506 patent Asserted Claims are directed to a memory module with delay circuitry. ’506 patent at Abstract. The ’506 patent Asserted Claims merely unite old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person

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having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the '506 patent Asserted Claims.

All of the '506 patent Asserted Claims are directed to memory modules configurable to delay certain signals. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, was widely known before the alleged priority date of the '506 Patent, as evidenced by the references in Appendix A. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claims 1, 2;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 18;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-

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52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;

- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, 10, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:23-37, 4:38-5:20, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87,

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88, 119, 120, 139, 141;

- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2,

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Committee Item Number 158.01 at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4;
- RA-35 (Shaeffer) at Figs. 5, 18, 31, 38, 3:26–39, 4:18–42, 5:11–31, 6:32–47, 9:29–51. 31:58–33:33, 35:40–36:6, 40:40–42:7.
- RA-36 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 10:62–11:9, 24:23–44, and 28:6–27.
- RA-37 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.

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One of ordinary skill in the art would have been motivated to combine any of the references in Appendix A because at the time of the alleged invention delaying signals in memory modules was a common problem with a well-known solution. *See, e.g.*,:

- ’506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claims 1, 2;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 18;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-

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0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;

- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, 10, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27- 50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:23-37, 4:38-5:20, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-

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11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73, RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;

- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item*

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Number 2192.62 at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Figs. 5, 18, 31, 38, 3:26–39, 4:18–42, 5:11–31, 6:32–47, 9:29–51. 31:58–33:33, 35:40–36:6, 40:40–42:7.
- RA-36 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 10:62–11:9, 24:23–44, and 28:6–27.
- RA-37 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.

Further, it was common knowledge to one of skill in the art at the time of the alleged invention that delaying signals can improve performance of the memory module. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054],

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[0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claims 1, 2;

- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 18;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, 10, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26,

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5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;

- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:23-37, 4:38-5:20, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73, RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128; RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at

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7, 8, 9, 12, 13, 14, 15; RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44; RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory*

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Bandwidth at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Figs. 5, 18, 31, 38, 3:26–39, 4:18–42, 5:11–31, 6:32–47, 9:29–51. 31:58–33:33, 35:40–36:6, 40:40–42:7.
- RA-36 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 10:62–11:9, 24:23–44, and 28:6–27.
- RA-37 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix A at the time of the alleged invention. Common problems with conventional techniques for delaying signals in memory modules were known to persons of ordinary skill in the art and incorporating delay circuitry in the memory modules was a well-known solution to achieve improved performance. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at [0099], Fig. 5;
- RA-3 (Butt) at [0018-0020], [0034-0035];
- RA-4 (Tokuhiro) at 2:10-23, 2:29-49, Figs. 5, 6;
- RA-5 (Ellsberry) at [0033-0034];
- RA-6 (Halbert) at 2:6-60, 5:66-6:65, 6:66-7:20, 9:4-35, Figs. 5, 6;
- RA-7 (Bhakta) at 25:11-26:19, Figs. 6C, 6D;
- RA-8 (Chen) at 4:3-7, 4:14-27, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 7:34-67,

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8:1-42, 8:43-9:9, Figs. 1A, 1B, 4, 5A, 5B, 7A, 7B, 8, Claims 11, 16, 17;

- RA-9 (Kuroki) at 1:25-33, 1:39-52, 1:53-2:4, 2:5-22, 2:52-3:16, 3:17-25, 4:1-3, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at JESD205 at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, JESD82-20 at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at JESD79-3C at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, JEDEC 21-C at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 5:22-30, 5:47-58, 10:27-41, 6:18-26;
- RA-13 (SK Hynix FBGA) at FBGA Specification at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at DDR3 SDRAM User's Manual at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at FB-DIMM Design Specification Revision 3.0 at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, AMB Specification at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91,

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143, 145, Committee Item Number 2118.08 at 3, 4, Committee Item Number 2135.01 at 20, Committee Item Number 2171.02 at 4, 6, Committee Item Number 2171.07 at 3, 5, 6, 7, 8, 9, 10, JC-45 Meeting No. 11 Minutes at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at Committee Item Number 142.62B at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, Committee Item Number 158.01 at 2, Committee Item Number 158.02 at 5, Committee Item Number 0311.12 at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, Committee Item Number 0311.13 at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, Committee Item Number 0311.14 at 3, 4, 5, 6, 7, 8, 9, 10, JC-40 Meeting No. 169 Minutes at 9, 10, Committee Item Number 2222.01 at 2, Committee Item Number 2222.03 at 2, 7, Committee Item Number 2192.62 at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37; RA-17 (Lattice DDR3) at Lattice DDR3 White Paper at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at NXP DDR Presentation at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at QBM Specification Rev. 0.93 at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, QBM2 Interface Overview at 3, QBM Informational Showing Item #1133 at 4, 5, 6, 8, 9, 15, QBM2 Technical Features Overview at 3, 5, 8, 11, 14, 15, QBM2 Technical Highlights at 19, QBM Doubling DDR Memory Bandwidth at 11, 12, 13, QBM2 Technology Overview at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, QBM Interim JEDEC Meeting at 6, 11, 20, 22, QBM Informational Showing Item #1341 at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4;

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- RA-25 (DFi DDR PHY 1) at 55-56, 58; RA-26 (DFi DDR PHY 2) at 117, 119;
- RA-27 (NXP MSC8152) at 12-84 through 12-92;
- RA-28 (Xilinx 1) at 227-229;
- RA-29 (Xilinx) at 18;
- RA-30 (Aqueel) at 2;
- RA-31 (Jang) at 634-35;
- RA-32 (Jang-Woo Lee) at 46-47;
- RA-33 (Alexandropoulos) at 388-89;
- RA-34 (Hwang) at 357-58;
- RA-35 (Shaeffer) at Figs. 5, 18, 31, 38, 3:26–39, 4:18–42, 5:11–31, 6:32–47, 9:29–51. 31:58–33:33, 35:40–36:6, 40:40–42:7.
- RA-36 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 10:62–11:9, 24:23–44, and 28:6–27.
- RA-37 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.
- RA-38 (LaBerge) at Fig. 4, 2:30–3:42, 9:14–11:12.
- RA-39 (Uchida) at Figs. 12, 13, 22–28, 6:28–33, 12: 15–13:17, 15:58–19:33.
- RA-40 (Hampel) at Figs.1, 2A–2B, 3a, 7:6–18.

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can be operable in a computer system to communicate, or to communicate data, with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus. *See, e.g.*,:

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- ’506 patent at 1:49-60, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at Abstract, [0010], [0013-0014], [0045-0046], [0047], [0049], [0060], [0065], [0069], [0102-0103], [0107], Figs. 1, 2, 3, 7;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0015-0016], [0017], [0018-0020], [0036], [0063], Figs. 1, 2;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-33, 1:34-48, 1:63-2:9, 2:39-45, 4:62-5:41, 5:42-56, Figs. 1, 2, 4, 5, 6;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0010-0012], [0021], [0023], [0026-0027], [0028-0031], [0034], [0047-0051], [0052], [0054], [0056], Figs. 1, 2, 3, 4, 5, 6, 11, 13;
- RA-6 (Halbert) at Abstract, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-5:5, 5:6-39, 5:66-6:28, 7:31-61, 8:1-48, Figs. 1, 4, 7, 8, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:34-42, 2:46-58, 5:11-26, 7:45-62, Figs. 1A, 1B;
- RA-8 (Chen) at Abstract, 1:22-2:52, 4:34-35, Figs 1A, 1B;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:25-33, 2:34-48, 2:52-3:16, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, Fig. 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at JESD79-3C at cover, 1, 3, 6, 13,

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18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,

- RA-12 (Lee) at 4:66-5:20, 7:11-20, Fig. 1, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpid aDDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDECFBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee*

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Item Number 2222.01 at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1pre] and [14a].
- RA-36 (Muralimanohar) at Ex. A-22 at [1pre] and [14a].
- RA-37 (Karamcheti) at Ex. A-23 at [1pre] and [14a].
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It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a module board having edge connections to be coupled to respective signal lines in the memory bus. *See, e.g.*,:

- '506 patent at 1:49-60;
- RA-2 (Hirashi) at [0010], [0045], [0047], [0048], [0049], Figs. 1, 3;

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- RA-3 (Butt) at [0015-0017], [0018-0020], [0063], Figs. 1, 2 ;
- RA-4 (Tokuhiro) at 1:15-20, 1:22-33, 1:34-48, 1:63-2:9, 5:31-64, Figs. 1, 2, 4;
- RA-5 (Ellsberry) at [0002-0003],[0005], [0021], [0027], [0028-0031], [0047-0051], Figs. 2, 5, 6, Claims 9, 18;
- RA-6 (Halbert) at 1:16-19, 1:61-2:14, Figs. 1, 7, 8;
- RA-7 (Bhakta) at 1:23-32, 2:46-58, 5:11-26, 6:10-17, Figs. 1A, 1B;
- RA-8 (Chen) at Abstract, 1:22-2:52, 4:34-35, Figs 1A, 1B;
- RA-9 (Kuroki) at 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, Fig. 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 4:66-5:20, Fig. 1, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;

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- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory*

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Bandwidth at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1a] and [14a].
- RA-36 (Muralimanohar) at Ex. A-22 at [1a] and [14a].
- RA-37 (Karamcheti) at Ex. A-23 at [1a] and [14a].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a module control device on the module board that is configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines, and to output registered C/A signals in response to the input C/A signals, and to output module control signals. *See, e.g.*,:

- '506 patent at 1:49-60, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at [0018-0019], [0045-0046], [0047], [0049], [0054], [0058-0062], [0069], [0073], [0095-0096], [0097-0100], [0106-0108], [0122-0131], Figs. 1, 6, 7, 11;
- RA-3 (Butt) at [0015-0017], [0018-0020], [0022-0023], [0033], [0036], Figs. 1, 2;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-48, 1:63-2:23, 2:46-49, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 13:16-29, 14:11-48, 15:32-16:7, 17:23-29, 18:15-35, 19:40-46, 20:48-56, 24:49-55, 25:66-26:4, Figs. 4, 5, 6, 12, 14, 19;

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- RA-5 (Ellsberry) at Abstract, [0010-0012], [0018-0019], [0026], [0028-0031], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0051-0056], Figs. 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13;
- RA-6 (Halbert) at 4:36-39, 4:40-48, 5:23-39, 6:15-28, 6:66-7:20, 7:31-53, 8:19-32, Figs. 4, 6, 7, 8, 10;
- RA-7 (Bhakta) at 2:46-58, 5:11-26, 7:45-62, Figs. 1A, 1B;
- RA-8 (Chen) at 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-7, 4:14-27, 4:34-35, 4:64-5:11, 5:33-59, 6:6-18, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:25-33, 1:39-52, 2:34-48, 2:52-3:16, 3:17-25, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:45-6:4, 6:49-54, Fig. 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 4:66-5:20, 5:43-53, 7:11-20, 9:46-53, Fig. 1, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30,

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86, 89, 128;

- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20,

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- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1b] and [14a].
- RA-36 (Muralimanohar) at Ex. A-22 at [1b] and [14a].
- RA-37 (Karamcheti) at Ex. A-23 at [1b] and [14a].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include "memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at Abstract, [0004], [0010], [0045-0046], [0048], [0050-0053], [0105-0106], [0107],[0110-0115], [0117-0118], Figs. 1, 7;
- RA-3 (Butt) at [0002], [0003], [0005-0006], [0008-0009], [0015-0017], [0024], [0037], [0038], [0054], [0061], Figs. 1, 2,;
- RA-4 (Tokuhiro) at 1:15-20, 1:38-48, 3:16-26, 3:56-63, 4:62-5:3, 5:9-23, 5:24-30, 5:31-41, 5:42-56, 5:57-64, 6:1-6, 8:42-58, Figs. 4, 6, 7, 11;
- RA-5 (Ellsberry) at Abstract, [0003], [0010-0012], [0023], [0026], [0028-0032],

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[0033], [0035-0036], [0037], [0039], [0040], [0041-0042], [0045-0050], [0052-0056], Figs. 2, 5, 6, 7A, 11, 13;

- RA-6 (Halbert) at 4:36-39, 4:49-59, 5:6-22, 7:31-53, 7:54-61, 9:20-35, 9:55-65, Figs. 1, 4, 7, 8, Claim 4;
- RA-7 (Bhakta) at 1:23-32, 2:16-22, 2:46-58, 5:11-26, 6:18-26, 6:38-46, 7:45-62, Figs. 1A, 1B;
- RA-8 (Chen) at 1:22-2:52, 4:34-35, 4:60-5:24, Figs. 1A, 1B;
- RA-9 (Kuroki) at 1:16-33, 4:38-5:20, 6:49-54, 7:41-67, 8:45-50, Fig. 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 4:66-5:20, 6:58-64, 7:11-20, 7:43-55, Fig. 1, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;

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- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM*

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Doubling DDR Memory Bandwidth at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1c] and [14a].
- RA-36 (Muralimanohar) at Ex. A-22 at [1c] and [14a].
- RA-37 (Karamcheti) at Ex. A-23 at [1c] and [14a]

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include registered C/A signals that cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation. *See, e.g.*,

- '506 patent at 2:7-16, 2:17-27;
- RA-2 (Hirashi) at [0006], [0048-0049], [0051-0053], [0054], [0056], [0061], [0075-0076], [0078-0080], [0087-0088], [0091], [0102-0103], [0105], [0117-0119], [0120-0129], [0163], [0170], Figs. 1, 4, 7;
- RA-3 (Butt) at Abstract, [0005], [0015-0017], [0018-0020], [0024-0025], [0027-0028], [0029-0032], [0033-0036], [0044], [0046], Figs. 1, 2, 3A, 3B, 4;
- RA-4 (Tokuhiro) at 1:34-2:9, 5:9-41, 5:31-64, 6:1-6, 7:55-8:58, 9:12-16, 9:53-57, 19:66-20:38, 22:6-52, Fig. 4;
- RA-5 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0028-0033], [0035-0036], [0037-0038], [0039], [0040-0041], [0042-0043], [0044], [0045], [0047], [0052], [0053-0056], [0057], Figs 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13;

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- RA-6 (Halbert) at 2:6-60, 4:23-5:5, 5:6-22, 5:40-50, 7:31-53, 7:54-61, 9:20-35, Figs. 4, 7, 8;
- RA-7 (Bhakta) at 7:45-62, 8:65-67, 24:57-25:10, Figs. 1A, 1B, 6B, Table 2;
- RA-8 (Chen) at 1:22-2:52, 4:3-31, 4:34-35, Figs. 1A, 1B;
- RA-9 (Kuroki) at 1:16-33, 2:52-3:52, 4:23-37, 4:38-5:20, 5:12-44, 6:10-28, 6:29-34, 6:49-54, 7:41-67, 8:45-50, Figs. 3, 4A, 4B;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 4:66-5:20, 5:43-53, 7:11-20, Fig. 1, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59,

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- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim*

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JEDEC Meeting at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1d] and [14e].
- RA-36 (Muralimanohar) at Ex. A-22 at [1d] and [14e].
- RA-37 (Karamcheti) at Ex. A-23 at [1d] and [14e].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a first memory device in the selected rank that is configurable to output a first section of the read data and a first read strobe. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at [0006], [0048-0049], [0051-0053], [0054], [0056], [0061], [0075-0076], [0078-0080], [0087-0088], [0091], [0102-0103], [0105], [0117-0119], [0120-0129], [0163], [0170], Figs. 1, 4, 7;
- RA-3 (Butt) at Abstract, [0005], [0015-0017], [0018-0020], [0024-0025], [0027-0028], [0029-0032], [0033-0036], [0044], [0046], Figs. 1, 2, 3A, 3B, 4;
- RA-4 (Tokuhiro) at 1:34-2:9, 5:9-41, 5:31-64, 6:1-6, 7:55-8:58, 9:12-16, 9:53-57, 19:66-20:38, 22:6-52, Fig. 4;
- RA-5 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0028-0033], [0035-0036], [0037-0038], [0039], [0040-0041], [0042-0043], [0044], [0045], [0047], [0052], [0053-0056], [0057], Figs 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13;
- RA-6 (Halbert) at 2:6-60, 4:23-5:5, 5:6-22, 5:40-50, 7:31-53, 7:54-61, 9:20-35, Figs. 4, 7, 8;

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- RA-7 (Bhakta) at 24:57-25:10, 25:11-26:19, Figs. 6B, 6C, 6D;
- RA-8 (Chen) at 1:22-2:52, 4:3-31, 4:34-35, Figs. 1A, 1B;
- RA-9 (Kuroki) at 1:16-33, 2:52-3:52, 4:23-37, 4:38-5:20, 5:12-44, 6:10-28, 6:29-34, 6:49-54, 7:41-67, 8:45-50, Figs. 3, 4A, 4B;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 5:43-53;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145,

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Committee Item Number 2118.08 at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

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- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1e] and [14f].
- RA-36 (Muralimanohar) at Ex. A-22 at [1e] and [14f].
- RA-37 (Karamcheti) at Ex. A-23 at [1e] and [14f].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include data buffers on the module board and coupled between the edge connections and the memory devices. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at Abstract, [0010-0011], [0017], [0045-0046], [0050-0053], [0055-0056], [0083-0085], [0092-0093], [0099-0100], [0103-0108], [0100-0111], Figs. 1, 5, 7;
- RA-3 (Butt) at [0015-0017], [0018-0020], [0022-0023], [0033], [0036], Figs. 1, 2;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-48, 1:63-2:23, 2:46-49, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 13:16-29, 14:11-48, 15:32-16:7, 17:23-29, 18:15-35, 19:40-46, 20:48-56, 24:49-55, 25:66-26:4, Figs. 4, 5, 6, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0010-0012], [0018-0019], [0021], [0026], [0028-0033], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050], [0052-0056], Figs. 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claim 1;
- RA-6 (Halbert) at Abstract, 3:42-57, 4:23-35, 4:36-59, 4:60-5:50, 6:40-65, 6:66-

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7:20, 7:31-53, 7:62-67, 9:4-35, 9:36-54, Figs. 4, 7, 8, 9;

- RA-7 (Bhakta) at 3:17-30, 5:27-50, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-7, 4:14-27, 4:34-35, 4:64-5:11, 5:33-59, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, Claims 2, 3;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:25-33, 1:39-52, 2:34-48, 2:52-3:16, 3:17-25, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:42-48, 6:49-54, Fig. 3, Claim 1;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:64-4:8, 4:66-5:20, 6:48-53, 8:1-9, 8:33-52, 9:13-22, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;

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- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM*

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- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1f] and [14a].
- RA-36 (Muralimanohar) at Ex. A-22 at [1f] and [14a].
- RA-37 (Karamcheti) at Ex. A-23 at [1f] and [14a].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a respective data buffer of the data buffers that is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device. *See, e.g.*,

- '506 patent at 1:49-60, 2:17-27;
- RA-2 (Hirashi) at [0010-0011], [0017], [0045], [0050-0052], [0055-0056], [0084-0085], [0099], Figs. 1, 5, 7;
- RA-3 (Butt) at [0015-0017], Figs. 1, 2;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-48, 1:63-2:23, 2:46-49, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:26, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 13:16-29, 14:11-48, 15:32-16:7, 17:23-29, 18:15-35, 19:40-46, 20:48-56, 24:49-55, 25:66-26:4, Figs. 4, 5, 6, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0010-0012], [0018], [0021], [0026], [0028-0033],

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[0035], [0037], [0038-0039], [0040-0041], [0042], [0045-0046], [0049], [0050], [0052-0056], Figs. 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13;

- RA-6 (Halbert) at Abstract, 3:42-57, 4:23-35, 4:36-59, 4:60-5:50, 6:40-65, 6:66-7:20, 7:31-53, 7:62-67, 9:4-35, 9:36-54, Figs. 4, 7, 8, 9;
- RA-7 (Bhakta) at 3:17-30, 5:27-50, 5:61-6:9, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-7, 4:14-27, 4:34-35, 4:64-5:11, 5:33-59, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, Claims 2, 3;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:25-33, 1:39-52, 2:34-48, 2:52-3:16, 3:17-25, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:42-48, 6:49-54, Fig. 3, Claim 1;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:64-4:8, 4:66-5:20, 6:48-53, 8:1-9, 8:33-52, Figs. 1, 2, Claims

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1, 20;

- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33,

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35, 36, 37, 42;

- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1g] and [14i].
- RA-36 (Muralimanohar) at Ex. A-22 at [1g] and [14i].
- RA-37 (Karamcheti) at Ex. A-23 at [1g] and [14i].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a first data buffer of the data buffers that is coupled to the first memory device. *See, e.g.*,

- ’506 patent at 1:49-60, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at [0045], [0055-0056], [0084-0085], [0099], [0103], Figs. 1, 7;
- RA-3 (Butt) at [0015-0017], Figs. 1, 2;
- RA-4 (Tokuhiro) at 6:1-6, 6:29-35, 6:45-51, Figs. 4, 5, 6;
- RA-5 (Ellsberry) at Abstract, [0010-0012], [0018], [0021], [0026], [0028-0033], [0035], [0037], [0038-0039], [0040-0041], [0042], [0045-0046], [0049], [0050], [0052-0056], Figs. 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13;

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- RA-6 (Halbert) at Abstract, 3:42-57, 4:23-35, 4:36-59, 4:60-5:50, 6:40-65, 6:66-7:20, 7:31-53, 7:62-67, 9:4-35, 9:36-54, Figs. 4, 7, 8, 9;
- RA-7 (Bhakta) at 3:17-30, 5:27-50, 5:61-6:9, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-7, 4:14-27, 4:34-35, 4:64-5:11, 5:33-59, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, Claims 2, 3;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:25-33, 1:39-52, 2:34-48, 2:52-3:16, 3:17-25, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:42-48, 6:49-54, Fig. 3, Claim 1;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141; RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:64-4:8, 4:66-5:20, 6:48-53, 8:1-9, 8:33-52, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30,

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86, 89, 128;

- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21,

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26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [1h] and [14i].
- RA-36 (Muralimanohar) at Ex. A-22 at [1h] and [14i].
- RA-37 (Karamcheti) at Ex. A-23 at [1h] and [14i].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a first data buffer configurable to in response to one or more of the module control signals delay “the first read strobe by a first predetermined amount to generate a first delayed read strobe. *See, e.g.*,

- ’506 patent at 1:49-60, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at [0045], [0055-0056], [0084-0085], [0091], [0099], [0103-0106], [0120-0129], [0134-0136], [0147], [0148-0150], [0155], Figs. 1, 5, 7, 13, 15;
- RA-3 (Butt) at Abstract, [0005-0006], [0013-0014], [0015-0019], [0020-0022], [0025-0028], [0029-0032], [0035], [0037], [0038], [0045-0047], [0048-0054], [0060-0061], Figs. 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at 2:13-18, 2:54-59, 9:33-40, 13:30-37, 16:43-46, 18:53-65,

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Figs. 5, 6, 7, 10, 11;

- RA-5 (Ellsberry) at [0033-0034];
- RA-6 (Halbert) at 2:6-60, 5:66-6:65, 6:66-7:20, 9:4-35, Figs. 5, 6;
- RA-7 (Bhakta) at 25:11-26:19, Figs. 6C, 6D;
- RA-8 (Chen) at 2:66-3:5, 3:6-43, 3:44-67, 4:3-7, 4:14-27, 4:64-5:11, 5:33-59, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3;
- RA-9 (Kuroki) at Abstract, 2:52-3:16, 3:17-25, 4:1-3, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 5:22-30, 5:47-58, 6:18-26, 10:27-41;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;

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- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item umber 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational*

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Showing Item #1133 at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4;
- RA-21 (Altera 1) at 3-8 through 3-14;
- RA-22 (Altera 2) at 5-6 through 5-8;
- RA-23 (Altera 3) at 5-7 through 5-8;
- RA-24 (Altera 4) at 7-9;
- RA-25 (DFi DDR PHY 1) at 55-56, 58;
- RA-26 (DFi DDR PHY 2) at 117, 119;
- RA-27 (NXP MSC8152) at 12-84 through 12-92;
- RA-28 (Xilinx 1) at 227-29; RA-29 (Xilinx 2) at 18;
- RA-30 (Aqueel) at 2;
- RA-31 (Jang) at 634-35;
- RA-32 (Jang-Woo Lee) at 46-47;
- RA-33 (Alexandropoulos) at 388-89;
- RA-34 (Hwang) at 357-58;
- RA-35 (Shaeffer) at Ex. A-21 at [1i] and [14j].
- RA-36 (Muralimanohar) at Ex. A-22 at [1i] and [14j].
- RA-37 (Karamcheti) at Ex. A-23 at [1i] and [14j].
- RA-38 (LaBerge) at Fig. 4, 2:30–3:42, 9:14–11:12.

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- RA-39 (Uchida) at Figs. 12, 13, 22–28, 6:28–33, 12: 15–13:17, 15:58–19:33.

RA-40 (Hampel) at Figs.1, 2A–2B, 3a, 7:6–18. It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a first data buffer configurable to in response to one or more module control signals, sample the first section of the read data using the first delayed read strobe. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at [0099], Fig. 5;
- RA-3 (Butt) at [0018-0020], [0034-0035];
- RA-4 (Tokuhiro) at 2:10-23, 2:29-49, Figs. 5, 6;
- RA-5 (Ellsberry) at [0033-0034];
- RA-6 (Halbert) at 2:6-60, 5:66-6:65, 6:66-7:20, 9:4-35, Figs. 5, 6;
- RA-7 (Bhakta) at 25:11-26:19, Figs. 6C, 6D;
- RA-8 (Chen) at 4:3-7, 4:14-27, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 4, 5A, 5B, 7A, 7B, 8, Claims 11, 16, 17;
- RA-9 (Kuroki) at 1:25-33, 1:39-52, 1:53-2:4, 2:5-22, 2:52-3:16, 3:17-25, 4:1-3, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;

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- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 5:22-30, 5:47-58, 10:27-41, 6:18-26;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number*

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0311.14 at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4; RA-25 (DFi DDR PHY 1) at 55-56, 58;
- RA-26 (DFi DDR PHY 2) at 117, 119;
- RA-27 (NXP MSC8152) at 12-84 through 12-92;
- RA-28 (Xilinx 1) at 227-229;
- RA-29 (Xilinx) at 18; RA-30 (Aqueel) at 2;
- RA-31 (Jang) at 634-35; RA-32 (Jang-Woo Lee) at 46-47;
- RA-33 (Alexandropoulos) at 388-89;
- RA-34 (Hwang) at 357-58;
- RA-35 (Shaeffer) at Ex. A-21 at [1j] and [14k].

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- RA-36 (Muralimanohar) at Ex. A-22 at [1j] and [14k].
- RA-37 (Karamcheti) at Ex. A-23 at [1j] and [14k].
- RA-38 (LaBerge) at Fig. 4, 2:30–3:42, 9:14–11:12.
- RA-39 (Uchida) at Figs. 12, 13, 22–28, 6:28–33, 12: 15–13:17, 15:58–19:33.

RA-40 (Hampel) at Figs.1, 2A–2B, 3a, 7:6–18. It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a first data buffer configurable to in response to one or more module control signals, transmit the first section of the read data to a first section of the data bus. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at [0006], [0048-0049], [0051-0053], [0054], [0056], [0061], [0075-0076], [0078-0080], [0087-0088], [0091], [0102-0103], [0105], 0117-0119], 0120-0129], [0163], [0170], Figs. 1, 4, 5, 7;
- RA-3 (Butt) at Abstract, [0005], [0015-0017], [0018-0020], [0024-0025], [0027-0028], [0029-0032], [0033-0036], [0044], [0046], Figs. 1, 2, 3A, 3B, 4;
- RA-4 (Tokuhiro) at 5:9-30, 5:31-64, 6:1-6, 7:55-8:58, 9:12-16, 9:53-57, 19:66-20:38, 22:6-52, Fig. 4;
- RA-5 (Ellsberry) at [0003], [0010-0012], [0018], [0026], [0028-0032], [0033-0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042-0043], [0045], [0047], [0052], [0053-0056], [0057], Figs 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13;
- RA-6 (Halbert) at 2:6-60, 4:23-5:5, 5:6-22, 5:40-50, 7:31-53, 7:54-61, 9:20-35, Figs. 4, 7, 8 ;
- RA-7 (Bhakta) at 25:11-26:19, Figs. 6C, 6D;

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- RA-8 (Chen) at 1:22-2:52, 4:3-31, Figs. 1A, 1B;
- RA-9 (Kuroki) at 1:16-33, 2:52-3:52, 4:23-37, 4:38-5:20, 5:12-44, 6:10-28, 6:29-34, 6:49-54, 7:41-67, 8:45-50, Figs. 3, 4A, 4B;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 5:22-30, 5:47-58, 6:18-26, 10:27-41;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number*

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2135.01 at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42; RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4;
- RA-28 (Xilinx) at 227-229;
- RA-29 (Xilinx) at 18.

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- RA-35 (Shaeffer) at Ex. A-21 at [1k] and [14l].
- RA-36 (Muralimanohar) at Ex. A-22 at [1k] and [14l].
- RA-37 (Karamcheti) at Ex. A-23 at [1k] and [14l].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a first predetermined amount that is determined based at least on signals received by the first data buffer during one or more previous operations, or where before receiving the input C/A signals corresponding to the memory read operation at the module control device, the first predetermined amount is determined based at least on signals received by the first data buffer. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at [0028], [0090-0091], [0104], [0117], [0120-0129], [0135-0136], [0139], [0140], [0147], [0148-0150], [0160], [0163], Figs. 5, 13, 15;
- RA-3 (Butt) at [0005], [0017-0018], [0022], [0033], [0034-0035], [0036], [0037], [0044], [0045], [0046], [0048-0061], Figs. 2, 3A, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at 2:13-18, 2:54-59, 6:17-28, 9:33-40, 13:30-37, 16:18, 16:43-46, 18:53-65, Figs. 5, 6, 7, 10, 11;
- RA-5 (Ellsberry) at [0033-0034];
- RA-6 (Halbert) at 2:6-60, 5:66-6:65, 6:66-7:20, 9:4-35, Figs. 5, 6;
- RA-7 (Bhakta) at 25:11-26:19, Figs. 6C, 6D;
- RA-8 (Chen) at 2:66-3:5, 3:6-43, 3:44-67, 4:3-7, 4:14-27, 4:64-5:11, 5:33-59, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2;

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- RA-9 (Kuroki) at Abstract, 2:23-33, 2:52-3:16, 3:17-25, 4:1-3, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 5:22-30, 5:47-58, 6:18-26, 10:27-41;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number*

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2135.01 at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4;
- RA-25 (DFi DDR PHY) at 58-59;

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- RA-26 (DFi DDR PHY) at 119-120;
- RA-27 (NXP MSC8152) at 12-84 through 12-92;
- RA-31 (Jang) at 634-35;
- RA-32 (Jang-Woo Lee) at 46-47.
- RA-35 (Shaeffer) at Ex. A-21 at [11] and [14m].
- RA-36 (Muralimanohar) at Ex. A-22 at [11] and [14m].
- RA-37 (Karamcheti) at Ex. A-23 at [1l] and [14m].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include each respective data buffer that is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks. *See, e.g.*,

- '506 patent at 1:49-60, 2:7-16, 2:17-27;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063],

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Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;

- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7,

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8, 9, Claims 1, 2, 3;

- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20,

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Committee Item Number 2171.02 at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [14b].

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- RA-36 (Muralimanohar) at Ex. A-22 at [14b].
- RA-37 (Karamcheti) at Ex. A-23 at [14b].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a second memory device in the selected rank that is configurable to output a second section of the read data and a second read strobe. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claims 1, 2;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 18;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;

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- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, 10, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:23-37, 4:38-5:20, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;

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- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10,

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11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [2a] and [15a].
- RA-36 (Muralimanohar) at Ex. A-22 at [2a] and [15a].
- RA-37 (Karamcheti) at Ex. A-23 at [2a] and [15a].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a second data buffer can be configurable to, in response to the one or more of the module control signals, delay the second read strobe by a second predetermined amount to generate

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a second delayed read strobe. *See, e.g.*,

- ’506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claim 1;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66- 20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026- 0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;

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- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, 10, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23- 33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,

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- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

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- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.

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- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097- 0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5,

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6, 7, 11, 13, 15;

- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020- 0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045- 0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49- 55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035- 0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11- 26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11- 26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43- 9:9, Figs.

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- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25- 44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
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- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
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- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15,

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16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [2c] and [15b].
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- '506 patent at 1:49-60, 1:61- 67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083- 0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110- 0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005- 0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029- 0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;

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- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53- 57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38- 46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;

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- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB*-DIMM *Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5,

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6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [2d] and [15b].
- RA-36 (Muralimanohar) at Ex. A-22 at [2d] and [15b].

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- RA-37 (Karamcheti) at Ex. A-23 at [2d] and [15b].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a second data buffer can be "configurable to, in response to the one or more of the module control signals, transmit the second section of the read data to a second section of the data bus. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134- 0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;

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- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047- 0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55- 65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46- 58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52- 3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;

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- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43- 55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84- 85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-

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7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [2e] and [15b].
- RA-36 (Muralimanohar) at Ex. A-22 at [2e] and [15b].
- RA-37 (Karamcheti) at Ex. A-23 at [2e] and [15b].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the second predetermined amount can be determined based at least on signals received by the second data buffer during one or more previous operations. *See, e.g.*,

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- ’506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078- 0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103- 0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010- 0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8,

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4:23-35, 4:36-59, 4:60-5:50, 5:66- 6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;

- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12- 34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64- 4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-

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64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;

- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9- 16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;

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- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [2f] and [15c].
- RA-36 (Muralimanohar) at Ex. A-22 at [2f] and [15c].
- RA-37 (Karamcheti) at Ex. A-23 at [2f] and [15c].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a third memory device in the selected rank can be configurable to output a third section of the read data and a third read strobe. *See, e.g.*,

- ’506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055- 0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087- 0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117- 0119], [0120-0131], [0134-0136],

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[0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claims 1, 2;

- RA-3 (Butt) at Abstract, [0002], [0003], [0005- 0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029- 0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 18;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33- 40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040- 0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61- 2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18- 21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35,

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4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;

- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53- 2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;

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- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19,

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QBM Doubling DDR Memory Bandwidth at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [3a] and [16a].
- RA-36 (Muralimanohar) at Ex. A-22 at [3a] and [16a].
- RA-37 (Karamcheti) at Ex. A-23 at [3a] and [16a].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that each of the first section, the second section, and the third section of the read data can be 4-bit wide. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092- 0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 10, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A,

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3B, 4, 5, 6, 7;

- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028- 0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:40-60, 1:61-2:5, 2:6-60, 3:5-6, 3:11- 14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 8:63- 9:3, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23- 33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:13-30, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A,

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4B, 5, 7, 8, 9, Claims 1, 2, 3;

- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20,

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Committee Item Number 2171.02 at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [3b].

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- RA-36 (Muralimanohar) at Ex. A-22 at [3b].
- RA-37 (Karamcheti) at Ex. A-23 at [3b].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a first data buffer can be further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals, delay the third read strobe by a third predetermined amount to generate a third delayed read strobe. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-

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56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;

- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010- 0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037- 0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66- 6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12- 34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87,

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88, 119, 120, 139, 141;

- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64- 4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9- 16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at

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2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [3c], [3d], and [16b].
- RA-36 (Muralimanohar) at Ex. A-22 at [3c], [3d], and [16b].
- RA-37 (Karamcheti) at Ex. A-23 at [3c], [3d], and [16b].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a first data buffer can be further coupled to the third memory device and is further

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configurable to, in response to the one or more of the module control signals, sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe. *See, e.g.*,

- ’506 patent at 1:49-60, 1:61- 67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083- 0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110- 0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005- 0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029- 0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53- 57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-

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0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;

- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38- 46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10,

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4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,

- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB*-DIMM *Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee*

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Item Number 2222.01 at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [3e] and [16b].
- RA-36 (Muralimanohar) at Ex. A-22 at [3e] and [16b].
- RA-37 (Karamcheti) at Ex. A-23 at [3e] and [16b].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a first data buffer can be further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals, transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus. *See, e.g.*,

- ’506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;

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- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083- 0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110- 0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005- 0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029- 0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53- 57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62- 67, 8:1-48, 9:4-

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35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;

- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38- 46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1,

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20;

- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33,

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35, 36, 37, 42;

- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [3f] and [16b].
- RA-36 (Muralimanohar) at Ex. A-22 at [3f] and [16b].
- RA-37 (Karamcheti) at Ex. A-23 at [3f] and [16b].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a third predetermined amount can be determined based at least on signals received by the first data buffer during one or more previous operations. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050- 0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2,

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3, 4, 5, 6, 7, 11, 13, 15;

- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33- 40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040- 0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61- 2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18- 21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33- 59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9,

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Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;

- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53- 2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision*

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3.0 at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology*

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Overview at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [3g] and [16c].
- RA-36 (Muralimanohar) at Ex. A-22 at [3g] and [16c].
- RA-37 (Karamcheti) at Ex. A-23 at [3g] and [16c].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that each of the first section and the second section of the read data can be 4-bit wide, and that the at least one respective memory device in each of the multiple rank can include one memory device having a bit width of 8 or two memory devices each having a bit width of 4. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075- 0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 10, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032],

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[0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;

- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22- 2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:40-60, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 6:63-9:3, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65- 67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22- 2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64- 7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28,

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6:29-34, 6:42-48, 6:49- 54, 7:13-30, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;

- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4- 12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4- 66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91,

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143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.

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- RA-35 (Shaeffer) at Ex. A-21 at [5].
- RA-36 (Muralimanohar) at Ex. A-22 at [5].
- RA-37 (Karamcheti) at Ex. A-23 at [5].

It was well-known to one of skill in the art before the time of the '506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first data buffer can include circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0090-0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134- 0136], [0139], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 1;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62- 5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18,

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16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66- 20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;

- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026- 0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16- 22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23- 33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23,

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24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;

- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82,

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83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [11].
- RA-36 (Muralimanohar) at Ex. A-22 at [11].
- RA-37 (Karamcheti) at Ex. A-23 at [11].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement

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contentions, that the first section of the read data can be 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050- 0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 10, 11, 13, 15;
- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010- 0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037- 0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049],

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[0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;

- RA-6 (Halbert) at Abstract, 1:16-19, 1:40-60, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60- 5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 8:63-9:3, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1- 42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23- 47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:13-30, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-

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11, 4.20.4-12, 4.20.4-13, 4.20.4- 14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,

- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1- 9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84- 85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10,

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Committee Item Number 2222.01 at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;

- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [12].
- RA-36 (Muralimanohar) at Ex. A-22 at [12].
- RA-37 (Karamcheti) at Ex. A-23 at [12]

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the memory devices can be selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory. *See, e.g.*,

- ’506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017],

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[0018- 0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058- 0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120- 0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15;

- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0011], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62- 5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66- 20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0004], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026- 0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;

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- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16- 22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:60-5:24, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;
- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23- 33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;

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- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;

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- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;
- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [13].
- RA-36 (Muralimanohar) at Ex. A-22 at [13].
- RA-37 (Karamcheti) at Ex. A-23 at [13].

It was well-known to one of skill in the art before the time of the ’506 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the data buffers further can include a second data buffer, and a second memory device in the selected rank can be coupled to the second data buffer and is configurable to output a second section of the read data and a second read strobe. *See, e.g.*,

- ’506 patent at 1:49-60, 1:61- 67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075-0076], [0078-0080], [0083- 0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110- 0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5,

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6, 7, 11, 13, 15;

- RA-3 (Butt) at Abstract, [0002], [0003], [0005- 0006], [0008-0009], [0013-0014], [0015-0019], [0020-0022], [0023], [0024], [0025-0028], [0029- 0032], [0033-0036], [0037], [0038], [0044], [0045-0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53- 57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047-0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55-65, Figs. 1, 4, 5, 6, 7, 8, 9, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38- 46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:34-35, 4:64-5:11, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9,

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Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;

- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52-3:52, 4:1-3, 4:23-47, 4:48-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision*

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3.0 at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84-85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11,

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12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM Informational Showing Item #1341* at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Ex. A-21 at [15a].
- RA-36 (Muralimanohar) at Ex. A-22 at [15a].
- RA-37 (Karamcheti) at Ex. A-23 at [15a].

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time that the disclosures relating to memory devices and circuitry could be integrated into memory modules.

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*,

- '506 patent at 1:49-60, 1:61-67, 2:7-16, 2:17-27, 2:28-36;
- RA-2 (Hirashi) at Abstract, [0004], [0006], [0010-0011], [0013-0014], [0017], [0018-0019], [0028], [0045-0046], [0047], [0048], [0049], [0050-0053], [0054], [0055-0056], [0058-0062], [0065], [0069], [0073], [0075- 0076], [0078-0080], [0083-0085], [0087-0088], [0091], [0092-0093], [0095-0096], [0097-0100], [0102], [0103-0108], [0110-0015], [0117-0119], [0120-0131], [0134-0136], [0140], [0147], [0148-0150], [0155], [0160], [0163], [0170], Figs. 1, 2, 3, 4, 5, 6, 7, 11, 13, 15, Claims 1, 2;

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- RA-3 (Butt) at Abstract, [0002], [0003], [0005-0006], [0008-0009], [0013-0014], [0015-0019], [0020- 0022], [0023], [0024], [0025-0028], [0029-0032], [0033-0036], [0037], [0038], [0044], [0045- 0047], [0048-0061], [0063], Figs. 1, 2, 3A, 3B, 4, 5, 6, 7, Claim 18;
- RA-4 (Tokuhiro) at Abstract, 1:15-20, 1:22-2:23, 2:29-49, 2:54-59, 2:62-3:8, 3:16-26, 3:53-63, 4:62-5:41, 5:42-6:6, 6:7-16, 6:17-35, 6:45-51, 7:34-43, 7:55-8:58, 9:12-26, 9:33-40, 9:53-57, 13:16-29, 13:30-37, 14:11-48, 15:32-16:7, 16:18, 16:43-46, 17:23-29, 18:15-35, 18:53-65, 19:40-46, 19:66-20:38, 20:48-56, 22:6-52, 24:49-55, 25:66-26:4, Figs. 1, 2, 4, 5, 6, 7, 10, 11, 12, 14, 19;
- RA-5 (Ellsberry) at Abstract, [0002-0003], [0005], [0010-0012], [0018-0019], [0021], [0023], [0026-0027], [0028-0033], [0034], [0035-0036], [0037-0038], [0039], [0040-0041], [0042], [0044], [0045-0046], [0047- 0048], [0049], [0050-0051], [0052-0056], [0057], Figs. 1, 2, 3, 4, 5, 6, 7A, 8A, 8B, 9, 11, 13, Claims 1, 9, 18;
- RA-6 (Halbert) at Abstract, 1:16-19, 1:61-2:5, 2:6-60, 3:5-6, 3:11-14, 3:32-4:8, 4:23-35, 4:36-59, 4:60-5:50, 5:66-6:65, 6:66-7:20, 7:31-61, 7:62-67, 8:1-48, 9:4-35, 9:36-54, 9:55- 65, Figs. 1, 4, 5, 6, 7, 8, 9, 10, Claim 4;
- RA-7 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46- 58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 8:65-67, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B; 6C, 6D, Table 2;
- RA-8 (Chen) at Abstract, 1:22-2:52, 2:53-3:5, 3:6-43, 3:44-67, 4:3-31, 4:23-37, 4:38-5:20, 5:33-59, 5:60-6:24, 6:25-63, 6:64-7:33, 7:34-67, 8:1-42, 8:43-9:9, Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 6, 7A, 7B, 8, Claims 1, 2, 3, 11, 16, 17;

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- RA-9 (Kuroki) at Abstract, 1:13-14, 1:16-33, 1:39-52, 1:53-2:4, 2:5-22, 2:23-33, 2:34-48, 2:52- 3:52, 4:1-3, 4:23-47, 4:38-5:11, 5:12-34, 5:35-44, 5:45-6:9, 6:10-28, 6:29-34, 6:42-48, 6:49-54, 7:41-67, 8:45-55, 9:25-44, Figs. 3, 4A, 4B, 5, 7, 8, 9, Claims 1, 2, 3;
- RA-10 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 29, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 71, 72, 77, 85, 87, 88, 119, 120, 139, 141;
- RA-11 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, 1, 3, 6, 13, 18, 22, 23, 24, 25, 26, 27-31, 37, 33, 34, 42, 43, 44, 48-54, 56, 57, 58-67, 91, Fig. 4, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-21, 4.20.4-29, 4.20.4-31, 4.20.4-35, 4.20.4-66, 4.20.4-73,
- RA-12 (Lee) at 3:49-63, 3:64-4:8, 4:66-5:20, 5:22-30, 5:43-58, 6:18-26, 6:48-64, 7:11-20, 7:43- 55, 8:1-9, 8:33-52, 9:13-22, 9:46-53, 10:27-41, Figs. 1, 2, Claims 1, 20;
- RA-13 (SK Hynix FBGA) at *FBGA Specification* at 3, 5, 6, 7, 9, 10, 11, 15, 30, 86, 89, 128;
- RA-14 (Elpida DDR3 SDRAM) at *DDR3 SDRAM User's Manual* at 7, 8, 9, 12, 13, 14, 15;
- RA-15 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 41, 51, 57, 58-59,

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64, 78, *AMB Specification* at 13, 15, 16, 17, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 75, 76, 81, 90, 91, 143, 145, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RA-16 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 142.62B* at 1, 2, 3, 4, 5, 8, 9-16, 17, 18-19, 21, 22, 23-29, 30, 31-33, 34, 35, 36, 59, 60, 82, 83, 84- 85, 91, 92-100, 126-168, 216, 218, *Committee Item Number 158.01* at 2, *Committee Item Number 158.02* at 5, *Committee Item Number 0311.12* at 3, 4, 5-7, 8, 10, 11, 12, 13, 14, 15-17, 19, 22, 23, 24, 25-28, *Committee Item Number 0311.13* at 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, *Committee Item Number 0311.14* at 3, 4, 5, 6, 7, 8, 9, 10, *JC-40 Meeting No. 169 Minutes* at 9, 10, *Committee Item Number 2222.01* at 2, *Committee Item Number 2222.03* at 2, 7, *Committee Item Number 2192.62* at 4, 6, 7-11, 12, 26, 27-30, 34, 35, 36, 37;
- RA-17 (Lattice DDR3) at *Lattice DDR3 White Paper* at 2, 3, 4, 5, 6, 7, 8;
- RA-18 (NXP DDR) at *NXP DDR Presentation* at 7, 8, 9, 10, 11, 12, 13, 26, 33, 35, 36, 37, 42;
- RA-19 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 9, 10, 11, 12, 16, 19, 20, 21, 26, 27, 32, 34, 36, 37, 42, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, 9, 15, *QBM2 Technical Features Overview* at 3, 5, 8, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, 25, *QBM Interim JEDEC Meeting* at 6, 11, 20, 22, *QBM*

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Informational Showing Item #1341 at 3, 9, 15;

- RA-20 (MORPHEUS SDRAM Controller) at 1, 2, 3, 4, 5, 6, 7, Figs. 1, 2, 3, 4.
- RA-35 (Shaeffer) at Figs. 5, 18, 31, 38, 3:26–39, 4:18–42, 5:11–31, 6:32–47, 9:29–51. 31:58–33:33, 35:40–36:6, 40:40–42:7.
- RA-36 (Muralimanohar) at Figs. 1, 2, 4, 9, 4:6–67, 5:1–58, 6:25–53, 7:5–8:25, 10:62–11:9, 24:23–44, and 28:6–27.
- RA-37 (Karamcheti) at Figs. 1–6, 13, and accompanying disclosures, 1:8–32, 2:40–3:48, 8:63–9:26, 18:1–13.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the ’506 Patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the Asserted Claims are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the ’506 Patent. See ’506 patent at 1:43-2:36; 9:19-26.

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Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '506 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix A for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

b) *Obviousness Combinations*

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix A with any other reference or references listed in Appendix A along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '506 patent. For example, and without limitation, the Asserted Claims of the '506 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
Asserted Patent's Admitted Prior Art (APA) (RA-1)	• U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2010/0312956 Hirashi (RA-2)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2007/0008791 Butt (RA-3)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,020,022 Tokuhiro (RA-4)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2006/0277355 Ellsberry (RA-5)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,024,518 Halbert (RA-6)	• Asserted Patent's Admitted Prior Art (APA) (RA-1);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,289,386 Bhakta (RA-7)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,391,089 Chen (RA-8)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,111,565 Kuroki (RA-9)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
JEDEC FBDIMM Standards (RA-10)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
JEDEC SDRAM/DIMM Standards (RA-11)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,001,434 (Lee) (RA-12)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
SK hynix FBGA (RA-13)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
Elpida DDR3 SDRAM (RA-14)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
JEDEC FBDIMM Proposals (RA-15)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
JEDEC SDRAM/DIMM Proposals (RA-16)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
Lattice DDR3 (RA-17)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
NXP DDR (RA-18)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
Kentron's QBM (RA-19)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
MORPHEUS SDRAM Controller (RA-20)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• The knowledge of a person of ordinary skill.
U.S. Patent No. 7,562,271 (Shaeffer) (RA-35)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 8,806,116 (Karamcheti) (RA-37); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,806,116 (Karamcheti) (RA-37)	• Asserted Patent's Admitted Prior Art (APA) (RA-1); • U.S. Patent App. Pub. No. 2010/0312956 (Hirashi) (RA-2); • U.S. Patent App. Pub. No. 2007/0008791 (Butt) (RA-3); • U.S. Patent No. 8,020,022 (Tokuhiro) (RA-4); • U.S. Patent No. 8,391,089 (Chen) (RA-8); • U.S. Patent No. 8,111,565 Kuroki (RA-9); • JEDEC FBDIMM Standards (RA-10); • JEDEC SDRAM/DIMM Standards (RA-11); • U.S. Patent No. 8,001,434 (Lee) (RA-12); • Elpida DDR3 SDRAM (RA-14); • JEDEC FBDIMM Proposals (RA-15); • JEDEC SDRAM/DIMM Proposals (RA-16); • Kentron's QBM (RA-19); • MORPHEUS SDRAM Controller (RA-20); • Altera 1 (RA-21); • DFi DDR PHY1 (RA-25); • U.S. Patent No. 7,562,271 (Shaeffer) (RA-35); • U.S. Patent No. 9,361,955 (Muralimanohar) (RA-36); and/or • The knowledge of a person of ordinary skill.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the

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scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

2. U.S. Patent No. 10,949,339

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix B the prior art references that render obvious the Asserted Claims of the '339 patent and include below exemplary combinations showing the obviousness of the '339 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix B, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of skill in the art at the time of the '339 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix B, such reference may be combined with any other references listed in Appendix B for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '339 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '339 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

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a) *Obviousness Rationale*

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix B along with the knowledge of one of ordinary skill in the art to meet the limitations of the '339 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '339 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. See KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." Id. at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix B would have been obvious because these references would have been combined using: known methods

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to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix B would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the '339 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix B is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known

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technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of skill in the art to consult and/or combine any of the prior art listed in Appendix B because all of these references relate to the same area of technology and/or are from analogous art. The ’339 patent Asserted Claims are directed to a memory module with circuitry to control the transmission of data signals. ’339 patent at Abstract. The ’339 patent Asserted Claims merely unite old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the ’339 patent Asserted Claims.

All of the ’339 patent Asserted Claims are directed to a memory modules configurable to control the transmission of data signals. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, was widely known before the alleged priority date of the ’339 Patent, as evidenced by the references in Appendix B. *See, e.g.*,

- ’339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0049], [0051-0052], Fig. 2, 6, 11;

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- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 4:49-5:14, 7:31-61, 8:63-9:3, 9:36-54, Figs. 4, 7;
- RB-4 (Solomon) at 31:45-56, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28- 9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53- 12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1- 5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59- 3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53- 64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3- 38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20- 31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;

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- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30- 63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34- 42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24- 25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3,

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JC-45 Meeting No. 22 Minutes at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21

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- RB-26 (Karamcheti) at Abstract, [0002]-[0004], [0021]-[0022], [0150]-[0152], FIGS. 1-5 (and related disclosures);

RB-27 (Shaeffer) at Ex. Abstract, [0003], FIGS. 5-8, 9A-C, 18, 19, 36 (and related disclosures).One of ordinary skill in the art would have been motivated to combine any of the references in Appendix B because at the time of the alleged invention controlling transmission of data signals in memory modules was a common problem with a well-known solution. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0049], [0051-0052], Fig. 2, 6, 11;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 4:49-5:14, 7:31-61, 8:63-9:3, 9:36-54, Figs. 4, 7;
- RB-4 (Solomon) at 31:45-56, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7- 28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;

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- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110,

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JESD82-20 at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;

- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4,

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5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21.
- RB-26 (Karamcheti) at Abstract, [0002]-[0004], [0021]-[0022], [0150]-[0152], FIGS. 1-5 (and related disclosures);
- RB-27 (Shaeffer) at Ex. Abstract, [0003], FIGS. 5-8, 9A-C, 18, 19, 36 (and related disclosures).

Further, it was common knowledge to one of skill in the art at the time of the alleged invention that controlling the transmission of data signals can improve performance of the memory module. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0049], [0051-0052], Fig. 2, 6, 11;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 4:49-5:14, 7:31-61, 8:63-9:3, 9:36-54, Figs. 4, 7;
- RB-4 (Solomon) at 31:45-56, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20- 30, 4:20-47, 4:48-65, 5:7-28,

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5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1- 5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59- 3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53- 64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3- 38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20- 31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30- 63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13- 18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

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- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34- 42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24- 25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64,

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78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21.
- RB-26 (Karamcheti) at Abstract, [0002]-[0004], [0021]-[0022], [0150]-[0152], [0034], [0057], [0068], FIGS. 1-5 (and related disclosures);
- RB-27 (Shaeffer) at Ex. Abstract, [0003], FIGS. 5-8, 9A-C, 18, 19, 36 (and

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related disclosures).

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix B at the time of the alleged invention. Common problems with conventional techniques for controlling the transmission of data signals in memory modules were known to persons of ordinary skill in the art and incorporating circuitry in the memory modules directed to controlling data signal transmission was a well-known solution to achieve improved performance. *See, e.g.*,

- '339 patent at 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010- 0012], [0028-0033], [0039-0040], [0042], [0044-0046], [0050], [0052], [0054], [0056-0057], Fig. 1-2, 4, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 6:40- 7:20, 7:31-67, 9:4-65, Figs. 3-9;
- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59- 8:34, 8:48-9:5, 21:28-54, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20- 47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;

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- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 2B* at 11, 12, 22, 23-29, *JESD79-2A* at 14, 24, 25, 26-32, *JESD79-3C* at 23, 24, 26, 22, 25, 27-31, 91;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 11, 16, 29, 30, 31, 32, 40, 46, 63, 70, 71- 73, 80, 81-83, *JESD82-20* at 1, 2, 3, 4, 6, 7, 11, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 68, 71, 72, 104, 154, 155, 160, 161;

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- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4,

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5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-24 (Kingston FBDIMM) at 1-2;
- RB-25 (Hongzhong Zheng) at 212-13.
- RB-26 (Karamcheti) at Abstract, [0002]-[0004], [0021]-[0022], [0150]-[0152], [0034], [0057], [0068], FIGS. 1-5 (and related disclosures);
- RB-27 (Shaeffer) at Ex. Abstract, [0003], FIGS. 5-8, 9A-C, 18, 19, 36 (and related disclosures).

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be N-bit-wide, mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, and that "each set of data signal lines is a byte wide or n bit wide. *See, e.g.*,

- '339 patent at 1:24-62, 4:38-47, 4:48-5:3, 5:4-22, Figs. 1A, 1B;

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- RB-2 (Ellsberry) at Abstract, [0002-0003], [0011], [0014], [0021], [0023], [0026-0027], [0028-0031], [0034], [0047-0051], [0052], [0054], [0056], Figs. 1-5, 11, 13;
- RB-3 (Halbert) at Abstract, 1:16-20, 2:6-20, 3:5-6, 3:11-14, 3:32-4:8, 4:23-5:5, 5:6-39, 5:66-6:28, 7:31-61, 8:1- 48, claim 4, Figs. 1, 4, 7-8;
- RB-4 (Solomon) at 1:34-42, 2:42-50, 4:56-5:2, 5:21-24, 15:7-25, Fig. 1;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055- 0069], [0070-0108], [0112-0113], Claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12- 2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, Claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35,

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7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at 1, 42, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 11, 12, 16, 37, 38, 39, 40, 110, *JESD82-20* at 1;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24- 25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

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- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21.
- RB-26 (Karamcheti) at Ex. R-24 at [1pre];

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- RB-27 (Shaeffer) at Ex. R-25 at [1pre].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket. *See, e.g.*,

- '339 patent at 1:24-36;
- RB-2 (Ellsberry) at [0002-0003], [0021], [0027], [0028-0031], [0047-0051], Figs. 2, 5-6;
- RB-3 (Halbert) at 1:16-19, 1:61-2:14, Figs. 1, 7, 8;
- RB-4 (Solomon) at 1:34-42, 15:7-25, 15:60-67;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37- 60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42- 60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8- 63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;

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- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JEDEC 21-C* at 4.20.4-6, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79-3C* at 3;
- RB-15 (JEDEC FBDIMM Standards) at *JESD82-20* at 6, 43, 77, *JESD205* at 10, 12, 37, 38, 39, 40, 84;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee*

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Item Number 2192.05 at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

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- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [1a], [11a];
- RB-27 (Shaeffer) at Ex. R-25 at [1a], [11a].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks, and that each N-bit-wide rank includes n DDR DRAM devices. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, Figs. 1A, 1B;
- RB-2 (Ellsberry) at [0003], [0026], [0028-0032], [0040], [0046-0050], [0052], [0054], [0056], Figs. 2, 5-6, 11, 13;
- RB-3 (Halbert) at 4:36-39, 4:49-59, 5:6- 22, 7:31-53, 7:54-61, 9:20-35, 9:55-65, claim 4, Figs. 1, 4, 7-8;
- RB-4 (Solomon) at 1:34-42, 2:24- 30, 4:56-5:2, 5:40-47, 5:64-6:3, 15:7-25, 16:1-9, Fig. 1;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

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- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024- 0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62- 9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79* at cover, *JEDEC 21-C* at

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cover, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, *JESD79-2B* at cover, 6, *JESD79-2A* at cover, 6, *JESD79-3C* at cover;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 13, 14, 15, 16, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, *JESD82-20* at 1;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3,

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4, 5, 6, 11, Table 11;

- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [1b]. [11b];
- RB-27 (Shaeffer) at Ex. R-25 at [1b], [11b].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include DDR DRAM devices configurable to perform the memory write operation by receiving write data in response to the first registered address and control signals, and to perform the memory read operation by outputting read data in response to the second registered address and control signals. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48- 5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0028-0033],

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[0035-0036], [0037], [0039], [0040], [0042], [0045-0050], [0052], [0054], [0056], 8A, 8B, Figs. 2-7, 11, 13;

- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48- 7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55,

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2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07*

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at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing*

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Item #1341 at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [27c];
- RB-27 (Shaeffer) at Ex. R-25 at [27c].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0028- 0033], [0035-0036], [0037], [0039], [0042], [0045], [0047], [0049], [0052], [0054],

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[0056], 8A, 8B, Figs. 2-7, 11, 13;

- RB-3 (Halbert) at 4:36-48, 5:23-39, 6:15-28, 6:66-7:20, 7:31-53, 8:19-32, Figs. 4, 6-8, 10;
- RB-4 (Solomon) at 2:42-50, 4:56-5:2, 6:4-18, 6:63-7:18, 15:7-49, 16:10-18, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055- 0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

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- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79* at 13, *JESD79* at 17, 26, *JEDEC 21-C* at 4.20.4-6, 4.20.4-29, 4.20.4-35, *JESD79-2B* at 46, 21-30, *JESD79-2A* at 24-33, 48, 49, *JESD79-3C* at Fig. 4, 56, 57, 42, 3;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 11, 13, 14, 15, 16, 29, 30, 31, 32, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, *JESD82-20* at 1, 3, 4, 11, 19, 20, 21;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting*

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No. 22 Minutes at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;

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- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21
- RB-26 (Karamcheti) at Ex. R-24 at [1c];
- RB-27 (Shaeffer) at Ex. R-25 at [1c].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals. *See, e.g.*,

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- ’339 patent 1:24-36, 1:37- 51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0028-0033], [0035-0036], [0037], [0039], [0040], [0042], [0045-0050], [0052], [0054], [0056], 8A, 8B, Figs. 2-7, 11, 13;
- RB-3 (Halbert) at 4:36-48, 5:23- 39, 5:66-6:65, 6:66-7:20, 7:31-53, 8:19-32, Figs. 4, 6-8, 10;
- RB-4 (Solomon) at 2:42-50, 4:56-5:2, 6:4-18, 6:63-7:18, 15:7-49, 16:10-18, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28- 9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53- 12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1- 5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;

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- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59- 3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53- 64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3- 38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20- 31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30- 63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13- 18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34- 42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, JESD79 at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43- 55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;

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- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory*

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Bandwidth at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [19c];
- RB-27 (Shaeffer) at Ex. R-25 at [19c].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a module controller coupled to the PCB and configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals. *See, e.g.*,

- '339 patent at 1:24- 36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0028-0033],

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[0035-0036], [0037], [0039], [0042], [0045], [0047], [0049], [0052], [0054], [0056], 8A, 8B, Figs. 2-7, 11, 13;

- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 2:42-50, 4:56-5:2, 6:4-18, 6:63-7:18, 13:5-49, 15:7-49, 16:10-18, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37- 60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42- 60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8- 63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

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- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item*

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Number 2192.14 at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17,

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18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [27b];
- RB-27 (Shaeffer) at Ex. R-25 at [27b].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines. *See, e.g.*,

- '339 patent at 1:24-36, 6:65-7:14, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0011], [0028-0033], [0042], [0045], [0047], [0050], [0052], [0054], [0056], Figs. 2-6, 8A, 8B, 11-13;
- RB-3 (Halbert) at Abstract, 3:42-57, 4:23-5:50, 6:40-7:20, 7:31-55, 7:62-67, 9:4-54, Figs. 4, 7-9;
- RB-4 (Solomon) at 5:32-39, 6:19-26, 6:48-7:3, 7:59-8:34, 8:48-9:5, 15:7-49, Fig.

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9A;

- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37- 60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42- 60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8- 63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18,

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6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JEDEC 21-C* at 4.20.4-8, 4.20.4-9, *JESD79-3C* at 13, 23, 24, 26, 22, 25, 27-31, 91, *JESD79-2B* at 11, 12, 22, 23-29, *JESD79-2A* at 14, 24, 25, 26-32;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 11, 13, 14, 15, 16, 29, 30, 31, 32, 37, 38, 39, 40, 46, 63, 70, 71-73, 80, 81-83, *JESD82-20* at 1, 3, 4, 11, 19, 20, 21;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93,

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128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [1d];
- RB-27 (Shaeffer) at Ex. R-25 at [1d].

It was well-known to one of skill in the art before the time of the '339 patent, at least

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partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the each respective byte-wise buffer can further include logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period. *See, e.g.*,

- '339 patent at 6:65- 7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0028-0033], [0039-0040], [0042], [0044-0046], [0050], [0052], [0054], [0056-0057], Fig. 1-2, 4, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 6:40-7:20, 7:31-67, 9:4-65, Figs. 3-9;
- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36- 6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28- 56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22- 55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57,

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claims 1, 2, 11-13, Figs. 1-4;

- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-2B* at 11, 12, 22, 23-29, *JESD79-2A* at 14, 24, 25, 26-32, *JESD79-3C* at 23, 24, 26, 22, 25, 27-31, 91;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 11, 16, 29, 30, 31, 32, 40, 46, 63, 70, 71-73, 80, 81-83, *JESD82-20* at 1, 2, 3, 4, 6, 7, 11, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 68, 71, 72, 104, 154, 155, 160, 161;

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- RB-16 (Lee) at 4:66-5:20, 5:30- 37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15,

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QBM2 Technical Highlights at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-24 (Kingston FBDIMM) at 1-2;
- RB-25 (Hongzhong Zheng) at 212-13;
- RB-26 (Karamcheti) at Ex. R-24 at [1e];
- RB-27 (Shaeffer) at Ex. R-25 at [1e].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the byte-wise data path can include first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period. *See, e.g.*,

- '339 patent at 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0027-0033], [0044-0046], [0050], [0052], [0054], [0056-0057],Fig. 1-2, 4, 8A, 9, 11-13;
- RB-3 (Halbert) at 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 6:40-7:20, 7:31-67, 9:4-65, Figs. 3-9;

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- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36- 6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22- 55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14,

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4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-2B* at 11, 12, 22, 23-29, *JESD79-2A* at 14, 24, 25, 26-32, *JESD79-3C* at 23, 24, 26, 22, 25, 27-31, 91;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 11, 16, 29, 30, 31, 32, 40, 46, 63, 64-65, 70, 71-73, 80, 81- 83, *JESD82-20* at 1, 2, 3, 4, 6, 7, 11, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 40, 41, 42, 43, 45, 48, 59, 62, 64, 65, 66, 67, 68, 71, 72, 104, 154, 155, 160, 161;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59,

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64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-24 (Kingston FBDIMM) at 1-2;
- RB-25 (Hongzhong Zheng) at 212-13;
- RB-26 (Karamcheti) at Ex. R-24 at [1f];

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- RB-27 (Shaeffer) at Ex. R-25 at [1f].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include n/2 data transmission circuits mounted on the PCB, wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data signal lines among the plurality of sets of data signal lines, and wherein the each of the n/2 data transmission circuits has a first side configured to be operatively coupled to the respective set of data signal lines, a second side that is operatively coupled to a respective pair of DDR DRAM devices in each of the multiple ranks via respective module data lines, and data paths between the first side and the second side. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0028-0033], [0039-0040], [0042], [0039- 0040], [0044-0046], [0049], [0050-0052], [0054], [0056-0057], Fig. 1-2, 4, 6, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at Abstract, 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:66-6:65; 6:40-7:20, 7:31-55, 7:62-67, 9:4-65, Figs. 3-4, 7-9;
- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, 15:7-49, 31:45-56, Fig. 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26- 12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

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- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6- 36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62- 9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3,

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13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59- 64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6,

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Committee Item Number 2171.07 at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [11c];
- RB-27 (Shaeffer) at Ex. R-25 at [11c].

It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that in response to the module control signals, each respective data transmission circuit” can be “configurable to enable the data paths for a first time period in accordance with a

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latency parameter to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period. *See, e.g.*,

- '339 patent at 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0050], [0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at 1:48- 52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:65-6:65; 6:40-7:20, 7:31-67, 9:4-65, Figs. 3-9;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1- 9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17- 24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12- 27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024- 0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23,

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3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;

- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62- 9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;

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- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59- 64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15,

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QBM2 Technical Highlights at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [11e];
- RB-27 (Shaeffer) at Ex. R-25 at [11e].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a first subsection of the respective section of the N-bit wide write data output from the second side of the each respective data transmission circuit can be written into a first one of the respective pair of DDR DRAM devices in the first N-bit wide rank, while a second subsection of the respective section of the N-bit wide write data output from the second side of the each respective data transmission circuit can be written into a second one of the respective pair of DDR DRAM devices in the first N-bit wide rank. *See, e.g.*,

- '339 patent at 6:65-7:14, 7:15-43, 9:3- 9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0027-0033], [0039-0040], [0042], [0044-0046], [0049-0052], [0054], [0056-0057], Fig. 1-2, 4, 6, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:65-6:66; 6:40-7:20, 7:31-67, 9:4-65, Figs. 3- 9;

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- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35- 49, 31:45-56;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;

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- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3,

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- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;

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- RB-26 (Karamcheti) at Ex. R-24 at [11f];
- RB-27 (Shaeffer) at Ex. R-25 at [11f].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the data paths can include first tristate buffers, and the respective data transmission circuit in response to the module control signals can be "configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, and to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks. *See, e.g.*,

- '339 patent at 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0027-0033], [0039-0040], [0042], [0044-0046], [0049-0052], [0054], [0056-0057], Fig. 1-2, 4, 6, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at 1:48- 52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:65-6:66; 6:40-7:20, 7:31-67, 9:4-65, Figs. 3-9;
- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, 31:45-56;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36- 6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28- 56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-

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12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22- 55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;

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- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item*

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Number 2135.01 at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [11g];
- RB-27 (Shaeffer) at Ex. R-25 at [11g].

It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include “a plurality of buffers coupled to the PCB and configured to receive the first module control signals and to receive the second module control

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signals, wherein each respective buffer of the plurality of buffers has a first side that is operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and data paths between the first side and the second-side, wherein the each respective buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0028-0033], [0039-0040], [0042], [0044-0046], [0049-0052], [0054], [0056-0057], Fig. 1-2, 4, 6, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at Abstract, 1:48-52, 2:46-60, 3:42- 57, 3:67-4:2, 4:23-5:50, 6:40-7:20, 7:31-61, 7:62-67, 8:63-9:65, Figs. 3-4, 7-9;
- RB-4 (Solomon) at 2:42-50, 4:56-5:2, 6:4-18, 6:63-7:18, 15:7-49, 16:10-18, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33- 8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070- 0108],

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[0112-0113], claim 16, Figs. 1-5, 10;

- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50- 9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33- 41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39- 6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61- 6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64- 5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10- 17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46,

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JESD79-2A at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66- 5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;

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- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [19d];
- RB-27 (Shaeffer) at Ex. R-25 at [19d].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that each respective buffer can further include "logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period,

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wherein the data paths are disabled after the first time period and before the second time period. *See, e.g.*,

- '339 patent at 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0003], [0010-0012], [0027-0033], [0039-0040], [0042], [0044-0046], [0050], [0052], [0054], [0056-0057], Fig. 1-4, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:66-6:65, 6:40-7:20, 7:31-67, 8:63-9:3, 9:4-65, Figs. 3-9;
- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, 15:7-25, 31:45-56;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims

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1, 6, 9-10, Figs. 2-5, 7-16;

- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9,

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9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;

- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11,

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12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [19e];
- RB-27 (Shaeffer) at Ex. R-25 at [19e].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include "a plurality of n-bit-wide data buffers coupled to the PCB and configured to receive the first module control signals and subsequently the second module control signals, wherein each respective n-bit-wide data buffer of the plurality of n-bit-wide data buffers has a first side that is operatively coupled to a respective set of data signal lines, and a second side that is operatively coupled to a respective n-bit-wide section of the DDR DRAM devices via respective module data lines. *See, e.g.*,

- '339 patent at 1:24-36, 6:65-7:14, 9:3-9, Figs. 2C, 2D, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B;
- RB-2 (Ellsberry) at [0003], [0010-0012], [0028-0033], [0039-0040], [0042], [0044-0046], [0049-0052], [0054], [0056-0057], Fig. 1-4, 6, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3- 10;

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- RB-4 (Solomon) at 5:32-39, 5:59-63, 6:19-26, 6:48-7:43, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35- 49, 15:7-49, 31:45-56, Fig. 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14,

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4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79- 2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1- 9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

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- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at

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7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;

- RB-26 (Karamcheti) at Ex. R-24 at [27d];
- RB-27 (Shaeffer) at Ex. R-25 at [27d].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the each respective n-bit-wide data buffer" can include "a first set of input buffers configurable to receive a respective n-bit section of the write data from the respective set of data signal lines, a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, a second set of input buffers configurable to receive a respective n-bit section of the read data from the respective module data lines, a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0010-0012], [0027-0033], [0039-0040], [0042], [0044-0046], [0049-0052], [0054], [0056-0057], Fig. 1-4, 6, 8A, 8B, 9, 11-13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23- 5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1- 9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17- 24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28,

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5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12- 27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024- 0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-

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26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;

- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79- 2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29,

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30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21
- RB-26 (Karamcheti) at Ex. R-24 at [27e];
- RB-27 (Shaeffer) at Ex. R-25 at [27e].

It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement

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contentions, that the logic in response to the first module control signals can be configured to enable the first set of tristate buffers for a first time period corresponding to the memory write operation to drive the respective n-bit section of the write data. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34- 42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28- 54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57,

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claims 1, 2, 11-13, Figs. 1-4;

- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79- 2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15,

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16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;

- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43- 55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;

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- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [27f];
- RB-27 (Shaeffer) at Ex. R-25 at [27f].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the logic in response to the second module control signals can be configured to enable the second set of tristate buffers for a second time period corresponding to the memory read operation to drive the respective n-bit section of the read data. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-

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0057], Figs. 1-7, 8A, 8B, 9, 11, 13;

- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15- 28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34- 42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28- 54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

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- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79- 2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43- 55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number*

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2192.14 at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17,

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18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [27g];
- RB-27 (Shaeffer) at Ex. R-25 at [27g].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first set of tristate buffers can be disabled during the second time period; and the second set of tristate buffers are disabled during the first time period. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027- 0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28,

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5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28- 9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53- 12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1- 5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59- 3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53- 64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3- 38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20- 31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30- 63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13- 18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34- 42, 2:46-58, 3:17-30, 5:11-

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26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;

- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26- 32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24- 25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30,

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31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [27h];
- RB-27 (Shaeffer) at Ex. R-25 at [27h].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's

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infringement contentions, that the DDR DRAM devices can each have a bit width of 4 bits, wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0049], [0051-0052], Fig. 2, 6, 11;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 4:49-5:14, 7:31-61, 8:63-9:3, 9:36-54, Figs. 4, 7;
- RB-4 (Solomon) at 31:45-56, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33- 8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070- 0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims

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1, 6, 9-10, Figs. 2-5, 7-16;

- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33- 41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39- 6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61- 6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64- 5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10- 17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9,

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9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;

- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2*

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Technical Highlights at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [2a], [20];
- RB-27 (Shaeffer) at Ex. R-25 at [2a], [20].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a first subset of the first tristate buffers can be enabled for the first time period to drive a first nibble of the respective byte-wise section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, while a second subset of the first tristate buffers" can be "enabled for the first time period to drive a second nibble of the respective byte-wise section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033],

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[0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;

- RB-3 (Halbert) at Abstract, 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, 31:45-56, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35,

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7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee*

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Item Number 2192.05 at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing*

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Item #1341 at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [2b];
- RB-27 (Shaeffer) at Ex. R-25 at [2b].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the byte-wise data path can further include a set of write buffers configurable to receive the respective byte-wise section of the N-bit wide write data from the respective set of data signal lines before the first tristate buffers regenerate and drive the respective byte-wise section of the N-bit wide data to the second side of the each respective byte-wise buffer. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:48-52, 2:46-60, 3:42-57, 3:67-4:2, 4:23-5:50, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, 31:45-56, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28,

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5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48- 10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26,

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5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;

- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29,

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30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [3];
- RB-27 (Shaeffer) at Ex. R-25 at [3].

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It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that each of the write buffers or each of the set of write buffers can be comparable or comparable in loading to an input buffer on one of the DDR DRAM devices such that the each respective byte-wise buffer” or data transmission circuit presents to the memory controller one DDR DRAM device load during the memory operation or the memory write operation. *See, e.g.*,

- ’339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056- 0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1- 9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, 31:45-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33- 8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;

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- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070- 0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50- 9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33- 41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39- 6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61- 6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64- 5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10- 17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14,

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4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, 65, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49, 63;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 47, 56, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs.

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2, 3, 4, Table 3;

- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [4], [15];
- RB-27 (Shaeffer) at Ex. R-25 at [4], [15].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the logic can be configurable to enable the first tristate buffers at a beginning of the first time period and to disable the first tristate buffers at an end of first time period. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033],

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[0035-0036], [0037], [0039-0040], [0042], [0044-0050], [0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;

- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3- 10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1- 9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4- 23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024- 0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35,

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7:36-8:47, 8:62- 9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59- 64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee*

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Item Number 2192.05 at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

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- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [6];
- RB-27 (Shaeffer) at Ex. R-25 at [6].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the module controller can be configured to use the module control signals to control timing of the first time period in accordance with the latency parameter. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0050], [0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59- 8:34, 8:48-9:5, 21:28-54, 13:35-49, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28- 9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

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- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1- 5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59- 3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53- 64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3- 38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20- 31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30- 63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13- 18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34- 42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3,

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13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43- 55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6,

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- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [7];
- RB-27 (Shaeffer) at Ex. R-25 at [7].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the registered address and control signals can include rank select signals, the rank

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select signals including one rank select signal for each of the multiple N-bit-wide ranks, and "the rank select signal received by the first N-bit-wide rank" can be different from the rank select signal received by any other N-bit-wide rank of the multiple N-bit-wide ranks. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027- 0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0050], [0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;

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- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 26, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84,

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110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;

- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13- 22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36,

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37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [8];
- RB-27 (Shaeffer) at Ex. R-25 at [8].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that each of the respective module data lines can be configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory write operation. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0050], [0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;

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- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055- 0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12- 2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48,

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3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;

- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 26, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item*

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Number 2192.22 at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;

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- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [9], [13]. [32];
- RB-27 (Shaeffer) at Ex. R-25 at [9], [13]. [32].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the module controller can be further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals for a memory read operation to read N-bit-wide read data from the memory controller from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals, the second N bit-wide rank can be configurable to output the N bit-wide read data associated with the memory read operation in response to at least some of the additional registered address and control signals, and the module controller can be further configurable to output additional module control signals in response to the additional input address and control signals. *See, e.g.*,

- '339 patent at 1:24-36, 1:37- 51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0003], [0010-0011], [0029-0031], [0040], [0045-0046], [0050], Figs. 2-4, 8-9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at 15:7- 25, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48- 9:5, 21:28-54, 13:35-49, Fig. 1, 9A;

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- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20- 47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

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- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59,

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64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [10a], [18a];

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- RB-27 (Shaeffer) at Ex. R-25 at [10a], [18a].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the logic in the each respective byte-wise buffer can be further configurable to control the byte-wise data path in response to the additional module control signals, the byte-wise data path can be enabled for a second time period to actively drive a respective byte-wise section of the N bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals, the byte-wise data path can further include second tristate buffers configurable to be enabled by the logic to drive the respective byte-wise section of the N-bit wide read data to the respective set of data signal lines during the second time period, and the second tristate buffers can be disabled during the first time period and the first tristate buffers are disabled during the second time period. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0003], [0010-0011], [0029-0031], [0040], [0045-0046], [0050], Figs. 2-4, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4- 65, Figs. 1, 3-10;
- RB-4 (Solomon) at 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-49, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33,

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9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26- 12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6- 36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 24:57-

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25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;

- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79- 2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93,

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128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [10b];
- RB-27 (Shaeffer) at Ex. R-25 at [10b].

It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the data paths can further include a set of write buffers configurable to receive

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the respective section of the N-bit wide data from the respective set of data signal lines before the respective section of the N-bit wide write data is regenerated and driven by—the first tristate buffers to the respective module data lines. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7- 28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;

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- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 26, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83,

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84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 29, 43, 77;

- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4,

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5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [14];
- RB-27 (Shaeffer) at Ex. R-25 at [14].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the each respective data transmission circuit can be configured to present to the memory controller one DDR DRAM device load on each of the respective set of data lines during the memory write operation. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63- 9:3, 9:4-65, Figs. 1, 3-10;

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- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64- 6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47,

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9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;

- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, 65, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49, 63;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 47, 56, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46- 53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6,

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Committee Item Number 2192.32 at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification*

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at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;

- RB-26 (Karamcheti) at Ex. R-24 at [17];
- RB-27 (Shaeffer) at Ex. R-25 at [17].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the each respective data transmission circuit can be further configurable to enable the data paths for a second time period to actively drive a respective section of the N-bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals, the data paths can further include second tristate buffers configurable to be enabled during the second time period to drive the respective section of the N-bit wide read data to the respective set of data signal lines, and the each respective data transmission circuit can be further configurable to keep the second tristate buffers disabled during the first time period and to keep the first tristate buffers disabled during the second time period. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65- 6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40- 60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1,

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9A;

- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14,

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4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

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- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [18b];

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- RB-27 (Shaeffer) at Ex. R-25 at [18b].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the DDR DRAM devices can each have a bit width of 4 bits, the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks can include a respective pair of DDR DRAM devices, and a first nibble of the respective section of the first N bit wide data can be output by a first one of the respective pair of DDR DRAM devices in the first N-bit wide rank, while a second nibble of the respective section of the first N bit wide data is output by a second one of the respective pair of DDR DRAM devices in the first N-bit wide rank. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056- 0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1- 9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17- 24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12- 27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

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- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024- 0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62- 9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3,

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13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79- 2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee*

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Item Number 2171.07 at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-(Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-(Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [20];
- RB-27 (Shaeffer) at Ex. R-25 at [20].

It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the module controller can be configured to use the first module control signals to control timing of the first time period in accordance with a latency parameter and to use the second module control signals to control timing of the second time period in accordance with the latency

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parameter. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6- 60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48- 7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;

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- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110,

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JESD82-20 at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;

- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4,

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5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [21];
- RB-27 (Shaeffer) at Ex. R-25 at [21].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the each respective buffer can be configured to present to the at least one respective DDR DRAM device a load that is similar to that of the memory controller during the first or the second memory operation. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;

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- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7- 28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14,

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4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;

- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, 65, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49, 63;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 47, 56, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13- 22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

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- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at

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7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;

- RB-26 (Karamcheti) at Ex. R-24 at [22];
- RB-27 (Shaeffer) at Ex. R-25 at [22].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first registered address and control signals can include a first set of rank select signals corresponding to respective ones of the multiple N-bit wide ranks, the first set of rank select signals including a first rank select signal received by the first N-bit wide rank that is different from each of the other rank select signals in the first set of rank select signals, and the second registered address and control signals can include "a second set of rank select signals corresponding to respective ones of the multiple N-bit wide ranks, the second set of rank select signals including a second rank select signal received by the second N-bit wide rank that is different from each of the other rank select signals in the second set of rank select signals. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056- 0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1- 9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig.

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1, 9A;

- RB-5 (Raynham) at Abstract, 1:17- 24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12- 27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024- 0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40- 3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32- 55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62- 9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41- 8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38- 2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57- 6:12, 6:13-18, 6:19-

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34, 6:35-54, Figs. 1, 2, Claims 1, 12;

- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47- 7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79- 2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 26, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 6, 11, 19, 20, 21, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30- 37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision*

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3.0 at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-(Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-(Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [23];
- RB-27 (Shaeffer) at Ex. R-25 at [23].

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It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the data paths can include a set of input buffers configurable to receive the respective section of the first or second N-bit wide data from the respective set of module data lines and a set of output buffers configurable to regenerate and drive the respective section of the first or second N-bit wide data to the first side, at least the set of output buffers are tristate buffers configurable to be enabled by the logic during the first time period in response to the first module control signals and during the second time period in response to the second module control signals," and "at least the set of output buffers are disabled by the logic after the first time period and before the second time period. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7- 28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;

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- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3,

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13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3- 26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee*

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Item Number 2171.07 at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;

- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [26];
- RB-27 (Shaeffer) at Ex. R-25 at [26].

It was well-known to one of skill in the art before the time of the ’339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the logic can be configurable to keep the first set of tristate buffers and the second set of tristate buffers disabled when the memory module is not targeted by the memory controller for any memory operations. *See, e.g.*,

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- ’339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63- 9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64- 6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23,

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3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;

- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;

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- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3- 26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2*

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- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [28];
- RB-27 (Shaeffer) at Ex. R-25 at [28].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the DDR DRAM devices can "include a plurality of ranks of DDR DRAM devices, the each respective n-bit-wide buffer can be coupled to at least one respective DDR DRAM device in each of the plurality of ranks via the respective module data lines, the first registered address and control signals can cause one rank of DDR DRAM devices to perform the memory write operation by receiving the write data, and the second registered address and control signals can cause one rank of DDR DRAM devices to perform the memory read operation by outputting the read data. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65- 6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057],

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Figs. 1-7, 8A, 8B, 9, 11, 13;

- RB-3 (Halbert) at Abstract, 1:40- 60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35,

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7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 26, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee*

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Item Number 2192.05 at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing*

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Item #1341 at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [29];
- RB-27 (Shaeffer) at Ex. R-25 at [29].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the at least one respective DDR DRAM device in each of the plurality of ranks can include a respective pair of DDR DRAM devices, a first n/2-bit section of the respective n-bit section of the write_data can be driven by a first subset of the first set of tristate buffers to a first one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory write operation, a second n/2-bit section of the respective n-bit section of the write_data can be driven by a second subset of the first set of tristate buffers to a second one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory write operation, a first n/2-bit section of the respective n-bit section of the read_data can be received by a first subset of the second set of input buffers from a first one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory read operation, and a second n/2-bit section of the respective n-bit section of the read_data can be"received by a second subset of the second set of input buffers from the second one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory read operation. *See, e.g.*,

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- ’339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65- 6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40- 60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23,

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3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;

- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 26, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;

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- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2*

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- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [30];
- RB-27 (Shaeffer) at Ex. R-25 at [30].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the module controller can be further configurable to receive from the memory controller via the address and control signal lines third address and control signals for a subsequent memory read operation, and to output third registered address and control signals and third module control signals for the subsequent memory read operation in response to receiving the third address and control signals, the DDR DRAM devices can be configurable to perform the subsequent memory read operation by outputting additional read data in response to the third registered address and control signals, the subsequent memory read operation can be performed by another rank of DDR DRAM devices that is different from the one rank of DDR DRAM devices performing the memory read operation, the logic in response to the third module control signals can enable the second set of tristate buffers for a third time period corresponding to the subsequent memory read operation to drive a respective n-bit section of the additional read data, and the logic

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can be further configurable to disable the second set of tristate buffers after the second time period and before the third time period. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63- 9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64- 6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57,

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claims 1, 2, 11-13, Figs. 1-4;

- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15,

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16, 26, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;

- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37,

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56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [33];
- RB-27 (Shaeffer) at Ex. R-25 at [33].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first set of tristate buffers can be enabled for the first time period in accordance with a latency parameter. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63- 9:3, 9:4-65, Figs. 1, 3-10;

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- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64- 6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006- 0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53- 5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47,

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9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;

- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45- 63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61- 6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23- 29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3- 26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item*

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Number 2192.32 at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification*

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at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;

- RB-26 (Karamcheti) at Ex. R-24 at [34];
- RB-27 (Shaeffer) at Ex. R-25 at [34].

It was well-known to one of skill in the art before the time of the '339 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the second set of tristate buffers can be enabled for the second time period in accordance with a latency parameter. *See, e.g.*,

- '339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at Abstract, [0003], [0010-0012], [0018], [0026], [0027-0033], [0035-0036], [0037], [0039-0040], [0042], [0044-0052], [0054], [0056-0057], Figs. 1-7, 8A, 8B, 9, 11, 13;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 3:42-57, 3:67-4:2, 4:23-5:50, 5:56-65, 6:15-28, 6:40-7:20, 7:31-67, 8:19-32, 8:63-9:3, 9:4-65, Figs. 1, 3-10;
- RB-4 (Solomon) at Abstract, 1:34-42, 2:24-30, 4:56-5:2, 5:32-47, 5:64-6:26, 6:48-7:43, 15:7-25, 16:1-9, 7:59-8:34, 8:48-9:5, 21:28-54, 13:35-56, claim 1, Fig. 1, 9A;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20-47, 4:48-65, 5:7- 28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002- 0004], [0006-0008], [0015], [0017-0022],

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[0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;

- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64-4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59- 61, 3:66-4:38, 4:39-6:67, 7:9-35, 7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;
- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29- 52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15- 44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79-3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4-5, 4.20.4-6, 4.20.4-8, 4.20.4- 9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4- 35, 4.20.4-66, 4.20.4-73, *JESD79* at

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cover, 8, 9, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 27, 33, 48, 49;

- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 33, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13-22, 9:46-53, 10:3- 26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150, *Committee Item Number 2192.05* at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;
- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;

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- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM Informational Showing Item #1341* at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;
- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Ex. R-24 at [35];
- RB-27 (Shaeffer) at Ex. R-25 at [35].

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time that the disclosures relating to memory devices and circuitry could be integrated into memory modules.

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See,*

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e.g.,

- ’339 patent at 1:24-36, 1:37-51, 4:48-5:3, 5:4-22, 5:44-64, 5:65-6:16, Figs. 1A, 1B, 6:65-7:14, 7:15-43, 9:3-9, Figs. 2C, 2D;
- RB-2 (Ellsberry) at [0049], [0051-0052], Fig. 2, 6, 11;
- RB-3 (Halbert) at Abstract, 1:40-60, 2:6-60, 4:49-5:14, 7:31-61, 8:63-9:3, 9:36-54, Figs. 4, 7;
- RB-4 (Solomon) at 31:45-56, 13:35-49;
- RB-5 (Raynham) at Abstract, 1:17-24, 2:4-23, 4:20-30, 4:20- 47, 4:48-65, 5:7-28, 5:36-6:59, Fig. 4A, 6:6-59, 7:33-8:27, Fig. 4B, 8:12-27, 8:28-9:18, 8:37-60, 9:6-33, 9:48-10:9, 10:28-56, Fig. 4C, 10:63-11:7, 10:38-11:25, 11:26-12:9, 11:53-12-8, 12:42-60, 12:10-26, 13:1-17, Fig. 4D, 12:27-41, Claim 1, Claim 2, Claim 6;
- RB-6 (Yen) at Abstract, 1:8-63, 2:61-67, 3:8-12, 3:22-55, 4:37-64, 5:21-28, 5:59-6:30, 6:55-7:4, 7:6-36, Figs. 5, 7;
- RB-7 (Rajan) at Abstract, [0002-0004], [0006-0008], [0015], [0017-0022], [0024-0032], [0034], [0037], [0040], [0042-0053], [0055-0069], [0070-0108], [0112-0113], claim 16, Figs. 1-5, 10;
- RB-8 (Ruckerbauer) at Abstract, 1:12-2:19, 2:23-67, 3:16-30, 3:50-67, 4:1-57, claims 1, 2, 11-13, Figs. 1-4;
- RB-9 (Gower 375) at Abstract, 1:7-32, 1:42-2:11, 2:21-31, 2:40-3:13, 3:19-23, 3:32-59, 3:64- 4:67, 5:1-6:42, 6:43-61, 6:62-8:49, 8:50-9:28, 9:51-11:31, Claims 1, 6, 9-10, Figs. 2-5, 7-16;
- RB-10 (Gower 762) at Abstract, 1:7-32, 1:33-41, 1:42-2:11, 2:21-31, 2:32-55, 2:59-3:26, 3:35-36, 3:47-48, 3:51-55, 3:59-61, 3:66-4:38, 4:39-6:67, 7:9-35,

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7:36-8:47, 8:62-9:5, 9:53-64, 10:9-29, Figs. 2-5, 7-12;

- RB-11 (Cowell) at Abstract, 1:7-41, 1:42-55, 1:56-2:12, 2:22-62, 3:3-38, 3:47-48, 3:59-67, 4:19-21, 4:29-52, 4:53-5:60, 5:61-6:14, 6:15-7:3, 7:4-40, 7:41-8:47, 9:20-31, 9:48-64, 10:32-11:13, Fig. 2-5, 7, 9-13;
- RB-12 (Doblar) at Abstract, 1:19-37, 1:38-2:29, 2:30-63, 2:66-3:17, 3:58-4:14, 4:1-14, 4:15-44, 4:45-63, 4:64-5:12, 5:13-35, 5:36-56, 5:57-6:12, 6:13-18, 6:19-34, 6:35-54, Figs. 1, 2, Claims 1, 12;
- RB-13 (Bhakta) at 1:18-21, 1:23-32, 2:16-22, 2:34-42, 2:46-58, 3:17-30, 5:11-26, 5:27-50, 5:61-6:9, 6:10-17, 6:18-26, 6:38-46, 6:47-7:5, 7:45-62, 24:57-25:10, 25:11-26:19, Figs. 1A, 1B, 6B, 6C, 6D;
- RB-14 (JEDEC SDRAM/DIMM Standards) at *JESD79- 3C* at cover, Fig. 4, 1, 3, 13, 22, 23, 24, 25, 26, 27-31, 42, 56, 57, 91, *JEDEC 21-C* at cover, 4.20.4- 5, 4.20.4-6, 4.20.4-8, 4.20.4-9, 4.20.4-10, 4.20.4-11, 4.20.4-12, 4.20.4-13, 4.20.4-14, 4.20.4-15, 4.20.4-16, 4.20.4-29, 4.20.4-35, 4.20.4-66, 4.20.4-73, *JESD79* at cover, 13, 17, 26, *JESD79-2B* at cover, 6, 11, 12, 21, 22, 23-29, 30, 46, *JESD79-2A* at cover, 6, 14, 24, 25, 26-32, 33, 48, 49;
- RB-15 (JEDEC FBDIMM Standards) at *JESD205* at 1, 9, 10, 11, 12, 13, 14, 15, 16, 29, 30, 31, 32, 34, 37, 38, 39, 40, 46, 63, 64-65, 70, 71-73, 80, 81-83, 84, 110, *JESD82-20* at 1, 3, 4, 5, 6, 11, 19, 20, 21, 29, 43, 77;
- RB-16 (Lee) at 4:66-5:20, 5:30-37, 5:59-64, 6:48-64, 7:11-20, 7:43-55, 8:1-9, 9:13- 22, 9:46-53, 10:3-26, Figs. 1, 2, 3, Claims 1, 20;
- RB-17 (JEDEC SDRAM/DIMM Proposals) at *Committee Item Number 1680.07* at 1, 3, 13, 15, 17, 18, 22, 23, 24-25, 26, 27, 27-31, 42, 53, 56, 57, 150,

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Committee Item Number 2192.05 at 5, 10, 11, 13, 16, 17, 19, *Committee Item Number 2192.14* at 2, 3, 4, 5, 8, *Committee Item Number 2192.21* at 6, 8, *Committee Item Number 2192.22* at 3, 8, *Committee Item Number 2192.29* at 6, *Committee Item Number 2192.32* at 3, 6, 7, *Committee Item Number 2204.03* at 3, *JC-45 Meeting No. 22 Minutes* at 12-13;

- RB-18 (JEDEC FBDIMM Proposals) at *FB-DIMM Design Specification Revision 3.0* at 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 29, 30, 33, 34, 35, 36, 51, 57, 58-59, 64, 78, *AMB Specification* at 13, 14, 15, 16, 17, 18, 19, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 46, 47, 48, 63, 66, 68, 71, 81, 93, 128, 143, 145, 147, 164, *Committee Item Number 2118.08* at 3, 4, *Committee Item Number 2135.01* at 20, *Committee Item Number 2171.02* at 4, 5, 6, *Committee Item Number 2171.07* at 3, 5, 6, 7, 8, 9, 10, *JC-45 Meeting No. 11 Minutes* at 44;
- RB-19 (Micron DDR2 SDRAM FBDIMM) at *FBDIMM Specification* at 7, Figs. 2, 3, 4, Table 3;
- RB-20 (IBM X990 eServer) at 367, 369, 370, 371, 372, 373, 378, 379, Figs. 2, 3, 4, 5, 6, 11, Table 11;
- RB-21 (QBM) at *QBM Specification Rev. 0.93* at 5, 6, 8, 9, 10, 11, 32, 34, 36, 37, 56, *QBM2 Interface Overview* at 3, *QBM Informational Showing Item #1133* at 4, 5, 6, 8, *QBM2 Technical Features Overview* at 3, 4, 5, 6, 8, 10, 11, 14, 15, *QBM2 Technical Highlights* at 19, *QBM Doubling DDR Memory Bandwidth* at 8, 10, 11, 12, 13, *QBM2 Technology Overview* at 5, 8, 11, 12, 13, 14, 15, 16, 17, 19, 20, 23, 24, *QBM Interim JEDEC Meeting* at 6, 11, 22, *QBM*

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Informational Showing Item #1341 at 3, 9, 15, *QBM Platform Conference* at 17, 18, 19, 22;

- RB-22 (Samsung DDR3 SDRAM) at *Samsung DDR3 SDRAM Specification* at 8, 12, 13, 49, 51;
- RB-23 (Samsung DDR2 FBDIMM) at *Samsung DDR2 FBDIMM Specification* at 7, 8, 12, 13, Figs. 4, 11, 12, 17, 19, 21;
- RB-26 (Karamcheti) at Abstract, [0002]-[0004], [0021]-[0022], [0150]-[0152], FIGS. 1-5 (and related disclosures);
- RB-27 (Shaeffer) at Ex. Abstract, [0003], FIGS. 5-8, 9A-C, 18, 19, 36 (and related disclosures).

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the ’339 Patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the Asserted Claims are well known in the art. Indeed,

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the listed inventors of the Asserted Patents admitted as much in the specification of the '339 Patent. See '339 patent at 4:16-7:43; 8:54-9:9; 10:50-53.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '339 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix B for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

b) *Obviousness Combinations*

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix B with any other reference or references listed in Appendix B along with the knowledge of one of

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ordinary skill in the art to arrive at the inventions claims in the ’339 patent. For example, and without limitation, the Asserted Claims of the ’339 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
Asserted Patent’s Admitted Prior Art (APA) (RB-1)	• U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24) • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27) and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2)	• Asserted Patent’s Admitted Prior Art (APA) (RB-1); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,024,518 (Halbert) (RB-3)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,532,537 (Solomon) (RB-4)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No.

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 6,530,033 (Raynham) (RB-5)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 6,947,304 (Yen) (RB-	• Asserted Patent's Admitted Prior Art (APA)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
6)	(RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 6,972,981 (Ruckerbauer) (RB-8)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,389,375 (Gower 375) (RB-9)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,512,762 (Gower 762) (RB-10)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 7,395,476 (Cowell) (RB-11)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No.

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	2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 6,714,433 (Doblar) (RB-12)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-

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	26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill. • Micron DDR2 SDRAM FBDIMM (RB-19);
U.S. Patent No. 7,289,386 (Bhakta) (RB-13)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
JEDEC SDRAM/DIMM Standards (RB-14)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC FBDIMM Standards (RA-15);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
JEDEC FBDIMM Standards (RB-15)	Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,001,434 (Lee) (RB-16)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
JEDEC SDRAM/DIMM Proposals (RB-17)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• The knowledge of a person of ordinary skill.
JEDEC FBDIMM Proposals (RB-18)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
Micron DDR2 SDRAM FBDIMM (RB-19)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • IBM Z990 eServer (R-20);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27); and/or • The knowledge of a person of ordinary skill.
IBM Z990 eServer (RB-20)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27) and/or • The knowledge of a person of ordinary skill.
QBM (RB-21)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27) and/or • The knowledge of a person of ordinary skill.
Samsung DDR3 SDRAM (RB-22)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27) and/or • The knowledge of a person of ordinary skill.
Samsung DDR2 FBDIMM (RB-23)	• Asserted Patent's Admitted Prior Art (APA) (RB-1);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); • U.S. Patent App. Pub. No. 2008/008021 (RB-27) and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2009/0210616 (RB-26)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2008/008021 (RB-27) and/or • The knowledge of a person of ordinary skill.
U.S. Patent App. Pub. No. 2008/0080261 (RB-27)	• Asserted Patent's Admitted Prior Art (APA) (RB-1); • U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry) (RB-2); • U.S. Patent No. 7,024,518 (Halbert) (RB-3); • U.S. Patent No. 6,530,033 (Raynham) (RB-5); • U.S. Patent App. Pub. No. 2008/0028135 (Rajan) (RB-7); • U.S. Patent No. 7,389,375 (Gower 375) (RB-9); • U.S. Patent No. 7,532,537 (Solomon) (RB-4); • U.S. Patent No, 7,289,386 (Bhakta) (RB-13); • JEDEC SDRAM/DIMM Standards (RA-14); • JEDEC FBDIMM Standards (RA-15); • JEDEC SDRAM/DIMM Proposals (RB-17); • JEDEC FBDIMM Proposals (RB-18); • Micron DDR2 SDRAM FBDIMM (RB-19); • IBM Z990 eServer (R-20); • QBM (RB-21); • Kingston FBDIMM (RB-24); • U.S. Patent App. Pub. No. 2009/0210616 (RB-26); and/or • The knowledge of a person of ordinary skill.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well

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as to detail and explain such combinations.

3. U.S. Patent No. 11,016,918

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix C the prior art references that render obvious the Asserted Claims of the ’918 patent and include below exemplary combinations showing the obviousness of the ’918 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix C, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of skill in the art at the time of the ’918 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix C, such reference may be combined with any other references listed in Appendix C for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the ’918 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the ’918 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

a) *Obviousness Rationale*

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix C along with the knowledge of one of ordinary skill in the art to meet the limitations of the ’918 patent Asserted Claims.

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Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '918 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. See KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21.

Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix C would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would

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have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix C would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the '918 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix C is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various

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technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of skill in the art to consult and/or combine any of the prior art listed in Appendix C because all of these references relate to the same area of technology and/or are from analogous art. The ’918 patent Asserted Claims are directed to computer memory modules that use multiple memory devices. ’918 patent at 1:66-2:2. The ’918 patent Asserted Claims merely united old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the ’918 patent Asserted Claims.

All of the ’918 patent Asserted Claims are directed to computer memory devices that use multiple memory devices. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, was widely known before the alleged priority date of the ’918 Patent, as evidenced by the references in Appendix C. *See, e.g.*,

- ’918 patent at 2:40-50; 2:56-3:4; 3:12-21; 3:47-53; 13:6-15; 8:60-63; Figs. 1, 2;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26- 32, 2:28-54, 2:55-3:3, 3:24-

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38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19- 58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1- 6, 19:13-33, Claims 1, 10, 11, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix C because at the time of the alleged invention incorporating memory devices and

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circuitry to a printed circuit board was a common problem with a well-known solution. *See, e.g.*,

- '918 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; Figs. 1, 2;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2, 3;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59- 8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32- 14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072],

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Figs. 1, 2;

- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix C at the time of the alleged invention. Common problems with conventional techniques for combining memory devices were known to persons of ordinary skill in the art and incorporating memory devices and circuitry to a printed circuit board was a well-known solution to achieve memory modules with improved data transfer and/or power management. *See, e.g.*,

- '918 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; 27:59-29:64; Figs. 1, 2, 16;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2, 3;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19- 31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-

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49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a printed circuit board (“PCB”) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a

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plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system. *See, e.g.*,

- '918 patent at 2:40-50; 2:56-3:4; 3:12- 21; 3:47-53; 13:6-15; 8:60-63, Figs. 1, 2;
- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0012], [0013], [0017], [0018], [0019], Claims 20, 24, 28, Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0034], [0037], [0039], [0054], Figs. 3, 5, 9, 10, 11;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55- 3:3, 3:3-23, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at Abstract, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19- 35, Figs. 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0072], Fig. 1;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;

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- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a first buck converter configured to provide a first regulated voltage having a first voltage amplitude, a second buck converter configured to provide a second regulated voltage having a second voltage amplitude, a third buck converter configured to provide a third regulated voltage having a third voltage amplitude, and a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude. *See, e.g.*,

- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0012], [0017], Figs. 1A, 3;
- RC-3 (Spiers) at [0037], [0039], [0054], Figs. 4, 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55-3:3, 3:37-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;
- RC-5 (Kim) at 2:18-32, 3:52-65, 5:56-65, 6:16-18, 6:19-50, 6:51-7:16, Figs. 4, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 17, 18-20, 11, 13, 14-16, 30, 33, 68,

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JESD82-20 at 83, 31, 32, 44, *JESD79-2B* at 6-7, 2, 3, *JESD79* at 1, 7, 54, 60, *JC-42.3 Meeting No. 120 Minutes* at 27;

- RC-8 (Ootani) at [0027], [0034], [0036], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 5, 12;
- RC-18 (TPS65023) at Datasheet at 1, 22, User Guide at 1, 10;
- RC-10 (Shi) at pg. 85 col. 2, pg. 86 cols. 1 and 2, Figs. 1 and 7;
- RC-11 (MAX1917) at pgs. 1, 9 11, and 15;
- RC-12 (Byoun) at pg. 70 col.1, pg. 72 col. 1, Fig. 1 (pg. 70), Fig. 2 (pg. 70), Fig. 1 (pg. 71), and Fig. 3 (pg. 73);
- RC-19 (IRU3048) at 1, 3, 4, 5, 6, 7, 10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages. *See, e.g.*,

- '918 patent at 13:6-15;
- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0011], [0012], [0013], [0017], [0018], [0019], Claims 20, 24, 28, Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0037], [0046], [0054], Figs. 4, 5, 9, 10, 11;
- RC-4 (Kanapathippillai) at Abstract, 2:28-54, 2:55-3:3, 3:4-23, 3:39-4:23, 4:51-

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65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56- 13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 17:15-35, 17:48-49, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 3, 5, 6, 8, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at Figs. 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0091], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 15, 17, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 11, 30, 33, 13, 14-16, 68, *JESD82-20* at 31, 32, 44, 83;
- RC-8 (Ootani) at Fig. 1;
- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5;
- RC-18 (TPS65023) at Datasheet at 1;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 14, 15, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage. *See, e.g.*,

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- ’918 patent at 2:40-50; 3:47-53; 8:60-61, Fig. 1;
- RC-2 (Harris) at [0009], [0011], Claims 20, 28, Figs. 1A, 3;
- RC-3 (Spiers) at [0036], [0037], [0038], Fig. 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57- 16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 3, 5, 6, 8, 10, 11, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 6:19-50, Fig. 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 17, 18-20, 47, *JESD79-2B* at cover, 2, 3, 6-7, 9, *JESD79* at cover, 1, 7, 54, 60;
- RC-8 (Ootani) at [0025], [0026], Fig. 1;
- RC-9 (Samsung FBDIMM) at 5;
- RC-18 (TPS65023) at Datasheet at 1;
- RC-19 (IRU3048) at 1, 11;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

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It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a plurality of components can include at least one circuit coupled between a first ortion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes. *See, e.g.*,

- '918 patent at Fig. 2;
- RC-2 (Harris) at [0002], [0003], [0009], [0012], [0013], [0017], [0018], [0019], Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0037], [0039], [0044], [0045], [0046], Figs. 5, 9;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55-3:3, 3:4-23, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, Claims 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 1:21-31, 2:18-32, 5:66-6:7, 6:53-7:16, Figs. 1, 4, 9;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0027], [0028]-[0071], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0078], [0084], [0091], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;

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- RC-7 (JEDEC Standards) at *JESD205* at 9, 11, 30, 33, 13, 14-16, 84, 100, *JESD82-20* at 1, 3, 4, 8, 31, 32, 43, 81-82, 83;
- RC-8 (Ootani) at [0034], [0036], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5, 12, 16, 17, 18, 1, 15;
- RC-13 (Ito) at [0002], [0067], [0074], Figs. 24 and 28;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 22, 28, User Guide at 1, 3-4, 10;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first and third buck converters, the second and third buck converters, or the second and third buck converters can be configured to operate as a dual buck converter. *See, e.g.*,

- RC-2 (Harris) at [0010], Fig. 1A;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 15, 17, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, *JESD79-2B* at 6-7, *JC42.2* at 5;
- RC-19 (IRU3048) at 1, 4, 5, 6, 7, 11, 12.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement

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contentions, that at least one of the first, second, third and fourth regulated voltages have a voltage amplitude of 1.8 volts. *See, e.g.*,

- RC-2 (Harris) at [0002], [0009], [0011];
- RC-3 (Spiers) at Figs. 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 3:39-4:23, 3:39-4:23, Claims 19, 21, 27;
- RC-5 (Kim) at 2:18-32, Fig. 4;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]- [0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 30, 33, *JESD82-20* at 83, JESD79-*2B* at 6-7;
- RC-8 (Ootani) at [0034], [0036];
- RC-9 (Samsung FBDIMM) at 1, 15;
- RC-18 (TPS65023) at Datasheet at 5, 28, User Guide at 3-4;
- RC-19 (IRU3048) at 1, 4, 5, 6, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage

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monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage or less than a second threshold voltage. *See, e.g.*,

- RC-2 (Harris) at [0010], [0012], [0013], [0019], Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0036], [0037], [0041], [0054], Figs. 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55-3:3, 3:39-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;
- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0007]-[0016], [0022], [0028], [0042], Claims 1-10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 44;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-14 (Amidi) at 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6, 14, and 15;
- RC-15 (Hajeck) at Abstract, 3:30-39, 4:62-65, Fig. 1;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 31;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the second threshold voltage can correspond to a voltage level that is ten percent

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less than a specified operating voltage. *See, e.g.*,

- RC-2 (Harris) at [0013];
- RC-3 (Spiers) at [0037];
- RC-5 (Kim) at 2:18-32;
- RC-7 (JEDEC Standards) at *JESD82-20* at 32, JESD79-*2B* at 6-7;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-14 (Amidi) at 4:44-55, 8:23-36, Figs. 6, 14;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12. It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first threshold voltage can correspond to a voltage level that is ten percent greater than a specified operating voltage. *See, e.g.*,
- RC-2 (Harris) at [0013];
- RC-3 (Spiers) at [0037];
- RC-5 (Kim) at 2:18-32;
- RC-7 (JEDEC Standards) at *JESD82-20* at 32, JESD79-*2B* at 6-7;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-15 (Hajeck) at Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, Fig. 1;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;

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- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that plurality of components can include a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information. *See, e.g.*,

- '918 patent at 2:61-3:4;
- RC-2 (Harris) at [0009], [0012], [0013], [0015], [0019], Figs. 1A, 1B, 3;
- RC-3 (Spiers) at [0038], [0054], [0055], [0056], Fig. 14;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-32, 9:33-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57-16:16, 16:48-59, 17:15-35, 17:48-49, 17:50- 56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 3, 5, 6, 8, 10, 11, 15, 16, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]-[0026], [0027]-[0071], [0078], [0084], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 13, 14-16, 30, 32, *JESD82-20* at 25, 95, 96, 141;
- RC-8 (Ootani) at [0026], Fig.1;
- RC-9 (Samsung FBDIMM) at 11, 27;
- RC-16 (Hsu) at Abstract, 2:20- 28, 2:46-49, 5:1-6:9, 6:10-57, 6:58-7:10, Figs. 1,

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2A, and 2B;

- RC-17 (McManis) at 4:40-52, 5:8- 43, 5:51-6:8, and Fig. 1;
- RC-18 (TPS65023) at User Guide at 4;
- RC-19 (IRU3048) at 1, 4, 5, 6;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that in response to the trigger signal, the logic element can write information into the non-volatile memory. *See, e.g.*,

- '918 patent at 2:61-3:4, 3:27-33;
- RC-3 (Spiers) at [0037], [0054], [0055], [0056], Fig. 14;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-32, 9:33-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57-16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 3, 5, 6, 8, 10, 11, 15, 16, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]-[0026], [0027]-[0071], [0078], [0084], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120],

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[0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;

- RC-7 (JEDEC Standards) at *JESD205* at 44, *JESD82-20* at 25;
- RC-9 (Samsung FBDIMM) at 11;
- RC-18 (TPS65023) at Datasheet at 29;
- RC-19 (IRU3048) at 1, 2, 4, 5, 6, 8-10;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that plurality of components can include a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory. *See, e.g.*,

- '918 patent at 2:61-3:4;
- RC-2 (Harris) at [0009], [0010], [0017], Claim 1;
- RC-3 (Spiers) at [0034], [0037], [0038], [0039], [0054], [0055], [0056], Figs. 5, 14;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-32, 9:33-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57- 16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 3, 5, 6, 8, 10, 11, 15, 16, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C,

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5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]-[0026], [0027]-[0071], [0078], [0084], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD82-20* at 25, 95, 96, 141;
- RC-8 (Ootani) at [0026], Fig.1;
- RC-9 (Samsung FBDIMM) at 11;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 31;
- RC-19 (IRU3048) at 1, 2, 4, 5, 6, 8-10;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module could include first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, and a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively. *See, e.g.*,

- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0011], [0012], [0013], [0017], Figs. 1A, 3;
- RC-3 (Spiers) at [0037], [0039], [0054], [0055], [0056], Figs. 4, 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55-3:3, 3:39- 4:23, Claims 1, 2, 10, 11, 12,

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14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;

- RC-5 (Kim) at 2:18- 32, 3:52-65, 5:56-65, 6:16-18, 6:19-50, 6:51-7:16, Figs. 4, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0078], [0084], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD82-20* at 32, *JESD79-2B* at 6-7;
- RC-9 (Samsung FBDIMM) at 5, 12;
- RC-18 (TPS65023) at Datasheet at 1, 22, User Guide at 1, 10;
- RC-19 (IRU3048) at 1, 3, 4, 5, 6, 7, 10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage. *See, e.g.*,

- RC-2 (Harris) at [0010], [0012], [0013], [0019], Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0036], [0037], [0041], [0054], Figs. 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55-3:3, 3:39-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;

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- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0007]-[0016], [0022], [0028], [0042], Claims 1-10, Figs. 1, 2-14, 16, 18; ;
- RC-7 (JEDEC Standards) at *JESD205* at 44;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 31;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that plurality of components can include a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element. *See, e.g.*,

- RC-2 (Harris) at [0009], [0012], [0013], [0015], [0016], [0019], Figs. 1A, 1B, 2, 3;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 2:28-54, 2:28-54, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-32, 9:33-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57- 16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 3, 5, 6, 8, 10, 11,

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15, 16, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]-[0026], [0027]-[0071], [0078], [0084], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-9 (Samsung FBDIMM) at 11, 27;
- RC-19 (IRU3048) at 1, 2, 4, 5, 6, 8-10;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that plurality of components can include a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections. *See, e.g.*,

- '918 patent at 13:6-15, 2:40-50, 3:47-53, 8:60-61, Figs. 1, 2;
- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0011], [0012], [0013], [0017], [0018], [0019], Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0036], [0037], [0038], [0039], [0044], [0045], [0046], [0054], Figs. 4, 5, 9, 10, 11;

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- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55-3:3, 3:4-23, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19- 31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 17:50-56, 19:1-6, 19:13-33, Claims 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 1:21-31, 2:18-32, 5:66-6:7, 6:19-50, 6:53-7:16, Figs. 1, 4, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0078], [0084], [0072]- [0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 11, 13, 17, 18-20, 30, 33, 13, 14-16, 68, 84, 100, *JESD82-20* at 1, 3, 4, 8, 31, 32, 43, 44, 81-82, 83, *JESD79-2B* at cover, 2, 3, 6-7, 9, *JESD79* at cover, 1, 7, 54, 60;
- RC-8 (Ootani) at [0025], [0026], [0034], [0036], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5, 12, 16, 17, 18, 1, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 22, 28, User Guide at 1, 3-4, 10;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 14, 15, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

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It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the second regulated voltage can be configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on. *See, e.g.*,

- RC-2 (Harris) at [0009], [0019];
- RC-3 (Spiers) at [0034], [0036], [0037], [0054], [0055], [0056], Fig. 14;
- RC-4 (Kanapathippillai) at Abstract, 6:66-7:18, 7:41-58, 8:13-46, 9:20-42, 10:1-33, 10:57-11:15, 12:41-67, 13:19-63, 15:23-35, Claims 23, 24, Figs. 3A, 4A, 5A, 5B, 5C, 8A, 8B, 8C;
- RC-5 (Kim) at 6:19-50, Fig. 10;
- RC-6 (Okimoto) at [0005], [0024], [0030], [0036], [0037], [0045], [0051], [0058], [0092]-[0098], [0100]-[0101], [0026], [0032], Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD82-20* at 21, 39;
- RC-9 (Samsung FBDIMM) at 19;
- RC-18 (TPS65023) at Datasheet at 24;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that if the second regulated voltage is switched on while at least the plurality of

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SDRAM devices are powered on, the one or more registers can be configured to couple the first plurality of address and control signals to the plurality of SDRAM devices. *See, e.g.*,

- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0012], [0013], [0017], [0018], [0019], Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0041], [0043], Fig. 8;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55-3:3, 3:4-23, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:59-8:13, 8:13-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, Claims 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 1:21-31, 2:18-32, 5:66-6:7, 6:19-50, 6:53-7:16, Figs. 1, 4, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0027], [0028]-[0071], [0078], [0084], [0092]-[0098], [0100]-[0101], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 11, 13, 14-16, 30, 33, 84, 100, *JESD82-20* at 1, 3, 4, 8, 21, 31, 32, 39, 43, 81-82, 83;
- RC-8 (Ootani) at [0034], [0036], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5, 12, 16, 17, 18, 1, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 22, 24, 28, User Guide at 1, 3-4, 10;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 8-10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2,

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3.3, 3.4, 4.1, and 4.2;

- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers can be configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals. *See, e.g.*,

- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0012], [0013], [0017], [0018], [0019], Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0034], [0036], [0037], [0054], [0055], [0056], Fig. 14;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55-3:3, 3:4-23, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53- 65, 6:66-7:18, 7:59-8:13, 8:13-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19- 14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, Claims 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 1:21-31, 2:18-32, 5:66-6:7, 6:19-50, 6:53-7:16, Figs. 1, 4, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0027], [0028]- [0071], [0078], [0084], [0092]-[0098], [0100]-[0101], [0072]-[0077], [0079]-[0083], [0085]- [0090], [0120], [0122], [0124], [0091], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD82-20* at 21, 39;
- RC-8 (Ootani) at [0034], [0036], Figs. 1, 2;

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- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5, 12, 16, 17, 18, 1, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 22, 24, 28, User Guide at 1, 3-4, 10;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 8-10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time that the disclosures regarding memory devices and circuitry could be integrated into memory modules.

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*,

- '918 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; Figs. 1, 2;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2, 3;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26- 32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19- 58, 7:59-

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8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1- 6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

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In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the combination of memory devices and circuitry, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '918 patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the asserted claims are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the '918 patent. See '918 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; Figs. 1, 2.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '918 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve

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the right to rely on the disclosures of the references listed in Appendix C for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

b) *Obviousness Combinations*

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix C with any other reference or references listed in Appendix C along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '918 patent. For example, and without limitation, the Asserted Claims of the '918 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
Asserted Patents Admitted Prior Art (APA) (RC-1)	• JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent Publication No. 2006/0174140 (Harris) (RC-2)	• Asserted Patents Admitted Prior Art (APA) (RC-1);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent Publication No. 2006/0080515 (Spiers) (RC-3)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,189,328 (Kanapathippillai) (RC-4)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6*

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	Supercomputing Platform (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
JP11-073762 (Okimoto) (RC-6)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
JEDEC Standards (RC-7)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
JP2006-156814 (Ootani) (RC-8)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
Samsung DDR2 Fully Buffered DIMM (RC-9)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
TPS65023 (RC-18)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • IRU3048 (RC-19); • *The Physical Design of the ILLIAC 6*

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	Supercomputing Platform (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
IRU3048 (RC-19)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
The Physical Design of the ILLIAC 6 Supercomputing Platform (Keller) (RC-20)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • IRU3048 (RC-19); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management*	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
(SUMMIT) (RC-21)	• A Highly Integrated Power Management IC for Advanced Mobile Applications (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • IRU3048 (RC-19); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); and/or • The knowledge of a person of ordinary skill.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

4. U.S. Patent No. 11,232,054

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix D the prior art references that render obvious the Asserted Claims of the '054 patent and include below exemplary combinations showing the obviousness of the '054 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix D, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of skill in

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the art at the time of the ’054 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix D, such reference may be combined with any other references listed in Appendix D for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the ’054 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the ’054 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

a) *Obviousness Rationale*

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix D along with the knowledge of one of ordinary skill in the art to meet the limitations of the ’054 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants’ inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the ’054 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above

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and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. See KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." Id. at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix D would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix D would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the

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marketplace; the existence of a known problem for which there was an obvious solution encompassed by the ’054 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix D is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of skill in the art to consult and/or combine any of the prior art listed in Appendix D because all of these references relate to the same area of technology and/or are from analogous art. The ’054 patent Asserted Claims are directed to computer memory modules that use multiple memory devices. ’054 patent at 1:66-2:2. The ’054 patent Asserted Claims merely united old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for

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one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the ’054 patent Asserted Claims.

All of the ’054 patent Asserted Claims are directed to computer memory devices that use multiple memory devices. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, was widely known before the alleged priority date of the ’054 Patent, as evidenced by the references in Appendix D. *See, e.g.*,

- ’054 patent at 2:40-50; 2:56-3:4; 3:12-21; 3:47-53; 13:6-15; 8:60-63; Figs. 1, 2;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26- 32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19- 58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1- 6, 19:13-33, Claims 1, 10, 11, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-

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[0119], [0121], [0123], [0091], [0126], Figs. 1, 2-14, 16, 18;

- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix D because at the time of the alleged invention incorporating memory devices and circuitry to a printed circuit board was a common problem with a well-known solution. *See, e.g.*,

- '054 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; Figs. 1, 2;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2, 3;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28- 54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18,

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13:19-31, 13:32- 14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix D at the time of the alleged invention. Common problems with conventional techniques for combining memory devices were known to persons of ordinary skill in the art and

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incorporating memory devices and circuitry to a printed circuit board was a well-known solution to achieve memory modules with improved data transfer and/or power management. *See, e.g.*,

- '054 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; 27:59-29:64; Figs. 1, 2 ,16;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2, 3;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19- 31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-35, Figs. 1, 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20*

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at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;

- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a printed circuit board ("PCB") having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system. *See, e.g.*,

- '054 patent at 2:40-50; 2:56-3:4; 3:12- 21; 3:47-53; 13:6-15; 8:60-63, Figs. 1, 2;
- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0012], [0013], [0017], [0018], [0019], Claims 20, 24, 28, Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0034], [0037], [0039], [0054], Figs. 3, 5, 9, 10, 11;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55- 3:3, 3:3-23, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29- 15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56,

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18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at Abstract, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19- 35, Figs. 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0072], Fig. 1;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage

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of the at least three regulated voltages. *See, e.g.*,

- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0012], [0017], Figs. 1A, 3;
- RC-3 (Spiers) at [0037], [0039], [0054], Figs. 4, 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55-3:3, 3:37-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;
- RC-5 (Kim) at 2:18-32, 3:52-65, 5:56-65, 6:16-18, 6:19-50, 6:51-7:16, Figs. 4, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 17, 18-20, 11, 13, 14-16, 30, 33, 68, *JESD82-20* at 83, 31, 32, 44, *JESD79-2B* at 6-7, 2, 3, *JESD79* at 1, 7, 54, 60, *JC-42.3 Meeting No. 120 Minutes* at 27;
- RC-8 (Ootani) at [0027], [0034], [0036], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 5, 12;
- RC-10 (Shi) at pg. 85 col. 2, pg. 86 cols. 1 and 2, Figs. 1 and 7;
- RC-11 (MAX1917) at pgs. 1, 9 11, and 15;
- RC-12 (Byoun) at pg. 70 col.1, pg. 72 col. 1, Fig. 1 (pg. 70), Fig. 2 (pg. 70), Fig. 1 (pg. 71), and Fig. 3 (pg. 73);
- RC-18 (TPS65023) at Datasheet at 1, 22, User Guide at 1, 10;
- RC-19 (IRU3048) at 1, 3, 4, 5, 6, 7, 10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;

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- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages. *See, e.g.*,

- '054 patent at 13:6-15;
- RC-2 (Harris) at [0002], [0003], [0009], [0010], [0011], [0012], [0013], [0017], [0018], [0019], Claims 20, 24, 28, Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0037], [0046], [0054], Figs. 4, 5, 9, 10, 11;
- RC-4 (Kanapathippillai) at Abstract, 2:28-54, 2:55-3:3, 3:4-23, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 17:15-35, 17:48-49, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 3, 5, 6, 8, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at Figs. 8b, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0072]- [0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0091], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 15, 17, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 11, 30, 33, 13, 14-16, 68, *JESD82-20* at 31, 32, 44, 83;

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- RC-8 (Ootani) at Fig. 1;
- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5;
- RC-18 (TPS65023) at Datasheet at 1;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 14, 15, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a plurality of components can include a plurality of synchronous dynamic random access memory (SDRAM) devices and the plurality of SDRAM devices can be coupled to the first regulated voltage of the at least three regulated voltages. *See, e.g.*,

- '054 patent at 2:40-50; 3:47- 53; 8:60-61, Fig. 1;
- RC-2 (Harris) at [0009], [0011], Claims 20, 28, Figs. 1A, 3;
- RC-3 (Spiers) at [0036], [0037], [0038], Fig. 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57-16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1- 6, 19:13-33, Claims 1, 3, 5, 6, 8, 10, 11, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 6:19-50, Fig. 10;

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- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 17, 18-20, 47, *JESD79-2B* at cover, 2, 3, 6-7, 9, *JESD79* at cover, 1, 7, 54, 60;
- RC-8 (Ootani) at [0025], [0026], Fig. 1;
- RC-9 (Samsung FBDIMM) at 5;
- RC-18 (TPS65023) at Datasheet at 1;
- RC-19 (IRU3048) at 1, 11;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a plurality of components can include a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages. *See, e.g.*,

- '054 patent at 2:40-50; 3:47-53; 8:60-61, Fig. 1, Fig. 2;
- RC-2 (Harris) at [0002], [0003], [0009], [0011], [0012], [0013], [0017], [0018], [0019], Claims 20, 28, Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0036], [0037], [0038], [0039], [0044], [0045], [0046], Figs. 5, 9;

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- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26-32, 2:28-54, 2:55-3:3, 3:4-23, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 1:21-31, 2:18-32, 5:66-6:7, 6:19- 50, 6:53-7:16, Figs. 1, 4, 9, 10;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]- [0027], [0028]-[0071], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0078], [0084], [0091], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 11, 30, 33, 13, 14-16, 17, 18-20, 47, 84, 100, *JESD82-20* at 1, 3, 4, 8, 31, 32, 43, 81-82, 83, *JESD79-2B* at cover, 2, 3, 6-7, 9, *JESD79* at cover, 1, 7, 54, 60;
- RC-8 (Ootani) at [0025], [0026], [0034], [0036], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5, 12, 16, 17, 18, 1, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 22, 28, User Guide at 1, 3-4, 10;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’054 patent, at least

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partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first regulated voltage can have a first voltage amplitude, and the second regulated voltage can have a second voltage amplitude, and a first one of the first and second voltage amplitudes can be less than a second one of the first and second voltage amplitudes. *See, e.g.*,

- '054 patent at Fig. 2;
- RC-2 (Harris) at [0002], [0003], [0009], [0012], [0013], [0017], [0018], [0019], Figs. 1A, 3, 4;
- RC-3 (Spiers) at [0037], [0039], [0044], [0045], [0046], Figs. 5, 9;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 2:55-3:3, 3:4-23, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19-58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, Claims 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 1:21-31, 2:18-32, 5:66-6:7, 6:53-7:16, Figs. 1, 4, 9;
- RC-6 (Okimoto) at Abstract, [0001]-[0019], [0092]-[0104], [0021]-[0027], [0028]-[0071], [0072]-[0077], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0078], [0084], [0091], [0126], Claims 1-13, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 11, 30, 33, 13, 14-16, 84, 100, *JESD82-20* at 1, 3, 4, 8, 31, 32, 43, 81-82, 83;
- RC-8 (Ootani) at [0034], [0036], Figs. 1, 2;

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- RC-9 (Samsung FBDIMM) at 28, 30, 32, 5, 12, 16, 17, 18, 1, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 22, 28, User Guide at 1, 3-4, 10;
- RC-13 (Ito) at [0002], [0067], [0074], Figs. 24 and 28;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a third regulated voltage of the at least three regulated voltages can have a voltage amplitude of 1.8 volts. *See, e.g.*,

- RC-2 (Harris) at [0002], [0009], [0011];
- RC-3 (Spiers) at Figs. 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:26-32, 2:28-54, 3:39-4:23, 3:39-4:23, Claims 19, 21, 27;
- RC-5 (Kim) at 2:18-32, Fig. 4;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0021]- [0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, 30, 33, *JESD82-20* at 83, JESD79-*2B* at 6-7;
- RC-8 (Ootani) at [0034], [0036];
- RC-9 (Samsung FBDIMM) at 1, 15;

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- RC-18 (TPS65023) at Datasheet at 5, 28, User Guide at 3-4;
- RC-19 (IRU3048) at 1, 4, 5, 6, 11, 12, 14, 15;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below or above a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal. *See, e.g.*,

- RC-2 (Harris) at [0010], [0012], [0013], [0019], Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0036], [0037], [0041], [0054], Figs. 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55- 3:3, 3:39-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;
- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0007]-[0016], [0022], [0028], [0042], Claims 1-10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 44;
- RC-8 (Ootani) at [0043], [0044];

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- RC-9 (Samsung FBDIMM) at 11;
- RC-14 (Amidi) at 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6, 14, and 15;
- RC-15 (Hajeck) at Abstract, 3:30-39, 4:62-65, Fig. 1;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 31;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '918 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory. *See, e.g.*,

- '054 patent at 2:61-3:4, 3:27-33;
- RC-2 (Harris) at [0009], [0010], [0012], [0013], [0017], [0019], Claim 1, Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0034], [0036], [0037], [0038], [0041], [0054], [0055], [0056], Figs. 5, 14;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47- 9:19, 9:20-32, 9:33-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57-16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 3, 5, 6, 8, 10, 11,

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12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;

- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0007]-[0016], [0021]-[0026], [0027]-[0081], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Claims 1-10, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 44, *JESD82-20* at 25, 95, 96, 141;
- RC-8 (Ootani) at [0026], [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 29, 31;
- RC-16 (Hsu) at Abstract, 2:20-28, 2:46-49, 5:1-6:9, 6:10-57, 6:58- 7:10, Figs. 1, 2A, and 2B;
- RC-17 (McManis) at 4:40-52, 5:8-43, 5:51-6:8, and Fig. 1;
- RC-19 (IRU3048) at 1, 2, 4, 5, 6, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the ’054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal

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to one or more portions of the controller. *See, e.g.*,

- '054 patent at 2:61-3:4, 3:27-33;
- RC-2 (Harris) at [0009], [0010], [0012], [0013], [0017], [0019], Claim 1, Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0034], [0036], [0037], [0038], [0041], [0054], [0055], [0056], Figs. 5, 14;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-47, 6:24-52, 6:53-65, 6:66-7:18, 7:19-32, 7:59-8:13, 8:14-22, 8:23-38, 8:47-9:19, 9:20-32, 9:33-67, 10:25-57, 11:9-15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-56, 13:64-14:12, 14:29-15:56, 15:57- 16:16, 16:48-59, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 3, 5, 6, 8, 10, 11, 12, 14, 15, 16, 17, 19, 20, 21, 22, 25, 26, 27, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0001]-[0004], [0006], [0007]-[0016], [0021]-[0026], [0027]-[0081], [0079]-[0083], [0085]-[0090], [0120], [0122], [0124], [0091], [0126], Claims 1-10, Figs. 1, 2-14, 15, 16, 17, 18, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 44, *JESD82-20* at 25, 95, 96, 141;
- RC-8 (Ootani) at [0026], [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 29, 31;
- RC-14 (Amidi) at 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6, 14, and 15;
- RC-15 (Hajeck) at Abstract, 3:30-39, 4:62-65, Fig. 1;

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- RC-19 (IRU3048) at 1, 2, 4, 5, 6, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the voltage monitor circuit detecting a power threshold condition can include the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and wherein the first predetermined threshold voltage is above a specified operating voltage. *See, e.g.*,

- RC-2 (Harris) at [0010], [0012], [0013], [0019], Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0036], [0037], [0041], [0054], Figs. 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55-3:3, 3:39-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;
- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0007]-[0016], [0022], [0028], [0042], Claims 1-10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 44, *JESD82-20* at 32;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-14 (Amidi) at 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6, 14, and 15;
- RC-15 (Hajeck) at Abstract, 3:30-39, 4:62-65, Fig. 1;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 31;

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- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first predetermined threshold voltage can be ten percent above the specified operating voltage. *See, e.g.*,

- RC-2 (Harris) at [0013];
- RC-3 (Spiers) at [0037];
- RC-5 (Kim) at 2:18-32;
- RC-7 (JEDEC Standards) at *JESD82-20* at 32, JESD79-*2B* at 6-7;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-15 (Hajeck) at Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, Fig. 1;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the second predetermined threshold voltage can be ten percent below the specified operating voltage.. *See, e.g.*,

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- RC-2 (Harris) at [0013];
- RC-3 (Spiers) at [0037];
- RC-5 (Kim) at 2:18-32;
- RC-7 (JEDEC Standards) at *JESD82-20* at 32, JESD79-*2B* at 6-7;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-14 (Amidi) at 4:44-55, 8:23-36, Figs. 6, 14;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the voltage monitor circuit detecting a power threshold condition can include the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage. *See, e.g.*,

- RC-2 (Harris) at [0010], [0012], [0013], [0019], Figs. 1A, 3;
- RC-3 (Spiers) at [0002], [0036], [0037], [0041], [0054], Figs. 5, 14;
- RC-4 (Kanapathippillai) at 2:28-54, 2:55- 3:3, 3:39-4:23, Claims 1, 2, 10, 11, 12, 14, 17, 19, 20, 21, 22, 25, 26, 27, 28, Fig. 1A;
- RC-5 (Kim) at 6:53-7:16;
- RC-6 (Okimoto) at Abstract, [0007]-[0016], [0022], [0028], [0042], Claims 1-10, Figs. 1, 2-14, 16, 18;

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- RC-7 (JEDEC Standards) at *JESD205* at 44;
- RC-8 (Ootani) at [0043], [0044];
- RC-9 (Samsung FBDIMM) at 11;
- RC-14 (Amidi) at 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6, 14, and 15;
- RC-15 (Hajeck) at Abstract, 3:30-39, 4:62-65, Fig. 1;
- RC-18 (TPS65023) at Datasheet at 1, 9, 28, 31;
- RC-19 (IRU3048) at 1, 2, 4, 5, 8-10, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

It was well-known to one of skill in the art before the time of the '054 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that two of the at least three buck converters can be configured to operate as a dual-buck converter. *See, e.g.*,

- RC-2 (Harris) at [0010], Fig. 1A;
- RC-6 (Okimoto) at Abstract, [0001]- [0019], [0092]-[0104], [0021]-[0026], [0027]-[0071], [0072]-[0077], [0078], [0079]-[0083], [0084], [0085]-[0090], [0120], [0122], [0124], [0126], Claims 1-13, Figs. 15, 17, 19;
- RC-7 (JEDEC Standards) at *JESD205* at 9, *JESD79-2B* at 6-7, *JC42.2* at 5;
- RC-19 (IRU3048) at 1, 4, 5, 6, 7, 11, 12;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

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In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time that the disclosures regarding memory devices and circuitry could be integrated into memory modules.

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*,

- '054 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; Figs. 1, 2;
- RC-2 (Harris) at Abstract, [0002], [0004], [0005], [0006], [0007], [0009], [0010], [0011], [0014], [0016], [0017], [0018], [0020], Claims 20, 24, 28, Figs. 1A, 1B, 2, 3;
- RC-3 (Spiers) at Abstract, [0001], [0002], [0034], [0036], [0037], [0038], Figs. 3, 4, 5;
- RC-4 (Kanapathippillai) at Abstract, 1:21-22, 1:26- 32, 2:28-54, 2:55-3:3, 3:24-38, 3:39-4:23, 4:51-65, 5:10-6:7, 6:24-52, 6:53-65, 6:66-7:18, 7:19- 58, 7:59-8:13, 8:14-22, 8:23-46, 8:47-9:19, 9:20-32, 9:33-11:15, 11:56-13:7, 13:8-18, 13:19-31, 13:32-14:19, 14:29-15:56, 15:57-16:16, 16:48-67, 17:15-35, 17:48-49, 17:50-56, 18:17-25, 19:1-6, 19:13-33, Claims 1, 2, 10, 11, 12, 14, 17, 20, 22, 25, 26, 28, Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 6, 7A, 7B, 8A, 8B, 8C, 8D, 9;
- RC-5 (Kim) at Abstract, 1:21-31, 3:39-65, 4:66-5:3, 5:56-65, 5:66-6:15, 6:19-

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35, Figs. 1, 8b, 9, 10;

- RC-6 (Okimoto) at Abstract, [0001], [0002], [0003], [0004], [0006], [0007]-[0019], [0092-0104], [0021], [0022], [0023], [0024], [0025], [0026], [0027]-[0071], [0078], [0084], [0106]-[0119], [0121], [0123], [0091], [0126], Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, Figs. 1, 2-14, 16, 18;
- RC-7 (JEDEC Standards) at *JESD205* at 1, 9, 10, 13, 29, 38, 84, 100, *JESD82-20* at 3, 4, 43, 77, 38-39, *JESD79-2B* at cover, 6, 46-47, 52;
- RC-8 (Ootani) at [Problem], [Resolution Means], [0024], [0025], [0026], [0072], Figs. 1, 2;
- RC-9 (Samsung FBDIMM) at 4, 5, 28, 30, 32, 11, 12, 14, 15;
- RC-18 (TPS65023) at Datasheet at 1, 5, 6, 21, 45, 54, User Guide at 2, 5;
- RC-19 (IRU3048) at 1, 2, 3, 4, 5, 6, 10, 11, 12, 16, 17, 18;
- RC-20 (Keller) at pages 4, 6-7, 11-15, 18, and 23, and at figures 2.1, 2.2, 3.1, 3.2, 3.3, 3.4, 4.1, and 4.2;
- RC-21 (SUMMIT) at pages 1-3 and at figures 1-3.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the combination of memory devices and circuitry, and would have been able to select appropriate

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attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '054 patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the asserted claims are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the '054 patent. *See* '054 patent at 2:6-55; 2:56-3:23; 3:24-3:46; 3:47-62; 8:60-63; Figs. 1, 2. Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '054 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix D for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

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b) *Obviousness Combinations*

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix D with any other reference or references listed in Appendix D along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '054 patent. For example, and without limitation, the Asserted Claims of the '054 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
Asserted Patents Admitted Prior Art (APA) (RC-1)	• JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent Publication No. 2006/0174140 (Harris) (RC-2)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power*

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	Management (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent Publication No. 2006/0080515 (Spiers) (RC-3)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,189,328 (Kanapathippillai) (RC-4)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
U.S. Patent No. 6,707,724 (Kim) (RC-5)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
JP11-073762 (Okimoto) (RC-6)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
JEDEC Standards (RC-7)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
JP2006-156814 (Ootani) (RC-8)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
Samsung DDR2 Fully Buffered DIMM (RC-9)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
TPS65023 (RC-18)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15);

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 6,670,234 (Hsu) (RC-16); • IRU3048 (RC-19); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
IRU3048 (RC-19)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.
The Physical Design of the ILLIAC 6 Supercomputing Platform (Keller) (RC-20)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • IRU3048 (RC-19); • SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21); and/or • The knowledge of a person of ordinary skill.

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
SUMMIT Microelectronics Application Note 59, *Platform Solution for DDR SDRAM Power Management* (SUMMIT) (RC-21)	• Asserted Patents Admitted Prior Art (APA) (RC-1); • JEDEC Standards (RC-7); • *A Highly Integrated Power Management IC for Advanced Mobile Applications* (Shi) (RC-10); • JP2002083872A (Ito) (RC-13); • U.S. Patent No. 7,724,604 (Amidi) (RC-14); • U.S. Patent No. 6,856,556 (Hajeck) (RC-15); • U.S. Patent No. 6,670,234 (Hsu) (RC-16); • TPS65023 (RC-18); • IRU3048 (RC-19); • *The Physical Design of the ILLIAC 6 Supercomputing Platform* (Keller) (RC-20); and/or • The knowledge of a person of ordinary skill.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

5. U.S. Patent No. 8,787,060

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix E the prior art references that render obvious the Asserted Claims of the '060 patent and include below exemplary combinations showing the obviousness of the '060 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix E, the limitation would have been obvious in light of the

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disclosures within the reference and the knowledge of one of skill in the art at the time of the '060 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix E, such reference may be combined with any other references listed in Appendix E for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '060 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '060 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

a) *Obviousness Rationale*

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix E along with the knowledge of one of ordinary skill in the art to meet the limitations of the '060 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '060 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a

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specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. See KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." Id. at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix E would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix E would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references;

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common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the ’060 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix E is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of skill in the art to consult and/or combine any of the prior art listed in Appendix E because all of these references relate to the same area of technology and/or are from analogous art. The ’060 patent Asserted Claims are directed to memory packages with stacked array dies and related methods for reducing the load of drivers on the memory modules. ’060 patent at Abstract, 1:18-22. The ’060 patent Asserted Claims merely unite old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design

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community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the ’060 patent Asserted Claims.

All of the ’060 patent Asserted Claims are directed to memory packages with stacked array dies or related methods for reducing the load of drivers on the memory modules. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, was widely known before the alleged priority date of the ’060 patent, as evidenced by the references in Appendix E. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30- 56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;

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- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47, 5:30-31, 5:32-45, 5:46-47, 5:48- 6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

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- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36- 42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65- 67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at

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3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;

- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B.
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix E because at the time of the alleged invention reducing the load of drivers in a memory package on a memory module was a common problem with a well-known solution. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43,

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44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;

- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13- 26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24,

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26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46- 47, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9- 25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65- 2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;

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- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27- 51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48- 51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-

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67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B.

- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

Further, it was common knowledge to one of skill in the art at the time of the alleged invention that reducing the load of drivers in a memory package can improve performance of the memory module. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19- 34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;

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- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47, 5:30-31, 5:32-45, 5:46- 47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57,

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5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;

- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46- 53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18- 24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1,

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4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.

- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48- 51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58- 8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26- 33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B.
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix E at the time of the alleged invention. Common problems with conventional techniques for reducing the load of drivers in a memory package were known to persons of ordinary skill in the art and electrically communicating with groups of array dies was a well-known solution to achieve improved performance. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30- 56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43,

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- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24,

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- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47, 5:30-31, 5:32-45, 5:46-47, 5:48- 6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36- 42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;

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- RD-17 (Rajan 881) at Abstract, 1:65- 67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. Vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A,

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6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B.

- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

Memory packages were well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:63-2:7, 4:55-5:11, 18:57-19:7, 19:8-20, Figs. 1A and 1B; *see also*
- RD-2 (Rajan 137) at Abstract, ¶¶ 2, 6, 17, 24, 43, 44, Figs. 1, 2C;
- RD-3 (Kim) at Abstract, ¶¶ 23, 27, 46, 47, 48, 49, 50, Fig. 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:59-60, 5:10-15, 6:32-39, Claims 1, 3, 5, Figs 1 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 7, 11, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 37, 38, 62, 121, Claims 1, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 64, Figs. 1, 2 and 3A;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 27, 36, 37, 58, 79, Claims 1, 12, Figs. 5B, 10, 12, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 40, Figs. 1, 2, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 16, 20, 21, 24, 26, 28, 29, 30, 31, 32, 47, 69, 70, 71, 72, 73, 75, Figs. 1, 3, 5, 6;

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- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 5:30-31, 5:32-45, 5:46- 47, 5:48-6:3, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39- 43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62¸5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, Claim 1;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 8:58-9:3, 9:4-13, Claim 1, Fig. 5;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25- 31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00*

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September 2011 at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at *Ex. E*-19 at 1pre, 11pre, 20pre.
- RD-20 (Lee) at Abstract, 1:17- 21, 1:22-29, 1:30-36, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19- 21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B.
- RD-21 (Micron LRDIMM System) at Ex. *E-21* at 1pre, 11pre, 20pre.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices. *See, e.g.*,

- '060 patent at 1:30-56, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 9, 21, 22, 25, 33, 51, 76, 82, 84, 87, Claims 1, 19, 20, Figs. 2C, 3, 4, 5, 6;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 6, 12, 13, 14, 15, 16, 17, 28, 29, 30, 50, Claims 1, 5, 6, 10, 11, 14, 15, 18,R 19, 21, 25, Figs. 1, 2;
- RD-4 (Ware) at 2:59-3:3, 4:24-41, 4:58-5:9, 7:4-18, Claims 1 and 3, Figs. 1, 2, 6 and 8;

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- RD-5 (Riho 293) at Abstract, ¶¶ 4, 12, 15, 16, 26, 30, 31, 33, Claim 1, Figs. 1 and 2;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 69, 70, 71, 72, 73, Claims 1, 11, Figs. 1, 2 and 3B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 17, 27, 38, 41, 42, 43, 47, 58, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 2:12-15, 4:1-25, 5:58- 6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 5, 7, 15, 21, 22, 25, 26, 29, 33, 37, Figs. 1, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 19, 21, 24, 26, 28, 29, 30, 31, 32, 33, 47, 48, 69, 71, 72, 73, 74, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at 1:24-25, 1:46-47, 5:30-31, 6:62-7:8, 15:31-36, 16:19-41, Figs. 3, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:61-3:8, 3:9-20, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49- 9:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at 1:14-21, 1:22-28, 1:37-44, 2:35-44, 3:46-4:12;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 3:1-3, 3:4- 6, 3:7-9, 3:10-15, 3:14-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Figs. 1, 2, 3, 4, 5, 6, 7;

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- RD-15 (Ruckerbauer) at Abstract, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33- 45, 7:29-48, 8:58-9:3, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, Claims 1, 2, 5, Figs. 1, 2, 4, 5;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6- 7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at 1a;
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 2:48-51, 3:24-27, 3:31-35, 3:36-39, 8:6-7, 8:8-20, 10:51-55, 10:56- 59, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 4, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at 1a.

It was well-known to one of skill in the art before the time of the ’060 patent, at least

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partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports; *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 21, 25, 44, 46, 50, 51, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 23, 27, 47, 48, 49, Claim 1, Fig. 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 6:10-18, 6:32-39, Claims 1, 2, 3, 5, 10, Figs. 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 7, 11, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 62, 121, Claim 1, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 64, 65, 66, 67, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 27, 36, 37, 38, 41, 58, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 20C;
- RD-8 (Foster) at Abstract, 1:27- 44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 40, Figs. 1, 2, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 38, 39, 40, 41, 47, 48, 69, 70, 71, 72, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 5:30-31,

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5:32-45, 5:46-47, 5:48-6:3, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;

- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39- 43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:35-44, 4:21-45, 5:58- 6:3, Claim 1, Figs. 4, 7;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16- 44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:57-3:6, 8:58-9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:51-61, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 3:27-30, 4:25-34, 4:48-50, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00*

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September 2011 at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at 1b;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B.
- RD-21 (Micron LRDIMM System) at Ex. E-21 at 1b.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. *See, e.g.*,

- '060 patent at 1:30- 56, 18:14-30, 18:37-56, Figs. 1B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 36, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 13, 14, 15, 16, 17, 23, 27, 28, 29, 30, 32, 33, 45, 47, 48, 49, Claim 1, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 4:6-23, 5:66-6:9, 6:10-18, 6:19-26,

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6:27-31, 6:32-39, 6:40-50, 6:51-62, Claim 1, Figs. 2, 5 and 6;

- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 64, 65, 66, 67, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at ¶¶ 14, 27, 36, 37, 38, 39, 40, 41, 42, 43, 58, 79, Figs. 1, 2, 10, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 16, 18, 19, 22, 23, 24, 33, 39, 53, Figs. 2, 5 *see also* Jeddeloh 365 at Abstract, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 20, 24, 26, 28, 30, 35, 38, 39, 40, 41, 47, 48, 53, 69, 79, Figs. 1, 3, 5;
- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20- 23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;

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- RD-15 (Ruckerbauer) at 1:7-23, 1:46-53, 2:57-3:6, 8:58-9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, Claims 1, 2, 5, Figs. 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:56-3:2, 3:3-7, 3:8-23, 8:27-51, 3:52-61, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, *Committee Item Number 1777.00* at 8, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, *Committee Item Number 1797.00 September 2011* at 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at E-19 at 1c;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:4-6, 3:24-27, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at 1c.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory package can include a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first

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terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:37-56, 18:57-19:7, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 25, 26, 27, 28, 29, 30, 32, 33, 35, 36, 45, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 45, 46, 48, 62, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 14, 16, 21, 27, 38, 41, 57, 62, 79, Figs. 1, 2, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 14, 19, 21, 22, 23, 24, 25, 33, 37, Figs. 1, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;

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- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 19, 21, 24, 26, 28, 29, 30, 31, 32, 47, 48, 53, 69, 71, 72, 73, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56- 10:22, Claims 10, 11, Figs. 3, 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55- 64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 4:55-5:4:3, 5:24-38, 6:11-29, 6:53- 62, 6:63-7:3, 7:4-20, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37- 44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 4:21-45, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claim 1, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56-10:8, 10:28-36, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at

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6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, *Committee Item Number 1787.01* at 4, 8;

- RD-19 (Micron Hybrid Memory Cube System) at E-19 at 1d;
- RD-20 (Lee) at Abstract, 1:30-36, 3:4-6, 3:24-27, 3:31-35, 7:44-57, 7:58-8:5, 10:51-55, 10:56-59, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, Figs. 3, 12A, 12B, 13, 14, 22A, 22B and 24;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at 1d.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control signals can include data path control signals for controlling the first and second data conduits. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 3:65-67, 18:37-56, 19:41-63, Figs. 1A, 1B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20 Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-

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41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;

- RD-5 (Riho 293) at
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30- 31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3,

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5:24-38, 5:39-48, 5:49- 62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4- 13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46- 65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18- 24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at

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3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at *claim 2*;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 2.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control circuit can be configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 3:65-67, 18:37-56, 19:41-63, Figs. 1A, 1B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20 Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19,

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21, 25, Figs. 1, 2, 3, 5;

- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-

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2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21- 38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58- 6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56- 10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at

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6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at E-19 at claim 3;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44- 45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B.
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 3.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the control signals can include command/address signals and the control die can be configured to provide the command/address signals to the plurality of stacked array dies. *See, e.g.*,

- ’060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103,

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104, 105, 106, 107, Claims 1, 19, 20 Figs. 2C, 2F, 10;

- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48- 63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32- 33, 1:46-47, 5:30-31, 6:31-

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49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;

- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24- 27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62,

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Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 4;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44- 45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 4.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the first die interconnect can comprise a first through-silicon via and the second die interconnect can comprise a second through-silicon via. *See, e.g.*,

- ’060 patent at 1:30-56, 5:46- 62, 18:14-30, 18:37-56, Figs. 1B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 23, 36, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, Fig. 2C;

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- RD-3 (Kim) at Abstract, ¶¶ 13, 14, 15, 16, 17, 23, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, Claims 1, 15, 16, 17, 19, 20, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:49-67, 4:6-23, 4:42-57, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claim 1, Figs. 2, 3, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 64, 65, 66, 67, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at ¶¶ 14, 27, 36, 37, 38, 39, 40, 41, 42, 43, 45, 49, 58, 79, Figs. 1, 2, 10, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 16, 18, 19, 22, 23, 24, 33, 39, 53, Figs. 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 20, 24, 26, 28, 30, 35, 38, 39, 40, 41, 47, 48, 53, 69, 79, Figs. 1, 3, 5;
- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53-62, 6:63- 7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:22-28, 1:14-21, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58- 6:3,

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6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;

- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at 1:7-23, 1:23-42, 1:46-53, 2:57-3:6, 3:11-20, 3:40-48, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:15-27, 10:28-36, 10:40-43, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:56-3:2, 3:3-7, 3:8-23, 8:27-51, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, *Committee Item Number 1777.00* at 8, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, *Committee Item Number 1797.00 September 2011* at 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 5.
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:4-6, 3:24-27, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A,

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6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 5.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control die can further comprise chip-select conduits, and the memory package can further comprise third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies. *See, e.g.*,

- '060 patent at 1:23- 29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24- 41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claims 1, 2, 3, 5, 10, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 41, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;

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- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 40, 53, Figs. 1, 2, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:28-29, 1:32-33, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61- 3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45- 52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15- 20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5- 8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 4:30-57, 4:64-67, 5:1-11, 5:9-16, 5:33-46, 5:47-55, 5:56-57, 5:58-6:15, 6:29-40, 6:41-56, 6:57-7:20, 7:21- 45, 7:46-63, 7:64-

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8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;

- RD-15 (Ruckerbauer) at Abstract, 1:7- 23, 1:23-42, 1:46-53, 2:17-24, 2:57-3:6, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:28-36, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45- 46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22- 32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40- 48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 6;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 10:40-42, 10:43- 50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65- 16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14,

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24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 6.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die can be selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63- 2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 3:35-42, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 6:63-7:3, Claims 1, 2, 3, 5, 10, Figs. 1, 2, 5 and 6;

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- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 41, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, 99, 100, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 40, 53, Figs. 1, 2, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 54, 69, 70, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:28- 29, 1:32-33, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9- 25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34- 35, 1:37-44, 1:45-52, 2:11-

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13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;

- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:9-23, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56-10:8, 10:28-36, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 7;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47,

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7:44-57, 7:58-8:5, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 7.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the respective states of the first data conduit and the second data conduit can be controlled by one or more data path control signals, and the control die can be configurable to operate in any one of a first mode and a second mode, wherein in the first mode, the control die receives the data path control signals from the one or more external devices; and in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 38, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19,

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21, 25, Figs. 1, 2, 3, 5;

- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66- 6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48- 63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32- 33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-

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2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15- 27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8- 23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6,

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8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at E-19 at claim 8;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46- 52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B.
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 8.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the control die can further comprise command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address. *See, e.g.*,

- ’060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103,

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104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;

- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 75, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46- 57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31- 49,

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6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;

- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63- 6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30- 57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17- 24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28- 35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18- 21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32- 36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-

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62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 9;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 9.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the control die can further comprise one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies. *See, e.g.*,

- ’060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 10:56-67, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs.

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1A, 1B, 6A, 6B and 7;

- RD-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, 100, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 74, 79, 90, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66- 7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29,

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30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1- 8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 5:33-45, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:28-36, 10:40-43, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30- 38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41,

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7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44- 50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at E-19 at claim 10;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:38-50, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 10.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory package can include a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external

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devices. *See, e.g.*,

- '060 patent at 1:30-56, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 4, 9, 21, 22, 25, 33, 51, 76, 82, 84, 87, Claims 1, 19, 20, Figs. 2C, 3, 4, 5, 6;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 28, 29, 30, 50, Claims 1, 5, 6, 10, 11, 14, 15, 18, 19, 21, 25, Figs. 1, 2;
- RD-4 (Ware) at 2:59-3:3, 4:24-41, 4:58-5:9, 7:4-18, Claims 1 and 3, Figs. 1, 2, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 4, 12, 15, 16, 26, 30, 31, 33, Claim 1, Figs. 1 and 2;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 69, 70, 71, 72, 73, Claims 1, 11, Figs. 1, 2 and 3B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 17, 27, 38, 41, 42, 43, 47, 58, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 2:12-15, 4:1-25, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 5, 7, 15, 21, 22, 25, 26, 29, 33, 37, Figs. 1, 4, 5 *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 19, 21, 24, 26, 28, 29, 30, 31, 32, 33, 47, 48, 69, 71, 72, 73, 74, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at 1:24-25, 1:46-47, 5:30-31, 6:62-7:8, 15:31-36, 16:19-41, Figs.

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3, 9;

- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:61-3:8, 3:9-20, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at 1:14-21, 1:22-28, 1:37-44, 2:35-44, 3:46-4:12;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:14-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:29-48, 8:58- 9:3, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, Claims 1, 2, 5, Figs. 1, 2, 4, 5;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item*

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Number 1787.05 at 2, 4, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at E-19 at claim 11a;
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 2:48-51, 3:24-27, 3:31-35, 3:36-39, 8:6-7, 8:8-20, 10:51-55, 10:56-59, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15- 18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20- 24, Figs. 4, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 11a.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 21, 25, 44, 46, 50, 51, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 23, 27, 47, 48, 49, Claim 1, Fig. 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 6:10-18, 6:32-39, Claims 1, 2, 3, 5, 10, Figs. 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 7, 11, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 62, 121, Claim 1, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 64, 65, 66, 67, 73, 74, 75, 76, 26, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 27, 36, 37, 38, 41, 58, 79, Claims 1, 12, Figs.

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1, 2, 5B, 10, 12, 20C;

- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12- 15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 40, Figs. 1, 2, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 38, 39, 40, 41, 47, 48, 69, 70, 75, 71, 72, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:34-35, 1:28-29, 1:32-33, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53- 62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:19-20, 2:35-44, 2:11-13, 4:21-45, 5:58-6:3, Claim 1, Figs. 4, 7;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:57-3:6, 8:58-9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, 13:18-21, Claims 1, 2, 5;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23,

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4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51- 62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 11b;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 11b.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory package can include at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second

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die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. *See, e.g.*,

- '060 patent at 1:30- 56, 18:14-30, 18:37-56, Figs. 1B and 7;
- RD-2 (Rajan 137) at ¶¶ 6, 36, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, Fig. 2C; RD-3 (Kim) at Abstract, ¶¶ 13, 14, 15, 16, 17, 23, 27, 28, 29, 30, 32, 33, 47, 48, 49, Claim 1, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59- 60, 2:1-36, 4:6-23, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claim 1, Figs. 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 64, 65, 66, 67, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at ¶¶ 14, 27, 36, 37, 38, 39, 40, 41, 42, 43, 58, 79, Figs. 1, 2, 10, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 16, 18, 19, 22, 23, 24, 33, 39, 53, Figs. 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 20, 24, 26, 28, 30, 35, 38, 39, 40, 41, 47, 48, 53, 69, 79, Figs. 1, 3, 5;
- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20- 23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:20-

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33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;

- RD-13 (Wyman) at Abstract, 1:22-28, 1:14-21, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at 1:7-23, 1:46-53, 2:57-3:6, 8:58-9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, Claims 1, 2, 5, Figs. 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:56-3:2, 3:3-7, 3:8-23, 8:27-51, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, *Committee Item Number 1777.00* at 8, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, *Committee Item Number 1797.00 September 2011* at 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-21 at claim 11c;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47- 54, 2:37-39, 3:4-6, 3:24-27, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:19-21, 23:22-30, 23:44-

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45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 11c.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, at least a second data conduit between the second die interconnect and the first terminal, and chip select conduits for providing chip select signals to respective array dies. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 45, 46, 48, 62, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 59, 60, 64, 65, 66, 67, 70, 71,

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72, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 3A, 3B and 7B;

- RD-7 (Best) at Abstract, ¶¶ 2, 14, 16, 21, 27, 38, 41, 57, 62, 79, Figs. 1, 2, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 14, 19, 21, 22, 23, 24, 25, 33, 37, Figs. 1, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 19, 21, 24, 26, 28, 29, 30, 31, 32, 47, 48, 53, 69, 71, 72, 73, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Claims 10, 11, Figs. 3, 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 4:55-5:4:3, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 4:21-45, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claim 1, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12- 33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 4:30-57, 4:64- 67, 5:1-11, 5:9-16, 5:33-46, 5:47-55, 5:56-57, 5:58-6:15, 6:29-40, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56- 10:8, 10:28-36,

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13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;

- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25- 31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, *Committee Item Number 1787.01* at 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 11d;
- RD-20 (Lee) at Abstract, 1:30-36, 3:4-6, 3:24-27, 3:31-35, 7:44-57, 7:58-8:5, 10:51-55, 10:56-59, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, Figs. 3, 12A, 12B, 13, 14, 22A, 22B and 24;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 11d.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the control die can further comprise a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected

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by at least one of the chip-select signals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8- 15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10- 18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claims 1, 2, 3, 5, 10, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 41, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 40, 53, Figs. 1, 2, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;

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- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56- 10:22, Claims 10, 11, Figs. 3, 5A, 6;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39- 43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 4:30-57, 4:64-67, 5:1-11, 5:9-16, 5:33- 46, 5:47-55, 5:56-57, 5:58-6:15, 6:29-40, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12- 50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:57-3:6, 3:11-20, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49- 55, 9:56-10:8, 10:28-36, 12:1-24, 13:18-21, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-

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41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 11e;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 10:40-42, 10:43- 50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65- 16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 11e.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the chip select conduits can pass through the control die. *See, e.g.*,

- ’060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67,

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4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;

- *RD*-2 (Rajan 137) at ¶¶ 6, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claims 1, 2, 3, 5, 10, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 41, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58- 6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 40, 53, Figs. 1, 2, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 75,

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79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:28-29, 1:32-33, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63- 7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58- 6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40- 48, 4:8-19, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49- 55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A, 7, 8;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-

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41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 12;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 12.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the chip select conduits can include drivers to drive the chip select signals to the respective array dies. *See, e.g.*,

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- ’060 patent at 1:23-29, 1:30-56, 1:57-62, 2:8-15, 3:61-64, 3:65- 67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claims 1, 2, 3, 5, 10, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 41, 43, 45, 46, 62, 79, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, 99, 100, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 40, 53, Figs. 1, 2, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24,

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26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:28-29, 1:32-33, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49- 63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44- 50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46- 2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 4:30-57, 4:64-67, 5:1-11, 5:9-16, 5:33-46, 5:47-55, 5:56-57, 5:58-6:15, 6:29-40, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56-10:8, 10:28-36, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41,

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7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32- 36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 13;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22- 29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46- 52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 13.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the first die interconnect can comprise one or more through silicon vias and the

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second die interconnect can comprise one or more through silicon vias. *See, e.g.*,

- '060 patent at 1:30-56, 5:46-62, 18:14-30, 18:37-56, Figs. 1B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 23, 36, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 13, 14, 15, 16, 17, 23, 27, 28, 29, 30, 32, 33, 47, 48, 49, Claim 1, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 4:6-23, 4:42-57, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40- 50, 6:51-62, Claim 1, Figs. 2, 3, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 64, 65, 66, 67, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at ¶¶ 14, 27, 36, 37, 38, 39, 40, 41, 42, 43, 45, 49, 58, 79, Figs. 1, 2, 10, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58- 6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 16, 18, 19, 22, 23, 24, 33, 39, 53, Figs. 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 20, 24, 26, 28, 30, 35, 38, 39, 40, 41, 47, 48, 53, 69, 79, Figs. 1, 3, 5;
- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:20-

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33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66- 11:7, Figs. 1, 5, 7;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21- 30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12- 33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at 1:7-23, 1:23- 42, 1:46-53, 2:57-3:6, 3:11-20, 3:40-48, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:15-27, 10:28-36, 10:40-43, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65- 67, 2:6-7, 2:56-3:2, 3:3-7, 3:8-23, 8:27-51, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, *Committee Item Number 1777.00* at 8, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, *Committee Item Number 1797.00 September 2011* at 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 14;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:4-6,

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3:24-27, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 14.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control die can be configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and the chip select signal can be generated using an address signal in the control/address signals. *See, e.g.*,

- '060 patent at 1:30- 56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 38, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10- 18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;

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- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12- 15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46- 47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-

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13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;

- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4- 13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46- 65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18- 24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;

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- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 16;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 16.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control circuit can control the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;

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- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58- 6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62- 7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3,

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5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30- 57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17- 24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28- 35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18- 21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32- 36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock*

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Proposal at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at E-19 at claim 17;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 17.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control/address signals can comprise at least one command signal, at least one address signal, and at least one data path control signal. *See, e.g.*,

- '060 patent at 1:30-56, 1:57- 62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21- 40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;

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- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 38, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1- 25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10,

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11, Figs. 3, 5A, 6, 9;

- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4- 13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46- 65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18- 24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

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- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 18;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 18.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control die can be configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and the control circuit can control the respective states of the first data conduit in response to the data path control signals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B

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and 7;

- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29,

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30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21- 38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58- 6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45- 46, 2:56-3:2, 3:3-7, 3:8-23,

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4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22- 32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40- 48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 19;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44- 45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 19.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that load can be optimized in a memory package comprising a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array

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die, at least a first die interconnect and a second die interconnect, a control die, and a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 2, 4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 35, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 3:35-42, 4:6-23, 4:24-41, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 6:63-7:3, 7:4-18, Claims 1, 2, 3, 5, 10, Figs 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, 99, 100, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A and 7B;

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- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47, 5:30-31, 5:32-45, 5:46- 47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-

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60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;

- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 20pre;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59,

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10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 20pre.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for optimizing load in such a memory package can include receiving a data signal at a first terminal of the plurality of input/output terminals. *See, e.g.*,

- '060 patent at 1:30-56, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 9, 21, 22, 25, 33, 51, 76, 82, 84, 87, Claims 1, 19, 20, Figs. 2C, 3, 4, 5, 6;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 28, 29, 30, 50, Claims 1, 5, 6, 10, 11, 14, 15, 18, 19, 21, 25, Figs. 1, 2;
- RD-4 (Ware) at 2:59- 3:3, 4:24-41, 4:58-5:9, 7:4-18, Claims 1 and 3, Figs. 1, 2, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 4, 12, 15, 16, 26, 30, 31, 33, Claim 1, Figs. 1 and 2;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 69, 70, 71, 72, 73, Claims 1, 11, Figs. 1, 2 and 3B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 17, 27, 38, 41, 42, 43, 47, 58, 79, Claims 1,

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12, Figs. 1, 2, 5B, 10, 12, 13, 20C;

- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 2:12-15, 4:1-25, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 5, 7, 15, 21, 22, 25, 26, 29, 33, 37, Figs. 1, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 19, 21, 24, 26, 28, 29, 30, 31, 32, 33, 47, 48, 69, 71, 72, 73, 74, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at 1:24-25, 1:46-47, 5:30-31, 6:62-7:8, 15:31-36, 16:19-41, Figs. 3, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:61-3:8, 3:9-20, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at 1:14-21, 1:22-28, 1:37-44, 2:35-44, 3:46-4:12;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12- 33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:14-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4- 13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46- 65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;

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- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25- 31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 20a;
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 2:48-51, 3:24-27, 3:31-35, 3:36-39, 8:6-7, 8:8-20, 10:51-55, 10:56-59, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44- 45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 4, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 20a.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a method for optimizing load in such a memory package can include receiving control signals at second terminals of the plurality of input/output terminals. *See, e.g.*,

- ’060 patent at 1:30-56, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56,

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- *RD*-2 (Rajan 137) at ¶¶ 4, 9, 21, 22, 25, 33, 51, 76, 82, 84, 87, Claims 1, 19, 20, Figs. 2C, 3, 4, 5, 6;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 28, 29, 30, 50, Claims 1, 5, 6, 10, 11, 14, 15, 18, 19, 21, 25, Figs. 1, 2;
- RD-4 (Ware) at 2:59-3:3, 4:24-41, 4:58-5:9, 7:4-18, Claims 1 and 3, Figs. 1, 2, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 4, 12, 15, 16, 26, 30, 31, 33, Claim 1, Figs. 1 and 2;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 69, 70, 71, 72, 73, Claims 1, 11, Figs. 1, 2 and 3B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 17, 27, 38, 41, 42, 43, 47, 58, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 2:12-15, 4:1-25, 5:58-6:15, 6:16-32, 6:66- 7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 5, 7, 15, 21, 22, 25, 26, 29, 33, 37, Figs. 1, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 19, 21, 24, 26, 28, 29, 30, 31, 32, 33, 47, 48, 69, 71, 72, 73, 74, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at 1:24-25, 1:46-47, 5:30-31, 6:62-7:8, 15:31- 36, 16:19-41, Figs. 3, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-

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2:10, 2:61-3:8, 3:9-20, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at 1:14-21, 1:22-28, 1:37-44, 2:35-44, 3:46-4:12;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:14-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49- 62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;

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- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 20b;
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 2:48-51, 3:24-27, 3:31-35, 3:36-39, 8:6-7, 8:8-20, 10:51-55, 10:56-59, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 4, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 20b.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for optimizing load in such a memory package can include providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-

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18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;

- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20- 33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

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- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30- 57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17- 24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18- 24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee*

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Item Number 1787.05 at 2, 4, *Committee Item Number 1787.01* at 3, 4;

- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-21 at claim 20c;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 20c.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for optimizing load in such a memory package can include selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;

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- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66- 7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1,

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3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1- 8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56-10:8, 10:28-36, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16,

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13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 20d;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22- 30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 20d.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a method for optimizing load in such a memory package can include selecting a first driver size for the first driver based, at least in part, on a load on the first driver and selecting a second driver size for the second driver based, at least in part, on a load on the second driver. *See, e.g.*,

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- ’060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 3:35-42, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32- 39, 6:40-50, 6:51-62, 6:63-7:3, Claims 1, 2, 3, 5, 10, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 41, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, 99, 100, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 40, 53, Figs. 1, 2, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21,

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24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 54, 69, 70, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63- 7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58- 6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:9-23, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56-10:8, 10:28-36, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

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- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 21;
- RD-20 (Lee) at Abstract, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:1-3, 3:4-6, 3:24- 27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15- 18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20- 24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 21.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the method for optimizing load in such a memory package can include generating the chip select signals from at least some of the control signals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;

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- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1,

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3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4- 13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46- 65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41,

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7:42-48, 7:49-62, 8:27-51, 12:18- 24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 23;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60- 67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 23.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control signals can include the chip-select signals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A,

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6B and 7;

- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66- 6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48- 63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29,

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30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32- 33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15- 27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8- 23,

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4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 24;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36- 39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46- 52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 24.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the first and second die interconnects can each comprise at least one through silicon vias. *See, e.g.*,

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- ’060 patent at 1:30-56, 5:46-62, 18:14-30, 18:37-56, Figs. 1B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 23, 36, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 13, 14, 15, 16, 17, 23, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, Claims 1, 15, 16, 17, 19, 20, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:49- 67, 4:6-23, 4:42-57, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claim 1, Figs. 2, 3, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 64, 65, 66, 67, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 3B, 7A and 7B;
- RD-7 (Best) at ¶¶ 14, 27, 36, 37, 38, 39, 40, 41, 42, 43, 45, 49, 58, 79, Figs. 1, 2, 10, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 16, 18, 19, 22, 23, 24, 33, 39, 53, Figs. 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 20, 24, 26, 28, 30, 35, 38, 39, 40, 41, 47, 48, 53, 69, 79, Figs. 1, 3, 5;
- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21- 38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10,

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6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at 1:7-23, 1:23-42, 1:46-53, 2:57-3:6, 3:11-20, 3:40-48, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:15- 27, 10:28-36, 10:40-43, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:56-3:2, 3:3-7, 3:8-23, 8:27- 51, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, *Committee Item Number 1777.00* at 8, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, *Committee Item Number 1797.00 September 2011* at 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 25;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:4-6, 3:24-27, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52,

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21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 25.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the chip select signals can pass through through-silicon-vias in the control die. *See, e.g.*,

- '060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51- 62, Claim 1, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 59, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, Figs. 1, 2, 3A, 3B, 7A

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and 7B;

- RD-7 (Best) at ¶¶ 2, 14, 16, 27, 36, 37, 38, 39, 40, 41, 42, 43, 57, 58, 62, 79, Figs. 1, 2, 9, 10, 12, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 14, 16, 18, 19, 21, 22, 23, 24, 25, 33, 37, 39, 53, Figs. 1, 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63- 6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45- 3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11- 20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49- 55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-

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36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;

- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 26;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 26.

It was well-known to one of skill in the art before the time of the ’060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement

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contentions, that the method for optimizing load in such a memory package can further include generating data path control signals from at least some of the control signals, the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:37-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51- 62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;

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- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66- 7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1- 8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;

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- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 27;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4,

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6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 27.

It was well-known to one of skill in the art before the time of the '060 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the one of the first driver and the second driver can be selected using at least some of the control signals. *See, e.g.*,

- '060 patent at 1:30-56, 1:57-62, 1:63-2:7, 2:8-15, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 6, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, 23, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51- 62, 7:4-18, Claims 1 and 3, Figs. 1, 2, 5, 6 and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38,39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B and 7B;

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- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38,39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66- 7:27, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 71, 72, 73, 74, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1- 8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:9-20, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57,

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4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;

- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. E-19 at claim 28;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33,

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22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. E-21 at claim 28.

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time that the disclosures relating to memory devices and circuitry could be integrated into memory modules.

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;

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- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33– 37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58- 5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46- 47, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9- 25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;

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- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65- 2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27- 51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number*

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1797.00 June 2011 at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;

- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3;
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48- 51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B;
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

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In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the ’060 Patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the Asserted Claims are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the ’060 Patent. See ’060 patent at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7. Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent ’060 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

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In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix E for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

b) *Obviousness Combinations*

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix E with any other reference or references listed in Appendix E along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '060 patent. For example, and without limitation, the Asserted Claims of the '060 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
Asserted Patent's Admitted Prior Art (APA) (RA-1)	• U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent No. 9,142,262 (Ware) (RD-4)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12)

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	• U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low	• Asserted Patent's Admitted Prior Art (APA) (RA-1)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
Power Memories (JEDEC HBM and Low Power Proposals) (RD-18)	• U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
Micron Hybrid Memory Cube (RD-19)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication

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	No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,471,362 (Lee) (RD-20)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
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Micron LRDIMM System (RD-21)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • The knowledge of a person of ordinary skill.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a

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Markman Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

6. U.S. Patent No. 9,318,160

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix F the prior art references that render obvious the Asserted Claims of the '160 patent and include below exemplary combinations showing the obviousness of the '160 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix F, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of skill in the art at the time of the '160 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix F, such reference may be combined with any other references listed in Appendix F for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '160 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '160 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

a) *Obviousness Rationale*

For at least the reasons described in these contentions, it would have been obvious to one

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of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix F along with the knowledge of one of ordinary skill in the art to meet the limitations of the '160 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '160 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix F would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one

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known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix F would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the '160 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix F is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified

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predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces. Additionally, it would be obvious to one of skill in the art to consult and/or combine any of the prior art listed in Appendix F because all of these references relate to the same area of technology and/or are from analogous art. The '160 patent Asserted Claims are directed to memory packages with stacked array dies and related methods for reducing the load of drivers on the memory modules. '160 patent at Abstract, 1:20-24. The '160 patent Asserted Claims merely unite old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the '160 patent Asserted Claims.

All of the '160 patent Asserted Claims are directed to memory packages with stacked array dies or related methods for reducing the load of drivers on the memory modules. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, was widely known before the alleged priority date of the '160 Patent, as evidenced by the references in Appendix F. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70,

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75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;

- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59- 3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27- 31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75,

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76, 79, Figs. 1, 3, 5, 6;

- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47, 5:30-31, 5:32-45, 5:46-47, 5:48- 6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36- 42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65- 67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23,

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4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B;

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- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix F because at the time of the alleged invention reducing the load of drivers in a memory package on a memory module was a common problem with a well-known solution. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97,

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98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;

- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13- 26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46- 47, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9- 25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65- 2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;

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- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27- 51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List*

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Presentation at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.

- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B;
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

Further, it was common knowledge to one of skill in the art at the time of the alleged invention that reducing the load of drivers in a memory package can improve performance of the memory module. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;

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- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51- 62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66- 7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47,

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5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65- 8:12, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;

- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 3:9- 20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58- 6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56- 3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33- 41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16,

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13:40-48, 14:6- 10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3.
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46- 52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B;
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10,

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11, fig. 2.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix F at the time of the alleged invention. Common problems with conventional techniques for reducing the load of drivers in a memory package were known to persons of ordinary skill in the art and electrically communicating with groups of array dies was a well-known solution to achieve improved performance. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30- 56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22,

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26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;

- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46-47, 5:30-31, 5:32-45, 5:46-47, 5:48- 6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50- 60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46- 4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4,

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7, 8, 9;

- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36- 42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65- 67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;
- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List*

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Presentation at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3;

- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38- 52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B;
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

Memory packages were well-known to one of skill in the art before the time of the '160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions. *See, e.g.*,

- '160 patent at 1:25-31, 1:32-58, 1:65-2:9, 4:58-5:14, 18:45-62, 18:63-19:8, Figs. 1A and 1B;
- RD-2 (Rajan 137) at Abstract, ¶¶ 2, 6, 17, 24, 43, 44, Figs. 1, 2C;
- RD-3 (Kim) at Abstract, ¶¶ 23, 27, 46, 47, 48, 49, 50, Fig. 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:59-60, 6:32-39, 5:10-15, Claims 1, 3, 5, Figs. 1 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 7, 11, 13, 15, 16, 18, 26, 28, 29, 30, 31,

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33, 37, 38, 62, 121, Claim 1, Figs. 1, 2 and 4;

- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 64, Figs. 1, 2, 3A;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 27, 36, 37, 58, 79, Claims 1, 12, Figs. 5B, 10, 12, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 14, 15, 16, 17, 18, 9, 40, Figs. 1, 2, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 16, 20, 21, 24, 26, 28, 29, 30, 31, 32, 47, 69, 70, 75, 71, 72, 73, Figs. 1, 3, 5, 6,
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 5:30-31, 5:32-45, 5:46-47, 5:48- 6:3, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55- 64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49- 62¸5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, Claim 1;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 8:58-9:3, 9:4-13, Claim 1, Fig. 5;

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- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62- 6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 1pre;
- RD-20 (Lee) at Abstract, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 2:37-39, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44- 45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14¸ 24:15-19, 24:20-24; Figs. 1A, 1B, 1C, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 1pre.

It was well-known to one of skill in the art before the time of the ’160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory package can include data terminals and control terminals. *See, e.g.*,

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- ’160 patent at 1:32-58, 3:64-67, 4:1-3, 18:5-18, 18:26-44, 18:45-62, 18:63-19:8, 19:9-25, 19:26-48, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 9, 21, 22, 25, 33, 51, 75, 76, 82, 84, 87, Claims 1, 19, 20, Figs. 2C, 3, 4, 5, 6;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 28, 29, 30, 50, Claims 1, 5, 6, 10, 11, 14, 15, 18, 19, 21, 25, Figs. 1 and 2;
- RD-4 (Ware) at 2:59-3:3, 4:24-41, 4:58-5:9, 7:4-18, Claims 1, 3, Figs. 2, 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 4, 12, 15, 16, 26, 30, 31, 33, Claim 1, Figs. 1 and 2;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 69, 70, 71, 72, 73, Claims 1, 11, Figs. 1, 2, 3B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 17, 27, 38, 41, 42, 43, 47, 58, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:13-26, 1:7-10, 2:12-15, 4:1-25, 6:66-7:27, 5:58-6:15, 6:16-32, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 5, 7, 15, 21, 22, 25, 26, 29, 33, 37, Figs. 1, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 19, 21, 24, 26, 28, 29, 30, 31, 32, 33, 47, 48, 69, 71, 72, 73, 74, 75, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at 1:24-25, 1:46-47, 5:30-31, 6:62-7:8, 15:31-36, 16:19-41, Figs. 3, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-

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2:10, 2:61-3:8, 3:9- 20, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at 1:14-21, 1:22-28, 1:37-44, 2:35-44, 3:46-4:12;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:14-15, 3:19-38, 3:57- 4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:29-48, 8:58-9:3, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, Claims 1, 2, 5, Figs. 1, 2, 4, 5;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25- 31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 1a;

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- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 2:48-51, 3:24-27, 3:31-35, 3:36-39, 8:6-7, 8:8-20, 10:51-55, 10:56-59, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25,22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 4, 22A, 22B, 24, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 1a.

It was well-known to one of skill in the art before the time of the '160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include stacked array dies including a first group of array dies and a second group of at least one array die. *See, e.g.*,

- '160 patent at 1:25-31, 1:32-58, 1:59- 64, 4:58-5:14, 18:5-18, 18:26-44, 18:45-62, 18:63-19:8, 19:26-48, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 21, 25, 44, 46, 50, 51, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 23, 27, 47, 48, 49, Claim 1, Fig. 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33–37, 1:45-47, 1:59- 60, 2:1-36, 6:32-39, 5:10-15, 6:10-18, 6:32-39, Claims 1, 2, 3, 5, Figs. 1 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 7, 11, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 37, 38, 62, 121, Claim 1, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 20, 21, 22, 26, 64, 65, 66, 67, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 8, 14, 16, 27, 36, 37, 38, 41, 58, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 2:12-15, 5:46-57, 5:58-6:15, Fig. 3;

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- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 9, 14, 15, 16, 17, 18, 40, Figs. 1, 2, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 38, 39, 40, 41, 47, 48, 69, 70, 75, 71, 72, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 5:30-31, 5:32-45, 5:46-47, 5:48- 6:3, 6:62-7:8, 7:9-17, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:55- 64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14- 21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:35-44, 4:21-45, 5:58-6:3, Claim 1, Figs. 4, 7;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34-45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 2:17-24, 2:57-3:6, 8:58-9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8- 23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48,

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14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;

- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 1b;
- RD-20 (Lee) at Abstract, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:47-54, 2:37-39, 3:4-6, 3:24-27, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 3:1-3, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 3:31-35, 23:8-10, 23:11-14, 23:15-18, 3:36-39, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B and 24;
- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 1b.

It was well-known to one of skill in the art before the time of the ’160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory package can include first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. *See, e.g.*,

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- ’160 patent at 1:32- 58, 4:1-3, 18:5-18, 18:26-44, 18:45-62, Figs. 1B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 36, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 67, Fig. 2C;
- RD-3 (Kim) at Abstract, ¶¶ 13, 14, 15, 16, 17, 23, 27, 28, 29, 30, 33, 47, 48, 49, Claim 1, Figs. 1, 2, 3, 5
- RD-4 (Ware) at 1:59- 60, 2:1-36, 4:6-23, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claim 1, Figs. 2 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 37, 38, 43, 45, 46, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 64, 65, 66, 67, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶ 2, 8, 14, 16, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 48, 58, 79, Claim 12, Figs. 1, 2, 5B, 10, 12, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 16, 18, 19, 22, 23, 24, 33, 39, 53, Figs. 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 7, 8, 9, 10, 11, 12, 20, 24, 26, 28, 30, 35, 38, 39, 40, 41, 47, 48, 53, 69, 79, Figs. 1, 3, 5;
- RD-11 (Bilger) at Abstract, 1:28-29, 1:32-33, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Figs. 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 5:24-38, 5:39-48, 5:49-62, 5:63-

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6:10, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64- 8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at 1:7-23, 1:46-53, 2:57-3:6, 8:58- 9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, Claims 1, 2, 5, Figs. 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:56-3:2, 3:3-7, 3:8-23, 8:27-51, Figs. 1, 4;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, *Committee Item Number 1777.00* at 8, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, *Committee Item Number 1797.00 September 2011* at 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 1c;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 3:4-6, 3:24-27, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs.

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1A, 1B, 1C, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 1c.

It was well-known to one of skill in the art before the time of the '160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory package can include a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size. *See, e.g.*, '160 patent at 1:32-58, 1:59-64, 1:65-2:9, 2:10-17, 3:64-67, 4:1-3, 4:58-5:14, 18:26- 44, 18:45-62, 19:9-25, 19:26-48, Figs. 1A, 1B, 6A, 6B and 7;

- *RD*-2 (Rajan 137) at ¶¶ 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 96, 103, 104, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. ,1 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 3:35-42, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 6:63-7:3;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36,

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37, 38, 39, 41, 45, 46, 62, Claims 1, 5, Figs. 1, 2 and 4;

- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 41, 47, 48, 57, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58- 6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 14, 19, 21, 22, 23, 24, 25, 33, 37, Figs. 1, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 6, 7, 8, 9, 10, 11, 12, 19, 21, 24, 26, 28, 29, 30, 31, 32, 47, 48, 53, 54, 69, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Claims 10, 11, Figs. 3, 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 4:55-5:4:3, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 4:21-45, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claim 1, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:46-63, 7:64-8:11, 8:12-50, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23-42, 1:46-53, 3:11-20, 7:24-27, 7:29-48, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:56-10:8, 10:28- 36, 13:18-

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21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;

- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30- 38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51- 62, Claims 1, 4, 5, 8, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, *Committee Item Number 1787.01* at 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 1d;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 1d.

It was well-known to one of skill in the art before the time of the '160 patent, at least

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partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the second die interconnects can be longer than the first die interconnects, and the second driver size can be larger than the first driver size. *See, e.g.*,

- '160 patent at 1:32-58, 1:59-64, 1:65-2:9, 2:10-17, 3:64-67, 4:1-3, 4:58-5:14, 18:26-44, 18:45-62, 19:9-25, 19:26-48, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 6, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 96, 103, 104, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. ,1 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 4:6-23, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, Claim 1, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 48, 57, 58, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 5, 14, 16, 17, 18, 19, 22, 23, 24, 25, 33, 37, 39, 53, Figs. 1, 2, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;

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- RD-10 (Gillingham) at ¶¶ 6, 7, 8, 9, 10, 11, 12, 19, 20, 21, 24, 26, 28, 30, 31, 32, 35, 38, 39, 40, 41, 47, 48, 53, 54, 69, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28- 29, 1:32-33, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Claims 10, 11, Figs. 3, 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 4:55-5:4:3, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 10:66-11:7, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14- 21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claim 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at 1:7-23, 1:46-53, 2:57-3:6, 7:9-23, 8:58-9:3, 9:4-13, 9:14-27, 9:49-55, 12:1-24, Claims 1, 2, 5, Figs. 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27-51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51- 62, Claims 1, 4, 5, 8, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8,

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9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4, 8;

- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 2;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1-5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;
- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 2.

It was well-known to one of skill in the art before the time of the ’160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that the first driver size and the second driver size can be related to a load on the first driver and a load on the second driver. *See, e.g.*,

- ’160 patent at 1:32-58, 1:59-64, 1:65-2:9, 2:10- 17, 3:64-67, 4:1-3, 4:58-5:14, 18:26-44, 18:45-62, 19:9-25, 19:26-48, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 103, 104, 105, 106, 107, Figs. 2C, 2F, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30,

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32, 33, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, Figs. ,1 2, 3, 5;

- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40- 50, 6:51-62, Figs. 1, 2, 5 and 6;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 5, 6, 7, 12, 13, 15, 16, 18, 26, 28, 29, 30, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2 and 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 20, 22, 26, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 48, 57, 58, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:27-44, 1:48-63, 5:46-57, 5:58-6:15, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, Figs. 1, 2, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at ¶¶ 6, 7, 8, 9, 10, 11, 12, 19, 21, 24, 26, 28, 29, 30, 31, 32, 47, 48, 53, 54, 69, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28-29, 1:32-33, 5:30- 31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, Claims 10, 11, Figs. 3, 5A, 6;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 4:55-5:4:3, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, Figs. 1, 5, 7;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8,

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6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claim 1, 2, Figs. 4, 7, 8, 9;

- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:7-9, 3:10-15, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;
- RD-15 (Ruckerbauer) at 1:7-23, 1:23-42, 1:46-53, 2:57-3:6, 3:11-20, 7:9-23, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:28-36, 12:1- 24, 13:18-21, Claims 1, 2, 5, 7, Figs. 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30- 38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51- 62, Claims 1, 4, 5, 8, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, *Committee Item Number 1787.01* at 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 4;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:60-

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65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 4.

It was well-known to one of skill in the art before the time of the '160 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the control die can further comprise a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals. *See, e.g.*,

- '160 patent at 1:32-58, 1:59-64, 1:65-2:9, 2:10-17, 3:64-67, 4:1-3, 4:58-5:14, 18:5-18, 18:26-44, 18:45-62, 18:63-19:8, 19:9-25, 19:26-48, Figs. 1A, 1B, 6A, 6B and 7;
- *RD*-2 (Rajan 137) at ¶¶ 4, 9, 21, 22, 25, 26, 29, 33, 35, 36, 44, 45, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67,68, 69, 70, 76, 82, 84, 87, 103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. ,1 2, 3, 5;
- RD-4 (Ware) at 1:57-58, 1:59-60, 2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58-5:9, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51- 62, 7:4-18, Claims 1, 3, Figs. 1, 2, 5, 6, and 8;
- RD-5 (Riho 293) at Abstract, ¶¶ 3, 4, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36,

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37, 38, 39, 41, 45, 46, 48, 62, Claims 1, 5, Figs. 1, 2 and 4;

- RD-6 (Riho 364) at Abstract, ¶¶ 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 94, 95, 96, 97, 98, Claims 1, 11, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 41, 42, 43, 47, 48, 57, 58, 62, 76, 79, Claims 1, 12, Figs. 1, 2, 5B, 10, 12, 13, 17A, 20C;
- RD-8 (Foster) at Abstract, 1:13-26, 1:7-10, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:66-7:27, 5:58-6:15, 6:16-32, Fig. 3;
- RD-9 (Jeddeloh) at ¶¶ 1, 5, 7, 14, 15, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, Figs. 1, 4, 5; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 19, 21, 24, 26, 28, 29, 30, 31, 32, 33, 47, 48, 53, 54, 69, 71, 72, 73, 75, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:24-25, 1:28- 29, 1:32-33, 1:46-47, 5:30-31, 6:31-49, 6:62-7:8, 8:27-67, 9:1-8, 9:9-25, 9:56-10:22, 15:31-36, 16:19-41, Claims 10, 11, Figs. 3, 5A, 6, 9;
- RD-12 (Keeth) at Abstract, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64, 1:65-2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:9-20, 4:55-5:4:3, 5:24-38, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, Figs. 1, 5, 7, 10;
- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35- 44, 4:21-45, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31-43, 6:44-50, 6:51-7:3, Claim 1, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:46-2:4, 2:5-14, 2:64-65, 2:66-67, 3:7-9, 3:10-s15,

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6:41-56, 6:57- 7:20, 7:46-63, 7:64-8:11, 8:12-50, Claim 1, Figs. 1, 2, 5, 6;

- RD-15 (Ruckerbauer) at Abstract, 1:7- 23, 1:23-42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 10:28-36, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs.1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49- 62, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 13, 14, 16, 17, 18, *Committee Item Number 1777.00* at 6, 8, 9, *Committee Item Number 1782.01* at 5, *Read Clock Proposal* at 3, 4, *Item Number 1777.29* at 2, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7,9, 11, 12, 18, 20, *Committee Item Number 1787.05* at 2, 4, *Committee Item Number 1787.01* at 3, 4, 8;
- RD-19 (Micron Hybrid Memory Cube System) at Ex. F-19 at claim 5;
- RD-20 (Lee) at Abstract, 1:17-21, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48-51, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56- 59, 10:60-67, 13:60-65, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52,

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23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 3, 4, 6A, 6B, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A and 26B;

- RD-21 (Micron LRDIMM System) at Ex. F-21 at claim 5.

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time that the disclosures relating to memory devices and circuitry could be integrated into memory modules.

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*,

- RD-1 (Admitted Prior Art) at 1:23-29, 1:30-56, 1:57-62, 1:63-2:7, 3:61-64, 3:65-67, 4:55-5:11, 18:14-30, 18:38-56, 18:57-19:7, 19:8-20, 19:21-40, 19:41-63, Figs. 1A, 1B, 6A, 6B, 7,
- RD-2 (Gillingham) at Abstract, ¶¶ 2,4, 6, 9, 17, 21, 22, 24, 25, 26, 29, 33, 36, 43, 44, 45, 46, 48, 49, 50, 51, 52, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 75, 76, 82, 84, 87,103, 104, 105, 106, 107, Claims 1, 19, 20, Figs. 1, 2C, 2F, 3, 4, 5, 6, 10;
- RD-3 (Kim) at Abstract, ¶¶ 3, 5, 12, 13, 14, 15, 16, 17, 23, 25, 26, 27, 28, 29, 30, 32, 33, 46, 47, 48, 49, 50, Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 14, 15, 16, 17, 18, 19, 21, 25, Figs. 1, 2, 3, 5;
- RD-4 (Ware) at Abstract, 1:18-20, 1:24-32, 1:33– 37, 1:45-47, 1:57-58, 1:59-60,

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2:1-36, 2:59-3:3, 3:4-18, 3:19-34, 4:6-23, 4:24-41, 4:42-57, 4:58- 5:9, 5:10-15, 5:66-6:9, 6:10-18, 6:19-26, 6:27-31, 6:32-39, 6:40-50, 6:51-62, 7:4-18, Claims 1, 2, 3, 5, 6, 10, Figs. 1, 2, 5, 6, 8;

- RD-5 (Riho 293) at Abstract, ¶¶ 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 16, 18, 26, 28, 29, 30, 31, 33, 36, 37, 38, 39, 41, 43, 45, 46, 48, 62, 121, Claims 1, 5, Figs. 1, 2, 4;
- RD-6 (Riho 364) at Abstract, ¶¶ 3, 5, 6, 9, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 26, 37, 59, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 74, 75, 76, 80, 94, 95, 96, 97, 98, Claims 1, 8, 11, 18, Figs. 1, 2, 3A, 3B, 7A, 7B;
- RD-7 (Best) at Abstract, ¶¶ 2, 8, 14, 16, 17, 21, 27, 36, 37, 38, 39, 40, 41, 42, 43, 47, 57, 58, 62, 79, Claims 1, 2, 12, Figs. 1, 2, 5B, 9, 10, 12, 13, 20C;
- RD-8 (Foster) at Abstract, 1:7-10, 1:13-26, 1:27-44, 1:48-63, 2:12-15, 4:1-25, 5:46-57, 5:58-6:15, 6:16-32, 6:66-7:27, Figs. 3;
- RD-9 (Jeddeloh) at Abstract, ¶¶ 1, 2, 5, 7, 9, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 29, 33, 37, 39, 40, 53, Figs. 1, 2, 3, 4, 5, 5A; *see also* Jeddeloh 365 at Abstract, 1:57-2:14, 2:33-62, 2:63-3:27, 3:29-61, 6:1-29, Figs. 1, 2A, 2B, 4, 5;
- RD-10 (Gillingham) at Abstract, ¶¶ 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 16, 19, 20, 21, 24, 26, 28, 29, 30, 31, 32, 33, 35, 38, 39, 40, 41, 47, 48, 53, 69, 70, 71, 72, 73, 74, 75, 76, 79, Figs. 1, 3, 5, 6;
- RD-11 (Bilger) at Abstract, 1:6-7, 1:24-25, 1:28-29, 1:32-33, 1:34-35, 1:46- 47, 5:30-31, 5:32-45, 5:46-47, 5:48-6:3, 6:31-49, 6:62-7:8, 7:9-17, 7:65-8:12, 8:27-67, 9:1-8, 9:9- 25, 9:56-10:22, 12:34-39, 12:40-48, 12:49-63, 15:31-36, 16:19-41, Claims 1, 10, 11, Figs. 3, 5A, 6, 7A, 9;
- RD-12 (Keeth) at Abstract, 1:11-16, 1:20-23, 1:33-35, 1:39-43, 1:48-51, 1:55-64,

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1:65- 2:10, 2:11-19, 2:20-33, 2:34-49, 2:50-60, 2:61-3:8, 3:21-38, 3:9-20, 4:55-5:4, 5:24-38, 5:39-48, 5:49-62, 5:63-6:10, 6:11-29, 6:53-62, 6:63-7:3, 7:4-20, 8:49-9:7, 10:66-11:7, Figs. 1, 5, 7, 10;

- RD-13 (Wyman) at Abstract, 1:14-21, 1:22-28, 1:34-35, 1:37-44, 1:45-52, 2:11-13, 2:19-20, 2:21-23, 2:24-25, 2:35-44, 2:45-3:7, 3:46-4:12, 4:21-45, 5:45-57, 5:58-6:3, 6:4-8, 6:15-20, 6:21-30, 6:31- 43, 6:44-50, 6:51-7:3, Claims 1, 2, Figs. 4, 7, 8, 9;
- RD-14 (Ma) at Abstract, 1:5-8, 1:12-33, 1:34- 45, 1:46-2:4, 2:5-14, 2:16-44, 2:45-60, 2:64-65, 2:66-67, 3:1-3, 3:4-6, 3:7-9, 3:10-15, 3:19-38, 3:57-4:29, 4:30-57, 4:58-63, 5:27-32, 6:41-56, 6:57-7:20, 7:21-45, 7:46-63, 7:64-8:11, 8:12-50, 8:51-9:3, 9:4-42, Claim 1, Figs. 1, 2, 3, 4, 5, 6, 7;
- RD-15 (Ruckerbauer) at Abstract, 1:7-23, 1:23- 42, 1:46-53, 2:17-24, 2:25-30, 2:47-56, 2:57-3:6, 3:11-20, 3:40-48, 5:33-45, 7:24-27, 7:29-48, 8:58-9:3, 9:4-13, 9:14-27, 9:28-35, 9:36-42, 9:43-48, 9:49-55, 9:56-10:8, 10:9-14, 10:15-27, 11:46-65, 12:1-24, 13:18-21, Claims 1, 2, 5, 7, Figs. 1, 2, 4, 5, 5A;
- RD-16 (Loh) at 453, 454, 455, 456;
- RD-17 (Rajan 881) at Abstract, 1:65-67, 2:6-7, 2:45-46, 2:56-3:2, 3:3-7, 3:8-23, 4:25-34, 5:36-43, 5:62-6:2, 6:30-38, 6:39-56, 6:57-7:3, 7:4-21, 7:22-32, 7:33-41, 7:42-48, 7:49-62, 8:27- 51, 12:18-24, 12:25-31, 12:32-36, 12:48-55, 13:6-16, 13:40-48, 14:6-10, 14:11-26, 14:27-36, 14:37-39, 14:39-43, 14:44-50, 14:51-62, Claims 1, 4, 5, 8, 9, 10, 12, 15, 16, 25, Figs. 1, 4, 18;
- RD-18 (JEDEC HBM and Low Power Proposals) at *Committee Item Number 1797.00 June 2011* at 5, 6, 7, 13, 14, 16, 17, 18, *Committee Item Number*

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1777.00 at 6, 8, 9, *Committee Item Number 1782.01* at 2, 3, 5, 6, *Read Clock Proposal* at 3, 4, *Committee Item Number 1777.18* at 3, *Committee Item Number 1797.00 September 2011* at 5, 6, 7, 9, 11, 12, 18, 20, *Committee Item Number 1787.01* at 3, 4, 8, *Item Number 1777.29* at 2, *Committee Item Number 1787.05* at 2, 4;

- RD-19 (Micron Hybrid Memory Cube) at *Hot Chips HMC Presentation* at pgs. 1, 4, 5, 6, 8, 13; *Phoenix 2nd Generation Presentation* at pgs. 2, 3; *Pad List Presentation* at pgs. 2, 5; *HBDRAM Gen2 Cube Design Guide* at pgs. vii, 1, 3; *E80a Design Review* at pgs. 87, 89; *IBM/Micron 3D Collaboration* at pgs. 10, 14, *HBDRAM Solutions* at pgs. 9, 10; *DDR4 Core Design Guide* at pg. 3;
- RD-20 (Lee) at Abstract, 1:30-36, 1:47-54, 1:17-21, 1:22-29, 1:30-36, 1:43-46, 1:47-54, 2:37-39, 2:48- 51, 3:1-3, 3:4-6, 3:24-27, 3:31-35, 3:36-39, 4:18-30, 4:31-34, 4:35-39, 4:40-47, 7:44-57, 7:58-8:5, 8:6-7, 8:8-20, 10:40-42, 10:43-50, 10:51-55, 10:56-59, 10:60-67, 13:24-26, 13:27-43, 13:44-52, 13:53-65, 13:66-14:3, 15:65-16:9, 21:22-37, 21:38-52, 21:53-22:3, 22:4-19, 22:20-25, 22:26-33, 22:34-45, 23:8-10, 23:11-14, 23:15-18, 23:19-21, 23:22-30, 23:44-45, 23:46-52, 23:64-67, 24:1- 5, 24:6-9, 24:10-14, 24:15-19, 24:20-24, Figs. 1A, 1B, 1C, 4, 6A, 6B, 11, 12A, 12B, 13, 14, 22A, 22B, 24, 25, 26A, 26B;
- RD-21 (Micron LRDIMM System) at *Micron LRDIMM Data Sheet* at pgs. 4, 5, 10, 11, fig. 2.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

In accordance with these advances, the prior art could have been combined according to

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methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '160 Patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the Asserted Claims are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the '160 Patent. See '160 patent at 1:25-31, 1:32-58, 1:59-64, 1:65-2:9, 2:10-17, 3:64-67, 4:1-3, 4:58-5:14, 18:5-18, 18:26-44, 18:45-62, 18:63-19:8, 19:9-25, 19:26-48, Figs. 1A, 1B, 6A, 6B, and 7. Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '160 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix F for additional

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motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

b) *Obviousness Combinations*

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix F with any other reference or references listed in Appendix F along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '160 patent. For example, and without limitation, the Asserted Claims of the '160 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
Asserted Patent's Admitted Prior Art (APA) (RA-1)	• U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13)

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U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory

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U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology,

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U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer

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U.S. Patent No. 8,258,619 (Foster) (RD-8)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16)

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U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth

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U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	skill.
Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,041,881 (Rajan 881) (RD-17)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication

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JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication

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Micron Hybrid Memory Cube (RD-19)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3)

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	• U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • Micron LRDIMM System (RD-21) • The knowledge of a person of ordinary skill.
U.S. Patent No. 8,471,362 (Lee) (RD-20)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4)

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
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• Micron LRDIMM System (RD-21)	• Asserted Patent's Admitted Prior Art (APA) (RA-1) • U.S. Patent Application Publication No. 2008/0025137 (Rajan 137) (RD-2) • U.S. Patent Application Publication No. 2011/0103156 (Kim) (RD-3) • U.S. Patent No. 9,142,262 (Ware) (RD-4) • U.S. Patent Application Publication

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Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	No. 2011/0026293 (Riho 293) (RD-5) • U.S. Patent Application Publication No. 2010/0195364 (Riho 364) (RD-6) • U.S. Patent Application Publication No. 2010/0091537 (Best) (RD-7) • U.S. Patent No. 8,258,619 (Foster) (RD-8) • U.S. Patent Application Publication No. 2010/0110745 (Jeddeloh) (RD-9); *see also* Jeddeloh 365 • U.S. Patent Application Publication No. 2011/0208906 (Gillingham) (RD-10) • U.S. Patent No. 8,120,958 (Bilger) (RD-11) • U.S. Patent No. 9,123,552 (Keeth) (RD-12) • U.S. Patent No. 7,969,192 (Wyman) (RD-13) • U.S. Patent No. 9,160,349 (Ma) (RD-14) • U.S. Patent No. 7,796,446 (Ruckerbauer) (RD-15) • Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh) (RD-16) • U.S. Patent No. 8,041,881 (Rajan 881) (RD-17) • JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals) (RD-18) • Micron Hybrid Memory Cube (RD-19) • U.S. Patent No. 8,471,362 (Lee) (RD-20) • The knowledge of a person of ordinary skill.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary

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combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

V. P.R. 3-3(c) – Claim Charts

Pursuant to Rule 3-3(d), Defendants identify invalidity claim charts identifying disclosures in the references identified in Section III supra as to the Asserted Claims of the Asserted Patents are provided in attached Appendix A (’506 Patent), Appendix B (’339 Patent), Appendix C (’918 Patent), Appendix D (’054 Patent), Appendix E (’060 Patent), an Appendix F (’160 Patent).

Defendants have identified relevant portions and/or features of the prior art. However, the identified prior art may contain additional descriptions of or alternative support for the claim limitations. Defendants may rely on uncited portions or features of the identified prior art, other documents, and expert testimony, to provide context or to aid in understanding the identified prior art and the state of the art. Citations to a particular figure in a reference include the caption and description of the figure and any text relating to the figure. Similarly, citations to particular text referring to a figure include the figure and caption as well. Portions relevant to dependent claims incorporate by reference the citations to the chain of claims from which that dependent claim derives. Likewise, portions related to subsequent limitations that refer to claim elements identified, described, and/or cited to in earlier limitations may rely on the citations related to those portions of the claim chart that identify and/or describe these elements.

Throughout the invalidity claim charts in Appendices A-F, Defendants provide examples of where references disclose subject matter recited in preambles of the Asserted Claims, regardless whether the preambles limit the claims. Defendants reserve the right to argue that the preambles are or are not limitations. Further, where an entry in a claim chart corresponding to a

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given limitation refers back to the discussion of another claim, the entry incorporates all evidence cited for the other claim.

VI. P.R. 3-3(d) – Other Grounds for Invalidity

A. U.S. Patent No. 10,860,506

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '506 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '506 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '506 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '506 patent Asserted Claims at the time the '506 patent was filed. Ariad Pharms., Inc. v. Eli Lilly & Co., 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the

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claimed subject matter as of the filing date." Id. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '506 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '506 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '506 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[76]

Term	Relevant Claim(s)
"memory module"	1, 2, 3, 5, 11, 12, 13, 14
"edge connections"	1, 14
"coupled"	1, 3, 14, 15, 16
"respective signal lines"	1, 14
"module control device"	1, 14
"a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals"	1
"receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines"	14
"outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe"	14
"outputting, at the module control device, module control signals"	14

[7] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed

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Term	Relevant Claim(s)
"receiving, at each of the data buffers, the module control signals from the module control device"	14
"data buffer"	1, 2, 3, 11, 14, 15, 16
"data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data	1
buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus"	
"data buffers on the module board and coupled between the edge connections and the memory devices"	14
"the method further comprising, at the first data buffer, in response to one of more of the module control signals: delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe; sampling the first section of the read data using the first delayed read strobe; and transmitting the first section of the read data to a first section of the data bus"	14
"wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals: delay the second read strobe by a second predetermined amount to generate a second delayed read strobe; sample the second section of the read data using the second delayed read strobe; and transmit the second section of the read data to a second section of the data bus"	2
"wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals: delay the third read strobe by a third predetermined amount to generate a third delayed read strobe; sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of	3

Term	Relevant Claim(s)
the data bus”	
“the method further comprising, at the second data buffer, in response to the one or more of the module control signals: delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe; sampling the second section of the read data using the second delayed read strobe; and transmitting the second section of the read data to a second section of the data bus”	15
“the method further comprising, at the first data buffer, in response to the one or more of the module control signals: delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe; sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus”	16
“first predetermined amount”	1, 11, 14
“second predetermined amount”	2, 15
“third predetermined amount”	3, 16
“determined”	1, 2, 3, 15, 16
“determining”	14
“based at least on”	1, 2, 3, 11, 14
“signals”	1, 2, 3, 11, 14, 15, 16
“received”	1, 2, 3, 11, 14, 15, 16
“receiving”	14, 16
“during”	1, 2, 3, 11, 15, 16
“previous operations”	1, 2, 3, 11, 15, 16
“before”	14
“wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations”	1
“wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations”	2, 15
“wherein the third predetermined amount is determined based at least	3, 16

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Term	Relevant Claim(s)
on signals received by the first data buffer during one or more previous operations"	
"the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer"	14

2. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v.* Biosig Instruments, Inc., 572 U.S. 898, 901 (2014). Several of the '506 patent Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite under § 112, ¶ 2, for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the '506 patent Asserted Claims are indefinite in whole, in part or in combination:[8]

Term	Relevant Claim(s)
"memory module"	1, 2, 3, 5, 11, 12, 13, 14
"edge connections"	1, 14
"coupled"	1, 3, 14, 15, 16
"respective signal lines"	1, 14
"module control device"	1, 14
"a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module	1

[8] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
control signals”	
“receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines”	14
“outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe”	14
“outputting, at the module control device, module control signals”	14
“receiving, at each of the data buffers, the module control signals from the module control device”	14
“data buffer”	1, 2, 3, 11, 14, 15, 16
“data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or	1
more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus”	
“data buffers on the module board and coupled between the edge connections and the memory devices”	14
“the method further comprising, at the first data buffer, in response to one of more of the module control signals: delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe; sampling the first section of the read data using the first delayed read strobe; and transmitting the first section of the read data to a first section of the data bus”	14
“wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals: delay the second read strobe by a second predetermined amount to generate a second delayed read strobe; sample the second section of the read data using the second delayed read strobe; and	2

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Term	Relevant Claim(s)
transmit the second section of the read data to a second section of the data bus”	
“wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals: delay the third read strobe by a third predetermined amount to generate a third delayed read strobe; sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus”	3
“the method further comprising, at the second data buffer, in response to the one or more of the module control signals: delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe; sampling the second section of the read data using the second delayed read strobe; and transmitting the second section of the read data to a second section of the data bus”	15
“the method further comprising, at the first data buffer, in response to the one or more of the module control signals: delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe; sampling the third section of the read data using the third delayed read strobe concurrently with	16
receiving the first section of the read data using the first delayed read strobe; and transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus”	
“first predetermined amount”	1, 11, 14
“second predetermined amount”	2, 15
“third predetermined amount”	3, 16
“determined”	1, 2, 3, 15, 16
“determining”	14
“based at least on”	1, 2, 3, 11, 14
“signals”	1, 2, 3, 11, 14, 15, 16
“received”	1, 2, 3, 11, 14, 15, 16

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Term	Relevant Claim(s)
"receiving"	14, 16
"during"	1, 2, 3, 11, 15, 16
"previous operations"	1, 2, 3, 11, 15, 16
"before"	14
"wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations"	1
"wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations"	2, 15
"wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations"	3, 16
"the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer"	14

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '506 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '506 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '506 patent Asserted Claims are indefinite in whole, in part or in combination:[8]

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Term	Relevant Claim(s)
"module control device"	1, 14

B. U.S. Patent No. 10,949,339

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '339 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '339 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. <u>Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1</u>

The '339 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '339 patent Asserted Claims at the time the '339 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." Id. One of ordinary skill in the art would not have

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understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '339 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '339 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '339 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[9]

Term	Relevant Claim(s)
"memory module	All claims
"edge connector"	1, 11, 19, 27
"positioned"	1, 11, 19, 27
"on an edge"	1, 11, 19, 27
"releasably coupled"	1, 11, 19, 27
"corresponding contacts"	1, 11, 19, 27
"module controller"	1, 7, 10, 11, 16, 18, 19, 21, 27, 33
"a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the	1
memory controller into a first N-bit-wide rank of the multiple N- bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N- bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals"	
" a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable	11

[9] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank among the multiple N-bit-wide ranks, and to output registered address and control signals in response to the input address and control signal, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit- wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals"	
" a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit- wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N- bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output	19
second module control signals for the second memory operation in response to receiving the second address and control signals"	
" a module controller coupled to the PCB and configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in	27

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Term	Relevant Claim(s)
response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals”	
“cause”	1, 11, 19, 29
“receive”	1, 3, 8, 10, 11, 14, 18, 19, 23, 27, 30, 33
“receiving”	1, 11, 19, 27, 29, 33
“by receiving”	1, 11, 27, 29
“wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data”	1, 11
“wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation”	19
“the first registered address and control signals cause one rank of DDR DRAM devices to perform the memory write operation by receiving the write data”	29
“the second registered address and control signals cause one rank of DDR DRAM devices to perform the memory read operation by outputting the read data.”	29
“byte-wise buffer”	1, 3, 4, 10
“plurality of buffers” / “each respective buffer”	19, 22
“data buffer” / “n-bit-wide data buffer” / “n-bit wide buffer”	27, 29
“data transmission circuit”	11, 15, 17, 18
“a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines”	1
“n/2 data transmission circuits mounted on the PCB, wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data signal	11

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Term	Relevant Claim(s)
lines among the plurality of sets of data signal lines, and wherein the each of the n/2 data transmission circuits has a first side configured to be operatively coupled to the respective set of data signal lines, a second side that is operatively coupled to a respective pair of DDR DRAM devices in each of the multiple ranks via respective module data lines, and data paths between the first side and the second side"	
"a plurality of buffers coupled to the PCB and configured to receive the first module control signals and to receive the second module control signals, wherein each respective buffer of the plurality of buffers has a first side that is operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines"	19
"a plurality of n-bit-wide data buffers coupled to the PCB and configured to receive the first module control signals and subsequently the second module control signals, wherein each respective n-bit-wide data buffer of the plurality of n-bit-wide data buffers has a first side that is operatively coupled to a respective set of data signal lines, and a second side that is operatively coupled to a respective n-bit-wide section of the DDR DRAM devices via respective module data lines"	27
"byte-wise data path"	1, 3, 10
"byte-wise data path between the first side and the second side"	1
"data paths"	11, 14, 18, 19, 26
"data paths between the first side and the second-side"	11, 19
"disposed"	1, 11, 19
"respective position" / "respective positions"	1, 11, 19
"respective set of the plurality of sets of data signal lines" / "respective set of data signal lines"	1, 3, 10, 11, 14, 17, 18, 19, 27
"wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines"	1
" wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data signal lines among the plurality of sets of data signal lines"	11
" wherein the each respective buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines"	19

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Term	Relevant Claim(s)
“logic”	1, 6, 10, 19, 26, 27, 28, 33
“logic configurable to”	1, 19, 27
“control the byte-wise data path”	1, 10
“control at least the first set of tristate buffers and the second set of tristate buffers”	27
“wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals”	1
“ wherein, in response to the module control signals, each respective data transmission circuit is configurable to enable the data paths for a first time period in accordance with a latency parameter to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period”	11
“ wherein the each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period, wherein the data paths are disabled after the first time period and before the second time period”	19
“ the each respective n-bit-wide data buffer includes a first set of input buffers configurable to receive a respective n-bit section of the write data from the respective set of data signal lines, a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, a second set of input buffers configurable to receive a respective n-bit section of the read data from the respective module data lines, a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers”	27
“ the logic in response to the first module control signals is configured to enable the first set of tristate buffers for a first time period corresponding to the memory write operation to drive the respective n-bit section of the write data”	27

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Term	Relevant Claim(s)
“ the logic in response to the second module control signals is configured to enable the second set of tristate buffers for a second time period corresponding to the memory read operation to drive the respective n-bit section of the read data”	27
“ the first set of tristate buffers are disabled during the second time period”	27
“ the second set of tristate buffers are disabled during the first time period”	27
“enable” / “enables”	1, 6, 11, 18, 19, 27, 33
“enabled”	1, 2, 10, 18, 26, 34, 35
“disable”	6, 33
“disabled”	10, 18, 19, 26, 27, 28
“drive”	1, 2, 3, 10, 11, 14, 18, 19, 26, 27, 33
“driven”	30
“actively drive”	1, 10, 11, 18, 19
“ wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period”	1
“ wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period”	1
“ wherein the data paths includes first tristate buffers, and the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit- wide ranks, and to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks”	11

2. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." Nautilus, Inc. v. Biosig Instruments, Inc., 572 U.S. 898, 901 (2014). Several of the '339 patent Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite under § 112, ¶ 2, for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the '339 patent Asserted Claims are indefinite in whole, in part or in combination:[10]

Term	Relevant Claim(s)
"memory module	All claims
"edge connector"	1, 11, 19, 27
"positioned"	1, 11, 19, 27
"on an edge"	1, 11, 19, 27
"releasably coupled"	1, 11, 19, 27
"corresponding contacts"	1, 11, 19, 27
"module controller"	1, 7, 10, 11, 16, 18, 19, 21, 27, 33
"a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N- bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N- bit-wide rank to perform the memory write operation by receiving the N-bit-	1

[10] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals”	
“ a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank among the multiple N-bit-wide ranks, and to output registered address and control signals in response to the input address and control signal, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit- wide write data, wherein the module controller is further	11
configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals”	
“ a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit- wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N- bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals”	19
“ a module controller coupled to the PCB and configurable to receive from the memory controller via the address and control signal lines	27

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Term	Relevant Claim(s)
first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals”	
“cause”	1, 11, 19, 29
“receive”	1, 3, 8, 10, 11, 14, 18, 19, 23, 27, 30, 33
“receiving”	1, 11, 19, 27, 29, 33
“by receiving”	1, 11, 27, 29
“wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data”	1, 11
“wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation”	19
“the first registered address and control signals cause one rank of DDR DRAM devices to perform the memory write operation by receiving the write data”	29
“the second registered address and control signals cause one rank of DDR DRAM devices to perform the memory read operation by outputting the read data.”	29
“byte-wise buffer”	1, 3, 4, 10
“plurality of buffers” / “each respective buffer”	19, 22
“data buffer” / “n-bit-wide data buffer” / “n-bit wide buffer”	27, 29
“data transmission circuit”	11, 15, 17, 18
“a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide	1

Term	Relevant Claim(s)
ranks via respective module data lines”	
“n/2 data transmission circuits mounted on the PCB, wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data signal lines among the plurality of sets of data signal lines, and wherein the each of the n/2 data transmission circuits has a first side configured to be operatively coupled to the respective set of data signal lines, a second side that is operatively coupled to a respective pair of DDR DRAM devices in each of the multiple ranks via respective module data lines, and data paths between the first side and the second side”	11
“a plurality of buffers coupled to the PCB and configured to receive the first module control signals and to receive the second module control signals, wherein each respective buffer of the plurality of buffers has a first side that is operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines”	19
“a plurality of n-bit-wide data buffers coupled to the PCB and configured to receive the first module control signals and	27
subsequently the second module control signals, wherein each respective n-bit-wide data buffer of the plurality of n-bit-wide data buffers has a first side that is operatively coupled to a respective set of data signal lines, and a second side that is operatively coupled to a respective n-bit-wide section of the DDR DRAM devices via respective module data lines”	
“byte-wise data path”	1, 3, 10
“byte-wise data path between the first side and the second side”	1
“data paths”	11, 14, 18, 19, 26
“data paths between the first side and the second-side”	11, 19
“disposed”	1, 11, 19
“respective position” / “respective positions”	1, 11, 19
“respective set of the plurality of sets of data signal lines” / “respective set of data signal lines”	1, 3, 10, 11, 14, 17, 18, 19, 27
“wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines”	1
“ wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data	11

Term	Relevant Claim(s)
signal lines among the plurality of sets of data signal lines”	
“ wherein the each respective buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines”	19
“logic”	1, 6, 10, 19, 26, 27, 28, 33
“logic configurable to”	1, 19, 27
“control the byte-wise data path”	1, 10
“control at least the first set of tristate buffers and the second set of tristate buffers”	27
“wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals”	1
“ wherein, in response to the module control signals, each respective data transmission circuit is configurable to enable the data paths for a first time period in accordance with a latency parameter to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period”	11
“ wherein the each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data	19
associated with the second memory operation from the second side to the first side during the second time period, wherein the data paths are disabled after the first time period and before the second time period”	
“ the each respective n-bit-wide data buffer includes a first set of input buffers configurable to receive a respective n-bit section of the write data from the respective set of data signal lines, a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, a second set of input buffers configurable to receive a respective n-bit section of the read data from the respective module data lines, a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and	27

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Term	Relevant Claim(s)
the second set of tristate buffers”	
“ the logic in response to the first module control signals is configured to enable the first set of tristate buffers for a first time period corresponding to the memory write operation to drive the respective n-bit section of the write data”	27
“ the logic in response to the second module control signals is configured to enable the second set of tristate buffers for a second time period corresponding to the memory read operation to drive the respective n-bit section of the read data”	27
“ the first set of tristate buffers are disabled during the second time period”	27
“ the second set of tristate buffers are disabled during the first time period”	27
“enable” / “enables”	1, 6, 11, 18, 19, 27, 33
“enabled”	1, 2, 10, 18, 26, 34, 35
“disable”	6, 33
“disabled”	10, 18, 19, 26, 27, 28
“drive”	1, 2, 3, 10, 11, 14, 18, 19, 26, 27, 33
“driven”	30
“actively drive”	1, 10, 11, 18, 19
“ wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period”	1
“ wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period”	1
“ wherein the data paths includes first tristate buffers, and the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit- wide ranks,	11

Term	Relevant Claim(s)
and to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks"	

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. Ibormeith IP, LLC v. Mercedes-Benz USA, LLC, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '339 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '339 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '339 patent Asserted Claims are indefinite in whole, in part or in combination: [11]

Term	Relevant Claim(s)
"module controller"	1, 7, 10, 11, 16, 18, 19, 21, 27, 33
"logic"	1, 6, 10, 19, 26, 27, 28, 33
"logic configurable to"	1, 19, 27
"data transmission circuit"	11, 15, 17, 18
"byte-wise buffer"	1, 3, 4, 10

[11] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
"buffer"	19, 22, 26

C. U.S. Patent No. 11,016,918

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '918 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '918 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '918 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '918 patent Asserted Claims at the time the '918 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have

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understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '918 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '918 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '918 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[12]

Term	Relevant Claim(s)
"regulated voltage(s)"	All asserted claims
"memory module"*	All asserted claims
"voltage amplitude(s)"	1-3, 5-7, 9-13, 15-22
"a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude"*	1-3, 5-7, 9-13, 15
"converter circuit"*	All asserted claims
"a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude"	1-3, 5-7, 9-13, 15
"at least one circuit"*	1-3, 5-7, 9-13, 15, 21
"the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage"	1-3, 5-7, 9-13, 15, 21
"wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes"	1-3, 5-7, 9-13, 15, 21
"circuit operable to"	1-3, 5-7, 9-13, 15, 21
"at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and	1-3, 5-7, 9-13, 15

[12] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices"*	
"a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices"*	1-3, 5-7, 9-13, 15
"dual buck converter"	2, 17
"voltage monitor circuit"*	5-6, 16-22, 24-27
"the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage"	5-7, 9-13
"wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage"	6-7
"voltage level"	7, 9
"configuration information"	10-11, 15, 22
"non-volatile memory"*	10-12, 15, 19, 22, 26
"a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information"	10-11
"in response to the trigger signal, the logic element writes information into the non-volatile memory"	11
"a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory"	12
"wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit"	13
"write operation" / "writes information into the non-volatile memory" / "write operation to the non-volatile memory" / "writing data information into non-volatile memory" / "writing data information to non-volatile memory"*	11-12, 18-19, 25-26
"logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile	15

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Term	Relevant Claim(s)
memory is configured to store configuration information"	
"pre-regulated input voltage"	16-22, 30
"input voltage"	16-22
"first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; ; a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage"*	16-22
"a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage"*	16-22
"wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively"*	16-22
"the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices"	16-22
"the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage"	16-22
"a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal"	18-19
"a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element"	22
"wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts"	20, 29
"selectively switched on or off"	23-30
"powered on"	23-30
"switched on" / "switched off"	23-30
"each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages"*	23-30
"first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and a converter circuit configured to provide the fourth regulated voltage"*	23-30

Term	Relevant Claim(s)
"wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on, wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals"*	23-30
"the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage"*	23-30
"pre-regulated voltage input"	30
"a converter circuit configured to provide the fourth regulated voltage"	23-30
"the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage"	24-27
"a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation"	25-26
"wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage"	27
"wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage"	30

*In addition, claims reciting these terms are invalid under 35 U.S.C. § 112, ¶ 1 because the entirety of the specification does not support the breadth of the claims as written. For example, and without limitation, the entirety of the specification clearly indicates that it is narrower than the claims reciting a "memory module" such that those claims are invalid for lack of written description. For example, the title of the '918 patent is "Flash-DRAM Hybrid Memory

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Module" but independent claims 1, 16, and 23 of the '918 patent do not require use of Flash or non- volatile memory.

2. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014). Several of the '918 patent Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite under § 112, ¶ 2, for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the '918 patent Asserted Claims are indefinite in whole, in part or in combination: [13]

Term	Relevant Claim(s)
"regulated voltage(s)"	All asserted claims
"converter circuit"	All asserted claims
"voltage amplitude(s)"	1-3, 5-7, 9-13, 15-22
"circuit [operable to]"	1-3, 5-7, 9-13, 15, 21
"wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes"	1-3, 5-7, 9-13, 15
"dual buck converter"	2, 17
"voltage level"	7, 9
"configuration information" / "information" / "data information"	10-11, 15, 19, 22, 26
"controller"	12, 18-19, 25-26
"logic element including one or more integrated circuits and discrete electrical elements"	15

[13] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
“pre-regulated input voltage”	16-22, 30
“input voltage”	5-7, 13, 16-22, 24-27, 30
“wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts”	20, 29
“selectively switched on or off”	23-30
“powered on”	8, 23-30
“switched on” / “switched off”	8, 23-30
“pre-regulated voltage input”	30
“a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage”	1-3, 5-7, 9-13, 15
“at least one circuit”	1-3, 5-7, 9-13, 15, 21
“voltage monitor circuit”	5-6, 16-22, 24-27
“a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information”	10-11
“in response to the trigger signal, the logic element writes information into the non-volatile memory”	11
“wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit”	13
“at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts”	20, 29
“a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element”	22
“one or more registers [1160], the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage,”	23-30
“wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on”	23-30
“wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on, wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are	23-30

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Term	Relevant Claim(s)
configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals"	

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. Ibormeith IP, LLC v. Mercedes-Benz USA, LLC, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '918 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '918 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '918 patent Asserted Claims are indefinite in whole, in part or in combination:[14]

Term	Relevant Claim(s)
"converter circuit"	All asserted claims
"interface"	All asserted claims
"edge connections"	All asserted claims
"buck converter"	All asserted claims
"circuit [operable to]"	1-3, 5-7, 9-13, 15, 21
"voltage monitor circuit"	5-6, 16-22, 24-27

[14] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
"registers"	8, 14, 23-30
"non-volatile memory"	10-12, 15, 19, 22, 26
"controller"	12, 18-19, 25-26
"SDRAM devices"	20, 29
"voltage"	23-30
"at least one circuit"	1-3, 5-7, 9-13, 15, 21
"logic element"	10-11, 15, 22

D. U.S. Patent No. 11,232,054

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '054 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '054 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '054 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '054 patent Asserted Claims

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at the time the '054 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '054 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '054 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '054 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1: [15]

Term	Relevant Claim(s)
"regulated voltage(s)"	All asserted claims
"memory module"*	All asserted claims
"voltage conversion circuit"*	All asserted claims
"first circuit"*	1-13, 15
"a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages"*	1-13, 15
"a voltage conversion circuit coupled to the PCB"	1-13, 15-17, 23
"a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages"*	1-13, 15
"wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and wherein the plurality of SDRAM devices are coupled to the	1-13, 15

[15] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
first regulated voltage of the at least three regulated voltages"*	
"wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages"*	1-13, 15
"wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages"*	1-13, 15
"a plurality of synchronous dynamic random access memory (SDRAM) devices and a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages"*	1-13, 15
"voltage amplitude(s)" / "amplitude of the input voltage" / "amplitude change in the input voltage"	2-5, 6-7, 9-12, 16-17, 23-25, 29-30
"wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes"	2
"operable state"	4-7, 11-12, 16-17, 23, 25
"voltage monitor circuit"*	4-13, 16-17, 23-25, 29-30
"write operation" / "write operation to transfer data to non-volatile memory" / "write operation to transfer data into non-volatile memory"*	5-7, 23, 24-25, 29-30
"power threshold condition"	8-13
"power reduction condition"	13
"dual-buck converter"	15
"a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages"*	16-17, 23
"wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages; a plurality of	16-17, 23
components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages"*	
"the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, the plurality of SDRAM devices coupled to a first	16-17, 23

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Term	Relevant Claim(s)
regulated voltage of the plurality of regulated voltages"*	
"a voltage conversion circuit configured to provide a plurality of regulated voltages"*	24-25, 29-30
"the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages"*	24-25, 29-30
"wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages"*	24-25, 29-30
"a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices"*	24-25, 29-30
"wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage"*	24-25, 29-30
"wherein the one or more operations include a write operation to transfer data into non-volatile memory"*	24-25, 29-30
"the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal"	4-5
"controller"	5-13, 16-17, 23, 24-25, 29-30
"a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"	5
"the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal"	6-7
"a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"	7

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Term	Relevant Claim(s)
"the voltage monitor circuit transmits a signal to one or more portions of the controller"	8
"the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and wherein the first predetermined threshold voltage is above a specified operating voltage"	9-12
"the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage, wherein the second predetermined threshold voltage is below the specified operating voltage, and wherein the memory module transitions from a first operable state to a second operable state in response to the signal"	11-12
"the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage"	13
"the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages"	16-17, 23-24
"a controller coupled to the PCB, the controller including a voltage monitor circuit"	16-17, 23
"wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state"	16-17, 23
"wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"	23
"the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory"	24-25
"wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state"	25

*In addition, claims reciting these terms are invalid under 35 U.S.C. § 112, ¶ 1 because the entirety of the specification does not support the breadth of the claims as written. For example, and without limitation, the entirety of the specification clearly indicates that it is narrower than the claims reciting a "memory module" such that those claims are invalid for lack

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of written description. For example, the title of the '054 patent is "Flash-DRAM Hybrid Memory Module" but independent claims 1, 16, and 24 of the '054 patent do not require use of Flash or non- volatile memory.

2. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014). Several of the '054 patent Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite under § 112, ¶ 2, for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the '054 patent Asserted Claims are indefinite in whole, in part or in combination:[16]

Term	Relevant Claim(s)
"regulated voltage(s)"	All asserted claims
"voltage conversion circuit"	All asserted claims
"a voltage conversion circuit coupled to the PCB"	1-13, 15-17, 23
"first circuit"	1-13, 15
"voltage amplitude(s)" / "amplitude of the input voltage" / "amplitude change in the input voltage"	2-5, 6-7, 9-12, 16-17, 23-25, 29-30
"wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes"	2
"operable state"	4-7, 11-12, 16-17, 23, 25

[16] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
"controller"	5-13, 16-17, 23, 24-25, 29-30
"write operation" / "write operation to transfer data to non-volatile memory" / "write operation to transfer data into non-volatile memory"	5-7, 23, 24-25, 29-30
"power threshold condition"	8-13
"power reduction condition"	13
"dual-buck converter"	15
"wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages"	1-13, 15
"wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages"	1-13, 15
"voltage monitor circuit"	4-13, 16-17, 23-25, 29-30
"the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal"	4-5
"a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"	5
"the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal"	6-7
"a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"	7
"the voltage monitor circuit transmits a signal to one or more portions of the controller"	8
"the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and wherein the first predetermined threshold voltage is above a specified operating voltage"	9-12
"the voltage monitor circuit detecting an amplitude of the input	11-12

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Term	Relevant Claim(s)
voltage being below a second predetermined threshold voltage, wherein the second predetermined threshold voltage is below the specified operating voltage, and wherein the memory module transitions from a first operable state to a second operable state in response to the signal"	
"the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage"	13
"the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages"	16-17, 23-24
"a controller coupled to the PCB, the controller including a voltage monitor circuit"	16-17, 23
"wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state"	16-17, 23
"wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"	23
"the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory"	24-25
"wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state"	25

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '054 patent Asserted Claims are invalid under § 112, ¶ 6 because they

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contain means-plus-function terms and the '054 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '054 patent Asserted Claims are indefinite in whole, in part or in combination: [17]

Term	Relevant Claim(s)
"voltage conversion circuit"	All asserted claims
"interface"	All asserted claims
"buck converter"	All asserted claims
"edge connections"	1-13, 15
"first circuit"	1-13, 15
"voltage monitor circuit"	4-13, 16-17, 23-25, 29-30
"controller"	5, 7-13, 16-17, 23-25, 28-29

E. U.S. Patent No. 8,787,060

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '060 patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity

[17] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '060 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '060 patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '060 patent Asserted Claims at the time the '060 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '060 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '060 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '060 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1: [18]

Term	Relevant Claim(s)
"array die"	1-14, 16-21, 23-28
"in electrical communication with"	1-14, 16-21, 23-28

[18] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
“not in electrical communication with”	1-14, 16-21, 23-28
“die interconnect”	1-14, 16-21, 23-28
“control die”	1-14, 16-21, 23-28
“control/address signal”	1-14, 16-21, 23-28
“data ports”	1-10
“control circuit”	1-14, 16-19
“control signal”	1-10, 16, 18-21, 23-28
“data path control signal”	2, 3, 8, 18, 19, 27
“data conduit”	1-14, 16-19
“control respective states of the first data conduit and the second data conduit”	1-14, 16-19
“command/address signal”	4, 9
“selected in consideration of”	7
“to reduce a difference between a first load on the first data conduit and a second load on the second data conduit”	7
“chip select signal” / “chip-select signal”	11-14, 16-21, 23-28
“optimizing load”	20-21, 23-28
“selecting one of a first driver and a second driver”	20-21, 23-28
“selecting a [first / second] driver size for the [first / second] driver based, at least in part, on a load on the [first / second] driver”	21
“generate” / “generates” / “generated” / “generating”	3, 8, 16, 19, 23, 27
“a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and	1

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Term	Relevant Claim(s)
the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."	
"the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies"	1
"a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, at least a second data conduit between the second die interconnect and the first terminal, and chip select conduits for providing chip select signals to respective array dies; wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals"	11
"the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies"	11
"providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals"	20
"the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies"	20

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2. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." Nautilus, Inc. v. Biosig Instruments, Inc., 572 U.S. 898, 901 (2014). Several of the '060 patent Asserted Claims are

invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite under § 112, ¶ 2, for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the '060 patent Asserted Claims are indefinite in whole, in part or in combination: [19]

Term	Relevant Claim(s)
"array die"	1-14, 16-21, 23-28
"die interconnect"	1-14, 16-21, 23-28
"in electrical communication with"	1-14, 16-21, 23-28
"not in electrical communication with"	1-14, 16-21, 23-28
"control die"	1-14, 16-21, 23-28
"control/address signal"	1-14, 16-21, 23-28
"data ports"	1-10
"control circuit"	1-14, 16-19
"control signal"	1-10, 16, 18-21, 23-28
"data path control signal"	2, 3, 8, 18, 19, 27
"data conduit"	1-14, 16-19
"control respective states of the first data conduit and the second data conduit"	1-14, 16-19
"command/address signal"	4, 9

[19] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
"selected in consideration of"	7
"to reduce a difference between a first load on the first data conduit and a second load on the second data conduit"	7
"chip select signal" / "chip-select signal"	11-14, 16-21, 23-28
"optimizing load"	20-21, 23-28
"selecting one of a first driver and a second driver"	20-21, 23-28
"selecting a [first / second] driver size for the [first / second] driver based, at least in part, on a load on the [first / second] driver"	21
"generate" / "generates" / "generated" / "generating"	3, 8, 16, 19, 23, 27

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '060 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '060 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '060 patent Asserted Claims are indefinite in whole, in part or in combination: [20]

Term	Relevant Claim(s)
"array die"	1-14, 16-21, 23-28

[20] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
"die interconnect"	1-14, 16-21, 23-28
"control die"	1-14, 16-21, 23-28
"control/address signal"	1-14, 16-21, 23-28
"data ports"	1-10
"control circuit"	1-14, 16-19
"control signal"	1-10, 16, 18-21, 23-28
"data path control signal"	2, 3, 8, 18, 19, 27
"data conduit"	1-14, 16-19
"command/address signal"	4, 9
"chip select signal" / "chip-select signal"	11-14, 16-21, 23-28

F. U.S. Patent No. 9,318,160

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '160 patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '160 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

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1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The ’160 patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the ’160 patent Asserted Claims at the time the ’160 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id*. One of ordinary skill in the art would not have

understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the ’160 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the ’160 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the ’160 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[21]

Term	Relevant Claim(s)
“array die”	1, 2, 4, 5
“die interconnect”	1, 2, 4, 5
“in electrical communication with”	1, 2, 4, 5
“not in electrical communication with”	1, 2, 4, 5
“control die”	1, 2, 4, 5
“the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data	1, 2, 4, 5

[21] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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Term	Relevant Claim(s)
terminal to the first group of array dies"	
"the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die"	1, 2, 4, 5
"the second driver size being different from the first driver size"	1, 2, 4, 5
"the second die interconnects are longer than the first die interconnects"	2
"the second driver size is larger than the first driver size"	2
"the first driver size and the second driver size are related to a load on the first driver and a load on the second driver"	4
"control circuit"	5
"data conduit"	5
"control signal"	5
"a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size."	1
"the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies"	1

2. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014). Several of the '160 patent Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with

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reasonable certainty and are indefinite under § 112, ¶ 2, for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the '160 patent Asserted Claims are indefinite in whole, in part or in combination: [22]

Term	Relevant Claim(s)
"array die"	1, 2, 4, 5
"die interconnect"	1, 2, 4, 5
"in electrical communication with"	1, 2, 4, 5
"not in electrical communication with"	1, 2, 4, 5
"control die"	1, 2, 4, 5
"the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies"	1, 2, 4, 5
"the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die"	1, 2, 4, 5
"the second driver size being different from the first driver size"	1, 2, 4, 5
"the second die interconnects are longer than the first die interconnects"	2
"the second driver size is larger than the first driver size"	2
"the first driver size and the second driver size are related to a load on the first driver and a load on the second driver"	4
"control circuit"	5
"data conduit"	5
"control signal"	5

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must

[22] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '160 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '160 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '160 patent Asserted Claims are indefinite in whole, in part or in combination: [23]

Term	Relevant Claim(s)
"array die"	1, 2, 4, 5
"die interconnect"	1, 2, 4, 5
"control die"	1, 2, 4, 5
"control circuit"	5
"data conduit"	5
"control signal"	5

VII. Priority Dates

A. Priority Date for U.S. Patent Nos. 11,016,918 and 11,232,054

Plaintiff is not entitled to a priority date of at least June 1, 2007 for the '918 and '054 patents.

The claims of the '918 and '054 patents do not have support in any application filed before June 2, 2008. For example, in the '918 patent, the three "buck converter" and one "converter circuit" claim limitations (resulting in four regulated voltages) lack support in the earliest provisional, which just discloses a "step-down transformer 84." Furthermore, there is no

[23] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

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disclosure of a "dual buck converter" in the earliest provisional, and even the later applications fail to disclose a "dual buck converter" providing a first regulated voltage coupled to the SDRAM devices as required by several claims.

Similarly, in the '054 patent, the claimed "voltage conversion circuit" with "three buck converters" lacks support in the earliest provisional, which just discloses a "step-down transformer 84." Furthermore, there is no disclosure of a "dual buck converter" or a first or second "diode" in the earliest provisional as required by multiple claims.

The earliest provisional Plaintiff relies on for its alleged priority date spans 5 pages (19 paragraphs) with 3 figures:

06-01-2007	SPEC	Specification	PROSECUTION	5
06-01-2007	DRW	Drawings-only black and white line drawings	PROSECUTION	3

The '918 patent spans 75 pages (183 paragraphs) with 22 figures:

12-30-2020	DRW	Drawings-only black and white line drawings	PROSECUTION	22
12-30-2020	SPEC	Specification	PROSECUTION	75

The '054 patent, a continuation of the '918 patent, matches the '918 patent:

05-24-2021	SPEC	Specification	PROSECUTION	75
05-24-2021	CLM	Claims	PROSECUTION	1
05-24-2021	ABST	Abstract	PROSECUTION	1
05-24-2021	DRW	Drawings-only black and white line drawings	PROSECUTION	22

Defendants incorporate by reference its more fulsome analysis of the '918 and '054 patents' effective filing dates from Samsung's '918 patent IPR dated May 17, 2022 and Samsung's '054 patent IPR dated May 17, 2022. *See* IPR2022-00996, Paper 1 (Petition) at Section IV.A.; *see also* IPR2022-00999, Paper 1 (Petition) at Section IV.A.

Because the provisional application Plaintiff relies on for its alleged priority date for the

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Asserted Claims of the ’918 and ’054 patents lacks support for many claim limitations in the Asserted Claims, Plaintiff is not entitled to its alleged June 1, 2007 priority date.

B. Priority Date for U.S. Patent No. 10,949,339

Plaintiff is not entitled a priority date of at least July 16, 2009 for the ’339 patent.

The claims of the ’339 patent do not have support in any application filed before April 15, 2010. For example, the “byte-wise buffer,” “n/2 data transmission circuits,” “plurality of buffers,” and “n-bit wide data buffers” claim limitations lack support in the original application, which just discloses a “load-reducing circuit” and “load-reducing switching circuit.”

The earliest application Plaintiff relies on for its alleged priority date spans 15 pages with 5 figures:

07-16-2009	SPEC	Specification	PROSECUTION	15
07-16-2009	CLM	Claims	PROSECUTION	3
07-16-2009	ABST	Abstract	PROSECUTION	1
07-16-2009	DRW	Drawings-only black and white line drawings	PROSECUTION	5

The ’339 patent spans 27 pages with 13 figures:

03-27-2017	SPEC	Specification	PROSECUTION	27
03-27-2017	CLM	Claims	PROSECUTION	7
03-27-2017	ABST	Abstract	PROSECUTION	1
03-27-2017	DRW.NONBW	Drawings-other than black and white line drawings	PROSECUTION	13

Because the application Plaintiff relies on for its alleged priority date for the Asserted Claims of the ’339 patent lacks support for many claim limitations in the Asserted Claims, Plaintiff is not entitled to its alleged July 16, 2009 priority date.

C. Priority Date for U.S. Patent Nos. 8,787,060 and 9.318,160

Plaintiff is not entitled to a priority date of at least November 3, 2010 for the ’060 or ’160 patent.

The claims of the ’060 and ’160 patents do not have support in any application filed

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before November 3, 2011. For example, in the '060 patent, the claim limitations (1) "at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies" and (2) "selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies" lack support in the November 3, 2010 provisional.

Similarly, in the '160 patent, the limitation "first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies" lacks support in the November 3, 2010 provisional.

The earliest provisional Plaintiff relies on for its alleged priority date spans 4 pages (14 paragraphs) with 3 figures:

11-03-2010	SPEC	Specification	PROSECUTION	4
11-03-2010	DRW	Drawings-only black and white line drawings	PROSECUTION	3

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The ’060 patent spans 39 pages (113 paragraphs) with 8 figures:

11-03-2011	SPEC	Specification	PROSECUTION	39
11-03-2011	CLM	Claims	PROSECUTION	8
11-03-2011	ABST	Abstract	PROSECUTION	1
11-03-2011	DRW	Drawings-only black and white line drawings	PROSECUTION	8

The ’160 patent, a continuation of the ’060 patent, matches the ’060 patent:

07-21-2014	SPEC	Specification	PROSECUTION	37
07-21-2014	CLM	Claims	PROSECUTION	3
07-21-2014	ABST	Abstract	PROSECUTION	1
07-21-2014	DRW	Drawings-only black and white line drawings	PROSECUTION	8

Because the application Plaintiff relies on for its alleged priority date for the Asserted Claims of the ’060 and ’160 patents lacks support for many claim limitations in the Asserted Claims, Plaintiff is not entitled to its alleged November 3, 2010 priority date.

VIII. P.R. 3-4 Production In connection with these Invalidity Contentions,

Defendants also hereby provide the documents required by P.R. 3-4. *See* MICNL203-00000001 - MICNL203-00043740. Pursuant to P.R. 3-4(a) and the Protective Order, Defendants produce or are making available for inspections documents, source code, and other materials sufficient to show the operation of the Accused Products identified by Plaintiff in its P.R. 3-1(c) charts.

Pursuant to P.R. 3-4(b), Defendants also produce a copy of each item of prior art identified herein. These prior art references and corroborating evidence include those cited in attached invalidity claim charts in Appendices A-F. Defendants will also make available for inspection any prior art systems or devices upon request to the extent Defendants acquire such systems or devices. References that were cited during prosecution of the Asserted Patents may not be contained in Defendants’ production as they are not required to be under the local patent rules.

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Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art systems and devices is ongoing. Accordingly, Defendants reserve the right to supplement their production as Defendants obtain additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

Dated: November 21, 2022

Respectfully submitted,

By: */s/ Michael R. Rueckheim*

Thomas M. Melsheimer
State Bar No. 13922550
TMelsheimer@winston.com
Natalie Arbaugh
State Bar No. 24033378
NArbaugh@winston.com
WINSTON & STRAWN LLP
2121 N. Pearl Street, Suite 900
Dallas, TX 75201
Telephone: (214) 453-6500
Facsimile: (214) 453-6400

Michael R. Rueckheim
State Bar No. 24081129
MRueckheim@winston.com
WINSTON & STRAWN LLP
255 Shoreline Drive, Suite 520
Redwood City, CA 94065
Telephone: (650) 858-6500
Facsimile: (650) 858-6559

David Enzminger
Pro Hac Vice
DEnzminger@winston.com
WINSTON & STRAWN LLP
333 S. Grand Avenue
Los Angeles, CA 90071-1543
Telephone: (213) 615-1700
Facsimile: (213) 615-1750

Matthew Hopkins
Pro Hac Vice
State Bar No. 1500598
MHopkins@winston.com

Netlist EX2005
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WINSTON & STRAWN LLP
1901 L Street, N.W.
Washington, D.C. 20036-3506
Telephone: (202) 282-5000
Facsimile: (202) 282-5100

Juan C. Yaquian
State Bar No. 24110559
Pro Hac Vice
JYaquian@winston.com
WINSTON & STRAWN LLP
800 Capital Street, Suite 2400
Houston, TX 77002-2925
Telephone: (713) 651-2600
Facsimile: (713) 651-2700

Attorneys for Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC

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CERTIFICATE OF SERVICE

I hereby certify that, on November 21, 2022, a copy of the foregoing and Exhibits A-F attached thereto were served to all counsel of record.

By: */s/ Michael R. Rueckheim*
Michael R. Rueckheim

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