UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

No. IPR2023-00847

vs.

NETLIST, INC.,

Patent Owner.

_____/

DEPOSITION OF ROBERT G. WEDIG, PH.D.

Remote Zoom Proceeding

Sunnyvale, California

Tuesday, March 12, 2024

REPORTED BY:

LESLIE ROCKWOOD ROSAS, RPR, CSR 3462

Pages 1 - 155 Job No. 6584925

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Deposition of ROBERT G. WEDIG, PH.D., taken on behalf of Patent Owner, Remote Zoom Proceeding from Sunnyvale, California, beginning at 9:09 a.m. Pacific Daylight Time and ending at 4:22 p.m. Pacific Daylight Time, on Tuesday, March 12, 2024, before Leslie Rockwood Rosas, RPR, CSR No. 3462.

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I N D E X

TUESDAY, MARCH 12, 2024

WITNESS	EXAMINATION
ROBERT G. WEDIG, PH.D.	
BY MR. LINDSAY	7, 140
BY MR. CHANDLER	111

QUESTIONS WITNESS INSTRUCTED NOT TO ANSWER:

Page	Line
140	23

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DEPOSITION EXHIBITS

ROBERT G. WEDIG, PH.D.

NUMBER	DESCRIPTION	IDENTIFIED
Exhibit 1001	Patent No.: US 10,268,608 B2	6
Exhibit 1003	Declaration of Dr. Robert Wedig Regarding U.S. Patent Number 10,268,608	6
Exhibit 1005	United States Patent Application Publication, US 2010/0312956 A1	6
Exhibit 1006	Patent No.: US 8,020,022 B2	6
Exhibit 1029	US Patent Application, Pub. No.: US 2007/0008791 A1	6
Exhibit 1069	S4 and S5 in Hiraishi.pdf	110
Exhibit 1070	S4 read leveling in Hiraishi.pdf	110
Exhibit 1071	S4 write leveling in Hiraishi.pdf	111

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9:09 A.M.

PROCEEDINGS

ROBERT G. WEDIG, PH.D.,

called as a witness, having been duly sworn, was examined and testified as follows:

(Exhibit 1001, Patent No.: US 10,268,608 B2, marked for identification electronically by counsel.)

(Exhibit 1003, Declaration of Dr. Robert Wedig Regarding U.S. Patent Number 10,268,608, marked for identification electronically by counsel.)

(Exhibit 1005, United States Patent Application Publication, US 2010/0312956 A1, marked for identification electronically by counsel.)

(Exhibit 1006, Patent No.: US 8,020,022 B2, marked for identification electronically by counsel.)

(Exhibit 1029, US Patent Application, Pub. No.: US 2007/0008791 A1, marked for identification electronically by counsel.)

THE REPORTER: You may proceed, Counsel, and introduce yourselves. 09:09:21

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MR. LINDSAY: This is Jonathan Lindsay for Patent Owner Netlist, Inc., with Irell & Manella.

MR. CHANDLER: Good morning. This is Ted Chandler from Baker Botts on behalf of the petitioner, Samsung Electronics Co., Limited, and with me is my colleague, Dr. Ferenc Pazmandi.

THE REPORTER: Thank you.

You may proceed, Counsel.

EXAMINATION

BY MR. LINDSAY:

Q. Thank you for coming today, Dr. Wedig. This is a deposition for IPR2023-00847, challenging the claims of US Patent Number 10,268,603 -- I'm sorry -- 608.

And I may refer to that patent as just the '608 patent. Is that okay? Would you understand which patent I'm referring to?

A. Yes, I would.

Q. Okay. And for the IPR proceeding, you know, since there are several between the parties, instead of reading the number, is it okay if I refer to "this proceeding" or "this IPR" and you'll know I mean the one in which the '608 patent is being challenged?

A. Yes. So you'll refer to that as the '847 IPR?

Q. Yes. We can refer to it as the '847 IPR, but I

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may get lazy as the day goes on and just say "this IPR" or "this proceeding," and you'll know I mean the '847 IPR; is that okay?

A. Yes, that's fine.

Q. Okay. And I know you know all of the -- all the ground rules, but for this record, I'd like to go over them, if that's okay. 09:11:01

A. That's fine.

Hang on a second. I've got -- I'm going to shut the window here, because the light is just shining in. One second. 09:11:17

Q. Sure. Okay.

A. Okay.

Q. So you understand you've taken an oath to tell the truth here today, Dr. Wedig; is that right? 09:11:34

A. Yes, I know that.

Q. And you understand that this oath is of the same force and effect as if it were given in a court of law before a judge and a jury?

A. Yes, I understand that. 09:11:45

Q. And you understand that you could be subject to penalty of perjury for providing false or misleading statements during -- during your testimony today?

A. Yes, I understand.

Q. Is there anything preventing you from giving 09:12:00

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full and accurate answers today, Dr. Wedig?

A. No, there's not.

Q. If you need me to clarify a question, you know, please do so. However, if you don't ask me to clarify a question, I'll assume you understood the question; is that fair? 09:12:16

A. That's fair.

Q. And even during our breaks today, you understand that you're still under oath; is that right?

A. I understand. 09:12:27

Q. And during those breaks, you understand that your counsel cannot discuss with you the subject matter of your testimony, frankly, with anyone else as well. Is that your understanding?

A. I understand. 09:12:45

Q. And you understand your counsel can't instruct you not to answer a question unless it's necessary to preserve the attorney-client privilege or another related privilege?

A. I understand. 09:13:00

Q. Dr. Wedig, what did you do to prepare for this deposition?

A. I reviewed my declaration, I reviewed the prior art that I referred to in my declaration, and I had some conversations with Samsung counsel. 09:13:29

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Q. Who -- who did you meet with at Samsung?

A. Ted Chandler and Ferenc Pazmandi.

Q. I see.

Anyone else?

A. No. 09:13:52

Q. And about how long did you meet with -- with counsel?

A. We had a total of three meetings. Each meeting went for about one and a half to two hours.

Q. I'm sorry, how long? 09:14:12

A. Three meetings. Each one was one and a half to two hours.

Q. Okay. Do you have any documents with you today, physical documents in front of you?

A. Yes. I do have a paper copy (indicating) of my declaration, and I also -- I do still have -- just for convenience, I've got some paper copies (indicating) of exhibits. Just to be clear, these are paper copies that were originally printed for the '506 patent, and so the exhibit numbers may be different, but they're useful for being able to just see things on paper if I need to. Okay. That's the only two documents that I have here. 09:14:27 09:14:52

Q. Sure.

So with respect to that binder with the '506 documents, would you mind just identifying for the record 09:15:10

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kind of each document and exhibit number that's in the -- in the binder?

A. Okay. So the first -- okay. Exhibit 1001 is the '506 patent. I next have Exhibit 1004, which is my CV. 1005 is the Hiraishi patent. 1006 is the Tokuhiro patent. 1007 is the Ellsberry patent. 1008 is the Kim patent. 1018 is the design specification for the PC 2100 and PC 1600 DRR SDRAM registered DIMM. Exhibit 1020 is the JEDEC Standard JSD79-3C. And Exhibit 1029 is the Butt patent. B-U-T-T, Butt patent. Those are all the documents that I have in paper form. 09:15:43 09:16:54

Q. Thank you. That's helpful.

I did not hear you list Exhibit 1003 from the '506 IPR, which was your declaration in that case. Do you have a physical copy of that document in the binder, or is that not part of it? 09:17:30

A. No. That's not in this binder. That's not -- no.

Q. Okay.

A. I may have it separately somewhere, but I -- I wasn't referring to that. 09:17:41

Q. Okay. And in preparation for the deposition today, you reviewed, to varying degrees I'm sure, the documents that you just listed on the record; is that correct? 09:18:02

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A. That's correct.

Q. Did you also review your declaration from the '506 IPR?

A. No. I don't -- I don't recall -- I don't believe I did. I can't recall that I did so. 09:18:21

Q. Okay. For your declaration, 1003, which was introduced here to Exhibit Share for this IPR, would you mind opening that up?

A. Okay.

Q. And if you could take a look at paragraph 67 when you have that open. 09:18:53

A. Okay.

MR. CHANDLER: This is page 31?

MR. LINDSAY: Yes, yes.

THE WITNESS: Just for my future reference, is there a search capability? No. Oh, yeah, I guess there is. 09:19:37

Q. BY MR. LINDSAY: There should be.

A. Okay. Uh-huh. All right.

Okay. So I am at paragraph -- I'm sorry, you said 67? 09:19:47

Q. Yes.

A. I'm here, yes.

Q. Okay. In this paragraph, you're referencing the declaration that you submitted in the '506 IPR; is 09:19:59

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that -- is that correct?

A. Yes, that's what I see here. Yes.

Q. Okay. And -- and how is the '506 patent related to the '608 patent, if you remember?

A. My best understanding is that the '608 patent is in the lineage of patents that was originally filed with a singular specification, and '506 drew from that specification to have some claims, and then the '608 patent drew from the same specification to have other claims. And the exact order of which ones came first, which one came second, I'd have to look that up. 09:20:23 09:21:02

Q. That's fair enough.

So the references -- the prior art references that you opined on in the '506 IPR, those are the same references that you're opining on here with respect to the '608 IPR; is that correct? 09:21:25

A. Generally, yes. I mean, there may be a few more, a few less. I didn't do a correlation between all of the '506 references versus '608 references, but for the main references at least, yes, that's correct. 09:21:51

Q. Sure. And so by "the main references," would that include Hiraishi, Butt and Tokuhiro?

A. Yes. And, I mean, to a certain extent Ellsberry also.

Q. Understood. 09:22:09

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Is the declaration that you submitted in the '506 IPR accurate?

A. As I said, to the best of my memory. I haven't looked at it -- I haven't really reviewed it since last year. 09:22:28

Q. Do you know if any of your opinions with respect to those references that are in common are different in the '506 IPR than they are in the '608 IPR?

MR. CHANDLER: Objection. Form.

THE WITNESS: I haven't reviewed for that, so I can't -- I can't say yes or no. I mean, '608 is a different patent, so I -- like I said, I have not tried to do a comparison. 09:22:51

Q. BY MR. LINDSAY: Right. I'm just asking you about the prior art references, the same Hiraishi, Butt, Tokuhiro. 09:23:09

A. Uh-huh.

Q. Have your opinions changed between the two IPRs is all I'm asking, about those specific references?

MR. CHANDLER: Objection. Form. 09:23:22

THE WITNESS: So I guess I want some clarifications. My opinions? I believe that they're still relevant -- they're still relevant art. That opinion is the same. I mean, is that what you're asking?

Q. BY MR. LINDSAY: So about what they generally 09:23:40

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teach, what they disclose, the way the systems work, things of that nature. Have your opinions changed?

A. Oh --

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah. I would say that my understanding of those -- of those pieces of art are the same, in that I believe when I understood them last year when we worked on '506, that my understanding of how that art works has not changed. So I have the same -- same understanding of the technology that's being taught by those references as I did when I reviewed -- reviewed them for the '506 patent. 09:23:54 09:24:21

Q. BY MR. LINDSAY: And if we could move down to paragraph 68, just below what we were just looking at there. 09:24:42

A. Uh-huh.

Q. So here you're summarizing what the Board found in the '506 IPR, and in the second sentence, which begins at the bottom of page 32 about three lines up, it says, "In doing so, the Board credited my testimony in that proceeding." 09:25:04

Do you see that part?

A. Yes, I see that.

Q. So you're standing by your testimony from the '506 IPR. Is that a fair statement? 09:25:16

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A. Well, I absolutely stand by what I said in relation to the '506 patent. I haven't -- I haven't changed my opinion as to whether the '506 patent is made obvious by those -- by those references. So yes, I stand by that. 09:25:52

Q. Sure.

And do you also stand by your testimony about the prior art references that are in common between the '506 and the '608 IPRs?

MR. CHANDLER: Objection. Form. 09:26:08

THE WITNESS: I thought I answered that, that I still understand those references, and I believe that I have the same understanding of those reference as I did when I worked on the '506 patent.

Q. BY MR. LINDSAY: Okay. No, that's fair enough. 09:26:30

I want to take a look at the Hiraishi reference, so you should have that available, Exhibit 1005. Let me know when you have that.

A. Okay.

Okay. I have that on the screen. 09:26:52

Q. Is it your position that Hiraishi discloses a delay circuit that reads on the delay circuit that's claimed in the '608 patent?

A. Yes, it does.

Q. And what is the delay circuit that's disclosed 09:27:21

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in Hiraishi that reads on the delay circuit that's claimed in the '608 patent?

A. Okay. I'd like to refer to my -- to my declaration to make sure that I identify all the different parts of it, if I could. 09:27:38

Q. Sure. Sure. And I can probably direct your attention. If you want to take a look at paragraph 166, although of course feel free to -- to review it as -- as you need to.

A. Okay. One moment, please. 09:28:14

Okay. So this particular paragraph that you directed me to points to the delay circuit for read operations, and as I said in paragraph 166, it includes the read FIFO, the delay circuit 372, the strobe generating circuit 376, and the DLL circuit 310. Okay. 09:29:17 So that -- that is what I see for the delay circuit for read operation.

There is additional circuitry for delay circuit for write operations.

Q. Before we get there, can I ask you a question 09:29:52 about the delay circuit for read operations?

A. Sure.

Q. Okay. So I'm trying to understand, so is the delay circuit that reads on Claim 1's delay circuit in your opinion, is that the combination of the components 09:30:14

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that you list here?

A. Well, I believe that all of those different parts make up the delay circuit, so I guess yes, it's a combination of those. I mean, they all work together to implement the delay circuit. 09:30:33

Q. Okay. I think I understand. And I apologize. You were going to go ahead and look at the delay circuit for write operations, so I'll let you continue.

A. Okay. Let me find that.

Q. That may be paragraph 152. It's not structured the same way, but it appears to be consistent with what we've been talking about. 09:31:17

A. Okay. Okay. It includes at least the FIFO write -- the FIFO write circuit 301, and then other parts were for the read circuit, I mean, I already identified. 09:32:16

Q. So maybe this is generic as to read and write operation is --

A. Some of the logic -- some of the logic is used for both read and write, and so I'm not sure if I already said, but I will say again, that in addition to the FIFO write circuit 301, it's made up of the FIFO read circuit 302, the delay circuits 370 and 372, and the strobe generating circuits 374 and 376. 09:32:42

So let me see if I have everything else.

Okay. I describe a little more clearly, I 09:33:50

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think -- or to address your question better, on page 123, that the delay circuit for write operations includes the FIFO write circuit 301 and performs -- it performs the operation that it does with the delayed CLK LCLKW. And that's generated by the DLL circuit, which I believe I already -- DLL circuit 310 that I already referenced. And as I said, strobe generating circuit 370 and 374. 09:34:20

And I don't believe I said before, but just to include it, I believe that the -- in the -- in the -- the delay circuit for read operations should also include the LCLKR. 09:34:48

And so I think I've covered everything now.

Q. Okay. Let me see if maybe I can unpack that a little bit. Let's go -- what paragraph are we at here? 161. Okay. We'll come back to it. 09:35:14

So in the delay circuit for read operations, you identify the FIFO read circuit 302, delay circuit 372, strobe generating circuit 376 and the DLL circuit 310 as being in combination the delay circuit; is that -- is that correct? 09:35:51

A. Well, I'm sorry. I don't have the privilege of seeing live feed. So I'm not sure that you said everything. If you give me one moment -- okay. If you could just say those individual items again, I now have the -- I now have a list in front of me. 09:36:15

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Q. Oh, okay. I was just trying to read from your paragraph 166.

A. Okay. I'm now -- I'm now with you on paragraph 166, so if you could say it again so that I can -- so that I can agree or not agree with you. 09:36:27

Q. Okay. And I know you answered this earlier, but then there was one thing you said at the end about the CLK. I just wanted to make sure I understood your position on that, but the first part will be repetitive.

So is it your opinion that the delay circuit 09:36:42 that Hiraishi discloses that reads on the claims of the '608 patent includes the FIFO read circuit 302, the delay circuit 372, the strobe generating circuit 376 and then the DLL circuit 310?

A. As part of it, yes. And then additionally it 09:37:09 has the LCLKR signal.

Q. Okay. So that's what I wanted to -- thank you. That's what I wanted to kind of drill down on for a moment.

So I'm trying to understand if we're reading on 09:37:23 a circuit how a CLK signal is part of the circuit, as opposed to the DLL circuit, you know, itself.

A. Well, the LCLKR -- the LCLKR signal participates in the operations that are involved in the delay, so it's necessary in order to -- in order to perform the 09:37:59

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operation of the delay.

Q. So -- right. So the delay circuit is generating -- is receiving signals and generating signals, and I guess what I'm just trying to get at is, is it -- when we're talking about the element delay circuit, not what it does, but what it comprises -- 09:38:24

A. Uh-huh.

Q. -- it includes -- and I know there's other things.

It includes the DLL circuit 310. I understand that. That makes sense. But you also said it includes the local CLKR signal, and so I'm just trying to understand is it -- is it the case that the circuit includes the signal or the circuit generates the signal? 09:38:32

A. Well, it generates -- it generates the signal in order to use it, so it does both. The circuit -- the signal is created as part of the delay circuit to be used in order to perform the delay, so it both creates it and uses it. 09:38:54

Q. Yeah, I think we're saying the same thing. I was just thinking from a structural perspective; right? So the claims have certain structural elements. 09:39:15

A. Right.

Q. And I was trying to understand if you meant that the signal was a structural element that made up the 09:39:28

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delay circuit, which I don't think so -- correct me if I'm wrong -- or if it's -- the local CLK signal is -- is used -- is generated and used by the delay circuit. I think that's what you're saying; is that correct?

A. Well, no. I think it's structural. Because -- 09:39:47

I mean, my interpretation is it's structural, because if you look at the other elements that I referred to as part of the delay circuit, and I'll just use an example, the DLL circuit and the strobe generating circuit 376, those are both in the delay circuit and the LCLKR provides 09:40:15 information from the DLL circuit to the strobe generating circuit.

So the LCLKR, it is my understanding, is part of the structure of that delay circuit, because it is necessary to perform the delay specifically in 09:40:37 communicating between the DLL circuit and the strobe generating circuit. And, I mean, that was the example. In addition, it also communicates with the FIFO read circuit.

Q. Okay. So on the strobe generating circuit 372, 09:41:08 is the strobe signal that's generated by the strobe generating circuit 372 also part of the structural composition of the -- of Hiraishi's delay circuit?

A. Yes. I think so. Yes, it is.

Q. Okay. And for the delay circuit 372, that 09:41:48

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delays an input strobe signal; right?

A. Yes, it does.

Q. Is either the input strobe signal or the delayed output strobe signal from circuit 372, is that part of the structural composition of Hiraishi's delay circuit? 09:42:19

A. I want to make sure I understand your question. Your question was: Is the input to the delay circuit and is the output to the delay circuit part of the structure of the delay circuit?

Q. Well, it was really a "or," but, I mean, we could take them individually. 09:42:37

A. Well, I think the delay circuit 372 of Hiraishi is part of the delay circuit referenced in Claim 1 of the '608 patent, and that is comprised of an input and an output, so since the delay circuit 372 is part of the delay circuit in Claim 1 of the '608 patent, then necessarily the input to that and the output of that would also be part of the delay circuit. 09:43:06

Q. So when you say input and output, is that -- are you referring to a physical, you know, contact on the component or are you referring to the signal that's on the -- the lead into that component? 09:43:37

A. I'm referring to the signal that drives the delay circuit 372. I mean, it's not a contact, because this -- you know, this delay circuit 372 is deep inside 09:44:10

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of a component that, you know, provides buffering -- provides buffering for -- you know, for memory -- for memory chips. So it's actually the -- you know, it's the wire that -- or the actual -- yeah, it's the input -- the actual wire that goes into the delay circuit and comes out of the delay circuit. I mean, it starts at -- it starts at where it enters the delay circuit and it goes on from there. 09:44:49

Q. Okay. So when you -- okay. So are you using the term "wire" to refer to the signal line that physically goes into delay circuit -- since we're talking about this component, delay circuit 372, or are you talking about the electrical wave that's on that wire that's being input to delay circuit 372? 09:45:08

A. Oh, okay. I see where you're going. I understand. Yeah, because you're talking about structure. You're talking about something physical; right? 09:45:35

So, yeah, no, I'm referring to, you know, when I say "wire," that's a broad term. I mean the trace, the -- whatever it is that conducts electricity into the delay circuit. 09:45:51

Q. Okay.

A. As I said, starting at the delay circuit and going on from there. 09:46:12

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Q. I understand.

So -- so you're including the wires that are connecting these individual components as part of the overall delay circuit?

A. Yes, I am. They're necessary. They're necessary in order to affect the operation of the delay circuit. 09:46:29

Q. Right, no. I follow you now. Earlier I had understood you to be referring to the signals that were going into, again, the electrical wave forms that were going into the components as being part of the structure, and that's why I was asking so many questions about that. 09:46:44

A. I understand. Yeah. Thank you.

Q. But that's not the case, you're not referring to this -- the electrical signals as structure, you're referring to the traces or wires connecting the component as part of the structure. Is that -- just so we're on the same page, is that accurate? 09:47:01

A. Yes. I mean, there's the structure and there's the function. So, you know, we're talking about structure now. I tried to point out all the structure. Of course, it does the function of performing a delay, and that would be in other parts of the -- of the claim in order to explain its operation. And so using this -- using this structure that I identified, I believe it 09:47:22 09:47:41

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performs the function that is being called for in the claim.

Q. Okay. Thank you.

So we also talked about the delay circuit for write operations. And just so the record's clear, is it your opinion that Hiraishi discloses corresponding components to what you have here for write operations? So there is a strobe generating circuit for write operations. It has a different number. I think it's 374. There's a delay circuit for write operations. I think it's 370. 09:47:58 09:48:31

But it's the same corollary to the components that you have listed here. Is that -- is that fair? Is that accurate?

MR. CHANDLER: Objection. Form. 09:48:45

THE WITNESS: Generally, that's correct. I mean, you didn't -- you didn't list every item, but, yeah, it's the -- it's similar components.

Q. BY MR. LINDSAY: So Mr. Chandler's right. That was not a good question. 09:49:01

Would you read the components that comprise the delay circuit for write operations for the record?

A. Okay. And I'm referring, for your benefit, to the middle of page 123 of my declaration.

It's -- the delay circuit for write operations 09:49:22

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is comprised of the FIFO write circuit 301 and the LCLKW. Let's see here. The strobe generating circuit 370 and 374. Those are the -- those are the main components.

Q. Okay. And when you say the LCLKW --

A. Uh-huh. 09:50:03

Q. -- are you referring to the DLL circuit 310?

A. Oh. Well, that would also be part of the -- of the write -- the write circuit, but, no, that's not what I was referring to. I mean, the L -- the DLL circuit 310 generates the LCLKW signal -- signal. Yeah, it generates 09:50:28 that signal. And so the -- so the DLL circuit is connected to -- provides -- provides the value for the LCLKW.

Q. Okay. So let's go back to paragraph 152 for a moment. 09:50:58

A. Okay.

Okay. I'm there.

Q. Okay. So for the limitation in Claim 1 of a command processing circuit, do you see that? You listed the data register control circuit 320 and logic in DLL 09:51:30 circuit 310.

A. Yes.

Q. So the way I read this, is it the case that you are relying on the DLL circuit 310 to be part of the command processing circuit as well as part of the delay 09:52:02

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circuit of Claim 1?

A. Well, yeah. It's needed for both purposes. The command processing circuit -- the command processing circuit produces the command to delay, and then that is sent to the DLL circuit, and so that part that is 09:52:31 interpreting the command, performing the command, is partially in the DLL circuit, and then the DLL circuit performs -- initiates the delay, and so it's also part of the delay circuit. Yeah, so it actually performs double duty. 09:52:59

Q. So is your opinion that the recited delay circuit and command processing circuit can be satisfied by the same circuitry?

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, no, I didn't say that. 09:53:24 That's not my intention.

Q. BY MR. LINDSAY: What do you mean then?

A. What I mean is that there is logic that performs command processing in the command processing circuit, which are identified as being comprised of the data 09:53:48 register control circuit 320, and that does -- that does command processing. But it also extends out to the DLL circuit, because that command needs to be interpreted by the DLL circuit and then it needs to affect the delay, and so it needs to interpret the command, and then at 09:54:18

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that point it -- once it's interpreted, it begins to perform the delay.

So my understanding is that there is components in the DLL circuit that begins to perform the delay, and then there are other components beyond the DLL circuit that are also involved in performing the delay. So I'm saying there is an overlap, but I never intended to say that the command processing circuit and the delay circuit are made up of the same circuitry. 09:54:41

Q. Right. Thank you. 09:55:04

So if these -- if the delay circuit and the command processing circuit were -- you know, think of a Venn diagram.

A. Uh-huh.

Q. Are you saying it would be -- there would be some overlap between the two, but they would otherwise not be a perfect overlap? Is that -- is that what you're saying? 09:55:20

A. That's partially correct. I mean, let me -- since you're -- since you want to drill down into this, let me try and make sure I'm absolutely clear. 09:55:40

The DLL circuit that is shown in Figure 5 is a box. There's additional information in the Hiraishi patent that describes the different aspects of that DLL circuit, and so in the description where it says that it 09:56:08

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receives information from the data register control circuit 320, to the extent that that circuitry does command interpretation, that would be part of the command circuit.

And then there's additional description in the Hiraishi patent that talks about how the DLL circuit performs a delay. To extent that DLL circuit performs a delay, that would be in the delay circuit. Okay? 09:56:34

So the -- the DLL circuit 310 is described, to a certain extent in showing Figure 5, it is through further explanation in the Hiraishi patent that helps to understand in more detail what the DLL circuit is doing and how it's comprised of both a command -- a portion that interprets the command and a portion that actually performs the delay. 09:57:12 09:57:33

Q. Okay. That's helpful. Thank you.

So in paragraph 152, same paragraph, Claim 1 also recites "at least one tristate buffer." Do you see that about the fourth line down?

A. Yes, I see that. 09:58:03

Q. And -- and for that limitation, you've identified the output buffers OUTB and input buffers INB as disclosed in Hiraishi; is that correct?

A. That's correct.

Q. So is your opinion that Hiraishi's output 09:58:29

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buffers and input buffers are each a tristate buffer?

A. Yes. The buffers that I identified, yes.

Q. Right. And -- and in Figure 5 of Hiraishi, and we can look at that just so we're clear, those are the triangles, right, along the right side that are labeled INB and OUTB, and then on the left side the triangles that are again labeled OUTB and INB; is that right? 09:59:05

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes. I mean, I agree with what you're saying, assuming that we are both looking at the same set of triangles, but I believe -- I think we're on the same page. 09:59:34

Q. BY MR. LINDSAY: Yeah, this is one of those areas that would be more effective in person.

A. True. 09:59:55

Q. But they're the only triangles that have the INB/OUTB leads to them, although not every one of them has that label, but like you said, I think we're on the same page.

So your -- is it your opinion that those are tristate buffers then? 10:00:09

A. Yes. That's my understanding, yes.

Q. And so those tristate buffers, those OUTB and INB buffers, are those part of the delay circuit as well?

A. No, they're not. 10:00:33

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Q. And what, if any, claim constructions did you apply in your declaration?

A. Well, let me see here. I have a section in the early part of my declaration on claim construction. Let me see if I can find that. 10:01:22

Okay. So I gave -- in doing this analysis, I gave all the claim terms there ordinary and custom -- ordinary and customary meaning as understood by one of ordinary skill in the art. However, I do understand that in some other IPR proceedings, there have been some claim 10:02:17 interpretations or claim constructions given, and so I listed those.

And -- but I -- I tried to explain that these terms were used in other IPRs and that, you know, you could -- you know, you should consider them at least when 10:02:55 making a claim interpretation.

Q. I didn't want to interrupt you, but I'm not sure where you're -- you said you listed some. What paragraph are we --

A. I'm looking at -- starting on page 34 of my 10:03:08 declaration.

Q. Okay.

A. So that area covers my understanding of claim construction.

Q. Okay. So that would be under the section -- 10:03:36

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subsection F, Construction of Terms Used in the Patent Claims, then, that you were referring to?

A. That's correct.

Q. In the first sentence, I see that you've identified your understanding that claim terms should be given their ordinary and customary meaning as understood by one of ordinary skill in the art in view of the patent and its file history. 10:03:56

A. Yes, that's correct.

Q. So did you consider the disclosure of the '608 patent in coming to an understanding as to what each of the claim terms means? 10:04:19

A. Yes, I did.

Q. And did you review the file history to understand what the claim terms mean as well? 10:04:45

A. Yes, I did.

Q. Do you recall seeing anything in the patent or the file history which was unusual or deviated from what you understood would be the ordinary and customary meaning of terms that were used in the claims? 10:05:09

MR. CHANDLER: Objection. Form.

THE WITNESS: Nothing was out of the ordinary.

Q. BY MR. LINDSAY: So obviously there's a lot of terms in the patent, a lot of words, but just focusing on the claim terms, did you see any usage of claim terms in 10:05:34

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the patent that would suggest a meaning different than the ordinary and customary meaning to a person skilled in the art?

A. Claim terms? Well, I think that there's some -- there is some dispute, and so I think there is some maybe misunderstanding of at least one of the claim terms as to how it should be interpreted. 10:06:18

Q. Right. No, I understand. So setting aside specific -- the way one party might be reading a claim term versus another party reading a claim term, I'm just asking in terms of your reading of the specification of the '608 patent, its description -- 10:06:51

A. Uh-huh.

Q. -- is there anything in there that -- I just want to make sure I get the paragraph back up here. 10:07:08

Sorry.

Was there anything in there that suggested the claim terms should not be given their ordinary and customary meaning as understood by a person skilled in the art, understanding that there's a dispute about what that ordinary and customary meaning might be? 10:07:37

A. Let me try and answer it this way and see if this satisfies what you're -- what you're trying to ask.

I believe that I have an understanding of the ordinary and customary meaning of the individual claim 10:07:55

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terms, and I don't believe that they deviate from what one of ordinary skill in the art would interpret those terms to mean. I don't believe that they have any special meaning that is caused by some specific wording in the specification or the file history. I believe that they are all the normal terms that one of ordinary skill in the art would use. 10:08:25

Q. Okay. That's fair.

Okay. Take a look at paragraph 89 in your declaration. 10:09:18

A. Okay.

Okay. I see it.

Q. Towards the bottom of the page there's a sentence that starts, "Indeed, although institution of the IPR to the related '632 patent." 10:09:37

Do you see that?

A. I see that.

Q. Okay. And then you reference a -- another patent publication, which I'll pronounce as "Saito" or "Saito," which I'm sure is incorrect. 10:09:57

But do you see that?

A. I see that.

Q. Is the Saito reference, is that the -- is that the same as the Hiraishi reference?

MR. CHANDLER: Objection. Form. 10:10:19

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THE WITNESS: My understanding is that it is the same specification, obviously different claims, but my understanding is it's the same -- it uses the same specification.

Q. BY MR. LINDSAY: Okay. And then -- so, yeah, let's take a look down at paragraph 170, then, if we could. It also discusses Saito. 10:10:47

A. Paragraph 170 of my declaration?

Q. Yes.

A. I see it. 10:11:21

Q. Okay. And you say in the second sentence there, so -- that, "Saito discloses a delay circuit, including a read and write FIFO, strobe delay and strobe generation circuits and the DLL circuit."

Do you see that part? 10:11:45

A. I see that.

Q. So that's consistent with what you're just saying, that they have the same specification, so naturally Saito, just like Hiraishi, would also disclose a delay circuit in the form of those components? 10:12:02

A. Yes. It has the same specification, so it would describe it the same way.

Q. And then taking -- going down further, if we could, to paragraph 255.

A. Okay. 10:12:35

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Q. So in this paragraph you cite to the Board's decision in the '632 IPR; is that -- is that correct?

A. Let me -- let me get up to speed here.

Okay. I'm sorry. What was the question?

Q. So I was just setting our -- our baseline, which is what this is -- what this paragraph in part is doing, which is citing to the decision from the -- from the Patent Board in the '632 IPR. 10:14:13

A. Okay.

Q. Is that -- is that your understanding of what you're citing here? 10:14:43

A. Yes, I am citing the '632 IPR decision.

Q. And that's Exhibit 1014?

A. That's my understanding. Unless I made a mistake, I believe that is the correct exhibit number. 10:15:09

Q. Okay. And we can look at that if you'd like, too, but I was just going to ask you about the statement that's in the declaration itself.

A. Okay.

Q. So the cited sentence from the decision is: "Saito describes using the determined time interval only to adjust the timing of an input buffer of memory controller 12, not to adjust the timing of output by data register buffer 300." 10:15:20

Do you see that? 10:15:43

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A. I see that.

Q. That's the Board's statement from the decision?

A. Yes, that's correct.

Q. Do you agree with the Board's statement there?

A. No, I do not. 10:16:01

Q. Why did you cite to it then?

A. Well, it -- it talks about how -- what I'm talking about is how Hiraishi has the problem that it does not provide the data back to the memory controller, such that it's all provided at the exact same time. And 10:16:34 so I agree that -- with the Board's decision that the -- the data that's taught by Hiraishi does not all go back to the memory controller at the identical time.

It's -- but what I don't agree with is that it doesn't -- that it does not adjust the timing at all and 10:17:06 that -- and furthermore, that it doesn't adjust the timing of the output by the data buffer 300.

So it depends on how you interpret this sentence. There is -- there's still more adjustment that needs to be done within the -- within the memory 10:17:31 controller, but there is still adjustment being made, just not -- it doesn't completely level it. It doesn't completely provide it all at the same time.

Q. Okay. Why don't we take a break if you're amenable now, since we've been going for over an hour, 10:17:57

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and maybe I'll track down that exhibit and we can talk about it a little bit more.

A. Okay.

THE REPORTER: Off the record, Counsel.

(Recess.) 10:18:52

THE REPORTER: Back on the record.

Q. BY MR. LINDSAY: Okay. Dr. Wedig, will you take a look at your declaration, paragraph 142, or I guess it's easier just to turn to page 98, because I wanted to talk about the figures there. 10:30:11

A. Okay. Let me get oriented with what's being discussed here.

Okay. I see it.

Q. So you've annotated this Figure 5 from Hiraishi with certain colors. Those are your additions; right? 10:30:53

A. Yes, that's correct.

Q. Okay. What is the difference between the -- I'll call them orange solid lines and then the orange crosshatched lines, or if you prefer a different description? 10:31:19

A. No, that's fine.

So the solid lines indicates memory data being transferred, and the orange crosshatched lines indicates DQS signals being transferred.

Q. So are the solid orange lines a data path? 10:31:53

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MR. CHANDLER: Object to form.

THE WITNESS: They're part of the data path.

Q. BY MR. LINDSAY: Does a -- suppose a bit of DQ data is presented at L1 and output on the other side at L0. Has the bit of DQ data traveled along a data path? 10:32:31

A. Yes, it has.

Q. So with respect to the dashed lines now, are those dashed lines a data path?

MR. CHANDLER: Objection. Form.

THE WITNESS: They are part of the data path. 10:33:05

Q. BY MR. LINDSAY: What is the data path through Hiraishi's buffer shown in Figure 5?

MR. CHANDLER: Objection. Form.

THE WITNESS: So it's -- it's at least all of the orange lines, both solid and hashed, shown in the two depictions of Figure 5 on page 98 of my declaration. 10:33:38

Q. BY MR. LINDSAY: So is that the data path that you've identified to satisfy the limitation in Claim 1 that recites a data path?

A. Yes, that's correct. 10:34:28

Q. So to satisfy the data path that's recited in Claim 1, you're identifying the combination of the solid orange DQ paths and the crosshatched DQS paths; is that -- do I understand that correctly?

A. Yes, as illustrated in the two representations 10:35:02

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of Figure 5. Yes, that's correct.

Q. How about the red -- I guess red lines? Are those part of the data path?

A. No, they're not. They're not part of the data path. 10:36:13

Q. What are -- what are the red lines signifying?

A. The red lines signify the control of the data path.

Q. Do the red lines transmit control signals then?

A. To the extent that they affect the data path -- 10:36:44 control the data path, I mean, that's one way to describe it. I mean, "control" is a very broad term, so, yes, they control the data path, so you could describe them as control signals.

Q. Well, I -- that's fair. 10:37:02

Let me ask you: What is your understanding of what Hiraishi transmits on the red lines?

A. It transmits signals which control the data path.

Q. And those signals are not part of the data path, 10:37:26 I think you just said a second ago?

A. I mean, they're not -- no. They're not literally part of the data path. I mean, they're used to control the data path. So, yeah, I mean -- yeah, it's not part of the data path. 10:37:49

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Q. How about the CLK signals LCLKR and LCLKW, are those part of the data path through Hiraishi's data buffer?

A. No, they're not.

Q. Looking at the same page we've been looking at, page 98, what's the difference between these two annotated figures? 10:38:45

A. One of them shows the use of a data path -- the top one shows the use of the data path for transmitting data from -- from the memory -- the memory device to the memory controller, so it's a read operation. 10:39:10

The bottom version of Figure 5 shows the transmission of data from the memory controller to the memory device. That is a write operation.

Q. I see. 10:39:43

So the orange lines in the top figure represent, in your opinion, that data path for read operation, and then the orange lines in the bottom figure represent the data path for a write operation. Did I get that right?

A. Yes, that's correct. 10:40:09

Q. Is the data register control circuit 320 part of the data path through Hiraishi's data buffer?

A. No, it's not.

Q. Is the DLL circuit 310 part of the data path through Hiraishi's data buffer? 10:40:37

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A. No, it's not.

Q. Is it your opinion that DQS signals that correspond to DQ data signals follow the same data path?

MR. CHANDLER: Objection. Form.

THE WITNESS: I guess I'm not sure exactly what you mean by "follow the same data path." I mean, they don't always travel alongside the data signal. I mean -- but they -- they do perform logically alongside. I mean, they do -- they do help -- they do facilitate the transfer of the data. 10:41:40 10:42:07

Q. BY MR. LINDSAY: Right. So when I say "correspond," just so we can have a common terminology --

A. Uh-huh.

Q. -- when you're transmitting data, it's known in the art to transmit strobe signal along with that data. 10:42:22

And why is that done?

A. Well, because the strobe signal helps to give the information of when the data is valid at a particular point in time.

Q. Okay. So if I say strobe signal that corresponds to a data signal, that's what I'm referring to. It's the strobe signal that's being used to validate the -- the data that it's being transmitted to. If you'd prefer a different way to describe it, we can. I'm just trying to have at least a common understanding of -- of 10:42:50 10:43:25

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the question.

So with that in mind, when data is transmitted with corresponding strobe signals, does the data and the strobe signals travel along the same data path?

A. That's my -- the last part is the part that confuses me a little bit, and it's simply that does it travel along the same data path. It's all part of the same data path. The -- it is always the case that a DQS signal is associated with a particular data signal, and that same relationship continues from one side of the data path to the other, if that's your question. It's not the case that the DQS will change partners, so to speak, in going through the -- in the process of traveling through the data path. 10:43:59 10:44:32

Q. Right. So -- all right. I'll try to rephrase that. 10:45:10

A. Okay.

Q. I see your point.

So when data is transmitted with corresponding strobe signals, do the data and strobe signals -- strike that. 10:45:23

So when data's transmitted with corresponding strobe signals, does the data and the strobe signals travel along a common data path?

A. I'll answer yes, with this understanding, that 10:46:10

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as I said earlier, the -- the data lines and the -- and the strobe signals are all part of the data path. There's -- we're only talking about one data path here. So do they travel along a common data path, yes, of course. They are all part of the one data path that we've been discussing. 10:46:37

Q. And why is it your understanding that the strobe signals are part of the data path?

A. Well, primarily because I think one of ordinary skill understands that they are, but I believe there is support in the '608 patent that says that they are. 10:47:03

Q. Do you have a -- I guess I'll take those in reverse order.

Do you have a citation for where in the '608 patent it says that the strobe signals are part of a data path? 10:47:31

A. Well, the easiest place -- I'm sure -- I mean, I haven't looked lately in the specification. I can spend the time searching for it if you'd like. But the simplest place to see it clearly, I think, might be back at Claim 10. 10:47:51

In particular, it says that -- in Claim 10A it says, "Each respective buffer circuit includes a first data path for transmitting a strobe signal."

So it says quite clearly there that it's the 10:48:20

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understanding of the inventor of the '608 patent that the strobe was part of the data path.

Q. So is it your understanding that the term "a first data path" there is referring to the same data path from Claim 1? 10:48:52

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes. My understanding of the claim interpretation is that when you say "A," it means you're referring to something previously. I think if you say -- I'm sorry. Let me get this straight. Well, no, 10:49:16 I'm not going to try and play lawyer here. But my understanding is that yes, that's the same data path from Claim 1.

Q. BY MR. LINDSAY: Is there -- besides Claim 10, is there any other part of the '608 patent that in your 10:49:40 opinion supports the idea that a strobe signal can be sent on a data path?

A. Well, let me look.

I'm going to need a little bit of time to search the patent, I guess, because I don't have anything in 10:50:29 mind at the moment, but I can search if you'd like.

Q. Well, let's -- let's do this in a couple stages, so do you cite to anything in your declaration from the '608 patent that supports the idea that a strobe signal is sent on a data path? 10:50:54

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A. Give me a moment.

Again, I'm going to need to do a search. I'm going to search my -- search my declaration.

You specifically asked for citations in the '608 patent; correct? 10:52:29

Q. Well, I was -- yes. And then I asked for any citations in your declaration to the '608 patent, because I thought it might be easier to identify.

A. Sure. Okay. All right. One moment, please.

The -- I'm not finding the patent -- '608 patent, as searchable. I'm going to use a -- I'm going to use a PDF version of it to do searching. 10:56:24

Q. Sure.

A. Okay. So you asked me in relation to my declaration, and I don't see it in my declaration, but I do see references in the '608 patent, and I have more beyond that. But are you interested in hearing from the '608 patent? 10:58:22

Q. Yes.

A. Okay. Well, first of all, it says generally on -- in column 3, approximately line -- starting on line 57, "also each buffer circuit associated with a respective group of memory devices is in the data path between the respective group of memory devices and the memory controller." 10:58:43 10:59:15

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That confirms that there is a data path between the memory devices and the memory controller.

Q. Okay.

A. One minute.

Okay. So Claim 10 is what I see for -- in relation to the patent. However, there is further support of what one would have understood at the time of this patent in Butt, B-U-T-T, the Butt reference, in that it also shows a data path, and it shows the -- it shows the strobe signals being part of the data path there also. 11:03:21 11:03:51

Q. Okay. Yeah. Thank you for taking the time to look through that. Let's put that aside for a moment, so we'll take this in pieces, if you don't mind.

A. Okay. 11:04:09

Q. So the first question is: Do you cite to anything in your declaration, now after reviewing it, from the '608 patent that supports the idea that a strobe signal is sent over a data path?

A. Let me look. 11:04:42

Let me make sure I understood your question. Would you ask one more time, please?

Q. Sure.

Did you cite to anything in your declaration from the '608 patent that supports this idea that a 11:05:19

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strobe signal is sent over a data path?

A. I'm having trouble with understanding "a strobe signal is sent over a data path," or that -- yeah, I guess it's the same thing -- would you also accept it's the same thing as saying that a strobe signal is part of a data path? 11:05:45

Q. Yes. That's a fine way of saying it as well.

A. Okay. One moment.

Well, I don't see anything in my declaration that gives a definition of data path that includes the DQS signal, but there's nothing in my declaration that says that it's not. And there is nothing in the -- in the '608 patent that says that there's not, and, in fact, there is support to one of ordinary skill that a DQS signal is part of a data path in other references that were available at the time of the '608 patent. 11:08:02 11:08:34

Q. Okay. So thank you, but --

A. In addition to what I already pointed out, of course.

Q. Right. 11:08:52

A. I already pointed out Claim 10.

Q. Right. So I want to break that down just so the record's -- the record's clear.

So there are no citations in your declaration to the '608 patent that supports the idea that a strobe 11:09:08

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signal is sent over a data path?

MR. CHANDLER: Object to form.

Q. BY MR. LINDSAY: Is that fair?

MR. CHANDLER: Same objection.

THE WITNESS: Other than where I discuss in my declaration the interpretation of Claim 10. Of course, I do discuss Claim 10, which is part of the '608 patent, and which clearly identifies that a strobe signal is part of a data path, and so that part of my -- I mean, I can identify the pages if you'd like, but that part of my -- of my declaration does, of course, cite to Claim 10, showing it to be part -- that the strobe signal is part of the data path. 11:09:23 11:09:44

Q. BY MR. LINDSAY: Okay. Yeah, that's fair.

Besides Claim 10, which -- since we've talked about that, is there anything in the '608 patent that supports the idea that a strobe signal is sent over a data path? 11:10:05

A. Or that is part of the data path?

Q. Or that is part of the data path, correct. 11:10:30

A. Yeah, no. I -- I searched the '608 patent. At least as I sit here now, all I see is Claim 10.

Q. Okay. And then -- so we can transition to the Butt reference, if you'd like then, so that we're breaking this down. 11:10:53

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The Butt reference uses the term "data path" to include both data signals and strobe signals. Is that your position?

A. That's -- yes, that's my position.

Q. Outside of the Butt reference, have you ever seen another reference describe a strobe signal as being sent over a data path or as part of a data path? 11:11:16

A. I'm sure that I have. Because I think one of ordinary skill would understand that a strobe signal is part of a data path. It travels from the memory controller to the memory device, and it also travels from the memory device back to the memory controller to facilitate data transfer. So I'm sure I've seen it. 11:11:47

I mean, I gave the -- it's like -- I gave the references that I did, but I'd have to go through all of my papers, all of my books in order to show you where it's also shown. I mean, I cited to the ones that I thought were the most relevant. 11:12:11

Q. The ones that were most relevant being -- being the Butt reference? 11:12:35

A. Correct.

Q. And you said that a person -- I'm sorry. You said that a person skilled in the art would understand that a strobe signal is part of the data path. Why specifically would a strobe signal be part of a data path 11:13:01

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and not a CLK signal, for example?

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, because it travels -- it travels with the data. It helps to define when the data is valid. It is -- it is specific to a particular data element, and, therefore, is not a CLK, as at least I define a CLK. 11:13:26

Q. BY MR. LINDSAY: Hiraishi does not transmit strobe signals over the DQ data path, does it?

MR. CHANDLER: Objection. Form. 11:14:21

THE WITNESS: It does not transmit strobe signals over the DQ portion of the data path. It sends it over the DQS portion of the data path.

Q. BY MR. LINDSAY: And the Butt reference, does it send strobe signals over the DQ portion of the data path, as you say? 11:14:45

A. No, it does not.

Q. So in both Hiraishi and Butt, strobe signals are always sent on the strobe signal portion of the data path and not the DQ data portion of the data path; is that correct? 11:15:19

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes, with the understanding that the DQS portion of the data path is intertwined with the DQ portion of the data path. I mean, they're -- as I 11:15:45

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said before, each DQS signal is associated with a particular data signal, and so it's not as though there are two separate data paths. They are -- there is one data path, and it all works together.

But the DQ lines, or as what -- as what I'm defining to be the DQS portion, those lines within the data path that send strobe signals, and the DQ portion of the data path is what I've defined to be that portion of the general data path that sends data. 11:16:08

Q. BY MR. LINDSAY: Okay. Maybe a helpful way to distinguish the portions of the data path might be if we refer to the signal lines then. 11:16:37

A. Okay.

Q. So Hiraishi Figure 5 shows data signal lines and separately shows strobe signal lines; correct? 11:17:01

A. That's correct.

Q. And the Butt reference also has data signal lines and separate strobe signal lines. Is that also correct?

A. That's correct. All within modules that are defined to be the data path. 11:17:22

Q. And strobe signals never travel over data signal lines as we've defined them, DQ data signal lines, that is. Is that --

MR. CHANDLER: Objection. Form. 11:17:53

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MR. LINDSAY: Okay. Let me -- let me strike that and rephrase.

Q. Do strobe signals ever travel over DQ signal lines?

MR. CHANDLER: Objection. Form. 11:18:12

THE WITNESS: No, not in -- not in normal traditional memory module design.

Q. BY MR. LINDSAY: And conversely, do DQ signals ever travel over DQS signal lines?

MR. CHANDLER: Objection. Form. 11:18:44

THE WITNESS: No. As I said, the DQS lines work to provide information as to when the DQ lines are valid. So they are required, and they are -- they're needed in order to assist in the data transfer, and they are associated with individual DQ lines. So you have a DQS 11:19:15 line working with a DQ line. Those two signals working together help to perform the data transfer. So the DQ line wouldn't really be operational without the DQ -- without the DQS line.

Q. BY MR. LINDSAY: Well, that hasn't always been 11:19:39 the case; right? I mean, strobe signals are a relatively recent construct; right?

A. Recent is a relative term. They've been around for a long time in relation to DDR RAMs. My understanding is they go all the way back to the first 11:20:01

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DDR RAMs, so --

Q. Right. But before the double data rate architecture, strobe signals were not used to send data. Is that fair to say?

A. That's my understanding. They were introduced with double data rate RAMs in order to provide the speeds necessary to allow them to operate. As I said, they -- they're essential to allow the data to transfer, and they are associated with individual data lines, so you can't operate a double data rate RAM without them. 11:20:24 11:20:50

Q. Right. And before double data rate, how was data accurately transmitted then if there were no strobe signal to -- to verify it?

A. I'd have to go back and review, but I believe it -- it used a CLK edge. But it's -- that's going way back. 11:21:19

Q. When does Hiraishi perform its leveling operations?

MR. CHANDLER: Objection. Form.

THE WITNESS: That question's a little vague. The question -- my -- my -- the clarification I would need is: Are you asking when does it determine that the leveling operations need to be performed or that -- determine the amount of leveling? Or are you asking when does it do it in the course of a normal data transfer? 11:22:27 11:22:48

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Q. BY MR. LINDSAY: Right.

So I guess stepping back, Hiraishi describes what it calls S4 leveling and S5 leveling; correct?

A. Right.

Q. And it describes that in the context of both read leveling and write leveling? 11:23:08

A. Correct.

Q. So my question is, then: With respect to Hiraishi's S4 and S5 leveling, when are those leveling operations performed? 11:23:24

A. I think you answered the question. It's performed during -- do you want me to break down the actual process of what happens during S4 and S5 leveling?

Q. Well, yeah, we can do that, but maybe -- this isn't supposed to be controversial. 11:23:47

A. Okay.

Q. If you get Figure 13 of Hiraishi.

A. Okay.

Q. And it describes a process there, S1 through S5.

A. I see it. 11:24:11

Q. And it says for S4 -- there's a block. It says, "Read/Write Leveling," and it's between the data register buffer and the memory chip.

And then after that is, "Read/Write Leveling," S5, and that's between the memory controller and the data 11:24:23

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buffer.

A. I see it.

Q. Okay. And my question is: Is that process of Figure 13, which includes S4 leveling, S5 leveling, when does that occur? 11:24:43

A. That -- oh, I see. Now I understand your question. Yeah, it's a simple question.

It occurs when you first start your system in your first -- your first -- your first -- initializing your memory system. 11:24:58

Q. And we -- I just said it, but just so it's a separate question, so an S4 leveling, that's between the data buffer and the memory chips or devices; correct?

A. Correct.

Q. And then S5 leveling, as Hiraishi describes it, is between the memory controller and the data buffer? 11:25:30

A. That's correct.

Q. And is Hiraishi's S4 leveling performed by circuitry in the data buffer?

MR. CHANDLER: Objection. Form. 11:25:56

THE WITNESS: Yes, it is.

Q. BY MR. LINDSAY: And for Hiraishi's S5 leveling, is it performed by the memory controller?

A. It's controlled by the memory controller. I mean, it -- it interacts with the memory buffer in the 11:26:13

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process of doing its -- doing its read/write leveling. So it doesn't only happen in the memory controller. It interacts with the memory buffer also.

Q. Okay. Let's -- I was going to start with S4, but maybe since we're on the topic we can talk about S5. 11:26:39

What is your understanding as to how Hiraishi's S5 leveling is performed?

A. Okay. It depends. There's two parts to S5. There's read leveling and there's write leveling. Which would you like to go through first? 11:27:13

Q. I'll leave it up to you.

A. Okay. So let's do write leveling first.

And that is illustrated in Figure 16A and B of Hiraishi. And what that does is it sends a -- it sends a DQS strobe signal from the memory controller to the data 11:27:47 buffer.

In the data buffer, the DQS signal is used to sample the CLK signal. And then that signal is returned via a DQ line to the memory controller to determine whether the sample signal is high or low. 11:28:16

And then what happens is the DQS signal -- the timing of the DQS signal that was sent is shifted, and it's made -- it's delayed. And then another sample is taken and that DQS signal is returned.

And that process continues until the signal that 11:28:43

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is returned on the DQ signal is different from what it was initially until it sees a transition. Specifically, it's looking for a transition of low to high.

Once it finds that transition, it knows that the DQS signal, as it -- as it arrived to the data buffer, is now in sync or now in phase with the CLK that is at that data register buffer. 11:29:13

And at that time, it then stores into its control circuitry how much it's going to need to delay the DQS signal when speaking with the data register buffer in order to allow it to operate correctly. 11:29:41

Q. And when you say it then stores in its control circuitry how much it's going to need to delay the DQS signal, are you referring to the memory controller?

A. Yes. This is -- the memory controller would -- would be in charge of this. The memory controller would -- would need to have that information, because it's the memory controller that needs to do that delay. 11:30:12

Q. And -- and by "that delay," you're referring to whatever delay the memory controller determines is necessary so that the DQS is in phase with the CLK signal? 11:30:42

MR. CHANDLER: Objection. Form.

THE WITNESS: At the data register buffer.

Q. BY MR. LINDSAY: Okay. And is -- I lied. I 11:30:59

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said we would stick with S5, but since we're on write leveling, it might be easier to talk about Hiraishi's S4 write leveling.

A. Okay.

Q. Can you describe that in similar detail, as you just described the S5 write leveling? 11:31:17

A. Sure. So what happens in S4 write leveling -- and now I'm referring to Figure 14, 14A and 14B.

So what happens in S4 write leveling -- we are now looking at the relationship between the CLK and the DQS signal that appears at the input to the memory device. We want that to now be in synch. 11:31:43

So what happens is the -- the module -- the -- the memory -- not memory. Let me get my terminology correct here. 11:32:13

The -- not memory module, but the module -- the 118. The module that communicates -- the buffer. I'm sorry. I'm saying module, but the buffer that communicates with the -- with the memory device, it sends out a DQS signal to the memory device, and then the memory device samples the CLK at the time of the DQS transition. 11:32:32

That signal -- that signal that's captured, which is what the state or the value of the CLK is at that instant, is then sent back on a DQ in or a DQ line, 11:33:04

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a data line, back to the memory buffer.

The memory buffer looks at that and is -- looks at what its value is, and then it shifts the -- it then shifts the -- the DQS signal, and it performs that step again, where it sends it out, it samples the CLK signal 11:33:33 and returns that value on a DQ signal -- DQ line.

That process continues until, again, there's a transition going from 1 to 0.

Once it sees that transition, it knows that now the DQS signal is in synch or in phase with the CLK 11:34:01 signal at the -- at the memory device.

So at that point, it stores into its control circuitry -- into the now memory buffer control circuitry, what that delay is in order to correctly send data to a memory device and be able to have it received 11:34:31 correctly and stored correctly.

Q. Okay. And why -- what is Hiraishi's right leveling in each case trying to correct for? In other words, why does -- the DQS and the CLK signal, why do they become misaligned? 11:35:09

A. They become misaligned because of the fly-by clause that are caused by the -- caused by the transmission of signals across the distance.

So whenever you transmit a signal on a line, it takes a finite amount of time for it to travel from the 11:35:33

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source to the destination.

And the CLK is no different. The CLK travels across all of the -- all of the memory devices. And so it takes longer for the CLK to reach the most distant memory device than it does for the closest memory device to the source, which is the module controller. 11:36:00

So that means that the -- the memory device that it sees first -- sorry. Let me be more clear.

When you generate the CLK in the module controller, the memory device that is closest to the module controller will see the CLK first -- receive it first. 11:36:23

Q. Dr. Wedig, I think you said, "Module controller." Did you mean data buffer?

A. Well, it depends. There's actually two ways to do it. I mean, the Hiraishi -- the patent talks about both -- both Hiraishi and the '608 patent talks about generating the CLK in the data buffer. You can also general it in the module controller. Okay? 11:36:40

The -- the problem occurs in either case, but -- so I'm talking about where the problem occurs most dramatically. That is, when you generate the CLK in the module controller. Okay? All right? 11:37:01

But as I said, you can also have the same problem when it's generated in the data buffer. 11:37:26

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Okay. Can I continue?

Q. Yes. Sorry.

A. Okay. So the CLK is generated. And as it passes down -- as it goes from one memory device to another, it takes longer for that CLK to arrive than -- than the closest memory device. So the closest memory device receives it at one time. The farthest memory device receives it at a later time. Okay? 11:37:42

So this is why you need to shift the DQS signal. Because, in fact, the DQS doesn't have to travel that long distance. The DQS signal is generated first by the -- first by the memory controller -- by the memory controller and then passed directly through to the -- through the -- through the buffer. And then it's going to go on to the memory device. And so there's a shorter distance that it has to travel. 11:38:07 11:38:32

And given that there's a shorter distance, that helps explain the SKU or the fly-by delay that occurs between -- between one memory device receiving the DQS signal versus another -- a farther away memory device receiving the DQS signal. 11:38:56

Okay. I don't know if I explained that clearly or not. I mean, I'm happy to answer the questions.

Q. Yes. Yes, that was very helpful.

And I believe a moment ago you talked about the 11:39:18

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result of this S4 right leveling being stored in the data buffer?

A. That's correct.

Q. And how is that result used, then, to actually correct these -- for this fly-by issue? 11:39:40

A. So what it does is once you have that -- the necessary delay, as I just said -- or you just said and I agreed with, once it stores that -- that value in the -- in the control section of the data buffer, it then uses that -- it uses that value to tell you how much to delay 11:40:07 the DQS signal and its associated DQ data in a -- when you're doing a normal write operation.

Q. And I guess my question was more specific, which is: Which -- and if we can look at Figure 5, if it's helpful -- which components actually carry out that 11:40:41 process of using that stored value to correct the -- for the fly-by issues?

A. Well, it's part of the write leveling circuit, 322, that's shown in Figure 5. And that write leveling circuit goes to the DLL circuit. And so it would control 11:41:08 the DLL circuit to adjust the LCLKW signal to perform that shift of the DQS in order to have it line up at the -- at the memory device at the proper time.

Q. And delay circuit 370 is what -- is receiving the local CLKW there. What is the delay circuit 370 11:41:47

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doing?

A. That -- that would be doing the approximately 90-degree shift in order to -- I mean, it -- it actually probably has multiple purposes. It -- it can do the approximately 90-degree shift that you have to do. It may also participate in the delay operation for -- for delaying the DQS signal. You could implement it in multiple ways. 11:42:13

Q. Is it delaying the local CLKW signal that it receives? 11:42:40

MR. CHANDLER: Objection. Form.

THE WITNESS: I'm sorry. One more time. The question was, is it doing what?

Q. BY MR. LINDSAY: Is it delaying the local CLKW signal that's -- it receives? 11:42:59

A. Yeah, as I said, it -- it can operate -- I think it can operate one of a couple ways. I might have to go back to absolutely verify what Hiraishi says about it, but my understanding was that it -- it takes the LCLKW, and it delays it by approximately 90 degrees. 11:43:23

As I said, it could also participate in the additional delay that is needed in order for the DQS to line up with the CLK signal.

Q. Right. Understood.

I guess my question was, though, in either of 11:43:43

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those situations --

A. Uh-huh.

Q. -- it's delaying the local CLKW signal that it receives. Is that -- do I have that right?

A. Yes, that's correct. 11:43:57

Q. And then what is strobe-generating circuit 372 doing with that now delayed CLK signal?

A. So it's taking --

MR. CHANDLER: Objection. Form.

The number is confusing, what you just said. 11:44:19

MR. LINDSAY: Oh. Oh, yes.

THE WITNESS: Good catch.

MR. LINDSAY: It should have been strobe-generating circuit 374.

THE WITNESS: Right. So that's doing what the 11:44:36 box says it's doing. It's taking a -- it's taking an indication -- it's taking some type of start instruction, meaning to start making a DQS signal. And that could simply be a transition that says: Take that signal and form a strobe out of that. 11:45:06

So create a rise, create a -- a hold for short time and then create a fall.

So make a strobe using the instruction from the -- from the delay circuit.

Q. BY MR. LINDSAY: So if we can look at Hiraishi 11:45:41

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itself.

A. Okay.

Q. And I'm looking at paragraph 123.

A. Okay. I see that.

Q. So Figure 11 is describing a -- a read memory operation. Is that -- is that your understanding? 11:46:12

A. Yes, it is.

Q. And so this is not a leveling operation in Figure 11?

MR. CHANDLER: Objection. Form. 11:46:31

THE WITNESS: No. This would occur after leveling has been performed. It would use the leveling information in order to perform a normal read operation. This is what is going to be done once your system is now fully operational. 11:46:49

Q. BY MR. LINDSAY: Okay. And -- and going down a bit to, then, Figure 15, and then focusing, I guess, on the language in paragraph 147 that describes Figure 15.

Do you see that?

A. Give me a moment, please. 11:47:14

I see paragraph 147.

Q. And this is saying Figure 15 is explaining the read leveling operation; right? So this is not a normal memory operation, which is what Figure 11 was about. Is that your understanding? 11:47:45

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A. Yes.

MR. CHANDLER: Objection to form.

THE WITNESS: Right.

Oh, sorry.

MR. LINDSAY: Okay. Okay. Can we go off the record for a second? 11:48:00

MR. CHANDLER: Sure.

THE REPORTER: Off the record.

(Recess.)

THE REPORTER: Back on the record. 12:47:25

Q. BY MR. LINDSAY: Okay. Dr. Wedig, I'm on page 125 of your declaration, looking at a Figure 11 from Hiraishi that has been annotated there.

A. I see it.

Q. Okay. The DQ out from the memory chip indicates there's a CAS latency of five CLK cycles; is that right? 12:48:14

A. Yes, that's correct.

Q. And then the DQ out from the data buffer indicates that latency is now six CLK cycles; is that -- am I reading that right? 12:48:56

A. Yes, you are.

Q. So does Hiraishi then describe setting the CAS latency to one CLK cycle to the immediately next CLK cycle --

MR. CHANDLER: Objection. Form. 12:49:36

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Q. BY MR. LINDSAY: -- in order to account for some flight time delays?

MR. CHANDLER: Objection. Form.

THE WITNESS: So more generally, the way I read Hiraishi is it teaches to extend the CAS latency or to 12:49:57
extend the -- more generally, the transfer back to account for the fly-by delays.

Now, in the particular example, they show it going from five to six. I don't think Hiraishi -- well, 12:50:30
first of all, I'm sure Hiraishi never deliberately said that you delay it by only one CLK cycle. It just shows this as the example.

But it does require that you extend it -- you extend the time from the time of the read until the data 12:50:53
is returned in order to account for the fly-by delays by inserting the delay.

Q. BY MR. LINDSAY: Right.

So in this example, he extends the latency by one CLK cycle. Does he provide any other examples of latency increases? 12:51:23

MR. CHANDLER: Objection. Form.

THE WITNESS: I have in mind -- I have to go check and make sure, but I have in mind that he shows -- he shows an example for a write operation. Let me -- let me -- let me check before I speak, please. 12:52:01

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So in, yeah, Figure 12 of Hiraishi, it shows an example where a write operation is extended from four -- the write latency is extended from four CLK cycles to five CLK cycles.

So I think the way -- what I learn out of Hiraishi is that you need to extend the memory operation to account for the fly-by delays, and I don't think we're fixed to being only four to five or five to six. It would be whatever -- whatever you initially had to something longer. And it would, you know, be the -- teaching is to take into account the fly-by delays by adding additional delay. 12:52:52 12:53:17

Q. BY MR. LINDSAY: Right.

But the two examples that Hiraishi gives, both those examples increase the latency by exactly one CLK cycle. 12:53:38

MR. CHANDLER: Objection. Form.

THE WITNESS: You're correct that the examples they give extend it by one CLK cycle. But as I said, I don't think Hiraishi is limited to that. 12:54:01

What I learn out of Hiraishi does not limit me to that.

Q. BY MR. LINDSAY: Okay. Does Hiraishi disclose how to correct for delays that are greater than one CLK cycle? 12:55:10

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A. I didn't see any discussion in Hiraishi about doing that, so I think your answer is no. I didn't find anything in Hiraishi that discussed that.

Q. And, in fact, it only show fly-by delays that are less than one CLK cycle; right? 12:55:35

A. That -- that's all that's given in your examples, yes, that's correct.

Q. Is it the case that regardless of fly-by delay, that Hiraishi's examples address that delay by adding one CLK cycle of additional latency? 12:56:14

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, to be clear, Hiraishi does not teach to simply add one CLK cycle of additional delay. What Hiraishi teaches in its examples is to add whatever delay is necessary in order to allow the -- the 12:56:41 individual memory devices to load the data buffers at the same time.

So in these examples, it shows one CLK cycle of delay. But the general teaching of Hiraishi is to account for the fly-by delays and then delay -- delay the 12:57:17 load until they -- until they all line up.

Q. Well, it's to delay the load until the next CLK cycle in the two examples that we were talking about; right?

MR. CHANDLER: Objection. Form. 12:57:41

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THE WITNESS: And, again, you're looking at just these specific examples, and I'm referring to the general teaching of Hiraishi.

Q. BY MR. LINDSAY: Right. Yes.

So, again, I think it would be most productive if we break things down. You know, we can look at other areas in Hiraishi that might support a more general reading. 12:57:54

A. Okay.

Q. But just so we're, I guess, moving forward on the examples, in the two examples, regardless of what the fly-by delays are, Hiraishi, in those examples, just sets latency to the next CLK cycle to address that? 12:58:05

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, now you're -- I heard you say something a little bit different. Can I -- can I address that? 12:58:32

Q. BY MR. LINDSAY: Sure. Of course.

A. Okay. So you're correct that in these examples, it changes the write latency and the read latency to add one more CLK cycle. However, Hiraishi is not delaying the load by just one CLK cycle. And the reason for that is it's -- it's delaying the load to be -- to -- as to whatever it needs to be in order to be able to account for the fly-by delay. 12:58:49 12:59:23

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So, for example, if you look at -- let me find it here.

If you look at Figure 15, in Figure 15 where we are determining what the delay of the data is coming back from the -- from the memory device, you see that the 12:59:45
memory device that's close to the -- that's close to the -- close to the center of the -- of the DIMM -- that is, data buffer -- what's being called data buffer 0 here, has a very short delay.

And then the one at the very -- at the very end 13:00:10
of the DIMM has a longer delay. And that's all due to fly-by delay. And so you see that the time "A" is only slightly longer than a T5, which is -- if it had been ideal, if it had -- if there were no fly-by delay at all, it would have arrived right at T5. 13:00:30

The one -- the device that's much further out is -- has gotten very close to T6.

And so what actually needed to happen is that there was a different delay that was inserted for the -- for the memory device that was close to the memory buff 13:00:54
or close to the center versus the delay that you needed to insert for the device -- for the memory device that was much further from the center of the DIMM.

So I just want to be clear that it wasn't simply adding one CLK cycle of delay. It was adding one CLK 13:01:17

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cycle to the memory read operation so that the -- so that all of the devices would have the data and would transfer at the same time. But the amount of delay that was occurring was depending upon the amount of time it needed to make up for in order for it to line up with CAS latency equal to -- equal to six. 13:01:46

Q. Right. No, I -- I think we're on the same page.

A. Okay.

Q. So the CLK signal, CK(IN), that's along the top there, that's -- is that a system CLK that's available to all the memory chips, the data buffer and a register, I guess, which isn't really shown, but it's a system-level CLK; is that correct? 13:02:09

A. Yes, that's correct. That same CLK is given to the memory chip -- the CLK that's given to the memory chip is the same CLK provided to the data register buffer. It's a system-level CLK. 13:02:30

Q. So -- so the data buffer and the memory chips will know when they are at T5 or T6?

In other words, it would be a common -- in other words, it would be the common understanding of where in the operation all the devices are? 13:03:03

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah, that's correct.

Q. BY MR. LINDSAY: And so we were just talking 13:03:24

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about the fact that memory chip 200-0 has a much shorter flight time delay because it's closer than memory chip 200-19, which has a longer delay and -- in order to -- in order to output data at the same time.

So to -- 13:04:09

A. Uh-huh.

Q. -- accommodate that different delay, the data buffer then is outputting it all at T6?

MR. CHANDLER: Objection. Form.

Q. BY MR. LINDSAY: Regardless of where it came from, it -- it would be output at T6? 13:04:24

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah, it output to T6. So they're all outputs at the same time. So that's why -- that's why their delay is necessary, to be inserted based on the different times at which the data is returned. 13:04:39

Q. BY MR. LINDSAY: Right.

And I guess I was just trying to -- I think we're saying the same thing, is that the output is -- the data's output at T6 regardless of how long the flight time delay was, it's just that some data has to be delayed longer than other data? 13:05:03

A. That's the --

MR. CHANDLER: Objection. Form.

THE WITNESS: The goal -- the goal is to be able 13:05:18

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to output the data at the same time, right. And so I think we are saying the same thing.

And so if it comes in quickly, you need to add more delay than if it comes in later.

Q. BY MR. LINDSAY: When you say add in more delay -- I mean, at a signal level -- 13:05:44

A. Uh-huh.

Q. -- how does that work?

A. I -- I don't understand your question. I mean, do you want to look at -- 13:06:10

Q. So I guess let me maybe pose it differently, if I could.

I have a series of data buffers, nine data buffers. They're receiving data at different times.

A. Uh-huh. 13:06:35

Q. In order to output them at the same time -- and I want to do that at T6 --

A. Okay. Uh-huh.

Q. -- am I, as a data buffer, looking at the CLK signal and then -- for that operation, obviously, when I get to T6, outputting whatever I've accumulated at that point? 13:06:56

I'm just trying to understand. Is that generally how it works?

MR. CHANDLER: Objection. Form. 13:07:12

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THE WITNESS: Well, it's -- it's -- yeah, it's going to hold. It's going to come into the data buffer. It's going to hold the data, if it came in early, and then it's going to output it at T6.

And if it comes into the data buffer later, then it's going to hold it until it gets to T6 in this example. 13:07:33

So the amount of hold time is going to be different based on when it came in. And so that's -- that's where the delay occurs. 13:07:50

Q. BY MR. LINDSAY: Right.

But I guess my question is: When I get to T6, what is -- where does the signal come to say: Okay, transmit it out. We're at T6.

A. Where does the signal come? I mean, that's the entire purpose of doing this retraining. You do the retraining to determine when the signals arrived so that you know how long to hold it. Maybe I'm not understanding your question. 13:08:16

Q. Right. So maybe I'm not clear. 13:08:38

So looking at -- you can look at whatever you want, but in -- you know, Figure 5 has the -- maybe the most information. And what I'm trying to figure out is on a signal level --

A. Uh-huh. 13:09:02

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Q. -- this data buffer, for example, is having data come into the FIFO --

A. Uh-huh.

Q. -- and -- remind me, were we talking about a read operation or a write operation? 13:09:19

A. Right now we're talking about a read operation.

Q. Okay.

A. Write operation -- write operation also has a delay, but we're talking about read right now.

Q. Okay. So the data's coming in to FIFO circuit 302 in -- in the context of what we've been talking about. And it's going to be -- it's going to get sent out at T6. So what -- is it the DLL circuit that's -- it's receiving the system CLK, so it knows T6. Is that DLL circuit what is triggering the clocking-out of the data, then, at T6? 13:09:29 13:09:59

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, the DLL -- I mean, in a sense, yes. I mean, the DLL circuit gives you the timing for the chip. So yeah, so it's going to generate the CLK. 13:10:16

So -- so after it's held it the appropriate amount of time, it will CLK it out at T6. And yeah, the DLL circuit is in charge of making that CLK.

Q. BY MR. LINDSAY: Okay. And then all the other 13:10:37

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eight data buffers, if we're -- if we're in that type of a module, are also receiving their CLK signals and their respective DLL circuits saying: Okay, for this operation we're at T6 --

A. Uh-huh. 13:10:56

Q. -- CLK out whatever we've got in the FIFO at that point?

A. Again, for this example --

MR. CHANDLER: Objection. Form.

THE WITNESS: Again, for this -- for this 13:11:03 example, right, it's going to hold it for whatever length of time it needs so that they all -- you know, to that -- you're going to hold it until the last one arrives, and then you send it out.

Q. BY MR. LINDSAY: Yeah, and so in Hiraishi's 13:11:24 case, his -- he doesn't disclose delays greater than one CLK cycle. So if you delay to one CLK cycle, you'll know that he has accounted for all possible delays in his system?

A. Again, I want to make sure we're clear on this. 13:11:51 We don't just delay one CLK cycle. We delay whatever time is necessary --

Q. Right.

A. -- in order that -- in order for it to line up. I mean, in fact -- but you're correct that in the 13:12:04

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examples, he doesn't show anything more than one CLK cycle, so -- but my understanding from Hiraishi is that you delay the length of time necessary for it to line up.

And that could be extended. If it requires multiple CLK cycles in -- you know, Hiraishi doesn't teach that. But I think one of ordinary skill could extend this using other references to assist in order to help understand how -- you know, a way to do that. But you could extend it to more than a CLK cycle with -- with further information. 13:12:23 13:12:47

Q. Is that -- are you -- you said with other references. Would Tokuhiro be an example of another reference that would suggest delays of greater than one CLK cycle?

A. Tokuhiro would help and Giovanni would help also. 13:13:11

Q. So a moment ago we talked about the examples -- a little while now, I suppose, we've been talking about the examples, and -- and you said that there were other teachings in Hiraishi about the delay of -- can you point me to what you were referring to then? 13:13:36

A. I'm trying to remember what I said it in reference to. I mean, Hiraishi is more than just the Figures, you know, 5 and 11 and, you know, 12. So, I mean, I guess -- remind me. 13:14:09

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Q. Okay.

A. Teachings for what in particular?

Q. Right.

So we were talking about the fact that in the two examples that Hiraishi shows in the figures -- 13:14:20

A. Uh-huh.

Q. -- he's setting the latency to, you know, one CLK cycle higher.

A. Right.

Q. And -- and I believe you said it doesn't have to be one CLK cycle that teaches -- it doesn't have to be one CLK cycle or something to that effect. 13:14:30

And so that's what I was trying to understand, is what other part of Hiraishi you would consider as teaching something other than setting latency to just the next highest CLK cycle? 13:14:56

A. Okay. Good. All right. Now I understand your question. One moment.

Okay. So looking in paragraph 128 of Hiraishi -- 13:16:24

Q. Okay.

A. -- they use -- they're using CL equals 5. It says, "In the example shown in Figure 11." So, I mean -- and then it goes on to say, "In the example shown in Figure 11," multiple places -- what they're is that 13:16:44

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nothing is fixed to being CL 5.

And down in 133, it says, "In this example, W" -- "WL = 4."

And so, you know, I just -- I think what you need to do is to focus on the general teaching and to not be caught up in the example being the only way to do it. 13:17:20

So I -- I use Hiraishi as a general teaching. And, you know, the examples are purely just examples.

Q. Right.

So I understand that setting -- having a CAS latency of 4, 5 or 6 would be -- you know, vary from system to system, design to design. 13:17:47

But what I was asking for more particularly is: Regardless of what that official latency value is --

A. Uh-huh. 13:18:13

Q. -- the two examples we looked at increased it by one CLK cycle.

MR. CHANDLER: Objection. Form.

Q. BY MR. LINDSAY: So I'm focusing on the increase. 13:18:23

A. Uh-huh.

Q. And I wanted to understand what broader teaching Hiraishi may have, in your opinion, that it didn't have to be the next CLK cycle, regardless of where you started. 13:18:37

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A. Okay. So the words "it doesn't have to be the next CLK cycle," those word were not found in Hiraishi. But what is found in Hiraishi is that you measure the time "A," and then you give that -- with that information, it tells you how long to delay. 13:19:04

And what I learned from that is that if you -- if you do need to delay longer than a CLK cycle, then you do that with appropriate modifications to -- to the design of Hiraishi, such as what we provided in other references. 13:19:31

Q. So -- right, so I think we're getting to it.

So the part about measuring time "A" and figuring out from there the delay, that part, where would I find that in Hiraishi?

A. You find it -- well, I can -- I mean, I can -- I can find the words. But I'll point to the figure, which is -- and if you'd like me to find the words for it, I will. But it has to do with -- one moment, please. 13:19:47

Back at Figure 15, in showing the time "A," it says -- it says to measure the time "A." And then it says to do things once you measure the time "A." And it does specifically say to -- well, I'll find the words for that because I know what you're looking for. 13:20:15

Okay. In paragraph 51 -- 151, it says, "The time is measured for each of the memory chips, stored in 13:20:54

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the data register control" -- let's see.

"The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in the adjustment of an activation timing of the input buffer INB and the like." 13:21:13

So it says for -- it's the activation of the input buffer and the like, meaning other things that need to be done.

And then when you get to looking at what "and the like" is, you see that it is doing the delay that's necessary in order to have it all line up. 13:21:27

Q. So the Butt reference we talked about earlier describes a strobe-centering process generally; right?

A. Generally, yes. 13:23:05

Q. And is -- is the Butt reference either advancing or delaying a strobe signal in order to optimize -- I think what it calls the data valid window?

A. It's -- yeah, it's -- it's adjusting the -- it's adjusting the DQS signal to be able to optimize where it samples the data in the -- in the data valid window. 13:23:45

Q. And what's the benefit of doing that?

A. Well, it gives you a reliable way to be able to capture the data.

Q. And does Butt delay or advance the DQ data 13:24:12

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signal as well?

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, it -- you know, well, Butt teaches primarily -- I mean, it -- when Butt teaches the optimization, it is in order to allow you to sample the -- the DQ signal in the best position. 13:24:46

So you're moving the DQS while holding the DQ the same. So it -- you're trying to get right in the -- right in the middle, the best, most optimal spot to where you want to sample the valid data. 13:25:15

Q. BY MR. LINDSAY: Okay. I think I understand that.

I'm going to jump ahead, then, in your declaration to page 211 --

A. Okay. 13:25:42

Q. -- and start talking about the Tokuhiro reference.

A. 211? I'm sorry, page 211?

Q. Yes, page -- there's a figure there, which is right above paragraph 262. But I thought it would be easier to give the page number. 13:25:58

A. Okay. I'm there.

Q. So in purple, there's a component labeled "DR-1."

A. That's correct. 13:26:19

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Q. Is that a delay element from Tokuhiro?

A. Yes, it is.

Q. And what kind of a delay circuit does Tokuhiro say that could be?

A. Well, he gives the details of it in Tokuhiro. Takes it all the way down to the logic gate design. But it's a -- it's an element that performs what it says. It -- it takes an input, it delays it by a programable amount and then produces an output. 13:26:36

Q. And it's kind of small. I was going to ask you about Figure 5 of Tokuhiro. So maybe we should just go to the reference itself. 13:27:06

A. Okay. Sorry. You -- you want me to open up Tokuhiro?

Q. Yeah. 13:27:27

So if we could take a look at Tokuhiro Figure 5. I just think that version on -- in your declaration's too small. At least for my eyes?

A. Okay. So just to be clear, if we're still focused on page 211 -- oh, I see. Yes, Figure 5. 13:27:40

Okay. I have that in larger -- I have a Tokuhiro reference opened, and I have Figure 5 filling my screen.

Q. Okay. So Figure 5, in roughly the middle there, labels a component DR-1, right below the DR-2 -- 13:28:06

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A. Uh-huh.

Q. -- and so on.

Is that the delay circuit in purple that we were looking at on page 211 of your declaration?

MR. CHANDLER: If I could make a suggestion so the record's clear. I mean, page 186 of the -- Exhibit 1003 has a bigger picture of Figure 5. There's a lot going on in that figure, so I just want to be able to follow along what you're saying. It's hard to get from the words. 13:28:23 13:28:44

MR. LINDSAY: Okay. Yeah, that's fine. Thanks.

Q. Let's focus on page 186 of your declaration. I think that's -- could work better.

A. Okay. I'm there.

Q. Okay. So in the purple boxes in the middle of Figure 5 from Tokuhiro, on page 186 of your declaration, there are components labeled "DR-1" and "DR-2." 13:29:00

Do you see that?

A. Yes, I see that.

Q. Okay. And so the DR-1 element, is that the delay circuit that we were just looking at on page 186 of your declaration? 13:29:16

A. So I am looking at 186, so --

Q. I'm sorry. Apologies. 211. Page 211.

A. Yes, that's the same -- that's the same delay 13:29:46

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element.

Q. And that delay element, DR-1, that's in purple at page 186 and 211 of your declaration, is being added to the buffer circuit 300 of Hiraishi?

A. Yeah. Well, to be clear, the teachings of Tokuhiro are being added to Hiraishi. And part of that requires that you incorporate the delay elements that are taught in Tokuhiro into the buffer circuit of Hiraishi. 13:30:18

Q. Okay. Understood.

And in Figure 5 of Tokuhiro, on page 186 of your declaration, what signal is the DR-1 element delaying? 13:30:42

A. Your question is: What element is DR-1 delaying?

Q. Not exactly.

So it's -- on page 186 of your declaration, Figure 5 of Tokuhiro -- 13:31:14

A. Uh-huh.

Q. -- what signal is the DR-1 element delaying?

MR. CHANDLER: Objection. Form, because there are two DR1s. 13:31:31

THE WITNESS: Do you want to clarify?

Q. BY MR. LINDSAY: You can answer the question individually or together.

A. Okay. DR-1 is delaying -- in the first case, in the upper case, it's delaying DQ1[1]. 13:31:51

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In the lower case, DR-1 is delaying the signal DQ1[K].

Q. So in each of those cases, the DR-1 component is delaying a DQ data signal?

A. Yes, that's correct. 13:32:30

Q. And then if we could look at page 213 of your declaration, the figure there.

A. Okay.

Q. So in purple, this is the DR-1 element that we were just discussing from Tokuhiro; right? 13:33:18

A. Yes, that's correct.

Q. And here, the DR-1 element is being added to Hiraishi's strobe-generating circuit 376?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes, that's correct. 13:33:51

Q. BY MR. LINDSAY: And is the delay element DR-1 delaying both the read data strobe signal 350 and the local CLK signal that's going to the read FIFO?

A. Yeah, that's correct. That would need to be the case because you want to make sure that you output your 13:34:24 data with the same delay as you output the strobe.

Q. Is the amount of delay that is applied to the read data strobe signal 350 the same or different than the amount of delay that's applied to the local CLK signal sent to the FIFO? 13:35:01

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A. Well, first of all, what you refer to as the local CLK signal -- I want to make sure that we understand each other. The signal that goes directly down to the FIFO is the same delayed signal that came from DR-1. So I don't think it's correct to refer to that as a local CLK signal. It's not. 13:35:28

Q. Okay. Well, maybe we'll back up, then.

So LCLKR, the local CLK signal from the DLL circuit, is being provided to Hiraishi's strobe-generating circuit 376; right? 13:35:59

A. That's correct.

Q. And that's also correct in the modified version of Hiraishi shown here?

A. That's correct.

Q. Okay. Is the unlabeled line that comes out of the bottom of strobe-generating circuit 376 a delayed version of the LCLKR signal that's being provided by the DLL circuit to the strobe-generating circuit 376? 13:36:11

A. Not exactly. Can I explain what it is?

Q. Please. 13:36:51

A. What it is is the same -- it's essentially the same as what comes out to the left of the box from 376. It is a -- it's a signal that took LCLKR as input to help provide the activation timing, but then it has generated a strobe -- it generated a strobe signal. It delayed it, 13:37:22

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and then that is the signal that then goes down to the FIFO. So I could have shown it as attaching to the left side and coming over and coming down because it's the same signal.

Q. I see. That was not clear to me originally. 13:37:45

So just for the record so it's clear, the strobe-generating circuit 376 --

A. Uh-huh.

Q. -- is generating a strobe; correct? And that strobe is being then delayed by DR-1? 13:38:05

A. Uh-huh.

Q. And then that delayed strobe is being output in two places, one where the crosshatch orange goes out to 350 --

A. Uh-huh. 13:38:28

Q. -- and second, down to CLK the data out of the FIFO read circuit 302?

A. That's correct.

Q. So if we could go back to 186 of your declaration and take a look at Figure 5 of Tokuhiro 13:39:15 again.

A. Okay.

Q. So here there's a memory controller 12, and it's connected to a CPU 13; is that -- is that right? Am I reading this right? 13:39:35

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A. Yes.

Q. And is -- that CPU 13, is that the main CPU of the computer?

A. Yes, that's what I understand.

Q. And there's a line labeled "d1" going from CPU 13 to certain delay elements. And then there's a second line labeled "d2" that's going from CPU 13 to other delay elements. Is that also correct? 13:39:48

A. That's correct.

Q. And what are those lines, d1 and d2, if you recall? 13:40:18

A. Those lines are control lines for setting the delay values for DR-1 in the case of d1 -- I'm sorry. Let me correct that.

So those are control lines for setting the values in the delay elements. d1 appears to be connected for a set of delay elements that are not highlighted. And d2 are for delay elements that are highlighted. 13:40:41

Q. Okay. Right.

And so just to kind of explain that a little bit, so d1 is connected to control the delay elements that are labeled "DW1," "DW2." And then again at the bottom DW1 and DW2. 13:41:08

A. That's correct.

Q. So -- so the signal line d1 is dedicated to the 13:41:35

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DW delay elements, and control signal line d2 is dedicated to the DR control elements?

A. That's -- that's the way Tokuhiro implemented it, yes. It's not -- not germane to my combination, but what you're saying is correct. 13:42:06

Q. And is it your understanding that Tokuhiro programs those delay elements in the memory controller using logic in the CPU 13?

A. That's the way Tokuhiro does it, but it can be done other ways also. I mean, that's -- that's just the way this Tokuhiro happened to implement it, but that's not the only way. 13:42:36

Q. Does -- so switching gears for a second. I'm going to ask you about JEDEC standards.

A. Okay. 13:43:11

Q. Is it your understanding that JEDEC sets limits on the size of DDR memory modules -- physical size of the memory modules?

MR. CHANDLER: Objection. Form. Objection. Form. 13:43:28

THE WITNESS: I mean, they're only limited by the addressability. I mean, I -- I think there are limits in the extent that there's only so many address lines. Other than that, it doesn't say -- they don't specifically say you cannot make a memory module larger 13:43:46

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than such-and-such.

Are you talking about physical -- I'm sorry. Are you referring to the physical size of the module?

Q. BY MR. LINDSAY: Correct.

A. Oh, okay. I'm sorry. I'm thinking of the -- of the contents of the memory. 13:43:56

Q. Right.

A. Yes. No, they -- they specify the -- the physical size that you are to make your memory module, that's correct. 13:44:08

Q. So if I wanted to make a bigger, you know -- you know, DDR memory module, that would not be compliant with the JEDEC standard if it exceeded their -- their prescribed dimensions for memory modules of that -- of that type? 13:44:34

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah, it's correct. They specify -- they specify pretty exacting what the size of the -- of the memory module should be.

Q. BY MR. LINDSAY: Does JEDEC also prescribe the dimensions for the size of the memory controller? 13:44:53

A. No, not that I know of.

Q. So Tokuhiro -- I want to look at Figure 11. I don't know if it's in your declaration, but we can -- it's up to you, if you want to pull up the reference 13:45:38

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itself or find it in your declaration.

A. I -- I have it. I've got Figure 11 from Tokuhiro on my screen.

Q. Okay.

MR. CHANDLER: It's on page 195 of your declaration, if you want. 13:45:50

THE WITNESS: I'm sorry. What did you say?

MR. CHANDLER: I'm looking at page 195 of your declaration, if that's what you guys are referring to.

THE WITNESS: Okay. 13:46:02

Q. BY MR. LINDSAY: Whatever is easiest for you, Dr. Wedig.

A. Okay. I have them both here.

Q. Okay. So in Tokuhiro Figure 11, the delay elements DR-1 through DR-n, those are in the memory controller; is that correct? 13:46:24

A. Well, the way Tokuhiro did his specific implementation, yes, that's the way it's shown.

Q. And so the DQ data and DQS strobe signals, those are being delayed in the memory controller in Tokuhiro; right? 13:46:48

A. Well, specifically, the -- the captured DQ data is being delayed, just to clarify. What you said was not exactly correct.

Q. You're right. I'll rephrase the question. 13:47:21

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In Figure 11 of Tokuhiro, is this showing that the DQ data is being delayed in the memory controller?

A. Yes. From the way Tokuhiro did his specific implementation, that's -- that's where he put it.

Q. And is this DQ data that's being delayed in the memory controller, is that arriving between T9 and T10? 13:47:45

A. Yes, that's correct.

Q. And then is the DQ data being delayed so that it all is available at T10 in the memory controller?

A. Yeah, that's exactly what Tokuhiro's teaching. Yeah, in order to have them so that they're all available at the same time. So that it all appears as though, to the system, that they arrived at T10. 13:48:24

Q. And I apologize for jumping around, but if we could go back to Figure 5 of Tokuhiro again. 13:48:59

A. Okay.

Q. And I think that was -- I'm sorry. Yeah, Figure 5 on 186.

A. Okay.

Q. So -- 13:49:23

A. One moment, please.

Okay.

Q. So in Figure 5 of Tokuhiro, what is your understanding of what is connecting the CPU 13 to the memory controller 12? 13:49:42

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A. What's connecting the two? In -- in Tokuhiro, it's all the lines that you see connect -- that are -- that are horizontally shown between the CPU and the memory controller.

Q. Right. So that -- 13:50:10

MR. CHANDLER: It's a bit garbled. Just a sec. Hold on one sec.

Can you guys hear me now?

MR. LINDSAY: Yeah.

THE WITNESS: Yes, we can hear you now. 13:50:33

MR. CHANDLER: Got it. Sorry. It got a bit garbled. Go ahead.

The question was: What's -- what's connecting CPU 13 to memory controller 12? And I heard an answer about the lines -- horizontal lines. 13:50:51

MR. LINDSAY: Right.

Q. So my question was more specific about what would -- what would the -- what would those lines be referred to? Is that a data bus or control signal bus?

I mean, in the context of the memory board where 13:51:15 these components are inserted into, what would be your understanding of what is connecting the CPU and memory controller?

A. I guess I'm not exactly sure of the question. I mean, it's made up of multiple things. It's made up of 13:51:35

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data lines, which you could call a data bus. But a data bus normally -- it also has additional signals, such as address and control.

So, I mean, I -- I don't know if I want to characterize it any more than the wires that you see here. The -- the connections between the CPU and the memory controller comprised of the lines that you see on this page. 13:51:56

Q. And on a -- on a mother board, would there be a socket to -- for the CPU to be inserted into and a separate socket for the memory controller to be inserted into? 13:52:18

MR. CHANDLER: Objection. Form.

THE WITNESS: I'm sorry. That's -- that's very system dependent. It's -- some -- some systems now have the memory controller as part of the CPU. Some of them have it separate. You know, where you draw the boxes is very system dependent. 13:52:31

Q. BY MR. LINDSAY: So in the -- that's fair enough. But in the time of Tokuhiro -- 13:52:56

A. Uh-huh.

Q. -- in the 2007/2008 time frame, would you expect the CPU to be inserted into one socket of the memory -- of the motherboard and the memory controller to be inserted into a separate socket? 13:53:21

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MR. CHANDLER: Objection. Form.

THE WITNESS: I -- you know, I don't want to characterize. It depends on -- it depends on the CPU. There were CPUs that had their own memory controllers internal in that time frame. So I -- I can't universally say one way or the other. 13:53:38

Q. BY MR. LINDSAY: You're aware of CPUs that had internal memory controllers in 2007?

A. I'm familiar with CPUs that had memory control such that you could have a CPU that talked directly to memory. Now, whether you call that a memory controller or not, anything that can control memory directly you could call a memory controller. So yes, I'm familiar with that. 13:53:57

Q. And continuing to look at our Figure 5 from Tokuhiro, what is connecting the memory controller 12, then, to the DIMM 11? 13:54:15

A. Just same answer as before, that it's a set of lines that have a set of controls and data, as shown in the -- in the diagram. 13:54:43

Q. Right.

So would that set of lines include a data bus?

A. Well, again, "data bus" is a very broad term, and it's a very loaded term. Because I don't think I'd characterize this as specifically a data bus. It is a 13:55:01

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bus which carries data. But the word "data bus" also includes address, control, read/write signals.

What I see is a series of data signals, strobe signals and a CLK.

Q. Right. 13:55:21

A. So I don't -- like I said, I -- I'm not willing to give it that labeling of a -- of a data bus only because it's -- that's a -- you know, that's a loaded term that has multiple meanings.

Q. Right. 13:55:39

Okay. And is it your understanding that Tokuhiro describes a DDR3 system?

A. Yes, I think so. I mean, let me see what Tokuhiro has to say about that.

Yeah, it's -- he's described it in the DDR3 time frame, yes. 13:56:09

Q. And I can help. Maybe one spot in column 5, line 57.

A. Column 5, 57.

Okay. Yeah, I see that. 13:56:35

Q. Okay. And so -- just to orient the next question, so in Tokuhiro Figure 5 we were looking at, would you understand that the DIMM module 11 is a DDR3 module?

A. I think it would be in the DDR3 family. 13:57:21

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Q. Fair enough.

A. There are multiple different kinds of DDR3 modules. But it would be in that family.

Q. Fair enough.

And is it your understanding that -- excuse me. 13:57:36

Is it your understanding that the memory controller 12 communicates with DIMM 11 using DDR3 signaling protocols?

A. I -- I don't see that specified in Tokuhiro. First of all, it doesn't give all of the -- it doesn't 13:58:18 give all the signals that are necessary for it to communicate by that protocol, and it also doesn't show the timing for transmitting the signals, so...

Q. Right.

So we described a second ago -- I understand -- 13:58:35 I appreciate that Tokuhiro doesn't say that it uses DDR3 signaling protocols to communicate between the memory controller 12 and the DIMM 11.

A. Uh-huh.

Q. My question is about reading Tokuhiro and the 13:58:58 fact that column 5, line 57, it says the memory controller 12 is a DDR3 memory interface --

A. Uh-huh.

Q. -- for controlling read/write operations.

Is it your understanding that that memory 13:59:15

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controller 12 would then be communicating with DIMM 11 using DDR3 signaling protocols?

A. I would say that, you know, it's possible that it could. It -- you know, I -- I read Tokuhiro more broadly to say that, you know, this is -- this is what was being done in that time frame and that a memory controller -- memory controller would -- you know, could operate in that -- with that protocol. But I don't see -- I don't see Tokuhiro limiting you to that. 13:59:53

Q. Have you ever seen a DDR3 memory interface that did not use DDR3 signaling protocols? 14:00:33

A. In actual -- in actual usage, no. But it doesn't mean that a patent that talks about DDR3 technology requires that everything be exactly DDR3 transmission protocols. 14:01:27

Q. Would it -- could you at least agree that Tokuhiro's memory controller 12 is communicating with the DIMM 11 using some signaling protocol?

A. Yes, I can agree with that. It has to have something that they agree on for communication. 14:01:51

Q. And if the DIMM module 11 were a DDR3 DIMM module --

A. Uh-huh.

Q. -- then would it be your expectation that that signaling protocol would be in accordance with the DDR3 14:02:30

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signaling standard?

A. Well, given that restriction, given that you're saying the -- the hypothetical is that the DIMM module is a DDR3 DIMM module, then yes, I would expect it to -- in that situation, to be using DDR3 communication protocol. 14:02:53

Q. Right.

And if the DIMM module were DDR2, would your answer be the same, that you would expect the memory module -- I'm sorry -- the memory controller and the DIMM to be communicating in accordance with DDR2 signaling 14:03:15 protocol?

A. Again, same answer. Given that restriction of being a DDR2 DIMM module, then yes, I would expect it to be using DDR2 signaling protocol.

Q. So in the combination -- the Hiraishi/Tokuhiro 14:03:48 combination that we've been discussing --

A. Uh-huh.

Q. -- does Hiraishi's memory controller still include delay elements on its own?

A. Hiraishi -- 14:04:14

THE WITNESS: Sorry. Mr. Chandler, did you want to say something?

MR. CHANDLER: Yeah.

Objection. Form.

THE WITNESS: Okay. 14:04:23

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Hiraishi has very little discussion about what its memory controller does. Are you asking me what's taught, or are you asking me what I would expect?

Q. BY MR. LINDSAY: What -- what would you expect?

A. Well, given that Hiraishi -- that the data that enters Hiraishi is -- the DQS and the CLK are aligned, and the data from individual -- individual data buffers are aligned. But given that the data across all the data buffers is not aligned, then I would suspect that there is going to need to be some type of alignment mechanism performed inside the memory controller. And that may involve delay elements. But, you know, they can do it however they want. 14:04:47 14:05:32

Q. And, I mean, what is the general way in the art that the memory controller in the Hiraishi/Tokuhiro combination would address those varying delays across different memory buffers then? 14:05:56

A. Well, if you -- if you have to do alignment -- if you have to make a series of data inputs that come in at different times line up to be able to have them all appear at the same time, then you're going to need to do some type of delay somewhere. 14:06:32

And Hiraishi has it occurring -- you know, that it puts that problem off to the memory controller. But this is where I thought one of the values of Tokuhiro 14:07:01

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was, that it now makes it so that Hiraishi does not cause the memory controller to have to perform that realignment.

Q. Right.

So your last answer makes me think that maybe you didn't understand my first question. 14:07:19

A. Maybe not.

Q. In the -- in the combination of the Hiraishi -- Hiraishi and Tokuhiro references, so in your combination -- 14:07:39

A. Uh-huh.

Q. -- the question was: Does the memory controller still include delay elements of its own?

A. Okay. Yeah, I'm sorry, I did not hear the combination. I heard Hiraishi. So you're correct. So strike all of my previous comments on that. 14:07:55

Yeah, the intention is that once you have read all the data and received it into the data buffer using the teachings -- okay. Into a -- okay. Let me be clear here. You receive into basically a Hiraishi data buffer and you add the additional teachings of Tokuhiro, that that data would then be supplied to the memory controller without any substantial delay. 14:08:28

Now, might it be the case that the memory controller has to do some clean-up, some slight 14:08:51

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adjustment? Possibly. But the intention is that the data is effectively all in line by the time it enters the memory controller.

So I would not expect any -- or very little realignment needing to be done in the memory controller when you have a Hiraishi/Tokuhiro combination data buffer. 14:09:11

Q. So how about offsetting the DQS by 90 degrees, would that still be done by the memory controller in the Hiraishi/Tokuhiro combination? 14:09:36

A. I think -- it would need to do that because the protocol -- the standard is to output the data with the strobe edge aligned from the -- from the data buffer.

So yeah, you would still need to -- you would still need to do that. 14:10:19

Q. Right.

And so the memory controller in the Hiraishi/Tokuhiro combination, you would expect to include a delay element for offsetting the DQS by approximately 90 degrees? 14:10:44

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah, that would be -- yeah, a simple, yeah, 90-degree offset in order to capture the data in its -- you know, in -- in the appropriate window.

Q. BY MR. LINDSAY: And so you also mentioned that 14:11:03

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the memory controller may need to do some clean-up. What did you mean?

A. Well, I mean, I don't know. I'm just leaving open the possibility that the memory controller -- I don't know that -- I just want to leave open the possibility that the memory controller may need to deal with a few nanoseconds of offset, you know, due to flight time, for example. 14:11:24

But I'm not -- I don't envision any significant delays. The hard part's been done. The hard part of lining up the data has already been taken care of. But, you know, every time you transfer something from one place to another, there's potential for flight delays and you want to make sure that you are handling that. 14:11:44

Q. And is that what Hiraishi's S5 leveling is addressing, flight delays between the buffer and the memory controller? 14:12:06

MR. CHANDLER: Objection. Form.

THE WITNESS: Are we referring to Hiraishi without the Tokuhiro combination? 14:12:28

Q. BY MR. LINDSAY: Yes. Sure. We can start there.

A. Okay. So yeah, Hiraishi is doing more than dealing with flight delays. It's also dealing with fly-by from -- from the buffers. So it's not just the 14:12:43

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flight delays of the data, the DQ and the DQS signals going from the buffer into the memory controller, it's dealing with the fly-by delays of the signals that go across the individual data buffers.

Q. Okay. So you're -- you're distinguishing between fly-by delays -- 14:13:11

A. Uh-huh.

Q. -- and flight delays. Did I say that correctly?

A. Yes.

Q. And what is the difference? 14:13:25

A. So a fly-by delay is a signal that goes across multiple data buffers. And so it will travel the -- you know, in the case of nine data buffers, it will travel, you know, across, you know, nine different data buses or four on one side, four on the other, depending upon the actual layout. And so there's a more significant delay. 14:13:48

A flight delay is the difference in timing. When you send out two signals at essentially the same time and they arrive to the same destination, there may be a difference in timing between when one arrives versus the other due to -- you know, due to line lengths, capacitance, temperature, voltage, et cetera. 14:14:13

Q. Okay. So I think I understand that.

So in the context of an architecture where you have, you know, several buffers that are all sending data 14:14:40

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to a memory controller, each of those buffers will have, as you said, different -- may have different line lengths, temperature, different factors that -- that affect the timing of when the memory controller actually receives the data? 14:15:10

A. They could. It is a possibility, yes.

Q. And the memory controller can take care of that, as is generally known in the art, I imagine?

A. Yes, of course. Yeah. You just have to keep -- you have to take that into account. And I -- 14:15:36

(Reporter clarification.)

THE WITNESS: You have to take that into account.

Q. BY MR. LINDSAY: And so Hiraishi, by itself, takes that flight delays as well as fly-by delays into account when it performs its S5 leveling? 14:15:51

MR. CHANDLER: Objection. Form.

THE WITNESS: Hiraishi I think really can only address the fly-by delays in S5 because S5 -- well, no. I mean, it -- it's not clear. Hiraishi does not really describe in detail what happens when you get into the memory controller. 14:16:25

I mean, it does talk about how the time for the read is going to come in at different times. And so I guess, yeah, that does take into account -- I mean, it 14:16:48

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takes into account the fly-by delays. But since that time is also going to be dependent upon the flight time, in that sense I think S5 takes both of those into consideration.

I don't want to stop you, but if you're at a breaking time -- time when you might be able to take a break, I'd appreciate that. 14:17:15

MR. LINDSAY: Sure. We can go off the record.

THE REPORTER: Off the record.

(Recess.) 14:21:54

THE REPORTER: Back on the record.

MR. CHANDLER: So you asked when we'd like a final, and we would like a final in one week, on Tuesday, March 19th. And we'd like the opportunity to review and make any corrections as needed. 14:30:27

THE REPORTER: And a rough transcript?

MR. CHANDLER: And a rough, yes. Thank you.

THE REPORTER: Okay, Counsel.

MR. LINDSAY: I have no further questions.

MR. CHANDLER: Can we go off the record? 14:30:46

THE REPORTER: Off the record.

(Recess.)

(Exhibit 1069, S4 and S5 in Hiraishi.pdf, marked for identification electronically by counsel.)

(Exhibit 1070, S4 read leveling in Hiraishi.pdf,

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marked for identification electronically by counsel.)

(Exhibit 1071, S4 write leveling in Hiraishi.pdf, marked for identification electronically by counsel.) 14:57:54

THE REPORTER: Back on the record.

EXAMINATION

BY MR. CHANDLER:

Q. So, Dr. Wedig, do you have Exhibits 1069, 1070 and 1071 in front of you? 15:01:57

A. One moment.

MR. LINDSAY: Object to these new exhibits, 1069, 1070 and 1071.

THE WITNESS: Yes, I have them in front of me. 15:02:19

Q. BY MR. CHANDLER: So just so we're all on the same page, Exhibit 1069 is an exhibit that shows Figure 5 of Hiraishi in the middle of the page, and then on the right there's a green box that represents a memory chip. And on the left, there's a -- a white box that represents the system memory controller on the host computer. 15:02:44

Do you see that --

A. Yes.

Q. -- Dr. Wedig?

A. Yes, I do. 15:02:53

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Q. And in Hiraishi, is it correct that S4 leveling is between the memory chip and the data buffer? Is that correct?

MR. LINDSAY: Objection. Leading, form.

THE WITNESS: That's correct. 15:03:08

Q. BY MR. CHANDLER: And S5 level, that's between the -- the data buffer and the system memory controller; is that correct?

MR. LINDSAY: Objection. Leading and form.

THE WITNESS: Yes, that's correct. 15:03:18

Q. BY MR. CHANDLER: All right. And then Exhibit 1070, what I've done there is I've just -- I've put on one page a number of the figures and paragraphs of Hiraishi that you discussed with counsel for Netlist.

So, for example, in the upper left of 15:03:36 Exhibit 1070 is a figure from page 98 of your declaration.

On the right side of Exhibit 1070 are the annotated figures 11 and 15 of Hiraishi that come from pages 124 and 125 of your declaration marked as 15:03:54 Exhibit 1003.

And then on the bottom left and bottom are paragraphs 147, 150, 151, 123 and 130 from the Hiraishi reference marked as Exhibit 1005.

Do you see that? 15:04:14

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A. Yes, I do.

Q. And then in Exhibit 1071, a similar exercise but with respect to right leveling.

So in the upper left of Exhibit 1071 is your annotation of Figure 5 of Hiraishi from page 98 of your expert declaration, marked as Exhibit 1003. 15:04:27

And then at the bottom are paragraphs 142, 143, 144, 145 and 146 from the Hiraishi reference marked as Exhibit 1005.

And then the upper right are figures 14A and 14B from Hiraishi, with the annotations from Exhibit 13, page 15. And then just colored in with the green and blue highlighting added there. 15:04:47

So do you see all of that in Exhibit 1071?

A. Yes, I do. 15:05:05

Q. So I want to follow up on questions about read leveling and write level.

In Hiraishi marked as 1005 -- and to the extent it's helpful for you, feel free to refer to Exhibit 1070 and 1071. But don't feel limited to those. You're welcome to look at Hiraishi directly or other parts of your expert declaration. Understood? 15:05:27

A. I understand.

Q. In Hiraishi Figure 5, do you see there's a reference to read leveling circuit 323 and write leveling 15:05:48

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circuit 322?

A. Yes, I do.

Q. Hiraishi performs read leveling and write leveling. To what extent is there a teaching of the read leveling circuit and the right leveling circuit interacting with the DQ signal and the DQS signals? 15:06:21

MR. LINDSAY: Objection. Form.

THE WITNESS: Well, there's a teaching that those signals, upon performing read leveling and write leveling, that the DQ and the DQS signals need to be delayed in order to allow the system to operate correctly. 15:06:46

Q. BY MR. CHANDLER: And in your opinion, do the read leveling and write leveling circuits taught by Hiraishi connect to the DQ lines and the DQS lines in the data buffer? 15:07:13

MR. LINDSAY: Objection. Form, outside the scope of cross.

THE WITNESS: Although they're not shown in Figure 5, the text makes it clear that there must be a connection between DQS and DQ to -- to the read and write leveling circuitry. 15:07:34

Q. BY MR. CHANDLER: So taking read leveling as an example --

A. Uh-huh. 15:08:03

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Q. -- what are some of the texts in the figures that, in your opinion, teach to a person of ordinary skill that the read leveling circuit in Figure 5 of Hiraishi would connect to the DQ and DQS lines, even if Figure 5 as a block diagram doesn't show that connection between the DQ and DQS lines in the read leveling circuit 323?

MR. LINDSAY: Objection. Outside of the cross-examination.

THE WITNESS: If you look at paragraph 151 from Hiraishi, it indicates that the read -- the read data DQ that comes from the memory chip is going to have a value -- is going to -- that's going to have data on it that will generate a time "A." "A" being the time from the read command until the data started to arrive.

And as it says in 151, it says that that time is measured for each of the memory chips stored in the data register control circuit 320 in the data register buffer 300.

And so it's necessary to measure at time "A." And the circuitry that's doing that is the control circuitry. And then the time "A" is stored in the control circuitry. And the only way to measure something is to have access to it.

So you have to have DQ and DQS connected to the

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control circuitry in order to allow that to operate correctly in order for this -- in order for this paragraph to make any sense.

Q. BY MR. CHANDLER: And what's the number for the control circuitry you've been referring to? 15:10:14

A. 320.

Q. And what does Figure 15 of Hiraishi depict?

A. It depicts a -- a read operation that is occurring in the normal course of usage. And it demonstrates that once the -- 15:10:41

Q. Let me pause -- let me pause you there.

MR. LINDSAY: You're going to interrupt your --

THE WITNESS: I'm sorry. I'm sorry. I'm sorry. Let me restate that.

I'm looking -- Figure 15 is -- the Figure 15 number is below the figure. Okay? So I misread it. Let me -- let me correct myself. 15:11:03

Figure 15 is the figure above the words that say, "Figure 15." And Figure 11 is actually above the words that say, "Figure 11." So let me start over. 15:11:21

Figure 15 demonstrates the two different times that you could see data coming in based on where the buffer is located on the -- on the memory module. And it shows the different time "A"s that you might encounter in -- when doing read -- read leveling. 15:11:47

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Q. BY MR. CHANDLER: How is Figure 15 of Hiraishi related to the read leveling?

A. So what it does is it demonstrates that -- it shows the releveling process. This is -- this is the actual releveling process for two different -- for two different memory -- memory devices and register buffers. 15:12:11

It shows what happens when you do the read leveling operation with a memory chip and memory buffer that are in one position versus the read leveling operation that occurs in a different position. And it shows how the time "A" can vary between the two, which -- you know, which then means that you need to vary your delay based on the length of the time "A." 15:12:36

Q. Does Figure 15 indicate that the read leveling circuit 323 within the data register control circuit 320 be connected to the DQ and DQS lines on the data path? 15:13:13

MR. LINDSAY: Objection. Outside the scope of cross-examination, form.

THE WITNESS: Yes. Figure 15 helps to support what I said earlier, that it shows that the DQ -- the DQS lines return from the memory chip to the data buffer at different times for different memory register buffer combinations. 15:13:36

And it shows that there are different lengths, different times A, which need to be measured, as it talks 15:14:00

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about in paragraph 151.

So Figure 15 demonstrates that it's the DQ and DQS lines that are used for generating the time "A." And so, therefore, it demonstrates that -- that those are the signal lines that need to attach -- need to communicate with, connect to, the data registered control circuit 320, specifically the read leveling logic, in order to be able to perform that calculation and then store that time "A" in the register leveling circuit. 15:14:20

Q. BY MR. CHANDLER: And then similarly for write leveling, what do Figures 14A and 14B teach with respect to whether or not the DQS line and the DQ line in the data path are connected to the data register control circuit 320, which includes the write leveling circuit 322? 15:14:43 15:15:06

MR. LINDSAY: Objection. Outside the scope of cross-examination and form.

THE WITNESS: Okay. So I now have turned to Exhibit 1071.

And so what -- what we're looking at here is that Figure 14A and 14B are demonstrating the right leveling operation. And it shows that the DQS signal is going to be -- is being provided to the memory chip. 15:15:19

The memory chip is then returning the -- the -- the result of that reading of the CLK line to the DQ 15:15:50

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signal. That DQ signal needs to be checked to see whether it's high or low. And so there is no indication of that in Figure 5.

But in reading the text from the Hiraishi patent, it's clear that it's necessary to check those signals. In particular -- let me find it in the text. 15:16:18

Okay. So looking at paragraph 144, it says in the example in Figure 14A they're showing a case at a logical level of the CLK signal at rising edge of the data strobe signal DQS is, quote, "high level," closed quote. In response to the logical level of the CLK signal. 15:16:48

And so it's going to operate -- there's actions that are going to occur in response to the logical level of the clock signal, which was provided on the DQ signal. 15:17:06

And so -- so it's necessary -- what this shows is that it's necessary for the DQ signal to be connected to the data register control circuit in order to be able to detect the logical level of the -- of the CLK signal that is being carried on the DQ signal. 15:17:35

And so this further reinforces that it's necessary to connect the DQ signal to the -- to the data register control circuit.

Q. BY MR. CHANDLER: And you're referring to the data register control circuit 320? 15:17:58

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A. That's correct, 320.

MR. LINDSAY: Leading.

Q. BY MR. CHANDLER: Could you pull up your declaration? And let me know when you have it.

A. Okay. I'll look at my paper copy, if you don't mind. 15:18:14

Q. Sure.

And I want to look at pages 82 and 83, where you've annotated Figures 1 and 7 of Hiraishi.

A. I'm sorry. Paragraph or page? 15:18:35

Q. Page. Page 82 and page 83.

A. Yes, I have it here.

Q. And the first thing I just want to talk about briefly is you've got this footnote 2 on the bottom of page 83 about -- about an issue. Can you just describe that issue briefly? 15:18:51

MR. LINDSAY: Objection. Outside the scope of cross-examination, leading.

THE WITNESS: Okay. So what's being talked about in the footnote is that the numbering system changes from one figure to the other, whereas -- whereas the figure on page 82, which is, I believe -- yeah, Figure 1 from Hiraishi shows numbering of the -- of the buffer -- of the buffer circuit to start -- go from 300-0, 300-1, 300-2, et cetera, from left to right. 15:19:09 15:19:40

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And, therefore, the buffer that is closest to the module control device would be 1 -- 0, 1, 2, 3 -- would be 300-4. Okay? So 4 is closest and then 0 is farthest.

When you look at the figure from Figure 7 on page 83, they've now renumbered it so that the buffer -- or the data register buffer is now renumbered to be -- 0 is closest and 4 is farthest. 15:20:10

So it's just a -- I think one of ordinary skill could easily figure that out by seeing all the connections. They just did a renumbering of how they're referring to the different -- the different register buffers and memory chips. 15:20:30

Q. BY MR. CHANDLER: Okay. So I'm going to ask you some questions about Figure 1 and 7, and potentially other figures. And when I ask the question and when you give the answer, I just want to make sure that we're both clear if there's a question about, for example, memory chip 200-0, that -- it's important that we clarify whether we're talking about the memory chip that's closest to the middle or whether we're referring to the memory chip that's furthest from the middle. 15:20:43 15:21:03

So understood what -- what clarifications that need to be made?

A. So just to be -- just to make it simple, do we 15:21:21

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want to focus on just one of the figures so that we're using consistent numbering?

Q. No, no. No. Because I think the numbers are hard to remember. What's easy for me to remember is close and far. That's generally what I'm going to be speaking about, is close and far. 15:21:37

A. Okay. Got it.

Q. But if you need to be more precise and put a number on it, that's fine. But just make sure --

A. Okay. 15:21:46

Q. -- you know, if you're putting a number on it, you're explaining whether it's the close version of 200-0 or the far version of 200-0. Understood?

A. Understood.

Q. All right. So counsel for Netlist, they asked you some questions about delays and fly-by delays. And there were a lot of questions about time T6. 15:21:59

A. Uh-huh.

Q. Do you remember questions and answers about time T6? 15:22:14

A. I do.

Q. And it was confusing to me, I'll be honest, the questions and the answers. So I want to get some clarification about that.

And the first thing I want to start with is if 15:22:22

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you look at Figure 1 of Hiraishi, what is the -- just describe in general, sort of, what the delay is or what the fly-by delay is with respect to the CLK signal and the read command.

What's the delay that's taking place? 15:22:41

A. Okay.

MR. LINDSAY: Objection. Form.

THE WITNESS: The delay that's taking place is the -- is the propagation delay or the time that it takes for the CLK signal and the read signal to travel from the 15:22:56 module control device for the center -- that's at the center to propagate to the left, to the farthest memory device and memory buffer, as going from the center to the left, and also for those same signals, CLK and read, and other signals also, but for them to propagate from the 15:23:26 center off to the right.

And the issue is that it takes time to go from the module control device along each of the different memory devices and memory buffers until it finally reaches the end. And that time is what we're calling the 15:23:48 fly-by delay. As it flies by, as it -- as it travels from the center to the left or the center to the right, it takes time for that and that's what we're trying to compensate for.

Q. BY MR. CHANDLER: Okay. And if you could look 15:24:05

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at Figures 11 and 15, which are reprinted on Exhibit 1070. But you can also find them directly in Hiraishi Exhibit 1005.

I want to follow up on the questions about time T6. So just let me know when you're oriented and ready to talk about that. 15:24:27

A. Okay. I'm ready.

Q. There were questions about T6 and outputting at the same time. And the big picture question I want to ask is if -- look at Hiraishi's memory module, as shown for example, in Figure 1. 15:24:55

Do all of the data buffers highlighted in blue output read data down to the memory controller all at exactly the same time?

A. As taught by Hiraishi, no. 15:25:22

Q. All right. Then -- and so it's a little confusing to me because there were questions answered about time T6 and it all happening at the same time.

A. Right.

Q. So I just want to get clarity as to what's time T6 if they're not all outputting at the same time? In other words, are there multiple -- are there multiple time T6s? And if so, how does that work? 15:25:39

MR. LINDSAY: Objection. Form.

THE WITNESS: Well, the problem is that -- as I 15:25:54

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said a few moments ago, you have these fly-by delays. And so it means that T6 occurs at a -- at a buffer module -- a buffer device at -- at an early time, when it's close to the center of the memory module. And T6 occurs at a later time, when it is at the buffer that is at the left end or the right end of the memory module.

So T6 does not occur at identically the same time across the entire module.

Q. BY MR. CHANDLER: Does each data buffer in Hiraishi during read operation output data at a different time T6, even though -- within each data buffer that's called time T6, does the time T6 vary from one data buffer to the next? 15:26:24 15:27:01

MR. LINDSAY: Objection. Form.

THE WITNESS: The exact instant of when T6 occurs, one data buffer to the next is different. Because T6 is being propagated from one buffer to the next. 15:27:27

So at a given instant of time, T6 is occurring at one -- at one data buffer. And then a little bit later, another T6 is occurring at the next data buffer. And a little short period of time, T6 is occurring at the next data buffer. 15:27:54

So T6 is not happening at the exact same instant of time across all data buffers. 15:28:13

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Q. BY MR. CHANDLER: And there were some questions and answers from counsel from Netlist about the system level CLK, which, again, was a little confusing to me, and so I just want to get clarity about that. It was in the same colloquy about time T6. 15:28:30

Let me -- let me just pause there and make sure you recall the colloquies about the system level CLK.

A. I remember the question was -- yeah, where was the system level CLK? Or what was -- was this the system level CLK? I remember that -- I remember that 15:28:48 discussion.

Q. And so my question is similar to the previous questions, which is when there was discussion about time T6 and the system level CLK.

A. Uh-huh. 15:29:06

Q. The ambiguity is that the system level CLK can be transmitted along different paths. And those paths can take time.

And so when you say "T6," it's a little unclear if you're talking about T6 at the system -- at the -- at 15:29:26 the host computer or whether it's T6 after the CLK has traveled a distance and you get a different T6 at each memory buffer.

So for clarity, when the questions and answers from counsel from Netlist were asking about the data 15:29:54

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buffers outputting at time T6 relative to the system CLK, did that mean that all the data buffers in Figure 1 of Hiraishi were all outputting read data at precisely the same time, or does each data buffer have a different time T6? 15:30:20

MR. LINDSAY: Objection. Form, leading.

THE WITNESS: Each data buffer outputs or performs the CLK T6 at a different time due to fly-by delays.

So when I said that there was a system CLK -- or when I agreed that there was a system CLK, there is a CLK that gets propagated from the center module control device down to both ends. 15:30:44

That -- that is the same CLK in the sense that it has the same frequency. But the exact time of when it reaches different devices is going to be different so that -- so that the system CLK that provides T6 is not happening at the exact same time on every device. 15:31:06

Q. BY MR. CHANDLER: Okay. I want to shift to a slightly different colloquy with counsel for Netlist, which was this notion of a CAS latency of five versus a CAS latency of six and whether there's always a one CLK cycle delay that's added by the -- the data buffer. 15:31:36

And so the first question for you is just, do you recall generally the colloquies about those issues? 15:32:01

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A. Yes, I do.

Q. So sticking with Figure 1 of Hiraishi, as shown, for example, on page 82 of your expert declaration marked as Exhibit 1003 --

A. Uh-huh. 15:32:17

Q. -- do you see that there are two rows of memory devices highlighted in green? There's one row that's sort of in the middle, and then there's a second row of memory devices towards the top of the memory module.

A. Yes, I see that. 15:32:34

Q. So when you have -- to take the example of a -- a read command that goes horizontally from the module control device in read out to the left and to the right to all these memory devices. I want to focus on two different memory devices, just to be concrete. 15:33:02

So let's take the memory device that's to the bottom left, closest to the center.

Have you got that one there? So the -- do you see which one I'm referring to?

A. I -- I believe so, yes. 15:33:34

Q. And then above it, there's another memory device that's sort of in the top row.

Do you see -- do you see that?

A. I see that, yes.

Q. Okay. So if -- let's imagine there's a read 15:33:52

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command that goes out horizontally, and the read command arrives at both -- both memory devices at the top and at the bottom. They are highlighted in green. Are you with me so far?

A. I am. 15:34:15

Q. And let's say that that read command reaches those memory devices at time T0. Are you with me so far?

A. Yes.

Q. And let's assume there's a CAS latency of 5, meaning that each memory device will output its read data 15:34:32 starting at time T5. Are you with me so far?

A. Yes.

Q. All right. When the bottom memory device outputs its data --

A. Uh-huh. 15:34:48

Q. -- down to the buffer circuit in blue, what is the difference -- the relative difference in time between when the data arrives at the buffer circuit from the lower memory device versus when a memory device in the upper row outputs its data? 15:35:17

So in other words, does a memory device at the top output data that arrived at the buffer circuit the same time as a memory device in the bottom when it outputs data, or will data arrive at the buffer circuit in blue at different times depending on how far away the 15:35:40

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memory device is?

MR. LINDSAY: Objection. Form.

THE WITNESS: Okay. So what will happen is both devices will -- both memory devices, the upper and the lower one, will output their data at the same time. 15:35:56

However, the upper device has a longer path to travel. So, therefore, the data will arrive at the data buffer from the lower device first because it has a shorter line to travel -- it has a shorter distance to travel. That will be followed sometime later by the data 15:36:23 from the upper device that has a longer distance to travel.

Q. BY MR. CHANDLER: And does Hiraishi teach that in any of the figures?

A. Yes. I think that that's part of -- that's also 15:36:50 part of the read leveling process, so that -- I think it teaches that also in 15, because that's also a type of fly-by delay.

Q. Okay. So sticking with Figure 1 of Hiraishi as shown, for example, on page 82 of your expert declaration 15:37:10 marked as Exhibit 1003, taking the example where you have a memory device in the top row that receives the read command at time 0 and it outputs read data at time T5, and then you indicate that there would be some delay between when the data's output from the memory device and 15:37:36

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when that data arrives at the data buffer circuit.

And I want you to assume that the amount of delay from the upper memory device down to the data buffer is half a CLK cycle, which means that the data buffer in blue receives the read data from that top memory device at time 5 and a half CLK cycles. Okay? Do you have that in mind? 15:38:04

A. Yes.

Q. And then I want you to assume that the bottom memory device, which is closer to the data buffer, it's going to get the read command again at time 0. It's going to output data again at time T5, because there's a CAS latency of 5, but it's closer to the data buffer, and so when it outputs its data at time T5, that data's going to arrive at the data buffer at time 5 and one quarter CLK cycles. Okay? 15:38:23 15:38:44

Do you understand the hypothetical?

A. I understand.

Q. So in this hypothetical, the memory device that's further away sends read data to the buffer circuit in blue, and that buffer circuit in blue get that read data at time 5.5, whereas the memory device that's closer sends data that's received by the buffer circuit at time 5.25; correct? 15:38:57

A. That's your hypothetical, yes. I understand 15:39:18

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that.

Q. All right. And then what does Hiraishi teach as to when the data buffer in blue is going to output the data? Does Hiraishi teach that the data buffer just adds a CLK cycle, and so if it receives data at 5.5, it's going to output it at 6.5, and if it receives data at 5.25, it's going to output data at 6.25 or not? What does Hiraishi teach? 15:39:32

MR. LINDSAY: Objection. Form, leading.

THE WITNESS: Okay. This is what I was trying to make clear with counsel for Netlist, that it does not simply add a CLK cycle. It adds the time necessary such that they all line up so that -- so that the data that arrived later is in alignment with the data that arrived earlier. 15:39:49 15:40:14

So for the data that arrived earlier, there is a delay, a longer delay, than for the data that arrived later. In the case of the example, it delays it until T6. But it does -- it inserts a necessary delay so that they both are output at the same time for that data buffer. Whereas, different data buffers may output at different times because their T6s are later. But they each output -- for a given data buffer, its output at the same time, regardless of when the data arrived, early or late. 15:40:36 15:41:00

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And it does that by inserting the necessary delays. It does not do it -- it does not delay for a fixed time period of only -- of it -- in your hypothetical, it does not delay it until 6.25 or 6.5. it delays it the time necessary so that it can output it at 6 in this example.

Q. BY MR. CHANDLER: So just to follow up on that, and following up on my hypothetical, where the memory device at the top row outputs its read data at time T5, that read data arrived at the buffer circuit at time T5.5. In that hypothetical, how much delay does the buffer circuit add in that examples.

A. In that example, it would add an additional .5 CLK delay for the -- for the upper circuit, and it would delay in the case of the lower circuit, which arrived at 5 -- at CLK 5.25, it would need to add another .75 CLKs in order to make them both outbound at time T6.

Q. Is there a figure in Hiraishi that teaches what you just explained just now?

A. Well, it's -- again, the read timing circuitry, Figure 15, shows the process of doing the measuring. Figure 11 shows the -- the -- the delay that's incorporated, the delay based on the length of A, what delay is necessary in order to be able to allow the data to be output in the -- at the appropriate time, in this

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case T6.

Q. Okay. Could you pull up the '608 patent marked as Exhibit 1001 and let me know you have it, or if you have it printed as a paper copy, that's fine as well, whichever you prefer. 15:43:32

A. Okay. I have an online copy.

I have it in front of me.

Q. All right. I want to follow up on the questions that you were asked by counsel for Netlist about the data path, and you pointed to column 3, line 58 or so. Maybe it's 59. 15:43:52

Can you direct us to where you were looking previously?

A. Yeah, the word "data path" occurred in line 59. The sentence starts back on line 54. I was looking in that general area. 15:44:29

Q. All right. So in the '608 patent marked as Exhibit 1001, column 3, starting at line 57, has a sentence that states: "Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the restrictive group of memory devices and the memory controller." 15:44:48

Did I read that accurately?

A. Yes, you did.

Q. Does the Hiraishi reference marked as 15:45:07

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Exhibit 1005 teach a buffer circuit associated with a respective group of memory devices in a data path between the respective group of memory devices and the memory controller?

A. Yes, it does. 15:45:22

Q. Does the Hiraishi reference marked as Exhibit 1005 teach that the buffer circuit includes a delay circuit configured to delay a signal through the data path?

MR. LINDSAY: Objection. Form. 15:46:12

THE WITNESS: You had a pause in that question. Can you ask it one more time, please?

Q. BY MR. CHANDLER: Does the Hiraishi reference marked as Exhibit 1005 teach that the buffer circuit includes a delay circuit configured to delay a signal 15:46:28 through the data path?

MR. LINDSAY: Objection. Form.

THE WITNESS: Yes, I believe it does.

Q. BY MR. CHANDLER: Could you turn to page 98 of your expert declaration marked as Exhibit 1003? 15:46:59

A. Okay.

Q. And let me know when you're there.

A. I'm there.

Q. So on page 98 of your expert declaration marked as Exhibit 1003, you have two annotations of Figure 5 of 15:47:17

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Hiraishi. The top annotation concerns the write direction. The bottom annotation concerns the -- I'm sorry. The top annotation concerns the read direction. The bottom annotation concerns the write direction; is that fair? 15:47:40

A. That's correct.

Q. And, again, on page 98 of your expert declaration marked as Exhibit 1003, there's a read leveling circuit and a write leveling circuit inside of data register control circuit 320 where Figure 5 does not 15:47:59 explicitly show any connection between the DQS line and DQ line of the data path being connected to the read leveling circuit and the write leveling circuit.

But for clarity, in your opinion, do the read leveling circuit and the write leveling circuit, as shown 15:48:29 on page 98 of your declaration marked as Exhibit 1003, connect to the DQS line and the DQ line of the data path?

MR. LINDSAY: Objection. Form, outside the scope of cross-examination.

THE WITNESS: As we spoke about earlier, they 15:48:51 necessarily have to in order to allow read leveling and write leveling to operate. They use information from the DQ and the DQS line in order to perform read leveling or write leveling for Hiraishi.

Q. BY MR. CHANDLER: And, again, what are some of 15:49:18

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the figures, other than Figure 5, that inform your opinions about that?

MR. LINDSAY: Objection. Outside the scope of cross-examination.

THE WITNESS: It would be Figure 15, which shows read leveling and how the time "A" is created that travels on the DQ line, and the DQS line showing when -- when that data is valid. And there's also Figure 14A and 14B, which shows the DQ line being -- providing a value, high or low, that is needed by the write leveling circuit to determine when the DQS signal has been aligned with the CLK. 15:49:29 15:50:04

Q. BY MR. CHANDLER: In Hiraishi, is the data register control circuit 320 in the data buffer that's on the data path? 15:51:04

A. Yes. It's most definitely -- most definitely in the data buffer. It is in the data buffer that's on the data path.

Q. In Hiraishi, is the DLL circuit 310 in the data buffer that's on the data path? 15:51:24

A. Yes. The DLL circuit is in the data buffer that's on the data path.

Q. Could you pull up the Butt reference? I want to follow up on some questions about that reference. Just let me know when you have it. 15:51:51

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A. Okay.

Q. And actually -- you know what, actually, it's also in your declaration, so that may just be easier. You already have your declaration in front of you, so, for example, it's -- you have some annotations of Butt Figures 2 and 3A around page 100 and 101. 15:52:05

Do you see those?

A. I see those, yes.

Q. All right. So focusing on Figure 2 of the Butt reference marked as Exhibit 1029, which you've annotated on page 100 of your expert declaration marked as Exhibit 1003. 15:52:32

A. Uh-huh.

Q. Do you have that in front of you?

A. Yes, I do. 15:52:47

Q. Okay. Does the Butt reference marked as Exhibit 1029 teach delaying the data? So not just changing the timing of the DQS strobe signal to center it, but does the Butt reference teach delaying the data? And if so, where? 15:53:19

MR. LINDSAY: Objection. Form.

THE WITNESS: Yes, it does teach it. It shows it in the asynchronous FIFO, so the -- the signals come out from the physical data path 114 and then go into the asynchronous FIFO 113, and as it travels through the 15:53:40

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FIFO, that causes a delay.

Q. BY MR. CHANDLER: Could you pull up the claim language from the '608 patent, so you can either look at the beginning of -- sorry -- the end of your declaration or the patent itself, either one. And just let me know when you've read it. 15:54:13

A. I have it in front of me.

Q. There were some questions that counsel for Netlist asked you about JEDEC standards. Do you recall those? 15:54:27

A. Yes, I do.

Q. Do any of the claims of the '608 patent limit the claimed memory module to any particular physical dimensions as set forth in any particular JEDEC specification? 15:54:50

A. No. There's no mention of JEDEC in the claims. There's no limitations for -- for size as described in the claims.

Q. Does JEDEC permit memory modules that are larger than the most popular standardized sizes for memory modules? Or does JEDEC -- or does JEDEC somehow prohibit the industry from ever making a memory module that's outside of the physical dimensions of a particular JEDEC specification? 15:55:26

MR. LINDSAY: Objection. Form. 15:55:53

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THE WITNESS: Well, there's a lot of different JEDEC standards. There's standards -- I mean, the JEDEC standard for a DDR3 SDRAM. There are standards for physical size, but there are multiple standards for multiple physical sizes. So there is no one JEDEC physical size standard. I mean, I can't name them all to you, but there are multiple different standard sizes. There is not just one. 15:56:16

MR. CHANDLER: Okay. I pass the witness. 15:56:40

FURTHER EXAMINATION

BY MR. LINDSAY:

Q. Dr. Wedig, did you discuss your testimony today with counsel after I concluded my questions earlier?

MR. CHANDLER: Objection. Form. 15:56:56

THE WITNESS: Yes, I did.

Q. BY MR. LINDSAY: And about how long did you discuss your testimony with counsel?

A. Basically the time from shortly after you stopped asking questions until we came back on. 15:57:13

Q. Right. And about how long was that?

A. I don't know. I didn't time it.

Q. And to be clear, this discussion included the substance of your testimony earlier today?

MR. CHANDLER: Objection. Work product. So I 15:57:41

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direct the witness not to answer.

THE WITNESS: All right. I will not answer it.

MR. LINDSAY: Okay. So the standard is whether substance of the testimony was discussed, and I'm asking whether substance of his testimony was discussed. That's not getting to what was discussed. 15:57:59

MR. CHANDLER: I disagree with the distinction you're trying to draw. So my objection is the same, and I would again direct the witness not to answer.

THE WITNESS: I will not answer that. 15:58:20

Q. BY MR. LINDSAY: So looking at Hiraishi Figure 5, we talked about the system CLK CK earlier today. Where does that come from?

MR. CHANDLER: Objection. Form.

THE WITNESS: That comes from the module controller that is found in the center of the memory module. 15:59:09

Q. BY MR. LINDSAY: Okay. And Hiraishi has a number of timing diagrams that have along the top CK and then T -- various T values; right? So Figure 11, Figure 12, so on. 15:59:39

A. Yes, that's correct.

Q. Is that referring to that system CLK that the module controller is sending out?

MR. CHANDLER: Objection. Form. 15:59:57

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THE WITNESS: It's referring to the CLK that is at the input of the particular module that it's referring to in the diagram, so it is output by the system controller. It reaches each of the different modules, and when you see CLK (IN), that's the CLK at the time that it's at that particular module. 16:00:25

Q. BY MR. LINDSAY: Okay. When you say module --

A. I'm sorry. That's imprecise. If I can clarify.

The particular component or the particular logic that is being described in the timing diagrams below it, so if I can give an example, and if you go to Figure 11, you'll see the word "connector." That would be the CLK (IN) at the connector. And then anything below that you'll see command address control register buffer. That's what I've been calling the controller buffer. The CLK (IN) is the CLK signal at the time it enters that particular component, et cetera. 16:00:54 16:01:18

Q. Okay. And then in Figure 15, if you want to take a look at that.

A. Okay. I'm there. 16:01:42

Q. And the top is the command address control register buffer timing -- signal timing; right? And that's what we were calling the module controller?

A. Yes, that's correct.

Q. And the CK (OUT) is then the CLK that it's 16:02:03

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providing to the memory chips and the various data buffers?

A. That's correct.

MR. CHANDLER: Object to form.

Q. BY MR. LINDSAY: At the bottom of Figure 15, there's two time "A"s. 16:02:21

Do you see that?

A. Yes, I see that.

Q. The top time "A" is from memory chip 200-0 to data register buffer 300-0; right? 16:02:38

A. That's what it says, yes.

Q. And below that it says that it's the time "A" for memory chip 200-19 to data register buffer 300-4; is that right?

A. That's what -- that's what the words say. 16:03:01

Q. So those time "A"s are comparing signal timing for different memory chips going to different data buffers?

A. That's correct.

Q. And the system CLK CK (IN) is the same for memory chip 200 A and memory chip 200-19? 16:03:19

MR. CHANDLER: Objection. Form. And you said 200 A. I think you meant 200-0. Why don't you ask the question again. I'll still object to it, but I'll let you have your question correct. 16:04:01

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MR. LINDSAY: Sure.

THE WITNESS: I'm sorry. Do you want to ask the question again?

Q. BY MR. LINDSAY: Yes. I will.

So the system CLK CK in Figure 15 that we were just looking at -- 16:04:08

A. Uh-huh.

Q. -- at the bottom of 15, it's laying over the two time "A"s.

Do you see that? 16:04:30

A. Yes.

Q. That system CLK, that's the same for both those time "A" measurements?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah. They start -- they both have the same start time. T0 lines up, yes. 16:04:45

Q. BY MR. LINDSAY: And those are -- those are for different memory chips and different data register buffers? That --

A. That's correct. I'm sorry. 16:05:00

That's correct.

Q. Take a look at the '608 patent. Mr. Chandler asked you about a sentence in column 3. Do you remember that?

A. Yes. I have it here. 16:05:27

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Q. Where in the sentence that he asked you about does it say anything about strobe signals?

A. It doesn't -- it doesn't say the word "strobe signals." It refers to data paths. One of ordinary skill would understand that data paths include strobe signals, so though it doesn't say data paths, that is included in the word "data path." 16:06:09

Also it says, "each buffer circuit," and the buffer circuit which it is describing also includes strobe signals. 16:06:34

Q. So the sentence doesn't provide direct support for the idea that strobe signals are part of a data path or are transmitted on a data path, does it?

A. Well, the support is in the wording of the word "buffer circuit," and the patent makes clear what the buffer circuit is. It's the -- you know, it's the buffer -- the buffer component, the memory buffer, and that includes strobe signals. So it does not use the word "strobes," but I understand it to include strobes based on the wording of the sentence. 16:07:15 16:07:38

Q. Are CLK signals part of the data path.

A. CLK signals drive the data path. I mean, they contribute to it. They are -- they're needed by the data point.

Q. But they're not part of the data path? 16:08:01

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MR. CHANDLER: Object to form.

THE WITNESS: The term "data path" is a very broad term, so I think it's debatable. I mean, data path is whatever is necessary to help transfer data. So I -- you could argue that a CLK is included in the data path because it's needed. But this -- I think this sentence here makes it clear that in the '608 patent, they believe that the buffer circuit is in the data path, and, therefore, from the '608 patent, whatever is in the buffer circuit is part of the data path by their definition. 16:08:29 16:08:55

Q. BY MR. LINDSAY: Would you agree that the term "data path" can have different meanings in different patents and different references?

A. Well, of course. I mean, some patents may specifically define it to mean different things, but I think one of ordinary skill in the art has a general understanding of data path, but it's a broad term. 16:09:10

Q. And if a particular reference defined data path to include CLK signals, for example, then that would be -- then that would be the way you would interpret data path to include CLK signals in that reference because it described it that way; right? 16:09:29

A. Obviously. You've got to look to the specification to understand the terms. So if that is 16:09:48

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their particular definition for it, then I would obviously use that in order to help come up with my definition for data path.

Q. And if a patent excluded strobe signals from a data path -- 16:10:09

A. Uh-huh.

Q. -- then would you also agree that in that case you should understand the term "data path" is not including strobe signals?

A. If it -- if it actually says exclusively that you are to exclude strobe signals from the data path, then of course I would exclude it because of that specialized definition. 16:10:21

Q. And going back to this paragraph -- or sorry -- this sentence that we were talking about, so the buffer circuit is in the data path, is the way you understand this sentence; right? 16:10:48

A. That's what the words say.

Q. So is it the case that any signals into or out of the buffer circuit are part of the data path? Is that your understanding? 16:11:06

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah. I'm reading it just like you are. It appears as though -- it appears as -- that anything associated with the buffer circuit, it seems to 16:11:22

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me that -- yes, I agree with you. If a signal's associated with a buffer circuit, then it's part of the data path, according to this sentence.

Q. BY MR. LINDSAY: So in -- if we go over to Hiraishi and we look at their buffer circuit 5 -- Figure 5, there's a -- there's the system CLK signal that we talked about that's going into the data buffer in Hiraishi. 16:11:45

A. Uh-huh.

Q. Is it your opinion, then, that based on that sentence in the '608 patent, that the CLK signal CK is part of the data path or is on the data path? 16:12:07

A. I think you can make an argument for that. I mean, it's necessary in order to help transfer the data, so... 16:12:40

Q. Well, you've included strobe signals --

A. Uh-huh.

Q. -- on the data path because they're necessary to transmit the data and they're received by the data buffer, which is on the data path; right? 16:12:50

A. Yes, it is.

Q. Okay. And then the CLK signal is also received by the data buffer.

A. Uh-huh.

Q. It's necessary to transmit the data. Isn't it 16:12:59

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then, under that reasoning, also part of the data path?

A. It would seem like it, yes.

Q. And then how about the DRC signal that's at the top of Figure 5 that's received by the data buffer, what does that consist of? What's your understanding of what that consists of? 16:13:28

A. Well, that would be the read/write signals for indicating what operation to perform. It would also be pretty much any command for instructing the data buffer to do an operation, such as when to perform write leveling and read leveling, when to set mode registers, et cetera, so it's all the command signals to the data buffer. 16:13:45

Q. Are command signals needed in order to transfer transmit data? 16:14:05

A. Of course.

Q. So under your reasoning as to why the DQS value is on the data path, wouldn't the command signals carried in DRC going into the data buffer also be part of the data path or on the data path? 16:14:27

A. You know, if you were to take this reasoning to the extreme, you would -- you would have to argue that the entire computer system would be in the data path, because everything depends on everything, so you have to draw some limits to it. 16:14:49

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And I don't really have an opinion as to whether DRC is on the data path or not, because it's really outside of my opinion, and it's really not relevant for -- for the claims that I analyzed.

I mean, I do refer to the DRC, in that it has certain functions in order to help facilitate the operation of the -- the operation of the buffer, but I don't really take a position as to whether it's on the data path or not. 16:15:06

Q. Right. But you've applied a certain understanding of the term "data path" to include any signal going into the data buffer that is necessary to transmit data, and -- is that correct? Correct me if I'm wrong. Is that accurate? 16:15:25

A. I'm -- I'm reading the patent usage of the word "data path," and it says that it's -- the buffer circuit is in the data path, so I'm trying to read that -- use that information in order to help to understand how the patent wants to use the word "data path." 16:15:50

So it's -- you know, the data path clearly relates to transmitting data. That's -- that is the wording. That's what the word says, data path, the path of the data. Beyond that, there's -- you know, what is actually included and what is not, it depends on the -- you know, how you use it. 16:16:20 16:16:42

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And as I said, I gave -- I gave the components earlier today as to what I thought was the relevant parts of the data path for my interpretation of the claims. If there's more, there may be more, but it's not -- it's not important for my interpretation of the claims and finding whether they -- whether the claims are made obvious or not. 16:17:04

Q. Okay. That's fair enough.

If a -- if a patent -- if the '608 patent is ultimately interpreted as not including strobe signals on the data path -- 16:17:24

A. Okay.

Q. -- would you agree that Hiraishi does not anticipate or render obvious the claims of the '608 patent? 16:17:47

A. Absolutely not.

Q. I understand you disagree with what data path --

A. Right. But --

Q. -- means, but if ultimately it's not inclusive of the strobe signals -- 16:18:00

A. Uh-huh.

Q. -- would Hiraishi then not satisfy all the claim limitations?

A. There's a lot of nots in there. I'll say it in a positive way, that even without the strobe signals, I 16:18:16

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believe that Hiraishi makes obvious the claims, at least Claims 1 to 5, of the '608 patent.

Q. Is the Hiraishi reference -- do you understand the reference is describing a DDR3 architecture?

A. I am not understanding it to be limited to DDR3. I believe it is -- it is discussing a technology that would have been available in the time frame of DDR3. I don't believe it's limited to DDR3. 16:18:52

Q. Right. So you could implement Hiraishi's teachings in a -- a nonDDR3-compliant module, is what you're saying? 16:19:18

A. Yes.

Q. Could you also implement it in a DDR3-compliant module?

A. I believe so, yes. 16:19:35

Q. Give me one second.

A. Okay.

MR. LINDSAY: No more questions.

MR. CHANDLER: Thank you.

And so for the court reporter, again, we'd like the final transcript by Tuesday, March 19th, so we can have an opportunity to review and make any corrections as appropriate. And I would also like the rough transcript. 16:20:47

THE REPORTER: Thank you, Counsel. 16:21:02

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Off the record?

MR. CHANDLER: Sure.

(Time noted: 4:22 p.m.)

--oOo--

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I declare under the penalty of perjury under the laws of the State of California that the foregoing is true and correct.

Executed on _____, 2024, at _____, _____.

_____

ROBERT G. WEDIG, PH.D.

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STATE OF CALIFORNIA) ss:
COUNTY OF MARIN)

I, LESLIE ROCKWOOD ROSAS, RPR, CSR NO. 3462, do hereby certify:

That the foregoing deposition testimony was taken before me at the time and place therein set forth and at which time the witness was administered the oath;

That testimony of the witness and all objections made by counsel at the time of the examination were recorded stenographically by me, and were thereafter transcribed under my direction and supervision, and that the foregoing pages contain a full, true and accurate record of all proceedings and testimony to the best of my skill and ability.

I further certify that I am neither counsel for any party to said action, nor am I related to any party to said action, nor am I in any way interested in the outcome thereof.

IN WITNESS WHEREOF, I have subscribed my name this 18th day of March, 2024.

LESLIE ROCKWOOD ROSAS, RPR, CSR NO. 3462

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THEODORE W. CHANDLER, ESQ.

ted.chandler@bakerbotts.com

March 18, 2024

RE: SAMSUNG ELECTRONICS CO. vs. NETLIST, INC.

March 12, 2024-ROBERT G. WEDIG, PH.D.-JOB NO.6584925

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ROBERT G. WEDIG, PH.D.-JOB NO.6584925

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

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