A 20-mA-Receive, 55-mA-Transmit, Single-Chip GSM Transceiver in 0.25-μm CMOS

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***Abstract*— This paper presents a low-power 900-MHz GSM transceiver developed in a 0.25-μm CMOS technology. The superhet receiver, with a single intermediate frequency at 71 MHz, has an overall worst case noise figure of 8.1 dB, including all filters. The overall gain can be digitally controlled over 98-dB range. The receiver consumes only 19.5 mA from the 2.5-V voltage supply while achieving the required blocking and intermodulation performance. The direct conversion transmitter has a fully integrated phase shifter and provides a 2-mW signal to the power amplifier with a low level of spurious emissions. The transmitted Gaussian minimum shift keying signal has an rms average phase error $<2^\circ$, and the overall current consumption of the transmitter is 55 mA.**

***Index Terms*— Analog RF-CMOS, direct-conversion transmitter, GSM, mobile communications, superheterodyne receiver, transceiver.**

I. Introduction

PROGRESS in the last five years in radio-frequency (RF) CMOS research [1]–[8] has shifted the debate from whether CMOS is capable of realizing RF circuits at the low gigahertz range to for what kind of applications it is suitable. It has gradually become widely accepted that applications such as wireless local-area networks and cordless telephony, where the radio environment is better defined and the portable transceiver is confined to within a smaller radius from both the base stations and the battery charger, are well suited for CMOS implementation at the radio frequencies. A high degree of integration has also come to be expected.

Considerable doubt has remained up to now, however, over whether high-end transceivers for narrow-band cellular applications could be realized with even the best CMOS technologies available today [9], [10]. The combination of much greater cell sizes and the absence of geographical restriction for the mobile terminal results in higher dynamic range on the one hand and more stringent power consumption requirements on the other. The dynamic range problem is characterized by very weak signals in the desired channels in the presence of very strong interfering signals from both adjacent radio channels within the same cellular service and those from other public radio services, such as TV broadcast and radar. The power consumption requirements stem from the fact that the user is usually far removed from his battery charger but nonetheless expects long talk- and especially standby-time from his handset, which at the same time must be physically small and lightweight. The intrinsically higher g_m/I (transconductance to bias current) ratio of bipolar transistors has made them the prevailing choice for the realization of today's commercial cellular RF transceivers. Typical power consumption for such transceivers is 50 mA at 3 V [11]–[13], which is half of the average CMOS transceivers at similar frequencies [2], [5]. With the advances of low-power design for digital VLSI and the steadily improving feature size of deep submicrometer CMOS, the power consumption of the digital portions of a mobile terminal is becoming increasingly insignificant compared to that of the RF transceiver. This increases the pressure for RF transceivers realized in bipolar junction transistor (BJT) technologies to further reduce power consumption, to satisfy demands for longer standby times. For CMOS realization of RF transceivers for cellular applications, the primary challenges are therefore twofold. The first is meeting the requirements of narrow-band cellular applications such as GSM, as typified by various type-approval test requirements. Moreover, low power consumption at or below the level of current BJT transceivers must be reached before CMOS can be considered competitive to BJT technologies. An additional constraint is manufacturability at low cost, which precludes circuit techniques that enhance individual performance parameters at the expense of substantially increasing their sensitivities to manufacturing tolerances and typical variations of operating conditions such as power-supply voltage and temperature. With the above requirements as the background, this paper reports the realization of a very low-power CMOS transceiver that satisfies the stringent requirements of the GSM cellular telephony standard.

This paper is organized as follows. In Section II, the specifications for the RF transceiver and the chosen architecture are presented. Sections III and IV discuss the design of the receiver and the achieved performance, respectively. Section V describes the design of the transmitter, while in Section VI, the corresponding measurement results are presented. The final conclusions are presented in Section VII.

II. Transceiver Specifications

The main task of the RF receiver is to select the wanted channel, amplify the RF signal to a convenient level, demodulate the information, and provide it to the baseband processor with sufficient signal-to-noise ratio (SNR) for digital detection, while rejecting all interfering signals. This translates into requirements in terms of dynamic range, sensitivity, blocking, and intermodulation performance. The transmitter, on the other hand, must modulate the baseband signal to the RF frequen-

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cies. It must minimize the generation of spurious signals, and supply the RF signal, with a defined power level, to an external power amplifier (PA) for final amplification. As in most digital wireless applications, GSM-type approval requirements are specified for the complete system. The specifications for the RF transceiver of a small mobile station (MS) must therefore be derived from the system specifications.

A. Receiver Requirements

- *Sensitivity:* for an additive white Gaussian noise channel condition, a bit error rate (BER) $<10^{-4}$ must be achieved for a -102-dBm reference input signal. The achievable BER depends on the chosen GMSK detector type. To achieve 10^{-4} BER, a suboptimal MSK-type detector needs 10-dB SNR [14]. This detector is sometimes preferred since, being simpler, it requires less silicon area and power. Furthermore, in realistic channel conditions, its performance is similar to an optimal maximum likelihood sequence estimation implementation. On the other hand, the noise floor of -121 dBm in a 200-kHz channel is 19 dB below the reference input of -102 dBm. Since the noise introduced by a well-designed voltage-controlled oscillator is negligible for our receiver architecture, the degradation in SNR is solely given by the noise introduced by the blocks in the receiver chain. Therefore, to satisfy the specifications for a MSK detector, a maximum noise figure (NF) of 9 dB, referred to the antenna input, is required.
- *Dynamic range:* the receiver must be able to detect signals up to -15 dBm. Considering that the reference sensitivity is specified for a -102-dBm input signal, 87-dB dynamic range is required to avoid the saturation of the baseband analog-to-digital (A/D) converters (which follow the RF front end). To account for component tolerances, as well as temperature and process parameter variations, a margin of 13 dB is added, so that a total of 100 dB results.
- *Blocking performance:* the cellular radio network environment is usually described as "hostile" partly because of the high-level interfering signals. Interferers outside the GSM receive band (935–960 MHz), such as ultra-high-frequency TV, which transmits with power levels as high as 50–100 kW in the 500–800-MHz band, must be rejected. To account for the near–far situation typical in cellular communication networks, minimum blocking performance is specified in GSM-type approval requirements. For a small MS, a -99-dBm reference signal must be demodulated with a BER $< 10^{-3}$, in the presence of in-band and out-of-band blocking signals, the power level of which depends on their frequency offset from the wanted channel frequency, as summarized in Fig. 1. For the active circuits in the receiver, the blocking specifications translate into compression point (CP) requirements.
- *Intermodulation performance:* similar to blocking signals, interfering signals in adjacent channels also degrade signal quality through intermodulation. In this case, intermodulation products produced by receiver nonlinearities may fall in the wanted channel, thereby decreasing the SNR. For a small MS, it is specified that a -99-dBm reference signal must be correctly demodulated (BER $< 10^{-3}$) in the presence of two -49-dBm signals, 800 kHz and 1.6 MHz away, respectively, from the desired channel. Since in our implementation the worst distortion is caused by the third-order intermodulation product, a specification for the third-order intercept point (IP3) for the various active blocks is sufficient. The required overall IP3 at the receiver input is -14.5 dBm, which can be derived using the graphical method shown in Fig. 2, where the required SNR is 10 dB, the signal output grows with a slope of one with the power of desired input, and the intermodulation product (-49 dBm $+ 3$ dBm $= -46$ dBm) grows with a slope of three with the power of interfering signals.

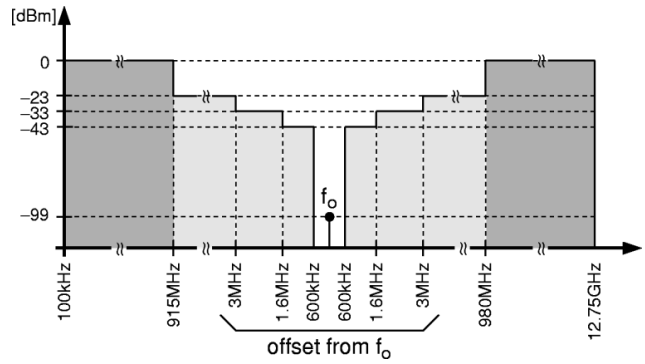

Fig. 1. Power level of blocking signals to be rejected.

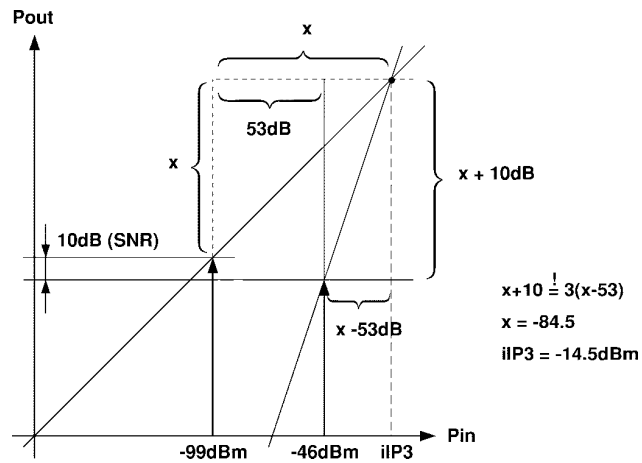

Fig. 2. Derivation of overall iIP3.

B. Transmitter Requirements

- *Spurious emissions:* to avoid the disruption of the communication between the base station and other MS or that of other radio systems, the spurious emissions from a GSM transmitter must be minimized. Stringent requirements are especially dictated by the GMSK modulation mask and by the maximum permitted emissions in the GSM receive band. The maximum permitted emissions

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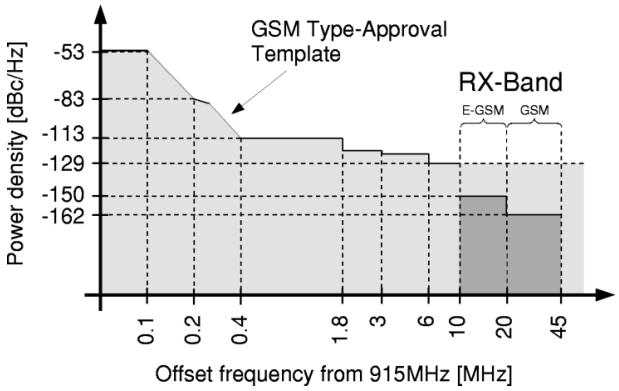

Fig. 3. Worst case unwanted emissions (915 MHz).

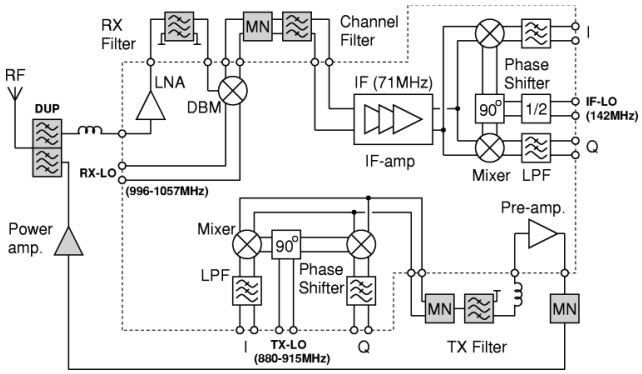

Fig. 4. GSM transceiver block diagram.

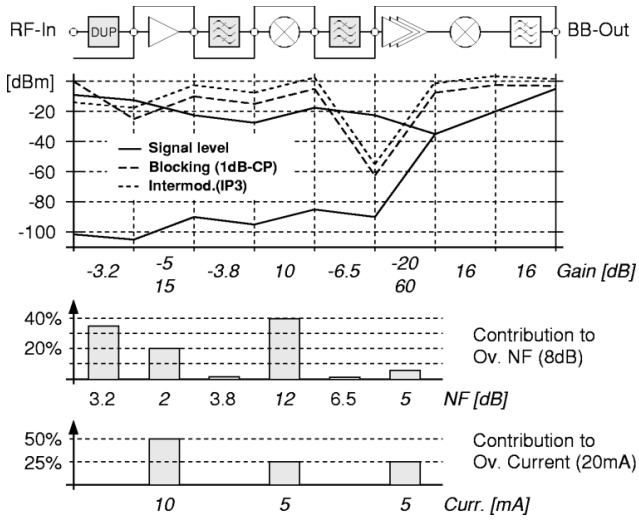

Fig. 5. Receiver planning.

in power density (dBc/Hz) for the worst case condition, where the transmitting channel is at maximum power and placed at the right corner of the GSM transmit band (915 MHz), is shown in Fig. 3. Wide-band noise 6 MHz offset from the channel must be less than −129 dBc/Hz, while the maximum noise in the E-GSM and GSM receiver band is −150 and −162 dBc/Hz, respectively.

- *Phase accuracy:* for any transmitted 148-bit pseudorandom sequence, the limits for an rms average and peak phase errors are 5° and 20°, respectively. The phase error or error vector magnitude (EVM) arises from the combination of all the spurious signals that are present in the transmitted signal and that are generated during the modulation process.
- *Output power:* typical commercial GSM class 4 (2 W) power amplifiers [15] provide 30-dB programmable gain external to the transmitter IC. To drive such power amplifiers, the transmitter IC must be able to deliver 2-mW output power.

C. Transceiver Architecture

The complete transceiver block diagram is shown in Fig. 4. External components are shown in gray while the integrated blocks are white. For the receive section, a superheterodyne architecture is used with a 71-MHz intermediate frequency (IF). Considering the overall requirements and the CMOS technology used, this architecture provides a good tradeoff in terms of achievable performance and needed power.

Direct up-conversion architecture is used for the transmitter. Main advantages in this case are the intrinsic low level of unwanted emissions in the absence of intermediate frequencies and the high integration level. Since the local oscillator is at the same frequency as the transmitted signal, one drawback of this architecture is the risk of local oscillator pulling. This problem will be solved using an offset local oscillator in the frequency synthesizer.

III. Receiver

Our optimization of the receiver plan is shown in Fig. 5, where the requirements for each block in the receiver chain are described. On the top graph, the requirements in terms of gain, CP, and IP3 are shown. In the middle, the required NF for each block as well as their percentage contribution to the overall NF are shown. To allow some margin, a worst case NF of 8 dB has been planned. In the bottom graph, the requirements in terms of current consumption are also displayed. An overall current consumption of 20 mA is aimed at.

At the input, a filter (the duplexer [16]) is used to suppress the out-of-band blocking signals that can be as strong as 0 dBm. Thanks to the suppression of interference by the filter, the required linearity, and therefore the low-noise amplifier (LNA) power consumption needed, is reduced. On the other hand, the filter has an insertion loss of 3.2 dB, which is responsible for as much as 35% of the overall noise, leaving only a tight NF budget of 4.8 dB to the rest of the receiver. For the LNA, 2-dB NF and 15-dB gain are specified. Although a higher gain would relax the NF requirements of the following circuit blocks, high current would be required in the LNA as well as in the mixer to achieve the needed gain and linearity and to drive the RF interstage filter [16] that is required in front of the mixer to suppress the image frequency. This filter, together with the duplexer, provides a minimum image suppression of 70 dB. For the mixer, similar considerations hold in terms of gain and linearity. As shown in the figure, with 12-dB single-sideband (SSB) NF, the mixer will be the

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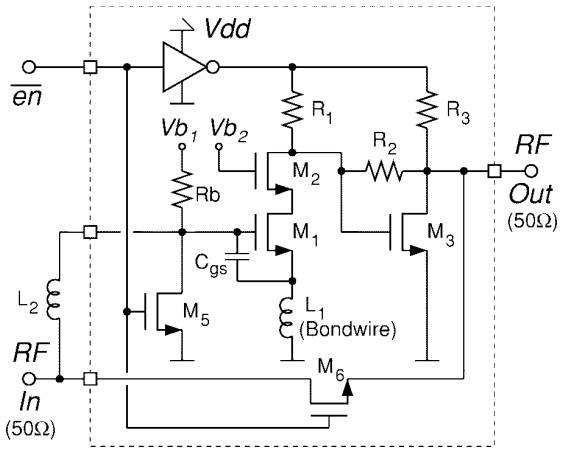

Fig. 6. Schematic of the LNA.

major contributor to the overall NF, followed by the duplexer and the LNA.

The required 100-dB variable gain is achieved with 20 dB in the switchable LNA and 80 dB in the 71-MHz IF amplifier. The IF amplifier is one of the most challenging blocks in the receiver. It must have high gain of up to 60 dB at a relatively high frequency of 71 MHz. It must be programmable in accurate 2-dB steps as specified by the interface with the baseband chip. Moreover, since a low-cost 71-MHz IF filter [16] does not suppress undesired channels completely, the IF amp must also possess a very high output linearity. All this must also be achieved without incurring excessive power consumption. At the IF-amp output, the wanted channel is regulated to a constant −35-dBm level. To achieve the wanted −2 dBm at the A/D converter input, 16-dB gain has been assigned to the quadrature demodulator, as well as the baseband low-pass filters (LPF). Since only 32-dB gain are assigned to baseband, potential problems such as dc-offset and flicker noise contribution are avoided. One last important requirement for all the blocks interfacing an external filter is that their input and output impedances must match to the characteristic impedance of the filters, to maintain the filters' designed transfer characteristics. The matching impedance for the RF filters is 50 Ω, while the IF filter must be terminated with 330 Ω.

The individual circuits in the receiver will be presented next. The focus is on the RF mixer, while the LNA and the IF strip, which are discussed in more detail elsewhere [18], [19], will only be briefly described.

A. Low-Noise Amplifier

The LNA schematic is shown in Fig. 6. Signal $\overline{en}$ is used to select the wanted gain.

If $\overline{en}$ is set to ground, the LNA is active and 15-dB amplification is obtained. To achieve the required performance without incurring excessive power consumption, a two-stage implementation has been chosen. To realize 2-dB NF as well as 50-Ω input impedance matching, the input stage has been designed using an inductively degenerated common-source configuration. Cascode transistor M_2 helps to reduce the parasitic influence of the Miller capacitance of M_1 and to increase reverse isolation. To guarantee broadband output impedance matching as well as high output linearity, a transimpedance configuration for the output stage has been used.

In the case of strong input signals, $\overline{en}$ is set to $V_{\rm dd}$. The LNA is switched off and bypassed using transistor M_6. Device M_6 is dimensioned to realize the 5-dB attenuation at the output for a 50-Ω load, and transistor M_5 is used to zero the Q of the network formed by L_1, L_2, and the gate capacitance of M_1.

B. RF Mixer

To reduce the relative importance of the noise introduced by the IF filter and the IF amplifier, 10-dB gain is required in the mixer. To handle in-band blocking as well as intermodulating signals, the mixer also needs to achieve more than −12 dBm of iCP and more than −3 dBm of iIP3. Good linearity is also necessary to minimize an in-band spurious response at 960.5 MHz caused by the second harmonics of the local oscillator (996 MHz for 925-MHz desired signal) and the interferer itself, which appears because of the 71-MHz IF. Moreover, 50-Ω input impedance and 12-dB SSB NF are required. The only active mixer configuration that can achieve such specifications at GSM frequencies is the Gilbert mixer. Since the RF-image filter is single ended, a single-ended input with embedded impedance matching is also desirable. A single balanced mixer (SBM) with common gate input can be used [18], which, in turn, requires the input transistor to have a g_m of 20 mS to achieve impedance matching. In an SBM, the attenuation introduced by the switches is at least $1/\pi$ so that the maximum conversion gain $(g_{\rm mc})$ is 6.8 mS. Although a mixer NF around 10–13 dB can be realized with such an implementation, to achieve the required 10-dB voltage gain as well as the right impedance matching to the IF filter, a load impedance above 5 kΩ and a Q ≈ 4 in the output LC-matching network is needed. The latter values have been considered too high for our implementation since it involves too high a swing at the output as well as a higher mismatch in the output impedance in case of deviation of the LC components from the nominal values. On the other hand, a double balanced mixer (DBM) with two input transistors can be used in common gate configuration, each having a g_m of 40 mS [18]. The advantage of such a structure is a lower attenuation $(2/\pi)$ in the switches, which translates into the doubling of $g_{\rm mc}$ (12.7 mS) and the halving of the Q in the output matching network. The main disadvantage is the differential input, which requires a single-ended to differential converter to interface with the RF filter. This means one more external balun, or, if the balun is integrated, a degradation in the overall mixer performance. To solve this problem, a single-ended input, double balanced mixer, derived from the BJT Micromixer [20] as shown in Fig. 7, has been implemented [21]. Single-ended to differential conversion is now achieved in the input stage of the mixer. Wide-band input impedance matching is performed by setting the g_m of M_1 to 20 mS. To maintain symmetry, the g_m of M_3 is also set to 20 mS. The resulting structure exploits class-AB operation, so that the mixer will not compress. A $g_{\rm mc}$ of about 9 mS assuming nonperfect switching devices as well as an NF of about 10–13

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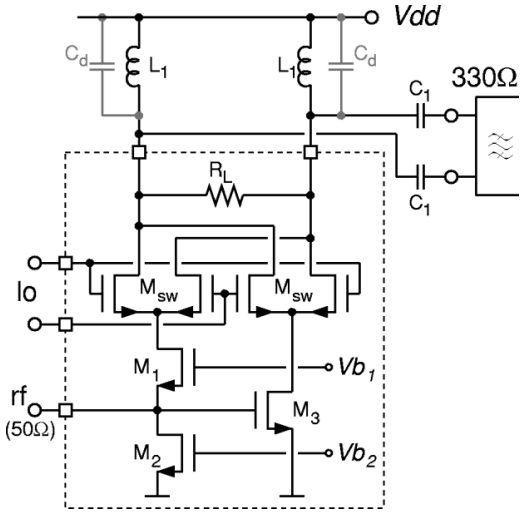

Fig. 7. Schematic of the single-ended input DBM.

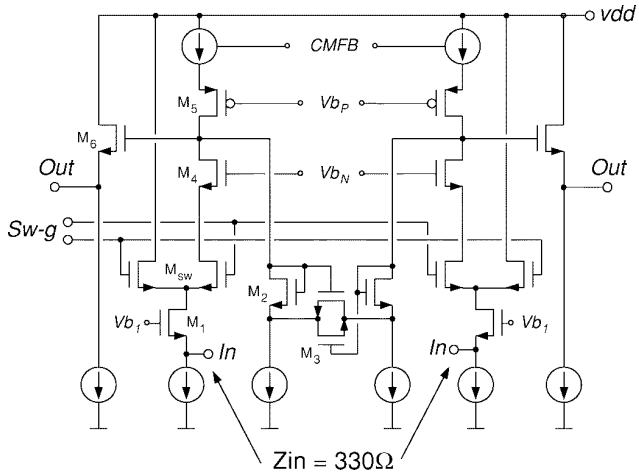

Fig. 8. Input stage of the 71-MHz IF amplifier.

dB can be expected for a total current consumption of only 4 mA. High values of IP3 can also be expected from the CMOS implementation, which tends to be much more linear than their BJT counterpart [6]. To achieve 10-dB voltage gain as well as impedance matching to the IF filter, a 1.4-kΩ load resistor R_L together with an external matching network having a Q $\approx$ 2 is needed at the output, as shown in Fig. 7.

C. IF Baseband Strip

The fully integrated IF strip consists of an IF amplifier [17], a quadrature demodulator, and two fourth-order Bessel low-pass filters. The first stage of the IF amplifier is shown in Fig. 8. A common gate configuration is used to provide impedance matching. The input stage consists of an array of common gate differential pairs (M_1), one of which is shown in the schematic. Gain control is achieved using a current steering principle, which employs transistors $M_{\rm sw}$ to switch the signal current of the corresponding differential pair either to $V_{\rm dd}$ or to the load. Cascode devices M_4 and M_5 are used to maintain the dominant pole at a constant frequency of 150 MHz for different gain configurations. High output linearity is achieved with the help of load degeneration, as shown in the Fig. 8. The first stage of the three-stage amplifier is programmable between 0–20 dB in 2-dB steps, while the second and third stages are programmable between -10 to 20 dB in 2-dB steps. At maximum gain, the complete IF amplifier draws 2.6 mA from the 2.5-V supply. The down-conversion mixers in the I, Q demodulator are implemented using a double balanced structure followed by a differential transimpedance stage to achieve 16-dB gain with sufficient linearity. Phase and amplitude accuracy in the I and Q paths is guaranteed by careful design of the integrated phase shifter and highly symmetrical layout. For the phase shifter, an enhancement source-coupled logic digital divider has been used to divide a 142-MHz input local oscillator (LO) into two 71-MHz signals in quadrature phase, to guarantee the best accuracy. The complete demodulator needs just 660 μA. The baseband filters are fourth-order Bessel LPF's with a cutoff frequency of 150 kHz. They have been implemented using an active-RC Sallen & Key structure, which realizes 16-dB gain and four poles using only two op-amps. Due to the tolerances of the integrated components, the cutoff frequency could vary up to $\pm$30%. Since the purpose of these filters is essentially anti-aliasing for the baseband A/D converters, this deviation is of no consequence provided a sufficiently high sampling rate is used. Total current consumption for the filters is 1.3 mA.

IV. Measured Receiver Performance

A micrograph of the complete GSM transceiver is shown in Fig. 9. To characterize the receiver, measurements have been carried out on the individual building blocks as well as the complete receiver. To measure the circuit performance, each bare die is directly bonded on a printed circuit board (PCB) with all required external components mounted on it. In Fig. 10, the measured NF is shown for two samples of the complete RF front end with all external filters. Both circuits have an S_{11} better than -8 dB at the duplexer input. In both cases, the measured SSB NF is less than 7 dB with a best case of 6.6 dB. These are much better than the worst case receiver plan because the external filters used are not worst case and therefore have less attenuation than that used in receiver planning. In Fig. 11, the measured mixer gain as well as its linearity characteristics are shown. For measurement purposes, the output matching resistor R_L has been set to 470 Ω in place of the nominal 1.4 kΩ. This together with the loading of the instrument (450 Ω) and 0.5-dB loss in the output matching network results in a power gain of -5 dB, as shown in the measurement. As stated earlier, one of the characteristics of the single-ended double balanced RF mixer is that, with a class-AB input stage, it does not compress. Moreover, thanks to the CMOS implementation and sufficient gate overdrive on the input transistors, the measured iIP3 is as high as $+7.5$ dBm. The measurement of the IF amplifier is shown in Fig. 12 in terms of the accuracy of the absolute gain as well as the differential accuracy of the 2-dB steps. The minimum gain is -20.9 dB, and the maximum gain is 58 dB, which shows good absolute accuracy considering the open-loop structure.

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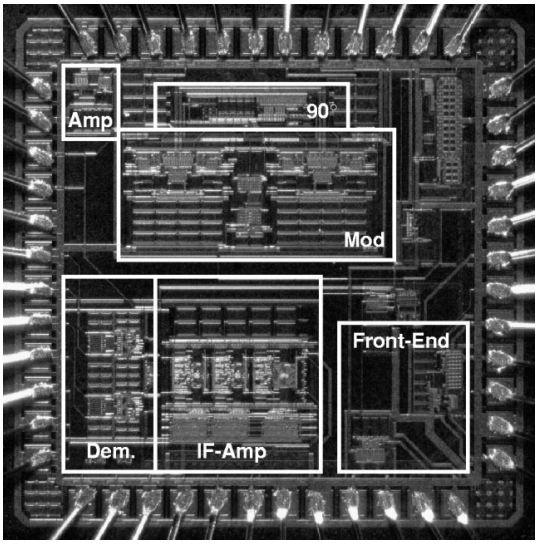

Fig. 9. Microphotograph of the transceiver.

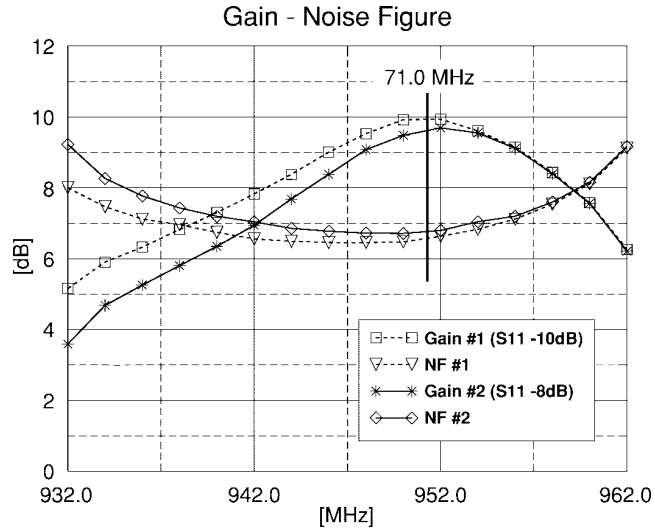

Fig. 10. Measured NF of the RF front end with both duplexer and image filter.

An excellent differential accuracy with typical error of 0.1–0.2 dB has been also achieved, despite the difficulty in matching devices at such a high frequency, low supply voltage, and low power. A summary of the measured performance of the complete receiver is shown in Fig. 13 against the requirements in the earlier plan. As shown in the top graph, a very high linearity has been achieved in all the receiver blocks, with measured CP and IP3 values exceeding the requirement by a good margin. The measured gain control range is 98 dB, as planned. Very low noise figures of 1.9, 12.6, and 3.8 dB have been achieved by the LNA, mixer, and IF strip, respectively. If the noise measurements of individual active devices are combined with the assumption that all external passive filters have the worst case specified by the manufacturer, overall NF is 8.1 dB. Current consumption is also in line with the requirement. Thanks to the low-power mixer and IF strip, a total current consumption of 19.5 mA, (<50 mW) has been achieved. Table I summarizes the achieved overall receiver performance.

V. Transmitter

As stated earlier, during the modulation process, the generation of unwanted emissions must be minimized. For a direct conversion implementation, the major contributors to the spurious signals are the intermodulation products generated by nonlinearities in the modulation circuits, imperfect suppression of the unwanted sideband signal, and the carrier feedthrough. At the circuit level, this means that high linearity and low LO feedthrough must be achieved in the I, Q up-conversion mixers, and high accuracy in the 90° phase shifter is required to keep the image low.

The transmit RF filter that suppresses out-of-band spurious signals has been placed between the modulator and the preamp. In this way, the preamp only has to deliver the required 2-mW output signal to the PA, and not 2 mW plus the attenuation of the filter, which would place more burden on the preamp. To achieve the required output power, the modulator is specified to deliver 20 μW to the TX filter, so that after the filter attenuation, 23 dB of gain is required in the preamp. For the transmitter, power consumption is not as important as it is in the receiver since in transmit mode, power consumption is dominated by the PA. However, to keep the power needed by the transmitter to a negligible level, current must not be wasted unnecessarily.

A. Up-Conversion Mixer

A schematic of one path of the I, Q modulator is shown in Fig. 14. It is basically a double balanced Gilbert mixer with a regulated input stage to ensure high linearity. Thanks to the differential input structure, even harmonics are rejected. The double balanced configuration suppresses the RF carrier at the mixer output. Since the I, Q signals at the input are at baseband, a power-efficient way to implement a highly linear circuit is to use negative feedback. The feedback loops based on the operational transconductance amplifiers (OTA's) regulate the currents in transistors M_1, so that the differential input voltage $V_{\rm in}$, assuming that R_1 equals R_2, will appear on resistor R_3. The input signal voltage is therefore translated into an input signal current I_s such that $I_s = V_{\rm in}/R_3$. Assuming perfect switching devices $M_{\rm sw}$, the mixer conversion g_m depends only on the linear component R_3 and can be calculated to be

$$g_m = \frac{2}{\pi} * \frac{1}{R3}. \tag{1}$$

Transistors $M_{\rm sw}$ are minimum length devices that are dimensioned to work in weak inversion, so that a −3-dBm carrier is sufficient to guarantee good switching. The 1.2-MHz first-order LPF required at the input has been realized in the feedback loop by resistor R_2 and capacitor C_2. Capacitor C_3 is introduced first to compensate the OTA and secondly to be a sink for high-frequency spurious signals, which may feed through the Miller capacitance of transistor M1 and which could cause instability in the amplifier. To minimize

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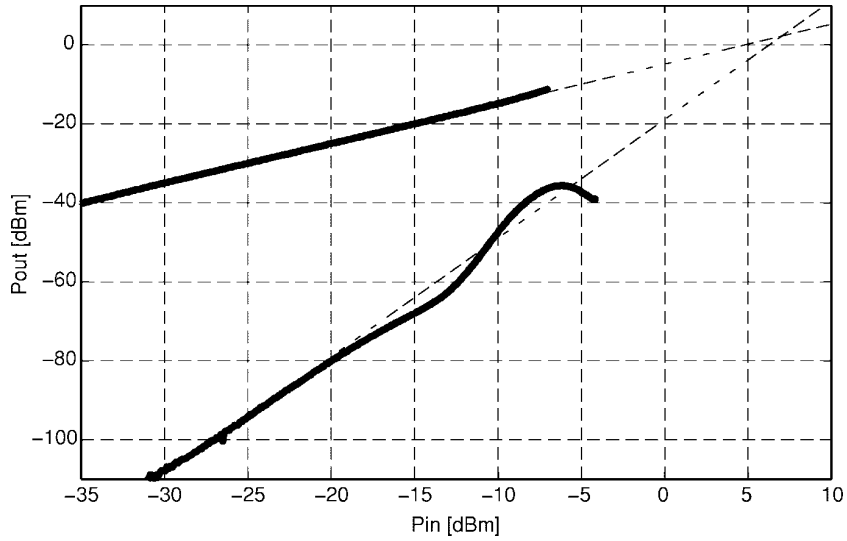

Fig. 11. Measured mixer linearity.

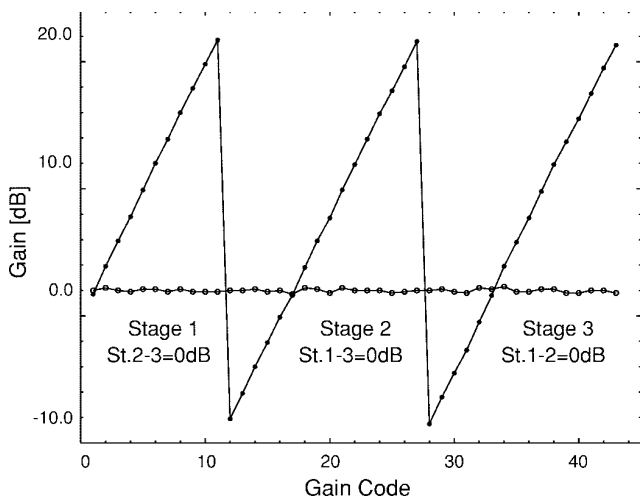

Fig. 12. Measured absolute and differential gain of the IF amp.

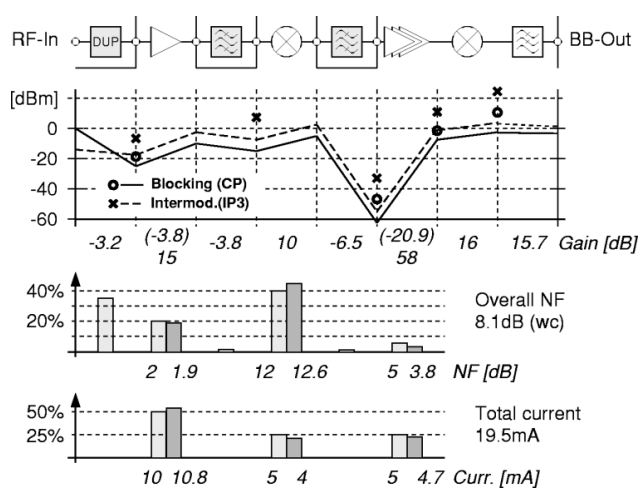

Fig. 13. Receiver planned and measured results.

TABLE I
SUMMARY OF MEASURED RX PERFORMANCE

Complete Receiver	Gain	101dB
(including duplexer	NF(50Ω)	8.1dB SSB
and filters)	iCP	−16dBm
	iIP3	−4dBm
	Blocking	+6dBm@915MHz (w.c.)
	Current Cons.	19.5mA@2.5V
LNA	Gain	+15.3dB,−3.8dB
	NF(50Ω)	1.9dB
	iCP	−19dBm
	iIP3	−7.5dBm
RF-mixer	Conv. g_m	8.5mS
	NF(50Ω)	12.6dB SSB
	iIP3	+7.5dBm
71MHz IF-Amp	Gain	−20.9 .. +58dB (2dB steps)
	Step Accuracy	0.1 − 0.2dB (Typical)
	NF(330Ω)	3.8dB
I,Q Demodulator	Gain	16dB
	Unwanted Sideband	
	Suppression	>43dB
Baseband Filters	Gain	15.7dB
	Cut-off Frequency	160kHz

the input offset, particular care has been taken in the design of the OTA's. Large input transistors as well as well-matched structures have been employed. Folded cascode OTA's with PMOS input stage are designed for 50-MHz bandwidth and draw 500 μA each from the 2.5-V supply. The minimum bias current required in each mixer can be calculated from the required output power of −17 dBm (20 μW), which the modulator must provide to the 50-Ω filter. Given the 50-Ω output resistance of the modulator required by impedance

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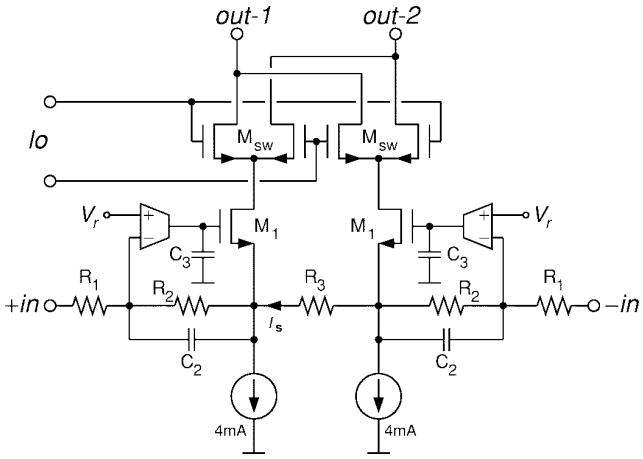

Fig. 14. Schematic of the modulator.

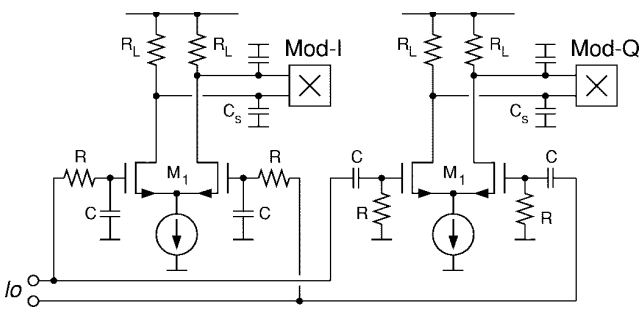

Fig. 15. Schematic of the 900-MHz, 90° phase shifter.

matching to the filter, the modulator must provide a total power of 40 μW to a total load of 25 Ω. For a quadrature modulation scheme, this means that each mixer must provide 40 μW to the load, and the output peak signal current is

$$I_{\rm os} = \sqrt{2} * \sqrt{\frac{40\ \mu\text{W}}{25\ \Omega}} = 1.8\ \text{mA}_p. \tag{2}$$

Taking into account approximately 6 dB of attenuation associated with the switching devices (−3.92 dB in case of perfect switching), the baseband signal current I_s flowing into $R_{\rm in}$ is 3.6 mA$_p$. To guarantee a minimum current in the devices M_1, the bias current I is set with some margin to 4 mA. The total power consumption of the I, Q modulator, including the OTA's, is therefore 18 mA.

B. Phase Shifter

One of the most challenging tasks in the transmitter design is the realization of the integrated 900-MHz, 90° phase shifter in a CMOS technology. Even with a 0.25-μm minimum channel length, the relatively low g_m/I ratio of MOS transistors makes it impractical to implement the emitter (source) followers found in some of the phase-shifting circuits in BJT transceivers [11], [22]. To meet the transmitter specs with some margin, the unwanted sideband (image) must be rejected by 30–35 dB. Using trigonometric analysis, the image rejection ratio (IRR)

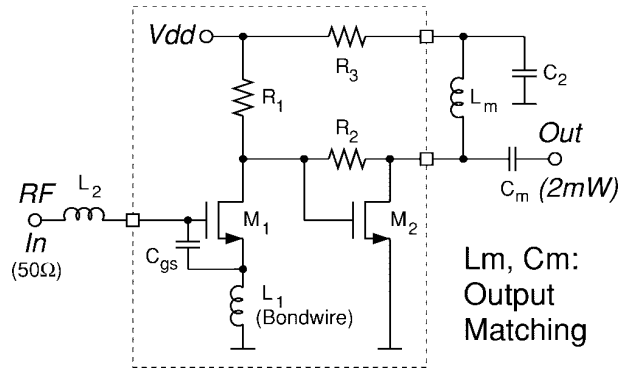

Fig. 16. Schematic of the preamplifier.

can be calculated to be

$$\text{IRR} = 20\ \log\left(\sqrt{\sin^2(\Delta\varphi/2) + \Delta A^2 \cos^2(\Delta\varphi/2)}\right) \tag{3}$$

where ΔA is the amplitude mismatch and $\Delta\varphi$ is the phase mismatch between the quadrature channels. If the I, Q mixers are carefully drawn with a symmetrical and matched layout, inaccuracies in the quadrature channels are mainly caused by the phase and amplitude mismatches of the LO signals due to the phase shifter. To achieve 30 dB, $\Delta A < 0.3$ dB and $\Delta\varphi < 3°$ are required. In our implementation, an RC-CR structure has been used in combination with limiting amplifiers, as shown in Fig. 15. The RC-CR network, assuming well-matched components, provides 90° constant phase shift independent of the frequency, the component values, and the parasitic capacitance C_p. This can be shown by considering the amplitude response A_i and phase response φ_i for the I-channel and A_q, φ_q for the Q-channel

$$A_i = \frac{1}{\sqrt{1 + (\omega R(C + C_p))^2}} \tag{4}$$

$$\varphi_i = 0° - atan(\omega R(C + C_p)) \tag{5}$$

$$A_q = \frac{\omega RC}{\sqrt{1 + (\omega R(C + C_p))^2}} \tag{6}$$

$$\varphi_q = 90° - atan(\omega R(C + C_p)). \tag{7}$$

The frequency/component-dependent amplitude variation is minimized by the limiting buffers and by the modulator switching transistors that work in weak inversion. Using this technique, sufficient IRR can be achieved for a center frequency of 900 MHz, for component tolerances as high as ±20% without spending excessive current. Additional phase correction circuits [11] have been found to require too much power in a CMOS implementation, and <1° accuracy is also not necessary. At the buffer output, the pole formed by resistor R_L and the sum of all stray capacitances C_s (which includes the drain capacitance of device M_1 of the phase shifter and the gate capacitance of the switching device $M_{\rm sw}$ of the mixer) has been placed to about 2.5 GHz. A relatively high frequency has been chosen so that any mismatch between the quadrature paths at this node, which occurs quite easily between stray

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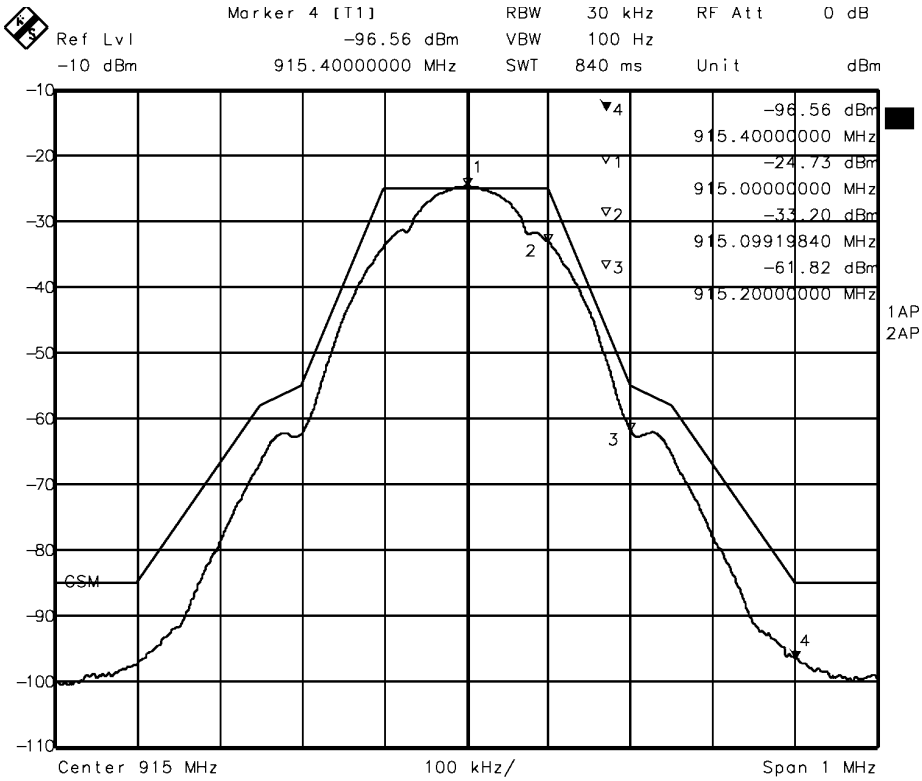

Fig. 17. GMSK modulated output.

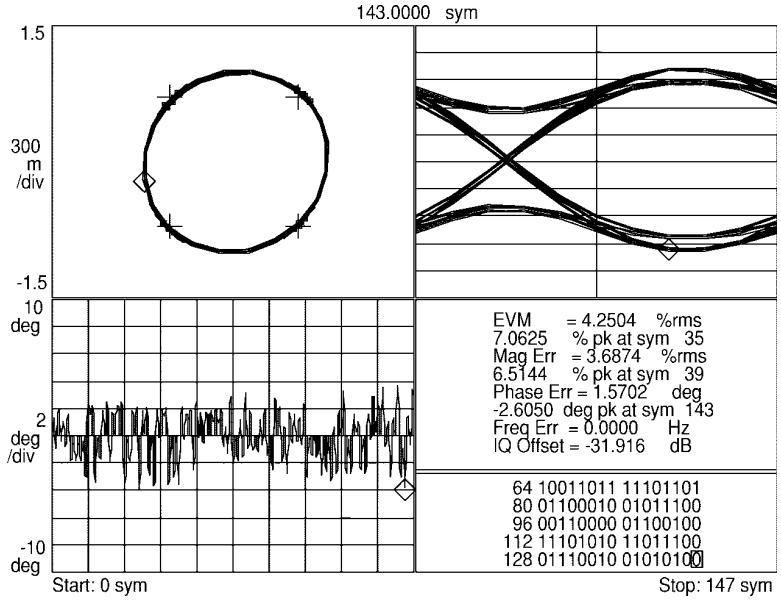

Fig. 18. Error vector measurement.

capacitances, will have little impact on the phase accuracy. To achieve sufficient gain despite the 3-dB attenuation in the RC network, 6 mA is required for each amplifier.

C. Preamplifier

The preamp, like the LNA, has been thoroughly discussed in [18]. Only a brief description will be given here. The preamplifier schematic is shown in Fig. 16. To achieve the required 23-dB gain, a two-stage implementation is necessary. The input stage is the same inductively degenerated common source input as that used in the LNA, to achieve low noise and impedance matching. Since the preamp must be able to handle a −17-dBm input signal, the cascode transistor has been removed to allow enough headroom, and a higher

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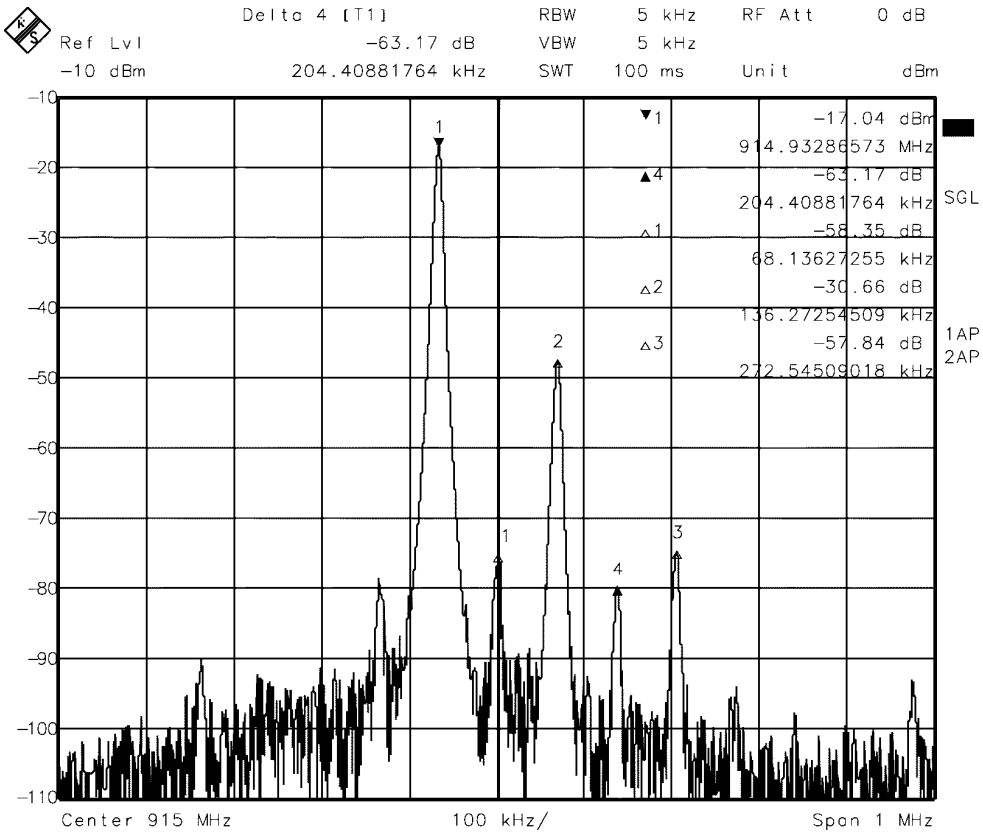

Fig. 19. Single-sideband modulated sinewave.

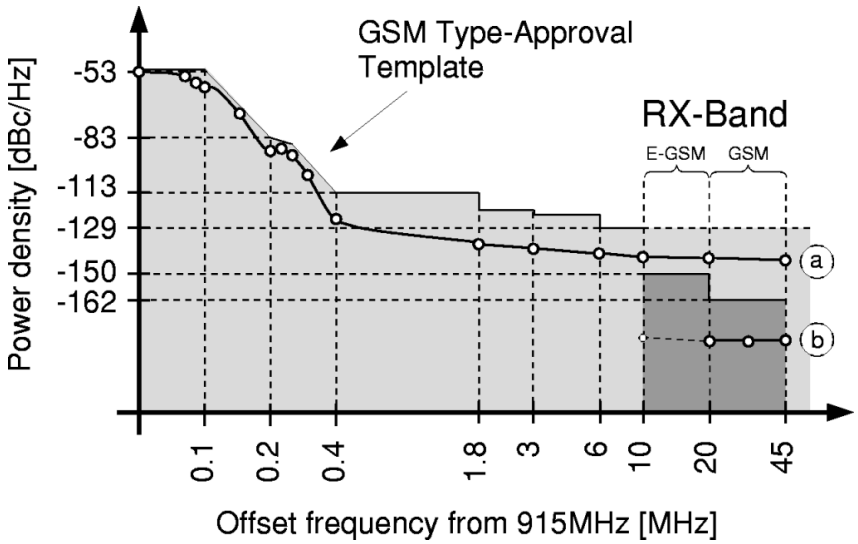

Fig. 20. Wide-band noise characteristic.

bias current is necessary to achieve the wanted linearity. The second stage is a simple class-A output with inductive load, so that little distortion is introduced by the preamp and power-added efficiency of the PA is hardly degraded. To prevent the output signal from swinging above $V_{\rm dd}$, thereby reducing the risk of damaging the chip, resistor R_3 has been added. To provide 2 mW to the PA with a suitable linearity, the preamp needs 25-mA current from the 2.5-V supply.

VI. Measured Transmitter Performance

The transmit section has been characterized by measuring bare dies attached to a PCB with all needed surface-mounted device (SMD) external components. The nominal 2.5-V voltage supply has been used. In the first step, the modulator alone was measured. The modulator output spectrum for a GMSK modulated input is shown in Fig. 17. A −3-dBm, 915-MHz LO carrier has been fed to the phase shifter input,

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TABLE II
SUMMARY OF MEASURED TX PERFORMANCE

Complete Transmitter (without PA)	Output power	2mW
	RMS phase error	<2°
	Peak phase error	<5°
	Current Cons.	55mA@2.5V
Modulator	Output power	−17dBm
	Carrier suppr.	>50dBc
	I,Q image suppr.	>31dBc
	Harmonics suppr.	>55dBc
Preamplifier	Gain	21dB
	oCP	5.8dBm

whereas the baseband I/Q input signal level is $1V_{\rm pp}$. The measured characteristic is well within the specified mask. The total integrated power at the modulator output is −17 dBm as specified. In Fig. 18, the EVM measurement is shown. The modulator's average rms phase error is about 1.6°, while the peak error is less than 3°. To appreciate the individual contribution of the various spurious components to the overall EVM, one can examine the EVM measurement shown in Fig. 19 for a 67-kHz, $1V_{\rm pp}$ quadrature input signal. The dominant contributor to phase error is the image signal. In fact, other spurious components are more or less negligible. The image signal is suppressed by about 31 dB, which means that an accuracy of $\Delta A = 0.3$ dB and $\Delta\varphi = 3°$ has been achieved in the quadrature channels. The carrier component is suppressed by more than 50 dB thanks to the double balanced structure and the well-matched OTA's. Higher harmonics are all suppressed by more than 50 dB, as a result of the modulator's differential implementation and the high linearity of the baseband feedback loop.

To show the wide-band noise characteristic at the modulator output, various points have been measured and are shown by curve (a) in the log–log graph of Fig. 20. For offset frequencies, <5-MHz modulator noise is clearly within the template with sufficient margin. Above 5 MHz, the measurement is limited by the noise floor of the spectrum analyzer. The noise floor of the modulator above 10-MHz offset should therefore be better than the −142 dBc/Hz shown there. Even at −142 dBc/Hz, the typical attenuation of 25 dB of a single duplexer alone will ensure that the required performance is met in the GSM receive band. Additional attenuation is also provided by the filter between the modulator and preamplifier. The preamplifier gain at 915 MHz is 21 dB. For a constant envelope modulation such as GMSK, the preamplifier can be used near compression without distorting the output signal significantly. The measured oCP of the preamplifier is 5.8 dBm, which corresponds to 3.5 mW, a value that is also well within specification. In a second step, the performance of the transmit chain including modulator, TX filter, preamp, and duplexer has been measured. The measured TX power at the duplexer output is 3.6 dBm. A noise measurement in the GSM receive band is shown by curve (b) of Fig. 20. Using a notch filter to reduce the signal power, the noise in GSM receive band can be better measured. The measured noise floor is now −180 dBc/Hz and is still limited by the instrument noise. Table II summarizes the transmitter performance.

VII. CONCLUSIONS

Narrow-band cellular wireless communications such as GSM telephony present significant challenges to CMOS realization of the RF transceiver with high frequency and high dynamic range, combined with low power consumption. With optimization at receiver planning as well as circuit design, however, deep submicrometer CMOS is indeed capable of providing the kind of high performance required by GSM-type approval tests. Furthermore, we have demonstrated that low power consumption is also achievable in CMOS, without sacrificing the tolerance of transceiver performance to variations in component values typical in batch fabrication. Indeed, the achieved power consumption of 20 mA at 2.5 V in receive mode is lower than most published transceivers at 900 MHz by a large margin, including those implemented in advanced BJT technologies. It is the authors' opinion that CMOS technologies will replace BJT technologies as the dominant choice for realizing RF transceivers, at least at the low gigahertz. The deciding factor is not so much whether bipolar transistors are better for RF circuits than their MOS counterparts as the economic base behind the development momentum of CMOS technologies.

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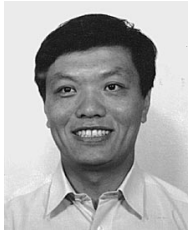

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