

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner,

v.

ENTROPIC COMMUNICATIONS, LLC.,
Patent Owner.

Patent No. 9,210,362
Filing Date: February 5, 2015
Issue Date: December 8, 2015
Title: WIDEBAND TUNER ARCHITECTURE

Inter Partes Review No.: IPR2024-00432

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

TABLE OF CONTENTS

I.	MANDATORY NOTICES	viii
II.	INTRODUCTION	1
III.	SUMMARY OF ARGUMENT.....	1
IV.	OVERVIEW OF THE '362 PATENT	2
	A. Brief Description	2
	B. Prosecution History	6
	C. Earliest Priority Date for the Claims	7
V.	OVERVIEW OF PRIOR ART	8
	A. Zhang.....	8
	B. Pandey	11
	C. Mirabbasi.....	13
	D. Karabinis	15
	E. Jensen	16
VI.	IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b).....	18
	A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based	18
	B. 314(a) Discretion Does Not Apply.....	19
	C. 325(d) Discretion Does Not Apply	20
	D. Level of Ordinary Skill	20
	E. Claim Construction.....	21
	1. “digitizing,” “selecting,” “outputting”	21
	2. “wideband” and “wideband analog-to-digital converter (ADC) module”	21
	3. “digital circuitry”	22
VII.	SPECIFIC GROUNDS FOR UNPATENTABILITY	23
	A. Grounds A/B: Claims 1-3, 8, 9, 11-13, 18, and 19 are Anticipated and Rendered Obvious by Zhang.....	23

1.	Independent Claim 1	23
2.	Dependent Claims 2 and 3	36
3.	Dependent Claims 8 and 9	40
4.	Independent Claim 11	42
5.	Dependent Claims 12-13, 18-19	42
B.	Ground C: Claims 2, 3, 12, and 13 are Rendered Obvious by Zhang-Pandey.....	43
1.	Dependent Claims 2 and 3	43
2.	Dependent Claims 12 and 13	47
C.	Ground D: Claims 4-6 and 14-16 are Rendered Obvious by Zhang-Mirabbasi.....	48
1.	Dependent Claim 4.....	50
2.	Dependent Claim 5.....	53
3.	Dependent Claim 6.....	55
4.	Dependent Claims 14-16.....	60
D.	Ground E: Claims 7 and 17 are Rendered Obvious by Zhang-Mirabbasi-Karabinis.....	60
1.	Dependent Claim 7.....	60
2.	Dependent Claim 17	68
E.	Ground F: Claims 10 and 20 are Rendered Obvious by Zhang in view of Jensen.	68
1.	Dependent Claim 10	68
2.	Dependent Claim 20	72
F.	Alternate Arguments and Grounds based on Means-Plus-Function Construction of “digital circuitry”	72
1.	Claims 1, 2-6, and 8-9 based on Grounds A/B, Claims 2-3 based on Ground C, Claims 4-6 based on Ground D, Claim 7 based on Ground E, and Claim 10 based on Ground E	72
2.	Claims 1-6 and 8-9 based on Zhang-Mirabbasi (Ground D), Claim 7 based on Zhang-Mirabbasi-Karabinis (Ground E)	74
3.	Claims 2 and 3 based on Zhang-Mirabbasi-Pandey (Ground G), and Claim 10 based on Mirabbasi-Jensen (Ground H)	77

VIII. GROUNDS FOR STANDING & FEE PAYMENT	77
IX. CONCLUSION.....	78
CERTIFICATION UNDER 37 CFR § 42.24(d)	79
CERTIFICATE OF SERVICE	80
CLAIM LISTING APPENDIX	81

EXHIBITS

- Ex. 1001: U.S. Patent No. 9,210,362 (“the ’362 patent”)
- Ex. 1002: Expert Declaration of David B. Lett
- Ex. 1003: Curriculum Vitae of David B. Lett
- Ex. 1004: Certified Prosecution History of the ’362 patent
- Ex. 1005: Certified Prosecution History of U.S. Patent No. 9,100,622
- Ex. 1006: Certified Prosecution History of U.S. Patent No. 8,526,898
- Ex. 1007: Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“’526 provisional”)
- Ex. 1008: Reserved
- Ex. 1009: Reserved
- Ex. 1010: Reserved
- Ex. 1011: Reserved
- Ex. 1012: Reserved
- Ex. 1013: U.S. Pub. No. 2003/0056221 (“Zhang”)
- Ex. 1014: U.S. Patent No. 7,237,214 (“Pandey”)
- Ex. 1015: Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)
- Ex. 1016: Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
- Ex. 1017: A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)

- Ex. 1018: S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
- Ex. 1019: U.S. Patent No. 6,061,406 (“Carson”)
- Ex. 1020: U.S. Pub. No. 2006/0233147 (“Karabinis”)
- Ex. 1021: Data-Over-Cable Service Interface Specifications, DOCSIS 2.0, Radio Frequency Interface Specification, CM-SP-RFIV2.0-I11-060602
- Ex. 1022: Certified File History (as of February 2, 2024) for *Ex Parte* Reexamination No. 90/019,255
- Ex. 1023: Certified Prosecution History of U.S. Patent No. 9,100,363
- Ex. 1024: Reserved
- Ex. 1025: J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
- Ex. 1026: U.S. Pub. No. 2007/0027943 (“Jensen ’943”)
- Ex. 1027: U.S. Patents and Patent Applications Family Tree for U.S. Patent No. 9,210,362
- Ex. 1028: Reserved
- Ex. 1029: Entropic Communications, LLC v. Charter Communications, Inc., No. 2:22-cv-00125-JRG (E.D. Tex. June 26, 2023) (Claim Construction Memorandum Opinion and Order)
- Ex. 1030: Reserved
- Ex. 1031: Reserved
- Ex. 1032: Reserved

- Ex. 1033: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2nd ed. 2004) (“Ciciora”)
- Ex. 1034: Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)
- Ex. 1035: U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
- Ex. 1036: U.S. Pub. No. 2003/0217362 (“Summers”)
- Ex. 1037: U.S. Pub. No. 2006/0256799 (“Eng”)
- Ex. 1038: U.S. Pub. No. 2006/0083335 (“Seendripu”)
- Ex. 1039: Excerpts of Chris Bowick, “RF Circuit Design” (2nd ed. 2008)
- Ex. 1040: Reserved
- Ex. 1041: Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)
- Ex. 1042: U.S. Patent No. 7,272,375 (“Tuttle”)
- Ex. 1043: U.S. Patent No. 7,130,576 (“Gurantz”)
- Ex. 1044: U.S. Patent No. 5,278,837 (“Kelley”)
- Ex. 1045: Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)
- Ex. 1046: U.S. Patent No. 7,213,042 (“Cannon”)
- Ex. 1047: Reserved
- Ex. 1048: Excerpts of William Buchanan, “Computer Busses” (2000) (“Buchanan”)
- Ex. 1049: U.S. Patent No. 7,079,528 (“Ziegler”)

Ex. 1050: Excerpts of “Software Defined Radio: Enabling Technologies”
(Walter H.W. Tuttlebee ed., 2003)

Exs. 1051-1072: Reserved

Ex. 1073: Expert Declaration of Dr. Sylvia Hall-Ellis

Ex. 1074 Reserved

Ex. 1075 U.S. Patent No. 6,791,995 (“Azenkot”)

Ex. 1076 U.S. Patent No. 6,542,203 (“Shadwell”)

I. MANDATORY NOTICES

Real Parties in Interest (37 C.F.R. § 42.8(b)(1))

The real parties-in-interest for this petition are (i) Comcast Corporation, (ii) Comcast Cable Communications, LLC, and (iii) Comcast Cable Communications Management, LLC. No unnamed entity is funding, controlling, or directing this Petition for *inter partes* review (IPR) of U.S. Patent No. 9,210,362 (“the ’362 patent”), or otherwise has an opportunity to control or direct this Petition or Petitioner’s participation in any resulting IPR.

Related Matters (37 C.F.R. § 42.8(b)(2))

Office Proceedings

This is the first of three petitions for *inter partes* review filed by Petitioner against the ’362 patent. Petitioner is also filing petitions for *inter partes* review against related U.S. Patent Nos. 11,381,866 and 11,399,206.

According to the Office’s records, a request for *ex parte* reexamination (Control No. 90/019,255) was filed September 20, 2023 for claims 1 and 11 of the ’362 patent, and an Order granting the request was issued on November 1, 2023. The requestor of the *ex parte* reexamination, Unified Patents, LLC, is not a real party-in-interest for this petition.

No other Office proceedings (e.g., *inter partes* review, post-grant review, or covered business method) have been filed against the ’362 patent.

Litigation matters

The '362 patent has been asserted in *Entropic Communications, LLC v. Comcast Corporation*, No. 2:23-cv-01050 (C.D. Cal. filed Feb. 10, 2023) and *Entropic Communications, LLC v. Cox Communications, Inc.*, No. 2-23-cv-01049 (C.D. Cal. filed Feb. 10, 2023) (collectively, “CA litigation”). These cases have been consolidated and remain pending. The '362 patent was also asserted in *Entropic Communications, LLC v. Charter Communications, Inc.*, No. 2:22-cv-00125-JRG (E.D. Tex. filed Apr. 27, 2022) (“TX litigation”), which was dismissed on December 10, 2023.

Continuity

According to Office records, the '362 patent is a continuation of U.S. Pat. App. No. 13/962,871, filed August 8, 2013 (issued as U.S. Pat. No. 9,100,622) which is a continuation of U.S. Pat. App. No. 12/762,900, filed April 19, 2010 (issued as U.S. Pat. No. 8,526,898), which claims the benefit of Provisional App. No. 61/170,526, filed April 17, 2009. The '362 patent is part of a family that includes thirteen additional patents or applications that purport to claim priority, via a chain of continuation applications, from App. No. 12/762,900. A family tree is included as Ex. 1027.

Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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II. INTRODUCTION

Comcast Cable Communications, LLC (“Petitioner”) petitions for *inter partes* review of claims 1-20 of U.S. Patent No. 9,210,362 (“the ’362 patent”) (Ex. 1001).

III. SUMMARY OF ARGUMENT

The ’362 patent generally claims a wideband receiver system and a corresponding method of operating such a system to select and output a plurality of television channels. The system includes a mixer module that downconverts a plurality of frequencies that include desired and undesired television channels, a wideband analog-to-digital converter (ADC) module that digitizes the plurality of frequencies, and digital circuitry that selects the desired channels from the digitized frequencies and outputs the selected channels as a digital data stream to a demodulator.

The ’362 patent admits that its disclosure of a mixer module, an ADC module, and other elements on the analog side of the wideband receiver system “is similar to conventional tuners.” Ex. 1007, p. 5; Ex. 1001, 1:5-11. The alleged inventive concept—demodulating multiple television channels from the digitized plurality of frequencies—simply copies well-known digital circuitry for demodulating each channel. The ’362 patent claims are disclosed or rendered obvious by the prior art, e.g., Zhang (Ex. 1013) and other references relied on herein.

Accordingly, claims 1-20 of the '362 patent are unpatentable and should be cancelled.

IV. OVERVIEW OF THE '362 PATENT

A. Brief Description

The '362 patent describes a wideband receiver system 200 “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1001, 1:15-18; Ex. 1002, ¶ 36. The system purports to group desired channels that extend over non-contiguous portions of the frequency spectrum “into a contiguous, or substantially-contiguous, frequency spectrum” to “increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator.” Ex. 1001, 1:18-23, 2:24-27. According to the '362 patent, a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” *Id.*, 1:24-27. Figure 2 is a “schematic block diagram of a wideband receiver system 200.” *Id.*, 4:16-18; Ex. 1002, ¶ 37.

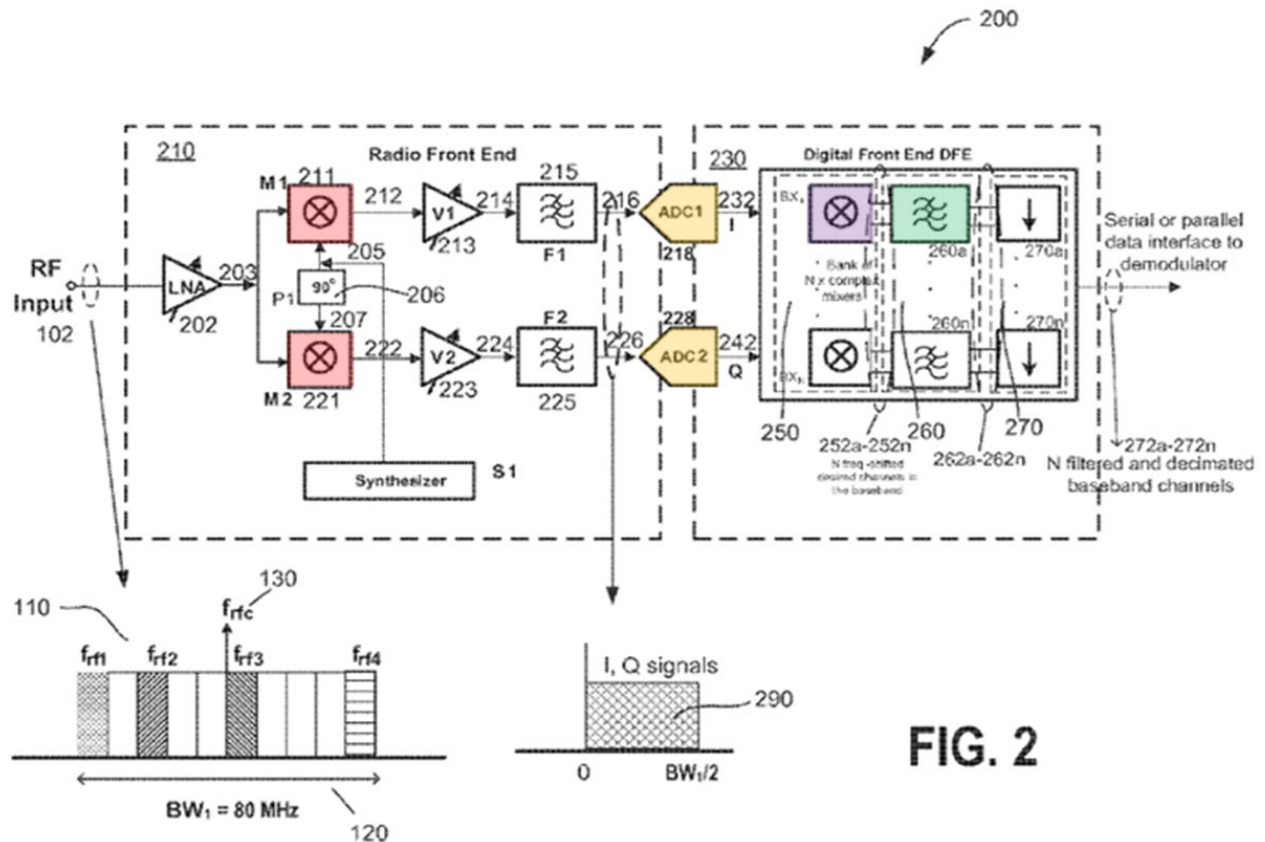


FIG. 2

Ex. 1001, Fig. 2 (annotated)

The wideband receiver system 200 receives both desired and undesired television channels as frequencies dispersed within a frequency bandwidth BW_1 . Ex. 1001, Abstract, 1:19-22; Ex. 1002, ¶ 38. Mixers “M1” and “M2” (red) “generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90° degree between them” and that have been downconverted to “the baseband or low

intermediate frequency (IF) band.”¹ Ex. 1001, 4:40-46, 2:45-49, *see also* 1:60-62. “[U]nwanted frequency components” are filtered from the in-phase and quadrature signals by respective filters 215 and 225. Ex. 1001, 4:64-5:3. The filtered signals are then individually digitized by wideband analog-to-digital converters ADC1 and ADC2 (**gold**) to generate a digital in-phase (I) signal 232 and a digital quadrature (Q) signal 242. Ex. 1001, 2:49-51, 5:28-31. U.S. Provisional App. No. 61/170,526 (“’526 provisional”), which the ’362 patent incorporates by reference, admits that the left side of Figure 2 (up to and including ADC1 and ADC2) “is similar to conventional tuners.” Ex. 1007, p. 5; Ex. 1001, 1:5-11; Ex. 1002, ¶ 38.

The digital I and Q signals 232 and 242 are input to a digital front end 230, containing a bank of N complex mixers 250 (one of which is shown above in **purple**), where N is “the number of desired RF channels.” ² Ex. 1001, 5:31-35.

¹ A mixer multiplies an input signal (frequency f_1) by a reference signal (frequency f_2) to produce new signals at the sum and difference frequencies (f_1+f_2 and f_1-f_2). Ex. 1002, ¶ 66. The reduced frequency (f_1-f_2) version is output as the “down converted” complex signal with real (I) and imaginary (Q) components. Ex. 1002, ¶ 67.

² Complex mixers multiply signals already separated into their complex I and Q components. Ex. 1002, ¶ 66.

“Each of the N complex mixers ... extract a different one of the desired channels” from the I and Q signals 232 and 242 and “frequency-shifts the extracted signals to the baseband frequency.”³ Ex. 1001, 5:49-52. The output of each mixer 250 leads to an associated filter module 260 (one of which is shown above in **green**), which filters the frequency-shifted desired channel. Ex. 1001, 5:52-54; Ex. 1002, ¶ 39.

Figure 3 “is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230” and shows the elements in one of the rows of digital front end 230 in Figure 2. Ex. 1001, 5:62-64; Ex. 1002, ¶ 40.

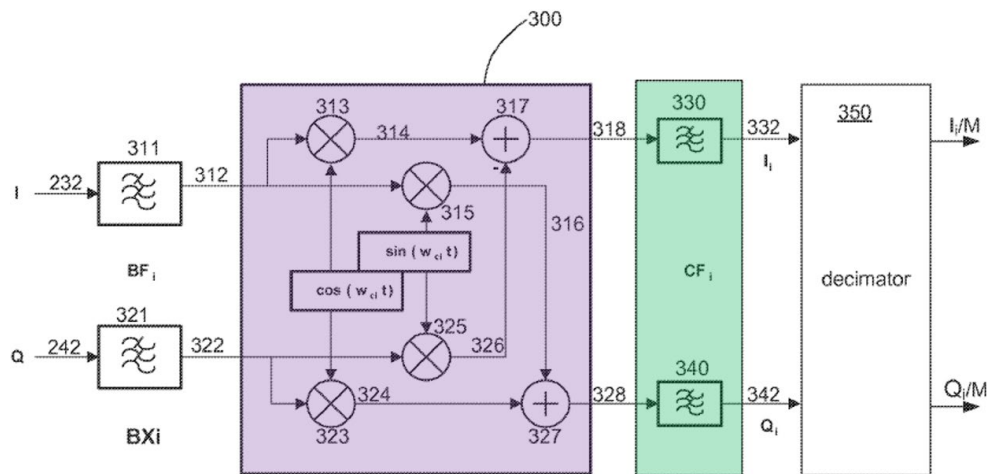


FIG. 3
Ex. 1001, Fig. 3 (annotated)

³ Signals have a center frequency f that is modulated with data. Shifting the signal to baseband reduces f to zero, leaving only the modulated data as the output. Ex. 1002, ¶ 63-64, 69.

Mixer 300 (**purple**) represents one of the complex mixers 250 and has multipliers 313, 315, 323, and 325 and adders 317 and 327. Ex. 1001, 6:7-17. “[C]omplex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain” by multiplying the I and Q signals by a frequency ω_{ci} that is “chosen [so] that each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband.” Ex. 1001, 6:17-34. Filters 330 and 340 (**green**), “one of the filters 260a-n” shown in Figure 2, filter baseband signals 318 and 328. Ex. 1001, 6:43-45; Ex. 1002, ¶ 41. This exact structure was a conventional design, simply copied multiple times to downconvert multiple channels, respectively. *See e.g.*, Ex. 1002, ¶ 64-69.

After decimation, “the N desired baseband channels” are sent “to a demodulator using a serial or parallel data interface according to commonly known methods.” Ex. 1001, 6:55-58; .

B. Prosecution History

The application which became the '362 patent was filed on February 5, 2015, with 20 claims including independent claims 1 and 11. Ex. 1004, pp. 2-53. Following a nonstatutory double patenting rejection over claims 1-27 of U.S. Patent No. 8,526,898, Applicant filed a terminal disclaimer. Ex. 1004, pp. 75-79, 90-99. A Notice of Allowance issued indicating that the prior art failed to describe a wideband receiver system with “digital circuitry configured to select a plurality of desired

television channels from the digitized plurality of frequencies and output said plurality of television channels to a demodulator as a digital datastream.” Ex. 1004, pp. 102-108. Following an RCE and an IDS (Ex. 1004, pp. 115-140), a second Notice of Allowance issued. Ex. 1004, pp. 141-147.

None of Zhang, Pandey, Mirabbasi, Karabinis, or Jensen was considered during prosecution. Ex. 1001, cover; Ex. 1002, ¶ 44.

The Office ordered reexamination (Control No. 90/019,255) of independent claims 1 and 11 of the ’362 patent on November 1, 2023. Ex. 1022, pp. 631-642. The reexamination is currently pending. None of Zhang, Pandey, Karabinis, or Jensen has been cited in the reexamination. Ex. 1022, p. 634; Ex. 1002, ¶ 45. Mirabbasi was cited as an exhibit in the *ex parte* request for the reexamination, but was not cited as a prior art reference or relied upon by the Office in ordering the reexamination. Ex. 1022, 393, 455, 732-743.

C. Earliest Priority Date for the Claims

The earliest possible effective filing date for the claims of the ’362 patent is April 17, 2009. Ex. 1002, ¶ 47. Each reference relied on herein is prior art to that date.

V. OVERVIEW OF PRIOR ART

A. Zhang

Zhang (U.S. Pub. No. 2003/0056221, Ex. 1013) published on March 20, 2003, and is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1002, ¶ 78.

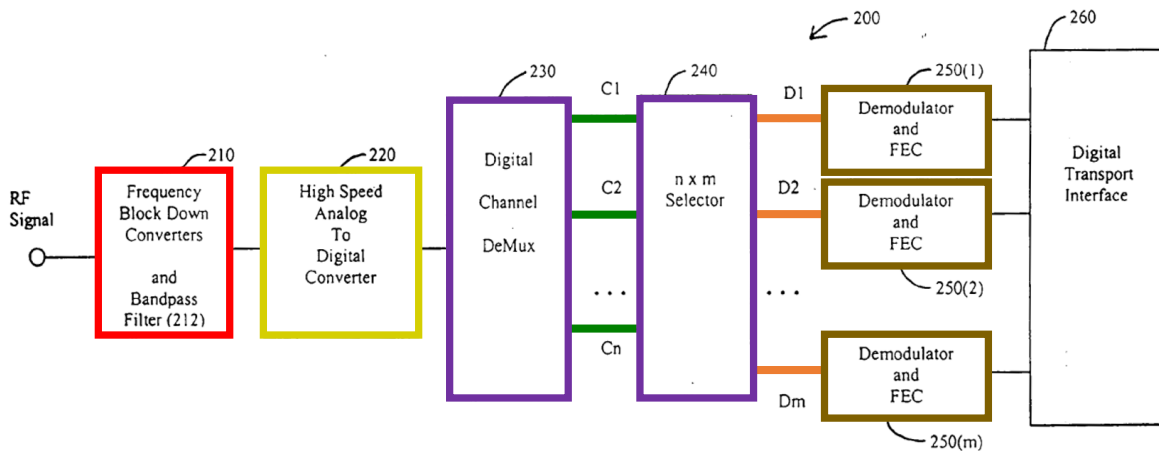


Fig. 2

Ex. 1013, Fig. 2 (annotated)

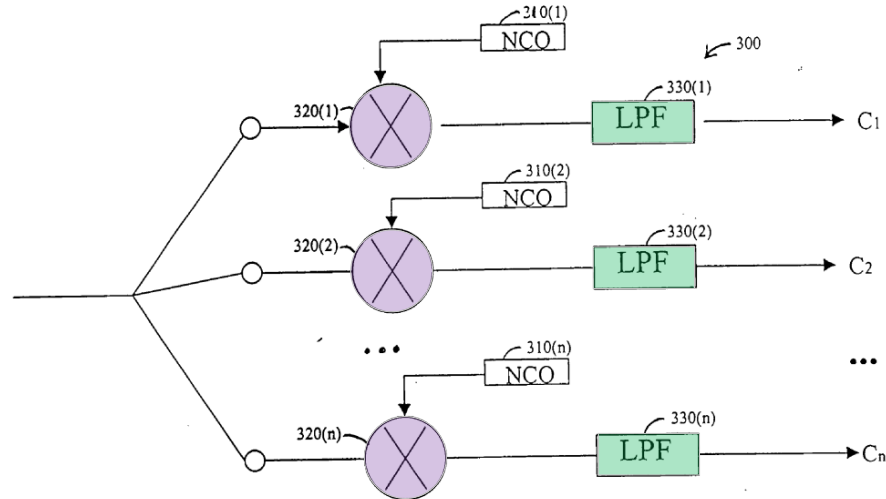
Zhang, which is analogous art to the '362 patent, describes a multi-channel demodulator circuit 200 (illustrated by Figure 2 reproduced above) that can be used as “advanced wide-band front-ends for digital set-top boxes, PVRs, home gateways and home media centers.” Ex. 1013, [0044]-[0045], Fig. 8; Ex. 1002, ¶¶ 79, 81. Circuit 200 receives a band of analog Radio Frequency (RF) signals comprising multiple content channels and demodulates signals only for those channels that a subscriber has selected. Ex. 1013, [0011], [0024], [0028]-[0029], [0038]-[0040], [0042]; Ex. 1002, ¶ 79. Circuit 200 comprises a frequency block down-converter 210 (red) that receives the band of analog RF signals and shifts the band to a lower frequency (comparable to the '362 patent's intermediate frequency band) such that

an analog-to-digital converter (**gold**) can better convert the analog RF signals to digital RF signals. Ex. 1013, [0010], [0023], [0025], [0027], [0030]-[0037], [0041]-[0042].

Much like the '362 patent's complex mixer and filters that extract various selected channels in parallel, Zhang's digital channel demultiplexer 230 (**purple**) separates channels selected by a subscriber in the incoming digital RF signals (e.g., channels C_1 to C_n), while digital selector 240 forwards any and all of the selected channels (e.g., channels D_1 to D_m) to one or more of demodulators 250(1) - 250(m) (**brown**), which may be "shared demodulators" with common functional blocks. Ex. 1013, [0010]-[0011], [0028]-[0029], [0042], [0047], claims 1, 4, 9, 31-32; Ex. 1002, ¶ 79. One or more of demodulators 250(1), 250(2), . . . 250(m) receive and demodulate the signals of the selected content channels and output them to a digital transport interface to eventually recover the audio and video data therein. Ex. 1013, [0007]; Ex. 1002, ¶ 79.

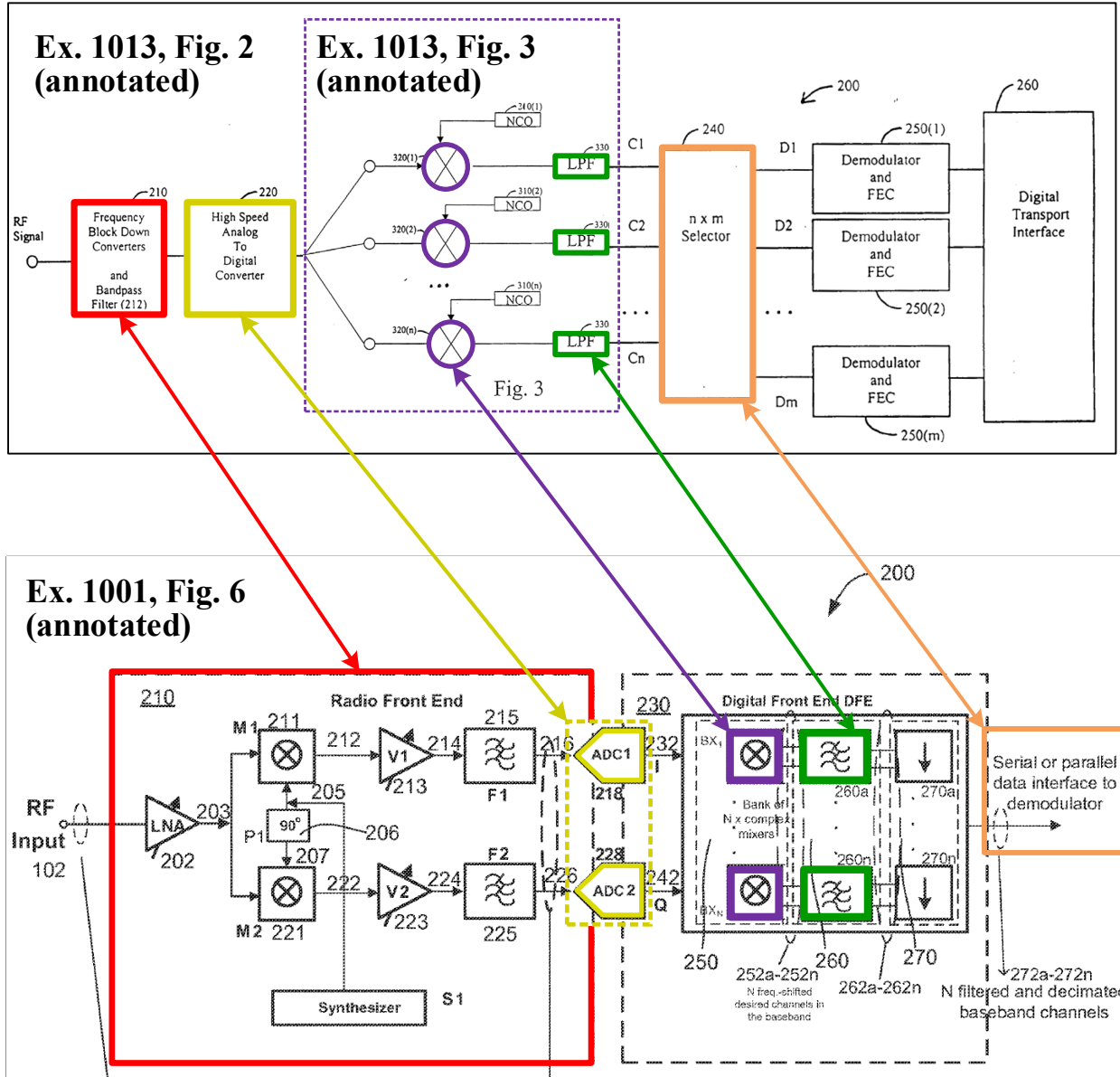
Zhang's demultiplexer 230 includes a bank of numeric control oscillators 310(1)-310(n), complex multipliers 320(1)-320(n) (**purple**), and low-pass filters (LPFs) 330(1)-330(n) (**green**). Ex. 1013, [0030]. The complex multipliers 320(1)-320(n), like the complex mixer in the '362 patent, multiply the digital RF signals with select frequencies provided by the numeric control oscillators 310(1)-310(n), which shifts the frequencies of the digital RF signals to baseband. Ex. 1013, [0032];

Ex. 1002, ¶ 80. The LPFs 330(1)-330(n) “filter[] undesired RF channels and pass[] only the target RF channel.” Ex. 1013, [0033], claim 37; Ex. 1002, ¶ 80.

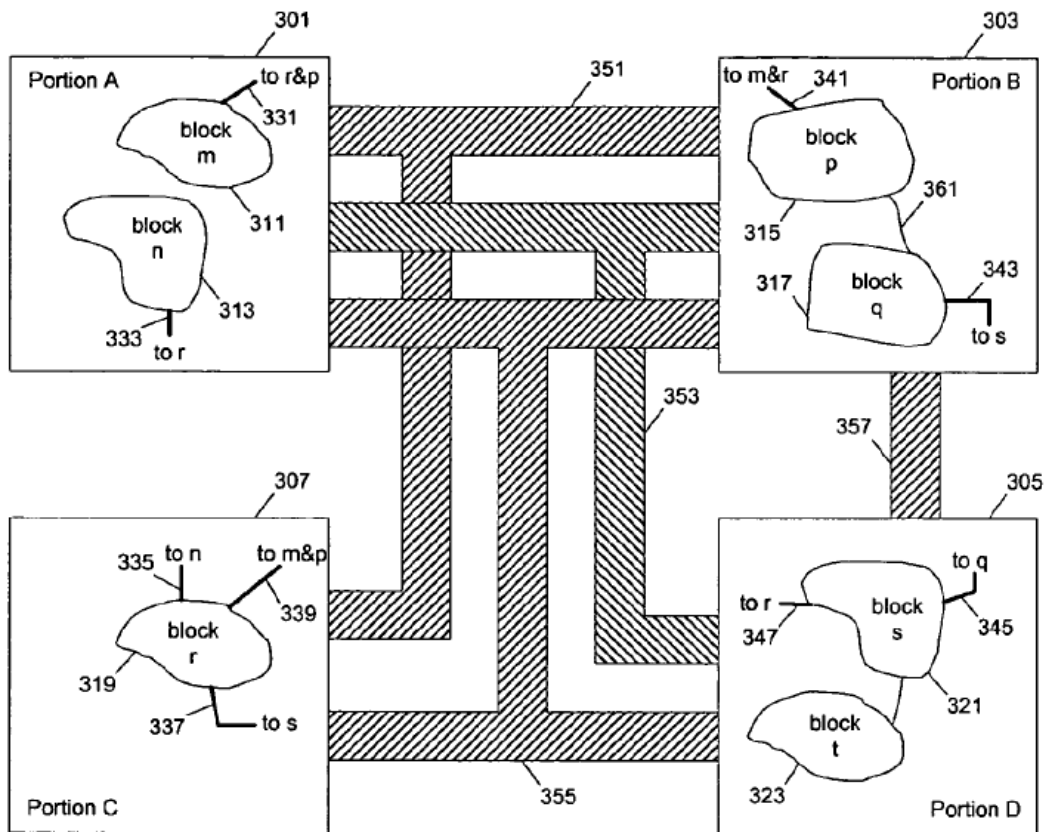


Ex. 1013, Fig. 3 (annotated)

As shown below and discussed *infra*, Zhang discloses the same system as the '362 patent, including a “mixer module” (**red**) (Element 1B), a “wideband analog-to-digital converter (ADC) module (**gold**) (Element [1C]), and “digital circuitry configured to: select said plurality of desired channels” (**purple/green**) (Element [1D]) and “output said selected plurality of television channels to a demodulator as a digital data stream” (**orange**) (Element [1D]). The digital circuitry further includes finite impulse response filters (**green**) (Claims 8, 9), and a serial/parallel interface in selector 240 (**orange**) (claims 2, 3).



1:15-55, 2:4-12; Ex. 1002, ¶ 83. Pandey's process involves partitioning functional blocks to different regions of an integrated circuit chip (e.g., 301, 303, 305, 307 as illustrated in Figure 3 of Pandey reproduced below) and assigning wire traces (e.g., 351, 353, 355, 357) to interconnect the partitioned blocks. Ex. 1014, 1:56-60, 2:6-12, 2:64-3, 6:10-15, 11:6-19, 13:33-14:7.



Ex. 1014, Fig. 3

The number of signals (nets) between function blocks in different partitions may exceed the number of traces available inside a chip, and in such cases, multiple signals must be time-multiplexed (i.e. transmitted serially) over a single trace. Ex. 1014, 10:24-53, 10:58-11:5, 29:44-58, 30:31-42; Ex. 1002, ¶ 84. Pandey's process

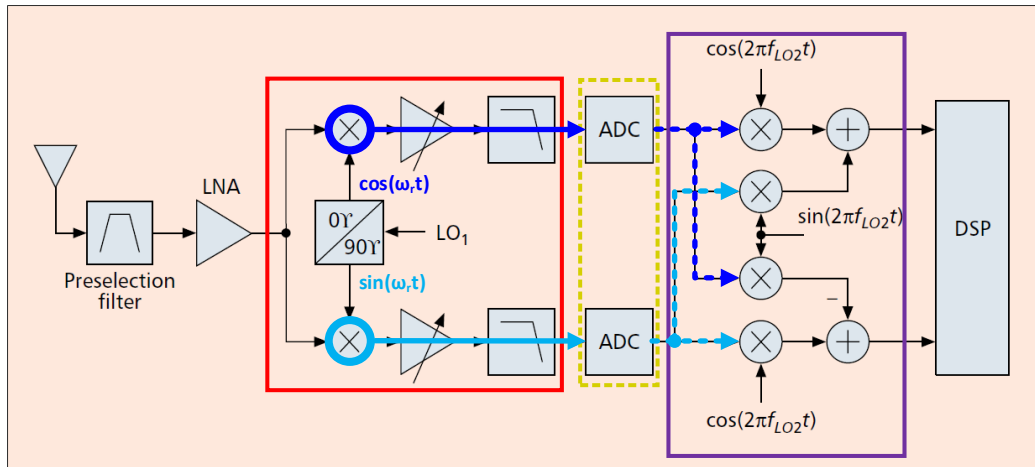
optimizes the design by attempting to reduce the number of signals assigned to each wire (referred to as the multiplexing ratio) between partitions. Ex. 1014, 5:50-53, 6:11-15, 6:44-53; 7:13-19, 29:44-30:9, 30:53-31:12, 31:56-63, Figs. 38-39; Ex. 1002, ¶ 84. Thus, depending upon the partitioning of the circuit design within finite area and finite interconnection of a chip, Pandey's optimization will in some layouts result in signals being grouped and time multiplexed through a serial interface, while in others the signals have individual dedicated traces with no multiplexing, which is a parallel interface. Ex. 1014, 31:20-22, 32:12-15; Ex. 1002, ¶ 84.

Pandey is reasonably pertinent to problems with which the '362 patent is concerned, and thus is analogous art to the '362 patent (and to Zhang) on at least that basis. Ex. 1002, ¶ 85.

C. Mirabbasi

Mirabbasi (Ex. 1018) is a journal article published on November 30, 2000 (Ex. 1073, pp. 78-85), and is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1002, ¶ 86.

Mirabbasi discusses the advantages of using complex mixing when frequency shifting RF signals to a lower frequency to avoid image band problems associated with real mixing. Ex. 1018, p. 5; Ex. 1002, ¶ 87.



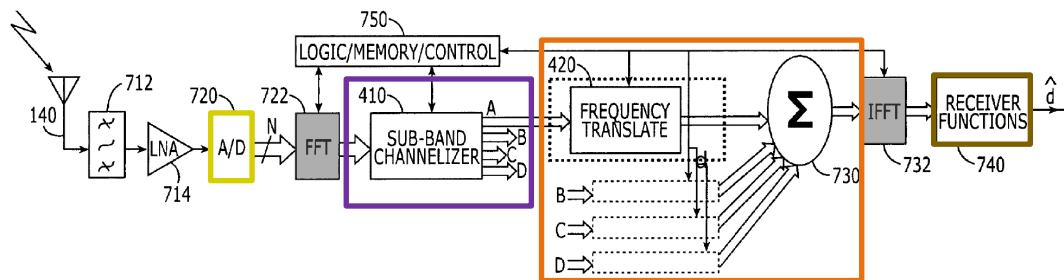
Ex. 1018, Fig. 10 (annotated)

Figure 10 shows an example of a well-known RF receiver architecture, like that in the '362 patent and Zhang, where signals are down-converted (i.e., frequency shifted to a lower frequency) through two mixing stages. Ex. 1018, p. 10; Ex. 1002, ¶ 88. The first mixing stage (**red**) mixes an analog signal with a complex exponential via a complex mixing circuit of two mixers (**dark blue** and **light blue**). Ex. 1018, pp. 6, 10; Ex. 1002, ¶ 88. The real and imaginary outputs of the first mixing stage are called the in-phase (I) and quadrature (Q) components of the frequency-shifted signal (since cosine and sine are in quadrature). Ex. 1018, p. 6; Ex. 1002, ¶ 88. The in-phase (I) and quadrature (Q) components of the frequency-shifted signal are digitized individually by two analog-to-digital converters (**gold**). Ex. 1018, p. 10; Ex. 1002, ¶ 88. The second mixing stage (**purple**) involves a complex mixing circuit with four mixers and two adders and further down-converts the digital in-phase (I) and quadrature (Q) components before forwarding them to the digital signal processor. Ex. 1018, pp. 6, 10; Ex. 1002, ¶ 88.

Mirabbasi discloses wideband receiver systems, the same field of endeavor as the '362 patent, and thus is analogous art. Ex. 1002, ¶ 89.

D. Karabinis

Karabinis (U.S. Pub. No. 2006/0233147, Ex. 1020) published on October 19, 2006, and is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1002, ¶ 90.



Ex. 1020, Fig. 7 (annotated)

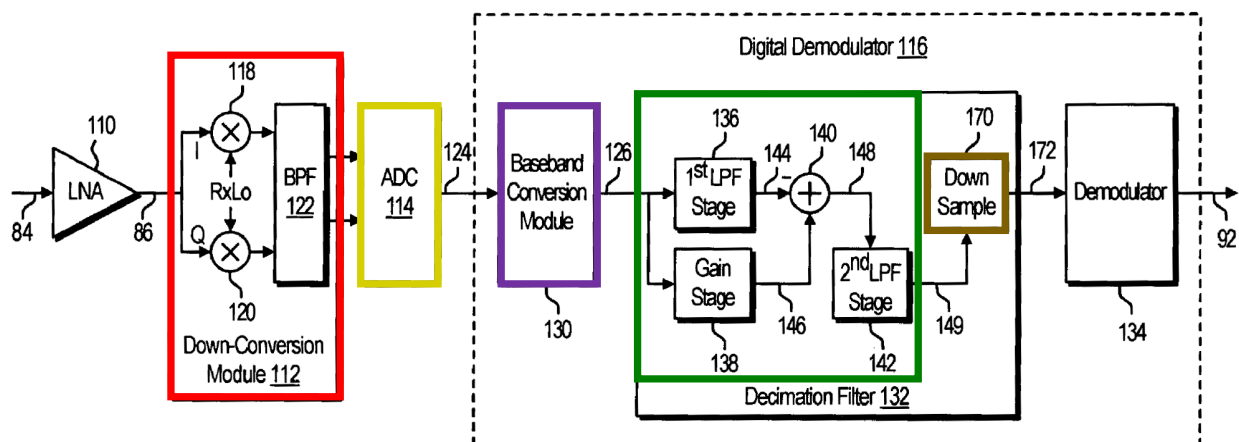
Karabinis describes a receiver, for example, as shown in Figure 7, configured to receive non-contiguous frequency bands and selectively frequency shift the bands to form a contiguous frequency band. Ex. 1020, [0017], [0042]; Ex. 1002, ¶ 91. The receiver comprises an analog-to-digital converter 720 (**gold**) and a Fast Fourier Transformer 722 (**grey**) that act as a digital (discrete-time) time-domain to frequency-domain converter. Ex. 1020, [0015], [0047]; Ex. 1002, ¶ 91. A sub-band channelizer 410 (**purple**) isolates the non-contiguous frequency bands, and the frequency translator 420 (**orange**) translates the isolated bands into one contiguous frequency band. Ex. 1020, [0017], [0049]; Ex. 1002, ¶ 91. An Inverse Fast Fourier Transformer 732 (also **grey**) converts the contiguous frequency band back into the

time domain. Ex. 1020, [0018], [0049]; Ex. 1002, ¶ 91. The receiver functions 740 (**brown**) includes a demodulator 430 that demodulates the contiguous frequency band. Ex. 1020, [0017], [0043], [0049], Figs. 1, 5; Ex. 1002, ¶ 91.

Karabinis relates to wideband receiver systems, the same field of endeavor as the '362 patent, and thus is analogous art. Ex. 1002, ¶ 92.

E. Jensen

Jensen (U.S. Pub. No. 2007/0027943, Ex. 1026) published on February 1, 2007, and is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1002, ¶ 93.



Ex. 1026, Fig. 1 (annotated)

Jensen describes a radio receiver (illustrated in Figure 1 above) that, similar to the receivers in the '362 patent and in Zhang, comprises a down-conversion module 112 (**red**), an analog-to-digital converter 114 (**gold**), a baseband conversion module 130 (**purple**), and a demodulator 134. Ex. 1026, [0024]-[0026]; Ex. 1002, ¶ 94. Jensen additionally discloses a decimation filter 132. Ex. 1026, [0028].

The down-conversion module 112 includes mixers 118 and 120 that mix the inbound RF signals 86 with in-phase (I) and quadrature (Q) components of a receiver local oscillator to produce in-phase and quadrature intermediate frequency (IF) mixed signals. Ex. 1026, [0024]-[0025]; Ex. 1002, ¶ 94. The analog-to-digital converter 114, like the '362 patent, digitizes these signals. Ex. 1026, [0025]; Ex. 1002, ¶ 94. The baseband conversion module 130, like the '362 patent's complex mixers, converts the digital IF signals 124 into digital baseband signals 126. Ex. 1026, [0026]-[0027]; Ex. 1002, ¶ 94. The channel-select decimation filter 132 includes a first low-pass filter stage 136, a gain stage 138, a subtraction module 140, and a second low-pass filter stage 142, which in combination (**green**) filters channel-selected signals 149 from the digital baseband signals 126. Ex. 1026, [0026]-[0027], [0029]; Ex. 1002, ¶ 94. The down-sampling module 170 (**brown**) reduces the sampling rate (also known as decimation) of the channel-select signals 149 to produce down-sampled signals 172. Ex. 1026, [0027]; Ex. 1002, ¶ 94. The demodulator 134 converts the down-sampled signals 172 into inbound digital symbols 92. Ex. 1026, [0027]; Ex. 1002, ¶ 94.

Jensen discloses a radio receiver with digital demodulation, and thus is reasonably pertinent to problems with which the '362 patent is concerned, and thus is analogous art. Ex. 1002, ¶ 95.

**VI. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R.
§ 42.104(B)**

**A. Claims for Which Review is Requested and Grounds on Which
Challenge Is Based**

Petitioner requests review of claims 1–20 on the following grounds.

Ground	References	Basis	Claims Challenged
A	Zhang	§102	1-3, 8, 9, 11-13, 18, 19
B	Zhang	§103	1-3, 8, 9, 11-13, 18, 19
C	Zhang-Pandey	§103	2, 3, 12, 13
D	Zhang-Mirabbasi	§103	1-6, 8-9, 14-16
E	Zhang-Mirabbasi-Karabinis	§103	7, 17
F	Zhang-Jensen	§103	10, 20
G	Zhang-Mirabbasi-Pandey	§103	2-3
H	Zhang-Mirabbasi-Jensen	§103	10

A declaration of David B. Lett is submitted with this petition and includes, e.g., a discussion of Mr. Lett’s background, the ’362 patent, and the prior art, as well as his opinions and an explanation of the bases for those opinions. Ex. 1002, ¶ 1-222. Mr. Lett at least meets the level of skill of a POSITA. *Id.*, ¶¶ 4-16, 31; Ex. 1003.

B. 314(a) Discretion Does Not Apply

The Fintiv factors as set forth in the Director's June 21, 2022 Guidance Memorandum do not warrant discretionary denial.

Factor one appears neutral. Petitioner has filed IPR petitions challenging all eight patents asserted in the District Court in case no. 2:23-cv-01050. If trial is instituted, and the case is not dismissed based on Petitioner's motion to dismiss the Second Amended Complaint, then Petitioner expects to request a stay, as decisions in Petitioner's favor would resolve the dispute in its entirety.

Factor two favors institution. Petitioner has filed a motion to dismiss the District Court case, Patent Owner has filed an Amended Complaint, and Petitioner will renew its Motion to Dismiss in order to seek dismissal of the operative complaint. In addition, no schedule beyond claim construction has been entered, and the Court has not set a trial date.

Factor three favors institution. To date, the investment by the District Court has been limited to considering motions to dismiss on the pleadings.

Factor four strongly favors institution. The petition challenges all claims in the '362 patent while only claims 11 and 12 are asserted in the District Court.

Factor five does not warrant denial as Petitioner is a defendant in the District Court case.

Factor six favors institution. Petitioner presents compelling unpatentability challenges that merit institution, relying on entirely different prior art than that considered during prosecution or argued in the pending *ex parte* reexamination.

C. 325(d) Discretion Does Not Apply

Considering the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Pap. 6, *8-9 (PTAB Feb. 13, 2020), the Board should not exercise its §325(d) discretion to deny institution. The grounds raised by this Petition are not the same or substantially the same as the art and arguments raised during prosecution, and to the extent that they are, the Examiner erred in a manner material to the patentability of the challenged claims by failing to find and consider all of the relevant prior art, including Zhang, that teach Element [1D]. Ex. 1004 at 107.

D. Level of Ordinary Skill

A person of ordinary skill in the art (a “POSITA”) at the time of the alleged invention would have had a degree in electrical engineering or a similar discipline, along with three-to-four years of experience with digital signal processing and RF tuning for satellite and/or cable digital communications. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. Ex. 1002, ¶¶ 30-32.

E. Claim Construction

All claim terms herein should be given their ordinary and customary meaning to a POSITA as they would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b).

1. “digitizing,” “selecting,” “outputting”

In the TX litigation, the District Court construed claim 11 as requiring that the “‘digitizing ...’ step must be performed before the ‘selecting ...’ step, and the ‘selecting ...’ step must be performed before the ‘outputting ...’ step,” but with “[n]o other order of steps” required. Ex. 1029, p. 52; Ex. 1002, ¶ 35.

2. “wideband” and “wideband analog-to-digital converter (ADC) module”

In the TX litigation, Patent Owner agreed that “wideband analog-to-digital converter (ADC) module” should be given its plain and ordinary meaning. Ex. 1029, pp. 7-8. Consistent with its ordinary meaning, the ’362 patent defines “wideband” as a band that carries multiple channels. For example, the ’362 patent states that a

receiver is “wideband” if it is “designed to concurrently receive several TV channels.” Ex. 1001, 1:25-27; Ex. 1002, ¶¶ 34.⁴

3. “digital circuitry”

To the extent “digital circuitry” of claim 1 is construed to be a means-plus-function term under 35 U.S.C. 112, paragraph 6, and to the extent the ’362 patent discloses corresponding structure for this limitation, that structure is illustrated in Figures 2 and 3, including complex mixers 250 and 300, and filters 260, 330, and 340. Ex. 1001, Figs. 2-3, 5:31-54, 6:7-58; Ex. 1002, ¶¶ 33-34.

⁴ The ’362 Patent also states that “the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum.” Ex. 1001, 18-21. “Non-contiguous portions” is omitted from the independent claims and added only in dependent claims 7 and 17, but should they be implicitly required of a “wideband receiver,” Zhang discloses them as presented below.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Grounds A/B: Claims 1-3, 8, 9, 11-13, 18, and 19 are Anticipated and Rendered Obvious by Zhang.

As set forth below, Zhang anticipates and renders obvious claims 1-3, 8, 9, 11-13, 18, and 19. Ex. 1002, ¶¶ 96-157.

1. Independent Claim 1

Elements [1A]-[1E] are taught by Zhang.

a. [1A] “A wideband receiver system comprising:”

While the preamble [1A] is not limiting,⁵ Zhang discloses it. Zhang describes “a wide-band receiver” for use in digital set-top boxes, PVRs, and home media centers. Ex. 1013, [0045]-[0047]; Ex. 1002, ¶¶ 98-99. Zhang’s multi-channel demodulator 200 illustrated below in Figure 2 receives an RF signal in a frequency band that carries multiple RF channels, with each channel having data streams modulated on a carrier signal. Ex. 1013, [0023]-[0024], [0041]-[0045], Figs. 2, 6-8; Ex. 1001, 1:24-27 (describing “wideband” as a band that carries multiple channels); Ex. 1002, ¶¶ 34, 99-100; Section VI.E, *supra*. The RF channels received by Zhang’s receiver are similar to those in ’362 patent (e.g., 32 channels in Zhang and 10

⁵ The limitations of the claims appear and are labelled in the Claims Listing Appendix.

channels in the '362 patent), within similar frequency bands (e.g., 192MHz in Zhang and 80Mhz in the '362 patent), where some of the channels are desired and some are not desired. *Compare* Ex. 1013, ¶ [0032], [0041]-[0042], [0048], claim 34, 37 with Ex. 1001, 4:16-31.

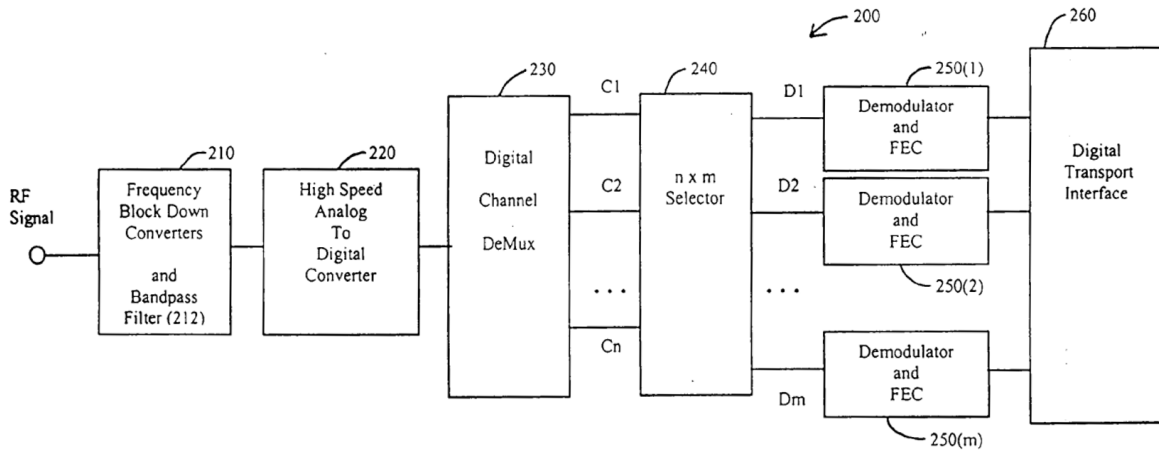


Fig. 2

Ex. 1013, Fig. 2

To the extent Patent Owner argues that Zhang’s receiver is not “wideband,” because it does not expressly disclose receiving desired channels in non-contiguous frequency bands, at the very least this would have been obvious, because as further discussed below, Zhang does not limit the frequencies of the channels a user selects within the received frequency bandwidth, and because Zhang discloses that the desired channels “can be in different frequency bands [and] need not be contiguous.” *Compare* Ex. 1013, ¶ [0048] with Ex. 1001, 4:28-31; Ex. 1002, 100 . Since Zhang’s receiver is capable of receiving any channel within the digitized frequency spectrum,

a POSITA would have had a high expectation of success using Zhang’s receiver for receiving non-contiguous desired channels.

- b. [1B] “a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”

Zhang discloses the claimed “mixer module,” for example, frequency block down converter 210 (red). Ex. 1002, ¶¶ 101-102.

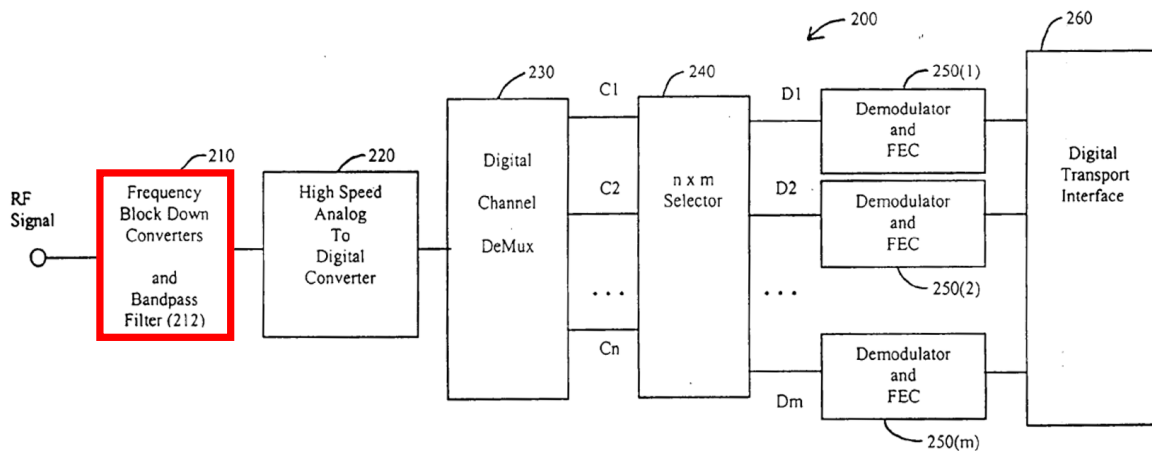


Fig. 2

Ex. 1013, Fig. 2 (annotated)

Like the mixer module of the '362 patent, Zhang’s down converter 210 multiplies (i.e. mixes) an incoming RF signal with a reference signal to downconvert the RF signal to a lower frequency band. Compare Ex. 1013, [0025] (“the multi-channel analog RF signal is multiplied by a reference signal to a lower frequency band”), claim 1 with Ex. 1001, 4:41-46 (“mixers 211 and 221 multiplies (mixes) an

amplified RF signal 203 with a respective first oscillator frequency”); Ex. 1002, ¶¶ 65-66, 102; *see also* Ex. 1018, Fig. 1, p. 5 (“frequency downconversion ... is performed by multiplying (mixing) the signal with a sinusoid such as $\cos(2\pi f_{\text{Lot}})$ ”).

The RF signal includes multiple RF carrier signals that each includes one or more TV content channels from a TV system. Ex. 1013, [0005], [0023]-[0025], [0029], [0041], claims 13, 27-30, 33; Ex. 1002, ¶¶ 103-104. Just as in the ’362 patent, some of Zhang’s RF carrier signals are “target” RF channels (the claimed “desired television channels”) that are selected by the subscriber for demodulation, and some are undesired RF channels (the claimed “undesired television channels”) which are later filtered out. *Compare* Ex. 1013, [0032], [0025], [0028], claims 2, 4, 34, 36, 37 *with* Ex. 1001, Abstract, 5:49-54, 6:32-34; 6:55-64; Ex. 1002, ¶¶ 103-106. Thus, Zhang teaches Element [1B]. Ex. 1002, ¶¶ 101-107.

To the extent Patent Owner argues that Zhang does not disclose the claimed “mixer module,” including a mixer module in Zhang’s down converter 210 would have been obvious, because such devices were “conventional,” as the ’362 patent admits. Ex. 1002, ¶¶ 38, 64-68, 107; Ex. 1007, p. 5; Ex. 1001, 1:5-11. Because mixer modules were “conventional,” a POSITA would have had a high expectation of success implementing them to perform Zhang’s downconversion.

- c. [1C] “a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”

Zhang discloses the claimed “wideband analog-to-digital converter (ADC) module” as ADC 220 (gold). Ex. 1002, ¶¶ 108-110.

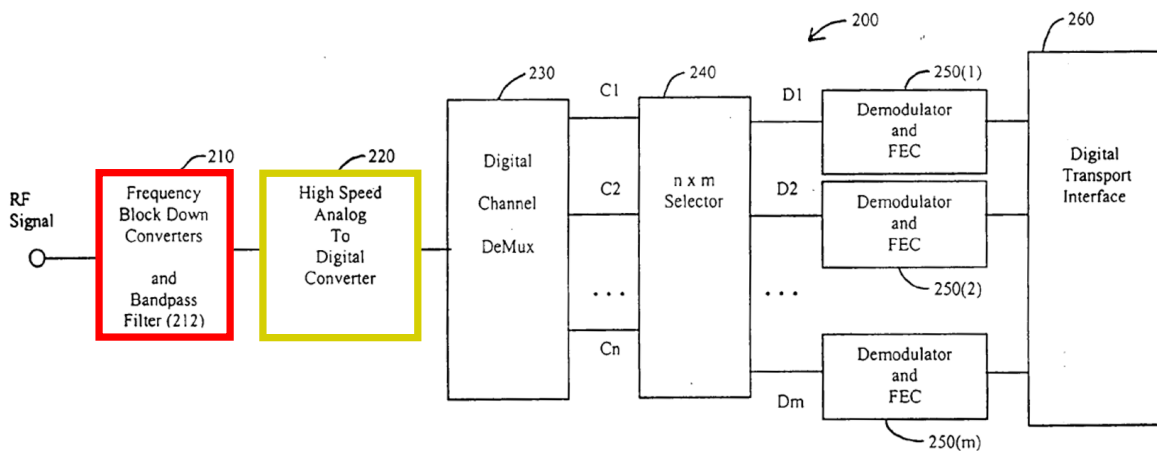


Fig. 2

Ex. 1013, Fig. 2 (annotated)

ADC 220 receives the down-converted multi-channel analog RF signal including desired and undesired channels, and converts the “entire signal band” to a multi-channel digital RF signal. *Compare* Ex. 1013, [0027]-[0028], [0042], claim 8 *with* Ex. 1001, 4:19-25, 4:51-54, 5:19-31 (describing ADC digitizing the down-converted RF signal at “low-IF band”); *see also* Ex. 1013, Abstract, [0010], [0025], [0031]-[0032], [0034], [0041]-[0042], claims 1, 2, 4, 7, 28, 34, 36, 37; Ex. 1002, ¶¶ 108-109.

Zhang’s ADC is “wideband” because it digitizes several channels within the frequency block concurrently. *Compare* Ex. 1013, [0010], [0025], [0027] *with* Ex.

1001, 1:24-27; Ex. 1002, ¶ 109. Thus, Zhang teaches Element [1C]. Ex. 1002, ¶¶ 108-110.

To the extent Patent Owner argues that Zhang’s ADC 220 is not wideband, for example, because it does not expressly disclose digitizing desired channels in non-contiguous frequency bands, at the very least this would have been obvious, because as further discussed below (*see* Sections VII.D.1.b, VII.F.1), Zhang does not limit the frequencies of the channels a user selects within the digitized bandwidth, and because Zhang discloses that the desired channels “can be in different frequency bands [and] need not be contiguous.” *Compare* Ex. 1013, ¶ [0048] *with* Ex. 1001, 4:28-31; Ex. 1002, 110 . Since Zhang’s receiver is capable of selecting any channel within the digitized frequency spectrum, a POSITA would have had a high expectation of success using Zhang’s receiver for selecting non-contiguous desired channels.

- d. [1D] **“digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.”**

Zhang teaches the claimed “digital circuitry” as Digital Channel Demultiplexer 230, either alone, or in combination with all or part of Digital Selector 240 (**purple**). Ex. 1002, 111-125. In Zhang these are implemented with “standard

process CMOS,” a well-known type of digital logic integrated circuit. Ex. 1013, [0044], [0048]; Ex. 1016, pp.17-19, 53-54; Ex. 1002, ¶ 112.

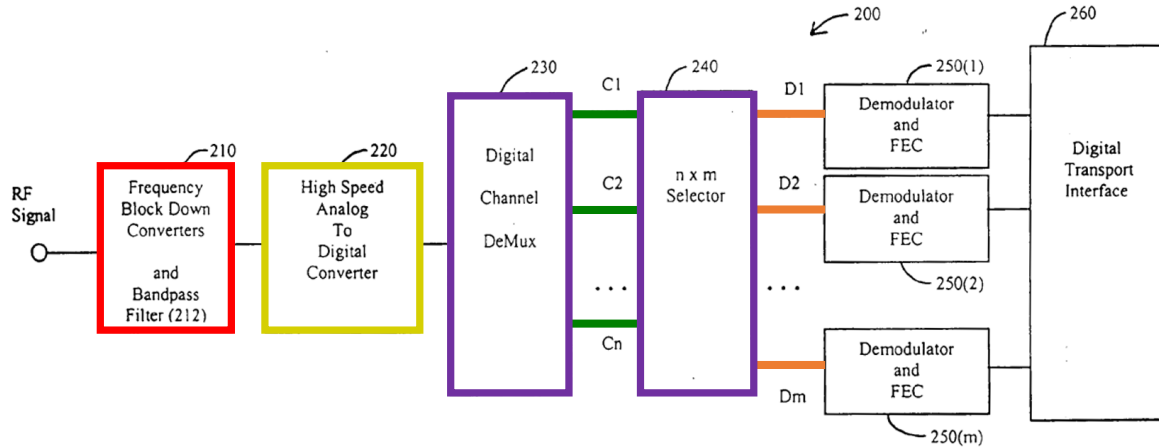


Fig. 2

Ex. 1013, Fig. 2 (annotated)

Digital Channel Demultiplexer 230 receives the multi-channel digital RF signal from ADC 220 and selects from this signal a number “n” of desired channels $C_1 - C_n$ (green), each at a unique “target” RF channel. Ex. 1013, [0028], [0030]-[0032], claims 1, 2, 10-11, 13, 17, 21, 23, 27-28, 30, 33-34, 36, 41, Figs. 2-3; Ex. 1002, ¶ 113. “RF channels C_1 to C_n contain content channels that are selected or used by a subscriber.” Ex. 1013, [0028], [0030]-[0032], [0042], claims 34, 36-41; Ex. 1002, ¶¶ 113-114.

As shown below, Zhang uses the same technique described in the ’362 patent for selection and outputting of desired channels $C_1 - C_n$: first using a bank of complex mixers (purple) to frequency-shift a digitized version of the downconverted wideband signal so that each mixer outputs a different desired channel shifted to

baseband (0 Hz), and then using low pass filters (**green**) to filter out the undesired channels so that only the desired channels remain.

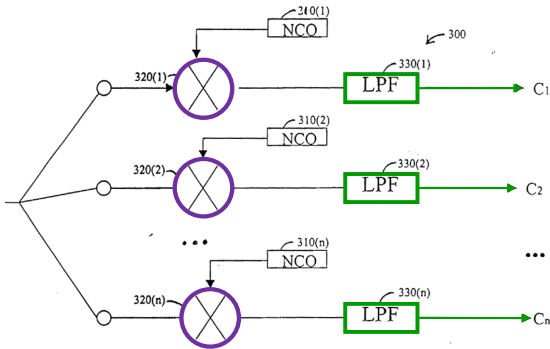
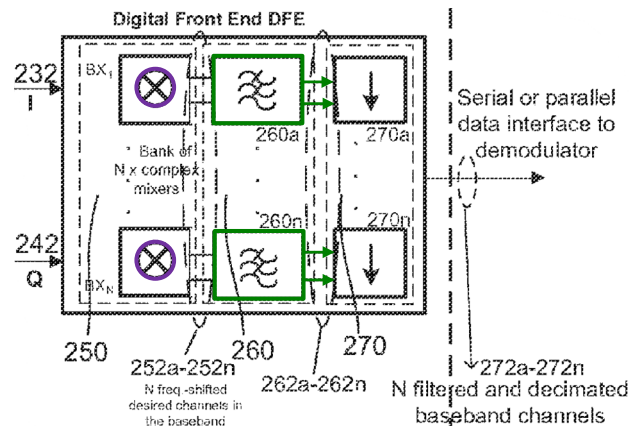


Fig. 3

Ex. 1013, Fig. 3 (annotated)



Ex. 1001, Fig. 2 (annotated)

Ex. 1002, ¶¶ 113-116; *Compare* Ex. 1001, 2:51-55, 5:49-6:54 (“Each of the N complex mixers 250 receives the digital signals I 232 and Q 242 from ADCs 218 and 228 to extract a different one of the desired channels and frequency-shifts the extracted signals to the baseband frequency. Each of the frequency shifted desired channels 252 is filtered by an associated filter module (identified as 260a to 260n).”) *with* Ex. 1013, [0027], [0030] (“Digital tuner 300 includes a bank of ... complex multipliers 320(1 . . . n), and low-pass filters (LPFs) 330(1 . . . n). One chain of each of these elements is used for each RF channel.”), [0031] (“[t]he same multi-channel RF signal from the ADC enters each multiplier”), [0032] (“the target RF channel is shifted to a baseband, i.e., centered at DC. LPFs 330(1 . . . n) ... each filters out all RF channels except for its target RF channel.”); *see also* Section VII.A.3 (claims 8 and 9), *infra*.

Each of the desired channels is output by Digital Channel Demultiplexer 230 as a parallel digital data stream on parallel paths C_1 to C_n (green) to “one or more” shared demodulators 250(1)-250(m) via Bus Selector 240. *Compare* Ex. 1013, Figs. 2-3, [0029], [0032], claims 2-5, 9 *with* Ex. 1001, 6:55-58 (“N desired baseband channels will be sent as a serial or parallel digital data stream . . . according to commonly known methods, as shown in FIG. 2.”). Ex. 1002, ¶¶ 117-118, 121.

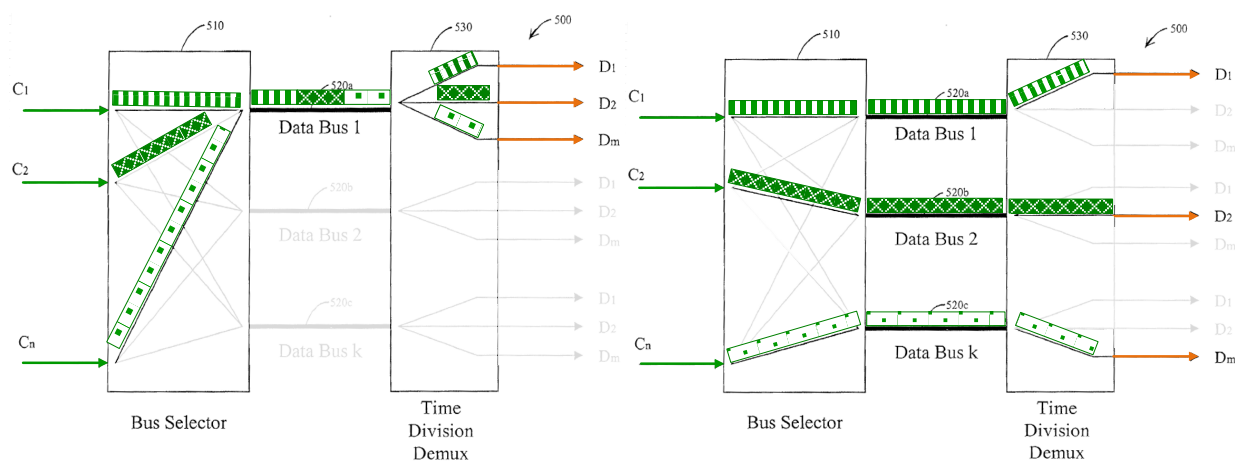
Thus, Digital Channel Demultiplexer 230 teaches Element [1D].

Alternatively and in addition, Digital Channel Demultiplexer 230 in combination with all or part of Digital Selector 240 also discloses Element [1D]. Digital Selector 240 selects channels $D_1 - D_m$ (which comprise any or all of channels $C_1 - C_n$) to output as a digital data stream to “one or more” demodulators 250(1) – 250(m). Ex. 1013, [0028]-[0029], [0038]-[0039], [0047], claims 2-4, Fig. 3; Ex. 1002, ¶¶ 119. For $m=n$, all of the selected channels are concurrently output to one or more demodulators, and for $m<n$, the user may output some or all n channels to the demodulator, just not concurrently. Ex. 1013, [0028]-[0029], [0038]-[0039] claims 2-4, 9, 31-32; Ex. 1002, ¶ 119. By switching through the demultiplexed channels $C_1 - C_n$ selected by the user, Digital Selector 240 provides the subscriber with fast channel search capabilities. Ex. 1013, [0005], [0028], [0047], claims 3, 30; Ex. 1002, ¶¶ 119.

Where $D_1 - D_m$ includes all $C_1 - C_n$, Digital Channel Demultiplexer 230 selects the desired channels and filters out the undesired channels as described above. Ex. 1002, ¶ 120. Alternatively, where $D_1 - D_m$ includes less than all channels $C_1 - C_n$, the combination of Digital Channel Demultiplexer 230 and Digital Selector 240 teaches the claimed selecting of the desired channels, in that a channel that is both demultiplexed by 230 and switched by 240 to a demodulator is “desired” and all other channels from the digital multi-channel RF signal are “undesired.” Ex. 1013, [0028] (“digital selector 240 ... selects one or more of the RF channels D_1 to D_m from one or more of the digital RF channels C_1 to C_n . RF channels C_1 to C_n contain content channels that are selected or used by a subscriber.”), [0029] (“demodulators 250(1... m) demodulate only the RF channels that are selected by digital selector 240”), [0030], [0032]-[0033], [0040], [0042], [0048], claims 36-37; Ex. 1002, ¶ 120.

Zhang also discloses that Digital Selector 240 is configured to output the claimed “digital data stream” with its bus selector 510, which receives channels C_1 to C_n and sends the channels across one or more clocked data buses. Ex. 1013, Fig. 5, [0038]-[0039]; Ex. 1002, ¶ 121. As Zhang explains, “each bus can be used by multiple RF channels with the use of time division multiplexing . . . and each output RF signal from a channel demultiplexer (not shown) can be selected to use any data bus.” Ex. 1013, Fig. 5, [0038]-[0039]. Zhang’s digital selector is shown annotated below (left) sending the selected channels using “time division multiplexing” (i.e.,

alternating data from each channel sequentially) across one bus in a serial digital data stream, and shown annotated below (right) sending the selected channels “through different data buses” in a parallel digital data stream. *Id.* Ex. 1002, ¶ 122, 126-136; Ex. 1016, pp. 79-80 (Figure 6-25); *see also* Section VII.A.2 (Claims 2 and 3 parallel and serial interfaces), *infra*. These are the same methods for outputting a digital data stream that the ’362 patent describes as “commonly known.” Ex. 1001, 6:55-58; Ex. 1002, ¶ 122.



Ex. 1013, Fig. 5 (annotated)

From the selector, Zhang discloses that the digital RF channels in the digital data stream are received and demodulated by “one or more demodulators,” and that multiple demodulators may be “shared demodulators” with common functional blocks. Ex. 1013, claim 1, *see also* [0029], [0038]-[0039], [0047], claims 4, 9, 31-32; Ex. 1002, ¶¶ 123-124.

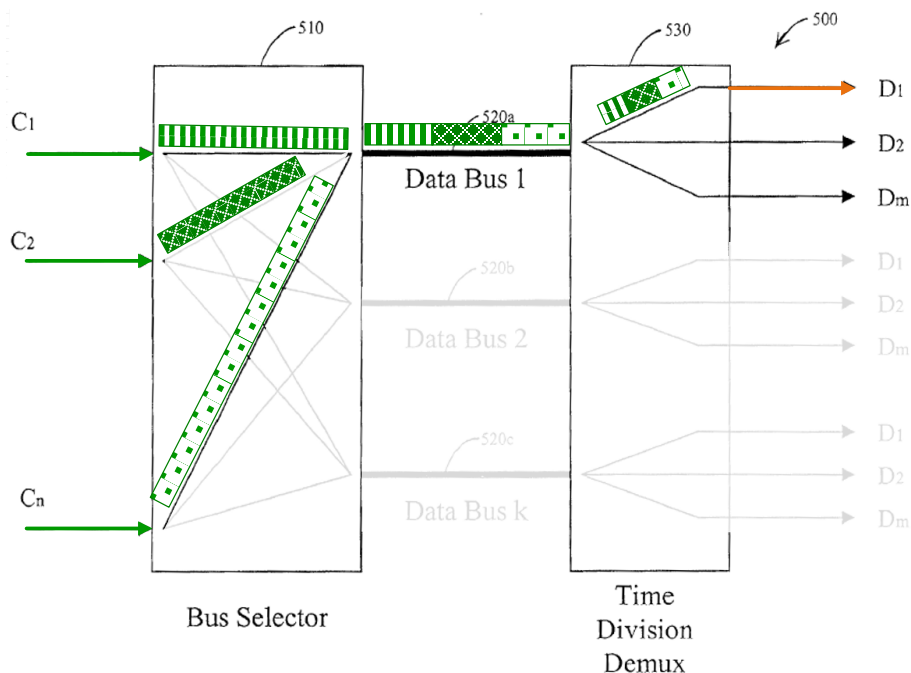
The ’362 patent uses the term “demodulator” generally to refer to a device that is a single unit for demodulating a respective single channel, a device that

includes multiple other devices to demodulate multiple channels, and a device that demodulates multiple channels, without any specificity as to its structure. Ex. 1001, 5:44-48, 5:54-60, 6:55-58, 7:66-8:9, 9:25-27; Ex. 1002, ¶ 124. Thus, a POSITA would have understood that either of Zhang’s embodiments—“one” demodulator or shared demodulators with common functional blocks—teach the claimed “demodulator.” Ex. 1002, ¶¶ 74, 124. Thus, Zhang teaches Element [1D].

To the extent Patent Owner argues that Element [1D] requires the digital circuitry to output all of the desired television channels as a digital datastream to only a single separate demodulator, such as one of Zhang’s demodulator 250, and that Zhang does not disclose this, having Zhang’s single demodulator 250 demodulating all desired channels would have been obvious. As Zhang explains, each bus in digital selector 240/500 “can be used by multiple RF channels” and “each data bus provides data to multiple demodulators.” Ex. 1013, ¶ [0039], Fig. 5; Ex. 1002, ¶ 125.

For example, as shown below, selector 500 is capable of outputting every channel C_1 - C_n (green) to D_1 (orange), using time-division multiplexing as discussed above and further discussed below with respect to claim 2. *See* Section VII.A.2, *infra*; Ex. 1013, [0029], [0038]-[0039]; Ex. 1002, ¶ 125. Zhang’s selector 500 could also use separate buses to route each channel to D_1 as discussed above and further

discussed below with respect to claim 3. Ex. 1013, [0029], [0038]-[0039]; *See* Section VII.A.3, *infra*; Ex. 1002, ¶ 125.



Ex. 1013, Fig. 5 (annotated)

A POSITA would thus understand that Zhang's system is capable of routing all desired channels in a digital data stream to a single demodulator 250. Ex. 1002, ¶ 125. Further, a POSITA would have been well aware that single demodulators at the time, such as demodulator 250 in Zhang, were capable of demodulating multiple selected channels. Ex. 1002, ¶ 74, 125; Ex. 1076, Abstract, 2:28-52, 3:6-17, 4:21-32, 6:19-37, Figs. 1a, 1b, 2; Ex. 1019, 1:67-2:7, 2:32-41, 2:50-63, 3:50-52, Figs. 1-2; Ex. 1075, Abstract, 6:14-22, 7:15-20, 32:53-33:14. The use of a single demodulator would beneficially reduce cost of the system, and enable certain functionality, such as providing a transport stream including two demodulated

television channels for picture-in-picture decoding, providing motivation to use this capability of Zhang. Ex. 1076, 2:13-26, 2:53-59; Ex. 1002, ¶ 74. Thus, to the extent Zhang's receiver is argued to not explicitly disclose outputting the plurality of desired channels as a digital data stream to a single demodulator 250, it would obviously do so. Ex 1002, ¶¶ 74, 125. Such a modification would have been simply combining prior art elements (Zhang's single demodulator and Zhang's multiple desired channels) according to known methods (Zhang's routing of all desired channels to a single demodulator) to yield predictable results (demodulating multiple desired channels). Using a single demodulator to demodulate multiple channels was well within the skillset of a POSITA, leading to a high expectation of success. Ex. 1002, ¶ 125. Thus, Zhang also renders obvious even this narrow construction of Element [1D].

For the reasons stated above, Zhang anticipates (ground A) and renders obvious (ground B) claim 1. Ex. 1002, ¶ 125.

2. Dependent Claims 2 and 3

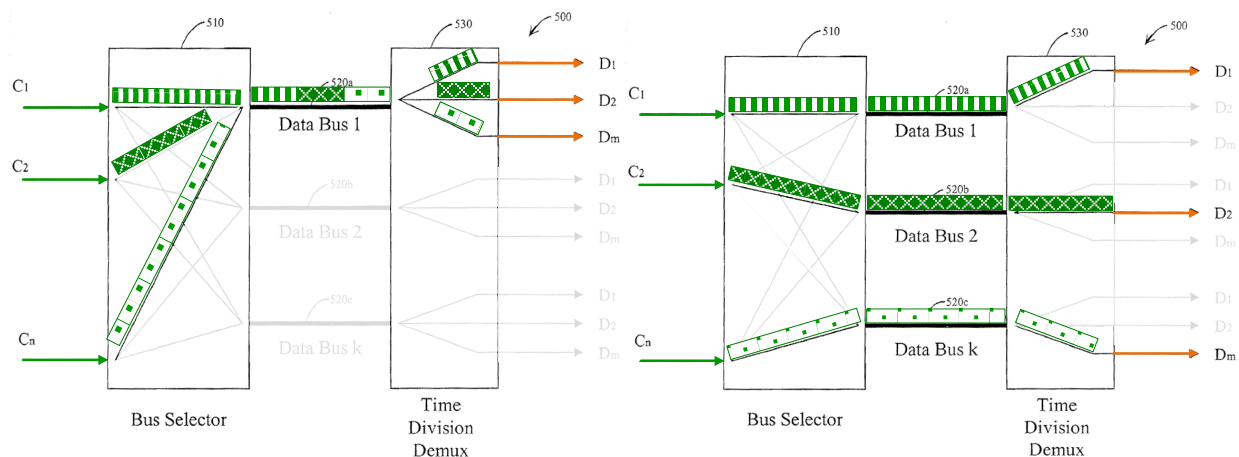
[2] “The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.”

[3] “The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.”

Zhang discloses claims 2 and 3. Ex. 1002, ¶¶ 126-136. As discussed above, Zhang's digital channel demultiplexer 230 alone, or in combination with selector

240, discloses Element [1D] (“digital circuitry configured: . . . to output ... as a digital datastream”). These components select one or more digital RF channels $C_1 - C_N$, and output any or all of these selected channels as $D_1 - D_M$ to one or multiple shared demodulators via one or more data buses 520 in Figure 5. Ex. 1013, [0029], [0038]-[0039]; Ex. 1002, ¶ 128.

Zhang describes the buses being used to: 1) send the selected channels across one bus “with the use of time division multiplexing,” and/or 2) send the selected channels “through different data buses.” *See* Section VII.A.1.d, *supra*. These two scenarios are illustrated below. Ex. 1013, [0038]-[0039]; Ex. 1002, ¶¶ 121-123, 129. As shown on the left, one bus (e.g., Data bus 1) receives data from each selected channel (represented by green blocks with different cross hatch patterns) and sends the data from the different channels sequentially in different time intervals (i.e., time division multiplexing). Ex. 1013, [0038]-[0039]; Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1002, ¶¶ 121-123, 129. As shown on the right, data from each bus is sent through a separate data bus. Ex. 1013, [0038]-[0039]; Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1002, ¶¶ 121-123, 129.



Ex. 1013, Fig. 5 (annotated)

A POSITA would have understood that Zhang’s single bus using time-division multiplexing teaches digital circuitry configured to output the digital datastream “via a serial interface” as recited in claim 2, and that using multiple buses, one per selected channel, teaches digital circuitry configured to output the digital datastream “via a parallel interface” as recited in claim 3. Ex. 1013, [0038]-[0039]; Ex. 1002, ¶¶ 75-77, 130-135 (citing Ex. 1014, 30:31-42, 31:15-22; Ex. 1016, pp. 79-80; Ex. 1017, pp. 354-355).

A POSITA would have understood that a digital integrated circuit represents data as binary units (“bits”) in the form of electrical signals (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1002, ¶ 133 (citing Ex. 1016, pp. 31-34, *see also* 48-51, 80 (Figure 6-25)). As shown below (as taken from the textbook “Digital Integrated Circuits: A Design Perspective” published in 1996 (“Rabaey”)), to output multiple bits (e.g., from multiple channels), the circuit can either transmit the bits over multiple separate wires, one wire for each bit, which was

known as a “parallel interface,” or the circuit can transmit the set of bits one at a time as sequential pulses over a single wire, according to a fixed sequence, which was known as a “serial interface” Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1002, ¶ 134.

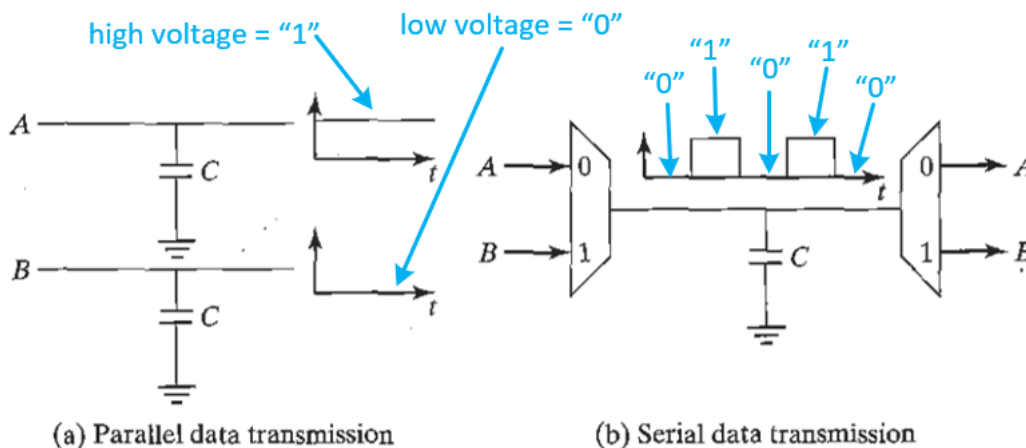


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1016, p. 80 (Figure 6-25) (annotated)

As shown in Zhang’s annotated Figure 5 above, Zhang implements serial and parallel interfaces as those terms were known in the art. Ex. 1002, ¶¶ 75-77, 135. Thus, Zhang anticipates (ground A) and renders obvious (ground B) claims 2 and 3.

To the extent Patent Owner argues that Zhang does not disclose serial and parallel interfaces, implementing Zhang’s digital circuitry to output the selected channels to demodulators 250 (either to an individual demodulator or to shared demodulators) via either option would have been obvious as one of two conventional design choices that were well known and used by POSITAs in integrated circuits designs at the time. Ex. 1002, ¶ 136; Ex. 1014, 30:31-42, 31:15-22; Ex. 1016, pp.

79-80; Ex. 1017, pp. 354-355. As the '362 patent concedes, outputting a digital data stream via serial (claim 2) or parallel (claim 3) interfaces were “commonly known methods,” i.e., Applicant Admitted Prior Art (AAPA). Ex. 1001, 6:55-58; Ex. 1002, ¶ 136.

Zhang’s circuit may be implemented “using standard-process CMOS,” which as described in Rabaey, can either transmit the bits over multiple separate wires (a parallel interface), or over one wire (a serial interface) Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1002, ¶¶ 133-134. Thus, a POSITA implementing the Zhang circuit in CMOS would have selected either or both of these options, both being obvious to try as identified, predictable choices, having a high expectation of success. Ex. 1002, ¶¶ 133-134, 136.

Zhang thus renders obvious claims 2 and 3 for this reason also.

3. Dependent Claims 8 and 9

[8] “The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.”

[9] “The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.”

Zhang discloses claims 8 and 9. Ex. 1002, ¶¶ 137-140. Zhang’s Demultiplexer 230 (included in the claimed “digital circuitry”) comprises a plurality of finite impulse response (FIR) channel filters that, like the filters in the '362 patent,

perform the claimed selection by allowing only the desired channels to pass, while blocking the undesired channels. Compare Ex. 1013, Fig. 3 (filters 330), [0030]-[0034], claims 37-40 with Ex. 1001, Fig. 2 (filters 260), 5:49-58, 6:43-54; Ex. 1002, ¶ 138.

Specifically, Zhang’s Demultiplexer 230 (below left), which is strikingly similar to the ’362 patent’s digital front end 230 (below right), includes a signal path for each the plurality of desired channels $C_1 - C_n$, with each path including a complex multiplier 320 (purple) (also known as a complex mixer) followed by a FIR low pass filter (LPF) 330 (green). Ex. 1013, [0030]-[0032], claims 21-22, 37-40; Ex. 1001, Fig. 2 (filters 260), 5:49-58, 6:43-54; Ex. 1002, ¶¶ 138-139.

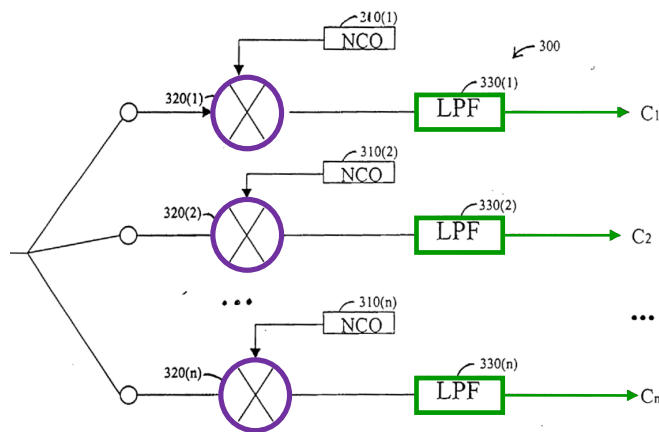
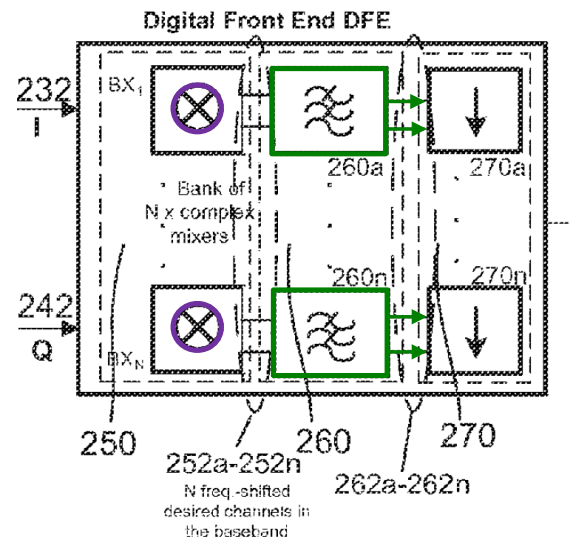


Fig. 3

Ex. 1013, Fig. 3 (annotated)



Ex. 1001, Fig. 2 (annotated)

The multi-channel RF signal enters each multiplier 320, which shifts the frequency of the signal (which includes desired and undesired channels) such that the “target” frequency of one of the desired channels is re-centered to baseband (i.e.,

0 Hz). Ex. 1013, [0031]-[0032]; Ex. 1002, ¶ 140. FIR LPF 330 then selects the desired channel at baseband by passing it to the output (e.g. C₁), while filtering out the remaining channels in the signal. Ex. 1013, [0031]-[0032]; Ex. 1002, ¶ 140. Zhang thus anticipates and renders obvious claims 8 and 9. Ex. 1002, ¶¶ 137-140.

4. Independent Claim 11

Elements [11A]-[11E] repeat the required functionality of Elements [1A]-[1D] as method steps performed by identical structural elements. Ex. 1002, ¶¶ 141-149. Thus, claim 11 is directed to substantially identical subject matter as claim 1 and is anticipated and rendered obvious by Zhang for the same reasons discussed above with respect to claim 1. *See* Section VII.A.1, *supra*.

5. Dependent Claims 12-13, 18-19

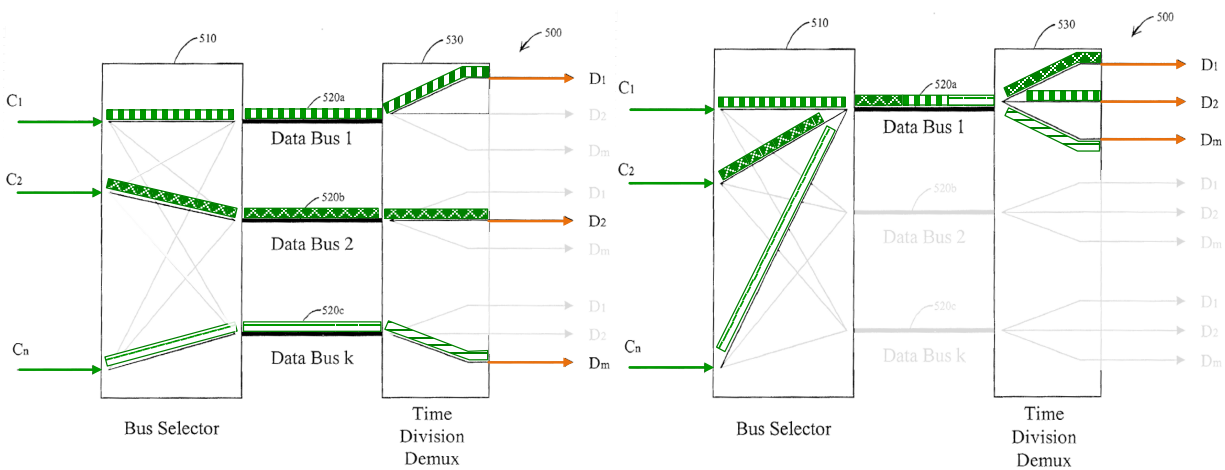
Claims 12 and 13 repeat the functionality of claims 2 and 3 as method steps performed by identical structural elements. Ex. 1002, ¶¶ 152-154. Claims 12 and 13 are anticipated and rendered obvious by Zhang for the same reasons discussed above with respect to claims 2 and 3. *See* Section VII.A.2, *supra*.

Claims 18 and 19 likewise are directed to substantially identical subject matter as claims 8 and 9, respectively, and thus are anticipated and rendered obvious by Zhang for the same reasons discussed above with respect to claims 8 and 9. Ex. 1002, ¶¶ 155-157; *see* Section VII.A.3, *supra*.

B. Ground C: Claims 2, 3, 12, and 13 are Rendered Obvious by Zhang-Pandey.

1. Dependent Claims 2 and 3

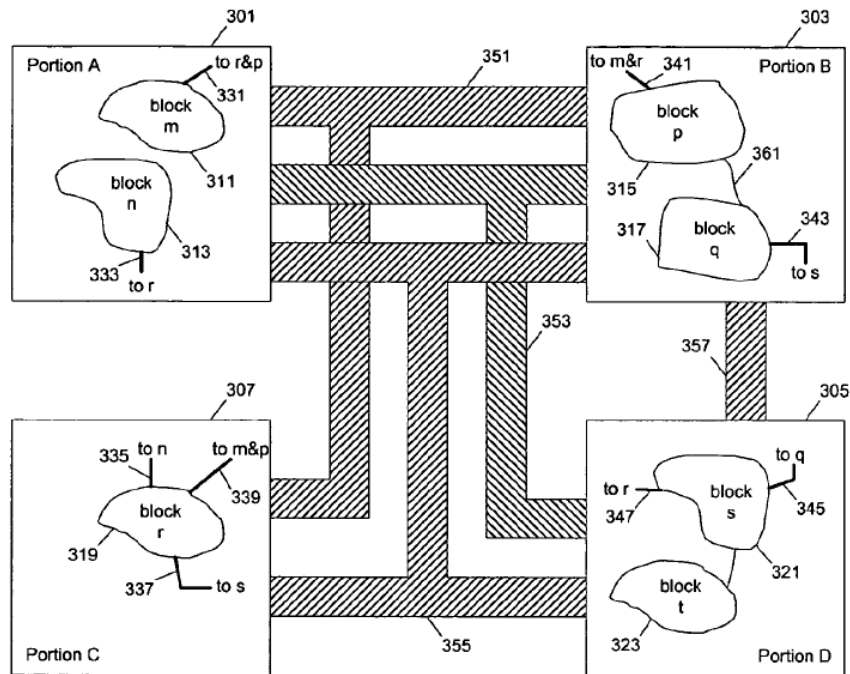
As described above, Zhang's digital selector implements both the serial and parallel interfaces of claims 2 and 3 to output a digital data stream of the selected channels, and to any extent it does not, such implementation would have been obvious based on Zhang in view of a POSITA's background knowledge (including the '362 patent's AAPA). See Section VII.A.2, *supra*; Ex. 1002, ¶¶ 126-136, 159; Ex. 1013, [0038]-[0039]; Ex. 1001, 6:55-58; Ex. 1014, 30:31-42, 31:15-22; Ex. 1016, 79-80; Ex. 1017, 354-355.



Ex. 1013, Fig. 5 (annotated)

In addition, Pandey teaches creating specific serial and parallel interfaces when implementing a digital circuit design (e.g., such as Zhang's digital circuitry) on a FGPA or ASIC chip. Ex. 1014, Abstract, 1:15-55, 2:4-12; Ex. 1002, ¶ 160. The process involves partitioning functional blocks (such as Zhang's channel

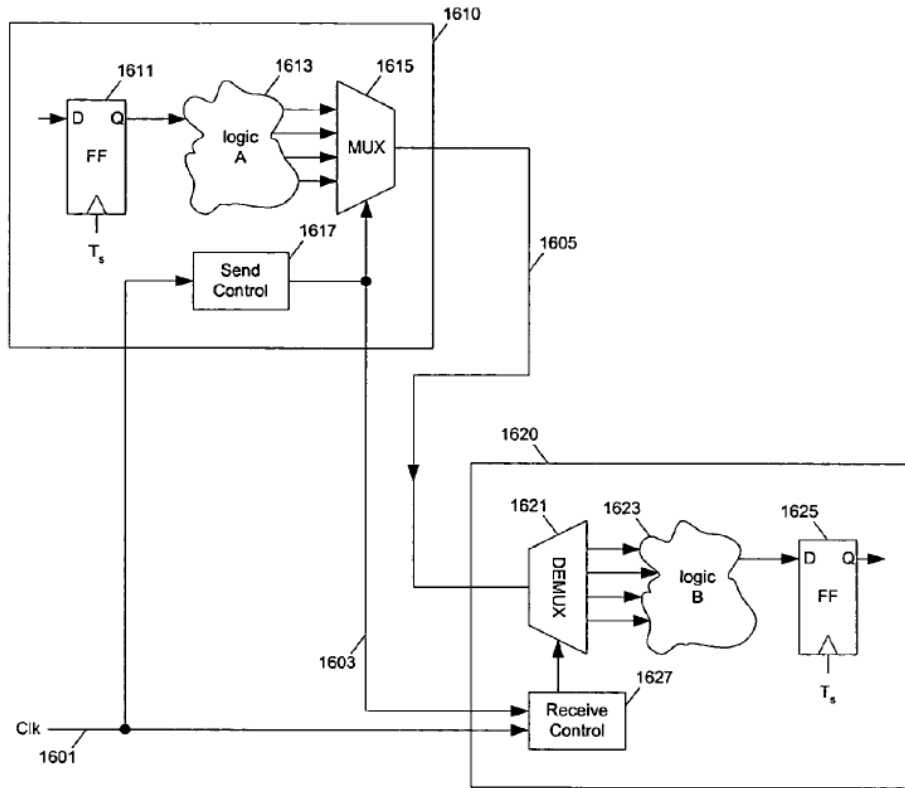
demultiplexer 230, digital selector 240, and demodulators 250) to different regions of an integrated circuit chip (e.g., 301, 303, 305, 307) and assigning wire traces (e.g., 351, 353, 355, 357) to interconnect the partitioned blocks. Ex. 1014, 1:56-60, 2:6-12, 2:64-3:5, 6:10-15, 11:6-19, 13:33-14:7; Ex. 1002, ¶ 160.



Ex. 1014, Fig. 3

Pandey recognizes that the number of signals (nets) between function blocks may exceed the number of traces available inside a chip, and that in such cases, multiple signals must be time-multiplexed (i.e. transmitted serially) over a single trace. Ex. 1014, 10:24-53; 10:58-11:5, 29:44-58, 30:31-42; Ex. 1002, ¶ 161. For example, as shown below, a plurality of parallel signals from logic block A 1613 in a first partition are multiplexed by 1615 onto a single trace 1605, and then

demultiplexed back into parallel signals input to logic block B 1623 in a second partition. Ex. 1014, 30:31-52, Fig. 37; Ex. 1002, ¶ 161.



Ex. 1014, Fig. 37

Pandey's process optimizes the partitioning of blocks based on reducing the multiplexing ratio of wires to signals required between partitions. Ex. 1014, 5:50-53, 6:11-15, 6:44-53, 7:13-19, 29:44-30:9, 30:53-31:12, 31:56-63, Figs. 38-39; Ex. 1002, ¶ 162. Thus, depending upon the partitioning, Pandey's optimization will in some layouts group and time-multiplex signals through a serial interface between partitions, and in other layouts send signals via individual dedicated traces with no multiplexing, which is a parallel interface. Ex. 1014, 31:20-22, 32:12-15; Ex. 1002, ¶ 162. Thus, Pandey teaches both serial and parallel interfaces for groups of signals

between digital functional blocks, with the selection between the two interfaces simply being dependent upon the area and interconnect resources of a particular integrated chip. Ex. 1014, 11:6-19, 13:33-55, 31:20-22, 32:12-15, Figs. 2-3; Ex. 1002, ¶ 162.

It would have been obvious to apply Pandey's dedicated (i.e., parallel) and/or time-multiplexed (i.e., serial) interconnection to the interconnection between Zhang's demultiplexer 230, digital selector 240, and/or demodulators 250. Ex. 1002, ¶ 163. Zhang teaches optimizing the real estate needed for implementing the digital portion of its system on a single chip, and the process described in Pandey would have beneficially supported this optimization. Ex. 1013, [0029], [0037], [0044], [0047]-[0048]; Ex. 1014, 1:20-2:12, 6:10-15; Ex. 1002, ¶ 163. As such, the modification of Zhang with Pandey that results in parallel and/or serial interfaces from, e.g., Zhang's Digital Channel DeMux 230 and Selector 240 to Demodulators 250 is nothing more than a combination of prior art elements (Zhang's circuit design and Pandey's parallel and serial interconnections in an integrated circuit chip) according to known methods (Pandey's process for implementing circuit designs with parallel and serial interfaces) to yield predictable results (data is sent via a parallel interface and/or a serial interface). Ex. 1002, ¶ 163.

Modifying Zhang with Pandey would also have been the use of a known technique for implementing data buses in an integrated circuit as taught in Pandey,

to improve a similar integrated circuit having data buses for outputting digital data streams as taught in Zhang, in the same way Pandey teaches to apply its technique. Ex. 1002, ¶ 163.

The resultant combination is predictable. Ex. 1014, 31:15-22, 32:7-15; Ex. 1002, ¶ 164. Where trace resources for a particular integrated circuit are insufficient, Pandey's process will predictably time-multiplex signals onto a single trace based on a desired multiplexer ratio, thus producing a serial interface to, e.g., Zhang's demodulators. *Id.* Likewise, where the resources are sufficient, Pandey's process will predictably reduce the multiplexer ratio to one and assign each signal to its own trace, thus producing a parallel interface to, e.g., Zhang's demodulators. *Id.* Further, a POSITA would have had a reasonable expectation of success, because Pandey's optimization utilized processes such as floor planning, partitioning, and trace routing that were standard and well within a POSITA's skillset. Ex. 1014, 1:20-2:38; Ex. 1002, ¶ 164.

2. Dependent Claims 12 and 13

Claims 12 and 13 repeat the functionality of claims 2 and 3 as method steps performed by identical structural elements. Ex. 1002, ¶¶ 165-166. Thus, claims 12 and 13 are directed to substantially identical subject matter as claims 2 and 3, respectively, and rendered obvious by Zhang-Pandey, for the same reasons discussed above with respect to claims 2 and 3. *See* Section VII.B.1, *supra*.

C. Ground D: Claims 4-6 and 14-16 are Rendered Obvious by Zhang-Mirabbasi.

Zhang-Mirabbasi teach claims 4-6. Ex. 1002, ¶¶ 167-188. As described above for Elements [1B] and [1C], Zhang’s frequency block down converter 210 (**red**) (the claimed “mixer module”) receives a multi-channel *analog* RF signal from a TV system and downconverts the signal to a lower frequency range so that signal can be digitized by ADC 220 (**gold**) (the claimed “wideband analog-to-digital converter”) to a multi-channel *digital* RF signal. Ex. 1013, [0005], [0023]-[0025], [0029], [0041], claims 13, 27, 33; Ex. 1002, ¶ 168; *see* Sections VII.A.1.b-c.

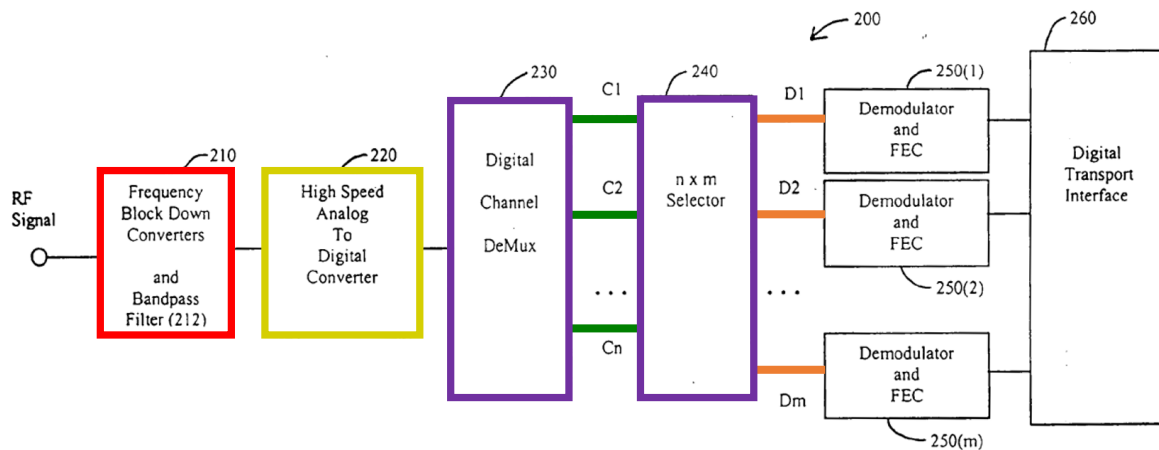
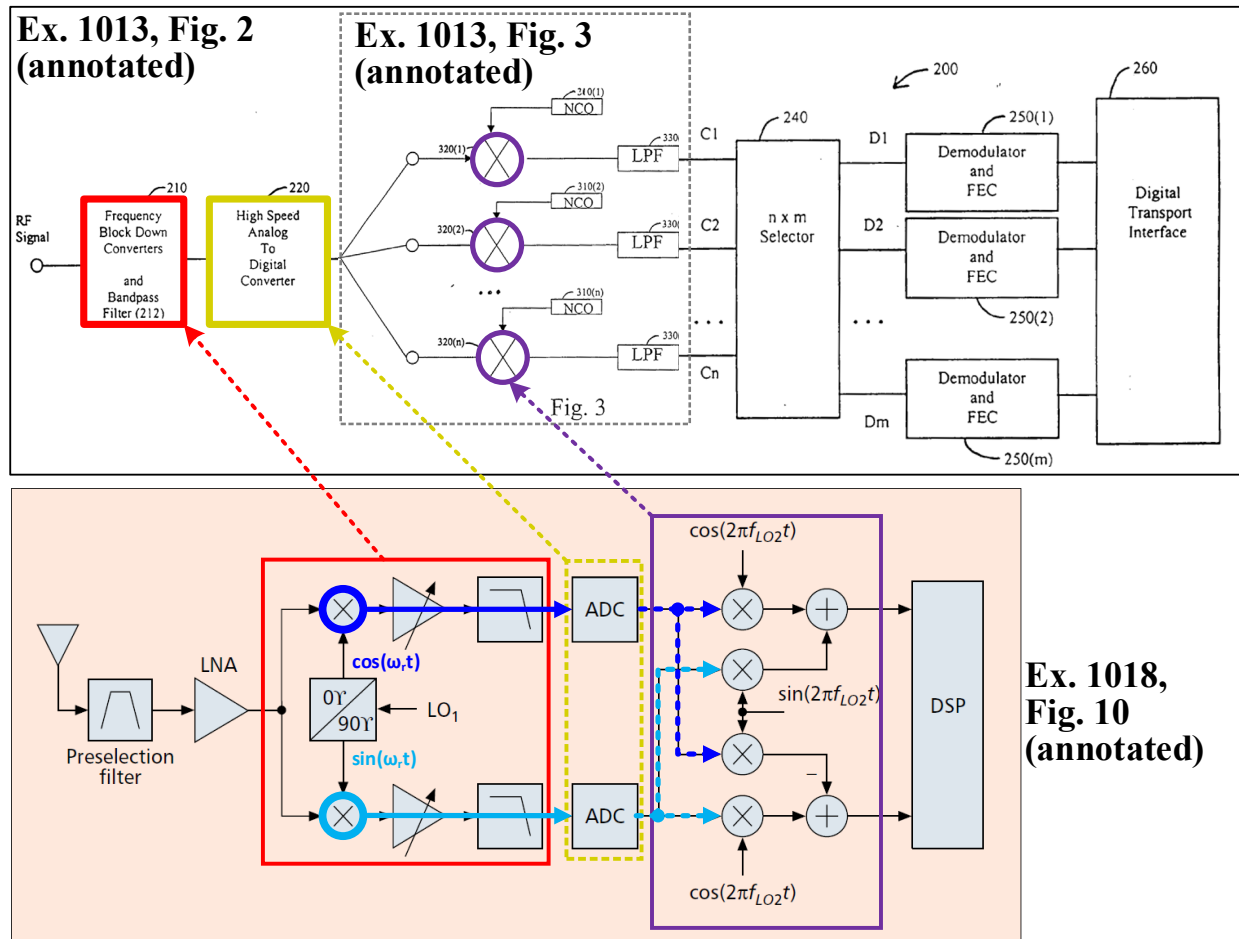


Fig. 2

Ex. 1013, Fig. 2 (annotated)

As further described above for Element [1D] and claim 8, Zhang’s digitized output from ADC 220 is input to individual complex multipliers 320 within Digital Channel Demultiplexer 230 (**purple**) (included within the claimed “digital circuitry”). Ex. 1013, [0030]-[0032]; Ex. 1002, ¶ 168; *see* Sections VII.A.1.d, VII.A.3, *supra*.

A POSITA would have found it obvious to implement Converter 210 (**red**), ADC 220 (**gold**), and Demultiplexer 230 (**purple**), with the circuits recited in claims 4, 5, and 6, respectively, based on Zhang’s teachings, the POSITA’s general knowledge, and Mirabbasi. Ex. 1002, ¶¶ 169-171. A composite of Figures 2 and 3 of Zhang alongside Figure 10 of Mirabbasi is provided below.



Mirabbasi provides a tutorial of known RF receiver architectures used for receiving digitally-modulated RF signals. Ex. 1018, pp. 4, 11; Ex. 1002, ¶ 170. As shown above, Mirabbasi depicts a “Low-IF Receiver” having the same architecture as that in Zhang, which includes a RF analog frontend (**red**) that performs frequency

downconversion of the analog input to an intermediate frequency (IF), followed by an analog-to-digital converter (**gold**) that digitizes the analog IF signal, followed by a digital multiplexer (**purple**) that further downconverts the digitized signal to a baseband signal, which is then processed by additional digital circuitry to demodulate the signal and recover the modulated data. Ex. 1018, pp. 9-10, Fig. 10; *see also* Ex. 1025, pp. 272, 279-280; Ex. 1034, pp. 54-63; Ex. 1013, [0023]-[0029], Fig. 2; Ex. 1002, ¶¶ 170-171.

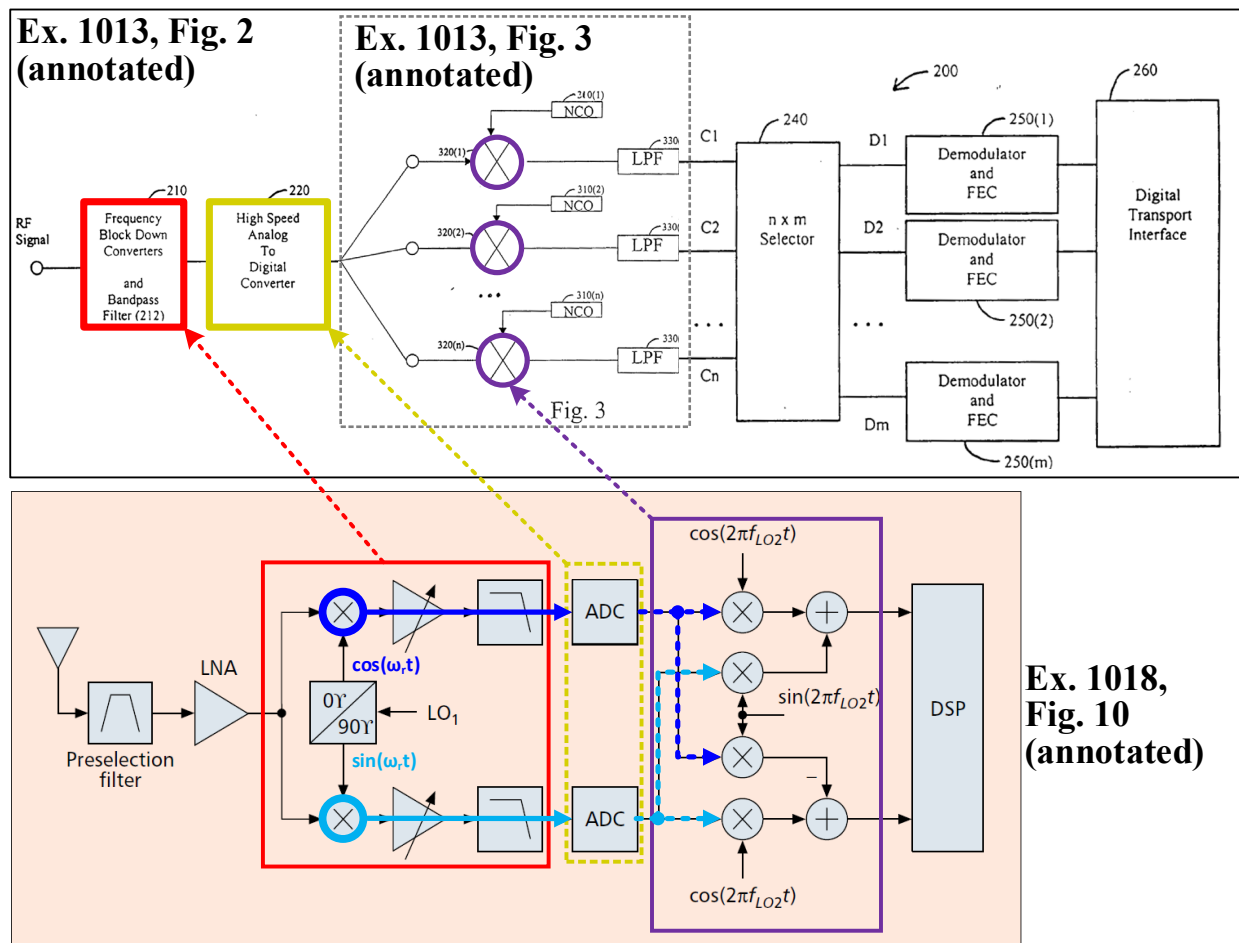
As described below, it would have been obvious to implement Zhang's converter 210, ADC 220 and digital multiplexer 230 using the well-known structures in Mirabbasi to teach and render obvious claims 4-6 and 14-16.

1. Dependent Claim 4

[4] “The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.”

As shown below, Mirabbasi's RF analog frontend (**red**) includes a complex mixer composed of a first real mixer (**dark blue circle**) and a second real mixer (**light blue circle**) that receive the analog RF signal through a low noise amplifier (LNA) and multiply the analog RF signal by a local oscillator (LO₁) sinusoid signal. Ex. 1018, pp. 5-6 (describing mixing a real input signal with a complex exponential per Mirabbasi Fig. 2 to produce in-phase and quadrature components), 137-138, Figs. 2, 10; Ex. 1002, ¶¶ 172-173. The first real mixer receives LO₁ with zero phase

shift (denoted “0Y”, e.g., $\cos(\omega t)$), causing the first mixer to generate an in-phase signal (**dark blue line**), and the second mixer receives the LO₁ signal with a 90-degree phase shift (denoted “90Y”, e.g., $\sin(\omega t)$), causing the second mixer to generate a quadrature signal (**light blue line**). Ex. 1018, pp. 5-6; Ex. 1025, pp. 274-275, Fig. 22; Ex. 1034, pp. 54-56; Ex. 1002, ¶¶ 173-175. Mirabbasi thus discloses the features of claim 4.



As described in Mirabbasi, the “low-IF” architecture (the **red, gold, purple circuits**) overcomes a number of issues found in other common RF receiver designs. Ex. 1018, pp.6-11; Ex. 1002, ¶¶ 185-186. The advantages include eliminating DC

offset in the baseband signals, making the sampling of the IF signal with ADCs more feasible because the IF signal is at a lower frequency, and eliminating gain and phase mismatches between the in-phase and quadrature signals because they are partially downconverted and corrected digitally. Ex. 1018, pp. 8, 138; Ex. 1002, ¶ 186. Because of these advantages, a POSITA would have been motivated to use Mirabbasi's low-IF design—e.g., its analog complex mixer (red) including first (dark blue) and second (light blue) mixers, the pair of ADCs (gold), and/or its complex mixer (purple box)—to implement Zhang's corresponding receiver components as described above. Indeed, some issues like DC offset are significant in CMOS, a technology in which the Zhang receiver is implemented, and thus a POSITA would have found Mirabbasi's low-IF architecture, which eliminates DC offset, to be particularly beneficial. Ex. 1013, [0048]; Ex. 1018, pp. 8-9; Ex. 1002, ¶¶ 185-186.

Thus, implementing Zhang with Mirabbasi as described above to include, for example the features of claim 4 (along with the features of claims 5 and 6 discussed below) would have been nothing more than using a known technique (Mirabbasi's low-IF receiver structures) to improve a similar device (Zhang's receiver having the same basic architecture) in the same way (providing the benefits over other common architectures as described by Mirabbasi) with a predictable result (e.g., the mixer

module comprises two mixers generating in-phase and quadrature signals, respectively). Ex. 1002, ¶ 187.

Mirabbasi's low-IF architecture uses components that were common and well-known to a POSITA, and the basic architecture of the low-IF receiver matches that of Zhang's receiver, thus requiring little or no deviation in Mirabbasi's implementation when applied to Zhang. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 188. Further, the implementation of Mirabbasi's receiver was taught in basic textbooks and well within a POSITA's skillset. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 188. All of this leads to an expectation of success.

For these reasons, claim 4 is obvious over Zhang-Mirabbasi.

2. Dependent Claim 5

[5A] “The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises:”

[5B] “a first ADC configured to generate a digital in-phase signal; and”

[5C] “a second ADC configured to generate a digital quadrature signal.”

In Mirabbasi, following generation by the mixers, the in-phase (**dark blue line**) and quadrature (**light blue line**) signals are passed through amplifiers and filters respectively to first and second ADCs (**gold**) to generate digital in-phase and quadrature signals, respectively, thus disclosing the features of claim 5. Ex. 1018,

p. 10; Ex. 1025, pp. 274-275, 279-280; Ex. 1034, pp. 54-56, 61-62, Fig. 3.29a; Ex. 1002, ¶¶ 176-177.

As discussed above for claim 4, Mirabbasi’s “low-IF” architecture (the **red, gold, purple circuits**) eliminates DC offset in the baseband signals, making the sampling of the IF signal with ADCs more feasible because the IF signal is at a lower frequency, and eliminating gain and phase mismatches between the in-phase and quadrature signals because they are partially downconverted and corrected digitally. Ex. 1018, pp. 6-10; Ex. 1002, ¶¶ 185-186. Because of these advantages, a POSITA would have been motivated to use Mirabbasi’s low-IF design—e.g., its analog complex mixer (**red**), the pair of ADCs (**gold**), and/or its complex mixer (**purple box**)—to implement Zhang’s corresponding receiver components as described above. Indeed, a POSITA would have found Mirabbasi’s low-IF architecture, which eliminates DC offset, to be particularly beneficial. Ex. 1013, [0048]; Ex. 1018, pp. 8-9; Ex. 1002, ¶ 186.

Thus, implementing Zhang with Mirabbasi as described above to include, for example the features of claim 5 (along with the features of claims 4 and 6) would have been nothing more than using a known technique (Mirabbasi’s low-IF receiver structures) to improve a similar device (Zhang’s receiver having the same basic architecture) in the same way (providing the benefits over other common architectures as described by Mirabbasi) with a predictable result (Zhang’s ADC

uses Mirabbasi's first and second ADCs to generate digital in-phase and quadrature signals). Ex. 1002, ¶ 187.

Mirabbasi's low-IF architecture uses components that were common and well-known to a POSITA, and the basic architecture of the low-IF receiver matches that of Zhang's receiver, thus requiring little or no deviation in Mirabbasi's implementation when applied to Zhang. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 188. Further, the implementation of Mirabbasi's receiver was taught in basic textbooks and well within a POSITA's skillset. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 188. All of this leads to an expectation of success.

For these reasons, claim 5 is obvious over Zhang-Mirabbasi.

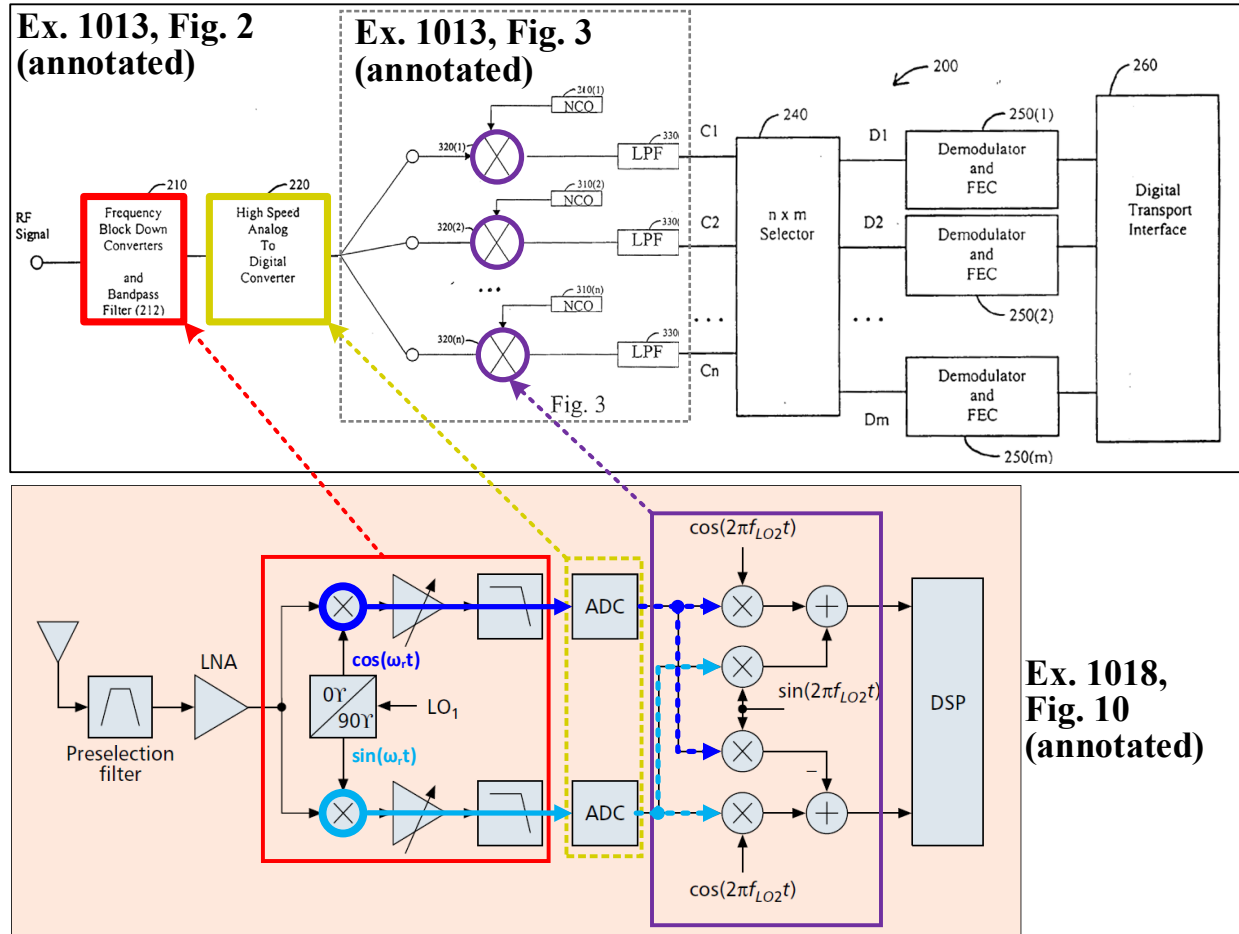
3. Dependent Claim 6

[6] “The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.”

As shown below, Mirabbasi's digital in-phase (**dashed dark blue line**) and quadrature (**dashed light blue line**) signals enter digital circuitry (**purple**), which in both Zhang and Mirabbasi include complex mixers for shifting the frequency of the selected desired television channels as recited in claim 6. Ex. 1002, ¶¶ 178-179.

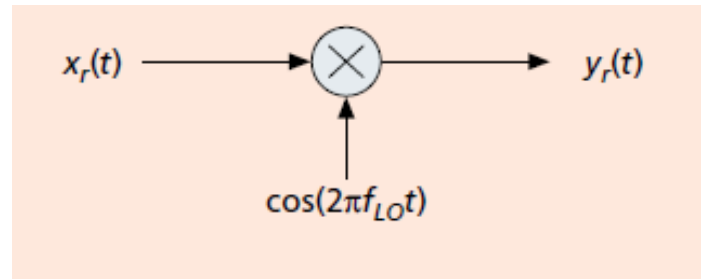
As described above with respect Element [1D], the digitized signals output by the ADC (**gold**) in Zhang are input to a Digital Channel Demultiplexer 230 (included

within the claimed “digital circuitry”), which includes individual “complex multipliers 320(1...n)” (**purple circles**). Ex. 1013, [0030]-[0032]; Ex. 1002, ¶ 180.



A POSITA would have understood that “multiplier” (as used in Zhang) and “mixer” are interchangeable names for the same device shown below, which multiplies an input signal (e.g., $x_r(t)$) by a sinusoidal signal (e.g., $\cos(2\pi f_{LO}t)$) to generate an output signal (e.g., $y_r(t)$) that matches the input signal, but at a shifted frequency. Ex. 1002, ¶¶ 66, 181-182; Ex. 1013, [0032]; Ex. 1018, Fig. 1, p. 5 (“frequency downconversion ... is performed by multiplying (mixing) the signal with a sinusoid such as $\cos(2\pi f_{LO}t)$ ”); Ex. 1001, 4:42-43 (“mixers 211 and 221

multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency”); *compare* Ex. 1001, 6:7-27 (describing the complex mixer in Figure 3 as including four “multipliers”) *with* Ex. 1001, 9:17-22 (describing a complex mixer in Figure 3 as including four “digital mixers”).

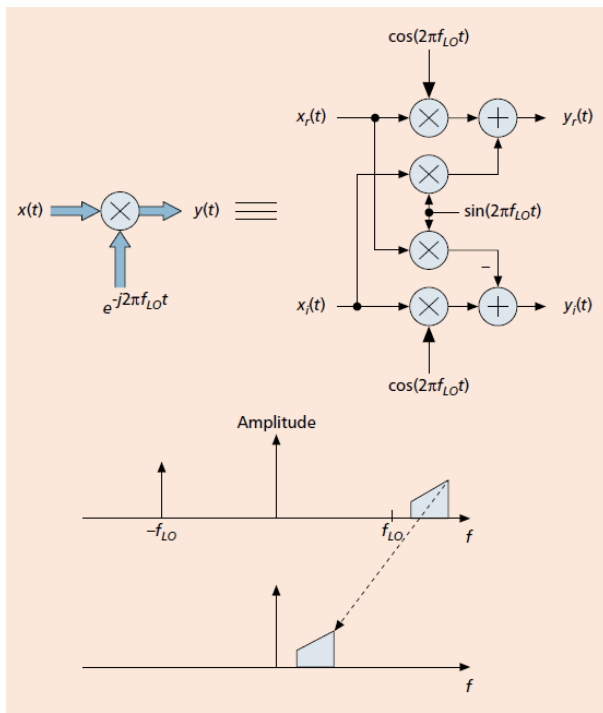


Ex. 1018, Fig. 1

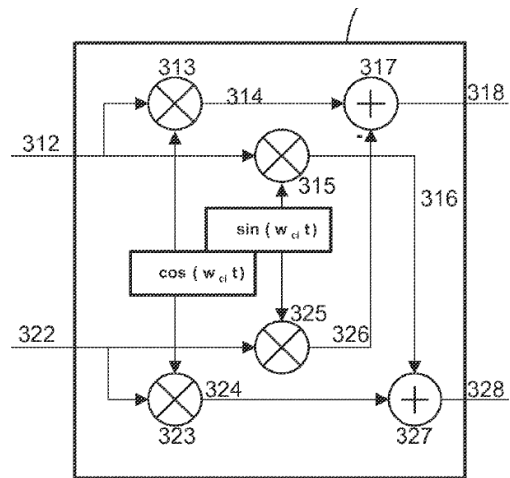
Each of Zhang’s complex multipliers (mixers) shifts the frequency of the multichannel digital RF signal such that “the frequency of the target RF channel signal is shifted to a desired channel,” which in some embodiments is “baseband, i.e., centered at DC.” Ex. 1013, [0012], [0030]-[0032]; Ex. 1002, ¶¶ 182-183. Zhang includes a plurality of complex multipliers (mixers) for shifting the frequency of the plurality of desired channels, respectively, thus disclosing the features of claim 6. Ex. 1013, [0030]-[0032]; Ex. 1002, ¶¶ 182-183.

Similarly, Mirabbasi discloses the structure of one complex mixer (**purple box**) receiving the digital in-phase (**dashed dark blue line**) and quadrature (**dashed light blue line**) signals from its ADCs (**gold**). As Mirabbasi explains and illustrates, a “complex” mixer includes multiple individual mixers, such as “four real mixers [] shown in Fig. 3” for mixing complex signals having in-phase and quadrature

components. Ex. 1018, pp. 5-6, Figs. 2-3, 10; *see also* Ex. 1034, pp. 35-36, Fig. 3.3; Ex. 1002, ¶ 184. Mirabbasi's complex mixer has the identical structure and performs the identical downconversion (i.e., shifting the frequency of in-phase and quadrature components of the digital complex input signal) as mixer 300 shown in Figure 3 of the '362 patent. Ex. 1018, pp. 9-10, Fig. 3; Ex. 1001, Fig. 3, 6:7-25, 9:17-22; *see also* Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶¶ 183-184.



Ex. 1018, Fig. 3



Ex. 1001, Fig. 3 (excerpted)

As discussed above with respect to claims 4 and 5, Mirabbasi's "low-IF" architecture (the **red**, **gold**, **purple circuits**) eliminates DC offset in the baseband signals, making the sampling of the IF signal with ADCs more feasible because the IF signal is at a lower frequency, and eliminating gain and phase mismatches between the in-phase and quadrature signals because they are partially

downconverted and corrected digitally. Ex. 1018, pp. 6-10; Ex. 1002, ¶¶ 185-186. Because of these advantages, a POSITA would have been motivated to use Mirabbasi's low-IF design—e.g., its analog complex mixer (**red**), the pair of ADCs (**gold**), and/or its complex mixer (**purple box**)—to implement Zhang's corresponding receiver components as described above. A POSITA would have found Mirabbasi's low-IF architecture, which eliminates DC offset, to be particularly beneficial. Ex. 1013, [0048]; Ex. 1018, pp. 8-9; Ex. 1002, ¶ 186.

Thus, implementing Zhang with Mirabbasi as described above to include, for example the features of claim 6 (along with the features of claims 4 and 5) would have been nothing more than using a known technique (Mirabbasi's low-IF receiver structures) to improve a similar device (Zhang's receiver having the same basic architecture) in the same way (providing the benefits over other common architectures as described by Mirabbasi) with a predictable result (e.g., Zhang contains a plurality of Mirabbasi's complex mixers configured to frequency shift the selected plurality of desired television channels). Ex. 1002, ¶ 187.

Mirabbasi's low-IF architecture uses components that were common and well-known to a POSITA, and the basic architecture of the low-IF receiver matches that of Zhang's receiver, thus requiring little or no deviation in Mirabbasi's implementation when applied to Zhang. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 188. Further, the implementation of Mirabbasi's receiver was

taught in basic textbooks and well within a POSITA's skillset. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 188. All of this leads to an expectation of success.

For these reasons, claim 6 is obvious over Zhang-Mirabbasi.

4. Dependent Claims 14-16

Claims 14-16 repeat the functionality of claims 4-6 as method steps performed by identical structural elements. Ex. 1002, ¶¶ 189-190. Thus, claims 14-16 are directed to substantially identical subject matter as claims 4-6, respectively and are rendered obvious by Zhang-Mirabbasi for the same reasons discussed above with respect to claims 4-6. *See* Sections VII.C.1-3, *supra*.

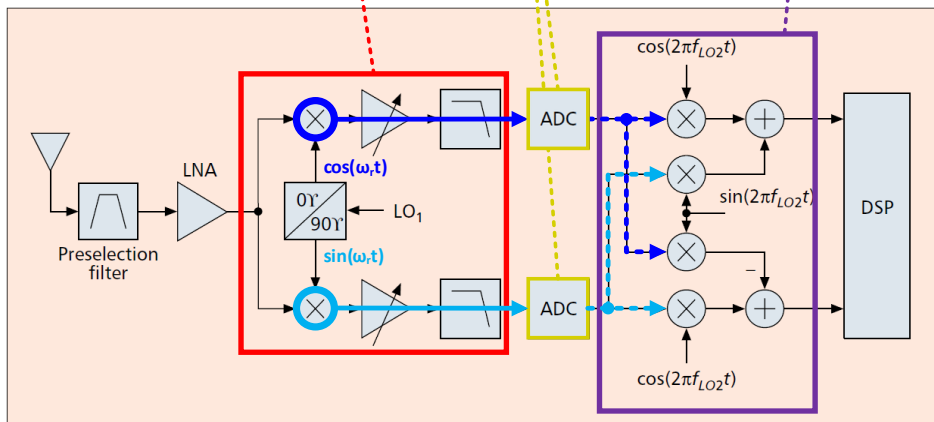
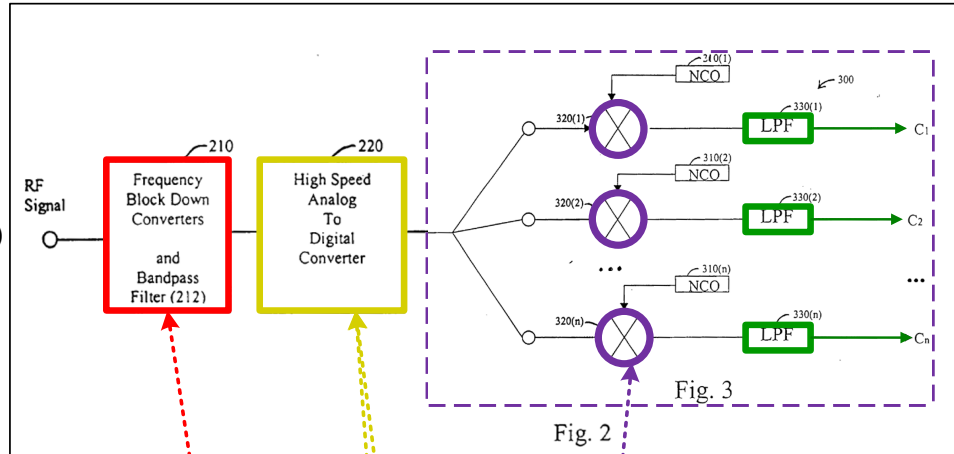
D. Ground E: Claims 7 and 17 are Rendered Obvious by Zhang-Mirabbasi-Karabinis.

1. Dependent Claim 7

a. [7A] “The wideband receiver system of claim 6, wherein:”

As discussed above, Zhang-Mirabbasi disclose all of the features of claim 6, from which claim 7 depends. *See* Section VII.C.3, *supra*. In this combination, Zhang's digital circuitry includes a plurality of complex mixers (as taught in Zhang and/or Mirabbasi) (purple) “configured to frequency shift said selected plurality of desired television channels” as recited in claim 6. Ex. 1013, [0030]-[0032]; Ex. 1002, ¶ 191-192.

**Ex. 1013,
Figs. 2, 3
(annotated)**



**Ex. 1018,
Fig. 10
(annotated)**

b. [7B] “prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”

Zhang-Mirabbasi disclose Element [7B]. Ex. 1002, ¶¶ 193-194. Zhang’s complex mixers (purple) receive from the ADC (gold) a digitized multi-channel RF signal that includes a plurality of channels, each with a unique frequency spaced apart from one another (e.g., at 6 MHz intervals) and within a particular frequency spectrum (e.g., 300 MHz). Ex. 1013, [0005]-[0006], [0024], [0027], [0030]; Ex. 1002, ¶ 193. Each of Zhang’s mixers select from the plurality of channels one

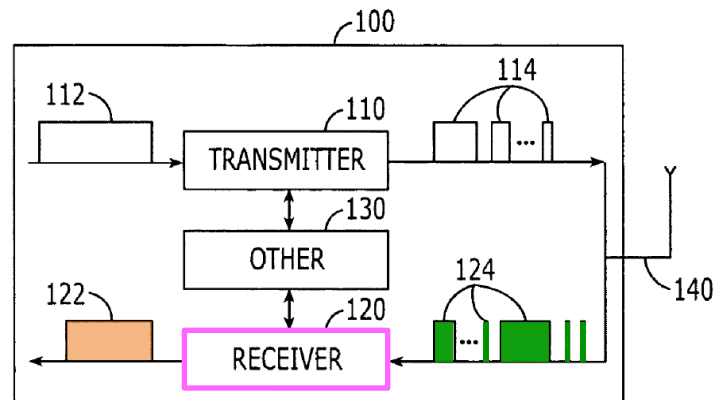
“desired” channel by controlling a numeric controlled oscillator 310 to the desired channels “target.” Ex. 1013, [0012], [0030]-[0032]; Ex. 1002, ¶ 193.

The Zhang-Mirabbasi system includes any number “n” of mixers for a corresponding “n” desired channels “that are selected or used by a subscriber,” with undesired channels filtered out by a low pass filter. Ex. 1013, [0028], [0030]-[0032], Figs. 2-4; Ex. 1002, ¶ 194. Zhang further discloses that the “RF channels need not be contiguous.” Ex. 1013, [0048]; Ex. 1002, ¶ 194. From this, a POSITA would have understood that the number of desired channels is less than all of the channels in the frequency band and that any two desired channels may obviously be separated by undesired channels in the digitized multi-channel RF signal. Ex. 1002, ¶ 194. Thus, the complex mixers in Zhang-Mirabbasi are configured to frequency shift the selected plurality of desired television channels, wherein prior to the frequency shift the selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum as recited in Element [7B].

c. [7C] “after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”

Zhang-Mirabbasi and Karabinis disclose Element [7C]. Ex. 1002, ¶¶ 195-202. As described above for claim 6, each of Zhang-Mirabbasi’s complex mixers shifts the frequency of the multichannel digital RF signal such that “the frequency of the target RF channel signal is shifted to a desired channel.” Ex. 1013, [0012],

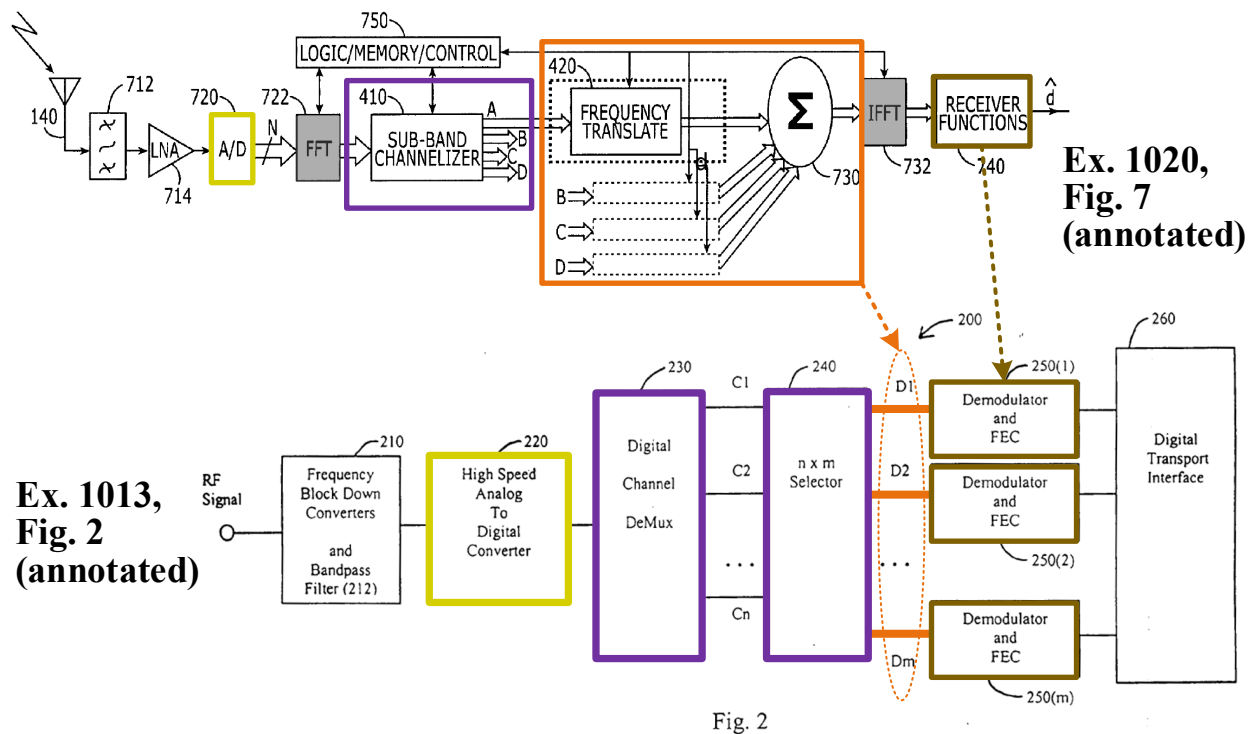
[0030]-[0032]. Zhang provides one example in which the target RF channels are shifted to baseband (centered at 0Hz), but Zhang does not expressly disclose other examples, such as the desired television channels being in a contiguous frequency spectrum as recited in Element [7C]. *Id.*; Ex. 1002, ¶ 195. Karabinis, however, provides such an example as illustrated below, in which a receiver 120 (pink) receives a plurality of signals with non-contiguous frequencies (green), and translates the frequencies so that the signals are output within a contiguous frequency band (orange). Ex. 1020, [0036]-[0038].



Ex. 1020, Fig. 1 (annotated)

As illustrated below, Karabinis's receiver (top figure) operates similarly to the Zhang-Mirabbasi receiver as described above with respect to claim 6. *See* Section VII.C.3, *supra*; Ex. 1020, [0036]-[0038], [0042]-[0044], [0047]-[0049], Figs. 1, 4-5, 7; Ex. 1002, ¶ 196. Like the receivers in Zhang and Mirabbasi, Karabinis's receiver is configured to receive signals at multiple non-contiguous frequencies, downconvert the signals using a mixer (not shown), and digitize the downconverted

signal using an analog-to-digital converter (**gold**). Ex. 1020, [0010], [0031], [0037]-[0038], [0042], [0047]-[0048]; Ex. 1013, Abstract, [0010], [0025], [0027]-[0028], [0031]-[0032], [0034], [0041]-[0042], claims 1-2, 4, 7-8, 28, 34, 36-37; Ex. 1002, ¶ 196.



Karabinis also includes digital circuitry—e.g., sub-band channelizer 410 (**purple**)—that performs the same function as Zhang’s digital channel demultiplexer 230 and selector 240, which is to isolate the plurality of the non-contiguous frequencies (desired channels in Zhang) from the digitized signal and output them for demodulation. Ex. 1020, [0042], [0044], [0047], [0049], Figs. 4-5, 7; Ex. 1002, ¶ 197.

In Zhang, “m” desired channels, each at baseband (0Hz), are output from selector 430 to demodulators 250 (**brown**) via a set of buses. Ex. 1013, Fig. 5, [0029], [0038]-[0039], claim 3; Ex. 1002, ¶ 198; *see* Section VII.A.1.d (Element [1D]), VII.A.2 (claims 2 and 3). Since each of the desired channels are at the same baseband frequency, they must be output on different buses in parallel or they must be time multiplexed serially on the same bus, since signals at the same baseband frequency would otherwise interfere with one another. Ex. 1002, ¶ 198; *see* Sections VII.A.1.d (Element [1D]), VII.A.2 (claims 2 and 3). For the same reasons, multiple Zhang demodulators simultaneously receive and process the desired channels, or a single demodulator may sequentially receive and process multiple desired channels one at a time. Ex. 1002, ¶ 199; *see* Sections VII.A.1.d (Element [1D]), VII.A.2 (claims 2 and 3).

Karabinis provides an alternate way to output Zhang-Mirabbasi’s desired channels for demodulation, which is to shift the frequencies of the desired channels (e.g., D_1 - D_m) into a contiguous frequency band 422 (the claimed “continuous frequency spectrum”) using a plurality of frequency translators 420, and summing

the shifted channels with a summer (collectively **orange**).⁶ Ex. 1020, ¶¶ 0017, 0042-0044, 0049; Ex. 1020, ¶ 200. For example, Zhang's outputs from bus selector 510 (in selector 240) would be input into Karabinis's frequency translators 420 (Zhang's D1 into Karabinis's channel A, Zhang's D2 into Karabinis's channel B, Zhang's D3 into Karabinis's channel C, etc.) to generate a summed contiguous frequency band, which is then output to a demodulator (**brown**) to extract the modulated data from the selected channels. Ex. 1020, [0017]-[0018], [0042]-[0043], [0049], claims 8-9, 27-28, Figs. 4-5, 7; Ex. 1013, Ex. 1002, ¶ 200.

A POSITA implementing the Zhang-Mirabbasi receiver would have considered it obvious to modify the design according to Karabinis to output the desired channels in a contiguous frequency spectrum because this was another known option for providing the channels for demodulation. Ex. 1002, ¶ 201. Doing so would have permitted a demodulator, such as the ones disclosed in Zhang-Mirabbasi and Karabinis, to receive all of the desired channels simultaneously over

⁶ Karabinis's sub-band channelizer 410 and frequency translator 420 may optionally work in either the frequency domain by including FFT and IFFT blocks (**grey**) before and after 410 and 420 (*see* Figure 5), or work in the time domain by excluding the FFT and IFFT blocks (*see* Figure 4). Ex. 1020, [0024], [0042]-[0044]; Ex. 1002, ¶ 201.

a single bus, which would have beneficially eliminated the need of having Zhang's multiple data buses (1 through k) and time division demultiplexer between the buses and the demodulator (*see* Figure 5). Ex. 1002, ¶ 201. It also would have enabled the Zhang-Mirabbasi receiver to use a single multichannel demodulator as in Karabinis, rather multiple single-channel demodulators. Ex. 1002, ¶ 201.

As such, the modification of the Zhang-Mirabbasi receiver with Karabinis would have been nothing more than the simple substitution of known elements (Zhang's data buses, time division demultiplexer, and single-channel demodulators 250) with other known elements (Karabinis's frequency translator 420, summer 730, and multichannel demodulator 430/740) to obtain predictable results (desired channels are in a contiguous frequency spectrum and can be demodulated via a single multichannel demodulator). Ex. 1002, ¶ 202. The modification would also have been the use of a known technique (Karabinis' channel translation from baseband to contiguous channels) to improve Zhang's similar device (by eliminating the need for Zhang's multiple buses and channel demultiplexer and enabling the use of a multichannel demodulator) in the same way as taught in Karabinis. Ex. 1002, ¶ 202. This substitution would have been predictable, and a POSITA would have a high expectation of success, because the substitution could be done with minimal modification to the surrounding hardware. Ex. 1002, ¶ 202. For example, the isolated signals received by frequency translators 420 from sub-band channelizer

410 in Karabinis, would have been similar to the signals output by digital channel demultiplexer 230 and channel selector 240 in Zhang, with the only potential difference being the frequencies of the selected channels that are being translated. Moreover, the circuits described in Zhang and Karabinis would have been well known to a POSITA. Ex. 1002, ¶ 202.

Accordingly, Element [7C], and the entirety of claim 7, is obvious over the combination of Zhang-Mirabbasi-Karabinis.

2. Dependent Claim 17

Claim 17 is directed to substantially identical subject matter as claim 7, and thus is rendered obvious by the combination of Zhang-Mirabbasi-Karabinis, for the same reasons discussed above with respect to claim 7. *See* Section VII.D.1, *supra*; Ex. 1002, ¶ 204.

E. Ground F: Claims 10 and 20 are Rendered Obvious by Zhang in view of Jenson.

1. Dependent Claim 10

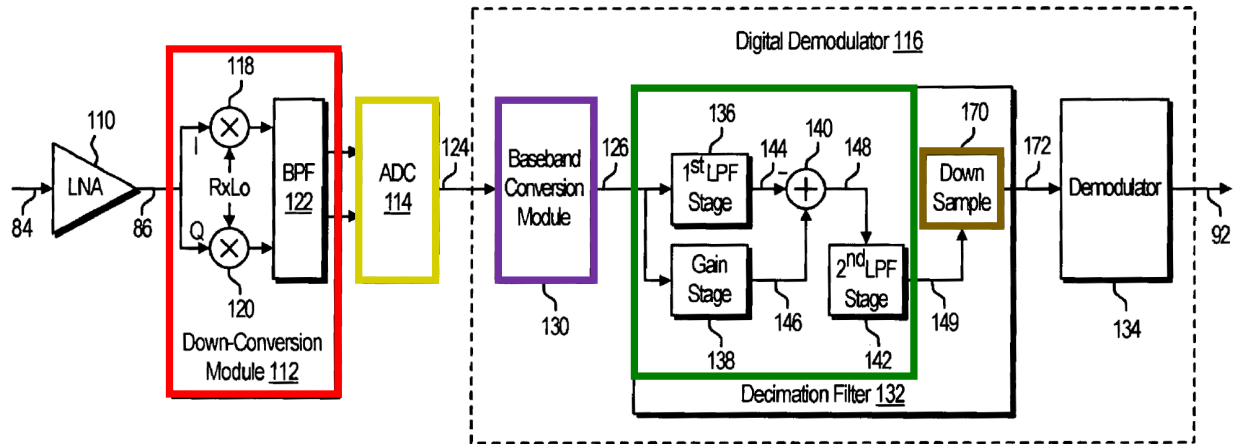
“The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.”

Zhang-Jenson teaches claim 10. Ex. 1002, ¶¶ 206-210. As explained in Section VII.A.1.d, Zhang’s Digital Channel Demultiplexer 230 alone, and Digital

Channel Demultiplexer 230 in combination with all or part of Digital Selector 240 teach Element [1D] (“digital circuitry configured to[] select said plurality of desired television channels ... and output ... as a digital datastream”). Zhang is silent with regard to whether Channel Demultiplexer 230 or Digital Selector 240 comprise a decimator circuit.

As explained by Jenson, however, decimation (**brown**) was commonly performed to reduce a sampling rate of a digital signal. Ex. 1026, [0027], [0007]; Ex. 1002, ¶ 206. For accurate reproduction of an analog signal, the ADC must sample the signal by at least twice the rate as the highest frequency in the signal (this is referred to as the Nyquist theorem). Ex. 1002, ¶¶ 73, 206; Ex. 1033, pp. 98-101. The RF signal sampled by the ADC includes a number of channels, thus having a wide bandwidth and requiring a high sampling rate. This results in a large amount of data produced by the ADC. *Id.* Processing this data to downconvert and filter produces the same amount of data, but that data now represents only single channel having a small bandwidth (e.g., 6 MHz). Because the processed data is much greater than needed to represent the single channel, the sample rate (i.e., the amount of data) can be reduced, which is referred to as decimation. Ex. 1026, [0007], [0027]; Ex. 1034 at 104; Ex. 1045 at 14-15, 70; 1002, ¶¶ 73, 206. Reducing the sampling rate reduces the amount of data processed by the digital circuitry, which reduces power

consumption and complexity in subsequent processing. Ex. 1026, [0007]; Ex. 1002, ¶ 206.



Ex. 1026, Fig. 1 (annotated)

Jensen discloses a similar receiver to that of Zhang, including having an analogous downconverter (**red**) to downconvert an RF signal to an IF signal, an ADC (**gold**) to convert the analog IF signal to a digital IF signal, a baseband conversion module (i.e., mixer module) (**purple**) to convert the digital IF signal to a baseband signal, and a low-pass channel select filter (**green**). Compare Ex. 1026, Fig. 1, [0023]-[0027] with Ex. 1013, Figs. 2, 3 (annotated below), [0026]-[0028], [0030]-[0032]; Ex. 1002, ¶ 207.

This issue of decimating to reduce unnecessary data sampling for downconverted signals described in Jensen is precisely the situation in Zhang's design, where the rate of Zhang's ADCs for sampling the wideband RF source signals is much higher (e.g., 300MHz) than the rate for demodulating individual

demultiplexed 6 MHz channels (e.g., requiring a sampling rate of only 12 MHz). Ex. 1013, [0007], [0025], [0029]; Ex. 1026, [0007], [0027]; Ex. 1002, ¶ 208.

Following Jenson, a POSITA would have included a decimator circuit in the Zhang's Channel Demultiplexer 230 or Digital Selector 240, either as a separate component following the low pass filters 330 or as part of the filters themselves (e.g., using channel-select decimation filters as low pass filters 330), to reduce the sampled data of the digital signals and thereby reduce power consumption and/or complexity in subsequent processing (e.g., in demodulators 250). Ex. 1013, Fig. 3, [0029]-[0032]; Ex. 1026, [0007]; Ex. 1002, ¶ 209. Such a combination of Zhang with Jensen would have been nothing more than the use of a known technique (Jensen's decimator following a channel select filter) to improve a similar device (Zhang's receiver with similar architecture) in the same way that Jensen describes (reduced power consumption and complexity).

As disclosed by Jenson, the use of decimation modules or of channel-select decimation filters (which combine a FIR filter with decimation) was common and merely requires removing some of the data in the output data stream, which easily could have been done with Zhang's digital circuitry and was well within the capability of a POSITA to implement, leading to an expectation of success. Ex. 1026, [0007]; Ex. 1002, ¶¶ 73, 210.

2. Dependent Claim 20

Claim 20 repeats the functionality of claim 10 as a method step performed by nearly identical structural elements. Ex. 1002, ¶ 211. Claim 10's functional language of "wherein said digital circuitry comprises a decimator circuit configured to decimate" is revised in claim 20 to the step of "decimating, by said digital circuitry." Thus, claim 20 is directed to substantially identical subject matter as claim 10 and is rendered obvious by Zhang-Jensen, for the same reasons discussed above with respect to claim 10. *See* Section VII.E.1, *supra*.

F. Alternate Arguments and Grounds based on Means-Plus-Function Construction of "digital circuitry"

1. Claims 1, 2-6, and 8-9 based on Grounds A/B, Claims 2-3 based on Ground C, Claims 4-6 based on Ground D, Claim 7 based on Ground E, and Claim 10 based on Ground E

To the extent "digital circuitry" of Element [1D] is construed to be a means-plus function term, as discussed above (Section VI.E.3), the corresponding structure is illustrated in Figures 2 and 3 of the '362 patent. As discussed above with respect to Element [1D] (Section VII.A.1.d) and shown in the comparison of Zhang to the '362 patent below, Zhang's demultiplexer 230 alone, and in combination with all or part of selector 240, include the same or equivalent structure as disclosed in the '362 patent (e.g., multiple parallel paths, each including a complex mixer followed by a

low pass filter followed by serial and parallel interfaces as shown in Figures 2 and 3 of Zhang and Figure 2 of the '362 patent), with any differences being insubstantial.

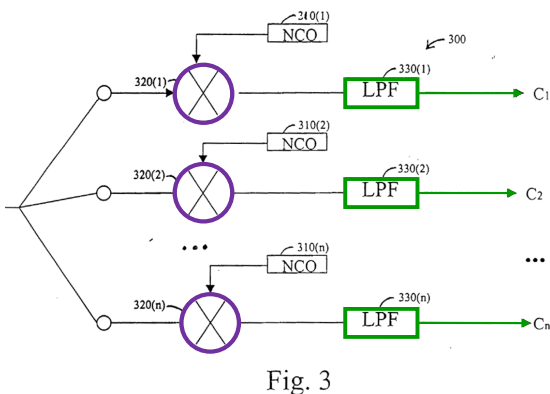
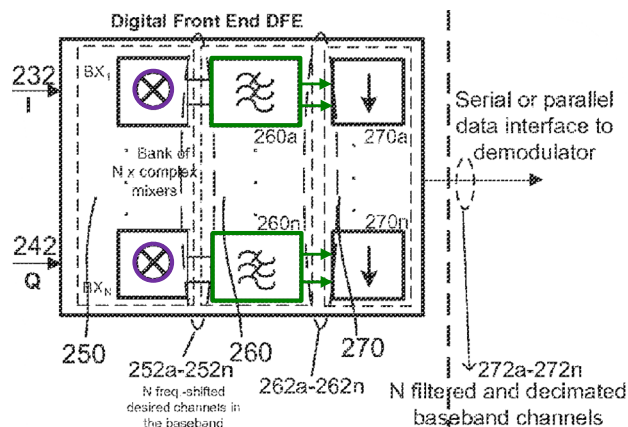


Fig. 3

Ex. 1013, Fig. 3 (annotated)



Ex. 1001, Fig. 2 (annotated)

Ex. 1002, ¶¶ 212-214; Compare Ex. 1001, 2:51-55, 5:49-6:54 with Ex. 1013, [0027], [0030], [0031], [0032]; see also Sections VII.A.1.d, VII.A.3 (claims 8 and 9), *supra*.

In both Zhang and the '362 patent, each path performs the same function of selecting and outputting a respective desired channel in the same way by, first, downconverting the respective desired channel to baseband and, then, low-pass filtering with a filter to isolate the channel, to achieve the same result of producing a plurality of desired channels as a digital data stream. Ex. 1002, ¶ 213.

Thus, Zhang anticipates and renders obvious claims 1, 2-3, 8-9 (Sections VII.A.1-3), Zhang-Pandey renders obvious claims 2-3 (Section VII.B.1), Zhang-Mirabbasi renders obvious claims 4-6 (Section VII.C.1-3), Zhang-Mirabbasi-Karabinis renders obvious claim 7 (Section VII.D.1), and Zhang-Jenson renders

obvious claim 10 (Section VII.E.1), for the reasons stated above, even if “digital circuitry” is given a means-plus-function construction. Ex. 1002, ¶ 214.

2. Claims 1-6 and 8-9 based on Zhang-Mirabbasi (Ground D), Claim 7 based on Zhang-Mirabbasi-Karabinis (Ground E)

To the extent “digital circuitry” of Element [1D] is construed to be a means-plus function term, and to the extent the corresponding structure is limited to only what is shown in Figure 3, Zhang-Mirabbasi teaches this element. Ex. 1002, ¶ 215.

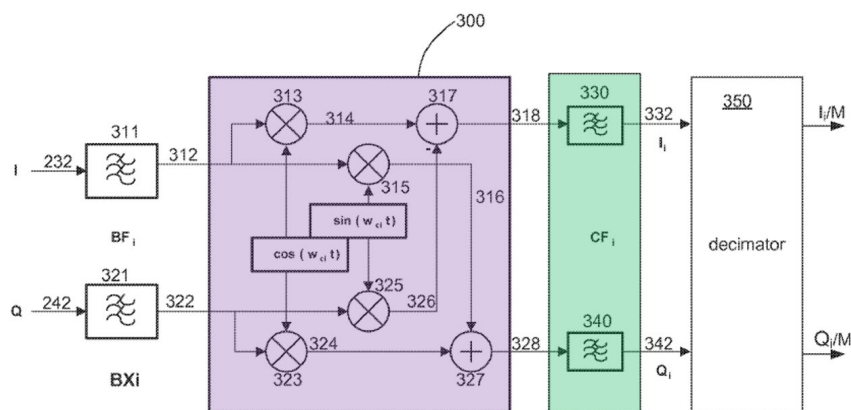
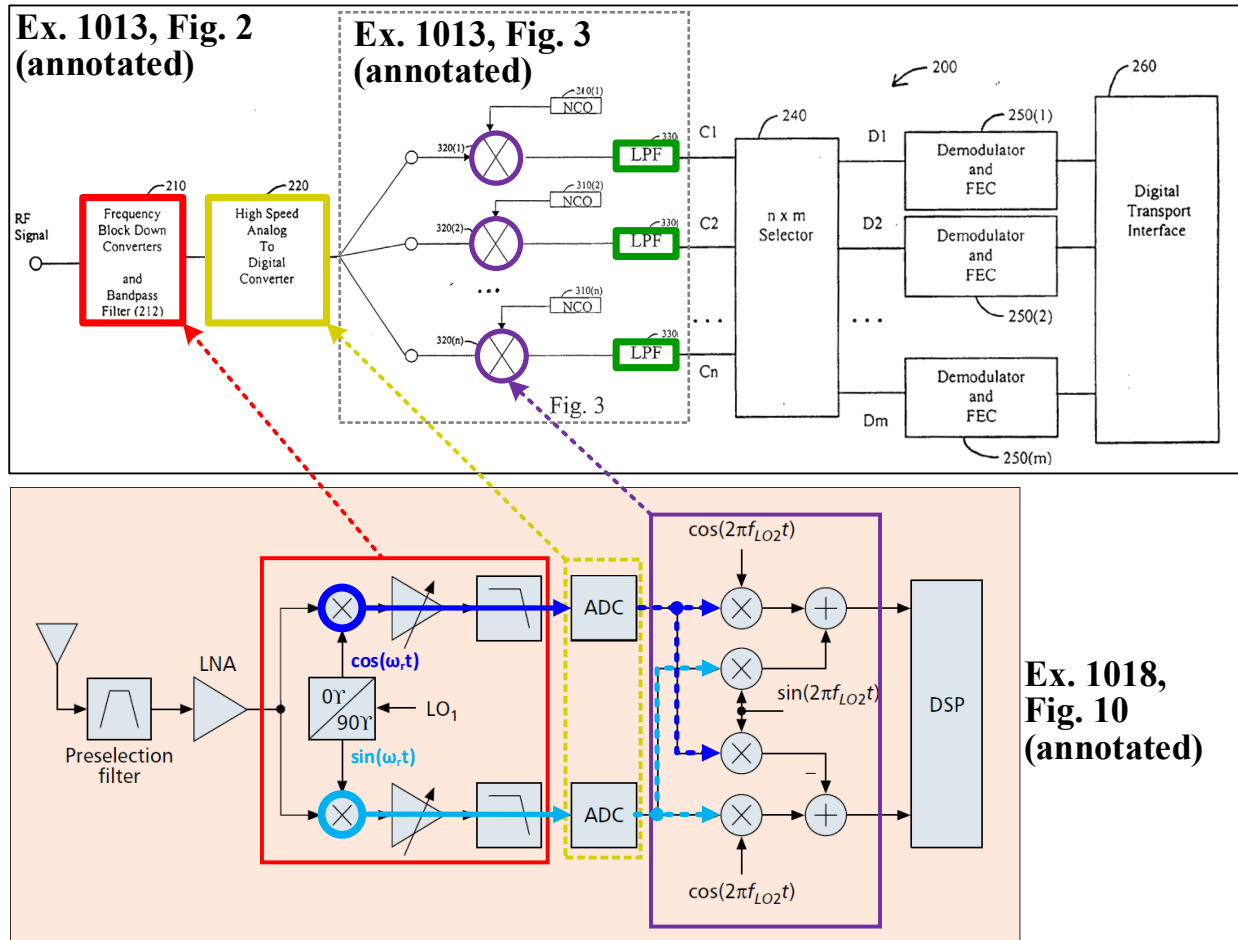
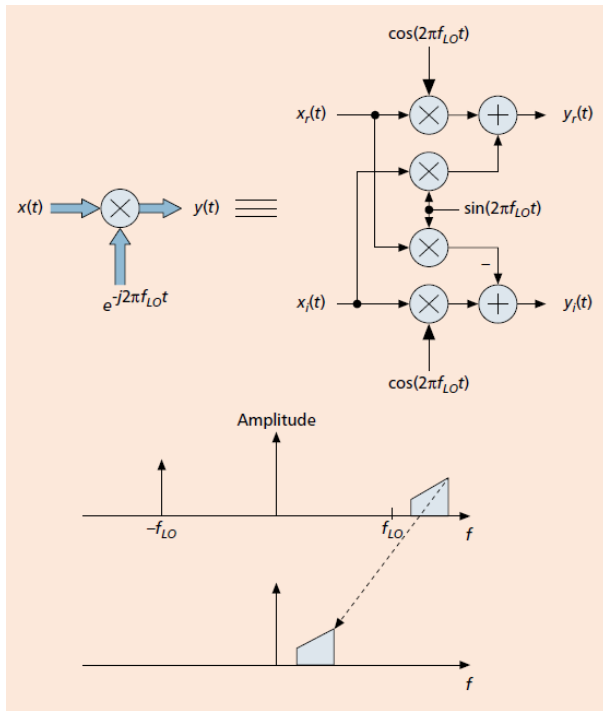


FIG. 3
Ex. 1001, Fig. 3 (annotated)

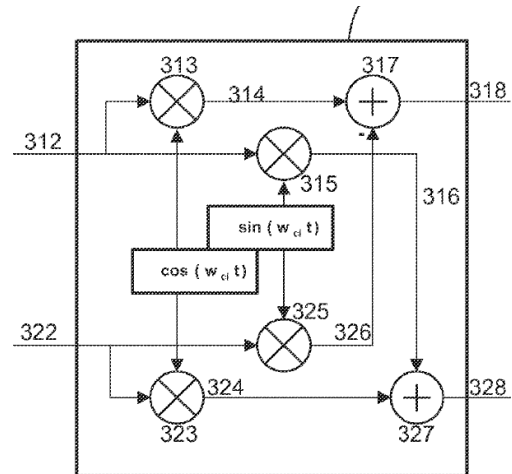
Zhang-Mirabbasi, as discussed above with respect to claim 6, teaches the same or equivalent structure, with any differences being insubstantial (e.g., multiple parallel paths, each including a complex mixer followed by a low pass filter followed by serial and parallel interfaces as shown in Figures 2 and 3 of Zhang and Figure 2 of the '362 patent). Ex. 1002, ¶ 216.



Moreover, Mirabbasi's complex mixer has the identical structure and performs the identical downconversion (i.e., shifting the frequency of in-phase and quadrature components of the digital complex input signal) as mixer 300 shown in Figure 3 of the '362 patent. Ex. 1018, pp. 9-10, Fig. 3; Ex. 1001, Fig. 3, 6:7-25, 9:17-22; *see also* Ex. 1025, pp. 279-280; Ex. 1034, p. 63; Ex. 1002, ¶ 217.



Ex. 1018, Fig. 3



Ex. 1001, Fig. 3 (excerpted)

In both Zhang-Mirabbasi and the '362 patent, each path performs the same function of selecting and outputting a respective desired channel in the same way by, first, downconverting the respective desired channel to baseband and, then, low pass filtering with a filter to isolate the channel, to achieve the same result of producing a plurality of desired channels as a digital data stream. Ex. 1002, ¶ 218.

Thus, Zhang-Mirabbasi renders claims 1-6 and 8-9 obvious, and Zhang-Mirabbasi-Karabinis renders claim 7 obvious, for the reasons stated above (Sections VII.A.1-3, VII.D.1), even if “digital circuitry” is given a means-plus-function construction. Ex. 1002, ¶ 219.

3. Claims 2 and 3 based on Zhang-Mirabbasi-Pandey (Ground G), and Claim 10 based on Mirabbasi-Jensen (Ground H)

The features added for “digital circuitry” to Zhang from Mirabbasi as discussed above with respect to claim 1 (Sections VII.F.2), are independent of the Pandey features (e.g., parallel and serial interfaces) added to Zhang in Ground C (Section VII.B) for claims 2 and 3, and the Jensen features (a decimator circuit) added to Zhang in Ground F (Section VII.E) for claim 10. Ex. 1002, ¶ 220. Thus, a POSITA would have added Mirabbasi’s teachings of a digital circuitry (Sections VII.F.2) to each of these combinations with the same motivations and expectation of success. Ex. 1002, ¶ 220.

Thus, Zhang-Pandey-Mirabbasi (ground G) renders claim 2 and 3 obvious, and Zhang-Mirabbasi-Jensen (ground H) renders claim 10 obvious, for the reasons discussed above with respect to each of these claims, even if “digital circuitry” is given a means-plus-function construction. Ex. 1002, ¶ 221.

VIII. GROUNDS FOR STANDING & FEE PAYMENT

Petitioner hereby certifies that the ’362 patent is available for, and Petitioner is not barred or estopped from requesting, *inter partes* review challenging claims 1-20.

Pursuant to 37 C.F.R. § 42.103, the undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

IX. CONCLUSION

Inter partes review should be instituted and claims 1-20 canceled.

Dated: February 16, 2024

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,908, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,799 words as counted by the Word Count feature of Microsoft Word and 109 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: February 16, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of this Petition for *Inter Partes* Review in connection with U.S. Patent No. 9,210,362 and supporting evidence to be served via FedEx Priority Overnight on February 16, 2024, on the following:

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Dated: February 16, 2024

By: /Frederic M. Meeker/

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CLAIM LISTING APPENDIX

U.S. Pat. No. 9,210,362

Designation	Claim Language
Claim 1	
[1A]	A wideband receiver system comprising:
[1B]	a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[1C]	a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;
[1D]	digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.
Claim 2	
2	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.
Claim 3	
3	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.
Claim 4	
4	The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.
Claim 5	
[5A]	The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises:
[5B]	a first ADC configured to generate a digital in-phase signal; and
[5C]	a second ADC configured to generate a digital quadrature signal.

Designation	Claim Language
Claim 6	
6	The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.
Claim 7	
[7A]	The wideband receiver system of claim 6, wherein:
[7B]	prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[7C]	after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 8	
8	The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.
Claim 9	
9	The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 10	
10	The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.
Claim 11	
[11A]	A method comprising: in a wideband receiver system:
[11B]	downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[11C]	digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

Designation	Claim Language
[11D]	selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and
[11E]	outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.
Claim 12	
12	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.
Claim 13	
13	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.
Claim 14	
[14A]	The method of claim 11, comprising:
[14B]	generating, by a first mixer of said mixer module, an in-phase signal; and
[14C]	generating, by a second mixer of said mixer module, a quadrature signal.
Claim 15	
[15A]	The method of claim 11, comprising:
[15B]	generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and
[15C]	generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.
Claim 16	
16	The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.
Claim 17	
[17A]	The method of claim 16, wherein:
[17B]	prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[17C]	after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 18	

Designation	Claim Language
18	The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.
Claim 19	
19	The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 20	
20	The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.