UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner

v.

ENTROPIC COMMUNICATIONS, LLC.,
Patent Owner.

Patent No. 9,210,362
Filing Date: February 5, 2015
Issue Date: December 8, 2015
Title: WIDEBAND TUNER ARCHITECTURE

Inter Partes Review No.: IPR2024-00432

DECLARATION OF DAVID B. LETT

IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.*

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I, David B. Lett, declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

1. INTRODUCTION

1. I have been retained as an expert witness on behalf of the Petitioner, Comcast Cable Communications, LLC, for the above-referenced *inter partes* review proceeding.

2. I have been asked to provide a declaration regarding certain matters pertaining to U.S. Patent No. 9,210,362 ("the '362 patent") (Ex. 1001) and the unpatentability grounds set forth in the Petition for this proceeding. My experience with television distribution systems, Set Top Boxes (STBs), modulation schemes, radio frequency systems, Video on Demand (VOD), and content delivery systems provides me with an understanding of the subject matter described and claimed in the '362 patent.

3. I am being compensated at my usual consulting rate or testimony rate of $385 per hour. My compensation is in no way dependent upon my opinions or testimony or the outcome of this proceeding. I have no financial interest in the party or in the outcome of this proceeding.

2. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

4. I am a technical consultant and product development industry veteran with expertise in electronics, software, hardware, video, audio, and data communications, having led product development organizations in cable, satellite, consumer electronics, home automation, asset tracking, remote tank logistics, and alarm industries. My current curriculum vitae is attached as Ex. 1003 and some highlights follow.

5. I earned my B.S. in Electrical Engineering (1982) with high honors from the University of Tennessee in Knoxville, Tennessee. I also attended the Georgia Institute of Technology from 1986 to 1987, completing 40% of the required degree hours for the M.S. Electrical Engineering program.

6. From 1982 to 1985, I worked at Scientific Atlanta as an Electrical Engineer designing video, audio, and data communications equipment for the cable television industry. I designed software and hardware including addressable data transmitters, video sync suppression scramblers, transaction format converters, and data channel monitors for addressable Cable Television systems and Set Top Boxes.

7. From 1983 to 1985, while working at Scientific Atlanta, I also worked as an Assistant Professor at DeVry Institute of Technology, teaching courses in electronics and microprocessor hardware/software.

8. From 1985 to 1990, I worked at Wegener Communications as a Senior Electrical Engineer, designing satellite communications equipment including forward error correction (FEC) coding systems, PSK modems, and analog control systems for RF modulators and PSK demodulators. I was promoted to the Hardware Engineering Manager, where I managed product development of video, audio, and data satellite receivers, modulators, graphics display systems, DSP-based compandors, FSK and PSK satellite modems, multiplexers, forward error correction (FEC) codecs, RF upconverters and downconverters, and baseband analog and digital processing components.

9. In 1990, I returned to Scientific Atlanta, which was acquired by Cisco in 2006. I worked as Engineering Manager running the set top box engineering group where I was promoted to Director and Vice President during my tenure until 2011. I led the design of many cable set top boxes and systems through the evolution of analog video, addressability, downloadable software, electronic program guides, digital video, VOD, software applications, high-definition TV, DVR, DOCSIS, full spectrum tuners, and multiroom DVR. These systems implemented various technologies including DOCSIS 1/2/3 and hybrid gateways, 802.11, IPTV, DVR, cable modems, ADSL, VDSL, DVB-T/C/S, bootloaders, factory diagnostics, application frameworks, Nagra, DRMs, conditional access, secure microprocessors, device management, Android, Adobe Flash, Linux, DVD play/record, MPEG-4,

MPEG-2, H.264, NTSC, PAL, DAVIC, MoCA, high-performance CPUs, cablecards, network processors, HDMI, multiple video/audio display interfaces, 2D/3D graphics, multiple RF tuners, and full spectrum tuners.

10. From 2011 to 2016, I worked for EchoStar Technologies, which served as the product development organization for sister company DISH Network. I served as Vice President of Engineering and was the Head of the Atlanta research and development center. I led the development of satellite set top boxes, consumer electronic equipment, and a home automation and security system. Technologies used included video/audio, IoT, H.265, HEVC, 3D, Satellite, wireless, MoCA, transcoding, embedded C Linux applications, mobile applications (IOS and Android), SaaS, web applications (JavaScript, HTML), BSS/OSS, AWS cloud storage, 2-way video/audio streaming, authentication, and VoIP.

11. In 2016, I started an independent consulting business in technology and intellectual property projects. I have consulted in various technology areas and industries including consumer electronics, Internet of Things (IoT), cable, satellite, television, media, and cryptocurrency.

12. From 2019 to 2022, I worked as Chief Technology Officer for Telular, an Ametek company. I was responsible for the development of Industrial Internet of Things (IIoT) recurring revenue solutions, combining wireless technologies,

purpose-built hardware, and SaaS in the commercial telematics, security and home automation markets and sold under the SkyBitz and Telguard brands.

13. My record of professional service includes awards on products I designed and developed from several organizations in my field of expertise, including Best of Show, Technology Emmy, and Best of Innovations.

14. I am a named inventor on at least 87 patents and published patent applications corresponding to the areas of my professional work. The patents and published applications involving video and audio technologies include:

- U.S. Patent No. 9,882,736 titled "Remote Sound Generation for a Home Automation System"
- U.S. Patent No. 9,615,139 titled "Determining Device That Performs Processing of Output Pictures"
- U.S. Patent No. 8,549,567 titled "Media Content Sharing Over a Home Network"
- U.S. Patent No. 8,161,388 titled "Interactive discovery of display device characteristics"

- U.S. Patent Nos. 8,120,924, 7,240,217, 6,785,817, 6,564,324, 6,212,278, and 5,440,632 titled "Reprogrammable Subscriber Terminal"

- U.S. Patent No. 7,908,625 titled "Networked Multimedia System"

- U.S. Patent Nos. 7,861,272 and 7,849,486 titled "Networked Subscriber Television Distribution"

- U.S. Patent Nos. 7,774,820 and 7,069,578 titled "Settop Cable Television Control Device and Method Including Bootloader Software and Code Version Table for Maintaining and Updating Settop Receiver Operating System Software"

- U.S. Patent No. 5,771,064 titled "Home Communications Terminal having an Applications Module"

- U.S. Patent No. 5,715,515 titled "Method and Apparatus for Downloading On-Screen Graphics and Captions to a Television Terminal"

- U.S. Patent No. 5,657,414 titled "Auxiliary Device Control for a Subscriber Terminal"

- U.S. Patent No. 5,592,551 titled "Method and Apparatus for Providing Interactive Electronic Programming Guide"
- U.S. Patent No. 5,539,822 titled "System and Method for Subscriber Interactivity in a Television System"
- U.S. Patent No. 5,357,276 titled "Method of Providing Video On Demand with VCR Like Functions"
- U.S. Patent Application Publication Nos. 2004/0068753 and 2008/0072272 titled "Video Transmission Systems and Methods for a Home Network"
- U.S. Patent Application Publication No. 2004/0133911 titled "Subscriber Network in a Satellite System"

15. I have a general understanding of the U.S. patent prosecution process and of the novelty and non-obviousness requirements for patentability.

16. I believe that my extensive industry experience and educational background qualify me as an expert in the relevant field of digital signal processing (DSP) and radio frequency (RF) tuning systems for satellite and/or cable communications. I am knowledgeable of the relevant skill set that would have been possessed by a hypothetical person of ordinary skill in the art at the time of the

invention of the ’362 patent, which I (as I discuss below) understand is early 2009 or early 2010.

3. MATERIALS CONSIDERED

17. In formulating my opinion, I reviewed and considered the ’362 patent (U.S. Pat. No. 9,210,362 to Reddy, et al.) (Ex. 1001), as to which I am offering my opinion regarding the validity of certain claims, as discussed herein.

18. In preparing this declaration, I also reviewed and considered the Petition and the file history of the ’362 patent (included in Ex. 1004) as well as the following references:

Ex. 1001:	U.S. Patent No. 9,210,362 (“the ’362 patent”)
Ex. 1003:	Curriculum Vitae of David B. Lett
Ex. 1004:	Certified Prosecution History of the ’362 patent
Ex. 1005:	Certified Prosecution History of U.S. Patent No. 9,100,622
Ex. 1006:	Certified Prosecution History of U.S. Patent No. 8,526,898
Ex. 1007:	Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“’526 provisional”)
Exs. 1008-1012:	Reserved
Ex. 1013:	U.S. Pub. No. 2003/0056221 (“Zhang”)
Ex. 1014:	U.S. Patent No. 7,237,214 (“Pandey”)

Ex. 1015:	Excerpts of "IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition" (IEEE Press. 2000) ("IEEE Std 100")
Ex. 1016:	Excerpts of Jan M Rabaey, "Digital Integrated Circuits: A Design Perspective" (Pearson, 2nd ed. 2002) ("Rabaey")
Ex. 1017:	A. P. Chandrakasan, "Ultra low power digital signal processing," Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 ("Chandrakasan")
Ex. 1018:	S. Mirabbasi and K. Martin, "Classical and Modern Receiver Architectures," IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 ("Mirabbasi")
Ex. 1019:	U.S. Patent No. 6,061,406 ("Carson")
Ex. 1020:	U.S. Pub. No. 2006/0233147 ("Karabinis")
Ex. 1021:	Data-Over-Cable Service Interface Specifications, DOCSIS 2.0, Radio Frequency Interface Specification, CM-SP-RFIv2.0-I11-060602
Ex. 1022:	Certified File History (as of February 2, 2024) for *Ex Parte* Reexamination No. 90/019,255
Ex. 1023:	Certified Prosecution History of U.S. Patent No. 9,100,363

Ex. 1024: Reserved

Ex. 1025: J. Crols and M. S. J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 ("Crols")

Ex. 1026: U.S. Pub. No. 2007/0027943 ("Jensen")

Ex. 1027: U.S. Patents and Patent Applications Family Tree for U.S. Patent No. 9,210,362

Ex. 1028: Reserved

Ex. 1029: Entropic Communications, LLC v. Charter Communications, Inc., No. 2:22-cv-00125-JRG (E.D. Tex. June 26, 2023) (Claim Construction Memorandum Opinion and Order)

Exs. 1030-1031:

Ex. 1033: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, "Modern Cable Television Technology: Video, Voice, and Data Communications" (2nd ed. 2004) ("Ciciora")

Ex. 1034: Excerpts of J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design" (1997)

Ex. 1035: U.S. Patent No. 7,340,230 ("Khoini-Poorfard")

Ex. 1036: U.S. Pub. No. 2003/0217362 ("Summers")

Ex. 1037: U.S. Pub. No. 2006/0256799 ("Eng")

Ex. 1038: U.S. Pub. No. 2006/0083335 ("Seendripu")

Ex. 1039: Excerpts of Chris Bowick, "RF Circuit Design" (2nd ed. 2008)

Ex. 1040: Reserved

Ex. 1041: Excerpts of Roland Priemer, "Introductory Signal Processing" (1991)

Ex. 1042: U.S. Patent No. 7, 272,375 ("Tuttle")

Ex. 1043: U.S. Patent No. 7,130,576 ("Gurantz")

Ex. 1044: U.S. Patent No. 5,278,837 ("Kelly")

Ex. 1045: Jeffrey Hugh Reed, "Software Radio: A Modern Approach to Radio Engineering" (2002)

Ex. 1046: U.S. Patent No. 7,213,042 ("Cannon")

Ex. 1047: Reserved

Ex. 1048: Excerpts of William Buchanan, "Computer Busses" (2000) ("Buchanan")

Ex. 1049: U.S. Patent No. 7,079,528 ("Ziegler")

Ex. 1050:	Excerpts of "Software Defined Radio: Enabling Technologies" (Walter H.W. Tuttlebee ed., 2003)
Exs. 1051-1072:	Reserved
Ex. 1073:	Expert Declaration of Dr. Sylvia Hall-Ellis
Ex. 1074	Reserved
Ex. 1075	U.S. Patent No. 6,791,995 ("Azenkot")
Ex. 1076	U.S. Patent No. 6,542,203 ("Shadwell")

4. UNDERSTANDING OF APPLICABLE LEGAL STANDARDS

19. Although I am not an attorney, I have a general understanding of the applicable legal standards pertaining to the patentability issues presented in this proceeding. I understand that the Petitioner is challenging the patentability of the claims of the '362 patent based on the following grounds:

- Ground A: Claims 1-3, 8, 9, 11-13, 18, and 19 anticipated by Zhang under pre-AIA 35 § 102(b) .
- Ground B: Claims 1-3, 8, 9, 11-13, 18, and 19 as obvious under pre-AIA § 103(a) based on Zhang.
- Ground C: Claims 2, 3, 12, and 13 as obvious under pre-AIA § 103(a) based on Zhang in view of Pandey.

- Ground D: Claims 1-3, 4-6, 8-9, and 14-16 as obvious under pre-AIA § 103(a) based on Zhang in view of Mirabbasi.
- Ground E: Claims 7 and 17 as obvious under pre-AIA § 103(a) based on Zhang in view of Mirabbasi and Karabinis.
- Ground F: Claims 10 and 20 as obvious under pre-AIA § 103(a) based on Zhang in view of Jensen.
- Ground G: Claims 2 and 3 as obvious under pre-AIA § 103(a) based on Zhang in view of Mirabbasi and Pandey.
- Ground H: Claim 10 as obvious under pre-AIA § 103(a) based on Zhang in view of Mirabbasi and Jensen.

20. I understand that, in this *inter partes* review, Petitioner has the burden of proving that each challenged claim is unpatentable by a preponderance of the evidence.

21. I understand that to be valid, a patent claim must be "novel," and is invalid if "anticipated" by a single prior art reference. I further understand a reference anticipates if it discloses each and every element as arranged in the claim so as to enable a person of ordinary skill in the art to make and use the claimed invention without undue experimentation.

22. I understand that a patent claim is unpatentable if, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine

the teachings of the prior art to yield the patent claim. It is my understanding that this determination is made after weighing the following factors: (1) the level of ordinary skill in the pertinent art; (2) the scope and content of the prior art; (3) the differences between the prior art as a whole and the claim at issue; and (4) as appropriate, other objective considerations identified below.

23. It is my understanding that the prior art and claimed invention should be viewed through the knowledge and understanding of a person of ordinary skill in the art – one should not use his or her own insight or hindsight in deciding whether a claim is obvious. I further understand that a claim may be rendered obvious if a person of ordinary skill in the art can implement the claimed invention as a predictable variation of a known product. I further understand that a person of ordinary skill in the art is presumed to have knowledge of the relevant prior art at the time of the claimed invention, which comprises any prior art that was reasonably pertinent to the particular problems the inventor faced.

24. I understand that a showing of obviousness requires some articulated reasoning with a rational underpinning to support the combination of the references. I understand that in consideration of the issue of obviousness it is important to identify whether a reason existed at the time of the invention that would have led a person of ordinary skill in the pertinent art to combine elements of the references in a way that yields the claimed invention.

25. I understand that a claim may be considered unpatentable for obviousness for various reasons. I have been informed that the following exemplary rationales may support a finding of obviousness:

(A) combining prior art elements according to known methods to yield predictable results;

(B) substituting one known element for another to obtain predictable results;

(C) use of a known technique to improve similar devices in the same way;

(D) applying a known technique to a known device ready for improvement to yield predictable results;

(E) choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;

(F) known work in a field that prompts variations in the work in the same or a different field that leads to predictable results; and

(G) some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify a prior art reference or combine multiple prior art references or teachings to arrive at the claimed invention.

26. I understand that various objective or "real world" factors may be indicative of non-obviousness. I understand that such factors include:

(A) the commercial success of the claimed invention;

(B) the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;

(C) failed attempts to solve the problem solved by the claimed invention;

(D) copying of the claimed invention;

(E) unexpected results of the claimed invention;

(F) praise for the claimed invention by others in the relevant field; and

(G) willingness of others to accept a license under the patent because of the merits of the claimed invention.

27. It is my understanding that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link may be based on the common sense of the person of ordinary skill in the pertinent art. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and market demand is sufficient motivation to combine references.

28. It is my understanding that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, common sense is a good reason for a person of ordinary skill to pursue known options when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions.

29. I further understand that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, it is my understanding that any need or problem known in the field at the time of invention and addressed by the patent can provide a reason for combining the limitations in the manner claimed.

5. THE RELEVANT ART AND LEVEL OF ORDINARY SKILL IN THE RELEVANT ART

30. I understand that obviousness is determined from the vantage point of a person of ordinary skill in the relevant art at the time of the alleged invention ("POSITA"). The '362 patent is directed to a wideband receiver system 200 "capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum." Ex. 1001, 1:18-23. I understand that a person of ordinary skill in the art is one who is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity.

31. I believe that a person of ordinary skill in the art of the '362 patent, at the time of the alleged invention of the '362 patent, would have a degree in electrical engineering or a similar discipline, along with three-to-four years of experience with digital signal processing (DSP) and radio frequency (RF) tuning systems for satellite and/or cable communications. Additional education may substitute for professional

experience, and significant work experience may substitute for formal education. I worked in the relevant field with such persons at, and leading up to, the time of the alleged invention of the ’362 patent, and thus, I am familiar with the knowledge that such persons had at the time (*i.e.*, early 2009 or early 2010). At that time, I had a skill level that was at least as high as the skill level I describe above for a person of ordinary skill in the art of the ’326 patent.

32. All of my statements in this declaration regarding what a person of ordinary skill in the art would have known, understood, appreciated, been motivated to do, etc., refer to a person of ordinary skill in the art in early 2009 to early 2010, before the earliest claimed priority date of the ’362 patent (which, as I discuss below, is April 17, 2009).

6. CLAIM CONSTRUCTION

33. I understand that my analysis requires an understanding of the scope of the claims of the ’362 patent. I understand that claim terms subject to *inter partes* review, absent some other definition provided in the patent, are given their ordinary meaning to a person of ordinary skill in the art in light of the patent specification. Therefore, in my analyses given below, I have assumed that all claim terms are given their ordinary interpretation as would have been understood by a POSITA reading the patent specification as of the priority date. I further understand that certain claim terms may be means plus function limitations. In particular, I understand that a

"means plus function" limitation should be interpreted to cover only the corresponding structure described in the specification that performs the recited function, and equivalents thereof. I also understand that a limitation will be presumed to be a means plus function limitation if (a) the claim limitation uses the phrase "means for"; (b) the "means for" is modified by functional language; and (c) the phrase "means for" is not modified by sufficient structure for achieving the specified function. I understand that a structure will be considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For example, a structure may be deemed to be a structural equivalent to the corresponding structure where the structure performs the same function in substantially the same way to achieve substantially the same result.

34. Though no claims in the '362 patent include "means for" language, I have been asked to consider a potential construction of "digital circuitry" in claim 1 as a means-plus-function limitation. Should the term be construed as such, the corresponding structure that performs the recited function for this limitation is illustrated in Figures 2 and 3, including complex mixers 250 and 300, and filters 260, 330, and 340. Ex. 1001, Figs. 2-3, 5:31-54, 6:7-58. As I discuss in my detail analysis below, the prior art discloses this limitation whether or not it is construed as a means-plus-function limitation. Further, it is my opinion that the term

"wideband" in the claims would be understood by a POSITA as a band that carries multiple channels, in view of the specification of the '362 patent that implicitly defines the term this way. For example, the '362 patent states that a receiver is "wideband" if it is "designed to concurrently receive several TV channels." Ex. 1001, 1:24-27, 1:16-18 ("wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum."). The '362 also refers to "the invention" as relating "to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum." Ex. 1001, 1:19-23 . While described as part of the invention, I note that "non-contiguous portions" is omitted from the independent claims and added only in dependent claims 7 and 17, which would lead a POSITA to conclude that receiving desired channels over "non-contiguous portions" are not necessary for a receiver to be considered "wideband" as that term is used in the '362 patent. In my opinion, this is consistent with the ordinary and customary meaning of "wideband." Nonetheless, even if non-contiguous bands were required, Zhang discloses it as presented below.

35. It is my understanding that the '362 patent was asserted in various litigations in California and in a litigation in Texas. In the Texas litigation, the court construed claim 11 of the '362 patent as requiring that the "digitizing …' step must be performed before the 'selecting …' step, and the 'selecting …' step must be

performed before the 'outputting …' step," but with "[n]o other order of steps" required. Ex. 1029 at 52. The parties in this case also agreed that "wideband analog-to-digital converter (ADC) module" should be given its plain and ordinary meaning. Ex. 1029, pp. 7-8.

7. OVERVIEW OF THE '362 PATENT

36. The '362 patent describes a wideband receiver system 200 for "capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum." Ex. 1001, 1:18-23.

37. The '362 patent states that the system groups the desired channels that extend over non-contiguous portions of the frequency spectrum "into a contiguous, or substantially-contiguous, frequency spectrum" to "increase the dynamic range without requiring expensive data conversion, filtering, and channel selection at the demodulator." Ex. 1001, 1:18-23, 2:24-27. According to the '362 patent, a receiver is "wideband" if it is "designed to concurrently receive several TV channels." *Id*., 1:24-27. Figure 2 is a "schematic block diagram of a wideband receiver system 200." *Id*., 4:16-18.

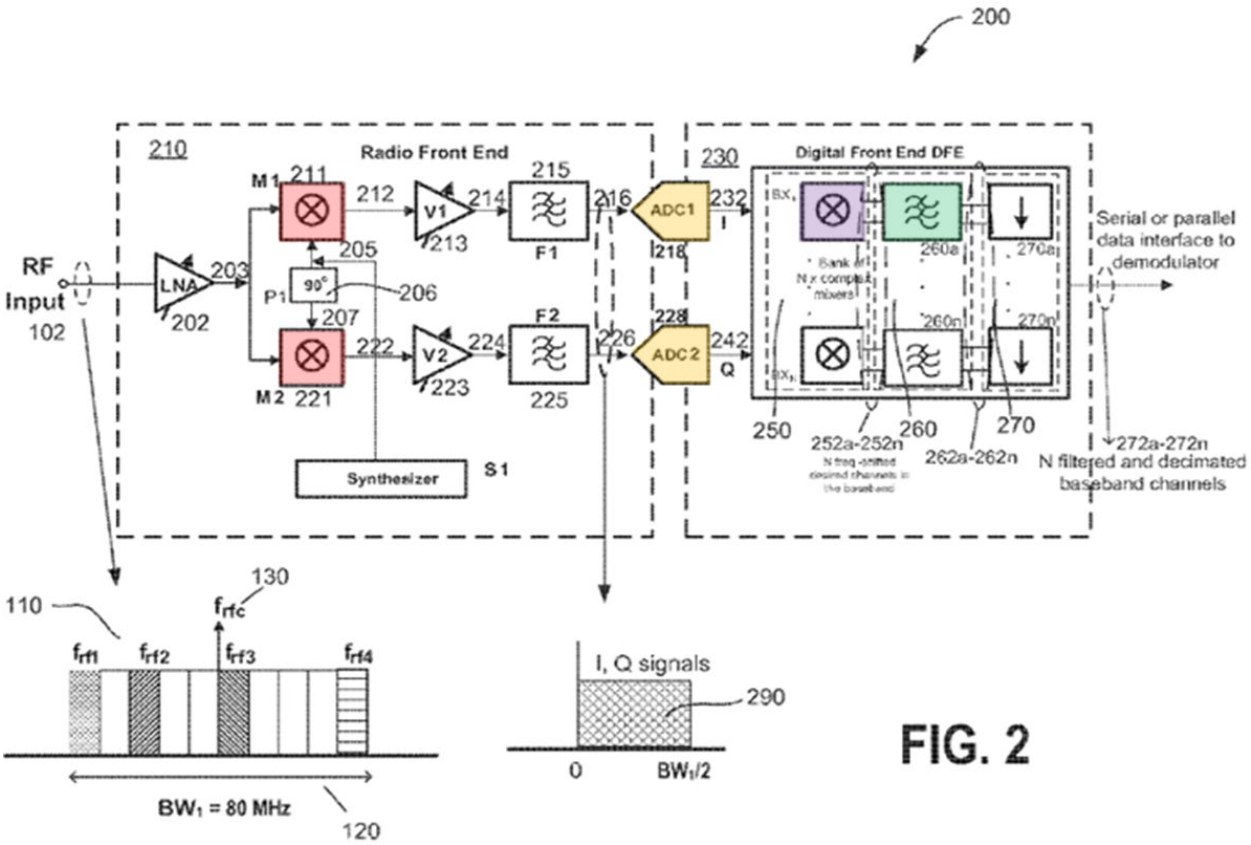


FIG. 2

Ex. 1001, Fig. 2 (annotated)

38. The wideband receiver system 200 receives both desired and undesired television channels as frequencies dispersed within a frequency bandwidth BW_1. Ex. 1001, Abstract, 1:19-22. Mixers "M1" and "M2," which are shown in red above, "generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90 degree between them" and that have been downconverted to "the baseband or low intermediate frequency (IF) band." Ex. 1001, 4:40-46, 2:45-49, *see* also 1:60-62. "[U]nwanted frequency components" are filtered from the in-phase signal and the quadrature signal by respective filters 215 and 225. Ex. 1001, 4:64-5:3. The filtered signals are then individually digitalized by wideband analog-to-digital

converters ADC1 and ADC2 (**gold**) to generate a digital in-phase (I) signal 232 and a digital quadrature (Q) signal 242. Ex. 1001, 2:49-51, 5:28-31. U.S. Provisional App. No. 61/170,526 ("the '526 provisional"), which the '362 patent incorporates by reference, admits that the left side of Figure 2 (up to and including ADC1 and ADC2) "is similar to conventional tuners." Ex. 1007, p. 5; Ex. 1001, 1:5-11.

39. The digital I and Q signals 232 and 242 are input to a bank of N complex mixers 250 (one of which is shown above in **purple**) in a digital front end 230, where "N is an integer value corresponding to the number of desired RF channels." Ex. 1001, 5:31-35. "Each of the N complex mixers … extract[s] a different one of the desired channels" from the I and Q signals 232 and 242 and "frequency-shifts the extracted signals to the baseband frequency." Ex. 1001, 5:49-52. An associated filter module of filters 260a-260*n* (one of which is shown above in **green**) filters the frequency-shifted desired channel. Ex. 1001, 5:52-54.

40. Figure 3 "is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230" and shows elements in one of the rows of digital front end 230 in Figure 2. Ex. 1001, 5:62-64.

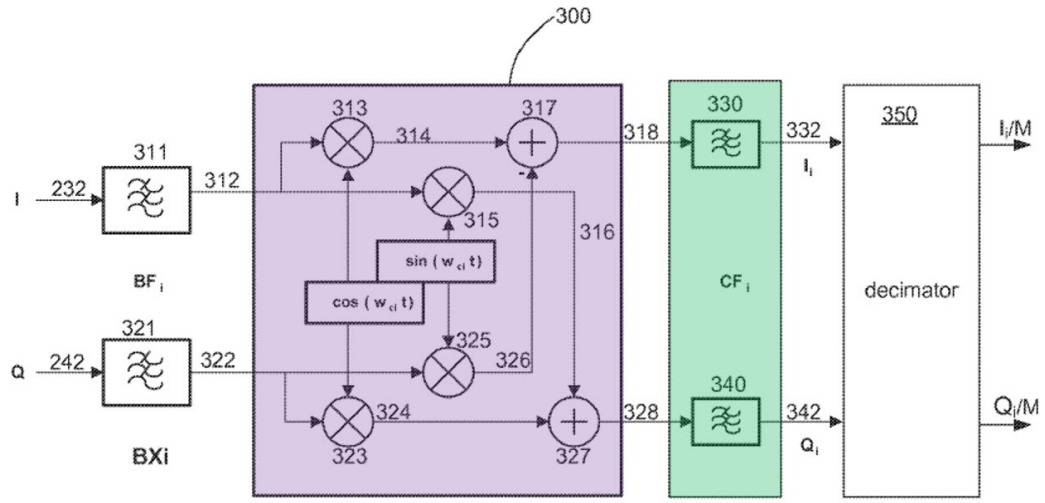


FIG. 3

Ex. 1001, Fig. 3 (annotated)

41. Mixer 300 (**purple**) represents one of the complex mixers 250 and has multipliers 313, 315, 323, and 325 and adders 317 and 327. Ex. 1001, 6:7-17. "[C]omplex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain" by using a frequency ω_{ci} that is chosen such that "each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband." Ex. 1001, 6:17-34. The baseband signals 318 and 328 are filtered by filters 330 and 340 (**green**) that are "one of the filters 260a-n" shown in Figure 2. Ex. 1001, 6:43-45.

42. After decimation, "the N desired baseband channels will be sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods." Ex. 1001, 6:55-58. The '362

patent does not provide any details of how N x 2 signals (N channels, with an I and a Q signal for each channel) might be manipulated, combined, and/or otherwise processed between the decimators 270 and a demodulator. Rather, the ’362 patent admits that this is performed “according to commonly known methods.” *Id*.

7.1. Prosecution History

43. It is my understanding that U.S. Application No. 14/614,543 (“’543 application”), which issued as the ’362 patent, was filed on February 5, 2015. The ’543 application was filed with 20 claims including independent claims 1 and 11. Ex. 1004 at 32-35. On May 14, 2015, Office Action rejected all claims on the basis of nonstatutory double patenting over claims 1-27 of U.S. Patent No. 8,526,898, and Applicant filed a terminal disclaimer on May 15, 2015. Ex. 1004 at 75-79, 90-99. On August 7, 2015, Notice of Allowance stated that the prior art failed to describe a wideband receiver system with “digital circuitry configured to select a plurality of desired television channels from the digitized plurality of frequencies and output said plurality of television channels to a demodulator as a digital datastream.” Ex. 1004 at 107. Applicant filed a Request for Continued Examination (RCE) and an Information Disclosure Statement (IDS) on September 11, 2015. Ex. 1004 at 115-122. An October 5, 2015, second Notice of Allowance stated that the IDS “did not present prior art that comprise [*sic*] the inventive claimed subject matter.” Ex. 1004 at 146. In an October 26, 2015, Amendment After Notice of Allowance, Applicant

amended dependent claims 5-7, 10, 16-17, and 20 to "merely clarify the antecedent basis for certain claim terms." Ex. 1004 at 160-165. The application issued as the '362 patent on December 8, 2015.

44. It appears that none of Zhang, Pandey, Mirabbasi, Karabinis, or Jensen was considered during prosecution of the '543 application. Ex. 1001, cover.

45. On September 20, 2023, Unified Patents, LLC filed a request, and in response the Office ordered reexamination (Control No. 90/019,255) on November 1, 2023 of independent claims 1 and 11 of the '362 patent. Ex. 1022 at 631-642. The reexamination is currently pending. It appears that none of Zhang, Pandey, Mirabbasi, Karabinis, or Jensen has been cited in the reexamination. Ex. 1022 at 634.

46. Reserved

7.2. Earliest Priority Date for the Claims

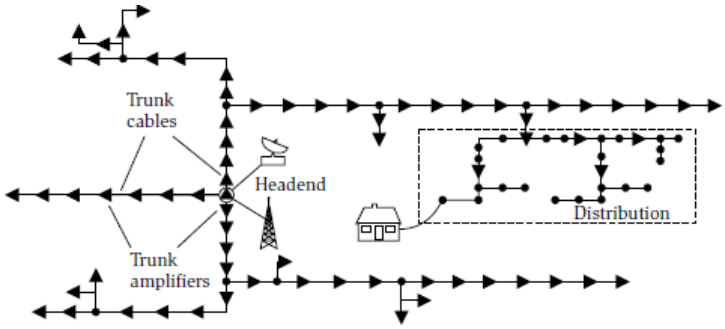
47. I understand that Application No. 14/614,543 ("the '543 application"), which eventually became the '362 patent, was filed on February 5, 2015. It is further my understanding that the '543 Application claims priority to a chain of applications that claim priority to the '526 provisional filed on April 17, 2009. It is my understanding that the '362 patent asserts to be entitled to a priority date of the filing date of the earliest application from which the '362 patent claims priority, *i.e.*, April 17, 2009, which is the filing date of the '526 provisional. Thus, the earliest possible

effective filing date for the claims of the ’362 patent is April 17, 2009. I understand that all of the references that I rely on in this Declaration were published or filed before April 17, 2009, and are prior art to that date.

8. OVERVIEW OF THE PRIOR ART

8.1. Cable and Satellite Television Networks

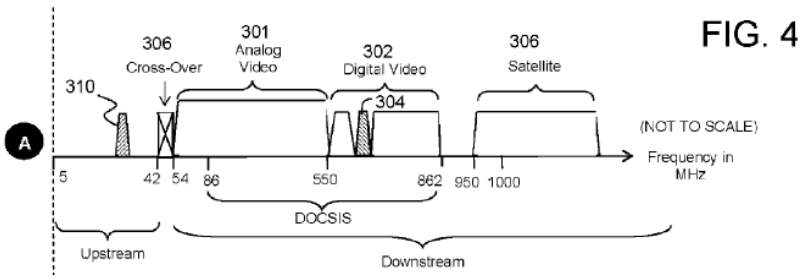
48. The origins of the cable and satellite television networks long predate the earliest claimed priority date (April 17, 2009) of the ’362 patent. Cable television networks are entertainment distribution systems that allow consumers to access and enjoy various television channels. Ex. 1033 at 22. The cable television networks include one or more headends that are designed to broadcast and distribute, via coaxial cables, the data for the television channels as modulated radio frequency (RF) signals to multiple terminal equipment belonging to the consumers (e.g., television receivers, set-top boxes, data modems, digital video recorders, personal video recorders, and other terminal equipment). Id. at 22, 29-30, 40, 352; Ex. 1034 at 20-21. This is illustrated in Figure 1.1 of Ex. 1033.



Ex. 1033, Fig. 1.1 (Excerpted) at 34

RF is the frequency range starting from 10 kHz to 100,000 MHz in the electromagnetic spectrum; signals having frequencies from this RF range are used for data transmission (wired or wireless) between devices. *See* Ex. 1015 at 7. The transmissions between the headends and the terminal equipment are governed by various well-known industry standards, including Data Over Cable Systems Interface Specification (DOCSIS). Ex. 1021 at 2-5, Fig. 1-2; Ex. 1033 at 27, 211-212.

49. Consumers can also access television channels from satellites via conventional home satellite television systems. Ex. 1035, 1:30-31; Ex. 1036, [0006]. Such home satellite television systems typically include a fixed dish antenna that receives television channels in modulated RF signals, as well as a satellite receiver or set-top box designed to process and demodulate the modulated RF signals. Ex. 1035, 1:31-35; Ex. 1036, [0013]. Satellites may also be used to distribute the television channels to headends of cable television networks, which are then redistributed to the consumers. Ex. 1033 at 262, 280-282; Ex. 1036, [0009].



Ex. 1037, Fig. 4 (Excerpted)

50. Figure 4 of Exhibit 1037 (partially reproduced above) illustrates the RF spectrum usage of television channels from cable and satellite television networks. Ex. 1037, [0079]-[0080]. In North America, television channels from cable television networks occupy the RF spectrum from 54 to 864 MHz, with digital channels occupying the RF spectrum above 550 MHz. Ex. 1033 at 413, 503; Ex. 1037, [0079]-[0080]. In 1941, the National Television System Committee, established by the United States Federal Communications Commission, set a standard that each television channel should be allocated 6 MHz of RF bandwidth and that the set of allocated television channels should occupy the RF spectrum in a contiguous manner. Ex. 1021 at 1, 23-24; Ex. 1033 at 45, 413, 515-520.

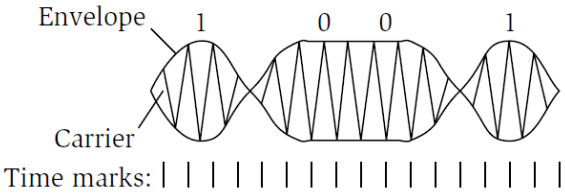
51. Television channels from satellite networks occupy various bands in frequencies greater than 950 MHz. Ex. 1035, 1:37-48; Ex. 1037, [0079]-[0080]. Signals in satellite bands are sent to a satellite receiver or set-top box, with the satellite bands carrying multiple transponder channels and each transponder channel carrying a number of different television channels. Ex. 1035, 1:37-48.

8.2. Modulated RF Signals

52. Modulation is a method where an RF carrier signal is varied (e.g., in amplitude, frequency, and/or phase) with information to be transmitted. Ex. 1033 at 155. The information to be transmitted can be digital data comprising of bits "1" and "0," such as the digital data of television channels for transmission from headends

of cable television networks or subscriber locations. *Id*. One of the main goals of modulation is to squeeze as much data into the allocated RF bandwidth as possible, and that objective, known as spectral efficiency, measures how quickly data can be transmitted in an assigned RF bandwidth. *Id.* at 156. The unit of measurement of spectral efficiency is bits per second per Hz (b/s/Hz). *Id.* As I discuss below, by the earliest claimed priority date of the ’362 patent, multiple modulation techniques facilitating high spectral efficiencies were known to a POSITA by the earliest claimed priority date of the ’362 patent.

8.2.1. Biphase Shift Keying



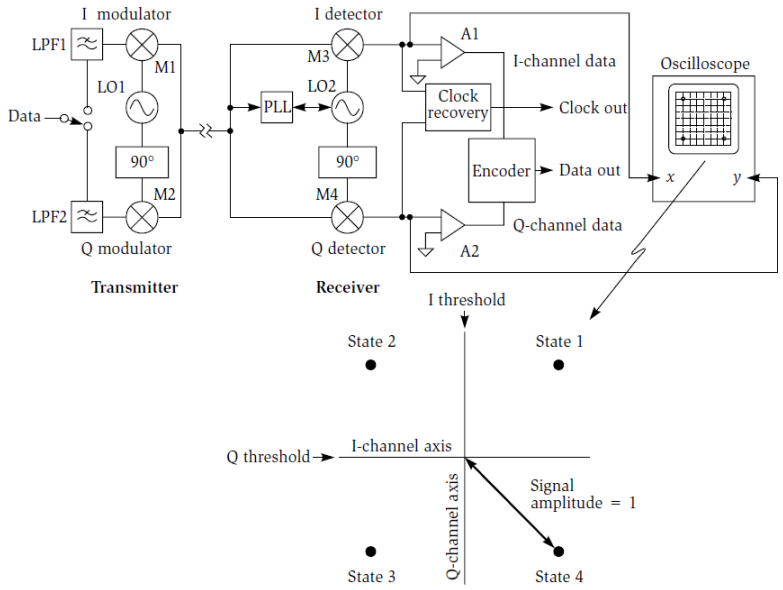
Ex. 1033, Fig. 4.3 (Excerpted) (page 161)

53. Biphase shift keying (BPSK) is a simple form of modulation that can be used in digital cable and satellite television networks, where the phase of an RF signal is shifted 180° in phase between transmission of bit “0” and bit “1.” Ex. 1033 at 160-161, Fig. 4.3 (partially reproduced above). The spectral efficiency of BPSK modulation is 1 bit/s/Hz. *Id.* at 156.

8.2.2. Quadrature Phase Shift Keying (QPSK)

54. In Quadrature Phase Shift Keying (also called 4-Quadrature Amplitude Modulation (4-QAM)), digital data is split into two components, an I (in-phase) component and a Q (quadrature) component. Ex. 1033 at 163-164, Fig. 4.4 (reproduced below). The same RF carrier signal is used for each component, but the phases of the two signals in the two components are 90° apart or in quadrature. *Id.* Signals in quadrature are orthogonal and do not interfere with one another. *Id.* Quadrature modulation takes advantage of this principal by combining two signals in quadrature for a combined output signal. *Id.* In quadrature modulation, digital data are broken into a discrete number of symbols, which are used to convey information. *Id.* at 164-165. These symbols are mapped to a discrete set of magnitude and phase values on an I/Q constellation, which are referred to as constellation points. *Id.* For example, in BPSK, each symbol can only represent a bit "0" or a bit "1" because the constellation of BPSK modulation has just two possible constellation points representing two possible states, or symbols, where each symbol represents a single bit of information. The constellation of QPSK modulation has four constellation points representing four different states, or symbols: state 1 (bits "00"), state 2 (bits "01"), state 3 (bits "11"), and state 4 (bits "11"). *Id*. QPSK can, therefore, transmit 2 bits per symbol. *Id.* The RF carrier signals in each of the I and Q components are encoded with one of the two bits of the symbol. *Id.* at 163. Therefore, QPSK can

transmit twice as much data using the same amount of bandwidth as BPSK, or it could transmit the same amount of data using half the bandwidth. *Id.* at 156.



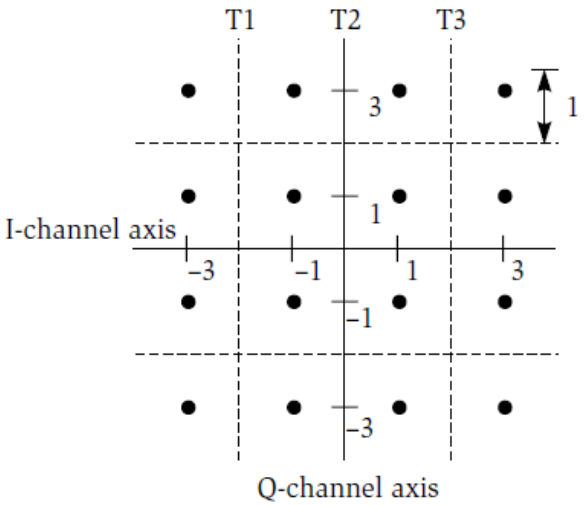
Ex. 1033, Fig. 4.4 (page 164)

55. After the two RF carrier signals from the two components I and Q are modulated, the RF carrier signals are combined for transmission to the receiver. Ex. 1033 at 163. At the receiver, the received combined signal is split back into the I-component and the Q-component by two mixers, M3 and M4. *Id.* The separation back into I/Q components allows the encoder inside the receiver to map the two components onto the QPSK I/Q constellation and interpret which of the four possible symbols are encoded in the components. *Id.* at 164.

56. A POSITA would have been well aware that satellite television networks primarily used QPSK modulation. Ex. 1033 at 280; Ex. 1036, [0071], [0075]. Satellite transponders that transmit RF signals to headends and dish antennas

are simply a frequency translator and a power amplifier, and for the sake of efficiency, it was preferred to use modulation formats that do not depend on amplitude changes to communicate information. Ex. 1033 at 280. QPSK modulation met this requirement of satellite transponders. *Id*.

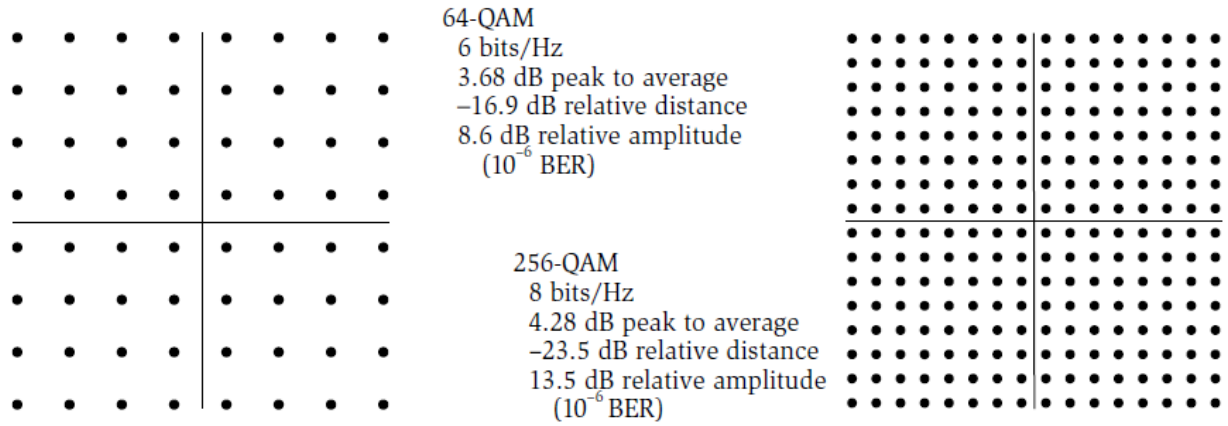
8.2.3. 16-Quadrature Amplitude Modulation (QAM), 64-QAM, and 256-QAM



Ex. 1033, Fig. 4.5 (Partial Excerpt) (page 167)

57. Modulation schemes with greater numbers of constellation points are able to transmit more information per symbol. Ex. 1033 at 166-169. The next denser known modulation format after QPSK was 16-QAM, where data is split into I and Q components and carried by two RF signals in quadrature. *Id.* at 166. However, the 16-QAM I/Q constellation has sixteen different states (as illustrated by the sixteen dots in Figure 4.5 of Ex. 1033, partially reproduced above), where each state is a symbol that contains one of 16 different combinations of amplitude

and phase levels. *Id.* Each symbol contains up to 4 bits and, therefore, can represent values from "0000" to "1111." *Id.* The spectral efficiency of 16-QAM is 4 bit/s/Hz. *Id*. at 168, Fig. 4.6.



Ex. 1033, Fig. 4.6 (Partial Excerpt) (page 168)

58. Similarly, the I/Q constellation of 64-QAM (illustrated by Figure 4.6 of Ex. 1033, partially reproduced above) has sixty-four different states, where each state is a symbol that contains one of 64 different combinations of amplitude and phase levels. *Id*. Each symbol contains up to 6 bits (representing values from "000000" to "111111"), and the spectral efficiency of 64-QAM is 6 bit/s/Hz. *Id.* The I/Q constellation of 256-QAM has 256 different states, where each state is a symbol that contains one of 256 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 8 bits (representing values from "00000000" to "11111111"), and the spectral efficiency of 256-QAM is 8 bit/s/Hz. *Id.*

59. DOCSIS (finalized in 1997), DOCSIS 1.1 (finalized in 2001), and DOCSIS 2.0 (finalized in 2002) mandate the use of either 64-QAM or 256-QAM for

downstream data transmission from headends to consumers' terminal equipment. Ex. 1033 at 168, 213-214. Therefore, a POSITA would have known that terminal equipment receiving signals from headends of cable television networks were required to demodulate signals that have been modulated using 64-QAM or 256-QAM. Moreover, a POSITA would have understood the relative benefits of using 64-QAM or 256-QAM versus BPSK, as 64-QAM and 256-QAM offer higher rates of spectral efficiencies than BPSK. *Id.* at 156.

8.3. Radio Receivers or Tuners for Cable and Satellite Television Networks

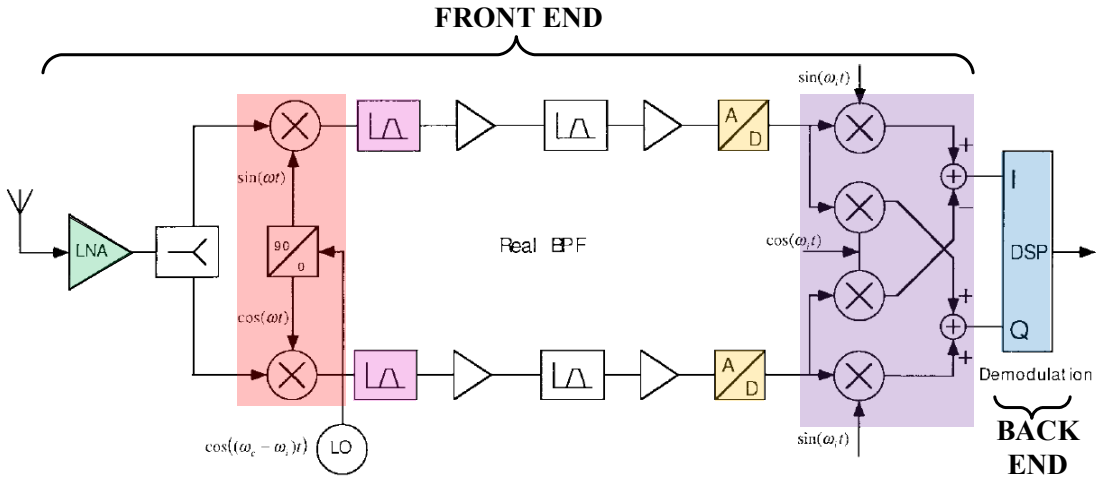
60. As discussed in Section 8.1, it was well-known to a POSITA that consumer terminal equipment (e.g., television receivers, cable set-top boxes, satellite set-top boxes, digital video recorders, personal video recorders, and other terminal equipment) receive modulated RF signals from headends and satellites. Ex. 1033 at 22, 30, 40, 352; Ex. 1035, 1:30-35; Ex. 1036, [0006]. A POSITA was also aware that consumer terminal equipment included a radio receiver (also known as a tuner) that received the RF signals and processed them in such a way that a demodulator could demodulate the RF signals to recover the digital data encoded in the RF signals. Ex. 1033 at 408-411, Fig. 22.1; Ex. 1035, 1:35-37, 1:49-52; Ex. 1036, [0018], [0020]-[0021].

61. Cable television RF receivers concurrently receive RF signals for multiple digital television channels allocated in the RF frequency spectrum of 550 to 864 MHz. Ex. 1033 at 413, 503; Ex. 1037, [0079]-[0080], Fig. 4. Satellite RF receivers concurrently receive RF signals for multiple television channels allocated in the RF frequency spectrum above 950 MHz. Ex. 1035, 1:37-47; Ex. 1037, [0080]. Furthermore, the POSITA was aware that cable and satellite television radio receivers could tune (i.e., select and extract) signals for certain desired television channels (e.g., channels selected for viewing by a consumer) from the received RF frequency spectrum. Ex. 1033 at 299; Ex. 1036, [0020]-[0021]; Ex. 1042, 4:10-36; Ex. 1044, 1:51-58.

62. One type of receiver is known as an IF (intermediate frequency) receiver, and in particular, a type of receiver known as a low-IF receiver. By the earliest claimed priority date of the ’362 patent, IF receivers, including low-IF receivers, were well-known in wireless communication systems for their high performance and low power consumption. Ex. 1025 at 270, 272; Ex. 1034 at 17, 65-74. It was also known to a POSITA, by the earliest claimed priority date of the ’362 patent, that low-IF receivers were conventionally used for receiving RF signals from cable television networks and satellite television networks. Ex. 1035, 1:49-61; Ex. 1038, [0022]-[0023], [0029]-[0030], [0042].

63. IF receivers have been used for a long time, and their way of operating is very well known. Ex. 1025 at 270. In general, IF receivers operate by initially downconverting RF signals, which may comprise multiple RF sub-bands each carrying one or more separate signals, from its RF carrier frequency to an intermediate frequency (IF). *Id*. The downconverted signals can be demodulated at the IF or further downconverted to baseband before being demodulated. *Id*. at 270, 279. When a band of signals is at baseband, the low end of the band is near zero frequency in the frequency spectrum or includes zero frequency. Ex. 1015 at 4. Intermediate frequency falls below the frequency of the RF signals but above the baseband frequency. Ex. 1034 at 22. Low-IF receivers initially downconvert to an IF that is at a relatively low frequency, such as a few hundred kilohertz. Ex. 1025. at 269.

8.3.1. Architecture of Low-IF receivers



Ex. 1025, Fig. 22(a) (annotated)

64. Low-IF receivers (illustrated by Figure 22(a) of Ex. 1025, reproduced and annotated above) comprise two main portions: a front end that performs frequency downconversion of the RF signals, and a back end including a digital signal processor (DSP) that performs the actual demodulation of the RF signals. Ex. 1034 at 22-23. The demodulation technique that will be used in the DSP depends on the modulation technique used to modulate the incoming RF signals, and therefore, if the incoming RF signals are modulated using QPSK or QAM techniques (which modulate I and Q components), then demodulation is typically performed to extract the I and Q components of the incoming RF signals. *Id.* at 23. DSPs typically perform demodulation on baseband signals. *Id.*; Ex. 1039 at 11; Ex. 1025 at 269, 279. However, the received RF signals are at much higher (non-baseband) frequencies. *Id.* Therefore, the front end must produce baseband quadrature I and Q components of the incoming RF signals to be usable by the DSP. Ex. 1034 at 23.

65. Still referring to Figure 22(a) of Ex. 1025 (reproduced and annotated above), in the front end of a low-IF receiver, the incoming RF signals are first amplified by a front-end low noise amplifier (LNA) (**green**) to provide enough gain to boost the received RF signal levels to an acceptable level such that further signal processing can be performed on the received RF signals; the LNA compensates for the attenuations of the RF signals during the transmission of the RF signals from another device. Ex. 1034 at 41; Ex. 1039 at 16. The RF signals are downconverted

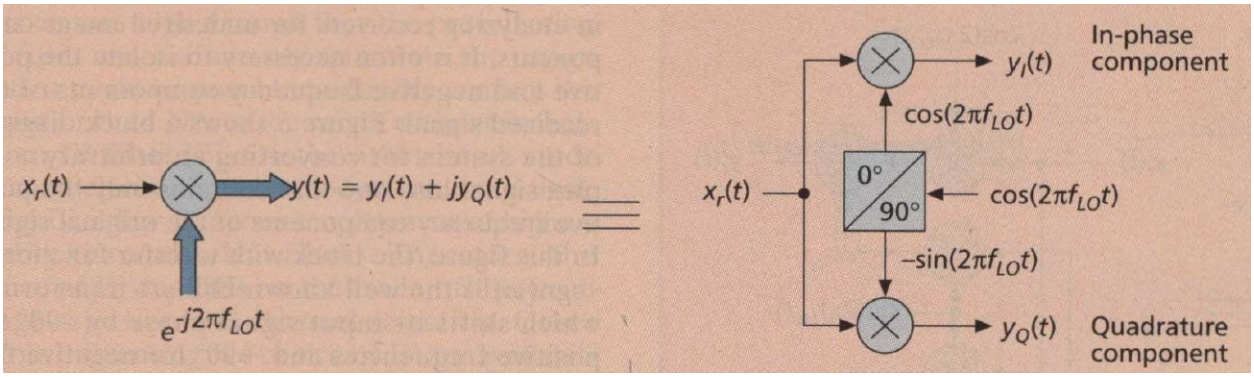
to baseband signals in two steps, where the first step (**red**) converts the RF signals to Intermediate Frequency (IF) signals before one or more analog-to-digital converters (ADCs) (**gold**) convert IF signals to digital signals, and the second step (**purple**) converts the digital signals of IF to baseband signals. Ex. 1025 at 270, 272; Ex. 1034 at 23.

66. In the first downconversion step, from RF to IF, the incoming RF signals are split and then down-converted by a quadrature downconverter (**red**), also referred to as a complex mixer or complex multiplier, which comprises two real mixers to produce I and Q components of the signals in IF. Ex. 1034 at 65-72. ; Ex. 1039 at 11 ("Two mixers are needed to retain both the amplitude and phase of the original modulated signal: one for the in-phase (I) and another for a quadrature (Q) baseband output."); Ex. 1018 at 133-134. For example, as explained in an an article by Shahriar Mirabbasi and Ken Martin in IEEE Communications Magazine in November 2000:

> The realization of a multiplier for mixing a real signal with a complex exponential *requires two real multipliers*, as illustrated in Fig. 2. *The real and imaginary parts of the mixer output are called the in-phase (I) and quadrature (Q) components* of the downconverted signal (since cosine and sine are in quadrature). In Fig. 2 the frequency of the complex exponential is chosen to be the same as the center

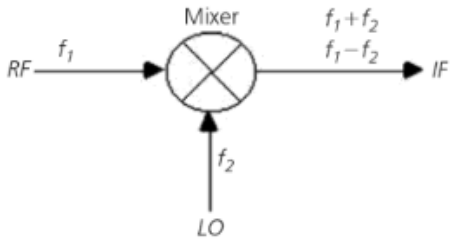
frequency of the passband signal, for comparison with case 2 in Fig. 1. In this case there is no image problem associated with the *complex mixer*.

Ex. 1018 at 134 (emphasis added).



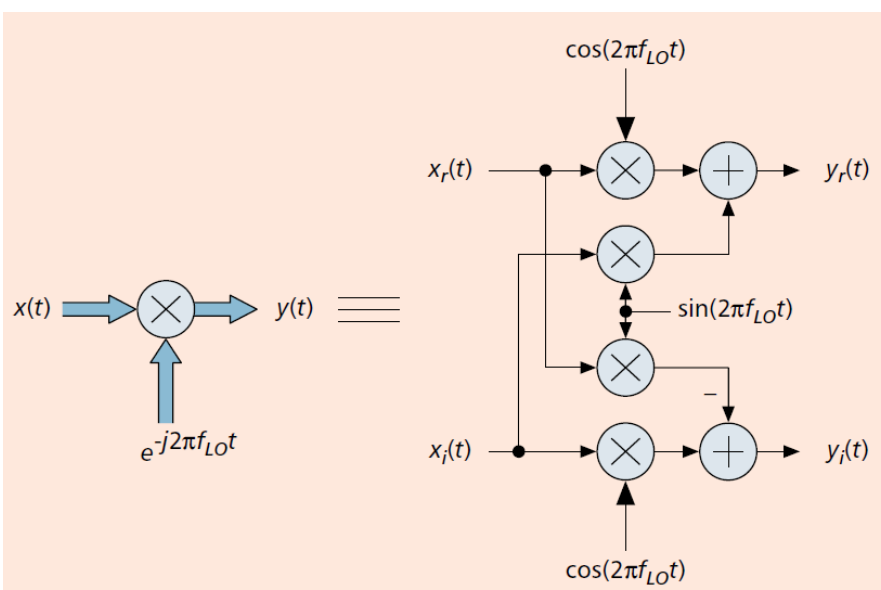
Ex. 1018, Fig. 2

The term "mixer" and "multiplier" are often used interchangeably to refer to an analog or digital electrical circuit (represented by the symbol ⊗)that multiples a modulated input signal (e.g., an RF signal) at frequency f_1 and a reference signal (e.g., from a local oscillator LO) at frequency f_2, which produces new signals at the sum and difference of the input frequencies, f_1+f_2 and f_1-f_2. Ex. 1039 at 12-13. This is illustrated in Figure 8-9 from Ex. 1039.



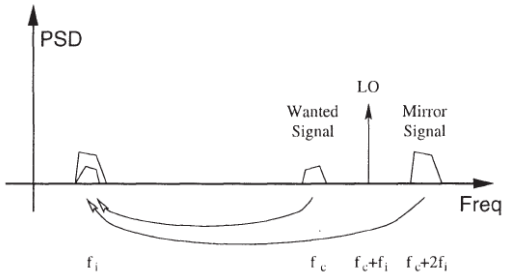
Ex. 1039, Fig. 8-9

By filtering out the signal with the sum (f_1+f_2), and passing only the signal with difference (f_1-f_2), the center frequency of the modulated input singal is reduced, or down-converted. A mixer/mulitplier is "complex," if it multiplies the input signal by a complex signal, having real and imaginary parts, to produce in-phase and quadrature signals. Ex. 1018 at 5. A complex mixer/multiplier can include two real mixers/multipliers when the input signal is real and the reference signal is complex as shown in Figure 22(a) of Ex. 1025 above, or it can include four real mixers/multipliers if both the input signal and reference signal are complex as shown below. Ex. 1018 at 5-6, Fig. 3. As shown in the figure below, the symbol ⊗ is used interchangeably to refer to a complex mixer (left) or individual real multiplier/mixers (right) that make up a complex mixer.

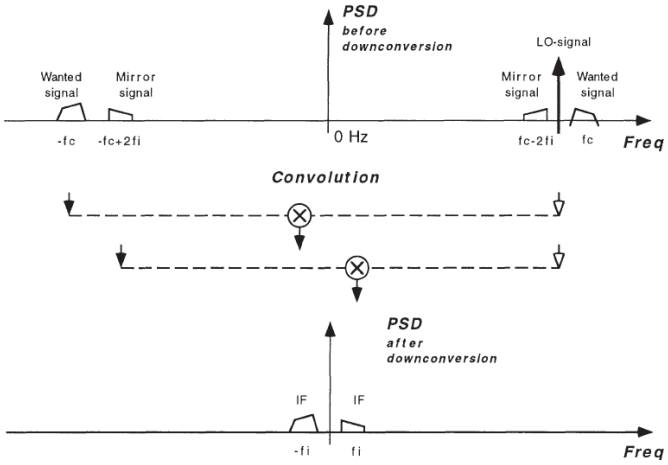


Ex. 1018, Fig. 3

Referring back to Figure 22(a) of Ex. 1025, the RF signals could also be downconverted using a single mixer and a sinusoidal signal (as shown by Figure 2.6 of Ex. 1034, reproduced below); however, the main disadvantage of mixing an RF signal of frequency fc with just a single sinusoidal signal cos(2πfit) to downconvert to intermediate frequency fi is that a second mirror signal of frequency fc+2i is also downconverted to frequency fi. Ex. 1034 at 24.



Ex. 1034, Fig. 2.6



Ex. 1034, Fig. 3.23

67. It was known that the mirror signal problem could be avoided by mixing the incoming RF signals with a complex signal, $\cos(2\pi f_i t) + j\sin(2\pi f_i t)$. Ex. 1034 at 28, 43; Ex. 1039 at 13. Mixing with such complex signals shifts a wanted RF signal at frequency f_c to frequency f_{-i} while the unwanted mirror (or image) frequency signal at f_{c+2i} is shifted to frequency f_i. *Id*. Furthermore, separately mixing the RF signals with the signal $\sin(2\pi f_i t)$ produces the I-components of the RF signals, while mixing with $\cos(2\pi f_i t)$ produces the Q-components for the RF signals, and both of these components are needed for the DSP at the back end to ultimately

demodulate the incoming RF signals. Ex. 1034 at 23. Filters (**pink**) can be used after the first stage of downconversion to filter out unwanted mirror signals. *Id*. at 28; Ex. 1039 at 17.

68. One could directly downconvert the incoming RF signal to baseband in the analog part of the RF receivers by using quadrature downconverters such that a second downconversion stage is not needed before the signals are forwarded to a demodulator; for example, zero-IF receivers perform such direct conversion. Ex. 1034 at 28; Ex. 1050 at 13-14. However, a significant problem in direct downconversion is the introduction of parasitic baseband signals at baseband, known as DC-offset, in the output of the quadrature downconverters. Ex. 1018 at 8; Ex. 1034 at 29; Ex. 1050 at 14-15. This DC-offset is mainly the result of the crosstalk between the incoming RF signals and the complex signal of the quadrature downconverters, the self-mixing phenomenon of the local oscillator producing the complex signal, the leakage of the complex signals to the input of the LNA, and/or capacitive/inductive bondings between the different components of the RF receivers. Ex. 1018 at 8; Ex. 1034 at 29, 55-62; Ex. 1050 at 14-15. Such DC-offset issues are not present in low-IF receivers as the output of the first stage of mixing is at IF and not at baseband, and the downconversion at the second step is digitally performed. Ex. 1018 at 9-10; Ex. 1034 at 18. Furthermore, in the analog part of the RF receivers, mismatches between the two components of the complex signal and differences

along the two branches of quadrature mixers and any following amplifiers and filters can cause the corruption of the I/Q components of the downconverted signals. Ex. 1018 at 10; Ex. 1034 at 29, 42, 55. However, such mismatches are not an issue in the second digital downconversion step. Ex. 1018 at 9; Ex. 1034 at 74, 76.

69. Analog-to-digital converters (ADCs) (**gold**) were commonly used in RF receivers for either IF or baseband signal sampling. Ex. 1039 at 18. Therefore, referring again to Figure 22(a) of Ex. 1025 (reproduced and annotated above), the quadrature downconverter (**red**) downconverts the incoming RF signals to produce I and Q components in IF before two ADCs separately digitize the IF I and Q components. Ex. 1034 at 42. The digitized I and Q components are further downconverted to baseband by a digital complex mixer (**purple**) (comprising four digital mixers represented by the symbol ⊗ and two summers) before being forwarded to the DSP (**blue**).

8.3.2. Channel Selection based on Digital Filters

70. RF receivers receive RF signals for multiple television channels from cable and satellite television networks. Ex. 1035, 1:37-47. An important function for RF receivers is the ability to tune or filter out the signals for a desired television channel from the received RF signals such that only the signals of the desired television channels are demodulated. Ex. 1033 at 510. A POSITA would have known that digital filters based on digital signal processing are far superior to

analog filters as digital filters do not suffer from manufacturing variations or aging, are easily programmable and tunable, have low power consumption, are unaffected by environmental influences, and have a superior performance-to-cost ratio. Ex. 1041 at 43. Digital filters, such as low pass filters and band pass filters, were known to select signals of desired television channels in RF receivers. Ex. 1035, 11:13-23, Fig. 7A; Ex. 1042, 6:5-8, Fig. 1B; Ex. 1043, 5:13-29, 5:46-53; Ex. 1050 at 44, 48.

- Low pass filter: A low-pass filter is a filter that passes signals with a frequency lower than a selected cutoff frequency (ω_c) and attenuates signals with frequencies higher than the cutoff frequency. Ex. 1041 at 14.

Fig. 1.23. Ideal LP filter magnitude frequency response.

Ex. 1041, Fig. 1.23

- Bandpass filter: A bandpass filter allows a specific range of frequencies (ω_1 to ω_2) to pass through while attenuating frequencies outside that range. Ex. 1041 at 21.

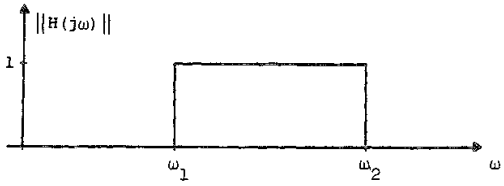


Fig. 1.27. Ideal BP filter.

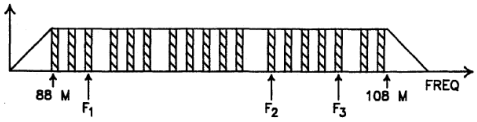
Ex. 1041, Fig. 1.27

A bandpass filter allows signals within a selected frequency range (e.g., signals for a selected television channel) to be isolated from undesired signals from outside the range. Ex. 1043, 5:13-15; Ex. 1050 at 44. Signals for a desired television channel can also be isolated from signals of undesired television channels by downconverting all the signals such that the signals for the desired television frequency are placed at baseband and then applying a low pass filter function to isolate the signals of the desired television channel. Ex. 1043, 5:46-50; Ex. 1050 at 48. However, low pass filters are preferred over bandpass filters as low pass filters require fewer computational steps and, therefore, less computational power than bandpass filters. Ex. 1050 at 33, 48-49. It was also known to a POSITA that low pass filters and bandpass filters use well-known digital architectures of Finite Impulse Response (FIR) filters. Ex. 1041 at 24-63; Ex. 1043, 5:15-17; Ex. 1050 at 44.

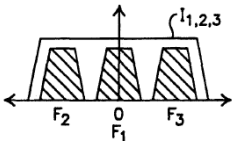
71. Some receivers may allow signals of two or more desired channels to be filtered out such that consumers may enjoy a feature called picture-in-picture, where a small window showing one of the desired television channels is inserted into a larger window showing another one of the desired television channels. Ex. 1033 at 467; Ex. 1035, 4:37-43. For example, Khoini-Poorfard (Ex. 1035) describes using two RF receivers to filter and demodulate two television channels such that

the filtered television channels can be used in the picture-in-picture feature. Ex. 1035, 4:37-43, 11:13-23, Fig. 7A.

8.3.3. Stacking of Desired Channels before Demodulation



Ex. 1044, Fig. 1



Ex. 1044, Fig. 6

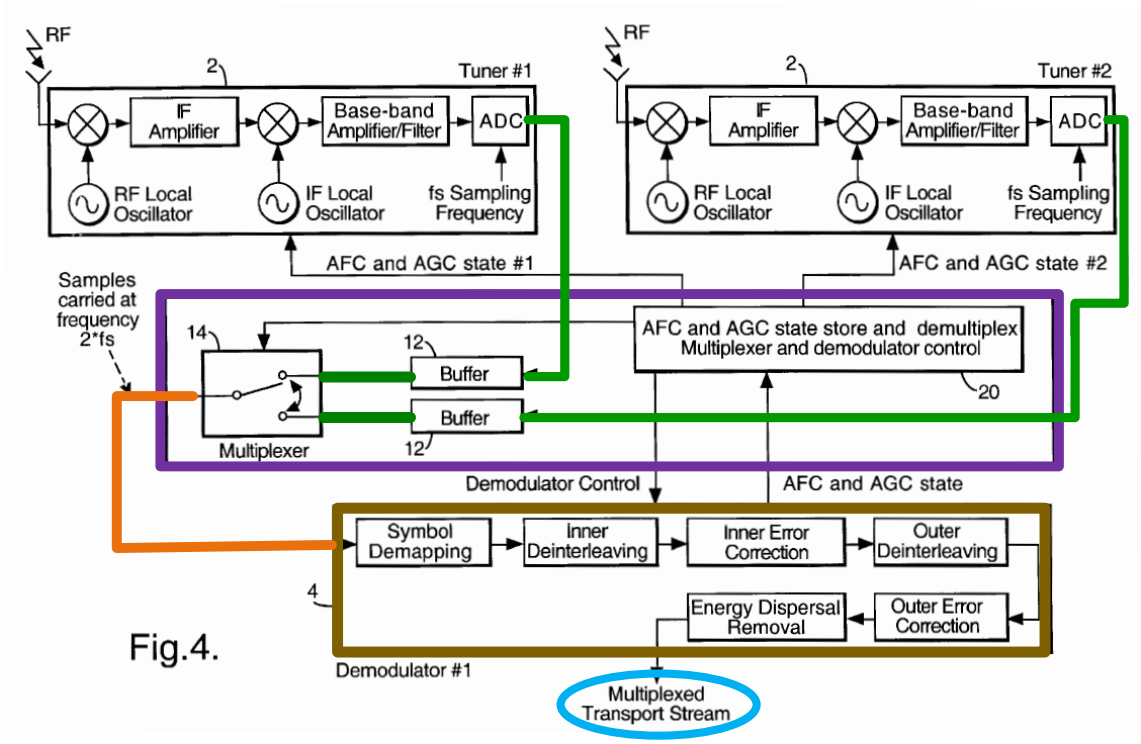
72. Khoini-Poorfard (Ex. 1035) describes using two RF receivers that individually filter and demodulate two television channels. Ex. 1035, 4:37-43, 11:13-23, Fig. 7A. Kelly (Ex. 1044) describes an RF receiver that demodulates multiple desired channel bands without expensive hardware requirements and hardware duplications. Ex. 1044, 2:42-50. The RF receiver in Kelly digitizes RF signals comprising multiple desired RF bands in an RF spectrum (e.g., bands F_1, F_2, and F_3 in Figure 1 of Ex. 1044 reproduced above) and subjects the digitized signals to multiple frequency translations such that the desired bands are adjacent to each other (e.g., bands F_1, F_2, and F_3 are adjacent to each other in Figure 6 of Ex. 1044 reproduced above). *Id*., 2:51-58, 4:38-40, 4:54-5:9. The desired frequency bands are then digitally separated, demodulated and processed to provide multiple outputs from the single receiver. *Id*. at 2:58-60.

8.3.4. Decimation

73. ADCs in RF receivers convert incoming RF signals to digital signals by sampling the RF signals at a rate that is at least twice the highest frequency of the RF signals. Ex. 1045 at 70. The reason for the high sampling rate is to prevent information loss during digitization; the Nyquist theorem specifies that a sinusoidal function in time or distance can be regenerated with no loss of information as long as it is sampled at a frequency greater than or equal to twice per cycle. *Id.*; Ex. 1033 at 98. That is, if you digitize an analog signal by sampling the signal at two or more times the highest frequency contained in the signal, that signal can be theoretically converted back to the exact same analog signal by passing the signal through a low pass filter. The Nyquist theorem is a fundamental principle that enables us to digital signal process (DSP) analog signals (radio waves, sound waves, vibrations, etc.) that exist in the real world. Ex. 1033 at 98-101. Because the sample rate of the resulting signal from an ADC may be too high for subsequent DSP processing, decimation is typically performed on the sampled signals at baseband to lower the sampling rate. Ex. 1034 at 104; Ex. 1045 at 70. Decimation is a well-known process that reduces the original sample rate of a signal to a lower rate. Ex. 1045 at 14-15. A decimation filter can be implemented in a digital signal processing block of an RF receiver after the second downconverting step. Ex. 1034 at 104; Ex. 1045, Fig. 3.57; Ex. 1046, 2:51-57.

8.3.5. Demodulation of Multiple Channels

74. A POSITA would have been well aware that either a single demodulator or multiple demodulators can perform demodulation of signals for multiple selected television channels. Ex. 1019, 1:67-2:7, 2:32-35, 2:61-63, 3:50-52; Ex. 1044, 7:53:57. For example, Carson (Ex. 1019) describes a multichannel time-shared demodulator that demodulates the signals of multiple channels concurrently using time division multiple access (TDMA) techniques. Ex. 1019, 1:67-2:7, 2:32-35, 2:61-63, 3:50-52. Another example is shown in Azenkot (Ex. 1075), which describes a single shared demodulator for demodulating multiple time-division multiplexed QAM channels in a cable modem termination system (CMTS) in a hybrid fiber-cable (HFC) network. Ex. 1057, Abstract, 1:6-14, 6:14-22, 6:30-37; 7:15-20, 32:53-33:14. As another example, Shadwell (Ex. 1076) discloses the system shown below, which receives multiple digitized downconverted channels (**green**), which are time-multiplexed together (**purple**) into a data stream (**orange**) that is output to a single demodulator (**brown**), which then provides a demodulated time-multiplexed output (**light blue**).

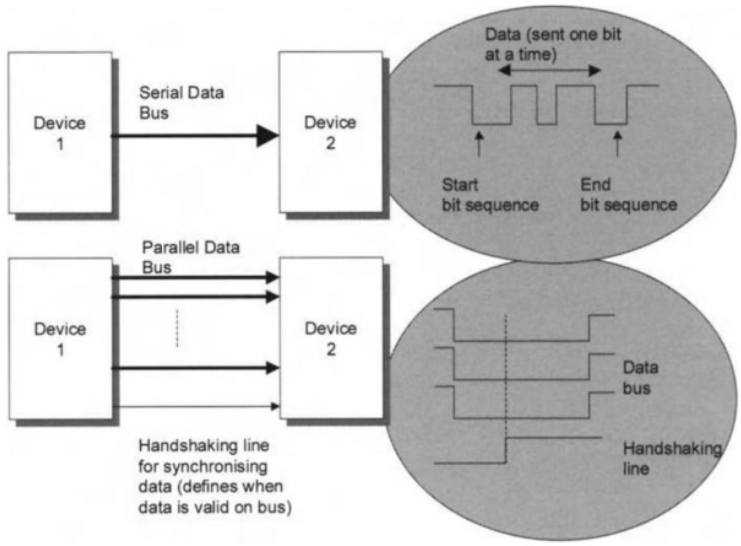


Ex. 1076, Fig. 4 (annotated).

A POSITA would have been well aware that single demodulator at the time, such as those disclosed in Carson, Azenkot, and Shadwell, or as disclosed in Zhang as further discussed below, were capable of demodulating multiple selected channels; Ex. 1076, Abstract, 2:28-52, 3:6-17, 4:21-32, 6:19-37, Figs. 1a, 1b, 2, 4. The use of a single demodulator would reduce cost of the system, and enable certain functionality, such as providing a transport stream including two demodulated television channels, for example, for decoding a picture-in-picture stream. Ex. 1076, 2:13-26, 2:53-59.

8.4. Serial vs. Parallel Data Communication

75. As described throughout subsection 8.3.1 above, the different components of an IF receiver, including a low-IF receiver, were known to a POSITA prior to the ’362 patent. It was also known to the POSITA by the earliest claimed priority date (April 17, 2009) of the ’362 patent that the different components of low-IF receivers, such as the front end and the back end, could be fabricated on the same chipset or as different chipsets, and different types of buses could later connect the chipsets. Ex. 1034 at 23, 183; Ex. 1048 at 16. Data buses were known to pass data between electronic components. Ex. 1048 at 16. The data could be either passed in a serial manner by passing one bit at a time in a single bus, or in a parallel manner where several bits are transmitted simultaneously and each along its own separate channel. *Id.*; Ex. 1049, 1:10-28.



Ex. 1048, Fig. 2.3 (page 17)

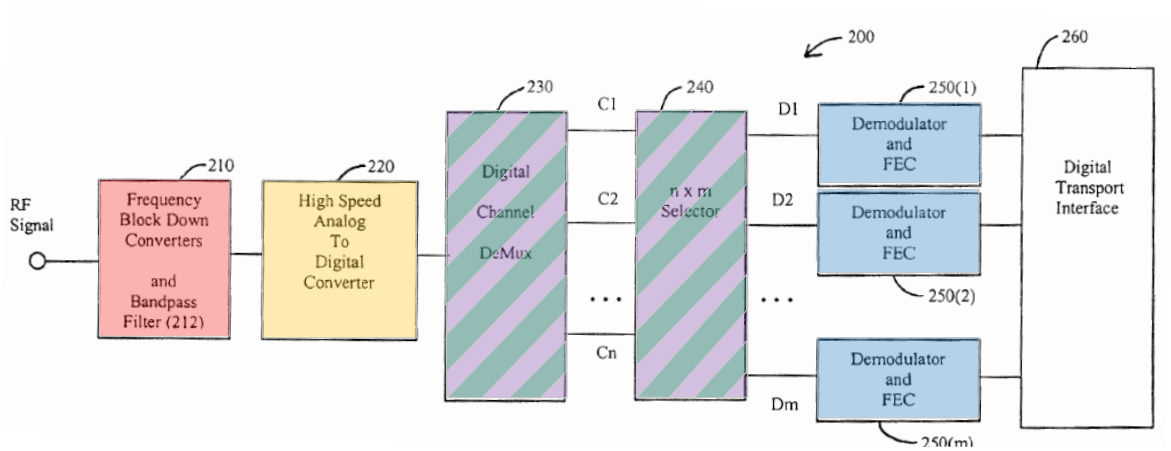
76. A POSITA would have known that data transmission using parallel data buses offers a much higher data transmission rate than data transmission using a serial data bus. Ex. 1048 at 16. However, the parallel bus structure requires a larger number of conductors and more space on the chip. Ex. 1049, 1:32-40. Furthermore, due to natural aberrations in the structure of each bus (e.g., resistance), signals in parallel data buses do not arrive at the same time, creating a problem known as "skew." *Id.* at 1:24-40. This problem becomes more severe as the distances between chipsets increase. *Id*.

77. Therefore, it was well known before the claimed priority date of the '362 patent to use technologies such as those described above in Sections 8.2-8.3 to broadcast data for television channels using QPSK and QAM modulated RF signals, and to use radio frequency receivers and tuners, such as low-IF receivers, to receive and process the RF signals to select one or more desired television channels. As also discussed above, such processing was well-known to include channel stacking, downconversion, channel selection (e.g., filtering), demodulation, and decimation, as well as parallel and serial bussing between receiver components.

8.5. U.S. Publication No. 2003/0056221 – Zhang (Ex. 1013)

78. U.S. Publication No. 2003/0056221 ("Zhang") (Ex. 1013) is a U.S. Published Application published on March 20, 2003, and thus, I understand that Zhang is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1013, cover. I also

understand that Zhang was not considered during the prosecution of the ’362 patent. Ex. 1001, cover.

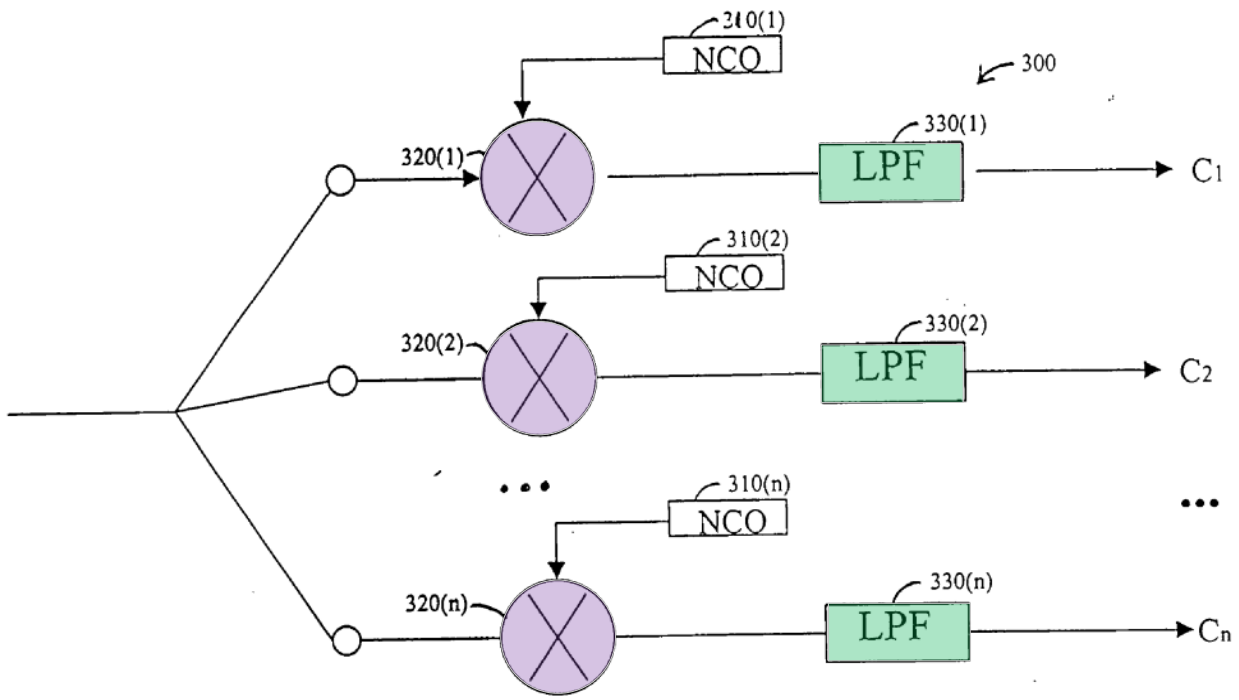


Ex. 1013, Fig. 2 (annotated)

79. Zhang describes a multi-channel demodulator circuit 200 (illustrated by Figure 2 of Zhang reproduced above) that can be used as “advanced wide-band front-ends for digital set-top boxes, PVRs, home gateways and home media centers.” Ex. 1013, [0044]-[0045], Fig. 8. The multi-channel demodulator circuit 200 receives a band of analog Radio Frequency (RF) signals comprising multiple content channels and only demodulates signals for those content channels that a subscriber has selected. Ex. 1013, [0011], [0024], [0028]-[0029], [0038]-[0040], [0042]. The Zhang multi-channel demodulator circuit comprises a frequency block down-converter 210 (**red**) that receives the band of analog RF signals and shifts the band to a lower frequency such that an analog-to-digital converter (**gold**) can better process the signal to convert the analog RF signals to digital RF signals. Ex. 1013, [0010], [0023], [0025], [0027], [0030]-[0037], [0041]-[0042]. A digital channel

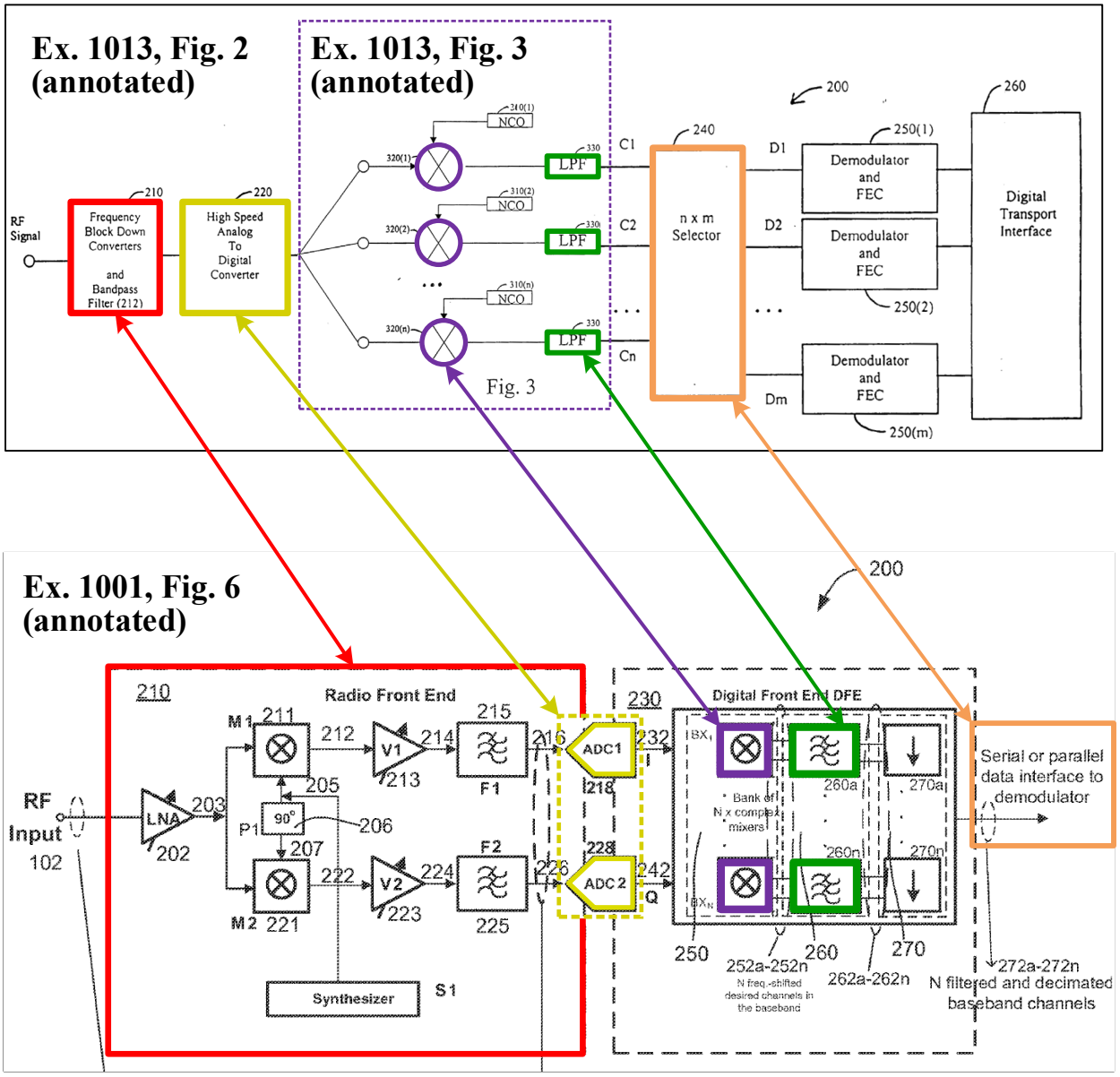
demultiplexer 230 (**green**/**purple**) then separates signals of all the content channels in the digital RF signals (e.g., channels C_1 to C_n), while a nxm digital selector 240 selects and forwards only signals for a subset of content channels selected by a subscriber (e.g., channels D_1 to D_m) to one or more of demodulators 250(1), 250(2), . . . 250(m) (**blue**), which may be "shared demodulators" with common functional blocks. Ex. 1013, [0010]-[0011], [0028]-[0029], [0042], [0047], claims 1, 4, 9, 31-32. The demodulators 250(1), 250(2), . . . 250(m) receive the signals of selected content channels and demodulate the signals and output to a digital transport interface to eventually recover audio and video data of the selected content channels. Ex. 1013, [0007].

80. Figure 3 shows additional details of the digital channel demultiplexer 230, which may include a bank of numeric control oscillators 310(1...n), complex multipliers 320(1... n) (**green**), and low-pass filters (LPFs) 330(1 . . . n) (**purple**). Ex. 1013, [0030]. The complex multipliers 320(1... n) multiply the digital RF signals with select frequencies provided by the numeric control oscillators 310(1...n), and shift the frequencies of the digital RF signals to be near baseband frequencies. Ex. 1013, [0032]. The low-pass filters (LPFs) 330(1 . . . n) enable "filtering [of] undesired RF channels and passing only the target RF channel." Ex. 1013, [0032], claim 37.



Ex. 1013, Fig. 3 (annotated)

As I show below and discuss in the following sections, Zhang discloses the same claimed system as in the '362 patent. This includes a "mixer module" (**red**) (Element [1B]/[11B]), a "wideband analog-to-digital converter (ADC) module" (**gold**) (Element [1C]/[11C]), and "digital circuitry configured to: select said plurality of desired channels" (**purple**/**green**) (Element [1D]/[11D]) and "output said selected plurality of television channels to a demodulator as a digital data stream" (**orange**) (Element [1D]/[11E]). The digital circuitry further includes finite impulse response filters (**green**) (Claims 8/18, 9/19), and serial/parallel interface in selector 240 (**orange**) (claims 2/12, 3/13).



81. It is my opinion that Zhang is in the same field of endeavor as the '362 patent, and thus is analogous art. For example, and like the '362 patent, which "relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum," Zhang relates to a system and method for "receiv[ing] a multi-channel analog RF signal." Ex. 1001, 1:15-18; Ex. 1013, [0010], Fig. 2. It is my

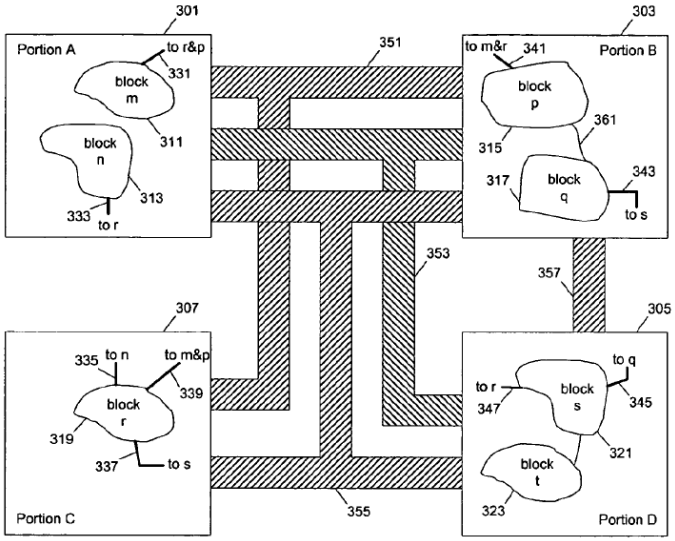
opinion that Zhang is also reasonably pertinent to problems with which the ’362 patent is concerned, and is also analogous art on that basis. For example, Zhang describes “support[ing] multiple simultaneous channels of digital content delivered over the cable system” by down-converting multi-channel analog RF signal to a multi-channel digital RF signal, conversion to baseband, and filtering in the same way as is described by the ’362 patent. Ex. 1001, 5:13-6:54, Figs. 2, 3; Ex. 1013, [0007], [0027], [0030], [0032], [0036], Figs. 2, 3.

8.6. U.S. Patent No. 7,237,214 – Pandey (Ex. 1014)

82. U.S. Patent No. 7,237,214 to Pandey (“Pandey”) indicates on its face that it was issued on June 26, 2007. Ex. 1014, cover. I understand that Pandey qualifies as prior art to the ’362 patent under pre-AIA § 102(b) because Pandey was published more than one year prior to the earliest claimed priority date (April 17, 2009) of the ’362 patent. I also understand that Pandey was not considered during prosecution of the ’362 patent. Ex. 1001, cover.

83. Pandey describes a computer aided technique for implementing a digital circuit design on a chip (e.g., field programmable gate arrays or application-specific integrated circuit). Ex. 1014, Abstract, 1:15-55; 2:4-12. The process involves partitioning functional blocks to different regions of an integrated circuit chip (e.g., 301, 303, 305, 307 as illustrated in Figure 3 of Pandey reproduced below)

and assigning wire traces (e.g., 351, 353, 355, 357) to interconnect the partitioned blocks. Ex. 1014, 1:56-60, 2:6-12, 2:64-3:5, 6:10-15; 11:6-19; 13:33-14:7.



Ex. 1014, Fig. 3

84. Pandey recognizes that the number of signals (nets) between function blocks in different partitions may exceed the number of traces (physical wires) available inside a chip, and that in such cases, multiple signals must be time-multiplexed (i.e. transmitted serially) over a single trace. Ex. 1014, 10:24-53; 10:58-11:5, 29:44-58; 30:31-42. Pandey's process optimizes the partitioning of blocks based on reducing the multiplexing ratio of wires to signals required between partitions. Ex. 1014, 5:50-53, 6:11-15; 6:44-53; 7:13-19; 29:44-30:9; 30:53-31:12; 31:56-63; Figs. 38-39. Thus, depending upon the partitioning of the circuit design within finite area and finite interconnection of a chip, Pandey's optimization will in some layouts result in signals being grouped and time multiplexed through a serial

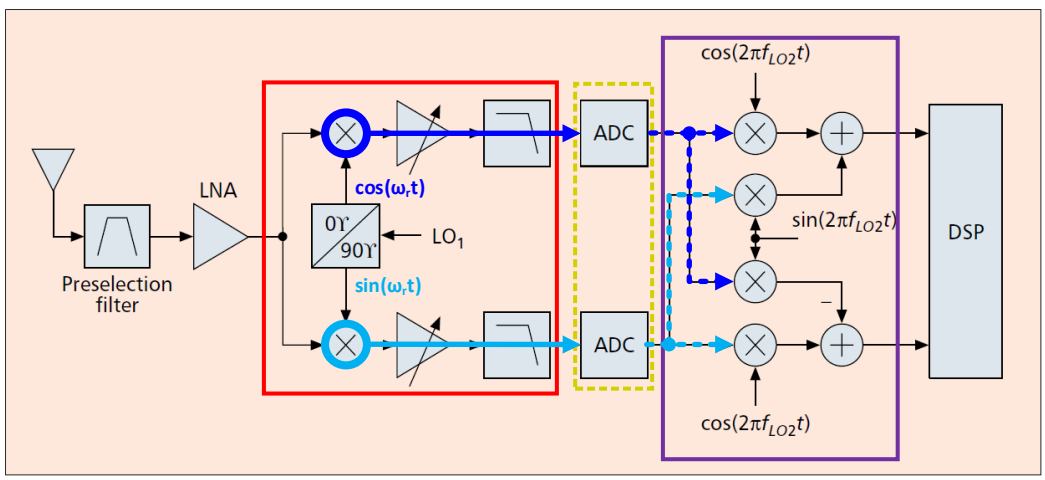
interface between partitions, and in other layouts result in signals having individual dedicated traces with no multiplexing, which is a parallel interface. Ex. 1014, 31:20-22, 32:12-15.

85. It is my opinion that Pandey is reasonably pertinent to problems with which the ’362 patent is concerned (as well as to problems with which Zhang is concerned), and is analogous art to the ’362 patent (and to Zhang) on at least that basis. The ’362 patent describes at length how signals may be processed in digital form. Ex. 1001, 5:31-6:64, Figs. 2-3. Zhang similarly includes such disclosure. Ex. 1013, [0025], [0027]-[0035], [0037]-[0039], [0042], Figs. 2-5. For example, the ’362 patent indicates that signals recovered from received RF signals may be output to a demodulator using a serial or parallel data interface, but leaves the particulars to “commonly known methods.” Ex. 1001, 6:55-58, Fig. 2. It is my opinion that a POSITA would consider Pandey, which describes both serial and parallel interfaces for groups of signals between digital functional blocks, as a pertinent example of those “commonly known method.” Ex. 1014, 11:6-19, 13:33-55; 31:20-22, 32:12-15, Figs 2-3. It is my opinion that a POSITA would similarly consider Pandey pertinent to Zhang, which describes digital circuitry configured to output the digital data stream using a single bus or multiple buses, which is functionally the same as the circuitry described in Pandey. Ex. 1013, [0038], [0039].

8.7. Mirabbasi (Ex. 1018)

86. Mirabbasi (Ex. 1018) is a Non-Patent Literature published on November 2000, and thus, I understand Mirabbasi is prior art under pre-AIA 35 U.S.C. 102(b). I also understand that Mirabbasi was not considered during the prosecution of the '362 patent. Ex. 1001, cover.

87. Mirabbasi discusses the advantages of using complex mixing (e.g., mixing RF signals with a complex exponential $\cos(2\pi f_{LO}t) - j\sin(2\pi f_{LO}t)$) instead of real mixing (e.g., multiplying RF signals with a sinusoid such as $\cos(2\pi f_{LO}t)$) when frequency shifting RF signals to a lower frequency to avoid image band problems associated with real mixing. Ex. 1018 at 5.



Ex. 1018, Fig. 10 (annotated)

88. Figure 10 of Mirabbasi shows an example of a well-known RF receiver architecture that is disclosed in the '362 patent (and in Zhang) where signals are down converted (i.e., frequency shifted to a lower frequency) through two mixing

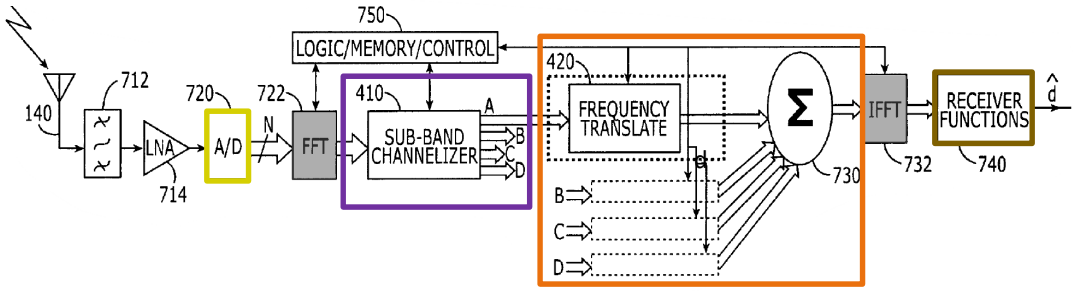
stages. Ex. 1018 at 10. The first mixing stage mixes an analog signal with a complex exponential via a complex mixing circuit of two mixers (dark blue and light blue). Ex. 1018 at 6, 10. The real and imaginary outputs of the first mixing stage are called the in-phase (I) and quadrature (Q) components of the frequency shifted signal (since cosine and sine are in quadrature). Ex. 1018 at 6. The in-phase (I) and quadrature (Q) components of the frequency shifted signal are digitized individually by two analog-to-digital converters (gold). Ex. 1018 at 10. The second mixing stage (**purple**) involves a complex mixing circuit with four mixers and two adders and further down converts the in-digital phase (I) and quadrature (Q) components before forwarding the components to the digital signal processor (DSP). Ex. 1018 at 6, 10.

89. It is my opinion that Mirabbasi is in the same field of endeavor as the ’362 patent, and thus is analogous art. For example, and like the ’362 patent, which “relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum,” Mirabbasi relates to “wireless receiver architectures used in wideband wireless communication systems.” Ex. 1001, 1:15-18; Ex. 1018, 4. It is my opinion that Mirabbasi is also reasonably pertinent to problems with which the ’362 patent and Zhang are concerned, and is analogous art to the ’362 patent (and to Zhang) on at least that basis. For example, the ’362 patent describes generating downconverted I and Q components of a received RF signal in the analog domain

and digitizing those signals using an analog-to-digital converter. Ex. 1001, 4:16-6:58, Figs. 2-3. Mirabbasi similarly describes that the I and Q components of the frequency shifted signal are digitized individually by analog-to-digital converters. Ex. 1018 at 10. It is my opinion that a POSITA would similarly consider Mirabbasi pertinent to Zhang, which also describes a frequency block down-converter that receives a band of analog RF signals and shifts the band to a lower frequency such that an analog-to-digital converter can better process the signal to convert the analog RF signals to digital RF signals. Ex. 1013, [0010], [0023], [0025], [0027], [0030]-[0037], [0041]-[0042].

8.8. U.S. Publication No. 2006/0233147 – Karabinis (Ex. 1020)

90. Karabinis (U.S. Pub. No. 2006/0233147, Ex. 1020) is a U.S. Published Application published on October 19, 2006, and thus I understand Karabinis is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1020, cover. I understand Karabinis was not considered during the prosecution of the ’362 patent. Ex. 1001, cover.



Ex. 1020, Fig. 7 (annotated)

91. Karabinis describes a receiver, for example, as shown in Figure 7 configured to receive non-contiguous frequency bands and selectively frequency shift the frequency bands to form a contiguous frequency band. Ex. 1020, [0017], [0042]. The receiver comprises an analog-to-digital converter 720 (gold) and a Fast Fourier Transformer 722 (grey) that act as a digital (discrete-time) time-domain to frequency-domain converter. Ex. 1020, [0015], [0047]. A sub-band channelizer 410 (purple) is configured to isolate the non-contiguous frequency bands, and the frequency translator 420 (orange) is configured to translate the isolated bands into one contiguous frequency band. Ex. 1020, [0017], [0049]. An Inverse Fast Fourier Transformer 732 (grey) is configured to convert the contiguous frequency band back into the time domain. Ex. 1020, [0018], [0049]. The receiver functions 740 (brown) includes a demodulator 430 configured to demodulate the contiguous frequency band. Ex. 1020, [0017], [0043], [0049], Figs. 1, 5.

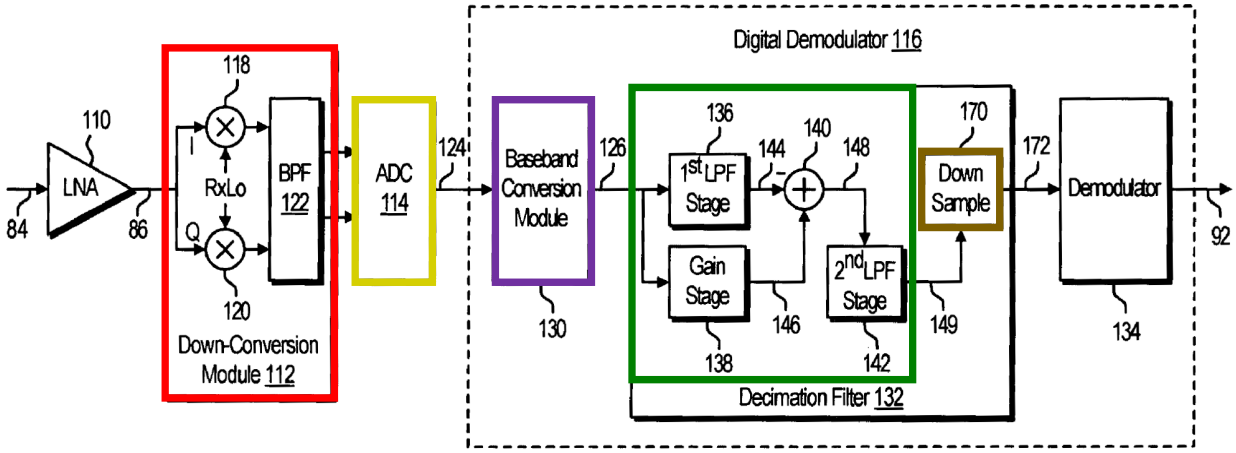
92. It is my opinion that Karabinis is in the same field of endeavor as the ’362 patent, and thus is analogous art. For example, and like the ’362 patent, which “relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum,” Karabinis relates to a “receiver [] configured to receive and selectively frequency shift portions of broadband information from multiple non-contiguous narrowband frequency bands/segments.” Ex. 1001, 1:15-18; Ex. 1020,

Abstract. It is my opinion that Karabinis is also reasonably pertinent to problems with which the ’362 is concerned (as well as to problems with which Zhang is concerned), and is analogous art to the ’362 patent (and to Zhang) on at least that basis. For example, the ’362 patent describes that “the receiver system may have to concurrently receive several desired channels that may or may not be contiguous” and “grouping them into a contiguous, or substantially-contiguous, frequency spectrum.” Ex. 1001, 1:22-23; 1:39-41, Fig. 1. Karabinis similarly describes a receiver configured to receive non-contiguous frequency bands and selectively frequency shift the frequency bands to form a contiguous frequency band. Ex. 1020, [0017], [0042]. I understand a POSITA would similarly consider Karabinis pertinent to Zhang, which also describes a frequency block down-converter that receives a band of analog RF signals and shifts the band to a lower frequency such that an analog-to-digital converter can better process the signal to convert the analog RF signals to digital RF signals. Ex. 1013, [0010], [0023], [0025], [0027], [0030]-[0037], [0041]-[0042].

8.9. U.S. Publication No. 2007/0027943 – Jensen (Ex. 1026)

93. Jensen (U.S. Pub. No. 2007/0027943, Ex. 1026) is a U.S. Published Application published on February 1, 2007. Thus, I understand that Jensen is prior art under pre-AIA 35 U.S.C. 102(b). Ex. 1026, cover. It is my understanding that

Jensen was not considered during the prosecution of the ’362 patent. Ex. 1001, cover.



Ex. 1026, Fig. 1 (annotated)

94. Jensen describes a radio receiver (illustrated in Jensen Figure 1 reproduced above) that comprises a down-conversion module 112 (**red**), an analog to digital converter 114 (**gold**), a baseband conversion module 130, a decimation filter 132, and a demodulator 134. Ex. 1026, [0024]-[0026]. The down-conversion module 112 includes mixers 118 and 120 that mix the inbound RF signals 86 with in-phase (I) and quadrature (Q) components of a receiver local oscillator to produce in-phase intermediate frequency (IF) mixed signals and quadrature IF mixed signals. Ex. 1026, [0024]-[0025]. The analog-to-digital converter 114 converts the in-phase IF mixed signals and quadrature IF mixed signals to digital IF signals 124. Ex. 1026, [0025]. The baseband conversion module 130 converts the digital IF signals 124 into digital baseband signals 126. Ex. 1026, [0026]-[0027]. The channel-select

decimation filter 132 includes a first low pass filter stage 136, a gain stage 138, a subtraction module 140, and a second low pass filter stage 138, which in combination (**green**) filters channel-selected signals 149 from the digital baseband signals 126. Ex. 1026, [0026]-[0027]. The first low pass filter stage 136 and the second low pass filter stage 142 are implemented with finite impulse response filters. Ex. 1026, [0007], [0029]. The down-sampling module 170 (**brown**) reduces the sampling rate (also known as decimation) of the channel-select signals 149 to produce down-sampled signals 172. Ex. 1026, [0027]. The demodulator 134 converts the down-sampled signals 172 into inbound digital symbols 92. Ex. 1026, [0027].

95. It is my opinion that Jensen is reasonably pertinent to problems with which the '362 patent is concerned (as well as to problems with which Zhang is concerned), and is analogous art to the '362 patent (and to Zhang) on that basis. *Netflix, Inc. v. DivX, LLC*, 80 F.4th at 1358. For example, the '362 patent describes generating downconverted I and Q components of a received RF signal in the analog domain, digitizing those signals, baseband converting those signals, and then filtering and decimating the baseband-converted digital signals. Ex. 1001, 4:16-6:58, Figs. 2-3. Zhang similarly describes receiving a band of analog RF signals, shifting the band to a lower frequency, converting the analog RF signals to digital

RF signals, conversion to baseband, and filtering the baseband-converted digital signals. Ex. 1013, [0010], [0023], [0025], [0027], [0030]-[0037], [0041]-[0042].

9. OPINIONS WITH RESPECT TO THE '362 PATENT

9.1. Zhang Anticipates (Ground A) and Renders Obvious (Ground B) Claims 1, 2, 3, 8, 9, 11-13, 18, and 19 .

96. In the following, I provide an element-by-element analysis showing how Zhang anticipates claims 1, 2, 3, 8, 9, 11-13, 18, and 19. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.1.1. Independent Claim 1

97. The elements of claim 1 appear in the Claims Listing Appendix, labeled as elements [1A]-[1D]. For the following reasons, it is my opinion that claim 1 is anticipated by Zhang.

a. [1A]: "A wideband receiver system comprising:"

98. It is my opinion that Zhang discloses "[a] wideband receiver system comprising:" as claimed.

99. It is my opinion that Zhang teaches this element. It is my opinion that Zhang's "wide-band receiver" is the same as or substantially similar to the "wideband receiver system" claimed in the '362 patent. Zhang describes "a wide-band receiver" for use in digital set-top boxes, PVRs, and home media centers. Ex.

1013, [0045]-[0047]. Specifically, Zhang describes that "[s]ystems using the invention are enabled to perform advanced wide-band front-ends for digital Set-top boxes, PVRs, home gateways and home media centers." Ex. 1013, [0045].

100. As an example of part of Zhang's system, Zhang's multi-channel demodulator 200 illustrated below in Figure 2 receives a RF signal in a frequency band that carries multiple RF channels, with each channel having data streams modulated on a carrier signal. Ex. 1013, [0023], [0024], [0041]-[0045], Figs. 2, 6-8; Ex. 1001, 1:24-27 (describing "wideband" as a band that carries multiple channels); Section 6, *supra*. Thus, it is my opinion that Zhang teaches Element [1A].

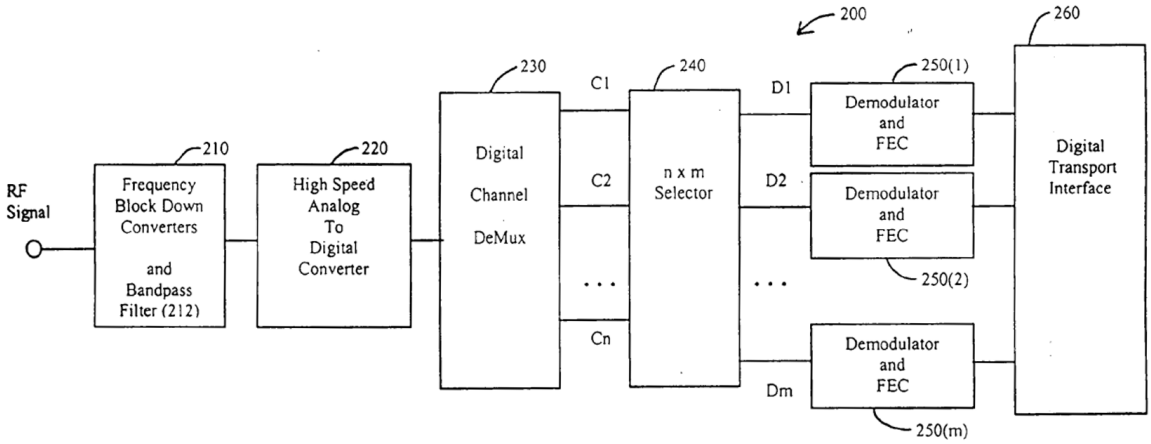


Fig. 2

Ex. 1013, Fig. 2

The RF channels received by Zhang's receiver are similar to those in '362 patent. For example, Zhang discloses 32 channels, whereas the 362 patent discloses 10. Also, Zhang discloses a frequency band of 192MHz, whereas the '362 patent discloses a frequency band of 80Mhz. In both, some of the channels are desired and

some are not desired. *Compare* Ex. 1013, ¶ [0032], [0041]-[0042], [0048], claim 34, 37 *with* Ex. 1001, 4:16-31. To the extent it is argued that Zhang's receiver is not "wideband," because it does not expressly disclose receiving desired channels in non-contiguous frequency bands, it would have been obvious to a POSITA, because as I further discuss below, Zhang does not limit the frequencies of the channels a user selects within the received frequency bandwidth, and because Zhang discloses that the desired channels "can be in different frequency bands [and] need not be contiguous." A POSITA would understand Zhang is capable of this and would be used in this manner to receive non-contiguous desired channels. *Compare* Ex. 1013, ¶ [0048] *with* Ex. 1001, 4:28-31. Since Zhang's receiver is capable of receiving any channel within the digitized frequency spectrum, a POSITA would have had a high expectation of success using Zhang's receiver for receiving non-contiguous desired channels

b. [1B]: "a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;"

101. It is my opinion that Zhang discloses "a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels," as claimed.

102. It is my opinion that Zhang discloses the claimed "mixer module," for example, as described with respect to frequency block down converter 210 (red).

Like the mixer module of the ’362 patent, Zhang’s down converter 210 multiplies (i.e., mixes) an incoming RF signal with a reference signal to downconvert the RF signal to a lower frequency band. Ex. 1013, [0025], claim 1; Ex. 1001, 4:41-46. A POSITA would have understood that a device that multiplies an RF signal by a reference signal in order to shift the frequency of the RF signal is referred to in the art as a “mixer,” and that the terms “mixer” and “multiplier” are often used interchangeably. For example, Mirabbasi, which provides a tutorial of known RF receiver architectures used for receiving digitally modulated RF signals states: “[t]ypically, frequency downconversion of a passband signal is performed by multiplying (mixing) the signal with a sinusoid such as $\cos(2\pi f_{LO}t)$”). Ex. 1018, pp. 4-5, 11, Fig. 1. The ’362 patent also uses the terms mixer and multiplier interchangeably. For example, it states that “mixers 211 and 221 multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency.” Ex. 1001, 4:42-43. It also refers to the elements in Figure 3 (circles with an “X” through them) interchangeably as four “multipliers” and also as four “digital mixers.” Ex. 1001, 6:7-27, 9:17-22. Thus, a POSITA would have understood Zhang’s Frequency Block Down Converter 210 to be a mixer module as recited in Element [1B].

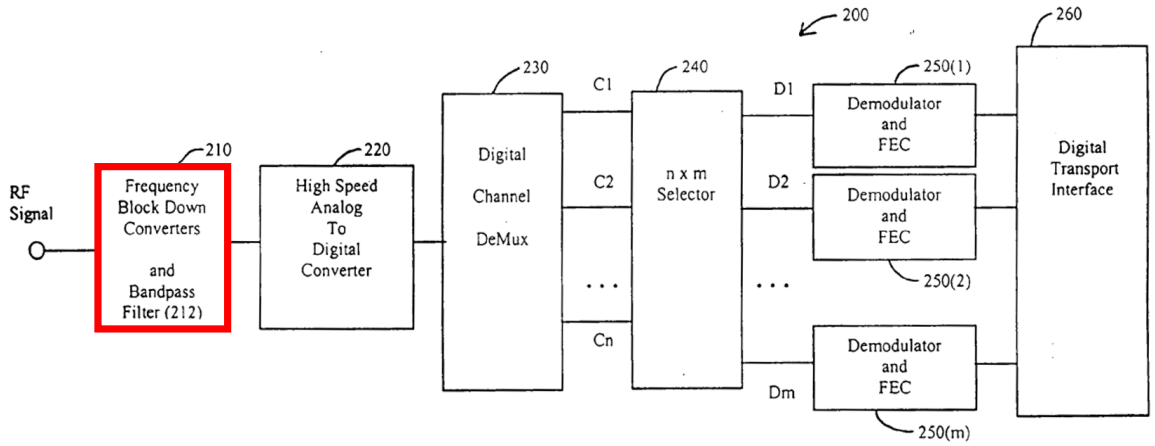


Fig. 2

Ex. 1013, Fig. 2 (annotated)

103. The RF signal includes multiple RF carrier signals that each includes one or more TV content channels from a TV system. Ex. 1013, [0005], [0023]-[0025], [0029], [0041], claims 13, 27, 28-30, 33. For example, Zhang describes that "[a] frequency-block down-converter 210 receives one or more multi-channel analog RF signals which can be sourced by a variety of systems such as satellite systems, terrestrial TV systems, cable systems, etc." Ex. 1013, [0023]. Zhang further describes that "Down converter 210 shifts the multi-channel analog RF signal to a lower frequency band." Ex. 1013, [0025].

104. To facilitate the understanding of how Zhang teaches Element [1B], I have included the following figure based on Zhang's description to illustrate how Zhang's system downconverts a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels. Based on the example described in Zhang, the figure shows a multi-channel analog RF signal between 540-750 MHz with 35 separate RF channels C1 to C35 spaced at

6 MHz intervals. Ex. 1013, [0006] ("6 MHz intervals") ("Each channel's bandwidth is less than the spacing of the carrier frequencies. For example, carrier frequencies in the UHF band (300 MHz to 3 GHz) may be spaced at 6 MHz intervals."), [0041] ("the multi-channel analog RF signal is shown to be between 540-750 MHz"), ; *see also*, Section 8.1, *supra* (citing Ex. 1033 at 45, 413, 515-520). The multi-channel analog RF signal is down converted to a lower frequency band of 20-230 MHz via Zhang's frequency block down converter 210. Ex. 1013, [0025].

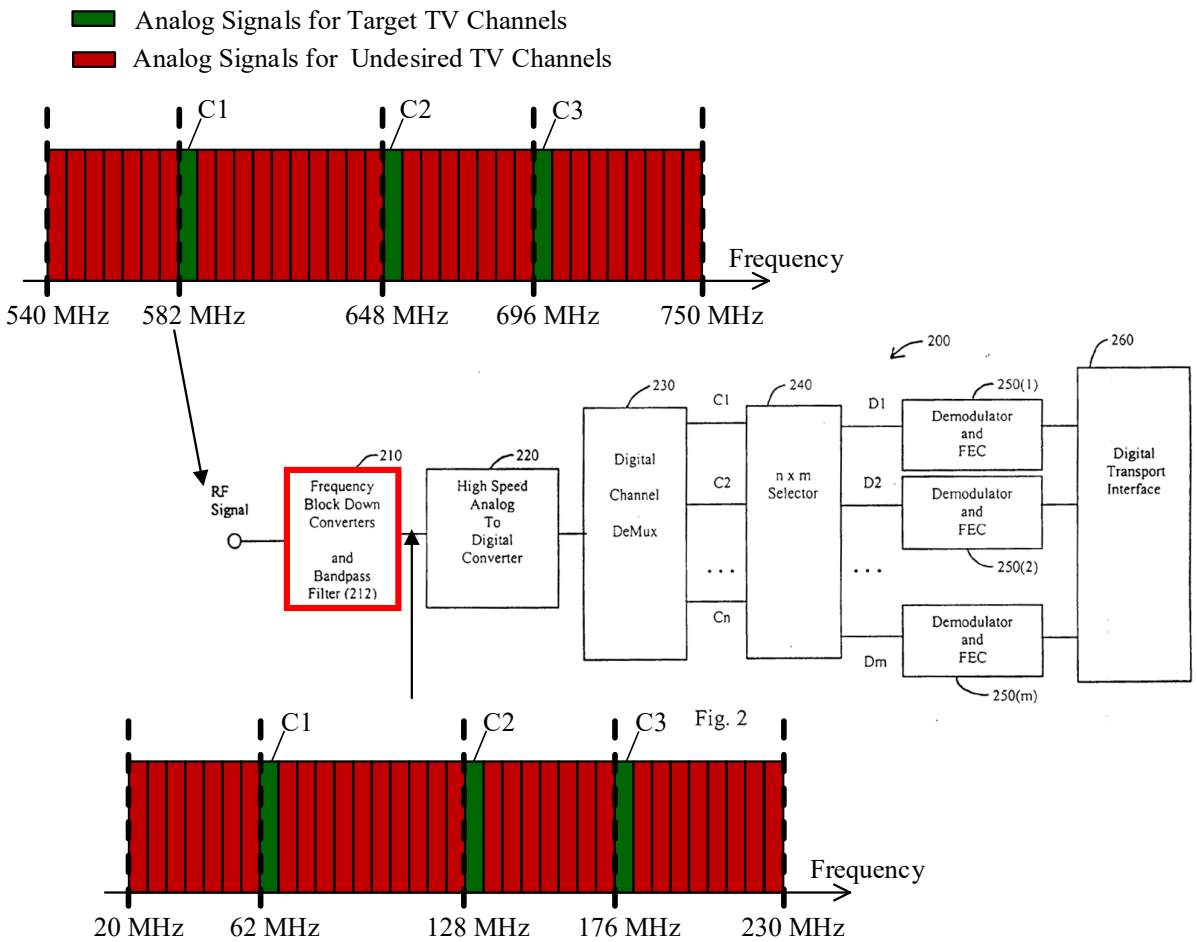


Fig. 2

105. The ’362 patent describes “desired” channels as those that are extracted from the RF input signal and sent to a demodulator and “undesired channels as those that are filtered out by the system. Ex. 1001, Abstract (The digital circuitry is configured to select the desired plurality of television channels from the digitized plurality of frequencies, and output the selected plurality of television channels to a demodulator”), 5:49-54 (“Each of the N complex mixers 250 … extract a different one of the desired channels”), 6:32-34 (“The frequency ω_{ct} is so chosen that each one of the desired channels … will be downshifted to the baseband.”); 6:55-64 ([T]he N desired baseband channels will be sent … to a demodulator…. This approach … removes undesired channels…). Just like the ’362 patent, Zhang’s multi-channel analog RF signal comprises multiple RF carrier signals that include a plurality of desired television channels selected by a subscriber (e.g., C1, C2, C3 marked in green) and a plurality of undesired television channels (marked in red) to be filtered out. Ex. 1013, [0024], [0025], [0028], [0032], claims 2, 4, 34, 36, 37.

106. Some of the RF carrier signals are “target” RF channels (the claimed “desired television channels”) and some are undesired RF channels (the claimed “undesired television channels”) which are filtered out. *Id*. The “target” RF channels may be selected by a subscriber or program provider, or pre-programmed. Ex. 1013, [0024] (“one RF channel can provide a variety of data streams, some of which are selected by a subscriber, e.g., audio, video, etc. Other data streams might be pre-

programmed or selected by a program provider, e.g., conditional access data, etc.”). Zhang further describes that a target frequency is generated to match the characteristic frequency of a desired RF channel in the multi-channel analog RF signal to select the desired RF channel. Ex. 1013, [0032], Fig. 3, claims 2, 34, 36, 37. Paragraph [0032] of Zhang is partially reproduced below.

> Numeric oscillator 310(1) generates a frequency, or “target” frequency, that matches the characteristic frequency of a desired RF channel, or “target” RF channel. The output of NCO 310(1) is multiplied by all the RF channels received at complex multiplier 320(1). When an [sic] multi-channel RF signal is multiplied with the output of NCO 310(1), the frequency of target RF channel signal is shifted to a desired channel.

107. Therefore, Zhang discloses “a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels,” as claimed. Thus, it is my opinion that Zhang teaches Element [1B] To the extent it is argued that Zhang does not disclose the claimed “mixer module,” for example, because it lacks detail as to how it performs downconverting, including a mixer module in Zhang’s down converter 210 would have been obvious, because such devices were “conventional,” as the ’362 patent admits. Ex. 1007, p. 5; Ex. 1001, 1:5-11. I describe above in Section 8.2.1 the design of a Low-IF receiver as one conventional example. Because mixer modules were “conventional,” a POSITA would have had a high expectation of success them in Zhang.

c. [1C]: "a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;"

108. It is my opinion that Zhang discloses "a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels," as claimed.

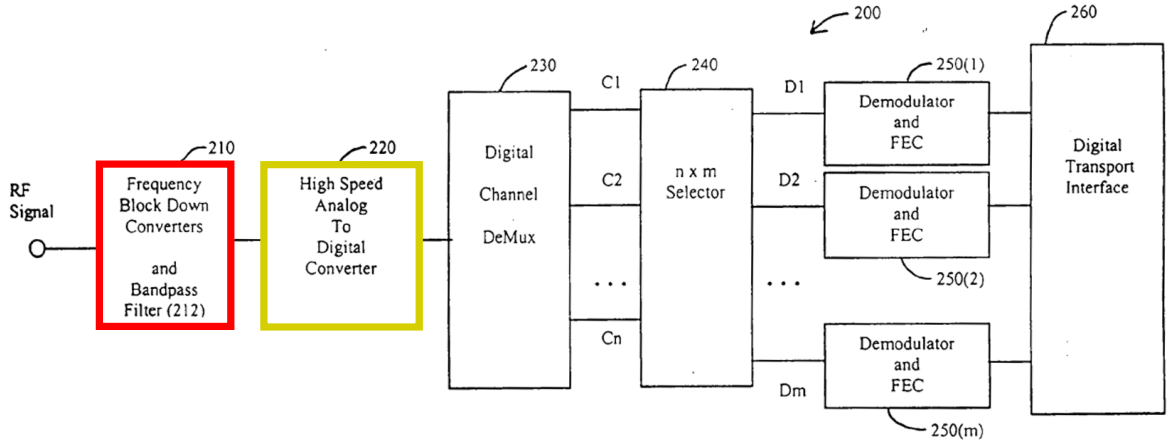


Fig. 2

Ex. 1013, Fig. 2 (annotated)

109. Zhang discloses the claimed "wideband analog-to-digital converter" as described with respect to ADC 220 (gold). ADC 220 receives the down-converted multi-channel analog RF signal including desired and undesired channels, and converts the "entire signal band" to a multi-channel digital RF signal. Ex. 1013, Abstract, [0010], [0025], [0027], [0028], [0031], [0032], [0034], [0041], [0042], claims 1, 2, 4, 7, 8, 28, 34, 36, 37. This is similar to how the '362 patent describes its wideband ADC. Ex. 1001, 4:19-25, 4:51-54, 5:19-31 (describing ADC digitizing

the down-converted RF signal at "low-IF band"). Zhang's ADC is "wideband" because it digitizes several channels within the frequency block concurrently. *Compare Ex.* 1013, [0010], [0025], [0027] *with* Ex. 1001, 1:24-27.

110. To facilitate the understanding of how Zhang teaches Element [1C], I have included the figure below based on Zhang's description to show an example of digitizing a plurality of frequencies comprising a plurality of desired television channels and a plurality of undesired television channels, as described in Zhang. As shown in the figure below, the downconverted multi-channel analog RF signal with the lower frequency band of 20-230 MHz is digitized by ADC 220 to a multi-channel digital RF signal. Ex. 1013, Abstract, [0010], [0025], [0027], [0028], [0031], [0032], [0034], [0041], [0042], claims 1, 2, 4, 7, 8, 28, 34, 36, 37. Thus, it is my opinion that Zhang teaches Element [1C]. To the extent it is argued that Zhang's ADC 220 is not wideband, for example, because it does not expressly disclose digitizing desired channels in non-contiguous frequency bands, at the very least this would have been obvious, because as further discussed below (*see* Section 9.4.1, 9.6.1), Zhang does not exclude any of the frequencies of the channels from being selected by the user within the digitized bandwidth, and because Zhang discloses that the desired channels "can be in different frequency bands [and] need not be contiguous," even if a detailed example of such is not explicitly presented. Compare Ex. 1013, ¶ [0048] with Ex. 1001, 4:28-31. Since Zhang's receiver is capable of selecting any

channel within the digitized frequency spectrum, a POSITA would have had a high expectation of success using Zhang's receiver for selecting non-contiguous desired channels.

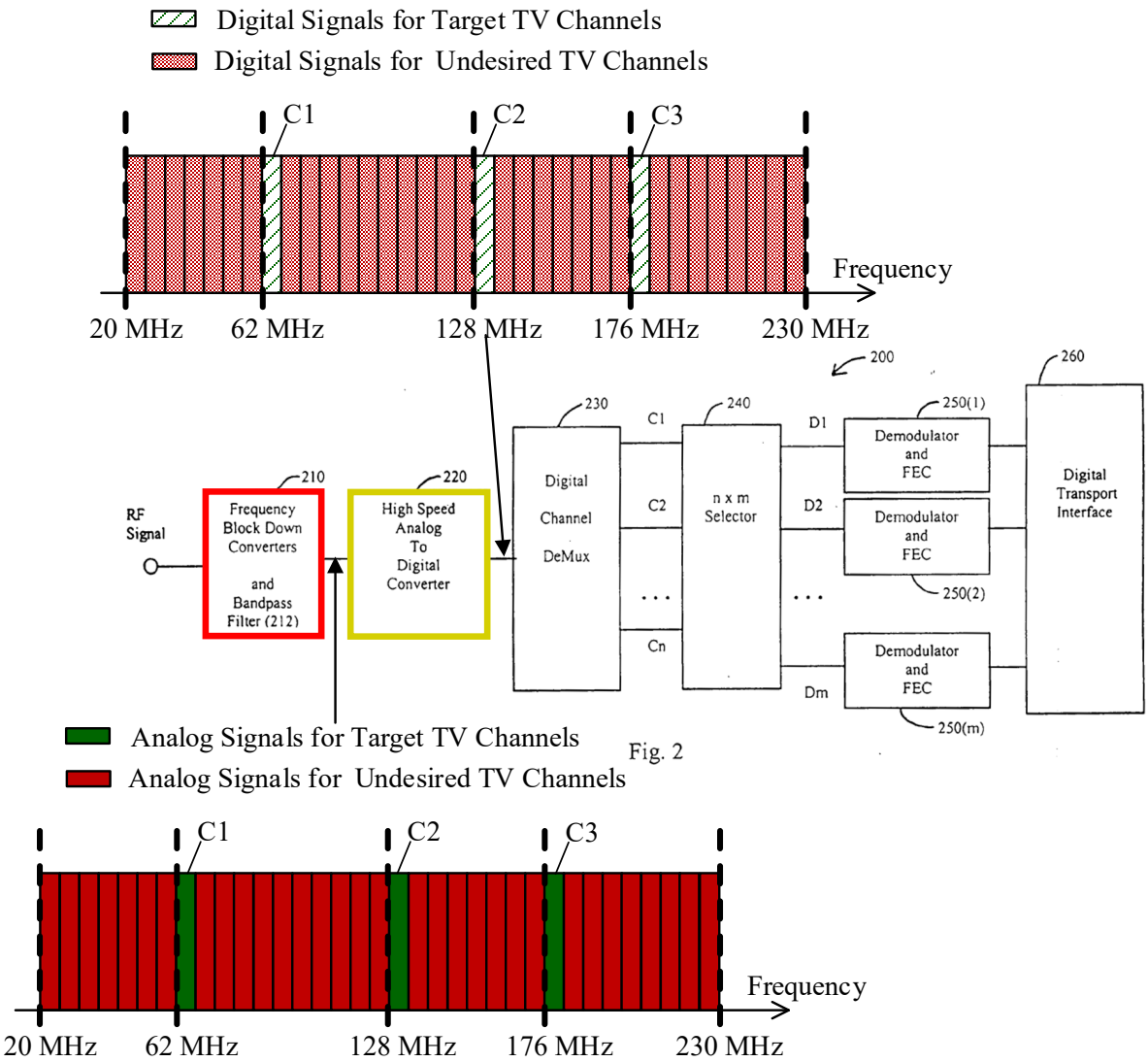
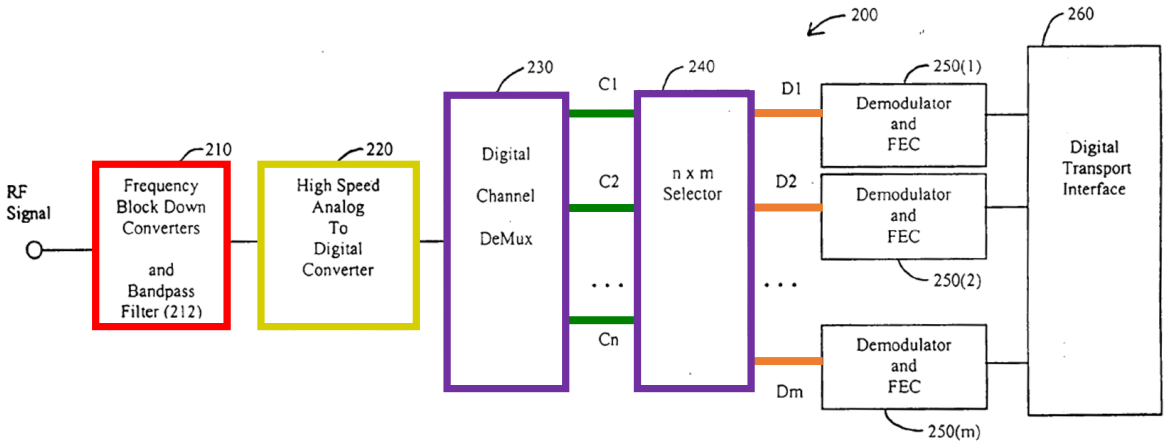


Fig. 2

d. [1D]: "digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream"

111. It is my opinion that Zhang discloses "digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies," as claimed.

112. Zhang teaches the claimed "digital circuitry" as described with respect to Digital Channel Demultiplexer 230, either alone or in combination with all or part of Digital Selector 240 (collectively purple). These components in Zhang are implemented with a "standard process CMOS," which is a well-known type of digital logic integrated circuit. Ex. 1013, [0044], [0048]; Ex. 1016, at 17-19, 53-54.



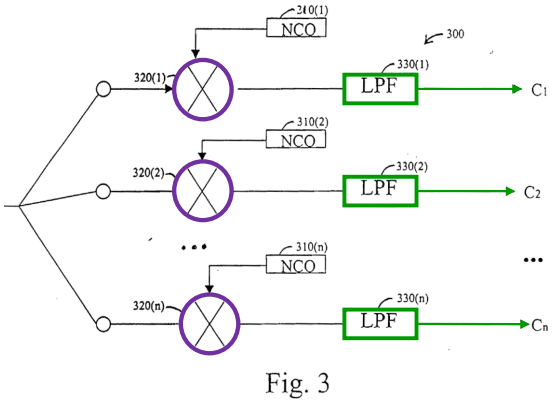
Ex. 1013, Fig. 2 (annotated)

113. Digital Channel Demultiplexer 230 (purple) receives the multi-channel digital RF signal from ADC 220 and selects from this signal a number "n" of desired

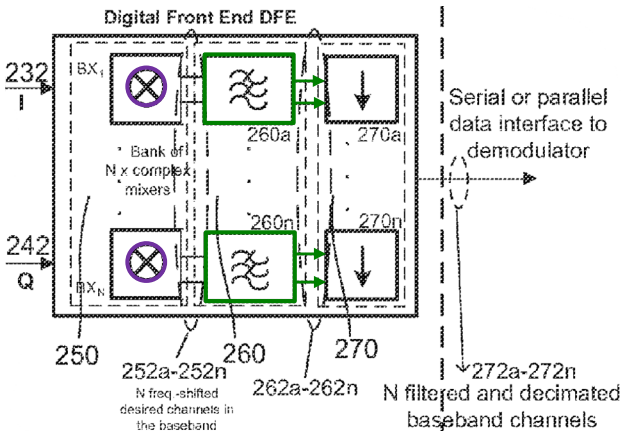
channels C_1 - C_n (green), each at a unique "target" RF frequency. Ex. 1013, [0028] ("RF channels C_1 to C_n contain content channels that are selected or used by a subscriber."), [0030-0032], [0042], claims 1, 2, 10, 11, 13, 16, 17, 21, 23, 27-28, 30, 33-34, 36-41, Figs. 2-3. Specifically, Digital Channel Demultiplexer 230 (purple) selects only the desired television channels. Ex. 1013, claim 37 ("The method of claim 34 further comprising filtering undesired RF channels and passing only the target RF channel.").

114. Zhang uses the same technique as described by the '362 patent for selecting and outputting desired channels C_1 - C_n: first using a bank of mixers (**purple**) to frequency shift a digitized version of the downconverted wideband signal so that each mixer outputs a different desired channel shifted to baseband, and then filtering out the undesired channels with a low pass filters (**green**) so that only the desired channels remain. *Compare* Ex. 1001, 2:51-55; 5:49-6:54 ("Each of the N complex mixers 250 receives the digital signals I 232 and Q 242 from ADCs 218 and 228 to extract a different one of the desired channels and frequency-shifts the extracted signals to the baseband frequency. Each of the frequency shifted desired channels 252 is filtered by an associated filter module (identified as 260 a to 260 n).") *with* Ex. 1013, [0027], [0030] ("Digital tuner 300 includes a bank of … complex multipliers 320(1 . . . n), and low-pass filters (LPFs) 330(1 . . . n). One chain of each of these elements is used for each RF channel."), [0031] ("[t]he same

multi-channel RF signal from the ADC enters each multiplier"), [0032] ("the target RF channel is shifted to a baseband, i.e., centered at DC". LPFs 330(1 . . . n) … each filters out all RF channels except for its target RF channel."); *see also* Section 9.1.3 (claims 8 and 9), *infra*.



Ex. 1013, Fig. 3 (annotated)

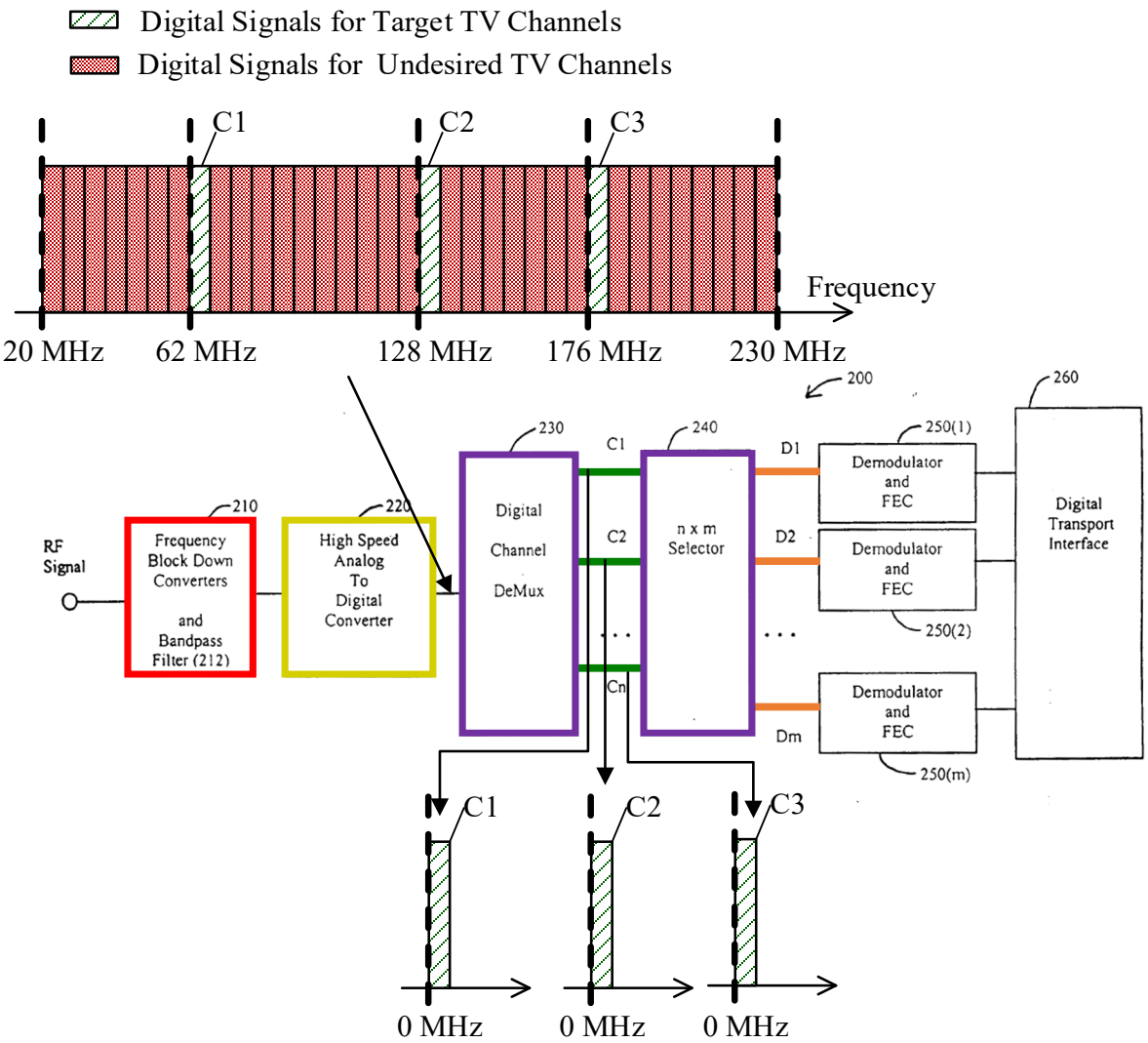


Ex. 1001, Fig. 2 (annotated)

115. To facilitate the understanding of how Zhang teaches Element [1D], I have included the following figure below to illustrate an example of selecting a plurality of desired television channels from digitized plurality of frequencies, as described in Zhang.

116. As shown in the figure below, each desired (i.e., target) channel is "shifted to a baseband, i.e., centered at DC." Ex. 1013, [0032]. As shown in Fig. 3 of Zhang and as I explain in Section 8.3.2, "LPFs 330 (1 . . . n) receive all RF channels and each filters out all RF channels except for its target RF channel." Ex.

1013, Fig. 3, [0032], claim 37. Accordingly, only the desired RF channels (e.g., C1, C2, and C3) are shifted to a baseband (e.g., 0 MHz) and selected. *Id*.



117. The desired channels are output by Digital Channel Demultiplexer 230 on paths C_1 to C_n (**green**), which a POSITA would have understood to be a serial or parallel digital data stream as described in the '362 patent, to demodulators 250(1)-250(m) via Bus Selector 240. *Compare* Ex. 1013, Figs. 2-3, [0032] *with* Ex. 1001,

6:55-58 ("N desired baseband channels will be sent as a serial or parallel digital data stream . . . according to commonly known methods, as shown in FIG. 2.").

118. Thus, it is my opinion that Digital Channel Demultiplexer 230 is digital circuitry that selects desired television channels originating in the multi-channel digital RF signal, and outputs the selected plurality of television channels to a demodulator as a digital datastream as required by Element [1D].

119. As an alternative and in addition to Demultiplexer 230 disclosing Element [1D], a POSITA would have considered a combination of Demultiplexer 230 and Digital Selector 240 as also disclosing this element. Digital Selector 240 selects channels D_1 – D_m to output as a serial or parallel digital data stream to "one or more" demodulators 250(1) – 250(m). Ex. 1013, [0028]-[0029], [0038]-[0039], [0047], claims 2-5, Fig. 3. D_1 – D_m may include all or just some of the channels C_1 – C_n. Ex. 1013, [0028] ("digital selector 240 … selects one or more of the RF channels D_1 to D_m. **from one or more** of the digital RF channels C_1 to C_n") (emphasis added). For m=n, all of the selected channels are concurrently output to one or more demodulators, and for m<n, the user may output some or all n channels to the demodulator, just not concurrently. Ex. 1013, [0028]-[0029], [0038]-[0039]. By switching through the demultiplexed channels C_1 - C_n selected by the user, Digital Selector 240 provides the subscriber with fast channel search capabilities. Ex. 1013, [0005], [0028] ("Channel-search capabilities of the digital selector 240

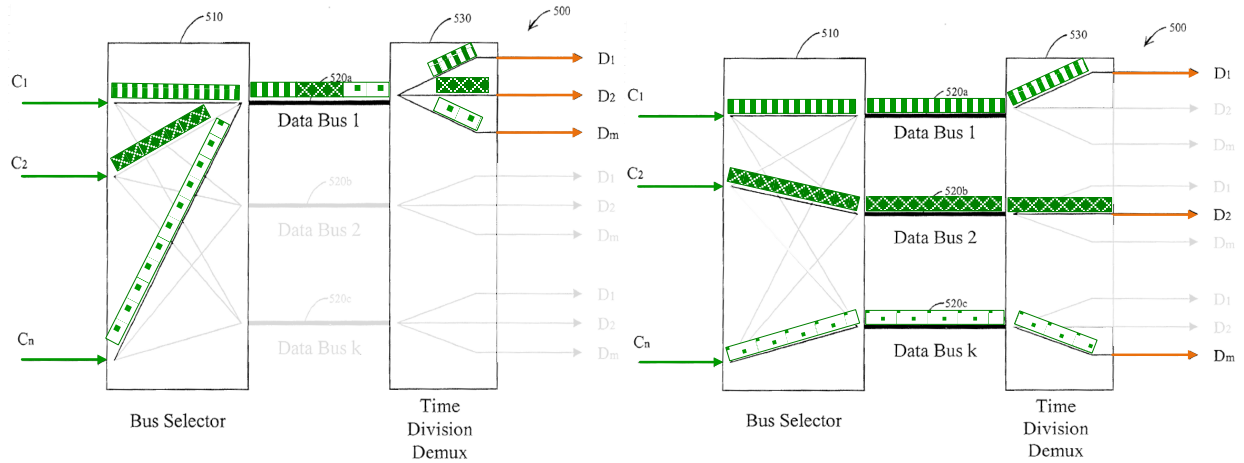
renders it much faster than traditional analog channel switching through RF tuners."), [0047], claims 3, 30.

120. Where $D_1 – D_m$ includes all C_1 - C_n, Digital Channel Demultiplexer 230 selects the desired channels and filters out the undesired channels as described above. Alternatively, a POSITA would understand that where $D_1 – D_m$ includes less than all channels C_1 - C_n, the combination of Digital Channel Demultiplexer 230 and Digital Selector 240 teaches the claimed selecting of the desired channels, in that a channel that is both demultiplexed by 230 and switched by 240 to a demodulator is "desired" and all other channels from the digital multi-channel RF signal are "undesired." Ex. 1013, [0028] ("digital selector 240 … selects one or more of the RF channels D_1 to D_m from one or more of the digital RF channels C_1 to C_n. RF channels C_1 to C_n contain content channels that are selected or used by a subscriber."), [0029] ("demodulators 250(1… m) demodulate only the RF channels that are selected by digital selector 240"). [0030], [0032]-[0033], [0040], [0042], [0048], claims 36-37.

121. Zhang's also discloses that Digital Selector 240 is configured to output the claimed "digital data stream" with its bus selector 510, which receives channels C_1 to C_n and sends the channels across one or more clocked data buses. Ex. 1013, Fig. 5, [0038], [0039]. As Zhang explains, "each bus can be used by multiple RF channels with the use of time division multiplexing . . . and each output RF signal

from a channel demultiplexer (not shown) can be selected to use any data bus." Ex. 1013, [0038].

122. Zhang's digital selector is shown annotated below (left) sending the selected channels using "time division multiplexing" (i.e., alternating data from each channel sequentially) across one bus in a serial digital data stream, and shown annotated below (right) sending the selected channels "through different data buses" in a parallel digital data stream. *Id.*; Ex. 1016, at 79-80 (Figure 6-25); *see also* Section 9.1.2 (Claims 2 and 3 parallel and serial interfaces), *infra*. These are the same methods for outputting a digital data stream that the '362 patent describes as "commonly known." Ex. 1001, 6:55-58 ("… N desired baseband channels will be sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods, as shown in FIG. 2.")

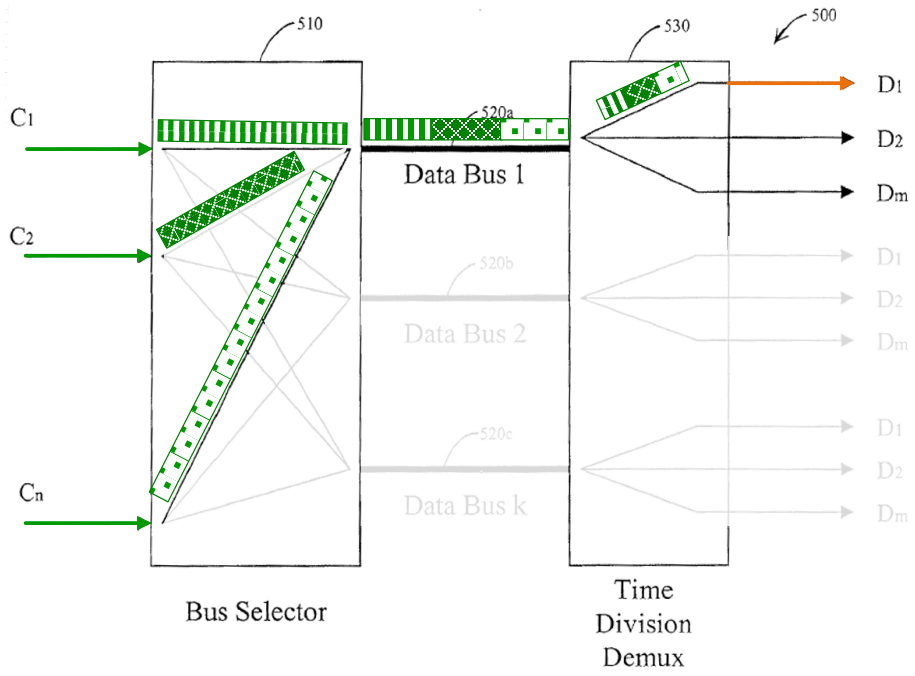


Ex. 1013, Fig. 5 (annotated)

123. From the selector, Zhang discloses that the digital RF channels in the digital data stream are received and demodulated by "one or more demodulators," and that multiple demodulators (250(1), 250(2), . . . 250(m)) may be "shared demodulators" with common functional blocks. Ex. 1013, claims 1, 2 ("one or more demodulators configured to receive one or more of the selected digital RF channels from the selector and to demodulate the one or more selected digital RF channels"), *see also* [0029], [0038], [0039], [0047], claims 4, 9, 31-32.

124. Zhang further teaches that multiple demodulators that share resources can be in a single chip. Ex. 1013, [0029] ("Many functional blocks can be shared between different demodulators ... Hence … more RF channels can be demodulated in a single chip."). This chip is similar to the device described in the '362 patent for demodulating multiple digital RF channels. Ex. 1001, 5:44-48, 5:54-60, 6:55-58, 7:66-8:9, 9:25-27. The '362 patent uses the term "demodulator" generally to refer to a device that is a single unit for demodulating a respective single channel, a device that includes multiple other devices to demodulate multiple channels, and a device that demodulates multiple channels without any specificity as to its structure. Ex. 1001, 5:44-48, 5:54-60, 6:55-58, 7:66-8:9, 9:25-27. Thus, a POSITA would have understood that either Zhang's single demodulator or Zhang's shared demodulators with common functional blocks teach the claimed "demodulator" as described in the '362 patent. Thus, it is my opinion that Zhang teaches Element [1D].

125. To the extent it is argued that Element [1D] requires the digital circuitry to output all of the desired television channels as a digital datastream to only a single separate demodulator, such as one of Zhang's demodulator 250, and that Zhang does not disclose this, having Zhang's single demodulator 250 demodulating all desired channels would have been obvious to a POSITA. Zhang explains that each bus in digital selector 240/500 "can be used by multiple RF channels" and "each data bus provides data to multiple demodulators." Ex. 1013, ¶ [0039], Fig. 5. For example, as shown below, selector 500 is capable of outputting every channel C1-Cn (green) to D1 (orange), using time-division multiplexing as discussed above and further discussed below with respect to claim 2. Ex. 1013, [0029], [0038]-[0039]. Zhang's selector 500 could also use separate buses to route each channel to D1 as discussed above and further discussed below with respect to claim 3. Ex. 1013, [0029], [0038]-[0039].



Ex. 1013, Fig. 5 (annotated)

Thus, it would have been clear to a POSITA that Zhang's system is capable of routing all desired channels in a digital data stream to a single demodulator 250. Further, a POSITA would have been well aware that single demodulators at the time, such as demodulator 250 in Zhang, were capable of demodulating multiple selected channels. *See* Section 8.3.5 above; Ex. 1076, Abstract, 2:28-52, 3:6-17, 4:21-32, 6:19-37, Figs. 1a, 1b, 2; Ex. 1019, 1:67-2:7, 2:32-41, 2:50-63, 3:50-52, Figs. 1-2; Ex. 1075, Abstract, 6:14-22, 7:15-20, 32:53-33:14. The use of a single demodulator would beneficially reduce cost of the system, and enable certain functionality, such as providing a transport stream including two demodulated television channels for picture-in-picture decoding, providing motivation to use this capability of Zhang. Ex. 1076, 2:13-26, 2:53-59. Thus, to the extent Zhang's receiver is argued to not

explicitly disclose outputting the plurality of desired channels as a digital data stream to a single demodulator 250, it would obviously do so. Such a modification would have been simply combining prior art elements (Zhang's single demodulator and Zhang's multiple desired channels) according to known methods (Zhang's routing of all desired channels to a single demodulator) to yield predictable results (demodulating multiple desired channels). Using a single demodulator to demodulate multiple channels was well within the skillset of a POSITA, leading to a high expectation of success. Thus, Zhang also renders obvious Element [1D] even under this narrow interpretation.

9.1.2. Dependent Claim 2 and 3

[2] "The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface."

[3] "The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface."

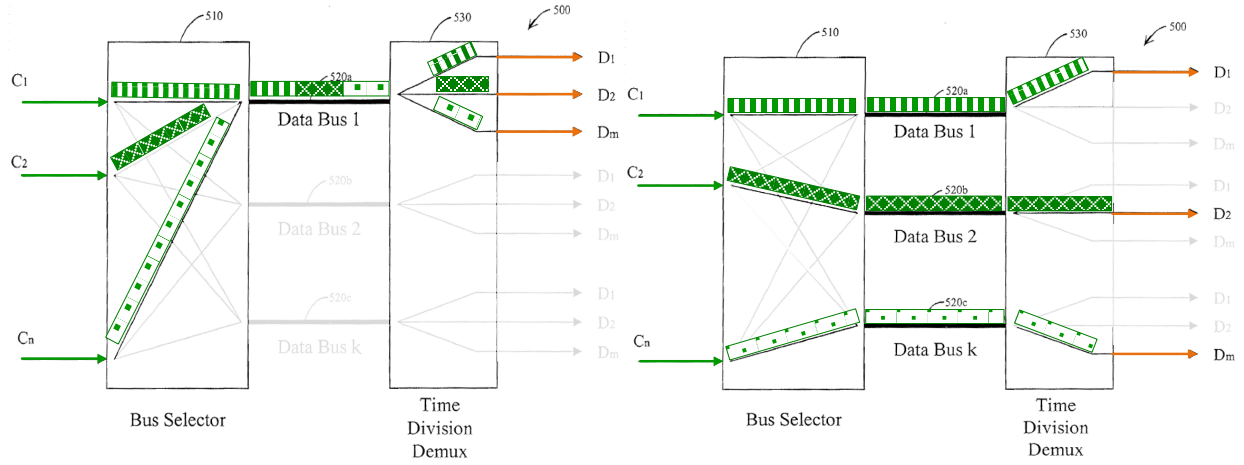
126. It is my opinion that Zhang describes "[t]he wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface," as recited in claim 2, and "[t]he wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface," as recited in claim 3.

127. Claims 2 and 3 are similar, and only differ with regard to a type of interface via which the digital datastream is output. Ex. 1001, claims 2, 3. Claim 2

recites output "via a serial interface," while claim 3 recites output "via a parallel interface." *Id*.

128. As I discuss above with respect to Element [1D] Zhang discloses a digital channel demultiplexer 230 and selector 240 that select one or more digital RF channels C_1 to C_N, and output all or a subset of these selected channels as D_1 to D_M to one or multiple shared demodulators via one or more data buses 520 in Fig. 5. Ex. 1013, [0029], [0038], [0039].

129. Zhang describes the buses being used in multiple different ways, including: A) sending the selected channels across one bus "with the use of time division multiplexing," and B) sending the selected channels "through different data buses." These two scenarios are illustrated in the annotated figures below. Ex. 1013, [0038], [0039]. As shown on the left, in the first scenario one bus (i.e., Data bus 1) receives data from each selected channel (represented by green blocks with different cross hatch patterns) and sends the data from the different channels sequentially in different time intervals (i.e., time division multiplexing). Ex. 1013, [0038], [0039]; Ex. 1016, at 79-80 (Figure 6-25). As shown on the right, in the second scenario data from each bus is sent through a separate data bus. Ex. 1013, [0038]-[0039]; Ex. 1016, at 79-80 (Figure 6-25).



Ex. 1013, Fig. 5 (annotated)

130. It is my opinion that a POSITA would have understood that Zhang's single bus using time division multiplexing on the right teaches digital circuitry configured to output the digital datastream "via a serial interface" as recited in claim 2, and that using multiple buses, one per selected channel, on the left teaches digital circuitry configured to output the digital datastream "via a parallel interface" as recited in claim 3. Ex. 1013, [0038]-[0039]. As I further explain below, this understanding is supported by basic text books and technical papers which show that these two interfaces were the standard options for outputting data in standard integrated circuit buses. Ex. 1014, 30:31-42, 31:15-22; Ex. 1016, at 17-19, 53-54; Ex. 1017, at 354-355.

131. (Reserved)

132. (Reserved)

133. For example, "Digital Integrated Circuits: A Design Perspective" published in 1996 ("Rabaey") is a textbook focused on the design of CMOS digital

integrated circuits, which is the same technology Zhang's digital circuitry is implemented in. Ex. 1016, 31-34, 48-51, 80; Ex. 1013, [0044], [0048]. As Rabaey discusses, a digital integrated circuit represents data as binary units (referred to as "bits") in the form of electrical signals on wires (e.g., high and low voltages for binary values "1" and "0" respectively). Ex. 1016, at 31-34, *see also* 48-51, 80 (Figure 6-25).

134. To output multiple bits (e.g., from multiple channels), the circuit can either transmit the bits over multiple separate wires, one wire for each bit, which was known as a "parallel interface," or the circuit can transmit the set of bits one at a time as sequential pulses over a single wire, according to a fixed sequence, which was known as a "serial interface." Ex. 1016, at 79-80 (Figure 6-25).

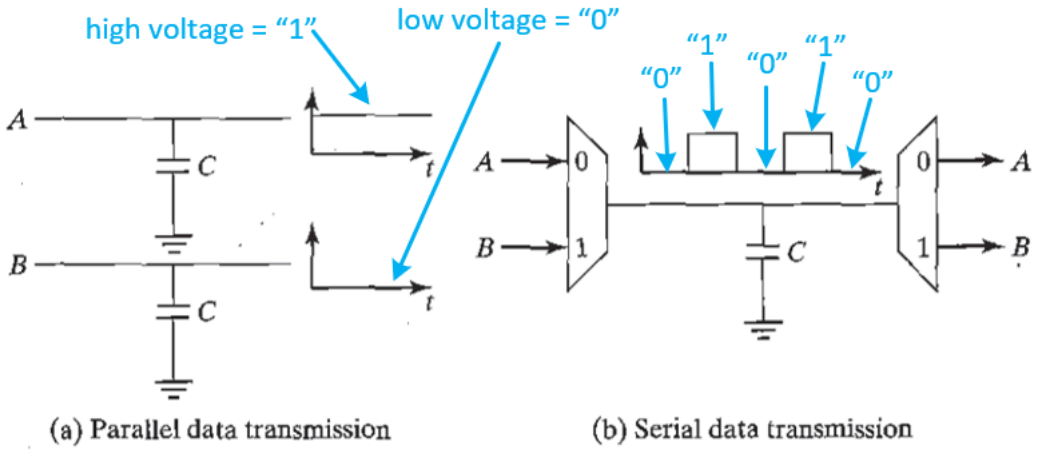


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1016, at 80 (Figure 6-25) (annotated)

135. As shown in Zhang's annotated Figure 5 above, Zhang implements serial and parallel interfaces as those terms are described in Rabaey and as were known in the art. Thus, it is my opinion that Zhang discloses claims 2 and 3.

136. To the extent Patent Owner argues that Zhang does not disclose serial and parallel interfaces, implementing Zhang's digital circuitry to output the selected channels to demodulators 250 (either to an individual demodulator or to shared demodulators) via either option would have been obvious as one of two design choices that where well known and used by POSITAs in integrated circuits designs at the time. Ex. 1014, 30:31-42, 31:15-22; Ex. 1016, at 79-80; Ex. 1017, at 354-355. Thus, a POSITA implementing the Zhang circuit, for example in CMOS, would have in the design process of implementing the output for the digital data stream chosen a serial interface and/or a parallel interface, both options being typical and thus obvious to try. As the '362 patent concedes, outputting a digital data steam via serial (claim 2) or parallel (claim 3) interfaces were "commonly known methods," i.e., Applicant Admitted Prior Art (AAPA). Ex. 1001, 6:55-58. For the same reasons, implementing serial and parallel interfaces would have been well within the POSITA's skillset, and thus, a POSITA selecting either interface would have had a high expectation of success leading to a predictable result.

9.1.3. Dependent Claim 8 and 9

[8] "The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels."

[9] "The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter."

137. It is my opinion that Zhang discloses "[t]he wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels," as recited in claim 8, and "[t]he wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter," as recited in claim 9.

138. Zhang's Demultiplexer 230, which is included in the claimed "digital circuitry" of Element [1D], comprises a plurality of finite impulse response (FIR) channel filters that, like the filter in the '362 patent, perform the claimed selection by allowing only the desired channels to pass through the system, and blocking the undesired channels. *Compare* Ex. 1013, Fig. 3 (filters 330), [0030]-[0032], claims 21-22, 37-40 *with* Ex. 1001, Fig. 2 (filters 260), 5:49-58, 6:43-54. Specifically, Zhang's Demultiplexer 300 (below left that "can be used to implement digital channel demultiplexer 230 of FIG. 2", Ex. 1013, [0030]), which is the same as the

’362 Patent’s digital front end 230 (below right), includes a signal path for each the plurality of desired channels $C_1 – C_n$, with each path including a complex multiplier 320 (purple) (also known as a complex mixer) followed by a FIR low pass filter (LPF) 330 (green). Ex. 1013, [0030] (“Digital tuner 300 includes a bank of n numeric control oscillators (NCOs) 310(1 . . . n), complex multipliers 320(1 . . . n), and low-pass filters (LPFs) 330(1 . . . n) … low-pass filters 330 are high-speed finite impulse response (FIR) filters.”).

139. Zhang explicitly discloses that the low-pass filters 330 are high-speed finite impulse response (FIR) filters. *Id*. In addition, as I explain in Section 8.3.2, it was also known to a POSITA that low pass filters and bandpass filters use well-known digital architectures of FIR filters. Ex. 1041 at 578; Ex. 1043 at 5:15-17; Section 8.3.2, *supra*.

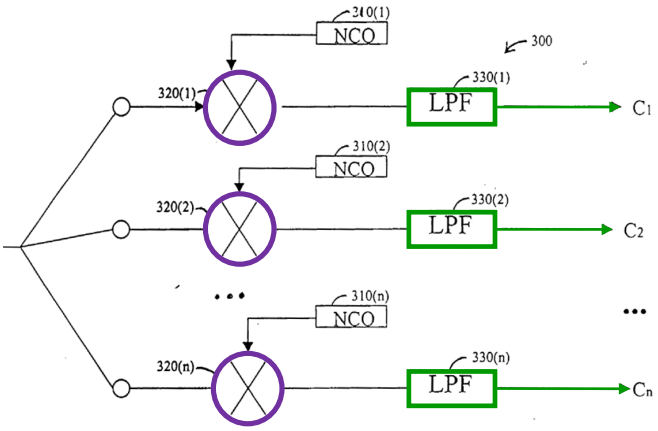
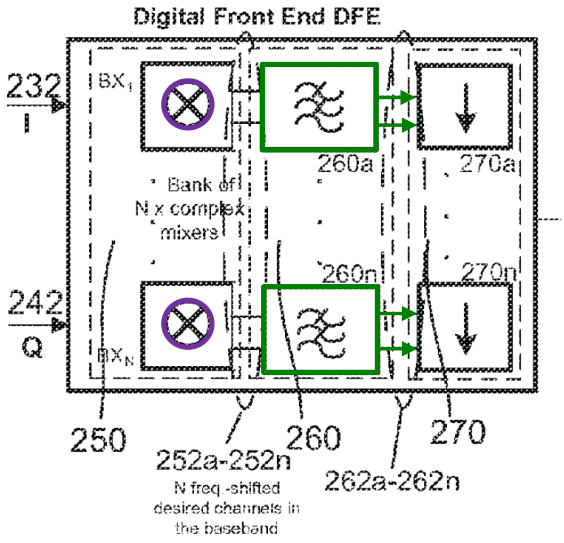


Fig. 3



Ex. 1013, Fig. 3 (annotated) **Ex. 1001, Fig. 2 (annotated)**

140. The multi-channel RF signal enters each multiplier 320, which shifts the frequency of the signal (which includes desired and undesired channels) such that the "target" frequency of one of the desired channels is re-centered to baseband (i.e., 0 Hz). Ex. 1013, [0031], [0032]. Each of a plurality of FIR LPFs 330(1) to 330(n) then selects a respective desired channel at baseband by passing it to the output (e.g., C_1), while filtering out the remaining channels in the signal. Ex. 1013, [0030]-[0032]. Thus, it is my opinion that Zhang discloses and teaches claims 8 and 9.

9.1.4. Independent Claim 11

141. The elements of claim 11 appear in the Claims Listing Appendix, labeled as elements [11A]-[11E]. Claim 11 is a method claim direct to substantially identical subject matter as system 1. Claim 11 includes steps that are the same functions performed by the same structures recited in claim 1. Thus, claim 11 is disclosed and taught by Zhang, for the same reasons discussed above with respect to claim 1. See my explanation above at Sections 9.1.1.a through 9.1.1.d.

a. [11A]: "A method comprising: in a wideband receiver system:"

142. It is my opinion that Zhang discloses "[a] method comprising: in a wideband receiver system:" as claimed.

143. Preamble [11A] is substantially identical to preamble [1A], and is disclosed and taught by Zhang for the same reasons set forth in connection with preamble [1A]. See my explanation at Section 9.1.1.a.

b. [11B]: "downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;"

144. It is my opinion that Zhang discloses "downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels," as claimed.

145. Element [11B] is substantially identical to Element [1B] and is disclosed and taught by Zhang for the same reasons set forth in connection with Element [1B]. See my explanation at Section 9.1.1.b. In particular, Element [11B] merely recasts the required functionality of Element [1B] as a performed step.

c. [11C]: "digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;"

146. It is my opinion that Zhang discloses "digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels," as claimed.

147. Element [11C] is substantially identical to Element [1C] and is disclosed and taught by Zhang for the same reasons set forth in connection with Element [1C]. See my explanation at Section 9.1.1.c. In particular, Element [11C] merely recasts the required functionality of Element [1C] as a performed step.

d. [11D] and [11E]:

[11D] "selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and"

[11E] "outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream."

148. It is my opinion that Zhang discloses "selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies," and "outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream" as claimed.

149. Elements [11D] and [11E] are substantially identical to Element [1D] and is disclosed and taught by Zhang for the same reasons set forth in connection with Element [1D]. See my explanation at Section 9.1.1.d. In particular, Elements [11D] and [11E] merely recasts the required functionality of Element [1D] as a performed step.

150. Reserved

151. Reserved

9.1.5. Dependent Claims 12 and 13

> **[12] "The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface."**
>
> **[13] "The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface."**

152. It is my opinion that Zhang discloses "[t]he method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface," as recited in claim 12, and "[t]he method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface," as recited in claim 13.

153. Claim 12 is substantially identical to claim 2 and is disclosed and taught by Zhang for the same reasons set forth in connection with claim 2. See my explanation at Section 9.1.2. In particular, claim 12 merely recasts the required functionality of claim 2 as a performed step.

154. Claim 13 is substantially identical to claim 3 and is disclosed and taught by Zhang for the same reasons set forth in connection with claim 3. See my explanation at Section 9.1.2. In particular, claim 13 merely recasts the required functionality of claim 3 as a performed step.

9.1.6. Dependent Claims 18 and 19

[18] "The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting."

[19] "The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter."

155. It is my opinion that Zhang discloses "[t]he method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting," as recited in claim 18, and "[t]he method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter," as recited in claim 19.

156. Claim 18 is substantially identical to claim 8 and is disclosed and taught by Zhang for the same reasons set forth in connection with claim 8. See my explanation at Section 9.1.3.

157. Claim 19 is substantially identical to claim 9 and is disclosed and taught by Zhang for the same reasons set forth in connection with claim 9. See my explanation at Section 9.1.3.

9.2. Zhang in View Pandey Render Claims 2, 3, 12, and 13 Obvious (Ground C)

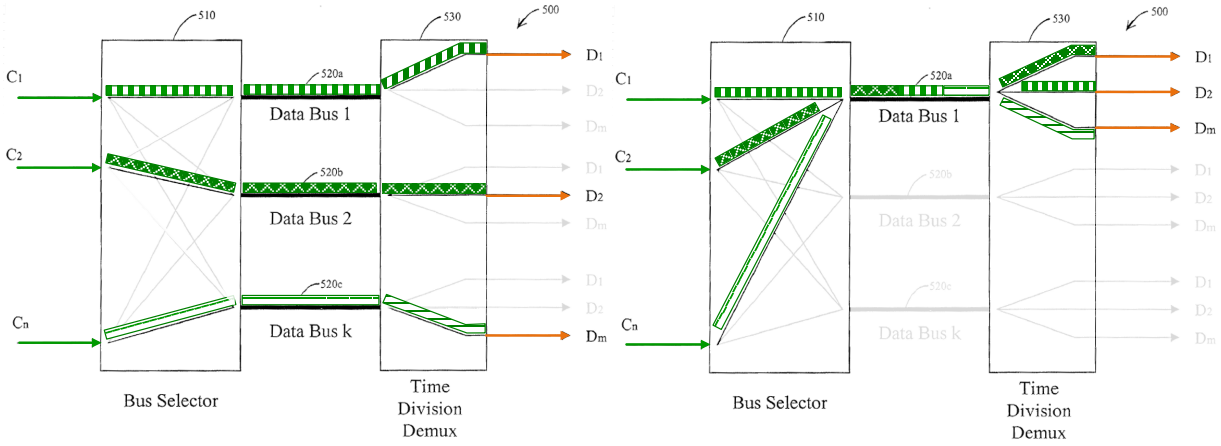
158. In the following, I provide an element-by-element analysis showing how Zhang in view of Pandey render claims 2, 3, 12, and 13 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.2.1. Dependent Claims 2 and 3

Claim 2: "The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface."

Claim 3: "The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface."

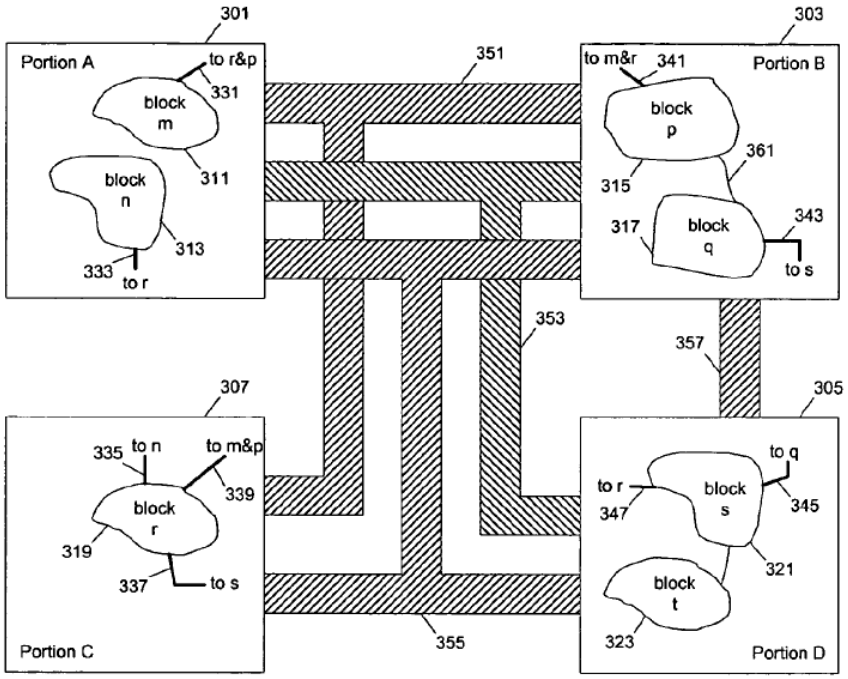
159. As described in Section 9.1.2, Zhang's digital selector implements both the serial and parallel interfaces of claims 2 and 3 to output a digital data stream of the selected channels, and to the extent it doesn't, such implementation would have been obvious based on Zhang in view of a POSITA's background knowledge (including the '362 Patent's AAPA). *See* Section 9.1.2, *supra*; Ex. 1013, [0038]-[0039]; Ex. 1001, 6:55-58; Ex. 1014, 30:31-42, 31:15-22; Ex. 1016, 79-80; Ex. 1017, 354-355.



Ex. 1013, Fig. 5 (annotated)

160. In addition, Pandey teaches creating specific serial and parallel interfaces using a computer aided technique for implementing a digital circuit design (e.g., such as Zhang's digital circuitry) on a FPGA or ASIC chip. Ex. 1014,

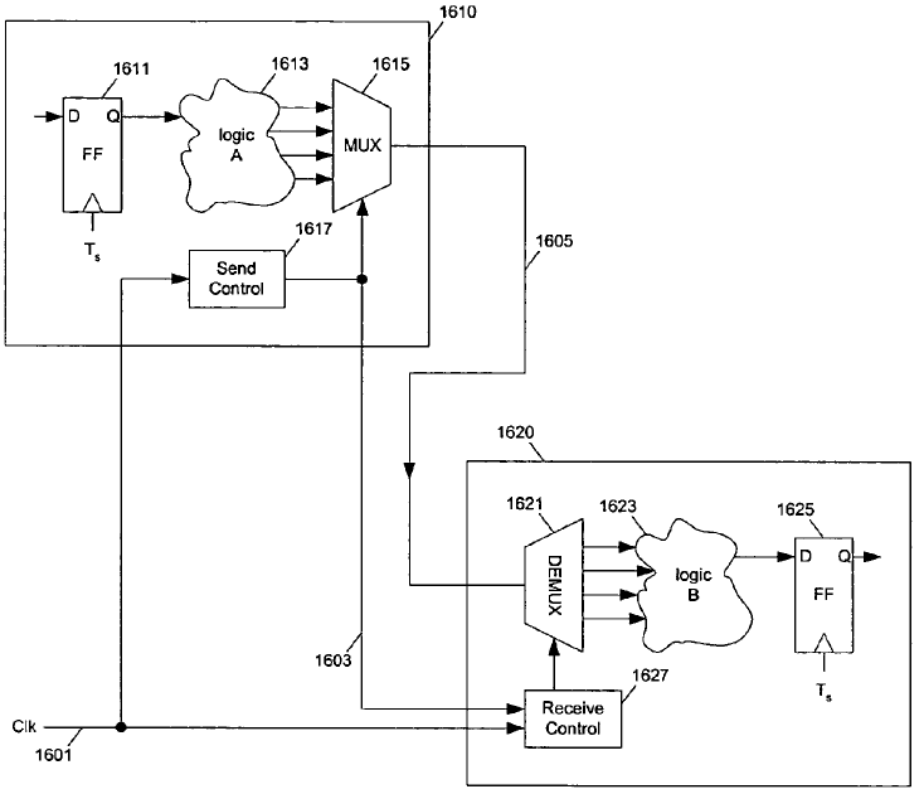
Abstract, 1:15-55, 2:4-12. The process involves partitioning functional blocks (such as Zhang's channel demultiplexer 230, digital selector 240, and demodulators 250) to different regions of an integrated circuit chip (e.g., 301, 303, 305, 307) and assigning wire traces (e.g., 351, 353, 355, 357) to interconnect the partitioned blocks. Ex. 1014, 1:56-60, 2:6-12, 2:64-3:5, 6:10-15, 11:6-19, 13:33-14:7.



Ex. 1014, Fig. 3

161. Pandey recognizes that the number of signals (nets) between function blocks in different partitions may exceed the number of traces (physical wires) available inside a chip, and that in such cases, multiple signals must be time-multiplexed (i.e. transmitted serially) over a single trace. Ex. 1014, 10:24-53, 10:58-11:5, 29:44-58, 30:31-42. For example, as shown below, a plurality of parallel signals from logic block A 1613 in a first partition are multiplexed by 1615 onto a

single trace 1605, and then demultiplexed back into parallel signals input to logic block B 1623 in a second partition. Ex. 1014, 30:31-52, Fig. 37.



Ex. 1014, Fig. 37

162. Pandey's process optimizes the partitioning of blocks based on reducing the multiplexing ratio of wires to signals required between partitions. Ex. 1014, 5:50-53, 6:11-15, 6:44-53, 7:13-19, 29:44-30:9, 30:53-31:12, 31:56-63, Figs. 38-39. Thus, depending upon the partitioning of the circuit design within finite area and finite interconnection of a chip, Pandey's optimization will in some layouts result in signals being grouped and time multiplexed through a serial interface between partitions, and in other layouts result in signals having individual dedicated traces with no multiplexing, which is a parallel interface. Ex. 1014, 31:20-22, 32:12-

15. Thus, Pandey teaches both serial and parallel interfaces for groups of signals between digital functional blocks, with the selection between the two interfaces being dependent on its optimization scheme for implementing a digital design and dependent upon the area and interconnect resources of a particular integrated chip. Ex. 1014, 11:6-19, 13:33-55, 31:20-22, 32:12-15, Figs. 2-3.

163. It is my opinion that it would have been obvious to apply Pandey's optimization for dedicated (i.e., parallel) and time-multiplexed (i.e., serial) interconnection to the interconnection between Zhang's demultiplexer 230, digital selector 240, and/or demodulators 250. Zhang teaches optimizing the real estate needed for implementing the digital portion of its system on a single chip, and the process described in Pandey would have been beneficial in this implementation. Ex. 1013, [0029], [0037], [0044], [0047]-[0048]; Ex. 1014, 1:20-2:12, 6:10-15. As such, the modification of Zhang with Pandey that results in parallel and/or serial interfaces from Zhang's Digital Channel DeMux 230 and Selector 240 to Demodulators 250 is merely a combination of prior art elements, for example, Zhang's circuit design and Pandey's interconnection in an integrated circuit chip, according to known methods (Pandey's process for implementing circuit designs with parallel and serial interfaces) to yield predictable results. A POSITA would also consider this combination as simply using a known technique for implementing data buses in an integrated circuit as taught in Pandy, to improve a similar integrated circuit having

data buses for outputting digital data streams as taught in Zhang, in the same way Pandy teaches to apply its technique

164. It would have been predictable for a POSITA to combine Zhang and Pandy in this way because Pandey's process considers available resources in terms of chip area and trace availability and is optimized to fit a target design (e.g., Zhang's digital circuit) within those resources. Ex. 1014, 31:15-22, 32:7-15. Where trace resources for a particular integrated circuit are insufficient, Pandey's process will predictably time-multiplex signals onto a single trace based on a desired multiplexer ratio, thus producing to a serial interface to Zhang's demodulators. *Id.* Likewise, where the resources are sufficient, Pandey's process will predictably reduce the multiplexer ratio to one and assign each signal to its own trace, thus producing a parallel interface to Zhang's demodulators. *Id*. Further, I understand that a POSITA would have had a reasonable expectation of success in combining Zhang and Pandey, because Pandey's optimization utilized processes such as floor planning, partitioning, and wire routing that were standard and well within a POSITA's skillset. Ex. 1014, 1:20-2:38.

9.2.2. Dependent Claim 12

Claim 12: "The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface."

165. Claim 12 is substantially identical to claim 2 and is taught by Zhang and Pandey, for the same reasons set forth in connection with claim 2. See my explanation at Section 9.2.1. In particular, claim 12 merely recasts the required functionality of claim 2 as a performed step.

9.2.3. Dependent Claim 13

Claim 13: "The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface."

166. Claim 13 is substantially identical to claim 3 and is taught by Zhang in view of Pandey, for the same reasons set forth in connection with claim 3. See my explanation at Section 9.2.1. In particular, claim 13 merely recasts the required functionality of claim 3 as a performed step.

9.3. Zhang in view Mirabbasi Render Claims 4-6 and 14-16 Obvious (Ground D)

167. In the following, I provide an element-by-element analysis showing how Zhang in view of Mirabbasi render claims 4-6 and 14-16 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.3.1. Dependent Claims 4-6

Claim 4: "The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal."

Claim [5A] "The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises:"

[5B] "a first ADC configured to generate a digital in-phase signal; and"

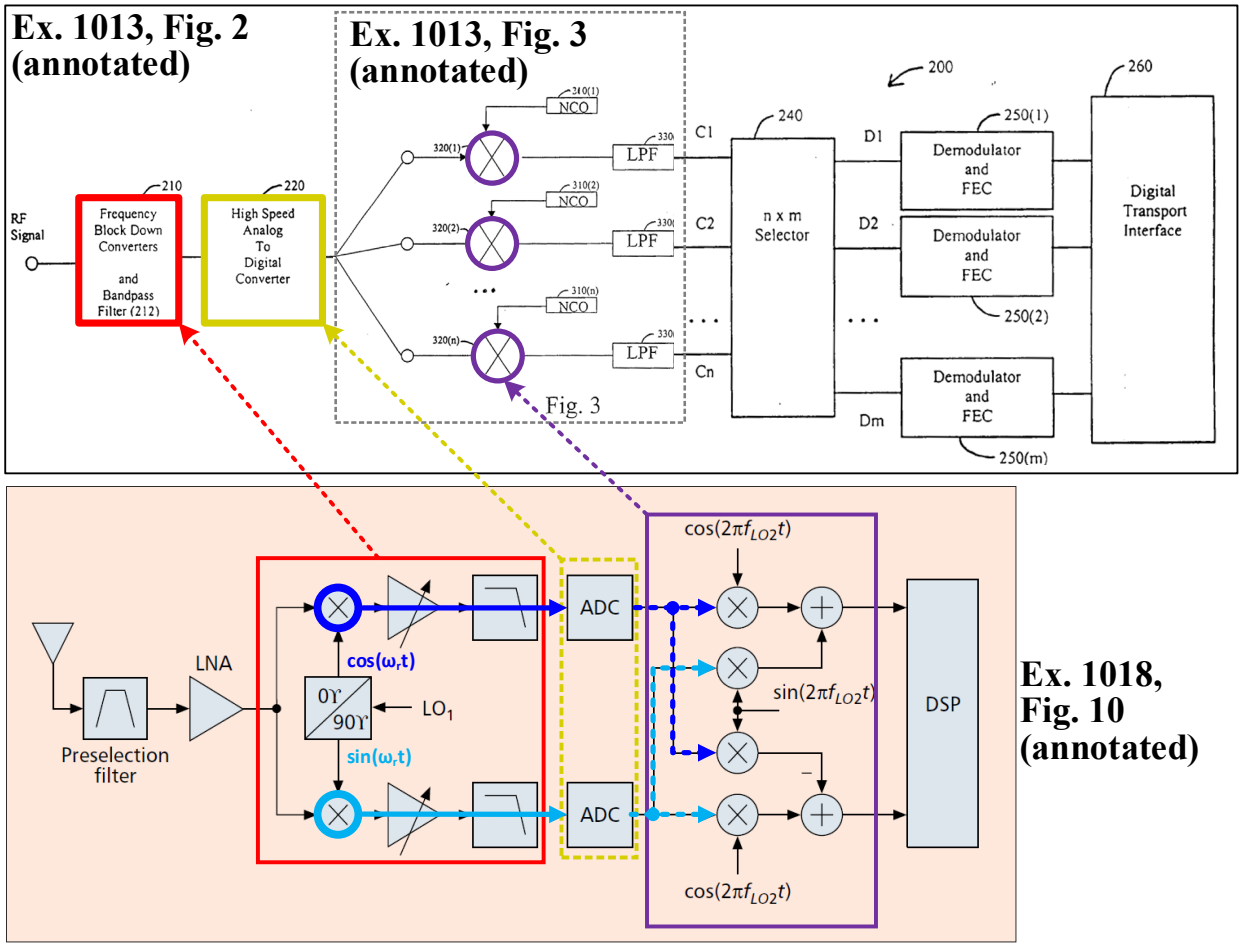
[5C] "a second ADC configured to generate a digital quadrature signal."

Claim 6: "The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels."

168. As I explain above with respect to Elements [1B] and [1C], Zhang's frequency block down converter 210 (red) (the claimed "mixer module") receives a multi-channel *analog* RF signal from a TV system and downconverts the signal to a lower frequency range so that signal can be digitized by ADC 220 (gold) (the claimed "wideband analog-to-digital converter") to a multi-channel *digital* RF signal. Ex. 1013, [0005], [0023]-[0025], [0029], [0041], claims 13, 27, 33. As I further explain with respect to Element [1D] and claim 8, Zhang's digitized output from ADC 220 is input to individual complex multipliers 320 within Digital Channel Demultiplexer 230 (purple) (the claimed "digital circuitry"). Ex. 1013, [0030]-[0032]; *see* Sections 9.1.1.d, 9.1.3, *supra*.

169. It is my opinion that a POSITA would have found it obvious to implement Converter 210 (red), ADC 220 (gold), and Demultiplexer 230 (purple), with the circuits recited in claims 4, 5, and 6, respectively, based on Zhang's teachings, the POSITA's general knowledge, and Mirabbasi.

170. Mirabbasi provides a tutorial of known RF receiver architectures used for receiving digitally modulated RF signals. Ex. 1018 at 4, 11. As shown below, Mirabbasi describes a well-known "Low-IF Receiver" having the same architecture as that in Zhang, which is a RF analog frontend (red) that performs frequency downconversion of the analog input to an intermediate frequency (IF), followed by an analog-to-digital converter (gold) that digitizes the analog IF signal, followed by a digital multiplexer (purple) that further downconverts the digitized signal to a baseband signal, which is then processed by additional digital circuitry to demodulate the signal and recover the modulated data. Ex. 1018 at 9-10, Fig. 10; *see also* Ex. 1025 at 272, 279-280; Ex. 1034 at 54-63; Ex. 1013, [0023]-[0029], Fig. 2.



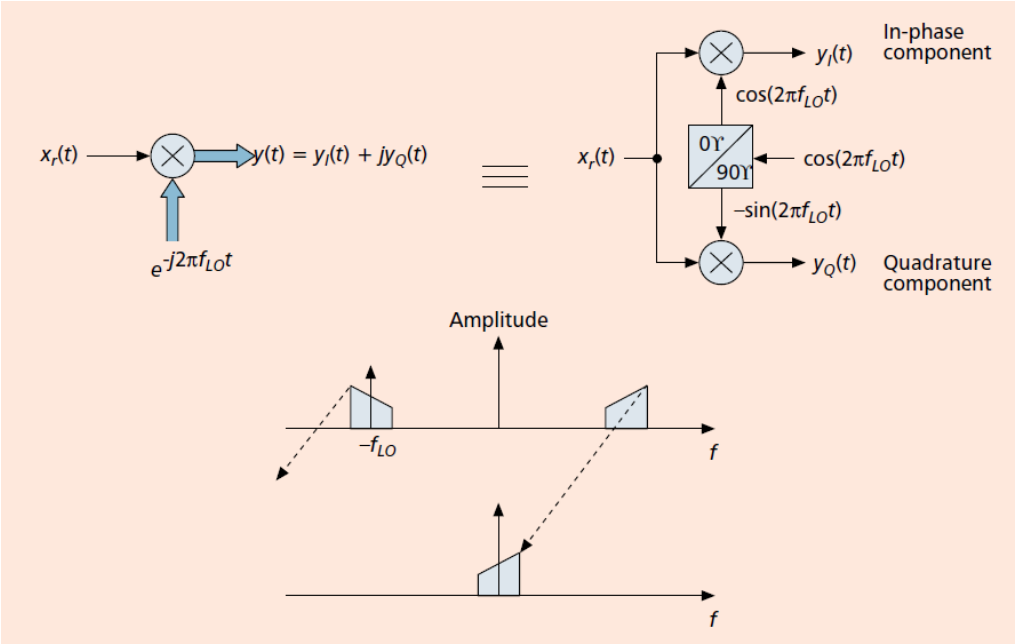
Ex. 1018, Fig. 10 (annotated)

171. Mirabbasi also describes a well-known "double-conversion wideband IF receiver" having a similar structure as the "Low-IF Receiver." Ex. 1018 at 9-10, Fig. 10. Both the "double-conversion wideband IF receiver" and the "Low-IF Receiver" employ "two quadrature downconversion paths in a heterodyne receiver, all of the required information for the separation of the wanted signal from unwanted signals, such as images, is available in the two IF signals." *Id*. at 138. Mirabbasi discusses the subtle differences between the two including the choice of IF and the requirements for the analog-to-digital converters. *Id*.

a. Claim 4

172. It is my opinion that Zhang in view of Mirabbasi disclose "[t]he wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal," as recited in claim 4.

173. As shown above, Mirabbasi's RF analog frontend (red), includes a complex mixer composed of a first real mixer (dark blue circle) and a second real mixer (light blue circle) that receive the analog RF signal through a low noise amplifier (LNA) and multiply the analog RF signal by a local oscillator (LO_1) sinusoid signal. Ex. 1018 at 5-6 (describing mixing a real input signal with a with complex exponential per Mirabbasi Figure 2 to produce in-phase and quadrature components), 137-138, Figs. 2, 10.



Ex. 1018, Fig. 2

174. Mirabbasi explains that "[t]he realization of a multiplier for mixing a real signal with a complex exponential requires two real multipliers, as illustrated in Fig. 2. The real and imaginary parts of the mixer output are called the *in-phase* (I) and *quadrature* (Q) components of the downconverted signal (since cosine and sine are in quadrature)." Ex. 1018 at 6. I understand that the in-phase (I) component of the mixer output is the same as or substantially similar to the claimed in-phase signal and the quadrature (Q) component of the mixer output is the same as or substantially similar to the claimed quadrature signal.

175. Specifically, as shown in Figure 10 of Mirabbasi, the first real mixer receives LO_1 with zero phase shift (denoted "0Y", e.g., cos(ωt)), causing the first mixer to generate an in-phase signal (dark blue line), and the second mixer receives the LO_1 signal with a 90-degree phase shift (denoted "90Y", e.g., sin(ωt)), causing the second mixer to generate a quadrature signal (light blue line). Ex. 1018 at 5-6, 10, Fig. 10; Ex. 1025 at 274-275, Fig. 22; Ex. 1034 at 54-56. Thus, it is my opinion that Mirabbasi thus discloses the features of claim 4.

b. Claim 5

176. It is my opinion that Zhang in view of Mirabbasi disclose "[t]he wideband receiver system of claim 1, wherein said wideband analog-to-digital

converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal," as recited in claim 5.

177. In Mirabbasi, following generation by the mixers, the in-phase (dark blue line) and quadrature (light blue line) signals are passed through amplifiers and filters respectively to first and second ADCs (gold) to generate a digital in-phase signal and a digital quadrature signal, respectively, thus disclosing the features of claim 5. Ex. 1018 at 10; Ex. 1025 at 274-275, 279-280; Ex. 1034 at 54-56, 61-62, Fig. 3.29a.

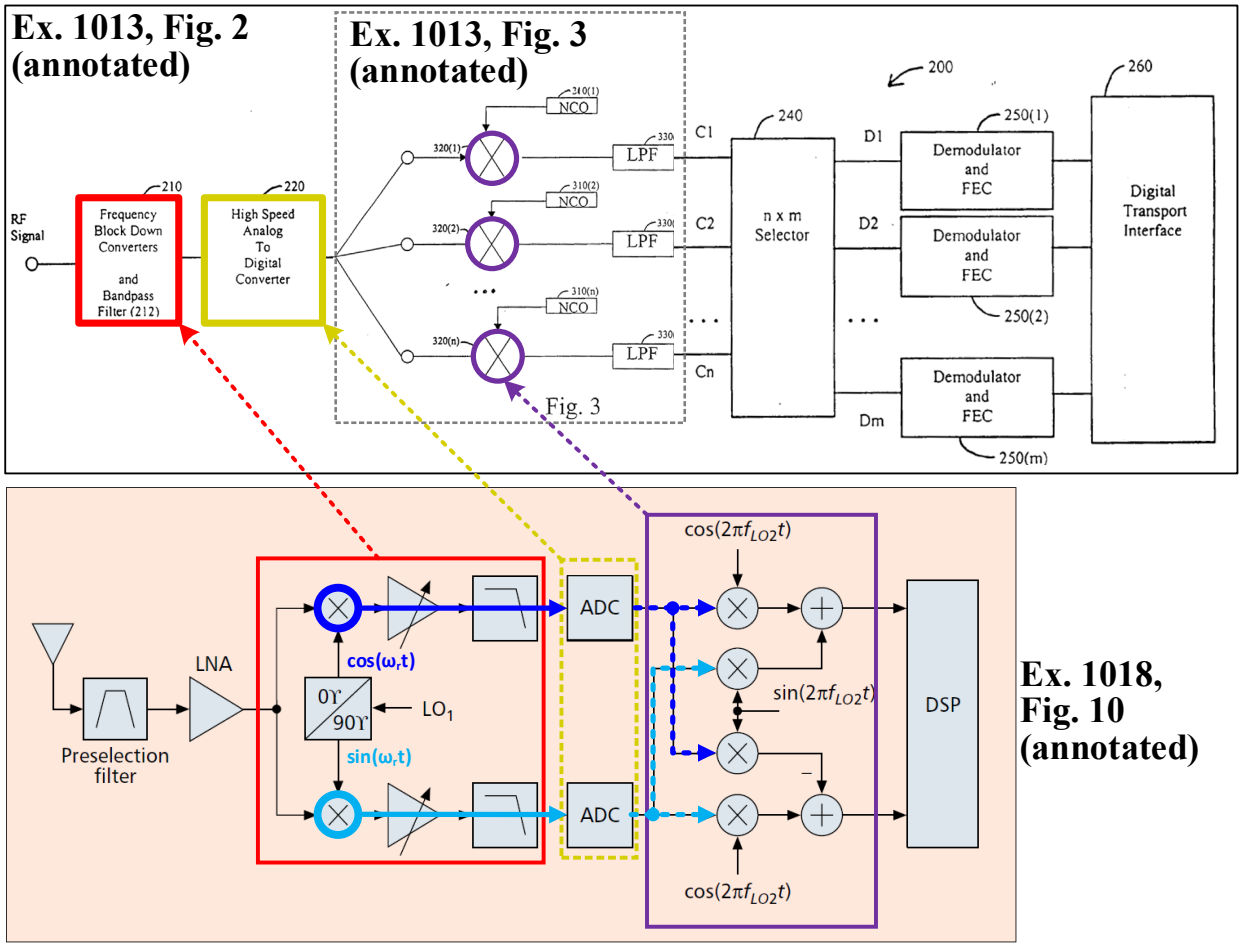
c. Claim 6

178. It is my opinion that Zhang in view of Mirabbasi disclose "[t]he wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels," as recited in claim 6.

179. Mirabbasi's digital in-phase (dashed dark blue line) and quadrature (dashed light blue line) signals then enter digital circuitry (purple), which in both Zhang and Mirabbasi include complex mixers for shifting the frequency of the selected desired television channels as recited in claim 6. A composite of Figures 2

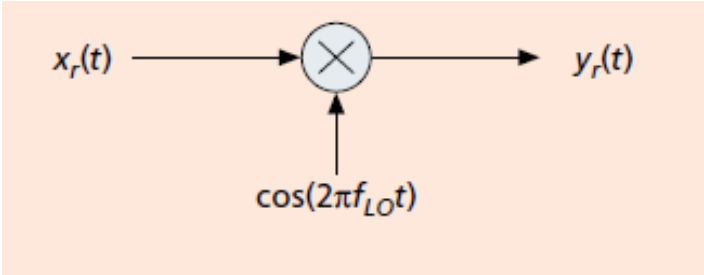
and 3 of Zhang alongside Figure 10 of Mirabbasi is provided below to illustrate the complex mixers within the combined system.

180. As described above with respect Element [1D], the digitized signal output by the ADC (gold) in Zhang is input to a Digital Channel Demultiplexer 230 (the claimed "digital circuitry"), which includes individual "complex multipliers 320(1…n)" (purple circles). Ex. 1013, [0030]-[0032].



181. It is my opinion that a POSITA would have understood that "multiplier" (as used in Zhang) and "mixer" are interchangeable names for the same device shown below, which multiplies an input signal (e.g., $x_r(t)$) by a sinusoidal signal

(e.g., $\cos(2\pi f_{LO}t)$) to generate an output signal (e.g., $y_r(t)$) that matches the input signal, but at a shifted frequency. Ex. 1013, [0032]; Ex. 1018 at Fig. 1, 5; Ex. 1001, 4:42-43, 6:7-27, 9:17-22. For example, Mirabbasi states: "[t]ypically, frequency downconversion of a passband signal is performed by multiplying (mixing) the signal with a sinusoid such as $\cos(2\pi f_{LO}t)$"). Ex. 1018, pp. 4-5, 11, Fig. 1.



Ex. 1018, Fig. 1 (cropped)

The '362 patent also uses the terms mixer and multiplier interchangeably. For example, it states that "mixers 211 and 221 multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency." Ex. 1001, 4:42-43. It also refers to the elements in Figure 3 (circles with an "X" through them as shown below) interchangeably as four "multipliers" and also as four "digital mixers." Ex. 1001, 6:7-27, 9:17-22.

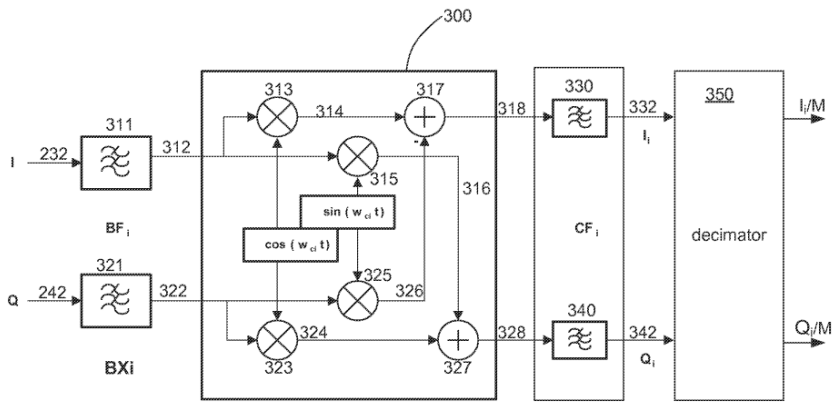
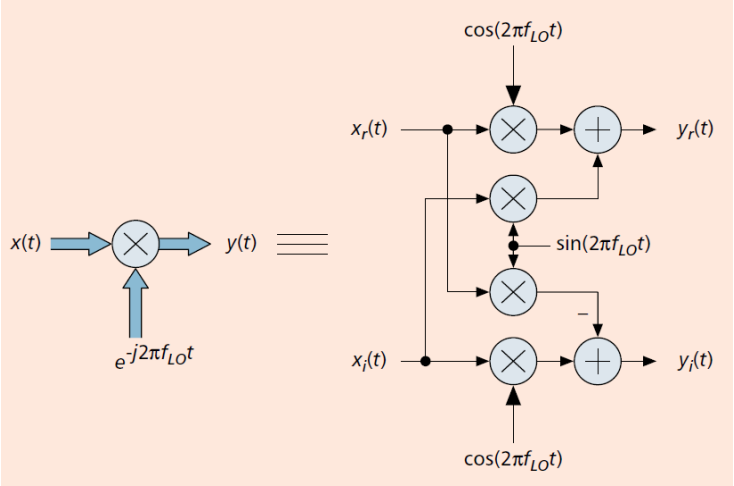


FIG. 3
Ex. 1001, Fig. 3

182. A mixer/mulitplier is "complex," if it multiplies the input RF signal by a complex signal, having real and imaginary parts, referred to as in-phase and quadrature signals. Ex. 1018, 5. A complex mixer/multiplier can include up to four real mixers/multipliers as shown in Figure 3 of Mirabasi below. As shown, a complex mixer/multipler may be represented schematically with the symbol of a single mixer/muliplier (left) (as in Zhang), or as by its combination of real mixers (right) as further described below.

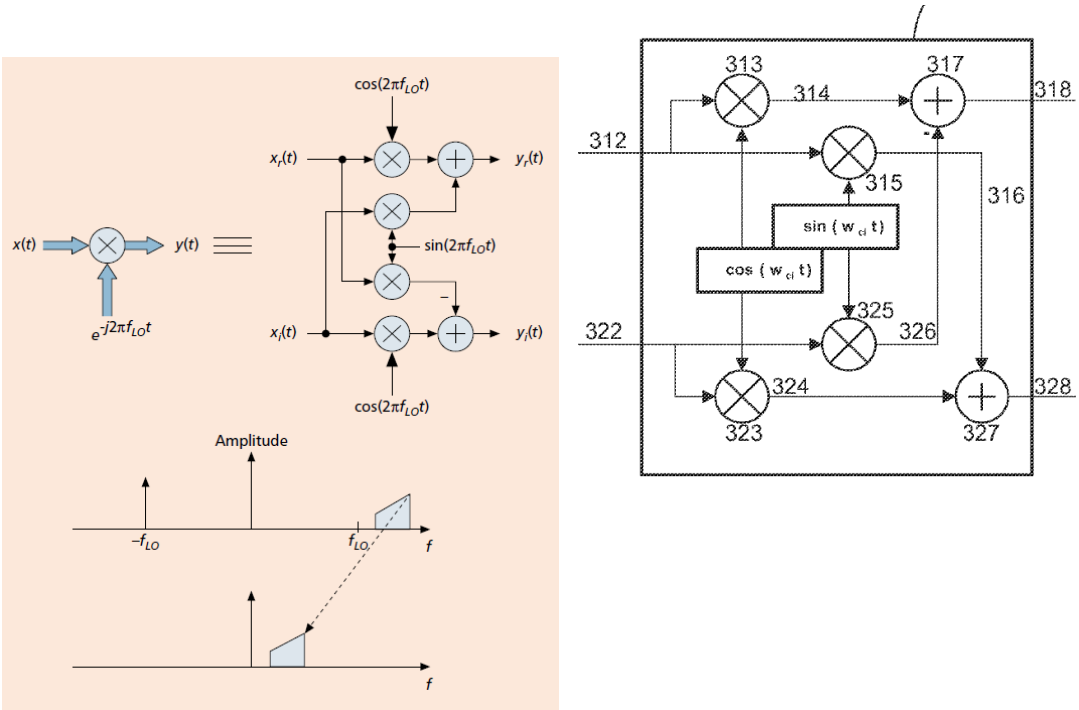


Ex. 1018, Fig. 3

183. Each of Zhang's complex multipliers (mixers) shifts the frequency of the multichannel digital RF signal such that "the frequency of target RF channel signal is shifted to a desired channel," which in some embodiments is "baseband, i.e., centered at DC." Ex. 1013, [0012], [0030]-[0032]. Zhang includes a plurality of complex multipliers (mixers) for shifting the frequency of the plurality of desired channels, respectively, thus disclosing the features of claim 6. Ex. 1013, [0030]-[0032].

184. Similarly, Mirabbasi, discloses the structure of one complex mixer (purple box) receiving the digital in-phase (dashed dark blue line) and quadrature (dashed light blue line) signals from its ADCs (gold). As Mirabbasi explains and illustrates, a "complex" mixer includes multiple individual mixers, such as "four real mixers is shown in Fig. 3" for mixing complex signals having in-phase and quadrature components. Ex. 1018 at 5-6, Figs. 2, 3, 10; *see also* Ex. 1034 at 35-36,

Fig. 3.3. Mirabbasi's complex mixer has the identical structure and performs the identical downconversion (i.e., shifting the frequency of in-phase and quadrature components of the digital complex input signal) as mixer 300 shown in Figure 3 of the '362 patent. Ex. 1018 at 9-10; Ex. 1001, Fig. 3, 6:7-25, 9:17-22; *see also* Ex. 1025 at 279-280; Ex. 1034 at 63.



Ex. 1018, Fig. 3; 1001, Fig. 3 (excerpted)

d. Rational to Modify Zhang with Mirabbasi for Teaching Claims 4, 5, and 6

185. As shown in the comparative figure above, Mirabbasi's low-IF receiver illustrated in Figure 10 has the same basic architecture and performs the same functions as Zhang's receiver illustrated in Figure 2. Mirabbasi's low-IF receiver provides specific implementation details that are absent in Zhang and which a

POSITA would have found advantageous to implement the Zhang receiver, for example, by implementing: 1) Zhang's Frequency Block Down Converter 210 using Mirabbasi's analog complex mixer (red) including first (green) and second (orange) mixers to generate in-phase and quadrature signals (claim 4); 2) Zhang's wideband analog-to-digital converter with Mirabbasi's pair of ADCs (gold) for digitizing the in-phase and quadrature signals (claim 5); and 3) each of Zhang's complex multipliers (mixers) as originally described in Zhang (purple circles) or with Mirabbasi's complex mixer (purple box).

186. As described in Mirabbasi, the "low-IF" architecture (the combination of red, gold, purple circuits) overcomes a number of issues found in other common RF receiver designs, such as heterodyne, homodyne, and wideband IF with double-conversion receivers. Ex. 1018 at 6-10. Such advantages of the low-IF receiver include eliminating DC offset in the baseband signals, making the sampling of the IF signal with ADCs more feasible because the IF signal is at a lower frequency, and eliminating gain and phase mismatches between the in-phase and quadrature signals because they are partially downconverted and corrected digitally. Ex. 1018 at 8, 10. Because of these advantages, a POSITA would have been motivated to use Mirabbasi's low-IF design—i.e., it's analog complex mixer (red) including first (green) and second (orange) mixers, pair of ADCs (gold), and (optionally) its complex mixer (purple box)—to implement Zhang's corresponding receiver

components as described above. Indeed, some issues like DC offset are significant in CMOS, a technology in which the Zhang receiver is implemented, and thus a POSITA would have found Mirabbasi's low-IF architecture, which eliminates DC offset, to be particularly beneficial. Ex. 1013, [0048]; Ex. 1018 at 8-9.

187. Thus, modifying Zhang with Mirabbasi as described above to include the features of claims 4, 5, and 6 would have been nothing more than using a known technique (Mirabbasi's low-IF receiver) to improve a similar device (Zhang's receiver having the same basic architecture) in the same way (Mirabbasi's low-IF receiver improves over other common architectures described by Mirabbasi) with a predictable result.

188. This combination of Zhang and Mirabbasi is predictable because Mirabbasi's low-IF architecture used components that were common and well known to a POSITA, and because the basic architecture of the low-IF receiver matched that of Zhang's receiver, thus requiring little or no deviation in Mirabbasi's implementation when applied to Zhang. *See e.g.,* Ex. 1025 at 279-280; Ex. 1034 at 63. Further, I understand a POSITA would have had a reasonable expectation of success in combining Zhang and Mirabbasi, because the implementation of Mirabbasi's receiver was taught in basic textbooks and well within a POSITA's skillset. *See e.g.,* Ex. 1025 at 279-280; Ex. 1034 at 63.

9.3.2. Dependent Claims 14-16

Claim [14A] "The method of claim 11, comprising:"

[14B] "generating, by a first mixer of said mixer module, an in-phase signal; and"

[14C] "generating, by a second mixer of said mixer module, a quadrature signal."

Claim [15A] "The method of claim 11, comprising:"

[15B] "generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and"

[15C] "generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal."

Claim [16] "The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry."

189. It is my opinion that Zhang in view of Mirabbasi disclose each of claims 14-16.

190. Claims 14-16 recast the required functionality of claims 4-6 as method steps performed by identical structural elements. Thus, claims 14-16 are directed to substantially identical subject matter as claims 4-6, respectively and are rendered obvious by the combination of Zhang and Mirabbasi, for the same reasons discussed above with respect to claims 4-6. *See* Section 9.3.1, *supra*.

9.4. Zhang in view Mirabbasi and Karabinis Render Claims 7 and 17 Obvious (Ground E)

191. In the following, I provide an element-by-element analysis showing how Zhang in view of Mirabbasi and Karabinis, render claims 7 and 17 obvious. To

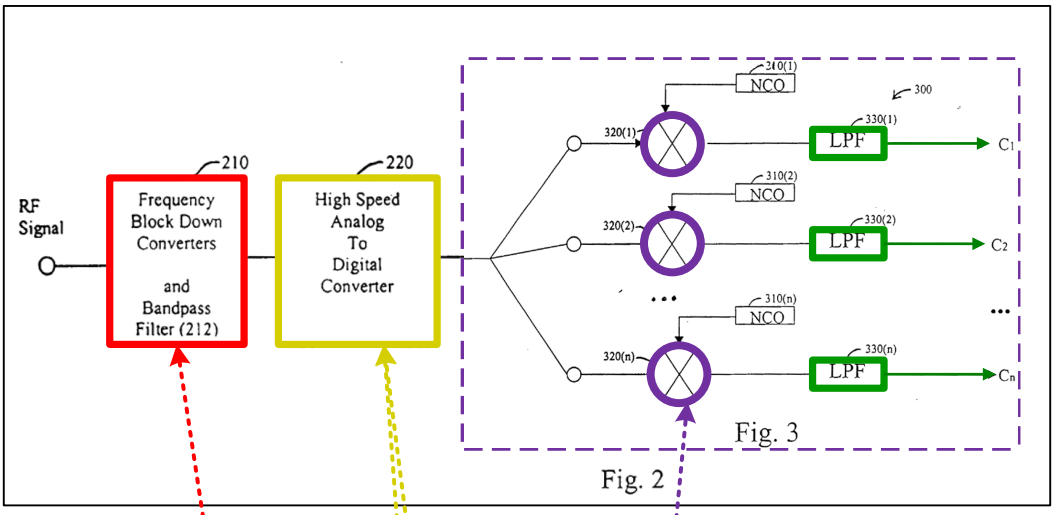
help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

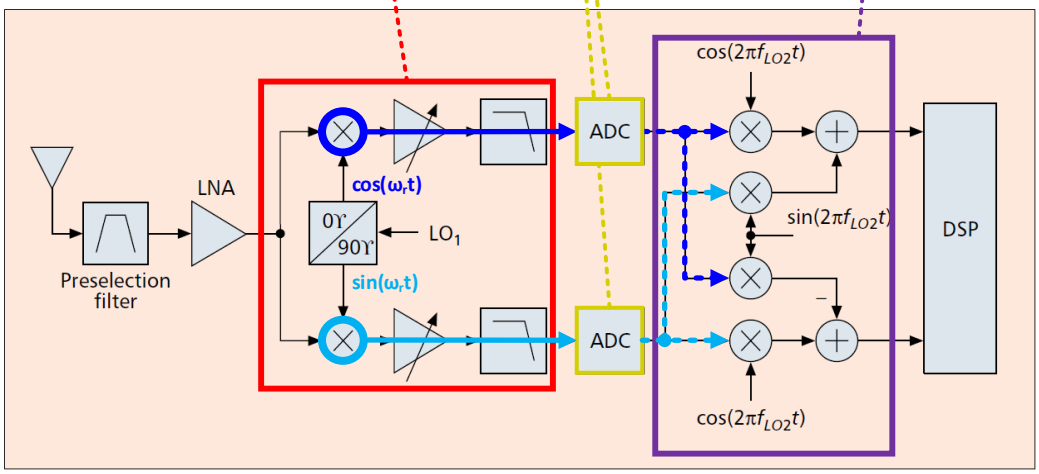
9.4.1. Dependent Claim 7

a. [7A] "The wideband receiver system of claim 6, wherein:"

192. As I explain in Section 9.3.1, Zhang in view of Mirabbasi disclose all of the features of claim 6, from which claim 7 depends. *See* Section 9.3.1, *supra.* In this combination, Zhang's digital circuitry includes a plurality of complex mixers (as taught in Zhang and/or Mirabbasi) (purple) "configured to frequency shift said selected plurality of desired television channels" as recited in claim 6. Ex. 1013, [0030]-[0032].

Ex. 1013, Figs. 2, 3 (annotated)





Ex. 1018, Fig. 10 (annotated)

b. [7B] "prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and"

193. Zhang's complex mixers (purple) receive from the ADC (red) a digitized multi-channel RF signal that includes a plurality of channels, each with a unique frequency spaced apart from one another (e.g., at 6 MHz intervals) and within a limited frequency band (e.g., 300 MHz). Ex. 1013, [0005]-[0006], [0024]-[0025], [0027], [0030]. Each of Zhang's mixers select from the plurality of channels one

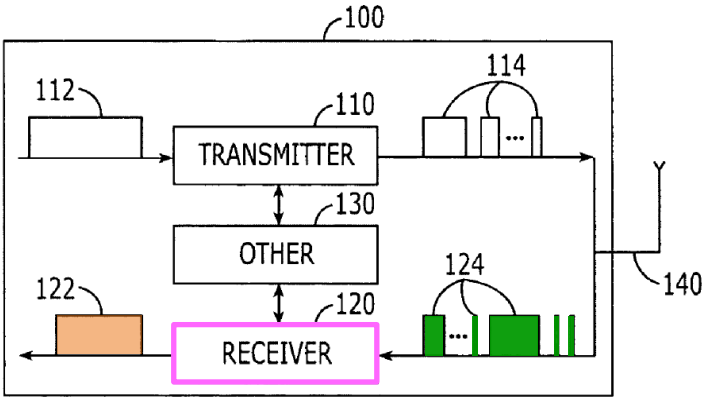
"desired" channel by controlling a numeric controlled oscillator 310 to the desired channels "target." Ex. 1013, [0012], [0030]-[0032].

194. The Zhang/Mirabbasi system includes any number "n" of mixers for a corresponding "n" desired channels "that are selected or used by a subscriber," with undesired channels filtered out by a low pass filter. Ex. 1013, [0028], [0030]-[0032], Figs. 2, 3, 4. Zhang further discloses that the RF channels need not be contiguous. Ex. 1013, [0048]. From this, it is my opinion that a POSITA would have understood that in some instances, the number of desired channels is less than all of the channels in the frequency band and any two desired channels may be separated by undesired channels in the digitized multi-channel RF signal. Thus, the complex mixers in the Zhang/Mirabbasi combination are configured to frequency shift the selected plurality of desired television channels, wherein prior to the frequency shift the selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum as recited in Element [7B].

c. [7C] "after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum."

195. As I explain above with respect to claim 6, each of Zhang/Mirabbasi's complex mixers shifts the frequency of the multichannel digital RF signal such that "the frequency of target RF channel signal is shifted to a desired channel." Ex. 1013, [0012], [0030]-[0032]. Zhang provides one example in which the target RF channels

are shifted to baseband (centered at 0Hz), but Zhang does not expressly disclose other examples, such as the desired television channels being in a contiguous frequency spectrum as recited in Element [7C]. *Id.* Karabinis, however, provides such an example as illustrated below, in which a receiver 120 (pink) receives a plurality of signals with non-contiguous frequencies (green), and translates the frequencies so that the signals are output within a contiguous frequency band (orange).



Ex. 1020, Fig. 1 (annotated)

196. As illustrated below, Karabinis's receiver (top figure) operates similarly to the Zhang/Mirabbasi receiver as I explain above with respect to claim 6. *See* Section 9.3.1, *supra*; Ex. 1020, [0036]-[0038], [0042]-[0044], [0047]-[0049], Figs. 1, 4, 5, 7. Like the receivers in Zhang and Mirabbasi, Karabinis's receiver is configured to receive signals at multiple non-contiguous frequencies, downconvert the signals using a mixer (not shown), and digitize the downconverted signal using an analog-to-digital converter (gold). Ex. 1020, [0010], [0031], [0037]-[0038],

[0042], [0047]-[0048]; Ex. 1013, Abstract, [0010], [0025], [0027]-[0028], [0031]-[0032], [0034], [0041]-[0042], claims 1, 2, 4, 7, 8, 28, 34, 36, 37.

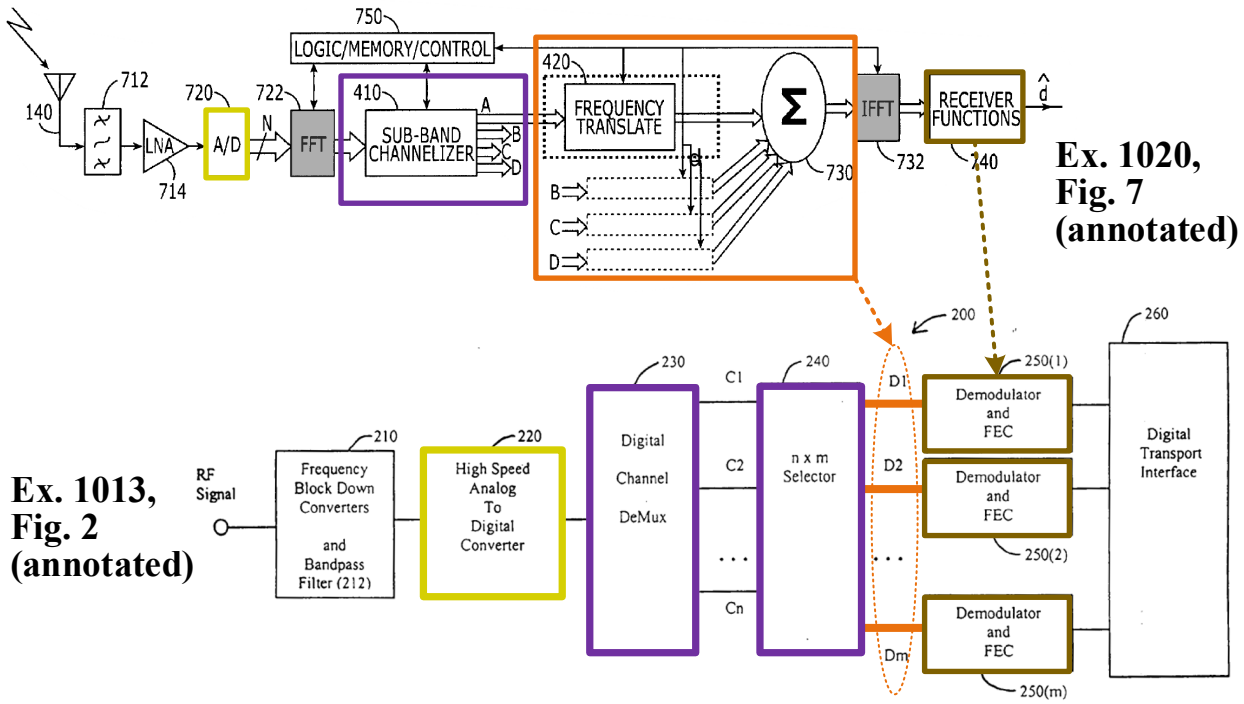


Fig. 2

197. Karabinis also includes digital circuitry—e.g., sub-band channelizer 410 (purple)—that performs the same function as Zhang's digital channel demultiplexer 230 and selector 240, which is to isolate the plurality of the non-contiguous frequencies (desired channels in Zhang) from the digitized signal and output them for demodulation. Ex. 1020, [0042], [0044], [0047], [0049], Figs. 4-5, 7.

198. Zhang's "m" desired channels, each at baseband (0Hz), are output from selector 240 to demodulators 250 (brown) via a set of buses. Ex. 1013, Fig. 5, [0029], [0038]-[0039], claim 3; *see* Sections 9.1.1.d (element [1D]), 9.1.2 (claims 2 and 3), *supra*. Since each of the desired channels are at the same baseband

frequency, they must be output on different buses in parallel or they must be time multiplexed serially on the same bus, since signals at the same baseband frequency would otherwise interfere with one another. *See* Sections 9.1.1.d (element [1D]), 9.1.2 (claims 2 and 3), *supra*.

199. For the same reasons, multiple Zhang demodulators are required for simultaneously receive and process the desired channels, or a single demodulator may sequentially receive and process multiple desired channels one at a time. *See* Sections 9.1.1.d (element [1D]), 9.1.2 (claims 2 and 3), *supra*.

200. Karabinis provides an alternate way to output Zhang/Mirabbasi's desired channels for demodulation, which is shift the frequencies of the desired channels (e.g., D_1-D_m) into a contiguous frequency band 422 (the claimed "contiguous frequency spectrum") using a plurality of frequency translators 420, and summing the shifted channels with a summer (orange).[1] Ex. 1020, [0017], [0042]-[0044], [0049]. For example, Zhang's outputs from selector 240 could be input into

---

[1] Karabinis's sub-band channelizer 410 and frequency translator 420 may optionally work in either the frequency domain by including FFT and IFFT blocks (grey) before and after 410 and 420 (*see* Figure 5), or work in the time domain by excluding the FFT and IFFT blocks (*see* Figure 4). Ex. 1020, [0024], [0041]-[0044], Figs. 4-5.

Karabinis's frequency translators 420 (Zhang's D1 into Karabinis's channel A, Zhang's D2 into Karabinis's channel B, Zhang's D3 into Karabinis's channel C, etc.) to generate a summed contiguous frequency band, which is then output to a demodulator (brown) to extract the modulated data from the selected channels. Ex. 1020, [0017]-[0018], [0042]-[0043], [0049], claims 8-9, 27-28, Figs. 4, 5, 7.

201. It is my opinion that a POSITA implementing the Zhang/Mirabbasi receiver would have considered it obvious to modify the design according to Karabinis to output a contiguous frequency spectrum with the desired channels as another known option for providing the channels for demodulation. Doing so would have permitted a demodulator, such as the one disclosed in Karabinis, to receive all of the desired channels simultaneously over a single bus, which would have eliminated the need of having Zhang's multiple data buses (1 through k) and time division demultiplexer between the buses and the demodulators (*see* Figure 5). It also would have enabled the Zhang/Mirabbasi receiver to use a single multichannel demodulator as in Karabinis, rather multiple single-channel demodulators.

202. As such, the modification of the Zhang/Mirabbasi receiver with Karabinis would have been nothing more than the simple substitution of known elements (Zhang's data buses, time division demultiplexer, and single-channel demodulators 250) with other known elements (Karabinis's frequency translator 420, summer 730, and multichannel demodulator 430/740) to obtain predictable

results. The modification would also have been the use of a known technique (Karabinis' channel translation from baseband to contiguous channels) to improve Zhang's similar device (by eliminating the need for Zhang's multiple buses and channel demultiplexer and enabling the use of a multichannel demodulator) in the same way as taught in Karabinis. This modification would have been predictable, and a POSITA would have a high expectation of success, because the substitution could be done with minimal modification to the surrounding hardware. For example, the isolated signals received by frequency translators 420 from sub-band channelizer 410 in Karabinis, would have been similar to the signals output by digital channel demultiplexer 230 and channel selector 240 in Zhang, with potentially the only difference being the frequencies of the selected channels that are being translated. Moreover, the circuits described in Zhang and Karabinis would have been well known to a POSITA.

203. Accordingly, Element [7C], and the entirety of claim 7, is obvious over the combination of Zhang, Mirabbasi, and Karabinis.

9.4.2. Dependent Claim 17

[17A] "The method of claim 16, wherein:"

[17B] "prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and"

[17C] "after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum."

204. Claim 17 is directed to substantially identical subject matter as claim 7, and thus is rendered obvious by the combination of Zhang, Mirabbasi and Karabinis, for the same reasons as I explain above with respect to claim 7. *See* Section 9.4.1, *supra*.

9.5. Zhang in view Jensen Render Claims 10 and 20 Obvious (Ground F)

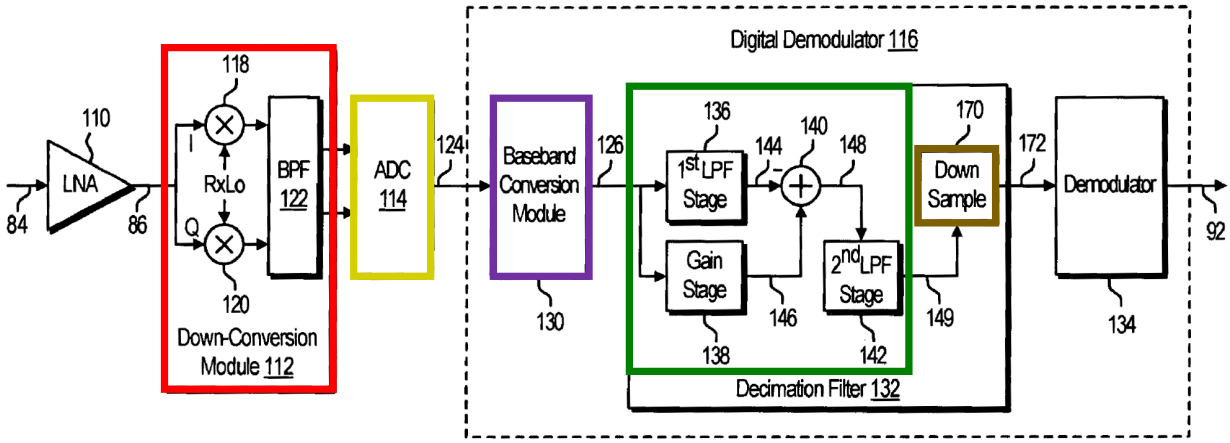
205. In the following, I provide an element-by-element analysis showing how Zhang in view of Jensen, render claims 10 and 20 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.5.1. Dependent Claim 10

Claim 10: "The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels."

206. As I explain in Sections9.1.1.d, Zhang discloses Digital Channel Demultiplexer 230 and Digital Selector 240, which individually and collectively teach Element [1D]("digital circuitry configured to[] select said plurality of desired television channels … and output … as a digital datastream"). *See* Section 9.1.1.d.

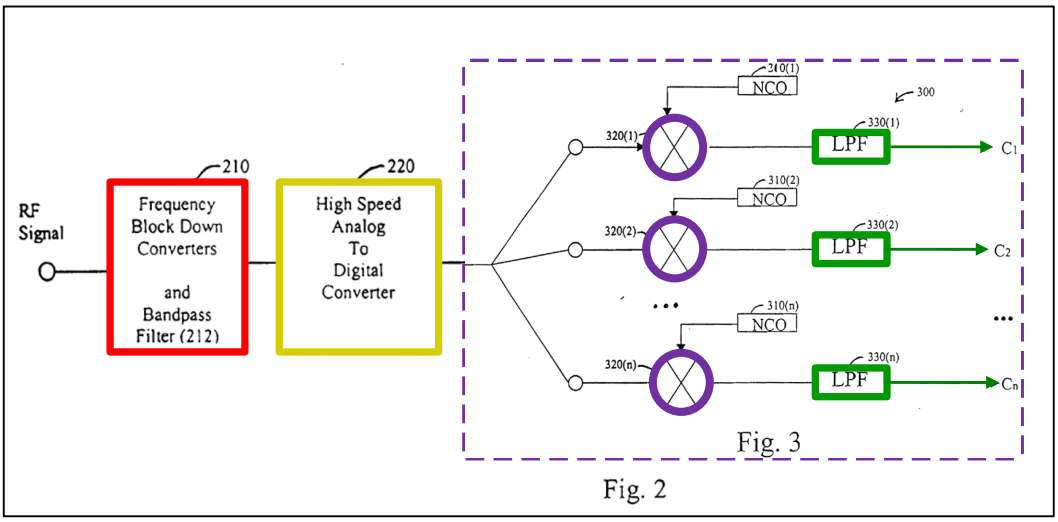
Zhang is silent with regard to whether Channel Demultiplexer 230 or Digital Selector 240 comprise a decimator circuit. As explained by Jensen, however, decimation (brown) was commonly performed to reduce a sampling rate of a digital signal. Ex. 1026, [0007], [0027]. For accurate reproduction of an analog signal, the ADC must sample the signal at least twice the rate as the highest frequency in the signal (this is referred to as the Nyquist theorem). *See* Section 8.3.4, *supra*. The RF signal sampled by the ADC includes a number of channels, thus having a wide bandwidth and requiring a high sampling rate. This results in a large amount of data produced by the ADC. *Id.* Processing this data to downconvert and filter produces the same amount of data, but that data now represents only single channel having a small bandwidth (e.g., 6 MHz). Because the processed data is much greater than needed to represent the single channel, the sample rate (i.e., the amount of data) can be reduced, which is referred to as decimation. Ex. 1026, [0007], [0027]; Ex. 1034 at 104; Ex. 1045 at 14-15, 70. Reducing the sampling rate reduces the amount of data processed by the digital circuitry, which reduces power consumption and complexity in subsequent processing. Ex. 1026, [0007]; *see also*, Section 8.3.4, *supra*.



Ex. 1026, Fig. 1 (annotated)

207. Jensen discloses a similar receiver to that of Zhang, including having an analogous down converter (red) to downconvert an RF signal to an IF signal, an ADC (gold) to convert the analog IF signal to a digital IF signal, a baseband conversion module (i.e., mixer module) (purple) to convert the digital IF signal to a baseband signal, and a low pass channel select filter (green). *Compare* Ex. 1026, Fig. 1, [0027] *with* Ex. 1013, Figs. 2, 3 (annotated below), [0026]-[0028], [0030]-[0032].

Ex. 1013, Figs. 2, 3 (annotated)



208. This issue of sampling rates described in Jensen is precisely the situation in Zhang's design, where the rate of Zhang's ADCs for sampling the wideband RF source signals is much higher (e.g., 300 MHz) than the rate for demodulating individual demultiplexed 6 MHz channels (e.g., requiring a sampling rate of 12 MHz). Ex. 1013, [0007], [0025], [0029]; Ex. 1026, [0030]; *see also*, Section 8.3.4, *supra* (explaining the Nyquist theorem).

209. Following Jensen, it is my opinion that a POSITA would have included a decimator circuit in the Zhang' Channel Demultiplexer 230 or Digital Selector 240, either as a separate component following the low pass filters 330 or as part of channel-select decimation filters used for the low pass filters 330, to reduce the sampling rate of digital signals and thereby reduce power consumption and/or complexity in subsequent processing (e.g., in demodulators 250). Ex. 1013, Fig. 3, [0029]-[0032]. Such a combination of Zhang with Jensen would have been nothing more than the use of a known technique (Jensen's decimator following a channel select filter) to improve a similar device (Zhang's receiver with similar architecture) in the same way that Jensen describes.

210. As disclosed by Jensen, the use of decimation modules or of channel-select decimation filters (which combined a FIR filter with decimation) was common (and thus well-known), and the result of including decimation in the Zhang's

Channel Demultiplexer 230 or Digital Selector 240 would thus have been predictable to a POSITA. Ex. 1026, [0007]. Thus, it is my opinion that Zhang in view of Jensen disclose claim 10. Further, a POSITA would have had a reasonable expectation of success in combining Zhang and Jensen, because Jensen's down sampler merely requires removing some of the data in the output data stream, which easily could have been done with Zhang's digital circuitry and was well within the capability of a POSITA to implement.

9.5.2. Dependent Claim 20

Claim 20: "The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels."

211. Claim 20 recasts the required functionality of claim 10 as a method step performed by nearly identical structural elements. Claim 10's functional language of "wherein said digital circuitry comprises a decimator circuit configured to decimate" is revised in claim 20 to the step of "decimating, by said digital circuitry." Thus, claim 20 is directed to substantially identical subject matter as claim 10 and rendered obvious by the combination of Zhang and Jensen, for the same reasons discussed above with respect to claim 10. *See* Section 9.5.1, *supra*.

9.6. Alternate Grounds based on Means-Plus-Function Construction of "digital circuitry"

9.6.1. Claims 1, 2-6, and 8-9 based on Zhang (Grounds A/B)

212. As I noted above in Section 6, I was asked to consider a potential means-plus function construction of "digital circuitry" of Element [1D] is construed to be a means-plus function term. As discussed in that section, the corresponding structure is illustrated in Figures 2 and 3 of the '362 patent.

213. To the extent "digital circuitry" of Element [1D] is construed to be a means-plus function term, it is my opinion that as shown in the comparison of Zhang to the '362 patent above, Zhang's Digital Channel Demultiplexer 230 includes the same or equivalent structure as disclosed in the '362 patent (e.g., multiple parallel paths, each including a complex mixer followed by a low pass filter followed by serial and parallel interfaces as shown in Figures 2 and 3 of Zhang and Figure 2 of the '362 patent), with any differences being insubstantial. In both Zhang and the '362 patent, each path performs the same function of outputting a respective desired channel, in the same way by first downconverting the respective desired channel to baseband and then low pass filtering with a FIR filter to isolate the channel, to achieve the same result of selecting and outputting a plurality of desired channels as a digital data stream

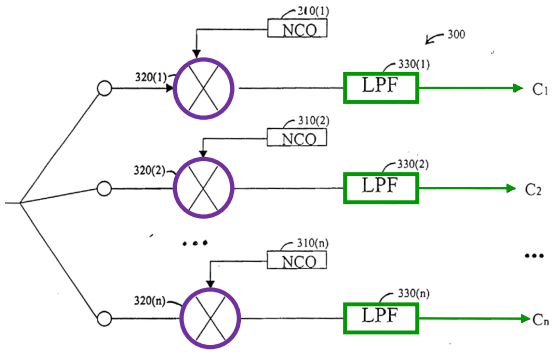
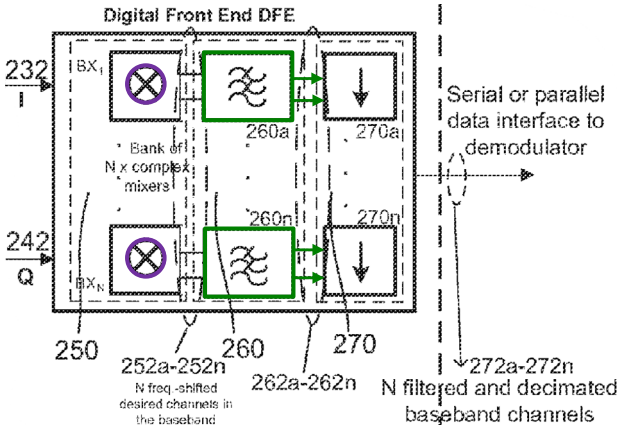


Fig. 3

Ex. 1013, Fig. 3 (annotated)



Ex. 1001, Fig. 2 (annotated)

Compare Ex. 1001, 2:51-55, 5:49-6:54 *with* Ex. 1013, [0027], [0030], [0031], [0032]; *see also* Sections 9.1.1.d, 9.1.3 (claims 8 and 9), *supra*.

214. Thus, Zhang anticipates and renders obvious claims 1, 2-3, 8-9 (Sections 9.1.1-3), Zhang-Pandey renders obvious claims 2-3 (Section 9.2.1), Zhang-Mirabbasi renders obvious claims 4-6 (Sections 9.3.1-3), Zhang-Mirabbasi-Karabinis renders obvious claim 7 (Section 9.4.1), and Zhang-Jenson renders obvious claim 10 (Section 9.5.1), for the reasons stated above, even if "digital circuitry" is given a means-plus-function construction.

9.6.2. Claims 1-9 based on Zhang-Mirabbasi (Ground D)

215. Further, if "digital circuitry" of Element [1D] were to be construed as a means-plus function term, and to the corresponding structure were limited to only what is shown in Figure 3, it is my opinion that Zhang-Mirabbassi teaches this element.

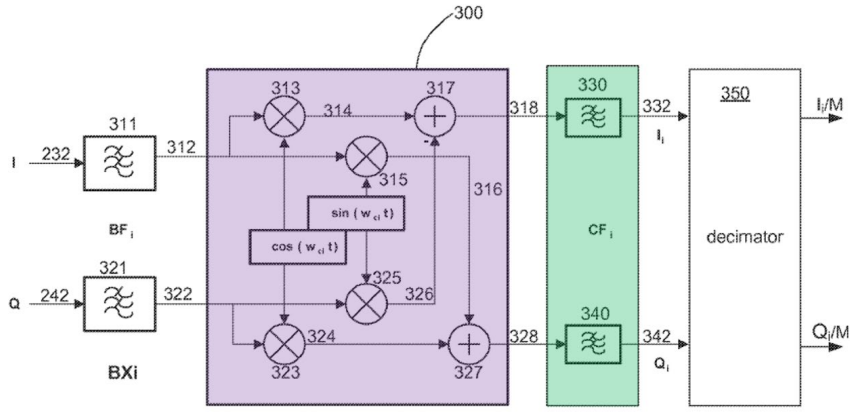
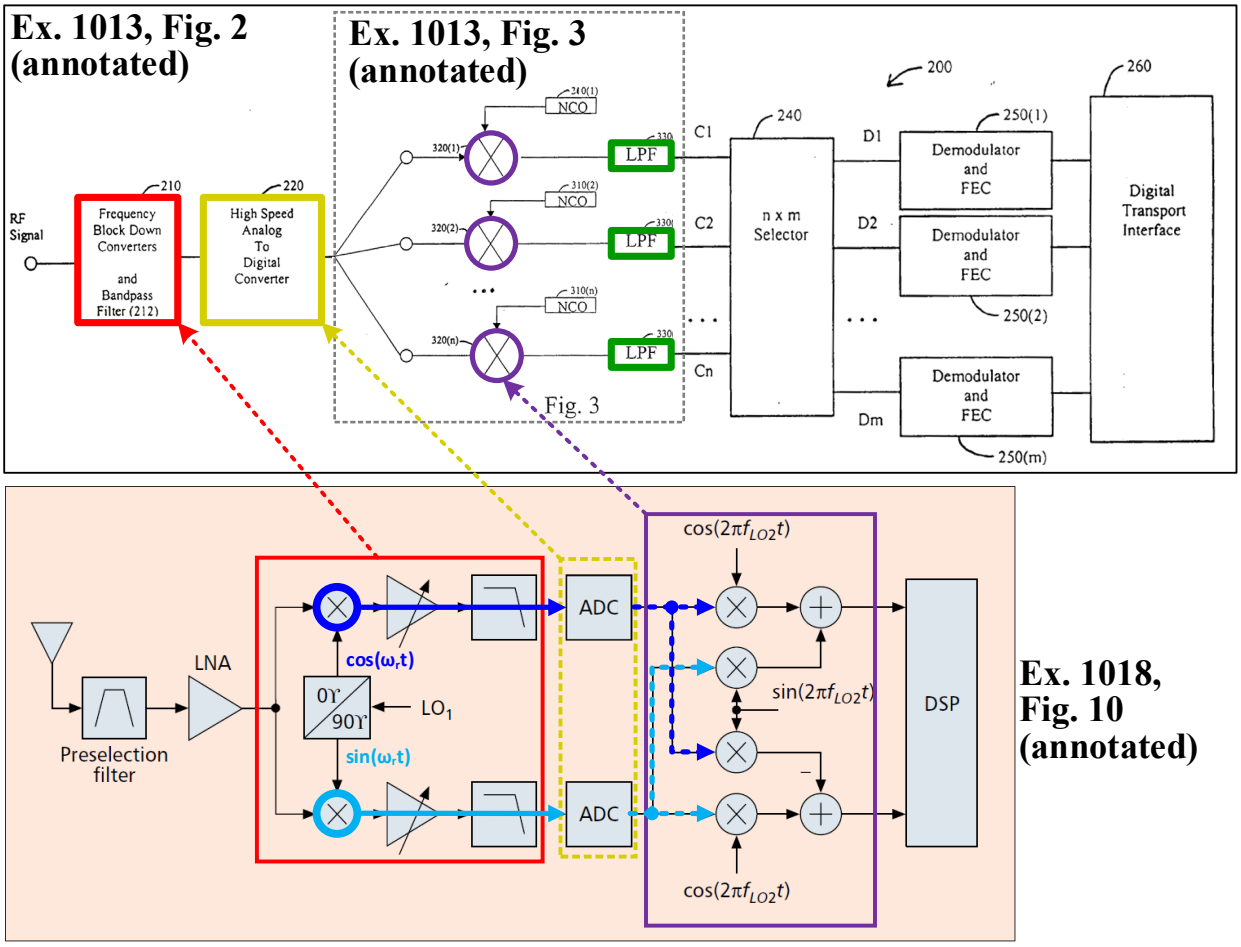


FIG. 3

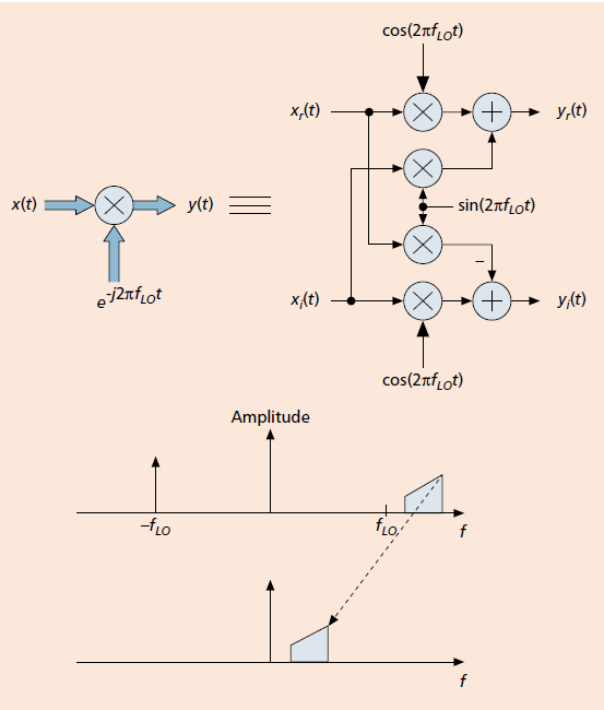
Ex. 1001, Fig. 3 (annotated)

216. Zhang-Mirabbassi as discussed above with respect to claim 6 teaches the same or equivalent structure, with any differences in my view being insubstantial (e.g., multiple parallel paths, each including a complex mixer followed by a low pass filter followed by serial and parallel interfaces as shown in Figures 2 and 3 of Zhang and Figure 2 of the ’362 patent).

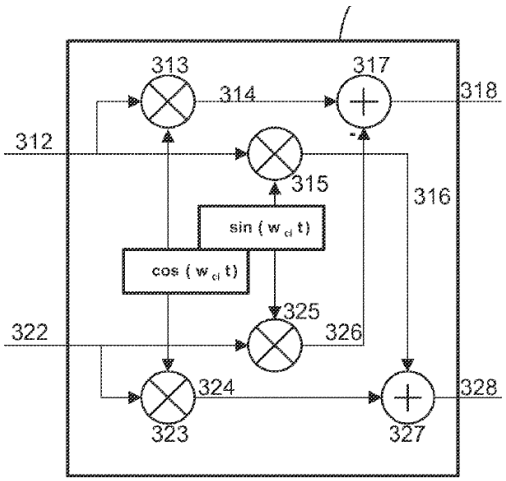


Ex. 1018, Fig. 10 (annotated)

217. Moreover, Mirabbasi's complex mixer has the identical structure and performs the identical downconversion (i.e., shifting the frequency of in-phase and quadrature components of the digital complex input signal) as mixer 300 shown in Figure 3 of the '362 patent. Ex. 1018, pp. 9-10, Fig. 3; Ex. 1001, Fig. 3, 6:7-25, 9:17-22; *see also* Ex. 1025, pp. 279-280; Ex. 1034, p. 63.



Ex. 1018, Fig. 3



Ex. 1001, Fig. 3 (excerpted)

218. In both Zhang-Mirabbasi and the ’362 patent, each path performs the same function of selecting and outputting a respective desired channel, in the same way by first downconverting the respective desired channel to baseband and then low pass filtering with a filter to isolate the channel, to achieve the same result of producing a plurality of desired channels as a digital data stream.

219. Thus, Zhang-Mirabbasi renders claims 1-6 and 8-9 obvious, and Zhang-Mirabbasi-Karabinis renders claim 7 obvious, for the reasons stated above (Sections 9.1.1-3, 9.4.1), and for Zhang-Mirabassi’s further teaching of “digital circuitry” under a means-plus-function construction.

9.6.3. Claims 2 and 3 based on Zhang-Mirabbasi-Pandey (Ground G), and Claim 10 based on Mirabbasi-Jensen (Ground H)

220. The features added for "digital circuitry" to Zhang from Mirabbasi as discussed above with respect to claim 1 (Sections 9.6.2), are independent of the Pandey features (e.g., parallel and serial interfaces) added to Zhang in Ground C (Section 9.2.1) for claims 2 and 3, and the Jensen features (a decimator circuit) added to Zhang in Ground F (Section 9.5) for claim 10. Thus, a POSITA would have added Mirabassi's teachings of a digital circuitry (Sections 9.6.2) to each of these combinations with the same motivations and expectation of success.

221. Thus, Zhang-Pandey-Mirabbasi (ground G) renders claim 2 and 3 obvious, and Zhang-Mirabbasi-Jensen (ground H) renders claim 10 obvious, for the reasons discussed above with respect to each of these claims, and for Mirabbasi's additional teaching of "digital circuitry" under a means-plus-function construction

10. CONCLUSION

222. All of the statements made in this declaration of my own knowledge are true. All statements made based on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Dated: 2/16/2024 By: David B. Lett

David B. Lett

CLAIM LISTING APPENDIX

U.S. Pat. No. 9,210,362

Designation	Claim Language
Claim 1	
[1A]	A wideband receiver system comprising:
[1B]	a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[1C]	a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;
[1D]	digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream
Claim 2	
2	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.
Claim 3	
3	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.
Claim 4	
4	The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.
Claim 5	
[5A]	The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises:
[5B]	a first ADC configured to generate a digital in-phase signal; and
[5C]	a second ADC configured to generate a digital quadrature signal.
Claim 6	

Designation	Claim Language
6	The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.
Claim 7	
[7A]	The wideband receiver system of claim 6, wherein:
[7B]	prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[7C]	after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 8	
8	The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.
Claim 9	
9	The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 10	
10	The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.
Claim 11	
[11A]	A method comprising: in a wideband receiver system:
[11B]	downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[11C]	digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;

Designation	Claim Language
[11D]	selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and
[11E]	outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.
Claim 12	
12	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.
Claim 13	
13	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.
Claim 14	
[14A]	The method of claim 11, comprising:
[14B]	generating, by a first mixer of said mixer module, an in-phase signal; and
[14C]	generating, by a second mixer of said mixer module, a quadrature signal.
Claim 15	
[15A]	The method of claim 11, comprising:
[15B]	generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and
[15C]	generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.
Claim 16	
16	The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.
Claim 17	
[17A]	The method of claim 16, wherein:
[17B]	prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[17C]	after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 18	

Designation	Claim Language
18	The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.
Claim 19	
19	The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 20	
20	The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.