

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner,

v.

ENTROPIC COMMUNICATIONS, LLC.,
Patent Owner.

Patent No. 9,210,362
Filing Date: February 5, 2015
Issue Date: December 8, 2015
Title: WIDEBAND TUNER ARCHITECTURE

Inter Partes Review No.: IPR2024-00433

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

TABLE OF CONTENTS

MANDATORY NOTICES.....	viii
I. INTRODUCTION	1
II. SUMMARY OF ARGUMENT.....	1
III. OVERVIEW OF THE '362 PATENT	2
A. Brief Description	2
B. Prosecution History	7
C. Earliest Priority Date for the Claims	8
IV. OVERVIEW OF PRIOR ART	8
A. Petrovic.....	8
1. Petrovic Priority Date	13
2. Pre-AIA 35 U.S.C. § 103(c) Does Not Apply	14
B. Eidson.....	14
C. Rabaey	16
D. Jensen	17
E. Takahiko.....	18
V. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b).....	19
A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based	19
B. 314(a) Discretion Does Not Apply.....	20
C. 325(d) Discretion Does Not Apply	21
D. Level of Ordinary Skill	21
E. Claim Construction.....	22
1. “digitizing,” “selecting,” “outputting”	22
2. “wideband” and “wideband analog-to-digital converter (ADC) module”	22
3. “digital circuitry”	23
VI. SPECIFIC GROUNDS FOR UNPATENTABILITY	23

A.	Petrovic-Eidson (Claims 1, 4-8, 11, 14-18)	23
1.	Independent Claim 1	24
2.	Claim 4	39
3.	Claim 5	41
4.	Claim 6	43
5.	Claim 7	45
6.	Claim 8	50
7.	Claim 11	52
8.	Claims 14-17	53
9.	Claim 18	54
B.	Petrovic-Takahiko-Eidson (Claims 1, 4-8, 11, 14-18).....	54
1.	Independent Claim 1	54
2.	Claims 4-7	57
3.	Claim 8	58
4.	Independent Claim 11	58
5.	Claims 14-17	58
6.	Claim 18	59
C.	Petrovic-Eidson-Rabaey (Claims 2-3, 12-13).....	59
1.	Claims 2-3	59
2.	Claims 12-13	64
D.	Petrovic-Takahiko-Eidson-Rabaey (Claims 2-3, 12-13)	64
E.	Petrovic-Eidson-Jensen (Claims 9-10, 19-20)	64
1.	Claim 9	65
2.	Claim 10	66
3.	Claim 19	68
4.	Claim 20	68
F.	Petrovic-Takahiko-Eidson-Jensen (Claims 9-10, 19-20).....	69
1.	Claims 9, 19	69
2.	Claims 10, 20	69

VII. GROUNDS FOR STANDING & FEE PAYMENT	70
VIII. CONCLUSION.....	70
CERTIFICATION UNDER 37 CFR § 42.24(d)	71
CERTIFICATE OF SERVICE	72
CLAIM LISTING APPENDIX	73

EXHIBITS

- Ex. 1101: U.S. Patent No. 9,210,362 (“the ’362 patent”)
- Ex. 1102: Expert Declaration of David B. Lett
- Ex. 1103: Curriculum Vitae of David B. Lett
- Ex. 1104: Certified Prosecution History of the ’362 patent
- Exs. 1105-1106: Reserved
- Ex. 1107: Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“’526 provisional”)
- Ex. 1108: U.S. Pub. No. 2009/0290659 (“Petrovic”)
- Ex. 1109: Certified Prosecution History of U.S. Provisional App. No. 61/054,886 (“Petrovic ’886”)
- Ex. 1110: U.S.P.T.O Assignment Record for U.S. Application No. 12/414,892
- Ex. 1111: Reserved
- Ex. 1112: U.S. Patent No. 7,783,958 (“Eidson”)
- Ex. 1113: Reserved
- Ex. 1114: U.S. Patent No. 7,237,214 (“Pandey”)
- Ex. 1115: Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)
- Ex. 1116: Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
- Ex. 1117: A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)

- Ex. 1118: S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
- Ex. 1119: U.S. Patent No. 6,061,406 (“Carson”)
- Ex. 1120: Reserved
- Ex. 1121: Data-Over-Cable Service Interface Specifications, DOCSIS 2.0, Radio Frequency Interface Specification, CM-SP-RFv2.0-I11-060602
- Ex. 1122: Certified File History (as of February 2, 2024) for *Ex Parte* Reexamination No. 90/019,255
- Exs. 1123-1124: Reserved
- Ex. 1125: J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
- Ex. 1126: U.S. Pub. No. 2007/0027943 (“Jensen”)
- Ex. 1127: U.S. Patents and Patent Applications Family Tree for U.S. Pat. 9,210,362
- Ex. 1128: Reserved
- Ex. 1129: Entropic Communications, LLC v. Charter Communications, Inc., No. 2:22-cv-00125-JRG (E.D. Tex. June 26, 2023) (Claim Construction Memorandum Opinion and Order)
- Exs. 1130-1132: Reserved
- Ex. 1133: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2nd ed. 2004) (“Ciciora”)
- Ex. 1134: Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)

- Ex. 1135: U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
- Ex. 1136: U.S. Pub. No. 2003/0217362 (“Summers”)
- Ex. 1137: U.S. Pub. No. 2006/0256799 (“Eng”)
- Ex. 1138: U.S. Pub. No. 2006/0083335 (“Seendripu”)
- Ex. 1139: Excerpts of Chris Bowick, “RF Circuit Design” (2nd ed. 2008)
- Ex. 1140: U.S. Pub. No. 2006/0031894 (“Petruzzelli”)
- Ex. 1141: Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)
- Ex. 1142: U.S. Patent No. 7,272,375 (“Tuttle”)
- Ex. 1143: U.S. Patent No. 7,130,576 (“Gurantz”)
- Ex. 1144: U.S. Patent No. 5,278,837 (“Kelley”)
- Ex. 1145: Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)
- Ex. 1146: U.S. Patent No. 7,213,042 (“Cannon”)
- Ex. 1147: Reserved
- Ex. 1148: Excerpts of William Buchanan, “Computer Busses” (2000) (“Buchanan”)
- Ex. 1149: U.S. Patent No. 7,079,528 (“Ziegler”)
- Ex. 1150: Excerpts of “Software Defined Radio: Enabling Technologies” (Walter H.W. Tuttlebee ed., 2003)
- Exs. 1151-1153: Reserved
- Ex. 1154: U.S. Pub. No. 2003/0220072 (“Coffin”)
- Ex. 1155: U.S. Patent No. 6,493,873 (“Williams”)

- Ex. 1156: U.S. Pub. No. 2007/0053314 (“Gat”)
- Exs. 1157-1160: Reserved
- Ex. 1161: U.S. Pub. No. 2006/0256216 (“Takahiko”)
- Exs. 1162-1169: Reserved
- Ex. 1170: U.S.P.T.O Assignment Record for U.S. Patent No. 8,526,898
- Ex. 1171: U.S.P.T.O Assignment Record for U.S. Patent No. 7,783,958 (“Eidson”)
- Ex. 1172: Reserved
- Ex. 1173: Expert Declaration of Dr. Sylvia Hall-Ellis
- Ex. 1174: Reserved
- Ex. 1175: U.S. Patent No. 6,791,995 (“Azenkot”)
- Ex. 1176: U.S. Patent No. 6,542,203 (“Shadwell”)

MANDATORY NOTICES

Real Parties in Interest (37 C.F.R. § 42.8(b)(1))

The real parties-in-interest for this petition are (i) Comcast Corporation, (ii) Comcast Cable Communications, LLC, and (iii) Comcast Cable Communications Management, LLC. No unnamed entity is funding, controlling, or directing this Petition for *inter partes* review (IPR) of U.S. Patent No. 9,210,362 (“the ’362 patent”), or otherwise has an opportunity to control or direct this Petition or Petitioner’s participation in any resulting IPR.

Related Matters (37 C.F.R. § 42.8(b)(2))

Office Proceedings

This is the second of three petitions for *inter partes* review filed by Petitioner against the ’362 patent. Petitioner is also filing petitions for *inter partes* review against related U.S. Patent Nos. 11,381,866 and 11,399,206.

According to the Office’s records, a request for *ex parte* reexamination (Control No. 90/019,255) was filed September 20, 2023 for claims 1 and 11 of the ’362 patent, and an Order granting the request was issued on November 1, 2023. The requestor of the *ex parte* reexamination, Unified Patents, LLC, is not a real party-in-interest for this petition.

No other Office proceedings (e.g., *inter partes* review, post-grant review, or covered business method) have been filed against the ’362 patent.

Litigation matters

The '362 patent has been asserted in *Entropic Communications, LLC v. Comcast Corporation*, No. 2:23-cv-01050 (C.D. Cal. filed Feb. 10, 2023) and *Entropic Communications, LLC v. Cox Communications, Inc.*, No. 2-23-cv-01049 (C.D. Cal. filed Feb. 10, 2023). These cases have been consolidated and remain pending. The '362 patent was also asserted in *Entropic Communications, LLC v. Charter Communications, Inc.*, No. 2:22-cv-00125-JRG (E.D. Tex. filed Apr. 27, 2022), which was dismissed on December 10, 2023.

Continuity

According to Office records, the '362 patent is a continuation of U.S. Pat. App. No. 13/962,871, filed August 8, 2013 (issued as U.S. Pat. No. 9,100,622), which is a continuation of U.S. Pat. App. No. 12/762,900, filed April 19, 2010 (issued as U.S. Pat. No. 8,526,898), which claims the benefit of U.S. Provisional App. No. 61/170,526, filed April 17, 2009. The '362 patent is part of a family that includes thirteen additional patents or applications that purport to claim priority, via a chain of continuation applications, from App. No. 12/762,900. A family tree is included as Ex. 1127.

Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

<u>Lead Counsel</u>	<u>Back-Up Counsel</u>
Frederic M. Meeker (Reg. No. 35,282) fmeeker@bannerwitcoff.com	Michael S .CuvIELlo (Reg. No. 59,255) mcuviello@bannerwitcoff.com
BANNER & WITCOFF, LTD. 1100 13th Street, NW Suite 1200 Washington, DC 20005 Tel: (202) 824-3000 Fax: (202) 824-3001	H. Wayne Porter (Reg. No. 42,084) wporter@bannerwitcoff.com
	Paul T. Qualey (Reg. No. 45,027) pqualey@bannerwitcoff.com
	Joshua L. Davenport (Reg. No. 72,756) jdavenport@bannerwitcoff.com
	BANNER & WITCOFF, LTD. 1100 13th Street, NW Suite 1200 Washington, DC 20005 Tel: (202) 824-3000 Fax: (202) 824-3001

Please address all correspondence to counsel at the address shown above.

Petitioner consents to electronic service by email at the above email addresses and at ComcastIPRService@bannerwitcoff.com.

I. INTRODUCTION

Comcast Cable Communications, LLC (“Petitioner”) petitions for *inter partes* review and cancellation of claims 1-20 of U.S. Patent No. 9,210,362 (“the ’362 patent”) (Ex. 1101).

II. SUMMARY OF ARGUMENT

The ’362 patent generally claims a wideband receiver system and a corresponding method of operating such a system to select and output a plurality of television channels. The system includes a mixer module that downconverts a plurality of frequencies that include desired and undesired television channels, a wideband analog-to-digital converter (ADC) module that digitizes the plurality of frequencies, and digital circuitry that selects the desired channels from the digitized frequencies and outputs the selected channels as a digital data stream to a demodulator.

The ’362 patent admits that its disclosure of a mixer module, an ADC module, and other elements on the analog side of the wideband receiver system “is similar to conventional tuners.” Ex. 1107, p. 5; Ex. 1101, 1:5-11. The alleged inventive concept—demodulating multiple television channels from the digitized plurality of frequencies—simply utilizes identical copies of well-known digital circuitry for demodulating each channel. These features, and additional features of the ’362

patent claims, are disclosed or rendered obvious by the prior art, e.g., Petrovic (Ex. 1108), Eidson (Ex. 1112), and other references relied on herein.

Accordingly, as set forth below, claims 1-20 of the '362 patent are unpatentable and should be cancelled.

III. OVERVIEW OF THE '362 PATENT

A. Brief Description

The '362 patent describes a wideband receiver system 200 “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1101, 1:15-18; Ex. 1102, ¶ 36. The system purports to group the desired channels that extend over non-contiguous portions of the frequency spectrum “into a contiguous, or substantially-contiguous, frequency spectrum” to “increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator.” Ex. 1101, 1:18-23, 2:24-27. According to the '362 patent, a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” *Id.*, 1:24-27. Figure 2 is a “schematic block diagram of a wideband receiver system 200.” *Id.*, 4:16-18; Ex. 1102, ¶ 37.

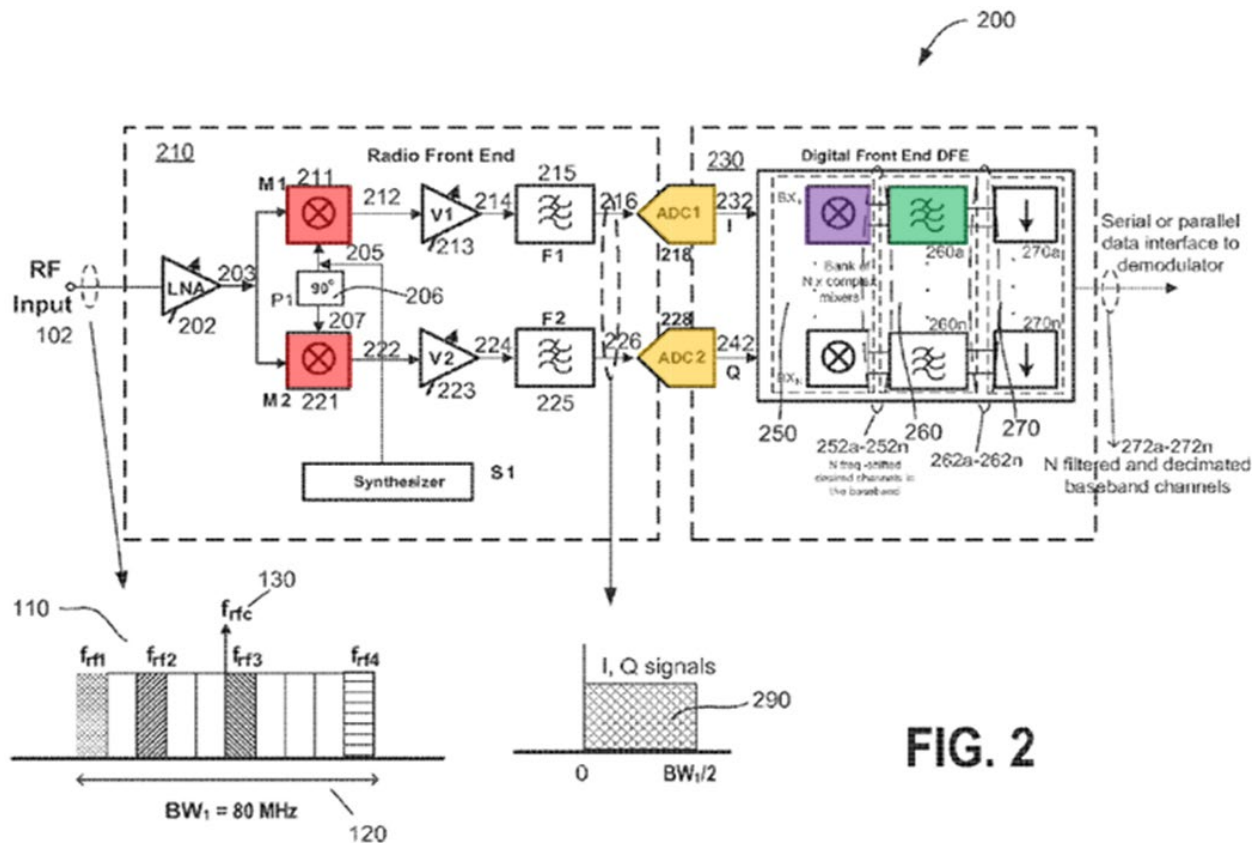


FIG. 2

Ex. 1101, Fig. 2 (annotated)

The wideband receiver system 200 receives both desired and undesired television channels as frequencies dispersed within a frequency bandwidth BW_1 . Ex. 1101, Abstract, 4:19-22. Mixers “M1” and “M2” (red) “generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90° degree [sic] between them” and that have been downconverted to “the baseband or low intermediate

frequency (IF) band.”¹ Ex. 1101, 4:40-46, 2:45-49, *see also* 1:60-62. “[U]nwanted frequency components” are filtered from the in-phase signal and quadrature signals by respective filters 215 and 225. Ex. 1101, 4:64-5:3. The filtered signals are then individually digitized by wideband analog-to-digital converters ADC1 and ADC2 (**gold**) to generate a digital in-phase (I) signal 232 and a digital quadrature (Q) signal 242. Ex. 1101, 2:49-51, 5:28-31. U.S. Provisional App. No. 61/170,526 (“the ’526 provisional”), which the ’362 patent incorporates by reference, admits that the left side of Figure 2 (up to and including ADC1 and ADC2) “is similar to conventional tuners.” Ex. 1107, p. 5; Ex. 1101, 1:5-11; Ex. 1102, ¶ 38.

The digital I and Q signals 232 and 242 are input to a digital front end 230, containing a bank of N complex mixers 250 (one of which is shown above in

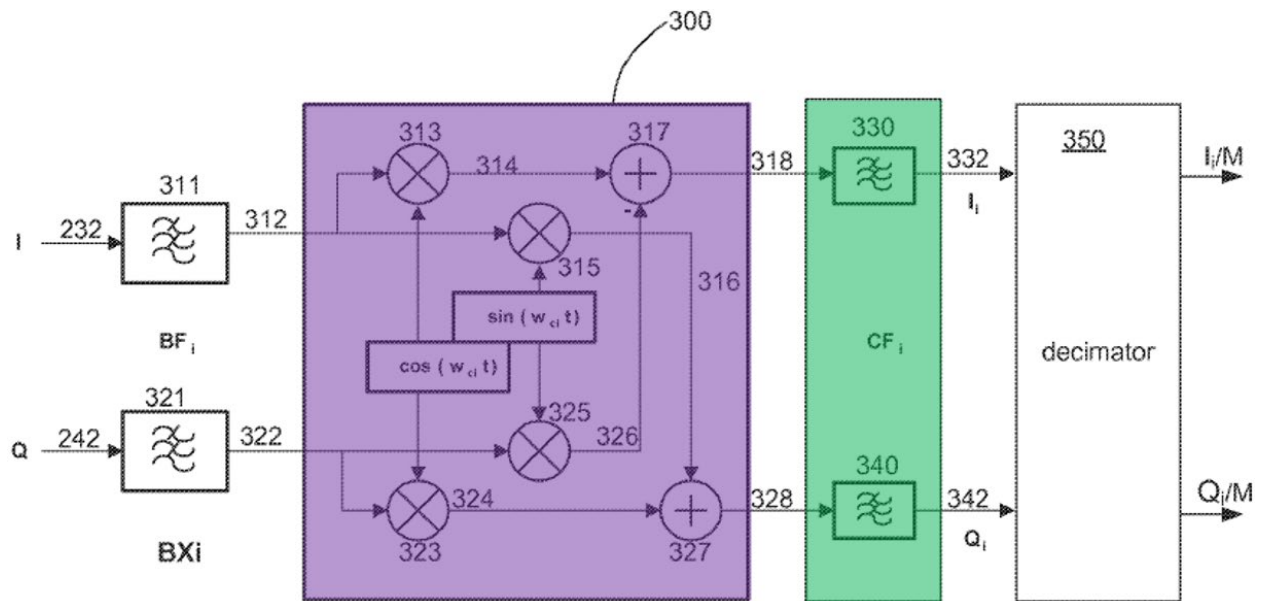
¹ A mixer multiplies an input signal (frequency f_1) by a reference signal (frequency f_2) to produce new signals at the sum and difference frequencies (f_1+f_2 and f_1-f_2). Ex. 1102, ¶¶ 38, 66. The reduced frequency (f_1-f_2) version is output as the “down converted” complex signal with real (I) and imaginary (Q) components. Ex. 1102, ¶¶ 38, 67.

purple), where N is “the number of desired RF channels.”² Ex. 1101, 5:31-35. “Each of the N complex mixers ... extract[s] a different one of the desired channels” from the I and Q signals 232 and 242 and “frequency-shifts the extracted signals to the baseband frequency.”³ Ex. 1101, 5:49-52. The output of each mixer 250 leads to an associated filter module 260 (one of which is shown above in green), which filters the frequency-shifted desired channel. Ex. 1101, 5:52-54; Ex. 1102, ¶ 39.

Figure 3 “is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230” and shows the elements in one of the rows of digital front end 230 in Figure 2. Ex. 1101, 5:62-64; Ex. 1102, ¶ 40.

² Complex mixers multiply signals already separated into their complex I and Q components. Ex. 1102, ¶ 66.

³ Signals have a center frequency f that is modulated with data. Shifting the signal to baseband reduces f to zero, leaving only the modulated data as the output. Ex. 1102, ¶¶ 63-64, 69.



Ex. 1101, Fig. 3 (annotated)

Mixer 300 (**purple**) represents one of the complex mixers 250 and has multipliers 313, 315, 323, and 325 and adders 317 and 327. Ex. 1101, 6:7-17. “[C]omplex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain” by multiplying the I and Q signals by a frequency ω_{ci} that is “chosen [so] that each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband.” Ex. 1101, 6:17-34. Filters 330 and 340 (**green**), “one of the filters 260a-n” shown in Figure 2, filter baseband signals 318 and 328. Ex. 1101, 6:43-45; Ex. 1102, ¶ 41. This exact structure was a conventional design, simply copied multiple times to downconvert multiple channels, respectively. *See e.g.*, Ex. 1102, ¶¶ 64-69.

After decimation, “the N desired baseband channels” are sent “to a demodulator using a serial or parallel data interface according to commonly known methods.” Ex. 1101, 6:55-58; Ex. 1102, ¶ 42.

B. Prosecution History

U.S. Application No. 14/614,543 (“the ’543 application”), which became the ’362 patent, was filed on February 5, 2015, with 20 claims including independent claims 1 and 11. Ex. 1104, pp. 2-35. Following a nonstatutory double patenting rejection over claims 1-27 of U.S. Patent No. 8,526,898, Applicant filed a terminal disclaimer. Ex. 1104, pp. 75-79, 90-99. A Notice of Allowance issued indicating that the prior art failed to describe a wideband receiver system with “digital circuitry configured to select a plurality of desired television channels from the digitized plurality of frequencies and output said plurality of television channels to a demodulator as a digital datastream.” Ex. 1104, pp. 102-108. Following a Request for Continued Examination (RCE) and an Information Disclosure Statement (IDS) (Ex. 1104, pp. 115-140), a second Notice of Allowance issued. Ex. 1104, pp. 141-147. None of Petrovic, Eidson, Rabaey, Jensen, or Takahiko was considered during prosecution of the ’543 application. Ex. 1101, cover; Ex. 1102, ¶ 45.

The Office ordered reexamination (Control No. 90/019,255) of independent claims 1 and 11 of the ’362 patent on November 1, 2023. Ex. 1122, pp. 732-743.

The reexamination is currently pending. None of Petrovic, Eidson, Rabaey, Jensen, or Takahiko has been cited in the reexamination. Ex. 1122, *passim*; Ex. 1102, ¶ 46.

C. Earliest Priority Date for the Claims

The earliest possible priority date for claims 1-8, 10-18, and 20 of the '362 patent is April 17, 2009, the filing date of the '526 provisional. Each of the references relied on herein is prior art to that date. Ex. 1102, ¶ 47. The earliest possible priority date for claims 9 and 19 is April 19, 2010, the filing date of Application No. 12/762,900, as the '526 provisional is silent regarding a “finite impulse response filter.” Ex. 1107, pp. 3-7; Ex. 1102, ¶ 47.

IV. OVERVIEW OF PRIOR ART

A. Petrovic

Petrovic (Ex. 1108) is a U.S. Patent Application Publication of Application No. 12/414,892, filed March 31, 2009, that claims priority to and incorporates by reference U.S. Provisional Application 61/054,886 (“Petrovic '886”, Ex. 1109⁴) in its entirety. Ex. 1108, cover, [0001]. As explained below, Petrovic is prior art under pre-AIA 35 U.S.C. § 102(e) as of the Petrovic '886 filing date of May 21, 2008. Ex. 1102, ¶¶ 78-79.

⁴ The specification and drawings of Petrovic '886, cited by paragraph and Figure numbers, are at pages 6-61 of Ex. 1109.

Petrovic, like the '362 patent, describes a wideband receiver system that it calls “channel stacking system 100” and that “assemble[s] channels resident within an RF signal into a composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box.” Ex. 1108, [0028]; Ex. 1109, [0008]; Ex. 1102, ¶ 80. Petrovic’s system 100 is shown below with color annotations to match corresponding features of the '362 patent drawings in Section III.A. Ex. 1108, [0028]; Ex. 1109, [0008], Fig. 1; Ex. 1102, ¶ 80.

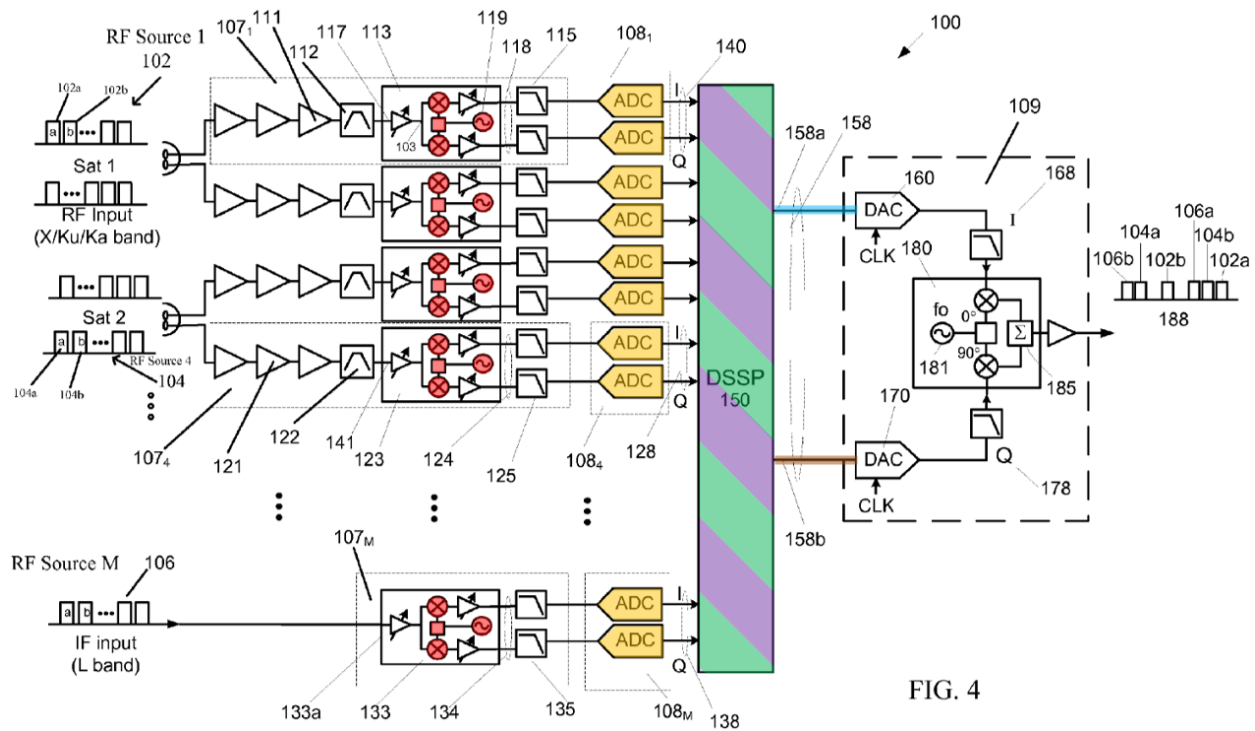


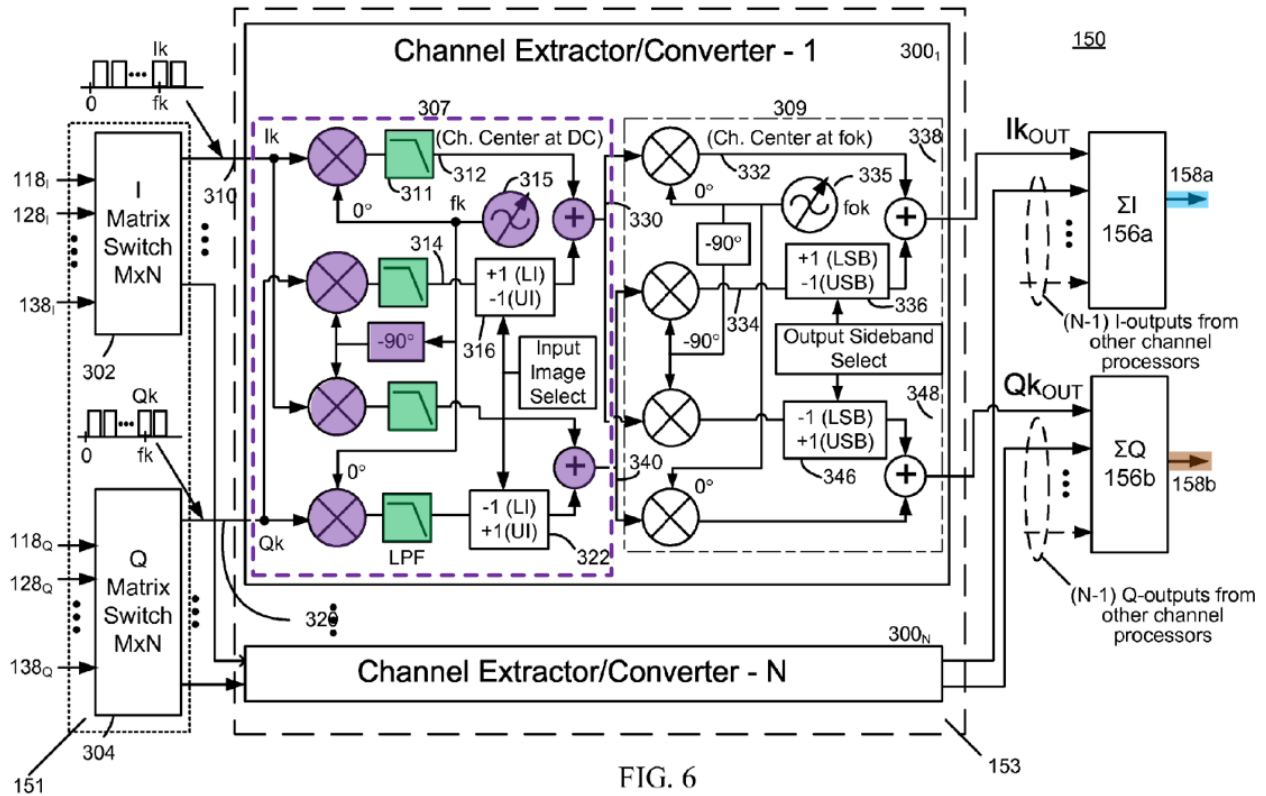
FIG. 4

Ex. 1108, Fig. 4 (annotated)

The system 100 receives signals 102-106 from a plurality of RF sources, such as satellites. Ex. 1108, [0029], Fig. 4; Ex. 1109, [0010]-[0013], [0016], [0023],

[0026], Fig. 1; Ex. 1102, ¶ 81. Each of those signals is wideband, as it may comprise multiple channels. Ex. 1108, [0029], Fig. 4; Ex. 1109, [0016], Fig. 1; Ex. 1102, ¶ 81. The signals 102-106 are coupled to respective “analog preprocessing and downconversion (APD) stages 107_{I-M}.” Ex. 1108, [0032], Fig. 4; Ex. 1109, [0010], [0013], [0020], Fig. 1; Ex. 1102, ¶ 81. Each of those APD stages includes a downconverter (**red**), that downconverts an RF signal into in-phase (I) and quadrature (Q) intermediate frequency (IF) signals. Ex. 1108, [0032]-[0038], Figs. 4-6; Ex. 1109, [0010], [0013], [0018]-[0023], [0031], [0032], Figs. 1-3A; Ex. 1102, ¶ 81. The downconverted I and Q signals are filtered and then converted to digital form in analog-to-digital converters 108_{I-M}, (**gold**). Ex. 1108, [0032], [0039], Fig. 4; Ex. 1109, [0010], [0013], [0018]-[0020], [0022], [0024], Fig. 1; Ex. 1102, ¶ 81.

A digital signal switching and pre-processing (DSSP) stage 150 (**green/purple**) receives the digitized signals and “extract[s] the channels of interest ... (i.e., remove[s] all of the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1; Ex. 1102, ¶ 82. The DSSP 150 outputs those channels as a composite signal with in-phase and quadrature components 158a (**blue**) and 158b (**brown**). Figure 6 shows additional details of the DSSP 150, which may include “channel extractor/converter circuit 300.” Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 82.



Ex. 1108, Fig. 6 (annotated)

Similar to the '362 patent, a channel is extracted from the digitized I and Q signals corresponding to one of the RF sources 102-106 by downconverting those signals to baseband in a complex mixer (purple and/or purple broken-line box) of a stage 307, and filtering using low pass filters 311 (green). Ex. 1108, [0060]-[0070]; Ex. 1109, [0037]-[0054]; Ex. 1102, ¶ 83. The frequency f_k used for the downconversion to baseband (much like frequency ω_{ci} in the '362 patent) is selected based on a frequency corresponding to a desired channel. Ex. 1108, [0066]; Ex. 1109, [0045]; Ex. 1102, ¶ 83.

The I and Q signals 330 and 340 of the extracted channel are upconverted to a desired output frequency in the stage 309, and then summed with other upconverted channels (from stages 309 of other channel/extractor converters) in combiners 156a and 156b to result in the I and Q signals 158a and 158b. Ex. 1108, [0078]-[0086]; Ex. 1109 [0055]-[0061]; Ex. 1102, ¶ 84.

Petrovic is in the same field of endeavor as the '362 patent, and thus is analogous art. Ex. 1102, ¶ 85. For example, and like the '362 patent, which “relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum,” Petrovic relates to a system and method for receiving a wideband radio frequency signal comprising multiple channels. Ex. 1101, 1:15-18; Ex. 1108, [0029], Fig. 4; Ex. 1109, [0010]-[0011], [0013], [0016], [0020], [0023], Fig. 1; Ex. 1102, ¶ 85. Petrovic is also reasonably pertinent to problems with which the '362 is concerned, and is also analogous art on that basis. Ex. 1102, ¶ 85. For example, Petrovic describes selecting individual channels by conversion to baseband and filtering in the same way as is described by the '362 patent. Ex. 1101, 5:62-6:54, Fig. 3; Ex. 1108, [0042], [0058]-[0077], Fig. 6; Ex. 1109, [0036]-[0054], Fig. 3A; Ex. 1102, ¶ 85.

1. Petrovic Priority Date

Petrovic is pre-AIA 35 U.S.C. § 102(e) prior art based on its March 31, 2009, filing date, and based on the May 21, 2008, filing date of Petrovic '886. At least claim 14 of Petrovic is supported by Petrovic '886. Ex. 1102, ¶¶ 86-87; *see Dynamic Drinkware, LLC v. National Graphics, Inc.*, 800 F.3d 1375, 1381 (Fed. Cir. 2015).

Petrovic – Claim 14	Petrovic '886
14. A method for assembling channels in a composite signal, the method comprising:	<i>E.g.</i> , [0001], [0004], [0008], claim 16.
a) downconverting, in a single frequency translation process, a first input signal comprising a first plurality of channels to a first IF signal comprising said plurality of first channels;	[0005], [0010], [0014], [0029], [0031]-[0032], claim 16, Figs. 1-2
b) converting the first IF signal into a first digital IF signal;	[0010], claim 16, Fig. 1
c) downconverting, in a single frequency translation process, a second input signal comprising a plurality of second channels to a second IF signal comprising said plurality of second channels;	[0005], [0013]-[0014], [0023], [0029], [0031]-[0032], claim 16, Figs. 1-2
d) converting the second IF signal into a second digital IF signal; and	[0005], [0013], [0024], claim 16, Fig.1
e) assembling, in the digital domain, at least one of the first channels and at least one of the second channels into a digital composite signal.	[0015], [0025], [0036]-[0068], [0080] claim 16, Figs. 3A-3B

Parallel citations to Petrovic and Petrovic '886 show that relied-on disclosure is prior art as of the May 21, 2008, filing date of Petrovic '886.

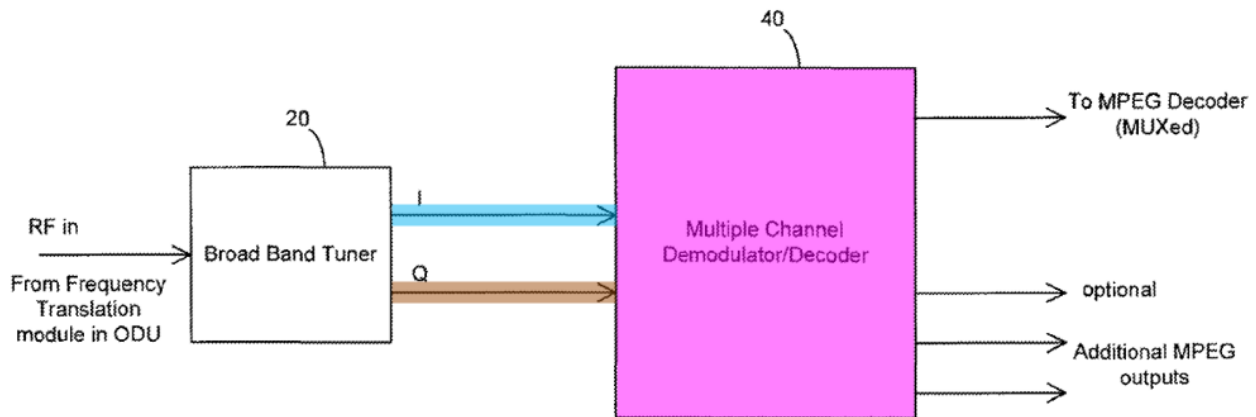
2. Pre-AIA 35 U.S.C. § 103(c) Does Not Apply

Petrovic was assigned to Entropic Communications, Inc. until April 30, 2015. Ex. 1108, cover; Ex. 1110, p. 3. The claimed invention of the '362 patent was not, at the time made, owned by Entropic Communications, Inc. Ex. 1170, pp. 2-5; Ex. 1101, cover. Petrovic cannot be avoided under pre-AIA 35 U.S.C. § 103(c).⁵

B. Eidson

Eidson is a U.S. Patent that issued based on an application filed November 1, 2006. Ex. 1112, cover. Eidson is pre-AIA 35 U.S.C. § 102(e) prior art and describes a multiple-channel receiver that demodulates multiple channels using a multiple channel demodulation and error correction decoding engine. Ex. 1112, Abstract, 8:27-30; Ex. 1102, ¶¶ 88-89. Eidson's Figure 8 "shows a broadband tuner and multi-channel demodulator and decoder". Ex. 1112, 7:58-59; Ex. 1102, ¶ 89.

⁵ Patent Owner has the burden under pre-AIA 35 U.S.C. § 103(c). *Global Tel*Link Corporation v. Securus Technologies, Inc.*, No. IPR2014-00825, Paper 36, at 11 (PTAB Dec. 2, 2015).



Ex. 1112, Fig. 8 (annotated)

A frequency translation module located in an outdoor unit selects desired satellite transponder channels and translates those selected channels to a contiguous section of bandwidth that is received by a broad band tuner 20. Ex. 1112, 8:43-57; Ex. 1102, ¶ 90. The digital outputs of the tuner 20 are I (**blue**) and Q (**brown**) signals that represent multiple selected transponder channels. Ex. 1112, 8:54-57, 9:5-25, Figs. 9-10; Ex. 1102, ¶ 90. As discussed in more detail below, these I and Q signals input to the multiple channel demodulator/decoder 40 (**pink**) are functionally the same as the summed I signal 158a and the summed Q signal 158b output by the Petrovic DSSP 150. Ex. 1102, ¶ 90. In Eidson, the digital I and Q output of the broadband tuner 20 “is processed by a multiple channel demodulator and decoder 40 to produce one or more MPEG streams comprising multiple video programs derived from the selected transponder channels.” Ex. 1112, 8:65-9:2; Ex. 1102, ¶ 90.

Eidson is reasonably pertinent to problems with which the '362 patent is concerned, and is analogous art to the '362 patent on at least that basis. Ex. 1102,

¶ 91. For example, the '362 patent indicates that signals recovered from received RF signals may be output to a demodulator, but leaves the particulars to “commonly known methods.” Ex. 1101, 6:55-58, Fig. 2; Ex. 1102, ¶ 91. A POSITA would consider Eidson, which relates to demodulation of signals for multiple channels, as a pertinent example of those “commonly known methods.” Ex. 1102, ¶ 91.

Eidson was, at all relevant times, assigned to Entropic Communications, Inc. Ex. 1112, cover; Ex. 1171, pp. 3-11. For reasons similar to those set forth in Section IV.A.2, pre-AIA 35 U.S.C. § 103(c) is inapplicable to Eidson.

C. Rabaey

Rabaey is a textbook on digital integrated circuit design. Ex. 1116, *Digital Integrated Circuits; A Design perspective*. Rabaey was published by October 22, 2003, and publicly available to a POSITA by that date, and is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1173, ¶¶ 47-54. Rabaey is reasonably pertinent to problems with which the '362 patent is concerned, and is analogous art to the '362 patent on at least that basis. Ex. 1102, ¶ 92. The '362 patent describes at length how signals may be processed in digital form. Ex. 1101, 5:31-6:65, Figs. 2-3; Ex. 1102, ¶ 92. Integrated circuits were a well-known and widely-used way to implement digital processing in electronics. Ex. 1116, pp. 17 (recognizing “continuous trend towards digital solutions in all other areas of electronics”), 28 (“The purpose of this textbook is to provide a bridge between the abstract vision of digital design and the underlying

digital circuit and its peculiarities”); Ex. 1102, ¶ 92. Rabaey describes the “commonly known methods” of sending “a serial or parallel digital data stream to a demodulator using a serial or parallel data interface” that the ’362 patent refers to and asserts, in claims 2-3 and 12-13, to be part of the purported invention. Ex. 1101, 6:55-58, 11:66-12:2, 12:54-59; Ex. 1102, ¶ 92.

D. Jensen

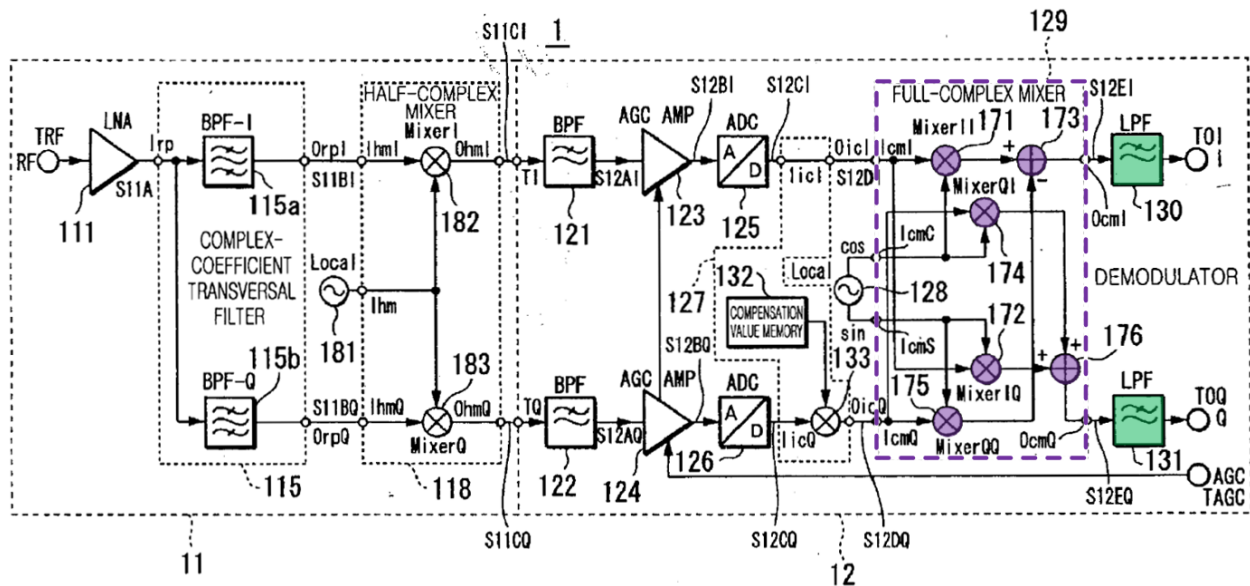
Jensen is a U.S. Patent Application Publication published on February 1, 2007. Ex. 1126, cover. Jensen is pre-AIA 35 U.S.C. § 102(b) prior art. Jensen discloses a channel-select decimation filter for digitally processing signals associated with received RF signals. Ex. 1126, [0023]-[0029], Figs. 1-2; Ex. 1102, ¶ 93. In particular, Jensen (like the ’362 patent) generates downconverted I and Q components of a received RF signal in the analog domain, generates a digital signal based on those I and Q components, baseband converts the digital signal, and then filters the baseband-converted digital signal. *Id.* Jensen explicitly discloses that the filtered baseband-converted digital signals are decimated.⁶ Jensen is reasonably pertinent to problems with which the ’362 patent is concerned, and is analogous art to the ’362 patent on that basis. Ex. 1102, ¶ 93. For example, the ’362 patent

⁶ Decimation is a well-known process that reduces the original sample rate of a signal to a lower rate. Ex. 1102, ¶¶ 73, 92.

describes generating downconverted I and Q components of a received RF signal in the analog domain, digitizing those signals, baseband converting those signals, and then filtering and decimating the baseband-converted digital signals. Ex. 1101, 4:16-6:58, Figs. 2-3; Ex. 1102, ¶¶ 36-42, 93.

E. Takahiko

Takahiko, a November 16, 2006, U.S. Patent Application Publication, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1161, cover. Takahiko discloses a downconverter of a radio receiver that includes a digital baseband complex mixer (purple) and low pass filters (green) similar to those of the '362 patent. Ex. 1161, [0143], [0153], [0156]; Ex. 1102, ¶ 94.



Ex. 1161, Fig. 1 (annotated)

Takahiko, by describing circuits also described by the '362 patent and which are used for similar purposes (reception and tuning of RF signals), is reasonably pertinent to problems with which the '362 patent is concerned, and is analogous art. Ex. 1161, [0143]-[0156], Fig. 1; Ex. 1102, ¶ 95.

V. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based

Petitioner requests review of claims 1-20 on the following grounds.

Ground	References	Basis	Claims Challenged
A	Petrovic-Eidson	§103	1, 4-8, 11, 14-18
B	Petrovic-Takahiko-Eidson	§103	1, 4-8, 11, 14-18
C	Petrovic-Eidson-Rabaey	§103	2, 3, 12, 13
D	Petrovic-Takahiko-Eidson-Rabaey	§103	2, 3, 12, 13
E	Petrovic-Eidson-Jensen	§103	9, 10, 19, 20
F	Petrovic-Takahiko-Eidson-Jensen	§103	9, 10, 19, 20

None of the prior art listed above was before the examiner during prosecution of the '362 patent.

A supporting declaration of David B. Lett includes, e.g., a discussion of Mr. Lett's background, the '362 patent, the prior art, and his opinions, and an explanation

of the bases for those opinions. Ex. 1102, ¶¶ 1-206. Mr. Lett at least meets the level of skill of a POSITA. *Id.*, ¶¶ 4-16, 31; Ex. 1103.

B. 314(a) Discretion Does Not Apply

The *Fintiv* factors as set forth in the Director's June 21, 2022 Guidance Memorandum do not warrant discretionary denial.

Factor one appears neutral. Petitioner has filed IPR petitions challenging all eight patents asserted in the District Court in case no. 2:23-cv-01050. If trial is instituted, and the case is not dismissed based on Petitioner's motion to dismiss the Second Amended Complaint, then Petitioner expects to request a stay, as decisions in Petitioner's favor would resolve the dispute in its entirety.

Factor two favors institution. Petitioner has filed a motion to dismiss the District Court case, Patent Owner has filed an Amended Complaint, and Petitioner will renew its Motion to Dismiss in order to seek dismissal of the operative complaint. In addition, no schedule beyond claim construction has been entered, and the Court has not set a trial date.

Factor three favors institution. To date, the investment by the District Court has been limited to considering motions to dismiss on the pleadings.

Factor four strongly favors institution. The petition challenges all claims in the '362 Patent while only claims 11 and 12 are asserted in the District Court.

Factor five does not warrant denial as Petitioner is a defendant in the District Court case.

Factor six favors institution. Petitioner presents compelling unpatentability challenges that merit institution, relying on entirely different prior art than that considered during prosecution or argued in the pending *ex parte* reexamination.

C. 325(d) Discretion Does Not Apply

Considering the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Pap. 6, *8-9 (PTAB Feb. 13, 2020), the Board should not deny institution. The grounds raised by this Petition are not the same or substantially the same as the art and arguments raised during prosecution, and to the extent that they are, the Examiner erred in a manner material to the patentability of the challenged claims by failing to find and consider all of the relevant prior art, including Petrovic and Eidson, that teach the limitations of the independent and dependent claims.

D. Level of Ordinary Skill

A person of ordinary skill in the art (a “POSITA”) at the time of the alleged invention would have had a degree in electrical engineering, or a similar discipline, along with three-to-four years of experience with digital signal processing (DSP) and RF tuning systems for satellite and/or cable communications. Ex. 1102, ¶¶ 30-

32. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. *Id.*

E. Claim Construction

All claim terms herein should be given their ordinary and customary meaning to a POSITA as they would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b).

1. “digitizing,” “selecting,” “outputting”

In the TX litigation, the District Court construed claim 11 as requiring that the “‘digitizing ...’ step must be performed before the ‘selecting ...’ step, and the ‘selecting ...’ step must be performed before the ‘outputting ...’ step,” but with “[n]o other order of steps” required. Ex. 1129, p. 52.

2. “wideband” and “wideband analog-to-digital converter (ADC) module”

In the TX litigation, Patent Owner agreed that “wideband analog-to-digital converter (ADC) module” should be given its plain and ordinary meaning. Ex. 1129, pp. 7-8. Consistent with its ordinary meaning, the ’362 patent defines “wideband” as a band that carries multiple channels. For example, the ’362 patent states that a

receiver is “wideband” if it is “designed to concurrently receive several TV channels.” Ex. 1101, 1:25-27; Ex. 1102, ¶¶ 33-35.⁷

3. “digital circuitry”

To the extent “digital circuitry” of claim 1 is construed to be a means-plus-function term under 35 U.S.C. 112, paragraph 6, and to the extent the ’362 patent discloses corresponding structure for this limitation, that structure is illustrated in Figures 2 and 3, including complex mixers 250 and 300, and filters 260, 330, and 340. Ex. 1101, Figs. 2-3, 5:31-54, 6:7-58; Ex. 1102, ¶¶ 33-34.

VI. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Petrovic-Eidson (Claims 1, 4-8, 11, 14-18)

As set forth below, claims 1, 4-8, 11, and 14-18 are obvious over Petrovic in view of Eidson. Ex. 1102, ¶¶ 96-169, *see also* ¶¶ 48-77.

⁷ The ’362 Patent also states that “the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum.” Ex. 1101, 1:18-21. “Non-contiguous portions” is omitted from the independent claims and added only in dependent claims 7 and 17, but should they be implicitly required of a “wideband receiver,” Petrovic-Eidson discloses them as presented below.

1. Independent Claim 1

a. [1A] “A wideband receiver system comprising:”

While the preamble [1A]⁸ is not limiting, Petrovic teaches it. Ex. 1102, ¶¶ 98-99. The Petrovic channel stacking system 100 receives signals 102-106 that each occupies a wide portion of RF spectrum bandwidth that includes multiple frequencies and that comprises multiple channels. Ex. 1108, [0028]-[0029], Fig. 4; Ex. 1109, [0005], [0010]-[0011], [0013], [0016], [0020], [0023], Fig. 1; Ex. 1102, ¶ 99. For example, “the total channel bandwidth” of the signal 102 “may be in the range of 100 MHz-5 GHz” and “the number of channels included in any particular received signal 102 may be 4, 6, 8, 16, 24, 28, 32, 40, 48, 60, 120 or more.” Ex. 1108, [0029]; Ex. 1109, [0016]; Ex. 1102, ¶ 99; *see* Ex. 1101, 1:24-27 (describing “wideband” as a band that carries multiple channels); Figs. 2, 6-8; *see* Section V.E.2.

Other Petrovic embodiments are similarly wideband receiver systems. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11; Ex. 1102, ¶ 99.

To the extent that Patent Owner argues that a “wideband receiver system” must receive desired channels in non-contiguous frequency bands, this is also taught

⁸ The limitations of the claims appear and are labelled in the Claims Listing Appendix.

by Petrovic, as explained below for limitation [7A] of claim 7. Ex. 1102, ¶ 99; Section VI.A.5.a.

- b. [1B] “a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”

The mixers (**red**) of any of the individual downconverters (broken red line boxes) shown in Petrovic’s Figure 4, or the mixers of any combination of those downconverters, is a mixer module according to limitation [1B]. Ex. 1102, ¶¶ 100-101; *see also* ¶¶ 48-51, 64-69.

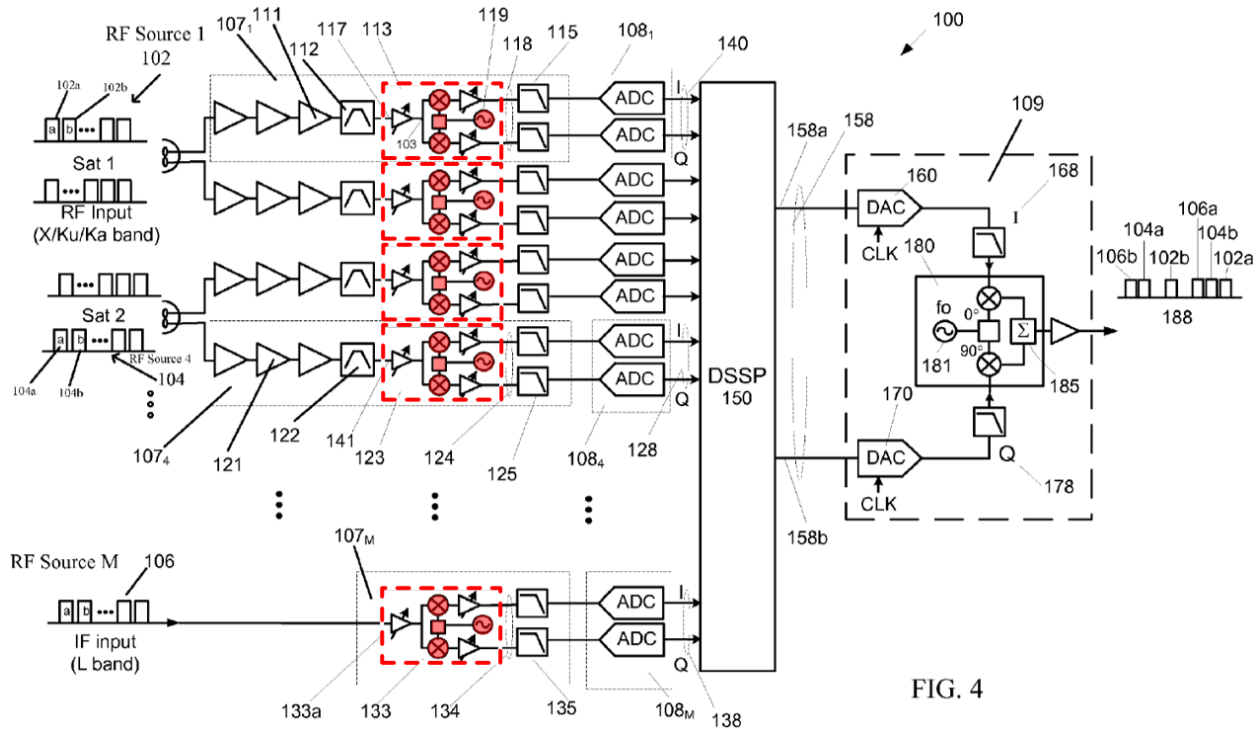


FIG. 4

Ex. 1108, Fig. 4 (annotated)

According to Petrovic, the mixers of a first downconverter 113 downconvert the frequency of the first RF input signal 102 to a first IF signal 118. Likewise, the

mixers of a second downconverter 123 downconvert the second RF input signal 104 to a second analog IF signal 124, and the mixers of a third downconverter 133 downconvert the third RF input signal 106 to a third IF signal 134. Ex. 1108, [0033]-[0034], [0036]-[0037], [0047], [0050], Figs. 4-5; Ex. 1109, [0005], [0010], [0013], [0020], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 102. Moreover, and as explained in Section VI.A.1.a for preamble [1A], each of the RF signals 102-106 downconverted by the mixers of the downconverters 113, 123, and 133 includes multiple channels in multiple frequencies. Ex. 1102, ¶ 102.

A POSITA would have understood those channels to include television channels. Ex. 1102, ¶ 103. For example, Petrovic discloses outputting signals from the channel stacking system 100 “to a rendering device, such as a set-top box, or other receiver/tuner,” which are devices associated with output of television programming to users. Ex. 1108, [0028], [0054]; Ex. 1109, [0008], [0030]; Ex. 1102, ¶ 103. And, because satellite communication was commonly used for transmission of television programming to end users, a POSITA would have been motivated to use the Petrovic channel stacking system 100 in a home satellite reception system for obtaining and outputting television programming. Ex. 1102, ¶ 103 (citing Ex. 1154, Ex. 1155, Ex. 1156).

Petrovic also discloses that the channels in the RF signals 102-106 may include “a plurality of desired channels” and a “plurality of undesired channels” as

claimed in the '362 patent. Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036]; Ex. 1102, ¶ 104. As explained in detail in Section VI.A.1.d for limitation [1D], Petrovic discloses later extracting, or selecting, less than all of the channels included in a received RF signal. Ex. 1108, [0042], [0053], [0055], [0058]; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036], Fig. 1; Ex. 1102, ¶ 104. Consistent with the use of “desired” and “undesired” in the '362 patent, a selected Petrovic channel is desired and an unselected Petrovic channel is undesired. Ex. 1101, Abstract, 1:29-34, 3:9-39, 4:19-33, 5:41-44, 5:49-61, 6:32-42, 6:55-64; Ex. 1102, ¶ 102.

Mixers of downconverters (individually or in combination) of other Petrovic embodiments are similarly mixer modules configured to perform the function recited in limitation [1B]. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11; Ex. 1102, ¶ 105.

c. [1C] “a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”

Any of the Petrovic analog-to-digital converter (ADC) pairs 108_I-108_M (**gold**), or any combination of those ADC pairs, is a wideband ADC module according to limitation [1C]. Ex. 1108, [0039], [0047], [0050]-[0052], Fig. 4; Ex.

1109, [0005], [0010], [0018], [0019], [0022], [0024], [0028], Fig. 1; Ex. 1102, ¶¶ 106-107; *see also* ¶¶ 64-71.

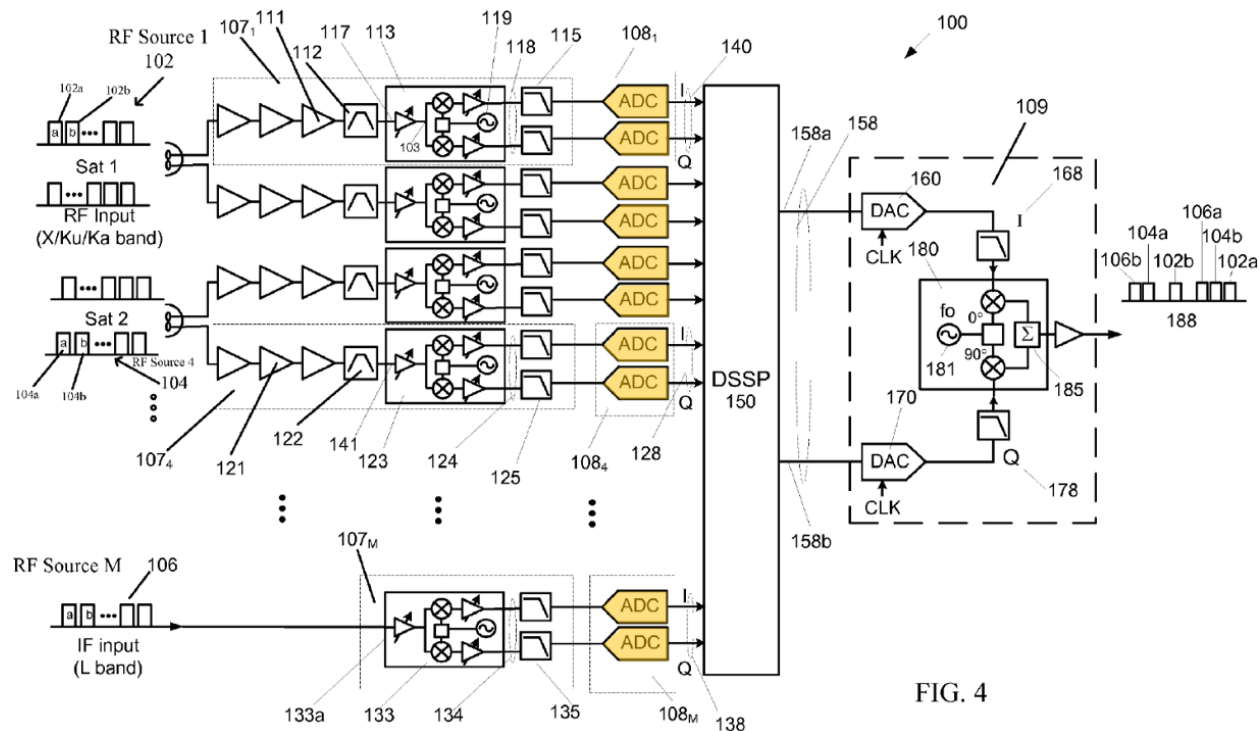


FIG. 4

Ex. 1108, Fig. 4 (annotated)

Each of the ADC pairs 108₁-108_M digitizes a pair of downconverted I and Q signals that include channels (desired and undesired) from a received RF input. E.g., Ex. 1108, Fig. 4; Ex. 1109, Fig. 1; Ex. 1102, ¶ 108. Any of the individual ADC pairs 108₁-108_M shown in Figure 4, or any combination of those ADC pairs, is a wideband ADC module according to limitation [1C]. Ex. 1102, ¶ 108. For example, if the downconverter 113 is treated as the mixer module of limitation [1B], the ADC pair 108₁ digitizes, after filtering in anti-aliasing filters 115, I and Q signals 118 that include channels 102a, 102b, etc., carried in the received RF signal 102. Ex. 1108,

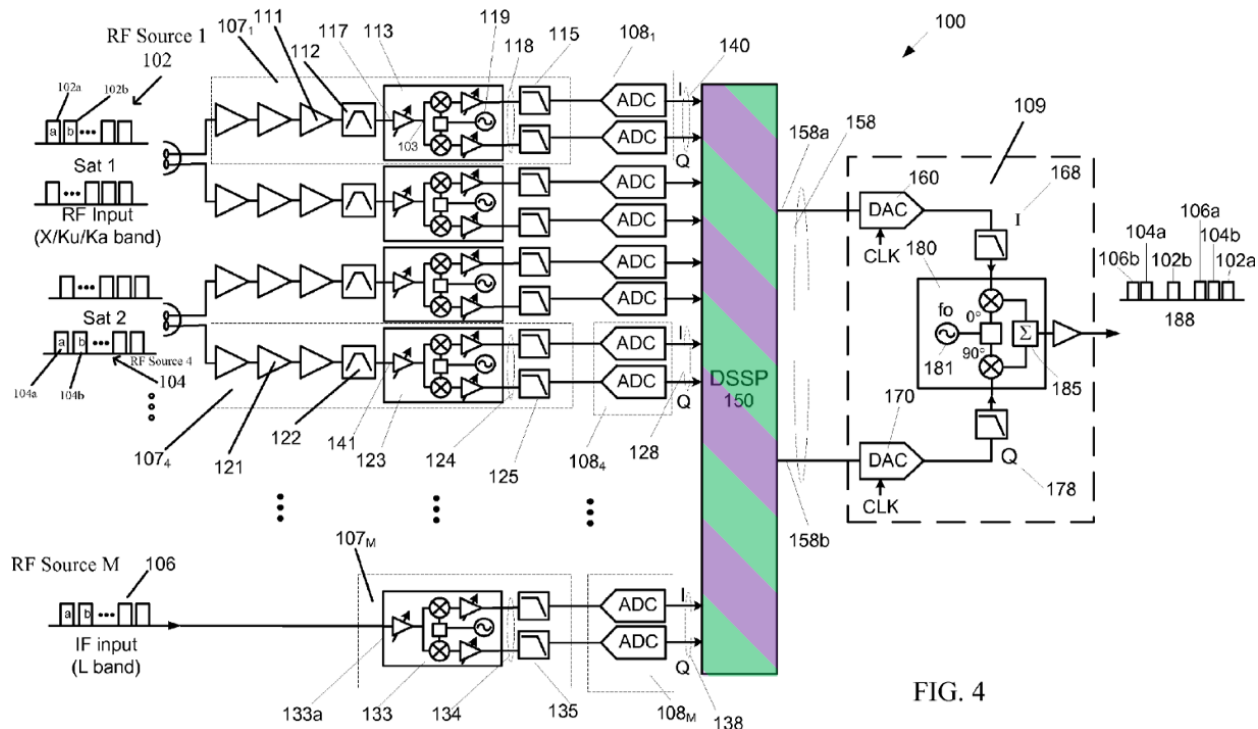
[0033], [0039], Fig. 4; Ex. 1109, [0010], Fig. 1; Ex. 1102, ¶ 108. As another example, and if the downconverter 113 and the downconverter 123 together are treated as the mixer module of limitation [1B], the ADC pair 108₁ and the ADC pair 108₄ collectively digitize, after filtering in anti-aliasing filters 115 and 125, I and Q signals 118 that include channels 102a, 102b, etc., carried in the received RF signal 102, as well as I and Q signals 124 that include the channels 104a, 104b, etc., carried in the received RF signal 104. Ex. 1108, [0033], [0039], [0047], Fig. 4; Ex. 1109, [0010], [0013], [0023]-[0024], Fig. 1; Ex. 1102, ¶ 108.

ADC pairs (individually or in combination) of other Petrovic embodiments are similarly ADC modules configured to perform the functions recited in limitation [1C]. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11; Ex. 1102, ¶ 109.

- d. [1D] “digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.”**

Petrovic in view of Eidson discloses limitation [1D]. A Digital Signal Switching and Preprocessing (DSSP) stage 150 (**green/purple**) of the Petrovic channel stacking system 100 is digital circuitry that selects desired television channels from digitized frequencies (i.e., from the digitized signals received from the ADC pairs 108₁-108_M). Ex. 1108, [0042], [0053], [0058]-[0077], Figs. 4, 6; Ex.

1109, [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025], [0033], [0037]-[0054], Fig. 1; Ex. 1102, ¶¶ 110-111; *see also* ¶¶ 70-71.



Ex. 1108, Fig. 4 (annotated)

As explained in Section VI.A.1.c for limitation [1C], and as can be seen in Figure 4, each of the ADC pairs 108₁-108_M digitizes a pair of downconverted I and Q signals that include channels (desired and undesired) from a received RF input. Ex. 1102, ¶ 112. The DSSP 150 comprises “channel extraction stages” that “extract [i.e., select] the channels of interest [i.e., desired channels]” from the signals received from the ADC pairs 108₁-108_M and that “remove all of the channels that are not of interest,” i.e., the claimed “undesired channels”. Ex. 1108, [0042], [0053],

[0055], [0058], Figs. 4, 6; Ex. 1109, [0003], [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025] (digital signal processor 150 “assemble[s] a composite signal 158 having the desired channels”), [0033] (channel extractor/converter circuits of digital signal processor 150 “extract a desired channel”), [0036], Fig. 1; Ex. 1102, ¶ 112. DSSPs of other Petrovic embodiments are similarly digital circuitry configured to select a plurality of desired television channels from a digitized plurality of frequencies. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11; Ex. 1102, ¶ 112.

Indeed, Petrovic describes the same selection technique described by the ’362 patent. *Compare* Ex. 1101, 5:62-6:54 (describing a frequency shift to baseband and filtering of the baseband signal), Fig. 3 *with* Ex. 1108, [0042] (desired channels digitally translated to baseband and “[t]he translated channels are then digitally lowpass filtered ..., leaving only the channel of interest”), [0058]-[0077], Fig. 6, *and* Ex. 1109, [0025] (“channel extraction ... is performed by direct digital conversion to zero IF, followed by channel filters”), [0036]-[0054], Fig. 3A; Ex. 1102, ¶ 113.

In addition to selecting channels, the DSSP 150 upconverts baseband I and Q signals for the selected channels, output from the first stages 307, to corresponding frequencies, sums the upconverted I and Q signals for all the selected channels to create a combined signal 158 having digital I component 158a (blue) and digital Q

component 158b (**brown**), and outputs those digital signals 158a, 158b. Ex. 1108, [0018]-[0024], [0043], [0053], [0078]-[0096], [0098]-[0122], Figs. 4, 6, 9-15; Ex. 1109, [0005], [0007], [0015], [0025], [0055]-[0069], [0071]-[0095], Figs. 1, 3A, 5-11; Ex. 1102, ¶ 114.

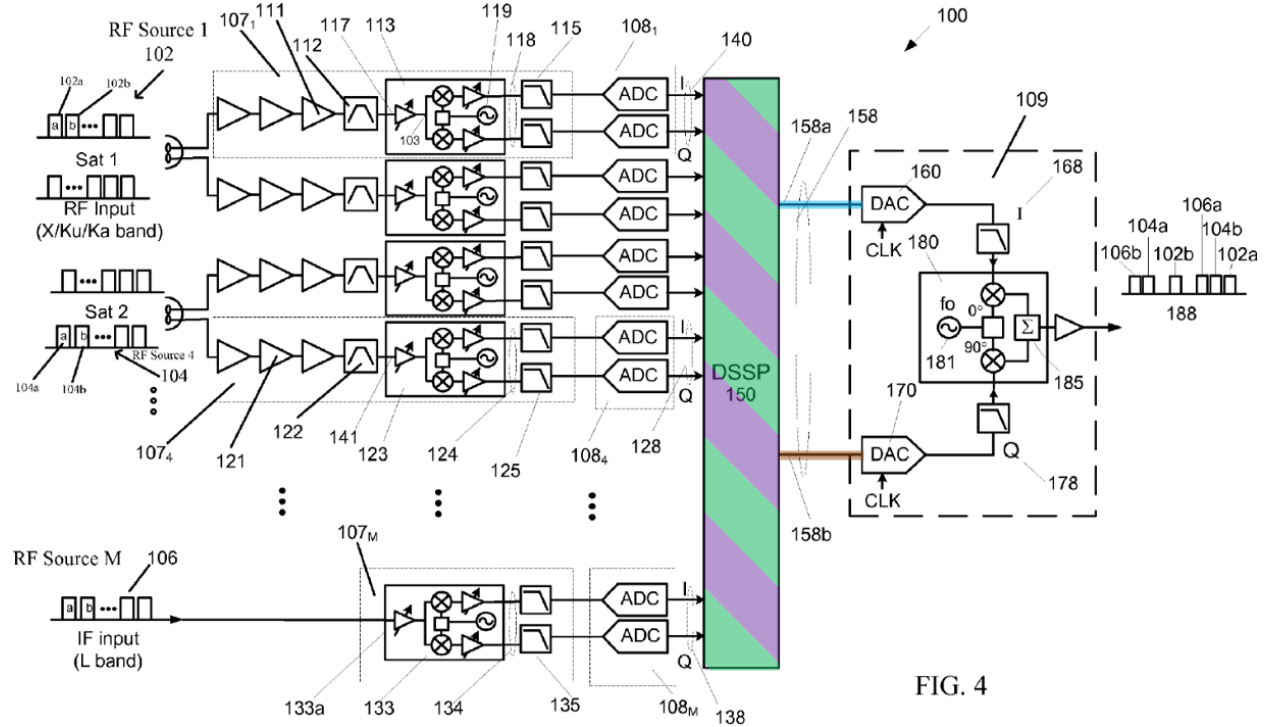


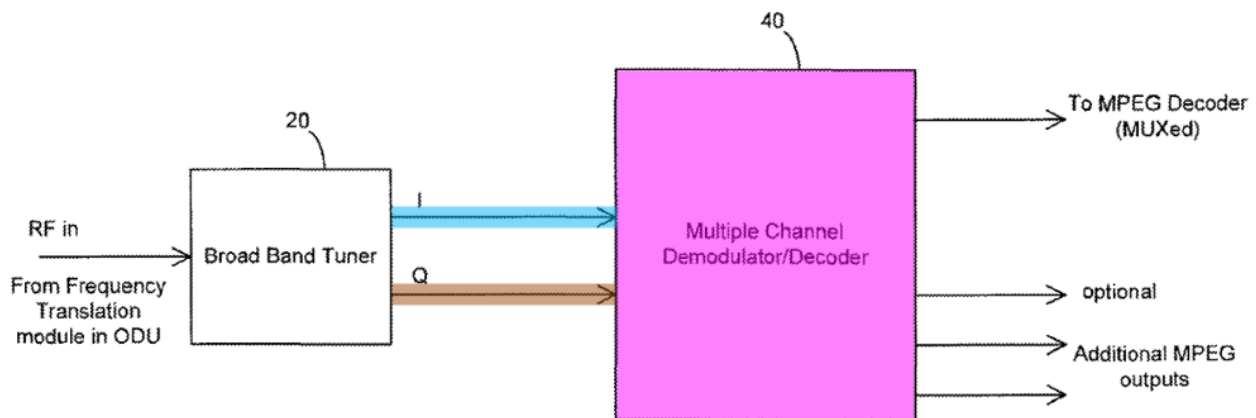
FIG. 4

Ex. 1108, Fig. 4 (annotated)

The signals 158a, 158b are a digital datastream that contains the selected channels. Ex. 1108, [0009], [0043], [0046] (referring to “digital composite signal 158”), [0054], [0055] (circuits of the DSSP 150 “extract a desired channel and locate or place the channel in the desired channel slot of the output signal 158”), Figs. 4, 6; Ex. 1109, [0005], [0015], [0025], [0030], [0033], Figs. 1, 3A; Ex. 1102, ¶ 115.

Although Petrovic indicates that its channel stacking system “may be implemented as an outdoor unit (ODU) as part of a satellite receiving system,” Petrovic does not limit its channel stacking system or its tuner (e.g., the Petrovic APD stage(s), the Petrovic ADC pair(s), and the Petrovic DSSP) to ODU use. Ex. 1108, [0054]; Ex. 1109, [0030]; Ex. 1102, ¶ 116. A POSITA would have been aware of other uses, as tuners were ubiquitous at the time, and in any event, Eidson teaches additional uses for the Petrovic tuner, and indeed, for the entire Petrovic channel stacking system. Ex. 1102, ¶ 116.

Eidson’s Figure 8 discloses “a broadband tuner and multi-channel demodulator and decoder [pink]” that can be used as a multiple channel receiver of a set top box. Ex. 1112, 1:48-50, 2:8-10, 2:25-33, 2:42-51, 5:59-60, 7:58-59, 8:27-9:2; Ex. 1102, ¶¶ 117-118.



Ex. 1112, Fig. 8 (annotated)

The multiple channel demodulator and decoder (“demodulator/decoder”) 40 receives digital I (blue) and Q (brown) signals from a front end that comprises a

broadband tuner 20 and a frequency translation module (FTM) of a satellite outdoor unit (ODU). Ex. 1112, 8:29-9:2, Fig. 8; Ex. 1102, ¶ 119. The FTM portion of the front end selects multiple channels, translates those selected channels to contiguous portions of a bandwidth, and sends an RF signal with those translated channels to the tuner 20. Ex. 1112, 8:30-47, 9:5-25, Figs. 8-10; Ex. 1102, ¶ 119. The tuner 20 downconverts the received RF signal, generates I and Q components of that downconverted signal, and digitizes those I and Q components to create digital I, Q signals. Ex. 1112, 8:43-47, 9:5-25, Figs. 8-10; Ex. 1102, ¶ 119. Those digital I, Q signals are output to the demodulator/decoder 40, which demodulates multiple channels in those signals. Ex. 1112, 8:65-9:2, 11:44-12:28, Figs. 8, 15-16; Ex. 1102, ¶ 119. Thus, Eidson teaches a demodulator to which “a selected plurality of television channels” is being output “as a digital datastream.” Ex. 1102, ¶¶ 119-120.

The I, Q signals received by the Eidson demodulator/decoder 40 from the front end (e.g., the FTM and the tuner 20) are functionally equivalent to the Petrovic I, Q signals 158a, 158b, as both sets of I, Q signals comprise multiple channels that have been placed into sequential slots of a bandwidth. Ex. 1102, ¶ 121. In particular, the I, Q signals received by the Eidson demodulator/decoder 40 are digital signals for multiple channels that have been selected and placed into contiguous portions of a bandwidth. Ex. 1112, 8:43-9:25, Figs. 8-10; Ex. 1102, ¶ 121. Similarly, the Petrovic I, Q signals 158a, 158b are digital signals for multiple channels that have

been selected and has been placed into sequential portions of a bandwidth. Ex. 1108, Title, [0002], [0008], [0028], [0041]-[0044], [0046], [0053]-[0055], [0059]-[0091], [0097], Figs. 3, 4, 6, 8; Ex. 1109, Title, [0001], [0004], [0008], [0015], [0025], [0030], [0033]-[0064], [0070], Figs. 1, 3A, 4; Ex. 1102, ¶¶ 121-122.

A POSITA would have appreciated that the I and Q signals output from Petrovic's DSSP could be readily sent to a demodulator for a STB, as taught in Eidson. Ex. 1102, ¶ 123. This could be done in place of Petrovic's stage 109, or in addition to it. Eidson teaches that its demodulator/decoder 40 operates by receiving I, Q signals that are functionally equivalent to the I, Q signals 158a, 158b output by the Petrovic DSSP. Ex. 1102, ¶ 123. A POSITA would have been motivated to combine a Petrovic tuner and the Eidson demodulator/decoder 40 so that the multiple selected channels output by the Petrovic DSSP (as I, Q signals 158a, 158b) could be demodulated in the digital domain with a single demodulator, which would have been more efficient than using multiple simultaneous demodulators for separate channels. Ex. 1112, 4:2-6; 6:36-38; Ex. 1102, ¶ 123.

Combining a Petrovic tuner with an Eidson demodulator/decoder 40 would also allow incorporation of tuning/channel selection and demodulating/decoding functionality into a single device, a configuration known in the art, but with the added benefits of digital tuning afforded by Petrovic and multichannel demodulation afforded by Eidson. Ex. 1108, [0007], [0094]; Ex. 1109, [0003], [0069]; Ex. 1112,

3:35-45; 4:2-6; 6:36-38; Ex. 1102, ¶ 124 (citing Ex. 1140, which describes a satellite set-top box (STB) able to receive multiple satellite signals, tune channels of received satellite signals, and demodulate those channels). For example, the Eidson demodulator/decoder 40 could be added to the Petrovic tuner in a set top box intended to function as a “media center STB,” that would feed other set top boxes. Ex. 1112, 2:28-31; Ex. 1102, ¶ 125. In such a set top box, the I, Q signals could be simultaneously output to the demodulator/decoder 40 (e.g., for demodulation/decoding for output to display or recording devices) and to the Petrovic DAC and Complex to Real Conversion stage 109 for generation of a signal 188 to transmit to other set top boxes or devices. Ex. 1102, ¶ 125. Alternatively, the stage 109 could be omitted to save cost if “media center STB” functionality was not needed, thereby allowing a further simplified design. *Id.*

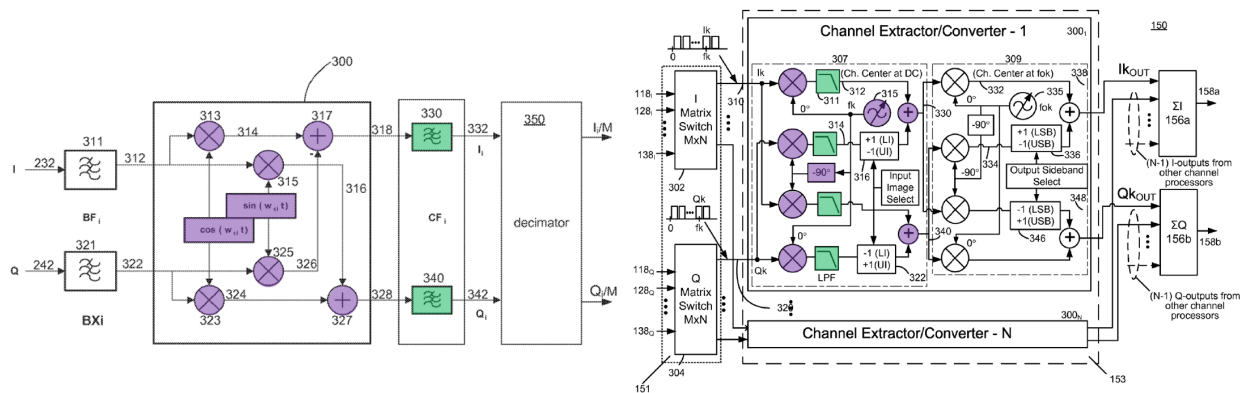
Moreover, combining a Petrovic tuner and the Eidson demodulator/decoder would have been a combination of known prior art elements (Petrovic’s mixers, ADCs, and DSSP and Eidson’s demodulator/decoder) according to known methods (sending the I and Q signals to the demodulator/decoder, as taught in Eidson) to yield predictable results (the signals are demodulated and decoded). Ex. 1102, ¶ 126. As explained above, and as a POSITA would have recognized, the output of a Petrovic tuner is the functional equivalent of the input to the Eidson demodulator/decoder. *Id.* A POSITA would thus have combined a Petrovic tuner and the Eidson

demodulator/decoder, as each would perform the same function in the combination that would be performed individually prior to the combination. *Id.* For the same reasons, the results of combining the Petrovic tuner with the Eidson demodulator/decoder would also have been predictable. *Id.* Neither the function of the Petrovic tuner, nor the function of the Eidson demodulator/decoder, would change appreciably if combined, and thus each element could operate as it did before, leading to an expectation of success. *Id.*

Although the above analysis explains why a POSITA would have added the Eidson demodulator/decoder to the Petrovic tuner, a POSITA would have been just as motivated to add the Petrovic tuner to the Eidson demodulator/decoder. *Id.*, ¶ 127. Petrovic, by virtue of the functional equivalence of the I, Q signals output by the Petrovic DSSP to the I, Q signals received by the Eidson demodulator/decoder 40, and by virtue of the equivalent selection and stacking functions performed by the Petrovic tuner and by the Eidson front end, teaches that the Petrovic tuner could be readily substituted for the Eidson front end. *Id.* The advantages of and motivation for that combination would be the same as those described above for modification of Petrovic based on Eidson. *Id.* And the combination would similarly have been a combination of known prior art elements according to known methods to yield predictable results with an expectation of success. *Id.*

In the Petrovic-Eidson system, the Petrovic DSSP is the “digital circuitry” of limitation [1D]. *Id.*, ¶ 128. The Petrovic DSSP in Petrovic-Eidson is configured to select said plurality of desired television channels from said digitized plurality of frequencies (i.e., select channels from the digitized plurality of frequencies received by the DSSP); and output said selected plurality of television channels to a demodulator (the Eidson demodulator/decoder) as a digital datastream (the signals 158a, 158b). *Id.*

To the extent “digital circuitry” of limitation [1D] is construed to be a means-plus-function term, and as seen by the below comparisons of Figure 6 and Petrovic and Figure 3 of the '362 patent, the Petrovic DSSP includes structure that is the same as, or equivalent to, structure of the complex mixers 250 and 300 and filters 260, 330, and 340 of the '362 patent. *Id.*, ¶ 129; *see* Section V.E.3.



Ex. 1101, Fig. 3 (annotated)

Ex. 1108, Fig. 6 (annotated)

Like complex mixer 300 of the '362 patent (purple), which is one of N complex mixers 250, the DSSP of Petrovic comprises N first stages 307, each of

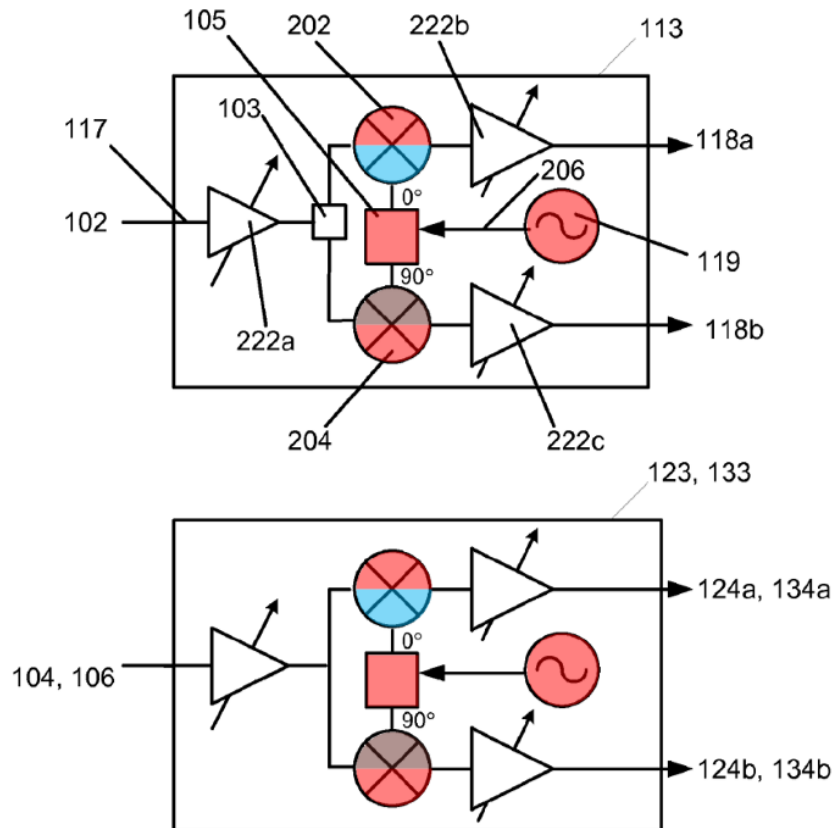
which comprises a complex mixer (**purple**). Ex. 1101, 6:7-42; Ex. 1108, [0066]-[0068], Fig. 6; Ex. 1109, [0045]-[0047], Fig. 3A; Ex. 1102, ¶ 130 (citing as background Ex. 1118 and Ex. 1134); *see* Section VI.A.6. Like the filters 330 and 340 of the '362 patent (**green**), which are one of N filter modules 260, each first stage 307 of the Petrovic DSSP comprises low pass filters (LPF) 311 (**green**). Ex. 1101, 6:43-47; Ex. 1108, [0066]-[0069]; Ex. 1109 [0045]-[0048]; Ex. 1102, ¶ 130; *see* Section VI.A.6. Any differences between the '362 patent structure (N mixers 300 and N filters 330 and 340) and the Petrovic first stages 307 are insubstantial. Ex. 1102, ¶ 130. Both perform the same function of selecting and outputting a respective desired channel, in the same way by first downconverting the respective desired channel to baseband and then low pass filtering with a filter to isolate the channel, to achieve the same result of producing a plurality of desired channels as a digital data stream. *Id.*; Ex. 1101, 5:49-6:47; Ex. 1108, [0060]-[0070]; Ex. 1109, [0037]-[0054].

2. Claim 4

[4] “The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.”

Claim 4 depends from claim 1, which is obvious over Petrovic-Eidson. Section VI.A.1. Petrovic also discloses the additional limitations of claim 4. Ex. 1102, ¶ 131. As explained in Section VI.A.1.b for limitation [1B], the mixers of any

of the individual downconverters shown in Figure 4 of Petrovic (e.g., downconverters 113, 123, 133), mixers of any of the individual downconverters of other Petrovic embodiments, or the mixers of any combination of those downconverters, is a mixer module. Ex. 1102, ¶ 132. As shown in the examples below, each of those downconverters comprises a first mixer (**red/blue**) configured to generate an in-phase signal and a second mixer (**red/brown**) configured to generate a quadrature signal. Ex. 1108, [0034] (describing downconversion mixing operation “during which the signal ... is converted into a complex representation having a real I (in-phase) component and an imaginary Q (quadrature) component”), [0036]-[0037], [0039], Figs. 4-5; Ex. 1109, [0010], [0018], [0023], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 132.



Ex. 1108, Fig. 5 (annotated)

Accordingly, claim 4 is also obvious over Petrovic-Eidson. Ex. 1102, ¶ 131.

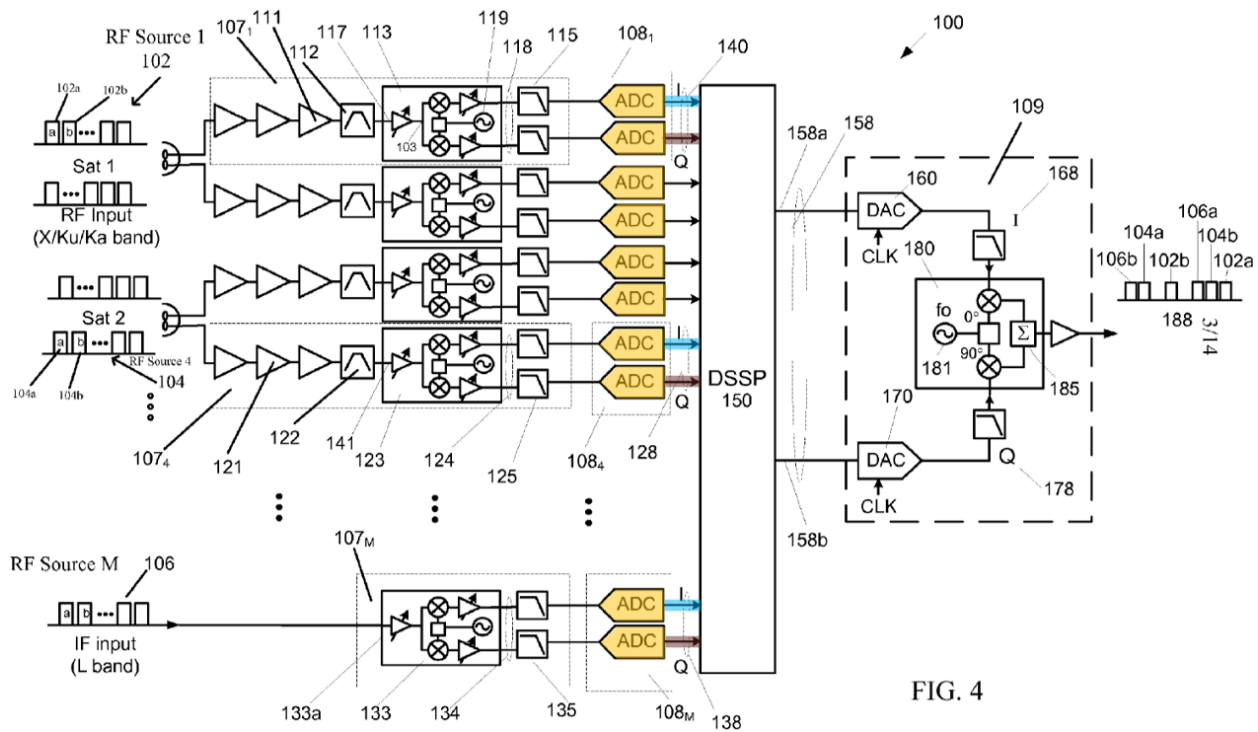
3. Claim 5

[5] “The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

Claim 5 depends from claim 1, which is obvious over Petrovic-Eidson.

Section VI.A.1. As explained in Section VI.A.1.c for limitation [1C], any of the individual ADC pairs 108₁-108_M shown in Figure 4 of Petrovic, any of the individual ADC pairs of other Petrovic embodiments, or any combination of those ADC pairs, is a wideband ADC module. Ex. 1102, ¶¶ 133-134. Each of those ADC pairs 108₁-

108_M comprises “a first ADC configured to generate a digital in-phase signal” and “a second ADC configured to generate a digital quadrature signal.” Ex. 1108, [0039], [0051]-[0052], Fig. 4; Ex. 1109, [0010], [0013], [0018], [0022], [0024], [0028], Fig. 1; Ex. 1102, ¶ 134. Indeed, “digital in-phase signal[s]” (**blue**) and “digital quadrature signal[s]” (**brown**) emanating from several of the Petrovic ADC pairs 108₁-108_M (**gold**) are labelled as such (“I” or “Q”) in Figure 4 of Petrovic. *Id.*

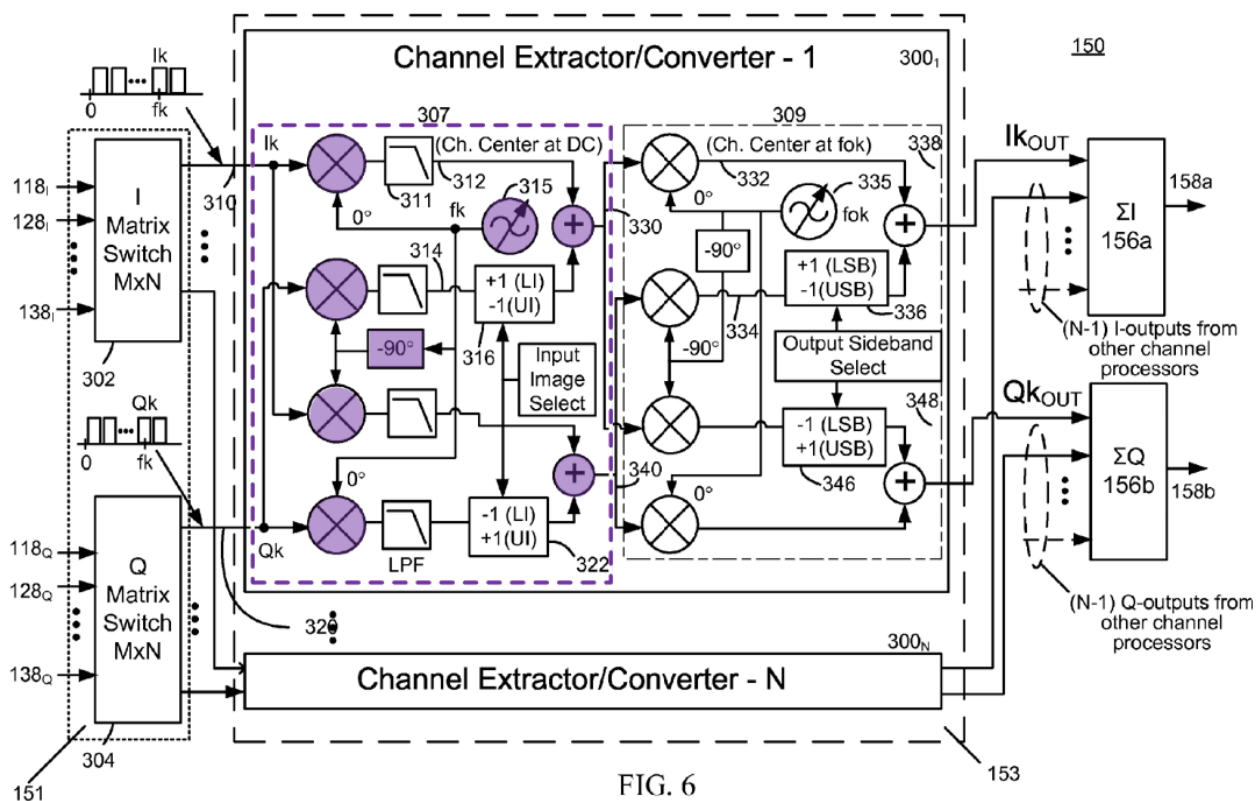


Ex. 1108, Fig. 4 (annotated)

4. Claim 6

[6] “The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.”

As explained in Section VI.A.1.d for limitation [1D], the Petrovic system 100 includes “digital circuitry” in the form of a DSSP (e.g., the DSSP 150). Ex. 1102, ¶¶ 135-136. Figure 6 shows additional details of the DSSP 150 and of the DSSP of other Petrovic embodiments, which may include “channel extractor/converter circuit[s] 300.” Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 136.



Ex. 1108, Fig. 6 (annotated)

The DSSP 150 may have N channel extractor/converter circuits 300, where N may be equal to the number of selected channels to be included in the output signal 158. Ex. 1108, [0055], Fig. 6; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 137. Each circuit 300 includes a first stage 307 (**purple** broken line) that selects a single desired channel. Ex. 1108, [0042], [0058]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1102, ¶¶ 137-138.

The first section 307 (and in particular, the individual shaded elements (**purple**)) is a complex mixer because it mixes (i.e., multiplies) a complex signal (i.e., a signal with in-phase and quadrature components) with a local oscillator (LO) signal, which shifts the frequency of the complex signal (i.e., downconverts the I_k signal 310 and the Q_k signal 320) by the frequency of the LO signal. Ex. 1108, [0066]-[0068], Fig. 6; Ex. 1109, [0045]-[0047], Fig. 3A; Ex. 1102, ¶ 139 (citing as background Ex. 1118 and Ex. 1134). Because the DSSP 150 (and each of the DSSPs of other embodiments) includes multiple circuits 300, with each having its own first section 307, the Petrovic DSSPs each includes “a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.” Ex. 1108, Fig. 6; Ex. 1109, Fig. 3A; Ex. 1102, ¶ 140.

Accordingly, claim 6 is also obvious over Petrovic-Eidson. Ex. 1102, ¶ 135.

5. Claim 7

- a. [7A] “The wideband receiver system of claim 6, wherein: prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”

Claim 7 depends from claim 6, which is obvious over Petrovic-Eidson. Section VI.A.4. Petrovic also discloses limitation [7A]. Ex. 1102, ¶¶ 141-142; *see also* ¶ 72. Figure 4 of Petrovic shows that a received RF signal 104 may include channels 104a (red), 104b, etc., received in a frequency band above 3GHz (e.g., the X band (7-12.5 GHz), Ku band (10.7-12.75 GHz), or Ka band (17.3-20.3 GHz)) and that a received RF signal 106 in the L band (950-2150 MHz) may include channels 106a, 106b (red), etc. Ex. 1108, [0029]-[0031], [0033], [0050], Fig. 4; Ex. 1109, [0010]-[0013], [0019]-[0020], [0023], Fig. 1; Ex. 1102, ¶ 143.

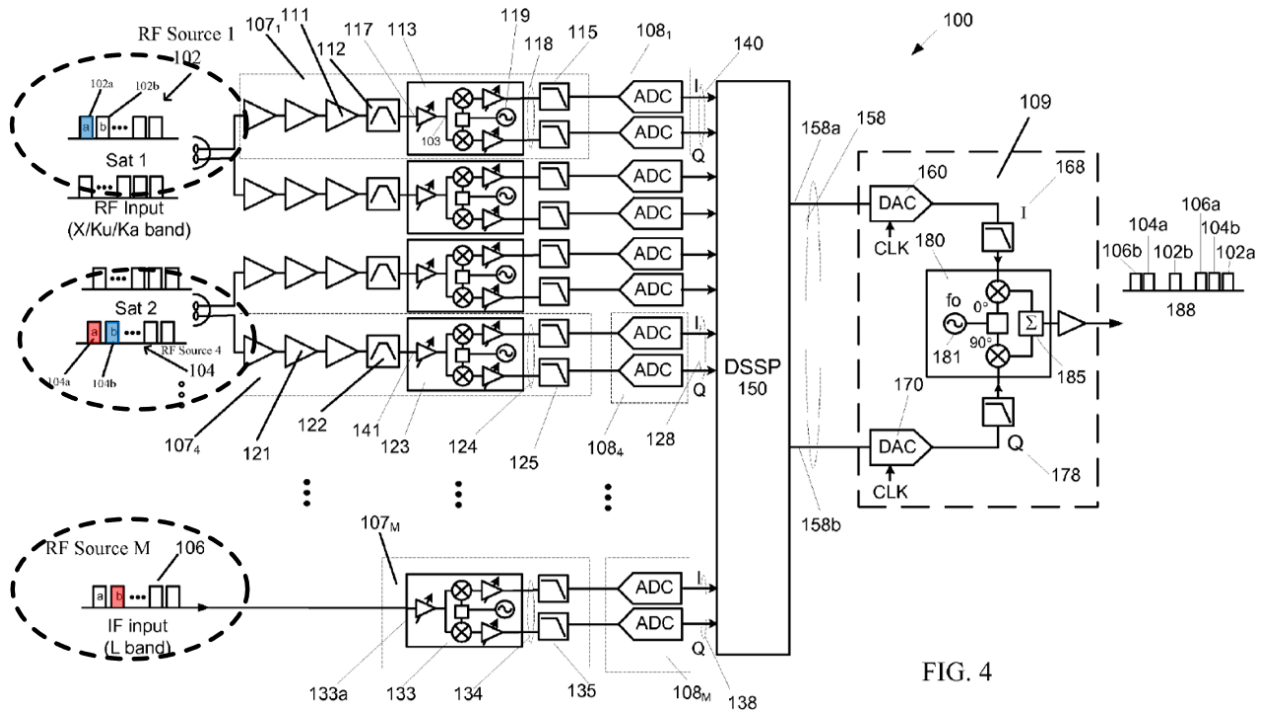


FIG. 4

Ex. 1108, Fig. 4 (annotated)

The signals 104a and 106b are channels that are assembled into the composite signal 158 that includes channels selected by the channel extractor/converter circuits 300 of the DSSP 150. Ex. 1108, [0053], Figs. 4, 6; Ex. 1109, Figs. 1, 3A; Ex. 1102, ¶ 144. As can be seen in Figure 4, and based on the signals 104 and 106 being in different bands, channels 104a and 106b are non-contiguous prior to the frequency shift that occurs in the DSSP 150. Ex. 1102, ¶ 144.

Moreover, Petrovic '886, which Petrovic incorporates by reference (Ex. 1108, [0001]), provides additional details regarding RF signals 102 and 104. In particular, Petrovic '886 indicates that the signals 102a (blue) and 102b may be in a lower half of the Ku band (10.7-11.725 GHz), and that the signals 104a and 104b (blue) may

be in an upper half of the Ku band (11.725-12.75 GHz). Ex. 1109, [0019]; Ex. 1102, ¶ 145. The signals 102a and 104b are channels that are assembled into the composite signal 158 that includes channels selected by the channel extractor/converter circuits 300 of the DSSP 150. Ex. 1108, [0053], Figs. 4, 6; Ex. 1109, Figs. 1, 3A; Ex. 1102, ¶ 145. As can be seen in Figure 4, and based on the signals 102a and 104b being in different halves of the Ku band, channels 102a and 104b are non-contiguous prior to the frequency shift that occurs in the DSSP 150. Ex. 1102, ¶ 145.

Finally, and even if Petrovic did not show two desired channels that are noncontiguous in an RF signals as received by a tuner (it does), a POSITA would have understood that the Petrovic system would receive noncontiguous desired channels. Ex. 1102, ¶ 146. For example, the Petrovic system 100 “‘stack[s]’ or assemble[s] channels resident within an RF signal into a composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box, or other receiver/tuner.” Ex. 1108, [0028]; Ex. 1109, [0008]. The number of available slots in that composite signal may be much less than the total number of channels received by the system 100. Ex. 1108, [0029] (received signal 102 may have 120 or more channels), [0055] (output signal 158 may have as few as four channel slots); Ex. 1109, [0016], [0033]. A POSITA would thus have understood from Petrovic that, in order for the system 100 to stack four channels selected from 120 channels in an input signal, the system 100 would

have been configured to select at least two channels that are not contiguous in the received RF signal. Ex. 1102, ¶ 146.

- b. [7B] “after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”**

Petrovic discloses limitation [7B]. Ex. 1102, ¶ 147; *see also* ¶ 72. As explained in Section VI.A.5.a for limitation [7A], Petrovic Figure 4 shows non-contiguous channels 104a and 106b in received signals 104 and 106, as well as non-contiguous channels 102a and 104b in received signals 102 and 104. Petrovic Figure 4 also shows that channels 104a (**red**) and 106b (**red**) are contiguous in a signal 188 that is after the frequency shift that occurs in the DSSP 150, as are the channels 102a (**blue**) and 104b (**blue**). Ex. 1108, [0053]-[0054], Fig. 4; Ex. 1109, [0025], [0030], Fig. 1; Ex. 1102, ¶ 148.

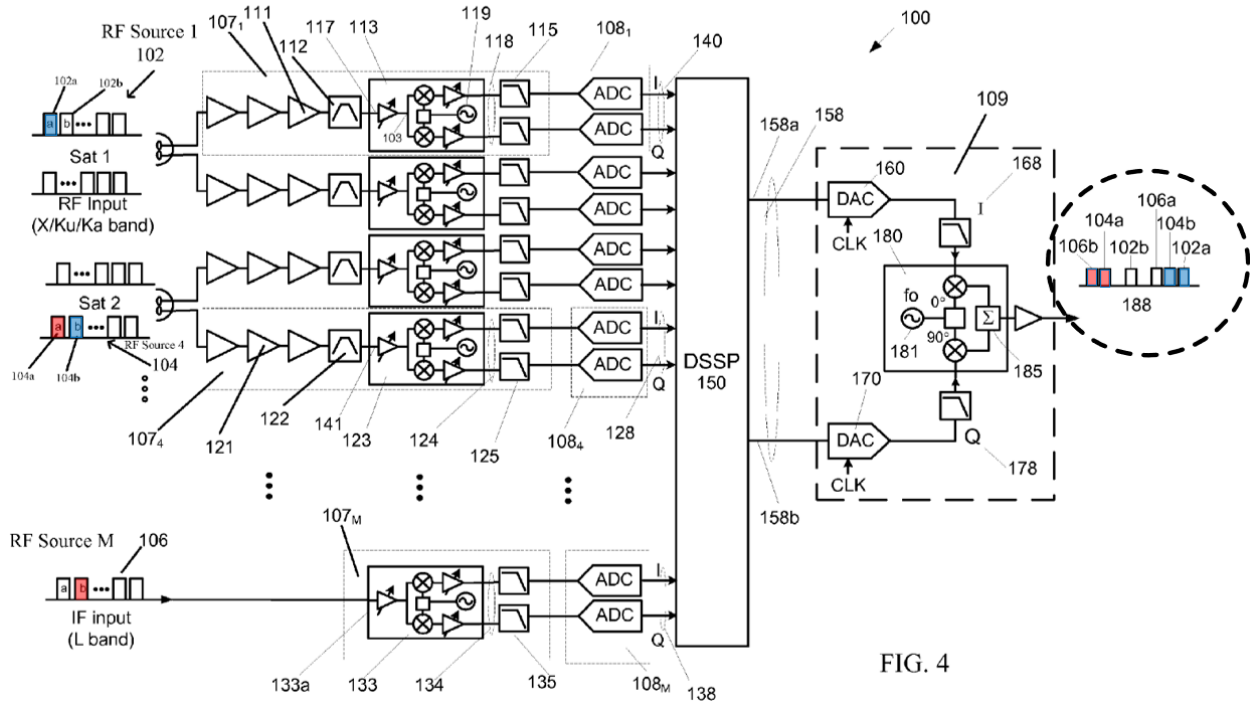


FIG. 4

Ex. 1108, Fig. 4 (annotated)

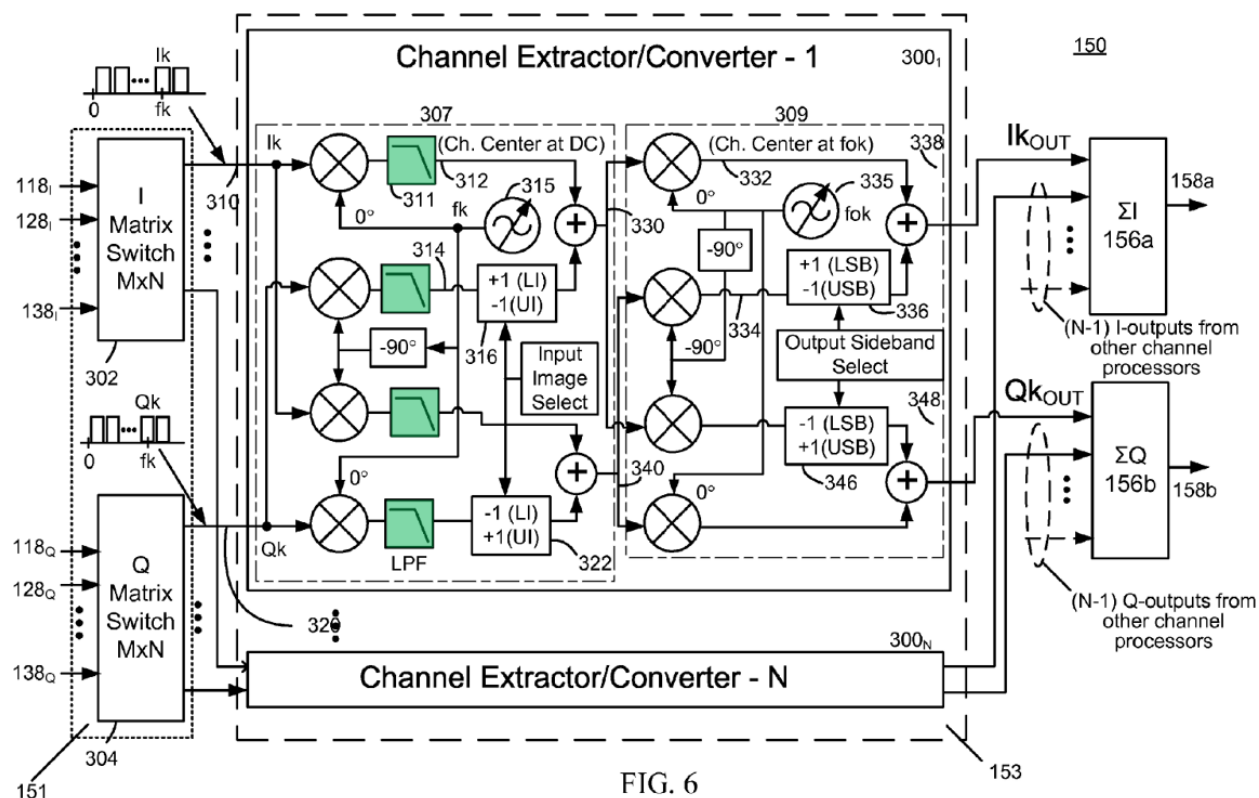
Because the stage 109 only converts the signals 158a and 158b to analog, upconverts those analog signals, and combines the upconverted analog signals, the channels 104a and 106b would also be contiguous in the signals 158a and 158b output from the DSSP 150, as would the channels 102a and 104b. Ex. 1108, [0054], [0097], Figs. 4, 8; Ex. 1109, [0030], [0070], Figs. 1, 4; Ex. 1102, ¶ 149.

Accordingly, claim 7 is also obvious over Petrovic-Eidson. Ex. 1102, ¶ 141.

6. Claim 8

[8] “The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.”

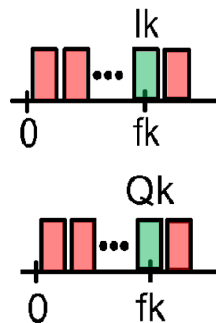
Claim 8 depends from claim 1, which is obvious over Petrovic-Eidson. Section VI.A.1. Petrovic discloses the limitations of claim 8. Ex. 1102, ¶ 150. As explained in Section VI.A.1.d for limitation [1D], the Petrovic system 100 includes “digital circuitry” in the form of the DSSP 150, additional details of which are shown in Figure 6. Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 151.



Ex. 1108, Fig. 6 (annotated)

The DSSP 150 includes multiple sets of low pass filters 311 (four in each first portion 307 of each circuit 300) (**green**) that are configured to perform selection of desired television channels. Specifically, first stage 307 receives the in-phase and quadrature signal components of the downconverted satellite signal, which contains a desired channel (I_k and Q_k in **green**) and undesired channels (**red**) as shown below.

Ex. 1108, [0061]; Ex. 1109, [0040]; Ex. 1102, ¶ 152.



Ex. 1108, Fig. 6 (excerpted and annotated)

Stage 307 first utilizes a combination of mixers (represented with the symbol “ $\otimes$ ”) to multiply these signals by a LO signal 315 having a frequency f_k , which shifts the desired channel to zero and undesired channels to adjacent frequencies. Ex. 1108, [0066]-[0068]; Ex. 1109, [0045]-[0047]; Ex. 1102, ¶ 153. Low pass filters 311 then select the desired channel by passing I_k and Q_k centered at zero to the output, while removing the undesired channels, which are outside of the filter channel bandwidth. Ex. 1108, [0066]-[0069]; Ex. 1109, [0045]-[0048]; Ex. 1102, ¶ 153. Such selection is the same as that described by the '362 patent. Ex. 1101, 6:43-47; Ex. 1102, ¶ 153.

Accordingly, claim 8 is also obvious over Petrovic-Eidson. Ex. 1102, ¶ 150.

7. **Claim 11**

[11A] “A method comprising: in a wideband receiver system:”

[11B] “downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”

[11C] “digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”

[11D] “selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and”

[11E] “outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.”

Elements [11A]-[11E] recast the required functionality of Elements [1A]-[1D] as method steps performed by identical structural elements. Ex. 1102, ¶¶ 154-162. Thus, claim 11 is directed to substantially identical subject matter as claim 1 and obvious over Petrovic-Eidson for the reasons discussed above with respect to claim 1. *Id.*; see Section VI.A.1.

8. Claims 14-17

[14] “The method of claim 11, comprising: generating, by a first mixer of said mixer module, an in-phase signal; and generating, by a second mixer of said mixer module, a quadrature signal.”

[15] “The method of claim 11, comprising: generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.”

[16] “The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.”

[17A] “The method of claim 16, wherein: prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”

[17B] “after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”

Claims 14-17 recast the required functionality of claims 4-7 as method steps performed by identical structural elements. Ex. 1102, ¶¶ 163-168. Thus, claims 14-17 are directed to substantially identical subject matter as claims 4-7 and obvious over Petrovic-Eidson for the reasons discussed above with respect to claims 4-7. *Id.*; see Sections VI.A.2.-VI.A.5.

9. Claim 18

[18] “The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.”

Claim 18 is directed to substantially identical subject matter as claim 8, and thus is obvious over Petrovic-Eidson for the reasons discussed above with respect to claim 8. Ex. 1102, ¶ 169; *see* Section VI.A.6.

B. Petrovic-Takahiko-Eidson (Claims 1, 4-8, 11, 14-18)

As set forth below, claims 1, 4-8, 11, and 14-18 are obvious over Petrovic in view of Takahiko and Eidson. Ex. 1102, ¶¶ 170-183, *see also* ¶¶ 48-77.

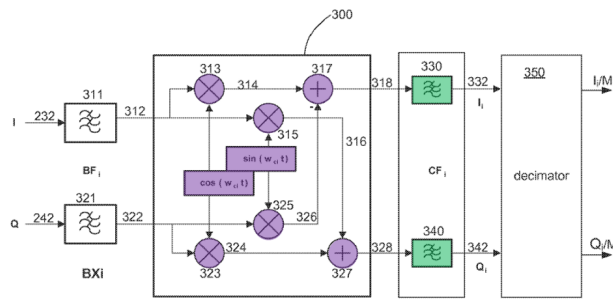
1. Independent Claim 1

a. [1A]-[1C]

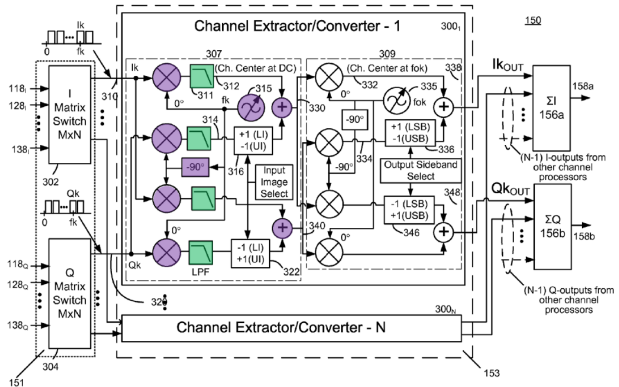
Petrovic discloses limitations [1A]-[1C] for the reasons explained in Sections VI.A.1.a-VI.A.1.c. Ex. 1102, ¶ 172.

b. [1D]

As explained in Section VI.A.1.d, and as illustrated by the side-by-side comparison of Figure 3 of the '362 patent and Figure 6 of Petrovic, any differences between the Petrovic first stage 307 and the mixer 300 and filters 330 and 340 of the '362 patent are insubstantial. Ex. 1102, ¶¶ 173-174.



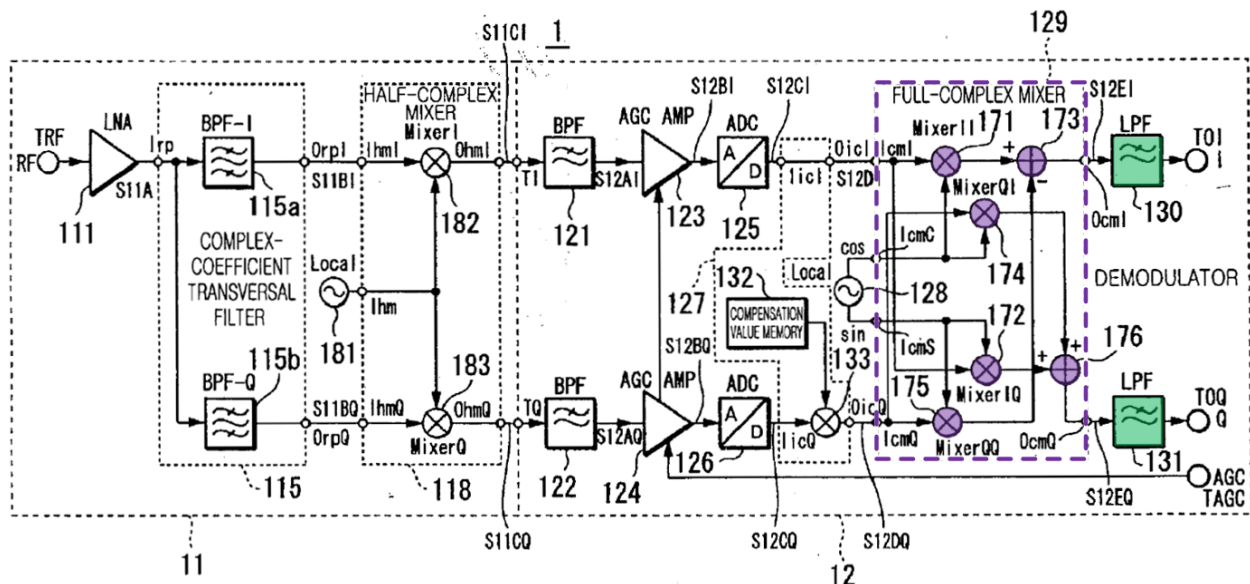
Ex. 1101, Fig. 3 (annotated)



Ex. 1108, Fig. 6 (annotated)

To the extent Patent Owner contends that the location of LPFs 311 within the complex mixer of Petrovic stage 307, as shown in Figure 6 of Petrovic, is not the same or equivalent structure as the complex mixer 300 and filters 330 and 340 of Figure 3 of the '362 patent (it is), placing four low pass filters before adders (the “⊕” symbols in the above Figures) of a complex mixer (as shown in Petrovic Figure 6) or two low pass filters after adders of a complex mixer (as shown in '362 patent Figures 2-3) would have been functionally equivalent and a matter of design choice, as both options were well known. Ex. 1102, ¶ 174.

For example, Takahiko describes a “downconverter” 1 that is used in a radio receiver, and that is very similar to the receiver of '362 patent Figure 2. Ex. 1161, [0143], Fig. 1; Ex. 1102 ¶ 175.



Ex. 1161, Fig. 1 (annotated)

Takahiko's downconverter 1 discloses a "full-complex mixer" 129 (purple, broken-line purple box) and low pass filters (green) 130 and 131 that are the same as what is shown in the '362 patent Figure 3. Ex. 1102, ¶ 176. Moreover, Takahiko uses full-complex mixer 129 and filters 130 and 131 in the same way that the '362 patent describes use of complex mixer 300 and filters 330 and 340: downconversion of digital I, Q signals so a desired channel is at baseband and removal of unwanted higher frequencies with low-pass filtering. Ex. 1161, [0153], [0156]; Ex. 1102, ¶ 176.

A POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 to use two low pass filters after the adders of the complex mixer, similar to the configuration of the Takahiko full-complex mixer 129 and filters 130 and 131 located after adders 173 and 176, and instead of four low pass filters within

the complex mixer, to make the circuit simpler and less expensive. Ex. 1102, ¶ 177. Because such a modification would have involved use of known circuit components in known arrangements, because of the similarity between the relevant portions of the Petrovic first sections 307 and the Takahiko full-complex mixer 129 and filters 130 and 131, and because the Takahiko full-complex mixer 129 and filters 130 and 131 would have been functionally equivalent to a Petrovic first section 307, a POSITA would have had a reasonable expectation of success and the results of the modification would have been predictable. *Id.*

A POSITA would have combined the Petrovic channel stacking system, as modified in view of Takahiko, with the Eidson demodulator/decoder for the reasons explained in Section VI.A.1.d, as the modification would not affect the input provided to a corresponding second stage 309 of the Petrovic DSSP, nor would it affect the signals 155a, 158b generated by the DSSP. Ex. 1102, ¶ 178.

Accordingly, claim 1 is obvious over Petrovic-Takahiko-Eidson. Ex. 1102, ¶ 171.

2. Claims 4-7

The limitations of claims 4-7 are taught by Petrovic-Takahiko-Eidson for the reasons explained in Sections VI.A.2-VI.A.5, as the addition of Takahiko does not affect the disclosure by Petrovic of those limitations. Ex. 1102, ¶ 179. Accordingly, claims 4-7 are obvious over Petrovic-Takahiko-Eidson. *Id.*

3. Claim 8

The limitation of claim 8 is taught by Petrovic-Takahiko-Eidson. Ex. 1102, ¶ 180. As modified in view of Takahiko, the LPFs would be located after the adders of the complex mixer of a Petrovic first stage 307, would have the same configuration as shown in Figure 3 of the '362 patent, and would operate, similar to the LPFs 311 of Petrovic, to select the desired channel by passing I_k and Q_k centered at zero to the output, while removing the undesired channels, which would be outside of the filter channel bandwidth. *Id.* Accordingly, claim 8 is obvious over Petrovic-Takahiko-Eidson. *Id.*

4. Independent Claim 11

Elements [11A]-[11E] recast the required functionality of Elements [1A]-[1D] as method steps performed by identical structural elements. Ex. 1102, ¶ 181. Thus, claim 11 is directed to substantially identical subject matter as claim 1 and is obvious over Petrovic-Takahiko-Eidson for the reasons discussed above with respect to claim 1. *Id.*; see Section VI.B.1.

5. Claims 14-17

Claims 14-17 recast the required functionality of claims 4-7 as method steps performed by identical structural elements. Ex. 1102, ¶ 182. Thus, claims 14-17 are directed to substantially identical subject matter as claims 4-7 and are obvious over Petrovic-Takahiko-Eidson for the reasons discussed above with respect to claims 4-7. *Id.*; see Section VI.B.2.

6. Claim 18

Claim 18 is directed to substantially identical subject matter as claim 8, and thus is obvious over Petrovic-Takahiko-Eidson for the reasons discussed above with respect to claim 8. Ex. 1102, ¶ 183; *see* Section VI.B.3.

C. Petrovic-Eidson-Rabaey (Claims 2-3, 12-13)

As set forth below, claims 2-3 and 12-13 are obvious over Petrovic in view of Eidson and Rabaey. Ex. 1102, ¶¶ 184-193, *see also* ¶¶ 48-77.

1. Claims 2-3

[2] “The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.”

[3] “The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.”

Claims 2-3 are similar, and only differ with regard to a type of interface via which the digital datastream of limitation [1D] is output. Ex. 1101, 11:66-12:2. Claim 2 recites output “via a serial interface,” while claim 3 recites output “via a parallel interface.” *Id.* But as explained below, either option would have been an obvious design choice, and thus claims 2 and 3 are obvious over Petrovic in view of Eidson and Rabaey. Ex. 1102, ¶¶ 184-185, *see also* ¶¶ 75-77.

As explained in Section VI.A.1.d, Petrovic discloses a DSSP 150 (or a DSSP of another Petrovic embodiment) as the “digital circuitry configured to output said selected plurality of television channels ... as a digital datastream” of limitation [1D]. Ex. 1102, ¶ 172. As the ’362 patent concedes, the outputting of a digital data

stream via serial (claim 2) and parallel (claim 3) interfaces were “commonly known methods.” Ex. 1101, 6:55-58; Ex. 1102, ¶ 186. Indeed, dictionaries, basic text books, and technical papers at the time confirm that a POSITA would have understood parallel and serial interfaces as the two common options for outputting data in standard integrated circuits. Ex. 1102, ¶¶ 186-187 (citing Ex. 1114, 9:44-50, 30:31-42, 31:15-22; Ex. 1115, pp. 5-6, 8; Ex. 1116, pp. 79-80; Ex. 1117, pp. 354-355). Notably, Petrovic discloses the DSSP 150 and other components of the system 100 may be implemented as “hardware” such as “application specific integrated circuits.” Ex. 1108, [0027], [0040], [0124]-[0125]; Ex. 1109, [0009], [0115]; Ex. 1102, ¶ 187. As explained in Section VI.A.1.d, a POSITA would have modified Petrovic so that a Petrovic tuner—which includes a DSSP outputting the digital data stream—would output digital data to the Eidson demodulator/decoder. Ex. 1102, ¶ 187. Eidson indicates that a front end and a multichannel demodulator/decoder could be integrated into a single package, which further indicates digital data would flow from a Petrovic DSSP to an Eidson demodulator/decoder using conventional integrated circuit interfaces. Ex. 1112, 6:33-35; Ex. 1102, ¶ 187.

At the most fundamental level, a digital integrated circuit represents data as binary units (“bits”) in the form of electrical signals on wires (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1102, ¶ 188; Ex. 1116, pp. 23-24, 27-29, 48-51. Multiple bits can be sent over multiple separate wires, one wire

for each bit (“parallel interface”), or one bit at a time over a single wire (“serial interface”). Ex. 1102, ¶ 188, *see also* ¶¶ 75-76; Ex. 1115, pp. 5-6; Ex. 1116, pp. 79-80 (Figure 6.25).

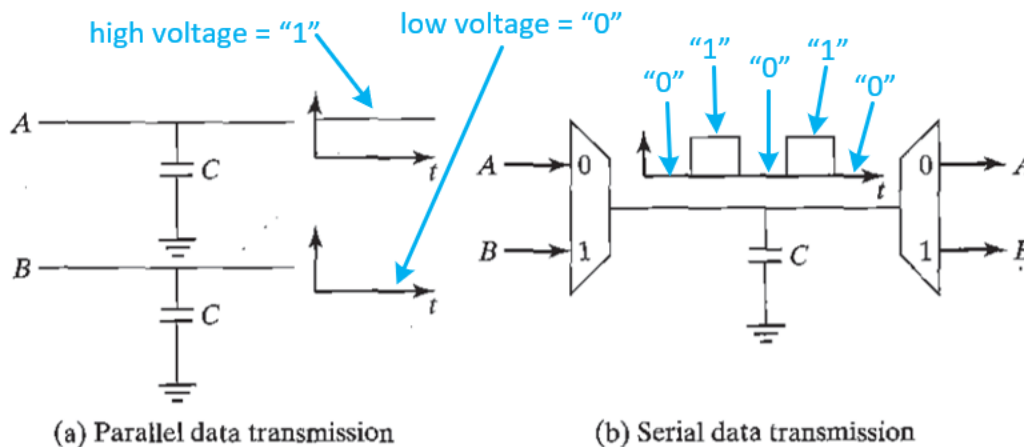


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1116, p. 80 Fig. 6.25 (annotated)

Implementing a data interface between a Petrovic DSSP and an Eidson demodulator/decoder using either option would have been equally obvious as one of two design choices, because both were “commonly known methods” used by POSITAs. Ex. 1102, ¶ 189, *see also* ¶¶ 75-76; Ex. 1114, 30:31-42, 31:15-22; Ex. 1115, pp. 4-6; Ex. 1116, pp. 79-80; Ex. 1117, pp. 354-355. For the same reasons, implementing serial and parallel interfaces would have been well within the POSITA’s skillset, and thus, a POSITA would have had a high expectation of success leading to a predictable result. Ex. 1102, ¶ 189.

For example, Rabaey, a textbook on implementing digital integrated circuits, teaches that both serial and parallel interfaces as illustrated in the Figure 6.25 above

were beneficially used in integrated circuits. Ex. 1116, pp. 79-80; Ex. 1102, ¶ 190. Per Rabaey, time-multiplexing (i.e., a serial interface) “is an often used technique to minimize the implementation area” of a design on a chip, but that this “minimum area solution does not always result in the lowest switching activity,” for example, when the data signals have high “temporal correlation.” Ex. 1116, pp. 79-80, *see also* pp. 72-74; Ex. 1102, ¶ 190. Minimizing circuit area minimizes the cost of the integrated circuit, while minimizing the switching activity minimizes the power consumed by the integrated circuit. Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 190. Thus, Rabaey teaches selecting between serial and parallel interfaces for transmitting digital data between two points, both of which have advantages over each other, depending upon area and power constraints and the temporal correlation between the signals. Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 190.

It would have been obvious to apply either of Rabaey’s parallel data or serial interfaces as illustrated in Figure 6.25 to the interconnection between Petrovic’s DSSP and Eidson’s demodulator/decoder. Ex. 1102, ¶ 191. Petrovic and Eidson teach implementation in an integrated circuit, and the techniques taught in Rabaey would have enabled such implementation. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116, pp. 76-80; Ex. 1102, ¶ 191.

As such, the modification of Petrovic and Eidson with Rabaey that results in a serial interface (claim 2) between Petrovic’s DSSP and Eidson’s

demodulator/decoder is nothing more than a combination of prior art elements (Petrovic's and Eidson's circuit designs and Rabaey's serial interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a serial interface to minimize chip area and cost) to yield predictable results (data is sent serially). Ex. 1102, ¶ 191.

Likewise, the modification of Petrovic and Eidson with Rabaey that results in a parallel interface (claim 3) between Petrovic's DSSP and Eidson's demodulator/decoder is also nothing more than a combination of prior art elements (Petrovic's and Eidson's circuit designs and Rabaey's parallel interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a parallel interface to minimize switching and power) to yield predictable results (data is sent in parallel). *Id.*

The resultant combinations of Petrovic, Eidson, and Rabaey are predictable and a POSITA would have had a reasonable expectation of success, because Rabaey teaches basic techniques used by POSITA to design integrated circuits, and because those techniques are specifically directed to overcoming specific issues, such as meeting area and power constraints, that a POSITA would customarily balance in their designs. Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 192.

2. Claims 12-13

[12] “The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.”

[13] “The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.”

Claims 12-13 recast the required functionality of claims 2-3 method steps performed by identical structural elements. Ex. 1102, ¶ 193. Thus, claims 12-13 are directed to substantially identical subject matter as claims 2-3 and rendered obvious by Petrovic in view of Eidson and Rabaey for the reasons discussed above with respect to claims 2-3. *Id.*; see Section VI.C.1.

D. Petrovic-Takahiko-Eidson-Rabaey (Claims 2-3, 12-13)

Claims 2-3 and 12-13 are obvious over Petrovic-Takahiko-Eidson-Rabaey for the reasons explained in Sections VI.B.1 and VI.C.1-VI.C.2, as modification in view of Takahiko does not affect modification in view of Rabaey. Ex. 1102, ¶ 194, *see also* ¶¶ 48-77.

E. Petrovic-Eidson-Jensen (Claims 9-10, 19-20)

As set forth below, claims 9-10 and 19-20 are obvious over Petrovic in view of Eidson and Jensen. Ex. 1102, ¶¶ 195-203, *see also* ¶¶ 48-77.

1. Claim 9

[9] “The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.”

As explained in Section VI.A.6 for claim 8, Petrovic discloses low pass filters 311 that are configured to perform selection of desired television channels. Ex. 1102, ¶ 196. Petrovic does not explicitly indicate whether the low pass filters 311 would be finite impulse response (FIR) filters. As explained by Jensen, however, FIR filters were “[a] popular class of filters for channel-select filtering ... because of their inherent linear phase response.” Ex. 1126, [0007]; Ex. 1102, ¶ 196. A POSITA would have selected FIR filters for use as the low pass filters 311 of Petrovic to take advantage of their linear phase response, which avoids distorting the received signal, and would have known to do so because of the popularity of such filters. Ex. 1126, [0006]; Ex. 1102, ¶ 196. As disclosed by Jensen, the use of FIR filters was popular (and thus well-known) for channel selection in the digital domain, and thus the result of using FIR filters for the Petrovic low pass filters 311 would have been predictable to a POSITA, leading to an expectation of success. Ex. 1126, [0006]-[0007]; Ex. 1102, ¶ 196.

Using FIR filters for the Petrovic low pass filters 311 would also have been a simple substitution of one known element for another to obtain predictable results. Ex. 1102, ¶ 197. FIR filters, their functions, and their uses were known in the art.

Ex. 1126, [0006]-[0007]; Ex. 1102, ¶ 197. Because FIR filters, their functions, and their uses were well known, a POSITA would have been able to implement the Petrovic circuit 300 using FIR filters as the low pass filters 300, and the results of doing so would have been predictable. Ex. 1102, ¶ 197.

2. Claim 10

[10] “The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.”

As explained in Section VI.A.1.d, Petrovic discloses a DSSP 150 as “digital circuitry configured to[] select said plurality of desired television channels ... and output said plurality of desired television channels ... as a digital datastream” of limitation [1D]. Ex. 1102, ¶ 198. Petrovic is silent with regard to whether the DSSP 150 comprises a decimator circuit. As explained by Jensen, however, decimation was commonly performed to reduce a sampling rate of a digital signal, as reducing sampling rate would reduce power consumption and complexity in subsequent processing. Ex. 1126, [0007]; Ex. 1102, ¶ 198, *see also* ¶ 73.

This would have been particularly relevant if the Petrovic stage 109 were retained after modification in view of Eidson. Ex. 1102, ¶ 199. As explained in Section VI.A.1.d, stage 109 may be retained if Petrovic were modified in view of Eidson to implement, as suggested by Eidson, a media center STB that would feed

other set top boxes. *Id.* In such a configuration, Petrovic as modified in view of Eidson would receive a wideband RF source that includes undesired and desired channels (e.g., 120 channels) and output a composite signal with a reduced number of desired channels (e.g., 4 channels) to a lower bandwidth cable. Ex. 1108, [0005], [0029], [0044]-[0045], [0054]-[0055]; Ex. 1102, ¶ 199. Thus, the rate of Petrovic's ADCs for sampling the RF source signals would be higher than the rate required by the digital-to-analog converters (DACs) in stage 109 to reproduce the analog composite signal. Ex. 1108, [0005], [0029], [0044]-[0045], [0054]-[0055]; Ex. 1102, ¶ 199.

Following Jensen, a POSITA would have included a decimator circuit in the Petrovic DSSP 150, either as a separate component following the low pass filters 311 or as part of channel-select decimation filters used for the low pass filters 311, to reduce the sampling rate of a digital signal and thereby reduce power consumption and/or complexity in subsequent processing, e.g., in stage 309 in DSSP 150, and potentially in stage 109 (including the DACs) that follows DSSP 150. Ex. 1126, [0007]; Ex. 1108, Figs. 4, 6; Ex. 1109, Figs. 1, 3A; Ex. 1102, ¶ 200. As disclosed by Jensen, the use of decimation modules or of channel-select decimation filters (which combined a FIR filter with decimation) was common (and thus well-known), and the result of including decimation in the Petrovic DSSP 150 would thus have been

predictable to a POSITA, leading to an expectation of success. Ex. 1126, [0007]; Ex. 1102, ¶ 200.

Including a decimator circuit in the Petrovic DSSP 150 would also have been a use of a known technique to improve a similar device and method in the same way. Ex. 1102, ¶ 201. Decimators, and their use in channel selection circuits, and the improvement resulting from decimator use, were well known. Ex. 1126, [0007]; Ex. 1102, ¶ 201, *see also* ¶ 73. Because decimators, their functions, and their improvement to channel selection circuits were well known, a POSITA would have been able to include a decimator in the Petrovic circuit 300, and the results of doing so would have been predictable. Ex. 1102, ¶ 201.

3. Claim 19

[19] “The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.”

Claim 19 is directed to substantially identical subject matter as claim 9, and thus is obvious over Petrovic-Eidson-Jensen for the reasons discussed above with respect to claim 9. Ex. 1102, ¶ 202; *see* Section VI.E.1.

4. Claim 20

[20] “The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.”

Claim 20 recasts the required functionality of claim 10 as a method step performed by identical structural elements. Ex. 1102, ¶ 203. Thus, claim 20 is

directed to substantially identical subject matter as claim 10 and obvious over Petrovic-Eidson-Jensen for the reasons discussed above with respect to claim 10. *Id.*; see Section VI.E.2.

F. Petrovic-Takahiko-Eidson-Jensen (Claims 9-10, 19-20)

As set forth below, claims 9-10 and 19-20 are obvious over Petrovic in view of Takahiko, Eidson, and Jensen. Ex. 1102, ¶¶ 204-205, *see also* ¶¶ 48-77.

1. Claims 9, 19

The limitations of claims 9 and 19 are disclosed by Petrovic-Takahiko-Eidson-Jensen for the reasons explained in Sections VI.B.1, VI.E.1, and VI.E.3, as the advantages of (and motivation for) using a FIR filter would still apply if the Petrovic first stages 307 were modified, in view of Takahiko, to have LPFs after the complex mixer. Ex. 1102, ¶ 204. Accordingly, claims 9 and 19 are obvious over Petrovic-Takahiko-Eidson-Jensen. *Id.*

2. Claims 10, 20

The limitations of claims 10 and 20 are obvious over Petrovic-Takahiko-Eidson-Jensen for the reasons explained in Sections VI.B.1, VI.E.2, and VI.E.4, as modification in view of Takahiko does not affect the motivation to modify Petrovic-Eidson, in view of Jensen, to include a decimator circuit (claim 10) or perform decimating (claim 20). For example, a POSITA would include a decimator circuit after the LPFs that would be placed (per Takahiko) after the Petrovic complex mixer or incorporate the decimator into such LPFs (per Jensen's disclosure of channel-

select decimation filters). Ex. 1102, ¶ 205. Accordingly, claims 10 and 20 are obvious over Petrovic-Takahiko-Eidson-Jensen. *Id.*

VII. GROUNDS FOR STANDING & FEE PAYMENT

Petitioner hereby certifies that the '362 patent is available for, and Petitioner is not barred or estopped from requesting, *inter partes* review challenging claims 1-20.

Pursuant to 37 C.F.R. § 42.103, the undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

VIII. CONCLUSION

Inter partes review should be instituted and claims 1-20 canceled.

Dated: February 16, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282
Banner & Witcoff, Ltd.
1100 13th Street, NW
Suite 1200
Washington, DC 20005
(202) 824-3000
fmeeker@bannerwitcoff.com

CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,139, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,126 words as counted by the Word Count feature of Microsoft Word and 13 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: February 16, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282
Banner & Witcoff, Ltd.
1100 13th Street, NW
Suite 1200
Washington, DC 20005
(202) 824-3000
fmeeker@bannerwitcoff.com

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of this Petition for *Inter Partes* Review in connection with U.S. Patent No. 9,210,362 and supporting evidence to be served via FedEx Priority Overnight on February 16, 2024, on the following:

23446 - MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

Dated: February 16, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282

CLAIM LISTING APPENDIX

U.S. Pat. No. 9,210,362

Designation	Claim Language
Claim 1	
[1A]	A wideband receiver system comprising:
[1B]	a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[1C]	a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;
[1D]	digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.
Claim 2	
2	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.
Claim 3	
3	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.
Claim 4	
4	The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.
Claim 5	
5	The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.
Claim 6	
6	The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.

Designation	Claim Language
Claim 7	
[7A]	The wideband receiver system of claim 6, wherein: prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[7B]	after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 8	
8	The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.
Claim 9	
9	The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 10	
10	The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.
Claim 11	
[11A]	A method comprising: in a wideband receiver system:
[11B]	downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[11C]	digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;
[11D]	selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and
[11E]	outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.

Designation	Claim Language
Claim 12	
12	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.
Claim 13	
13	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.
Claim 14	
14	The method of claim 11, comprising: generating, by a first mixer of said mixer module, an in-phase signal; and generating, by a second mixer of said mixer module, a quadrature signal.
Claim 15	
15	The method of claim 11, comprising: generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.
Claim 16	
16	The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.
Claim 17	
[17A]	The method of claim 16, wherein: prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[17B]	after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 18	
18	The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.
Claim 19	
19	The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 20	

Designation	Claim Language
20	The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.