

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner

v.

ENTROPIC COMMUNICATIONS, LLC.,
Patent Owner.

Patent No. 9,210,362
Filing Date: February 5, 2015
Issue Date: December 8, 2015
Title: WIDEBAND TUNER ARCHITECTURE

Inter Partes Review No.: IPR2024-00433

DECLARATION OF DAVID B. LETT

**IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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I, David B. Lett, declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

1. INTRODUCTION

1. I have been retained as an expert witness on behalf of the Petitioner, Comcast Cable Communications, LLC, for the above-referenced *inter partes* review proceeding.

2. I have been asked to provide a declaration regarding certain matters pertaining to U.S. Patent No. 9,210,362 (“the ’362 patent”) (Ex. 1101) and the unpatentability grounds set forth in the Petition for this proceeding. My experience with television distribution systems, Set Top Boxes (STBs), modulation schemes, radio frequency systems, Video on Demand (VOD), and content delivery systems provides me with an understanding of the subject matter described and claimed in the ’362 patent.

3. I am being compensated at my usual consulting rate or testimony rate of \$385 per hour. My compensation is in no way dependent upon my opinions or testimony or the outcome of this proceeding. I have no financial interest in the party or in the outcome of this proceeding.

2. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

4. I am a technical consultant and product development industry veteran with expertise in electronics, software, hardware, video, audio, and data

communications, having led product development organizations in cable, satellite, consumer electronics, home automation, asset tracking, remote tank logistics, and alarm industries. My current curriculum vitae is attached as Ex. 1103 and some highlights follow.

5. I earned my B.S. in Electrical Engineering (1982) with high honors from the University of Tennessee in Knoxville, Tennessee. I also attended the Georgia Institute of Technology from 1986 to 1987, completing 40% of the required degree hours for the M.S. Electrical Engineering program.

6. From 1982 to 1985, I worked at Scientific Atlanta as an Electrical Engineer designing video, audio, and data communications equipment for the cable television industry. I designed software and hardware including addressable data transmitters, video sync suppression scramblers, transaction format converters, and data channel monitors for addressable Cable Television systems and Set Top Boxes.

7. From 1983 to 1985, while working at Scientific Atlanta, I also worked as an Assistant Professor at DeVry Institute of Technology, teaching courses in electronics and microprocessor hardware/software.

8. From 1985 to 1990, I worked at Wegener Communications as a Senior Electrical Engineer, designing satellite communications equipment including forward error correction (FEC) coding systems, PSK modems, and analog control systems for RF modulators and PSK demodulators. I was promoted to the Hardware Engineering Manager, where I managed product development of video, audio, and

data satellite receivers, modulators, graphics display systems, DSP-based companders, FSK and PSK satellite modems, multiplexers, forward error correction (FEC) codecs, RF upconverters and downconverters, and baseband analog and digital processing components.

9. In 1990, I returned to Scientific Atlanta, which was acquired by Cisco in 2006. I worked as Engineering Manager running the set top box engineering group where I was promoted to Director and Vice President during my tenure until 2011. I led the design of many cable set top boxes and systems through the evolution of analog video, addressability, downloadable software, electronic program guides, digital video, VOD, software applications, high-definition TV, DVR, DOCSIS, full spectrum tuners, and multiroom DVR. These systems implemented various technologies including DOCSIS 1/2/3 and hybrid gateways, 802.11, IPTV, DVR, cable modems, ADSL, VDSL, DVB-T/C/S, bootloaders, factory diagnostics, application frameworks, Nagra, DRMs, conditional access, secure microprocessors, device management, Android, Adobe Flash, Linux, DVD play/record, MPEG-4, MPEG-2, H.264, NTSC, PAL, DAVIC, MoCA, high-performance CPUs, cablecards, network processors, HDMI, multiple video/audio display interfaces, 2D/3D graphics, multiple RF tuners, and full spectrum tuners.

10. From 2011 to 2016, I worked for EchoStar Technologies, which served as the product development organization for sister company DISH Network. I served as Vice President of Engineering and was the Head of the Atlanta research and

development center. I led the development of satellite set top boxes, consumer electronic equipment, and a home automation and security system. Technologies used included video/audio, IoT, H.265, HEVC, 3D, Satellite, wireless, MoCA, transcoding, embedded C Linux applications, mobile applications (IOS and Android), SaaS, web applications (Javascript, HTML), BSS/OSS, AWS cloud storage, 2-way video/audio streaming, authentication, and VoIP.

11. In 2016, I started an independent consulting business in technology and intellectual property projects. I have consulted in various technology areas and industries including consumer electronics, Internet of Things (IoT), cable, satellite, television, media, and cryptocurrency.

12. From 2019 to 2022, I worked as Chief Technology Officer for Telular, an Ametek company. I was responsible for the development of Industrial Internet of Things (IIoT) recurring revenue solutions, combining wireless technologies, purpose-built hardware, and SaaS in the commercial telematics, security and home automation markets and sold under the SkyBitz and Telguard brands.

13. My record of professional service includes awards on products I designed and developed from several organizations in my field of expertise, including Best of Show, Technology Emmy, and Best of Innovations.

14. I am a named inventor on at least 87 patents and published patent applications corresponding to the areas of my professional work. The patents and published applications involving video and audio technologies include:

- U.S. Patent No. 9,882,736 titled “Remote Sound Generation for a Home Automation System”
- U.S. Patent No. 9,615,139 titled “Determining Device That Performs Processing of Output Pictures”
- U.S. Patent No. 8,549,567 titled “Media Content Sharing Over a Home Network”
- U.S. Patent No. 8,161,388 titled “Interactive discovery of display device characteristics”
- U.S. Patent Nos. 8,120,924, 7,240,217, 6,785,817, 6,564,324, 6,212,278, and 5,440,632 titled “Reprogrammable Subscriber Terminal”
- U.S. Patent No. 7,908,625 titled “Networked Multimedia System”
- U.S. Patent Nos. 7,861,272 and 7,849,486 titled “Networked Subscriber Television Distribution”
- U.S. Patent Nos. 7,774,820 and 7,069,578 titled “Settop Cable Television Control Device and Method Including Bootloader Software and Code Version Table for Maintaining and Updating Settop Receiver Operating System Software”
- U.S. Patent No. 5,771,064 titled “Home Communications Terminal having an Applications Module”
- U.S. Patent No. 5,715,515 titled “Method and Apparatus for Downloading On-Screen Graphics and Captions to a Television Terminal”

- U.S. Patent No. 5,657,414 titled “Auxiliary Device Control for a Subscriber Terminal”
- U.S. Patent No. 5,592,551 titled “Method and Apparatus for Providing Interactive Electronic Programming Guide”
- U.S. Patent No. 5,539,822 titled “System and Method for Subscriber Interactivity in a Television System”
- U.S. Patent No. 5,357,276 titled “Method of Providing Video On Demand with VCR Like Functions”
- U.S. Patent Application Publication Nos. 2004/0068753 and 2008/0072272 titled “Video Transmission Systems and Methods for a Home Network”
- U.S. Patent Application Publication No. 2004/0133911 titled “Subscriber Network in a Satellite System”

15. I have a general understanding of the U.S. patent prosecution process and of the novelty and non-obviousness requirements for patentability.

16. I believe that my extensive industry experience and educational background qualify me as an expert in the relevant field of digital signal processing (DSP) and radio frequency (RF) tuning systems for satellite and/or cable communications. I am knowledgeable of the relevant skill set that would have been possessed by a hypothetical person of ordinary skill in the art at the time of the invention of the '362 patent, which I (as I discuss below in Section 5) understand is early 2009 or early 2010.

3. MATERIALS CONSIDERED

17. In formulating my opinion, I reviewed and considered the '362 patent (U.S. Pat. No. 9,210,362 to Reddy, et al.) (Ex. 1101), as to which I am offering my opinion regarding the validity of certain claims, as discussed herein.

18. In preparing this declaration, I also reviewed and considered the Petition and the file history of the '362 patent (included in Ex. 1104) as well as the following references:

Ex. 1101: U.S. Patent No. 9,210,362 (“the '362 patent”)

Ex. 1102: Expert Declaration of David B. Lett

Ex. 1103: Curriculum Vitae of David B. Lett

Ex. 1104: Certified Prosecution History of the '362 patent

Ex. 1107: Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“'526 provisional”)

Ex. 1108: U.S. Pub. No. 2009/0290659 (“Petrovic”)

Ex. 1109: Certified Prosecution History of U.S. Provisional App. No. 61/054,886 (“Petrovic '886”)

Ex. 1110: U.S.P.T.O Assignment Record for U.S. Application No. 12/414,892

Ex. 1112: U.S. Patent No. 7,783,958 (“Eidson”)

Ex. 1114: U.S. Patent No. 7,237,214 (“Pandey”)

Ex. 1115: Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)

- Ex. 1116: Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
- Ex. 1117: A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)
- Ex. 1118: S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
- Ex. 1119: U.S. Patent No. 6,061,406 (“Carson”)
- Ex. 1121: Data-Over-Cable Service Interface Specifications, DOCSIS 2.0, Radio Frequency Interface Specification, CM-SP-RFIV2.0-I11-060602
- Ex. 1122: Certified File History (as of February 2, 2024) for Ex Parte Reexamination No. 90/019,255
- Ex. 1125: J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
- Ex. 1126: U.S. Pub. No. 2007/0027943 (“Jensen”)
- Ex. 1127: U.S. Patents and Patent Applications Family Tree for U.S. Pat. 9,210,362

- Ex. 1129: Entropic Communications, LLC v. Charter Communications, Inc., No. 2:22-cv-00125-JRG (E.D. Tex. June 26, 2023) (Claim Construction Memorandum Opinion and Order)
- Ex. 1133: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2nd ed. 2004) (“Ciciora”)
- Ex. 1134: Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)
- Ex. 1135: U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
- Ex. 1136: U.S. Pub. No. 2003/0217362 (“Summers”)
- Ex. 1137: U.S. Pub. No. 2006/0256799 (“Eng”)
- Ex. 1138: U.S. Pub. No. 2006/0083335 (“Seendripu”)
- Ex. 1139: Excerpts of Chris Bowick, “RF Circuit Design” (2nd ed. 2008)
- Ex. 1140: U.S. Pub. No. 2006/0031894 (“Petruzzelli”)
- Ex. 1141: Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)
- Ex. 1142: U.S. Patent No. 7, 272, 375 (“Tuttle”)
- Ex. 1143: U.S. Patent No. 7,130,576 (“Gurantz”)
- Ex. 1144: U.S. Patent No. 5,278,837 (“Kelly”)
- Ex. 1145: Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)

- Ex. 1146: U.S. Patent No. 7,213,042 (“Cannon”)
- Ex. 1148: Excerpts of William Buchanan, “Computer Busses” (2000)
- Ex. 1149: U.S. Patent No. 7,079,528 (“Ziegler”)
- Ex. 1150: Excerpts of “Software Defined Radio: Enabling Technologies” (Walter H.W. Tuttlebee ed., 2003)
- Ex. 1154: U.S. Pub. No. 2003/0220072 (“Coffin”)
- Ex. 1155: U.S. Patent No. 6,493,873 (“Williams”)
- Ex. 1156: U.S. Pub. No. 2007/0053314 (“Gat”)
- Ex. 1161: U.S. Pub. No. 2006/0256216 (“Takahiko”)
- Ex. 1170: U.S.P.T.O Assignment Record for U.S. Patent No. 8,526,898
- Ex. 1171: U.S.P.T.O. Assignment Record for U.S. Patent No. 7,783,958 (“Eidson”)
- Ex. 1173: Expert Declaration of Dr. Sylvia Hall-Ellis
- Ex. 1175: U.S. Patent No. 6,791,995 (“Azenkot”)
- Ex. 1176: U.S. Patent No. 6,542,203 (“Shadwell”)

4. UNDERSTANDING OF APPLICABLE LEGAL STANDARDS

19. Although I am not an attorney, I have a general understanding of the applicable legal standards pertaining to the patentability issues presented in this proceeding. I understand that the Petitioner is challenging the patentability of the claims of the '362 patent based on the following grounds:

- Claims 1, 4-8, 11, and 14-18 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson.
- Claims 1, 4-8, 11, and 14-18 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Takahiko and Eidson.
- Claims 2, 3, 12, and 13 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson and Rabaey.
- Claims 2, 3, 12, and 13 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Takahiko, Eidson, and Rabaey.
- Claims 9, 10, 19, and 20 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Eidson and Jensen.
- Claims 9, 10, 19, and 20 as obvious under pre-AIA 35 U.S.C. § 103(a) based on Petrovic in view of Takahiko, Eidson, and Jensen.

20. I understand that, in this *inter partes* review, Petitioner has the burden of proving that each challenged claim is unpatentable by a preponderance of the evidence.

21. I understand that to be valid, a patent claim must be “novel,” and is invalid if “anticipated” by a single prior art reference. I further understand a reference anticipates if it discloses each and every element as arranged in the claim so as to enable a person of ordinary skill in the art to make and use the claimed invention without undue experimentation.

22. I understand that a patent claim is unpatentable if, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of the prior art to yield the patent claim. It is my understanding that this determination is made after weighing the following factors: (1) the level of ordinary skill in the pertinent art; (2) the scope and content of the prior art; (3) the differences between the prior art as a whole and the claim at issue; and (4) as appropriate, other objective considerations identified below.

23. It is my understanding that the prior art and claimed invention should be viewed through the knowledge and understanding of a person of ordinary skill in the art – one should not use his or her own insight or hindsight in deciding whether a claim is obvious. I further understand that a claim may be rendered obvious if a person of ordinary skill in the art can implement the claimed invention as a predictable variation of a known product. I further understand that a person of ordinary skill in the art is presumed to have knowledge of the relevant prior art at the time of the claimed invention, which comprises any prior art that was reasonably pertinent to the particular problems the inventor faced.

24. I understand that a showing of obviousness requires some articulated reasoning with a rational underpinning to support the combination of the references. I understand that in consideration of the issue of obviousness it is important to identify whether a reason existed at the time of the invention that would have led a

person of ordinary skill in the pertinent art to combine elements of the references in a way that yields the claimed invention.

25. I understand that a claim may be considered unpatentable for obviousness for various reasons. I have been informed that the following exemplary rationales may support a finding of obviousness:

- (A) combining prior art elements according to known methods to yield predictable results;
- (B) substituting one known element for another to obtain predictable results;
- (C) use of a known technique to improve similar devices in the same way;
- (D) applying a known technique to a known device ready for improvement to yield predictable results;
- (E) choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- (F) known work in a field that prompts variations in the work in the same or a different field that leads to predictable results; and
- (G) some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify a prior art reference or combine multiple prior art references or teachings to arrive at the claimed invention.

26. I understand that various objective or “real world” factors may be indicative of non-obviousness. I understand that such factors include:

- (A) the commercial success of the claimed invention;
- (B) the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- (C) failed attempts to solve the problem solved by the claimed invention;
- (D) copying of the claimed invention;
- (E) unexpected results of the claimed invention;
- (F) praise for the claimed invention by others in the relevant field; and
- (G) willingness of others to accept a license under the patent because of the merits of the claimed invention.

27. It is my understanding that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link may be based on the common sense of the person of ordinary skill in the pertinent art. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and market demand is sufficient motivation to combine references.

28. It is my understanding that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, common sense is a good reason for a person of ordinary skill to pursue known options when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions.

29. I further understand that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, it is my understanding that any need or problem known in the field at the time of invention and addressed by the patent can provide a reason for combining the limitations in the manner claimed.

5. THE RELEVANT ART AND LEVEL OF ORDINARY SKILL IN THE RELEVANT ART

30. I understand that obviousness is determined from the vantage point of a person of ordinary skill in the relevant art at the time of the alleged invention (“POSITA”). The ’362 patent is directed to a wideband receiver system “capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum.” Ex. 1101, 1:18-23. I understand that a person of ordinary skill in the art is one who is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity.

31. I believe that a person of ordinary skill in the art of the ’362 patent, at the time of the alleged invention of the ’362 patent, would have a degree in electrical engineering or a similar discipline, along with three-to-four years of experience with digital signal processing (DSP) and radio frequency (RF) tuning systems for satellite and/or cable communications. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. I

worked in the relevant field with such persons at, and leading up to, the time of the alleged invention of the '362 patent, and thus, I am familiar with the knowledge that such persons had at the time (*i.e.*, early 2009 or early 2010). At that time, I had a skill level that was at least as high as the skill level I describe above for a person of ordinary skill in the art of the '362 patent.

32. All of my statements in this declaration regarding what a person of ordinary skill in the art would have known, understood, appreciated, been motivated to do, etc., refer to a person of ordinary skill in the art, before the earliest claimed priority date of the '362 patent (which, as I discuss below, is April 17, 2009). Although some claims of the '362 are entitled to different priority dates, the level of ordinary skill in the art would not have changed significantly between April 17, 2009, and April 19, 2010, and in any event, would not have decreased.

6. CLAIM CONSTRUCTION

33. I understand that my analysis requires an understanding of the scope of the claims of the '362 patent. I understand that claim terms subject to *inter partes* review, absent some other definition provided in the patent, are given their ordinary meaning to a person of ordinary skill in the art in light of the patent specification. Therefore, in my analyses given below, I have assumed that all claim terms are given their ordinary interpretation as would have been understood by a POSITA reading the patent specification as of the priority date. I further understand that certain claim terms may be means plus function limitations. In particular, I understand that a

“means plus function” limitation should be interpreted to cover only the corresponding structure described in the specification that performs the recited function, and equivalents thereof. I also understand that a limitation will be presumed to be a means plus function limitation if (a) the claim limitation uses the phrase “means for”; (b) the “means for” is modified by functional language; and (c) the phrase “means for” is not modified by sufficient structure for achieving the specified function. I understand that a structure will be considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For example, a structure may be deemed to be a structural equivalent to the corresponding structure where the structure performs the same function in substantially the same way to achieve substantially the same result.

34. Though no claims in the '362 patent include “means for” language, I have been asked to consider a potential construction of “digital circuitry” in claim 1 as a means-plus-function limitation. Should the term be construed as such, the corresponding structure that performs the recited function for this limitation is illustrated in Figures 2 and 3, including complex mixers 250 and 300, and filters 260, 330, and 340. Ex. 1101, Figs. 2-3, 5:31-54, 6:7-58. As I discuss in my detailed analysis below, the prior art discloses this limitation whether or not it is construed as a means-plus-function limitation. Further, it is my opinion that the term “wideband” in the claims would be understood by a POSITA as “a band that carries

multiple channels,” in view of the specification of the ’362 patent that implicitly defines the term this way. For example, the ’362 patent states that a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” Ex. 1101, 1:24-27, 1:16-18 (“wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum”), 1:19-23 (“wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum and grouping them into a contiguous, or substantially-contiguous, frequency spectrum”). In my opinion, this is consistent with the ordinary and customary meaning of “wideband.”

35. It is my understanding that the ’362 patent was asserted in various litigations in California and in a litigation in Texas. In the Texas litigation, the court construed claim 11 of the ’362 patent as requiring that the “‘digitizing ...’ step must be performed before the ‘selecting ...’ step, and the ‘selecting ...’ step must be performed before the ‘outputting ...’ step,” but with “[n]o other order of steps” required. Ex. 1129 at 52. The parties in that case also agreed that “wideband analog-to-digital converter (ADC) module” should be given its plain and ordinary meaning. Ex. 1129 at 7-8. As I discussed above in this section, that plain and ordinary meaning is a band that carries multiple channels. Ex. 1101, 1:24-27, 1:15-23.

7. OVERVIEW OF THE '362 PATENT

36. The '362 patent describes a wideband receiver system 200 “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1101, 1:15-18.

37. The '362 patent states that the system groups the desired channels “into a contiguous, or substantially-contiguous, frequency spectrum” to “increase the dynamic range without requiring expensive data conversion, filtering and channel selection at the demodulator.” Ex. 1101, 1:18-23, 2:24-27. According to the '362 patent, a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” *Id.*, 1:24-27. Figure 2 is a “schematic block diagram of a wideband receiver system 200.” *Id.*, 4:16-18.

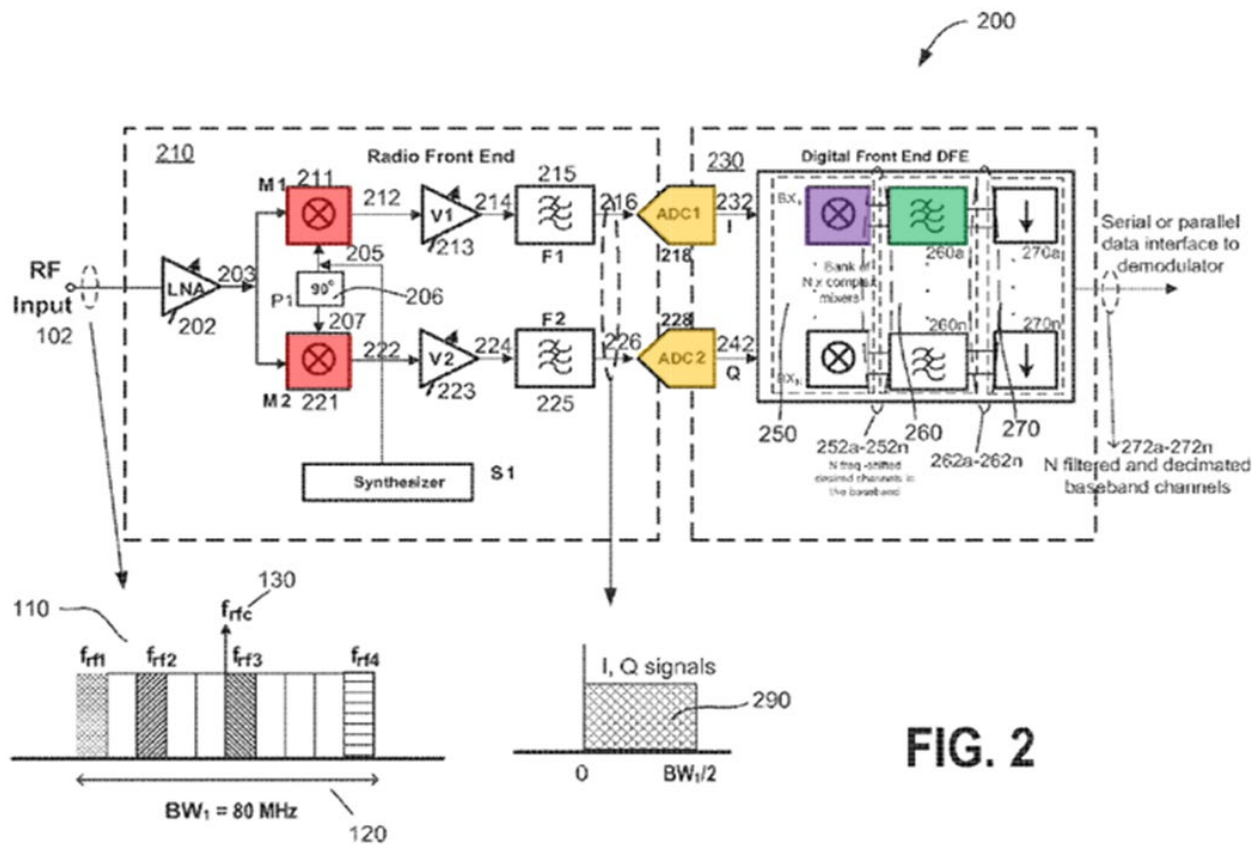


FIG. 2

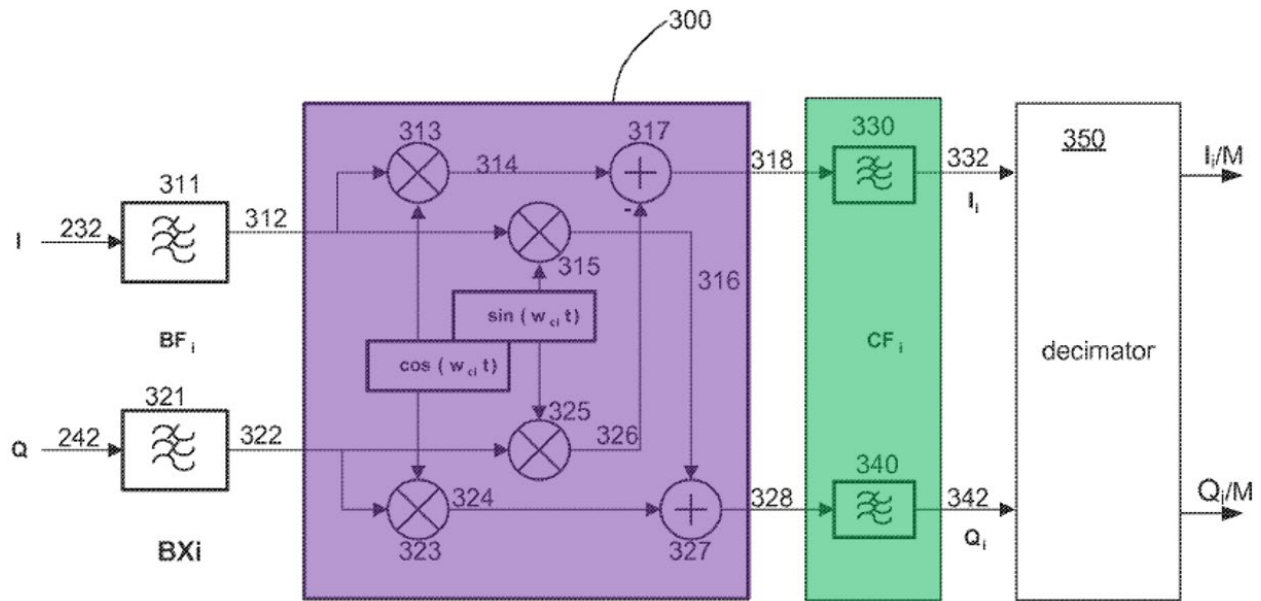
Ex. 1101, Fig. 2 (annotated)

38. The wideband receiver system 200 receives both desired and undesired television channels as frequencies dispersed within a frequency bandwidth BW_1 . Ex. 1101, Abstract, 4:19-22. Mixers “M1” and “M2” (red) “generate an in-phase signal 212 and a quadrature signal 222 that have a phase shift of 90° degree [sic] between them” and that have been downconverted to “the baseband or low intermediate frequency (IF) band.” Ex. 1101, 4:40-46, 2:45-49; *see also* 1:60-62. As I explain in Section 8.3.1 below, a mixer multiplies an input signal (frequency f_1) by a reference signal (frequency f_2) to produce new signals at the sum and difference frequencies (f_1+f_2 and f_1-f_2). The reduced frequency (f_1-f_2) version is output as the “down

converted” complex signal with real (I) and imaginary (Q) components. “[U]nwanted frequency components” are filtered from the in-phase signal and the quadrature signal by respective filters 215 and 225. Ex. 1101, 4:64-5:3. The filtered signals are then individually digitized by wideband analog-to-digital converters ADC1 and ADC2 (**gold**) to generate a digital in-phase (I) signal 232 and a digital quadrature (Q) signal 242. Ex. 1101, 2:49-51, 5:28-31. U.S. Provisional App. No. 61/170,526 (“the ’526 provisional”), which the ’362 patent incorporates by reference, admits that the left side of Figure 2 (up to and including ADC1 and ADC2) “is similar to conventional tuners.” Ex. 1107, at 5; Ex. 1101, 1:5-11.

39. The digital I and Q signals 232 and 242 are input to a digital front end 230, containing a bank of N complex mixers 250 (one of which is shown above in **purple**), where “N is an integer value corresponding to the number of desired RF channels.” Ex. 1101, 5:31-35. “Each of the N complex mixers ... extract[s] a different one of the desired channels” from the I and Q signals 232 and 242 and “frequency-shifts the extracted signals to the baseband frequency.” Ex. 1101, 5:49-52. The output of each mixer 250 connects to the input of an associated filter module 260 (one of which is shown above in **green**) that filters the frequency-shifted desired channel. Ex. 1101, 5:52-54.

40. Figure 3 “is a simplified circuit diagram of one of the signal paths 272a to 272n of digital front end 230” and shows elements in one of the rows of digital front end 230 in Figure 2. Ex. 1101, 5:62-64.



Ex. 1101, Fig. 3 (annotated)

41. Mixer 300 (**purple**) represents one of the complex mixers 250 and has multipliers 313, 315, 323, and 325 and adders 317 and 327. Ex. 1101, 6:7-17. “[C]omplex mixer 300 causes a frequency shift of the filtered components 312 and 322 to respective baseband signals 318 and 328 in the digital domain” by multiplying the I and Q signals by a frequency ω_{ci} that is chosen such that “each one of the desired channels embedded in the digital signals I 232 and Q 242 will be downshifted to the baseband.” Ex. 1101, 6:17-34. The baseband signals 318 and 328 are filtered by filters 330 and 340 (**green**) that are “one of the filters 260a-n” shown in Figure 2. Ex. 1101, 6:43-45. This exact structure was a conventional design, simply copied multiple times to downconvert multiple channels, respectively. *See* Section 8.3.1.

42. After decimation by a decimator 350 of the I, Q signals from the filters 330 and 340, “the N desired baseband channels will be sent as a serial or parallel

digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods.” Ex. 1101, 6:55-58. The ’362 patent does not provide any details of how $N \times 2$ signals (N channels, with an I and a Q signal for each channel) might be manipulated, combined, and/or otherwise processed between the decimators 270 and a demodulator. Rather, the ’362 patent admits that this is performed “according to commonly known methods.” *Id.*

7.1. Prosecution History

43. It is my understanding that U.S. Application No. 14/614,543 (“’543 application”), which issued as the ’362 patent, was filed on February 5, 2015. The ’543 application was filed with 20 claims including independent claims 1 and 11. Ex. 1104 at 32-35. On May 14, 2015, an Office Action rejected all claims on the basis of nonstatutory double patenting over claims 1-27 of U.S. Patent No. 8,526,898, and Applicant filed a terminal disclaimer on May 15, 2015. Ex. 1104 at 75-79, 90-99. An August 7, 2015, Notice of Allowance stated that the prior art failed to describe a wideband receiver system with “digital circuitry configured to select a plurality of desired television channels from the digitized plurality of frequencies and output said plurality of television channels to a demodulator as a digital datastream.” Ex. 1104 at 107.

44. Applicant filed a Request for Continued Examination (RCE) and an Information Disclosure Statement (IDS) on September 11, 2015. Ex. 1104 at 115-122. On October 5, 2015, a second Notice of Allowance issued.

45. It appears that none of Petrovic, Eidson, Rabaey, Jensen, or Takahiko was considered during prosecution of the '543 application. Ex. 1101, cover.

46. On September 20, 2023, Unified Patents, LLC filed a request, and in response the Office ordered reexamination (Control No. 90/019,255) on November 1, 2023, of independent claims 1 and 11 of the '362 patent. Ex. 1122 at 631-642. The reexamination is currently pending. It appears that none of Petrovic, Eidson, Rabaey, Jensen, or Takahiko has been cited in the reexamination. Ex. 1122, *passim*.

7.2. Earliest Priority Date for the Claims

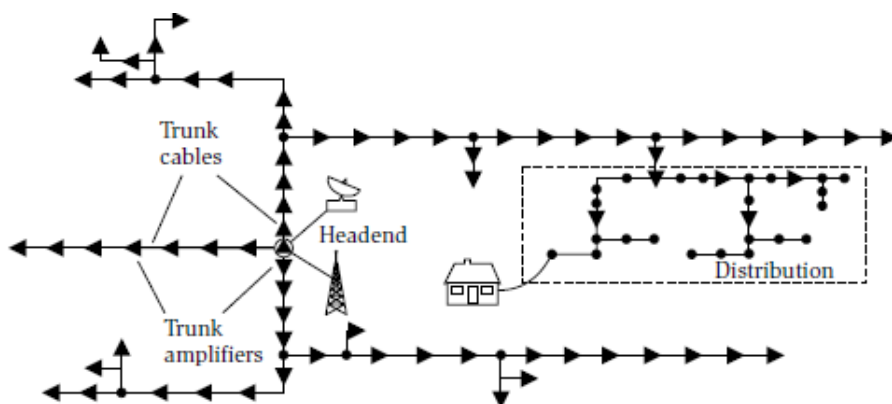
47. I understand that Application No. 14/614,543 (“the '543 application”), which eventually became the '362 patent, was filed on February 5, 2015. It is further my understanding that the '543 Application claims priority to a chain of applications that claim priority to the '526 provisional, which was filed on April 17, 2009. It is my understanding that the '362 patent asserts to be entitled to a priority date of the filing date of the earliest application from which the '362 patent claims priority, *i.e.*, April 17, 2009, which is the filing date of the '526 provisional. The earliest possible effective filing date for claims 1-8, 10-18, and 20 of the '362 patent is April 17, 2009, the filing date of the '526 provisional. However, the earliest possible priority date for claims 9 and 19 is April 19, 2010, the filing date of Application No. 12/762,900. This is because the '526 provisional is silent regarding a “finite impulse response filter” as recited in claims 9 and 19. Ex. 1107, *passim*. I understand that all

of the references that I rely on in this Declaration were published or filed before April 17, 2009, and are prior art to that date.

8. OVERVIEW OF THE PRIOR ART

8.1. Cable and Satellite Television Networks

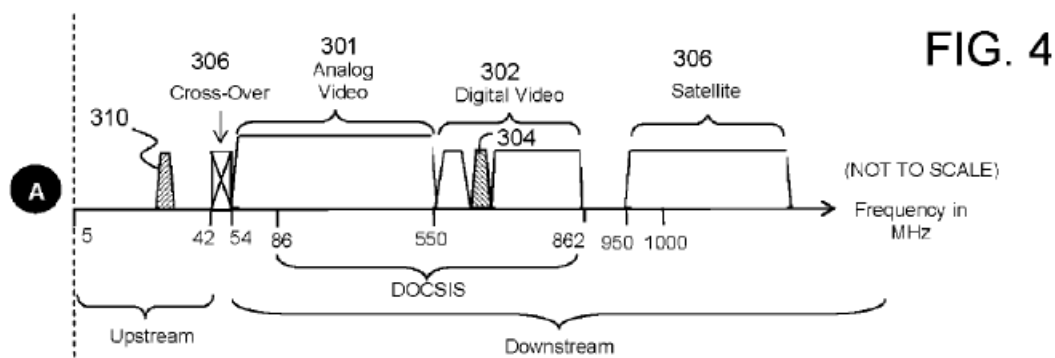
48. The origins of the cable and satellite television networks long predate the earliest claimed priority date (April 17, 2009) of the '362 patent. Cable television networks are entertainment distribution systems that allow consumers to access and enjoy various television channels. Ex. 1133 at 22. The cable television networks include one or more headends that are designed to broadcast and distribute, via coaxial cables, the data for the television channels as modulated radio frequency (RF) signals to multiple terminal equipment belonging to the consumers (e.g., television receivers, set-top boxes, data modems, digital video recorders, personal video recorders, and other terminal equipment). *Id.* at 22, 29-30, 40, 352; Ex. 1134 at 20-21. This is illustrated in Figure 1.1 of Ex. 1133.



Ex. 1133 at 34, Fig. 1.1 (Excerpted)

RF is the frequency range starting from 10 kHz to 100,000 MHz in the electromagnetic spectrum; signals having frequencies from this RF range are used for data transmission (wired or wireless) between devices. *See* Ex. 1115 at 7. The transmissions between the headends and the terminal equipment are governed by various well-known industry standards, including Data Over Cable Systems Interface Specification (DOCSIS). Ex. 1121 at 2-5, Fig. 1-2; Ex. 1133 at 27, 211-212.

49. Consumers can also access television channels from satellites via conventional home satellite television systems. Ex. 1135, 1:30-31; Ex. 1136, [0006]. Such home satellite television systems typically include a fixed dish antenna that receives television channels in modulated RF signals, as well as a satellite receiver or set-top box designed to process and demodulate the modulated RF signals. Ex. 1135, 1:31-35; Ex. 1136, [0013]. Satellites may also be used to distribute the television channels to headends of cable television networks, which are then redistributed to the consumers. Ex. 1133 at 262, 280-282; Ex. 1136, [0009].



Ex. 1137, Fig. 4 (Excerpted)

50. Figure 4 of Exhibit 1137 (partially reproduced above) illustrates the RF spectrum usage of television channels from cable and satellite television networks. Ex. 1137, [0079]-[0080]. In North America, television channels from cable television networks occupy the RF spectrum from 54 to 864 MHz, with digital channels occupying the RF spectrum above 550 MHz. Ex. 1133 at 413, 503; Ex. 1137, [0079]-[0080]. In 1941, the National Television System Committee, established by the United States Federal Communications Commission, set a standard that each television channel should be allocated 6 MHz of RF bandwidth and that the set of allocated television channels should occupy the RF spectrum in a contiguous manner. Ex. 1121 at 1, 23-24; Ex. 1133 at 45, 413, 515-520.

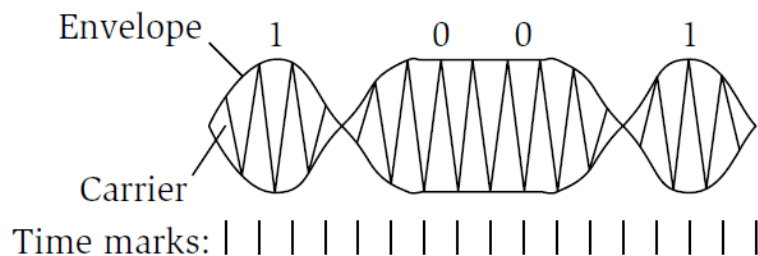
51. Television channels from satellite networks occupy various bands in frequencies greater than 950 MHz. Ex. 1135, 1:37-48; Ex. 1137, [0079]-[0080]. Signals in satellite bands are sent to a satellite receiver or set-top box, with the satellite bands carrying multiple transponder channels and each transponder channel carrying a number of different television channels. Ex. 1135, 1:37-48.

8.2. Modulated RF Signals

52. Modulation is a method where an RF carrier signal is varied (e.g., in amplitude, frequency, and/or phase) with information to be transmitted. Ex. 1133 at 155. The information to be transmitted can be digital data comprising of bits “1” and “0,” such as the digital data of television channels for transmission from headends of cable television networks or subscriber locations. *Id.* One of the main goals of

modulation is to squeeze as much data into the allocated RF bandwidth as possible, and that objective, known as spectral efficiency, measures how quickly data can be transmitted in an assigned RF bandwidth. *Id.* at 156. The unit of measurement of spectral efficiency is bits per second per Hz (b/s/Hz). *Id.* As I discuss below, by the earliest claimed priority date of the '362 patent, multiple modulation techniques facilitating high spectral efficiencies were known to a POSITA.

8.2.1. Biphase Shift Keying



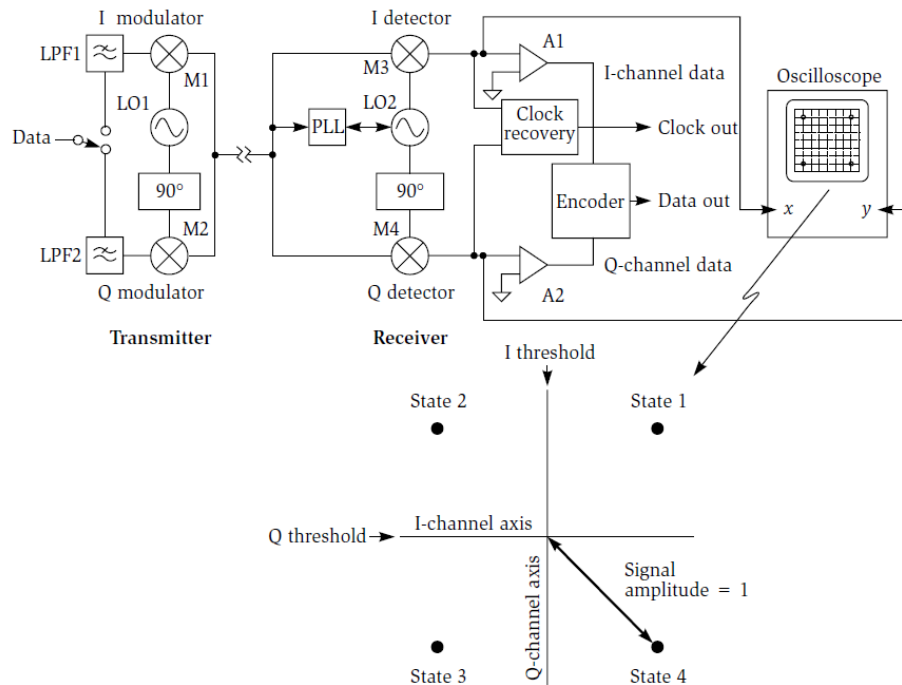
Ex. 1133 at 161, Fig. 4.3 (Excerpted)

53. Biphase shift keying (BPSK) is a simple form of modulation that can be used in digital cable and satellite television networks, where the phase of an RF signal is shifted 180° in phase between transmission of bit “0” and bit “1.” Ex. 1133 at 160-161, Fig. 4.3 (partially reproduced above). The spectral efficiency of BPSK modulation is 1 bit/s/Hz. *Id.* at 156.

8.2.2. Quadrature Phase Shift Keying (QPSK)

54. In Quadrature Phase Shift Keying (also called 4-Quadrature Amplitude Modulation (4-QAM)), digital data is split into two components, an I (in-phase) component and a Q (quadrature) component. Ex. 1133 at 163-164, Fig. 4.4

(reproduced below). The same RF carrier signal is used for each component, but the phases of the two signals in the two components are 90° apart or in quadrature. *Id.* Signals in quadrature are orthogonal and do not interfere with one another. *Id.* Quadrature modulation takes advantage of this principal by combining two signals in quadrature for a combined output signal. *Id.* In quadrature modulation, digital data are broken into a discrete number of symbols, which are used to convey information. *Id.* at 164-165. These symbols are mapped to a discrete set of magnitude and phase values on an I/Q constellation, which are referred to as constellation points. *Id.* For example, in BPSK, each symbol can only represent a bit “0” or a bit “1” because the constellation of BPSK modulation has just two possible constellation points representing two possible states, or symbols, where each symbol represents a single bit of information. The constellation of QPSK modulation has four constellation points representing four different states, or symbols: state 1 (bits “00”), state 2 (bits “01”), state 3 (bits “11”), and state 4 (bits “11”). *Id.* QPSK can, therefore, transmit 2 bits per symbol. *Id.* The RF carrier signals in each of the I and Q components are encoded with one of the two bits of the symbol. *Id.* at 163. Therefore, QPSK can transmit twice as much data using the same amount of bandwidth as BPSK, or it could transmit the same amount of data using half the bandwidth. *Id.* at 156.



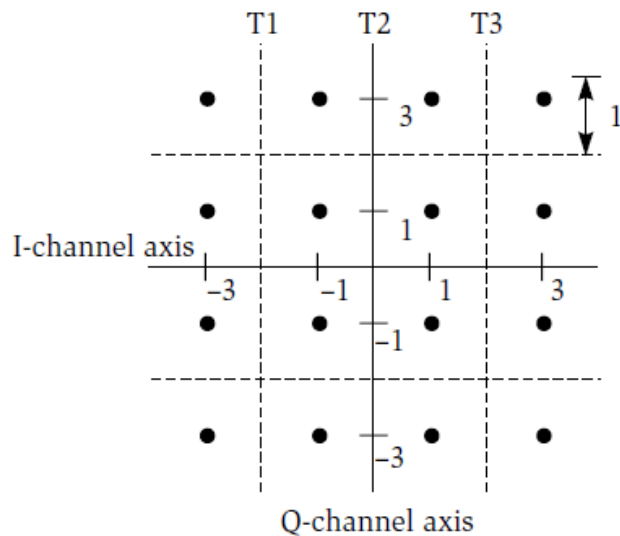
Ex. 1133 at 164, Fig. 4.4

55. After the two RF carrier signals from the two components I and Q are modulated, the RF carrier signals are combined for transmission to the receiver. Ex. 1133 at 163. At the receiver, the received combined signal is split back into the I-component and the Q-component by two mixers, M3 and M4. *Id.* at 163-164. The separation back into I/Q components allows the encoder inside the receiver to map the two components onto the QPSK I/Q constellation and interpret which of the four possible symbols are encoded in the components. *Id.* at 164.

56. A POSITA would have been well aware that satellite television networks primarily used QPSK modulation. Ex. 1133 at 280; Ex. 1136, [0071], [0075]. Satellite transponders that transmit RF signals to headends and dish antennas are simply a frequency translator and a power amplifier, and for the sake of

efficiency, it was preferred to use modulation formats that do not depend on amplitude changes to communicate information. Ex. 1133 at 280. QPSK modulation met this requirement of satellite transponders. *Id.*

8.2.3. 16-Quadrature Amplitude Modulation (QAM), 64-QAM, and 256-QAM

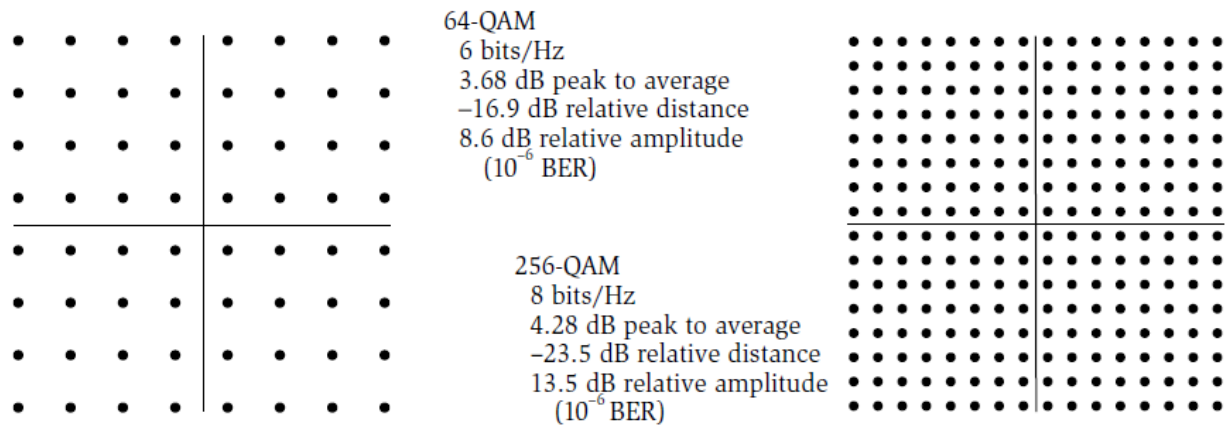


Ex. 1133 at 167, Fig. 4.5 (Partial Excerpt)

57. Modulation schemes with greater numbers of constellation points are able to transmit more information per symbol. Ex. 1133 at 166-169. The next denser known modulation format after QPSK was 16-QAM, where data is split into I and Q components and carried by two RF signals in quadrature. *Id.* at 166. However, the 16-QAM I/Q constellation has sixteen different states (as illustrated by the sixteen dots in Figure 4.5 of Ex. 1133, partially reproduced above), where each state is a symbol that contains one of 16 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 4 bits and, therefore, can represent values from

“0000” to “1111.” *Id.* at 166-167. The spectral efficiency of 16-QAM is 4 bit/s/Hz.

Id. at 168, Fig. 4.6.



Ex. 1133 at 168, Fig. 4.6 (Partial Excerpt)

58. Similarly, the I/Q constellation of 64-QAM (illustrated by Figure 4.6 of Ex. 1133, partially reproduced above) has sixty-four different states, where each state is a symbol that contains one of 64 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 6 bits (representing values from “000000” to “111111”), and the spectral efficiency of 64-QAM is 6 bit/s/Hz. *Id.* The I/Q constellation of 256-QAM has 256 different states, where each state is a symbol that contains one of 256 different combinations of amplitude and phase levels. *Id.* Each symbol contains up to 8 bits (representing values from “00000000” to “11111111”), and the spectral efficiency of 256-QAM is 8 bit/s/Hz. *Id.*

59. DOCSIS (finalized in 1997), DOCSIS 1.1 (finalized in 2001), and DOCSIS 2.0 (finalized in 2002) mandate the use of either 64-QAM or 256-QAM for

downstream data transmission from headends to consumers' terminal equipment. Ex. 1133 at 168, 213-214. Therefore, a POSITA would have known that terminal equipment receiving signals from headends of cable television networks were required to demodulate signals that have been modulated using 64-QAM or 256-QAM. Moreover, a POSITA would have understood the relative benefits of using 64-QAM or 256-QAM versus BPSK, as 64-QAM and 256-QAM offer higher rates of spectral efficiencies than BPSK. *Id.* at 156.

8.3. Radio Receivers or Tuners for Cable and Satellite Television Networks

60. As discussed in Section 8.1, it was well-known to a POSITA that consumer terminal equipment (e.g., television receivers, cable set-top boxes, satellite set-top boxes, digital video recorders, personal video recorders, and other terminal equipment) receive modulated RF signals from headends and satellites. Ex. 1133 at 22, 29-30, 40, 352; Ex. 1135, 1:30-35; Ex. 1136, [0006]. A POSITA was also aware that consumer terminal equipment included a radio receiver (also known as a tuner) that received the RF signals and processed them in such a way that a demodulator could demodulate the RF signals to recover the digital data encoded in the RF signals. Ex. 1133 at 408-411, Fig. 22.1; Ex. 1135, 1:35-37, 1:49-52; Ex. 1136, [0018], [0020]-[0021].

61. Cable television RF receivers concurrently receive RF signals for multiple digital television channels allocated in the RF frequency spectrum of 550

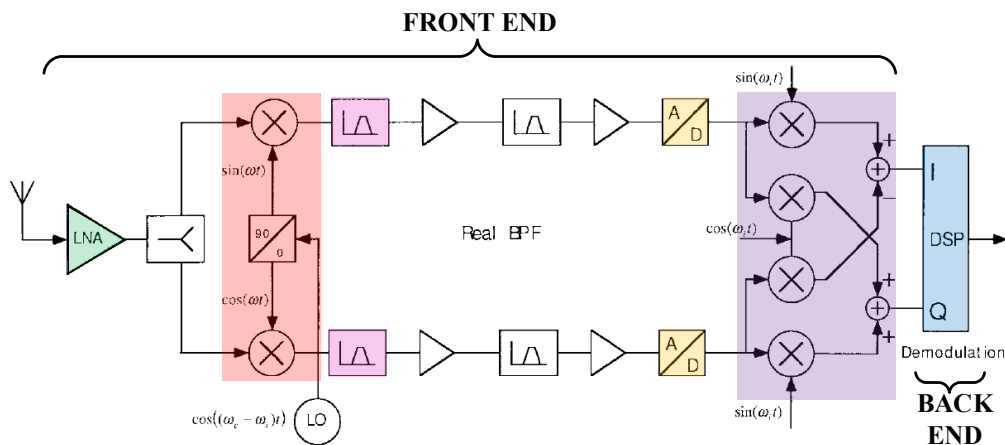
to 862 MHz. Ex. 1133 at 413, 503; Ex. 1137, [0079]-[0080], Fig. 4. Satellite RF receivers concurrently receive RF signals for multiple television channels allocated in the RF frequency spectrum above 950 MHz. Ex. 1135, 1:37-47; Ex. 1137, [0080]. Furthermore, the POSITA was aware that cable and satellite television radio receivers could tune (i.e., select and extract) signals for certain desired television channels (e.g., channels selected for viewing by a consumer) from the received RF frequency spectrum. Ex. 1133 at 299; Ex. 1136, [0020]-[0021]; Ex. 1142, 4:10-36; Ex. 1144, 1:51-58.

62. One type of receiver is known as an IF (intermediate frequency) receiver, and in particular, a type of receiver known as a low-IF receiver. By the earliest claimed priority date of the '362 patent, IF receivers, including low-IF receivers, were well-known in wireless communication systems for their high performance and low power consumption. Ex. 1125 at 270, 272; Ex. 1134 at 17, 65-74. It was also known to a POSITA, by the earliest claimed priority date of the '362 patent, that low-IF receivers were conventionally used for receiving RF signals from cable television networks and satellite television networks. Ex. 1135, 1:49-61; Ex. 1138, [0022]-[0023], [0029]-[0030], [0042].

63. IF receivers have been used for a long time, and their way of operating is very well known. Ex. 1125 at 270. In general, IF receivers operate by initially downconverting RF signals, which may comprise multiple RF sub-bands each carrying one or more separate signals, from its RF carrier frequency to an

intermediate frequency (IF). *Id.* The downconverted signals can be demodulated at the IF or further downconverted to baseband before being demodulated. *Id.* at 270, 279. When a band of signals is at baseband, the low end of the band is near zero frequency in the frequency spectrum or includes zero frequency. Ex. 1115 at 4. Intermediate frequency falls below the frequency of the RF signals but above the baseband frequency. Ex. 1134 at 22. Low-IF receivers initially downconvert to an IF that is at a relatively low frequency, such as a few hundred kilohertz. Ex. 1125, at 269.

8.3.1. Architecture of Low-IF receivers



Ex. 1125, Fig. 22(a) (excerpted and annotated)

64. Low-IF receivers (illustrated by Figure 22(a) of Ex. 1125, excerpted and annotated above) comprise two main portions: a front end that performs frequency downconversion of the RF signals, and a back end including a digital signal processor (DSP) that performs the actual demodulation of the RF signals. Ex.

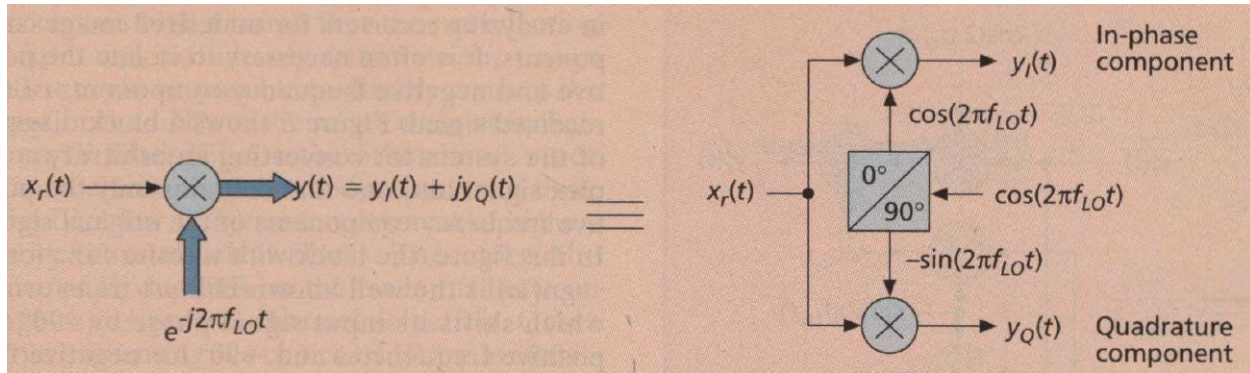
1134 at 22-23. The demodulation technique that will be used in the DSP depends on the modulation technique used to modulate the incoming RF signals, and therefore, if the incoming RF signals are modulated using QPSK or QAM techniques (which modulate I and Q components), then demodulation is typically performed to extract the I and Q components of the incoming RF signals. *Id.* at 23. DSPs typically perform demodulation on baseband signals. *Id.*; Ex. 1139 at 11; Ex. 1125 at 269, 279. However, the received RF signals are at much higher (non-baseband) frequencies. *Id.* Therefore, the front end must produce baseband quadrature I and Q components of the incoming RF signals to be usable by the DSP. Ex. 1134 at 23.

65. Still referring to Figure 22(a) of Ex. 1125 (reproduced and annotated above), in the front end of a low-IF receiver, the incoming RF signals are first amplified by a front-end low noise amplifier (LNA) (**green**) to provide enough gain to boost the received RF signal levels to an acceptable level such that further signal processing can be performed on the received RF signals; the LNA compensates for the attenuations of the RF signals during the transmission of the RF signals from another device. Ex. 1134 at 41; Ex. 1139 at 16. The RF signals are downconverted to baseband signals in two steps, where the first step (**red**) converts the RF signals to Intermediate Frequency (IF) signals before one or more analog-to-digital converters (ADCs) (**gold**) convert IF signals to digital signals, and the second step (**purple**) converts the digital signals of IF to baseband signals. Ex. 1125 at 270, 272; Ex. 1134 at 23.

66. In the first downconversion step, from RF to IF, the incoming RF signals are split and then down-converted by a quadrature downconverter (**red**), also referred to as a complex mixer or complex multiplier, which comprises two real mixers to produce I and Q components of the signals in IF. Ex. 1134 at 65-72; Ex. 1139 at 11 (“Two mixers are needed to retain both the amplitude and phase of the original modulated signal: one for the in-phase (I) and another for a quadrature (Q) baseband output.”); Ex. 1118 at 133-134. For example, as explained in an article by Shahriar Mirabbasi and Ken Martin in IEEE Communications Magazine in November 2000:

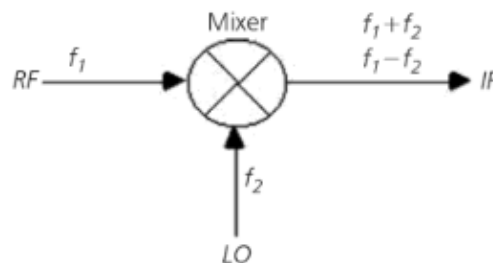
The realization of a multiplier for mixing a real signal with a complex exponential requires two real multipliers, as illustrated in Fig. 2. The real and imaginary parts of the mixer output are called the in-phase (I) and quadrature (Q) components of the downconverted signal (since cosine and sine are in quadrature). In Fig. 2 the frequency of the complex exponential is chosen to be the same as the center frequency of the passband signal, for comparison with case 2 in Fig. 1. In this case there is no image problem associated with the complex mixer.

Ex. 1118 at 134 (emphasis added).



Ex. 1118, Fig. 2

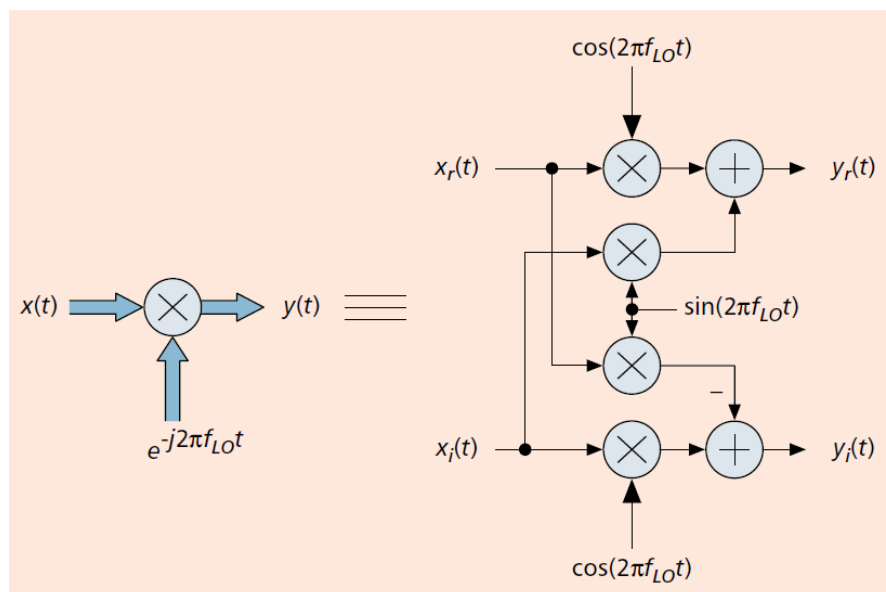
The term “mixer” and “multiplier” are often used interchangeably to refer to an analog or digital electrical circuit (represented by the symbol $\otimes$) that multiplies a modulated input signal (e.g., an RF signal) at frequency f_1 and a reference signal (e.g., from a local oscillator LO) at frequency f_2 , which produces new signals at the sum and difference of the input frequencies, f_1+f_2 and f_1-f_2 . Ex. 1139 at 12-13. This is illustrated in Figure 8-9 from Ex. 1139.



Ex. 1139, Fig. 8-9

By filtering out the signal with the sum (f_1+f_2), and passing only the signal with difference (f_1-f_2), the center frequency of the modulated input signal is reduced, or down-converted. A mixer/multiplier is “complex,” if it multiplies the input signal by a complex signal, having real and imaginary parts, to produce in-phase and

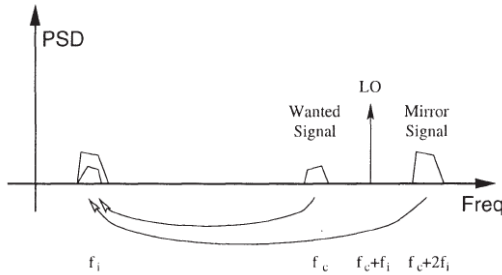
quadrature signals. Ex. 1118 at 133. A complex mixer/multiplier can include two real mixers/multipliers when the input signal is real and the reference signal is complex as shown in Figure 22(a) of Ex. 1125 above, or it can include four real mixers/multipliers if both the input signal and reference signal are complex as shown below. Ex. 1118 at 133-134, Fig. 3. As shown in the figure below, the symbol $\otimes$ is used interchangeably to refer to a complex mixer (left) or individual real multiplier/mixers (right) that make up a complex mixer.



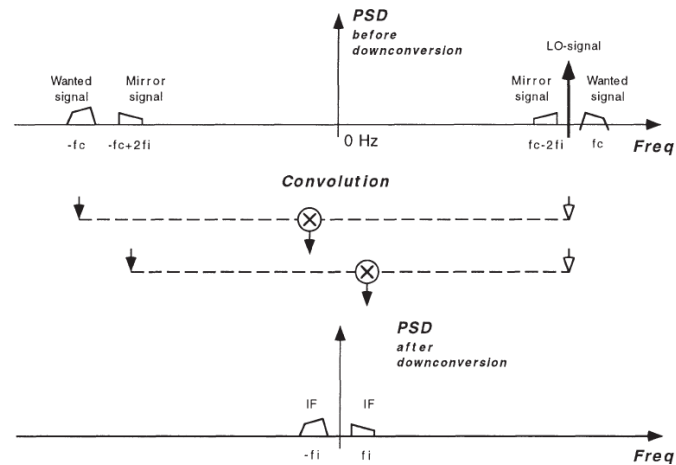
Ex. 1118, Fig. 3

Referring back to Figure 22(a) of Ex. 1125, the RF signals could also be downconverted using a single mixer and a sinusoidal signal (as shown by Figure 2.6 of Ex. 1134, reproduced below); however, the main disadvantage of mixing an RF signal of frequency f_c with just a single sinusoidal signal $\cos(2\pi f_{LO}t)$ to downconvert

to intermediate frequency f_i is that a second mirror signal of frequency f_c+2f_i is also downconverted to frequency f_i . Ex. 1134 at 24.



Ex. 1134 at 26, Fig. 2.6



Ex. 1134 at 67, Fig. 3.23

67. It was known that the mirror signal problem could be avoided by mixing the incoming RF signals with a complex signal, $\cos(2\pi f_i t) + j\sin(2\pi f_i t)$. Ex. 1134 at 28, 43; Ex. 1139 at 13. Mixing with such complex signals shifts a wanted RF signal at frequency f_c to frequency f_i while the unwanted mirror (or image) frequency signal at f_c+2f_i is shifted to frequency f_i . *Id.* Furthermore, separately mixing the RF signals with the signal $\sin(2\pi f_i t)$ produces the I-components of the RF signals, while mixing with $\cos(2\pi f_i t)$ produces the Q-components for the RF signals, and both of these components are needed for the DSP at the back end to ultimately demodulate the incoming RF signals. Ex. 1134 at 23. Filters (pink) can be used after the first stage of downconversion to filter out unwanted mirror signals. *Id.* at 28; Ex. 1139 at 17.

68. One could directly downconvert the incoming RF signal to baseband in the analog part of the RF receivers by using quadrature downconverters such that a second downconversion stage is not needed before the signals are forwarded to a demodulator; for example, zero-IF receivers perform such direct conversion. Ex. 1134 at 28; Ex. 1150 at 13-14. However, a significant problem in direct downconversion is the introduction of parasitic baseband signals at baseband, known as DC-offset, in the output of the quadrature downconverters. Ex. 1118 at 136; Ex. 1134 at 29; Ex. 1150 at 14-15. This DC-offset is mainly the result of the crosstalk between the incoming RF signals and the complex signal of the quadrature downconverters, the self-mixing phenomenon of the local oscillator producing the complex signal, the leakage of the complex signals to the input of the LNA, and/or capacitive/inductive bondings between the different components of the RF receivers. Ex. 1118 at 136; Ex. 1134 at 29, 55-62; Ex. 1150 at 14-15. Such DC-offset issues are not present in low-IF receivers as the output of the first stage of mixing is at IF and not at baseband, and the downconversion at the second step is digitally performed. Ex. 1118 at 137-138; Ex. 1134 at 18. Furthermore, in the analog part of the RF receivers, mismatches between the two components of the complex signal and differences along the two branches of quadrature mixers and any following amplifiers and filters can cause the corruption of the I/Q components of the downconverted signals. Ex. 1118 at 138; Ex. 1134 at 29, 42, 55. However, such

mismatches are not an issue in the second digital downconversion step. Ex. 1118 at 137; Ex. 1134 at 74, 76.

69. Analog-to-digital converters (ADCs) (**gold**) were commonly used in RF receivers for either IF or baseband signal sampling. Ex. 1139 at 18. Therefore, referring again to Figure 22(a) of Ex. 1125 (reproduced and annotated above), the quadrature downconverter (**red**) downconverts the incoming RF signals to produce I and Q components in IF before two ADCs separately digitize the IF I and Q components. Ex. 1134 at 42. The digitized I and Q components are further downconverted to baseband by a digital complex mixer (**purple**) (comprising four digital mixers represented by the symbol $\otimes$ and two summers) before being forwarded to the DSP (**blue**).

8.3.2. Channel Selection based on Digital Filters

70. RF receivers receive RF signals for multiple television channels from cable and satellite television networks. Ex. 1135, 1:37-47. An important function for RF receivers is the ability to tune or filter out the signals for a desired television channel from the received RF signals such that only the signals of the desired television channels are demodulated. Ex. 1133 at 510. A POSITA would have known that digital filters based on digital signal processing are far superior to analog filters as digital filters do not suffer from manufacturing variations or aging, are easily programmable and tunable, have low power consumption, are unaffected by environmental influences, and have a superior performance-to-cost ratio. Ex. 1141

at 43. Digital filters, such as low pass filters and band pass filters, were known to select signals of desired television channels in RF receivers. Ex. 1135, 11:13-23, Fig. 7A; Ex. 1142, 6:5-8, Fig. 1B; Ex. 1143, 5:13-29, 5:46-53; Ex. 1150 at 44, 48.

- Low pass filter: A low-pass filter is a filter that passes signals with a frequency lower than a selected cutoff frequency (ω_c) and attenuates signals with frequencies higher than the cutoff frequency. Ex. 1141 at 14.

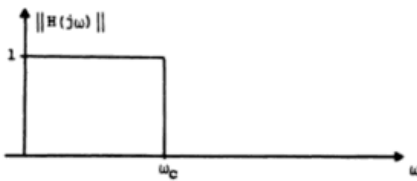


Fig. 1.23. Ideal LP filter magnitude frequency response.

Ex. 1141, Fig. 1.23

- Bandpass filter: A bandpass filter allows a specific range of frequencies (ω_1 to ω_2) to pass through while attenuating frequencies outside that range. Ex. 1141 at 21.

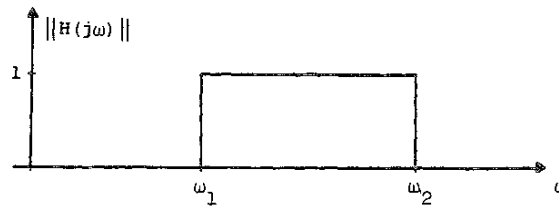


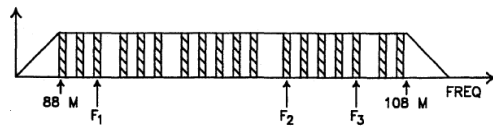
Fig. 1.27. Ideal BP filter.

Ex. 1141, Fig. 1.27

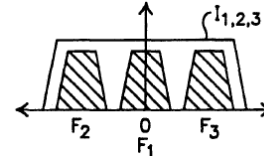
A bandpass filter allows signals within a selected frequency range (e.g., signals for a selected television channel) to be isolated from undesired signals from outside the range. Ex. 1143, 5:12-15; Ex. 1150 at 44. Signals for a desired television channel can also be isolated from signals of undesired television channels by downconverting all the signals such that the signals for the desired television frequency are placed at baseband and then applying a low pass filter function to isolate the signals of the desired television channel. Ex. 1143, 5:46-50; Ex. 1150 at 48. However, low pass filters are preferred over bandpass filters as low pass filters require fewer computational steps and, therefore, less computational power than bandpass filters. Ex. 1150 at 33, 48-49. It was also known to a POSITA that low pass filters and bandpass filters use well-known digital architectures of Finite Impulse Response (FIR) filters. Ex. 1141 at 24-63; Ex. 1143, 5:15-17; Ex. 1150 at 44.

71. Some receivers may allow signals of two or more desired channels to be filtered out such that consumers may enjoy a feature called picture-in-picture, where a small window showing one of the desired television channels is inserted into a larger window showing another one of the desired television channels. Ex. 1133 at 906; Ex. 1135, 4:37-43. For example, Khoini-Poorfard (Ex. 1135) describes using two RF receivers to filter and demodulate two television channels such that the filtered television channels can be used in the picture-in-picture feature. Ex. 1135, 4:37-43, 11:13-23, Fig. 7A.

8.3.3. Stacking of Desired Channels before Demodulation



Ex. 1144, Fig. 1



Ex. 1144, Fig. 6

72. Khoini-Poorfard (Ex. 1135) describes using two RF receivers that individually filter and demodulate two television channels. Ex. 1135, 4:37-43, 11:13-23, Fig. 7A. Kelly (Ex. 1144) describes an RF receiver that demodulates multiple desired channel bands without expensive hardware requirements and hardware duplications. Ex. 1144, 2:42-50. The RF receiver in Kelly digitizes RF signals comprising multiple desired RF bands in an RF spectrum (e.g., bands F_1 , F_2 , and F_3 in Figure 1 of Ex. 1144 reproduced above) and subjects the digitized signals to multiple frequency translations such that the desired bands are adjacent to each other (e.g., bands F_1 , F_2 , and F_3 are adjacent to each other in Figure 6 of Ex. 1144 reproduced above). *Id.*, 2:51-58, 4:38-40, 4:54-5:9. The desired frequency bands are then digitally separated, demodulated and processed to provide multiple outputs from the single receiver. *Id.*, 2:58-60.

8.3.4. Decimation

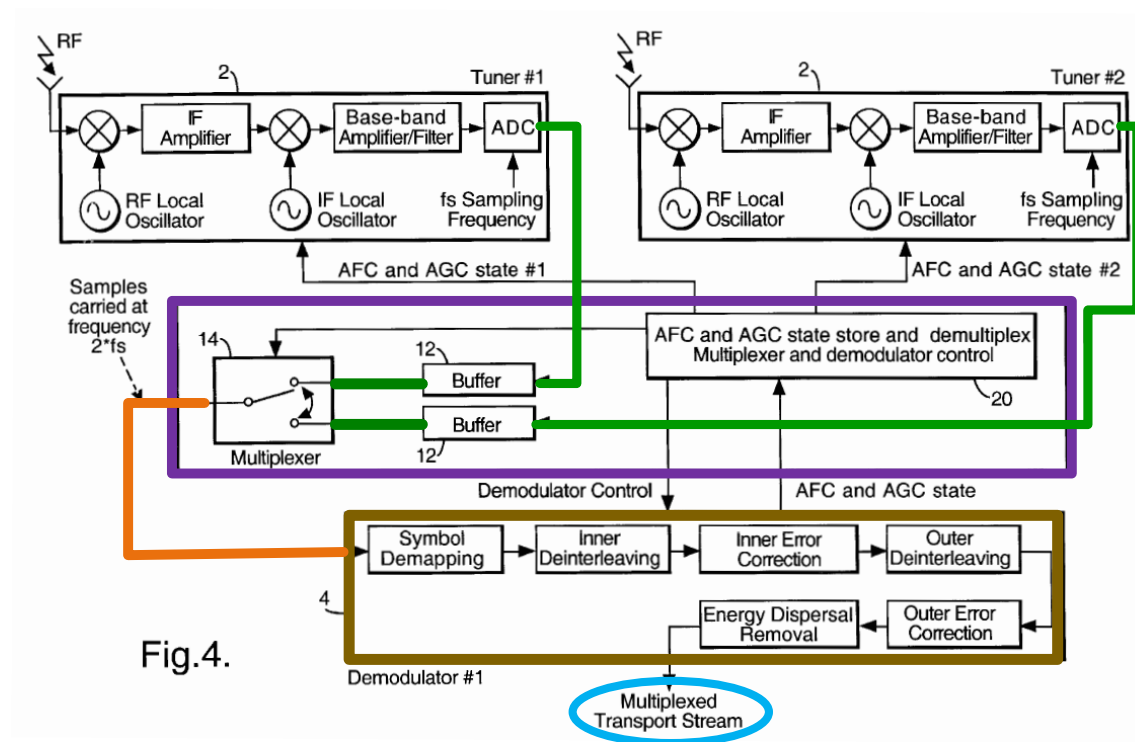
73. ADCs in RF receivers convert incoming RF signals to digital signals by sampling the RF signals at a rate that is at least twice the highest frequency of the RF signals. Ex. 1145 at 70. The reason for the high sampling rate is to prevent information loss during digitization; the Nyquist theorem specifies that a sinusoidal

function in time or distance can be regenerated with no loss of information as long as it is sampled at a frequency greater than or equal to twice per cycle. *Id.*; Ex. 1133 at 98-99. That is, if you digitize an analog signal by sampling the signal at two or more times the highest frequency contained in the signal, that signal can be theoretically converted back to the exact same analog signal by passing the signal through a low pass filter. The Nyquist theorem is a fundamental principle that enables us to digital signal process (DSP) analog signals (radio waves, sound waves, vibrations, etc.) that exist in the real world. Ex. 1133 at 98-101. Because the sample rate of the resulting signal from an ADC may be too high for subsequent DSP processing, decimation is typically performed on the sampled signals at baseband to lower the sampling rate. Ex. 1134 at 104; Ex. 1145 at 70. Decimation is a well-known process that reduces the original sample rate of a signal to a lower rate. Ex. 1145 at 14-15. A decimation filter can be implemented in a digital signal processing block of an RF receiver after the second downconverting step. Ex. 1134 at 104; Ex. 1145, Fig. 3.57 (at 71); Ex. 1146, 2:51-57.

8.3.5. Demodulation of Multiple Channels

74. A POSITA would have been well aware that either a single demodulator or multiple demodulators can perform demodulation of signals for multiple selected television channels. Ex. 1119, 1:67-2:7, 2:32-35, 2:61-63, 3:50-52; Ex. 1144, 7:53:57. For example, Carson (Ex. 1119) describes a multichannel time-shared demodulator that demodulates the signals of

multiple channels concurrently using time division multiple access (TDMA) techniques. Ex. 1119, 1:67-2:7, 2:32-35, 2:61-63, 3:50-52. Kelly (Ex. 1144) illustrates an RF receiver that demodulates two channels separately with two demodulators. Ex. 1144, 7:53:57. Another example is shown in Azenkot (Ex. 1175), which describes a single shared demodulator for demodulating multiple time-division multiplexed QAM channels in a cable modem termination system (CMTS) in a hybrid fiber-cable (HFC) network. Ex. 1175, Abstract, 1:6-14, 6:14-22, 6:30-37; 7:15-20, 32:53-33:14. As another example, Shadwell (Ex. 1176) discloses the system shown below, which receives multiple digitized downconverted channels (**green**), which are time-multiplexed together (**purple**) into a data stream (**orange**) that is output to a single demodulator (**brown**), which then provides a demodulated time-multiplexed output (**light blue**).



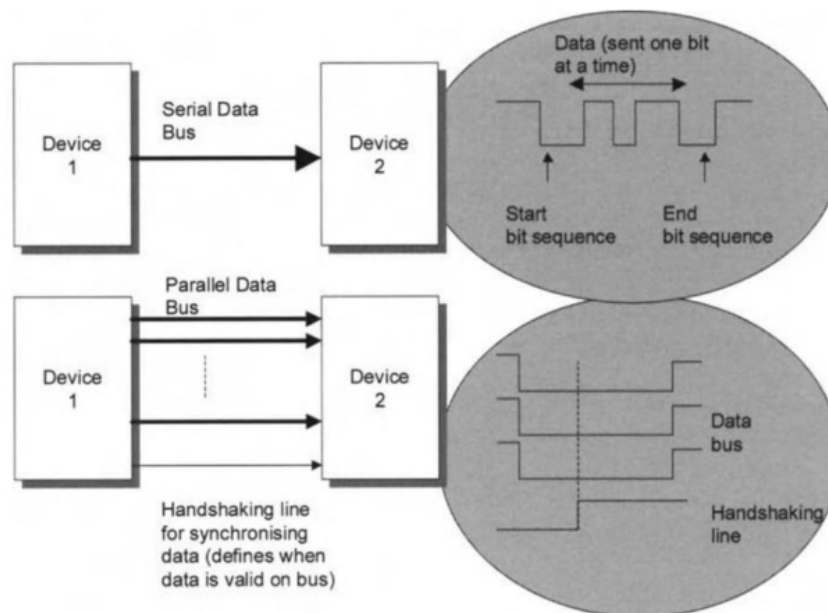
Ex. 1176, Fig. 4 (annotated)

A POSITA would have been well aware that single demodulator at the time, such as those disclosed in Carson, Azenkot, and Shadwell, were capable of demodulating multiple selected channels. Ex. 1176, Abstract, 2:28-52, 3:6-17, 4:21-32, 6:19-37, Figs. 1a, 1b, 2, 4. The use of a single demodulator would reduce cost of the system, and enable certain functionality, such as providing a transport stream including two demodulated television channels, for example, for decoding a picture-in-picture stream. Ex. 1176, 2:13-26, 2:53-59.

8.4. Serial vs. Parallel Data Communication

75. As described throughout subsection 8.3 above, the different components of an IF receiver, including a low-IF receiver, were known to a POSITA

prior to the '362 patent. It was also known to the POSITA by the earliest claimed priority date (April 17, 2009) of the '362 patent that the different components of low-IF receivers, such as the front end and the back end, could be fabricated on the same chipset or as different chipsets, and different types of buses could later connect the chipsets. Ex. 1134 at 23, 183; Ex. 1148 at 16. Data buses were known to pass data between electronic components. Ex. 1148 at 16. The data could be either passed in a serial manner by passing one bit at a time in a single bus, or in a parallel manner where several bits are transmitted simultaneously and each along its own separate channel. *Id.*; Ex. 1149, 1:10-28.



Ex. 1148 at 53 Fig. 2.3

76. A POSITA would have known that data transmission using parallel data buses offers a much higher data transmission rate than data transmission using a serial data bus. Ex. 1148 at 16. However, the parallel bus structure requires a larger

number of conductors and more space on the chip. Ex. 1149, 1:32-40. Furthermore, due to natural aberrations in the structure of each bus (e.g., resistance), signals in parallel data buses do not arrive at the same time, creating a problem known as “skew.” *Id.* at 1:24-40. This problem becomes more severe as the distances between chipsets increase. *Id.*

77. Therefore, it was well known before the claimed priority date of the ’362 patent to use technologies such as those described above in 8.3-8.4 to broadcast data for television channels using QPSK and QAM modulated RF signals, and to use radio frequency receivers and tuners, such as low-IF receivers, to receive and process the RF signals to select one or more desired television channels. As also discussed above, such processing was well-known to include channel stacking, downconversion, channel selection (e.g., filtering), demodulation, and decimation, as well as parallel and serial bussing between receiver components.

8.5. Petrovic (Ex. 1108)

78. U.S. Patent Application Publication No. 2009/0290659 (“Petrovic”) (Ex. 1108) is a publication of U.S. Application No. 12/414,892 (“the ’892 Application”), which claims priority to, and incorporates by reference, U.S. Provisional Patent Application No. 61/054,886 to Petrovic et al. (“Petrovic ’886”, Ex. 1109), which was filed May 21, 2008. Ex. 1108, cover, [0001]. In my analysis below, I provide parallel citations where appropriate to both Petrovic ’886 (Ex. 1109) and the published paragraphs of Petrovic (Ex. 1108). I refer to Petrovic ’886

using paragraph numbers and figure numbers from Petrovic '886 specification and drawings, which are at pages 6-61 of Ex. 1109.

79. As I show below in Section 8.5.1 of this Declaration, it is my opinion that Petrovic '886 provides written description support for at least independent claim 14 of Petrovic and provides written description support for the disclosure relied on in Petrovic. Petrovic '886 was filed on May 21, 2008. Ex. 1108, cover. Thus, I understand that Petrovic is prior art to the '362 patent under pre-AIA 35 U.S.C. § 102(e) for at least the material included in Petrovic '886, because both its filing date (March 31, 2009) and its earliest priority date (May 21, 2008) are before the earliest possible priority date of the '362 patent (April 17, 2009). I also understand that neither Petrovic nor Petrovic '886 were considered during prosecution of the '362 patent. Ex. 1101, cover, at 2.

80. Similar to the '362 patent, Petrovic describes a wideband receiver system that it calls “channel stacking system 100” and that “assemble[s] channels resident within an RF signal into a composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box.” Ex. 1108, [0028]. *See* Ex. 1109, [0008]. For convenience, Petrovic Figure 4 is annotated below using colors that match annotation colors for corresponding features of the '362 patent drawings in Section 7, above. Petrovic Figure 4 shows details of the system 100. Ex. 1108, [0028]. *See* Ex. 1109, [0008], Fig. 1.

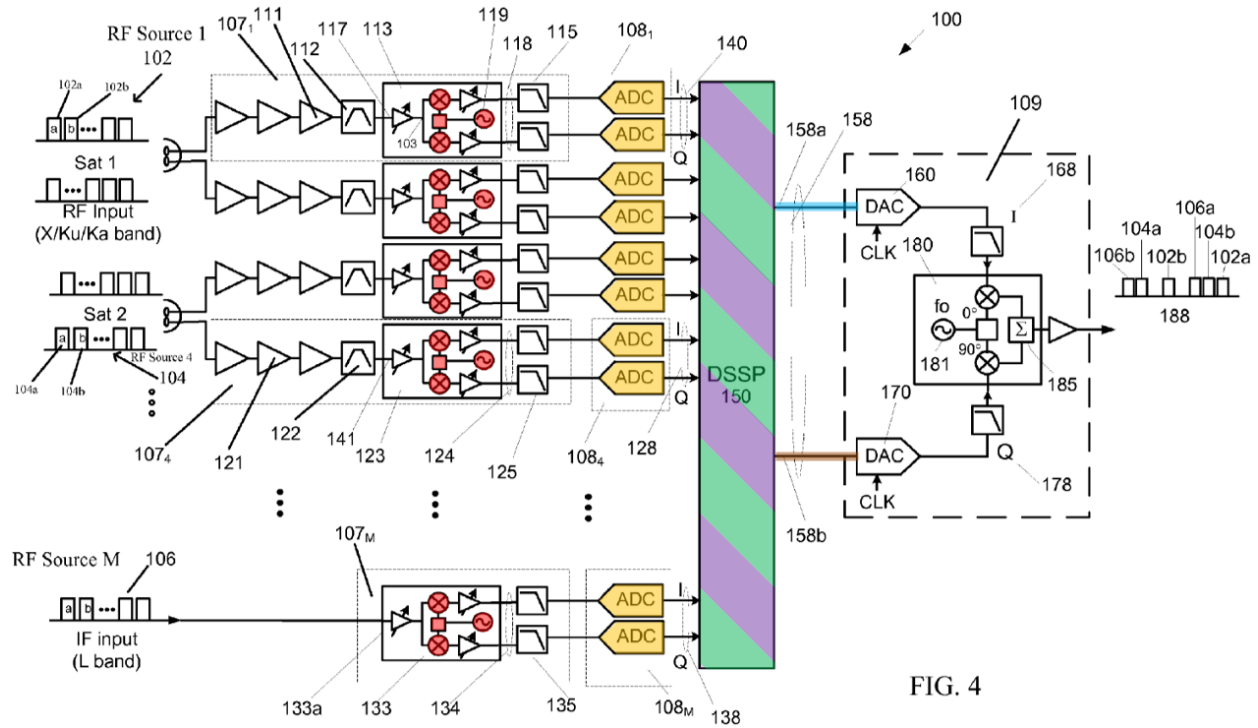


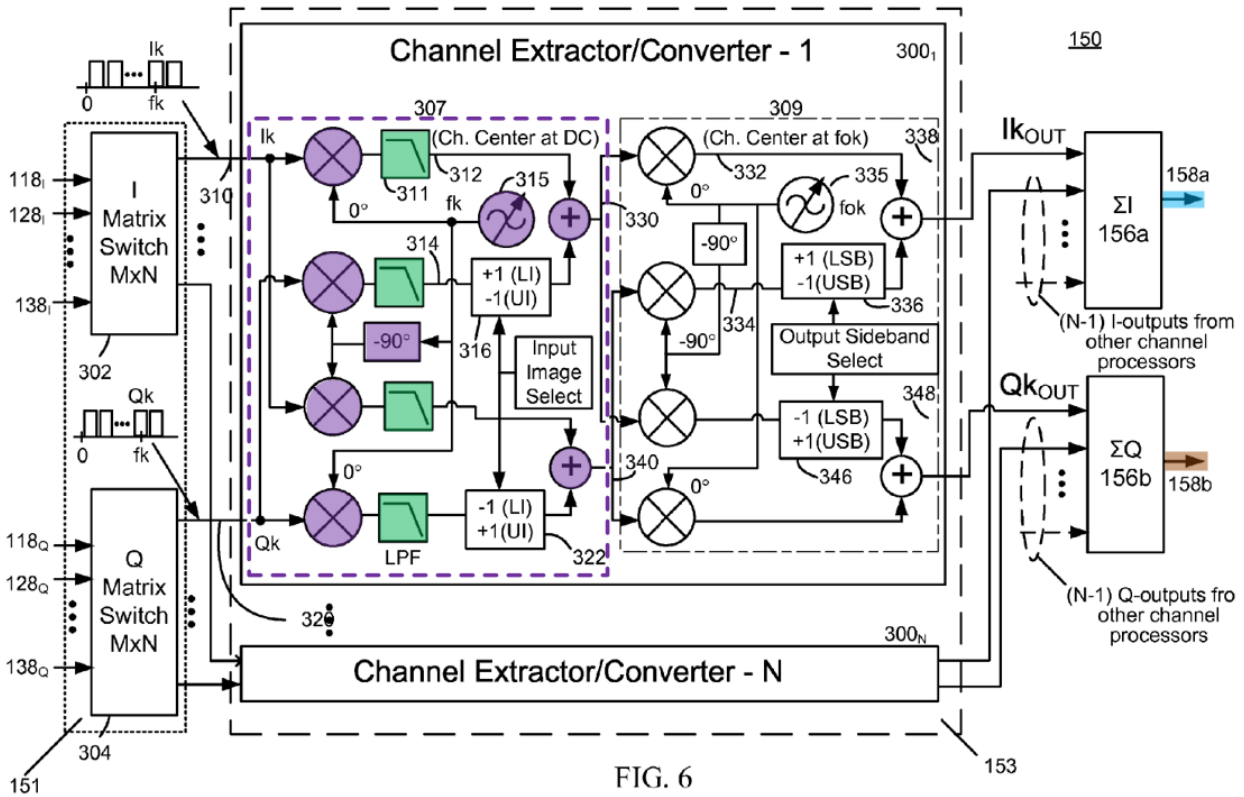
FIG. 4

Ex. 1108, Fig. 4 (annotated)

81. The system 100 receives signals 102-106 from a plurality of RF sources, such as satellites. Ex. 1108, [0029], Fig. 4; Ex. 1109, [0010]-[0013], [0016], [0023], [0026], Fig. 1. Each of those signals is wideband, as it may comprise multiple channels. Ex. 1108, [0029], Fig. 4; Ex. 1109, [0016], Fig. 1. The signals 102-106 are coupled to respective “analog preprocessing and downconversion (APD) stages 107_{I-M}.” Ex. 1108, [0032], Fig. 4; Ex. 1109, [0010], [0013], [0020], Fig. 1. Each of those APD stages includes a downconverter (**red**), that downconverts an RF signal into in-phase (I) and quadrature phase (Q) intermediate frequency (IF) signals. Ex. 1108, [0032]-[0038], Figs. 4-6; Ex. 1109, [0010], [0013], [0018]-[0023], [0031], [0032], Figs. 1-3A. The downconverted I and Q signals are filtered and converted to

digital form in analog-to-digital converters 108_{I-M}, (**gold**). Ex. 1108, [0032], [0039], Fig. 4; Ex. 1109, [0010], [0013], [0018]-[0020], [0022], [0024], Figs. 1-3A.

82. A digital signal switching and pre-processing (DSSP) stage 150 (**green/purple**) receives the digitized signals and “extract[s] the channels of interest ... (i.e., remove[s] all of the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1. The DSSP 150 outputs those channels as a composite signal with in-phase (**blue**) and quadrature (**brown**) components 158a and 158b. Figure 6 shows additional details of the DSSP 150, which may include “channel extractor/converter circuit 300.” Ex. 1108, [0058]; Ex. 1109, [0033], Fig. 3A.



Ex. 1108, Fig. 6 (annotated)

83. Also similar to the '362 patent, a channel is extracted from the digitized I and Q signals corresponding to one of the RF sources 102-106 by downconverting those signals to baseband in a complex mixer (**purple** and/or **purple** broken-line box) of a stage 307, and filtering using low pass filters 311 (**green**). Ex. 1108, [0060]-[0070]; Ex. 1109, [0037]-[0054]. The frequency f_k used for the downconversion to baseband (much like frequency ω_{ci} in the '362 patent) is selected based on a frequency corresponding to a desired channel. Ex. 1108, [0066]; Ex. 1109, [0045].

84. The I and Q signals 330 and 340 of the extracted channel are upconverted to a desired output frequency in the stage 309, and then summed with other upconverted channels (from stages 309 of other channel/extractor converters) in combiners 156a and 156b to result in the I and Q signals 158a and 158b. Ex. 1108, [0078]-[0086]; Ex. 1109 [0055]-[0061].

85. It is my opinion that Petrovic is in the same field of endeavor as the '362 patent, and thus is analogous art. For example, and like the '362 patent, which "relates to wideband receiver systems and methods having a wideband receiver that is capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum," Petrovic relates to a system and method for receiving a wideband radio frequency signal comprising multiple channels. Ex. 1101, 1:15-18; Ex. 1108, [0029], Fig. 4; Ex. 1109, [0010]-[0011], [0013], [0016], [0020], [0023], Fig. 1. Petrovic is also reasonably pertinent to problems with which the '362 patent is concerned, and is also analogous art on that basis. For example, Petrovic describes selecting individual channels by conversion to baseband and filtering in the same way as is described by the '362 patent. Ex. 1101, 5:62-6:54, Fig. 3; Ex. 1108, [0042], [0058]-[0077], Fig. 6; Ex. 1109, [0015], [0033], [0036]-[0054], Fig. 3A.

8.5.1. Petrovic is Entitled to a Priority date of May 21, 2008

86. It is my understanding that a reference patent or printed publication is entitled to claim the benefit of the filing date of an earlier-filed application if the

disclosure of the earlier-filed application provides support for one or more claims in the patent or printed publication.

87. As shown in the table below, Petrovic '886 provides written description support for at least claim 14 of Petrovic. Thus, Petrovic is entitled to the May 21, 2008 priority date of Petrovic '886, and is prior art to the '362 patent under pre-AIA 35 U.S.C. § 102(e) because its priority date is before the earliest possible priority date of the '362 patent (April 17, 2009).

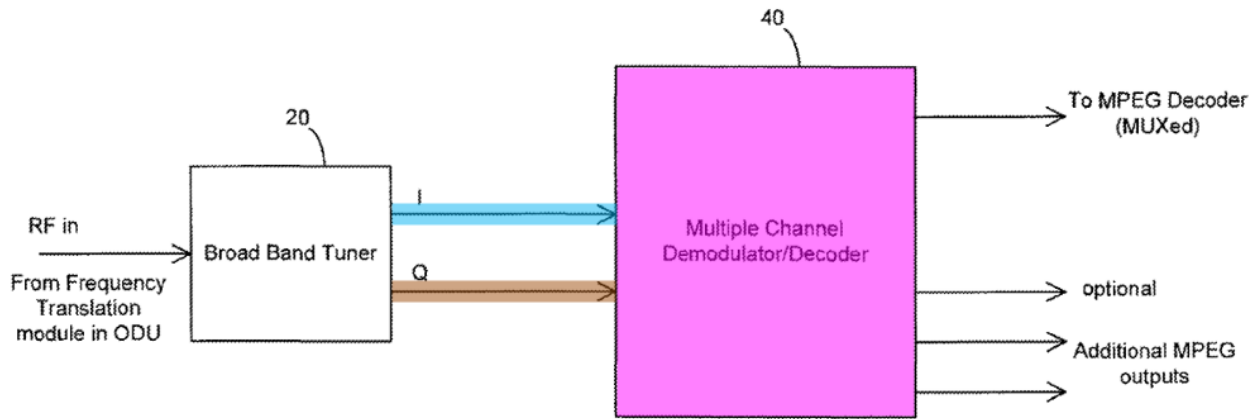
Petrovic – Claim 14 (Ex. 1108)	Petrovic '886 (Ex. 1109)
14. A method for assembling channels in a composite signal, the method comprising:	[0001], [0004], [0008], Claim 16.
a) downconverting, in a single frequency translation process, a first input signal comprising a first plurality of channels to a first IF signal comprising said plurality of first channels;	[0005], [0010], [0014], [0029], [0031], [0032], Claim 16, Figs. 1 and 2
b) converting the first IF signal into a first digital IF signal;	[0010], Claim 16, Fig. 1
c) downconverting, in a single frequency translation process, a second input signal comprising a plurality of second channels to a second IF signal comprising said plurality of second channels;	[0005], [0013], [0014], [0023], [0029], [0031], [0032], Claim 16, Figs. 1, 2

Petrovic – Claim 14 (Ex. 1108)	Petrovic '886 (Ex. 1109)
d) converting the second IF signal into a second digital IF signal; and	[0005], [0013], [0024], Claim 16, Fig.1
e) assembling, in the digital domain, at least one of the first channels and at least one of the second channels into a digital composite signal.	[0015], [0025], [0036]-[0068], [0080], Claim 16, Figs. 3A, 3B

8.6. Eidson (Ex. 1112)

88. U.S. Patent No. 7,783,958 to Eidson (“Eidson”) indicates on its face that it issued on August 24, 2010. Ex. 1112, cover. I understand that Eidson qualifies as prior art to the '362 patent under pre-AIA § 102(e), because the application on which Eidson is based was filed prior to the earliest possible priority date (April 17, 2009) of the '362 patent. I also understand that Eidson was not considered during prosecution of the '362 patent. Ex. 1101, cover, 2.

89. Eidson describes a multiple channel receiver that demodulates multiple channels using a multiple channel demodulation and error correction decoding engine. Ex. 1112, Abstract, 8:27-30. Eidson Figure 8 (below) “shows a broadband tuner and multi-channel demodulator and decoder” according to the Eidson invention. *Id.*, 7:58-59.



Ex. 1112, Fig. 8 (annotated)

90. A frequency translation module located in an outdoor unit selects desired satellite transponder channels and translates those selected channels to a contiguous section of bandwidth that is received by a broadband tuner 20. *Id.*, 8:43-57. Referring to the annotated version of Eidson Figure 8 shown above, the digital outputs of the tuner 20 are a pair of I (blue) and Q (brown) signals that represent multiple selected transponder channels. *Id.*, 8:54-57, 9:5-25, Figs. 9-10. As discussed in more detail below, the I and Q signals input to the multiple channel demodulator/decoder 40 (pink) are thus functionally the same as the summed I signal 158a and the summed Q signal 158b output by the Petrovic DSSP 150. In Eidson, the digital I and Q output of the broadband tuner 20 “is processed by a multiple channel demodulator and decoder 40 to produce one or more MPEG streams comprising multiple video programs derived from the selected transponder channels.” Ex. 1112, 8:65-9:2.

91. Eidson is reasonably pertinent to problems with which the '362 patent is concerned, as well as to problems with which Petrovic is concerned. On at least that basis, Eidson is analogous art to the '362 patent and to Petrovic. For example, the '362 patent indicates that signals recovered from received RF signals may be output to a demodulator, but leaves the particulars to “commonly known methods.” Ex. 1101, 6:55-58, Fig. 2. In my opinion, a POSITA would have considered Eidson, which relates to demodulation of signals for multiple channels, as a pertinent example of those “commonly known methods.” Moreover, a POSITA would have similarly considered Edison pertinent to Petrovic, which generates multichannel digital I and Q signals that are functionally the same as signals described in Eidson.

8.7. Rabaey (Ex. 1116)

92. Rabaey is a textbook on digital integrated circuit design. Ex. 1116 (“Digital Integrated Circuits[;] A Design Perspective”). It is my understanding that Rabaey was publicly available more than one year before the earliest possible priority date of the '362 patent, and that Rabaey is thus prior art to the '362 patent under pre-AIA 35 U.S.C. § 102(b). Ex. 1173, ¶¶ 47-54. In my opinion, Rabaey is reasonably pertinent to problems with which the '362 patent is concerned, and is analogous art. The '362 patent describes at length how signals may be processed in digital form. Ex. 1101, 5:31-6:65, Figs. 2-3. Integrated circuits were a well-known and widely-used way to implement digital processing in electronics. Ex. 1116, 17 (recognizing “continuous trend towards digital solutions in all other areas of

electronics”), 28 (“The purpose of this book is to provide a bridge between the abstract vision of digital design and the underlying digital circuit and its peculiarities”). Rabaey describes the “commonly known methods” of sending “a serial or parallel digital data stream to a demodulator using a serial or parallel data interface” that the ’362 patent refers to and asserts, in claims 2, 3, 12, and 13, to be part of the purported invention. Ex. 1101, 6:55-58, 11:66-12:2, 12:54-59.

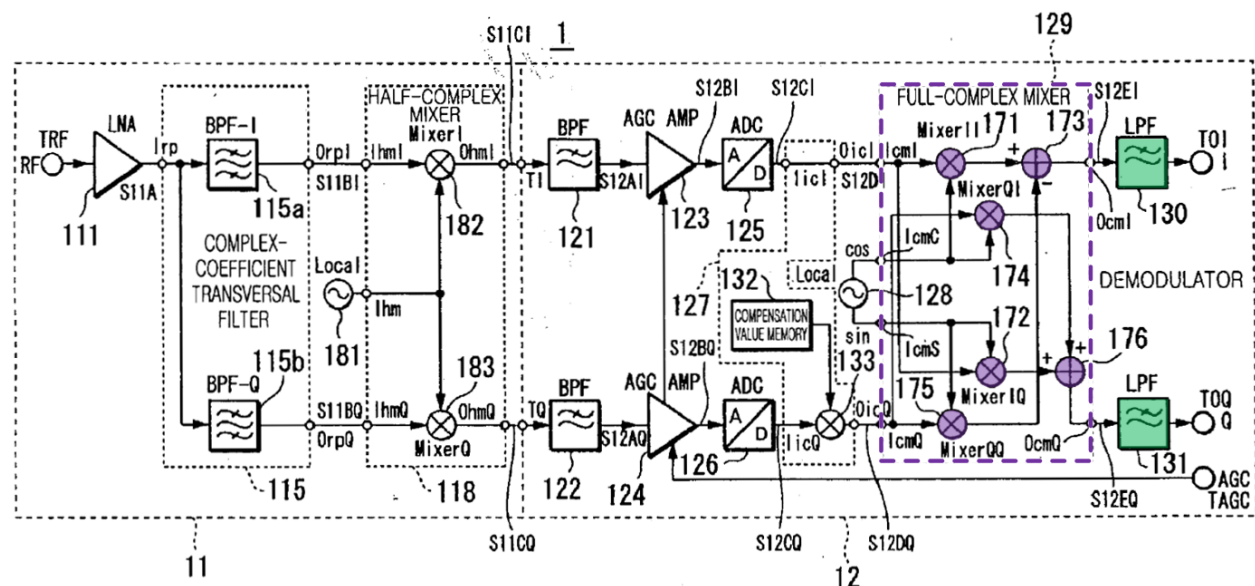
8.8. Jensen (Ex. 1126)

93. Jensen is a U.S. Patent Application Publication, which was published on February 1, 2007. Ex. 1126, cover. Jensen is prior art to the ’362 patent under pre-AIA 35 U.S.C. § 102(b), because Jensen was published more than one year prior to the earliest priority date of the ’362 patent. Jensen discloses a channel-select decimation filter for digitally processing signals associated with received RF signals. Ex. 1126, [0023]-[0029], Figs. 1-2. In particular, and like the ’362 patent, Jensen describes generating downconverted I and Q components of a received RF signal in the analog domain, generating a digital signal based on those I and Q components, baseband converting the digital signal, and then filtering the baseband-converted digital signal. *Id.* Jensen explicitly discloses that the filtered baseband-converted digital signals are decimated, which is a well-known process that reduces the original sample rate of a signal to a lower rate. *See* Section 8.3.4. Jensen is reasonably pertinent to problems with which the ’362 patent is concerned, and is analogous art to the ’362 patent on that basis. For example, the ’362 patent describes generating

downconverted I and Q components of a received RF signal in the analog domain, digitizing those signals, baseband converting those signals, and then filtering and decimating the baseband-converted digital signals. Ex. 1101, 4:16-6:58, Figs. 2-3; see Section 7.

8.9. Takahiko (Ex. 1161)

94. Takahiko, is a U.S. Patent Application Publication that published on November 16, 2006, more than one year prior to the earliest priority date of the '362 patent, and is therefore prior art to the '362 patent under pre-AIA 35 U.S.C. § 102(b). Ex. 1161, cover. Takahiko discloses a downconverter of a radio receiver that includes a digital baseband complex mixer (purple) and low pass filters (green) similar to those of the '362 patent. Ex. 1161, [0143], [0153], [0156].



Ex. 1161, Fig. 1 (annotated)

95. Takahiko describes circuits that are also described by the '362 patent and that are used for similar purposes (reception and tuning of RF signals). Ex. 1161, [0143]-[0156], Fig. 1. Thus, in my opinion Takahiko is reasonably pertinent to problems with which the '362 patent is concerned, and is analogous art.

9. OPINIONS WITH RESPECT TO THE '362 PATENT

9.1 Petrovic in View of Eidson Renders Claims 1, 4-8, 11, and 14-18 Obvious

96. In the following, I provide a limitation-by-limitation analysis showing how Petrovic in view of Eidson renders claims 1, 4-8, 11, and 14-18 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below. Also, in my analysis throughout this declaration, I will sometimes refer to combinations of references with dashes between them. For example, I will refer to a combination of Petrovic and Eidson as "Petrovic-Eidson."

9.1.1 Independent Claim 1

97. The limitations of claim 1 appear in the Claims Listing Appendix, labeled as limitations [1A]-[1D]. For the following reasons, it is my opinion that claim 1 is rendered obvious over Petrovic in view of Eidson.

a. [1A] “A wideband receiver system comprising:”

98. It is my opinion that Petrovic discloses “[a] wideband receiver system comprising:” as claimed.

99. To the extent the preamble is limiting, it is my opinion that Petrovic teaches this limitation. Petrovic describes a channel stacking system 100 that receives signals 102-106 that each occupies a wide portion of RF spectrum bandwidth that includes multiple frequencies and that comprises multiple channels. Ex. 1108, [0028]-[0029], Fig. 4; Ex. 1109, [0005], [0010]-[0011], [0013], [0016], [0020], [0023], Fig. 1. For example, “the total channel bandwidth” of the signal 102 “may be in the range of 100 MHz-5 GHz” and “the number of channels included in any particular received signal 102 may be 4, 6, 8, 16, 24, 28, 32, 40, 48, 60, 120 or more.” Ex. 1108, [0029]; Ex. 1109, [0016]; *see* Ex. 1101, 1:24-27 (describing “wideband” as a band that carries multiple channels), Figs. 2, 6-8. As I explain above in Section 6, the ’362 patent states that a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” Ex. 1101, 1:24-27. In my opinion, this is consistent with the ordinary and customary meaning of “wideband.” Because the channel stacking system 100 of Petrovic receives signals 102-106 that include multiple frequencies and comprise multiple changes, it is further my opinion that the channel stacking system 100 of Petrovic is a “wideband receiver system” as claimed, consistent with the usage of “wideband” in the ’362 patent. Moreover, Petrovic describes other similar embodiments of wideband receiver systems. For example,

Petrovic discloses at least “second,” “third,” “fourth,” and “fifth” embodiments of a channel stacking system, each of which is a wideband receiver system as in limitation [1A]. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11. To the extent that Patent Owner argues that a “wideband receiver system” must receive desired channels in non-contiguous frequency bands, this is also taught by Petrovic, as explained below in Section 9.1.5.a for limitation [7A] of claim 7.

b. [1B] “a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”

100. It is my opinion that Petrovic discloses “a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels,” as claimed.

101. Referring to annotated Figure 4 of Petrovic below, the mixers (**red**) of any of the individual downconverters (shown as broken **red** line boxes), or the mixers of any combination of those downconverters, is a mixer module according to limitation [1B].

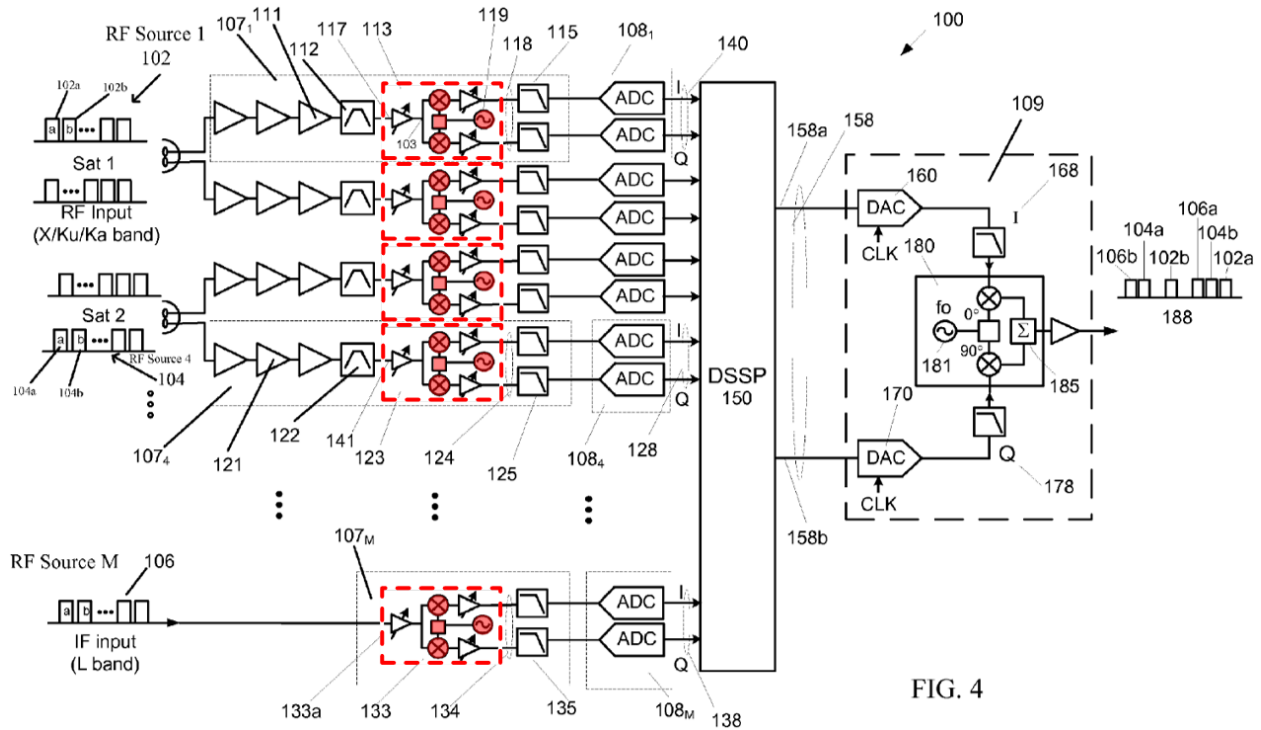


FIG. 4

Ex. 1108, Fig. 4 (annotated)

102. According to Petrovic, the mixers of a first downconverter 113 downconvert the first RF input signal 102 to a first IF signal 118, the mixers of a second downconverter 123 downconvert the second RF input signal 104 to a second analog IF signal 124, and the mixers of a third downconverter 133 downconvert the third RF input signal 106 to a third IF signal 134. Ex. 1108, [0033]-[0034], [0036]-[0037], [0047], [0050], Figs. 4-5; Ex. 1109, [0005], [0010], [0013], [0020], [0031]-[0032], Figs. 1-2.

103. As I explain in Section 9.1.1.a above for preamble [1A], each of the RF signals 102-106 in Petrovic, downconverted by the mixers of the downconverters 113, 123, and 133, includes multiple channels in multiple frequencies. In my opinion, a POSITA would have understood that the channels of Petrovic are

television channels. For example, Petrovic discloses outputting signals from the channel stacking system 100 “to a rendering device, such as a set-top box, or other receiver/tuner,” which are devices associated with output of television programming to users. Ex. 1108, [0028], [0054]; Ex. 1109, [0008], [0030]. Moreover, satellite communication has long been commonly used for transmission of television programming channels to end users. For example, Coffin discloses that video content received by home satellite receiving systems includes television programs Ex. 1154, [0011] (video content received by home satellite receiving systems includes television programs). *See also*, Ex. 1154, [0017], [0020]; Ex. 1155, 3:13-19 (satellite transmission of QPSK-modulated television channels). In fact, “[s]atellite television and data broadcast services from Direct Broadcast Satellites (DBS) operating in the Broadcast Satellite Service (BSS) to homes with stationary antennas comprises well known art.” Ex. 1156, [0005]. Because satellite communication was so commonly used for transmission of television programming to end users, in my opinion a POSITA would have been motivated to use the Petrovic channel stacking system 100 in a home satellite reception system for obtaining and outputting television programming via television channels. Doing so would have involved merely combining known prior art elements (Petrovic’s channel stacking system that receives channels that were transmitted by satellite, and the fact that it was well-known to receive television programming channels that were transmitted by satellite) according to known methods (by using the channel stacking system 100

in the manner Petrovic discloses to receive the channels) to yield predictable results (the channels of Petrovic being television channels that could be transmitted via satellite and received by the channel stacking system 100 of Petrovic).

104. Petrovic also discloses that the channels in the RF signals 102-106 may include “a plurality of desired channels” and a “plurality of undesired channels.” Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036]. As explained in detail in Section 9.1.1.d below for limitation [1D], Petrovic discloses later extracting, or selecting, less than all of the channels included in a received RF signal. Ex. 1108, [0042], [0053], [0055], [0058]; Ex. 1109, [0004]-[0005], [0015], [0025], [0033], [0036], Fig. 1. Consistent with the use of the terms “desired” and “undesired” in the ’362 patent, a selected channel of Petrovic is a “desired” channel, whereas an unselected channel of Petrovic is an “undesired” channel. Ex. 1101, Abstract, 1:29-34, 3:9-39, 4:19-33, 5:43-44, 5:49-61, 6:32-42, 6:55-64.

105. Moreover, Petrovic describes other embodiments in which mixers of downconverters (individually or in combination), in my opinion, are similarly mixer modules configured to perform the function recited in limitation [1B]. For example, Petrovic discloses at least “second,” “third,” “fourth,” and “fifth” embodiments of a channel stacking system, as well as variations within those embodiments and various further embodiments of downconverter stages of the channel stacking system embodiments, each having mixers of downconverters that are configured to perform

the function recited in limitation [1B]. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11.

- c. **[1C] “a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”**

106. It is my opinion that Petrovic discloses “a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels,” as claimed.

107. Referring to Petrovic Figure 4 annotated below, Petrovic’s channel stacking system 100 includes analog-to-digital converter (ADC) pairs 108₁-108_M (**gold**). Ex. 1108, [0039], [0047], [0050]-[0052], Fig. 4; Ex. 1109, [0005], [0010], [0018]-[0019], [0022], [0024], [0028], Fig. 1. In my opinion, any of the ADC pairs 108₁-108_M, or any combination of those ADC pairs 108₁-108_M, is a wideband ADC module according to limitation [1C]. Ex. 1108, [0039], [0047], [0050]-[0052], Fig. 4; Ex. 1109, [0005], [0010], [0018]-[0019], [0022], [0024], [0028], Fig. 1.

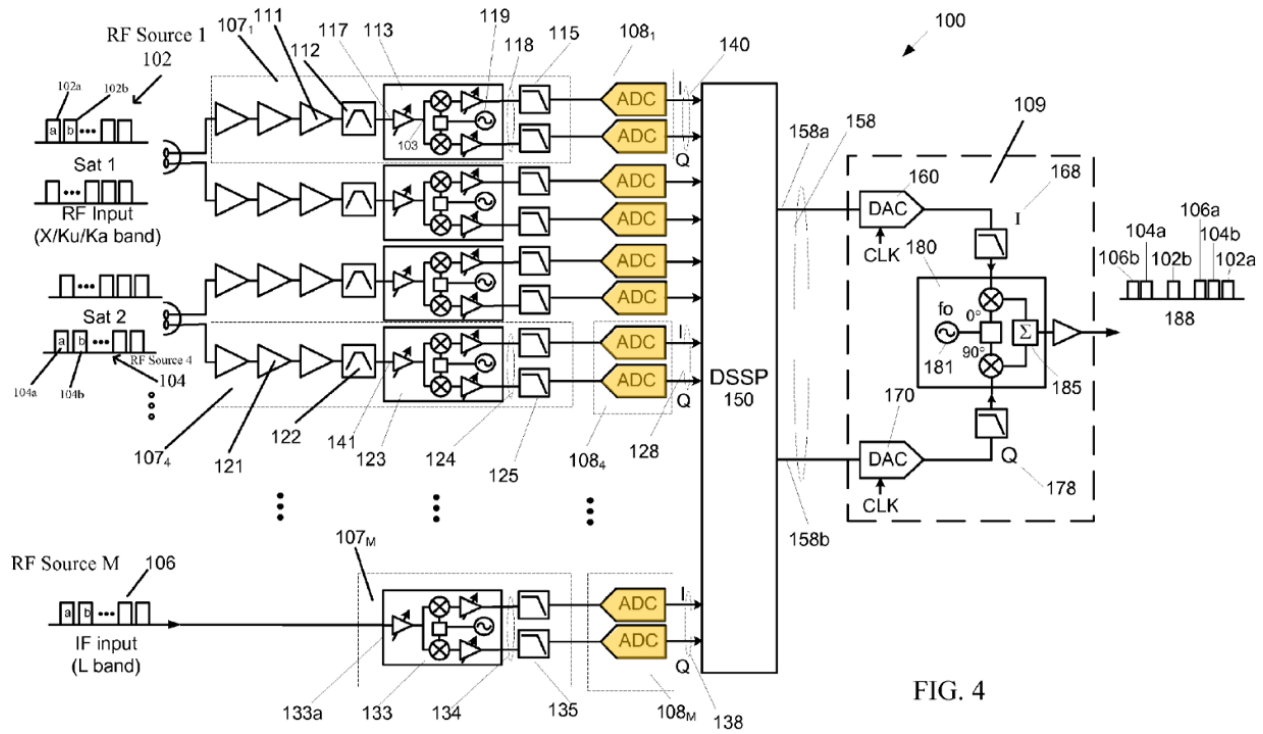


FIG. 4

Ex. 1108, Fig. 4 (annotated)

108. Each of the ADC pairs 108₁-108_M digitizes a pair of downconverted I and Q signals that include channels (both desired and undesired) from a received RF input. *E.g.*, Ex. 1108, Fig. 4; Ex. 1109, Fig. 1. Any of the individual ADC pairs 108₁-108_M shown in Figure 4, or any combination of those ADC pairs, is a wideband ADC module according to limitation [1C]. For example, if the downconverter 113 is treated as the mixer module of [1B], the ADC pair 108₁ digitizes, after filtering in anti-aliasing filters 115, I and Q signals 118 that include channels 102a, 102b, etc., carried in the received RF signal 102. Ex. 1108, [0033], [0039], Fig. 4; Ex. 1109, [0010], Fig. 1. As another example, and if the downconverter 113 and the downconverter 123 together are treated as the mixer module of [1B], the ADC pair

108₁ and the ADC pair 108₄ collectively digitize, after filtering in anti-aliasing filters 115 and 125, I and Q signals 118 that include channels 102a, 102b, etc., carried in the received RF signal 102, as well as I and Q signals 124 that include the channels 104a, 104b, etc., carried in the received RF signal 104. Ex. 1108, [0033], [0039], [0047], Fig. 4; Ex. 1109, [0010], [0013], [0023]-[0024], Fig. 1.

109. ADC pairs (individually or in combination) of other Petrovic embodiments are similarly the claimed ADC modules configured to perform the functions recited in limitation [1C]. For example, Petrovic discloses at least “second,” “third,” “fourth,” and “fifth” embodiments of a channel stacking system, as well as variations within those embodiments and various further embodiments of downconverter stages of the channel stacking system embodiments, each having ADC pairs that are the claimed ADC modules configured to perform the functions recited in limitation [1C]. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11.

- d. **[1D] “digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.”**

110. It is my opinion that Petrovic in view of Edison discloses “digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream” as claimed.

111. Referring to Petrovic Figure 4 annotated below, the Petrovic system 100 includes “digital circuitry” in the form of a Digital Signal Switching and Preprocessing (DSSP) stage 150 (**green/purple**) that selects desired television channels from digitized frequencies (i.e., from the digitized signals received from the ADC pairs 108₁-108_M). Ex. 1108, [0042], [0053], [0058]-[0077], Figs. 4, 6; Ex. 1109, [0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025], [0033], [0037]-[0054], Fig. 1.

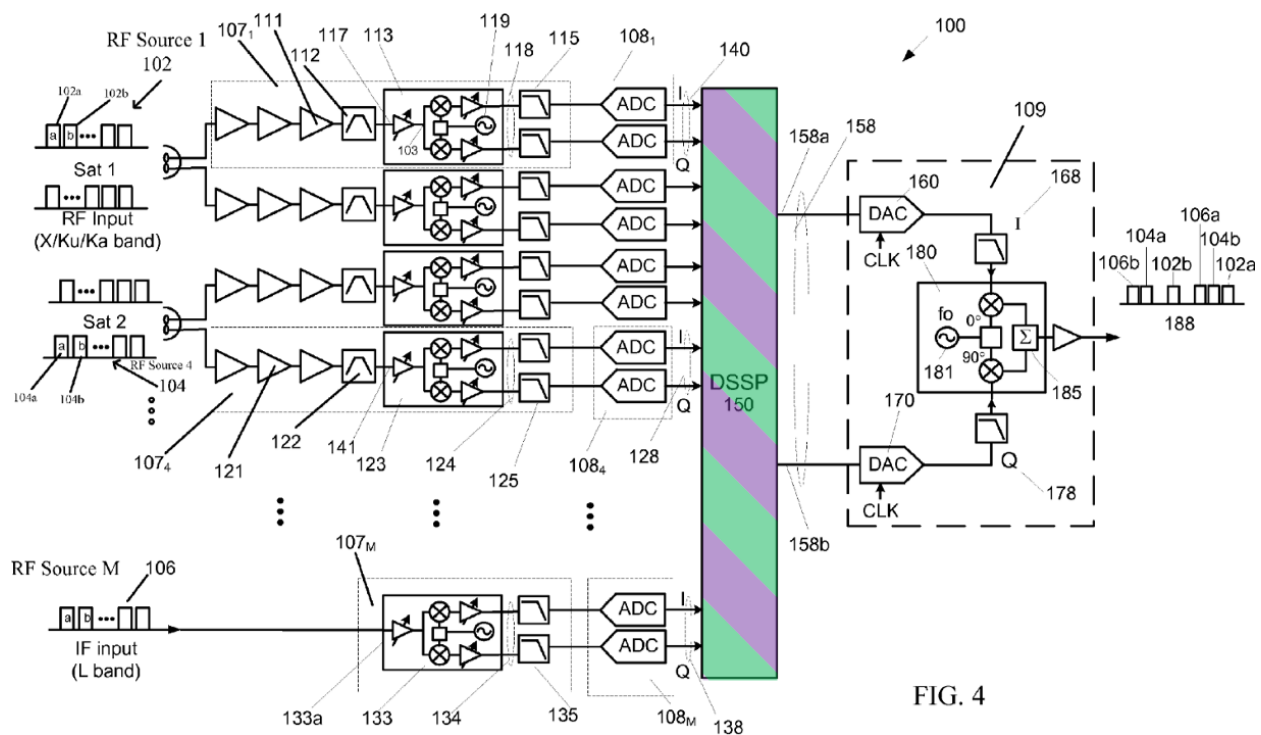


FIG. 4

Ex. 1108, Fig. 4 (annotated)

112. As I explain in Section 9.1.1.c above for limitation [1C], and as shown in Figure 4 of Petrovic, each of the ADC pairs 108₁-108_M digitizes a pair of downconverted I and Q signals that include channels (both desired and undesired)

from a received RF input. The DSSP 150 comprises “channel extraction stages” that “extract [i.e., select] the channels of interest [i.e., desired channels]” from the signals received from the ADC pairs 108₁-108_M and that “remove all of the channels that are not of interest,” i.e., the claimed “undesired channels.” Ex. 1108, [0042], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0003]-[0004] (“[t]he present invention provides for a channel stacking system ... which processes channel selection ... within the digital domain”), [0005], [0015], [0025] (digital signal processor 150 “assemble[s] a composite signal 158 having the desired channels”), [0033] (channel extractor/converter circuits of digital signal processor 150 “extract a desired channel”), [0036], Fig. 1. DSSPs of other Petrovic embodiments are similarly digital circuitry configured to select a plurality of desired television channels from a digitized plurality of frequencies. Ex. 1108, [0018]-[0024], [0098]-[0122], Figs. 9-15; Ex. 1109, [0007], [0071]-[0095], Figs. 5-11.

113. In fact, Petrovic describes the same selection technique that is described by the '362 patent. For example, the '362 patent discusses frequency shifting to baseband and filtering of the baseband signal, while Petrovic explains that desired channels are digitally translated to baseband and “[t]he translated channels are then digitally lowpass filtered ..., leaving only the channel of interest.” Ex. 1101, 5:62-6:54, Fig. 3; Ex. 1108, [0042], [0058]-[0077], Fig. 6. Petrovic '886 also describes the same selection technique that is described by the '362 patent. For example, Petrovic '886 explains that “channel extraction ... is performed by direct digital

conversion to zero IF, followed by channel filters.” Ex. 1109, [0025]; *see also* [0036]-[0054], Fig. 3A. Petrovic ’886 further explains that digital signal processor 150 is operable to “extract and order *at least one of* the first plurality of channels and *at least one of* the second plurality of channels into the desired channel slot positions,” thus indicating that not all of the channels need to be selected. Ex. 1109, [0015] (italics added). *See also* Ex. 1109, [0025] (“The digital signal processors 150 is operable to assemble *at least one of* the first channels 102a, 102b and *at least one of* the second channels 104a, 104b into a composite signal 158....”) (italics added). Consistent with the above-cited discussion in Petrovic ’886 of selecting fewer than all of the channels, Petrovic ’886 further explains that the number of extractor/converter circuits can be fewer than the total number of channels in the received RF signals, thus indicating that some undesired channels are not selected. Ex. 1109, [0033] (“the channel extractor/converter circuits 300, 350 are operable to extract a desired channel and to locate or place it in the desired channel slot of the output signal 158. Exemplary, the number of parallel-connect channel extractor/converter circuits will be equal to the number of available channels (i.e., channel slots) in the output signal 158..., although in other embodiments a larger or smaller number of channel extractor/converter circuits may be employed within the signal processors 150 as well.”).

114. In addition to selecting channels, the Petrovic DSSP 150 upconverts baseband I and Q components for the selected channels to corresponding

frequencies, sums the upconverted I and Q components for all the selected channels to create a combined signal 158 having digital I component 158a (blue) and digital Q component 158b (brown), and outputs those digital signals 158a, 158b. Ex. 1108, [0018]-[0024], [0043], [0053], [0078]-[0096], [0098]-[0122], Figs. 4, 6, 9-15; Ex. 1109, [0005], [0007], [0015], [0025], [0055]-[0069], [0071]-[0095], Figs. 1, 3A, 5-11.

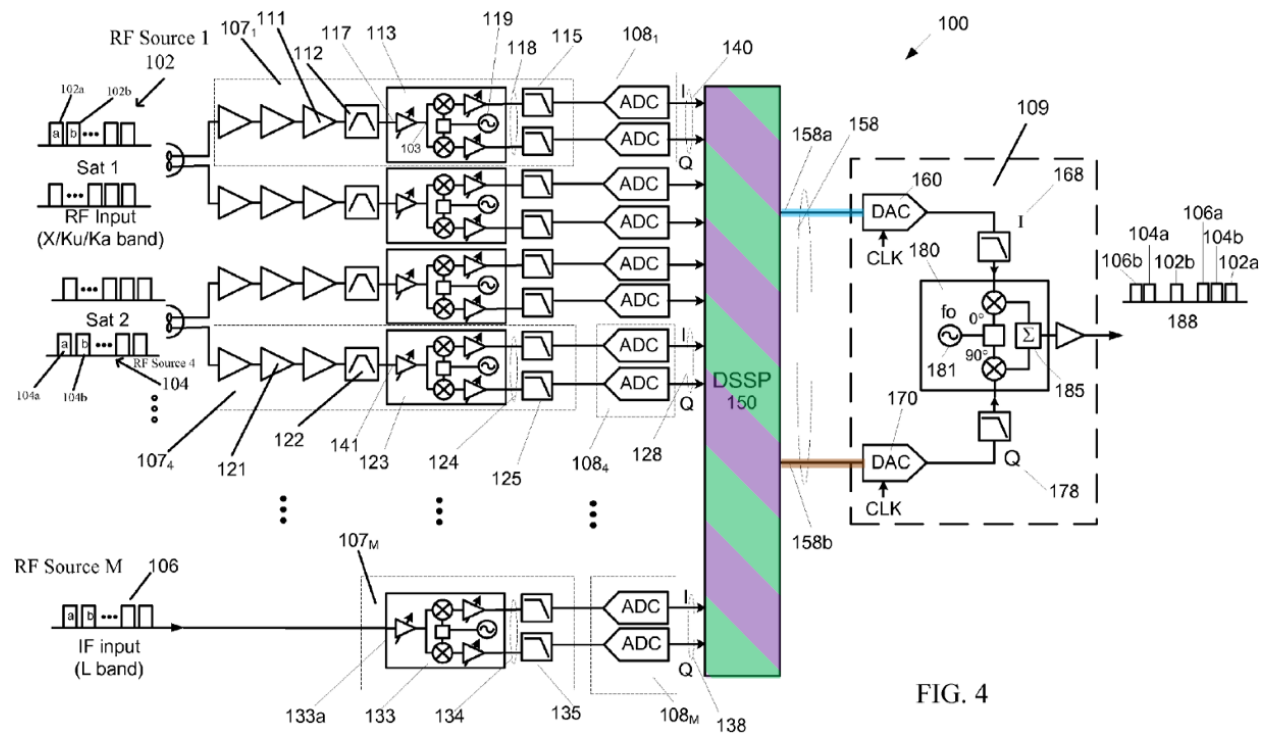


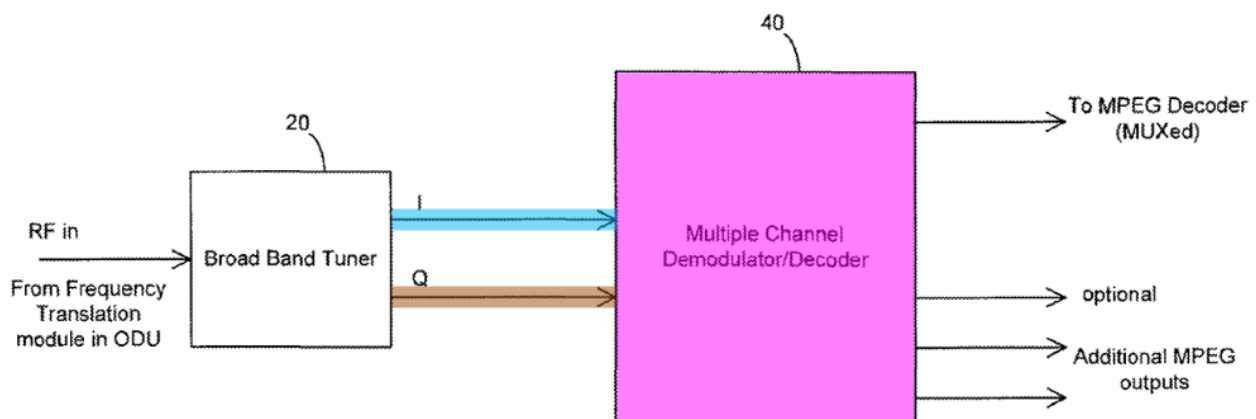
FIG. 4

Ex. 1108, Fig. 4 (annotated)

115. The signals 158a, 158b are a digital datastream that contains the selected channels. Ex. 1108, [0009], [0043], [0046] (referring to “digital composite signal 158”), [0054], [0055] (circuits of the DSSP 150 “extract a desired channel and locate or place the channel in the desired channel slot of the output signal 158”), Figs. 4, 6; Ex. 1109, [0005], [0015], [0025], [0030], [0033], Figs. 1, 3A.

116. Although Petrovic indicates that its channel stacking system “may be implemented as an outdoor unit (ODU) as a part of a satellite receiving system,” Petrovic does limit its channel stacking system or its tuner (e.g., the Petrovic APD stage(s), the Petrovic ADC pair(s), and the Petrovic DSSP) to ODU use. Ex. 1108, [0054]; Ex. 1109, [0030]. In my opinion, a POSITA would have been aware of other uses, as tuners were ubiquitous at the time, and in any event, Eidson teaches additional uses for the Petrovic tuner, and indeed, for the entire Petrovic channel stacking system.

117. Eidson Figure 8 discloses “a broadband tuner and multi-channel demodulator and decoder [pink].” Ex. 1112, 1:48-50, 2:8-10, 2:25-33, 2:42-51, 5:59-60, 7:58-59, 8:27-9:2.



Ex. 1112, Fig. 8 (annotated)

118. In my opinion, a POSITA would have understood that the tuning, demodulating, and decoding functions of the broadband tuner 20 and multi-channel demodulator decoder 40 of Eidson Figure 8 are functions that are normally

performed in a set top box or other receiver, and thus that the broadband tuner 20 and multi-channel demodulator decoder 40 would be part of a set top box. A POSITA would have understood this even more clearly in view the explanation in Eidson that the concepts described in the patent are to address “a need [that] exists for efficient processing of several transponder channels *in a set top box.*” Ex. 1112, 5:59-60 (italics added). There is discussion throughout Eidson making it clear that the channels are received by a set top box (which thus functions as a receiver), also referred to in Eidson as an “STB.” Ex. 1112, 2:8-10 (“The prior art architecture needs to be changed drastically once a single cable STB requires the simultaneous reception of more than two programs.”), 2:25-33 (e.g., “Thus, it is quite advantageous for the satellite operators to provide a STB with several channel receivers...”), 8:27-28 (“In the following sections we describe the various invention techniques to achieve an efficient, multiple channel receiver.”). *See also* Ex. 1112, 1:27-50, 2:42-61, 3:14-34, 8:43-48.

119. In Eidson, the multiple channel demodulator and decoder (“demodulator/decoder”) 40 receives digital I (blue) and Q (brown) signals from a front end that comprises the broadband tuner 20 and a frequency translation module (FTM) of a satellite outdoor unit (ODU). Ex. 1112, 8:29-9:2, Fig. 8. The FTM portion of the front end selects multiple channels, translates those selected channels to contiguous portions of a bandwidth, and sends an RF signal with those translated channels to the broadband tuner 20. Ex. 1112, 8:30-48, 9:5-25, Figs. 8-10. The

broadband tuner 20 downconverts the received RF signal, generates I and Q components of that downconverted signal, and digitizes those I and Q components to create digital I, Q signals. Ex. 1112, 8:43-9:25, Figs. 8-10. Those digital I, Q signals are output to the demodulator/decoder 40, which demodulates multiple channels in those signals. Ex. 1112, 8:65-9:2, 11:44-12:28, Figs. 8, 15-16. Eidson clearly states that the output (I, Q) of the broadband tuner is digital, and shows in Figure 9 an example implementation of a broadband tuner that has analog-to-digital (A/D) converters that provide digital I and Q signals to the demodulator/decoder. Ex. 1112, 7:61-62 (“FIG. 9 shows a broadband tuner”), 8:65-9:2, 9:5, Fig. 9. Thus, it is my opinion that Eidson teaches a demodulator to which “a selected plurality of television channels” is being output “as a digital datastream.”

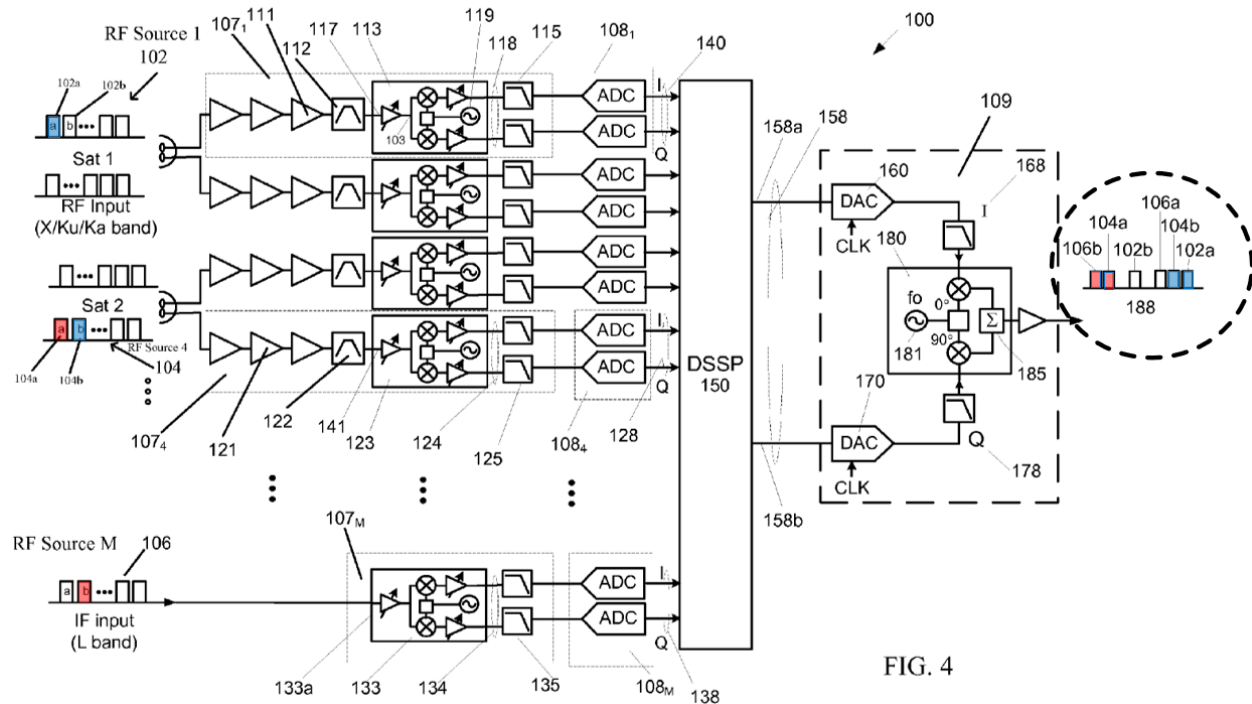
120. Eidson also shows a broadband demodulator 100 in Figure 15 as having A/D converters for received I and Q signals. Ex. 1112, 8:14-16, 11:44-49, Fig. 15. In my opinion, a POSITA would have understood from Eidson that the A/D converters could *either* be part of the broadband tuner or part of the demodulator. There would be no reason to use A/D converters for *both* the output of the tuner and the input of the demodulator. Thus, the A/D converters of the demodulator would be optional. In other words, a POSITA would have understood Eidson as disclosing two possibilities, in which the broadband tuner could have A/D converters to provide the digital I and Q signals to the demodulator, or in which the demodulator could instead digitize the I and Q signals. Thus, a POSITA would have understood Eidson

as disclosing either of these two options for A/D converter location. A POSITA would have also understood that there were two possibilities in Eidson to provide digital I and Q signals to the demodulator for processing – either the broadband tuner digitizes I and Q, or the demodulator digitizes I and Q. Thus, to the extent that it is argued that Eidson does not clearly disclose that the I and Q signals are digital when they are received by the demodulator, a POSITA would have considered it obvious to try either A/D converter location (as part of the broadband tuner or as part of the demodulator), since there are two possible locations for the A/D converters and both locations would result in successfully and predictably providing the demodulator with digital I and Q signals. Thus, the POSITA would be choosing from a finite (two) number of identified, predictable solutions (converting from analog to digital at the output of the broadband tuner, or converting from analog to digital at the input of the demodulator, so as to be compatible with the demodulator) with a reasonable expectation of success. Indeed, a POSITA would have considered the two solutions as equivalent and interchangeable, and providing the same result from the point of view of the ultimate demodulation function.

121. In my opinion, the I, Q signals received by the Eidson demodulator/decoder 40 from the front end (e.g., the FTM and the tuner 20) are functionally equivalent to the Petrovic I, Q signals 158a, 158b, as both sets of I, Q signals comprise multiple channels that have been placed into sequential slots of a bandwidth. In particular, the I, Q signals received by the Eidson

demodulator/decoder 40 are digital signals for multiple channels that have been selected and placed into contiguous portions of a bandwidth. Ex. 1112, 8:43-9:25, Figs. 8-10. Figure 10 of Eidson, for example, shows the spectral content of the I and Q signals in the Eidson broadband tuner and shows how channels have been placed into contiguous portions of bandwidth by a frequency translation module before the broadband tuner. Ex. 1112, 8:30-48; 9:21-22, Figs. 8-10. Similarly, the Petrovic I, Q signals 158a, 158b are digital signals for multiple channels that have been selected and has been placed into sequential portions of a bandwidth. Ex. 1108, Title, [0002], [0008], [0028], [0041]-[0044], [0046], [0053]-[0055], [0059]-[0091], [0097], Figs. 3-4, 6, 8; Ex. 1109, Title, [0001], [0004], [0008], [0015], [0025], [0030], [0033]-[0064], [0070], Figs. 1, 3A, 4. In particular, Petrovic is directed to a “channel *stacking* system and method,” the purpose of which is to “assembl[e] a desired *sequence of channels* to form a composite signal.” Ex. 1108, Title, [0002]; Ex. 1109, Title, [0001] (*italics added*). As I explain below, the composite signal containing the “desired sequence of channels” is signal 158 (made up of I, Q components 158a and 158b). Petrovic Figure 4 (annotated below) shows channels 104a (**red**) and 106b (**red**) in received RF signals 104 and 106, as well as channels 102a (**blue**) and 104b (**blue**) in received RF signals 102 and 104. While channels 104a (**red**) and 106b (**red**) are shown to be non-contiguous in signals 104 and 106, and channels 102a (**blue**) and 104b (**blue**) are shown to be non-contiguous in signals 102 and 104, the **red** pair of signals 104a/106b are shown to be contiguous in a signal 188, and

likewise the **blue** pair of signals 102a/104b are shown to be contiguous in the signal 188. Ex. 1108, [0053]-[0054], Fig. 4; Ex. 1009, [0025], [0030], Fig. 1. The signal 188 is after the frequency shift that occurs in the DSSP 150. *Id.*



Ex. 1108, Fig. 4 (annotated)

122. Because the stage 109 only converts signals 158a and 158b to analog, upconverts those analog signals, and combines the upconverted analog signals, channels 104a and 106b would also be contiguous in I, Q signals 158a and 158b that are output from the DSSP 150, and likewise channels 102a and 104b would be contiguous in the I, Q signals 158a and 158b. Ex. 1108, [0054], [0097], Figs. 4, 8; Ex. 1109, [0030], [0070], Figs. 1, 4. Therefore, channels 104a and 106b have been selected and has been placed into sequential portions of a bandwidth in the I, Q signals 158a and 158b, and likewise channels 102a and 104b have been selected and

has been placed into sequential portions of a bandwidth in the I, Q signals 158a and 158b.

123. Also, in my opinion, a POSITA would have appreciated that the I and Q signals output from Petrovic's DSSP could be readily sent to a demodulator for a STB, as taught in Eidson. This could be done in place of Petrovic's stage 109, or in addition to it. Eidson teaches that its demodulator/decoder 40 operates by receiving I, Q signals that are functionally equivalent to the I, Q signals 158a, 158b output by the Petrovic DSSP. It is also my opinion that a POSITA would have been motivated to combine a Petrovic tuner and the Eidson demodulator/decoder 40 so that the multiple selected channels output by the Petrovic DSSP (as I, Q signals 158a, 158b) could be demodulated in the digital domain with a single demodulator, which would have been more efficient than using multiple simultaneous demodulators for separate channels. Ex. 1112, 4:2-6, 6:36-38.

124. Combining a Petrovic tuner with an Eidson demodulator/decoder 40 would allow incorporation of tuning/channel selection and demodulating/decoding functionality into a single device, a configuration known in the art, but with the added benefits of digital tuning afforded by Petrovic and multichannel demodulation afforded by Eidson. Ex. 1108, [0007], [0094]; Ex. 1109, [0003], [0069]; Ex. 1112, 3:35-45, 4:2-6, 6:36-38. For instance, Petruzzelli describes a satellite STB that is able to receive multiple satellite signals, tune to channels of the received satellite signals, and demodulate those channels. Ex. 1140, [0019]-[0021], Fig. 2. In

particular Petruzzelli discloses that a satellite STB 200 (also referred to as a television converter 200) “may include one or more tuner devices 206, 246 that may receive a satellite signal 204 ... from satellite television distributor 1,” and that the STB 200 can select a channel from the satellite signal 204. Ex. 1140, [0020], [0023], Fig. 2. Petruzzelli further discloses that the satellite STB 200 performs demodulation on the satellite signal 204, using a demodulator 208. Ex. 1140, [0021], Fig. 2.

125. For example, the Eidson demodulator/decoder 40 could be added to the Petrovic tuner in a set top box intended to function as a “‘Media Center’ STB” that would feed other set top boxes. Ex. 1112, 2:28-33. In such a set top box, the I, Q signals could be simultaneously output to the demodulator/decoder 40 (e.g., for demodulation/decoding for output to display or recording devices) and to the Petrovic DAC and Complex to Real Conversion stage 109 for generation of a signal 188 to transmit to other set top boxes or devices. Alternatively, the stage 109 could be omitted to save cost if “media center STB” functionality was not needed, which would allow for a further simplified design.

126. Moreover, in my opinion, combining a Petrovic tuner and the Eidson demodulator/decoder would have merely been a combination of known prior art elements (Petrovic’s mixers, ADCs, and DSSP, and Eidson’s demodulator/decoder) according to known methods (sending the I and Q signals to the demodulator/decoder, as taught in Eidson) to yield predictable results (the signals are demodulated and decoded). As I explained above, and as a POSITA would have

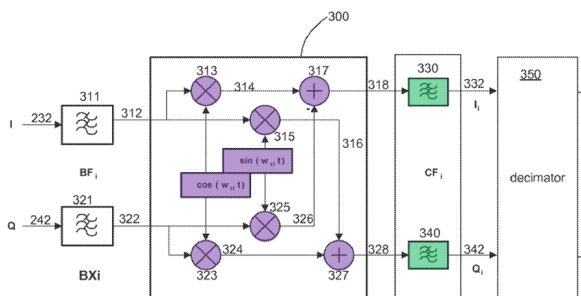
recognized, the output of a Petrovic tuner is the functional equivalent of the input to the Eidson demodulator/decoder. Thus, a POSITA could have, and would have, easily combined a Petrovic tuner and the Eidson demodulator/decoder, as each would perform the same function in the combination that would be performed individually prior to the combination. For the same reasons, it is my opinion that the results of combining the Petrovic tuner with the Eidson demodulator/decoder would have been predictable. Neither the function of the Petrovic tuner, nor the function of the Eidson demodulator/decoder, would change appreciably if combined, and thus each element could operate as it did before, leading to an expectation of success.

127. Although my above analysis explains why a POSITA would have added the Eidson demodulator/decoder to the Petrovic tuner, a POSITA would have been just as motivated to add the Petrovic tuner to the Eidson demodulator/decoder. This is because the I, Q signals output by the Petrovic DSSP are functionally equivalent to the I, Q signals received by the Eidson demodulator/decoder 40, and because the selection and stacking functions performed by the Petrovic tuner and by the Eidson front end are equivalent. Such equivalency would have taught a POSITA that the Petrovic tuner could be readily substituted for the Eidson front end. The advantages of, and motivation for, such a combination would have been the same as those described above for modifying Petrovic with Eidson. Moreover, in my opinion and for similar reasons, such a combination would have been merely a combination

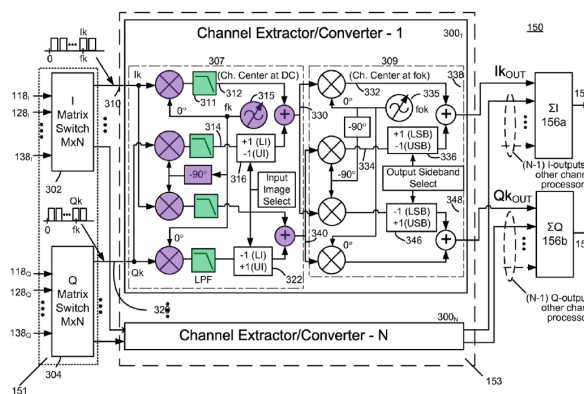
of known prior art elements according to known methods to yield predictable results with an expectation of success.

128. In the Petrovic-Eidson system, the Petrovic DSSP is, in my opinion, the “digital circuitry” of limitation [1D]. The Petrovic DSSP in Petrovic-Eidson is configured to select the plurality of desired television channels from the digitized plurality of frequencies (i.e., select channels from the digitized plurality of frequencies received by the DSSP); and output the selected plurality of television channels to a demodulator (the Eidson demodulator/decoder) as a digital datastream (the signals 158a, 158b).

129. To the extent that the “digital circuitry” of limitation [1D] is construed to be a means-plus-function term, and as seen by the below comparisons of Figure 6 and Petrovic and Figure 3 of the '362 patent, the Petrovic DSSP includes structure that is the same as, or equivalent to, structure of the complex mixers 250 and 300 and filters 260, 330, and 340 of the '362 patent. *See* Section 6.



Ex. 1101, Fig. 3 (annotated)



Ex. 1108, Fig. 6 (annotated)

130. Like complex mixer 300 of the '362 patent (**purple**), which is one of N complex mixers 250, the DSSP of Petrovic comprises N first stages 307, each of which comprises a complex mixer (**purple**). Ex. 1101, 6:7-42; Ex. 1108, [0066]-[0068], Fig. 6; Ex. 1109, [0045]-[0047], Fig. 3A; *see* Section 9.1.4; Ex. 1118 at 134, Figs. 2-3; Ex. 1134 at 35-36, Fig. 3.3. Like the filters 330 and 340 of the '362 patent (**green**), which are one of N filter modules 260, each first stage 307 of the Petrovic DSSP comprises low pass filters (LPF) 311 (**green**). Ex. 1101, 6:43-47; Ex. 1108, [0066]-[0069]; Ex. 1109 [0045]-[0048]; *see* Section 9.1.6. In my opinion, any differences between the '362 patent structure (N mixers 300 and N filters 330 and 340) and the Petrovic first stages 307 are insubstantial. Both perform the same function of selecting and outputting a respective desired channel, in the same way by first downconverting the respective desired channel to baseband and then low pass filtering with a filter to isolate the channel, to achieve the same result of producing a plurality of desired channels as a digital data stream. Ex. 1101, 5:49-6:47; Ex. 1108, [0060]-[0070]; Ex. 1109, [0037]-[0054].

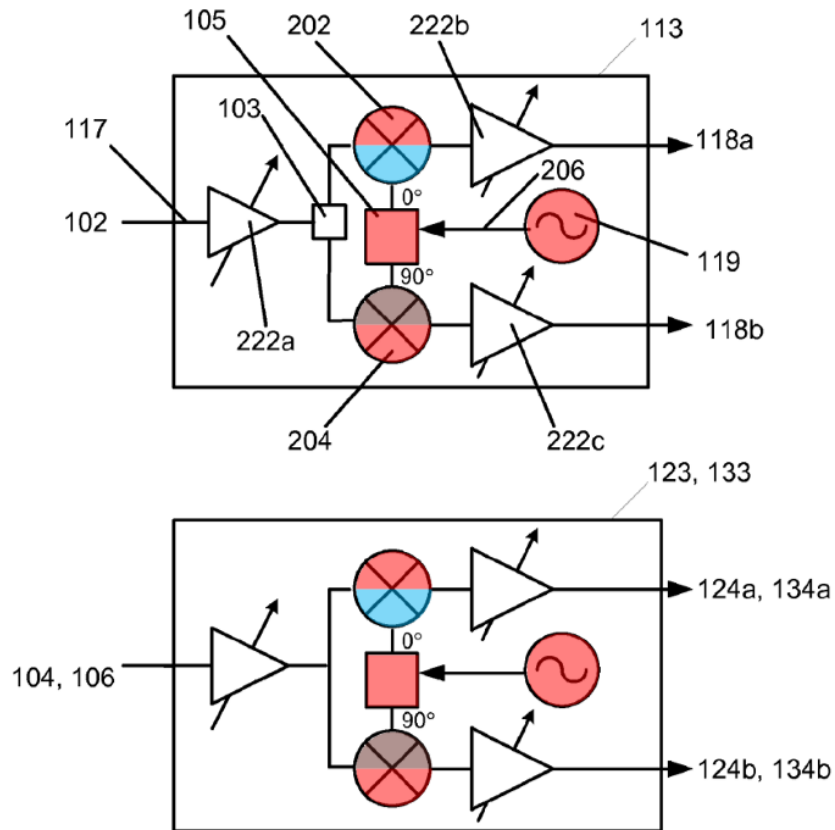
9.1.2 Dependent Claim 4

[4] “The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.”

131. It is my opinion that Petrovic describes “[t]he wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal,”

as recited in claim 4. Claim 4 depends from claim 1, which as I explained above is obvious over Petrovic-Eidson. *See* Section 9.1.1. As discussed below, Petrovic discloses the additional limitations of claim 4, and so claim 4 is also obvious over Petrovic-Eidson.

132. As I explained in Section 9.1.1.b above for limitation [1B], the mixers of any of the individual downconverters shown in Petrovic Figure 4 (e.g., downconverters 113, 123, 133), the mixers of any of the individual downconverters of other Petrovic embodiments, or the mixers of any combination of those downconverters, is a mixer module. Referring to Petrovic Figure 5 annotated below, each of those downconverters comprises a first mixer (**red/blue**) configured to generate an in-phase signal and a second mixer (**red/brown**) configured to generate a quadrature signal. Ex. 1108, [0034] (describing downconversion mixing operation “during which the signal ... is converted into a complex representation having a real I (in-phase) component and an imaginary Q (quadrature) component”), [0036]-[0037], [0039], Figs. 4-5; Ex. 1109, [0010], [0018], [0023], [0031]-[0032], Figs. 1-2.



Ex. 1108, Fig. 5 (annotated)

9.1.3 Dependent Claim 5

[5] “The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

133. It is my opinion that Petrovic discloses “[t]he wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal,” as recited in claim 5. Claim 5 depends from claim 1, which as I explained above is obvious over Petrovic-Eidson.

See Section 9.1.1. As discussed below, Petrovic discloses the additional limitations of claim 5, and so claim 5 is also obvious over Petrovic-Eidson.

134. As I explained in Section 9.1.1.c above for limitation [1C], any of the individual ADC pairs 108_I-108_M shown in Figure 4 of Petrovic, any of the individual ADC pairs of other Petrovic embodiments, or any combination of those ADC pairs, is a wideband ADC module. Each of those ADC pairs 108_I-108_M comprises “a first ADC configured to generate a digital in-phase signal” and “a second ADC configured to generate a digital quadrature signal.” Ex. 1108, [0039], [0051]-[0052], Fig. 4; Ex. 1109, [0010], [0013], [0018], [0022], [0024], [0028], Fig. 1. Referring to Petrovic Figure 4 as annotated below, “digital in-phase signal[s]” (**blue**) and “digital quadrature signal[s]” (**brown**) emanate from several of the Petrovic ADC pairs 108_I-108_M (**gold**), and are explicitly labeled as such (“I” or “Q”) in the figure.

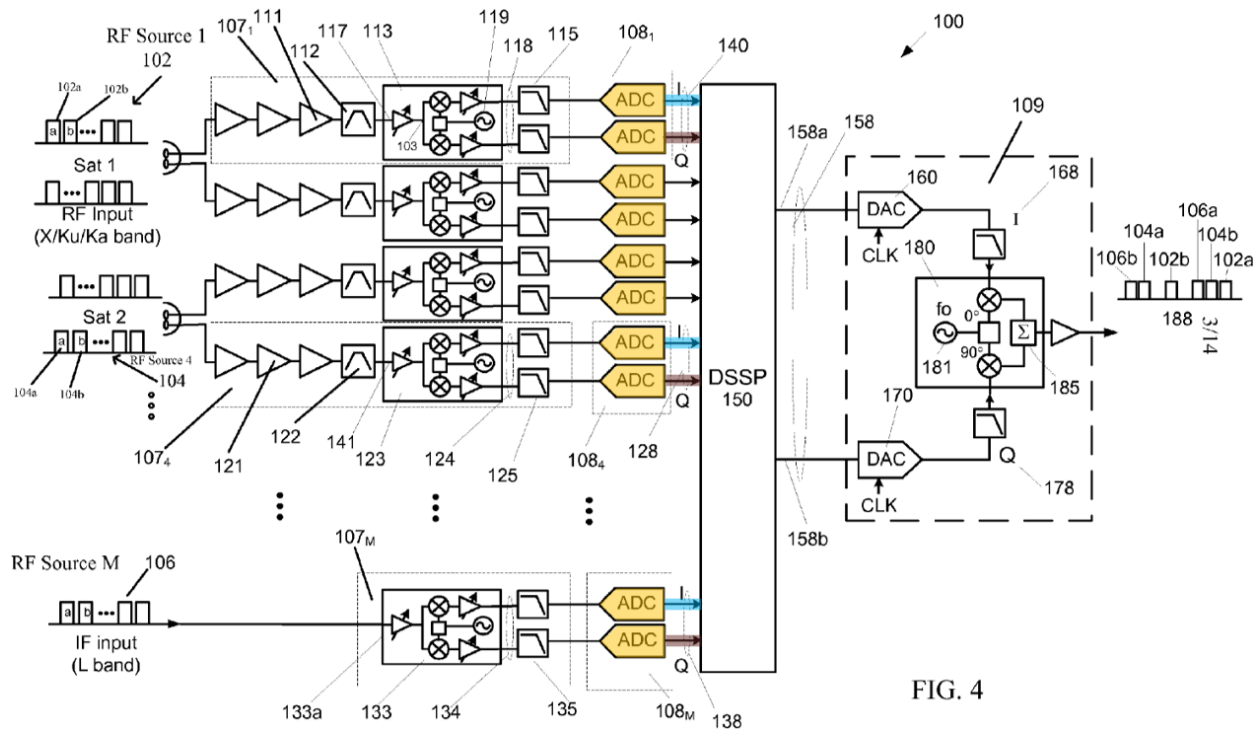


FIG. 4

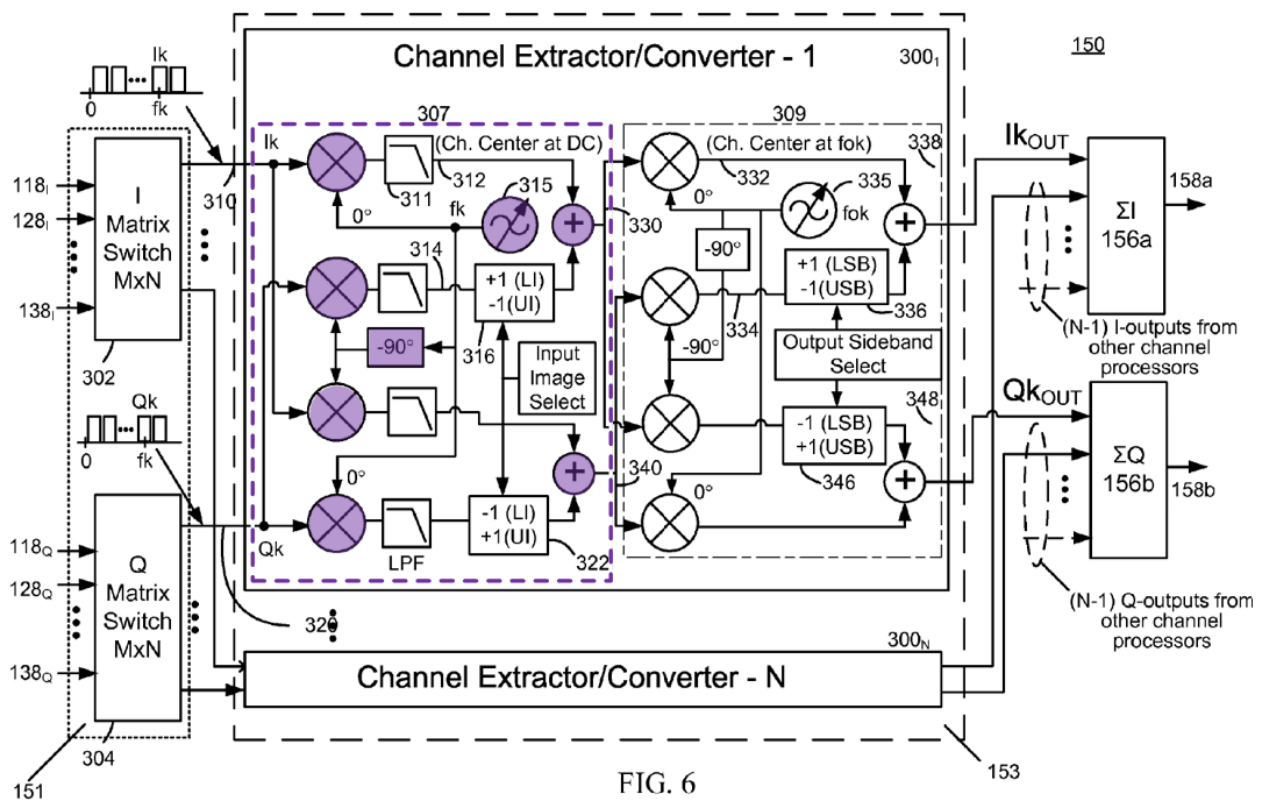
Ex. 1108, Fig. 4 (annotated)

9.1.4 Dependent Claim 6

[6] “The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.”

135. It is my opinion that Petrovic discloses “[t]he wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels,” as recited in claim 6. Claim 6 depends from claim 5, which as I explained above is obvious over Petrovic-Eidson. *See* Section 9.1.3. As discussed below, Petrovic discloses the additional limitations of claim 6, and so claim 6 is also obvious over Petrovic-Eidson.

136. As I explain above in Section 9.1.1.d for limitation [1D], the Petrovic system 100 includes “digital circuitry” in the form of a DSSP, for example the DSSP 150. Petrovic Figure 6 (annotated below) shows additional details of the DSSP 150 and of the DSSP of other Petrovic embodiments. The DSSP may include multiple “channel extractor/converter circuit[s] 300.” Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A.



Ex. 1108, Fig. 6 (annotated)

137. The DSSP 150 may have N channel extractor/converter circuits 300₁-300_N, where N may be equal to the number of selected channels to be included in the output signal 158. Ex. 1108, [0055], Fig. 6; Ex. 1109, [0033], Fig. 3A. Petrovic Figure 6 shows specific details of an exemplary channel extractor/converter circuit

300₁ of channel extractor/converter circuits 300₁-300_N. Ex. 1108, [0058], Fig. 6.; Ex. 1109, [0036], Fig. 3A. As is indicated by the subscript indices 1...N in Petrovic Figure 6, and as a POSITA would have understood, each of the other channel/extractor converter circuits 300 (of N total circuits 300) would have a structure identical or at least similar to that of circuit 300₁. Ex. 1108, Fig. 6; Ex. 1109, Fig. 3A. Moreover, the ellipsis in Figure 6 is commonly used in technical drawings to indicate repetition of like elements. Ex. 1108, Fig. 6; Ex. 1109, Fig. 3A. In addition, each of the circuits 300₁-300_N receives the same type of input (a digital Ik signal 310 and a digital Qk signal 320) and provides the same type of output (Ik_{OUT} and Qk_{OUT} signals for a selected channel), further indicating to a POSITA that each of the circuits 300 is the same as the circuit 300₁. Ex. 1108, [0061], [0086], Fig. 6; Ex. 1109, [0040], [0061], Fig. 3A.

138. Each of the N circuits 300₁-300_N thus includes a first stage 307 (**purple** broken line in Petrovic Figure 6 above) that selects a single desired channel. Ex. 1108, [0042], [0058]-[0077], Fig. 6; Ex. 1109, [0037]-[0054]. For each circuit 300, each of the in phase digital signal Ik 310 and the quadrature digital signal Qk 320 are multiplied by digital in-phase LO signal 315 and by the LO signals 315 quadrature phase (the LO signal 315 shifted in phase by 90 degrees). Ex. 1108, [0066]-[0077], Fig. 6; Ex. 1109, [0037]-[0054]. The results of these multiplications are the low-pass filtered (e.g., by LPFs 311) and recombined. *Id.*

139. For each of the N circuits 300₁-300_N, the first section 307, and in particular the individual shaded components (**purple**), is a complex mixer because it mixes (i.e., multiplies) a complex signal (i.e., a signal with in-phase and quadrature components) with the local oscillator (LO) signal 315. This mixing (multiplying) shifts the frequency of the complex signal (i.e., downconverts the I_k signal 310 and the Q_k signal 320) by the frequency of the LO signal. Ex. 1108, [0066]-[0068], Fig. 6; Ex. 1109, [0045]-[0047], Fig. 3A. As background, Mirabbasi explains that a complex mixer mixes a signal with a complex exponential, and is typically implemented with two real mixers for each component of the signal being mixed. Ex. 1118 at 134, Figs. 2-3. Where the signal is a real signal, then two real mixers are used; where the signal is a complex signal with two components (for example, in-phase and quadrature), then each component is mixed using two real mixers and an adder. *Id.*; *see also* Ex. 1134 at 35-36, Fig. 3.3 (showing a block diagram of a complex mixer). This is precisely what is shown in Petrovic Figure 6: the in-phase signal I_k is mixed using two real mixers and an adder, and the quadrature signal Q_k is mixed using two other real mixers and an adder. Ex. 1108, [0066]-[0077], Fig. 6; Ex. 1109, [0037]-[0054].

140. Because the DSSP 150 (and each of the DSSPs of other embodiments) includes multiple circuits 300 as I explained above, each having its own first section 307, each of the Petrovic DSSPs includes “a plurality of complex mixers configured

to frequency shift said selected plurality of desired television channels.” Ex. 1108, Fig. 6; Ex. 1109, Fig. 3A.

9.1.5 Dependent Claim 7

141. Claim 7 depends from claim 6, which as I explained above is obvious over Petrovic-Eidson. *See* Section 9.1.4. As discussed below, Petrovic also discloses limitations [7A] and [7B], and so claim 7 is also obvious over Petrovic-Eidson.

- a. **[7A] “The wideband receiver system of claim 6, wherein: prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”**

142. It is my opinion that Petrovic discloses “[t]he wideband receiver system of claim 6, wherein: prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum,” as claimed.

143. Petrovic Figure 4 shows that a received RF signal 104 may include channels 104a (**red**), 104b, etc., received in a frequency band above 3 GHz (e.g., the X band (7-12.5 GHz), Ku band (10.7-12.75 GHz), or Ka band (17.3-20.3 GHz)) and that a received RF signal 106 in the L band (950-2150 MHz) may include channels 106a, 106b (**red**), etc. Ex. 1108, [0029]-[0031], [0033], [0050], Fig. 4; Ex. 1109, [0010]-[0013], [0019]-[0020], [0023], Fig. 1.

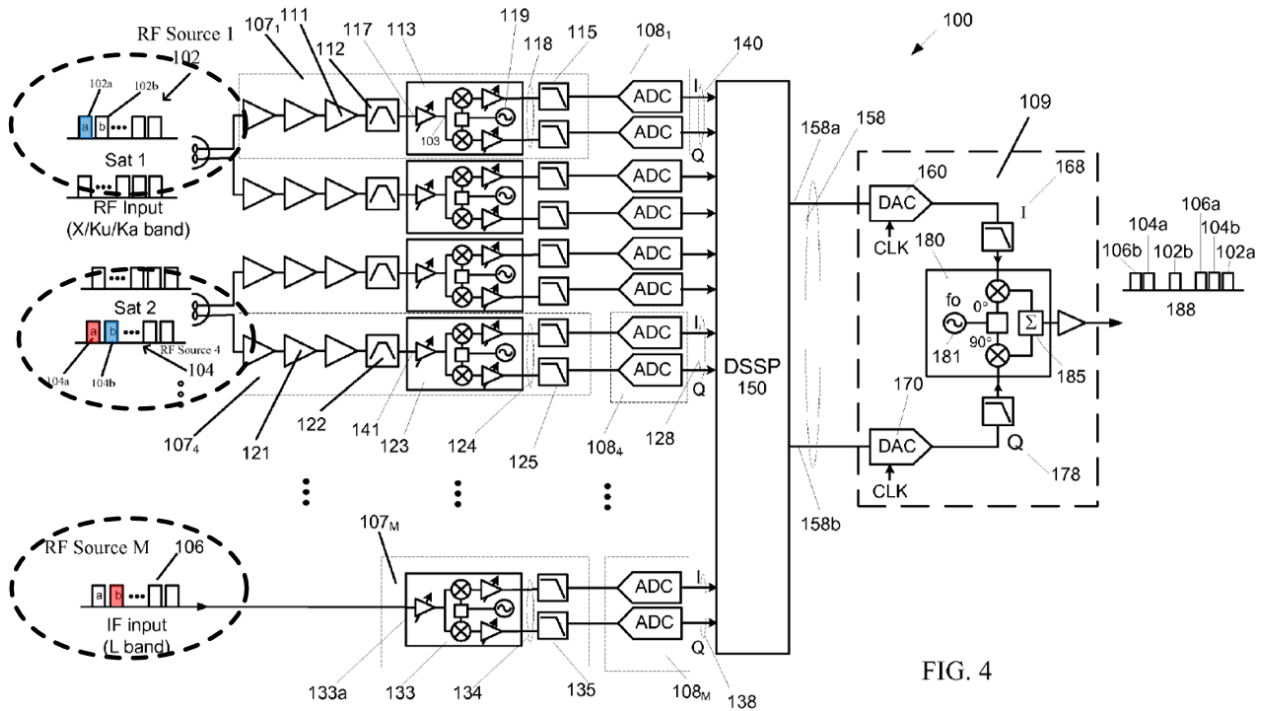


FIG. 4

Ex. 1108, Fig. 4 (annotated)

144. The signals 104a and 106b are channels that are assembled into the composite signal 158 that includes channels selected by the channel extractor/converter circuits 300 of the DSSP 150. Ex. 1108, [0053], Figs. 4, 6; Ex. 1109, Figs. 1, 3A. As shown in Figure 4 of Petrovic, the signals 104 and 106 are in different bands, and the channels 104a and 106b are non-contiguous prior to the frequency shift that occurs in the DSSP 150.

145. Moreover, Petrovic '886, which Petrovic incorporates by reference (Ex. 1108, [0001]), provides additional details regarding RF signals 102 and 104. In particular, Petrovic '886 indicates that the signals 102a (blue) and 102b may be in a lower half of the Ku band (10.7-11.725 GHz), and that the signals 104a and 104b (blue) may be in an upper half of the Ku band (11.725-12.75 GHz). Ex. 1109, [0019],

Fig. 1. The signals 102a and 104b are channels that are assembled into the composite signal 158 that includes channels selected by the channel extractor/converter circuits 300 of the DSSP 150. Ex. 1108, [0053], Figs. 4, 6; Ex. 1109, Figs. 1, 3A. As can be seen in Petrovic Figure 4 above, and based on the signals 102a and 104b being in different halves of the Ku band, channels 102a and 104b are non-contiguous prior to the frequency shift that occurs in the DSSP 150.

146. Even if Petrovic did not show two desired channels that are noncontiguous in an RF signal as received by a tuner (although I believe that Petrovic does show this), it is my opinion that a POSITA would have understood that the Petrovic system would receive at least some noncontiguous desired channels. In particular, the '362 patent admits that this is what "[e]xisting tuners" did. Ex. 1101, 1:27-31. Moreover, the very purpose of the Petrovic system 100 is to "'stack' or assemble channels resident within an RF signal into a composite signal in which the received channels are placed (or sequenced) in desired channel slots for output to a rendering device, such as a set-top box, or other receiver/tuner." Ex. 1108, [0028]; Ex. 1109, [0008]. The number of available slots in that composite signal may be much less than the total number of channels received by the system 100. Ex. 1108, [0029] (received signal 102 may have 120 or more channels), [0055] (output signal 158 may have as few as four channel slots); Ex. 1109, [0016], [0033]. In my opinion, a POSITA would thus have understood from Petrovic that, in order for the system 100 to *stack* four channels selected from 120 channels in an input signal, the system

100 would have been configured to select at least two channels that are not contiguous in the received RF signal.

b. [7B] “after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”

147. It is my opinion that Petrovic discloses “after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum,” as claimed.

148. As I explain in Section 9.1.5.a for limitation [7A], Petrovic Figure 4 shows non-contiguous channels 104a and 106b in received signals 104 and 106, as well as non-contiguous channels 102a and 104b in received signals 102 and 104. Referring to Petrovic Figure 4 annotated below, channels 104a (**red**) and 106b (**red**) are shown to be contiguous in a signal 188 that is after the frequency shift that occurs in the DSSP 150, and likewise channels 102a (**blue**) and 104b (**blue**) are shown to be contiguous in that signal 188. Ex. 1108, [0053]-[0054], Fig. 4; Ex. 1109, [0025], [0030], Fig. 1.

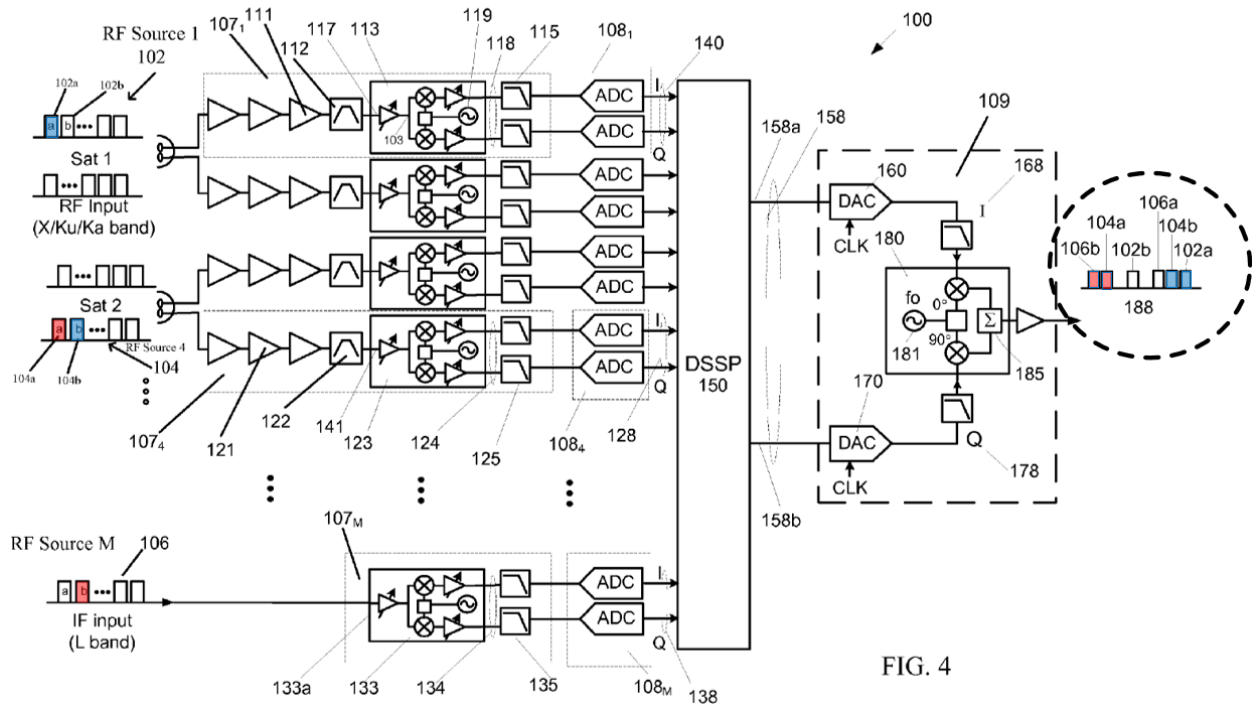


FIG. 4

Ex. 1108, Fig. 4 (annotated)

149. Because the stage 109 only converts signals 158a and 158b to analog, upconverts those analog signals, and combines the upconverted analog signals, channels 104a and 106b would also be contiguous in signals 158a and 158b that are output from the DSSP 150, and likewise channels 102a and 104b would be contiguous in those signals 158a and 158b. Ex. 1108, [0054], [0097], Figs. 4, 8; Ex. 1109, [0030], [0070], Figs. 1, 4.

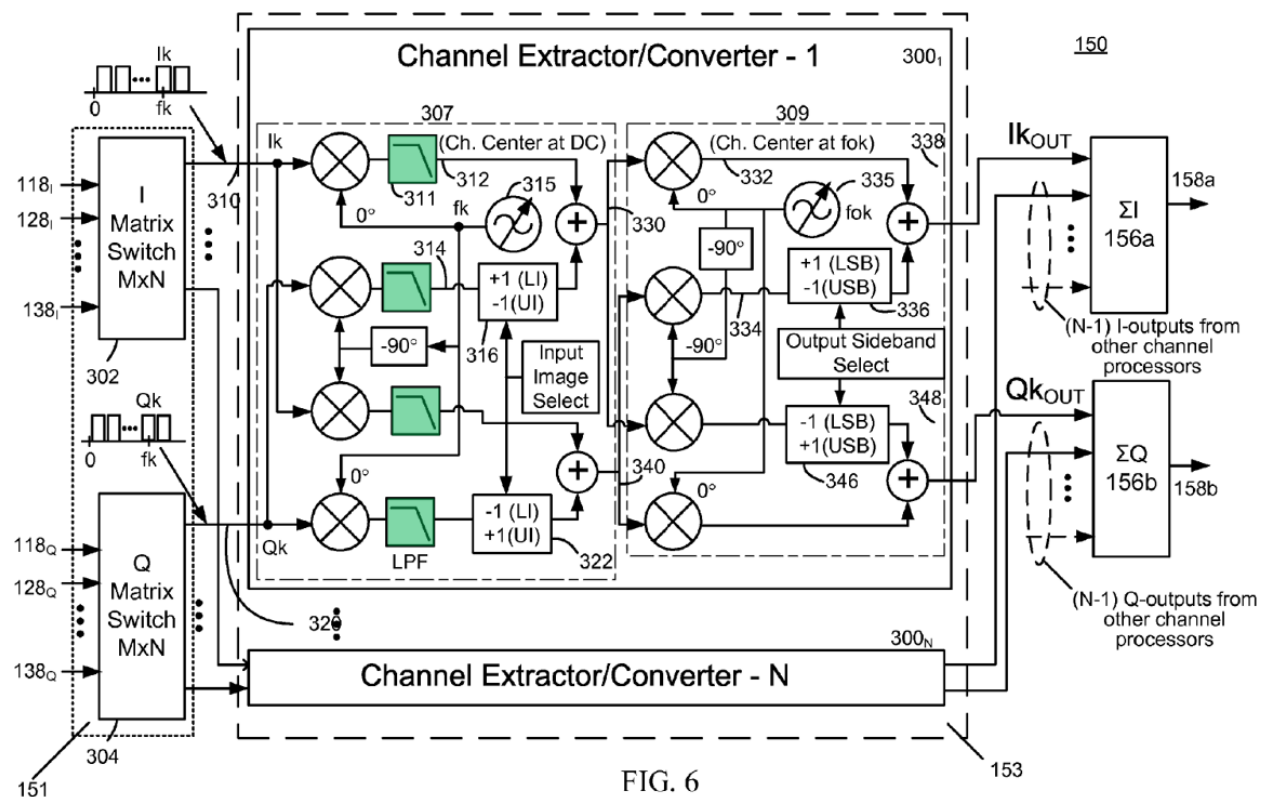
9.1.6 Dependent Claim 8

[8] “The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.”

150. It is my opinion that Petrovic discloses “[t]he wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters

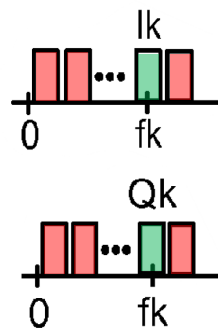
configured to perform said selection of said plurality of desired television channels,” as recited in claim 8. Claim 8 depends from claim 1, which as I explained above is obvious over Petrovic-Eidson. *See* Section 9.1.1. As discussed below, Petrovic discloses the additional limitations of claim 8, and so claim 8 is also obvious over Petrovic-Eidson.

151. As I explain in Section 9.1.1.d for limitation [1D], the Petrovic system 100 includes “digital circuitry” in the form of the DSSP 150, additional details of which are shown in Figure 6 as annotated below. Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A.



Ex. 1108, Fig. 6 (annotated)

152. Referring to Petrovic Figure 6 as annotated above, the DSSP 150 includes multiple sets of low pass filters 311 (four in each first portion 307 of each circuit 300) (**green**) that are configured to perform selection of desired television channels. Referring to an excerpted and annotated version of Petrovic Figure 6 below, first stage 307 receives the in-phase and quadrature signal components of the downconverted satellite signal, which contains a desired channel (I_k and Q_k in **green**) and undesired channels (**red**) as shown below. Ex. 1108, [0061]; Ex. 1109, [0040].



Ex. 1108, Fig. 6 (excerpted and annotated)

153. Stage 307 first utilizes a combination of mixers (represented with the symbol “ $\otimes$ ”) to multiply these signals by a LO signal 315 having a frequency f_k , which shifts the desired channel to zero and undesired channels to adjacent frequencies. Ex. 1108, [0066]-[0068]; Ex. 1109, [0045]-[0047]. Low pass filters 311 then select the desired channel by passing I_k and Q_k centered at zero to the output, while removing the undesired channels, which are outside of the filter channel bandwidth. Ex. 1108, [0066]-[0069]; Ex. 1109, [0045]-[0048]. This type of desired

channel selection in Petrovic is the same as that described by the '362 patent. Ex. 1101, 6:43-47.

9.1.7 Independent Claim 11

154. The limitations of claim 11 appear in the Claims Listing Appendix, labeled as limitations [11A]-[11E]. Claim 11 is a method claim directed to substantially identical subject matter as system 1, in which steps [11A]-[11E] recast the required functionality of limitations [1A]-[1D] as method steps performed by identical structural elements, and thus are rendered obvious by Petrovic in view of Eidson for the same reasons discussed above with respect to claim 1. See my explanation above at Sections 9.1.1.a through 9.1.1.d. *See also, e.g.*, Ex. 1108, Title (“Channel Stacking System and Method of Operation”) (underscore added), [0008]-[0009]; Ex. 1109, Title, [0004]-[0005].

a. [11A] “A method comprising: in a wideband receiver system:”

155. It is my opinion that Petrovic discloses “[a] method comprising: in a wideband receiver system:” as claimed.

156. Preamble [11A] is directed to substantially identical subject matter as preamble [1A] and thus is taught by Petrovic for the same reasons I discuss above with respect to preamble [1A]. See my explanation at Section 9.1.1.a.

- b. **[11B] “downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”**

157. It is my opinion that Petrovic discloses “downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels,” as claimed.

158. Limitation [11B] is directed to substantially identical subject matter as limitation [1B] and thus is taught by Petrovic for the same reasons I discuss above with respect to limitation [1B]. See my explanation at Section 9.1.1.b.

- c. **[11C] “digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”**

159. It is my opinion that Petrovic discloses “digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels,” as claimed.

160. Limitation [11C] is directed to substantially identical subject matter as limitation [1C] and thus is taught by Petrovic for the same reasons I discuss above with respect to limitation [1C]. See my explanation at Section 9.1.1.c.

- d. **[11D] “selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and”**

[11E] “outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.”

161. It is my opinion that Petrovic discloses “selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies,” and “outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream,” as claimed.

162. Limitations [11D] and [11E] are directed to substantially identical subject matter as limitation [1D] and thus are taught by Petrovic-Eidson for the same reasons I discuss above with respect to limitation [1D]. See my explanation at Section 9.1.1.d.

9.1.8 Dependent Claim 14

[14] “The method of claim 11, comprising: generating, by a first mixer of said mixer module, an in-phase signal; and generating, by a second mixer of said mixer module, a quadrature signal.”

163. Claim 14 is directed to substantially identical subject matter as claim 4, by recasting the required functionality of claim 4 as a method step performed by identical structural elements, and thus is rendered obvious by Petrovic in view of Eidson for the same reasons I discuss above with respect to claim 4. See my explanation at Section 9.1.2.

9.1.9 Dependent Claim 15

[15] “The method of claim 11, comprising: generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.”

164. Claim 15 is directed to substantially identical subject matter as claim 5, by recasting the required functionality of claim 5 as a method step performed by identical structural elements, and thus is rendered obvious by Petrovic in view of Eidson for the same reasons I discuss above with respect to claim 5. See my explanation at Section 9.1.3.

9.1.10 Dependent Claim 16

[16] “The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.”

165. Claim 16 is directed to substantially identical subject matter as claim 6, by recasting the required functionality of claim 6 as a method step performed by identical structural elements, and thus is rendered obvious by Petrovic in view of Eidson for the same reasons I discuss above with respect to claim 6. See my explanation at Section 9.1.4.

9.1.11 Dependent Claim 17

166. Claim 17 is directed to substantially identical subject matter as claim 7, by recasting the required functionality of claim 7 as a method step performed by identical structural elements, and thus is rendered obvious by Petrovic in view of

Eidson for the same reasons I discuss above with respect to claim 7. See my explanation at Section 9.1.5.

- a. [17A] **“The method of claim 16, wherein: prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”**

167. Limitation [17A] is directed to substantially identical subject matter as limitation [7A] and thus is rendered obvious by Petrovic in view of Eidson for the same reasons I discuss above with respect to limitation [7A]. See my explanation at Section 9.1.5.a.

- b. [17B] **“after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”**

168. Limitation [17B] is directed to substantially identical subject matter as limitation [7B] and thus is rendered obvious by Petrovic in view of Eidson for the same reasons I discuss above with respect to limitation [7B]. See my explanation at Section 9.1.5.b.

9.1.12 Dependent Claim 18

“The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.”

169. Claim 18 is directed to substantially identical subject matter as claim 8 and thus is rendered obvious by Petrovic in view of Eidson for the same reasons I discuss above with respect to claim 8. See my explanation at Section 9.1.6.

9.2 Petrovic in View of Takahiko, and further in view of Eidson, Render Claims 1, 4-8, 11, and 14-18 Obvious

170. In the following, I provide a limitation-by-limitation analysis showing how Petrovic in view of Takahiko, and further in view of Eidson, render 1, 4-8, and 14-18 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.2.1 Independent Claim 1

171. The limitations of claim 1 appear in the Claims Listing Appendix, labeled as limitations [1A]-[1D]. For the following reasons, it is my opinion that claim 1 is rendered obvious over Petrovic in view of Takahiko, and further in view of Eidson.

a. [1A] “A wideband receiver system comprising:”

[1B] “a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”

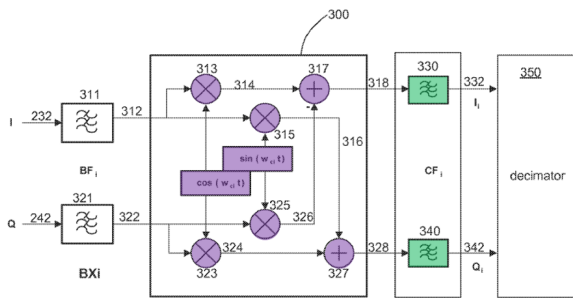
[1C] “a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”

172. Petrovic discloses limitations [1A]-[1C] for the reasons explained in Sections 9.1.1.a through 9.1.1.c, above.

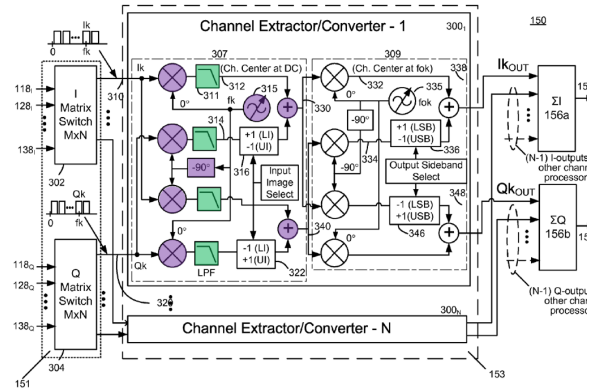
- b. [1D] “digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.”

173. As I explained in Section 9.1.1.d above, and as illustrated by the side-by-side comparison of Figure 3 of the '362 patent and Figure 6 of Petrovic, any differences between the Petrovic first stage 307 and the mixer 300 and filters 330 and 340 of the '362 patent are insubstantial.

174. In my opinion, the location of LPFs 311 within the complex mixer, as shown in Figure 6 of Petrovic (annotated below), is the same or equivalent structure as the complex mixer 300 and filters 330 and 340 of Figure 3 of the '362 patent (also annotated below). However, to the extent that the patent owner contends that the location of LPFs 311 is not the same or equivalent structure as the complex mixer 300 and filters 330 and 340, it is my opinion that placing four low pass filters before adders (the “ $\oplus$ ” symbols in the above Figures) of a complex mixer (as shown in Petrovic Fig. 6) or two low pass filters after adders of a complex mixer (as shown in '362 patent Figs. 2-3) would have been functionally equivalent and merely a matter of design choice, as both options were well known to a POSITA.

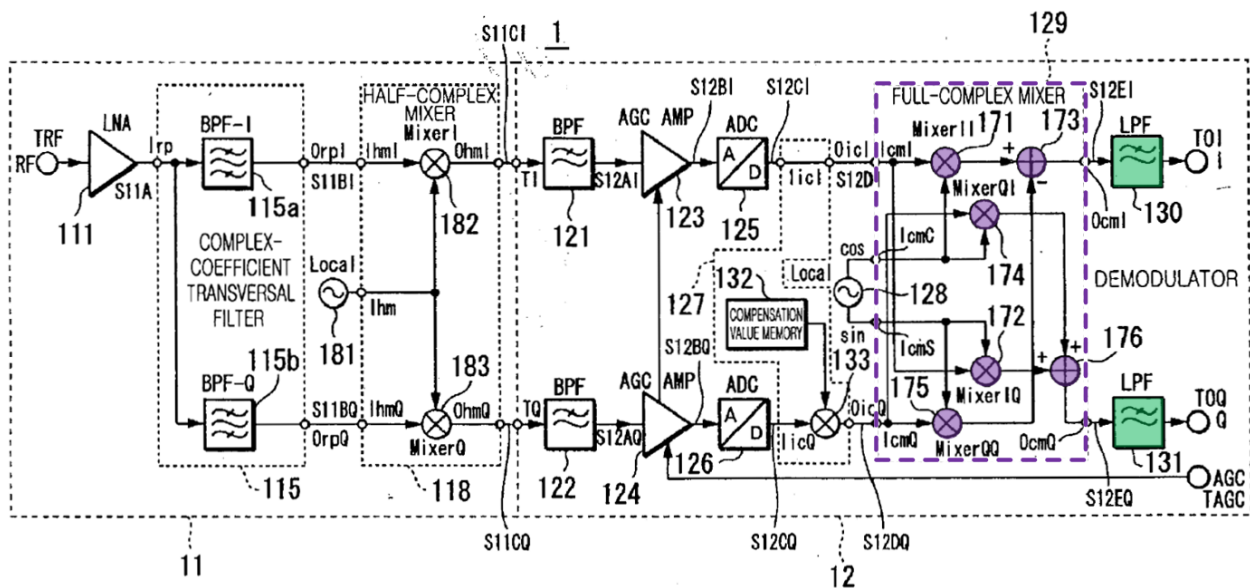


Ex. 1101, Fig. 3 (annotated)



Ex. 1108, Fig. 6 (annotated)

175. For example, Takahiko describes a “downconverter” 1 that is used in a radio receiver, and that is very similar to the receiver of '362 patent Figure 2. Ex. 1161, [0143], Fig. 1.



Ex. 1161, Fig. 1 (annotated)

176. Referring to the annotated figure above, Takahiko’s downconverter 1 discloses a “full-complex mixer” 129 (purple, broken-line purple box) and low pass filters (green) 130 and 131 that are the same as what is shown in Figure 3 of the

'362 patent. Moreover, in my opinion, Takahiko uses full-complex mixer 129 and filters 130 and 131 in the same way that the '362 patent describes use of complex mixer 300 and filters 330 and 340: downconversion of digital I, Q signals so a desired channel is at baseband and removal of unwanted higher frequencies with low-pass filtering. Ex. 1161, [0153], [0156].

177. In my opinion, a POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 to use two low pass filters after the adders of the complex mixer, similar to the configuration of the Takahiko full-complex mixer 129 and filters 130 and 131 located after adders 173 and 176, and instead of four low pass filters within the complex mixer, to make the circuit simpler and less expensive. Such a modification would have merely involved use of known circuit components in known arrangements, because of the similarity between the relevant portions of the Petrovic first sections 307 and the Takahiko full-complex mixer 129 and filters 130 and 131, and because the Takahiko full-complex mixer 129 and filters 130 and 131 would have been functionally equivalent to a Petrovic first section 307. Thus, a POSITA would have had a reasonable expectation of success, and the results of the modification would have been predictable to a POSITA.

178. It is also my opinion that a POSITA would have combined the Petrovic channel stacking system, as modified in view of Takahiko, with the Eidson demodulator/decoder for the reasons explained in Section 9.1.1.d., as the modification would not have affected the input provided to a corresponding second

stage 309 of the Petrovic DSSP, nor would it have affected the signals 155a, 158b generated by the DSSP.

9.2.2 Dependent Claims 4-7

[4] “The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.”

[5] “The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.”

[6] “The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.”

[7A] “The wideband receiver system of claim 6, wherein: prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”

[7B] “after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”

179. The limitations of claims 4-7 are taught by Petrovic-Takahiko-Eidson for the reasons explained in Sections 9.1.2 through 9.1.5, as the addition of Takahiko does not affect the disclosure by Petrovic of those limitations. Accordingly, in addition to being obvious over Petrovic-Eidson as discussed in Sections 9.1.2 through 9.1.5, claims 4-7 are also obvious over Petrovic-Takahiko-Eidson.

9.2.3 Dependent Claim 8

[8] “The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.”

180. The limitation of claim 8 is taught by Petrovic-Takahiko-Eidson. As modified in view of Takahiko, the LPFs would be located after the adders of the complex mixer of a Petrovic first stage 307, would have the same configuration as shown in Figure 3 of the '362 patent, and would operate, similar to the LPFs 311 of Petrovic, to select the desired channel by passing I_k and Q_k centered at zero to the output, while removing the undesired channels, which would be outside of the filter channel bandwidth. Furthermore, there are plurality Petrovic first stage 307 circuits, 1-N with a plurality of 311 filters in each stage as indicated by the ellipsis on Figure 6 as I described in section 9.1.4, claim 6. Accordingly, in addition to being obvious over Petrovic-Eidson as discussed in Section 9.1.6, claim 8 is also obvious over Petrovic-Takahiko-Eidson.

9.2.4 Independent Claim 11

[11A] “A method comprising: in a wideband receiver system:”

[11B] “downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;”

[11C] “digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;”

[11D] “selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and”

[11E] “outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.”

181. Limitation [11A]-[11E] recast the required functionality of limitations [1A]-[1D] as method steps performed by identical structural elements. Thus, claim 11 is directed to substantially identical subject matter as claim 1 and is obvious over Petrovic-Takahiko-Eidson for the reasons discussed above with respect to claim 1. *See* Section 9.2.1.

9.2.5 Dependent Claims 14-17

[14] “The method of claim 11, comprising: generating, by a first mixer of said mixer module, an in-phase signal; and generating, by a second mixer of said mixer module, a quadrature signal.”

[15] “The method of claim 11, comprising: generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.”

[16] “The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.”

[17A] “The method of claim 16, wherein: prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and”

[17B] “after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.”

182. Claims 14-17 recast the required functionality of claims 4-7 as method steps performed by identical structural elements. Thus, claims 14-17 are directed to substantially identical subject matter as claims 4-7 and are obvious over Petrovic-Takahiko-Eidson for the reasons discussed above with respect to claims 4-7. *See* Section 9.2.2.

9.2.6 Dependent Claim 18

“The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.”

183. Claim 18 is directed to substantially identical subject matter as claim 8, and thus is obvious over Petrovic-Takahiko-Eidson for the reasons discussed above with respect to claim 8. *See* Section 9.2.3.

9.3 Petrovic in View of Eidson, and further in View of Rabaey, Render Claims 2, 3, 12, and 13 Obvious

184. In the following, I provide a limitation-by-limitation analysis showing how Petrovic in view of Eidson, and further in view of Rabaey, render claims 2, 3, 12, and 13 obvious. To help illustrate how the disclosures of these references map to the claim limitations, I have color coded some of my remarks and some figures in the noted art below.

9.3.1 Dependent Claims 2 and 3

[2] “The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.”

[3] “The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.”

185. Claims 2 and 3 are similar, and only differ with regard to a type of interface via which the digital datastream of limitation [1D] is output. Ex. 1101, 11:66-12:2. Claim 2 recites output “via a serial interface,” while claim 3 recites output “via a parallel interface.” *Id.* But as explained below, either option would have been an obvious design choice, and thus it is my opinion that claims 2 and 3 are obvious over Petrovic in view of Eidson and Rabaey.

186. As I explain in Sections 8.5 and 8.6, Petrovic discloses a DSSP 150 (or a DSSP of another Petrovic embodiment) as the “digital circuitry configured to:... output said selected plurality of television channels ... as a digital datastream” of

limitation [1D]. As the '362 patent concedes, the outputting of a digital data stream via serial (claim [2]) and parallel (claim [3]) interfaces were “commonly known methods.” Ex. 1101, 6:55-58. Indeed, as confirmed by dictionaries, basic text books and technical papers on digital integrated circuit design at the time, a POSITA would have understood parallel and serial interfaces as the two common options for outputting data in standard integrated circuits. For example, Pandey explains that the Universal Serial Bus was well known. Ex 1114, 9:44-50. And Rabaey (which I discuss in more detail below) explains that data can be transmitted in a time-multiplexed manner using a serial data transmission architecture or using dedicated transmission resources with a parallel data transmission architecture. Ex. 1116 at 79-80. According to Rabaey, if the data being transmitted were random, then it would make no difference which architecture is used, and if the data has distinct temporal correlation, then it may be more power-efficient to use a parallel architecture. *Id.* On the other hand, a parallel architecture requires more physical electrical transmission conductors than a serial architecture. Compare, for example, the parallel data transmission architecture of Rabaey Figure 6.25(a) having two transmission conductors (one for signal A and another for signal B) as opposed to the serial data transmission architecture of Rabaey Figure 6.25(b) having only a single transmission conductor shared by signals A and B. *Id.*

187. Notably, Petrovic discloses the DSSP 150 and other components of the system 100 may be implemented as “hardware.” Ex. 1108, [0124]-[0125]; Ex. 1109,

[0115]. Petrovic also explains that “various actions described herein can be performed by specific circuits (e.g., discrete circuitry or application specific integrated circuits (ASICs))” and that the DSSP 150 can be an ASIC. Ex. 1108, [0027], [0040]; Ex. 1109, [0009]. A POSITA would have understood Petrovic’s use of the term “hardware” to include “circuits” such as ASICs. Thus, a POSITA would have understood Petrovic as disclosing that various components of the system 100, including the DSSP, may be implemented as hardware such as an ASIC. As I explain in Section 9.1.1.d for limitation [1D], a POSITA would have modified Petrovic so that a Petrovic tuner—which includes a DSSP outputting the digital data stream—would output digital data to the Eidson demodulator/decoder. Eidson indicates that a front end and a multichannel demodulator/decoder could be integrated into a single package, which further indicates digital data would flow from a Petrovic DSSP to an Edison demodulator/decoder using conventional integrated circuit interfaces. Ex. 1112, 6:33-35.

188. At the most fundamental level, a digital integrated circuit represents data as binary units (referred to as “bits”) in the form of electrical signals on wires (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1116 at 23-24, 27-29, 48-51. To output multiple bits (i.e., as a “digital datastream”), the circuit can either transmit the bits over multiple separate wires, one wire for each bit, which was known as a “parallel interface,” or the circuit can transmit the set of bits one at a time as sequential pulses over a single wire, according to a fixed

sequence, which was known as a “serial interface.” See my discussion above, in Section 8.4, about serial versus parallel data communication. *See also*, Ex. 1115 at 5-6; Ex. 1116 at 79-80 (Figure 6.25, annotated below).

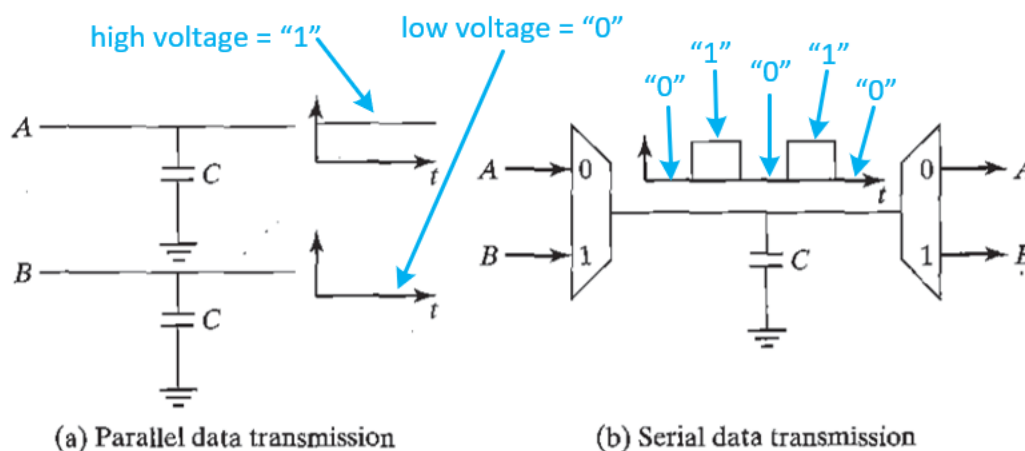


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1116 at 80 (Figure 6.25) (annotated)

189. In my opinion, implementing a data interface between a Petrovic DSSP and an Eidson demodulator/decoder using either option would have been equally obvious as one of two design choices, because both were “commonly known methods” used by POSITAs. Ex. 1114, 30:31-42, 31:15-22; Ex. 1115 at 4-6 (defining serial and parallel transmission); Ex. 1116 at 79-80; Ex. 1117 at 354-355. *Also see* Section 8.4 above for my discussion of serial data communication and parallel data communication. For the same reasons, implementing serial and parallel interfaces would have been well within the POSITA’s skillset, and thus, a POSITA would have had a high expectation of success leading to a predictable result.

190. Indeed, Rabaey and various background references teach and confirm why a POSITA would have applied parallel and serial interfaces to Petrovic's digital design. For example, Rabaey, a textbook on implementing digital integrated circuits, teaches that both serial and parallel interfaces as illustrated in the Figure 6.25 above were beneficially used in integrated circuits. Ex. 1116 at 79-80. According to Rabaey, time-multiplexing (i.e., a serial interface) "is an often used technique to minimize the implementation area" of a design on a chip, but that this "minimum area solution does not always result in the lowest switching activity," for example, when the data signals have high "temporal correlation." Ex. 1116 at 79-80; *see also Id.* at 72-74. Minimizing circuit area minimizes the cost of the integrated circuit, while minimizing the switching activity minimizes the "dynamic power consumption" of the integrated circuit. Ex. 1116 at 29-33, 43-44, 72-74, 76-80. In fact, the area taken up by a circuit on an integrated circuit can have a major impact on the cost of that integrated circuit. Where a circuit is implemented on a die of an integrated circuit wafer, "die costs are proportional to the fourth power of the area" of the die. Ex. 1116 at 31. Thus, Rabaey teaches selecting between serial and parallel interfaces for transmitting digital data between two points, both of which have advantages over each other, depending upon area and power constraints and the temporal correlation between the signals. Ex. 1116 at 29-33, 43-44, 72-74, 76-80.

191. In my opinion, it would have been obvious to apply either of Rabaey's parallel data or serial interfaces as illustrated in Figure 6.25 to the interconnection

between Petrovic's DSSP and Eidson's demodulator/decoder. Petrovic and Edison teach implementation in an integrated circuit, and the techniques taught in Rabaey would have enabled such implementation. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116 at 76-80. As such, the modification of Petrovic and Eidson with Rabaey that results in a serial interface (claim 2) between Petrovic's DSSP and Eidson's demodulator/decoder would have been nothing more than a combination of prior art elements, namely Petrovic's circuit design and Rabaey's serial interface interconnects, according to known methods (Rabaey's process for implementing circuit designs, including selecting a serial interface to minimize chip area and cost) to yield predictable results (data is sent serially). Likewise, the modification of Petrovic and Eidson with Rabaey that results in a parallel interface (claim 3) between Petrovic's DSSP and Eidson's demodulator/decoder would also have been nothing more than a combination of prior art elements (Petrovic's and Eidson's circuit designs and Rabaey's parallel interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a parallel interface to minimize switching and power) to yield predictable results (data is sent in parallel).

192. It is my opinion that the resultant combinations of Petrovic, Eidson, and Rabaey were predictable, and that a POSITA would have had a reasonable expectation of success, because Rabaey teaches basic techniques used by POSITAs to design integrated circuits, and because those techniques are specifically directed

to overcoming specific issues, such as meeting area and power constraints as I discussed above, that a POSITA would customarily balance in their designs. Ex. 1116 at 29-33, 43-44, 72-74, 76-80.

9.3.2 Dependent Claims 12 and 13

[12] “The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.”

[13] “The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.”

193. Claims 12 and 13 are directed to substantially identical subject matter as claims 2 and 3, respectively, by recasting the required functionality of claims 2 and 3 as method steps performed by identical structural elements. Thus, claims 12 and 13 are rendered obvious by Petrovic in view of Eidson and Rabaey for the same reasons I discuss above with respect to claims 2 and 3. See my explanation at Section 9.3.1.

9.4 Petrovic in View of Takahiko, and Further in View of Eidson and Rabaey, Render Claims 2, 3, 12, and 13 Obvious

194. In addition to being obvious over Petrovic-Eidson-Rabaey, claims 2-3 and 12-13 are also obvious over Petrovic-Takahiko-Eidson-Rabaey for the reasons explained in Sections 9.2.1, 9.3.1, and 9.3.2, as modification in view of Takahiko does not affect modification in view of Rabaey.

9.5 Petrovic in View of Eidson, and Further in View of Jensen, Render Claims 9, 10, 19, and 20 Obvious

195. In the following, I provide a limitation-by-limitation analysis showing how Petrovic in view of Eidson, and further in view of Jensen, render claims 9, 10, 19, and 20 obvious.

9.5.1 Dependent Claim 9

[9] “The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.”

196. As I explain in Section 9.1.6 for claim 8, Petrovic discloses low pass filters 311 that are configured to perform selection of desired television channels. Ex. 1108, [0066]-[0069], Fig. 6; Ex. 1109, [0045]-[0048], Fig. 3A. Petrovic does not explicitly indicate whether the low pass filters 311 would be finite impulse response (FIR) filters. As explained by Jensen, however, FIR filters were “[a] popular class of filters for channel-select filtering ... because of their inherent linear phase response.” Ex. 1126, [0007]. A POSITA would have selected FIR filters for use as the low pass filters 311 of Petrovic to take advantage of their linear phase response, which avoids distorting the received signal, and would have known to do so because of the popularity of such filters. Ex. 1126, [0006]. As disclosed by Jensen, the use of FIR filters was popular (and thus well-known) for channel selection in the digital domain and thus easily obtainable, and thus it is my opinion that the result of using

FIR filters for the Petrovic low pass filters 311 would have been predictable to a POSITA, leading to a reasonable expectation of success. Ex. 1126, [0006]-[0007].

197. Using FIR filters for the Petrovic low pass filters 311 would also have been, in my opinion, a simple substitution of one known element for another to obtain predictable results. FIR filters, their functions, and their uses were well-known in the art. Ex. 1126, [0006]-[0007]. Because FIR filters, their functions, and their uses were well known, a POSITA would have been able to successfully implement the Petrovic circuit 300 using FIR filters as the low pass filters 300, and the results of such a simple substitution would have been predictable to a POSITA.

9.5.2 Dependent Claim 10

[10] “The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.”

198. As I explain in Section 8.5 (introduction of Petrovic) and Section 9.1.1.d (limitation [1D]), Petrovic discloses a DSSP as “digital circuitry configured to[] select said plurality of desired television channels ... and output said selected plurality of television channels ... as a digital datastream”. Petrovic is silent with regard to whether the DSSP 150 comprises a decimator circuit. However, as explained by Jensen, decimation was commonly performed to reduce a sampling rate of a digital signal, because reducing sampling rate would reduce power consumption and complexity in subsequent processing. Ex. 1126, [0007]; *see also* Section 8.3.4.

199. Such decimation would have been particularly relevant if the Petrovic stage 109 were retained after modification of Petrovic in view of Eidson. As I explain in Section 9.1.1.d (for limitation [1D]), stage 109 may be retained if Petrovic were modified in view of Eidson to implement, as suggested by Eidson, a media center STB that would feed other set top boxes. In such a configuration, Petrovic as modified in view of Eidson would receive a wideband RF source that includes undesired and desired channels (for example, 120 channels) and output a composite signal with a reduced number of desired channels (for example, four channels) to a lower bandwidth cable. Ex. 1108, [0005], [0029], [0044]-[0045], [0054]-[0055]. Thus, the rate of Petrovic's ADCs for sampling the RF source signals would be higher than the rate required by the digital-to-analog converters (DACs) in stage 109 to reproduce the analog composite signal. Ex. 1108, [0005], [0029], [0044]-[0045], [0054]-[0055].

200. In my opinion, a POSITA would have followed the teachings of Jensen to include a decimator circuit in the Petrovic DSSP 150, either as a separate component following the low pass filters 311 or as part of channel-select decimation filters used for the low pass filters 311. This would have reduced the sampling rate of digital signal, thereby reducing power consumption and/or complexity in subsequent processing such as by stage 309 in DSSP 150, and potentially also in stage 109 (including the DACs) that follows DSSP 150. Ex. 1126, [0007]; Ex. 1108, Figs. 4, 6; Ex. 1109, Figs. 1, 3A. Jensen teaches that the use of decimation modules

or of channel-select decimation filters (which combined a FIR filter with decimation) was common (and thus well-known). In view of this teaching by Jensen, it is my opinion that the result of including decimation in the Petrovic DSSP 150 would have been predictable to a POSITA, leading to a reasonable expectation of success. Ex. 1126, [0007].

201. Moreover, and in my opinion, including a decimator circuit in the Petrovic DSSP 150 would have merely involved the use of a known technique to improve a similar device and method in the same way. Decimators, and their use in channel selection circuits, and the improvement resulting from decimator use, were well known. Ex. 1126, [0007]. Because decimators, their functions, and their improvement to channel selection circuits were well known (in addition to Jensen, *see* Section 8.3.4), in my opinion a POSITA would have been easily able to include a decimator in the Petrovic circuit 300, and the results of doing so would have been predictable to the POSITA.

9.5.3 Dependent Claim 19

[19] “The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.”

202. Claim 19 is directed to substantially identical subject matter as claim 9 and thus is rendered obvious by Petrovic in view of Eidson and Jensen for the same reasons I discuss above with respect to claim 9. See my explanation above at Section 9.5.1.

9.5.4 Dependent Claim 20

[20] “The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of desired television channels prior to said outputting of said selected plurality of television channels.”

203. Claim 20 is directed to substantially identical subject matter as claim 10, by recasting the required functionality of claim 10 as a method step performed by identical structural elements, and thus is rendered obvious by Petrovic in view of Eidson and Jensen for the same reasons I discuss above with respect to claim 10. See my explanation above at Section 9.5.2.

9.6 Petrovic in View of Takahiko, and Further in View of Eidson and Jensen, Render Claims 9, 10, 19, and 20 Obvious

9.6.1 Dependent Claims 9 and 19

204. The limitations of claims 9 and 19 are disclosed by Petrovic-Takahiko -Eidson-Jensen for the reasons explained in Sections 9.2.1, 9.5.1 and 9.5.3, as the advantages of (and motivation for) using a FIR filter would still apply if the Petrovic first stages 307 were modified, in view of Takahiko, to have LPFs after the complex mixer. Accordingly, claims 9 and 19 are obvious over Petrovic-Takahiko -Eidson-Jensen.

9.6.2 Dependent Claims 10 and 20

205. Claims 10 and 20 are obvious over Petrovic-Takahiko-Eidson-Jensen for the reasons explained in Sections 9.2.1, 9.5.2, and 9.5.4, as modification in view

of Takahiko does not affect the motivation to modify Petrovic-Eidson, in view of Jensen, to include a decimator circuit (claim 10) or perform decimating (claim 20). For example, a POSITA would include a decimator circuit after the LPFs that would be placed (per Takahiko) after the Petrovic complex mixer or incorporate the decimator into such LPFs (per Jensen's disclosure of channel-select decimation filters). Accordingly, claims 10 and 20 are obvious over Petrovic-Takahiko -Eidson-Jensen.

10. CONCLUSION

206. All of the statements made in this declaration of my own knowledge are true. All statements made based on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Dated: 2/16/2024 By: 
David B. Lett

CLAIM LISTING APPENDIX

U.S. Pat. No. 9,210,362

Designation	Claim Language
Claim 1	
[1A]	A wideband receiver system comprising:
[1B]	a mixer module configured to downconvert a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[1C]	a wideband analog-to-digital converter (ADC) module configured to digitize said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;
[1D]	digital circuitry configured to: select said plurality of desired television channels from said digitized plurality of frequencies; and output said selected plurality of television channels to a demodulator as a digital datastream.
Claim 2	
2	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a serial interface.
Claim 3	
3	The wideband receiver system of claim 1, wherein said output of said digital datastream is via a parallel interface.
Claim 4	
4	The wideband receiver system of claim 1, wherein said mixer module comprises a first mixer configured to generate an in-phase signal and a second mixer configured to generate a quadrature signal.
Claim 5	
5	The wideband receiver system of claim 1, wherein said wideband analog-to-digital converter comprises: a first ADC configured to generate a digital in-phase signal; and a second ADC configured to generate a digital quadrature signal.
Claim 6	
6	The wideband receiver system of claim 5, wherein said digital circuitry comprises a plurality of complex mixers configured to frequency shift said selected plurality of desired television channels.
Claim 7	

Designation	Claim Language
[7A]	The wideband receiver system of claim 6, wherein: prior to said frequency shift, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and
[7B]	after said frequency shift, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
Claim 8	
8	The wideband receiver system of claim 1, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selection of said plurality of desired television channels.
Claim 9	
9	The wideband receiver system of claim 8, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 10	
10	The wideband receiver system of claim 1, wherein said digital circuitry comprises a decimator circuit configured to decimate one or more of said selected plurality of television channels prior to said output of said selected plurality of desired television channels.
Claim 11	
[11A]	A method comprising: in a wideband receiver system:
[11B]	downconverting, by a mixer module of said wideband receiver system, a plurality of frequencies that comprises a plurality of desired television channels and a plurality of undesired television channels;
[11C]	digitizing, by a wideband analog-to-digital converter (ADC) module of said wideband receiver system, said plurality of frequencies comprising said plurality of desired television channels and said plurality of undesired television channels;
[11D]	selecting, by digital circuitry of said wideband receiver system, said plurality of desired television channels from said digitized plurality of frequencies; and
[11E]	outputting, by said digital circuitry of said wideband receiver system, said selected plurality of television channels to a demodulator as a digital datastream.
Claim 12	

Designation	Claim Language
12	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a serial interface.
Claim 13	
13	The method of claim 11, comprising outputting, by said digital circuitry of said wideband receiver system, said digital datastream via a parallel interface.
Claim 14	
14	The method of claim 11, comprising: generating, by a first mixer of said mixer module, an in-phase signal; and generating, by a second mixer of said mixer module, a quadrature signal.
Claim 15	
15	The method of claim 11, comprising: generating, via a first ADC of said wideband analog-to-digital converter, a digital in-phase signal; and generating, via a second ADC of said wideband analog-to-digital converter, a digital quadrature signal.
Claim 16	
16	The method of claim 15, comprising frequency shifting said selected plurality of desired television channels via a plurality of complex mixers of said digital circuitry.
Claim 17	
[17A]	The method of claim 16, wherein: prior to said frequency shifting, said selected plurality of desired television channels occupy non-contiguous portions of a frequency spectrum; and after said frequency shifting, said selected plurality of desired television channels occupy a contiguous frequency spectrum.
[17B]	
Claim 18	
18	The method of claim 11, wherein said digital circuitry comprises a plurality of channel filters configured to perform said selecting.
Claim 19	
19	The method of claim 18, wherein each one of said plurality of channel filters is a finite impulse response filter.
Claim 20	
20	The method of claim 11, comprising decimating, by said digital circuitry, one or more of said selected plurality of

Designation	Claim Language
	desired television channels prior to said outputting of said selected plurality of television channels.