

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner,

v.

ENTROPIC COMMUNICATIONS, LLC.,
Patent Owner.

Patent No. 11,381,866
Filing Date: January 28, 2022
Issue Date: July 5, 2022
Title: CABLE TELEVISION DEVICE

Inter Partes Review No.: IPR2024-00435

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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Ex. 1004:	Certified Prosecution History of the ’866 patent
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Ex. 1013:	U.S. Pub. No. 2003/0056221 (“Zhang”)
Ex. 1014:	U.S. Patent No. 7,237,214 (“Pandey”)
Ex. 1015:	Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)
Ex. 1016:	Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
Ex. 1017:	A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)
Ex. 1018:	S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
Ex. 1019:	U.S. Patent No. 6,061,406 (“Carson”)
Ex. 1020:	Reserved
Ex. 1021:	Data-Over-Cable Service Interface Specifications, DOCSIS 2.0, Radio Frequency Interface Specification, CM-SP-RFIV2.0-I11-060602

- Exs. 1022-1024: Reserved
- Ex. 1025: J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
- Ex. 1026: Reserved
- Ex. 1027: U.S. Patents and Patent Applications Family Tree for U.S. Pat. 11,381,866
- Exs. 1028-1032: Reserved
- Ex. 1033: Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2nd ed. 2004) (“Ciciora”)
- Ex. 1034: Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)
- Ex. 1035: U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
- Ex. 1036: U.S. Pub. No. 2003/0217362 (“Summers”)
- Ex. 1037: U.S. Pub. No. 2006/0256799 (“Eng”)
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- Ex. 1041: Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)
- Ex. 1042: U.S. Patent No. 7, 272, 375 (“Tuttle”)
- Ex. 1043: U.S. Patent No. 7,130,576 (“Gurantz”)
- Ex. 1044: U.S. Patent No. 5,278,837 (“Kelley”)

Ex. 1045:	Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)
Ex. 1046:	U.S. Patent No. 7,213,042 (“Cannon”)
Ex. 1047:	Reserved
Ex. 1048:	Excerpts of William Buchanan, “Computer Busses” (2000)
Ex. 1049:	U.S. Patent No. 7,079,528 (“Ziegler”)
Ex. 1050:	Excerpts of “Software Defined Radio: Enabling Technologies” (Walter H.W. Tuttlebee ed., 2003)
Ex. 1051:	U.S. Pub. No. 2005/0183015 (“Dunton”)
Ex. 1052:	U.S. Pub. No. 2003/0229900 (“Reisman”)
Exs. 1053-1056:	Reserved
Ex. 1057:	U.S. Pub. No. 2009/0113504 (“Jackson”)
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Ex. 1075:	U.S. Patent No. 6,791,995 (“Azenkot”)
Ex. 1076:	U.S. Patent No. 6,542,203 (“Shadwell”)

I. MANDATORY NOTICES

A. Real Parties in Interest (37 C.F.R. § 42.8(b)(1))

The real parties-in-interest for this petition are (i) Comcast Corporation, (ii) Comcast Cable Communications, LLC, and (iii) Comcast Cable Communications Management, LLC. No unnamed entity is funding, controlling, or directing this Petition for *inter partes* review (IPR) of U.S. Patent No. 11,381,866 (“the ’866 patent”), or otherwise has an opportunity to control or direct this Petition or Petitioner’s participation in any resulting IPR.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

Office Proceedings

This is the first of three petitions for *inter partes* review filed by Petitioner against the ’866 patent. Petitioner is also filing petitions for *inter partes* review against the related U.S. Patent Nos. 11,399,206 and 9,210,362.

No other Office proceedings (e.g., *inter partes* review, post-grant review, or covered business method) have been filed against the ’866 patent.

Litigation matters

The ’866 patent has been asserted in *Entropic Communications, LLC v. Comcast Corporation*, No. 2:23-cv-01050 (C.D. Cal. filed Feb. 10, 2023) and *Entropic Communications, LLC v. Cox Communications, Inc.*, No. 2-23-cv-01049 (C.D. Cal. filed Feb. 10, 2023) (collectively, “CA litigation”). These cases have been

consolidated and remain pending. The '866 patent was also asserted in *Entropic Communications, LLC v. Charter Communications, Inc.*, No. 2:22-cv-00052-JRG (E.D. Tex. filed April 27, 2022) (“TX litigation”), which case was dismissed on December 10, 2023.

Continuity

According to Office records, the '866 patent is a continuation of U.S. Pat. App. No. 17/217,244, filed March 30, 2021 (abandoned), which is a continuation of U.S. Pat. App. No. 16/430,506, filed June 4, 2019 (issued as U.S. Pat. No. 10,972,781), which is a continuation of U.S. Pat. App. No. 15/792,318, filed October 24, 2017 (issued as U.S. Pat. No. 10,313,733), which is a continuation of U.S. Pat. App. No. 14/948,881, filed November 23, 2015 (issued as U.S. Pat. No. 9,819,992), which is a continuation of U.S. Pat. App. No. 14/617,973, filed February 10, 2015 (issued as U.S. Pat. No. 9,210,363), which is a continuation of U.S. Pat. App. No. 13/962,871, filed August 8, 2013 (issued as U.S. Pat. No. 9,100,622), which is a continuation of U.S. Pat. App. No. 12/762,900, filed April 19, 2010 (issued as U.S. Pat. No. 8,526,898), which claims the benefit of U.S. Provisional App. No. 61/170,526, filed April 17, 2009. The '866 patent is part of a family that includes thirteen additional patents or applications that purport to claim priority, via a chain of continuation applications, from App. No. 12/762,900. A family tree is included as Ex. 1027.

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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II. INTRODUCTION

Comcast Cable Communications, LLC (“Petitioner”) petitions for *inter partes* review of claims 1-82 of U.S. Patent No. 11,381,866 (“the ’866 patent”).

III. SUMMARY OF ARGUMENT

The ’866 patent claims a cable television (TV) device including “wideband analog-to-digital converter (ADC)” for digitizing an input signal, which the ’866 patent admits “is similar to conventional tuners.” Ex. 1007, p. 5; Ex. 1001, 1:6-23. The alleged invention—digital circuitry for selecting from the input signal multiple desired channels and filtering out undesired channels—is disclosed and rendered obvious by the prior art, e.g., Zhang (Ex. 1013) and other references relied on herein. Accordingly, claims 1-82 of the ’866 patent are unpatentable and should be cancelled.

IV. OVERVIEW OF THE ’866 PATENT

A. Brief Description

The ’866 patent describes a wideband receiver system 200 “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1001, 1:26-29, 4:35-37. A receiver is “wideband” if it is “designed to concurrently receive several TV channels.” *Id.*, 1:35-38.

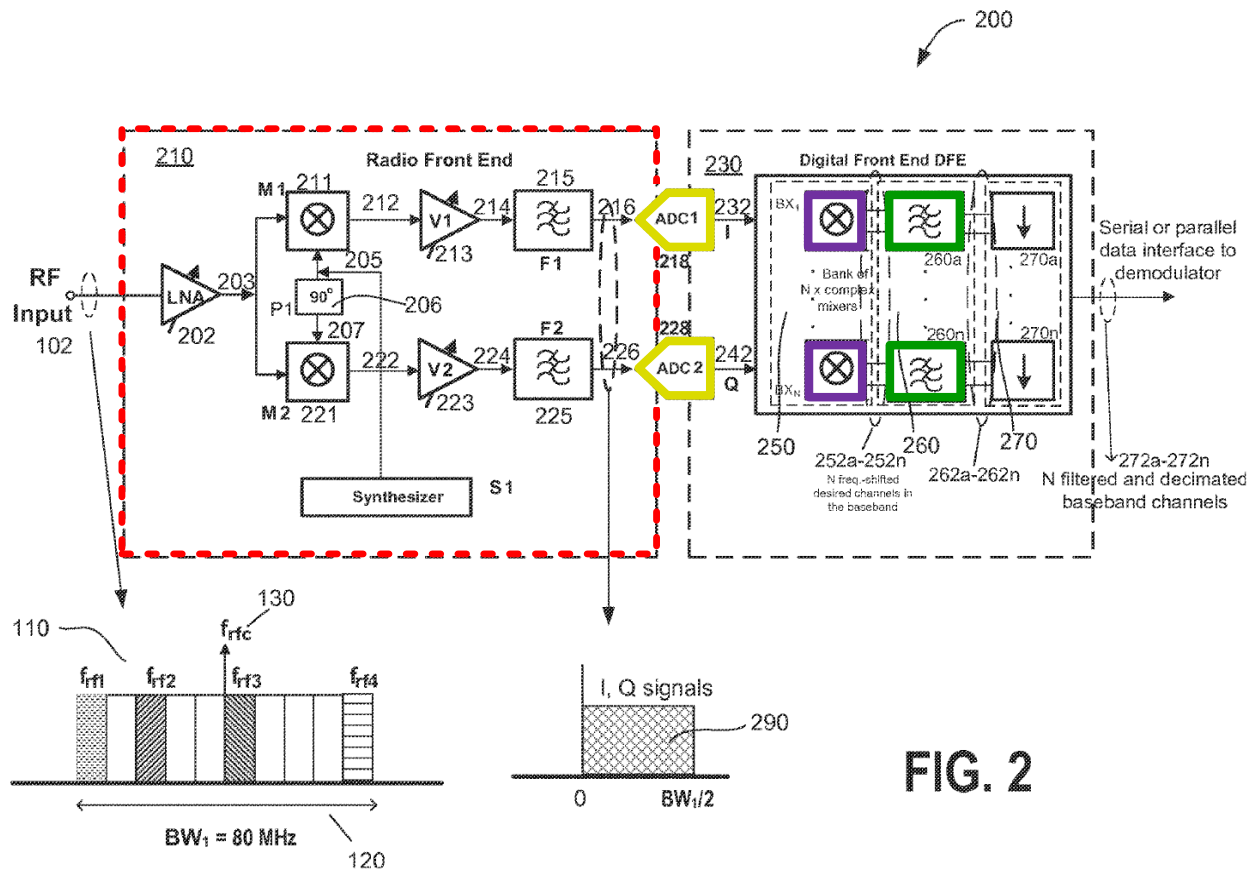


FIG. 2

Ex. 1001, Fig. 2 (annotated)

The system 200 receives television channels as frequencies dispersed within a bandwidth BW_1 . *Id.*, 4:38-50. The receiver includes a radio frontend 210 (**red**) that downconverts the bandwidth to an intermediate frequency as in-phase and quadrature signals 212 and 222, which are digitized by analog-to-digital converters ADC1/ADC2 (**gold**). *Id.*, 2:59-65, 4:61-24, 5:48-51. The '526 provisional application, incorporated by reference, admits that the left side of Figure 2 (up to and including ADC1/ADC2) “is similar to conventional tuners.” *Id.*, 1:6-22; Ex. 1007, p. 5.

The digital I and Q signals from ADC1/ADC2 are input to a bank of N complex mixers 250 (**purple**) in digital front end 230. Ex. 1001, 5:51-55. “Each of the N complex mixers ... extract[s] a different one of the desired channels” from the I and Q signals and “frequency-shifts the extracted signals to the baseband frequency.” *Id.*, 6:2-6. Filters 260a-260n (**green**) filter each baseband desired channel, which are then sent to a demodulator “using a serial or parallel data interface according to commonly known methods.” *Id.*, 6:6-8, 7:10-14.

B. Prosecution History

The application which became the '866 patent was filed on January 28, 2022, with a preliminary amendment cancelling claims 1-18 and adding claims 19-48. Ex. 1004, pp. 2-109. The Office rejected claims 19-27, 29-30, 33-42, 44-45, and 48 as obvious over U.S. Patent No. 6,760,342 (Skones et al.) in view of International Publication No. WO 02/087230 (Uskali et al.). *Id.*, pp. 119-132. Dependent claims 28 and 43 (providing channels “via a serial interface”), claims 31 and 46 (“DVR”), and claims 32 and 47 (“picture-in-picture display”) were deemed to contain allowable subject matter. *Id.*, p. 131.

Applicant received a Notice of Allowance after adding: the limitations of claim 28 to claim 19 (issued claim 1), the limitations of claim 43 to claim 34 (issued claim 14), new independent claim 49 (issued claim 27) based on original claims 19 and 31, new independent claim 63 (issued claim 41) based on original claims 34 and

46, new independent claim 77 (issued claim 55) based on original claims 19 and 32, new independent claim 91 (issued claim 69) based on original claims 34 and 47, and multiple sets of new dependent claims that paralleled existing dependent claims. *Id.*, pp. 148-175.

C. Earliest Priority Date for the Claims

The earliest possible priority date for the '866 patent claims is April 17, 2009. Ex. 1002, ¶ 45. Each of the references relied on herein is prior art to that date.

V. OVERVIEW OF PRIOR ART

A. Zhang

Zhang (Ex. 1013) published on March 20, 2003, and is prior art under pre-AIA 35 U.S.C. 102(b).

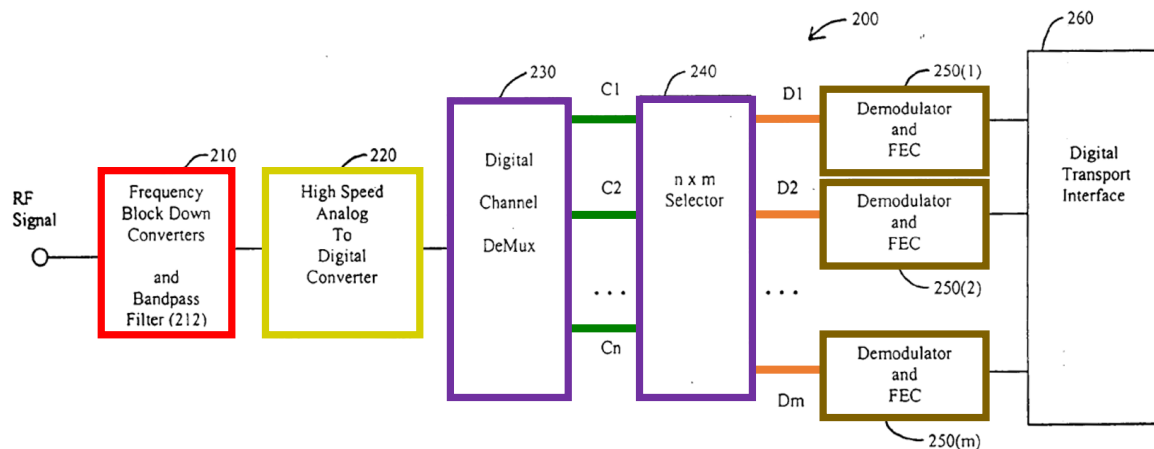


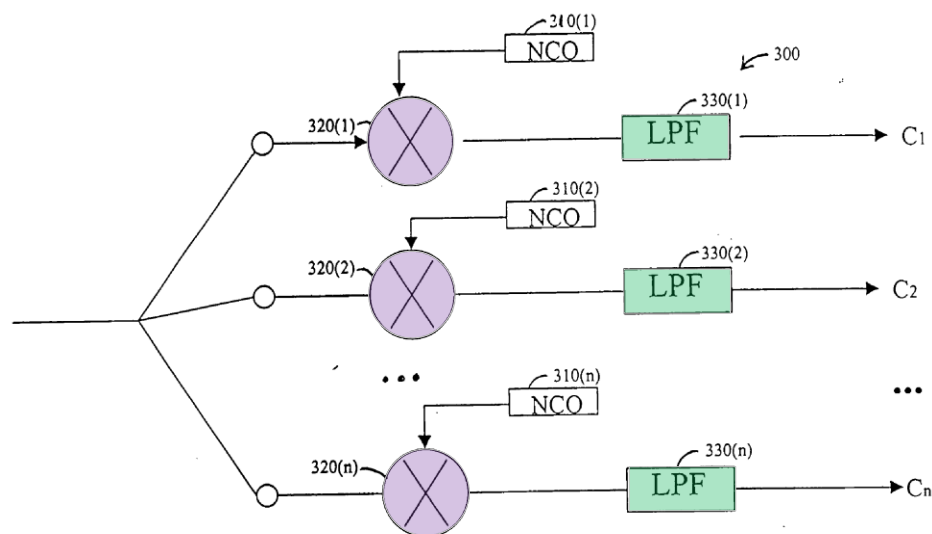
Fig. 2

Ex. 1013, Fig. 2 (annotated)

Zhang, which is analogous to the '866 patent, describes a multi-channel demodulator circuit 200 (illustrated above) useful as “advanced wide-band front-

ends for digital set-top boxes, PVRs” Ex. 1013, [0044]-[0045], Fig. 8; Ex. 1002, ¶ 77-80. Circuit 200 demodulates channels selected by a subscriber within a multi-channel Radio Frequency (RF) signal. Ex. 1013, [0011], [0024], [0028]-[0029], [0038]-[0040], [0042]. Circuit 200 comprises a frequency block down-converter 210 (**red**) that receives and shifts the analog RF signal to a lower frequency such that an ADC (**gold**) can digitize it. Ex. 1013, [0010], [0023], [0025], [0027], [0030]-[0037], [0041]-[0042].

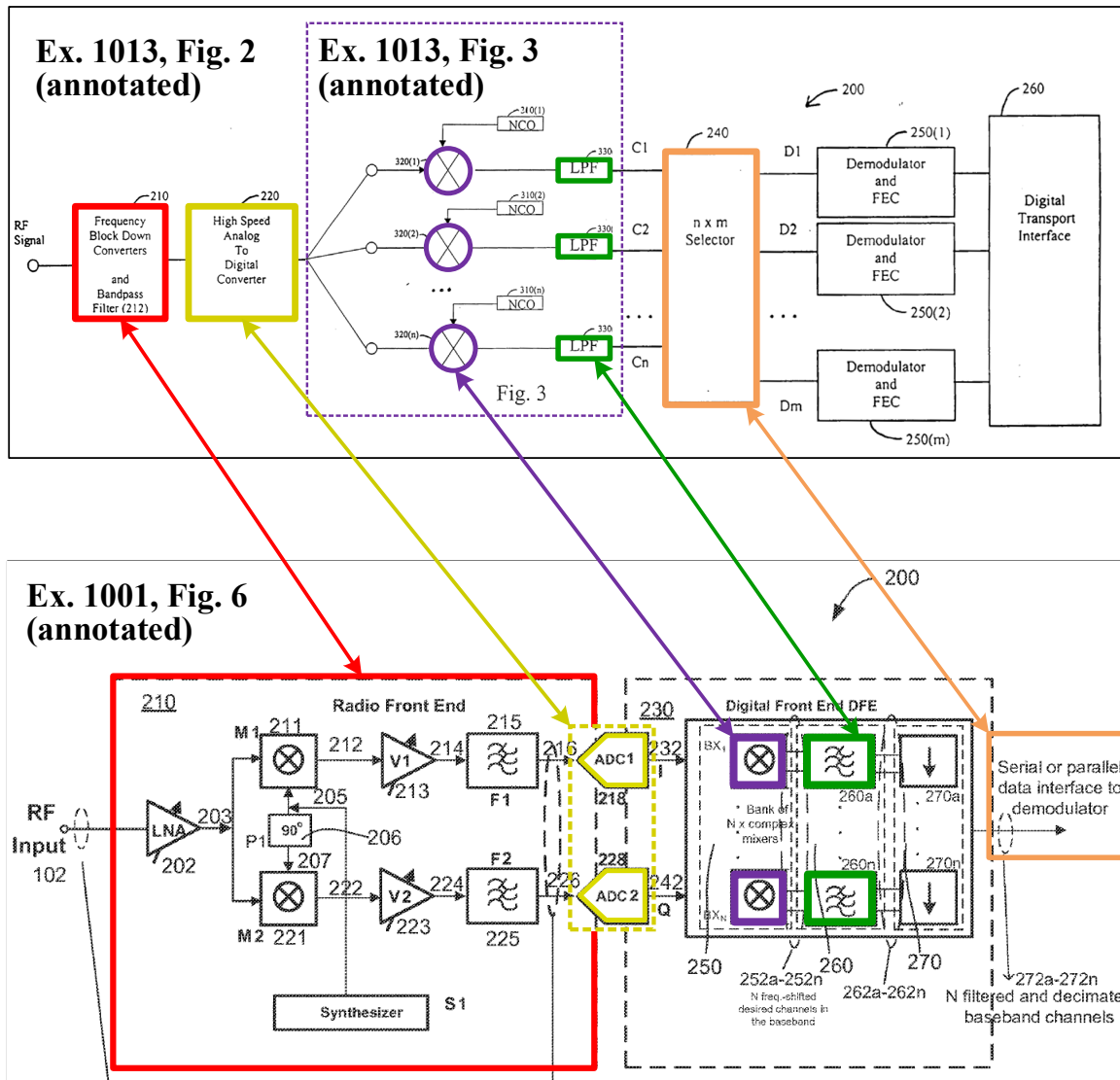
Like the '866 patent's complex mixer and filters that extract selected channels in parallel, Zhang's demultiplexer 230 (**purple**) separates channels (e.g., C_1 - C_n) within the digital RF signal, while digital selector 240 forwards any or all of the channels (e.g., D_1 - D_m) to one or more demodulators 250(1)-250(m) (**brown**) for recovery of audio and video content. Ex. 1013, [0007] [0010]-[0011], [0028]-[0029], [0042], [0047], claims 1, 4, 9, 31-32.



Ex. 1013, Fig. 3 (annotated)

As shown above, and like the '866 patent's DFE, Zhang's demultiplexer 230 includes a bank of numeric control oscillators (NCOs) 310(1)-310(n), complex multipliers 320(1)-320(n) (**purple**), and low-pass filters (LPFs) 330(1)-330(n) (**green**). Ex. 1013, [0030]; Ex. 1002, ¶ 79. Each complex multiplier multiplies the digital RF signal with a different frequency provided by a NCO to shift a target channel to baseband (0 Hz). Ex. 1013, [0032]. The low-pass filter then “filter[s] undesired RF channels and pass[es] only the target RF channel.” Ex. 1013, claim 37, [0032].

As shown below and discussed *infra*, Zhang discloses the same cable TV device as the '866 patent. This includes a “wideband analog-to-digital converter (ADC)” for digitizing a contiguous band of frequencies (**gold**) (Element [1B]), and a digital front end (DFE) for concurrently selecting a plurality of desired channels” (**purple/green**) (Element [1C]) and for providing a plurality of desired channels via a serial interface (**orange**) (Element [1C]).

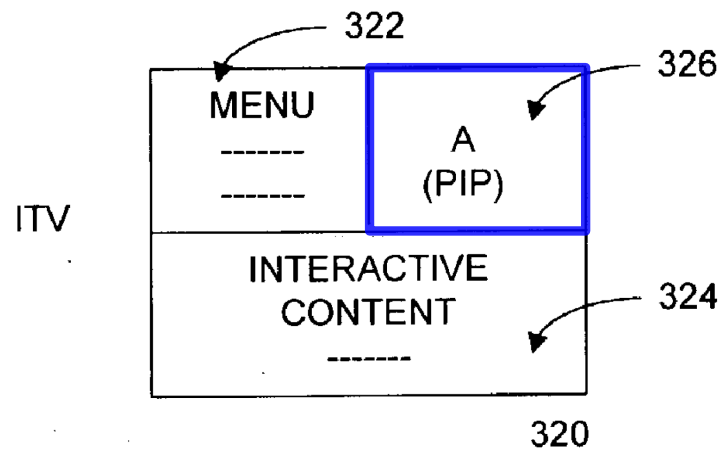


B. Reisman

Reisman (Ex. 1052) published on December 11, 2003, and thus, is prior art under pre-AIA 35 U.S.C. 102(b).

Reisman, which is analogous to the '866 patent, discloses TV systems that coordinate the viewing of traditional audiovisual content with hypermedia and interactive features. Ex. 1052, Abstract, Fig. 3, [0120]-[0121], [0125]; Ex. 1002, ¶¶

81-83. Reisman's systems include STBs with a digital video recorder (DVR) and "picture-in-picture display" capabilities, e.g., as shown below (**blue**). Ex. 1052, Fig. 3, [0005], [0043], [0048], [0060], [0073], [0118]-[0121], [0187], [0197], [0281]-[0285], [0291], [0296], [0534], [0537], [0546].



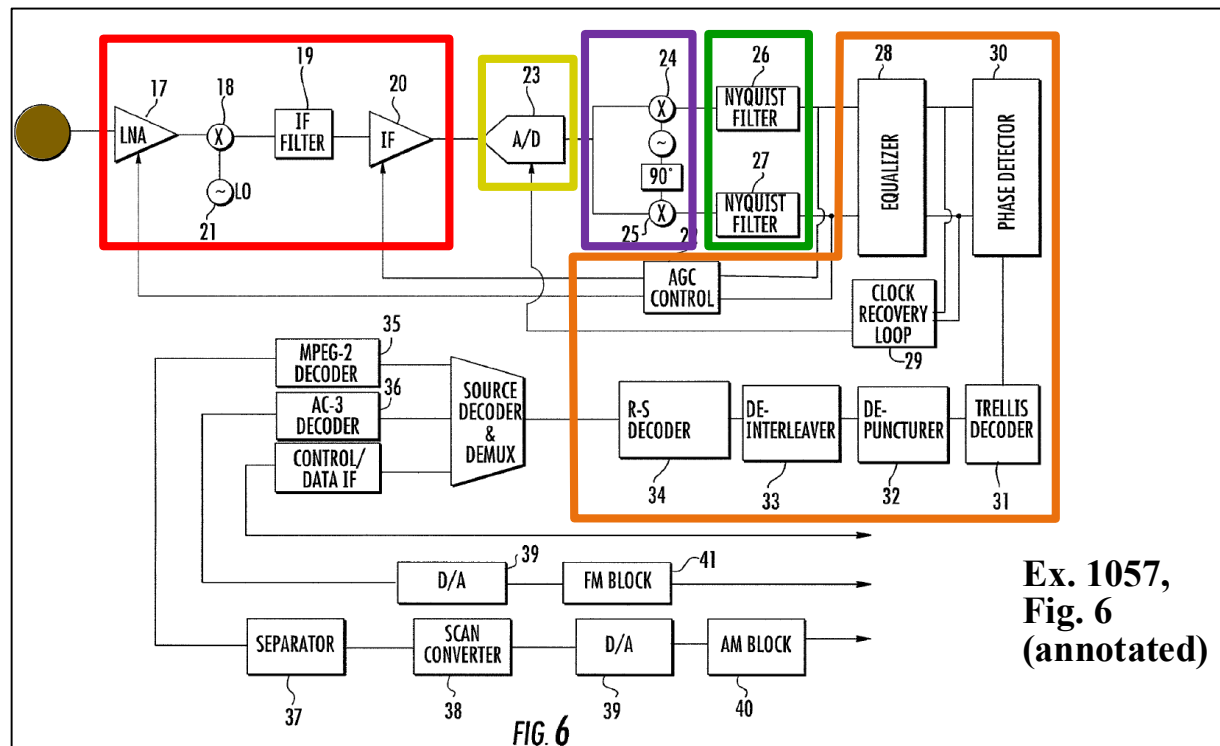
Ex. 1052, Fig. 3 (annotated)

C. Jackson

Jackson (Ex. 1057) was filed on October 26, 2007, and thus, is prior art under pre-AIA 35 U.S.C. 102(e).

Jackson discloses a receiver system (similar to that of the '866 patent) for demodulating digital cable (TV) channels, and is thus analogous to the '866 patent. Ex. 1057, [0001]-[0002]; Ex. 1002, ¶¶ 84-86. The system includes a cable network connector (**brown**), an RF tuner front end (**red**) with analog amplifiers and filters, an ADC (**gold**), a complex mixer (**purple**) that outputs in-band (I) and quadrature

components (Q), filters (**green**), and a demodulator (**orange**). Ex. 1057, Figs. 4b, 5-6, [0023]-[0027], claims 1, 8, 12.

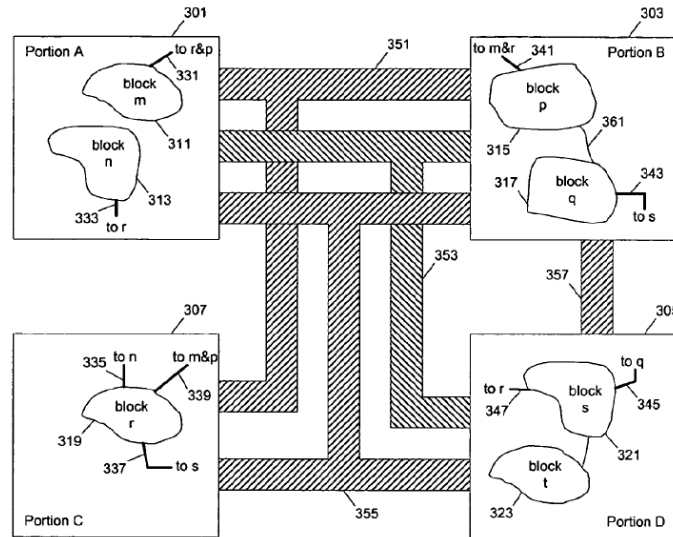


D. Pandey

Pandey (Ex. 1014) issued on June 26, 2007 and is prior art under pre-AIA 35 U.S.C. 102(b).

Pandey is cited for the common process of implementing serial and parallel interfaces (recited in claims 2 and 3) in an integrated circuit. Ex. 1014, Abstract, 1:15-55, 2:4-12; Ex. 1002, ¶¶ 87-90. The process partitions functional blocks in an integrated circuit chip (e.g., 301, 303, 305, 307 as illustrated below) and assigns

traces (e.g., 351, 353, 355, 357) to interconnect them. Ex. 1014, 1:56-60, 2:6-12, 2:64-3:27, 6:10-15, 11:6-19, 13:33-14:7.



Ex. 1014, Fig. 3

Pandey discloses layouts wherein signals are grouped and time-multiplexed through a serial interface between partitions, and others wherein signals have individual dedicated traces with no multiplexing, i.e., a parallel interface. *Id.*, 5:50-53, 6:11-15, 6:44-53, 7:13-19, 10:24-53, 10:58-11:5, 29:44-30:9, 30:31-42, 30:53-31:12, 31:20-22, 32:12-15.

VI. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(B)

A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based

Petitioner requests review of claims 1–82 under the following grounds.

Ground	References	Basis	Claims Challenged
A	Zhang	§102	1, 3-7, 9, 11, 13, 14, 16-20, 22, 24, 26, 27, 29-33, 35-37, 40, 41, 43-47, 49-51, 54
B	Zhang	§103	1, 3-7, 9, 11, 13, 14, 16-20, 22, 24, 26, 27, 29-33, 35-37, 40, 41, 43-47, 49-51, 54
C	Zhang-Reisman	§103	9-12, 22-25, 27, 29-33, 35-40, 41, 43-47, 49-54, 55, 57-61, 63-68, 69, 71-75, 77-82
D	Zhang-Jackson	§103	2-6, 15-19, 28-32, 42-46
E	Zhang-Reisman-Jackson	§103	28-32, 42-46, 56-60, 70-74
F	Zhang-Pandey	§103	1, 3-9, 11, 13, 14, 16-22, 24, 26, 34-36, 48-50

G	Zhang-Reisman-Pandey	§103	9-12, 22-25, 34-36, 48-50, 62-64, 76-78
H	Zhang-Pandey-Jackson	§103	2-6, 15-19

None of this prior art was cited during prosecution. Ex. 1001, cover, ¶¶ 42-44.

A declaration of David B. Lett in support of this petition includes, e.g., a discussion of Mr. Lett’s background, the ’866 patent, and the prior art, as well as his opinions and the bases therefor. Ex. 1002, ¶¶ 1-265. Mr. Lett at least meets the level of skill of a POSITA. *Id.* ¶¶ 4-16, 31; Ex. 1003.

B. Summary of the Grounds and Comparison of Claim Limitations

The ’866 patent includes independent claims 1, 14, 27, 41, 55, and 69. All are directed to a cable television (TV) device as illustrated in Figure 2 of the ’866 patent.

Independent claims 1, 27, and 55 recite “a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal ...” and “a digital front end (DFE) ... configured to concurrently select and provide each of the plurality of desired channels [] without providing any of the plurality of undesired channels.” Claims 1, 27, and 55 differ only by inclusion of a

single, well-known ancillary feature: “a serial interface” (claim 1), a “DVR” (claim 27), or “a picture-in-picture” display (claim 55).¹

Independent claims 14, 41, and 69 are nearly identical to claims 1, 27, and 55, respectively, except they lack a “contiguous band of frequencies” and replace the “digital front end” (DFE) with “a plurality of digital down converters.” The DFE and the “plurality of digital down converters” refer to the same structure illustrated as element 230 in Figure 2 of the ’866 patent.

Zhang discloses every feature of claims 1, 14, 27, and 41, and thus anticipates these claims (ground A), and to the extent Patent Owner argues otherwise, renders them obvious (ground B). Zhang discloses every feature of claims 55 and 69, except “picture-in-picture.” For this feature, Reisman is combined with Zhang (ground C). Other features, such as “DVR” in claims 27 and 41, are taught by both Zhang and Reisman, and thus grounds A, B, and C apply. Ex. 1002, ¶¶ 91-95.

Additional grounds add Jackson (D/E) for teaching certain analog components of a receiver, and Pandey (F/G) for teaching serial/parallel interfaces. Grounds D and F omit Reisman for claims that depend from claims 1, 14, 27, and 41 and those that do not include “picture-in-picture,” and grounds E and G include

¹ A summary of features cross referenced to claims and prior art is provided by Petitioner’s expert in Ex. 1002, ¶ 98.

Reisman for claims that depend from claims 27, 41, 55 and 69 or that otherwise include “DVR” or “picture-in-picture.” Ex. 1002, ¶¶ 96-97.

Ground H adds Pandey to ground D (Zhang-Jackson). Grounds F/G, and H are applied as additional grounds in which Pandey supplements Zhang for teaching serial/parallel interfaces.

C. 314(a) Discretion Does Not Apply

The *Fintiv* factors as set forth in the Director’s June 21, 2022, Guidance Memorandum do not warrant discretionary denial.

Factor one appears neutral. Petitioner has filed IPR petitions challenging all eight patents asserted in the District Court in case no. 2:23-cv-01050. If trial is instituted, and the case is not dismissed based on Petitioner’s motion to dismiss the Second Amended Complaint, then Petitioner expects to request a stay, as decisions in Petitioner’s favor would resolve the dispute in its entirety.

Factor two favors institution. Petitioner has filed a motion to dismiss the District Court case, Patent Owner has filed an Amended Complaint, and Petitioner will renew its Motion to Dismiss in order to seek dismissal of the operative complaint. In addition, no schedule beyond claim construction has been entered, and the Court has not set a trial date.

Factor three favors institution. To date, the investment by the District Court has been limited to considering motions to dismiss on the pleadings.

Factor four strongly favors institution. The petition challenges all claims in the '866 patent while only claims 27, 28, 33, 36, 37, 41, 42, 47, 50, and 51 are asserted in the District Court.

Factor five does not warrant denial as Petitioner is a defendant in the District Court case.

Factor six favors institution. Petitioner presents compelling unpatentability challenges that merit institution, relying on different prior art than was considered during prosecution.

D. 325(d) Discretion Does Not Apply

Considering the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, No. IPR2019-01469, Paper 6 at 8-9 (PTAB Feb. 13, 2020), the Board should not deny institution. The grounds raised herein are not the same or substantially the same as the art and arguments raised during prosecution, and to the extent that they are, the Examiner erred in a manner material to the patentability of the challenged claims by failing to find and consider all of the relevant prior art, including Zhang.

E. Level of Ordinary Skill

A person of ordinary skill in the art (a “POSITA”) at the time of the alleged invention would have had a degree in electrical engineering, or a similar discipline,

along with three-to-four years of experience with digital signal processing and RF tuning systems for satellite and/or cable communications. Ex. 1002, ¶¶ 30-32. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. *Id.*

F. Claim Construction

All claim terms herein should be given their ordinary and customary meaning to a POSITA as they would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b). Ex. 1002, ¶¶ 33-34.

1. “Wideband”

Consistent with its ordinary meaning, the ’866 patent defines “wideband” as a band that carries multiple channels. For example, the ’866 patent states that a receiver is “wideband” if it is “designed to concurrently receive several TV channels.”² Ex. 1001, 1:36-39; Ex. 1002, ¶ 35.

² The ’866 patent also states: “the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum.” Ex. 1001, 1:28-33. This does not change the ordinary meaning above for “wideband,” and in any

2. “Digital Down Converter”/ “Digital Front End”

Independent claims 14, 41, and 69 recite “digital down converter[s]” “operable to generate a digital channel output corresponding to each desired channel.” A digital down converter, as the term states, is digital circuitry that downconverts a digital signal. Ex. 1002, ¶ 36. The ’866 patent omits the term “digital down converter,” but describes a “Digital Front End (DFE)” that downconverts digital signals. Ex. 1002, ¶ 36.

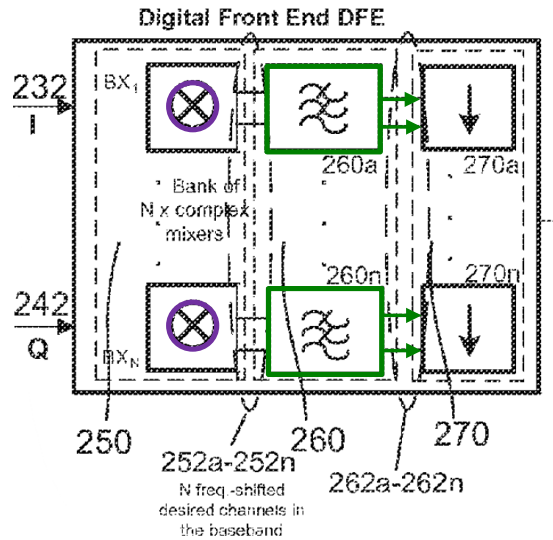
Independent claims 1, 27 and 25 use the term DFE that, similar to the digital downconverters of claims 14, 41, and 69, is “configured to concurrently select and provide each of the plurality of desired channels,” but with the further limitation “without providing any of the plurality of undesired channels.” *Id.*

The example DFE from Figure 2 (below) includes a plurality of signal paths, with each path including a complex mixer 250 (purple), a low pass filter 260 (green), and optionally a demodulator with a serial or parallel interface to the

event the claims recite only a “wideband analog-to-digital converter,” not a “wideband receiver system.”

demodulator.³ Ex. 1001, 5:51-7:9, 9:50-60, Figs. 2-3; Ex. 1002, ¶ 37. Each path performs the function that claims 14, 41, and 69 ascribe to a digital down converter—generating a digital channel output corresponding to a desired channel. Ex. 1001, 5:51-7:9, 9:50-60, Figs. 2-3; Ex. 1002, ¶ 37. That this structure is the digital down converter in the '866 patent is consistent with the dependent claims, which further require that the digital down converter(s) have, e.g., a digital mixer, filter, demodulator, and a serial or parallel interface. Ex. 1001, claims 16, 18-21, 40, 43-50, 68, and 71-76. The complex mixer in each path performs “down-converting,” which the '866 patent describes as shifting of the frequency of a signal to a lower frequency (also termed “down shift” and “frequency shift”). Ex. 1001, 1:38-40, 2:2-3:2, 4:60-66; 6:3-56, 7:47-55, 9:17-26; Ex. 1002, ¶ 37.

³ The '866 patent alternatively refers to the boxes following the filters in Figures 2 and 3 as decimators and/or demodulators, and also discloses the DFE as having outputs to a demodulator. Ex. 1001, 6:8-14, 7:4-9, 9:50-60, Figs. 2-3.



Ex. 1001, Fig. 2 (annotated and excerpted)

Neither “digital down converter” nor “digital front end” is a means-plus-function term. But in the event that either term is so construed, the corresponding structure for “digital down converter” includes the components in one signal path in the DFE, i.e., a complex mixer 250 and a filter 260, and the corresponding structure for a “digital front end” include two such signal paths. Ex. 1001, 5:51-7:9, 9:50-60, Figs. 2-3; Ex. 1002, ¶ 38.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground A/B: Zhang

Zhang anticipates (ground A) and renders obvious (ground B) claims 1, 3-7, 9, 11, 13-14, 16-20, 22, 24, 26-27, 29-33, 35-37, 40-41, 43-47, 49-51, and 54.

1. Independent Claim 1

a. [1A] “A cable television (TV) device comprising:”

While the preamble [1A] is not limiting,⁴ Zhang discloses it. Zhang describes an RF receiver, for example in a STB, receiving digital video channels over a cable system and having a DOCSIS return channel, which the '866 patent concedes is a protocol for “cable networks that carry TV programs.” Ex. 1013, Fig. 2, [0005]-[0006], [0023]-[0025], [0029], [0041], [0045]-[0047], claims 13, 27, 30, 33; Ex. 1001, 9:4:8; Ex. 1021 pp. 1-3; Ex. 1002, ¶ 101-102. Thus, Zhang’s receiver teaches Element [1A].

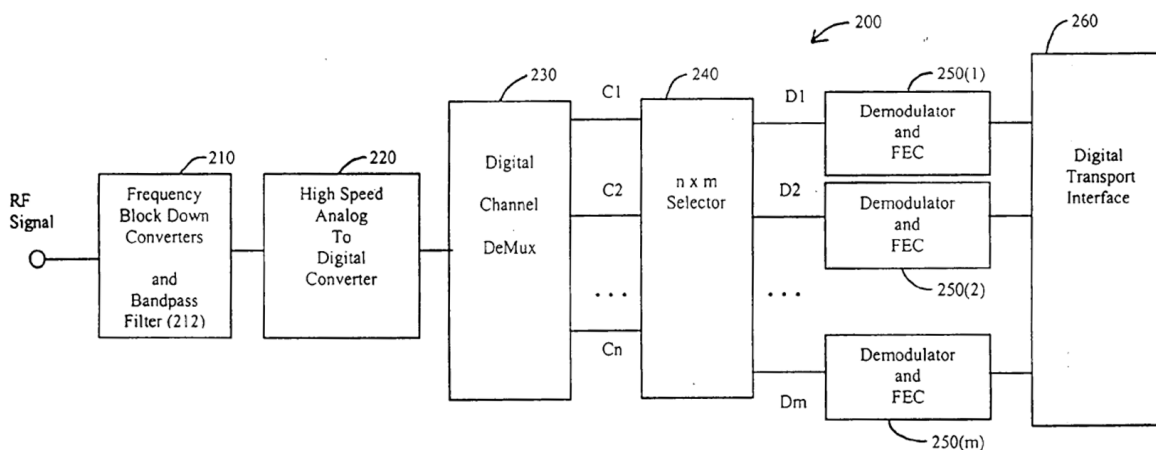


Fig. 2

Ex. 1013, Fig. 2

⁴ The limitations of the claims appear and are labeled in the Claims Listing Appendix.

b. [1B] “a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and”

Zhang discloses the claimed “wideband analog-to-digital converter” as ADC 220 (gold), which digitizes a multi-channel analog RF signal received from Frequency Block Downconverter 210 (red). Ex. 1013, Abstract, [0010], [0025], [0027], [0031], [0034], [0044]-[0045], Figs. 2, 6-8, claims 1, 8; Ex. 1002, ¶¶ 103-104.

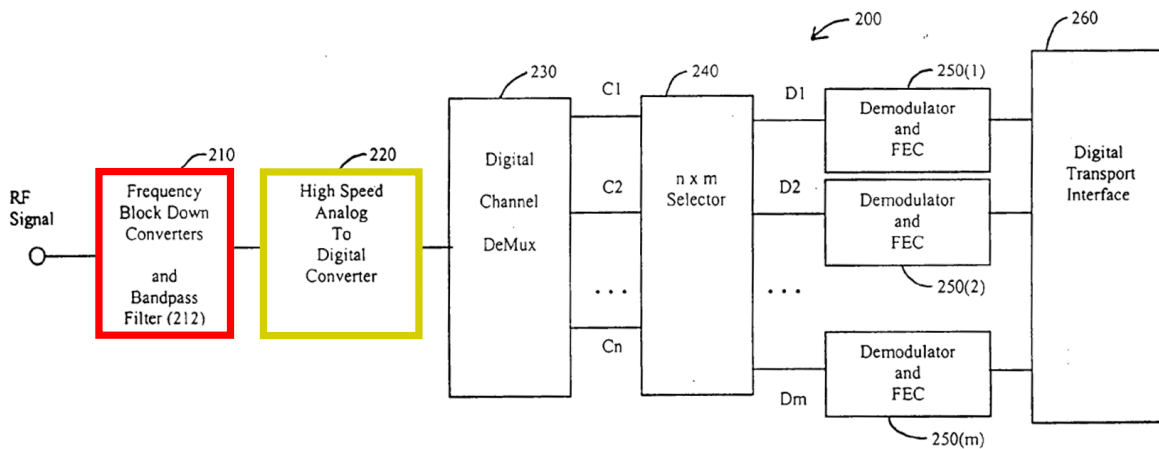


Fig. 2

Ex. 1013, Fig. 2 (annotated)

Zhang’s ADC is wideband because the digitized multi-channel RF signal includes several channels, and the channels form a contiguous band of frequencies because (like the ’866 patent) they are spaced next to each other within a frequency band with a precise frequency spacing (e.g., 6 MHz) that is a fraction of the multi-channel RF signal bandwidth (e.g., 540-750 MHz divided into 35 channels). Compare Ex. 1013, [0006], [0010], [0024]-[0025], [0027] (converting “an entire

signal band”), [0041]-[0042], [0047] (receiving “an entire 500 MHz band”) *with* Ex. 1001, 1:24-27 (“tuners designed to concurrently receive several TV channels are referred to as wideband tuners”), 2:50-59 (contiguous channels are “close to each other (e.g. as a fraction of the total system bandwidth)”) Ex. 1002, ¶ 105. Zhang further discloses that in alternate variations, “RF channels need not be contiguous,” teaching that in the embodiments otherwise described, the RF channels are contiguous. Ex. 1013, [0048]; Ex. 1002, ¶ 105.

The digitized multi-channel RF signal includes target RF channels that are selected and demodulated in subsequent stages (claimed “desired channels”), and undesired RF channels that are filtered out (claimed “undesired channels”). Ex. 1013, [0005], [0010]-[0012], [0027]-[0029], [0031]-[0032], [0035]-[0036], [0041]-[0042], claims 1, 2, 4, 8, 21, 28, 34, 37; Ex. 1002, ¶¶ 106-107.

Thus, Zhang teaches Element [1B].

- c. [1C] “a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels, via a serial interface, without providing any of the plurality of undesired channels.”**

Zhang teaches the claimed “digital frontend (DFE)” as Digital Channel Demultiplexer 230 and a portion of Digital Selector 240 (purple) (as detailed in Figure 5), which are coupled to ADC 220. Ex. 1013, [0028]; Ex. 1002, ¶¶ 108-109.

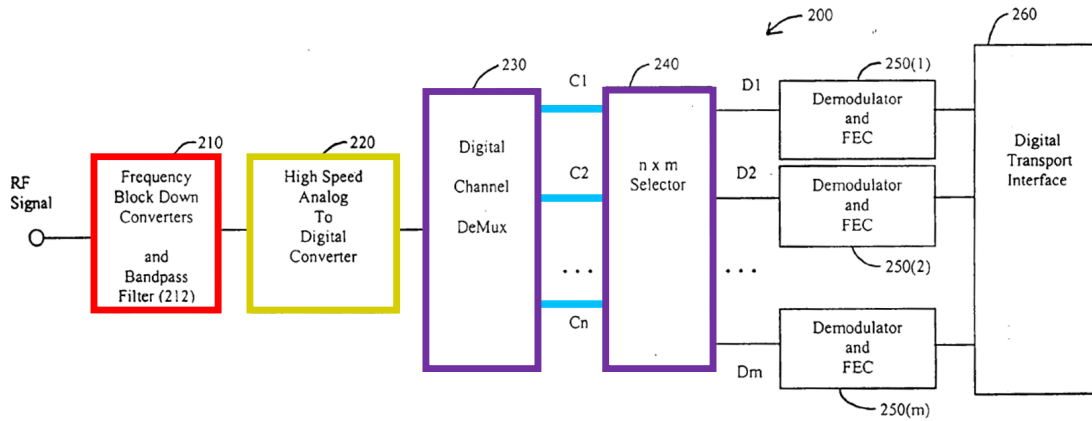


Fig. 2

Ex. 1013, Fig. 2 (annotated)

Digital tuner 300 (an embodiment of demultiplexer 230) (below left) has the same structure as the '866 patent's digital front end 230 (below right), including multiple signal paths for concurrently selecting and providing a plurality of desired channels C_1 - C_n (light blue). Compare Ex. 1013, Fig. 3 (filters 330), [0030]-[0034], claims 34, 36-37 with Ex. 1001, Fig. 2 (filters 260), 6:3-8; Ex. 1002, ¶ 110. Like the '866 patent's DFE, each path includes a complex multiplier 320 (purple) followed by a low pass filter (LPF) 330 (green).

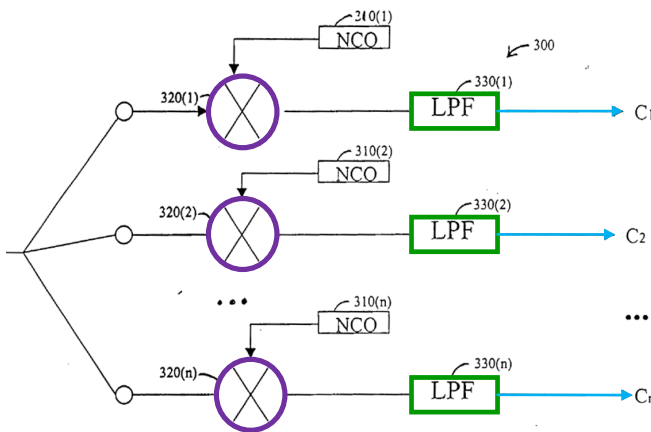
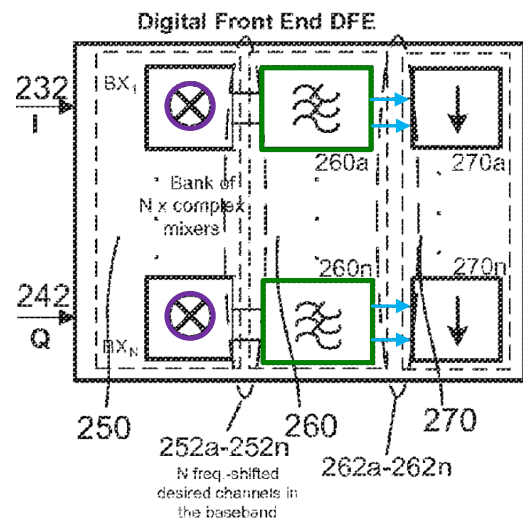


Fig. 3

Ex. 1013, Fig. 3 (annotated)



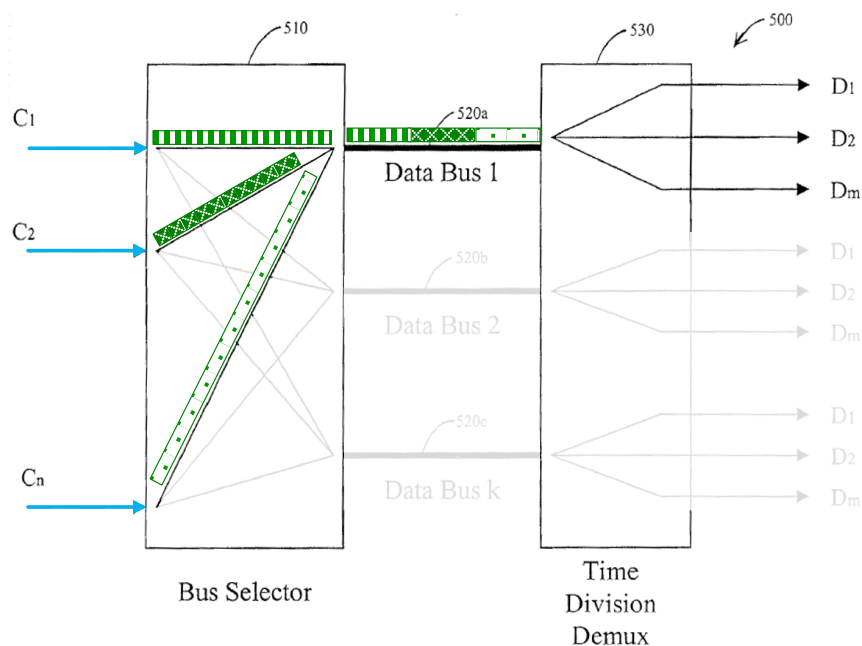
Ex. 1001, Fig. 2 (annotated)

Each path receives the multi-channel digital RF signal from ADC 220 and operates concurrently to select one respective desired channel. Ex. 1013, [0031]; Ex. 1002, ¶ 111. In each path, complex multiplier 320 first downconverts (shifts) the multi-channel RF signal frequency so that a different “target channel” within the signal is centered at baseband (0 Hz), and then low pass filter 330 filters out undesired channels, so that one of the “n” target digital channels C_1 - C_n (light blue) is output. Ex. 1013, [0028], [0031]-[0032] claims 34, 36-37; *see also* [0034]-[0037]; Ex. 1002, ¶ 111. Next, selector 240 provides “m” channels D_1 - D_m selected from any or all of channels C_1 - C_n (light blue) for demodulation by one or more demodulators. Ex. 1013, Figs. 2-3, [0005], [0028], [0038]-[0039], [0047], claims 2-4, 30, 32; Ex. 1002, ¶ 111.

Demultiplexer 230 and selector 240 output only user selected channels (either all or a subset of the user selected “C” channels) and filter out all other channels from the digitized multi-channel RF signal. Ex. 1013, [0028], [0032], [0039], [0047], claims 2, 30, 32; Ex. 1002, ¶ 112. Zhang thus discloses a DFE “configured to concurrently select and provide each of the plurality of desired channels ... without providing any of the plurality of undesired channels” as recited in Element [1C].

Selector 240 further provides the desired channels “via a serial interface” as recited in Element [1C]. Selector 240, implemented as illustrated in Figure 5, includes a bus selector 510 and one or more multiple data buses 520. Ex. 1013,

[0038]-[0039], Fig. 5; Ex. 1002, ¶ 113. Selector 240 with “one” bus (e.g., Data bus 1) receives channels C_1 - C_n from demultiplexer 230 (represented by green blocks with different patterns) and sends them across the bus “with the use of time division multiplexing.” *Id.*; Ex. 1016, pp. 79-80, Figs. 6-25; Ex. 1002, ¶ 113.



Ex. 1013, Fig. 5 (annotated)

A POSITA would have understood that this sends different channels sequentially (serially) in different time divisions over a single data path as shown, and that such a path is a “serial interface” as claimed in Element [1C]. Ex. 1013, [0038]-[0039]; Ex. 1002, ¶¶ 74-76, 114; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, p. 8; Ex. 1016, pp. 79-80; Ex. 1017, 354-355; Ex. 1034, pp. 23, 183; Ex. 1048, p. 16; Ex. 1049, 1:10-40. For example, as explained in the textbook “Digital Integrated Circuits: A Design Perspective” published in 1996 (“Rabaey”), digital circuits (like Zhang’s implemented in CMOS) represent data as binary units (“bits”) in the form

of electrical signals (e.g., high and low voltages for binary values “1” and “0” respectively). Ex. 1002, ¶ 115; Ex. 1016, pp. 31-34, *see also* 23, 49-51, 79-80. To output multiple bits (e.g., from multiple channels), the circuit can either transmit the bits over multiple separate wires, one wire for each bit, which was known as a “parallel interface,” or transmit the bits one at a time sequentially over a single wire, which was known as a “serial interface.” Ex. 1016, pp. 79-80 (Fig. 6-25); Ex. 1002, ¶¶ 74-76, 115.

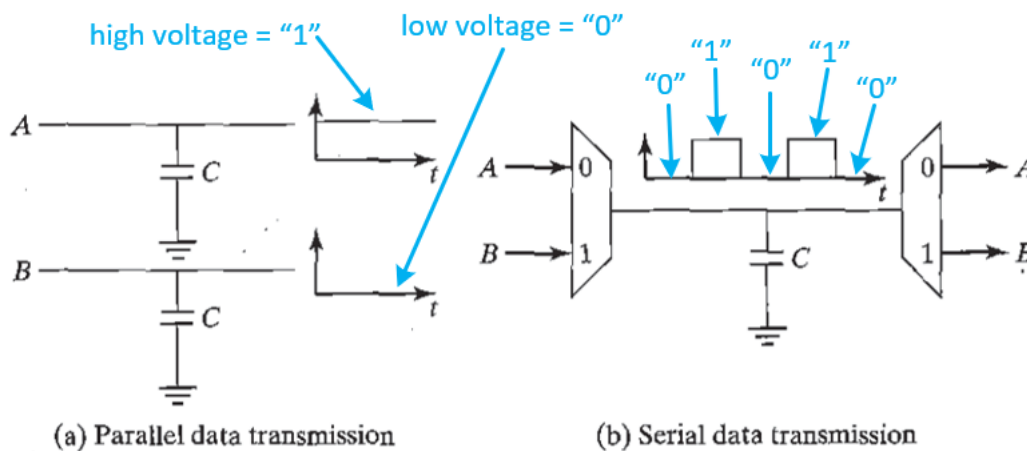


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1016, p. 80 (Fig. 6-25) (annotated)

As shown in Zhang’s annotated Figure 5 above, Zhang discloses embodiments with a serial interface. Ex. 1002, ¶ 116.

Zhang thus discloses element [1C].

To the extent Zhang does not disclose a serial interface, implementing Zhang’s circuitry to output the selected channels via a serial interface was obvious in light of the POSITA’s general knowledge, creativity, and common sense as one

of two common design choices that were well-known in integrated circuits at the time. Ex. 1002, ¶ 117; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, pp. 4-6; Ex. 1016, pp. 79-80; Ex. 1017, pp. 354-355. As the '866 patent concedes, outputting a digital data stream via serial interface was “commonly known,” i.e., Applicant Admitted Prior Art (AAPA). Ex. 1001, 7:10-14; Ex. 1002, ¶ 117.

Further, Zhang’s circuit is implemented in CMOS, which (as discussed in Rabaey), can either transmit the bits via parallel interface or via serial interface. Ex. 1016, pp. 79-80 (Fig. 6.25); Ex. 1002, 74-76, 118. A POSITA implementing the Zhang circuit in CMOS would have been aware of and fully able to implement a serial interface and/or a parallel interface, both being obvious to try as typical, predictable choices. Ex 1002, ¶¶ 118-119. Likewise, implementing a serial interface was well within the POSITA’s skillset, leading to a high expectation of success. *Id.*

Zhang alone, in view of the knowledge of a POSITA (as acknowledged in the '866 patent) thus also renders obvious Element [1C].

To the extent “DFE” is a means-plus-function limitation, Zhang discloses the same or equivalent structure as in the '866 patent (e.g., multiple paths, each including a complex and filter as shown in Figures 2 and 3 of Zhang and Figure 2 of the '866 patent), with any differences being insubstantial. Ex. 1013, Abstract, [0010], [0025], [0027], [0031], [0034], [0044]-[0045], Figs. 2, 3; Ex. 1001, Figs. 2-3, 5:51-7:9, 9:50-60. Ex. 1002, ¶ 120. In Zhang and the '866 patent, each path performs the same

function of selecting a respective desired channel, in the same way by first downconverting the respective desired channel to baseband and then low pass filtering with a filter to isolate the channel, to achieve the same result of generating a digital channel output corresponding to a respective desired channel. *Id.*

2. Independent Claim 14

Zhang anticipates and renders obvious Claim 14. Ex. 1002, ¶¶ 121-137.

a. [14A]-[14B]

Elements [14A]-[14B] are identical to Elements [1A]-[1B], except Element [14B] lacks “a contiguous band of frequencies.” Ex. 1002, ¶¶ 121-124. Zhang thus discloses and renders obvious Elements [14A]-[14B] for the same reasons discussed above for Elements [1A]-[1B]. *See* Sections VII.A.1.a-b.

b. [14C] “a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and”

As discussed above (Sections VI.F.2, VII.A.1.c), a POSITA would have understood “a plurality of digital down converters” to be included in the DFE digital circuit illustrated in Figure 2, which as described above, is the same circuit that Element [1C] is directed to. Ex. 1002, ¶¶ 36-38, 108-112. Zhang thus discloses the

digital downconverters of Element [14C] for the same reasons it discloses the DFE of Element[1C]. *See* Section VII.A.1.c; Ex. 1002, ¶ 125.

Specifically, Zhang’s demultiplexer 230 (below left) has the same structure as the ’866 patent’s digital front end 230 (below right), including a plurality of signal paths, each with a complex multiplier 320 (**purple**) and filter 330 (**green**) that are coupled to ADC 220 (claimed “wideband ADC”) and operable to generate “target” channels C_1 - C_n (**light blue**) selected by the subscriber (claimed “desired channels”). *Compare* Ex. 1013, Fig. 3 (320, 330), [0012], [0028], [0030]-[0032], claims 10-11, 21, 34-37 *with* Ex. 1001, Fig. 2 (250, 260), 2:65-3:2, 6:3-12, 6:50-63, 7:47-55; Ex. 1002, ¶ 126. Each path in Zhang is one of a “plurality of digital down converters ... operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels” as recited in Element [14C]. Ex. 1002, ¶¶ 126-127.

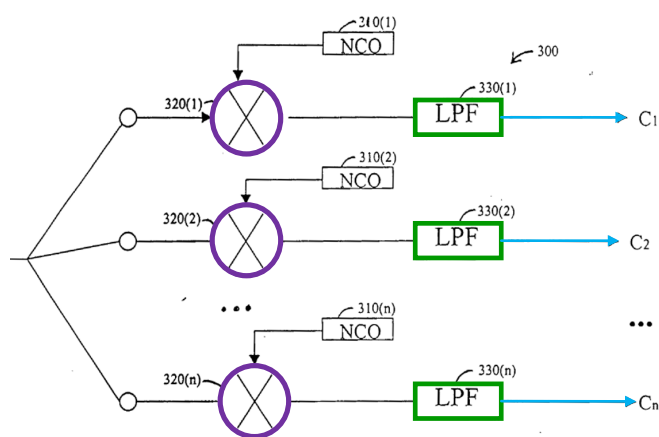
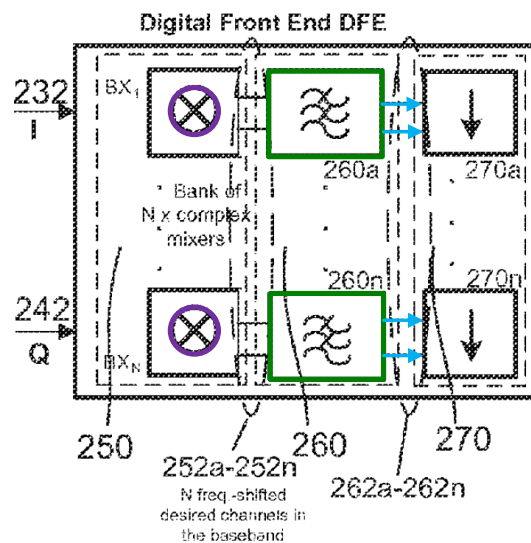


Fig. 3

Ex. 1013, Fig. 3 (annotated)



Ex. 1001, Fig. 2 (annotated)

To the extent “digital down converter” is construed to be a means-plus-function term, Zhang’s demultiplexer 230 includes the same or equivalent structure as disclosed in the ’866 patent (e.g., multiple parallel paths, each including a complex mixer followed by a low pass filter as shown in Figures 2 and 3 of Zhang and Figure 2 of the ’866 patent), with any differences being insubstantial. Ex. 1002, ¶ 128. In both Zhang and the ’866 patent, each path performs the same function of selecting a respective desired channel, in the same way by first downconverting the respective desired channel to baseband and then filtering with a filter to isolate the channel, to achieve the same result of generating a digital channel output corresponding to a respective desired channel. *Id.*

c. [14D] “wherein the plurality of digital down converters is operable to provide each digital channel output via a serial interface.”

As shown below, Zhang’s demultiplexer 230 (the claimed “plurality of digital down converters”) provides channels C_1 - C_n (light blue) (which include each claimed “digital channel output”) via a selector 240 as channels D_1 - D_m to one or more demodulators 250. Ex. 1013, [0005], [0028], [0038]-[0039], [0047], claims 2-4, 30; Ex. 1002, ¶¶ 129-130. Embodiments of selector 240 use a serial interface.

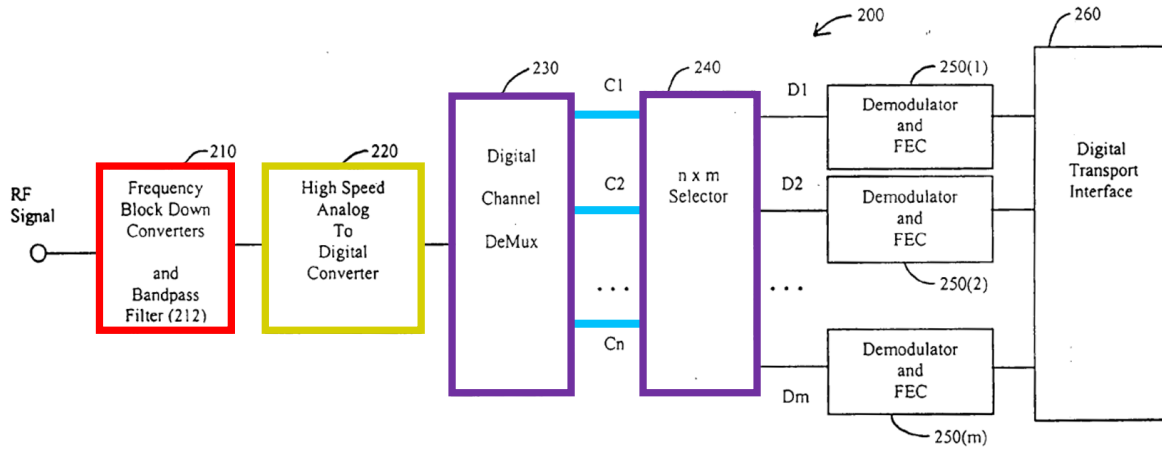
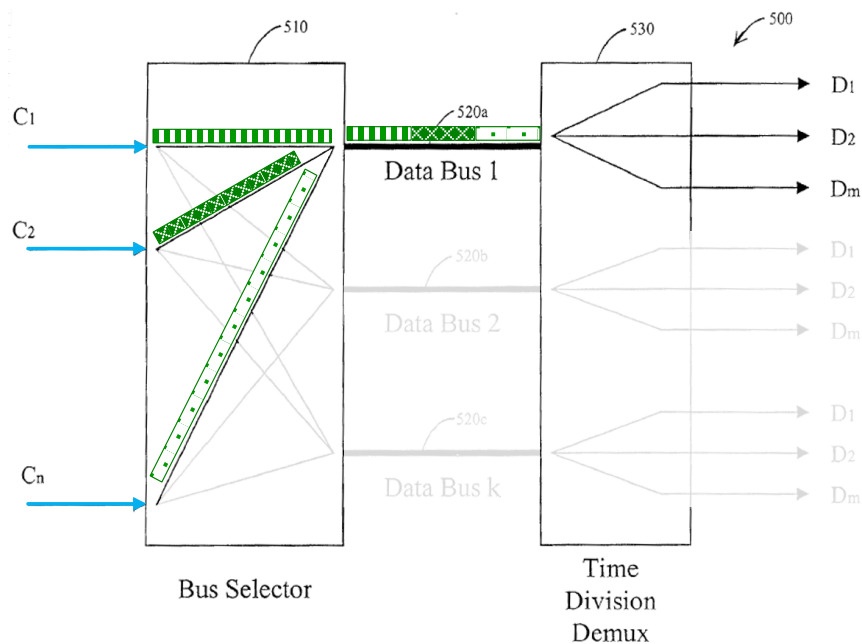


Fig. 2

Ex. 1013, Fig. 2 (annotated)

As explained for Element [1C] and as shown below, selector 240 may include a selector 510 that time-division multiplexes channels C_1 - C_n serially over a single data bus 520, thus providing the claimed “serial interface.” Ex. 1013, [0038]-[0039], Fig. 5; Ex. 1002, ¶¶ 113-119; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, p. 6; Ex. 1016, pp. 79-80; Ex. 1017, 354-355; Ex. 1034, 23, 183; Ex. 1048, 16; Ex. 1049, 1:10-40), 131-132; *see* Section VII.A.1.c.



Ex. 1013, Fig. 5 (annotated)

Zhang’s demultiplexer 230, which includes the claimed “plurality of digital down converters,” is thus operable to provide each desired channel C_1 - C_n output “via a serial interface” (via 510/Data Bus 1). Ex. 1002, ¶ 132.

Zhang thus discloses Element [14D].

To the extent Patent Owner argues that Zhang does not expressly disclose the claimed “serial interface,” implementing Zhang’s demultiplexer 230 to provide each digital channel output via a serial interface was obvious as one of two common and predictable design choices (as the ’866 Patent concedes) used by POSITAs as described above for Element [1C]. *See* Section VII.A.1.c; Ex. 1002, ¶ 117-119, 133-136; Ex. 1013, [0038]-[0039]; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, p. 8; Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1017, 354-355); Ex. 1001, 7:10-14. For the same reasons, implementing a serial interface would have been well within the POSITA’s skillset, leading to a high expectation of success. Ex. 1002, ¶ 135.

Thus, Zhang also renders obvious Element [14D].

3. Independent Claim 27

a. [27A]-[27C]

Elements [27A]-[27C] match Elements [1A]-[1C], except that Element [27C] lacks Element [1C]’s limitation “via a serial interface.” Ex. 1002, ¶¶ 137-138.

Elements [27A]-[27C] are thus taught by Zhang for the same reasons discussed above for Elements [1A]-[1C]. *See* Sections VII.A.1.a-c.

b. [27D] “wherein the cable TV device comprises a digital video recorder (DVR).”

Zhang’s cable TV device may be integrated as a wide-band front-end of a “set-top box/PVR/home media server.” Ex. 1013, [0045], Fig. 8; Ex. 1002, ¶ 139. A POSITA would have understood that “PVR” stands for “personal video recorder,” which is an alternate name for “DVR” or “digital video recorder” for recording content received by a STB. Ex. 1002, ¶¶ 139-140; Ex. 1051, [0018] (“A PVR is also referred to as [] digital video recorder (DVR)”); Ex. 1052, [0048], [0060] (“Digital Video Recorders (DVRs, also known as Personal Video Recorders, PVRs)”).

Claim 27 is thus anticipated and rendered obvious by Zhang.

4. Independent Claim 41

Elements [41A]-[41C] match Elements [14A]-[14C] and directed to substantially the same subject matter as Elements [27A]-[27C], and thus are disclosed and rendered obvious by Zhang for the same reasons discussed above for Elements [14A]-[14C] and [27A]-[27C]. *See* Sections VII.A.2.a-b, VII.A.3; *see also* Sections VII.A.1.a-c; Ex. 1002, ¶¶ 141-142.

Element [41D] (reciting a “DVR”) is identical to Element [27D]. Zhang teaches a DVR, as described above for Element [27D]. *See* Section VII.A.3.b; Ex. 1002, ¶¶ 143-144.

Accordingly, Zhang anticipates and renders obvious claim 41. *See* Sections VII.A.1-VII.A.3.

5. Dependent Claims 9, 22, 37, 51

[9/22/37/51] “The cable TV device of claim [1/14/27/41], wherein: the plurality of desired channels comprises at least one cable broadcast channel.”

Zhang’s desired channels are “cable downstream signals” transmitted in a cable system to STBs, e.g., within a “540-750 MHz” frequency band (a band reserved in the United States for broadcasting digital video to multiple users), and comprise data streams “pre-programmed” by a program provider, and “accessed or used by [plural] subscribers.” Ex. 1013, [0005]-[0007], [0024], [0029], [0041], [0045], [0047], claims 13, 27, 33; Ex. 1002, ¶¶ 145-146. A POSITA thus would have understood Zhang’s cable downstream signals are each a “cable broadcast channel” as claimed. Ex. 1033 pp. 22, 30, 40, 352; Ex. 1034 pp. 20-21.; Ex. 1002, ¶¶ 145-146.

Thus, Zhang anticipates and renders obvious claims 9, 22, 37, and 51. Ex. 1002, ¶ 147.

6. Dependent Claims 11, 24

[11/24] “The cable TV device of claim [1/14], wherein: the cable TV device comprises a digital video recorder (DVR).”

Claims 11 and 24 recite the identical limitation as Element [27D], and thus these claims are disclosed and rendered obvious by Zhang, for the same reasons discussed above for their base claims 1 and 14, respectively, and because Zhang teaches a DVR as described above for Element [27D]. *See* Sections VII.A.1, VII.A.2, VII.A.3.b; Ex. 1002, ¶¶ 148-149.

7. Dependent Claims 13, 26, 40, 54

[13/40] “The cable TV device of claim [1/27], wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.”

[26/54] “The cable TV device of claim [14/41], wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.”

Claims 13 and 40 (including their base claims) require that the ADC be configured to digitize a contiguous band of frequencies in an input signal, wherein the band comprises “a portion of a frequency spectrum of the input signal.” Claims 26 and 54 (including their base claims) require that the ADC is configured to digitize an input signal wherein the plurality of desired and undesired channels comprise “a portion of a frequency spectrum of the input signal.” Ex. 1002, ¶¶ 150-151.

As discussed above for Element [1B], Zhang's ADC 220 digitizes a multi-channel RF signal (previously downconverted to an IF frequency by Frequency Block Down Converter 210) that includes a contiguous band of frequencies of desired and undesired channels. *See* Sections VII.A.1.b, VII.A.2.a. Zhang's contiguous band of frequencies resides within the digitized multi-channel RF signal, and thus comprises "a portion of a frequency spectrum of the input signal" as recited in claims 13, 26, 40, and 54. Ex. 1002, ¶ 152.

However, to the extent claims 13, 26, 40, and 54 require the contiguous band of frequencies and desired/undesired channels to have a bandwidth that is less than the entire frequency spectrum of the input signal, Zhang teaches this as well. Ex. 1013, [0025], [0042]; Ex. 1002, ¶ 152. For example, Zhang's ADC may sample at 300 MHz, thus digitizing an input signal with a claimed "frequency spectrum" 0-150 MHz (due to the Nyquist theorem requiring sampling rate to be at least twice the frequency of the sampled signal). Ex. 1013, [0025], [0041]-[0042]; Ex. 1033 pp. 98-99; Ex. 1045, 114; Ex. 1002, ¶¶ 72, 152. Zhang's contiguous band of desired and undesired channels may comprise only a portion of this frequency spectrum from 20-130 MHz. Ex. 1013, [0025], [0041]-[0042]; Ex. 1033 at 98-99; Ex. 1045, 114; Ex. 1002, ¶¶ 72, 152.

Zhang thus anticipates and renders obvious claims 13, 26, 40, and 54. Ex. 1002, ¶ 153.

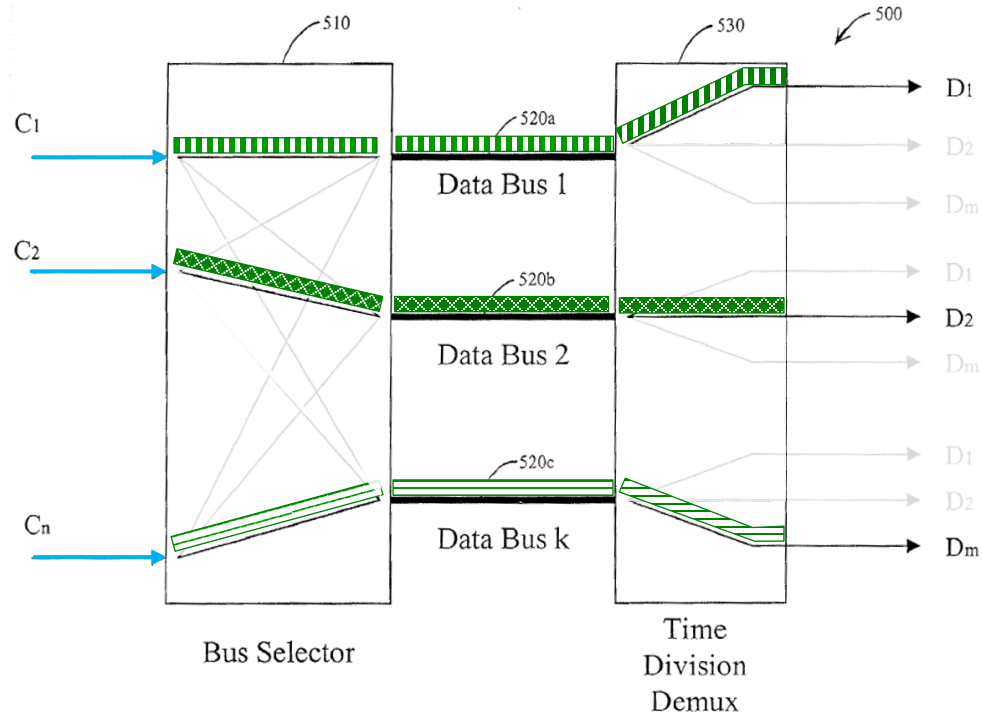
8. Dependent Claims 35, 49

[35] “The cable TV device of claim 27, wherein: the DFE is operable to provide the plurality of desired channels via a parallel interface.”

[49] “The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide a plurality of digital channel outputs, comprising each digital channel output, via a parallel interface.”

As discussed above for Elements [1C] and [14D], Zhang’s demultiplexer 230 and selector 240 output the “plurality of desired channels”/“plurality of digital channel outputs,” via one or more buses in Digital Selector 240. *See* Sections VII.A.1.c, VII.A.2.c. As also discussed above, for “one” bus using “time division multiplexing,” digital selector 240 is arranged as the “serial interface” recited in Elements [1C] and [14D]. Ex. 1002, ¶¶ 154-155; Sections VII.A.1.c, VII.A.2.c.

Zhang also describes other arrangements of selector 240, for example a version providing the channels “through different data buses” as shown below, which is a “parallel interface” as recited in claims 35 and 49. Ex. 1013, [0038]-[0039], Fig. 5; Ex. 1002, ¶¶ 74-76, 115-118, 156-157; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, p. 6; Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1017, 354-355; Ex. 1034, 23, 183; Ex. 1048, 16; Ex. 1049, 1:10-40; Ex. 1017, pp. 354-355.



Ex. 1013, Fig. 5 (annotated)

To the extent Patent Owner argues that Zhang does not expressly disclose the claimed “parallel interface,” such an interface was well-known (as the ’866 Patent concedes), and implementing Zhang’s demultiplexer 230 and selector 240 to provide the channels “via a parallel interface” would have been obvious based on a POSITA’s background knowledge, creativity, and common sense. Ex. 1002, ¶ 158; *see e.g.*, Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, p. 6; Ex. 1016, pp. 79-80 (Figure 6-25); Ex. 1017, pp. 354-355; Ex. 1034, pp. 23, 183; Ex. 1048, p. 16; Ex. 1049, 1:10-40; Ex. 1001, 6:55-58.

For example (as discussed above for Element [14D]), it was well-known that digital circuits implemented in CMOS (the technology used in Zhang) transmit data

either in parallel or in serial. *See* Section VII.2.c; Ex. 1002, ¶ 159; Ex. 1013, [0044], [0048]; Ex. 1016, pp. 23, 31-47, 49-51, 80 (Fig. 6-25); Ex. 1015, pp. 5-6.

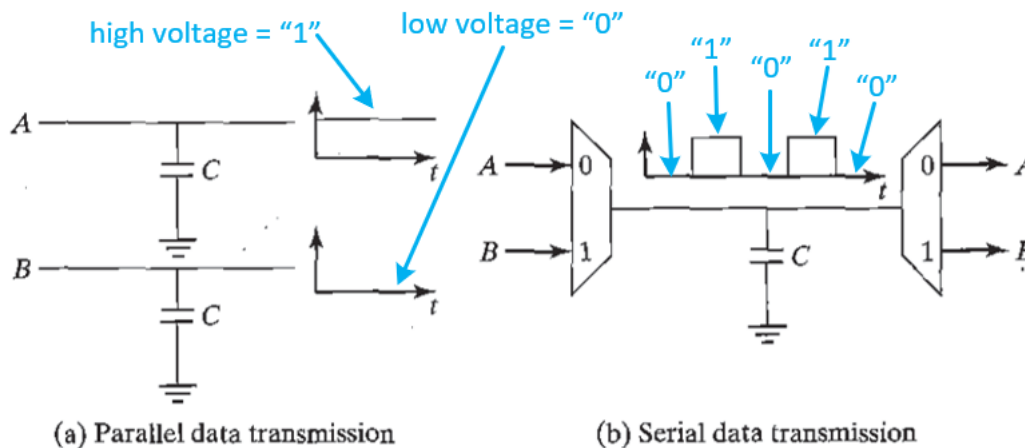


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1016, p. 80 (Figure 6-25) (annotated)

Thus, implementing Zhang’s circuits to provide the desired channels “via a parallel interface” would have simply been choosing among two identified, predictable design choices. Ex. 1002, ¶ 160; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, pp. 5-6; Ex. 1016, pp. 79-80; Ex. 1017, pp. 354-355. For the same reasons, implementing a parallel interface would have been well within the POSITA’s skillset, leading to a high expectation of success. Ex. 1002, ¶¶ 160-161.

Thus, Zhang’s Digital Channel Demultiplexer 230 and all or part of Digital Selector 240 anticipate and render obvious claims 35 and 49.

9. Dependent Claims 36, 50

**[36] “The cable TV device of claim 27, wherein:
the DFE is operable to provide the plurality of desired channels via a
serial interface.”**

[50] “The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide each digital channel output via a serial interface.”

Claims 36 and 50 are substantially identical to the “serial interface” limitation in Elements [1C] and [14D], respectively, which are taught by Zhang. *See* Sections VII.A.1.c, VII.A.2.c; Ex 1002, ¶¶ 162-163.

Claims 36 and 50 are thus anticipated and rendered obvious by Zhang for the same reasons discussed as their base claims, and for Zhang’s additional teaching (alone or with the knowledge of the POSITA) of the serial interface as described with respect to Elements [1C] and [14D]. *See* Sections VII.A.1.c, VII.A.2.c; Ex. 1002, ¶¶ 163-164.

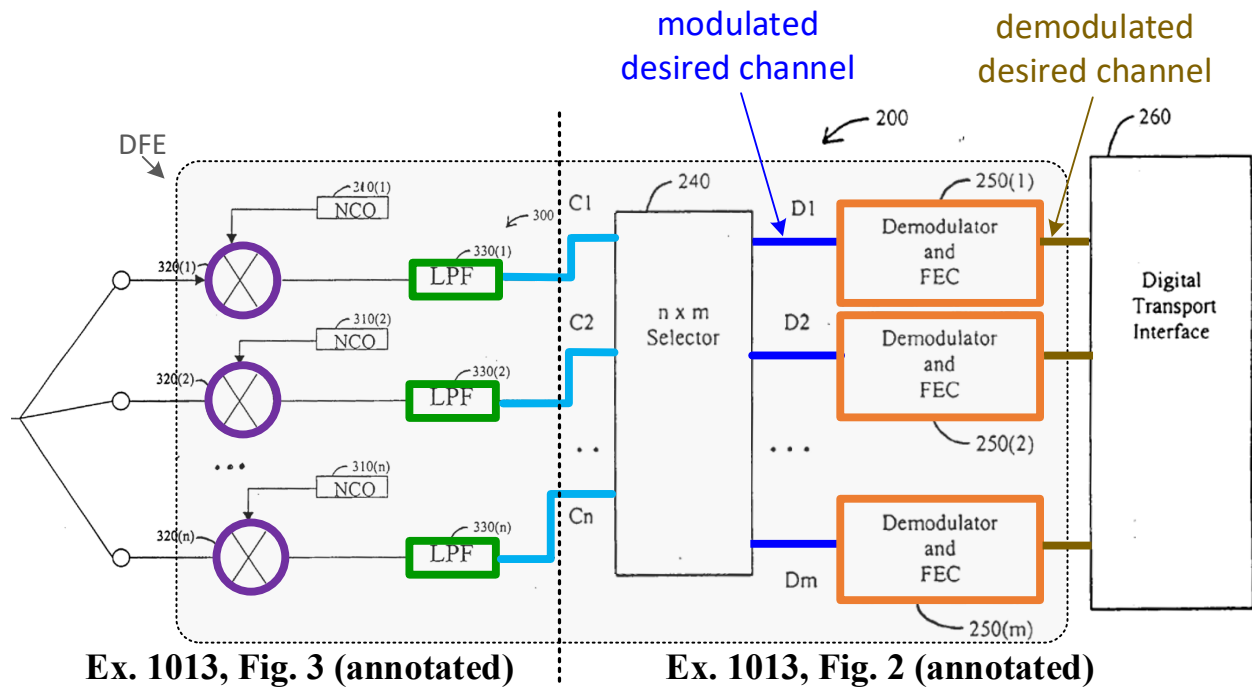
10. Dependent Claims 7, 20, 33, 47

[7/33] “The cable TV device of claim [1/27], wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.”

[20/47] “The cable TV device of claim [14/41], wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired channels, to provide a demodulated channel as the digital channel output.”

Zhang discloses claims 7, 20, 33, and 47. Ex. 1002, ¶ 165. The composite figure below illustrates Zhang’s Figure 3 embodiment 300 of demultiplexer 230 within Zhang’s system illustrated in Figure 2. Ex. 1002, ¶ 166. Zhang discloses a

plurality of digital demodulators 250(1)-250(m) (**orange**), which are part of the same digital circuitry, for example on the same chip, as demultiplexer 230/300 and selector 240, which are cited for the claimed “DFE” in independent claims 1 and 27 from which claims 7 and 33 respectively depend. Ex. 1013, [0005], [0011], [0029]-[0031], [0038]-[0039], [0044]-[0047]; Ex. 1002, ¶ 165-166; *see* Sections VII.A.1.b-c, VII.A.2.b-c, VII.A.3.a, VII.A.4.



Selector 240 receives modulated desired channels C_1 - C_n (**light blue**) from the filters 330 (**green**) and provides those channels (**dark blue**) as required in Element [1C]. *See* Section VII.A.1.c. As shown above, those channels are provided within the DFE to demodulators 250 (**orange**), which each demodulate one of the desired channels C_1 - C_n (received via D_1 - D_m) and which is outputted as demodulated

channels (**brown**). Ex. 1013, [0028]-[0032]; Ex. 1002, ¶ 167. Zhang thus anticipates and renders obvious claims 7 and 33.

Zhang’s demultiplexer 230 is also cited for the claimed “plurality of digital down converters” in claims 14 and 41, from which claims 20 and 47 depend. Claims 20/47 recite “each digital down converter comprises a digital demodulator,” which Zhang also discloses as shown below. Ex. 1002, ¶ 168.

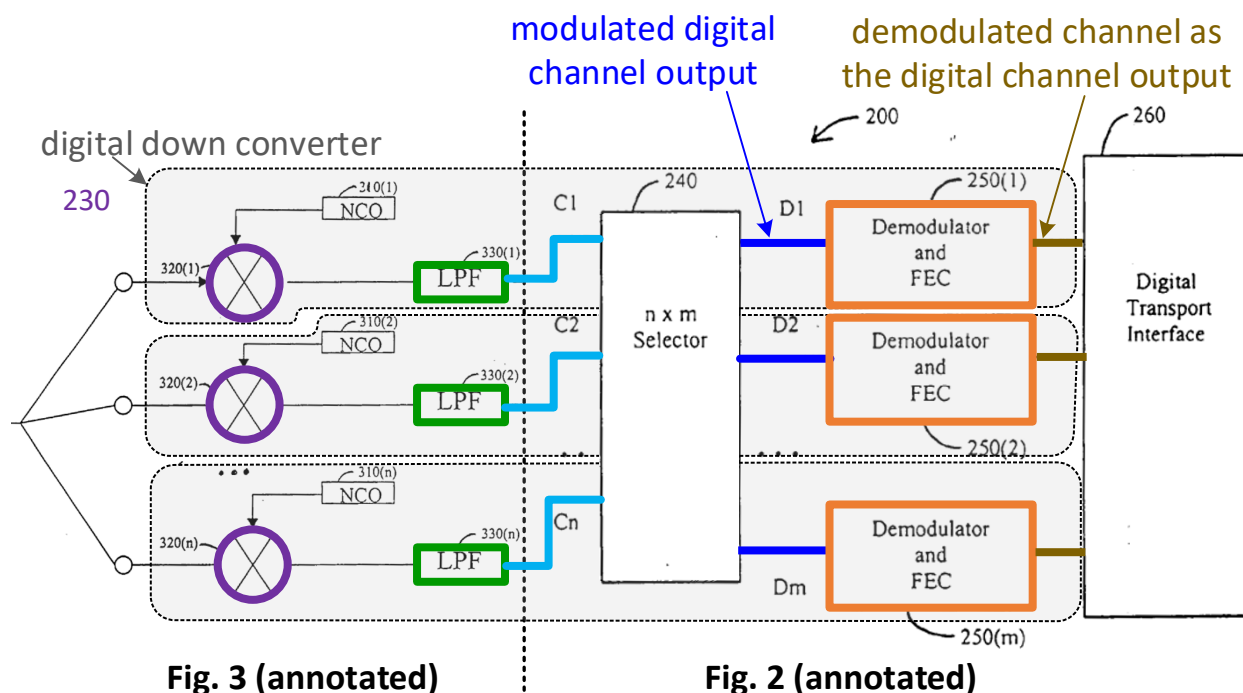


Fig. 3 (annotated)

Fig. 2 (annotated)

Ex. 1013, Figs. 2-3, 5 (annotated)

Each digital down converter in Zhang includes a complex multiplier 320 (**purple**) and filter 330 (**green**), with selector 240 providing modulated digital channel outputs (**dark blue**) as recited in Element [14D]. See Section VII.A.2.c. As shown above, these outputs are provided, within each digital down converter, to a respective demodulator 250 (**orange**), which then output demodulated digital

channel outputs (**brown**). Ex. 1013, [0028]-[0032]; Ex. 1002, ¶ 169; *see* Section VII.A.2.c. Thus, Zhang discloses that “each digital down converter comprises a digital demodulator operable to demodulate a desired channel ... to provide a demodulated channel as the digital channel output.” As such, Zhang anticipates and renders obvious claims 20 and 47. Ex. 1002, ¶¶ 169.

Furthermore, claims 7 and 20 require (as recited in base claims 1 and 14) that each desired channel/digital channel output is provided “via a serial interface.” Just as described in the ’866 patent, Zhang’s selector 240 (specifically, selector 510 and data bus 520 in Fig. 5 within selector 240) provide the desired channels/digital channel outputs in their modulated form via a serial interface to demodulators 250. *See* Sections VII.A.1.c, VII.A.2.c; Ex. 1001, 7:10-14; Ex. 1002, ¶ 170.

To the extent claim 7 and 20 require a serial interface to be at the output of the demodulators (or at any other point in the DFE and digital down converters as shown below), such an interface was well-known, and implementing Zhang’s DFE and plurality of digital down converters with a serial interface at the output of the demodulators would have been obvious in light of a POSITA’s general knowledge, creativity, and common sense.⁵ *See e.g.*, Ex. 1014, 30:31-42, 31:15-22; Ex. 1015,

⁵ Petitioner does not concede that such a construction is supported under pre-AIA 35 U.S.C. 112, ¶ 1.

pp. 5-6; Ex. 1016, pp.23, 31-37, 49-51, 79-80 (Figure 6-25); Ex. 1017, pp. 354-355; Ex. 1002, ¶ 170. As the '866 patent concedes, outputting a digital data stream via serial interface was “commonly known,” i.e., Applicant Admitted Prior Art (AAPA). Ex. 1001, 7:10-14; Ex. 1002, ¶ 170.

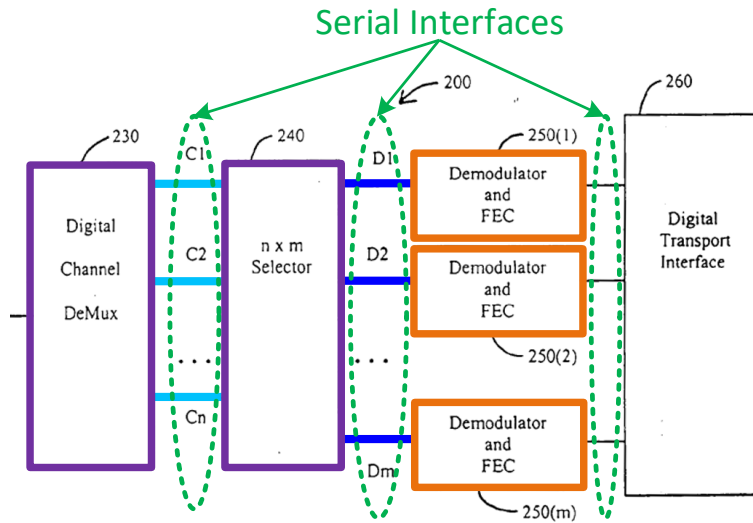


Fig. 2

Ex. 1013, Fig. 2 (annotated)

For example, as explained above with respect to Elements [1C] and [14D], CMOS digital circuits (the technology used in Zhang) transmit data either in parallel (one wire per bit), or serially (one bit at a time over a single wire). Ex. 1002, ¶ 171; Ex. 1016, pp. 23, 31-37, 49-51, 80 (Figure 6-25); Ex. 1015, pp. 5-6; *see* Section VII.A.1.c, VII.A.2.c.

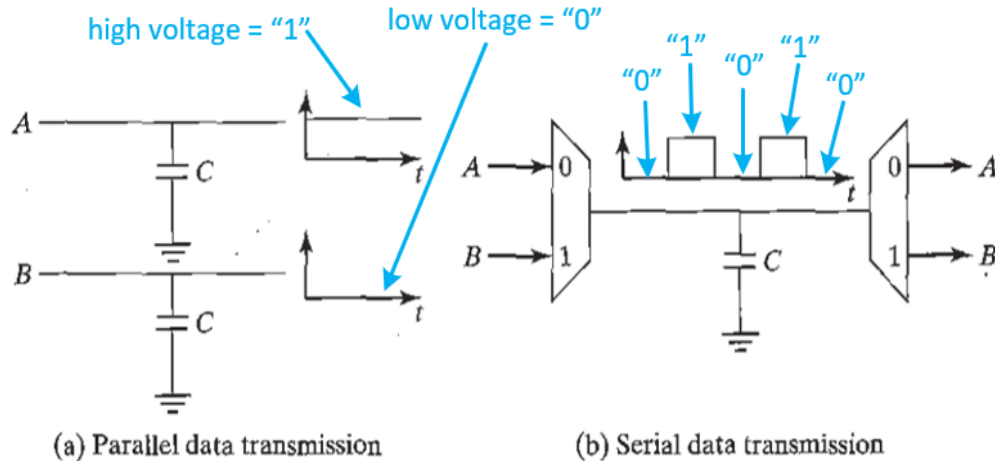


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1016, p. 80 (Figure 6-25) (annotated)

A POSITA implementing the Zhang circuit in CMOS would have been aware of and fully able to implement a serial interface between any of Zhang's digital circuit blocks as shown below, since it was obvious to try as a typical and predictable choice. Ex. 1002, ¶¶ 74-76, 172; Ex. 1014, 30:31-42, 31:15-22; Ex. 1015, pp. 5-6; Ex. 1016, pp. 79-80; Ex. 1017, pp. 354-355.

For the same reasons, implementing a serial interface was well within the POSITA's skillset, leading to a high expectation of success. Thus, Zhang renders obvious (ground B) claims 7 and 20 for this additional reason. Ex. 1002, ¶ 172.

11. Dependent Claims 3, 4, 16, 17, 29, 30, 43, 44

[3/29] "The cable TV device of claim [1/27], wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component."

[16/43] “The cable TV device of claim [14/41], wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.”

[4/17/30/4/] “The cable TV device of claim [3/16/29/43], wherein: the I and Q components of each corresponding complex signal are at baseband.”

Zhang’s demultiplexer 230/300 includes multiple paths, each including a “complex multiplier” 320 (purple) that downconverts a digital channel within the digital RF signal to baseband, and a filter 330 (green) that isolates the digital channel by filtering out all other channels. Ex. 1013, Figs. 2-3, [0012], [0030]-[0034], claims 34, 36-37; Ex. 1002, ¶¶ 173-174.

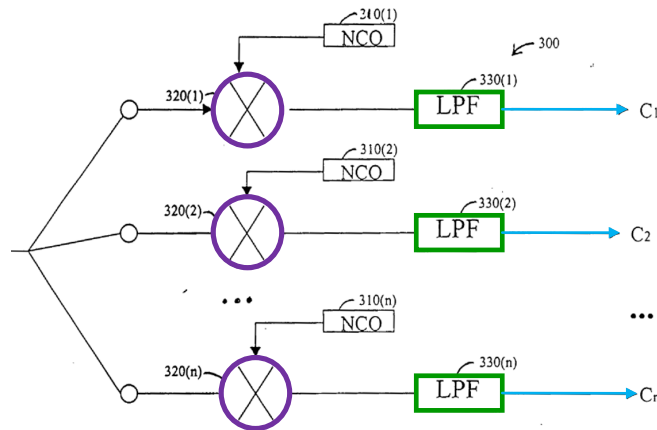


Fig. 3

Ex. 1013, Fig . 3

A POSITA would have understood that “multiplier” (as used in Zhang) and “mixer” are interchangeable names for the same device that shifts the frequency of a modulated signal by multiplying it by another sinusoidal signal having a frequency equal to the amount of the shift. Ex. 1002, ¶¶ 175; Ex. 1013, [0032]; Ex. 1001, 4:62-

64 (“mixers 211 and 221 multiplies (mixes) an amplified RF signal 203 with a respective first oscillator frequency”); *compare* Ex. 1001, 6:6-25 (describing four “multipliers” in complex mixer of Figure 3) *with* Ex. 1001, 9:18-60 (describing four “mixers” in complex mixer in Figure 3); *see also* Ex. 1018, Fig. 1, p. 133 (“frequency downconversion ... is performed by multiplying (mixing) the signal with a sinusoid”); Ex. 1002, ¶ 175.

Further, because Zhang’s multipliers are “complex,” a POSITA would have understood that each output at baseband would be a complex signal, i.e., having quadrature (Q) and in-phase (I) components. Ex. 1013, [0012], [0030], [0032]; Ex. 1002, ¶¶ 65-67, 176-177; *see also* Ex. 1039 pp. 11 Ex. 1018, pp. 133-134 (“The realization of a multiplier for mixing a real signal with a complex exponential requires two real multipliers, as illustrated in Fig. 2. The real and imaginary parts of the mixer output are called the *in-phase (I)* and *quadrature (Q)* components. In Fig. 2 the frequency of the complex exponential is chosen to be the same as the center frequency of the passband signal In this case there is no image problem associated with the *complex mixer*.” (emphasis added)).

Thus, Zhang anticipates and renders obvious claims 3, 4, 16, 17, 29, 30, 43, 44. Ex. 1002, ¶ 178.

12. Dependent Claims 5, 18, 31, 45

[5/31] “The cable TV device of claim [3/29], wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.”

[18/45] “The cable TV device of claim [16/43], wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.”

Zhang discloses filters 330 (**green**) that as described above for claim 3, 16, 29, and 43, filter the complex signal from the complex multiplier to isolate the selected channel at baseband and filter out unwanted channels. Ex. 1013, Fig. 3, [0032]; Ex. 1002, ¶¶ 78-79, 180; *see* Section VII.A.11. The channels are 6 MHz. Ex. 1013, [0006]; Ex. 1002, ¶¶ 179-180.

Thus, Zhang anticipates and renders obvious claims 5, 18, 31, and 45. Ex. 1002, ¶ 181.

13. Dependent Claims 6, 19, 32, 46

[6/32] “The cable TV device of claim [3/29], wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.”

[19/46] “The cable TV device of claim [16/43], wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.

Claims 6 and 32 recite identical limitations to claims 7 and 33, and claims 19, and 46 recite identical limitations to claims 20 and 47, except that “a desired channel,

of the plurality of desired channels” in claims 7, 20, 33, and 47 is replaced with “the corresponding complex signal” in claims 6, 19, 32, and 46. Ex. 1002, ¶¶ 182-183; *see* Section VII.A.10.

As discussed above (*see* Section VII.A.10) for claims 7, 20, 33, and 47, Zhang discloses the claimed “demodulating” and “plurality of demodulators” as digital demodulators 250(1)-250(m) (**orange**), each demodulating one of the desired channels received on inputs D_1 - D_m from Digital Selector 240, which receives the desired channels from inputs C_1 - C_n , and outputting the demodulated channel to Digital Transport Interface 260. Ex. 1013, [0005], [0011], [0029]-[0031], [0038]-[0039], [0042]-[0045]; Ex. 1002, ¶ 184. Moreover, as described above for claims 3-4, 16-17, 29-30, and 43-44, a POSITA would have understood that Zhang’s demodulators 250(1)-250(m) (**orange**) receive complex signals from the “complex multiplier.” *See* Section VII.A.11; Ex. 1002, ¶¶ 65-67, 184; Ex. 1018, pp. 133-134.

Thus, Zhang anticipates and renders obvious claims 6, 19, 32, and 46.

B. Ground C: Zhang-Reisman

Zhang-Reisman (ground C) renders obvious claims 10-12, 23-25, 27, 33, 35-41, 47, 49-55, 61, 63-69, 75, and 77-82. Ex. 1002, ¶¶ 185-220.

1. Independent Claims 27 and 41, and Dependent Claims 29-33, 35-37, 40, 43-47, 49-51, and 54

Zhang anticipates and renders obvious claims 27 and 41 (grounds A/B) for the reasons discussed above. *See* Sections VII.A.3-4. Ex. 1002, 185-187.

To the extent Patent Owner argues that Zhang’s PVR is not a “DVR” as recited in Elements [27D] and [41D], Reisman discloses this feature. Ex. 1002, ¶ 188. Reisman teaches that STBs in a cable system may include a digital video recorder (DVR). Ex. 1052, [0005], [0043], [0048], [0060], [0073], [0098] (“TV/ITV 130 is understood to commonly include a set-top box”), [0112], [0118], [0191], [0197], [0212], [0281]-[0285], [0296], [0546]; Ex. 1002, ¶¶ 188-189.

A POSITA would have been motivated include Reisman’s DVR in Zhang’s STB to provide a more feature-filled and individualized user experience, which in the proposed combination still includes Zhang’s wideband front-end receiver components cited for Elements [27A]-[27C] and [41A]-[41C]. *See* Sections VII.A.1, 3; Ex. 1002, ¶ 190. Reisman’s DVR improves user experience by allowing time-shifted and on-demand viewing, and enabling, e.g., fast-forwarding, rewinding, and pausing of live programming. Ex. 1052, [0191], [0197], [0212], [0284]-[0285], [0546], [0758]; Ex. 1002, ¶ 190. Adding Reisman’s DVR to Zhang’s system merely applies a known technique of integrating a DVR into a STB as taught in Reisman, to a known STB with a wideband front-end receiver as taught in Zhang that was

ready for improvement to yield a predictable result (DVR capabilities added to the STB). Ex. 1002, ¶ 190.

A POSITA would have had a reasonable expectation of success because STBs and DVRs were well-known, and assembling well-known components (CPUs, memory, connectors, QAM demodulators, MPEG-2 decoders, etc.) comprising such systems was within the ordinary skillset of a POSITA. Ex. 1052, [0072], [0112], [0197] (referring to “common usage” of a DVR in a cable system); Ex. 1002, ¶¶ 191-192.

Thus, Zhang-Reisman renders obvious claims 27 and 41, and claims 29-33, 35-37, 40, 43-47, 49-51, and 54, which depend from claims 27 or 41 and which are taught by Zhang as described above. *See* Sections VII.A.5-13; Ex. 1002, ¶ 192.

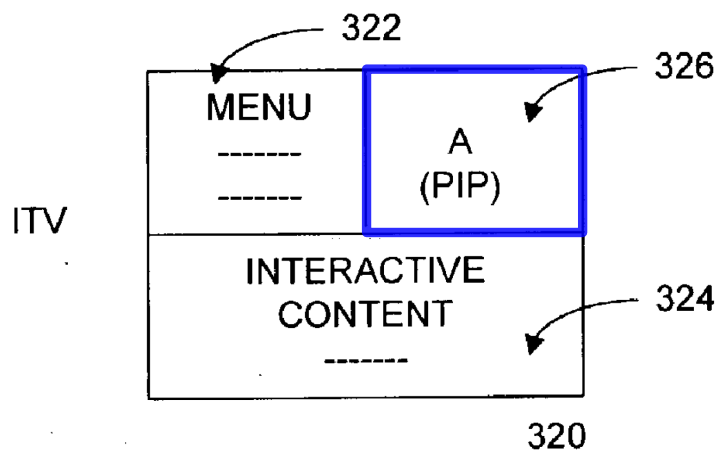
2. Independent Claim 55

a. [55A]-[55C]

Elements [55A]-[55C] match Elements [1A]-[1C], except that Element [55C] lacks Element [1C]’s limitation “via a serial interface.” Ex. 1002, ¶¶ 193-194. Elements [55A]-[55C] are thus taught by Zhang for the same reasons discussed above for Elements [1A]-[1C]. *See* Section VII.A.1.a-c.

b. [55D] “wherein the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.”

Reisman discloses Element [55D]. Ex. 1002, ¶¶ 195-198. Reisman teaches that STBs in a cable system include a “picture-in-picture display” as shown below (blue). Ex. 1052, [0073], [0098] (“TV/ITV 130 is understood to commonly include a set-top box”), [0118], [0120]-[0121] (“picture-in-picture (PIP) frame 326” used to present a base program), [0187], [0278], [0291], [0378], [0534], [0537], [0546], Fig. 3; Ex. 1002, ¶ 195.



Ex. 1052, Fig. 3 (annotated)

A POSITA would have been motivated to include Reisman’s “picture-in-picture display” capability in Zhang’s STB, which in the proposed combination still has the wideband front-end receiver components cited for Elements [55A]-[55C] (as discussed above with respect to [1A]-[1C]) to allow a user to view different content simultaneously. Ex. 1002, ¶ 196. Reisman teaches that “picture-in-picture” beneficially displays a program in a PIP window while simultaneously providing,

e.g., navigation options and interactive content in other windows. Ex. 1052, [0121], [0278], Fig. 3; Ex. 1002, ¶ 196. Reisman's PIP also enables "multitasking," by displaying, e.g., two TV programs, and swapping them between full screen and a smaller PIP window. Ex. 1052, [0061], [0063], [0378], [0546]. Thus, modifying Zhang with Reisman represents the obvious application of a known technique (having a STB configure and display desired channels in a picture-in-picture display, per Reisman) to a known device (Zhang's STB with a wideband digital front-end receiver) that was ready for improvement to yield a predictable result (PIP capability in the STB). Ex. 1002, ¶ 196.

A POSITA would have had a reasonable expectation of success, because STBs with PIP capability were well-known, and assembling and programming components (CPUs, software, memory, MPEG-2 decoders, etc.) making up such systems was well within the skillset of a POSITA. Ex. 1052, [0112], [0121] (PIP is "typical" for "common ITV system"), [0534]; Ex. 1002, ¶ 197. Moreover, Reisman's PIP and Zhang's receiver provide complementary features: Zhang's receiver provides multiple channels concurrently, and Reisman's PIP displays multiple programs concurrently. Ex. 1052, [0378], [0534]; Ex. 1013, [0005], [0045], *see also* [0011], [0029]-[0031], [0038]-[0039], [0042], [0044]; Ex. 1002, ¶ 197.

Zhang-Reisman renders obvious claim 55. *Id.*, ¶ 198.

3. Independent Claim 69

Elements [69A]-[69C] match Elements [14A]-[14C] and directed to substantially the same subject matter as Elements [55A]-[55C], and thus are anticipated and rendered obvious by Zhang for the same reasons discussed above for Elements [1A]-[1C] and [55A]-[55C]. *See* Sections VII.A.1.a-c, VII.A.2.a-b, VII.B.2. Ex. 1002, ¶¶ 199-200. Element [69D], like Element [55D], requires a “a picture-in-picture display.” Zhang-Reisman as discussed above for Element [55D] renders this obvious. *See* Section VII.B.2.b; Ex. 1052, [0073], [0098] (“TV/ITV 130 is understood to commonly include a set-top box”), [0118], [0120]-[0121] (“picture-in-picture (PIP) frame 326” used to present a base program), [0187], [0278], [0291], [0378], [0534], [0537], [0546], Fig. 3; Ex. 1002, ¶¶ 201.

For the reasons discussed above, Zhang-Reisman as described with respect to Element [55D] also teaches Element [69D], and thus renders claim 69 obvious. *See* Section VII.B.2 ; Ex. 1002, ¶¶ 202-203.

4. Dependent Claims 9, 22, 37, 51, 65, and 79

Claims 65 and 79 depend from claims 55 and 69 (rendered obvious by Zhang-Reisman), and recite identical limitations to claims 9, 22, 37 and 51, which as described above, are taught by Zhang. *See* Sections VII.A.5.

Zhang-Reisman thus renders claims 65 and 79 obvious for the same reasons discussed above for their base claims 55 and 69, respectively, and because Zhang

teaches a cable broadcast channel. Ex. 1002, ¶¶ 204-205; *see* Sections VII.A.5, VII.B.2-3.

Reisman additionally discloses the claimed “cable broadcast channel.” *Id.*, ¶ 206.

Reisman teaches that TV systems include STBs in a cable system, and further, Reisman teaches that programs may be sent “one-way, such as broadcast,” which Reisman describes as “any form of distribution intended to go simultaneously to many recipients (one-to-all, one-to-many), including ... cable and satellite distribution, and the like.” Ex. 1052, [0063], [0073], [0086]-[0088], [0090], [0098], [0120]-[0121], [0125], Fig. 1; Ex. 1002, ¶ 206; *see* Sections VII.B.1-3.

To the extent Zhang’s digital wideband receiver integrated in a STB is not already configured to receive desired channels that include “at least one cable broadcast channel,” it would have been obvious for Zhang to receive such a channel as taught in Reisman for the benefit of broadening the channels Zhang’s STB provides. Ex. 1052, [0008], [0643]-[0645]; Ex. 1002, ¶ 207. Such a modification would have been nothing more than applying a known technique (Reisman’s use of a STB to receive cable broadcast channel in a cable network) to a known device (Zhang’s STB) ready for improvement (by adding the ability to receive cable broadcasts from various sources) to yield predictable results (providing broadcast channels via the STB). Ex. 1052, [0008], [0643]-[0645]; Ex. 1002, ¶ 207.

A POSITA would have had a reasonable expectation of success because receiving cable broadcast channels on cable networks using STBs was ubiquitously well-known, and using Zhang’s STB to receive Reisman’s cable broadcast channels would have been well within capability of a POSITA. *Id.*, ¶¶ 208-209.

Thus, claims 9, 22, 37, 51, 65, and 79 are rendered obvious over Zhang-Reisman for this further reason.

5. Dependent Claims 10, 23, 38, 52, 66, and 80

[10/23/38/52/66/80] “The cable TV device of claim [1/14/27/41/55/69], wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.”

As discussed above for claims 9, 22, 37, 51, 65, and 79, each of Zhang and Reisman teaches a STB in a cable system that broadcasts channels, and it would have been obvious to use Zhang’s STB to receive them. Ex. 1052, [0008], [0063], [0073], [0086]-[0088], [0090], [0098], [0643]-[0645], Fig. 1; *See* Section VII.A.5, VII.B.4; Ex. 1002, ¶¶ 210-211. Reisman further teaches that transmission protocols in a cable system include “DOCSIS (Data Over Cable Service Interface Specification),” where transmission of base TV or video and enhancements may be by DOCSIS and “directed to ... STB [] addresses.” Ex. 1052, [0052], [0087], [0235]; Ex. 1002, ¶ 211.

A POSITA would have been motivated to add to Zhang’s STB the ability to receive a desired channel via DOCSIS as taught in Reisman. Ex. 1002, ¶ 212. Doing

so would allow desired channels to be addressed to a specific Zhang STB, which benefits the user by enabling enhanced features such as video-on-demand or other personalized content. *Id.* A POSITA would have further recognized that implementing DOCSIS in Zhang's STBs would allow for base video and enhancements to be sourced together over the same distribution infrastructure, eliminating the need for a separate infrastructure, such as a separate internet connection. *Id.*; Ex. 1052, [0089], [0149], [0304], [0484]. Such a modification represents the application of a known technique (Reisman's DOCSIS protocol for the transmission of channels) to a known device (Zhang's STB with the wideband digital front-end receiver) ready for improvement to yield predictable results (the STB receives channels via DOCSIS). Ex. 1002, ¶ 200. Moreover, Zhang already discloses incorporating a DOCSIS return channel, and adding a DOCSIS forward channel as disclosed in Reisman would simply have been a logical design choice to implement the entire DOCSIS standard. Ex. 1013, [0047]; Ex. 1002, ¶ 212.

A POSITA would have had a reasonable expectation of success because the DOCSIS protocol was a known standard designed for cable systems and STBs, and adopted by cable operators at the time. Ex. 1002, ¶ 213; Ex. 1021 pp. 2-5, Fig. 1-2; Ex. 1033 pp. 27, 211-212. Thus, POSITAs would have been familiar with the standard and accustomed to implementing it in STBs. Ex. 1002, ¶ 213. Modifying Zhang's STB to receive at least one desired channel via the DOCSIS protocol would

have been a straightforward engineering exercise well within the ordinary skillset of a POSITA. *Id.*, ¶¶ 213-214.

Claims 10, 23, 38, 52, 66, and 80 are rendered obvious over Zhang-Reisman.

6. Dependent Claims 11, 24, 67, and 81

Claims 11, 24, 67, and 81 recite the identical limitation as Element [27D], and thus these claims are rendered obvious by Zhang-Reisman, for the same reasons discussed above for their base claims 1, 14, 55, and 69, respectively, and because Reisman teaches a DVR as described and combined above with respect to Element [27D]. *See* Section VII.A.1-2, VII.A.3.b, VII.B.1; Ex. 1002, ¶¶ 215.

7. Dependent Claims 12, 25, 39, 53

Claims 12 and 39 recite the identical limitation of Element [55D], and claims 25 and 53 recite the identical limitation of Element [69D], which is substantially the same as Element [55D]. Ex. 1002, ¶¶ 216-217. As discussed above, Reisman discloses these limitations. *See* Sections VII.B.2.b VII.B.3; Ex 1002, ¶¶ 194-198, 201-203, 216-217.

Claims 12, 25, 39, and 53 are thus obvious over Zhang-Reisman for the same reasons discussed above for their base claims 1, 14, 27, and 41, respectively, and because Reisman teaches PIP as combined with Zhang as described above with respect to Elements [55D] and [69D]. *See* Sections VII.A.1-4 (base claims 1, 14,

27, 41), VII.B.1, VII.B.2.b (Element [55D]), VII.B.3 (Element [69D]); Ex. 1002, ¶ 218.

8. Dependent claims 57-61, 63-64, 68, 71-75, 77-78, and 82

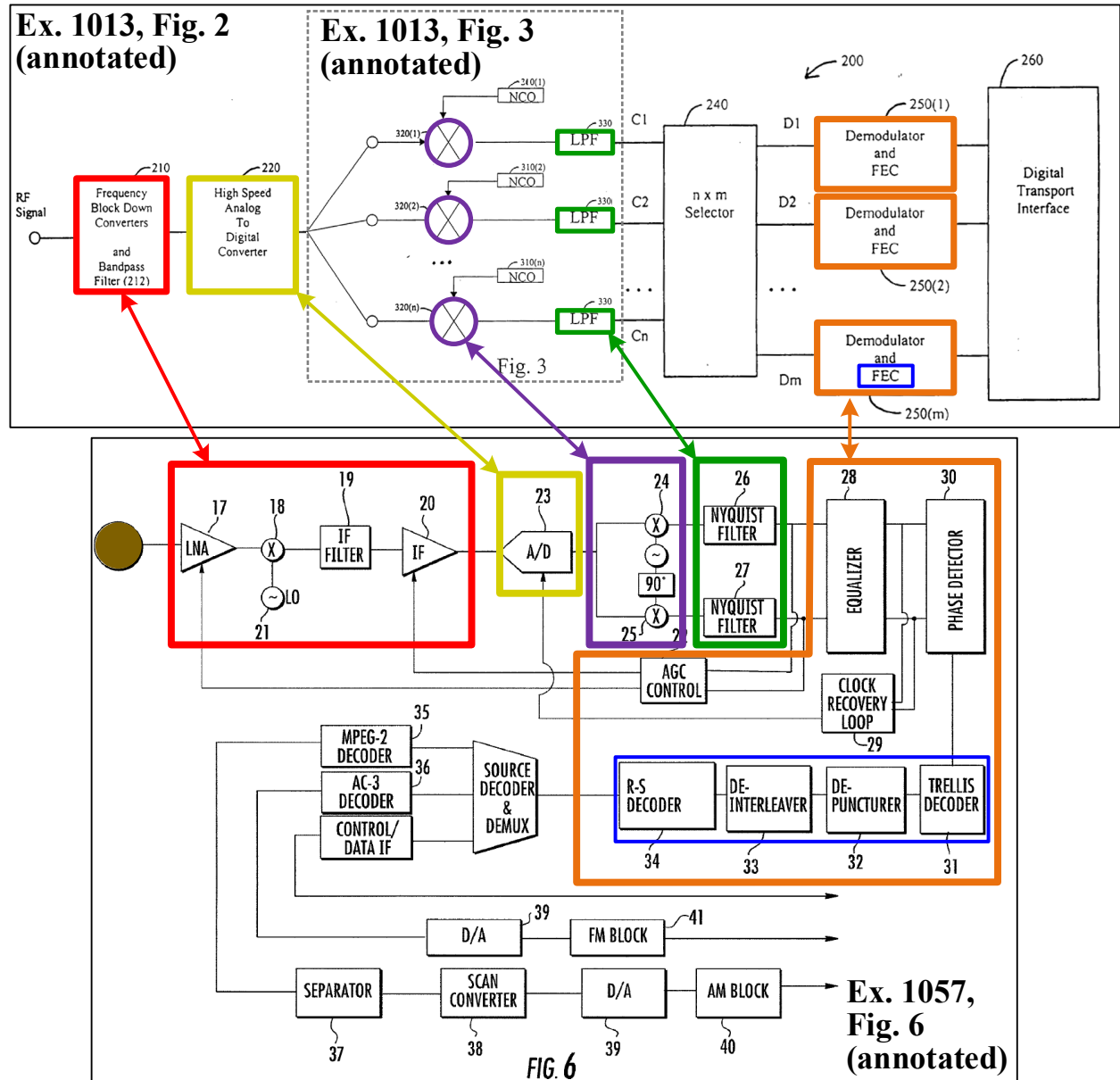
Claims 57-61, 63-64, 68, 71-75, 77-78, and 82 depend from claims 55 and 69 (rendered obvious by Zhang-Reisman) include identical limitations to claims 29-33, 35-36, 40, 43-47, 49-50, and 54, respectively. As described above, these limitations are taught by Zhang. *See* Sections VII.7-13. Ex. 1002, ¶¶ 150-184, 219

Zhang-Reisman thus renders claims 57-61, 63-64, 68, 71-75, 77-78, and 82 obvious for the same reasons discussed above for their base claims 55 and 69, and for Zhang's additional teaching of these limitations. *Id.*, ¶¶ 219-220.

C. Ground D: Zhang-Jackson, and Ground E: Zhang-Reisman-Jackson

Zhang-Jackson (ground D) renders obvious claims 2-6, 15-19, 28-32, and 42-46, and Zhang-Reisman-Jackson (ground E) renders obvious claims 28-32, 42-46, 56-60 and 70-74. Ex. 1002, ¶ 221.

As shown below, Jackson discloses in Figure 6 a receiver system for demodulating digitally-encoded cable TV channels, having the same general architecture and functionality as Zhang's multi-channel demodulator system in Figure 2. Ex. 1057, Fig. 6, [0025]-[0027]; Ex. 1013, Fig. 2, [0023], [0045]; Ex. 1002, ¶ 222.



Both systems have similar RF tuners (**red**) that downconvert an analog RF signal received from a cable system to a lower frequency, an analog to digital converter (**gold**) that digitizes the downconverted analog RF signal, a complex mixer/multiplier (**purple**) that downconverts a digital channel within the digital RF signal to baseband, a filter (**green**) that isolates the digital channel at baseband and

filters out all other channels, and a demodulator (**orange**) that demodulates the channel with the use of functional blocks like forward error correction (**dark blue**). Ex. 1013, Figs. 2-3, [0025]-[0031], [0045]; Ex. 1057, Fig. 6, [0025]; Ex. 1002, ¶ 223.

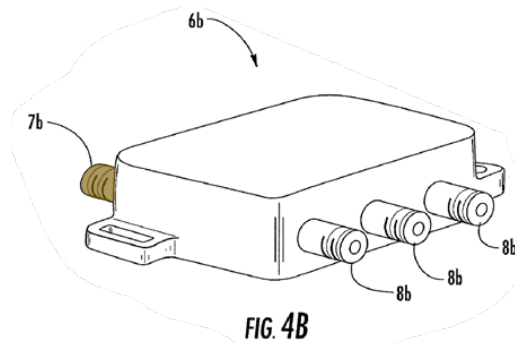
Jackson discloses additional details that teach the elements recited in claims 2-6, 15-19, 28-32, 42-46, 56-60, and 70-74, which a POSITA would have found advantageous for implementing the receivers in Zhang and Zhang-Reisman for the reasons discussed below. Ex. 1002, ¶ 224. The features in Jackson that are applied to Zhang as described below are independent of the Reisman features (e.g., the addition of a DVR, picture-in-picture) added to Zhang for claims 25, 38, 51, and 64, and thus a POSITA would have added Jackson's teachings to Zhang-Reisman or Zhang with the same motivation and expectation of success. Ex. 1002, ¶ 224.

1. Dependent Claims 2, 15, 28, 42, 56, and 70

[2/15/28/42/56/70] “The cable TV device of claim [1/14/27/41/55/69], wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.”

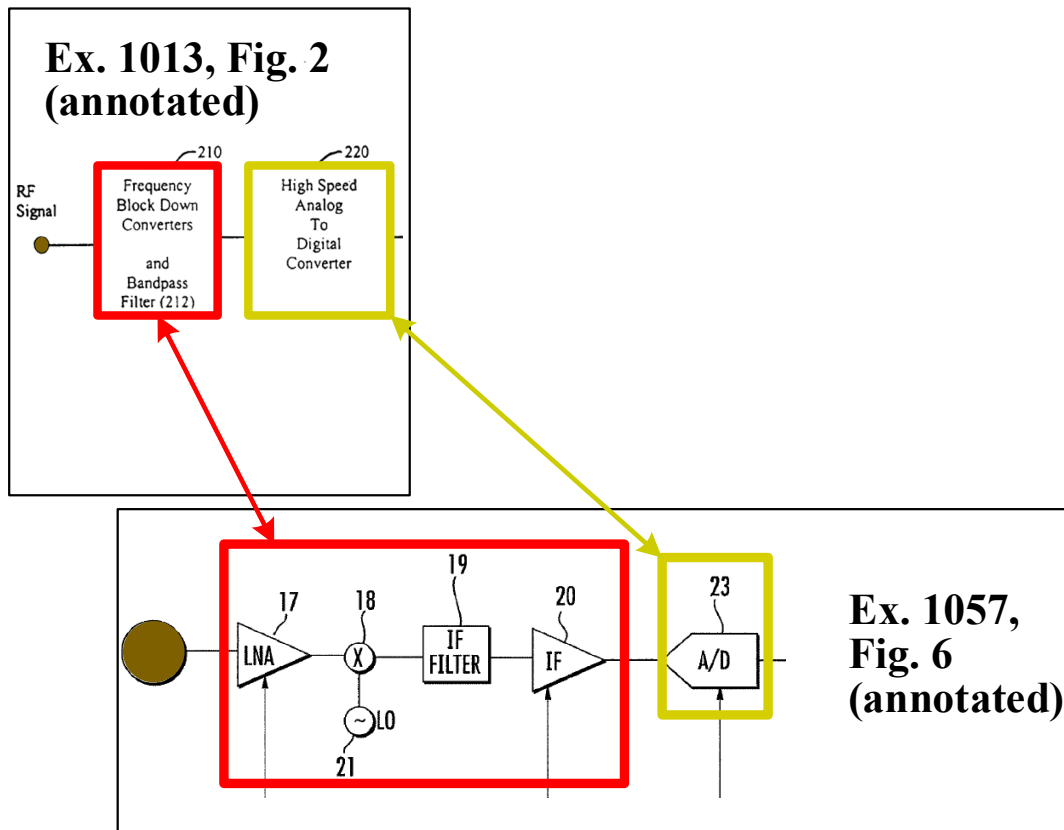
Both of Zhang's and Jackson's systems receive a RF input signal at a connection to a cable system, which a POSITA would have understood to be the claimed “cable network connector.” Ex. 1013, Fig. 2, [0023]; Ex. 1057, Fig. 6, [0006], [0023], [0025]; Ex. 1002, ¶¶ 225-226. As shown below, Jackson

additionally discloses an input connector 7b (**brown**) for connecting to the cable system (also a claimed “cable network connector.”) Ex. 1057, Fig. 4B, [0023], claims 1, 8, 12; Ex. 1002, ¶ 226.



Ex. 1057, Fig. 4B (annotated)

From this input, the RF signal is communicated in Jackson via an RF tuner (**red**) to the ADC (**gold**) as shown below, and the same would occur in Zhang-Jackson and Zhang-Reisman-Jackson. Both Zhang and Jackson disclose passing the signal through an analog bandpass filter (each a claimed “analog filter”). Ex. 1013, [0026], Fig. 2 (“Bandpass Filter 212”); Ex. 1057, [0027], Fig. 7; Ex. 1002, ¶ 227. Jackson additionally discloses that the path through the tuner may include an analog IF filter 19 (also a claimed “analog filter”) and analog amplifiers (e.g., low noise amplifier 17, IF amplifier 20) (each a claimed “analog amplifier”). Ex. 1057, [0025], [0027]; Ex. 1002, ¶ 227.



A POSITA would have been motivated to implement Zhang's RF input (brown) using Jackson's input connector (brown) because it would enable an installer to easily couple the receiver to the cable system. Ex. 1002, ¶ 228; Ex. 1057, [0023], Fig. 4b (connector 7b), claims 7-8. The combination represents a simple substitution of one known element (Jackson's input connector) for another (Zhang's RF input) to obtain a predictable result. Ex. 1002, ¶ 228. A POSITA would have had a reasonable expectation of success leading to a predictable result, because such connectors were ubiquitous in conventional CATV systems that utilize coaxial cable to connect to receiver systems, such as the STBs disclosed in Jackson and Zhang.

Ex. 1057, [0002]-[0004], [0019]-[0020], [0023], claim 8; Ex. 1013, [0005], [0015], [0045], 0048]; Ex. 1002, ¶ 228.

Further, while Zhang discloses that its Frequency Block Down Converter 210 comprises a Bandpass Filter 212, it is silent regarding other aspects of converter 210's implementation. However, a POSITA would have been motivated to implement Zhang's converter 210 with Jackson's analog amplifiers and analog filters because they would improve the performance of the system. Ex. 1002, ¶ 229; Ex. 1057, [0025], [0027]. Amplifiers boost the power and enable automatic gain control of the RF input signal, which is beneficial for obtaining the highest possible performance. Ex. 1057, [0025]; Ex. 1034, pp. 40-41; Ex. 1002, ¶¶ 64, 229. A POSITA would have further understood that Jackson's analog filters beneficially suppress unwanted signals to prevent interference with desired channels. Ex. 1057, [0025]; Ex. 1034, pp. 40-41; Ex. 1002, ¶ 229. Thus, the combination represents the use of a known technique (using Jackson's analog amplifiers and filters for amplification, gain control and filtering of unwanted signals in a front-end down converter) to improve a similar device (Zhang's Frequency Block Down Converter 210 that performs the same function as Jackson's front end tuner) in a similar way. *Id.*, ¶ 229.

A POSITA would have had a reasonable expectation of success because Jackson's receiver components were well known to a POSITA, because the basic

architecture of Jackson's receiver matches Zhang's receiver, and because these components from Jackson would perform the same functions in Zhang and Zhang-Reisman as they perform in Jackson. *Id.*, ¶ 230.

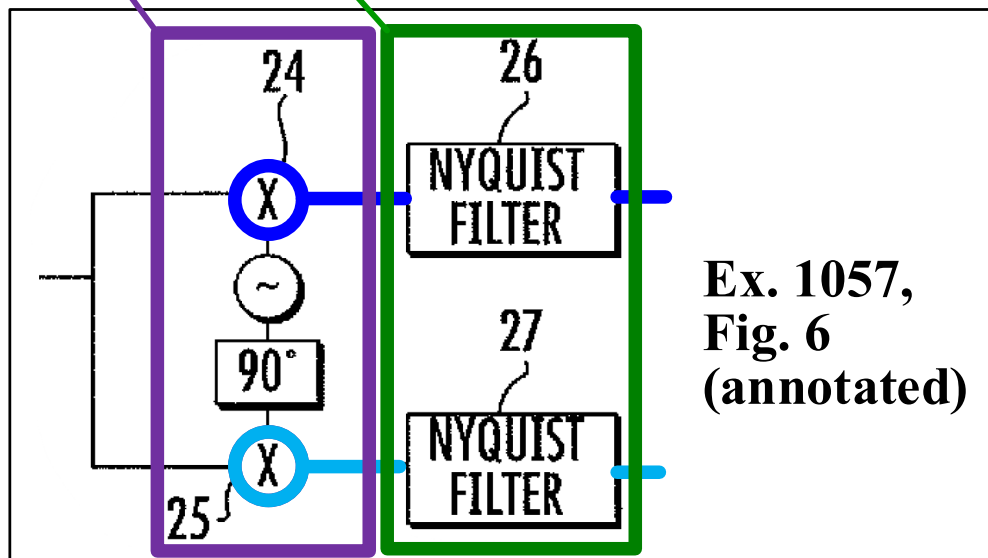
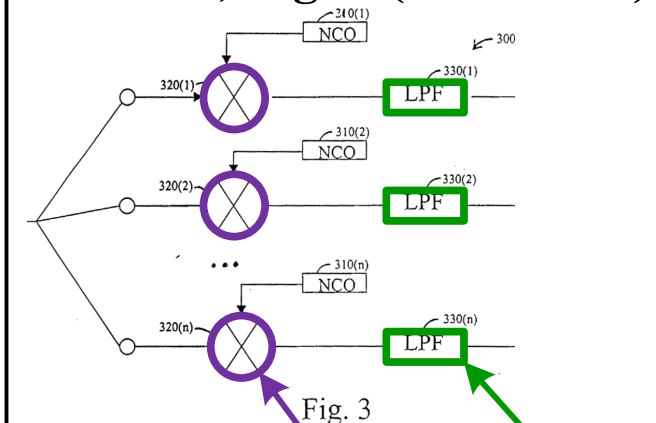
Thus, Zhang-Jackson renders obvious claims 2, 15, 28, and 42, and Zhang-Reisman-Jackson renders obvious claims 28, 42, 56, and 70. *Id.*, ¶ 231.

2. Dependent Claims 3, 4, 16, 17, 29, 30, 43, 44, 57, 58, 71, 72

As described above (Section VII.A.11), Zhang, discloses complex multipliers 320(1)-320(n) and filters 330(1)-330(n) that downconvert and output I and Q components of the desired channels at baseband, and thus Zhang anticipates and renders obvious claims 3, 4, 16, 17, 29, 30, 43, and 44, and Zhang-Reisman renders obvious claims, 57, 58, 71, and 72. *See* Sections VII.A.11, VII.B.8; Ex. 1002, ¶ 232.

To the extent Zhang's complex mixers do not teach I and Q outputs, Jackson discloses these. Ex. 1002, ¶ 233. Jackson discloses the structure of a complex mixer, which includes two real multipliers 24 and 25 (referred to as a "QAM demodulator") that generate quadrature (Q) (**dark blue**) and in-phase (I) (**light blue**) components, respectively. Ex. 1057, [0025], Fig. 6; Ex. 1039, pp. 11; Ex. 1018, pp. 133-134, Figs. 2-3 (illustrating "complex mixer[s]"); Ex. 1002, ¶¶ 65-67, 233.

Ex. 1013, Fig. 3 (annotated)



A POSITA reading Zhang’s teachings of a “complex multiplier” outputting a baseband signal would have found it obvious to turn to a known implementation, such as in Jackson (e.g., Jackson’s Figure 6), to implement this device. Ex. 1013, Figs. 2-3, [0025]-[0031], [0045]; Ex. 1002, ¶¶ 234-235. This would have been nothing more than a simple substitution of one known element (Jackson’s multipliers 24 and 25) for another (Zhang’s complex multiplier that outputs a baseband signal)

to obtain a predictable result (the mixer generates I and Q signals of desired channels at baseband, allowing the filtering of undesired channels). Ex. 1002, ¶ 235.

A POSITA would have further been motivated to implement Zhang's complex multipliers (purple) as taught by Jackson because doing so would enable Zhang's system to demodulate QAM modulated signals Ex. 1057, [0025]; Ex. 1002, ¶ 236. A POSITA would have further recognized the use of Jackson's I and Q components would enable Zhang's receiver to more effectively address known problems of mixers superimposing images of undesired signals over down-converted desired signals. Ex. 1018, p. 133-134; Ex. 1002, ¶¶ 65-66, 236. The Zhang-Jackson combination represents the use of a known technique (using Jackson's two real mixers 24 and 25 to implement a complex mixer with I and Q outputs) to improve a similar device (Zhang's complex multiplier) in the same way as taught in Jackson. Ex. 1002, ¶ 236.

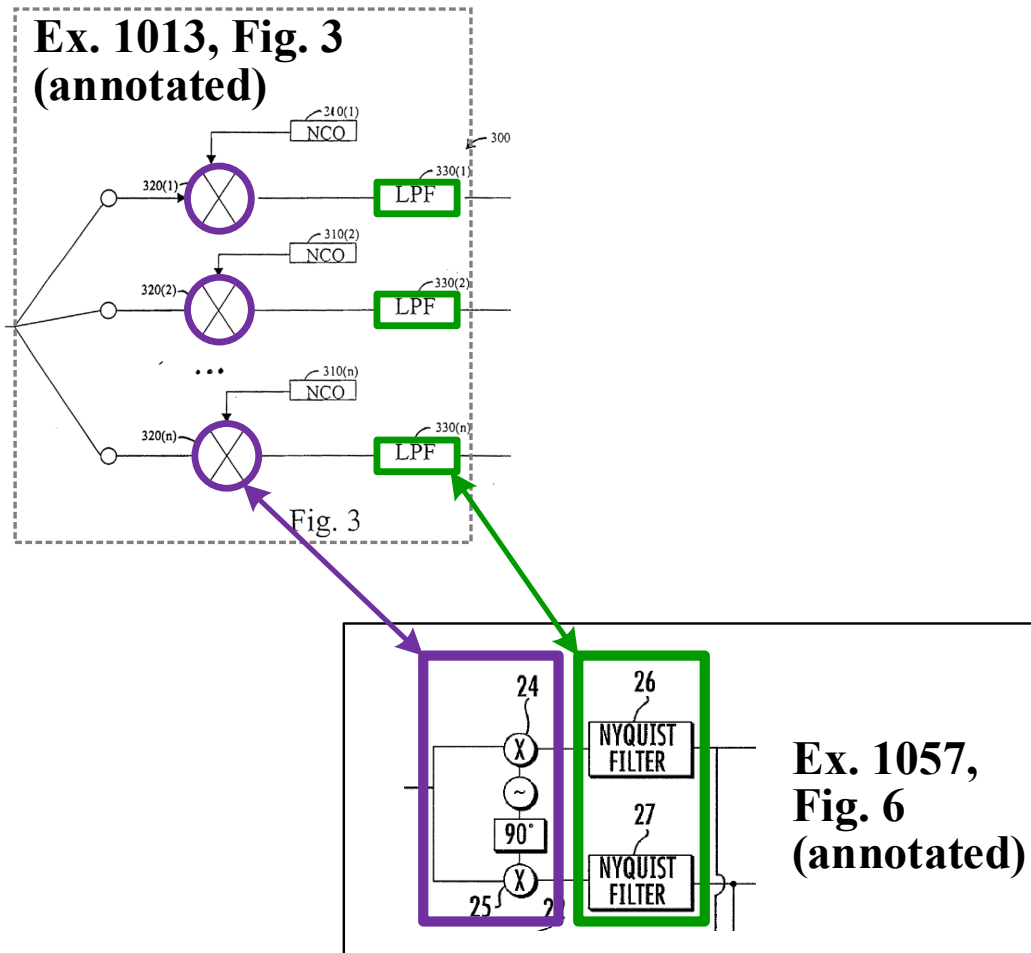
Jackson's receiver used typical components of a complex mixer that were well known to a POSITA, and its implementation in Zhang was well within the POSITA's skillset, leading to an expectation of success. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, pp. 65-76; Ex. 1018, p. 133-134, Fig. 3; Ex. 1002, ¶ 237. Indeed, the implementation of Jackson's receiver was taught in basic textbooks. *See e.g.*, Ex. 1025, pp. 279-280; Ex. 1034, pp. 65-75; Ex. 1018, pp. 134-139, Figs. 1-3, 6, 7, 9, 10; Ex. 1002, ¶ 237.

Thus, Zhang-Jackson (ground D) renders obvious claims 3, 4, 16, 17, 29, 30, 43, and 44, and Zhang-Reisman-Jackson (ground E) renders obvious claims 57, 58, 71, and 72. Ex. 1002, ¶ 238.

3. Dependent Claims 5, 18, 31, 45, 59, 73

As described above (Section VII.A.12), Zhang discloses filters 330(1)-330(n) that select 6MHz complex signals from the complex multiplier, and thus Zhang anticipates and renders obvious claims 5, 18, 31, and 45 (grounds A and B), and Zhang-Reisman renders obvious claims, 59 and 73 (ground C). *See* Sections VII.A.12, VII.B.8; Ex. 1002, ¶ 239.

To the extent Zhang's filters do not teach filtering 6MHz complex signals, Jackson discloses these. Jackson's Nyquist filters 26/27 (**green**) filter the complex signal output from the complex mixer to isolate the complex signal of a selected 6 MHz channel at baseband and filter out unwanted channels. Ex. 1013, Fig. 3, [0032]; Ex. 1057, Fig. 6, [0002], [0025]-[0026]; Ex. 1002, ¶¶ 240-242.



A POSITA would have been motivated to implement Zhang's filters 330 (green) with Jackson's filters 26/27 (green) to isolate the I and Q components of Zhang's 6 MHz selected channels. Ex. 1002, ¶ 243; Ex. 1013, [0006], [0012], [0025], [0030]-[0032]; Ex. 1057, [0002], [0025], Fig. 3. As illustrated in the comparative figure above, these modifications simply involve the one-to-one replacement of Zhang's components with Jackson's components that perform the exact same function, and thus, the combination is nothing more than a simple substitution of one known element (Jackson's filters) for another (Zhang's filters) to

obtain a predictable result (filtering 6MHz channels). Ex. 1002, ¶ 244. These filters were common and well-known to a POSITA and their implementation was well within the skillset of the POSITA, leading to an expectation of success. Ex. 1025, pp. 279-280; Ex. 1034, pp. 65-75; Ex. 1018, pp. 134-139, Figs. 1-3, 6, 7, 9, 10; Ex. 1002, ¶ 244.

Thus, Zhang-Jackson (ground D) renders obvious claims 5, 18, 31, and 45, and Zhang-Reisman-Jackson (ground E) renders obvious claims 31, 45, 59 and 73. Ex. 1002, ¶ 245.

4. Dependent Claims 6, 19, 32, 46, 60, 74

As described above (Section VII.A.13), Zhang anticipates and renders obvious claims 6, 19, 32, and 46 (grounds A and B), and Zhang-Reisman renders obvious claims, 60, and 74 (ground C). *See* Sections VII.A.13, VII.B.8; Ex. 1002, ¶ 246.

To the extent Zhang does not disclose demodulators that demodulate a complex signal, Jackson does. Jackson teaches an analogous demodulator (**orange**) that demodulates the complex signal separated into I and Q components to provide a demodulated channel as an MPEG-2 transport stream. Ex. 1057, [0025]; Ex. 1002, ¶ 247.

A POSITA reading Zhang's express teachings of a "demodulator" that received the output of a complex multiplier would have been motivated to turn to a

known implementation for use as Zhang's demodulator, such as taught by Jackson (e.g., as depicted in Jackson's Figure 6), because Jackson expressly shows its demodulator receiving and demodulating I and Q components of a complex signal to recover demodulated digital data. Ex. 1013, Figs. 2-3, [0028]-[0031], [0038]-[0039], [0047], claims 2, 4-5; Ex. 1057, [0024]-[0025], Figs. 5-6; Ex. 1002, ¶¶ 248-249. This simply involves implementing Zhang's demodulator according to Jackson's teaching of a demodulator that performs the same function, and thus, the combination represents a simple substitution of one known element (Jackson's demodulator) for another (Zhang's demodulator) to obtain a predictable result (demodulation of the Q and I signals). Ex. 1002, ¶ 248.

Jackson's demodulator used components that were well-known to a POSITA, and their implementation was within the skillset of the POSITA and requires little change to Zhang's architecture, leading to an expectation of success. Ex. 1025, pp. 279-280; Ex. 1034, pp. 65-75; Ex. 1018, pp. 134-139, Figs. 1-3, 6, 7, 9, 10; Ex. 1002, ¶ 249.

Thus, Zhang-Jackson (ground D) renders obvious claims 6, 19, 32, and 46, and Zhang-Reisman-Jackson (ground E) renders obvious claims 32, 46, 60 and 74. Ex. 1002, ¶ 250.

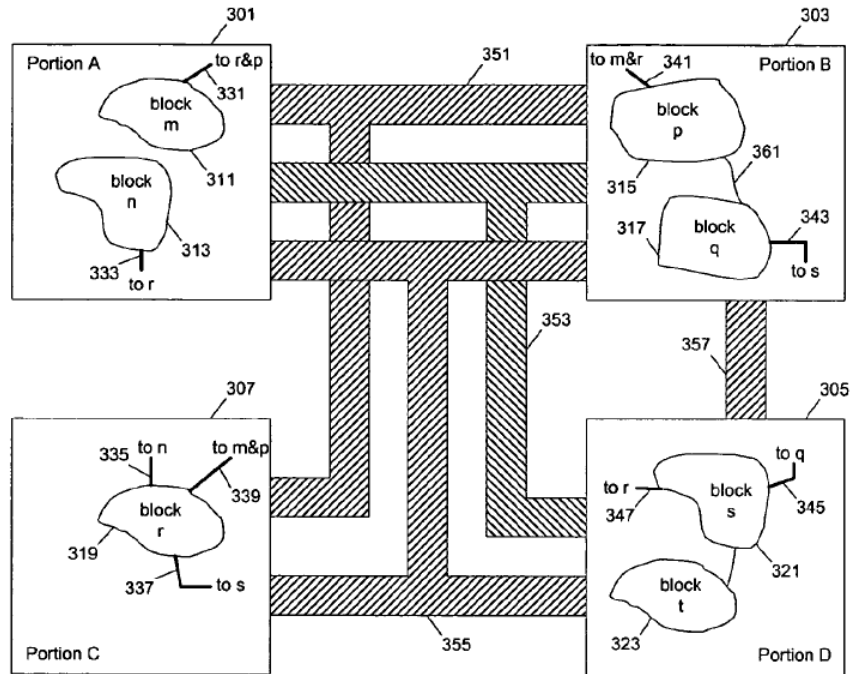
D. Ground F: Zhang-Pandey, and Ground G: Zhang-Reisman-Pandey

Zhang-Pandey (ground F) renders obvious claims 1, 3-9, 11, 13, 14, 16-22, 24, 26, 34-36, 48-50, and Zhang-Reisman-Pandey (ground G) renders obvious claims 10-12, 23-25, 34-36, 48-50, 62-64, 76-78. Ex. 1002, ¶ 251.

1. Claims 1, 3-7, 9-14, 16-20, 22-26, 35-36, 49-50, 63-64, 77-78

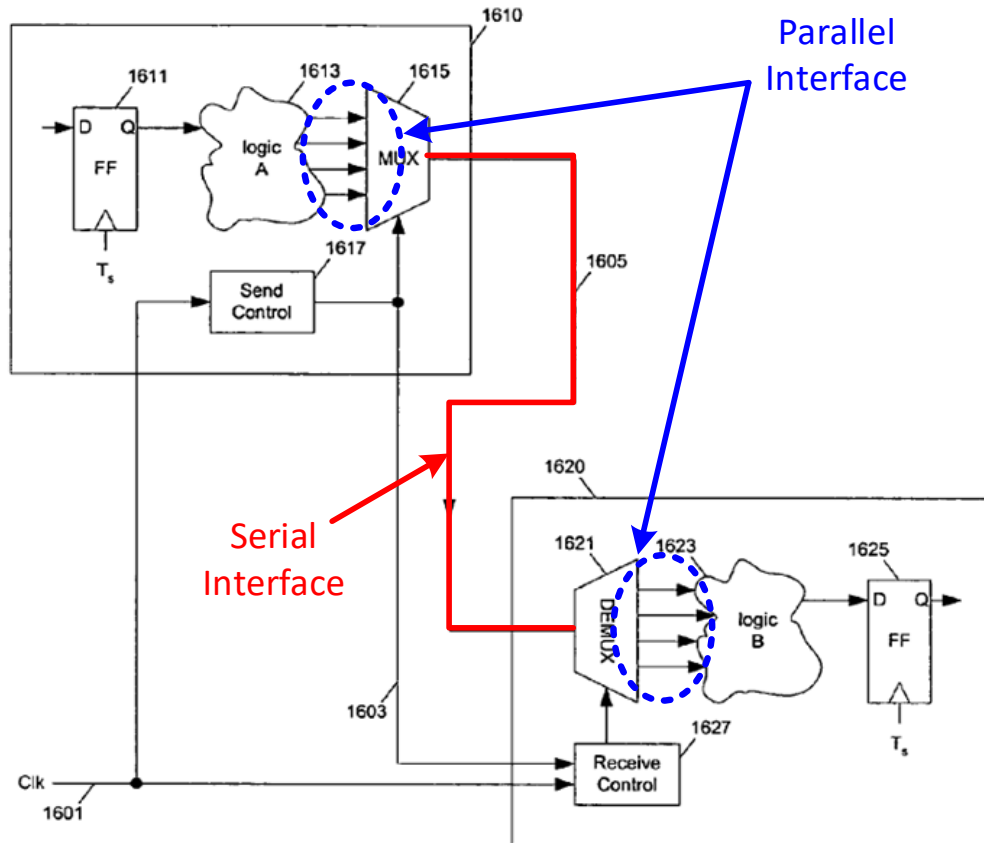
As discussed above, Zhang discloses the serial interface of claims 1, 14, 36, 50, 64, and 78 (and claims 3-7, 9-13, 16-20, and 22-26, which depend from claim 1 or 14), and the claimed “parallel interface” of claims 35, 49, 63, and 77. *See* Sections VII.A.1-2, VII.A.5-10, VII.B.4-8. While Zhang teaches these serial and parallel interfaces, so does Pandey. Ex. 1002, ¶ 252.

Pandey teaches a computer-aided technique for implementing a digital circuit design (e.g., such as Zhang’s digital circuitry) on a FPGA or ASIC chip. Ex. 1014, Abstract, 1:15-55, 2:4-12; Ex. 1002, ¶ 253. The process partitions functional blocks (such as Zhang’s demultiplexer 230, selector 240, and demodulators 250) into different regions of an integrated circuit chip (e.g., 301, 303, 305, 307) and assigns traces (conducting pathways) (e.g., 351, 353, 355, 357) to interconnect the partitioned blocks. Ex. 1014, 1:56-60, 2:6-12, 2:64-3:27, 6:10-15, 11:6-19, 13:33-14:7. Ex. 1002, ¶ 253.



Ex. 1014, Fig. 3

Pandey recognizes that the number of signals between blocks may exceed the number of traces available inside a chip, and that in such cases, multiple signals must be time-multiplexed (i.e. transmitted serially) over a single trace. Ex. 1014, 10:24-53, 10:58-11:5, 29:44-58, 30:31-42; Ex. 1002, ¶ 254. For example, as shown below, logic blocks A 1613 and B 1623 in separate partitions include a plurality of parallel signals to be transmitted from one to the other, i.e., via parallel interfaces (**blue**). Ex. 1014, 30:31-52, Fig. 37; Ex. 1002, ¶ 254. Multiplexer 1615 time multiplexes the signals from the parallel interface of 1613 onto a single trace (serial interface) (**red**), and then demultiplexer 1621 demultiplexes the signals back to the parallel interface of logic block B 1623. Ex. 1014, 30:31-52, Fig. 37; Ex. 1002, ¶ 254.

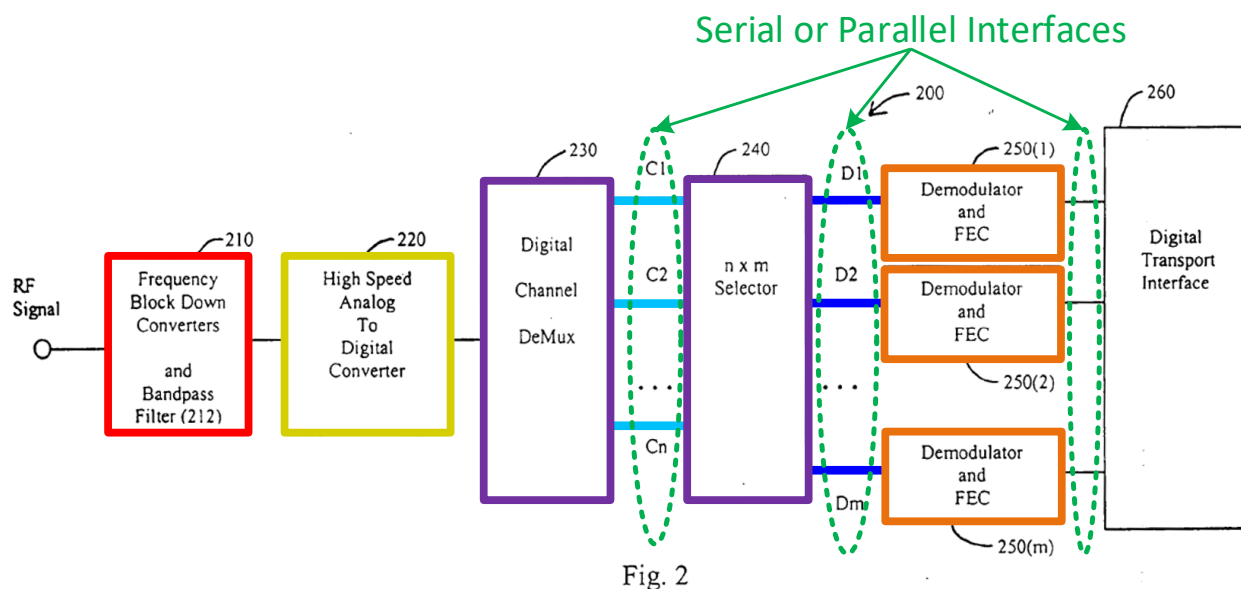


Ex. 1014, Fig. 37 (annotated)

Pandey's process partitions the blocks based on reducing the multiplexing ratio of wires to signals required between partitions. Ex. 1014, 5:50-53, 6:11-15, 6:44-53, 7:13-19, 29:44-30:9, 30:53-31:12, 31:56-63, Figs. 38-39; Ex. 1002, ¶ 255. Depending upon the circuit design and constraints of a chip, Pandey's optimization will in some layouts produces signals having individual dedicated traces with no multiplexing, resulting in only parallel interfaces between partitions, and in other layouts, produce signals between the partitions that are converted from a parallel interface, to a serial interface, and back to a parallel interface. Ex. 1014, 31:20-22, 32:12-15; Ex. 1002, ¶ 255. Thus, Pandey teaches both serial and parallel interfaces

for signals between digital functional blocks, with the implementation depending on upon the designer's selection of a particular integrated chip and the size of the circuit design (e.g., the number of channels to demodulate). Ex. 1014, 11:6-19, 13:33-55, 31:20-22, 32:12-15, Figs 2-3; Ex. 1002, ¶ 255.

It would have been obvious to apply Pandey's dedicated (i.e., parallel) and/or time-multiplexed (i.e., serial) interconnections to the interconnection between Zhang's demultiplexer 230, digital selector 240, demodulators 250, and/or digital transport interface 260 as shown below. Ex. 1002, ¶ 256.



Ex. 1013, Fig. 2 (annotated)

Zhang teaches optimizing the real estate needed for implementing the digital portion of its system on a single chip, and a POSITA would have looked to Pandey because it provides such optimization (using serial and parallel interfaces). Ex. 1013, [0029], [0037], [0044], [0047]-[0048]; Ex. 1014, 1:20-2:12, 6:10-15; Ex.

1002, ¶ 257. A designer, implementing Zhang's circuit using Pandey's process will decide on the number of RF channels to demodulate, and thus the number of functional blocks and traces (e.g. complex multipliers, filters) to be implemented. Ex. 1013, [0028]-[0030], [0040], [0042]. Ex. 1002, ¶ 257. A designer implementing a larger circuit design to demodulate a large number of RF channels would predictably lead to insufficient trace resources, resulting in Pandey's optimization inserting serial interfaces in between parallel interfaces of Zhang's digital blocks as shown in Pandey's Figure 37 above. Ex. 1014, 31:15-22, 32:7-15; Ex. 1002, ¶ 257. A designer implementing a smaller circuit for a small number of RF channels would predictably result in Pandey's optimization assigning each signal to its own trace, thus producing only parallel interfaces between Zhang's digital blocks. *Id.*

As such, using Pandey's parallel and/or serial interfaces between Zhang's digital demultiplexer 230, digital selector 240, demodulators 250, and/or digital transport interface 260 is nothing more than a combination of prior art elements (Zhang's circuit design and Pandey's parallel and serial interfaces between blocks) according to known methods (Pandey's optimization of chip layout and interconnection) to yield predictable results (data is transmitted effectively using serial and parallel interfaces). Ex. 1002, ¶ 258.

A POSITA would have had a reasonable expectation of success because Pandey's optimization utilized processes such as floor planning, partitioning, and

trace routing that were well within a POSITA's skillset. Ex. 1014, 1:20-2:38; Ex. 1002, ¶ 259.

Thus, claims 1, 3-7, 9, 11, 13-14, 16-20, 22, 24, 26, 35-36, and 49-50 are obvious over Zhang-Pandey, and claims 10-12, 23-25, 35-36, 49-50, 63-64, and 77-78 are obvious over Zhang-Reisman-Pandey. *See* Sections VII.A.1-2, 5-13, VII.B.4-8; Ex. 1002, ¶ 260.

2. Dependent Claims 8, 21, 34, 48, 62, 76

[8/34/62] “The cable TV device of claim [7/33/61], wherein: ‘the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.’”

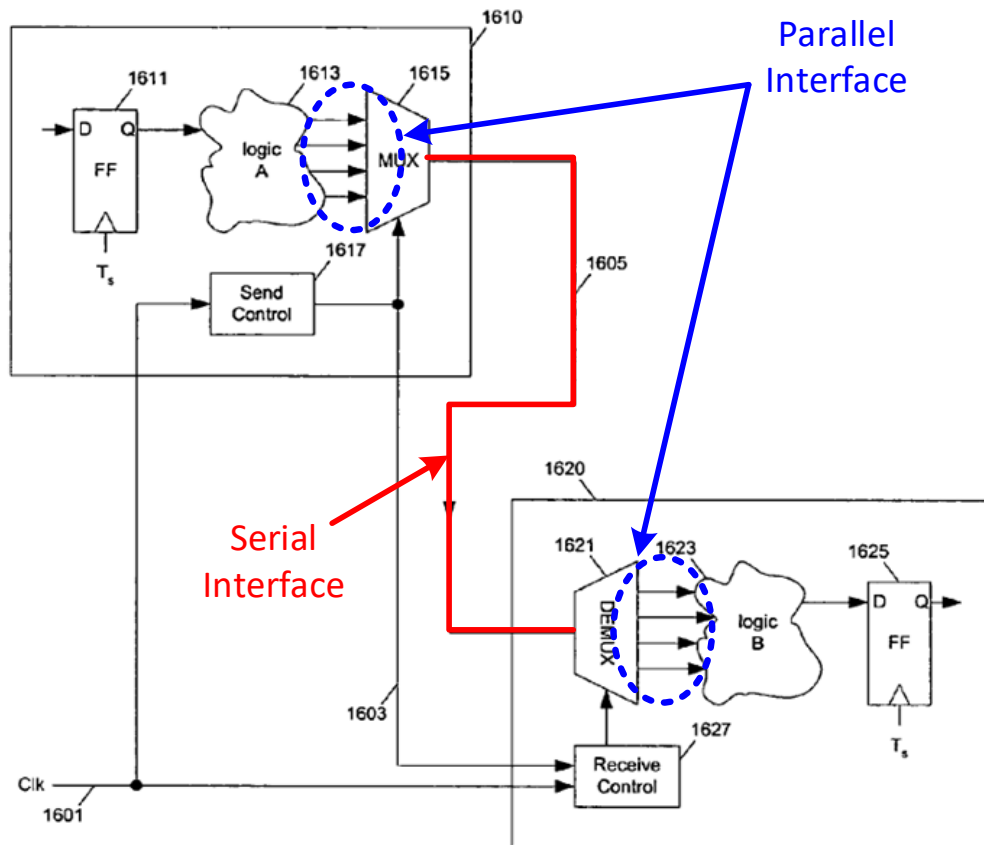
[21/48/76] “The cable TV device of claim [20/47/75], wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.”

As discussed above with respect to claims 7, 20, 33, 47, 61, and 75, Zhang teaches providing the demodulated channels at the output of Demodulators 250(1)-250(m), and as discussed in the previous section, Zhang-Pandey teaches that Zhang's Demodulator outputs be implemented with parallel interfaces.⁶ *See* Sections VII.A.10, VII.B.8, VII.D.1; Ex. 1002, ¶ 261. Thus, Zhang-Pandey teaches claims 8, 21, 34, and 48, and Zhang-Reisman-Pandey teaches claims 34, 48, 62, and

⁶ Petitioner does not concede these claims are properly supported under pre-AIA 35 U.S.C. 112, ¶ 1.

78, for the same reasons discussed above for their base claims 7, 20, 33, 47, 61, and 75, and further based on the additional teachings of Pandey as discussed above. *See* Section VII.A.10, VII.B.8, VII.D.1; Ex. 1002, ¶ 261.

As discussed above (*see* Section VII.A.10), claims 7 and 20 (from which claims 8 and 21 depend) require each desired channel/digital channel output to be provided “via a serial interface,” and to the extent this requires a serial interface at the outputs of the demodulators, claims 8 and 21 would further require the demodulator outputs to also have a parallel interface. Ex. 1002, ¶¶ 261-262. As described in the previous section (VII.D.1), Zhang-Pandey teaches this, since as shown below, Pandey’s optimization inserts serial interfaces in between parallel interfaces of different partitions (e.g., between Zhang’s demodulators 250 and digital transport interface 260). *Id.* Thus, Zhang-Pandey render claims 8 and 20 obvious even if these claims are construed to provide demodulated channels via both serial and parallel interfaces. *Id.*



Ex. 1014, Fig. 37 (annotated)

E. Ground H: Zhang-Jackson-Pandey (Claims 2-6, 15-19)

In ground D, Jackson is cited for teaching certain features of claims 2-6 and 15-19, and in ground F, Pandey is cited for teaching serial and parallel interfaces of independent claims 1 and 14 from which claims 2-6 and 15-19 depend. *See* Sections VII.C, VII.D.1. As these features in combination with Zhang are independent from one another, it would have been obvious to combine them all and thus, the motivations to combine Zhang with Jackson and with Pandey are the same as discussed above with respect to grounds D and F. *See* Sections VII.C, VII.D; Ex. 1002, ¶ 263.

Claims 2-6 and 15-19 are thus taught by Zhang-Jackson-Pandey. Ex. 1002,
¶ 264.

VIII. GROUNDS FOR STANDING & FEE PAYMENT

Petitioner hereby certifies that the '866 patent is available for, and Petitioner is not barred or estopped from requesting, *inter partes* review challenging claims 1-82.

Pursuant to 37 C.F.R. § 42.103, the undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

IX. CONCLUSION

Inter partes review should be instituted and claims 1-82 canceled.

Dated: February 16, 2024

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,830, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,716 words as counted by the Word Count feature of Microsoft Word and 114 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: February 16, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of this Petition for *Inter Partes* Review in connection with U.S. Patent No. 11,381,866 and supporting evidence to be served via FedEx Priority Overnight on February 16, 2024, on the following:

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SUITE 3400
CHICAGO, IL 60661
UNITED STATES

Dated: February 16, 2024

By: /Frederic M. Meeker/

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CLAIM LISTING APPENDIX
U.S. Pat. No. 11,381,866

Designation	Claim Language
Claim 1	
[1A]	A cable television (TV) device comprising:
[1B]	a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and
[1C]	a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels, via a serial interface, without providing any of the plurality of undesired channels.
Claim 2	
2	The cable TV device of claim 1, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 3	

Designation	Claim Language
3	The cable TV device of claim 1, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 4	
4	The cable TV device of claim 3, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 5	
5	The cable TV device of claim 3, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.
Claim 6	
6	The cable TV device of claim 3, wherein:

Designation	Claim Language
	the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.
Claim 7	
7	The cable TV device of claim 1, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.
Claim 8	
8	The cable TV device of claim 7, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 9	
9	The cable TV device of claim 1, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 10	
10	The cable TV device of claim 1, wherein:

Designation Claim Language	
	the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 11	
11	The cable TV device of claim 1, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 12	
12	The cable TV device of claim 1, wherein: the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.
Claim 13	
13	The cable TV device of claim 1, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.
Claim 14	
[14A]	A cable TV device comprising:
[14B]	a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a plurality of desired channels and a plurality of undesired channels; and
[14C]	a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and

Designation	Claim Language
[14D]	wherein the plurality of digital down converters is operable to provide each digital channel output via a serial interface.
Claim 15	
15	The cable TV device of claim 14, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 16	
16	The cable TV device of claim 14, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 17	
17	The cable TV device of claim 16, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 18	
18	The cable TV device of claim 16, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.
Claim 19	
19	The cable TV device of claim 16, wherein:

Designation Claim Language	
	each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.
Claim 20	
20	The cable TV device of claim 14, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired channels, to provide a demodulated channel as the digital channel output.
Claim 21	
21	The cable TV device of claim 20, wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 22	
22	The cable TV device of claim 14, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 23	
23	The cable TV device of claim 14, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 24	
24	The cable TV device of claim 14, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 25	

Designation	Claim Language
25	The cable TV of claim 14, wherein: the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.
Claim 26	
26	The cable TV device of claim 14, wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.
Claim 27	
[27A]	A cable television (TV) device comprising:
[27B]	a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and
[27C]	a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels without providing any of the plurality of undesired channels, and
[27D]	wherein the cable TV device comprises a digital video recorder (DVR).
Claim 28	
28	The cable TV device of claim 27, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network

Designation	Claim Language
	connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 29	
29	The cable TV device of claim 27, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 30	
30	The cable TV device of claim 29, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 31	
31	The cable TV device of claim 29, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.
Claim 32	
32	The cable TV device of claim 29, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.
Claim 33	
33	The cable TV device of claim 27, wherein:

Designation Claim Language	
	the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.
Claim 34	
34	The cable TV device of claim 33, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 35	
35	The cable TV device of claim 27, wherein: the DFE is operable to provide the plurality of desired channels via a parallel interface.
Claim 36	
36	The cable TV device of claim 27, wherein: the DFE is operable to provide the plurality of desired channels via a serial interface.
Claim 37	
37	The cable TV device of claim 27, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 38	
38	The cable TV device of claim 27, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.

Designation Claim Language	
Claim 39	
39	The cable TV device of claim 27, wherein: the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.
Claim 40	
40	The cable TV device of claim 27, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.
Claim 41	
[41A]	A cable TV device comprising:
[41B]	a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a plurality of desired channels and a plurality of undesired channels; and
[41C]	a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and
[41D]	wherein the cable TV device comprises a digital video recorder (DVR).
Claim 42	
42	The cable TV device of claim 41, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network

Designation Claim Language	
	connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 43	
43	The cable TV device of claim 41, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 44	
44	The cable TV device of claim 43, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 45	
45	The cable TV device of claim 43, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.
Claim 46	
46	The cable TV device of claim 43, wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.
Claim 47	
47	The cable TV device of claim 41, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired

Designation	Claim Language
	channels, to provide a demodulated channel as the digital channel output.
Claim 48	
48	The cable TV device of claim 47, wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 49	
49	The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide a plurality of digital channel outputs, comprising each digital channel output, via a parallel interface.
Claim 50	
50	The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide each digital channel output via a serial interface.
Claim 51	
51	The cable TV device of claim 41, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 52	
52	The cable TV device of claim 41, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 53	

Designation	Claim Language
53	The cable TV of claim 41, wherein: the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.
Claim 54	
54	The cable TV device of claim 41, wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.
Claim 55	
[55A]	A cable television (TV) device comprising:
[55B]	a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and
[55C]	a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels without providing any of the plurality of undesired channels, and
[55D]	wherein the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.
Claim 56	
56	The cable TV device of claim 55, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network

Designation	Claim Language
	connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 57	
57	The cable TV device of claim 55, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 58	
58	The cable TV device of claim 57, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 59	
59	The cable TV device of claim 57, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.
Claim 60	
60	The cable TV device of claim 57, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.
Claim 61	
61	The cable TV device of claim 55, wherein:

Designation Claim Language	
	the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.
Claim 62	
62	The cable TV device of claim 61, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 63	
63	The cable TV device of claim 55, wherein: the DFE is operable to provide the plurality of desired channels via a parallel interface.
Claim 64	
64	The cable TV device of claim 55, wherein: the DFE is operable to provide the plurality of desired channels via a serial interface.
Claim 65	
65	The cable TV device of claim 55, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 66	
66	The cable TV device of claim 55, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.

Designation Claim Language	
Claim 67	
67	The cable TV device of claim 55, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 68	
68	The cable TV device of claim 55, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.
Claim 69	
[69A]	A cable TV device comprising:
[69B]	a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a plurality of desired channels and a plurality of undesired channels; and
[69C]	a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and
[69D]	wherein the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.
Claim 70	
70	The cable TV device of claim 69, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.

Designation Claim Language	
Claim 71	
71	The cable TV device of claim 69, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 72	
72	The cable TV device of claim 71, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 73	
73	The cable TV device of claim 71, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.
Claim 74	
74	The cable TV device of claim 71, wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.
Claim 75	
75	The cable TV device of claim 69, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired channels, to provide a demodulated channel as the digital channel output.
Claim 76	
76	The cable TV device of claim 75, wherein:

Designation Claim Language	
	the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 77	
77	The cable TV device of claim 69, wherein: the plurality of digital down converters is operable to provide a plurality of digital channel outputs, comprising each digital channel output, via a parallel interface.
Claim 78	
78	The cable TV device of claim 69, wherein: the plurality of digital down converters is operable to provide each digital channel output via a serial interface.
Claim 79	
79	The cable TV device of claim 69, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 80	
80	The cable TV device of claim 69, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 81	
81	The cable TV device of claim 69, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 82	
82	The cable TV device of claim 69, wherein:

Designation	Claim Language
	the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.