

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMCAST CABLE COMMUNICATIONS, LLC,
Petitioner,

v.

ENTROPIC COMMUNICATIONS, LLC.,
Patent Owner.

Patent No. 11,381,866
Filing Date: January 28, 2022
Issue Date: July 5, 2022
Title: CABLE TELEVISION DEVICE

Inter Partes Review No.: IPR2024-00436

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.*

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EXHIBITS

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- Ex. 1102: Expert Declaration of David B. Lett
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- Ex. 1104: Certified Prosecution History of the ’866 patent
- Exs. 1105-1106: Reserved
- Ex. 1107: Certified Prosecution History of U.S. Provisional App. No. 61/170,526 (“’526 provisional”)
- Ex. 1108: U.S. Pub. No. 2009/0290659 (“Petrovic”)
- Ex. 1109: Specification and drawings of U.S. Provisional App. No. 61/054,886 (“Petrovic ’886”)
- Ex. 1110: U.S.P.T.O Assignment Record for U.S. Application No. 12/414,892
- Exs. 1111-1113: Reserved
- Ex. 1114: U.S. Patent No. 7,237,214 (“Pandey”)
- Ex. 1115: Excerpts of “IEEE Std 100-2000, The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition” (IEEE Press. 2000) (“IEEE Std 100”)
- Ex. 1116: Excerpts of Jan M Rabaey, “Digital Integrated Circuits: A Design Perspective” (Pearson, 2nd ed. 2002) (“Rabaey”)
- Ex. 1117: A. P. Chandrakasan, “Ultra low power digital signal processing,” Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357 (“Chandrakasan”)
- Ex. 1118: S. Mirabbasi and K. Martin, “Classical and Modern Receiver Architectures,” IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000 (“Mirabbasi”)
- Ex. 1119: U.S. Patent No. 6,061,406 (“Carson”)

Ex. 1120:	Reserved
Ex. 1121:	“Data-Over-Cable Service Interface Specifications: Radio Frequency Interface Specification CM-SP-RFIV2.0-I11-060602,” DOCSIS, June 2006
Exs. 1122-1124	Reserved
Ex. 1125:	J. Crols and M. S. J. Steyaert, “Low-IF topologies for high-performance analog front ends of fully integrated receivers,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998 (“Crols”)
Ex. 1126:	Reserved
Ex. 1127:	U.S. Patents and Patent Applications Family Tree for U.S. Pat. No. 11,381,866
Exs. 1128-1132:	Reserved
Ex. 1133:	Excerpts of W. Ciciora, J. Farmer, D. Large, and M. Adams, “Modern Cable Television Technology: Video, Voice, and Data Communications” (2 nd ed. 2004) (“Ciciora”)
Ex. 1134:	Excerpts of J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design” (1997)
Ex. 1135:	U.S. Patent No. 7,340,230 (“Khoini-Poorfard”)
Ex. 1136:	U.S. Pub. No. 2003/0217362 (“Summers”)
Ex. 1137:	U.S. Pub. No. 2006/0256799 (“Eng”)
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Ex. 1139:	Excerpts of Chris Bowick, “RF Circuit Design” (2 nd ed. 2008)
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Ex. 1141:	Excerpts of Roland Priemer, “Introductory Signal Processing” (1991)
Ex. 1142:	U.S. Patent No. 7,272,375 (“Tuttle”)

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Ex. 1144:	U.S. Patent No. 5,278,837 (“Kelley”)
Ex. 1145:	Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering” (2002)
Ex. 1146:	U.S. Patent No. 7,213,042 (“Cannon”)
Ex. 1147:	Reserved
Ex. 1148:	Excerpts of William Buchanan, “Computer Busses” (2000)
Ex. 1149:	U.S. Patent No. 7,079,528 (“Ziegler”)
Ex. 1150:	Excerpts of “Software Defined Radio: Enabling Technologies” (Walter H.W. Tuttlebee ed., 2003)
Exs. 1151-1152:	Reserved
Ex. 1153:	U.S. Pub. No. 2008/0039036 (“Lee”)
Exs. 1154-1157:	Reserved
Ex. 1158:	U.S. Pub. No. 2010/0020794 (“Cholas”)
Ex. 1159:	U.S. Pub. No. 2007/0232088 (“Burris”)
Ex. 1160:	U.S. Patent No. 6,160,443 (“Maalej”)
Ex. 1161:	U.S. Pub. No. 2006/0256216 (“Takahiko”)
Exs. 1162-1169	Reserved
Ex. 1170:	U.S.P.T.O Assignment Record for U.S. Patent No. 8,526,898
Ex. 1171-1172:	Reserved
Ex. 1173:	Expert Declaration of Dr. Sylvia Hall-Ellis
Ex. 1174:	Reserved
Ex. 1175:	U.S. Patent No. 6,791,995 (“Azenkot”)
Ex. 1176:	U.S. Patent No. 6,542,203 (“Shadwell”)

MANDATORY NOTICES

Real Parties in Interest (37 C.F.R. § 42.8(b)(1))

The real parties-in-interest for this petition are (i) Comcast Corporation, (ii) Comcast Cable Communications, LLC, and (iii) Comcast Cable Communications Management, LLC. No unnamed entity is funding, controlling, or directing this Petition for *inter partes* review (IPR) of U.S. Patent No. 11,381,866 (“the ’866 patent”), or otherwise has an opportunity to control or direct this Petition or Petitioner’s participation in any resulting IPR.

Related Matters (37 C.F.R. § 42.8(b)(2))

Office Proceedings

This is the second of three petitions for *inter partes* review filed by Petitioner against the ’866 patent. Petitioner is also filing petitions for *inter partes* review against related U.S. Patent Nos. 11,399,206 and 9,210,362.

No other Office proceedings (e.g., *inter partes* review, post-grant review, or covered business method) have been filed against the ’866 patent.

Litigation matters

The ’866 patent has been asserted in *Entropic Communications, LLC v. Comcast Corporation*, No. 2:23-cv-01050 (C.D. Cal. filed Feb. 10, 2023) and *Entropic Communications, LLC v. Cox Communications, Inc.*, No. 2-23-cv-01049 (C.D. Cal. filed Feb. 10, 2023). The ’866 patent was also asserted in *Entropic*

Communications, LLC v. Charter Communications, Inc., No. 2:22-cv-00052-JRG (E.D. Tex. filed Apr. 27, 2022), which case was dismissed on December 10, 2023.

Continuity

According to Office records, the '866 patent is a continuation of U.S. Pat. App. No. 17/217,244, filed March 30, 2021 (abandoned), which is a continuation of U.S. Pat. App. No. 16/430,506, filed June 4, 2019 (issued as U.S. Pat. No. 10,972,781), which is a continuation of U.S. Pat. App. No. 15/792,318, filed October 24, 2017 (issued as U.S. Pat. No. 10,313,733), which is a continuation of U.S. Pat. App. No. 14/948,881, filed November 23, 2015 (issued as U.S. Pat. No. 9,819,992), which is a continuation of U.S. Pat. App. No. 14/617,973, filed February 10, 2015 (issued as U.S. Pat. No. 9,210,363), which is a continuation of U.S. Pat. App. No. 13/962,871, filed August 8, 2013 (issued as U.S. Pat. No. 9,100,622), which is a continuation of U.S. Pat. App. No. 12/762,900, filed April 19, 2010 (issued as U.S. Pat. No. 8,526,898), which claims the benefit of U.S. Provisional App. No. 61/170,526, filed April 17, 2009. The '866 patent is part of a family that includes thirteen additional patents or applications that purport to claim priority, via a chain of continuation applications, from App. No. 12/762,900. A family tree is included as Ex. 1127.

Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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I. INTRODUCTION

Comcast Cable Communications, LLC (“Petitioner”) petitions for *inter partes* review of claims 1-82 of U.S. Patent No. 11,381,866 (“the ’866 patent”).

II. SUMMARY OF ARGUMENT

The ’866 patent generally claims a cable television (TV) device including a “wideband analog-to-digital converter (ADC)” for digitizing an input signal, which the ’866 patent admits “is similar to conventional tuners.” Ex. 1107, p. 5; Ex. 1101, 1:5-22. The alleged invention—digital circuitry for selecting desired channels from the input signal and filtering out undesired channels—is rendered obvious by the prior art, e.g., Cholas (Ex. 1158), Petrovic (Ex. 1108), and other references relied on herein. Claims 1-82 of the ’866 patent are unpatentable and should be cancelled.

III. OVERVIEW OF THE ’866 PATENT

A. Brief Description

The ’866 patent describes a wideband receiver system 200 (illustrated below) “capable of receiving multiple radio frequency channels located in a broad radio frequency spectrum.” Ex. 1101, 1:27-29. A receiver is “wideband” if it is “designed to concurrently receive several TV channels.” *Id.*, 1:35-38.

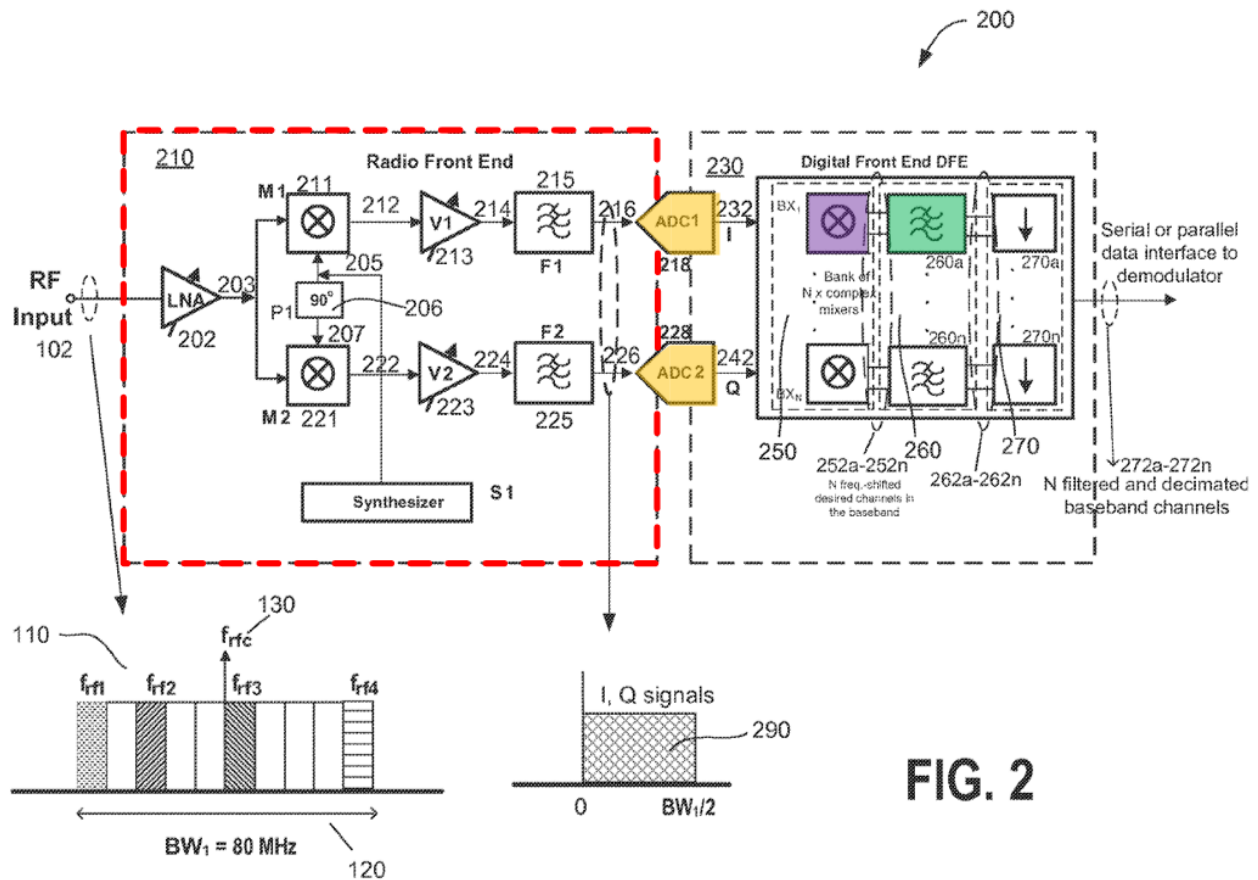


FIG. 2

Ex. 1101, Fig. 2 (annotated)

The system 200 receives desired and undesired television channels dispersed within a frequency bandwidth BW_1 . Ex. 1101, 4:35-51. A radio frontend 210 (**red**) downconverts the bandwidth as in-phase (I) and quadrature (Q) signals 212 and 222 at an intermediate frequency (IF), which are digitized by wideband analog-to-digital converters ADC1/ADC2 (**gold**). Ex. 1101, 2:59-65, 4:61-5:7, 5:20-24, 5:48-51. U.S. Provisional App. No. 61/170,526 (“526 provisional”), incorporated by reference, admits the left side of Figure 2 (including ADC1/ADC2) “is similar to conventional tuners.” *Id.*, 1:6-22; Ex. 1107, p. 5.

Digital I, Q signals 232, 242 from ADC1/ADC2 are input to a bank of N complex mixers 250 (**purple**) in digital front end 230. Ex. 1101, 5:51-55. “Each of the N complex mixers ... extract[s] a different one of the desired channels” from the I, Q signals and “frequency-shifts the extracted signals to the baseband frequency.” *Id.*, 1:6-22, 6:2-6. Filters 260a-260n (**green**) filter each frequency-shifted desired channel. *Id.*, 6:6-8. After (optional) decimation, baseband channels from multiple rows of digital front end 230 are “sent as a serial or parallel digital data stream to a demodulator using a serial or parallel data interface according to commonly known methods.” *Id.*, 7:10-14.

B. Prosecution History

U.S. Application No. 17/587,415, which became the '866 patent, was filed on January 28, 2022, with a preliminary amendment cancelling claims 1-18 and adding claims 19-48. Ex. 1104, pp. 2-109. The Office rejected claims 19-48 for non-statutory double patenting over claims 1-27 U.S. Patent No. 9,100,622, and rejected claims 19-27, 29, 30, 33-42, 44, 45, and 48 as obvious over U.S. Patent No. 6,760,342 (Skones et al.) in view of International Publication No. WO 02/087230 (Uskali et al.). *Id.*, pp. 119-132. The Office indicated that dependent claims 28 and 43 (reciting “a serial interface”), claims 31 and 46 (reciting a “DVR”), and claims 32 and 47 (reciting “a picture-in-picture display”) contained allowable subject matter. *Id.*, p. 131.

Applicant received a Notice of Allowance after it filed a terminal disclaimer and amended the claims based on the allowable subject matter. *Id.*, pp. 148-175. The '866 patent issued on July 5, 2022. Ex. 1101, cover.

C. Earliest Priority Date for the Claims

The earliest possible priority date for the claims 1-9, 13-22, and 26 of the '866 patent is April 17, 2009, the filing date of the '526 provisional. Each of the references relied on herein is prior art to that date. The earliest possible priority date for the remaining claims is April 19, 2010, the filing date of U.S. Pat. App. No. 12/762,900; the '526 provisional is silent regarding “DOCSIS[] protocol,” “DVR,” or “picture-in-picture display.” Ex. 1107, pp. 3-7.

IV. OVERVIEW OF PRIOR ART

A. Cholas

Cholas, a U.S. Patent Application Publication of U.S. Pat. App. No. 11/754,714, filed May 29, 2007, is pre-AIA 35 U.S.C. § 102(e) prior art. Ex. 1158, cover. Cholas describes a set-top box (STB) 1710 (**red**) with tuner/demodulator/demultiplexer chains 1-N that receive “input signal[s] [**blue**] ... from the cable network.” *Id.*, [0044], [0010]-[0011], [0024], [0059]-[0071], Figs. 4, 6; Ex. 1102, ¶¶ 77-78.

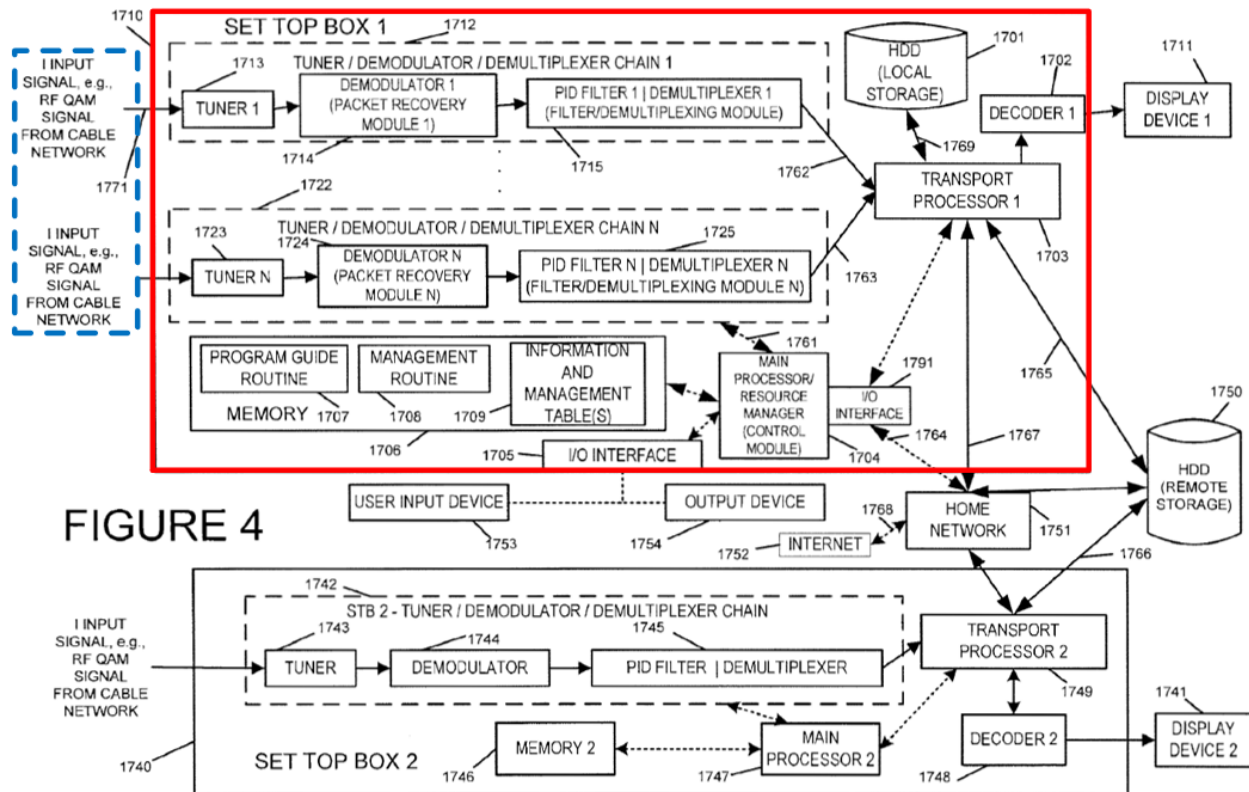


FIGURE 4

Ex. 1158, Fig. 4 (annotated)

Cholas is analogous art, as it is in the same field of endeavor as the '866 patent and reasonably pertinent to problems with which the '866 patent is concerned. Ex. 1102, ¶ 79. Like the '866 patent, Cholas “relates to wideband receiver systems that are capable of receiving multiple desired television channels.” Ex. 1101, 1:30-32; Ex. 1158, [0001], [0043]-[0045], [0052]-[0057], Figs. 4-5; Ex. 1102, ¶ 79. Cholas also relates to cable network STBs, an expected environment for the wideband receiver system of the '866 patent. Ex. 1101, 1:46-48, 5:8-12, claim 1; Ex. 1158, [0043]-[0045], Fig. 4; Ex. 1102, ¶ 79.

B. Petrovic

Petrovic is a U.S. Patent Application Publication of U.S. Pat. App. No. 12/414,892, filed March 31, 2009, that claims priority to and incorporates by reference U.S. Provisional Application 61/054,886 (“Petrovic ’886”).¹ Ex. 1108, cover, [0001]. Petrovic is pre-AIA 35 U.S.C. § 102(e) prior art, as explained below. Ex. 1102, ¶¶ 81, 88-89.

Petrovic, like the ’866 patent, describes a wideband receiver system that it calls a “channel stacking system” and that receives wideband RF signals 102-106. Ex. 1108, [0028]-[0029], Fig. 4; Ex. 1109, [0008], [0010]-[0013], [0016], [0023], [0026], Fig. 1; Ex. 1102, ¶¶ 82-83.

¹ The specification and drawings of Petrovic ’886, cited by paragraph and Figure numbers, are at pages 6-61 of Ex. 1109.

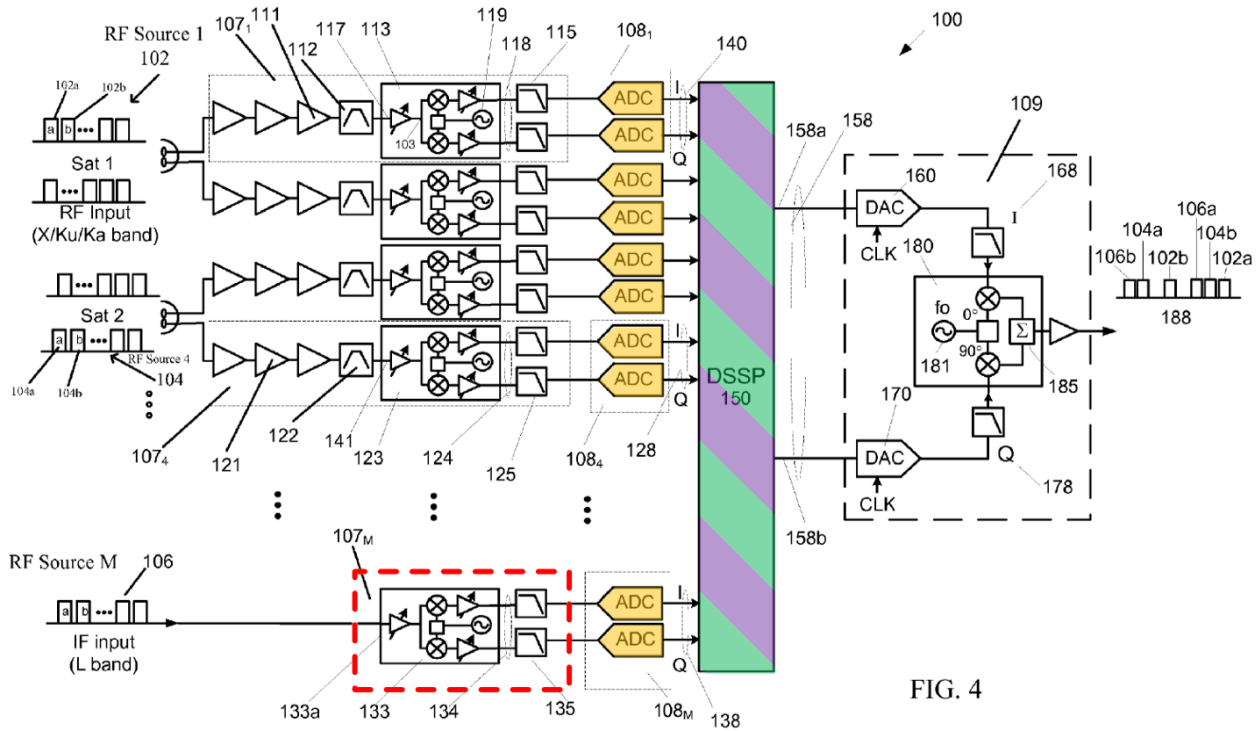


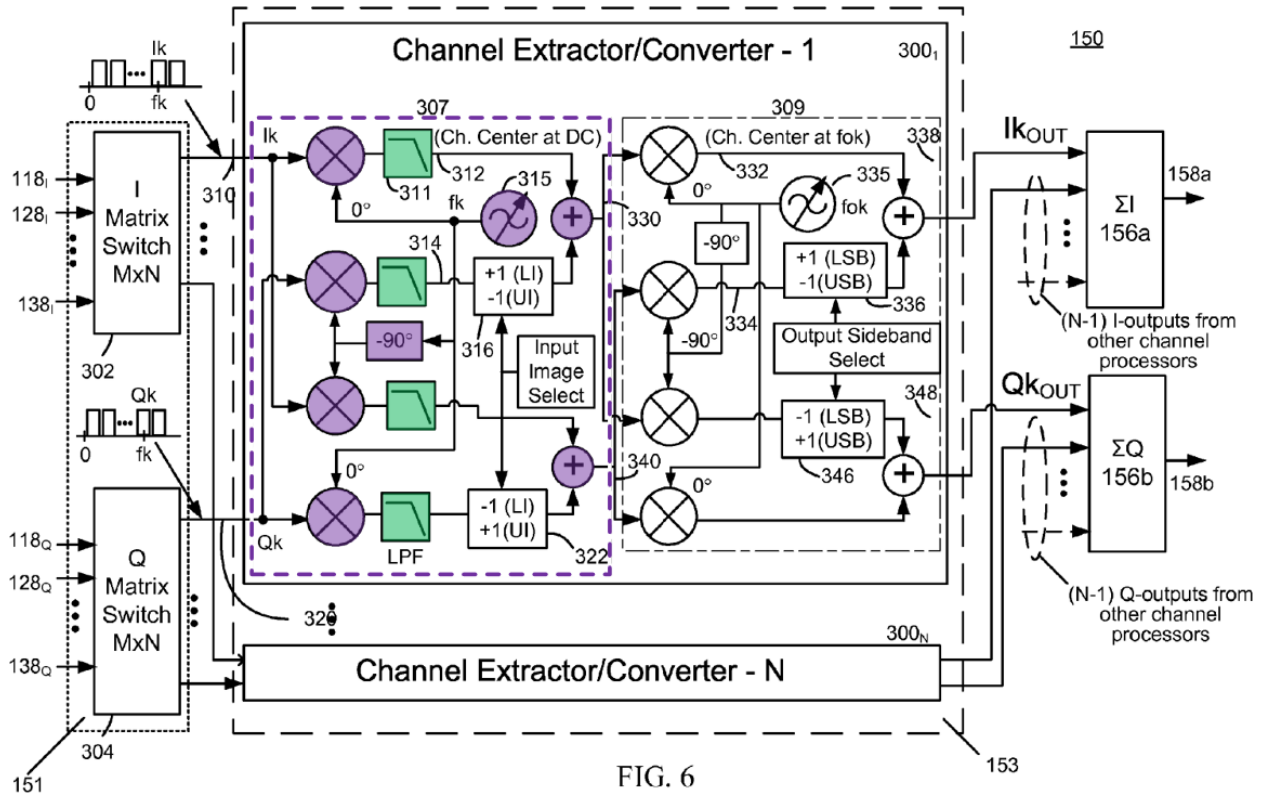
FIG. 4

Ex. 1108, Fig. 4 (annotated)

The signals 102-106 are coupled to “analog preprocessing and downconversion (APD) stages 107_{1-M} ” (one marked in **red**). Ex. 1108, [0032], Fig. 4; Ex. 1109, [0010], [0013], [0020], Fig. 1. Those APD stages downconvert RF signals into in-phase (I) and quadrature (Q) intermediate frequency (IF) signals that are, after filtering, digitized by analog-to-digital converters 108_{1-M} (**gold**). Ex. 1108, [0032]-[0039], [0050]-[0052], Figs. 4-6; Ex. 1109, [0010], [0013], [0018]-[0024], [0031]-[0032], Figs. 1-3A; Ex. 1102, ¶ 83.

Digital signal switching and pre-processing (DSSP) stage 150 (**green/purple**) receives the digitized signals and “extract[s] the channels of interest ... (i.e., remove[s] all the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig.

4; Ex. 1109, [0015], [0025], [0033], Fig. 1; Ex. 1102, ¶ 84. Figure 6 shows details of the DSSP 150, including “channel extractor/converter circuit 300.” Ex. 1108, [0058]; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 84.



Ex. 1108, Fig. 6 (annotated)

As in the '866 patent, a channel is extracted from the digitized I, Q signals corresponding to one of the RF sources 102-106 by downconverting those signals in a complex mixer (**purple** and/or **purple** broken-line box) of a stage 307 so the desired channel is at baseband, and filtering using low pass filters (LPFs) 311 (**green**), to create I, Q components 330, 340 for an extracted channel. Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1102 ¶¶ 85-86.

Petrovic, in the same field of endeavor as the '866 patent and reasonably pertinent to problems with which the '866 patent is concerned, is analogous art. Ex. 1102, ¶ 87. Petrovic describes a system and method for receiving wideband RF signals comprising multiple channels, as well as selecting individual channels (in the same way as the '866 patent) by conversion to baseband and filtering. *Id.*; Ex. 1108, Abstract, [0029]-[0030], [0042], [0047], [0050], [0058]-[0077], Figs. 4, 6; Ex. 1109, [0010]-[0011], [0013], [0015]-[0016], [0020], [0023], [0033], [0037]-[0054], Figs. 1, 3A; Ex. 1101, 6:16-7:9, Fig. 3.

1. Petrovic Priority Date

Petrovic is pre-AIA 35 U.S.C. § 102(e) prior art based on its March 31, 2009, filing date, and based on the May 21, 2008, filing date of Petrovic '886. At least claim 14 of Petrovic is supported by Petrovic '886. Ex. 1102, ¶¶ 88-89.

Petrovic – Claim 14 (Ex. 1108)	Petrovic '886 (Ex. 1109)
14. A method for assembling channels in a composite signal, the method comprising:	<i>E.g.</i> , [0001], [0004], [0008], claim 16.
a) downconverting, in a single frequency translation process, a first input signal comprising a first plurality of channels to a first IF signal comprising said plurality of first channels;	[0005], [0010], [0014], [0029], [0031]-[0032], claim 16, Figs. 1-2

Petrovic – Claim 14 (Ex. 1108)	Petrovic '886 (Ex. 1109)
b) converting the first IF signal into a first digital IF signal;	[0010], claim 16, Fig. 1
c) downconverting, in a single frequency translation process, a second input signal comprising a plurality of second channels to a second IF signal comprising said plurality of second channels;	[0005], [0013]-[0014], [0023], [0029], [0031]-[0032], claim 16, Figs. 1-2
d) converting the second IF signal into a second digital IF signal; and	[0005], [0013], [0024], claim 16, Fig.1
e) assembling, in the digital domain, at least one of the first channels and at least one of the second channels into a digital composite signal.	[0015], [0025], [0036]-[0068], [0080], claim 16, Figs. 3A-3B

Parallel citations to Petrovic and Petrovic '886 show relied-on disclosure is prior art as of the May 21, 2008, filing date of Petrovic '886.

2. Pre-AIA 35 U.S.C. § 103(c) Does Not Apply

Petrovic was assigned to Entropic Communications, Inc. until April 30, 2015. Ex. 1108, cover; Ex. 1110, pp. 3, 24. The claimed invention of the '866 patent was not, at the time made, owned by Entropic Communications, Inc. Ex. 1170, pp. 2-5.²

C. Burris

Burris, a U.S. Patent Application Publication published October 4, 2007, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1159, cover. Burris describes coaxial connector assemblies usable, e.g., for connection to ports on cable television devices. Ex. 1159, [0005]. Burris is analogous art because it relates to a claimed feature (“cable network connector”) and is reasonably pertinent to problems with which the '866 patent is concerned. Ex. 1159, [0005]; Ex. 1102, ¶ 90.

D. Maalej

Maalej, a U.S. Patent that issued December 12, 2000, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1160, cover. Maalej discloses a QAM demodulator for, e.g., demodulating 6 MHz CATV channels. Ex. 1160, 1:6-8, 1:28-33, 3:47-52; Ex. 1102, ¶ 91. Maalej is analogous art because it relates to a claimed feature (“demodulators”)

² Patent Owner has the burden under pre-AIA 35 U.S.C. § 103(c). *Global Tel*Link Corporation v. Securus Technologies, Inc.*, No. IPR2014-00825, Paper 36, 11-12 (PTAB Dec. 2, 2015).

and is reasonably pertinent to problems with which the '866 patent is concerned. Ex. 1160, 1:6-8, 1:28-32, 3:47-52; Ex. 1102, ¶ 91.

E. Rabaey

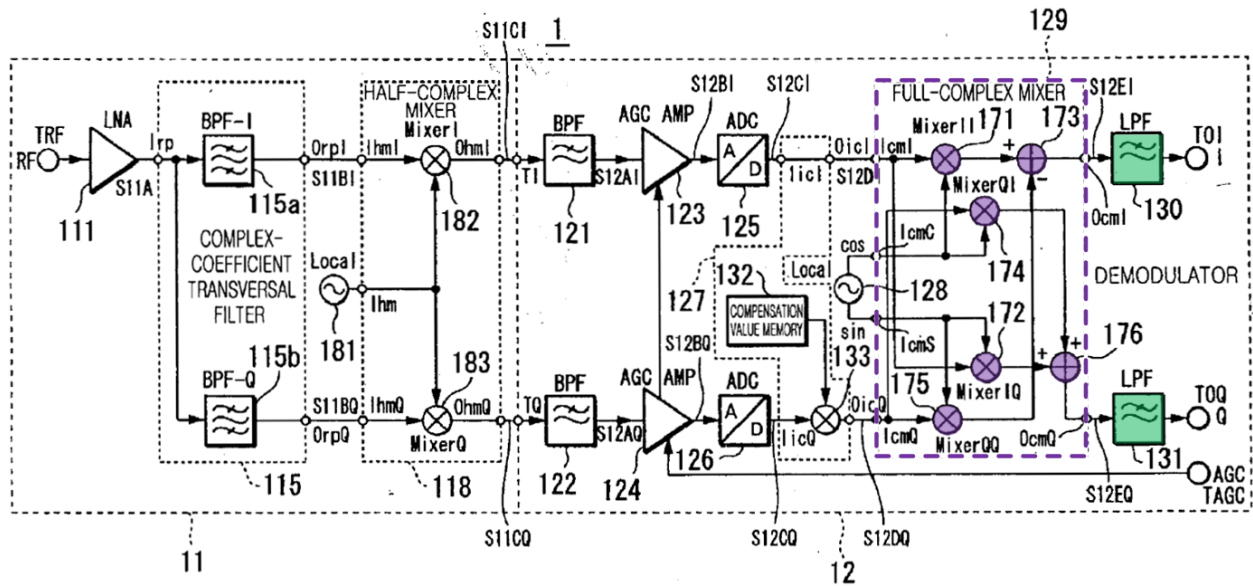
Rabaey is a textbook on digital integrated circuit design. Ex. 1116, p. 1. Rabaey was published by October 22, 2003, and publicly available to a POSITA by that date, and is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1173, ¶¶ 47-54. Rabaey is reasonably pertinent to problems with which the '866 patent is concerned (e.g., by describing the “commonly known methods” of sending “a serial or parallel digital data stream to a demodulator using a serial or parallel data interface” that the '866 patent references), and is analogous art to the '866 patent on at least that basis. Ex. 1101, 7:10-14; Ex. 1102, ¶ 92.

F. Lee

Lee, a February 14, 2008, U.S. Patent Application Publication, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1153, cover. Lee describes a STB that receives cable broadcasting signals. Ex. 1153, [0035]; Ex. 1102, ¶ 93. Lee is analogous art, as it is in the same field of endeavor as the '866 patent (e.g., receiving cable signals), and by describing a STB having claimed features (DOCSIS channels, picture-in-picture display), is reasonably pertinent to problems with which the '866 patent is concerned. Ex. 1153, [0007], [0031]; Ex. 1102, ¶ 93.

G. Takahiko

Takahiko, a November 16, 2006, U.S. Patent Application Publication, is pre-AIA 35 U.S.C. § 102(b) prior art. Ex. 1161, cover. Takahiko discloses a downconverter of a radio receiver that includes a digital baseband complex mixer (purple) and low pass filters (green) similar to those of the '866 patent. Ex. 1161, [0143], [0153], [0156]; Ex. 1102, ¶ 94.



Ex. 1161, Fig. 1 (annotated)

Takahiko, by describing circuits also described by the '866 patent and which are used for similar purposes (reception and tuning of RF signals), is reasonably pertinent to problems with which the '866 patent is concerned and is analogous art. Ex. 1161, [0143]-[0156], Fig. 1; Ex. 1102, ¶ 95.

V. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based

Petitioner requests review of claims 1-82 on the following pre-AIA 35 U.S.C.

§ 103 grounds:

Ground	References	Claims Challenged
A	Cholas-Petrovic	27-33, 37, 40-47, 51, 54
B	Cholas-Petrovic-Burris	28, 42
C	Cholas-Petrovic-Maalej	32-33, 46-47
D	Cholas-Petrovic-Rabaey	1-9, 11, 13-22, 24, 26, 34-36, 48-50
E	Cholas-Petrovic-Rabaey-Burris	2, 15
F	Cholas-Petrovic-Rabaey-Maalej	6-8, 19-21, 34, 48
G	Cholas-Petrovic-Lee	38-39, 52-53, 55-61, 65-75, 79-82
H	Cholas-Petrovic-Lee-Burris	56, 70
I	Cholas-Petrovic-Lee-Maalej	60-61, 74-75
J	Cholas-Petrovic-Lee-Maalej-Rabaey	62, 76
K	Cholas-Petrovic-Lee-Rabaey	10, 12, 23, 25, 63-64, 77-78
L	Cholas-Petrovic-Takahiko	27-33, 37, 40-47, 51, 54
M	Cholas-Petrovic-Takahiko-Burris	28, 42
N	Cholas-Petrovic-Takahiko-Maalej	32-33, 46-47

O	Cholas-Petrovic-Takahiko-Rabaey	1-8, 9, 11, 13-22, 24, 26, 35-36, 49-50
P	Cholas-Petrovic-Takahiko-Rabaey-Burris	2, 15
Q	Cholas-Petrovic-Takahiko-Rabaey-Maalej	6-8, 19-21, 34, 48
R	Cholas-Petrovic-Takahiko-Lee	38-39, 52-53, 55-61, 65-75, 79-82
S	Cholas-Petrovic-Takahiko-Lee-Burris	56, 70
T	Cholas-Petrovic-Takahiko-Lee-Maalej	60-61, 74-75
U	Cholas-Petrovic-Takahiko-Lee-Maalej-Rabaey	62, 76
V	Cholas-Petrovic-Takahiko-Lee-Rabaey	10, 12, 23, 25, 63-64, 77-78

None of the prior art listed above was cited during prosecution of the '866 patent. Ex. 1101, cover.

A supporting declaration of David B. Lett includes, e.g., a discussion of Mr. Lett's background, the '866 patent, the prior art, and his opinions, and an explanation of the bases for those opinions. Ex. 1102, ¶¶ 1-270. Mr. Lett at least meets the level of skill of a POSITA. *Id.*, ¶¶ 4-16, 31; Ex. 1103.

B. Summary of Grounds and Comparison of Claim Limitations

The '866 patent has 6 independent claims (1, 14, 27, 41, 55, and 69) with 12-13 dependent claims each. All of the claims are directed to a cable television (TV) device as illustrated in Figure 2 of the '866 patent.

Claims 1, 27, and 55 identically recite “a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal ...”

and “a digital front end (DFE) ... configured to concurrently select and provide each of the plurality of desired channels [] without providing any of the plurality of undesired channels,” and differ only by inclusion of a single, well-known ancillary feature: “a serial interface” (claim 1), “a digital video recorder” (claim 27), or “a picture-in-picture” display (claim 55). Independent claims 14, 41, and 69 are nearly identical to claims 1, 27, and 55, respectively, but lack a “contiguous band of frequencies” and replace the “digital front end” (DFE) with “a plurality of digital down converters.”

Cholas in view of Petrovic teaches a “wideband analog-to-digital converter,” a “digital front end”/“plurality of digital down converters,” a digital video recorder, and numerous other claim features. Rabaey and Lee respectively show that a serial interface (claims 1 and 14) and a picture-in-picture display (claims 55 and 69) were well-known features. To the extent Patent Owner argues that a “digital front end”/“plurality of digital down converters” requires a specific placement of filters relative to a complex mixer, Cholas in view of Petrovic and Takahiko also teaches a “digital front end”/“plurality of digital down converters.”

The dependent claims are directed to various known features. To the extent any of these additional features are not also taught by Cholas or Petrovic, the remaining references (Lee, Burris, Rabaey, and Maalej) show that such features were obvious.

C. 314(a) Discretion Does Not Apply

The *Fintiv* factors as set forth in the Director's June 21, 2022, Guidance Memorandum do not warrant discretionary denial.

Factor one appears neutral. Petitioner has filed IPR petitions challenging all eight patents asserted in the District Court in case no. 2:23-cv-01050. If trial is instituted, and the case is not dismissed based on Petitioner's motion to dismiss the Second Amended Complaint, then Petitioner expects to request a stay, as decisions in Petitioner's favor would resolve the dispute in its entirety.

Factor two favors institution. Petitioner has filed a motion to dismiss the District Court case, Patent Owner has filed an Amended Complaint, and Petitioner will renew its Motion to Dismiss in order to seek dismissal of the operative complaint. In addition, no schedule beyond claim construction has been entered, and the Court has not set a trial date.

Factor three favors institution. To date, the investment by the District Court has been limited to considering motions to dismiss on the pleadings.

Factor four strongly favors institution. The petition challenges all claims in the '866 Patent while only claims 27-28, 33, 36-37, 41-42, 47, and 50-51 are asserted in the District Court.

Factor five does not warrant denial as Petitioner is a defendant in the District Court case.

Factor six favors institution. Petitioner presents compelling unpatentability challenges that merit institution.

D. 325(d) Discretion Does Not Apply

Considering the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, No. IPR2019-01469, Paper 6 at 8-9 (PTAB Feb. 13, 2020), the Board should not deny institution. The grounds raised herein are not the same or substantially the same as the art and arguments raised during prosecution, and to the extent that they are, the Examiner erred in a manner material to the patentability of the challenged claims by failing to find and consider all of the relevant prior art, including Cholas and Petrovic, that teach the limitations of the independent and dependent claims.

E. Level of Ordinary Skill

A person of ordinary skill in the art (a “POSITA”) at the time of the alleged invention would have had a degree in electrical engineering, or a similar discipline, along with three-to-four years of experience with digital signal processing (DSP) and RF tuning systems for satellite and/or cable communications. Ex. 1102, ¶¶ 30-32. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. *Id.*

F. Claim Construction

All claim terms herein should be given their ordinary and customary meaning to a POSITA, as they would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b).

1. “Wideband”

Consistent with its ordinary meaning, the '866 patent defines “wideband” as a band that carries multiple channels. For example, the '866 patent states that a receiver is “wideband” if it is “designed to concurrently receive several TV channels.” Ex. 1101, 1:36-39; Ex. 1102, ¶ 35.³

2. “Digital Down Converter”/“Digital Front End”

Independent claims 14, 41, and 69 recite “digital down converter[s]” “operable to generate a digital channel output corresponding to each desired channel.” A digital down converter, as the term states, is digital circuitry that

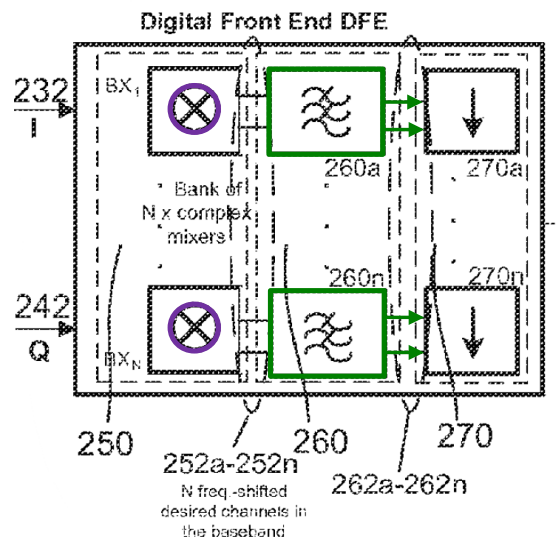
³ The '866 patent also states that “the invention relates to wideband receiver systems that are capable of receiving multiple desired television channels that extend over multiple non-contiguous portions of the broad frequency spectrum.” Ex. 1101, 1:29-33. This does not change the ordinary meaning above for “wideband,” and in any event the claims only recite a “wideband analog-to-digital converter,” not a “wideband receiver system.”

downconverts a digital signal. Ex. 1102, ¶ 36. The '866 patent omits the term “digital down converter,” but describes a “Digital Front End (DFE)” that downconverts digital signals. Ex. 1102, ¶ 36. Instead of digital down converters, independent claims 1, 27 and 55 recite a DFE that (like the digital down converters of claims 14, 41, and 69) is “configured to concurrently select and provide each of the plurality of desired channels,” but with the further limitation “without providing any of the plurality of undesired channels.”

The example DFE from Figure 2 (below) includes a plurality of signal paths, with each path including a complex mixer 250 (purple), an LPF 260 (green), and optionally a demodulator with a serial or parallel interface to the demodulator.⁴ Ex. 1101, 5:51-7:9, 9:50-60, Figs. 2-3; Ex. 1102, ¶ 37. Each of these signal paths performs the function claims 14, 41, and 69 ascribe to a digital down converter—generating a digital channel output corresponding to a desired channel. Ex. 1101, 5:51-7:9, 9:50-60, Figs. 2-3; Ex. 1102, ¶ 37. That this structure is the digital down converter is consistent with the dependent claims, which further require that the digital down converter(s) have, e.g., a digital mixer, filter, demodulator, and a serial

⁴ The '866 patent alternatively refers to the boxes following the filters in Figures 2 and 3 as decimators and/or demodulators, and also discloses the DFE as having outputs to a demodulator. Ex. 1101, 6:8-14, 7:4-9, 9:50-60, Figs. 2-3.

or parallel interface. Ex. 1101, claims 16, 18-21, 40, 43-50, 68, and 71-76. The complex mixer in each path performs “down-converting,” which the ’866 patent describes as shifting of the frequency of a signal to a lower frequency (also termed “down shift” and “frequency shift”). Ex. 1101, 1:38-40, 2:2-6, 2:13-28, 2:59-63, 2:65-3:2, 4:60-66, 6:3-6, 6:7-56, 7:47-55, 9:17-26; Ex. 1102, ¶ 37.



Ex. 1101, Fig. 2 (annotated and excerpted)

Neither “digital down converter” nor “digital front end” is a means-plus-function term. But if either term is so construed, the corresponding structure performing the recited function for “digital down converter” includes the components in one signal path in the DFE, i.e., a complex mixer 250 and a filter 260, and the corresponding structure for a “digital front end” include two such signal paths. Ex. 1101, 5:51-7:9, 9:50-60, Figs. 2-3; Ex. 1102, ¶ 38.

VI. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Cholas-Petrovic (Claims 27-33, 37, 40-47, 51, 54)

Claims 27-33, 37, 40-47, 51, and 54 are obvious over Cholas in view of Petrovic. Ex. 1102, ¶¶ 102-153, *see also* ¶¶ 47-76.

1. Independent Claim 27

a. [27A] “A cable television (TV) device comprising:”

Cholas discloses non-limiting preamble 27A.⁵ Ex. 1102, ¶¶ 104-106. Cholas’ STB 1710 (**red**) receives, “from the cable network,” an input signal (**blue**) having RF QAM (quadrature amplitude modulation) channels carrying TV programs. Ex. 1158, Abstract, [0001], [0002], [0004], [0006], [0010]-[0017], [0024], [0033], [0044], [0052]-[0057], [0059]-[0071], Figs. 4-6; Ex. 1102, ¶¶ 105-106.

⁵ The limitations of the claims appear and are labelled in the Claims Listing Appendix.

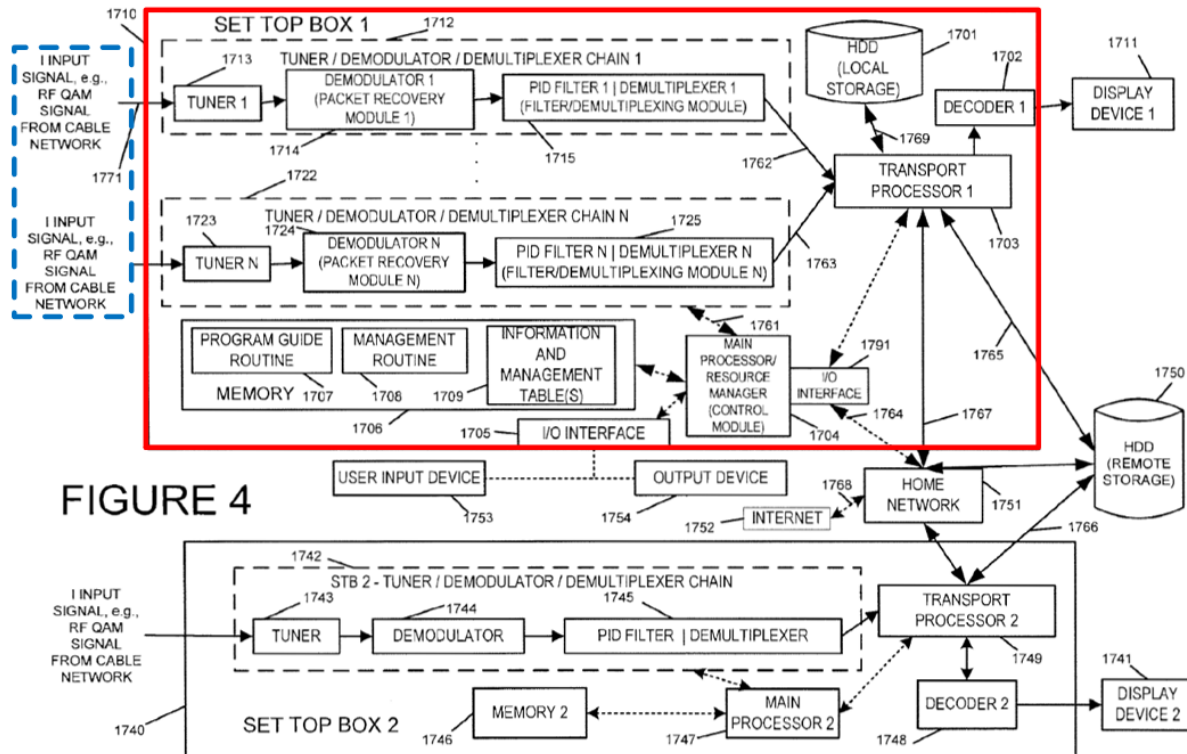


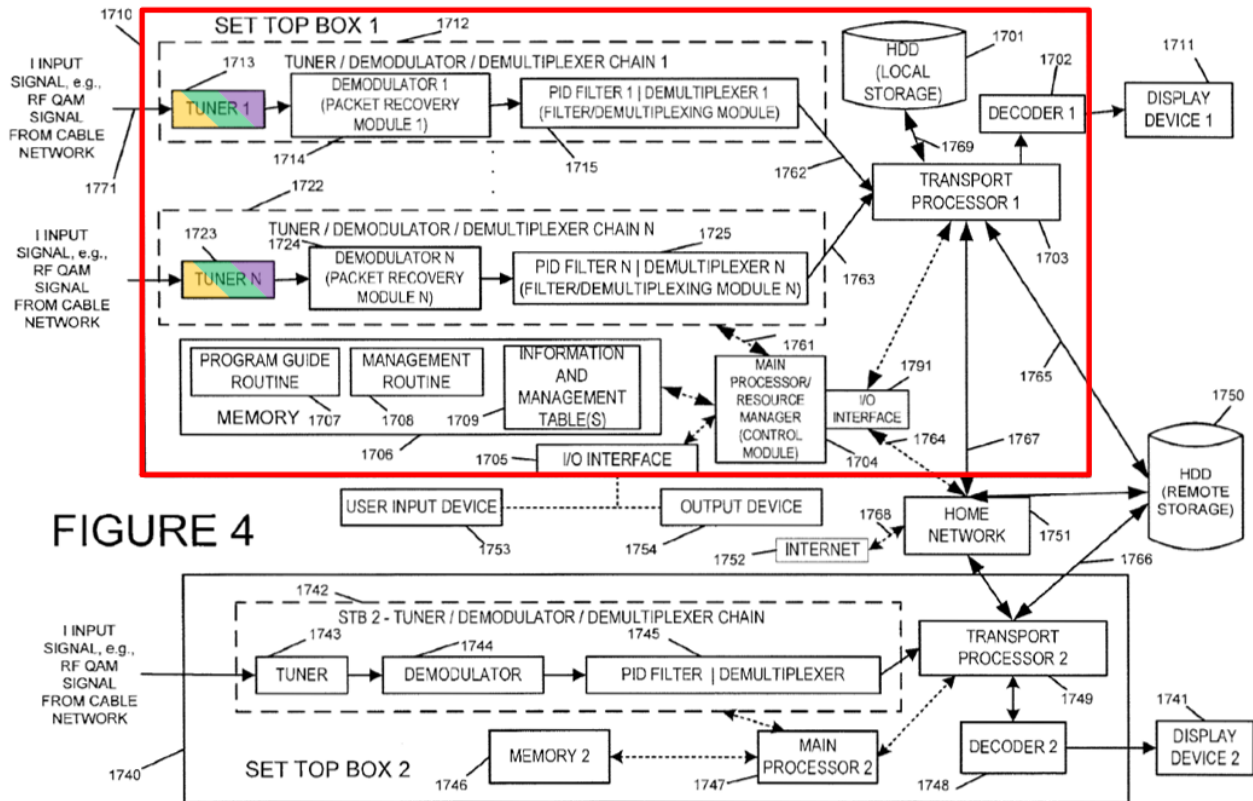
FIGURE 4

Ex. 1158, Fig. 4 (annotated)

- b. [27B] “a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and”

Cholas in view of Petrovic discloses limitation [27B]. Ex. 1102, ¶ 107. Cholas STB 1710 receives an input signal comprising a contiguous band of frequencies comprising all received channels that exist in the input signal, and the received channels comprise desired channels and undesired channels. Ex. 1102, ¶¶ 108-110. Per Cholas, “[a] typical RF signal enters” the STB 1710 “with multiple carriers between, e.g., frequencies 50-1000 MHz,” a bandwidth greater than the 800 MHz

“wide bandwidth” of the ’866 patent. Ex. 1158, [0045]; Ex. 1101, 2:34; Ex. 1102, ¶ 108. Each tuner (gold/green/purple striped) of the STB (red) “selects a single 6 MHz carrier frequency and passes the signal corresponding to the band” to a demodulator. Ex. 1158, [0045]; Ex. 1102, ¶ 108.



Ex. 1158, Fig. 4 (annotated)

A tuned channel is “desired” because it is tuned in response to a user’s program selection. Ex. 1158, [0059]-[0063]; Ex. 1102, ¶ 109-110. There are numerous 6 MHz channels between 50-1000 MHz and less than all of those channels would be tuned by the available tuners 1712-1722 at any given time, so at least some

channels are undesired. Ex. 1102, ¶ 110. In a conventional cable TV system, there are “undesired” channels that are not tuned by a particular STB. Ex. 1102, ¶ 110.

Petrovic’s channel stacking system 100 performs tuning functions similar to those of Cholas, and includes a wideband ADC that digitizes a contiguous band of frequencies in an input signal. Ex. 1102, ¶ 111.

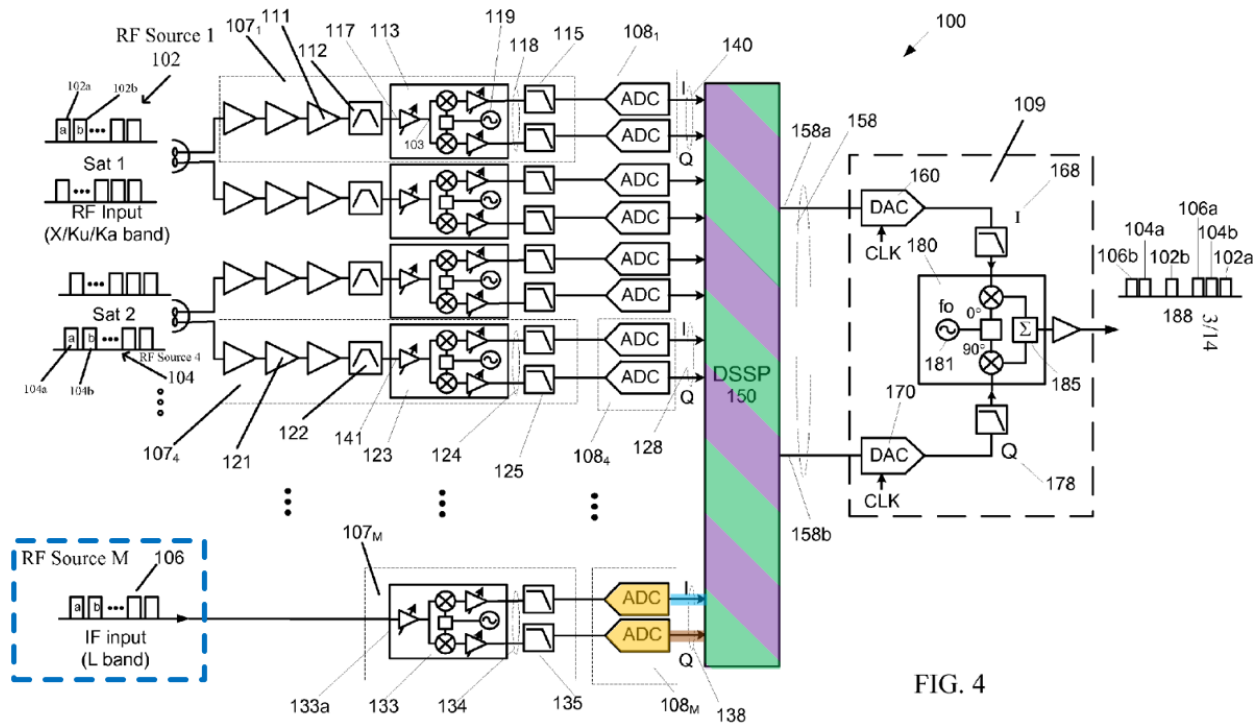


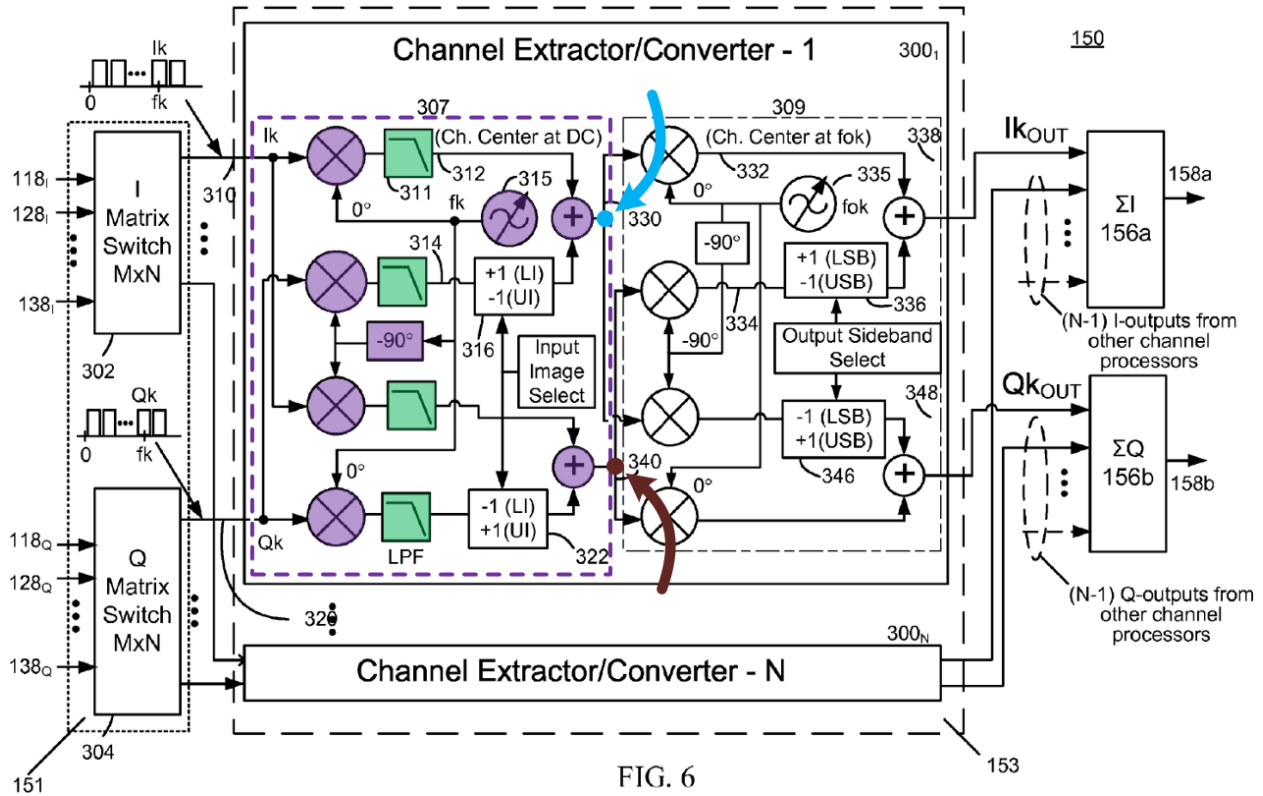
FIG. 4

Ex. 1108, Fig. 4 (annotated)

The system 100 receives signal 106 (blue broken-line box) that may be between 950-2150 MHz. Ex. 1108, [0029], [0031], [0050], Fig. 4; Ex. 1109, [0012], [0020], [0028], Fig. 1; Ex. 1102, ¶ 112. Signal 106 comprises multiple channels and is wideband. Ex. 1108, [0050], Fig. 4; Ex. 1109, [0028], Fig. 1; Ex. 1101, 2:34; Ex. 1102, ¶ 112.

“Analog preprocessing and downconversion (APD)” stage 107_M downconverts RF signal 106 into I, Q intermediate frequency (IF) signals 134 that are, after filtering, converted to digital form in analog-to-digital converters (ADCs) 108_M (gold). Ex. 1108, [0032]-[0035], [0048], [0050], [0052], Figs. 4-5; Ex. 1109, [0020]-[0022], [0028], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 113. ADCs 108_M digitize the entire band provided by the APD stage 107_M, which includes all received channels that exist in the signal 106, to generate digital I (blue), Q (brown) signals 138, making the ADCs 108_M “wideband.” Ex. 1108, [0039], Fig. 4; Ex. 1109, [0029], Fig. 1; Ex. 1102, ¶ 113.

Digital signal switching and pre-processing (DSSP) stage 150 (green/purple) receives the digitized signals 138 and “extract[s] the channels of interest ... (i.e., removes all the channels that are not of interest).” Ex. 1108, [0040], [0042], Fig. 4; Ex. 1109, [0015], [0025], [0033], Fig. 1; Ex. 1102, ¶ 114. Figure 6 shows additional details of the DSSP 150. Ex. 1108, [0058], Fig. 6; Ex. 1109, [0033], Fig. 3A; Ex. 1102, ¶ 114.

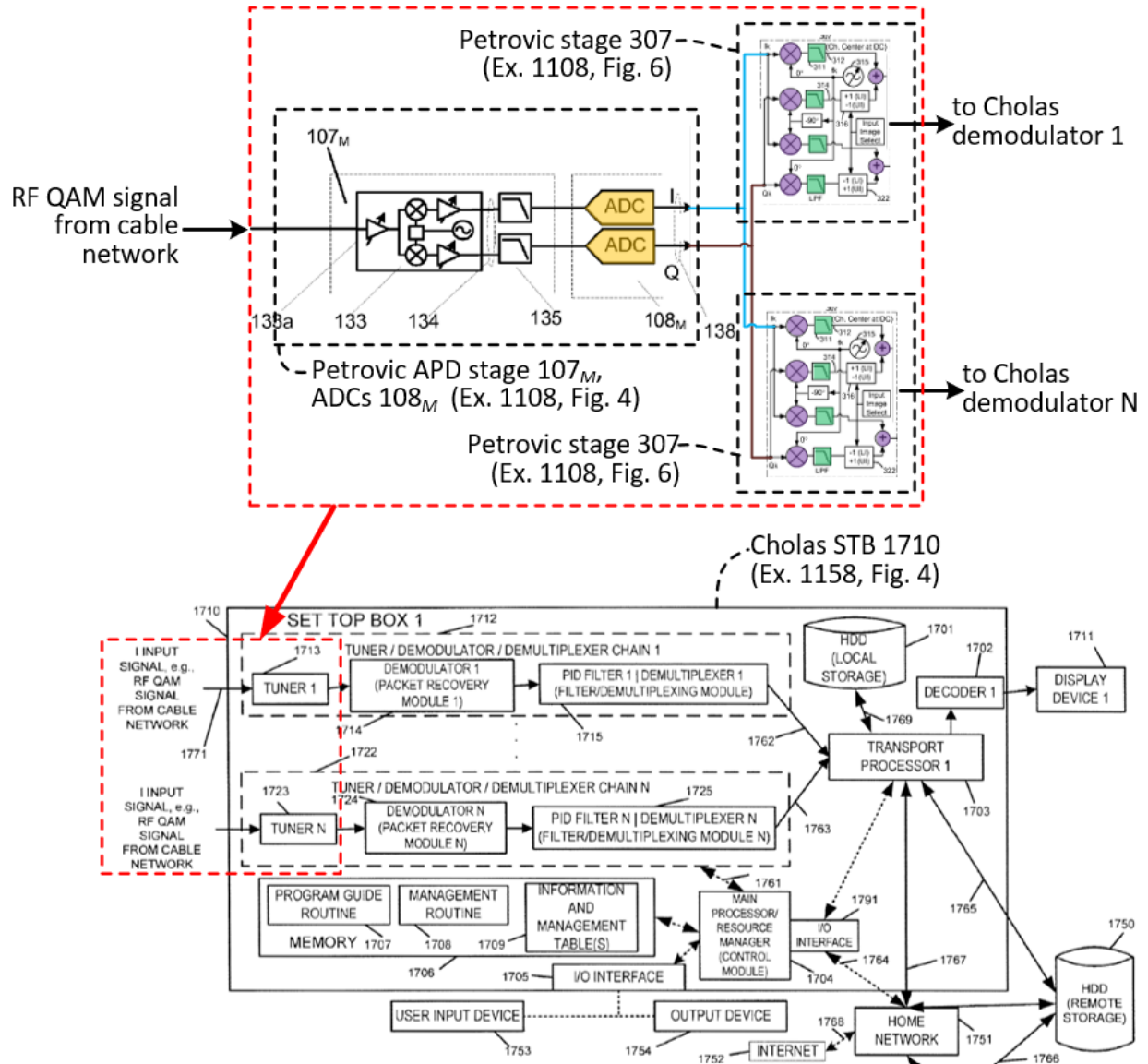


Ex. 1108, Fig. 6 (annotated)

The DSSP 150 includes multiple circuits 300, with each circuit 300 comprising a stage 307, and with each stage 307 able to select a different channel. Ex. 1108, [0055], [0059]-[0077], Fig. 6; Ex. 1109, [0033], [0037]-[0054], Fig. 3A; Ex. 1102, ¶ 115. A stage 307 extracts a channel from the digitized I, Q signals 138_I, 138_Q corresponding to the RF source 106 by digitally downconverting those signals so a desired channel is at baseband, and by filtering (green), in a complex mixer (purple and purple broken-line box). Ex. 1108, [0060]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1102, ¶ 115. The frequency f_k used for the downconversion is selected based on a frequency corresponding to a desired channel. Ex. 1108, [0066]; Ex.

1109, [0045]; Ex. 1102, ¶ 115. The complex mixer of a stage 307 outputs, from the adders (unnumbered purple “ $\oplus$ ” symbols) a quadrature pair comprising a digital I component 330 (blue dot and arrow) and a digital Q component 340 (brown dot and arrow) corresponding to a selected (i.e., “desired”) channel. Ex. 1108, [0077]; Ex. 1109, [0054]; Ex. 1102, ¶ 115.

In a Cholas-Petrovic STB, the Cholas tuners 1-N (tuners 1713-1723) would have been replaced with a single Petrovic tuner—the Petrovic APD stage 107_M, ADCs 108_M, and multiple stages 307 of the DSSP 150. Ex. 1102, ¶ 116. Each of the stages 307 would, like one of the replaced Cholas tuners 1-N, output a signal (a digital I, Q pair 330, 340) corresponding to a “desired” channel. Ex. 1102, ¶ 116. The annotated Figure below, prepared using Cholas Figure 4 and Petrovic Figures 4 and 6, shows the Cholas-Petrovic STB. Ex. 1102, ¶ 116.



Cholas-Petrovic STB

In the Cholas-Petrovic STB, the entire received band is output by the Petrovic APD stage 107_M, including all received channels that exist in the input RF QAM signal (desired and undesired). Ex. 1102, ¶ 117. All of those channels are digitized by the ADCs 108_M, and desired channels selected by Petrovic stages 307, as

explained for limitation [27C]. Ex. 1108, [0039], Fig. 4; Ex. 1109, [0029]; Ex. 1158, [0045], [0052]-[0053], [0055]-[0056], Fig. 5; Ex. 1102, ¶ 117.

A POSITA would have implemented the Cholas STB with a single Petrovic tuner, instead of multiple separate tuners, to beneficially simplify the STB and reduce the number of components. Ex. 1102, ¶ 118. Though Cholas does not disclose the tuners 1713-1723 performing downconversion, downconverting a received RF signal before further processing was a standard technique used in receivers. Ex. 1102, ¶ 118, *see also* ¶¶ 59-73. A single downconverter (as part of the APD stage 107_M) would use less power and be less expensive to implement than separate downconverters for multiple tuners. Ex. 1102, ¶ 118.

A single Petrovic tuner would also have improved the Cholas STB with digital tuning. Ex. 1102, ¶ 119. For example, selecting channels in the digital domain avoids the need for bandpass filtering and Hilbert transformers, thereby reducing circuit complexity and power consumption. Ex. 1108, [0007], [0096]; Ex. 1109, [0003], [0069]; Ex. 1102, ¶ 119, *see also* ¶ 69.

Implementing the Cholas STB with a Petrovic tuner instead of multiple separate tuners would have been a simple substitution, well within a POSITA's ability, of one known element for another to obtain predictable results. Ex. 1102, ¶ 120. As explained above, the output of each Petrovic stage 307 is an I, Q pair corresponding to a selected channel. Ex. 1102, ¶ 121. Cholas shows the output of

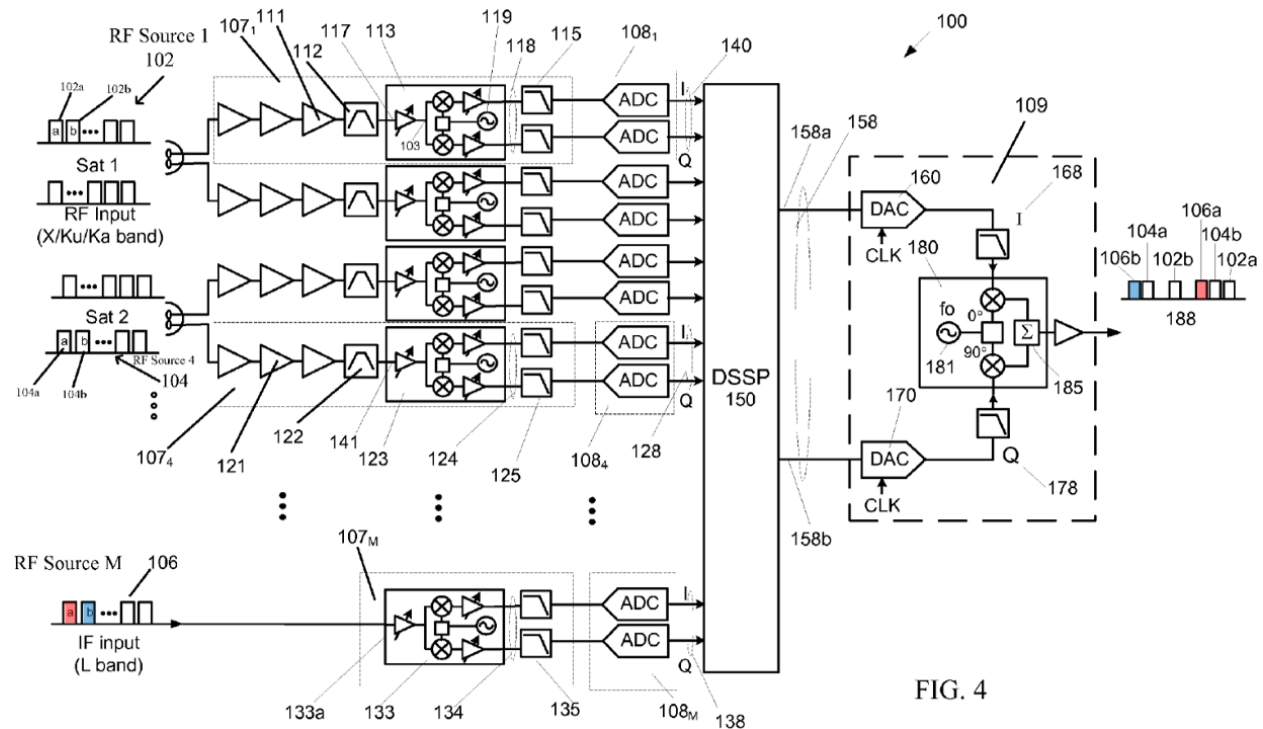
each tuner as the input to a dedicated QAM demodulator. Ex. 1158, Fig. 4; Ex. 1102, ¶ 121. Generating I, Q components was a well-known preliminary step in QAM demodulation. Ex. 1102, ¶ 121, *see also*, ¶ 54. Indeed, and as discussed in more detail in Section VI.C for dependent claims that recite “demodulators,” it was known that QAM demodulators may digitize, and create I, Q components for, a signal being demodulated. Ex. 1160, 4:5-19, Fig. 2; Ex. 1102, ¶ 121. A POSITA would thus have recognized that the outputs of Petrovic stages 307 usefully serve as inputs to demodulators. Ex. 1102, ¶ 121.

Modifying a Cholas STB to replace multiple separate tuners with a Petrovic tuner also would have been use of a known technique to improve a similar device in the same way. Ex. 1102, ¶ 122. For the same reasons explained above, a POSITA could have applied the improvement of the Petrovic tuner to the Cholas STB, and the results would have been predictable to a POSITA. Ex. 1102, ¶ 122.

- c. **[27C] “a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels without providing any of the plurality of undesired channels, and”**

Cholas-Petrovic discloses the DFE of limitation [27C]. Ex. 1102, ¶¶ 123-129. Petrovic stages 307, coupled to the ADC pair 108_M, select and provide desired channels without providing undesired channels. Ex. 1108, [0055]; Ex. 1109, [0033]; Ex. 1102, ¶ 124. In Cholas, various channels are received in an input signal from a

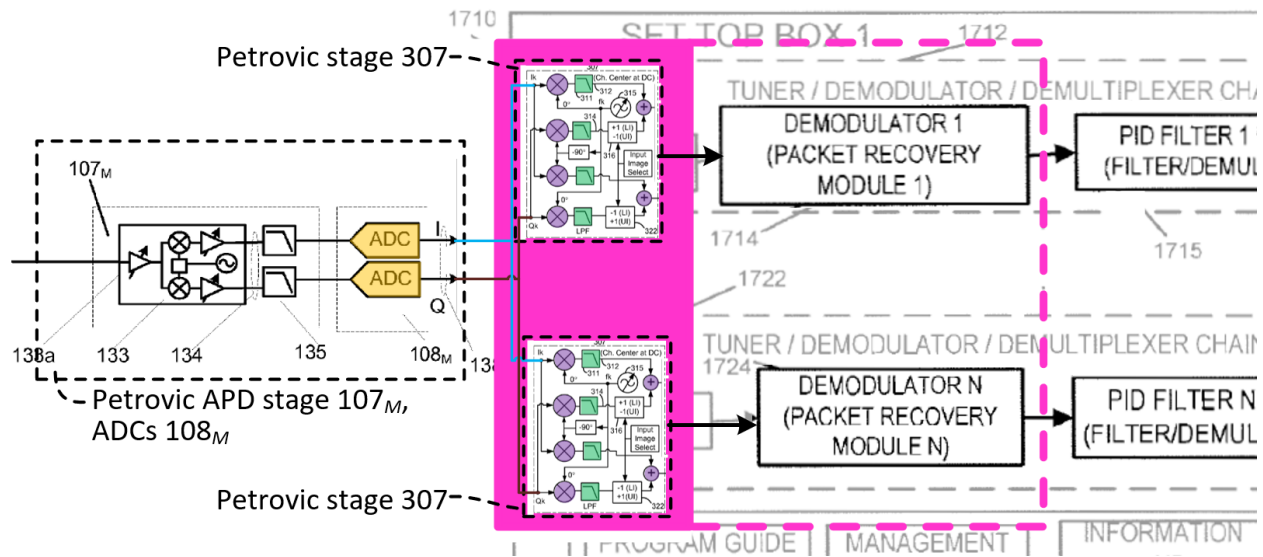
cable network, and multiple channels may be tuned (i.e., “selected”) concurrently. Ex. 1158, [0052]-[0053], [0055]-[0056]; Ex. 1102, ¶ 124; *see also* Ex. 1158, [0007], [0011]. This functionality remains in Cholas-Petrovic, as the multiple Petrovic stages 307 operate in parallel to select, from I, Q signals carrying multiple channels, desired channels. Ex. 1108, [0055], [0059]-[0077], Fig. 6; Ex. 1109, [0033], [0037]-[0054], Fig. 3A; Ex. 1102, ¶ 124. Petrovic Figure 4, where input RF signal 106 comprises channels 106a (red) and 106b (blue), shows concurrent selection and output (via parallel stages 307 within DSSP 150) of those channels. Ex. 1108, [0050], Figs. 4, 6; Ex. 1109, [0020], Figs. 1, 3A; Ex. 1102, ¶ 125.



Ex. 1108, Fig. 4 (annotated)

In a Cholas-Petrovic STB, the digital stages 307 would be configured to concurrently select each of the plurality of desired channels without selecting undesired channels. Ex. 1158, [0052]-[0053], [0055]-[0056], Fig. 5; Ex. 1108, [0042], [0050], [0053], [0055], [0058], Figs. 4, 6; Ex. 1109, [0004]-[0005], [0015], [0020], [0025], [0033], [0036], Figs. 1, 3A; Ex. 1102, ¶ 126; *see also* Ex. 1158, [0007], [0011]. The Cholas STB tunes channels in response to user selection of program carried on those channels, so tuned (or selected) channels are “desired” and “undesired” channels are not tuned. Ex. 1158, [0059]-[0063]; Ex. 1102, ¶ 126. This would not change in a Cholas-Petrovic STB, as only the components used to perform tuning (vs. components that cause tuning to be performed) would be modified. Ex. 1102, ¶ 126.

The stages 307 of Cholas-Petrovic may be a DFE according to limitations [27C], or the DFE may include more of the Cholas-Petrovic STB. For example, dependent claims 32 and 33 indicate the DFE may “comprise[] a plurality of digital demodulators.” Ex. 1102, ¶ 127. The below Figure shows the Cholas-Petrovic STB, which has been rearranged so the stages 307 are aligned with the Cholas demodulators, and portions of Cholas Figure 4 and of the STB have been omitted or faded for simplicity. Ex. 1102, ¶ 127.



“DFE” in Cholas-Petrovic

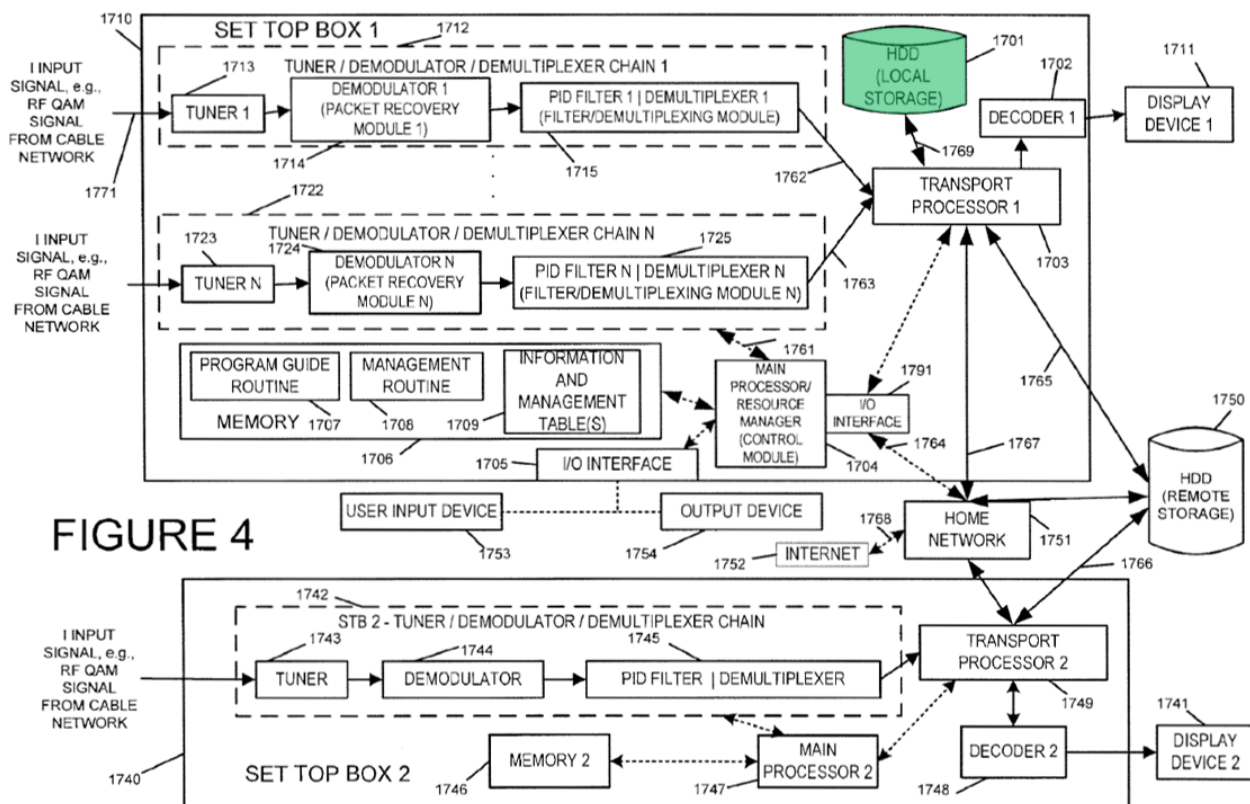
Either the stages 307 (solid pink box), or the stages 307 *plus* the demodulators (solid and broken-line pink boxes), are a DFE coupled to the wideband ADC pair 108_M and configured to concurrently select and provide (to the demodulators, or to the PID filters) each of the plurality of desired channels without providing any of the plurality of undesired channels. Ex. 1102, ¶ 128.

If the DFE of limitation [27C] is treated as means-plus-function, it is still disclosed by Cholas-Petrovic. Ex. 1102, ¶ 129. Each stage 307 has a complex mixer and low pass filters that select a desired channel. *Id.*; see Section VI.A.1.b (purple and green in annotated Figure 6). This is the same or equivalent structure as the DFE of ’866 patent Figure 2, which has a complex mixer 250 and filter 260 to select each desired channel. Ex. 1101, 5:51-65, 6:6-8, Fig. 2; Ex. 1102, ¶ 129. The Petrovic stages 307 operate in the same (or an equivalent) way as the ’866 patent DFE

(digitally downconverting digital I, Q components so that a desired channel is at baseband, and filtering out other channels), perform the same function, and achieve the same result (desired channels are selected and provided). Ex. 1102, ¶ 129.

d. [27D] “wherein the cable TV device comprises a digital video recorder (DVR).”

Cholas-Petrovic discloses limitation [27D]. Ex. 1102, ¶¶ 130-131. STB 1710 comprises a DVR 1701 (green), and this DVR remains in the Cholas-Petrovic STB. Ex. 1158, [0033] (“a digital storage device, e.g., a DVR, ... corresponding to the STB”), [0045] (streams can be directed to “internal HDD (local storage) 1701, typically a hard drive”), [0054]-[0057], Fig. 4; Ex. 1102, ¶ 131.



Ex. 1158, Fig. 4 (annotated)

2. Independent Claim 41

a. [41A] “A cable TV device comprising:”

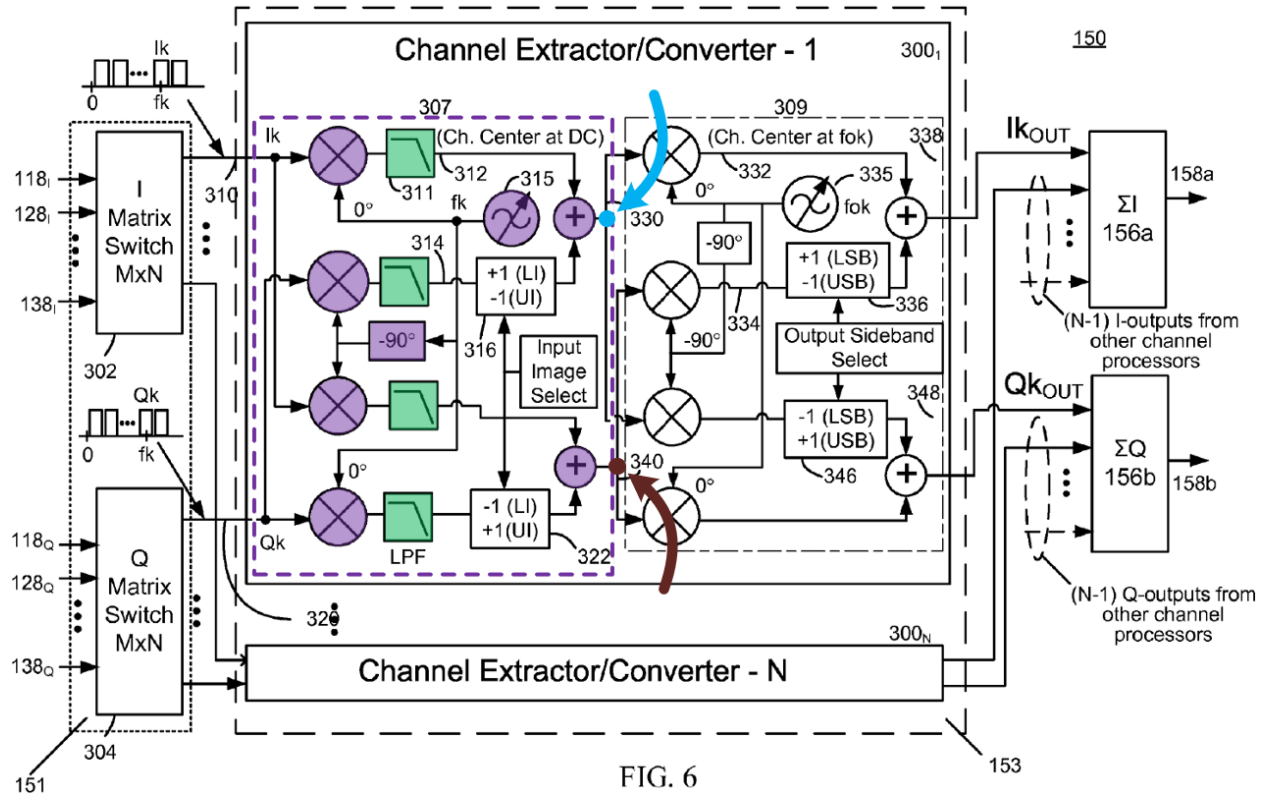
Cholas-Petrovic discloses non-limiting preamble [41A] for the reasons explained for preamble [27A]. Ex. 1102, ¶ 133; Section VI.A.1.a.

b. [41B] “a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a plurality of desired channels and a plurality of undesired channels; and”

Cholas-Petrovic discloses limitation [41B] for the reasons explained for limitation [27B]. Ex. 1102, ¶ 134; Section VI.A.1.b. As with limitation [27B], and for the reasons explained in Section VI.A.1.b, a POSITA would have been motivated to implement the Cholas STB to include a single Petrovic tuner (e.g., the Petrovic APD stage 107_M, ADCs 108_M, and multiple stages 307 of the DSSP 150). Ex. 1102, ¶ 135. To the extent there is any difference between limitation [27B], which recites that the wideband ADC is “configured to digitize a contiguous band of frequencies in an input signal,” and limitation [41B], which recites “configured to digitize an input signal,” both limitations are taught. Ex. 1102, ¶ 135. In Cholas-Petrovic, the entire band provided by the Petrovic APD stage 107_M includes all received channels (desired and undesired) and is digitized by the ADCs 108_M. Ex. 1108, [0039], Fig. 4; Ex. 1109, [0029]; Ex. 1158, [0045], [0052]-[0053], [0055]-[0056], Fig. 5; Ex. 1102, ¶ 135.

- c. [41C] “a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and”

Cholas-Petrovic discloses the “plurality of digital down converters” of limitation [41C] for reasons explained for limitation [27C]. Ex. 1102, ¶ 136; Section VI.A.1.c. Each of the stages 307 in Cholas-Petrovic is coupled to the ADC pair 108_M. Ex. 1108, [0055]; Ex. 1109, [0033]; Ex. 1102, ¶ 137.



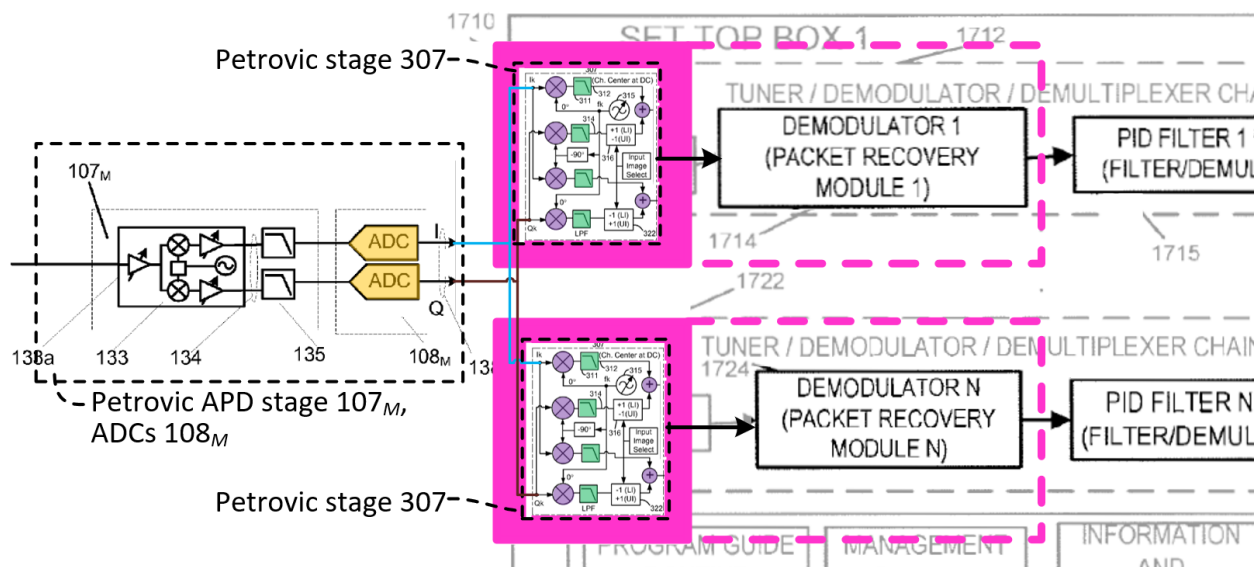
Ex. 1108, Fig. 6 (annotated)

Each stage 307 has a complex mixer (purple) and low pass filters (green) that select a desired channel through digital downconversion and that generate a digital

output (I, Q signals 330 (blue), 340 (brown)) corresponding to the desired channel.

Ex. 1102, ¶ 138; *see* Section VI.A.1.b.

Each of the stages 307 of Cholas-Petrovic may be a digital down converter according to limitation [41C], or digital down converters may include more of Cholas-Petrovic. Ex. 1102, ¶ 139. For example, dependent claims 46 and 47 indicate that the digital down converters may also “comprise[] a digital demodulator.” *Id.*



“Digital Down Converters” in Cholas-Petrovic

Each of the stages 307 (solid pink boxes) is a digital down converter that is coupled to the wideband ADC and that is configured to generate (and provide to a demodulator) a digital output corresponding to a desired channel. Ex. 1102, ¶ 140. Each of the stages 307 and a corresponding demodulator (solid and broken-line pink boxes) also is a digital down converter coupled to the wideband ADC and configured

to generate (and provide to a PID filter) a digital output corresponding to a desired channel. Ex. 1102, ¶ 140.

If “digital down converters” of limitation [41C] is treated as means-plus-function, it is still disclosed by Cholas-Petrovic. Ex. 1102, ¶ 141. Each stage 307 has a complex mixer and low pass filters that select a desired channel. Ex. 1102, ¶ 141. This is the same or equivalent structure of ’866 patent Figure 2, which has a complex mixer 250 and filter 260 to select each desired channel. Ex. 1101, 5:51-65, 6:6-8, Fig. 2; Ex. 1102, ¶ 141. The Petrovic stages 307 operate in the same (or an equivalent) way as the ’866 patent mixer 250 and filter 260 (digitally downconverting digital I, Q components so that a desired channel is at baseband, and filtering out other channels), perform the same function, and achieve the same result (desired channel digital channel outputs are generated). Ex. 1102, ¶ 141.

d. [41D] “wherein the cable TV device comprises a digital video recorder (DVR).”

Cholas-Petrovic discloses limitation [41D] for the same reasons explained for limitation [27D]. Ex. 1102, ¶ 142; *see* Section VI.A.1.d.

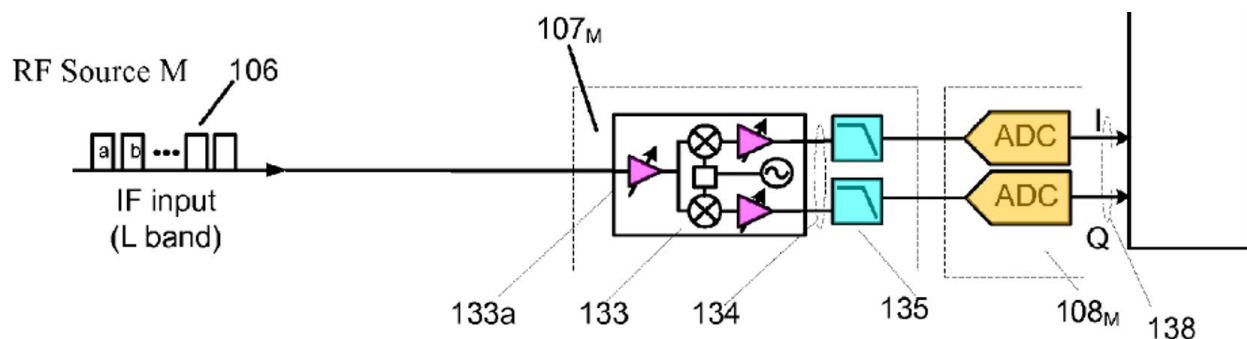
3. Claims 28, 42

[28/42] “The cable TV device of claim [27/41], wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.”

Claims 28 and 42 are obvious over Cholas-Petrovic. Ex. 1102, ¶¶ 143-144.

The Cholas-Petrovic STB receives input from a cable network, and a POSITA would have known it obviously had a “cable network connector” so that it could connect to that cable network to receive the input signal, as otherwise it would not function properly. Ex. 1158, [0044]; Ex. 1102, ¶ 143.

Petrovic discloses an analog amplifier (pink) and an analog filter (aqua) between an RF signal input and ADCs 108_M (gold). Ex. 1108, [0050], [0052], Figs. 4-5; Ex. 1109, [0020], [0031]-[0032], Figs. 1-2; Ex. 1102, ¶ 144.



Ex. 1108, Fig. 4 (excerpted and annotated)

In a Cholas-Petrovic STB, the Petrovic analog amplifier and analog filter would be located between the cable network connector and the ADC pair 108_M. Ex. 1102, ¶ 144.

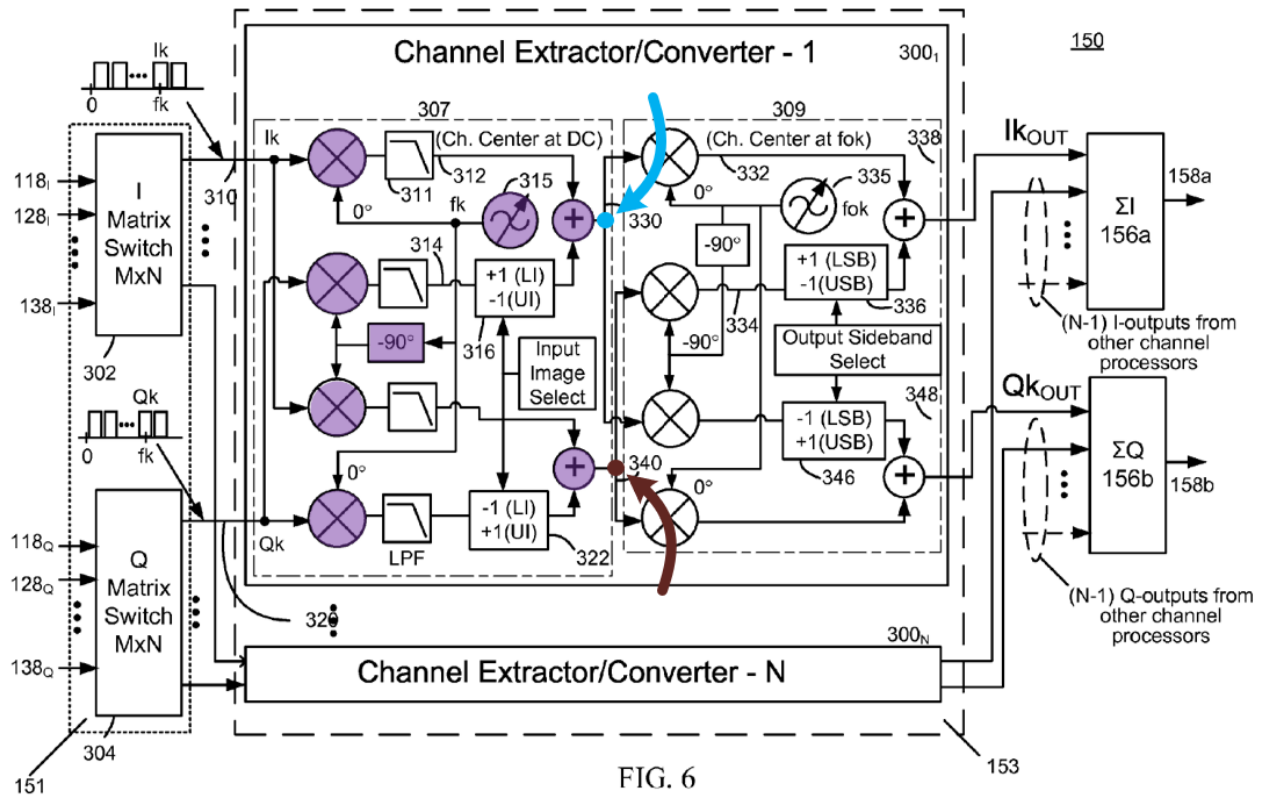
4. Claims 29-30, 43-44

[29] “The cable TV device of claim 27, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.”

[43] The cable TV device of claim 41, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.

[30/44] “The cable TV device of claim [29/43], wherein: the I and Q components of each corresponding complex signal are at baseband.”

Cholas-Petrovic, discloses claims 29-30 and 43-44 for the same reasons explained for limitations [27B]-[27C] (Sections VI.A.1.b-VI.A.1.c) and limitation [41C] (Section VI.A.2.c). Ex. 1102, ¶ 145. Each of the Petrovic stages 307 includes a complex mixer that digitally downconverts a signal (I, Q components 138_I and 138_Q) so that a desired channel is at baseband. Ex. 1108, [0059]-[0077]; Ex. 1109, [0037]-[0054]; Ex. 1102, ¶ 145. Each of those complex mixers outputs, from the adders (unnumbered purple “⊕” symbols), a quadrature pair comprising an I component 330 (blue dot and arrow) and a Q component 340 (brown dot and arrow) corresponding to a selected channel. Ex. 1108, [0077]; Ex. 1109, [0054]; Ex. 1102, ¶ 145.



Ex. 1108, Fig. 6 (annotated)

5. Claims 32-33, 46-47

[32] “The cable TV device of claim 29, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.”

[33] “The cable TV device of claim 27, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.”

[46] “The cable TV device of claim 43, wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.”

[47] “The cable TV device of claim 41, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired channels, to provide a demodulated channel as the digital channel output.”

Cholas-Petrovic discloses claims 32-33 and 46-47. Ex. 1102, ¶¶ 146-148. As explained with respect to elements [27C] and [41C], the digital downconverters and/or DFEs in Cholas-Petrovic can include demodulators. Sections VI.A.1.c and VI.A.2.c. Cholas discloses each tuner (gold/green/purple striped) outputting, to a corresponding demodulator (blue), a selected 6 MHz QAM channel. Ex. 1158, [0044]-[0045], [0050]-[0056], Figs. 4-5; Ex. 1102, ¶ 147.

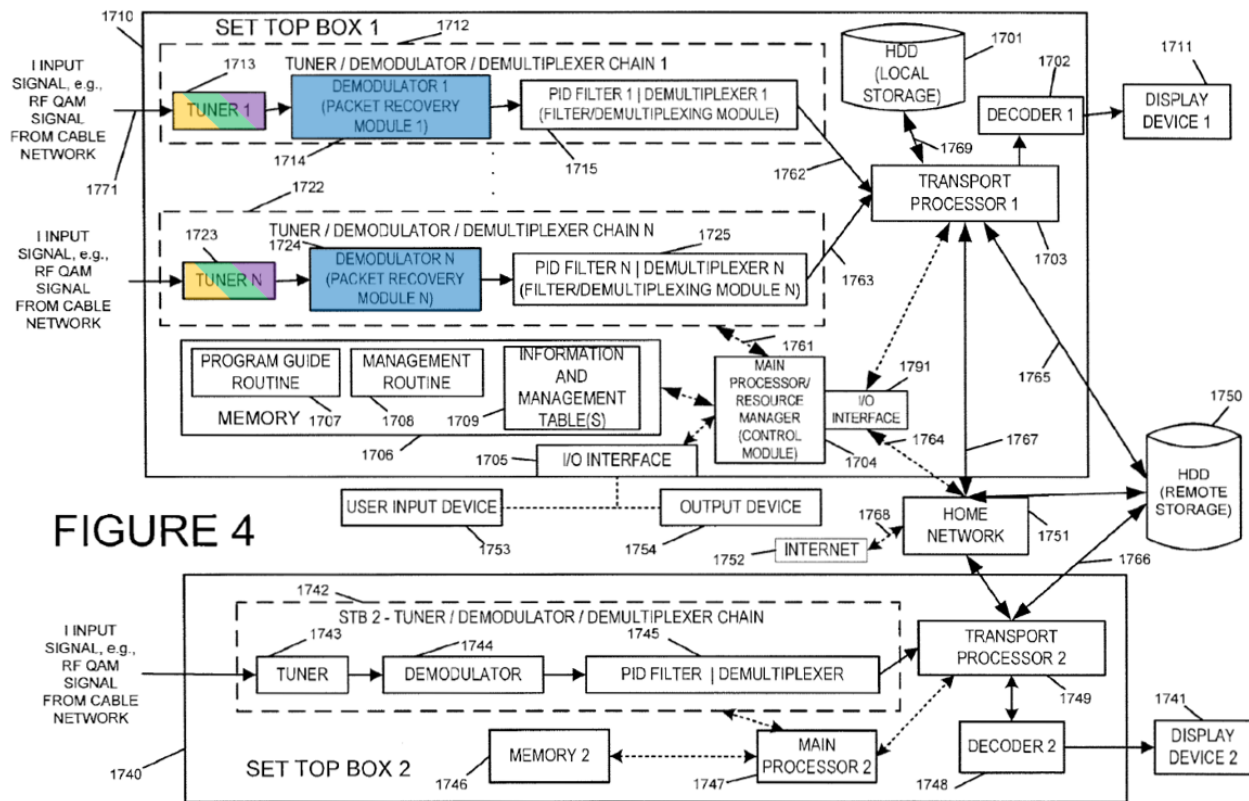


FIGURE 4

Ex. 1158, Fig. 4 (annotated)

In the Cholas-Petrovic STB, Petrovic stages 307 would output, to corresponding Cholas demodulators, I, Q pairs 330, 340 corresponding to selected channels. Ex. 1102, ¶¶ 148; *see* Sections VI.A.1.b (27B), VI.A.2.b (41B). Those demodulators demodulate the Cholas, I, Q pairs 330, 340 to provide demodulated channels. Ex. 1158, [0045]; Ex. 1102, ¶ 148.

6. Claims 31, 45

[31] “The cable TV device of claim 29, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.”

[45] “The cable TV device of claim 43, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.”

Cholas-Petrovic discloses claims 31 and 45. Ex. 1102, ¶ 149. As explained in Sections VI.A.1.b-VI.A.1.c and VI.A.2.c, the Petrovic stages 307 comprise filters (LPFs 311 in Petrovic Figure 6). Ex. 1102, ¶ 149. Moreover, Cholas discloses that signals received by the STB 1710 comprise 6 MHz channels. Ex. 1158, [0045]; Ex. 1102, ¶ 149.

7. Claims 37, 51

[37/51] “The cable TV device of claim [27/41], wherein: the plurality of desired channels comprises at least one cable broadcast channel.”

Cholas-Petrovic discloses claims 37 and 51. Ex. 1102, ¶ 150-151. The Cholas-Petrovic STB would receive cable broadcast channels. Ex. 1158, [0004]-[0006], [0044]-[0057], Figs. 4-5; Ex. 1102, ¶¶ 151.

8. Claims 40, 54

[40] “The cable TV device of claim 27, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.”

[54] “The cable TV device of claim 41, wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.”

The Cholas-Petrovic STB receives cable network signals comprising 6 MHz channels and a 50-1000 MHz range. Ex. 1158, [0045], Fig. 4; Ex. 1102, ¶ 153. As explained in Sections VI.A.1.b and VI.A.2.b, Cholas-Petrovic discloses a wideband ADC configured to digitize a “contiguous band of frequencies”/“input signal” that comprises a plurality of desired and undesired channels. Ex. 1102, ¶ 153. A plurality of desired channels (i.e., at least two) and a plurality of undesired channels (i.e., at least two) is four or more channels. *Id.* Four channels (or even forty channels), in the Cholas-Petrovic STB would comprise a portion of the 50-1000 MHz input signal frequency spectrum. *Id.*

B. Cholas-Petrovic-Burris (Claims 28, 42)

Claims 28 and 42 are also obvious over Cholas-Petrovic in view of Burris. Ex. 1102, ¶¶ 154-156; *see also* ¶¶ 47-76. Burris teaches that a cable network connector in the form of a coaxial port was a known feature of STBs. Ex. 1159, 1:41-44; Ex. 1102, ¶ 156. A POSITA would have included a coaxial port such as that taught by Burris in the Cholas STB 1710 because it was a routine and beneficial way of

connecting an STB to a cable network. Ex. 1102, ¶ 156. The remaining limitations of claims 28 and 42 are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.3, and modification in view of Burris does not affect that disclosure. Ex. 1102, ¶ 156.

C. Cholas-Petrovic-Maalej (Claims 32-33, 46-47)

Claims 32-33 and 46-47 are also obvious over Cholas-Petrovic in view of Maalej. Ex. 1102, ¶¶ 157-161; *see also id.*, ¶¶ 47-76.

Maalej discloses a QAM demodulator 99 for demodulating 6 MHz CATV channels. Ex. 1160, 1:6-8, 1:28-34, 3:47-52; Ex. 1102, ¶ 159.

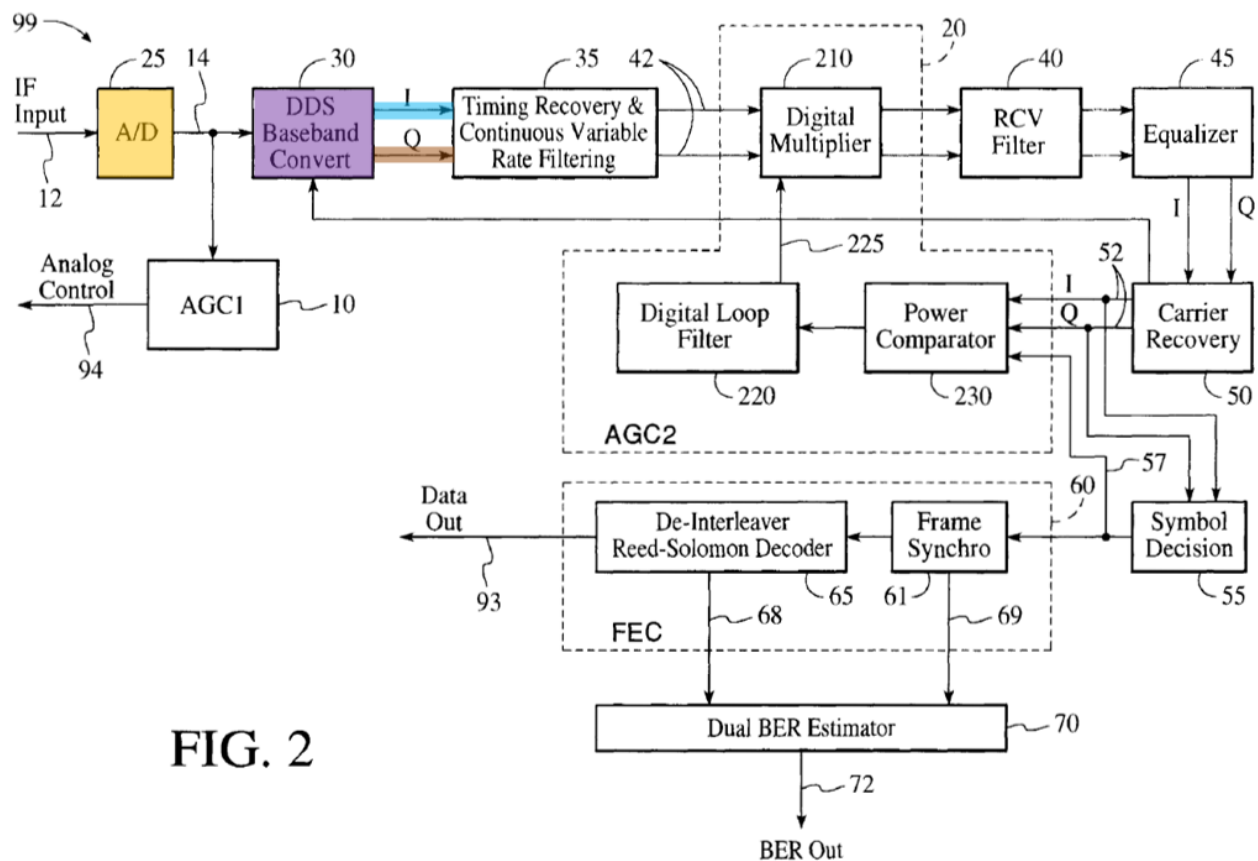


FIG. 2

Ex. 1160, Fig. 2 (annotated)

The demodulator 99 receives, as the signal to be demodulated, an IF signal 12. Ex. 1160, 3:52-4:7; Ex. 1102, ¶ 159. The IF signal 12 is digitized in an analog-to-digital (A/D) converter 25 (**gold**), and a Direct Digital Synthesizer (DDS) 30 (**purple**) converts the digitized signal to baseband I (**blue**), Q (**brown**) signals. Ex. 1160, 4:5-21, Fig. 2; Ex. 1102, ¶ 159.

The I, Q signals output by the Maalej DDS 30 are functionally equivalent to the Petrovic I, Q signals 330, 340, as both sets of I, Q signals comprise baseband digital I, Q components of a signal that is to be demodulated. Ex. 1102, ¶ 160. Moreover, the Maalej demodulator outputs, similar to the Cholas demodulators, MPEG2 Transport System (TS) packets. Ex. 1160, 5:12-15; Ex. 1158, [0045]; Ex. 1102, ¶ 160. Applying Maalej's teachings to Cholas-Petrovic, each of the Cholas demodulators would be implemented to include components of the Maalej demodulators (e.g., blocks 35, 210, 40, 45, 50, 230, 220, 55, 61, 65, and 70) that receive I, Q components 330, 340 from a Petrovic stage 307 and that output, to a respective Cholas PID filter, MPEG2 TS packets. Ex. 1102, ¶ 160.

This is merely a combination of known prior art elements according to known methods to yield predictable results. Ex. 1102, ¶ 161. A POSITA would have recognized the functional equivalence of a Petrovic stage 307 output and the output from the Maalej DDS 30, as well as the functional equivalence of the Maalej demodulator output and the inputs to Cholas PID filters/demultiplexers 1715-1725.

Ex. 1102, ¶ 161. A POSITA would also have recognized that, if I, Q signals of a QAM-modulated signal were to be demodulated so as to output, e.g., MPEG2 TS packets, the components of the Maalej demodulator could beneficially be used for a demodulator in the Cholas-Petrovic STB so that the signal could be demodulated.

Ex. 1102, ¶ 161. A POSITA would thus have easily combined a Petrovic stage 307 and components of the Maalej demodulator, as each would perform the same function in the combination that would be performed individually prior to the combination to beneficially demodulate the I and Q components. *Id.* For the same reasons, the results of combining a Petrovic stage 307 with Maalej demodulator components would have been predictable, with an expectation of success. Ex. 1102, ¶ 161.

D. Cholas-Petrovic-Rabaey (Claims 1-9, 11, 13-22, 24, 26, 35-36, 49-50)

Claims 1-9, 11, 13-22, 24, 26, 35-36, and 49-50 are obvious over Cholas-Petrovic in view of Rabaey. Ex. 1102, ¶¶ 162-189, *see also* ¶¶ 47-76.

1. Claim 35-36, 49-50

[35/36] “The cable TV device of claim 27, wherein: the DFE is operable to provide the plurality of desired channels via a [parallel/serial] interface.”

[49] “The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide a plurality of digital channel outputs, comprising each digital channel output, via a parallel interface.”

[50] “The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide each digital channel output via a serial interface.”

Claims 35-36 and 49-50 differ regarding the interface (parallel or serial) via which the DFE/digital down converters provide desired channels (claims 35 and 36) or digital channel outputs (claims 49 and 50). Choosing either interface would have been an obvious design choice, as explained below. Ex. 1102, ¶ 163.

Digital data, such as the I, Q signals 330, 340 output by Petrovic stages 307, is communicated as binary units (“bits”) in the form of electrical signals on wires. Ex. 1102, ¶ 164; Ex. 1116, pp. 23-24, 27-29, 48-51. Multiple bits can be sent over multiple separate wires, one wire for each bit (“parallel interface”), or one bit at a time over a single wire (“serial interface”). Ex. 1102, ¶ 164; Ex. 1115, pp. 5-6; Ex. 1116, pp. 79-80 (Figure 6.25).

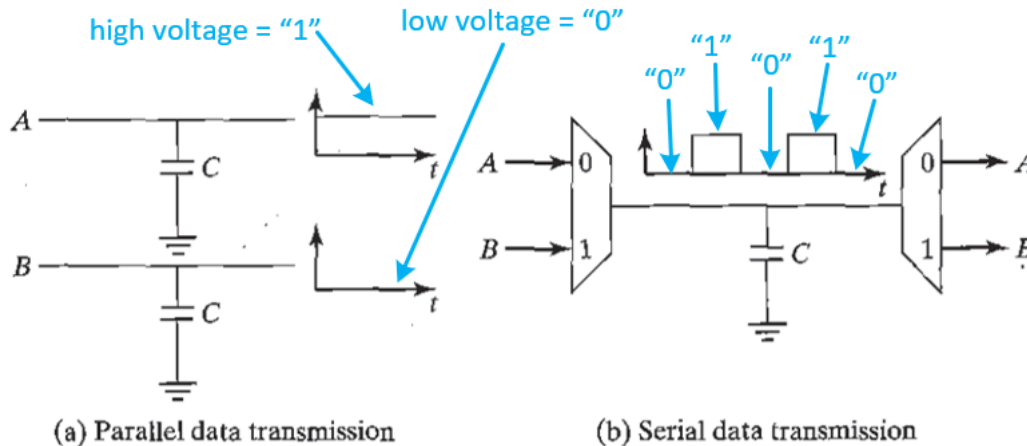


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1116, p. 80 (Figure 6.25) (annotated)

As explained in Sections VI.A.1.b and Section VI.A.2.c Petrovic stages 307 output desired channels as digital I, Q pairs 330, 340. The '866 patent concedes that outputs of digital data via serial or parallel interfaces were “commonly known methods.” Ex. 1101, 7:10-14; Ex. 1102, ¶ 165. Basic textbooks and technical papers on digital integrated circuit design confirm that a POSITA would have understood these two interfaces as the common options for outputting digital data. Ex. 1102, ¶ 165 (citing Ex. 1114, 30:31-42, 31:15-22; Ex. 1115, 6, 8; Ex. 1116, 79-80; Ex. 1117, 354-355).

For example, Rabaey, a textbook on digital integrated circuits, teaches that both serial and parallel interfaces as illustrated in the Figure 6.25 above were beneficially used in integrated circuits. Ex. 1116, pp. 79-80; Ex. 1102, ¶ 166. Per Rabaey, time-multiplexing (i.e., a serial interface) “is a technique often used to minimize the implementation area” of a design on a chip, but that this “minimum

area solution does not always result in the lowest switching activity,” for example, when the data signals have high “temporal correlation.” Ex. 1116, pp. 79-80, *see also* pp. 72-74; Ex. 1102, ¶ 166. Minimizing circuit area minimizes the cost of the integrated circuit, while minimizing the switching activity minimizes the power consumed by the integrated circuit. Ex. 1102, ¶ 166; Ex. 1116, pp. 29-33, 43-44, 72-74, 76-80. Thus, Rabaey teaches selecting between serial and parallel interfaces for transmitting digital data between two points, both of which have advantages over each other, depending upon area and power constraints and the temporal correlation between the signals. Ex. 1102, ¶ 166.

It would have been obvious to apply either of Rabaey’s parallel or serial interfaces as illustrated in Figure 6.25 to connect Petrovic’s stages 307 and demodulators, as the choice of interface would be a basic engineering choice between limited, predictable alternatives enabled by Rabaey. Ex. 1108, [0027], [0040], [0124]; Ex. 1109, [0009], [0115]; Ex. 1116, pp. 76-80; Ex. 1102, ¶ 167. Implementation of either interface would have been nothing more than a combination of prior art elements (Petrovic’s circuit design and Rabaey’s serial or parallel interface interconnects) according to known methods (Rabaey’s process for implementing circuit designs, including selecting a serial interface to minimize chip area and cost or a parallel interface to minimize switching and power) to yield predictable results (data sent serially or in parallel). Ex. 1102, ¶ 167.

The resultant combinations of Petrovic and Rabaey would have been predictable and a POSITA would have had a reasonable expectation of success, because Rabaey teaches basic techniques used by POSITAs to design integrated circuits, and how those basic techniques relate to design issues, such as meeting area and power constraints, with which a POSITA was very familiar. Ex. 1116, 29-33, 43-44, 72-74, 76-80; Ex. 1102, ¶ 168.

2. Claims 34, 48

[34] “The cable TV device of claim 33, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.”

[48] “The cable TV device of claim 47, wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.”

Claims 34 and 48 depend from claims 33 and 47, which are obvious over Cholas-Petrovic. Section VI.A.5. Claims 34 and 48 add a limitation taught by Rabaey, and are obvious over Cholas-Petrovic-Rabaey. Ex. 1102, ¶¶ 169-170. As explained for claims 35-36 and 49-50, sending data via a parallel interface would have been a routine, obvious design choice. Ex. 1102, ¶ 170; *see* Section VI.D.1.

This applies to demodulator outputs, as well. Ex. 1102, ¶ 171. Cholas teaches that its demodulators 1714 and 1724 output digital data to respective PID filters/demultiplexers 1715 and 1725. Ex. 1158, [0044]-[0045], Fig. 4; Ex. 1102, ¶ 171. As with the providing of “desired channels” or “digital channel outputs” of Petrovic’s stages 307 to demodulators, and for the same reasons explained in Section

VI.D.1, the selection of a parallel interface between Cholas' demodulators and Cholas' PID filters/demultiplexers would have been a routine design choice, implementing a parallel interface would have been well within a POSITA's skillset, and a POSITA would have had a high expectation of success. Ex. 1102, ¶ 171. Similarly, implementing a parallel interface between Cholas' demodulators and Cholas' PID filters/demultiplexers would have been a combination of prior art elements (Cholas' demodulators, Cholas' PID filters/demultiplexers, and Rabaey's parallel interface interconnects) according to known methods (Rabaey's process for implementing circuit designs, including selecting a parallel interface to minimize switching and power) to yield predictable results (data sent in parallel). *Id.*

3. Independent Claim 1

a. [1A], [1B]

Preamble [1A] and limitation [1B] are the same as preamble [27A] and limitation [27B] and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.a-VI.A.1.b, and modification in view of Rabaey does not affect that disclosure. Ex. 1102, ¶¶ 172-174.

b. [1C] “a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels, via a serial interface, without providing any of the plurality of undesired channels.”

But for “via a serial interface,” limitation [1C] is the same as limitation [27C], which is disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.1.c.

Ex. 1102, ¶ 175. The “via a serial interface” portion of limitation [1C] is disclosed by Cholas-Petrovic-Rabaey for the reasons explained in Section VI.D.1, and claim 1 is obvious over Cholas-Petrovic-Rabaey. *Id.*

4. Independent Claim 14

a. [14A] “A cable TV device comprising:”

Preamble [14A] and limitations [14B]-[14C] are the same as preamble [41A] and limitations [41B]-[41C] and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.2.a-VI.A.2.c, and modification in view of Rabaey does not affect that disclosure. Ex. 1102, ¶¶ 176-179.

b. [14D] “wherein the plurality of digital down converters is operable to provide each digital channel output via a serial interface.”

Limitation [14D] is the same as claim 50 and disclosed by Cholas-Petrovic-Rabaey for the reasons explained in Section VI.D.1, and claim 14 is obvious over Cholas-Petrovic-Rabaey. Ex. 1102, ¶ 180.

5. Claims 2, 15

Claims 2 and 15 add the same limitations as claims 28 and 42 and are disclosed by Cholas-Petrovic for the reasons explained in section V.A.3. Ex. 1102, ¶ 181. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 2 and 15, which are obvious over Cholas-Petrovic-Rabaey. Ex. 1102, ¶ 181.

6. Claims 3-4, 16-17

Claims 3, 4, 16, and 17 add the same limitations as claims 29, 30, 43, and 44, and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.4. Ex. 1102, ¶ 182. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 3, 4, 16, and 17, which are obvious over Cholas-Petrovic-Rabaey. *Id.*

7. Claims 5, 18

Claims 5 and 18 add the same limitations as claims 31 and 45 and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.b-VI.A.1.c, VI.A.2.c, and VI.A.6. Ex. 1102, ¶ 183. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 5 and 18, which are obvious over Cholas-Petrovic-Rabaey. *Id.*

8. Claims 6-7, 19-20

Claims 6-7 and 19-20 add the same limitations as claims 32-33 and 46-47 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.5. Ex. 1102, ¶ 184. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 6-7 and 19-20, which are obvious over Cholas-Petrovic-Rabaey. Ex. 1102, ¶ 184.

9. Claims 8, 21

Claims 8 and 21 add the same limitations as claims 34 and 48, which are disclosed by Cholas-Petrovic-Rabaey for the reasons explained in Section VI.D.2. Ex. 1102, ¶ 185.

To the extent claim 8 or claim 21 requires a demodulator to output via a parallel interface and via a serial interface, this is also taught by Cholas-Petrovic-Rabaey, which shows that transmission via a parallel interface (light green) may be multiplexed into transmission via a serial interface (light blue), and vice versa. Ex. 1116, p. 80; Ex. 1102, ¶¶ 185-186.

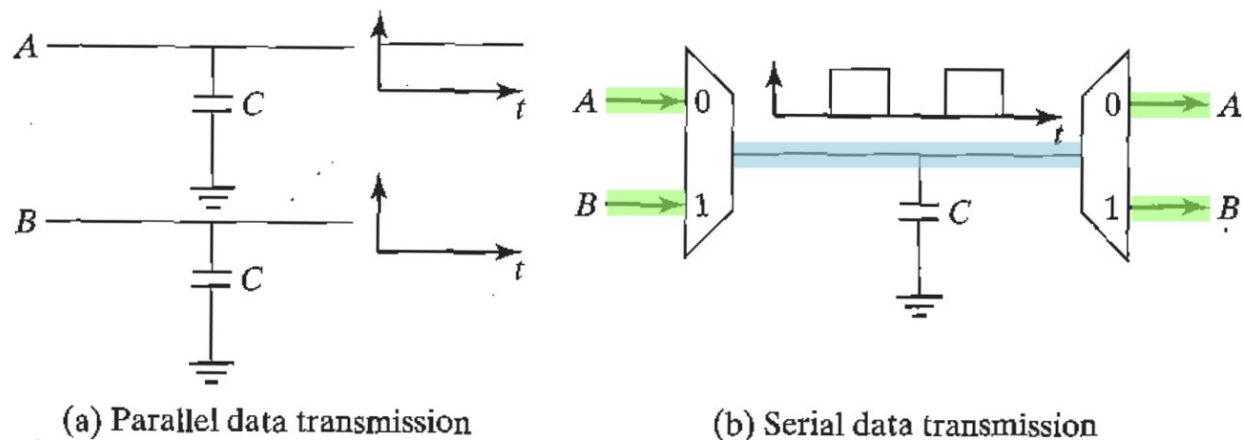


Figure 6-25 Parallel versus time-multiplexed data busses.

Ex. 1116, p. 80 (Figure 6.25) (annotated)

For the reasons explained in Section VI.D.1, a POSITA would have predictably combined Cholas-Petrovic demodulators and PID filters with the known multiplexing configuration, shown in Rabaey Figure 6.25, to change from parallel transmission to serial (or vice versa) to accommodate area, timing, and other

constraints associated with communicating digital data between functional blocks (e.g., between demodulators and PID) of a STB. Ex. 1102, ¶ 186. Accordingly, claims 8 and 21 are obvious over Cholas-Petrovic-Rabaey. Ex. 1102, ¶ 186.

10. Claims 9, 22

Claims 9 and 22 add the same limitations as claims 37 and 51 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.7. Ex. 1102, ¶ 187. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 9 and 22, which are obvious over Cholas-Petrovic-Rabaey. *Id.*

11. Claims 11, 24

Claims 11 and 24 add the same limitations as limitations [27D] and [41D] and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.d and VI.A.2.d. Ex. 1102, ¶ 188. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 11 and 24, which are obvious over Cholas-Petrovic-Rabaey. *Id.*

12. Claims 13, 26

Claims 13 and 26 add the same limitations as claims 40 and 54 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.8. Ex. 1102, ¶ 189. Modification in view of Rabaey does not affect the Cholas-Petrovic disclosure of the limitations of claims 13 and 26, which are obvious over Cholas-Petrovic-Rabaey. *Id.*

E. Cholas-Petrovic-Rabaey-Burris (Claims 2, 15)

Claims 2 and 15 add the same limitations as claims 28 and 42 and are disclosed by Cholas-Petrovic-Burris for the reasons explained in Section VI.B. Modification in view of Rabaey does not affect the modification of Cholas-Petrovic in view of Burris, and claims 2 and 15 are obvious over Cholas-Petrovic-Rabaey-Burris. Ex. 1102, ¶¶ 190-191; *see also* ¶¶ 47-76.

F. Cholas-Petrovic-Rabaey-Maalej (Claims 6-8, 19-21, 34, 38)

Claims 6-8, 19-21, 34, 48 are obvious over Cholas in view of Petrovic, Rabaey, and Maalej. Ex. 1102, ¶¶ 192-196; *see also* ¶¶ 47-76.

1. Claims 6-7, 19-20

Claims 6-7 and 19-20 add the same limitations as claims 32-33 and 46-47, which are obvious over Cholas-Petrovic-Maalej (Section VI.C). Claims 6-7 and 19-20 are obvious over Cholas-Petrovic-Rabaey-Maalej. Ex. 1102, ¶ 193. The reasons it would be obvious to add Rabaey to Cholas-Petrovic (Sections VI.D.1-VI.D.2) are also the reasons it would be obvious to add Rabaey to Cholas-Petrovic-Maalej, and modification in view of Maalej does not affect modification of Cholas-Petrovic in view of Rabaey. *Id.*

2. Claims 8, 21

Claims 8 and 21 depend from claims 7 and 20, which are obvious in view of Cholas-Petrovic-Rabaey-Maalej. Section VI.F.1. Claims 8 and 21 add a limitation taught by Rabaey, and are also obvious over Cholas-Petrovic-Rabaey-Maalej. Ex.

1102, ¶ 194. As explained for claims 35-36 and 49-50, sending data via a parallel interface would have been a routine, obvious design choice. *Id.*; see Section VI.D.1.

All of this applies to being “operable to provide a plurality of demodulated desired channels via a parallel interface.” Ex. 1102, ¶ 195. Maalej teaches digital output (MPEG2 TS packets) from its demodulator 99. Ex. 1160, 5:12-15; Ex. 1102, ¶ 195. As with the providing of “desired channels” or “digital channel outputs” of Petrovic’s stages 307 to demodulators, and for the reasons explained in Section VI.D.1, the selection of a parallel interface between Maalej’s demodulators and Cholas’ PID filters/demultiplexers would have been a routine design choice, implementing a parallel interface would have been well within a POSITA’s skillset, and a POSITA would have had a high expectation of success. Ex. 1102, ¶ 195. Similarly, implementing a parallel interface between Maalej’s demodulators and Cholas’ PID filters/demultiplexers would have been a combination of prior art elements (Maalej’s circuit design, Cholas’ PID filters/demultiplexers, and Rabaey’s parallel interface interconnects) according to known methods (Rabaey’s process for implementing circuit designs, including selecting a parallel interface to minimize switching and power) to yield predictable results (data sent in parallel). *Id.* To the extent claim 8 or claim 21 requires a demodulator to output via a parallel interface and via a serial interface, and for the reasons explained in Section VI.D.1, a POSITA would have predictably combined Cholas-Petrovic-Maalej demodulators and PID

filters with the known multiplexing configuration, shown in Rabaey Figure 6.25, to change from parallel transmission to serial (or vice versa) to accommodate area, timing, and other constraints associated with communicating digital data between functional blocks (e.g., between demodulators and PID) of a STB. *Id.*

3. Claims 34, 48

Claims 34 and 48 depend from claims 33 and 47, which are obvious over Cholas-Petrovic-Maalej (Section VI.C). Ex. 1102, ¶ 196. Claims 34 and 48 add the same limitations to claims 33 and 47 that claims 8 and 21 add to claims 7 and 20, which are obvious over Cholas-Petrovic-Rabaey-Maalej (Section VI.F.1). *Id.* For the reasons explained in claims 8 and 21 (Section VI.F.2), claims 34 and 48 are obvious over Cholas-Petrovic-Rabaey-Maalej. *Id.*

G. Cholas-Petrovic-Lee (Claims 38-39, 52-53, 55-61, 65-75, 79-82)

Claims 38-39, 52-53, 55-61, 65-75, and 79-82 are obvious over Cholas in view of Petrovic and Lee. Ex. 1102, ¶¶ 197-221; *see also* ¶¶ 47-76.

1. Claims 38, 52

[38/52] “The cable TV device of claim [27/41], wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.”

Lee discloses that STBs included tuners to receive DOCSIS channel signals. Ex. 1153, [0007]; Ex. 1102, ¶ 199. A POSITA would have configured the Cholas-Petrovic STB to receive DOCSIS channels so that, e.g., the STB could provide an

open cable application platform (OCAP). Ex. 1153, [0006]-[0007]; Ex. 1102, ¶ 199. A POSITA would also have been motivated to configure the Cholas-Petrovic STB to receive DOCSIS channels so that a common 2-way data infrastructure in the cable system could be used for cable modems as well as STB communications. Ex. 1102, ¶ 199.

Using the Cholas-Petrovic STB to receive DOCSIS channels would also have been a use of a known technique (receiving DOCSIS channels in an STB, per Lee) to improve a similar device (a Cholas-Petrovic STB) in the same way. Ex. 1102, ¶ 200. A POSITA could have readily modified the Cholas-Petrovic STB to receive DOCSIS channels, as taught by Lee, because DOCSIS protocols were established and understood. *Id.*; *see also* ¶ 47. For the same reasons, the results of that modification would have been predictable and POSITA would have had an expectation of success. *Id.*, ¶ 200.

2. Claims 39, 53

[39] “The cable TV device of claim 27, wherein: the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.”

[53] “The cable TV of claim 41, wherein: the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.”

Lee discloses that it was known for STBs to tune multiple channels and use those tuned channels to provide picture-in-picture (PIP) functionality. Ex. 1153,

[0031]; Ex. 1102, ¶ 202. A POSITA would have configured the Cholas-Petrovic STB to provide a PIP display so that the STB could provide additional functionality for the user. Ex. 1153, [0006]; Ex. 1102, ¶ 202.

Using the Cholas-Petrovic STB to provide PIP functionality would also have been a use of a known technique (providing PIP output using an STB, per Lee) to improve a similar device (a Cholas-Petrovic STB) in the same way. Ex. 1102, ¶ 203. A POSITA could have readily modified the Cholas-Petrovic STB to provide PIP functionality, as taught by Lee, because PIP output was established and understood. *Id.*, ¶¶ 70, 203. For the same reasons, the results of that modification would have been predictable and POSITA would have had an expectation of success. *Id.*, ¶ 203.

3. Independent Claim 55

a. [55A], [55B]-[55C]

Preamble [55A] and limitations [55B]-[55C] are the same as preamble [27A] and limitations [27B]-[27C] and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.a-VI.A.1.c, and modification in view of Lee does not affect that disclosure. Ex. 1102, ¶¶ 205-207.

b. [55D]

Limitation [55D] adds the same limitation as claim 39 (taught by Lee) and is disclosed by Cholas-Petrovic-Lee for the reasons explained in Section VI.G.2. Ex. 1102, ¶ 208.

4. Independent Claim 69

a. [69A], [69B]-[69C]

Preamble [69A] and limitations [69B]-[69C] are the same as preamble [41A] and limitations [41B]-[41C] and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.a-VI.A.1.c and VI.A.2.a-VI.A.2.c, and modification in view of Lee does not affect that disclosure. Ex. 1102, ¶¶ 210-212.

b. [69D]

Limitation [69D] adds the same limitation as claim 53 (taught by Lee) and is disclosed by Cholas-Petrovic-Lee for the reasons explained in Section VI.G.2. Ex. 1102, ¶ 213.

5. Claims 57-58, 71-72

Claims 57-58 and 71-72 add the same limitations as claims 29-30 and 43-44 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.4. Ex. 1102, ¶ 214. Modification in view of Lee does not affect the Cholas-Petrovic disclosure of the limitations of claims 57-58 and 71-72, which are obvious over Cholas-Petrovic-Lee. *Id.*

6. Claims 59, 73

Claims 59 and 73 add the same limitations as claims 31 and 45 and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.c (limitation [27C]), VI.A.2.c (limitation [41C]), and VI.A.6 (claims 31 and 45). Ex. 1102, ¶ 215. Modification in view of Lee does not affect the Cholas-Petrovic

disclosure of the limitations of claims 59 and 73, which are obvious over Cholas-Petrovic-Lee. *Id.*

7. Claims 60-61, 74-75

Claims 60-61 and 74-75 add the same limitations as claims 32-33 and 46-47 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.5. Ex. 1102, ¶ 216. Modification in view of Lee does not affect the Cholas-Petrovic disclosure of the limitations of claims 60-61 and 74-75, which are obvious over Cholas-Petrovic-Lee. *Id.*

8. Claims 65, 79

Claims 65 and 79 add the same limitation as claims 37 and 51 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.7. Ex. 1102, ¶ 217. Modification in view of Lee does not affect the Cholas-Petrovic disclosure of the limitations of claims 65 and 79, which are obvious over Cholas-Petrovic-Lee. *Id.*

9. Claims 66, 80

Claims 66 and 80 add the same limitation as claims 38 and 52 and are disclosed by Cholas-Petrovic-Lee for the same reasons explained in Section VI.G.1. Ex. 1102, ¶ 218.

10. Claims 67, 81

Claims 67 and 81 add the same limitation as limitations [27D] and [41D] and are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.d and VI.A.2.d. Ex. 1102, ¶ 219. Modification in view of Lee does not affect the Cholas-

Petrovic disclosure of the limitations of claims 67 and 81, which are obvious over Cholas-Petrovic-Lee. *Id.*

11. Claims 68, 82

Claims 68 and 82 add the same limitations as claims 40 and 54 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.8. Ex. 1102, ¶ 220. Modification in view of Lee does not affect the Cholas-Petrovic disclosure of the limitations of claims 68 and 82, which are obvious over Cholas-Petrovic-Lee. *Id.*

12. Claims 56, 70

Claims 56 and 70 add the same limitations as claims 28 and 42 and are disclosed by Cholas-Petrovic for the reasons explained in Section VI.A.3. Ex. 1102, ¶ 221. Modification in view of Lee does not affect the Cholas-Petrovic disclosure of the limitations of claims 56 and 60, which are obvious over Cholas-Petrovic-Lee. *Id.*

H. Cholas-Petrovic-Lee-Burris (Claims 56, 70)

Claims 56 and 70 add the same limitations as claims 28 and 42 and are disclosed by Cholas-Petrovic-Burris for the reasons explained in Section VI.B. Modification in view of Lee does not affect the modification of Cholas-Petrovic in view of Burris, and claims 56 and 70 are obvious over Cholas-Petrovic-Lee-Burris. Ex. 1102, ¶ 223, *see also* ¶¶ 47-76.

I. Cholas-Petrovic-Lee-Maalej (Claims 60-61, 74-75)

Claims 60-61 and 74-75 add the same limitations as claims 32-33 and 46-47, which are obvious over Cholas-Petrovic-Maalej (Section VI.C). Claims 60-61 and

74-75 are obvious over Cholas-Petrovic-Lee-Maalej. Ex. 1102, ¶¶ 224-225, *see also* ¶¶ 47-76. The reasons it would be obvious to add Lee to Cholas-Petrovic (Sections VI.G.1-VI.G.2) are also the reasons it would be obvious to add Lee to Cholas-Petrovic-Maalej, and modification in view of Maalej does not affect modification of Cholas-Petrovic in view of Lee. Ex. 1102, ¶ 225.

J. Cholas-Petrovic-Lee-Maalej-Rabaey (Claims 62, 76)

Claims 62 and 76 add the same limitations as claims 8 and 21. Claims 61 and 75 (from which claims 62 and 76 depend) are obvious over Cholas-Petrovic-Lee-Maalej (Section VI.I). Ex. 1102, ¶ 227. It would be obvious to add Rabaey to Cholas-Petrovic-Lee-Maalej and render claims 62 and 76 obvious for the same reasons, as explained in Section VI.F.2, it would be obvious to add Rabaey to Cholas-Petrovic-Maalej. Ex. 1102, ¶¶ 227, *see also* ¶¶ 47-76. Modification of Cholas-Petrovic-Maalej in view of Lee does not affect modification in view of Rabaey. *Id.*, ¶ 227.

K. Cholas-Petrovic-Lee-Rabaey (Claims 10, 12, 23, 25, 63-64, 77-78)

Claims 10, 12, 23, 25, 63-64, and 77-78 are obvious over Cholas in view of Petrovic, Lee, and Rabaey. Ex. 1102, ¶¶ 228-231, *see also* ¶¶ 47-76.

1. Claims 10, 23

Claims 10 and 23 add the same limitation as claims 38 and 52 and are disclosed by Cholas-Petrovic-Lee for the reasons explained in Section VI.G.1. Ex. 1102, ¶ 229. Modification in view of Rabaey does not affect the Cholas-Petrovic-

Lee disclosure of the limitations of claims 10 and 23, which are obvious over Cholas-Petrovic-Lee-Rabaey. *Id.*

2. Claims 12, 25

Claims 12 and 25 add the same limitations as claims 39 and 53 and are disclosed by Cholas-Petrovic-Lee for the reasons explained in Section VI.G.2. Ex. 1102, ¶ 230. Modification in view of Rabaey does not affect the Cholas-Petrovic-Lee disclosure of the limitations of claims 12 and 25, which are obvious over Cholas-Petrovic-Lee-Rabaey. *Id.*

3. Claims 63-64, 77-78

Claims 63-64 and 77-78 add the same limitations as claims 35-36 and 49-50 and are disclosed by Cholas-Petrovic-Rabaey for the reasons explained in Section VI.D.1. Ex. 1102, ¶ 231. Modification in view of Lee does not affect the Cholas-Petrovic-Rabaey disclosure of the limitations of claims 63-64 and 77-78, which are obvious over Cholas-Petrovic-Lee-Rabaey. *Id.*

L. Cholas-Petrovic-Takahiko (Claims 27-33, 37, 40-47, 51, 54)

Claims 27-33, 37, 40-47, 51, 54 are obvious over Cholas in view of Petrovic and Takahiko. Ex. 1102, ¶¶ 232-243, *see also* ¶¶ 47-96.

1. Independent Claim 27

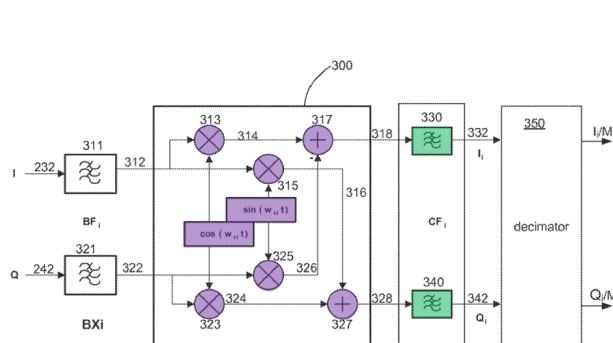
a. [27A]-[27B], [27D]

Preamble [27A] and limitations [27B] and [27D] are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.1.a-VI.A.1.b and VI.A.1.d.

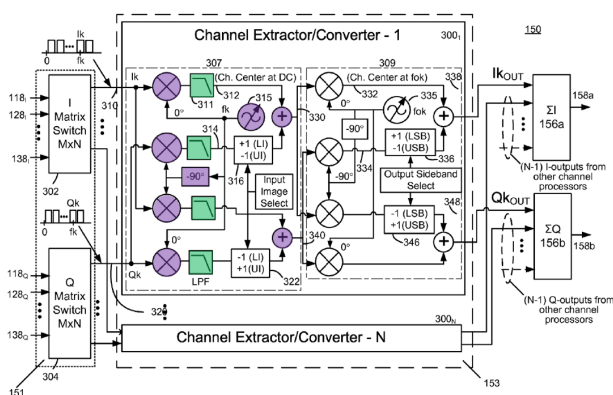
Modification in view of Takahiko, described below for limitation [27C], does not affect that Cholas-Petrovic disclosure. Ex. 1102, ¶ 233.

b. [27C]

Petrovic LPFs 311 are located within complex mixers of stages 307, while the '866 patent's filters 330 and 340 (an example of filter 260) are located after complex mixers 300 (an example of complex mixer 250). Ex. 1102, ¶ 234.



Ex. 1101, Fig. 3 (annotated)

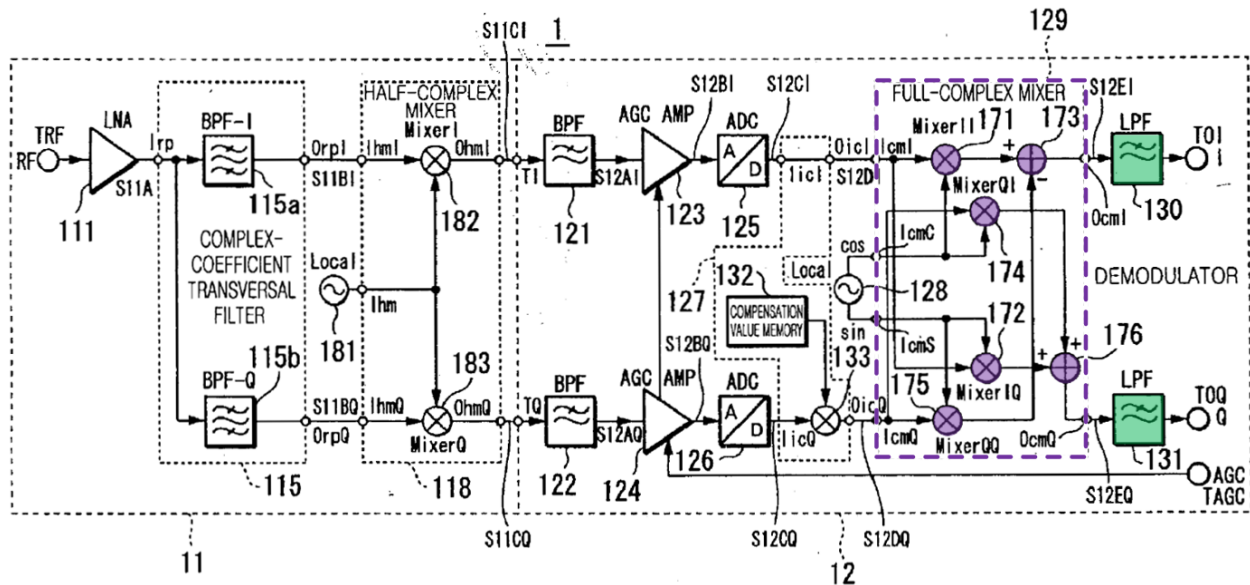


Ex. 1108, Fig. 6 (annotated)

To the extent Patent Owner contends the configuration of the Petrovic stage 307 is not the same or equivalent structure as the complex mixer 300 and filters 330 and 340 of the '866 patent, any difference would have been trivial, and the structure of the '866 patent (i.e., filters after the complex mixer) is taught by Cholas in view of Petrovic and Takahiko. Ex. 1102, ¶ 235.

Placing four LPFs before adders of a complex mixer or two LPFs after adders of a complex mixer would have been functionally equivalent and a matter of design choice, as both options were well known. Ex. 1102, ¶ 236. Takahiko describes a

“downconverter” that is used in a radio receiver, and that is very similar to the receiver of ’866 patent Figure 2. Ex. 1161, [0143]; Ex. 1102, ¶ 236.



Ex. 1161, Fig. 1 (annotated)

The “full-complex mixer” 129 (purple, broken-line purple box) and LPFs (green) 130 and 131 of Takahiko’s downconverter are the same as those of ’866 patent Figure 3 and are used the same way: downconversion of digital I, Q signals so a desired channel is at baseband and removal of unwanted higher frequencies with low-pass filtering. Ex. 1161, [0153], [0156]; Ex. 1102, ¶ 237.

A POSITA would have modified the complex mixers of the Petrovic stages 307 to use two low pass filters after the adders of the complex mixer, similar to the configuration of the Takahiko full-complex mixer 129 and filters 130 and 131, and instead of four low pass filters within the complex mixer, to make the circuit simpler and less expensive. Ex. 1102, ¶ 238. Because such a modification would have

involved use of known circuit components in known arrangements, because of the similarity between the relevant portions of the Petrovic stages 307 and the Takahiko full-complex mixer 129 and filters 130 and 131, and because the Takahiko full-complex mixer 129 and filters 130 and 131 would have been functionally equivalent to a Petrovic stage 307, a POSITA would have had a reasonable expectation of success and the results of the modification would have been predictable. Ex. 1102, ¶ 238.

As modified in view of Takahiko, the Petrovic stages 307 would operate as described in Section VI.A.1.c, but with the I, Q, signals coming from the output of LPFs located after the complex mixer. The stages 307 would have a structure (low pass filters after complex mixers) that is the same as (or equivalent to) the '866 patent structure, that operates in the same way (digitally downconvert I, Q components so desired channel is at baseband, filter out other channels), that performs the same function, and that achieves the same result (desired channels are selected and provided), and claim 27 is obvious over Cholas-Petrovic-Takahiko. Ex. 1102, ¶ 239.

2. Independent Claim 41

a. [41A]-[41B], [41D]

Preamble [41A] and limitations [41B] and [41D] are disclosed by Cholas-Petrovic for the reasons explained in Sections VI.A.2.a-b and VI.A.2.d. Modification

in view of Takahiko, described below for limitation [41C], does not affect that disclosure. Ex. 1102, ¶ 240.

b. [41C]

For the reasons explained in Section VI.L.1.b, a POSITA would have been motivated to modify the complex mixers of the Petrovic stages 307 to have a structure that is the same as shown in the '866 patent (LPFs after a complex mixer), that operates in the same or an equivalent way (digitally downconvert I, Q components so desired channel is at baseband, filter out other channels), that performs the same function, and that achieves the same result (digital channel outputs for desired channels generated), and claim 41 is obvious over Cholas-Petrovic-Takahiko. Ex. 1102, ¶ 241. As modified in view of Takahiko, the Petrovic stages 307 would operate as described in Section VI.A.2.c, but with the I, Q, signals coming from the output of LPFs located after the complex mixer. *Id.*

3. Claims 28-30, 32-33, 37, 40, 42-44, 46-47, 51, 54

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic of the limitations of claims 28-30, 32-33, 37, 40, 42-44, 46-47, 51, and 54 explained in Sections VI.A.3 (claims 28, 42), VI.A.4 (claims 29-30, 43-44), VI.A.5 (claims 32-33, 46, 47), VI.A.7 (claims 37, 51), and VI.A.8 (claims 40, 54), and these claims are obvious over Cholas-Petrovic-Takahiko. Ex. 1102, ¶ 242.

4. Claims 31, 45

The limitations of claims 31 and 45 are disclosed by Cholas-Petrovic-Takahiko. Ex. 1102, ¶ 243. As modified in view of Takahiko, the LPFs would be located after the adders of the complex mixer of a Petrovic stage 307 and would filter the corresponding complex signals output by the complex mixers. *Id.* Moreover, Cholas discloses that signals received by the STB comprise 6 MHz channels. Ex. 1158, [0045]; Ex. 1102, ¶ 243. Accordingly, claims 31 and 45 are obvious over Cholas-Petrovic-Takahiko. *Id.*

M. Cholas-Petrovic-Takahiko-Burris (Claims 28, 42)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Burris of the limitations of claims 28 and 42 explained in Section VI.B, and these claims are obvious over Cholas-Petrovic-Takahiko-Burris. Ex. 1102, ¶¶ 244-245, *see also* ¶¶ 47-76.

N. Cholas-Petrovic-Takahiko-Maalej (Claims 32-33 and 46-47)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Maalej of the limitations of claims 32-33 and 46-47 explained in Section VI.C, and these claims are obvious over Cholas-Petrovic-Takahiko-Maalej. Ex. 1102, ¶¶ 246-247, *see also* ¶¶ 47-76.

O. Cholas-Petrovic-Takahiko-Rabaey (Claims 1-9, 11, 13-22, 24, 26, 35-36, 49-50)

Claims 1-9, 11, 13-22, 24, 26, 35-36, and 49-50 are obvious over Cholas in view of Petrovic, Takahiko, and Rabaey. Ex. 1102, ¶¶ 248-252, *see also* ¶¶ 47-76.

1. Independent Claim 1

Limitation [1C], with the exception of the “via a serial interface” limitation, is disclosed by Cholas-Petrovic-Takahiko for the reasons explained in Section VI.L.1.b., and preamble [1A], limitation [1B] and the “via a serial interface” portion of limitation [1C] are disclosed by Cholas-Petrovic-Rabaey for the reasons explained in Section VI.D.3.a-b. Ex. 1102, ¶ 249. Modification in view of Takahiko does not affect modification in view of Rabaey, and claim 1 is obvious over Cholas-Petrovic-Takahiko-Rabaey. *Id.*

2. Independent Claim 14

Limitation [14C] is disclosed by Cholas-Petrovic-Takahiko for the reasons explained in Section VI.L.2.b, and preamble [14A] and limitations [14B] and [14D] are disclosed by Cholas-Petrovic-Rabaey for the reasons explained in Sections VI.D.4.a-VI.D.4.b and VI.D.4.d. Ex. 1102, ¶ 250. Modification in view of Takahiko does not affect modification in view of Rabaey, and claim 14 is obvious over Cholas-Petrovic-Takahiko-Rabaey. *Id.*

3. Claims 2-4, 6-9, 11, 13, 15-17, 19-22, 24, 26, 35-36, 49-50

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Rabaey of the limitations of claims 2-4, 6-9, 11, 13-17, 19-22, 24, 26, 35-36, and 49-50 explained in Sections VI.D.1 (claims 35-36, 49, 50), VI.D.2 (claims 34, 48), VI.D.5 (claims 2, 15), VI.D.6 (claims 3-4, 16-17), VI.D.8 (claims 6-7, 19-20), VI.D.9 (claims 8, 21), VI.D.10 (claims 9, 22), VI.D.11 (claims 11, 24), and VI.D.12 (claims 13 and 26), and these claims are obvious over Cholas-Petrovic-Takahiko-Rabaey. Ex. 1102, ¶ 251.

4. Claims 5, 18

Claims 5 and 18 add the same limitations as claims 31 and 45, are disclosed by Cholas-Petrovic-Takahiko for the reasons explained in Section VI.L.4, and are obvious over Cholas-Petrovic-Takahiko-Rabaey, as modification in view of Rabaey does not affect the disclosure of claims 5 and 18 by Cholas-Petrovic-Takahiko. Ex. 1102, ¶ 252.

P. Cholas-Petrovic-Takahiko-Rabaey-Burris (Claims 2, 15)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Rabaey-Burris of the limitations of claims 2 and 15 explained in Section VI.E, and these claims are obvious over Cholas-Petrovic-Takahiko-Rabaey-Burris. Ex. 1102, ¶¶ 253-254, *see also* ¶¶ 47-76.

Q. Cholas-Petrovic-Takahiko-Rabaey-Maalej (Claims 6-8, 19-21, 34, 48)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Rabaey-Maalej of the limitations of claims 6-8, 19-21, 34, and 48 explained in Sections VI.F.1-VI.F3, and these claims are obvious over Cholas-Petrovic-Takahiko-Rabaey-Maalej. Ex. 1102, ¶¶ 255-256, *see also* ¶¶ 47-76.

R. Cholas-Petrovic-Takahiko-Lee (Claims 38-39, 52-53, 55-61, 65-75, 79-82)

Claims 38-39, 52-53, 55-61, 65-75, and 79-82 are obvious over Cholas in view of Petrovic, Takahiko, and Lee. Ex. 1102, ¶¶ 257-261; *see also* ¶¶ 47-76.

1. Independent Claim 55

Limitation [55C] is disclosed by Cholas-Petrovic-Takahiko for the reasons explained in Section VI.L.1.b, and preamble [55A] and limitations [55B] and [55D] are disclosed by Cholas-Petrovic-Lee for the reasons explained in Sections VI.G.3.a-VI.G.3.b. Ex. 1102, ¶ 258. Modification in view of Takahiko does not affect modification in view of Lee, and claim 55 is obvious over Cholas-Petrovic-Takahiko-Lee. *Id*

2. Independent Claim 69

Limitation [69C] is disclosed by Cholas-Petrovic-Takahiko for the reasons explained in Section VI.L.1.b, and preamble [69A] and limitations [69B] and [69D] are disclosed by Cholas-Petrovic-Lee for the reasons explained in Sections VI.G.4.a-VI.G.4.b. Ex. 1102, ¶ 259. Modification in view of Takahiko does not affect

modification in view of Lee, claim 69 is obvious over Cholas-Petrovic-Takahiko-Lee. *Id.*

3. Claims 38-39, 52-53, 56-58, 60-61, 65-68, 70-72, 74-75, 79-82

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Lee of the limitations of claims 38-39, 52-53, 56-58, 60-61, 65-68, 70-72, 74-75, and 79-82 explained in Sections VI.G.1 (claims 38, 52), VI.G.2 (claims 39, 53), VI.G.5 (claims 57-58, 71-72), VI.G.7 (claims 60-61, 74-75), VI.G.8 (claims 65, 69), VI.G.9 (claims 66, 80), VI.G.10 (claims 67, 81), VI.G.11 (claims 68, 82), and VI.G.12 (claims 56, 70) and these claims are obvious over Cholas-Petrovic-Takahiko-Lee. Ex. 1102, ¶ 260.

4. Claims 59, 73

Claims 59 and 73 add the same limitations as claims 31 and 45, are disclosed by Cholas-Petrovic-Takahiko for the reasons explained in Section VI.L.4, and are obvious over Cholas-Petrovic-Takahiko-Lee, as modification in view of Lee does not affect the disclosure of claims 59 and 73 by Cholas-Petrovic-Takahiko. Ex. 1102, ¶ 261.

S. Cholas-Petrovic-Takahiko-Lee-Burris (Claims 56, 70)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Lee-Burris of the limitations of claims 56 and 70 explained in Section VI.H, and these claims are obvious over Cholas-Petrovic-Takahiko-Lee-Burris. Ex. 1102, ¶¶ 262-263, *see also* ¶¶ 47-76.

T. Cholas-Petrovic-Takahiko-Lee-Maalej (60-61, 74-75)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Lee-Maalej of the limitations of claims 60-61 and 74-75 explained in Section VI.I, and these claims are obvious over Cholas-Petrovic-Takahiko-Lee-Maalej. Ex. 1102, ¶¶ 264-265, *see also* ¶¶ 47-76.

U. Cholas-Petrovic-Takahiko-Lee-Maalej-Rabaey (Claims 62, 76)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Lee-Maalej-Rabaey of the limitations of claims 62 and 76 explained in Section VI.J, and these claims are obvious over Cholas-Petrovic-Takahiko-Lee-Maalej-Rabaey. Ex. 1102, ¶¶ 266-267, *see also* ¶¶ 47-76.

V. Cholas-Petrovic-Takahiko-Lee-Rabaey (Claims 10, 12, 23, 25, 63-64, 77-78)

Modification in view of Takahiko does not affect the disclosure by Cholas-Petrovic-Lee-Rabaey of the limitations of claims 10, 12, 23, 25, 63-64, and 77-78 explained in Section VI.K, and these claims are obvious over Cholas-Petrovic-Takahiko-Lee-Rabaey. Ex. 1102, ¶¶ 268-269, *see also* ¶¶ 47-76.

VII. GROUNDS FOR STANDING & FEE PAYMENT

Petitioner hereby certifies that the '866 patent is available for, and Petitioner is not barred or estopped from requesting, *inter partes* review challenging claims 1-82.

Pursuant to 37 C.F.R. § 42.103, the undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

VIII. CONCLUSION

Inter partes review should be instituted and claims 1-82 canceled.

Dated: February 16, 2024

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,934, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,852 words as counted by the Word Count feature of Microsoft Word and 82 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: February 16, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of this Petition for *Inter Partes* Review in connection with U.S. Patent No. 11,381,866 and supporting evidence to be served via FedEx Priority Overnight on February 16, 2024, on the following:

23446 - MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661
UNITED STATES

Dated: February 16, 2024

By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282

CLAIMS LISTING APPENDIX

U.S. Pat. No. 11,381,866

Designation	Claim Language
Claim 1	
[1A]	A cable television (TV) device comprising:
[1B]	a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and
[1C]	a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels, via a serial interface, without providing any of the plurality of undesired channels.
Claim 2	
2	The cable TV device of claim 1, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 3	
3	The cable TV device of claim 1, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 4	
4	The cable TV device of claim 3, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 5	
5	The cable TV device of claim 3, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.
Claim 6	

Designation	Claim Language
6	The cable TV device of claim 3, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.
Claim 7	
7	The cable TV device of claim 1, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.
Claim 8	
8	The cable TV device of claim 7, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 9	
9	The cable TV device of claim 1, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 10	
10	The cable TV device of claim 1, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 11	
11	The cable TV device of claim 1, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 12	
12	The cable TV device of claim 1, wherein: the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.
Claim 13	
13	The cable TV device of claim 1, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.
Claim 14	
[14A]	A cable TV device comprising:
[14B]	a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a

Designation	Claim Language
	plurality of desired channels and a plurality of undesired channels; and
[14C]	a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and
[14D]	wherein the plurality of digital down converters is operable to provide each digital channel output via a serial interface.
Claim 15	
15	The cable TV device of claim 14, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 16	
16	The cable TV device of claim 14, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 17	
17	The cable TV device of claim 16, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 18	
18	The cable TV device of claim 16, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.
Claim 19	
19	The cable TV device of claim 16, wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.
Claim 20	
20	The cable TV device of claim 14, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired

Designation	Claim Language
	channels, to provide a demodulated channel as the digital channel output.
Claim 21	
21	The cable TV device of claim 20, wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 22	
22	The cable TV device of claim 14, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 23	
23	The cable TV device of claim 14, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 24	
24	The cable TV device of claim 14, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 25	
25	The cable TV of claim 14, wherein: the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.
Claim 26	
26	The cable TV device of claim 14, wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.
Claim 27	
[27A]	A cable television (TV) device comprising:
[27B]	a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and
[27C]	a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels without providing any of the plurality of undesired channels, and

Designation	Claim Language
[27D]	wherein the cable TV device comprises a digital video recorder (DVR).
Claim 28	
28	The cable TV device of claim 27, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 29	
29	The cable TV device of claim 27, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 30	
30	The cable TV device of claim 29, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 31	
31	The cable TV device of claim 29, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.
Claim 32	
32	The cable TV device of claim 29, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.
Claim 33	
33	The cable TV device of claim 27, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.
Claim 34	
34	The cable TV device of claim 33, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.

Designation	Claim Language
Claim 35	
35	The cable TV device of claim 27, wherein: the DFE is operable to provide the plurality of desired channels via a parallel interface.
Claim 36	
36	The cable TV device of claim 27, wherein: the DFE is operable to provide the plurality of desired channels via a serial interface.
Claim 37	
37	The cable TV device of claim 27, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 38	
38	The cable TV device of claim 27, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 39	
39	The cable TV device of claim 27, wherein: the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.
Claim 40	
40	The cable TV device of claim 27, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.
Claim 41	
[41A]	A cable TV device comprising:
[41B]	a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a plurality of desired channels and a plurality of undesired channels; and
[41C]	a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and
[41D]	wherein the cable TV device comprises a digital video recorder (DVR).

Designation	Claim Language
Claim 42	
42	The cable TV device of claim 41, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 43	
43	The cable TV device of claim 41, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 44	
44	The cable TV device of claim 43, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 45	
45	The cable TV device of claim 43, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.
Claim 46	
46	The cable TV device of claim 43, wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.
Claim 47	
47	The cable TV device of claim 41, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired channels, to provide a demodulated channel as the digital channel output.
Claim 48	
48	The cable TV device of claim 47, wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 49	
49	The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide a plurality of

Designation	Claim Language
	digital channel outputs, comprising each digital channel output, via a parallel interface.
Claim 50	
50	The cable TV device of claim 41, wherein: the plurality of digital down converters is operable to provide each digital channel output via a serial interface.
Claim 51	
51	The cable TV device of claim 41, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 52	
52	The cable TV device of claim 41, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 53	
53	The cable TV of claim 41, wherein: the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.
Claim 54	
54	The cable TV device of claim 41, wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.
Claim 55	
[55A]	A cable television (TV) device comprising:
[55B]	a wideband analog-to-digital converter (ADC) configured to digitize a contiguous band of frequencies in an input signal, wherein the contiguous band of frequencies comprises a plurality of desired channels and a plurality of undesired channels; and
[55C]	a digital frontend (DFE) coupled to the wideband ADC, wherein the DFE is configured to concurrently select and provide each of the plurality of desired channels without providing any of the plurality of undesired channels, and
[55D]	wherein the cable TV device is operable to configure at least some of the plurality of desired channels as an output for a picture-in-picture display.
Claim 56	

Designation	Claim Language
56	The cable TV device of claim 55, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 57	
57	The cable TV device of claim 55, wherein: the DFE comprises a plurality of mixers, and each mixer, of the plurality of mixers, is operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 58	
58	The cable TV device of claim 57, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 59	
59	The cable TV device of claim 57, wherein: the DFE comprises a plurality of filters, and each filter, of the plurality of filters, is operable to filter the corresponding complex signal comprising a 6 MHz channel.
Claim 60	
60	The cable TV device of claim 57, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate the corresponding complex signal.
Claim 61	
61	The cable TV device of claim 55, wherein: the DFE comprises a plurality of digital demodulators, and each digital demodulator, of the plurality of digital demodulators, is operable to demodulate a desired channel, of the plurality of desired channels.
Claim 62	
62	The cable TV device of claim 61, wherein: the DFE is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 63	

Designation	Claim Language
63	The cable TV device of claim 55, wherein: the DFE is operable to provide the plurality of desired channels via a parallel interface.
Claim 64	
64	The cable TV device of claim 55, wherein: the DFE is operable to provide the plurality of desired channels via a serial interface.
Claim 65	
65	The cable TV device of claim 55, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 66	
66	The cable TV device of claim 55, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 67	
67	The cable TV device of claim 55, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 68	
68	The cable TV device of claim 55, wherein: the contiguous band of frequencies comprises a portion of a frequency spectrum of the input signal.
Claim 69	
[69A]	A cable TV device comprising:
[69B]	a wideband analog-to-digital converter (ADC) configured to digitize an input signal, wherein the input signal comprises a plurality of desired channels and a plurality of undesired channels; and
[69C]	a plurality of digital down converters coupled to the wideband ADC, wherein each digital down converter, of the plurality of digital down converters, is operable to generate a digital channel output corresponding to each desired channel, of the plurality of desired channels, and
[69D]	wherein the cable TV device is operable to provide a picture-in-picture display according to the plurality of digital channel outputs.
Claim 70	

Designation	Claim Language
70	The cable TV device of claim 69, wherein: the cable TV device comprises a cable network connector, and the input signal is operably communicated from the cable network connector to the wideband ADC via at least one of an analog amplifier and an analog filter.
Claim 71	
71	The cable TV device of claim 69, wherein: each digital down converter comprises a digital mixer operable to generate a corresponding complex signal comprising an in-phase (I) component and a quadrature (Q) component.
Claim 72	
72	The cable TV device of claim 71, wherein: the I and Q components of each corresponding complex signal are at baseband.
Claim 73	
73	The cable TV device of claim 71, wherein: each digital down converter comprises a filter operable to select the corresponding complex signal comprising a 6 MHz channel.
Claim 74	
74	The cable TV device of claim 71, wherein: each digital down converter comprises a digital demodulator operable to demodulate the corresponding complex signal to provide a demodulated channel as the digital channel output.
Claim 75	
75	The cable TV device of claim 69, wherein: each digital down converter comprises a digital demodulator operable to demodulate a desired channel, of the plurality of desired channels, to provide a demodulated channel as the digital channel output.
Claim 76	
76	The cable TV device of claim 75, wherein: the plurality of digital down converters is operable to provide a plurality of demodulated desired channels via a parallel interface.
Claim 77	
77	The cable TV device of claim 69, wherein: the plurality of digital down converters is operable to provide a plurality of digital channel outputs, comprising each digital channel output, via a parallel interface.

Designation	Claim Language
Claim 78	
78	The cable TV device of claim 69, wherein: the plurality of digital down converters is operable to provide each digital channel output via a serial interface.
Claim 79	
79	The cable TV device of claim 69, wherein: the plurality of desired channels comprises at least one cable broadcast channel.
Claim 80	
80	The cable TV device of claim 69, wherein: the plurality of desired channels comprises at least one channel delivered via a Data Over Cable Service Interface Specification (DOCSIS) protocol.
Claim 81	
81	The cable TV device of claim 69, wherein: the cable TV device comprises a digital video recorder (DVR).
Claim 82	
82	The cable TV device of claim 69, wherein: the plurality of desired channels and the plurality of undesired channels comprise a portion of a frequency spectrum of the input signal.