UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MONOLITHIC POWER SYSTEMS, INC.,

Petitioner,

v.

GREENTHREAD LLC,

Patent Owner.

U.S. PATENT NO. 8,421,195
PTAB Case No. IPR2024-00468

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,421,195 UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

TABLE OF CONTENTS

I. MANDATORY NOTICES **1**

A. Real Party-In-Interest 1

B. Related Matters 1

C. Counsel Service Information 3

D. 37 C.F.R. §42.8(b)(4): Service Information 3

II. PAYMENT OF FEES UNDER 37 C.F.R. §42.103 **3**

III. CERTIFICATION OF GROUNDS FOR STANDING **3**

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED **4**

A. Prior Art Printed Publications 4

B. Relief Requested 4

V. PERSON OF ORDINARY SKILL IN THE ART **5**

VI. CLAIM CONSTRUCTION **5**

VII. THE '195 PATENT AND BACKGROUND **7**

A. The '195 Patent's Purported Improvements **7**

B. General Background On Static Unidirectional Electric Drift Fields as Related to Semiconductor Layers Having Graded Dopant Profiles **9**

C. Patent Owner's Representation of Claim Scope **13**

VIII. SPECIFIC GROUNDS **17**

A. Ground I: Onoda Renders Obvious Claims 1, 2, 3, 5, and 6. 17

1. Independent Claim 1 17

a. Preamble: "A CMOS semiconductor device comprising:" 19

b. Element [1.1]: "a surface layer;" 20

c. Element [1.2]: "a substrate;" 23

d. Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;" 24

e. Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate," 28

f. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and" 32

g. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate." 34

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 40

3. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein the said drift layer is an epitaxial layer." 42

4. Dependent Claim 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient." 43

5. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient." 44

B. Ground II: Onoda in view of Nishizawa Renders Obvious Claims 1, 2, 3, 5, and 6. 46

1. Independent Claim 1 49

a. Preamble: "A CMOS semiconductor device comprising:" 49

b. Elements [1.1]-[1.4] 50

c. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and" 50

d. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a

second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate." 52

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 52

C. Ground III: Kawagoe Renders Obvious Claims 1, 2, 3, 5, and 6. 53

1. Independent Claim 1 54

a. Preamble: "A CMOS semiconductor device comprising:" 54

b. Element [1.1]: "a surface layer;" 55

c. Element [1.2]: "a substrate;" 58

d. Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;" 59

e. Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate," 63

f. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and" 70

g. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate." 74

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 80

3. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein the said drift layer is an epitaxial layer." 81

4. Dependent Claim 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient." 83

5. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient." 85

IX. THE BOARD SHOULD INSTITUTE IPR **87**

1. 35 U.S.C. § 314(a) 87

2. 35 U.S.C. § 325(d) 88

3. Prior Petitions Do Not Warrant Denying Institution 91

TABLE OF AUTHORITIES

FEDERAL CASES

Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH,
IPR2019- 01469 89

*Apple Inc. v. Uniloc 2017 L*LC,
IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020) 91

Becton, Dickinson, & Co. v. B. Braun Melsungen AG,
IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017) 88

Bowtech Inc. v. MCP IP, LLC,
IPR2019-00383, Paper 14 (P.T.A.B. Aug. 6, 2019) 89

Fasteners for Retail, Inc. v. RTC Indus., Inc.,
IPR2019-00994, Paper 9 (P.T.A.B. Nov. 5, 2019) 89

In re Epstein,
32 F.3d 1559 (Fed. Cir. 1994) 44, 46, 85, 87

Intel Corp. v. Greenthread, LLC,
IPR2023-00548 2

KSR Intern. Co. v. Teleflex, Inc.
550 U.S. 398 (2007) ..... passim

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C. 5

PopSockets LLC v. Flygrip, Inc.,
IPR2022- 00938 88

Samsung Electronics, Co., Ltd., v. Greenthread, LLC,
IPR2020-00289 2

Xilinx, Inc. v. Arbor Global Strategies, LLC,
IPR2020-01568, Paper No. 12 (P.T.A.B. Mar. 5, 2021) 91

OTHER CASES

Ex Parte Nico Hawley-Weld, Dan Volpe, & Ben Silverman,
No. APPEAL 2023-000345, 2022 WL 17495059 ..... 44, 46, 85, 87

Greenthread, LLC v. Cirrus Logic, Inc.,
Civil Action No. 1:23-cv-00369 1

Greenthread, LLC v. Intel Corp. et al.,
Case No. 6:22-cv-00105, Dkt. 96 6

Greenthread, LLC v. Intel Corp. et al.,
Case No. 6:22-cv-105-ADA ..... passim

Greenthread, LLC v. Intel Corporation,
Civil Action No. 6:22-cv-01293 2

Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.,
Civil Action No. 6:22-cv-00105 2

Greenthread, LLC v. Micron Technology, Inc. et al.,
Civil Action No. 1:23-cv-00333 2

Greenthread, LLC v. Monolithic Power Systems, Inc.,
Civil Action No. 1:23-cv-00579 1

Greenthread, LLC v. OmniVision Technologies, Inc.,
Civil Action No. 2:23-cv-00212 1

Greenthread, LLC v. OSRAM GmbH et al,
Civil Action No. 2:23-cv-00179 1

Greenthread, LLC v. Samsung Electronics Co. Ltd.,
Case No. 2-19-cv-00147 ..... 2, 5

Greenthread, LLC v Texas Instruments Incorporated,
Civil Action No. 2:23-cv-00157 1

Greenthread, LLC v. Western Digital Corporation et al,
Civil Action No. 1:23-cv-00326 2

FEDERAL STATUTES

35 U.S.C. § 103 ..... 4, 5

35 U.S.C. § 314(a) 87, 88

35 U.S.C. § 325(d) 88, 89

pre-America Invents Act.....4

RULES

Rule 42.104(a) 3

REGULATIONS

37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4) and 42.10(a).....3

37 C.F.R. § 42.8(b)(4) 3

37 C.F.R. § 42.10(b) 3

37 C.F.R. § 42.15(a)(1).....3

37 C.F.R. § 42.103.....3

TABLE OF EXHIBITS

Ex. 1001	U.S. Patent No. 8,421,195 (the "'195 Patent")
Ex. 1002	Prosecution History of the '195 Patent ("the Prosecution History")
Ex. 1003	Declaration of Dr. Stephen Campbell
Ex. 1004	Curriculum Vitae of Dr. Stephen Campbell
Ex. 1005	U.S. Patent No. 4,684,971 ("Payne")
Ex. 1006	U.S. Patent No. 4,907,058 to Sakai ("Sakai")
Ex. 1007	U.S. Patent No. 6,043,114 to Kawagoe, et al., ("Kawagoe")
Ex. 1008	Wolf and Tauber, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (2000)
Ex. 1009	U.S. Patent No. 4,160,985 ("Kamins")
Ex. 1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
Ex. 1011	U.S. Patent Application Publication No. 2003/0042511 ("Rhodes")
Ex. 1012	U.S. Patent Application Publication No. 2002/0102783 ("Fujimoto")
Ex. 1013	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
Ex. 1014	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
Ex. 1015	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 ("Watters Decl.")
Ex. 1016	IPR2020-00289, Patent Owner Preliminary Response
Ex. 1017	U.S. Pat. No. 11,121,222 (the "'222 Patent")
Ex. 1018	U.S. Pat. No. 11,316,014 (the "'014 Patent")

Ex. 1019	Civil Action No. 2:19-cv-00147-JRG, Dkt. 67 (E.D. Tex. Apr. 20, 2019)
Ex. 1020	Prosecution History of U.S. Pat. No. 11,121,222
Ex. 1021	Prosecution History of U.S. Pat. No. 11,316,014
Ex. 1022	U.S. Patent Application Publication No. 2004/0063288 ("Kenney")
Ex. 1023	Jaeger, *Introduction to Microelectronic Fabrication*, Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) ("Jaeger")
Ex. 1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics, dated June 30, 2023
Ex. 1025	U.S. Patent No. 4,435,896 ("Parrillo")
Ex. 1026	L.C. Parrillo, R.S. Payne et al., *Twin-Tub CMOS - A Technology for VLSI Circuits*, IEEE 1980 ("Parrillo2")
Ex. 1027	U.S. Patent Application Publication No. 2007/0045682 to Hong *et al*. ("Hong")
Ex. 1028	The Oxford American Dictionary and Language Guide, Oxford University Press (1996)
Ex. 1029	RESERVED
Ex. 1030	Patent Owner's Responsive Claim Construction Brief
Ex. 1031	RESERVED
Ex. 1032	Patent Owner's Sur-Reply Claim Construction Brief
Ex. 1033	Proposed Claim Constructions in the District Court Case
Ex. 1034	Redacted District Court Case Transfer Order
Ex. 1035	Civil Action No. 2:19-cv-00147-JRG, Dkt. 105 (E.D. Tex. Jul. 9, 2020)
Ex. 1036	Publication Declaration of Sylvia Hall-Ellis for Wolf

Ex. 1037	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105
Ex. 1038	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
Ex. 1039	Parrillo IEEE Citation List
Ex. 1040	Dictionary of Engineering, McGraw Hill (2003)
Ex. 1041	Rubin et al., *Ranges and Moments of Depth Distributions of Boron and Phosphorus Implanted into Silicon in the Energy Range 1.7 -5.0 MeV with an Eaton NV-GSD/VHE Implanter*, IEEE 1997 ("Rubin")
Ex. 1042	Certified translation of Japanese Unexamined Patent Application Publication No. H8-279598 ("Onoda")
Ex. 1043	Japanese Unexamined Patent Application Publication No. H8-279598, published on October 22, 1996
Ex. 1044	IPR2020-289, Termination Order
Ex. 1045	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
Ex. 1046	U.S. Pat. No. 5,384,476 (the "'576 Patent") ("Nishizawa")
Ex. 1047	U.S. Pat. No. 6,900,091 (the " '091 Patent") ("Williams")

Monolithic Power Systems, Inc. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-3, 5, and 6 (the "Challenged Claims") of U.S. Patent No. 8,421,195 (Ex. 1001, the "'195 Patent").

I. MANDATORY NOTICES

A. Real Party-In-Interest

Monolithic Power Systems, Inc. is the real party-in-interest.

B. Related Matters

The '195 Patent is the subject of the following active proceedings:

- *Greenthread, LLC v. Monolithic Power Systems, Inc.*, Civil Action No. 1:23-cv-00579 in the District of Delaware, filed May 26, 2023 ("MPS Litigation");
- *Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-00369 in the Western District of Texas, filed March 31, 2023;
- *Greenthread, LLC v Texas Instruments Incorporated*, Civil Action No. 2:23-cv-00157 in the Eastern District of Texas, filed April 6, 2023;
- *Greenthread, LLC v. OSRAM GmbH et al*, Civil Action No. 2:23-cv-00179 in the Eastern District of Texas, filed April 19, 2023; and
- *Greenthread, LLC v. OmniVision Technologies, Inc.*, Civil Action No. 2:23-cv-00212 in the Eastern District of Texas, filed May 10, 2023.

The '195 Patent was previously subject to the following proceedings, which are no longer pending:

- *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-00105 in the Western District of Texas ("Intel Litigation"), filed January 27, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6:22-cv-01293 in the Western District of Texas, severed December 21, 2022, and transferred to District of Oregon as 3:22-cv-02001;
- *Greenthread, LLC v. Western Digital Corporation et al*, Civil Action No. 1:23-cv-00326 in the District of Delaware, filed March 24, 2023;
- *Greenthread, LLC v. Micron Technology, Inc. et al.*, Civil Action No. 1:23-cv-00333 in the District of Delaware, filed March 24, 2023;
- *Greenthread, LLC v. Samsung Electronics Co. Ltd.*, Case No. 2-19-cv-00147, filed on April 30, 2019.
- *Samsung Electronics, Co., Ltd., v. Greenthread, LLC,* IPR2020-00289, filed on December 23, 2019.
- *Intel Corp. v. Greenthread, LLC,* IPR2023-00548, filed on January 30, 2023.

The'195 Patent is or was involved in the following PTAB proceedings as of today:

AIA review # 2	Filing date (mm/dd/yyyy) 1	Institution decision date (mm/dd/yyyy)	Termination date (mm/dd/yyyy)	Petitioner application #	Petitioner patent #	Petitioner	Petitioner tech center	PO/Respondent application #	PO/Responsent patent #	PO/Respondent	PO/Respondent tech center	Status
IPR2024-00266	12/11/2023					Semiconductor Com...		11622496	8421195	Greenthread, LLC	2800	Pending
IPR2024-00017	10/18/2023					Cirrus Logic, Inc. et al.		11622496	8421195	Greenthread, LLC	2800	Pending
IPR2023-00548	01/30/2023		05/18/2023			Intel Corporation		11622496	8421195	Greenthread, LLC	2800	Terminated-Settled
IPR2020-00289	12/23/2019		07/10/2020			Samsung Electronics ...		11622496	8421195	Greenthread LLC	2800	Terminated-Settled

C. Counsel Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints Miguel Bombach (Reg. No. 68,636) as its lead counsel, and Bing Ai (Reg. No. 43,312), John D. Esterhay (Reg. No. 73,512), John P. Schnurer (Reg. No. 52,196), Brianna Kadjo (Reg. No. 74,307), and Runkun (Justin) Jiang (Reg. No. 78,118) as its back-up counsel.

D. 37 C.F.R. §42.8(b)(4): Service Information

Petitioner concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address: PerkinsServiceMPS-GreenthreadIPR@perkinscoie.com

II. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 50-0665. Review of claims 1-3, and 5-6 is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '195 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims

on the grounds identified in this Petition.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Prior Art Printed Publications

The '195 Patent claims priority to September 3, 2004. Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '195 Patent:

- **Onoda** – Japanese Application H8-279598 to Onoda (Ex. 1043, certified translation 1042) published on October 22, 1996 and is prior art under §102(b).[1]
- **Kawagoe**: U.S. Patent No. 6,043,114 to Kawagoe et al. (Ex. 1007) issued on March 28, 2000 and is prior art under §102(b).
- **Nishizawa:** U.S. Patent No. 5,384,476 to Nishizawa et al. (Ex. 1046) issued on January 24, 1995 and is prior art under §102(b).

B. Relief Requested

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Campbell (Ex.1003).

Ground	Basis	Challenged Claims	Reference(s)
I	§ 103	1-3, 5-6	Onoda

[1] Citations to §§102/103 are to the pre-America Invents Act (pre-AIA) versions.

II	§ 103	1-3, 5-6	Onoda and Nishizawa
III	§ 103	1-3, 5-6	Kawagoe

V. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") of the subject matter of the '195 Patent would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. (Ex. 1003, ¶ 17.) Additional education might compensate for a deficiency in experience, and vice-versa. *Id*.

VI. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). No terms need to be construed to resolve the issues presented in this Petition.[2]

[2] The Eastern District of Texas construed "single drift layer . . . having a graded concentration of dopants . . . said drift layer further having a first static unidirectional electric drift field" as "single drift layer . . . having a concentration of dopants at the interface of the single drift layer and surface layer that is different than the concentration of dopants at the interface of the single drift layer and the substrate . . . said drift layer further having a first static unidirectional electric drift field." Ex. 1019 at 17 (*Greenthread, LLC v. Samsung Electronics Co., Ltd*., et al., Case No.

The file history of the '195 Patent shows that the originally filed specification of the '195 Patent does not use or mention the claim terms of "surface layer" and "drift layer"/ "single drift layer." (Ex. 1002 at 8) See, for example, the published patent publication No. US20070158790A1 which is the original filed application for the '195 Patent. On May 14, 2010, Patent Owner added new claims that became the patented claims in a response to the 4th, final office action dated Dec. 30, 2009 by introducing the above claim terms. (Ex. 1002 at 163-66)

In the Intel Litigation, Patent Owner took positions on the meaning of certain claim terms, which are listed below. (*Greenthread, LLC v. Intel Corp. et al.,* Case No. 6:22-cv-00105, Dkt. 96, Ex. 1030.)

Claim Term	**Patent Owner's Proposed Construction**
"surface layer"	Plain and ordinary meaning ("a layer at the surface") (Ex. 1030 at 9-15.)
"substrate"	Plain and ordinary meaning ("underlying layer") (Ex. 1030 at 15-18.)
"active region"	Plain and ordinary meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed") (Ex. 1030 at 19-20.)
"unidirectional electric drift field"	Plain and ordinary meaning (Ex. 1030 at 20-25.)
"to aid carrier movement from … [to/towards] …"	Plain and ordinary meaning (Ex. 1030 at 25-30.)

2:19-cv-00147-JRG (Dkt. 67) (April 20, 2020).) Whether or not this construction is proper is not material to institution, and no construction need be entered.

"well region"	Plain and ordinary meaning ("a doped region that surrounds the active region of a semiconductor device") (Ex. 1030 at 30-31.)

In the Intel Litigation, the Court provided its "preliminary constructions" in advance of the claim construction hearing, in which the Court offered a "preliminary construction" of plain and ordinary meaning as to each of the above-listed terms.[3] (*See* Ex. 1037 (Intel's Ex. 1037).) Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition. Petitioner reserves the right to respond to any purported claim constructions that Patent Owner raises.

VII. THE '195 PATENT AND BACKGROUND

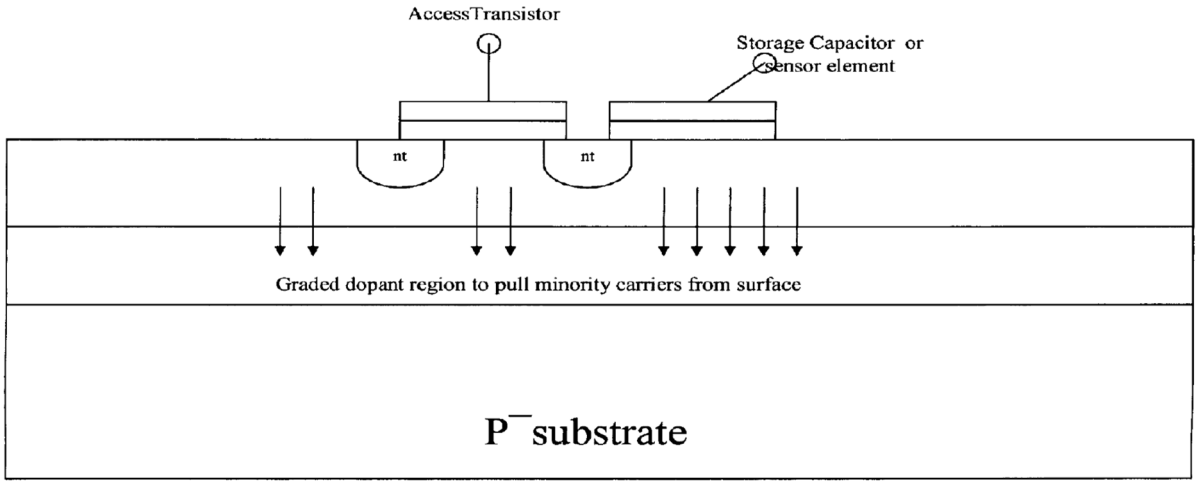
A. The '195 Patent's Purported Improvements

The '195 Patent is directed to a CMOS semiconductor device whose semiconductor layers have a graded dopant concentration that creates an electric drift field that sweeps minority carriers from the semiconductor's active region at the surface to its substrate. ('195 Patent at Abstract & 3:30-33.)

The '195 Patent states that some prior art bipolar junction transistors employed

[3] The court in the Western District of Texas did provide a note that the plain and ordinary meaning of well region does not include portions of a well. (Intel Litigation Preliminary Constructions, Ex. 1037 at 4 (stating that "portions of a well are not well regions").)

a graded dopant base to create an "'aiding drift field' to enhance the diffusing minority carrier's speed from emitter to collector." ('195 Patent at 1:34-36.) According to the '195 Patent, however, "most semiconductor devices … still use a uniformly doped drift epitaxial region in the base." (*Id.* at 1:36-40.) The '195 Patent claims the prior art semiconductor devices could be improved by providing a graded dopant region between the surface and the substrate to carry minority carriers from the surface to the substrate as quickly as possible (indicated by arrows in FIG. 5(b)). (*Id.* at 3:30-35; *see also id.* at 4:28-29; 2:51-67 (stating that the dopant gradient exists in the epitaxial layer).) This purported improvement is illustrated below from FIG. 5(b).)



('195 Patent at FIG. 5(b).)

The '195 Patent did not, however, use a new or unknown dopant profile to achieve the purported novelty. Rather, it utilized known doping techniques to known physical layers. (Ex. 1003 at ¶¶ 23, 25-28.). A POSITA would have understood that semiconductor layers and regions are doped to control their conductance and electric

drift fields, including by using gradient doping profiles. (*Id.* at ¶ 27-31.) This was admitted as known by the '195 Patent, at least with regard to the base portion of some prior art transistors ('195 Patent at 1:34-36; FIG. 1 (illustrating a doping impurity gradient in the base portion of a bipolar junction transistor that varies with depth)). In any event, the existence of, benefits from, and technologies necessary to achieve such gradient doping were known to a POSITA at the time, as the Patent Owner subsequently admitted during prosecution. Furthermore, when describing various dopant profiles that could be used (*e.g.*, "linear, quasi linear, exponential"), the '195 Patent merely lists them as possible options (*id.* at 2:40-42), confirming that they were known and that a POSITA would know how to implement them without further explanation.

The purported novelty in the '195 Patent is merely taking known doping techniques, applied to known layers, to create electric drift fields to diffuse minority carriers to a substrate. (Ex. 1003 at ¶¶ 27-31.) As demonstrated by Petitioner's prior art (Onoda, Nishizawa, and Kawagoe), all of this was well-known and obvious at the time of the purported invention.

B. General Background On Static Unidirectional Electric Drift Fields as Related to Semiconductor Layers Having Graded Dopant Profiles

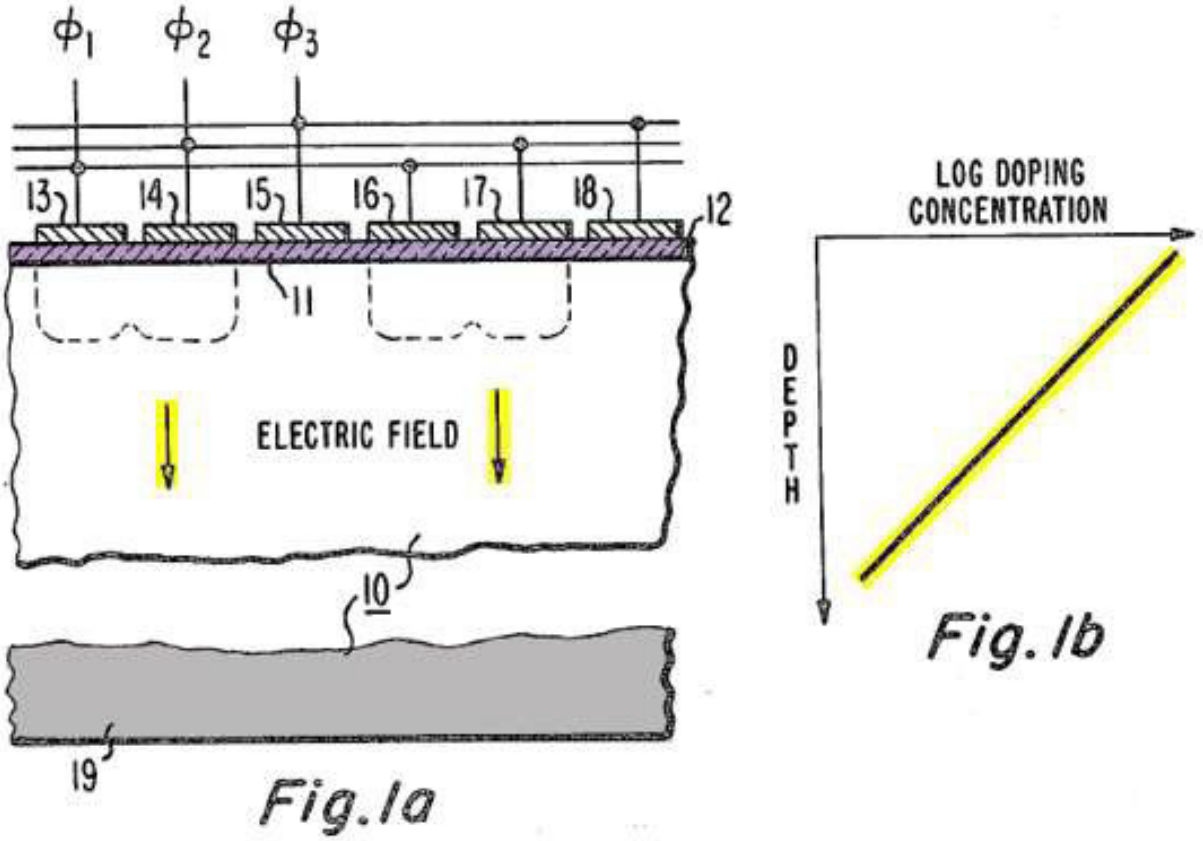
At the time of the alleged invention, Patent Owner represented that it was well-known that a graded dopant concentration creates a static unidirectional electric drift field. During prosecution, Patent Owner admitted that both upward and downward-

sloping graded dopant concentrations were known and created an "inherent 'built-in' unidirectional electric field'":

> "[T]he graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carriers into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant."

(Ex. 1002 at 289-290 (underlining in original).)

Patent Owner further represented to the USPTO that "a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way… Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept 'down' … or 'up…'" (Ex. 1002 at 289.) Patent Owner cited Jastrzebski in support. (*Id*. at 290.) In Jastrzebski, the graded-dopant concentration is "decreasing with depth" from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. (Ex. 1010 at 5:14-22.)

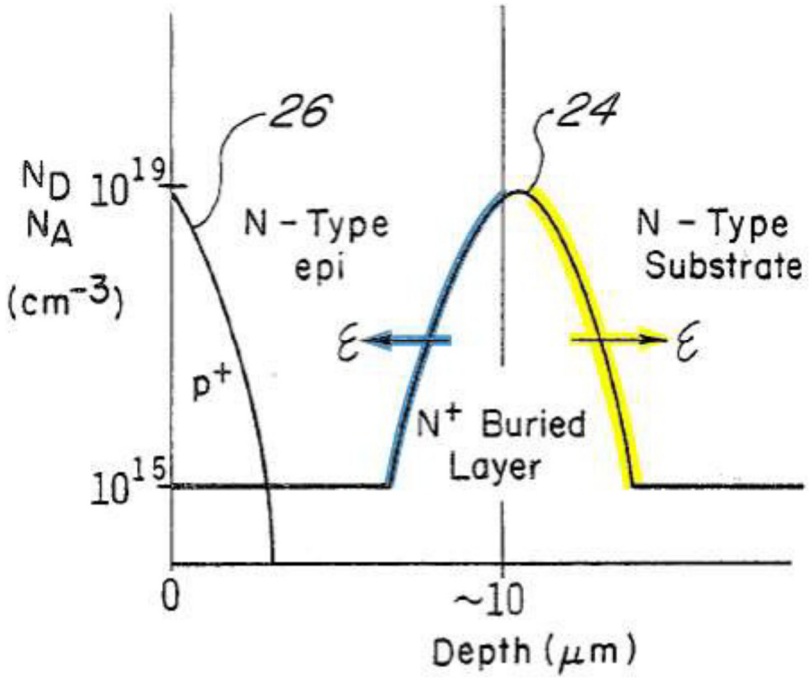


(Ex. 1010 at FIGS. 1a, 1b.)

Jastrzebski teaches that this downward-sloping graded-dopant concentration creates an electric drift field that "force[s] most of the charge carriers … deep into the substrate[.]" (*Id.* at 5:14-22; *id.* at 2:27-32 ("This is done by creating a field, such as a drift field, in the semiconductor substrate to sweep minority charge carriers…into the bulk [substrate], away from the electrode-bearing surface of the substrate.").)

Patent Owner made the same representation to the Patent Office regarding the Kamins prior art. (Ex. 1002 at 237-238, 253-254.) According to Patent Owner, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant

concentrations, respectively. (*Id.* at 237, 253 (citing Ex. 1009 at 3:6-13, FIGS. 2-3).)



(Ex. 1009 at FIG. 3.)

Patent Owner explained that Kamins "show[s] minority carrie[r]s accelerated into the substrate." (*Id.* (citing Ex. 1009, FIG. 2 and quoting Ex. 1009 at 3:6-13 ("carriers… accelerated… away from the surface… into the substrate")).) According to Patent Owner, the electric field associated with the downward-sloping graded concentration at depth beyond ~10μm causes "[minority] carriers created [in that region to be] … accelerated into the substrate …." (*Id.* (citing Ex.1009 at 3:6-13, FIGS. 2-3); Ex.1030 at 24 (Kamin's "bottom electric field [(yellow)] draws a minority carrier from the substrate to a deeper part of the substrate."); Ex.1009 at 2:67-3:14 ("The non-uniform dopant concentration in the substrate creates electric fields in the substrate indicated by arrows labeled 'ε' in [Kamins'] FIGS. 2 and 3" such that "[minority]

carriers created below the maximum dopant concentration are accelerated into the substrate."), FIG. 2 (referring to these carriers as "photogenerated minority carriers"), 2:11-16 (same).)

Patent Owner also described "static," and conceded that "Kamins (US 4,160,985), just like the '195 Patent, discloses the presence of a 'static' drift field: 'because the drift field is created by graded concentration of dopants which does not change over time.'" (Ex.1002 at 318 (citing Ex.1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and Ex.1002, 302- 03), 333 (same).)

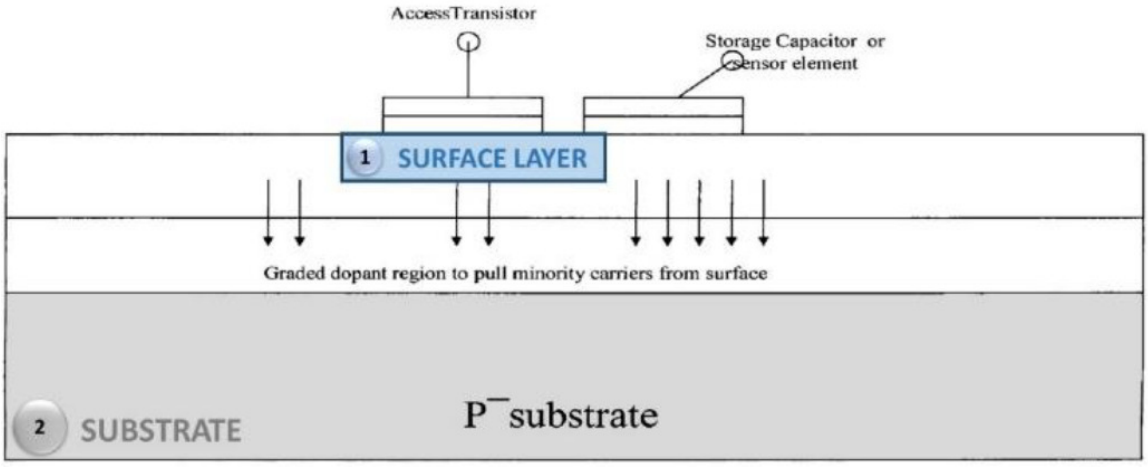
C. Patent Owner's Representation of Claim Scope

In a prior litigation against Intel, Patent Owner provided a description of the '195 Patent's claim terms with reference to its figures, which depict Patent Owner's perceived claim scope. *See* Ex. 1030 (*Greenthread, LLC v. Intel Corp. et al.,* Case No. 6:22-cv-105-ADA). Provided below is a Patent-Owner-created graphic of claim 1 of the '195 Patent:

Term	U.S. Patent No. 8,421,195, Claim 1 (195:1)
1	A CMOS Semiconductor device comprising: a **surface layer**;
2	a **substrate**;
3	an **active region** including a source and a drain, disposed on one surface of said surface layer;
4 5	a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static **unidirectional electric drift field** **to aid the movement of minority carriers from said surface layer to said substrate**; and
6	at least one **well region** disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

(*Id.* at 5 (annotations by Patent Owner).)

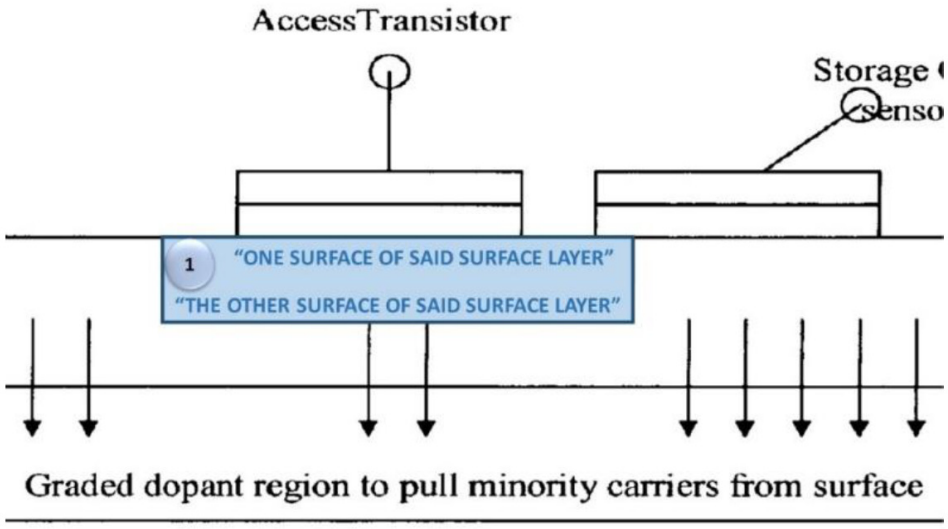
Patent Owner also annotated FIG. 5(b) to demonstrate each term's purported support. Shown below, Patent Owner identified a "surface layer" in blue and described it as "a layer at the surface of the silicon." (*Id.* at 6.)



(*Id.* at 6 (annotations by Patent Owner).)

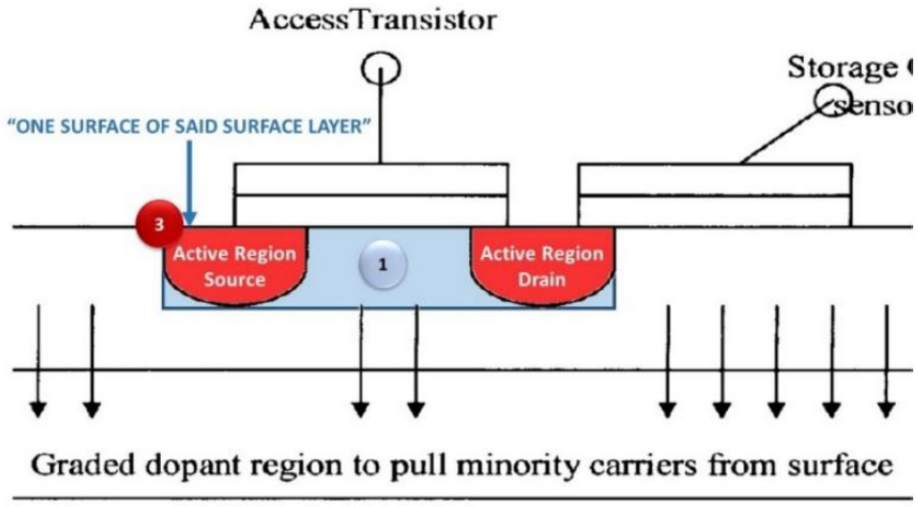
The "surface layer" as described by Patent Owner has two surfaces, "one

surface" and "the other surface" each on opposite ends of the "surface layer."



(*Id.* at 6 (annotations by Patent Owner).)

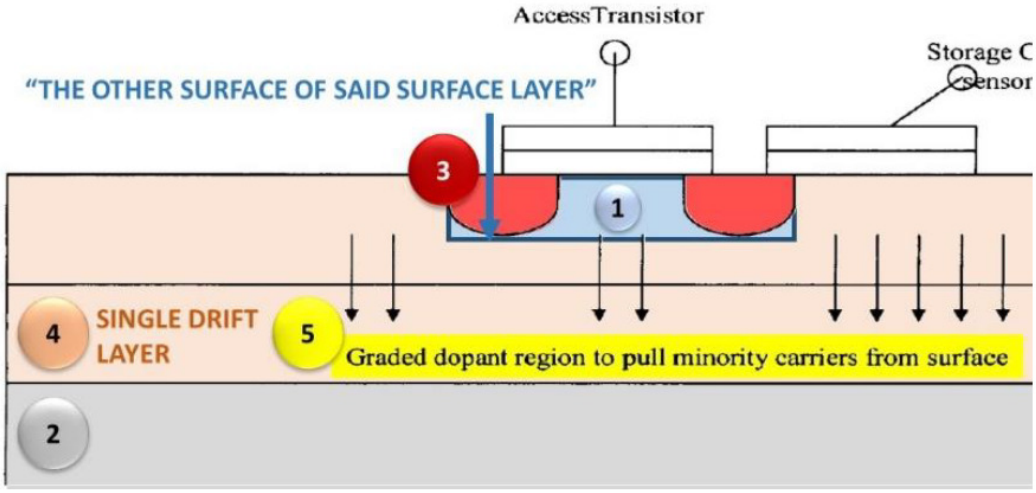
According to Patent Owner, "[t]he 'active region' is a doped region where a transistor can be formed" and is disposed on "one surface of said surface layer." (*Id.* at 7.)



(*Id.* at 7 (annotations by Patent Owner).)

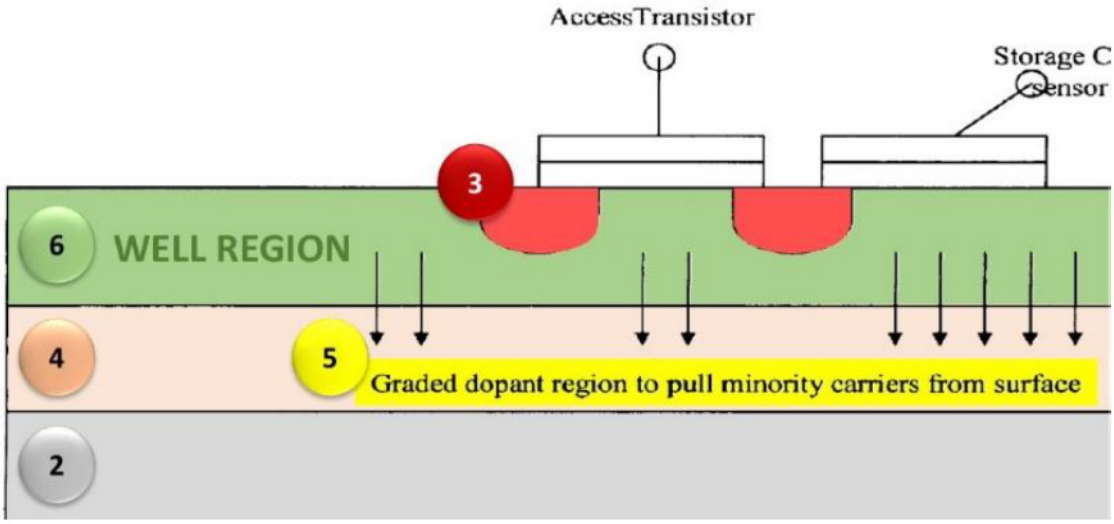
Patent Owner argued in claim construction that the "single drift layer [is]

disposed between 'the other surface of said surface layer' and the substrate. The single drift layer has a graded concentration of dopants" that "create an electric field that aids in the movement of minority carriers." (*Id.* at 7.)



(*Id.* at 7 (annotations by Patent Owner).)

Finally, Patent Owner argued that "there is a well region disposed in the single drift layer." (*Id.* at 7.) According to Patent Owner, "POSITAs normally use the term 'well region' to describe the doped silicon that surrounds the source and drain." (*Id.* at 4.)



(*Id.* at 7 (annotations by Patent Owner).)

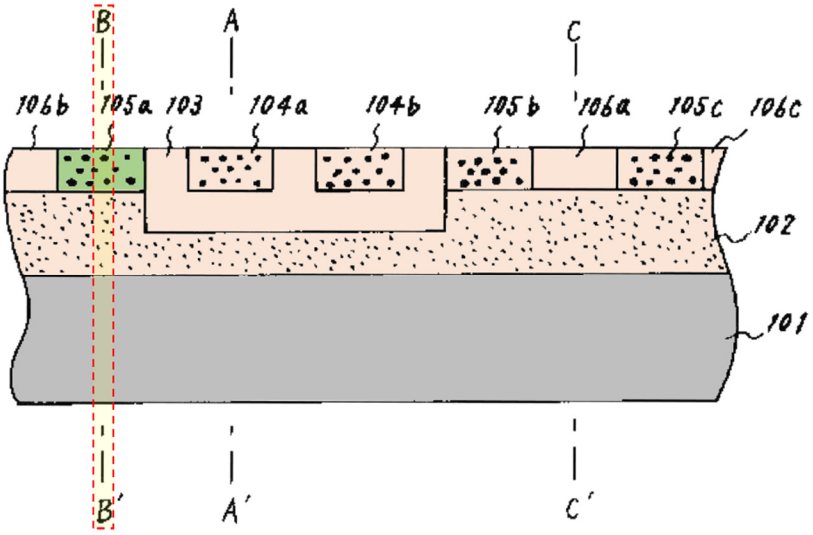
VIII. SPECIFIC GROUNDS

A. Ground I: Onoda Renders Obvious Claims 1, 2, 3, 5, and 6.

1. Independent Claim 1

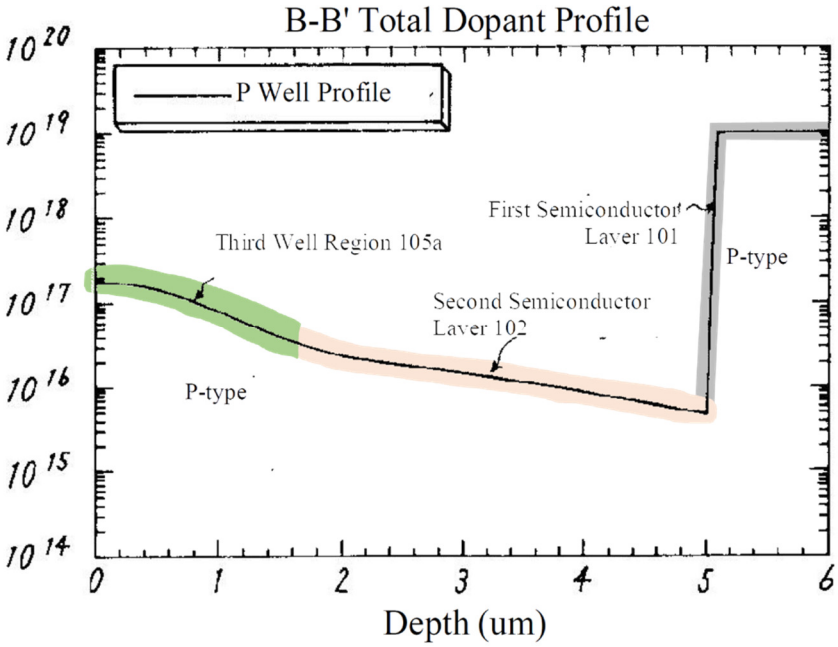
Onoda teaches a CMOS device that has a dopant profile where the dopant concentration gradually decreases from the surface of the device—through the epitaxial layer—to the substrate. This is depicted in the cross-sectional B-B' of FIG. 8 (shown in FIG. 11, both excerpted below), where the dopant gradient decreases from the surface, through the well-region (green),[4] through the epitaxial layer 102 (tan), to the substrate 101 (grey). (Onoda at [0046]-[0047], [0052].)

[4] There are several well regions; only a single one is emphasized and discussed in the grounds (*i.e.* 105a).



(Onoda at FIG. 8.)

As can be seen from the below, the impurity concentration decreases from the surface to the substrate (the X-axis represents depth while the Y-axis represents concentration of impurities).



(Onoda at FIG. 11.)

The purported novelty of the '195 Patent matches Onoda's structure. Onoda's

dopant profile consists of two layers (105a and 102) that create a unidirectional electric field, where such a field would accelerate minority carrier electrons from the surface toward the substrate. (Ex. 1003 at ¶¶ 32-34, 72-83.) This matches the '195 Patent's purported improvement; it claims that the prior art was deficient because it purportedly provided uniformly doped epitaxial regions ('195 Patent at 1:36-40) while the purported invention provided—as an improvement—a graded dopant layer [or region] between the surface layer and the substrate to sweep unwanted minority carriers into the substrate. (*Id.* at 3:30-35.)

Onoda thusly renders obvious claims 1, 2, 3, 5, and 6 as detailed below.

a. Preamble: "A CMOS semiconductor device comprising:"

To the extent the preamble is limiting, Onoda discloses a CMOS semiconductor device.

Onoda discloses both N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the circuitry of its flash memory devices. (Onoda at [0052], [0044]-[0045], FIG. 2, Claim 2.) A POSITA would have understood this to disclose CMOS because: (a) CMOS is a complimentary pair of NMOS and PMOS transistors and (b) CMOS was at the time (and still is) the dominant fabrication technology used in memory devices. (Ex. 1003 at ¶¶ 55-57.) Onoda further mentions that one of the objectives of the invention "is to provide a semiconductor integrated device … with improved resistance to latch-up" (*id.* at [0006]), which a POSITA would have

understood to be a problem of CMOS transistors. (Ex. 1003 at ¶ 56.)

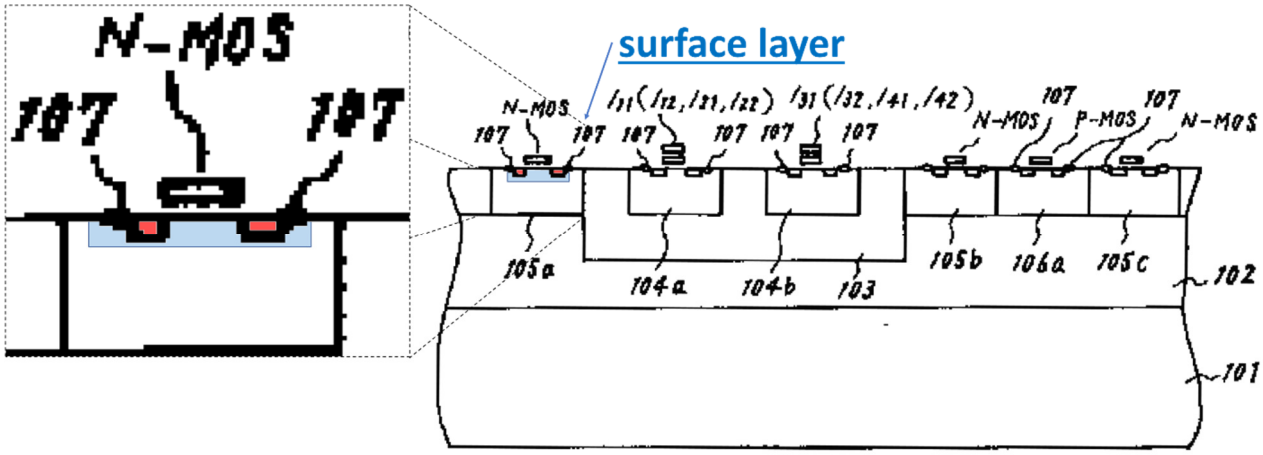
Furthermore, by the 1980s, CMOS had become the dominant IC fabrication technology and has remained so to the present day. (*Id.* at ¶ 55-57.) Flash memory devices have been fabricated almost exclusively with CMOS since at least the late 1980s. (*Id.*). Thus, when Onoda was published, a POSITA would understand its teachings to be directed to CMOS-based fabrication technologies and a POSITA would have thusly understood Onoda to disclose CMOS. (*Id.*)

To the extent Patent Owner argues that Onoda does not teach CMOS and that the preamble is limiting, it would have nonetheless been obvious to employ the teachings of Onoda to CMOS devices. CMOS devices are complimentary MOS devices, which use complimentary NMOS and PMOS transistors, and Onoda teaches a single device with both. (Onoda at FIG. 3.) A POSITA would have found it obvious to apply Onoda's teachings in a well-known CMOS structure, which is almost universally used in memory devices. (Ex. 1003 at ¶ 57.) A POSITA would have found it obvious to try, would have yielded predictable results, and would have been the application of known techniques to achieve those results. (*Id.*)

b. Element [1.1]: "a surface layer;"

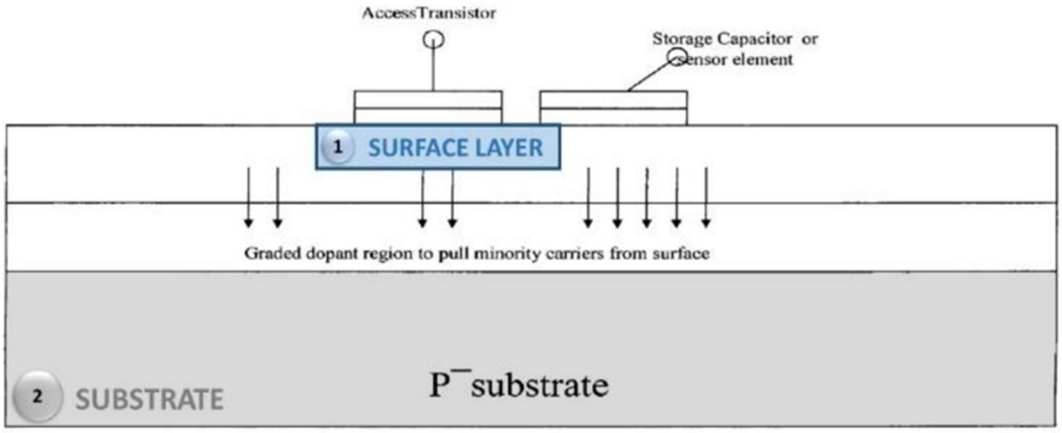
Onoda teaches a surface layer (annotated blue, below). Onoda's surface layer is shown below in a region of the NMOS transistor (excerpted below) within the doped p-well region 105a, where the well has source/drain regions (the active region discussed in more detail in Element [1.3]). (Onoda at [0043] ("105a, 105b, and 105c

are P-type [] well regions"); *see also id.* at [0044], Claim 2 ("floating gate electrode formed over the second well region, positioned between the source region and the drain region").) As can be seen from the below, Onoda's surface layer is at the surface of semiconductor substrate 101, and the source and drain regions (red) of Onoda's transistors are in that layer. (Ex. 1003 at ¶¶ 58-59.)



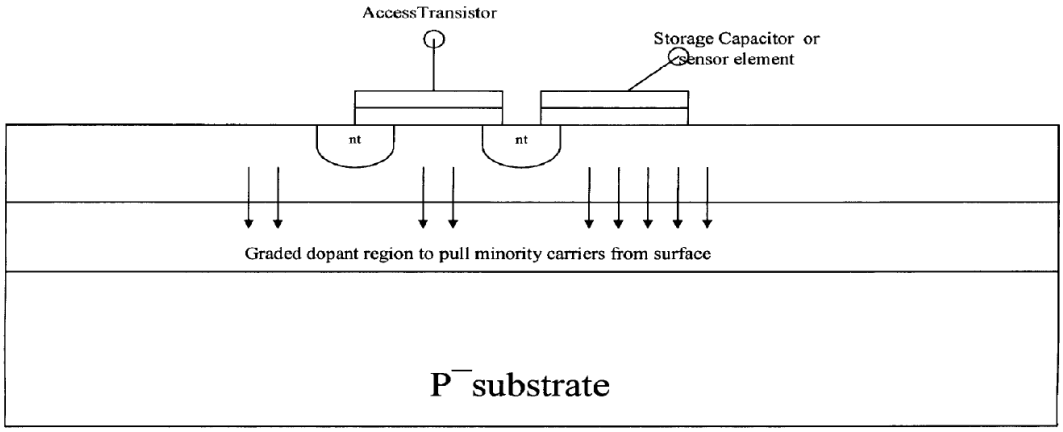
(Onoda at FIG. 3.)

Onoda's teaching of the "surface layer" matches Patent Owner's articulation of the '195 Patent's claim scope. Patent Owner annotated FIG. 5(b) to depict its purported scope of "surface layer" (the region surrounding the active region), and further argued in construction that the "surface layer" refers to "a layer at the surface of the silicon." (Ex. 1030 at 13.) This matches Onoda's teachings.



(Ex. 1030 at 6 (annotations to FIG. 5(b) of the '195 Patent by Patent Owner).)

Patent Owner annotated over FIG. 5(b) obscuring some regions (*e.g.*, the source/drain); a non-annotated version of the '195 Patent is excerpted below, which illustrates the active region.



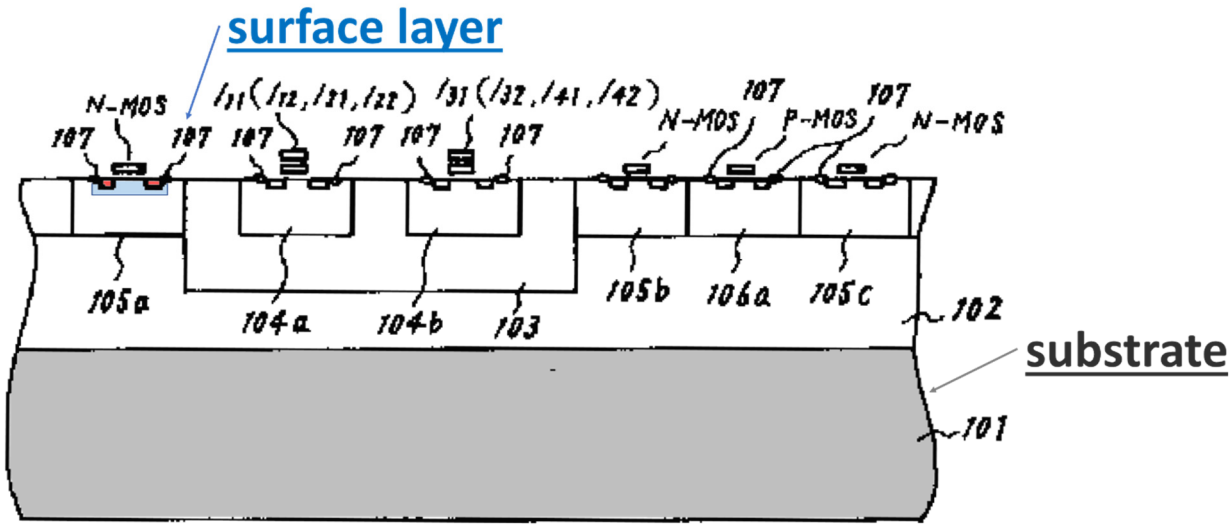
('195 Patent at FIG. 5(b).)

Onoda teaches the "surface layer" in an identical manner as described by the '195 Patent's purported written description support of this same limitation, and thusly discloses Element [1.1].

c. Element [1.2]: "a substrate;"

Onoda discloses this element.

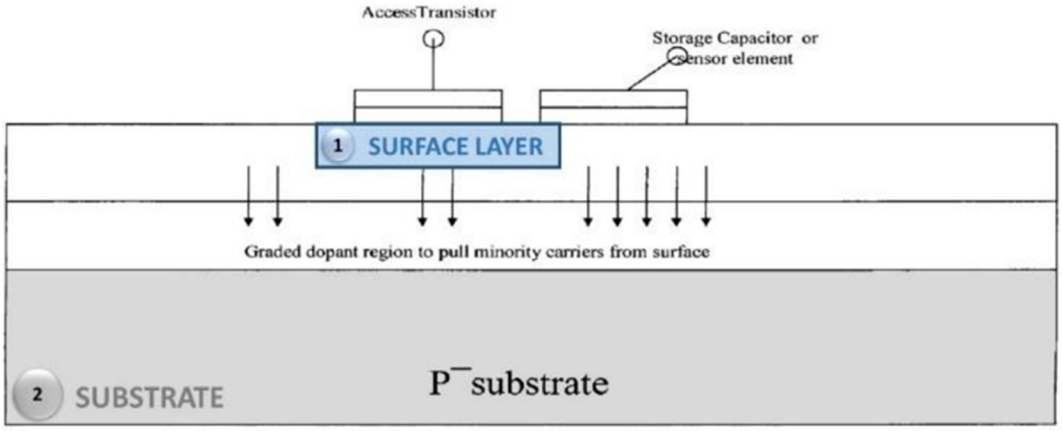
Onoda discloses "a semiconductor substrate 100" on which the flash memory is formed. (Onoda at [0041] ("FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention").) Within the semiconductor substrate is element 101 (annotated grey, below), which "is a first semiconductor layer made from a heavily-doped … P-type silicon substrate." (*Id.*). Shown below is FIG. 3 with element 101, the "p-type silicon substrate" (annotated in grey). (*Id.* at [0041]; *see also id.* at "Brief Description of the Drawings" describing FIGS. 1 through 14 as describing features of the "first embodiment.")



(Onoda at FIG. 3.)

Similar to the "surface layer," Onoda's teaching of the "substrate" matches Patent Owner's district court claim construction, where it construed the "substrate" as "an underlying layer." (Ex. 1030 at 15.) Patent Owner's annotations to FIG. 5(b) of

the '195 Patent are below.



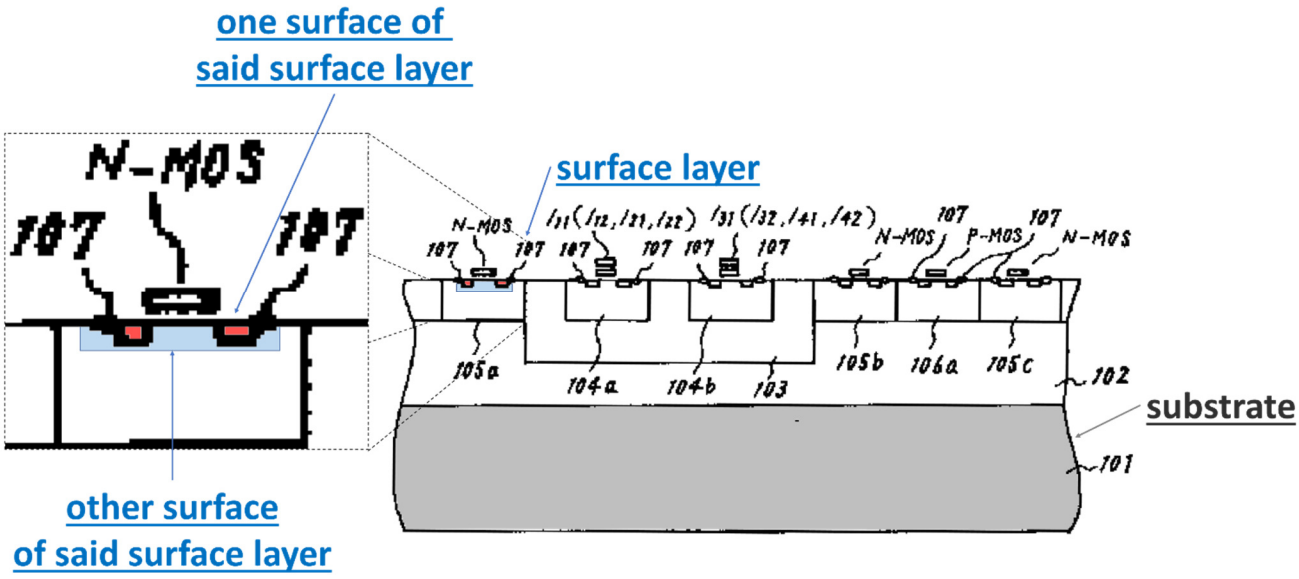
((Ex. 1030 at 6) (annotations by Patent Owner).)

Onoda thusly discloses Element [1.2].

d. Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

Onoda discloses this element.

As depicted in annotated FIG. 3 below, the surface layer contains a source and drain which form an active region. (Onoda at [0029] ("each a memory cell having a source region comprising an N-type diffusion layer, a drain region comprising an N-type diffusion layer that is separate from the source region, a floating electrode formed over a channel region that is positioned between the source region and the drain region, with a gate oxide film, comprising a tunnel oxide film, interposed therebetween, and a control gate electrode disposed facing the floating gate electrode with an interlayer insulating films interposed therebetween."), [0043] ("105a, 105b, and 105c are P-type [] well regions"); *see also id.* at [0044], Claim 2 ("floating gate electrode formed over the second well region, positioned between the source region and the drain region").)



(Onoda at FIG. 3 (active region called out for greater emphasis).)

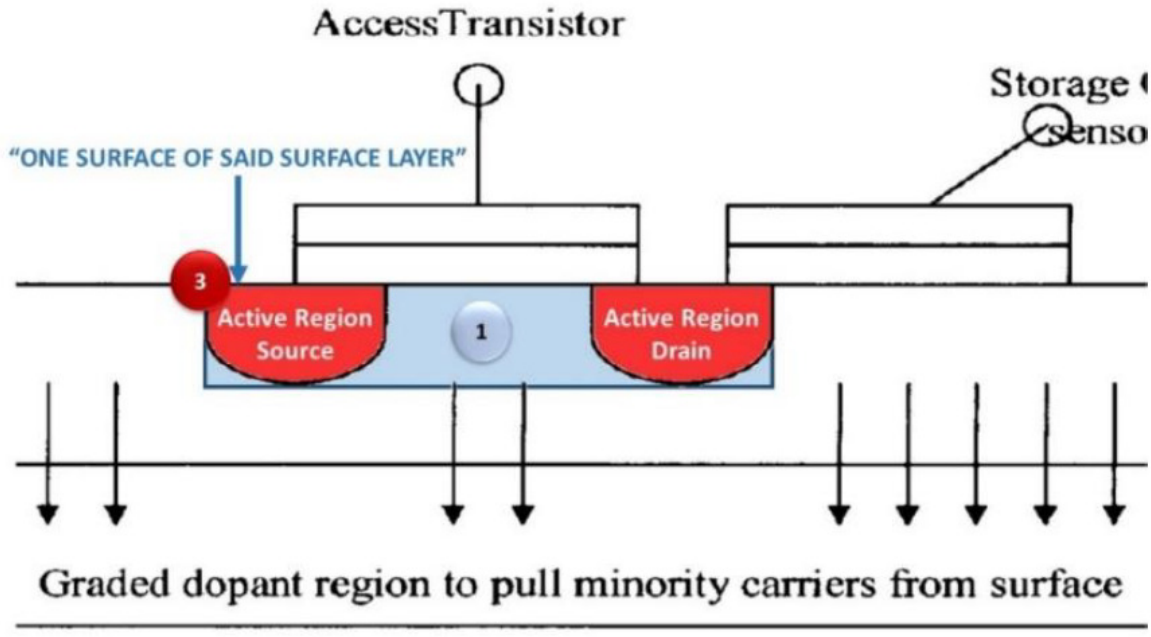
The active region is disposed to the top surface of the surface layer, *i.e.*, the claimed "one surface on said surface layer." (Ex. 1003 at ¶¶ 62-65). This orientation—and discussion of each respective region—matches Patent Owner's articulation during claim construction in the district court. There, Patent Owner likened the orientation to a ceiling fan in a room, stating:

> "By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the ceiling fan is spinning around like a propeller on the roof of the house. Instead it means that the ceiling fan is hanging from the ceiling ***inside*** the room. The same is true about the active region and the surface layer."

(Ex. 1030 at 11 (emphasis added).)

Patent Owner further annotated FIG. 5(b) of the '195 Patent to depict this

orientation, where the active region source and drains were disposed on the surface of the surface layer (similar to Onoda's FIG. 3). (Ex. 1003 at ¶¶ 63-64.)

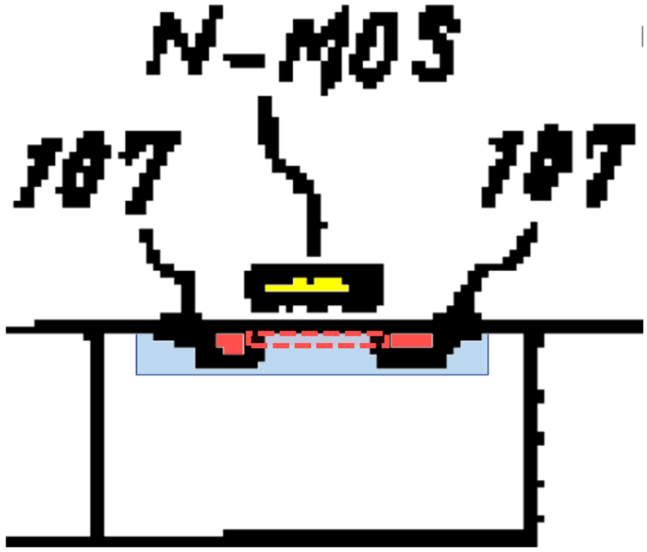


((Ex. 1030 at 7) (annotations by Patent Owner).)

Onoda thusly teaches the "an active region including a source and a drain, disposed on one surface of said surface layer."

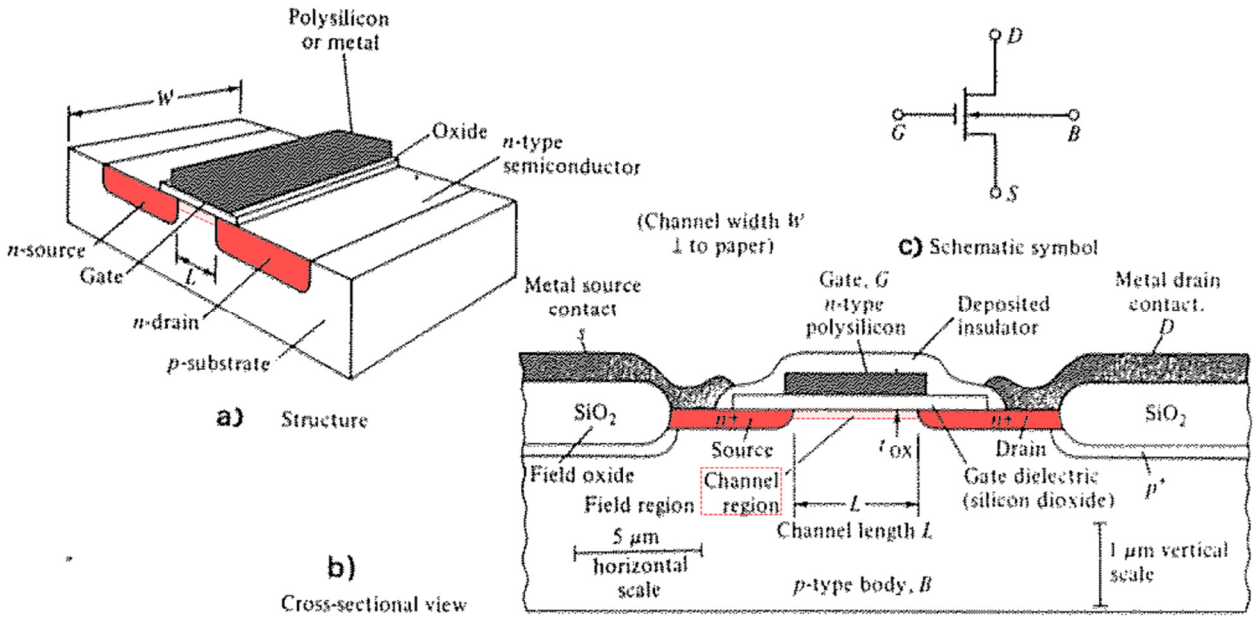
Furthermore, a POSITA would have understood that the above-described source and drain configurations of Onoda disclose an active region. (Ex. 1003 at ¶ 64.) As depicted in the enlarged excerpt of FIG. 3, below, a charge applied to gate electrode (annotated yellow, *see, e.g.,* Onoda at [0029] ("a floating electrode formed over a channel region that is positioned between the source region and the drain region")) causes a conductive channel (annotated in dashed-red) to form between the source and drain. (Ex. 1003 at ¶¶ 64-65.) A POSITA would understand the source, drain, and

channel to be an active region. (*Id.*)



(Onoda at FIG. 3 (Excerpted).)

This understanding of source, gate, drain, and transistor operation is confirmed via *Wolf and Tauber*, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions." (Ex. 1008 at 299; *see also* Ex. 1030 at 4-5 (Patent Owner acknowledging that a channel is formed between a source and drain to form an active region); Ex. 1003 at ¶ 65.)



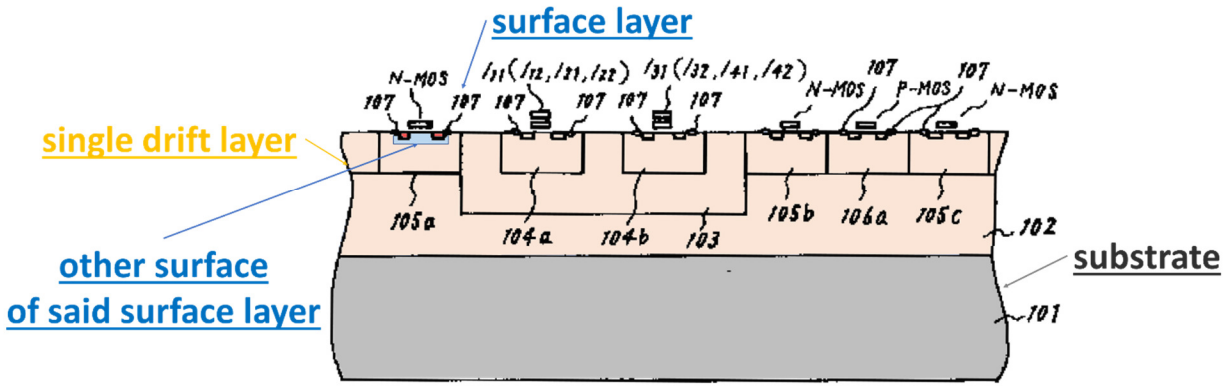
(Ex. 1008B at FIG. 5-1.)

Onoda thusly discloses Element [1.3].

e. Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate,"

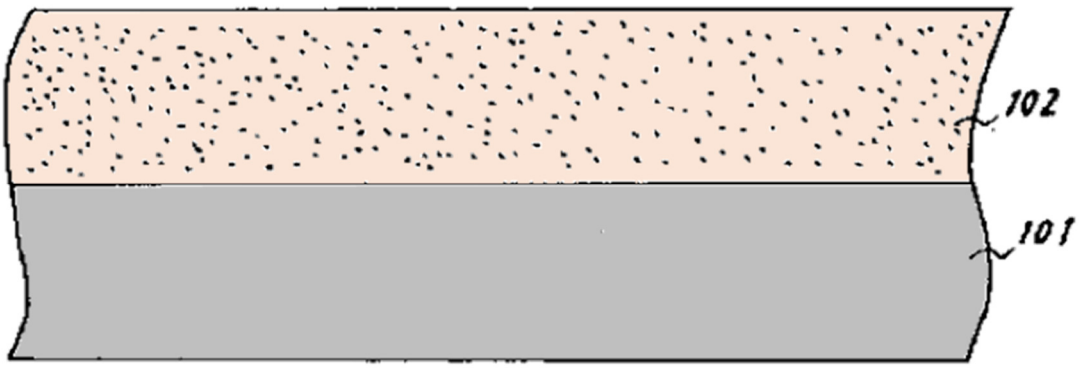
Onoda discloses this limitation.

Onoda discloses a single drift layer. In Onoda's FIG. 3, the second semiconductor layer 102 is an example of the claimed single drift layer (annotated tan, below). This single drift layer is "disposed between the "other surface of said surface layer" (the bottom surface) and the "substrate."



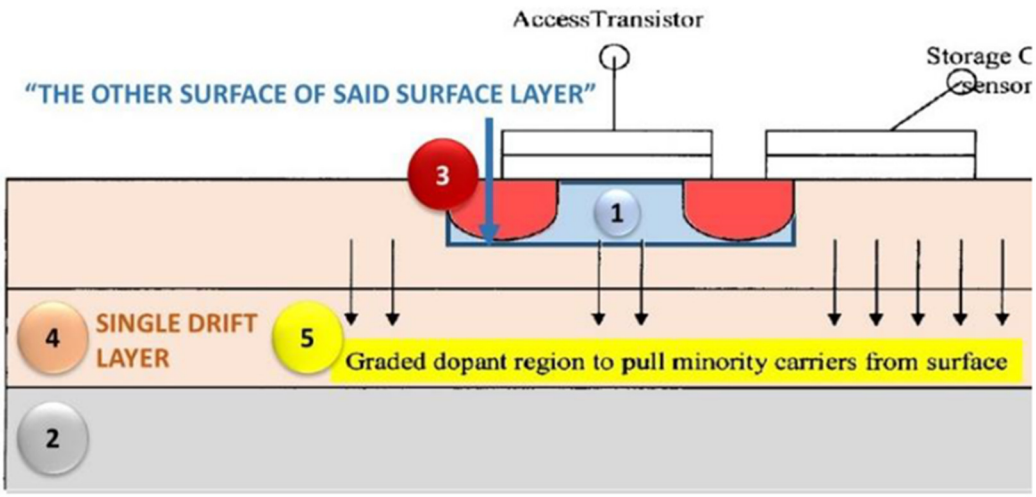
(Onoda at FIG. 3.)

The single drift layer is demonstrated in the intermediate processing step of FIG. 5, below, prior to well formation. (Onoda at [0047]; *see also id.* at FIGS. 10-12 (showing final dopant profiles); *see also id.* at [0041]-[0051].)



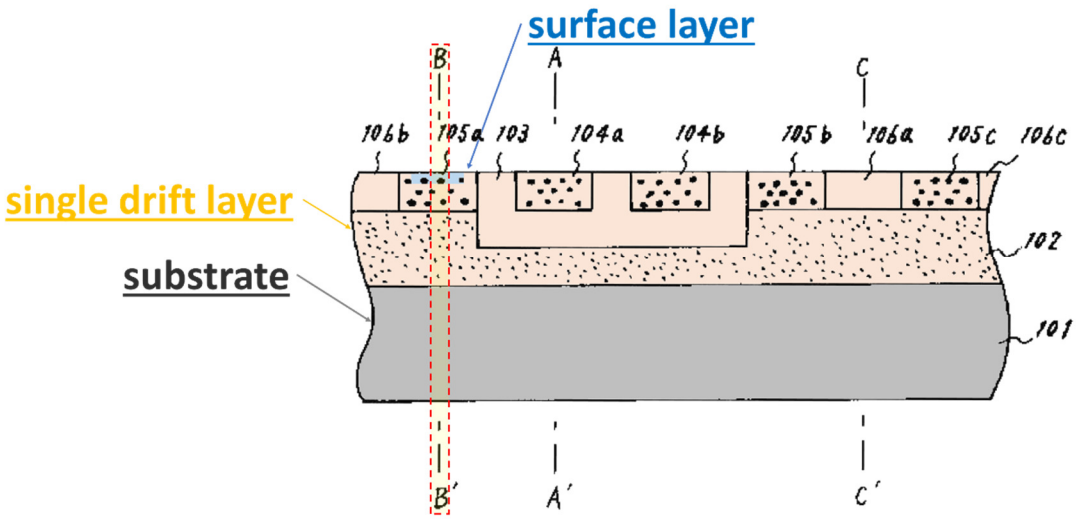
(Onoda at FIG. 5.)

Onoda's teachings further match Patent Owner's district court claim construction annotations to FIG. 5(b) of the '195 Patent. There, Patent Owner provided annotations demonstrating the position of the single drift layer in relationship to the surface layer's other surface and the substrate, where the single drift layer was below the surface layer.

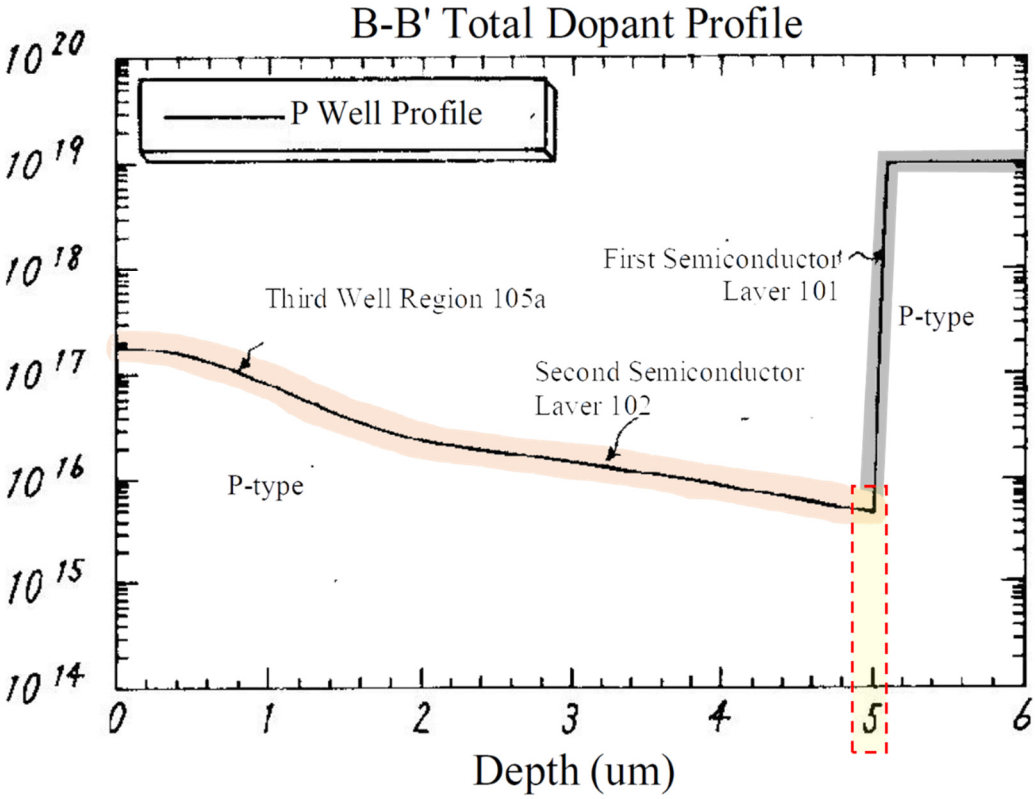


((Ex. 1030 at 7) (annotations by Patent Owner).)

Onoda's single drift layer further has a graded concentration of dopants extending between the surface layer and the substrate. FIG. 8 depicts the semiconductor device of Onoda, and FIG. 11 demonstrates that device's dopant profile of the portion marked as B-B' (cross-section annotated yellow). (Onoda at [0052].)



(Onoda at FIG. 8.)



(Onoda at FIG. 11.)

Comparing the two figures, Onoda's semiconductor device has a dopant profile whose impurities decrease from the surface, *i.e.*, depth 0, to the substrate, *i.e.*, depth of 5 um. (Onoda at [0046] (stating that the p-type epitaxial layer 102 has a thickness of about 5um); *see also id.* at [0052] ("both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly"); *see also id.* at [0047] (describing doping layer 102), [0048]-[0050] (stating how wells are created, which is discussed in further detail in Element [1.6]).) And, to create the gradient, Onoda describes implanting dopants and thereafter thermally diffusing them. (*Id.* at [0047]-

[0050].). Onoda thusly discloses a dopant profile with a downward doping gradient from the surface to the substrate. (Ex. 1003 at ¶¶ 66-71.).

Onoda thusly discloses Element [1.4].

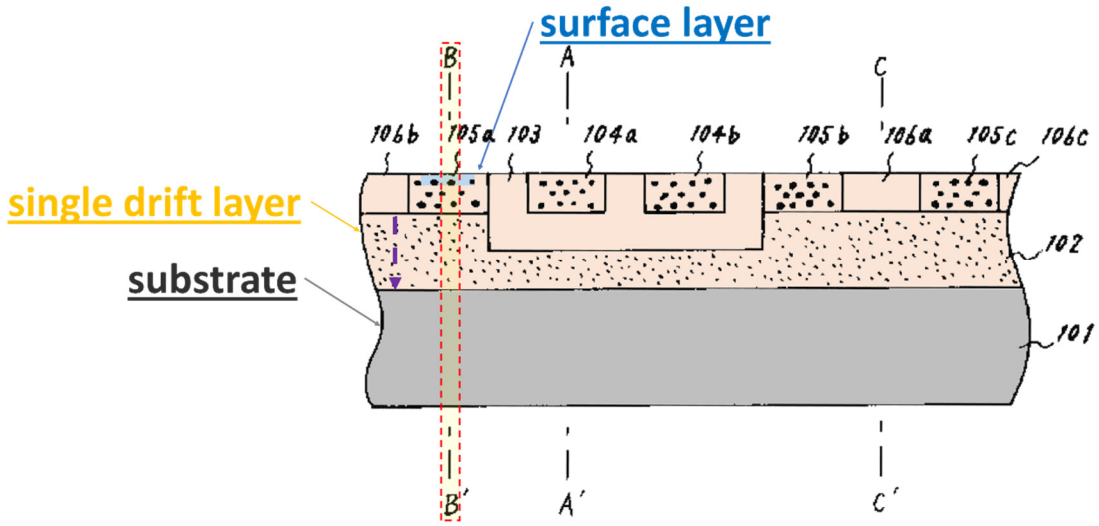
f. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

Onoda teaches this element.

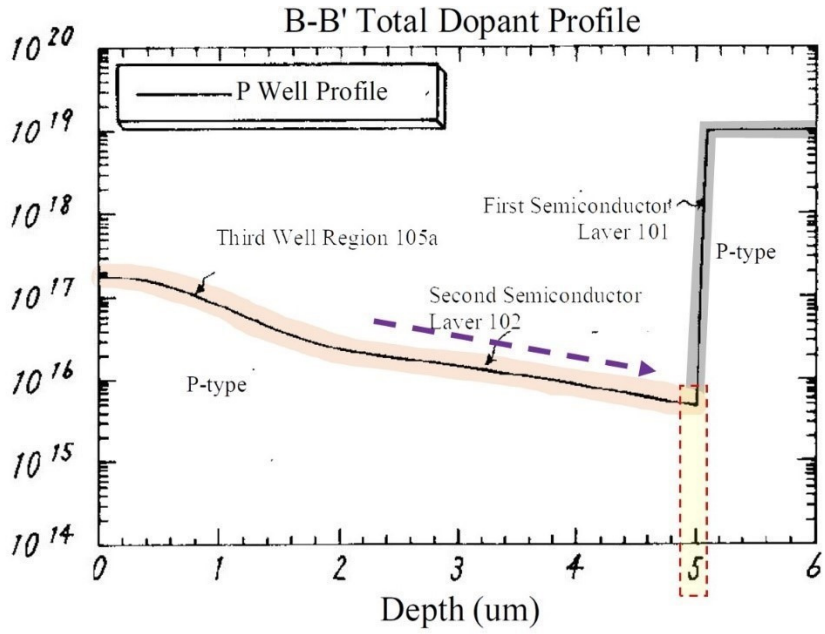
As discussed above with regard to Element [1.4], Onoda discloses a single drift layer (tan) having a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (gray, starting at the 5 μm depth level).

The below annotation of Onoda's FIGS. 8 and 11 depicts the first static unidirectional electric drift field (purple arrow)[5] that aids in the movement of minority carriers from the surface to the substrate, at a depth corresponding to Onoda's second semiconductor layer 102 (tan).

[5] The arrow indicates the movement of minority carriers from the surface layer to the substrate. (Ex. 1003 at ¶¶ 72-74). A POSITA would understand that the field would be in the opposite direction. (*Id.*)



(Onoda at FIG. 8.)



(Onoda at FIG. 11.)

As Patent Owner conceded during prosecution, a POSITA would have further understood that a downward-sloping graded-dopant concentration creates an inherent built-in unidirectional electric drift field to aid the movement of minority carriers. As detailed in section VII.B at pages 9-12, the Patent Owner in prosecution described a

downward graded dopant profile as providing an "inherent 'built-in' unidirectional electric field" that moves carriers into the substrate. (*Supra* at 9.) Moreover, a POSITA would have understood this to be an inherent property of a downward sloping doping gradient. (Ex. 1003 at ¶ 73.)

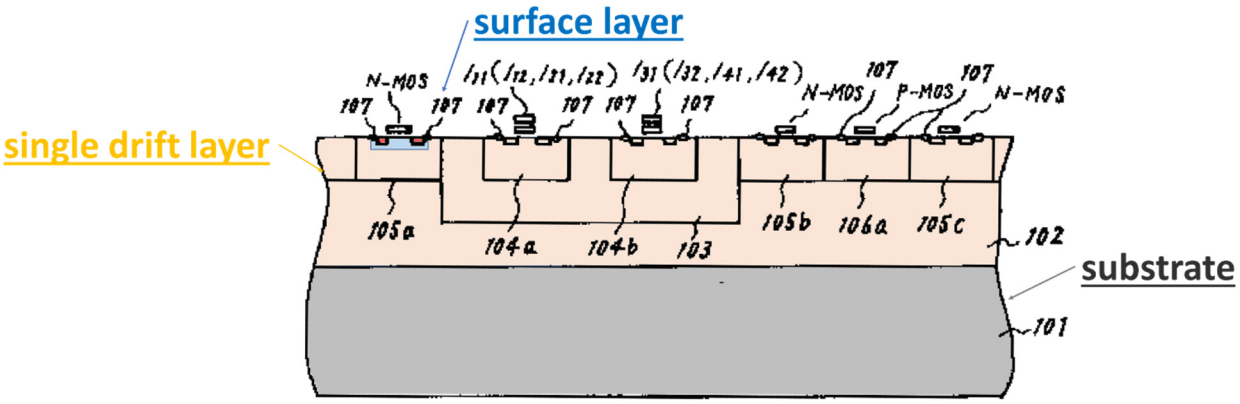
Furthermore, the static unidirectional electric drift field would have been understood to be static. (*Id.* at 74.) As discussed in [1.4], the dopant profile is created through ion implantation and thermal diffusion techniques and is thusly set once the device has been fabricated. (Onoda at [0047]-[0050]; *see also* Ex. 1003 at ¶¶ 66-71, 74.) In other words, this would have understood to be static to a POSITA. (Ex. 1003 at ¶ 74.) Patent Owner also described "static" similarly during prosecution, stating that a semiconductor device with a fabricated dopant profile provides a static unidirectional electric field. (Ex. 1002 at 318 (citing Ex. 1009), 333.) Consequently, a POSITA would have understood Onoda's downward sloping gradient to provide a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. (Ex. 1003 at ¶¶ 72-74.)

Onoda thusly discloses Element [1.5].

g. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

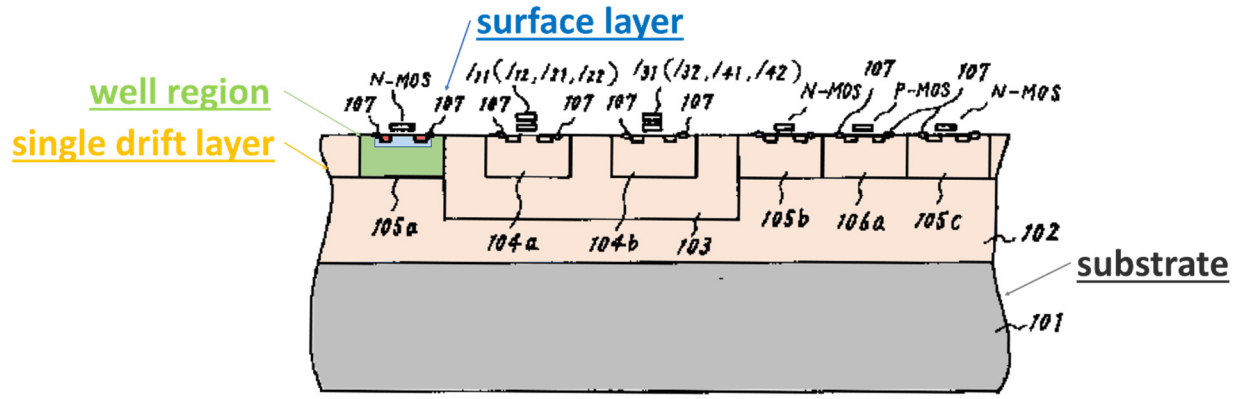
Onoda discloses this element.

Onoda discloses a well region disposed in the single drift layer. As described in Element [1.4], Onoda has a single drift layer (epitaxial layer 102, tan). (*See also* Onoda at [0046].)



(Onoda at FIG. 3.)

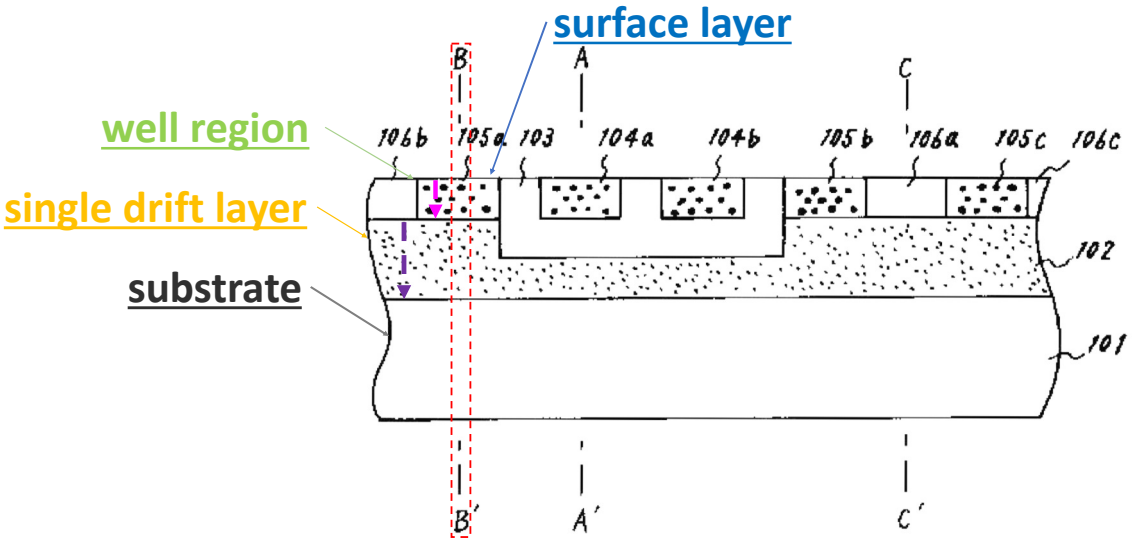
As shown below, disposed within that single drift layer is a well region (green) which is within the claimed single drift layer. (Onoda at [0042] ("105a, 105b, and 105c are P-type third well regions formed in the surface of the second semiconductor layer 102"); *see also id.* at [0044] ("the plurality of N-channel MOS transistors is formed in the third well regions 105a, 105b, 105c.").)



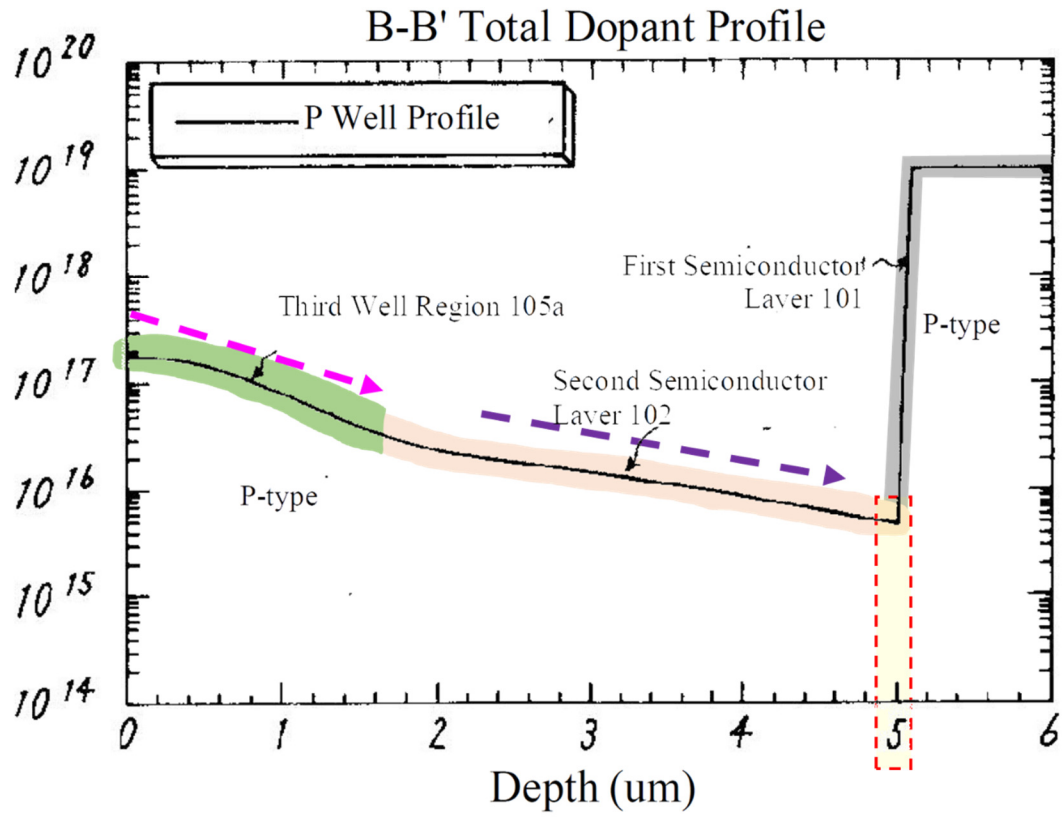
(Onoda at FIG. 3.)

Onoda discloses the steps to form the P-wells and the N-wells (including the exemplary claimed "well region") in the lightly-doped semiconductor layer 102. (Onoda at [0048]-[0050].) After forming the epitaxial second semiconductor layer 102, an N-type dopant (*e.g.*, phosphorus P) is implanted and heat treatment is carried out to form an N-type first well region 103 with a depth of about 3 μm. (*Id.* at [0048].) Thereafter, a P-type dopant (*e.g.*, boron B) is implanted to form P-type implantation layers 104a, 104b and 105a through 105c, and an N-type dopant is implanted to form N-type implantation layers 106a through 106c. (*Id.* at [0049].) Finally, after carrying out heat treatment, P-type second well regions 104a and 104b, P-type third well regions 105a through 105c, and N-type fourth well regions 106a through 106c are formed in the second semiconductor layer 102, as illustrated in FIG. 8 below. (*Id.* at [0050].) The well formation is depicted in FIG. 8, where P-well regions 105a, 105b, 105c, 104a and 104b and N-well regions 103, 106a, 106b and 106c are formed in semiconductor layer 102. (*Id.* at [0042], [0048]-[0050].)

Onoda discloses that its well region has a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. As noted in Element [1.5], FIG. 11 depicts the gradient profile of cross-sectional B-B' of FIG. 8 (annotated in yellow). (*See also* Onoda at [0052].) Both figures are provided below.



(Onoda at FIG. 8.)



(Onoda at FIG. 11.)

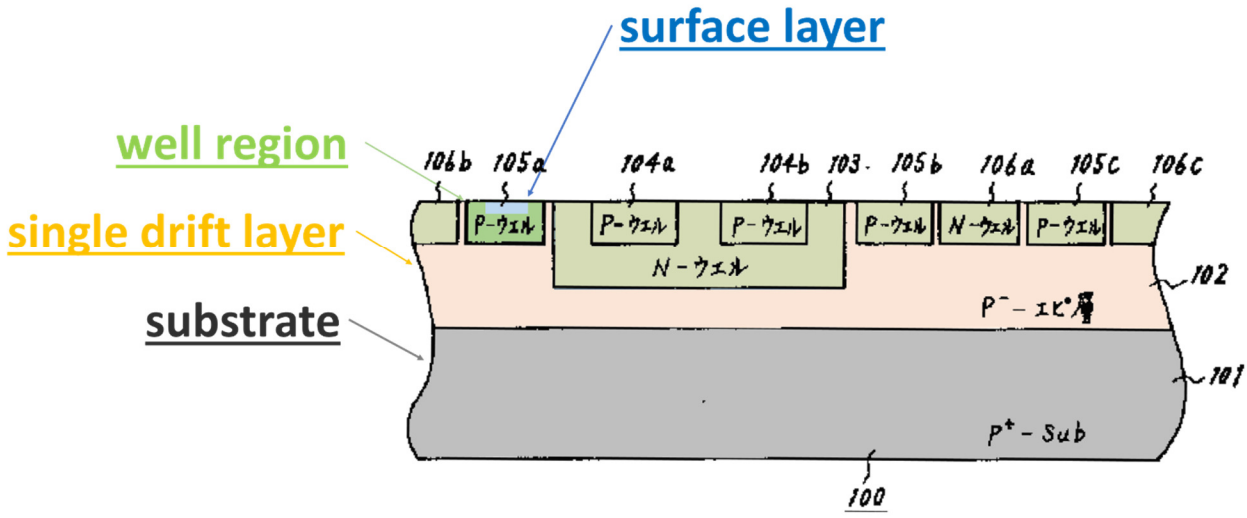
As can be seen in the two figures, the well region 105a, like the "single drift

layer" 102, has a dopant profile that has a downward sloping gradient. (Onoda at [0052].) The well region 105a has the claimed second static unidirectional electric drift field (*e.g.*, pink arrow)[6] to aid the movement of minority carriers from said surface layer to said substrate for the same reasons as described in Element [1.5]. And, as detailed in section VII.B at pages 9-12, Patent Owner in prosecution described a downward graded dopant profile as providing an "inherent 'built-in' unidirectional electric field" that moves carriers into the substrate. (*Supra* at 9.) A POSITA would have understood Onoda's dopant profile over the well region 105a to teach a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. (Ex. 1003 at ¶¶ 75-83.)

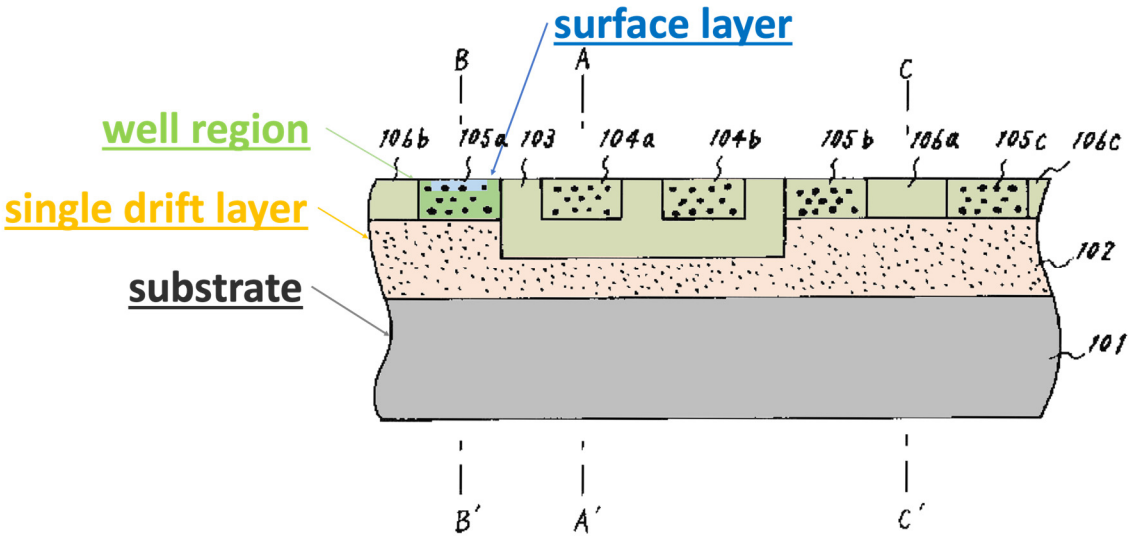
A singular well region (p well 105a) has been identified above. P well 105a is described in separate embodiments as: (1) being separated from other well regions; and (2) being part of a contagious set of well regions. Under any possible perceived construction argument surrounding "well region," it is taught by Onoda. First, FIG. 13 shows well region 105a as separated from others; it depicts well region 105a (dark green, below) encompassed within portions of the epitaxial layer 102 and separated from other well regions (light green). (Onoda at [0087] (stating that "the first well region 103, third well region 105, and fourth well region 106 are separated from each

[6] The arrow denotes the drift of electrons (minority carriers) in the p-well. (Ex. 1003 at ¶ 79.)

other, that is, wherein the second semiconductor layer 102 is interposed between the well regions, as depicted in FIG. 13"); [0042] (generally describing the well regions).)



(Onoda at FIG. 13.) Second, well region 105 (a) is part of a contiguous well structure, where the entire well region teaches the claimed "well region." This is depicted in FIG. 8, below, with the well region 105a annotated in dark green and the other well regions annotated in light green. (*See* Onoda at FIG. 8; [0042] (generally describing the well regions).)



(Onoda at FIG. 8.)

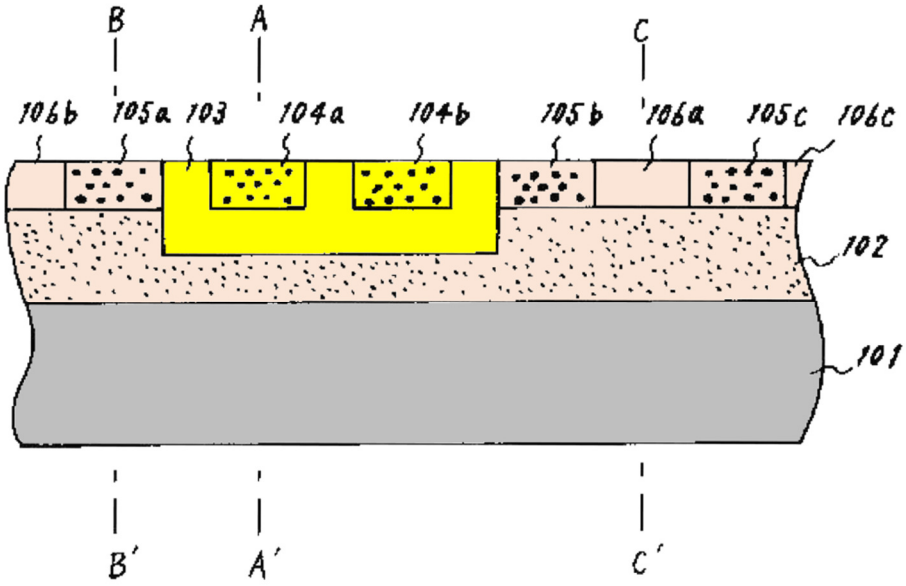
Finally, for the same reasons as described in Element [1.5], a POSITA would have understood Onoda's graded-dopant profile, including the dopant profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static. (Ex. 1003 at ¶¶ 75-83, 72-74; *see also* Onoda at [0048] (stating that the wells are doped and then dopants thermally diffused).)

Onoda thusly discloses or, at the very least, renders obvious Claim 1.

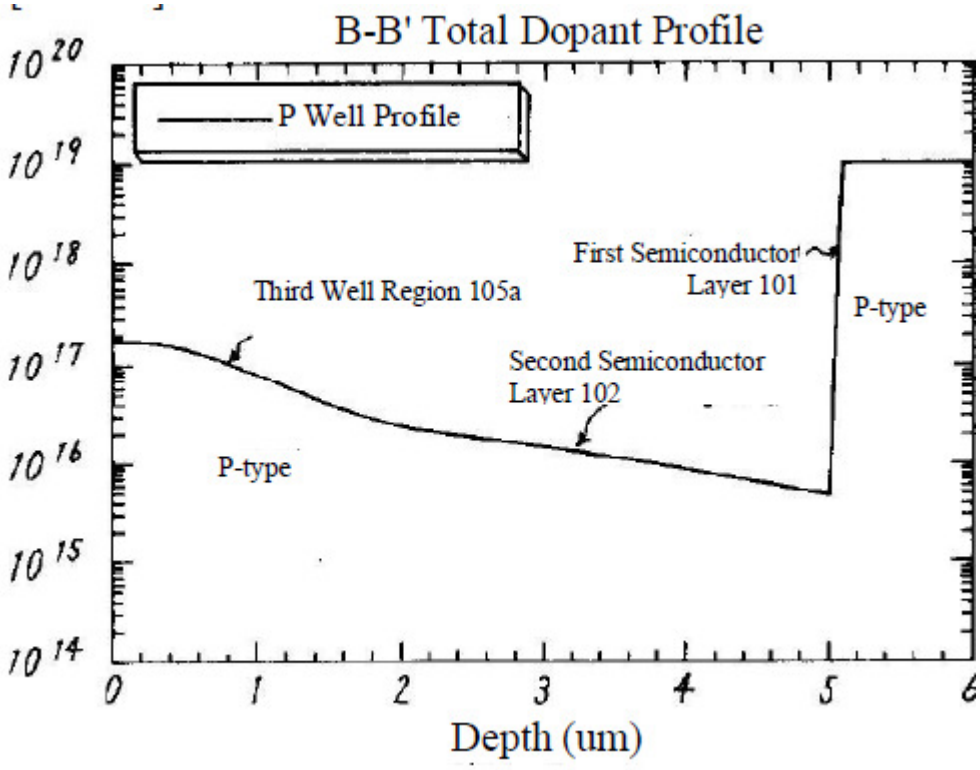
2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

Onoda discloses this limitation.

Onoda teaches that the doped semiconductor layer 102 is fabricated using ion implantation techniques and has a depth of "about 5 μm." (Onoda at [0046], FIG. 9.) Further, Onoda teaches forming its well structures with deep wells formed by ion implantation and thermal diffusion, extending 3-5 μm deep. (*Id.* at [0052].) Onoda, moreover, describes its n wells as being "deep" (annotated yellow) yet those wells do not go as "deep" as the claimed single drift layer (tan) (*id.* at FIGS. 8 and 11 (excerpted below)), further demonstrating that the drift layer is a "deeply-implanted layer." (Ex. 1003 at ¶ 84.).



(Onoda at FIG. 8.)



(Onoda at FIG. 11.)

Even if Patent Owner argued that Onoda does not disclose a "deeply-implanted

layer," it would have been obvious to try. As noted above, Onoda suggests implanting its layers "deep," and a POSITA would have found it obvious to do so in light of that suggestion. (Ex. 1003 at ¶¶ 84-85.) Furthermore, the '195 Patent provides little guidance as to what is meant by "deep"; it mentions the deeply implanted layer once (*e.g.*, '195 Patent at 3:37-38) and mentions "deep" in another context, sweeping carriers "deep into the substrate." (*Id.* at 3:33-35.) The specification, however, does not discuss the depth of the "deeply-implanted layer" or the process of forming such a layer, thus confirming that it was well-known and routine for a POSITA to implement. (Ex. 1003 at ¶ 85 .)

Onoda thusly discloses or, at the very least, renders obvious Claim 2.

3. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein the said drift layer is an epitaxial layer."

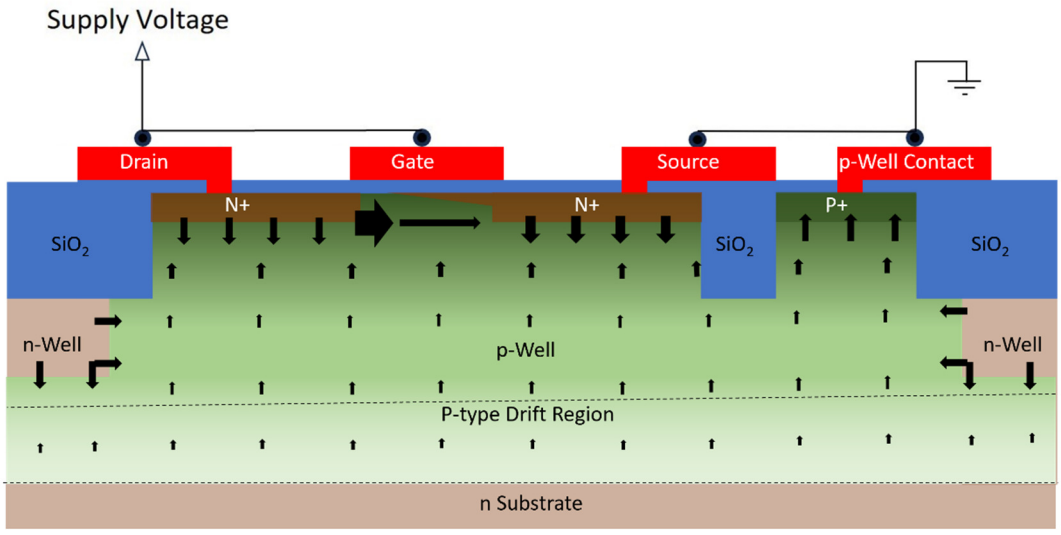
Onoda discloses Claim 3. When discussing formation of semiconductor layer 102 (the claimed single drift layer), Onoda discloses that it is within an epitaxial layer; it teaches that a lightly-doped P-type epitaxial layer 102a with a dopant concentration of 1 x 10^{15}/cm^3 is formed with a thickness of about 5 μm through epitaxial deposition onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x 10^{19}/cm^3. (Onoda at [0046].) Subsequent implantation of dopant (*e.g.*, boron B) creates an ion implantation layer 102b, which is then subjected to heat treatment to produce a lightly-doped P-type second semiconductor layer 102. A POSITA would have understood that

Onoda's lightly-doped P-type semiconductor layer 102 is an epitaxial layer. (Ex. 1003 at ¶ 86.)

4. Dependent Claim 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient."

Onoda discloses or, at the very least, renders obvious Claim 5.

Onoda teaches several dopant gradient profiles, in addition to providing graphical depictions of profiles to where a POSITA would have found a quasi-linear gradient obvious. For instance, Onoda teaches a gaussian distribution of dopants. (Onoda at [0053] ("the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate Gaussian distributions with the concentrations at maxima near the surface").) A POSITA would have known of quasi-linear gradient as one a few types of gradients and that the unidirectional doping also generates a unidirectional electric field. (Ex. 1003 at ¶ 87.)



Linearly graded profile with the graded drift region matching the bottom of the well

Onoda thusly discloses Claim 5.

Even if Patent Owner were to argue that Onoda does not disclose a quasi-linear gradient this limitation is still rendered obvious as it was a simple substitution of one known method with another to yield predictable results and was obvious to try. *See, e.g., KSR Intern. Co. v. Teleflex, Inc.* 550 U.S. 398 at 418 (2007). The '195 Patent only mentions a quasi-linear gradient once in a listing of known dopant profiles ('195 Patent at 2:40-42) and does not illustrate or otherwise describe it, or describe any process steps for obtaining it – thus confirming that such a gradient was a well-known alternative to a POSITA.[7] (Ex. 1003 at ¶ 87.)

Onoda thusly discloses or, at the very least, renders obvious claim 5.

5. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient."

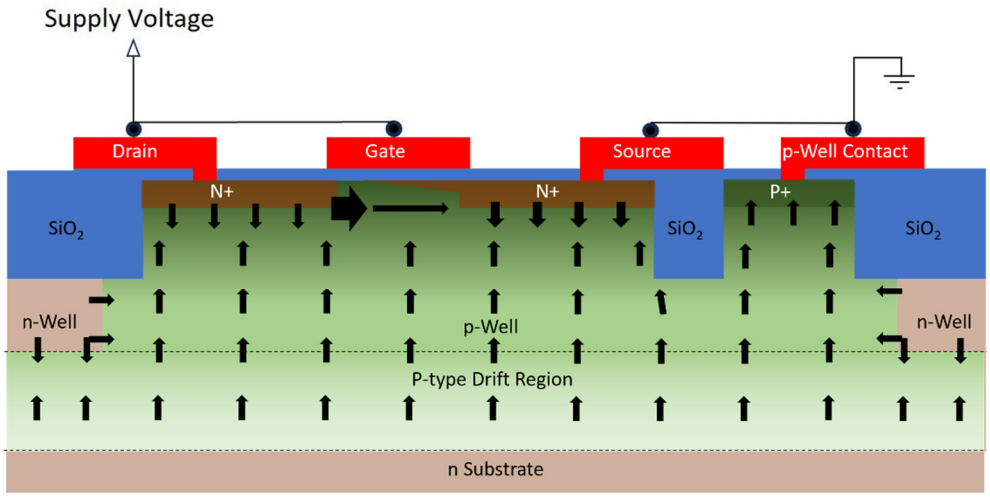
Onoda renders obvious Claim 6.

Onoda teaches a gaussian distribution of dopants. (Onoda at [0053].). A

[7] *See, e.g., Ex Parte Nico Hawley-Weld, Dan Volpe, & Ben Silverman*, No. APPEAL 2023-000345, 2022 WL 17495059, at *7 (P.T.A.B. Dec. 6, 2022) ("in the absence of specific description [in the specification], it is appropriate to assume that anyone desiring to perform the claimed function would know how to do so."); *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994).

POSITA would understand that a gaussian distribution is an exponential gradient. (Ex. 1003 at ¶ 88; *see also* Ex. 1047 U.S. Pat. No. 6,900,091 at 23:23-40 (describing a gaussian distribution with an exponential equation).)

Furthermore, as noted immediately above, Onoda teaches several distributions (Onoda at [0053]) and, moreover, Onoda's FIG. 11, when converted to a linear scale, depicts portions with an exponential gradient. (Ex. 1003 at ¶ 88)



Exponentially graded profile with the graded drift region matching the bottom of the well

Even if Patent Owner were to argue that Onoda's FIG. 11 does not disclose an exponential gradient, a POSITA would have nonetheless found it obvious to use one because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. *See, e.g., KSR*, 550 U.S. 398 at 418. A POSITA would understand that, in semiconductor processing, exponential profiles are widely used in semiconductor processing and thus it would be obvious to try. (Ex. 1003 at ¶ 88.) Furthermore, as with the "quasi-linear" gradient limitation, the '195

Patent only mentions "exponential" gradient once in a listing of known dopant profiles ('195 Patent at 2:40-42) and does not illustrate or otherwise describe it, or describe any process steps for obtaining it, thus confirming that it was a well-known alternative to a POSITA.[8]

Moreover, Onoda recognizes using downward dopant gradients. (Onoda at FIG. 11.). It would have been obvious to apply a POSITA's general knowledge in the art to achieve a known exponential gradient dopant profile. (Ex. 1003 at ¶ 88.) This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant and would have also been a simple substitution of one known dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success. (*Id.*.)

Onoda thusly discloses or, at the very least, renders obvious Claim 6.

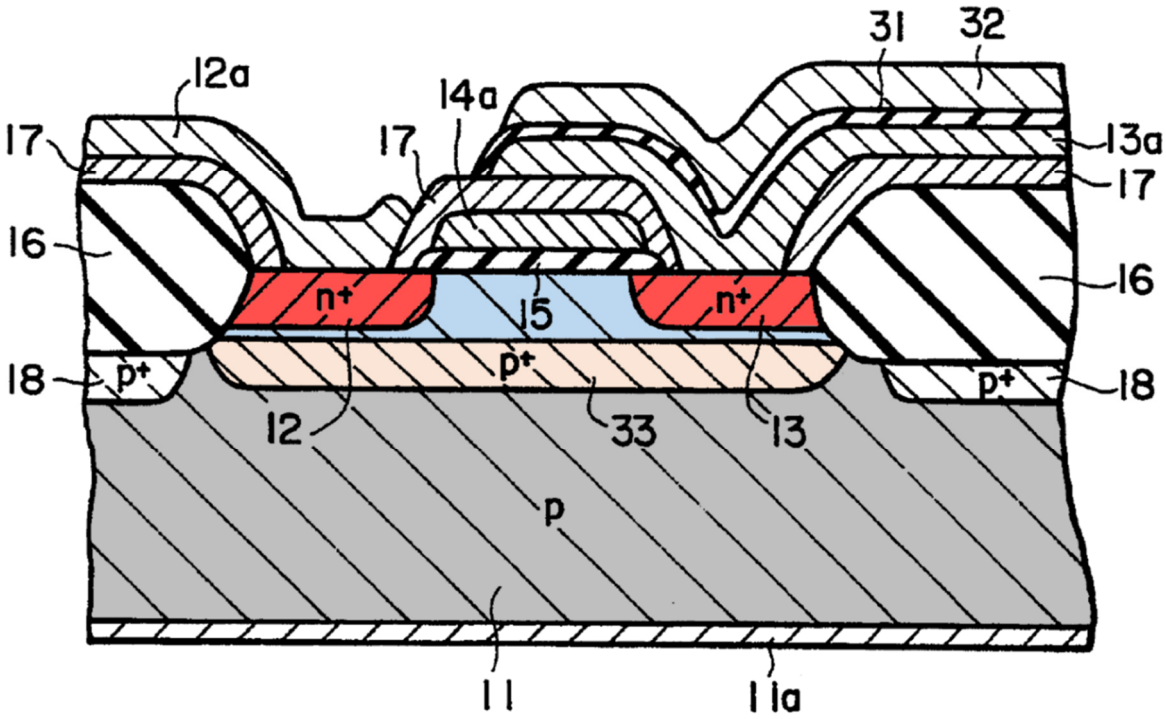
B. Ground II: Onoda in view of Nishizawa Renders Obvious Claims 1, 2, 3, 5, and 6.

Nishizawa teaches a CMOS device (*e.g.*, Nishizawa at 7:61-63, FIG. 32) that provides a buried region that has a graded dopant profile (annotated tan, below). (Nishizawa at FIG. 16, 18:46-67; *see also id.* at 20:25-27.) The graded dopant profile is provided to create an electric drift field (*id.* at 18:10-18) that flows minority carriers

[8] *See, e.g., Ex Parte Nico Hawley-Weld*, 2022 WL 17495059 at *7; *In re Epstein*, 32 F.3d at 1568.

(electrons) from the surface region (blue) having the source and drain (red) to the substrate (gray) in order to prevent device errors. (*Id.* at 19:1-9; *see also id.* at 16:19-24 (describing the migration of carriers flowing to the surface as causing errors).)

FIG. 16



(Nishizawa at FIG. 16.)

Ground II takes Nishizawa's teachings of CMOS and minority carrier diffusion, and combines it with teachings from Onoda. As described in Ground I, the CMOS and minority carrier diffusion elements are disclosed or, at the very least, rendered obvious by Onoda. Even if Patent Owner were to argue that these limitations were not disclosed by Onoda, Nishizawa nonetheless contains explicit statements about these elements making it clear that they were well-known to a POSITA.

A POSITA would have been motivated to make this combination for several reasons. (Ex. 1003 at ¶ 89-93.) Nishizawa's teachings of CMOS and minority carrier diffusion are well known elements which, when combined with Onoda, would yield predictable results. As depicted in Ground I, Element [Preamble], Onoda discloses CMOS (although not mentioning the word "CMOS" directly). A POSITA would have found it obvious to apply teachings of CMOS—which was well known and described in Nishizawa—and apply it to Onoda. (*Id.*.) For example, Nishizawa describes an NMOS and PMOS pair as being a CMOS (*e.g.*, Nishizawa at FIG. 32) for memory (*id.* at Abstract), and Onoda describes both NMOS and PMOS in a single memory device. (Onoda at FIG. 3.)

In a similar vein, a POSITA would have been motivated to apply Nishizawa's teachings of minority carrier diffusion based on a downward sloping dopant gradient (*e.g.*, Nishizawa at 18:46-67) to Onoda's teachings of a downward sloping dopant gradient (*e.g.*, Onoda at FIG. 11). (Ex. 1003 at ¶¶ 91-92.) Again, Nishizawa makes explicit the concept of an "electric field" that migrates minority carriers to a substrate based on a dopant gradient (Nishizawa at 18:10-18), whereas Onoda describes the structure (*e.g.*, the downward dopant gradient, Onoda at FIG. 11), which a POSITA would have understood necessarily creates the specified physical conditions. A POSITA would have been motivated to combine teachings of Nishizawa's explicit discussion of concepts to the structures described in Onoda. (Ex. 1003 at ¶¶ 92-93.)

Making this combination of teachings would have combined known elements to

achieve predictable results (*e.g.*, applying Onoda's PMOS and NMOS transistors to CMOS as disclosed by Nishizawa and applying Onoda's downward dopant gradient to Nishizawa's teaching of the electric fields and minority carrier drifts that a downward dopant gradient creates). A POSITA would have seen such combinations as yielding expected results with known prior art elements and would have moreover found it obvious to try. *Id.*

Moreover, both Nishizawa and Onoda are directed to similar devices, which face similar problems, and seek similar solutions. Both are directed to memory devices (Nishizawa at Abstract; Onoda at [0004]), and to reducing punch through. (Nishizawa at Title; Onoda at Object.) (Ex. 1003 at ¶¶ 89-90.)

The Onoda-Nishizawa combination teaches elements from Onoda as described in Ground I, as supplemented by the specific limitations below to render claim 1 obvious. Claims 2, 3, 5, and 6 are dependent claims of claim 1, and the Onoda-Nishizawa combination renders them obvious for the same reason.

1. Independent Claim 1

a. Preamble: "A CMOS semiconductor device comprising:"

As described in Ground I, preamble, a POSITA would have found Onoda to disclose and, at the very least, render obvious CMOS. As described in the motivation to combine section above at VII.B, a POSITA would have further found it obvious to combine Nishizawa's teachings of CMOS to Onoda's teachings of NMOS and PMOS.

Nishizawa teaches CMOS. FIG. 32 depicts using NMOS and PMOS as CMOS

(Nishizawa at FIG. 32 and 15:27-52) and further states one of its objects is to provide an improved CMOS device (*id.* at 7:61-63).

The Onoda-Nishizawa combination therefore renders obvious the preamble.

b. Elements [1.1]-[1.4]

For the same reasons as in Ground I, Elements 1.1-1.4 are disclosed and/or rendered obvious by the Onoda-Nishizawa combination.

c. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

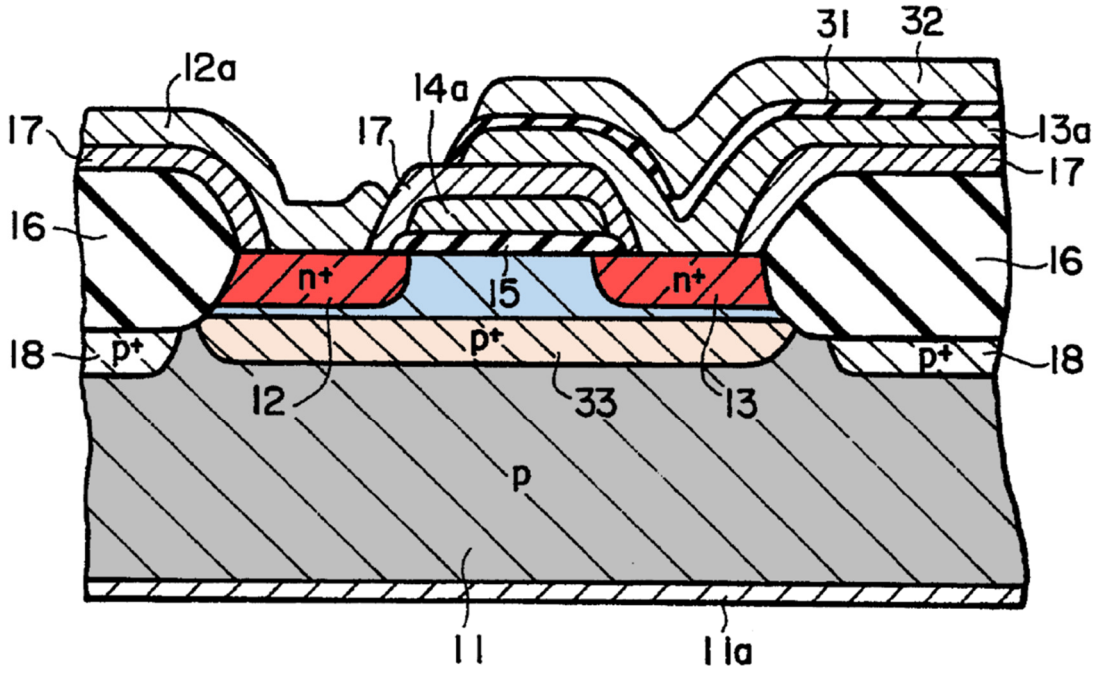
As described in Ground I, Element [1.5], Onoda discloses a drift layer whose dopant concentration has a downward gradient which a POSITA would have recognized as providing a built-in, static, unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate.

Nishizawa makes these elements explicit. FIG. 16[9] depicts a source and drain (red, below) at the surface region (blue), where buried region 33 (tan) provides an "impurity concentration gradient … [that is] progressively decreasing toward the p type substrate" (gray). (Nishizawa at 19:4-5; *see also id.* at 18:50-59 ("the impurity

[9] The cited-to text refers to the embodiment of FIG. 35, which is likewise applicable to the structure of FIG. 16 which is illustrated. (Nishizawa at 20:23-27.) (Ex. 1003 at ¶ 89, fn. 2.)

concentration of that portion of the p+ type buried region 33a located adjacent the channel region and the n+ type region 13 is set at about $1x10^{17}$ cm^{-3}, with progressively lowered concentration as the portions of the buried region 33a go progressively toward the p type substrate 11, in such manner that the impurity concentration of lowermost portion of the buried region is less than at least one third of that of the highest impurity concentration.")

FIG. 16



(Nishizawa at FIG. 16.)

As recognized by Nishizawa, "a drift electric field" is created when there is a "difference in the degree of impurity concentration," which is used to drift minority carriers to the substrate. (Nishizawa at 18:9-18.) To drift electrons within the p+ buried layer to the substrate, "an impurity concentration gradient in the p+ type buried region

33a in the direction toward the p type substrate" is formed. (*Id.* at 18:35-50; *see also id.* at 18:51-67 (stating that the impurity concentration has a downward gradient to the substrate); *see also id.* at 19:1-9.) (Ex. 1003 at ¶¶ 96-97.)

As described in Ground I, Element [1.5], Onoda discloses a drift layer with an impurity dopant profile with a downward gradient. The Onoda-Nishizawa combination makes clear and explicit that this drift layer in Onoda provides a static unidirectional electric drift field for purposes of aiding the movement of minority carriers from said surface layer to said substrate. (Ex. 1003 at ¶¶ 96-97.)

The Onoda-Nishizawa combination thusly renders Element [1.5] obvious.

d. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

As described immediately above, the Onoda-Nishizawa combination renders Element [1.5] obvious. As described in Ground I, Element [1.6], Onoda discloses a drift layer having a well-region with an impurity dopant profile with a downward gradient. The Onoda-Nishizawa combination makes clear that this well region in Onoda provides a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate for the same reasons described in Ground II, Element [1.5]. (Ex. 1003 at ¶ 98.)

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted

layer."

As described in Ground 1, Claim 2, Onoda renders obvious this limitation.

Nishizawa further teaches that its layer having a graded dopant profile (e.g., region 33a in FIG. 16) is a deeply implanted layer by referring to it as a "deep semiconductor region." (Nishizawa at 22:17 (describing the layer as "a deep semiconductor region (33)").) Furthermore, the layer is created via implantation. (*see also id.* at 18:64-67 (stating that the gradient can be created via implantation).) (Ex. 1003 at ¶ 99.)

The Onoda-Nishizawa combination thusly renders Claim 2 obvious.

C. Ground III: Kawagoe Renders Obvious Claims 1, 2, 3, 5, and 6.

Kawagoe teaches a CMOS device whose surface region (its epitaxial layer) has its "impurity concentration gradually lowered depth wise of said epitaxial layer." (Kawagoe at Abstract.) The "gradient … is gradually lowered in the depth wise direction from the surface of the epitaxial layer … so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient." (*Id.* at 16:3-8.)

Kawagoe's teachings and purpose of the doping gradient match that of the '195 Patent. The '195 Patent states that the prior art was deficient because it purportedly provided uniformly doped epitaxial regions ('195 Patent at 1:36-40), and the '195 Patent—as an improvement—provided a gradient doping profile at the surface to

sweep unwanted minority carriers into the substrate. (*Id.* at 3:30-35.) This purported improvement is described by Kawagoe.

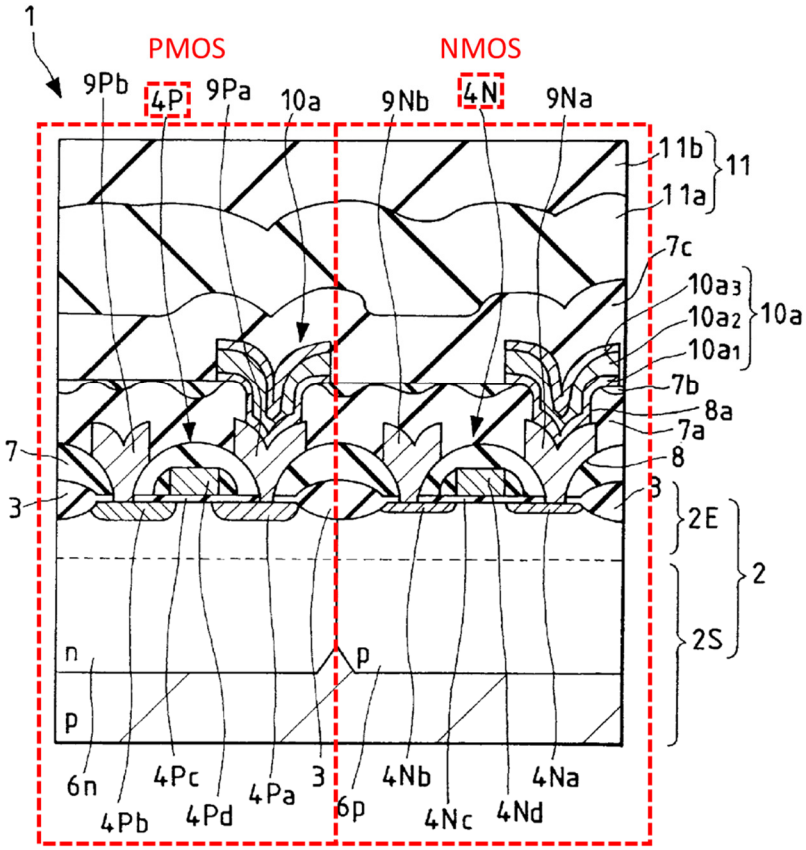
Kawagoe renders obvious claims 1, 2, 3, 5, and 6 as detailed below.

1. Independent Claim 1

a. Preamble: "A CMOS semiconductor device comprising:"

Kawagoe discloses a CMOS semiconductor device. (*See, e.g.,* Kawagoe at 15:37-40 (describing the CMOS structure of the embodiment of FIG. 16 having an NMOS 4N and PMOS 4P); *see also id.* at 8:46-54 (describing the CMOS).) (Ex. 1003 at ¶ 101.)

FIG. 16



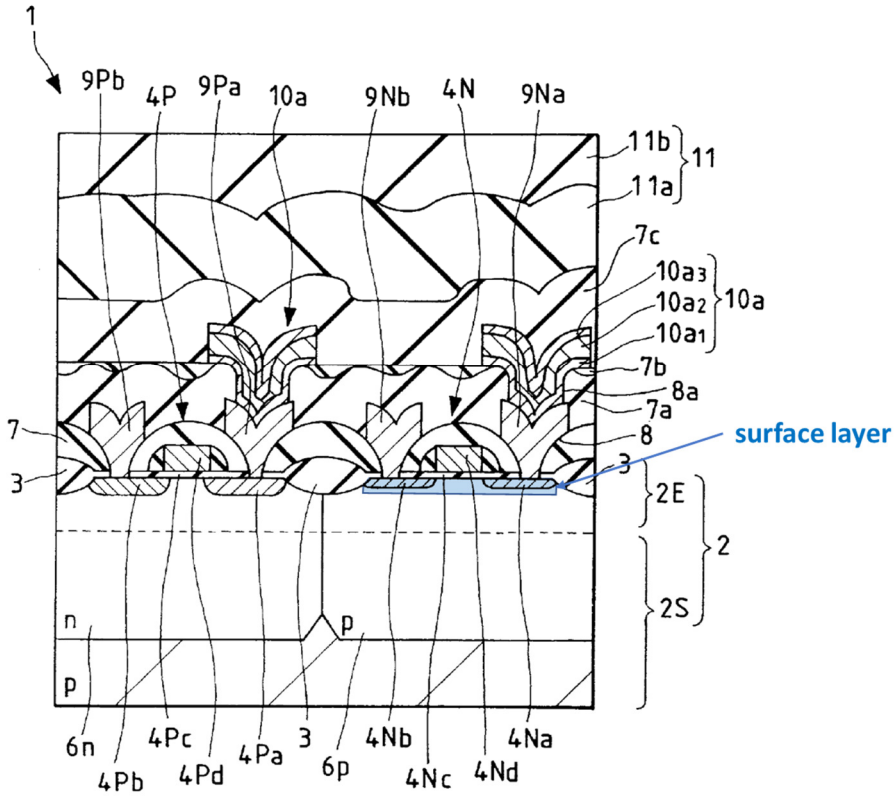
(Kawagoe at FIG. 16.)

b. Element [1.1]: "a surface layer;"

Kawagoe teaches a surface layer as depicted below in blue in annotated FIG. 16. Kawagoe's surface layer exists in the epitaxial layer (2E) and the surface layer has an active region with a source and drain formed within it (4Nb and 4Na) (discussed in more detail with respect to Element [1.3]).[10] (Kawagoe at 8:66-9:6; *see also id.* at 15:26-32.) (Ex. 1003 at ¶ 102.)

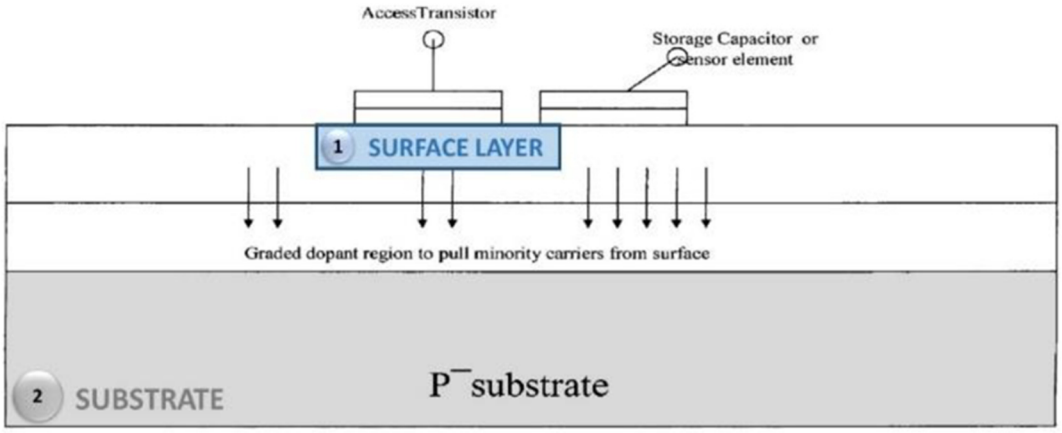
[10] FIG. 16 depicts the finalized devices, with insulating films 7, wirings 10, and protection films 11. (Kawagoe at 15:55-61.) A POSITA would understand that these additional components are not a part of the semiconductor's surface layer because they are, as they state, wirings and insulators for the semiconductor device that is fabricated on the silicon wafer. (Ex. 1003 at ¶ 102.)

FIG. 16



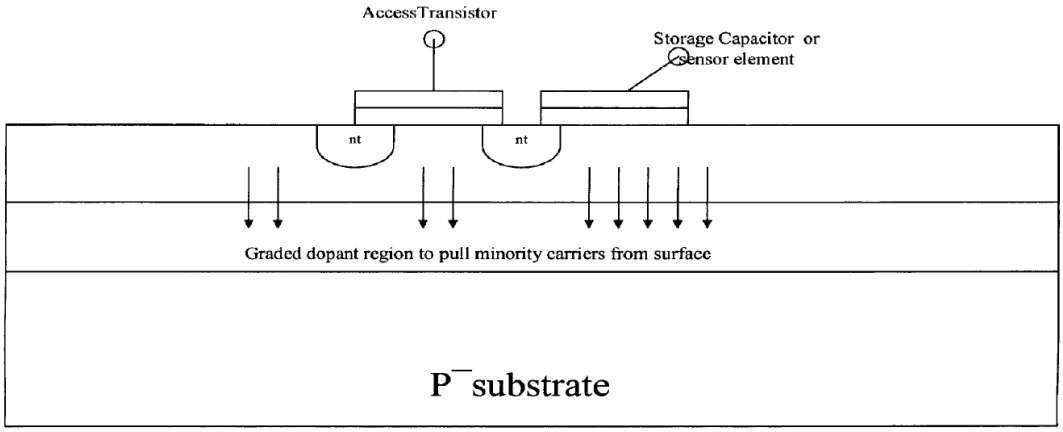
(Kawagoe at FIG. 16.)

Kawagoe's "surface layer" teachings match Patent Owner arguments made in its district court claim construction briefing. Shown below, Patent Owner annotated FIG. 5(b) as support to disclose a "surface layer" (the region surrounding the active region), and Patent Owner further argued in construction that the "surface layer" refers to "a layer at the surface of the silicon." (Ex. 1030 at 13.)



(Ex. 1030 at 6) (annotations to FIG. 5(b) of the '195 Patent by Patent Owner).

Patent Owner annotated over FIG. 5(b). A non-annotated version of FIG. 5(b) of the '195 Patent is excerpted below that more clearly illustrates the active region (the source and drain).



('195 Patent at FIG. 5(b).)

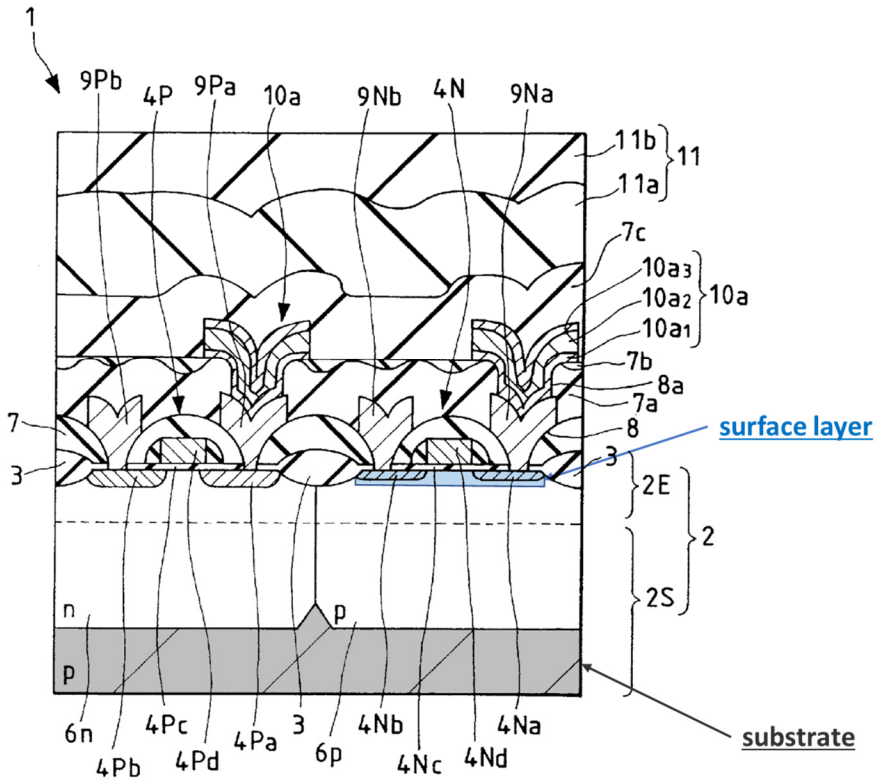
Kawagoe teaches the "surface layer" in an identical manner as described by the '195 Patent's purported written description support of the very same limitation, and thusly renders this limitation obvious.

c. Element [1.2]: "a substrate;"

Kawagoe teaches a substrate.

Kawagoe's substrate is annotated in gray in FIG. 16, below. Kawagoe forms its p-well 6p and n-well 6n in part of the substrate body 2S from the original wafer. (Kawagoe at 15:62-65, 17:50-61, FIG. 21.) A POSITA would understand that at least the portion of the substrate—separate from the well regions—would satisfy the claimed substrate. (Ex. 1003 at ¶ 104.).

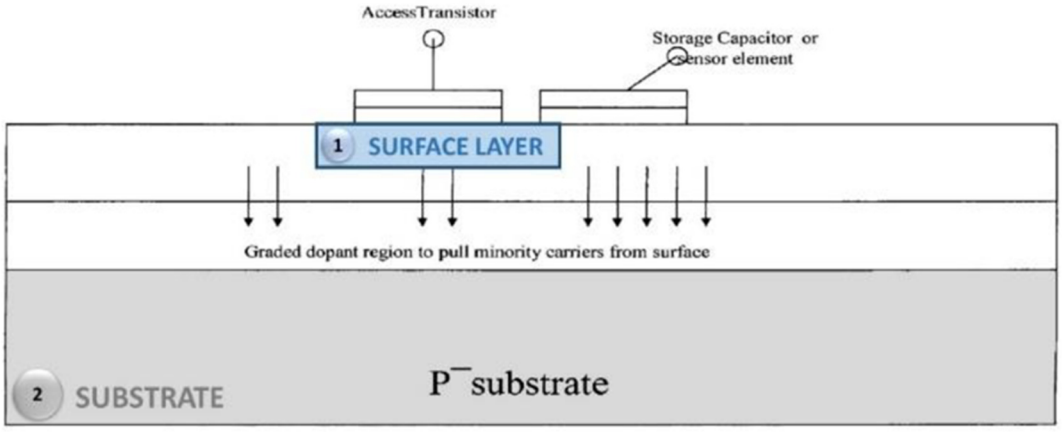
FIG. 16



(Kawagoe at FIG. 16.)

Kawagoe's teaching of the "substrate" matches Patent Owner's district court claim construction of "substrate," which was described as "an underlying layer" (Ex.

1030 at 15) and where Patent Owner provided annotation to FIG. 5(b) of the '195 Patent (excerpted below).[11]



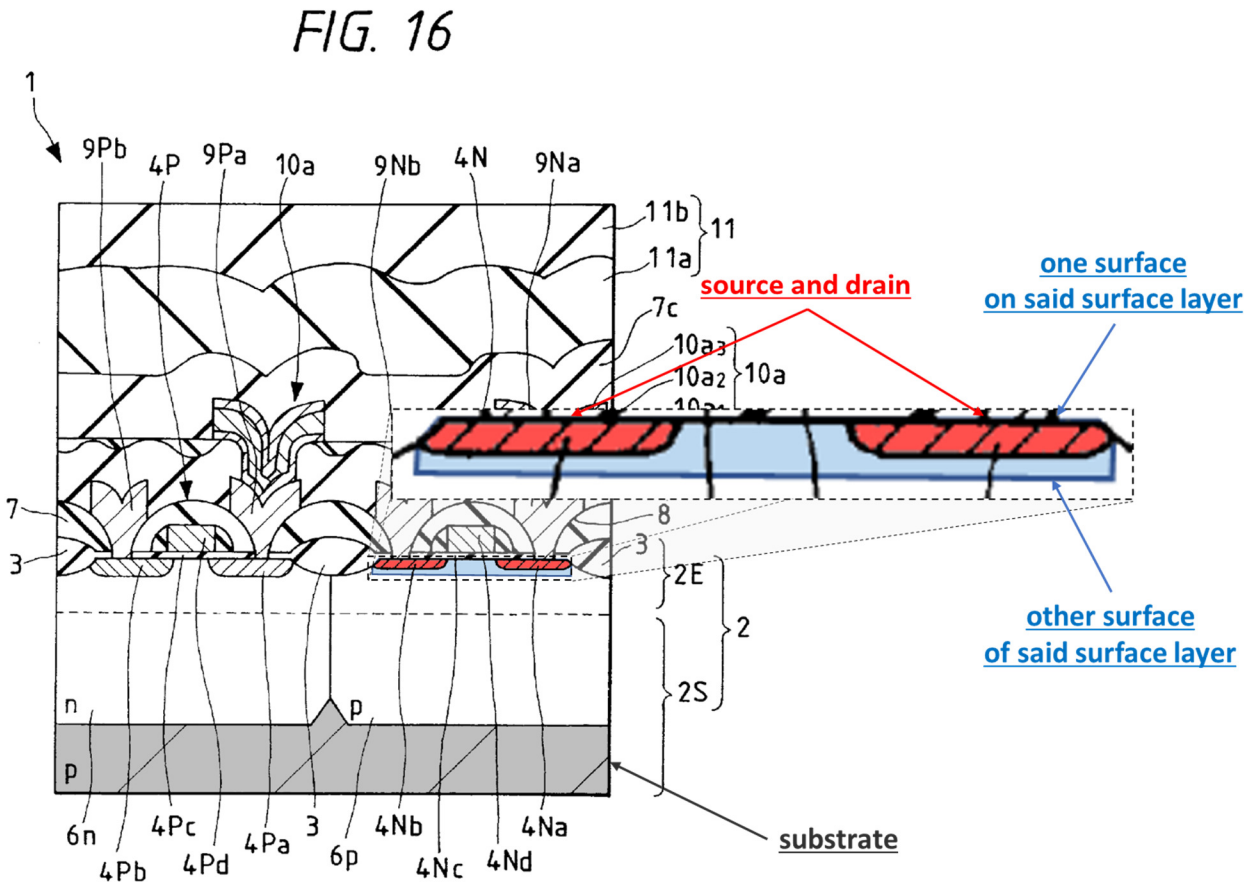
(Ex. 1030 at 6) (annotations by Patent Owner).

Element [1.2] is accordingly taught by Kawagoe.

d. Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

Kawagoe teaches an active region that has a source and a drain disposed on one surface of the surface layer. As depicted in annotated FIG. 16 below, the surface layer contains source and drain 4Nb and 4Na which form an active region (excerpted out for greater emphasis). (Kawagoe at 8:66-9:6, 9:47-53.) (Ex. 1003 at ¶ 106.)

[11] Moreover, layer 2S by itself further satisfies the "substrate" term (*e.g.*, Kawagoe at 15:7-8 (stating that "the p- -type epitaxial layer 2E is formed over the p-type semiconductor substrate).). This—and its relationship to the claimed "single drift layer"—are discussed in more detail with respect to Elements [1.4]-[1.6] below.



(Kawagoe at FIG. 16 (active region excerpted above).)

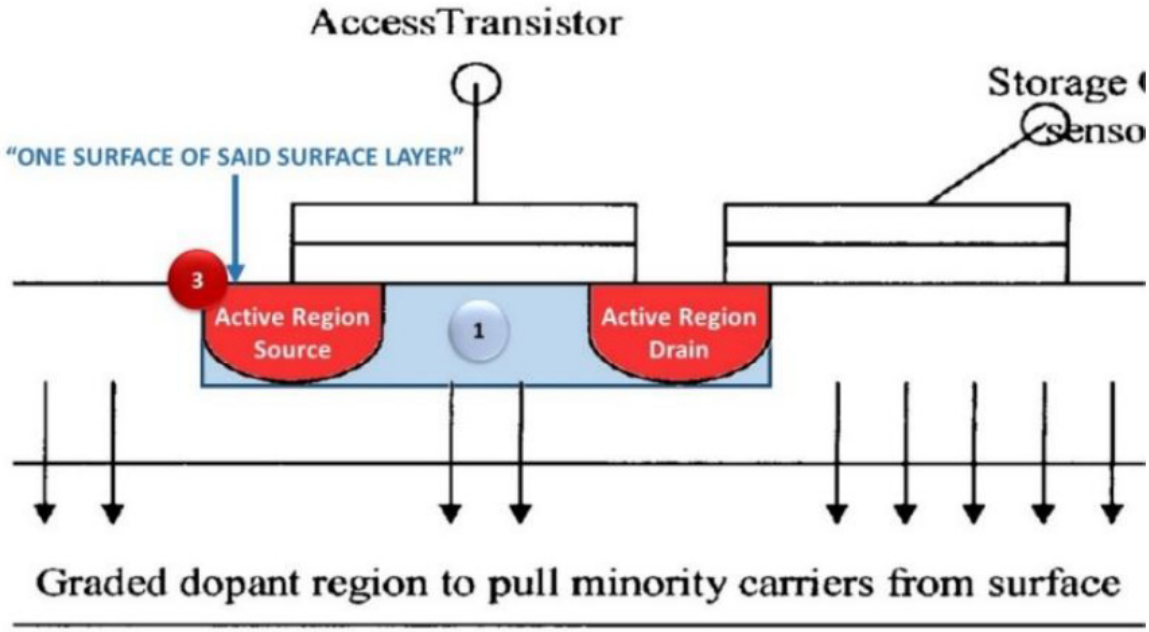
The active region is disposed to the top surface of the surface layer, *i.e.*, the claimed "one surface on said surface layer." (Ex. 1003 at ¶ 107.). This orientation—and discussion of each respective region—matches Patent Owner's articulation of this limitation during district court claim construction. There, it had likened the orientation to a ceiling fan in a room, stating:

> "By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the ceiling fan is spinning around like a propeller on the roof of the house. Instead it means that the ceiling fan is hanging from the ceiling ***inside***

> the room. The same is true about the active region and the surface layer."

(Ex. 1030 at 11 (emphasis in original).)

Patent Owner further annotated FIG. 5(b) of the '195 Patent to depict this configuration, where the active region source and drains were disposed on the surface of the surface layer (similar to Kawagoe's FIG. 16).

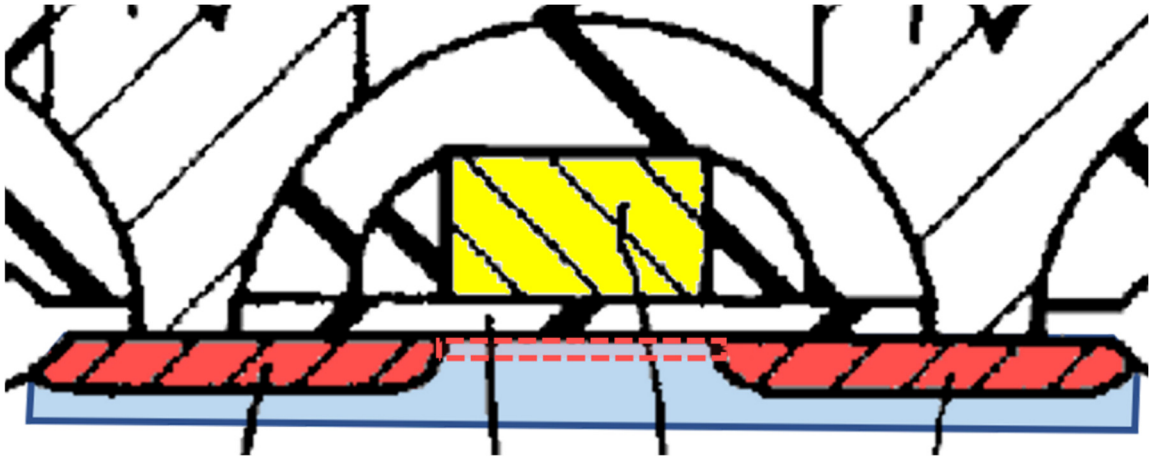


(Ex. 1030 at 7.)

Kawagoe thusly teaches the "an active region including a source and a drain, disposed on one surface of said surface layer," and moreover teaches it in a manner similarly to Patent Owner's stated written description support.

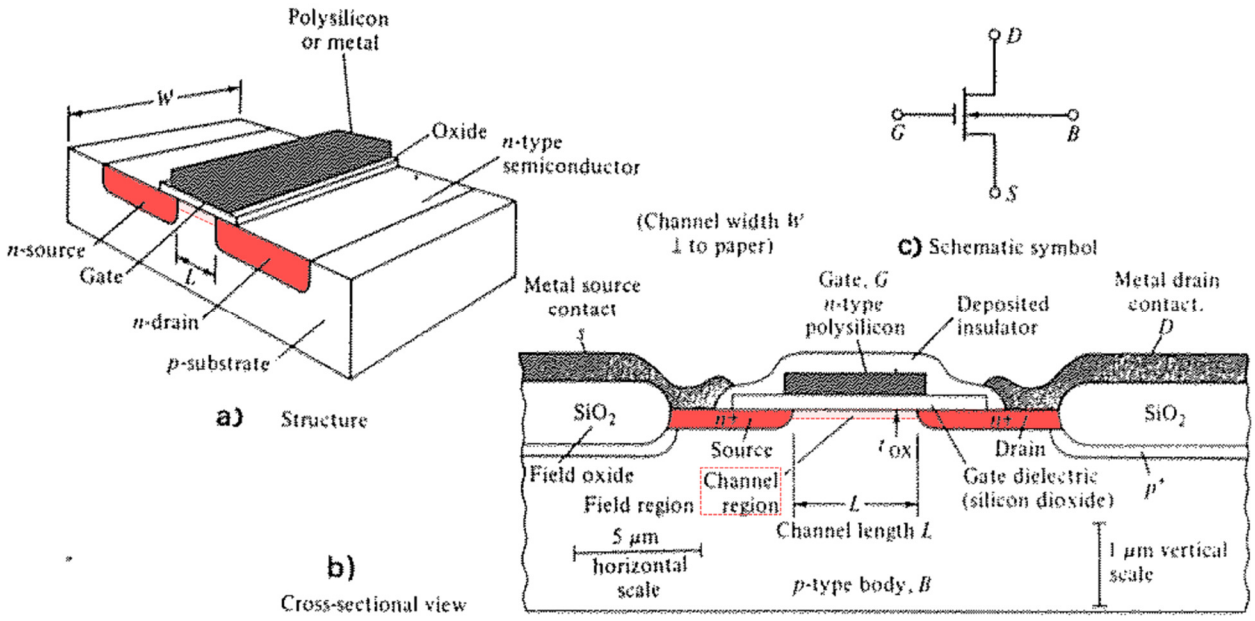
Furthermore, a POSITA would understand that the above-described source and drain configurations of Kawagoe provide an active region. (Ex. 1003 at ¶ 108.). As depicted in the enlarged excerpt of FIG. 16, below, a charge applied to gate electrode

4Nd (annotated in yellow, *see, e.g.,* Kawagoe at 9:20-26) causes a conductive channel (annotated in dashed-red) to form between the source and drain. (Ex. 1003 at ¶ 108.). A POSITA would understand the source, drain, and channel depicted below to be an active region. *Id.*.



(Kawagoe at FIG. 16 (excerpt).)

This understanding of source, drain, and channel operation in a MOS transistor is confirmed via *Wolf and Tauber*, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor as "[its] channel and [its] heavily doped source and drain regions." (Ex. 1008 at 299; *see also* Ex. 1030 at 4-5 (Patent Owner acknowledging that a channel is formed between a source and drain to form an active region).)



(Ex. 1008B at FIG. 5-1.)

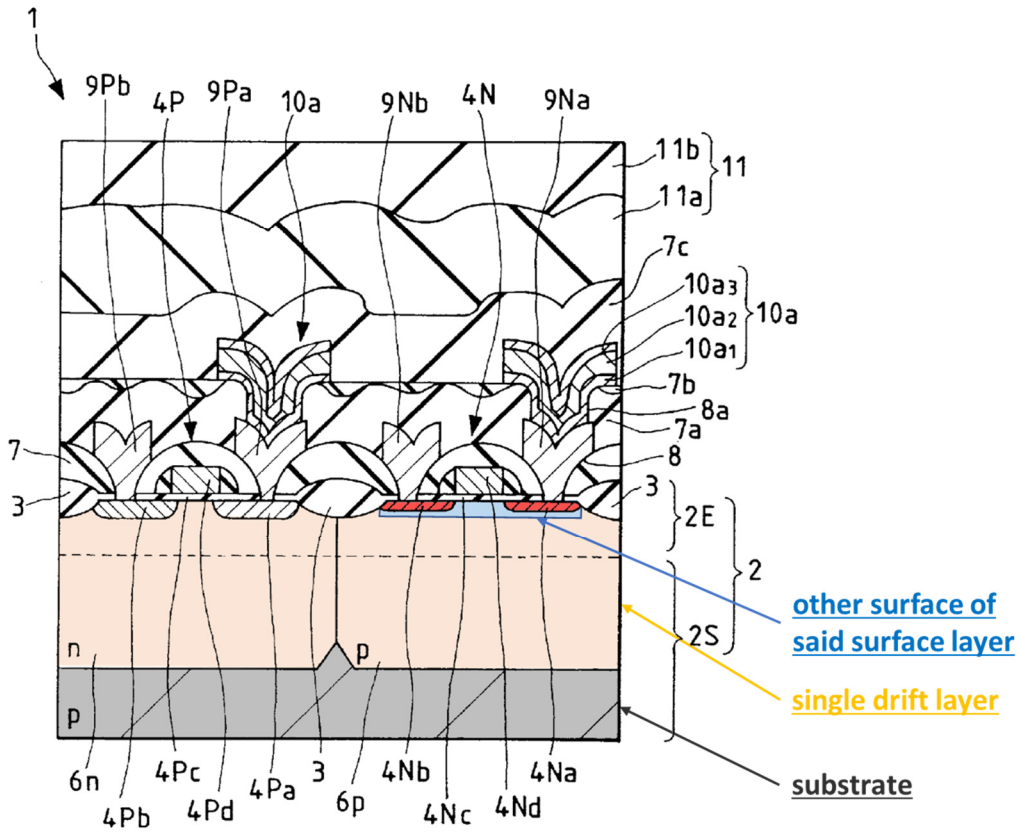
Kawagoe thusly teaches Element [1.3].

e. Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate,"

Kawagoe teaches this limitation.

Kawagoe teaches the claimed single drift layer (annotated tan, below) disposed between the other surface of said surface layer (blue) and said substrate (gray), where the drift layer has a graded concentration of dopants extending between the surface layer and substrate. Kawagoe's single drift layer includes the upper portion of the substrate body 2S colored in tan and the epitaxial layer 2E colored in tan that constitute an epitaxially integrated single structure. (Ex. 1003 at ¶¶110-111.)

FIG. 16



(Kawagoe at FIG. 16.)

Kawagoe's single drift layer (annotated in tan, above) is at the surface of the semiconductor device (Kawagoe at 15:62-16:15) and is formed into the CMOS device so that minority carriers (*e.g.*, electrons in the p-well) are attracted to the substrate to reduce errors. (Kawagoe at 16:7-11.) (Ex. 1003 at ¶ 111.) The single drift layer comprises both p-wells and n-wells, where the "impurity concentrations [of those wells are] gradually lowered in the depthwise direction from the principal surface … of the epitaxial layer 2E." (*Id.* at 15:66-16:2.) The depthwise gradient extends from the surface of the semiconductor device into its substrate (*id.* at 16:2-15) and is formed by

diffusing impurities in the upper portion of the semiconductor substrate. (*Id.* at 15:26-36). Kawagoe's graded concentration of dopants is depicted in FIG. 17 where the gradient of dopants in the drift layer (tan) extends from the surface of 2E (epitaxial layer of wafer) through the p and n wells (6p and 6n) (with depth depicted in yellow) and a portion of the substrate (substrate of wafer)[12]. ((Ex. 1003 at ¶ 111.)

[12] Patent Owner has argued in claim construction that the claims cover a drift layer that extends into the substrate. (Ex. 1030 at 17 (Patent Owner arguing in claim construction that "the claim never says the well region and drift layer cannot be part of the substrate. In fact, the specification says the opposite") (citing '195 Patent at 2:27-28).) To the extent Patent Owner argues a narrow view of "single drift layer" to be narrowly confined in some manner, that would be inconsistent with Patent Owner's own argument of claim scope.

FIG. 16

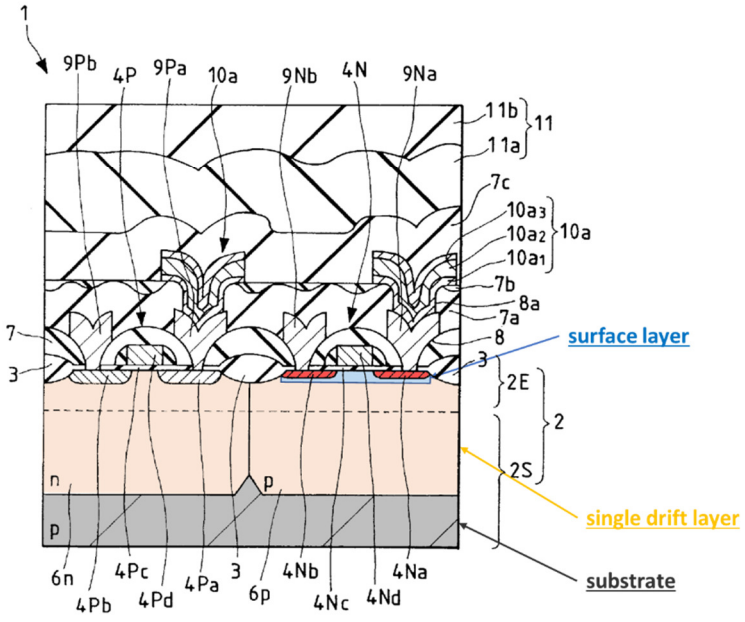
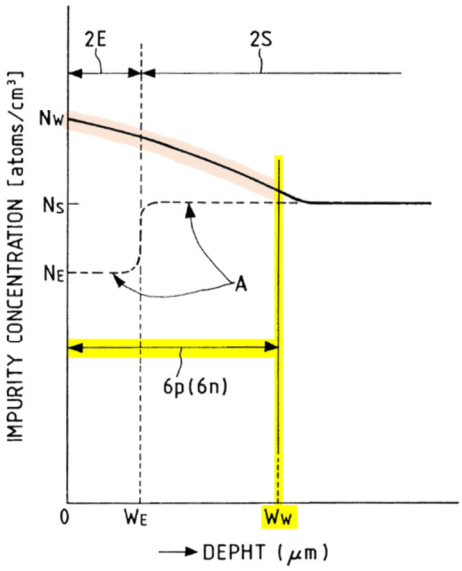


FIG. 17

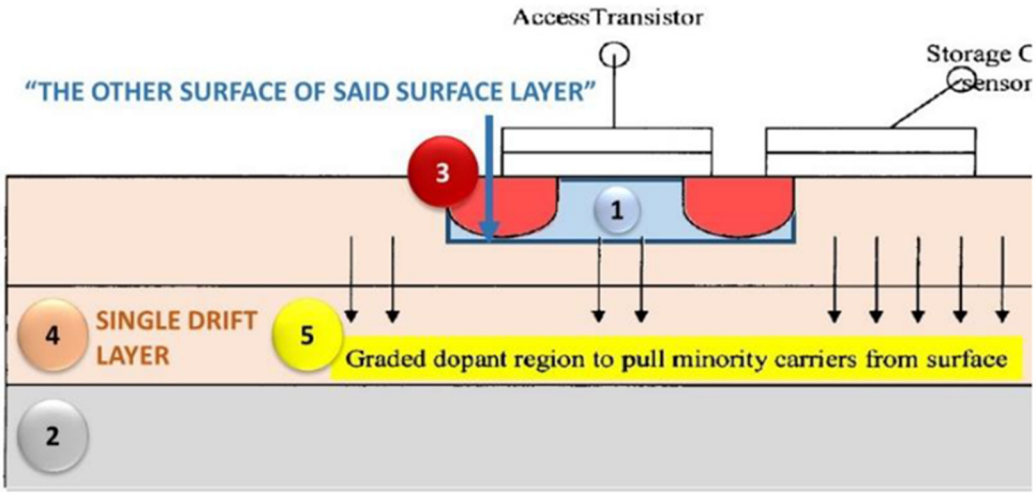


(Kawagoe at FIGS. 16 and 17.)

Kawagoe describes its impurity gradient region (which was annotated tan, above) as a "diffusion layer." Kawagoe discloses that a "diffusion layer" is created by diffusing impurities into a semiconductor device. (Kawagoe at 2:20-23; *see also id.* at 16:63-17:10 (stating that diffusion of impurities creates a "diffusion layer" when describing the state of the art); *see also id.* at 2:21-35; *see also id.* at 1:61-65 (describing how the referenced Japanese application, likewise describes this as a diffusion layer). And, as described above, diffusing impurities to create a diffusion layer is how Kawagoe's drift layer is created. (*Id.* at 15:26-36; *see also id.* at 17:50-54; *see also id.* at 25:27-30.). Finally, the term "drift layer" does not appear in the '195 Patent specification while "drift region" is repeatedly described. (*See, e.g.,* '195 Patent at 2:64-66 and 3:5-6.) Consequently, a POSITA would understand that Kawagoe's

diffusion layer discloses—or at least renders obvious because it uses similar verbiage as the claims—the claimed "single drift layer." (Ex. 1003 at ¶ 112.)

Kawagoe's teachings match Patent Owner's district court claim construction annotations to FIG. 5(b) of the '195 Patent, where it demonstrated the position of the single drift layer in relationship to the surface layer's other surface and the substrate. (Ex. 1003 at ¶ 113.)

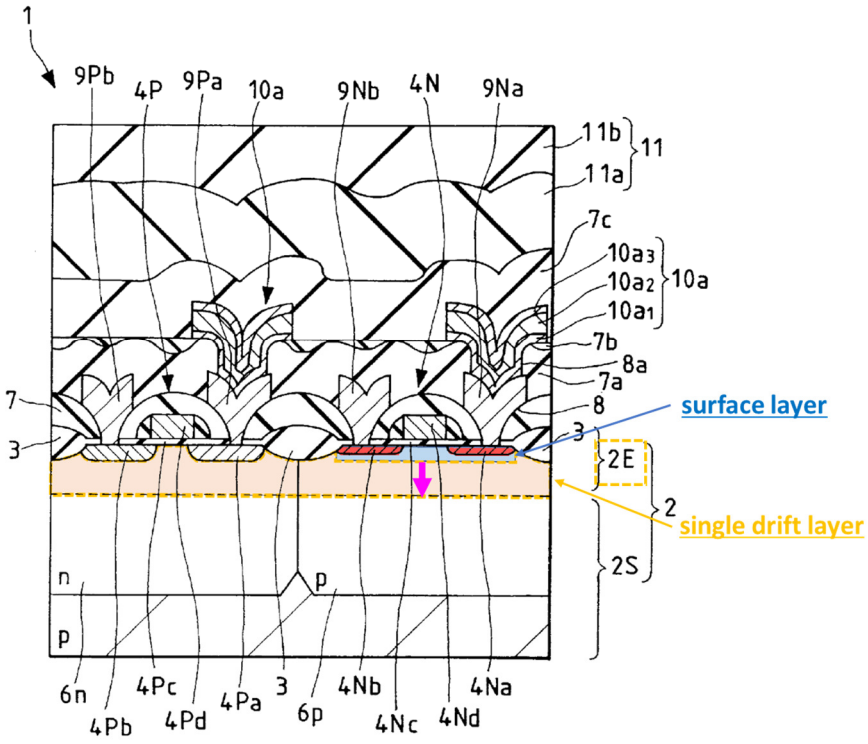


Kawagoe's diffusion layer thusly satisfies the claim limitations of Element [1.4].

Even if Patent Owner were to argue that Kawagoe's dopant gradient does not literally disclose Element [1.4] under a narrow interpretation of "single" or "layer" in the claim phrase "single drift layer," it nevertheless would be obvious because the epitaxial layer (*see* 2E in FIG. 16) itself, which has a graded dopant concentration (*see* line Nw in FIG. 17), is a singular layer that satisfies the claimed "single drift layer." The portion of the diffused impurity gradient that is within the epitaxial layer 2E—which satisfies the "single drift layer"—is annotated below in tan within the dashed

lines. (Ex. 1003 at ¶¶ 113-16.)

FIG. 16

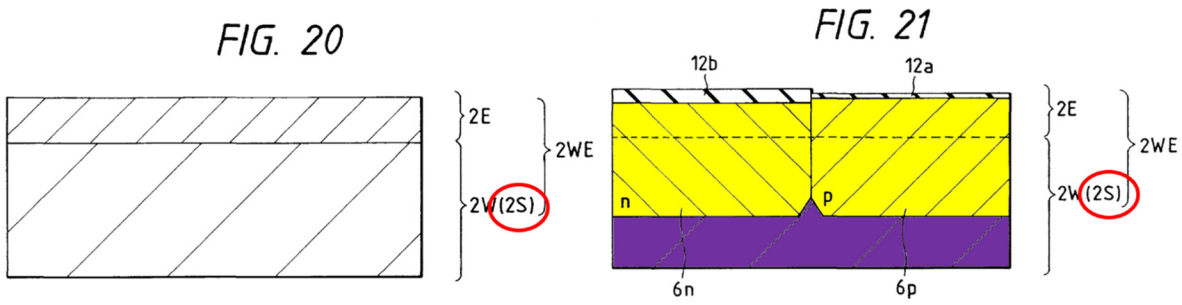


(Kawagoe at FIG. 16.)

Layers 2E and 2S are part of the semiconductor wafer prior to forming the diffusion layer. (*See* Kawagoe at FIGS. 20 and 21.) The substrate 2S is made of a p type Si single crystal which that is initially formed with a p type impurity such as boron and the epitaxial layer 2E is made up of a p- type Si single crystal. (*Id.* at 14:61-15:16.) After the wafer is formed, it is doped with impurities to create the diffusion layer that comprises n and p wells.[13] (*Id.* at 15:26-36.) This process is depicted in FIGS. 20 and 21 where—after the diffusion gradient is created (yellow)—only a portion of the

[13] 12a and 12b are masks used in the well-forming processes. (*Id.* at 17:40-49.)

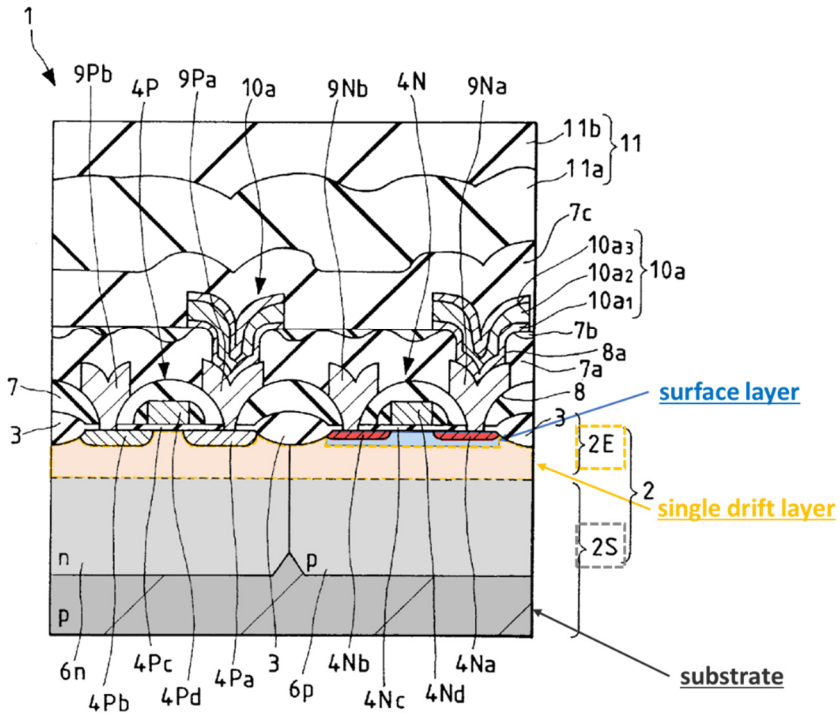
substrate has a uniform doping profile (purple). (*Id.* at 17:11-21.) (Ex. 1003 at ¶¶ 114-16.)



(Kawagoe at FIGS. 20 and 21.)

Layer 2E, if taken as a separate and distinct layer by itself, has a graded dopant concentration and satisfies the claimed "single drift layer." Ex. 1003 at ¶ 116. Its graded dopant concentration is similarly provided to attract minority carriers to the substrate. (Kawagoe at 15:62-16:11.) Layer 2E—which satisfies the "single drift layer"—is again depicted by the tan-dashed lines below. Furthermore, Layer 2S (substrate body, *e.g.*, *id.* at 15:1-17) as a whole, or merely the uniformly doped portion, further renders obvious the claimed "substrate" (both portions annotated in grey below, with the non-well region after doping in darker grey). (*See e.g.,* Element [1.2] discussion at pg. 59 and Fn. 12 (discussing "substrate.") Even under a narrow construction of Limitation [1.4], the Kawagoe structure still renders it obvious.

FIG. 16



(Kawagoe at FIGS. 16 and 17.)

Thusly, even under a prospective narrow view of Element [1.4]'s "single drift layer," one that is at odds with Patent Owner's own position in litigation and the '195 Patent specification, Kawagoe nonetheless renders Element [1.4] obvious.

Kawagoe accordingly discloses or at the very least renders Element [1.4] obvious.

f. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

Kawagoe teaches this limitation.

As described in Element [1.4], Kawagoe teaches a single drift layer with a

graded dopant profile. This graded dopant profile results in "electrons … [being] attracted to the substrate body 2S by that concentration gradient." (Kawagoe at 16:7-11.) A POSITA would understand that electrons refer to minority carriers in the p-well, and that the electrons are attracted to the substrate due to a static unidirectional electric drift field. (Ex. 1003 at ¶ 117) A POSITA would understand the field to be static because it is created by doping impurities that are fixed during device fabrication, as depicted in Kawagoe (*see, e.g.,* Kawagoe at 15:26-36, FIGS. 20-21). Ex. 1003 at ¶ 117. This was, moreover, recognized by Patent Owner as a property of a graded dopant profile in the specification of the '195 Patent and during prosecution. (Ex. 1003 at ¶ 36.) There are electric fields in separate regions due to the graded doping concentrations, *e.g.*, those depicted by pink and purple arrows in annotated FIG. 17 below, where the pink field satisfies the first static unidirectional electric drift field.[14] (Ex. 1003 at ¶ 118.).

[14] The arrow orientation and direction are depicting the drift of minority carriers (electrons) in the p-well. (Ex. 1003at ¶ 117). A POSITA would understand that the electric field would exist in the opposite direction. (*Id.*.)

FIG. 16

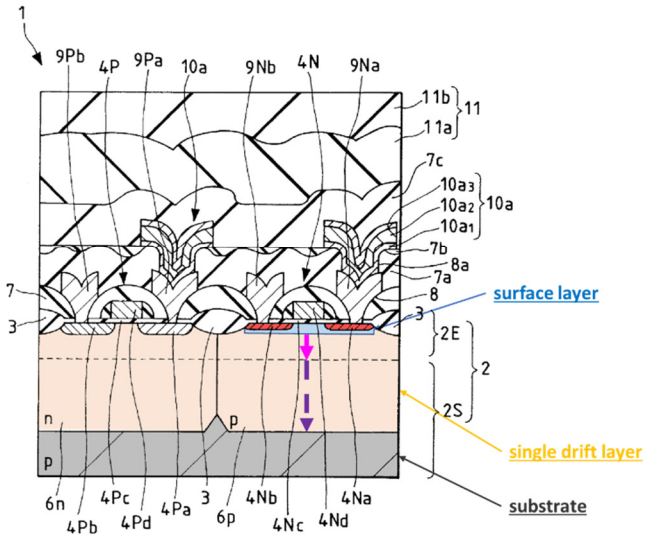
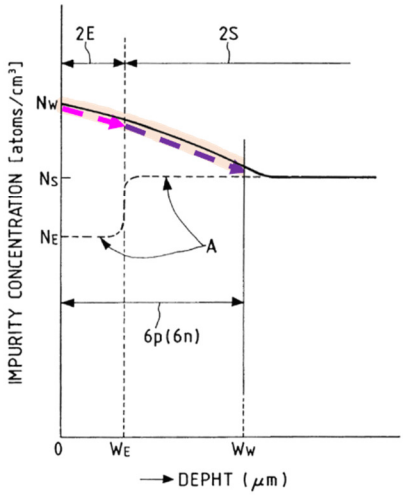


FIG. 17



(Kawagoe at FIGS. 16 and 17.)

These electric fields are not exhaustive, and a POSITA would understand that numerous fields exist in the diffusion layer to attract minority carriers to the substrate.[15] (Ex. 1003 at ¶ 118.) A POSITA would understand that Kawagoe's single drift layer has multiple static unidirectional electric drift fields that aid in the movement of minority carriers to the substrate, and that any one of them satisfies the claimed "first static unidirectional electric drift field," *e.g.*, the one depicted in pink over the epitaxial layer. (*Id.*.)

[15] Indeed, Patent Owner has argued that the limitation is not limited to a drift layer that has only one electric field, and covers the instance where there are multiple such fields. (Ex. 1030at 21 (stating that "[t]here is nothing in the claim preventing additional electric fields").)

Kawagoe thusly discloses Element [1.5].

Furthermore, as described in Element [1.4] at pages 67 - 69, Kawagoe's epitaxial layer (2E), by itself, renders obvious a narrow interpretation of the "single drift layer." Kawagoe (i.e., attracting the minority carriers to the substrate And, either the entire substrate layer (2S), or just the non-gradient portion of 2S renders the "substrate" of Element [1.2] obvious. (*Supra* at 58-59.) The epitaxial layer (2E) would similarly have the claimed "first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate" because it also has a graded dopant concentration. This is annotated by the pink arrow, below. (Ex. 1003 at ¶ 119.) For the same reasons described in Kawagoe (Kawagoe at 16:7-11) and as admitted by Patent Owner (Ex. 1030 at pg. 24), Kawagoe's graded dopant profile provides a static unidirectional electric field. (*Id.*). Thusly, a POSITA would have understood that a graded dopant concentration like Kawagoe's provides a first static unidirectional electric drift field.

FIG. 16

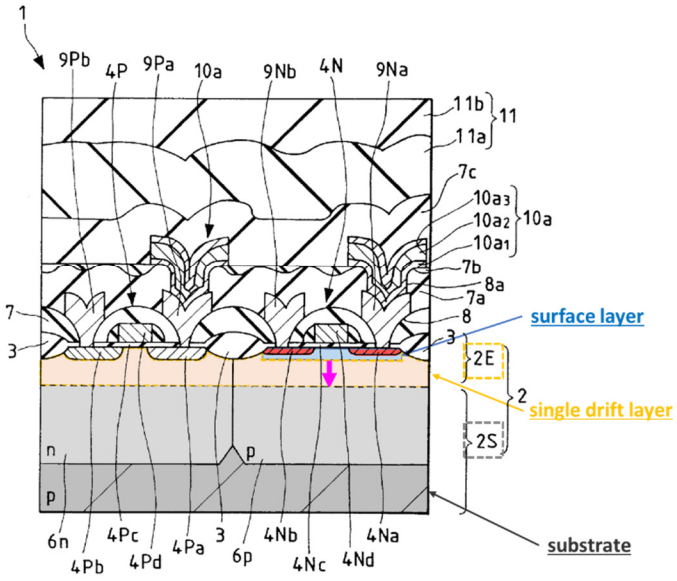
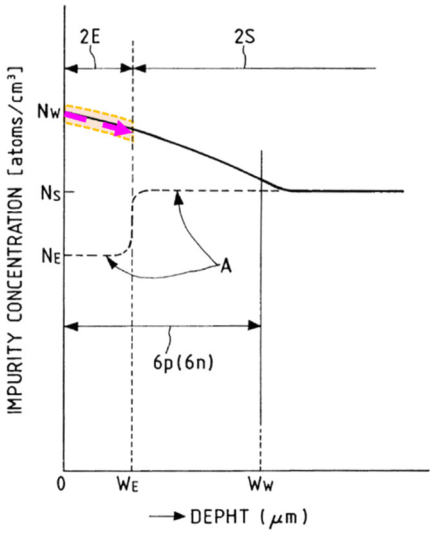


FIG. 17



Element [1.5] is thusly rendered obvious by Kawagoe.

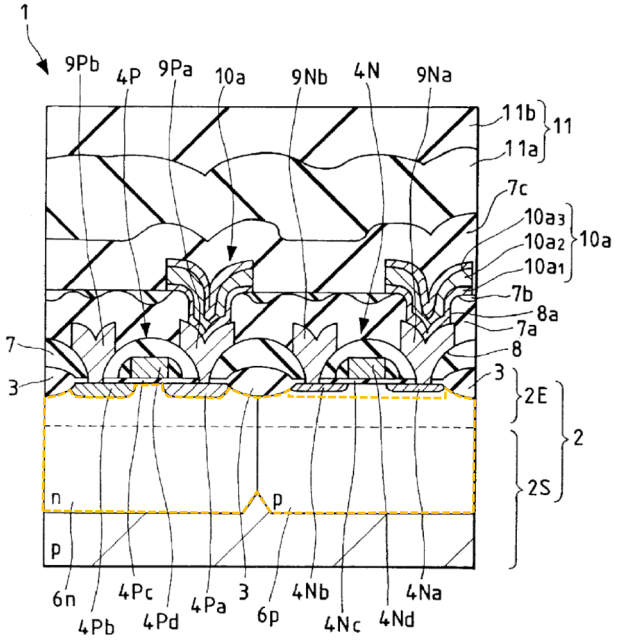
g. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

Kawagoe teaches Element [1.6].

As depicted below in annotated FIGS. 16 and 17, Kawagoe's single drift layer (the diffusion layer which comprises n and p wells) has at least one well region disposed within it (*e.g.*, the p well). This p-well is part of the diffusion layer and, like the diffusion layer described in Element [1.4], it has a graded dopant concentration. (Kawagoe at 15:62-16:15; *see also id.* at 15:26-36, 17:11-21; *see also id.* at 1:59-2:5, 2:20-23, 15:62-16:15.) (Ex. 1003 at ¶ 120.) And, as described in Element [1.5], this dopant concentration results in several static unidirectional electric drift fields, where

the pink arrow indicates the first static unidirectional electric drift field. (Ex. 1003 at ¶ 120.) The second static unidirectional electric drift field is annotated in purple. (*Id.*.) As depicted below, the well region (green) is disposed within the single drift layer (tan with tanned dashes) and graphically overlaps.

FIG. 16



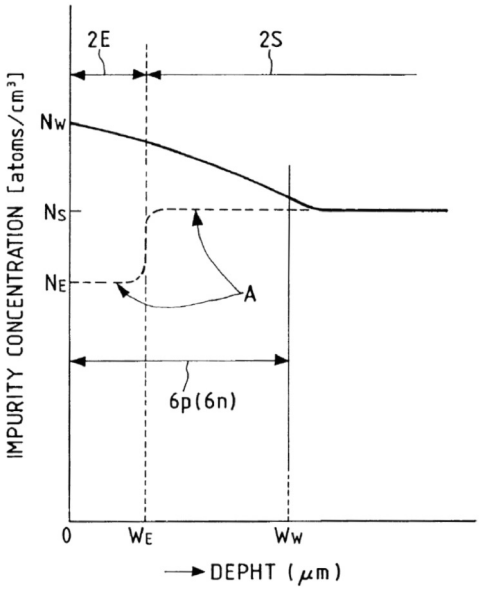
ace layer

ell region

ngle drift layer

bstrate

FIG. 17



(Kawagoe at FIGS. 16 and 17.)

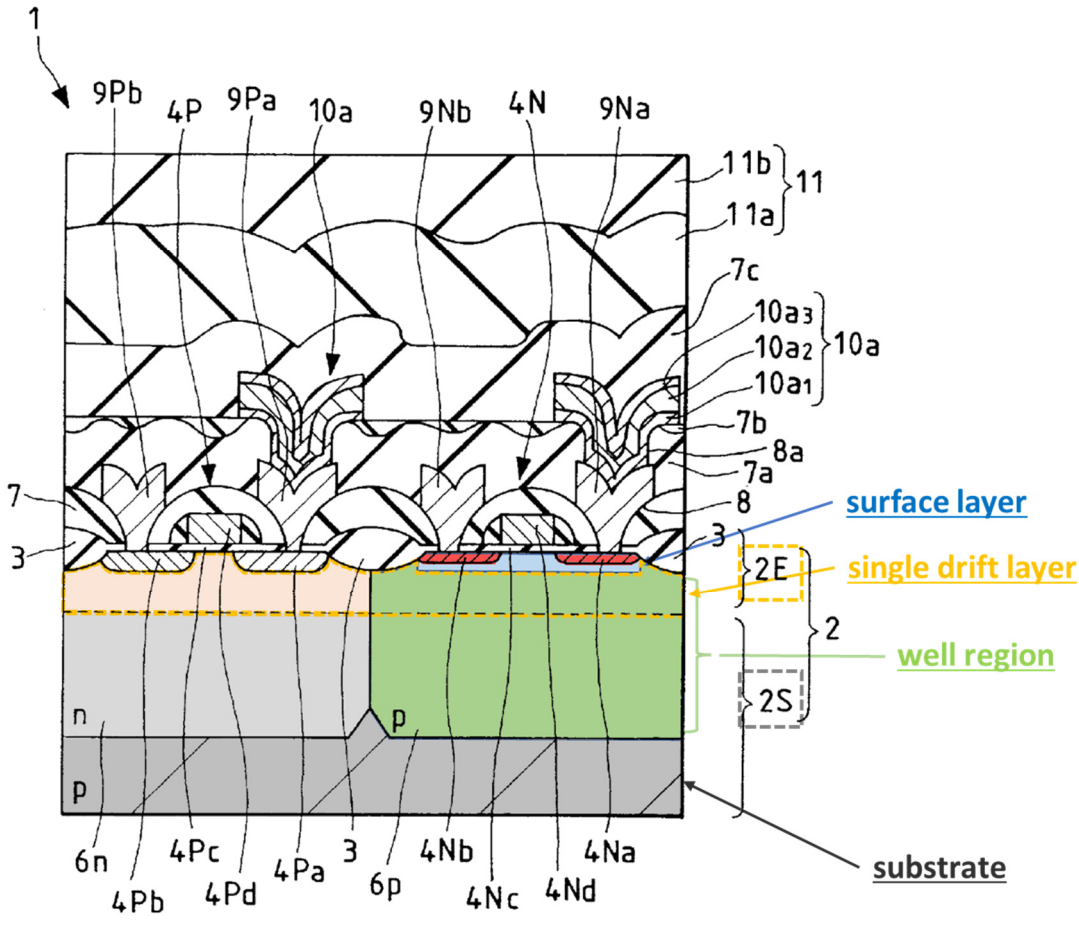
Kawagoe thusly teaches Element [1.6]

Furthermore, as described in Element [1.4], the claimed single drift layer is further rendered obvious even under a narrow construction of that term. This is because Kawagoe's epitaxial layer (2E) by itself renders obvious the claimed "single drift layer." (Ex. 1003 at ¶¶ 121-22.) And, either the entire substrate layer (2S) or just the portion of layer 2S that does not have a graded doping profile by itself independently

render obvious the "substrate" limitation. (*Id.*.) This is consistent with the limitations of Element [1.6].

The epitaxial layer (2E) has at least one well region that is disposed in it and it thusly satisfies the limitations of Element [1.6]. The "single drift layer" is annotated in tan and, as can be seen below, the well region (green) is disposed in the single drift layer and goes into the substrate body 2S (light grey, where the undoped portion is in darker grey).

FIG. 16



(Kawagoe at FIG. 16.)

The above comports with the claim language, which requires that the well region be "disposed in" the "single drift layer," and not that the well region be disposed entirely within the single drift layer. To use a real-world example, a finger is "disposed in" a cup of water if the finger is dipped in the water even though a portion of the finger is outside the cup. Similarly, Kawagoe's well-region is "disposed in" the epitaxial layer 2E (single drift layer) even though portions of it are outside of the single drift layer.

Moreover, the well-region similarly provides a static unidirectional electric drift field for the same reasons described in Element [1.5]. (Kawagoe at 16:62-16, FIG. 17; *see also* Ex. 1003at ¶ 124.) This is depicted below, where the second static unidirectional electric drift field (purple arrow) aids the movement of minority carriers from said surface layer to said substrate.

FIG. 16

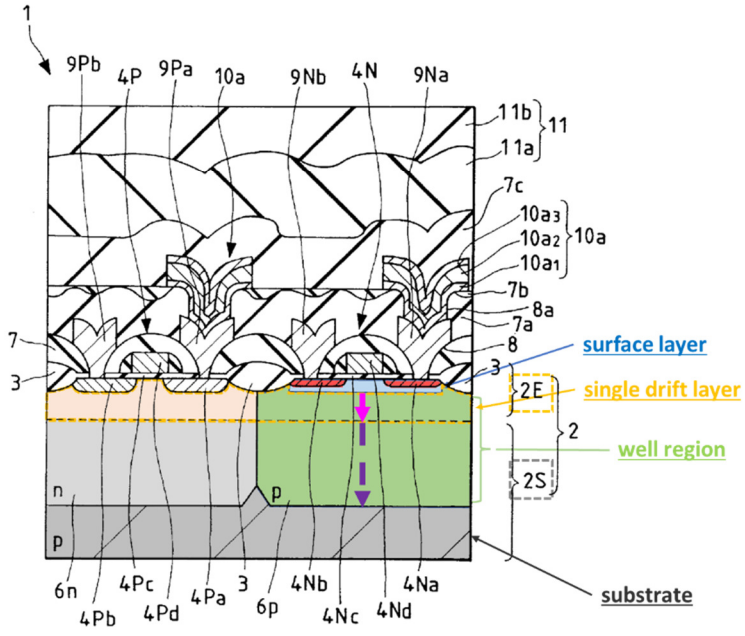
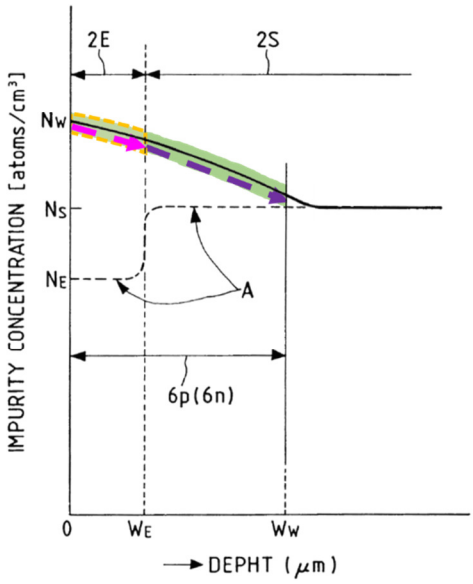
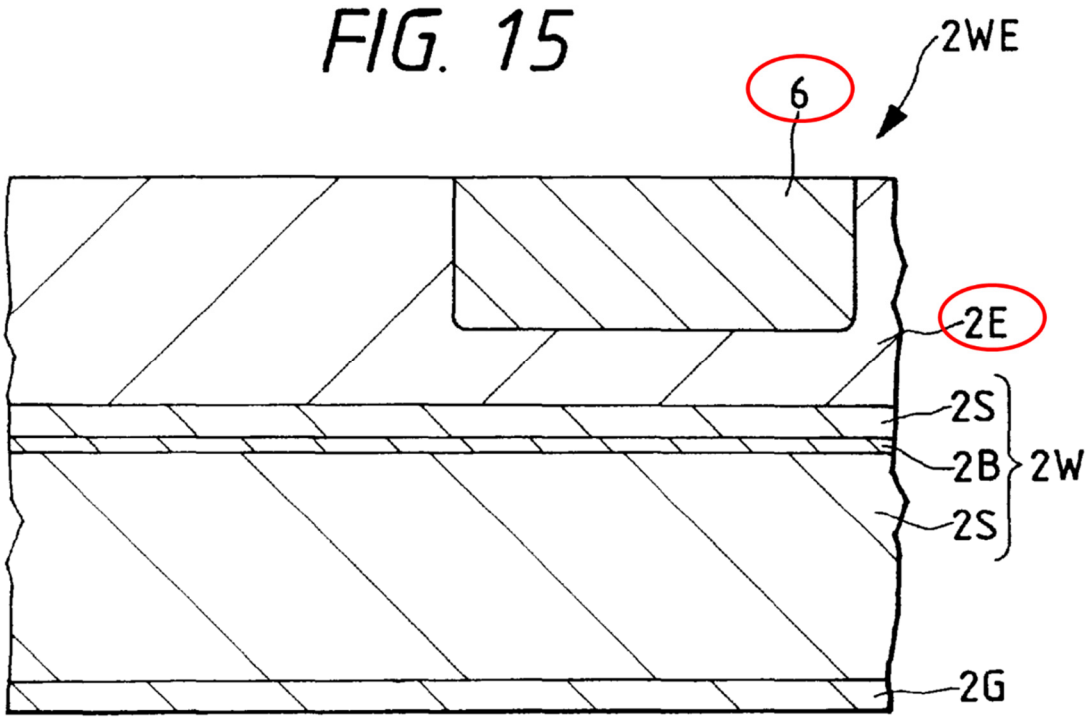


FIG. 17



(Kawagoe at FIGS. 16 and 17.)

Finally, even if "disposed in" were interpreted to require that the well region be disposed entirely within the epitaxial layer, it would have been obvious for a POSITA to modify Kawagoe's FIG. 16 embodiment to have its well region contained solely within the epitaxial layer, and not extend into the substrate (as is depicted in FIG. 16 and 17). (Ex. 1003 at ¶ 125.) Kawagoe teaches embodiments of thicker epitaxial layers (Kawagoe at 13:49-53) where the n and p well regions are confined within the epitaxial layer, and do not extend to the substrate. (*Id.* at FIG. 15 (excerpted and annotated below).)



(Kawagoe at FIG. 15.)

Kawagoe further teaches a gradient whose "impurity concentration gradually

lowered depthwise of said epitaxial layer" (Kawagoe at Abstract) and that the "impurity concentration [is] gradually lowered ***depthwise of said semiconductor single crystal layer***." (*Id.* at 3:22-23 (emphasis added); *see also id.* at 2:59-61 (making clear that the "semiconductor single crystal layer" is the epitaxial layer over the substrate).) (Ex. 1003 at ¶ 126.) Kawagoe thusly teaches a well region within the epitaxial layer.

A POSITA would have found it obvious to apply these teachings to modify the above-described FIG. 16 of Kawagoe to have the well region exist within the epitaxial layer (and not extend into the substrate), because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. *See, e.g., KSR*, 550 U.S. at 418. It would have been obvious to try; Kawagoe teaches that a POSITA has a degree of freedom for setting the impurity concentration and depth of its layers. (Kawagoe at 25:10-14.) A POSITA would have recognized this degree of freedom in creating layer depths, and would have found it an obvious variant to create the depth of the well region to be confined within the epitaxial layer and not extend into the substrate according to Kawagoe's other embodiments. (*See, e.g., id.* at 2:59-61, 3:22-23, 13:49-53, FIG. 16.) This would have been a simple substitution and would have yielded predictable results: a POSITA would understand that Kawagoe's well region, if it went up to but not into the substrate, would achieve a goal of Kawagoe (*i.e.,* attracting the minority carriers to the substrate, *id.* at 16:7-11) and would work for its intended purpose. (Ex. 1003 at ¶ 126.) .

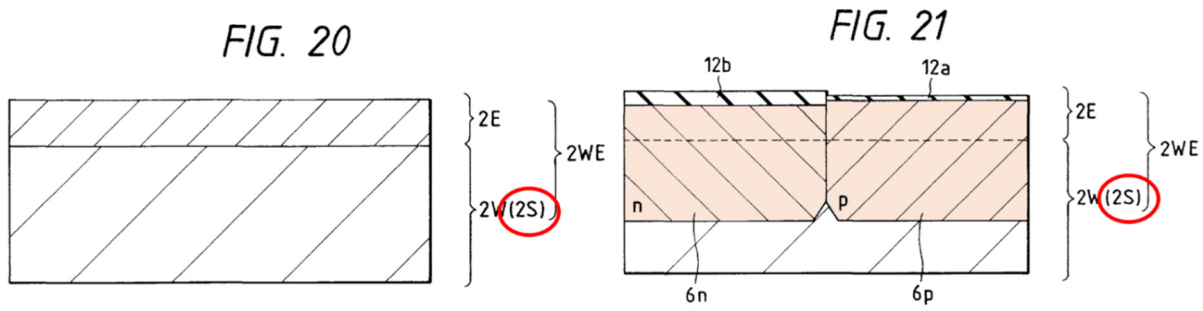
Thusly, Kawagoe discloses or at least renders obvious Element [1.6].

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

Kawagoe renders obvious claim 2.

The '195 Patent mentions the deeply implanted layer once (*e.g.*, '195 Patent at 3:37-38) and mentions "deep" in another context, sweeping carriers "deep into the substrate." (*Id.* at 3:33-35.) The specification, however, does not discuss the depth of the "deeply-planted layer" or the process of forming such a layer. However, a POSITA would understand a diffusion layer that goes into the substrate to be "deeply implanted." (Ex. 1003 at ¶ 127.)

Kawagoe teaches that its diffusion layer extends into the substrate. As depicted in FIGS. 16 and 17, the diffusion layer is "formed to extend from the surface of the epitaxial layer 2E to the upper portion of the substrate body … [where its] impurity concentration[] [is] gradually lowered in the depthwise direction." (Kawagoe at 15:62-16:4.) The layers of the wafer are originally formed via "ion implantation" (*id.* at 17:32-49) and are annealed to extend the diffusion. (*Id.* at 17:50-54.) As depicted in FIG. 20, the semiconductor wafer has two layers with one being substrate 2S (annotated red) and, after the fabrication process, the diffusion layer extends into 2S (annotated tan in FIG. 21). (Ex. 1003 at ¶ 128.)



(Kawagoe at FIGS. 20 and 21.)

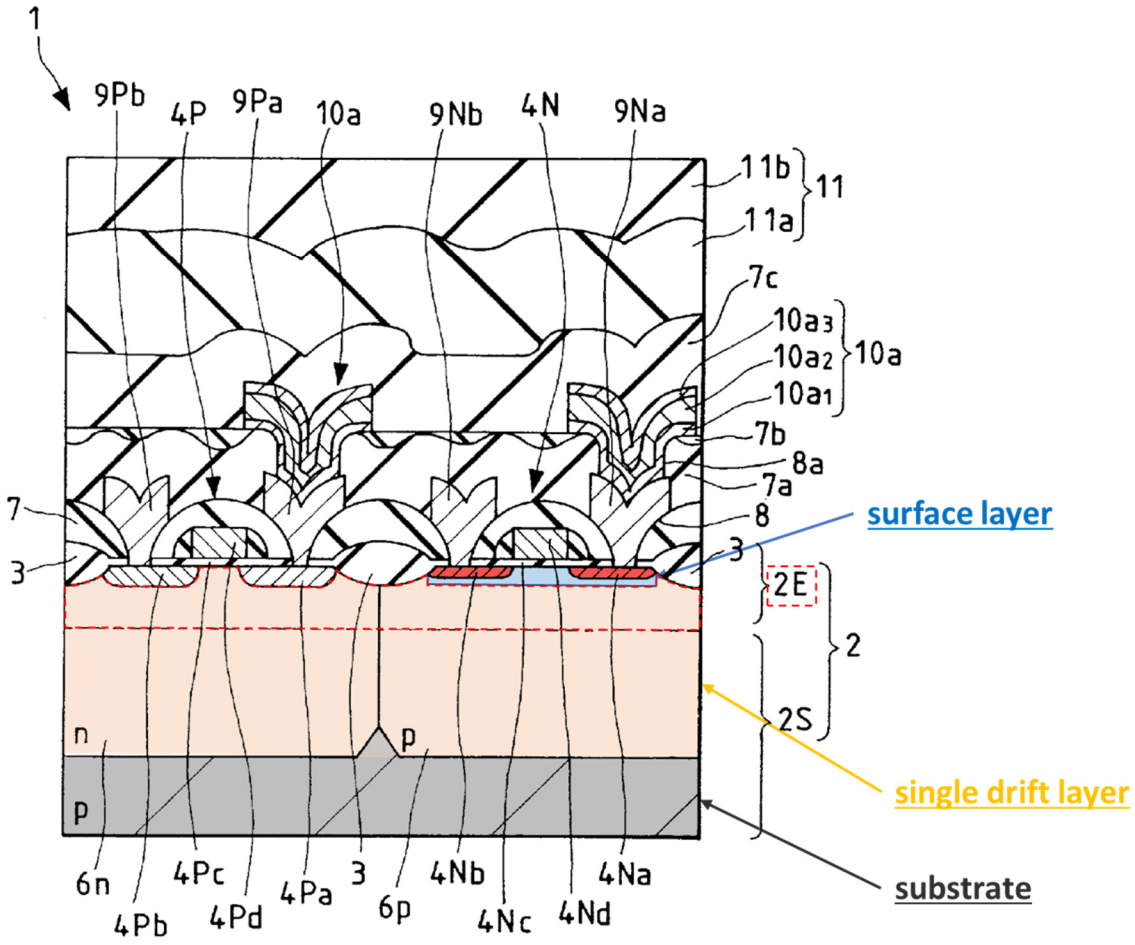
Kawagoe thusly renders obvious claim 2.

3. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein the said drift layer is an epitaxial layer."

Kawagoe renders obvious claim 3.

As described in Element [1.4], the claimed "drift layer" is partly within the epitaxial layer (*e.g.*, pages 63-67 detailing one aspect of claim scope) or entirely within the epitaxial layer (*e.g.*, pages 67-70 detailing one aspect of claim scope). This is depicted in annotated FIG. 16, below, where the epitaxial layer 2E is depicted as being bounded by the dashed-red border.

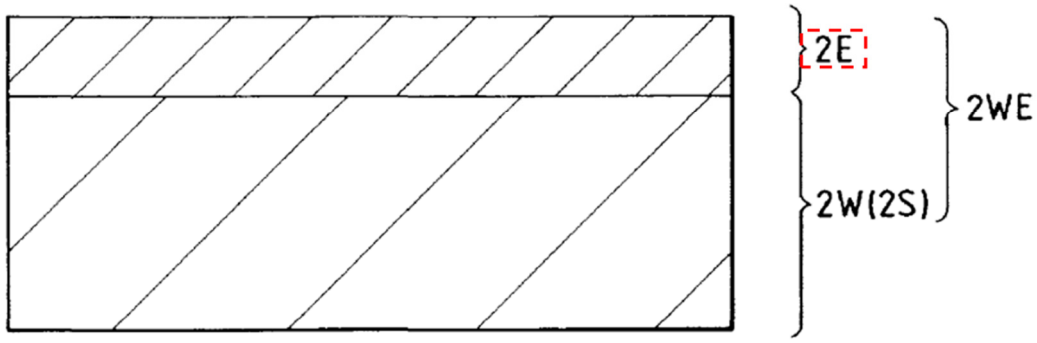
FIG. 16



(Kawagoe at FIG. 16.)

FIG. 20 depicts the epitaxial wafer 2WE (*e.g.*, Kawagoe at 14:23-29 (describing 2WE as the epitaxial wafer)) prior to formation of the graded dopant region. (*Id.* at 14:47-60 (describing FIGS. 20-24 as depicting manufacturing steps for Embodiment 4.) The epitaxial layer 2E is formed (*id.* at 15:26-36) and thereafter the diffusion layer is formed. (*Id.* at 15:62-16:15.) (Ex. 1003 at ¶¶ 129-30.)

FIG. 20



(Kawagoe at FIG. 20.)

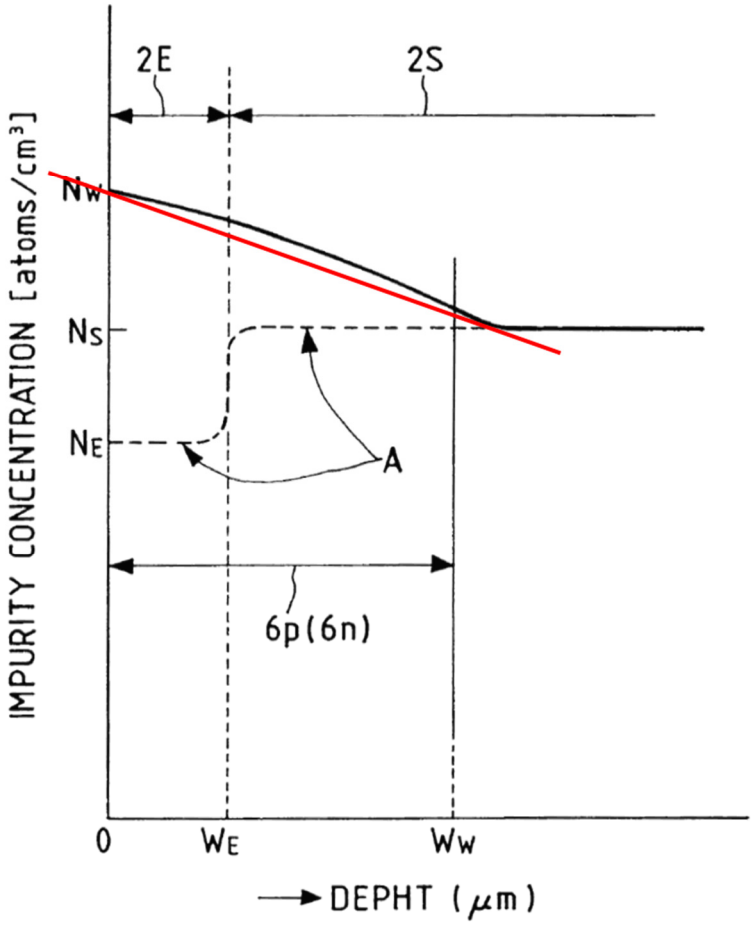
Kawagoe thusly renders obvious claim 3.

4. Dependent Claim 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient."

Kawagoe renders obvious Claim 5.

As detailed in Element [1.4], FIG. 17 depicts a graded concentration. (Kawagoe at 16:16-40.) A POSITA would have interpreted FIG. 17 to encompass a quasi linear gradient (a linear gradient is depicted in red). (Ex. 1003 at ¶¶ 131-32).

FIG. 17



(Kawagoe at FIG. 17.)

Even if Patent Owner were to argue that FIG. 17 does not render obvious a quasi-linear dopant profile, a POSITA would have nonetheless found it obvious to use a quasi-linear gradient because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. (Ex. 1003 at ¶¶ 132.) *See, e.g., KSR*, 550 U.S. 398 at 418. Indeed, the '195 Patent only mentions quasi-linear gradient once ('195 Patent at 2:40-42) and does not illustrate or otherwise describe it,

or describe any process steps for obtaining it – thus confirming that such a gradient was a well-known alternative to a POSITA.[16] It would have been obvious to modify Kawagoe's dopant profile (which is already graphically depicted as quasi-linear) based on the POSITA's general knowledge in the art to achieve a known quasi-linear gradient. (Ex. 1003 at ¶ 132.) This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success. (*Id.*.)

Kawagoe thusly renders obvious claim 5.

5. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient."

Kawagoe renders obvious claim 6.

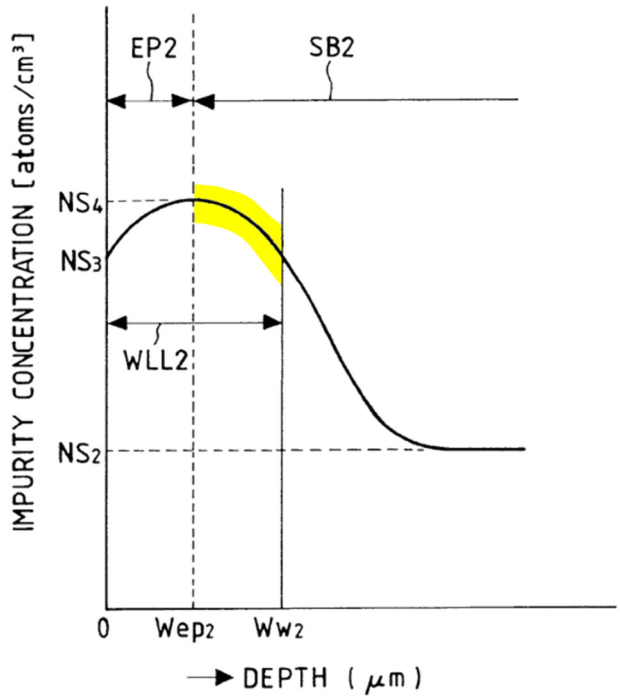
A POSITA would have found it obvious to modify Kawagoe's diffusion profile depicted in FIG. 17 to be exponential in view of Kawagoe's teachings. (Ex. 1003 at ¶¶ 133-34.)

Kawagoe depicts an exponentially downward dopant gradient for the well region (within the substrate) in FIG. 19. (Kawagoe at 16:62-17:10; *see also id.* at 1:58-65.)

[16] *See, e.g., Ex Parte Nico Hawley-Weld,* 2022 WL 17495059, at *7; *In re Epstein*, 32 F.3d at 1568.

As can be seen below, the rate of downward progression starts slowly then increases as depth increases, which a POSITA would understand to be an exponential decrease. (Ex. 1003 at ¶ 133.)

FIG. 19
PRIOR ART



(Kawagoe at FIG. 19.)

Moreover, a POSITA would have found it obvious to use an exponential gradient instead of, for example, a linear or quasi-linear gradient, because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. (Ex. 1003 at ¶ 134.) *See, e.g., KSR,* 550 U.S. 398 at 418. As with the "quasi-linear" gradient limitation in Claim 5, the '195 Patent only mentions "exponential" gradient once and does not illustrate or otherwise describe it, or describe

any process steps for obtaining it, thus confirming that it was a well-known alternative to a POSITA.[17] ('195 Patent at 2:40-42.)

Moreover, Kawagoe recognizes an exponential downward gradient as a known technique (Kawagoe at 16:62-17:10), and further recognizes that a downward gradient causes minority carriers to drift from the surface to the substrate. (*Id.* at 15:62-16:15.). It would have been obvious to modify Kawagoe's graded-dopant profile based on the POSITA's general knowledge in the art to achieve a known exponential gradient. (Ex. 1003 at ¶ 135.) .) This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success. (*Id.*.)

Kawagoe thusly renders claim 6 obvious.

IX. THE BOARD SHOULD INSTITUTE IPR

1. 35 U.S.C. § 314(a)

On June 21, 2022, the Director issued an interim procedure regarding application of the *Fintiv* factors (Interim Procedure) in which the Director clarified that "the PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling

[17] *See, e.g., Ex Parte Nico Hawley-Weld,* 2022 WL 17495059, at *7; *In re Epstein*, 32 F.3d at 1568.

evidence of unpatentability." Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," 9 (June 21, 2022). As just one example of compelling evidence here, Ground I is a single-reference obviousness ground explaining how Onoda discloses or, at a minimum, renders obvious all of the Challenged Claims. While Onoda is subject to a pending IPR (IPR2024-00017), it is being presented differently here on new grounds never before examined and also presented in Ground II in combination with never-before-examined Nishizawa. Moreover, IPR2024-00017 is in its preliminary stages, having not reached preliminary response at the time of this filing. Further, Kawagoe has never before been provided as a single reference obviousness ground, and was never subject to any examination or review by the Board.

None of Petitioner's references (Onoda, Kawagoe, Nishizawa) were examined by the Board or the USPTO during prosecution. And, this evidence, "if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable" (Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," at 4) and the Board must decline to exercise its discretion under §314(a) to deny institution. *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022- 00938, Paper 8 at 9 (P.T.A.B. Nov. 1, 2022).

2. 35 U.S.C. § 325(d)

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B.*

Braun Melsungen AG, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020).

The Board has consistently "held that a reference that 'was neither applied against the claims nor discussed by the Examiner does not weigh in favor of exercising [] discretion under §325(d)." *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7–11 (P.T.A.B. Nov. 5, 2019); *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5-6 (P.T.A.B. Aug. 6, 2019). That is the case here because none of the ground references (Onoda, Kawagoe, Nishizawa) is cited art, and the arguments presented herein were not considered during prosecution of the '195 Patent.

Patent Owner has previously incorrectly argued that other art not at issue in this Petition was cumulative to already-examined art (U.S. Pat. Pub. No. 2003/0042511, Rhodes). (Ex.1011 at 21-24.) Patent Owner's arguments there lack merit, and are similarly inapplicable to Onoda and Kawagoe.

Onoda and Kawagoe are not cumulative with Rhodes. The Examiner relied on Rhodes' paragraphs [0046], [0047], [0049], and [0049], and FIGS. 5-14 in rejection, stating that well-regions 160/170/180 aid carrier movement from the surface regions to the substrate. (Ex. 1002 at 55-56.) In response, Patent Owner amended the claims to recite "VLSI digital" and that "the active channel regions" aid in carrier movement (Ex. 1002 at 72, 94), and further argued that Rhodes is inapplicable to CMOS image sensors because it only provides a graded dopant concentration in the image sensor.

(*Id.* at 74; *see also id.* at 97.) Patent Owner argued:

> "Rhodes describes a CMOS image sensor- but, his sensor elements only uses electrons (a CMOS gate, by strict text book definition has a n-channel transistor that conducts electrons and a p-channel transistor that conducts holes). The 'graded dopant' as described by Rhodes, is only in the 'sensing element.' Rhodes may have one million sensors (he may have a few CMOS transistors in periphery on non image sensing function). However, that does not make the device in Rhodes VLSI and certainly not CMOS VLSI."

(*Id.* at 74; *see also id.* at 97.)

The Examiner thereafter dropped rejections based on Rhodes. (*Id.* at 111-115.)

Here, in contrast, both Onoda and Kawagoe describe CMOS and, moreover, provide graded dopants in p wells having active regions that form conductive channels in memory devices. (Ex. 1003 at ¶ 32-24.) Moreover, Figure 2 of Onoda discloses forming P-type well regions (105a through 105c) and N-type well regions (103, 106a through 106c) in a lightly-doped semiconductor layer 102 that is formed through epitaxial deposition. (Onoda at FIG. 2.) Kawagoe similarly provides well regions doped into an epitaxial layer. (Kawagoe at FIG. 16.) Onoda and Kawagoe describe non-cumulative systems that are relevant to the claims in a manner that Rhodes was not.

Onoda and Kawagoe are not cumulative and, even assuming *arguendo* that they were, the Examiner overlooked Rhodes' relevance to CMOS devices and downward

graded dopant well regions as claimed due to Patent Owner's arguments regarding Rhodes. In either case, review of the challenged claims is warranted.

3. Prior Petitions Do Not Warrant Denying Institution

While several Petitions have been filed, none of the prior challenges to the '195 Patent reached an institution decision. In addition, the entity challenging the '195 Patent in this Petition here is a defendant in a district court case and would potentially be severely prejudiced if this Petition is not instituted. *Apple Inc. v. Uniloc 2017 L*LC, IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020). In light of the foregoing, *General Plastic* factors weigh strongly against discretionary denial. *Xilinx, Inc. v. Arbor Global Strategies, LLC,* IPR2020-01568, Paper No. 12 at 10 (P.T.A.B. Mar. 5, 2021).

Dated: February 2, 2024

Respectfully submitted,

/ Bing Ai /

Lead Counsel
Miguel Bombach, Reg. No. 68,636

Back-up Counsel
Bing Ai, Reg. No. 43,312
John D. Esterhay, Reg. No. 73,512
John P. Schnurer, Reg. No. 52,196
Runkun (Justin) Jiang, Reg. No. 78,118

Attorneys for Petitioner

PERKINS COIE LLP
11452 El Camino Real, Ste 300
San Diego, California 92130-2080
858.720.5700 (phone)
858.720.5799 (fax)

CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(D)

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this *Petition for Inter Partes Review* totals 13,586 [max 14,000], excluding the parts exempted by 37 C.F.R. §42.24(a).

The word count was made using the built-in word count function in the Microsoft 365 software used to prepare this document.

Dated: February 2, 2024

Respectfully submitted,

/ Bing Ai /
Lead Counsel
Miguel Bombach, Reg. No. 68,636

Back-up Counsel
Bing Ai, Reg. No. 43,312
John D. Esterhay, Reg. No. 73,512
John P. Schnurer, Reg. No. 52,196
Runkun (Justin) Jiang, Reg. No. 78,118

Attorneys for Petitioner

PERKINS COIE LLP
11452 El Camino Real, Ste 300
San Diego, California 92130-2080
858.720.5700 (phone)
858.720.5799 (fax)

CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of this PETITION FOR INTER PARTES REVIEW and supporting materials (Exhibits 1001-1028, 1030, 1032-1047 and Power of Attorney) have been electronically served in their entireties on counsel for patent owner as follows:

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

and the attorneys of record for Plaintiff in the concurrent litigation matter:

Brian E. Farnan - bfarnan@farnanlaw.com
Alan L. Whitehurst - awhitehurst@mckoolsmith.com
Archis Ozarkar - nozarkar@mckoolsmith.com
Arvind Jairam - ajairam@mckoolsmith.com
Emily Tate - etate@mckoolsmith.com
John B. Campbell , Jr. - jcampbell@mckoolsmith.com
Kaitlyn M. Dawson - kdawson@mckoolsmith.com
Kaylee Hoffner - khoffner@mckoolsmith.com
Michael J. Farnan - mfarnan@farnanlaw.com
Nicholas T. Matich - nmatich@mckoolsmith.com

In addition, the undersigned certifies that a true copy of the petition and supporting materials have been served on Patent Owner via email to its legal counsel:

Patent Owner Attorney
GHowison@munckwilson.com

Dated: February 2, 2024

Respectfully submitted,

/Bing Ai/

Lead Counsel
Miguel Bombach, Reg. No. 68,636

Back-up Counsel
Bing Ai, Reg. No. 43,312
John D. Esterhay, Reg. No. 73,512
John P. Schnurer, Reg. No. 52,196
Runkun (Justin) Jiang, Reg. No. 78,118

Attorneys for Petitioner

PERKINS COIE LLP
11452 El Camino Real, Ste 300
San Diego, California 92130-2080
858.720.5700 (phone)
858.720.5799 (fax)