IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GREENTHREAD, LLC **Plaintiff,** **vs.** **MONOLITHIC POWER SYSTEMS, INC.** **Defendant.**	**Civil Action No. 23-cv-579-RGA-LDH** **JURY TRIAL DEMANDED**

GREENTHREAD'S PRELIMINARY INFRINGEMENT CONTENTIONS

Pursuant to the Court's Scheduling Order (D.I. 19), Plaintiff Greenthread, LLC ("Greenthread") provides its infringement contentions in the attached exhibits and the disclosure below.

Greenthread's disclosures are based on publicly available materials regarding the accused infringing products of Monolithic Power Systems, Inc. ("MPS"). Greenthread does not yet have access to any of Defendant's discovery materials that may be relevant to its infringement claims and thus relies on publicly available materials. In light of the absence of discovery and reliance on publicly available materials, Greenthread has procured limited physical testing to the extent practicable, of certain products believed to be representative of, and similar to, the accused infringing products in pertinent respects. Greenthread explicitly reserves the right to supplement or alter its disclosures herein, as a matter of right, as permitted by the Court, based on the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances.

Greenthread Ex. 2016, p. 1 of 76
MPS v. Greenthread
IPR2024-00468

I. ASSERTED PATENTS

Based on available information, Plaintiff served its Identification of Accused Products and Asserted Claims on Defendant on October 12, 2023. The Notice of Service was filed on October 12, 2023. (D.I. 22).

Greenthread explicitly reserves the right to supplement or alter its identification of asserted claims, as a matter of right, as permitted by the Court, based on any further claim constructions, additional information obtained through formal discovery or other means, and/or based on other circumstances.

II. MPS ACCUSED PRODUCTS

As referenced above, Plaintiff served its Identification of Accused Products and Asserted Claims on Defendant on October 12, 2023.

III. INFRINGEMENT CONTENTION CLAIM CHARTS

Based upon information presently available to it, Greenthread's preliminary infringement claim charts are provided as attached Exhibits A-1 through A-6. In each claim chart, the discussion for dependent claims should be read as incorporating by reference the discussion corresponding to the claims from which they depend. In addition, the discussion for each row in the chart should be read within the context of the discussion for the entire claim to which that row pertains. Where the charts incorporate excerpts of particular documents, the reference to those excerpts is exemplary and not to the exclusion of any other excerpt or version of the document or any versions of related documents.

Greenthread alleges that MPS directly infringes each of the Asserted Claims by making, using, offering for sale, and selling each of the Accused Products in the United States, or by importing the Accused Products into the United States. Greenthread alleges that the Accused Products literally infringe each limitation of each Asserted Claim. Greenthread further alleges that

MPS indirectly infringes each of the Asserted Claims of the Asserted Patents by inducing its customers to directly infringe those claims. Greenthread alleges that MPS has acted and continues to act with knowledge of the Asserted Claims of the Asserted Patents and with the intent to induce infringement by its customers by designing and marketing infringing products for sale, use, and importation into the United States. Greenthread incorporates by reference the allegations in Greenthread's Complaint (D.I. 1).

These infringement claim charts are based upon Greenthread's investigation to date. More complete information about the MPS Accused Products is in the possession of Defendant and is expected to be obtained through discovery. Greenthread explicitly reserves the right to supplement or alter its preliminary infringement claim charts, as a matter of right, as permitted by the Court, based on the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances.

IV. LITERAL INFRINGEMENT AND/OR DOCTRINE OF EQUIVALENTS

Unless otherwise noted in the claim charts, Greenthread alleges that Defendant infringes literally all asserted claims. To the extent any differences are alleged to exist between the asserted claims and Defendant's Accused Products, such differences are insubstantial and Defendant's Accused Products perform substantially the same function, in substantially the same way, to yield substantially the same result, and therefore Defendant infringes under the doctrine of equivalents.

Greenthread explicitly reserves the right to supplement or alter its disclosure concerning the doctrine of equivalents, as a matter of right, as permitted by the Court, based on the Court's claim constructions, based on additional information obtained through formal discovery or other means, and/or based on other circumstances. In the event that a claim limitation is deemed to be missing under a literal infringement analysis, Greenthread also reserves the right to demonstrate

the presence of a substantial equivalent of such limitation and to pursue infringement under the doctrine of equivalents.

Dated: December 13, 2023

Respectfully submitted,

FARNAN LLP

/s/ Brian E. Farnan

Brian E. Farnan (Bar No. 4089)
Michael J. Farnan (Bar No. 5165)
919 North Market St., 12th Floor
Wilmington, DE 19801
Tel: (302) 777-0300
Fax: (302) 777-0301
bfarnan@farnanlaw.com
mfarnan@farnanlaw.com

Alan Whitehurst (admitted *pro hac vice*)
Nicholas Matich (admitted *pro hac vice*)
Arvind Jairam (admitted *pro hac vice*)
MCKOOL SMITH, P.C.
1999 K Street, NW Suite 600
Washington, D.C. 20006
Telephone: (202) 370-8300
Telecopier: (202) 370-8344
awhitehurst@McKoolSmith.com
nmatich@McKoolSmith.com
ajairam@McKoolSmith.com

Samuel F. Baxter
Jennifer Truelove
MCKOOL SMITH, P.C.
104 East Houston Street, Suite 300
Marshall, TX 75670
Telephone: 903-923-9000
Telecopier: 903-923-9099
sbaxter@mckoolsmith.com
jtruelove@mckoolsmith.com

John B. Campbell (admitted *pro hac vice*)
MCKOOL SMITH, P.C.
303 Colorado Street, Suite 2100
Austin, TX 78701
Telephone: (512) 692-8730

jcampbell@McKoolSmith.com

Neil Ozarkar (admitted *pro hac vice*)
Kaylee Hoffner (admitted *pro hac vice*)
MCKOOL SMITH, P.C.
600 Travis Street, Suite 7000
Houston, Texas 77002
Telephone: 713-485-7300
Telecopier: 713-485-7344
nozarkar@mckoolsmith.com
khoffner@mckoolsmith.com

Emily B. Tate (admitted *pro hac vice*)
MCKOOL SMITH, P.C.
One Manhattan West
395 9th Avenue, 50th Floor
New York, NY 10001
Telephone: 212-402-9400
Telecopier: 212-402-9444
etate@mckoolsmith.com
Attorneys for Plaintiff Greenthread, LLC

CERTIFICATE OF SERVICE

I, Brian E. Farnan, hereby certify that on December 13, 2023, a copy of Greenthread's Preliminary Infringement Contentions was served on the following as indicated:

Via E-Mail
John G. Day
Andrew C. Mayo
ASHBY & GEDDES
500 Delaware Avenue, 8th Floor
P.O. Box 1150
Wilmington, DE 19899
jday@ashbygeddes.com
amayo@ashbygeddes.com

Attorneys for Defendant Monolithic Power Systems, Inc.

Via E-Mail
John P. Schnurer
John D. Esterhay
Miguel J. Bombach
PERKINS COIE LLP
JSchnurer@perkinscoie.com
JEsterhay@perkinscoie.com
MBombach@perkinscoie.com

Attorneys for Defendant Monolithic Power Systems, Inc.

/s/ Brian E. Farnan
Brian E. Farnan (Bar No. 4089)

U.S. Patent No. 10,510,842	Accused Products MPS Semiconductor 86905 SiC N-Channel MOSFET
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905"). The 86905 was analyzed in the below referenced report from Tech Insights. MPS MP86905 Intelli-PhaseTM Solution with Integrated HS/LS-FETs and Driver Power Essentials Summary ("MP86905 Report"), *available at* https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2202-801&genealogyCode=MPS-MP9502. The 86905 was also analyzed in a supplemental report from Tech Insights ("MP86905 Supplemental Report"). *See* Exhibit 8 (Supplemental Report for PEF-2202-801). The complete reports are hereby incorporated by reference into each and every claim and claim element discussed. Selected pages are reproduced herein to aid in understanding. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). The claimed invention would have application in numerous types of MPS products, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOFSET drivers, insolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, and current sensors, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. The MPS Accused Products, of which MPS 86905 is one example, are semiconductor devices.

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

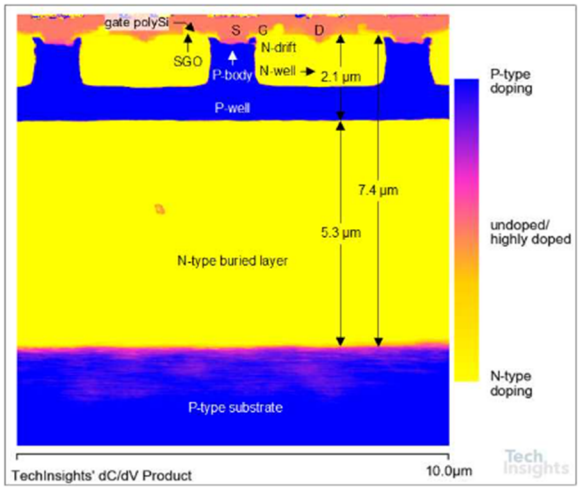
Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm²)
Minimum measured transistor gate length/pitch	0.40 µm/0.86 µm
Process generation	Likely 0.18 µm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Report at 5.

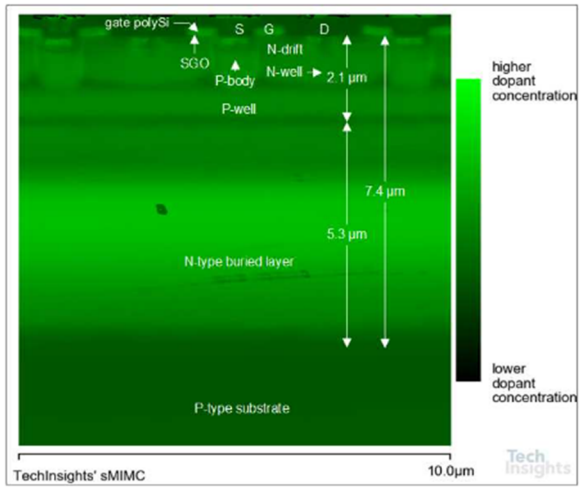
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

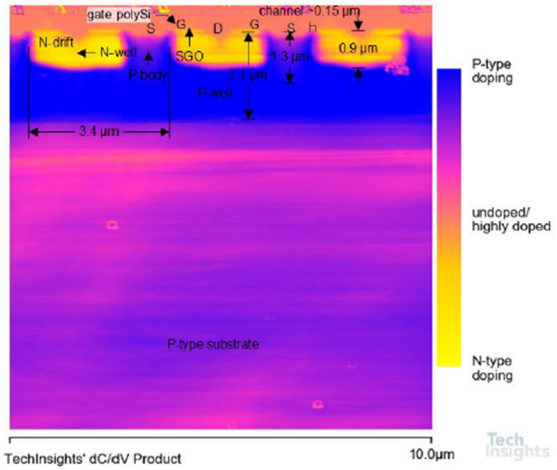
HSFET Array – sMIM-C Cross-Section A-A

All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Report at 42.

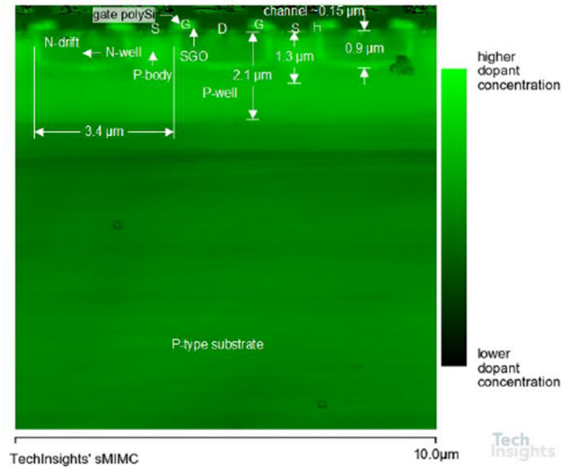
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

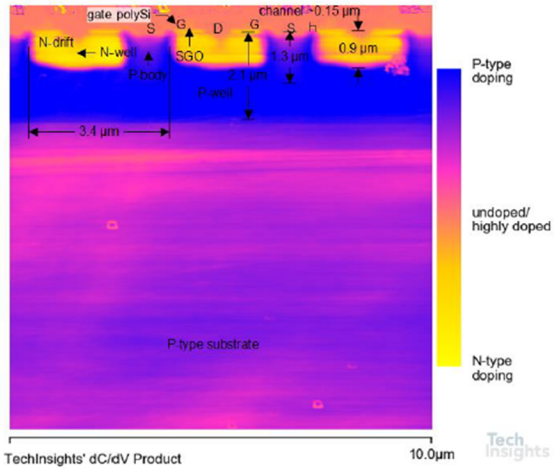
All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Supplemental Report at 2.

	Statement of Measurement Uncertainty and Scope Variation **Statement of Measurement Uncertainty** TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI). Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used. TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the micrometer's 100 µm pitch lines. Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width. TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers. The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration. Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request. **Statement of Scope Variation** Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports. 3 All content © 2022 TechInsights Inc. All rights reserved. TechInsights MP86905 Supplemental Report at 3.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary MPS Accused Product (the MPS 86905 discussed above) reveals the presence of such a substrate. For example, the MPS 86905 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

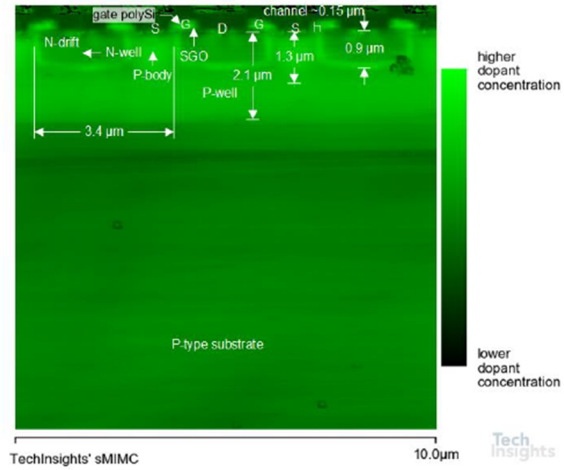
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



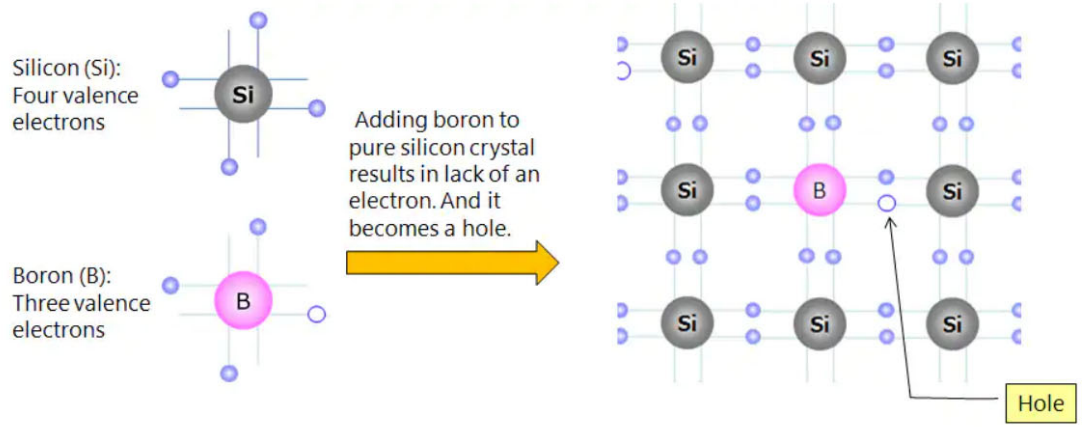
Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

All content © 2022 TechInsights Inc. All rights reserved.

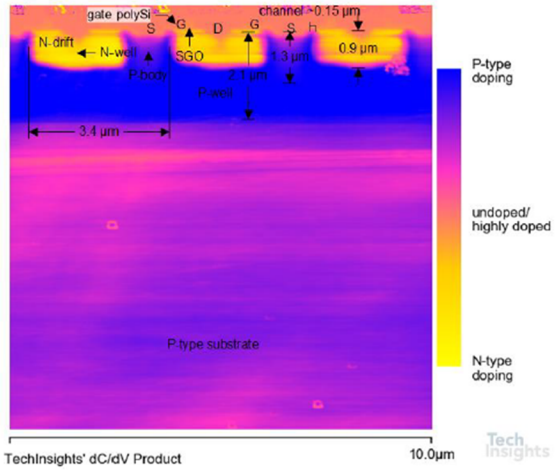
MP86905 Supplemental Report at 2.

	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which	The MPS Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary MPS 86905 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. *See* below showing "HSFET Array," and toward the top the source ("S"), gate ("g") and drain ("drain") where the transistors are, underneath each of the annotations are active regions. *See also* below showing "LSFET Array."

transistors can be formed;

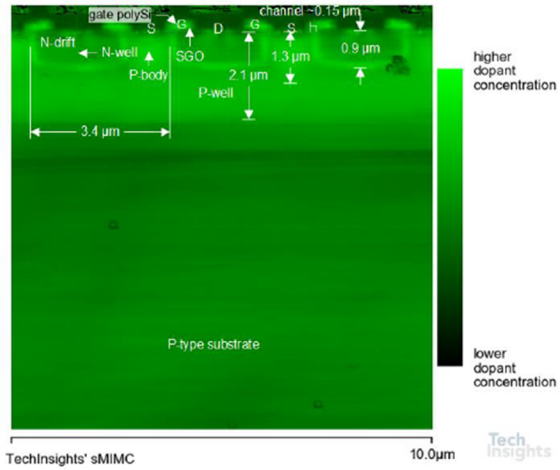
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

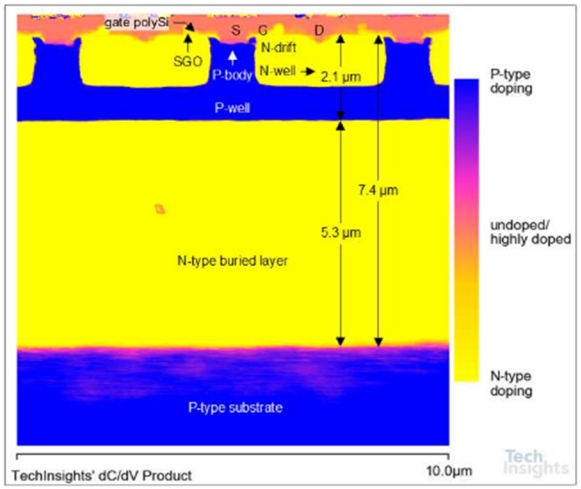
2

All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Supplemental Report at 2.

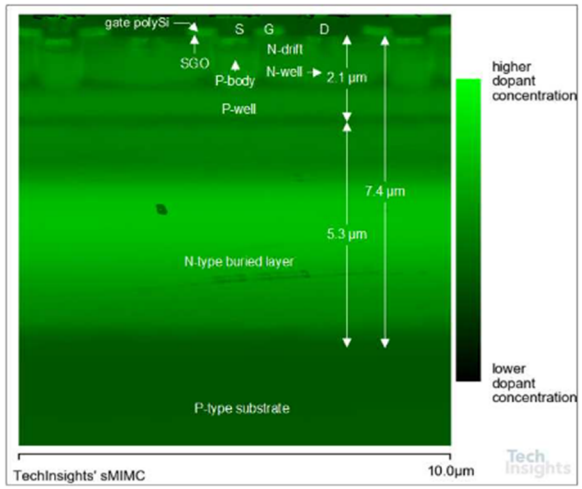
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

42 All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Report at 42.

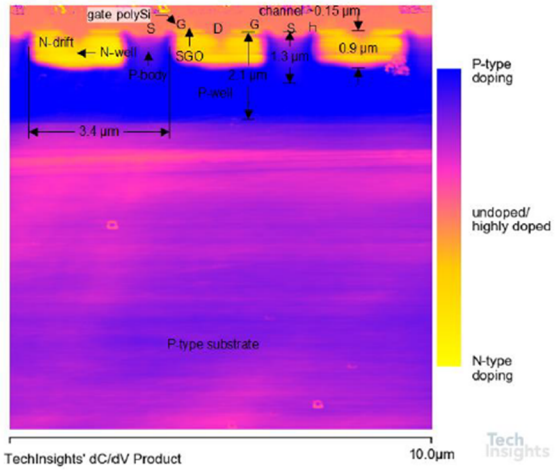
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and

The MPS Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the HSFET and LSFET arrays shown in the images reproduced at Claim 1, Element 2 shows multiple transistors with active regions.

within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Preamble, Elements 2-3 (discussing the HSFET AND LSFET arrays).
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The MPS Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps, which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/SMIM maps taken from MPS Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Zooming in on the sMIM-C image taken from page 43 of the Tech Insights report clearly shows vertical dopant grading in the active regions surounding the source, gate, and drain. The image of the LSFET array (reproduced below) also shows grading near the source and drain and in wells.

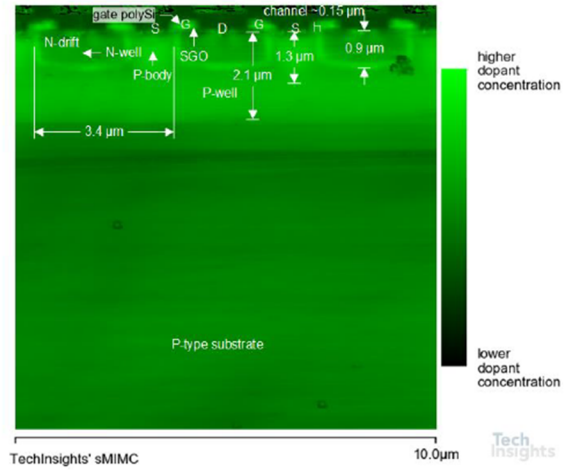
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

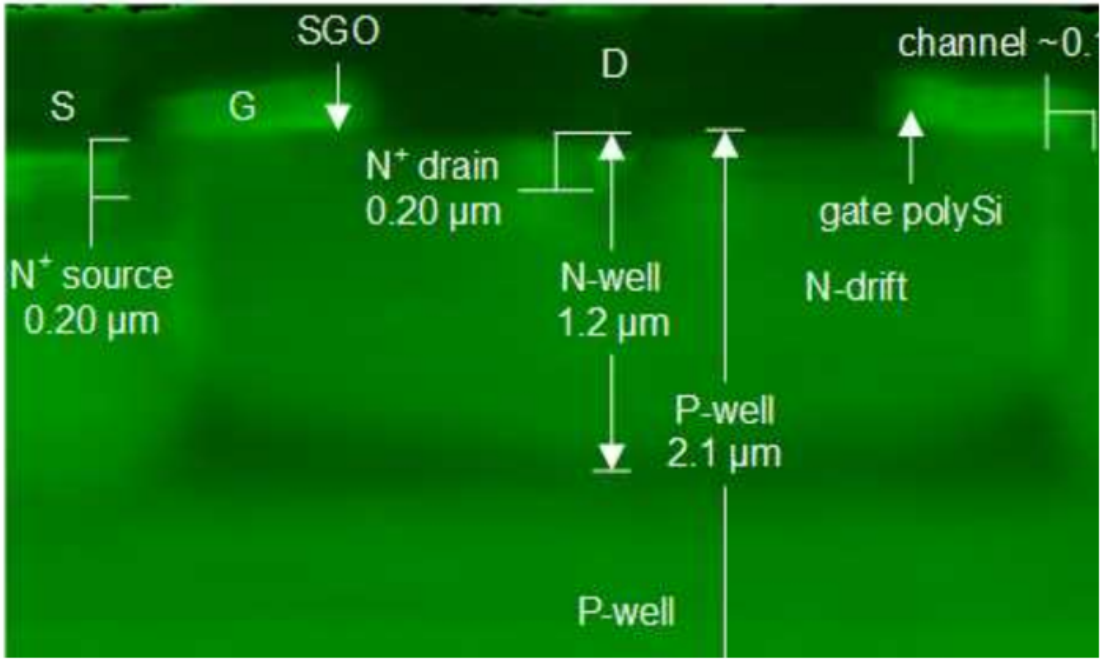
LSFET Array – sMIM-C Cross-Section A-A

2

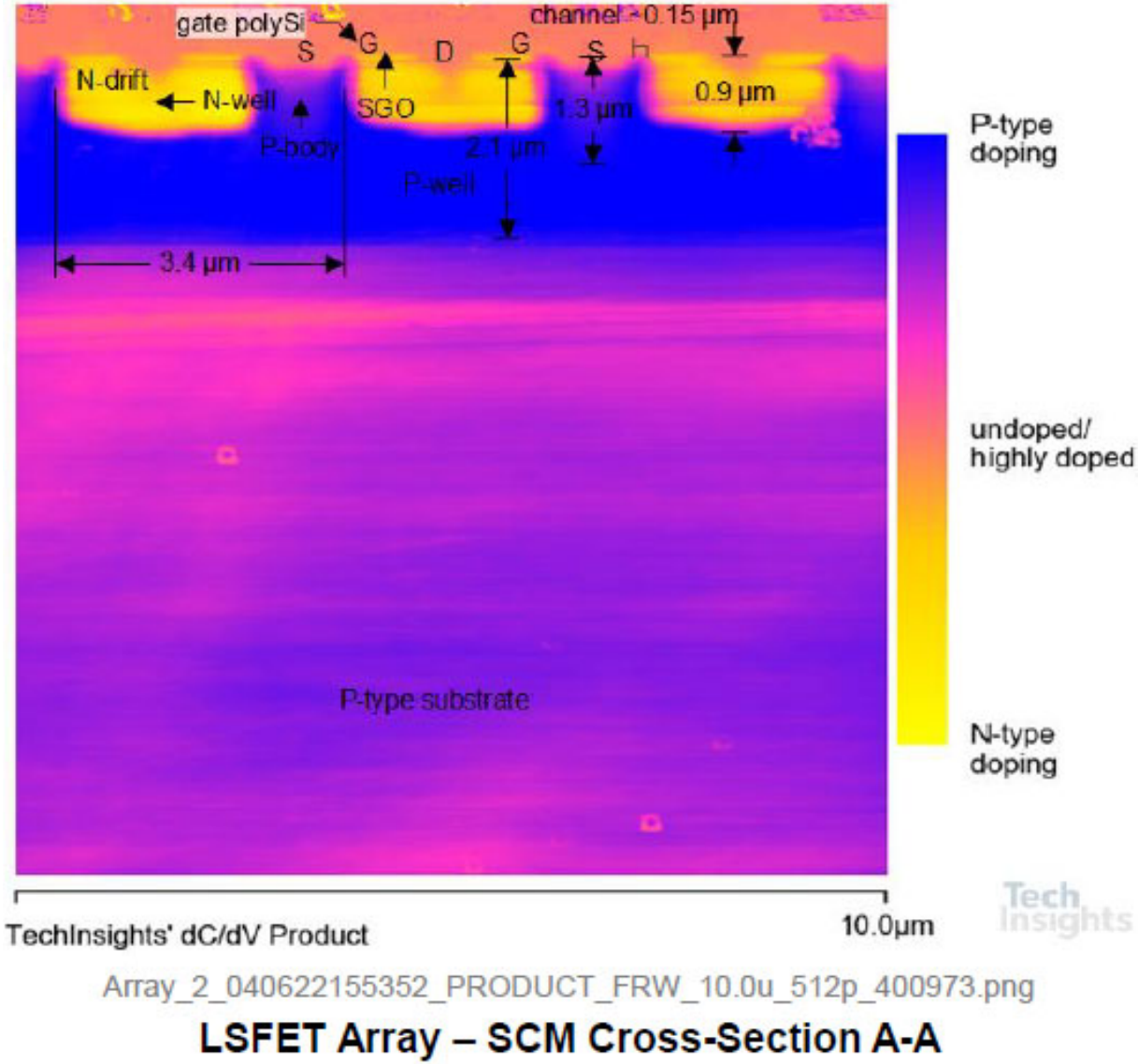
All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Supplemental Report at 2.

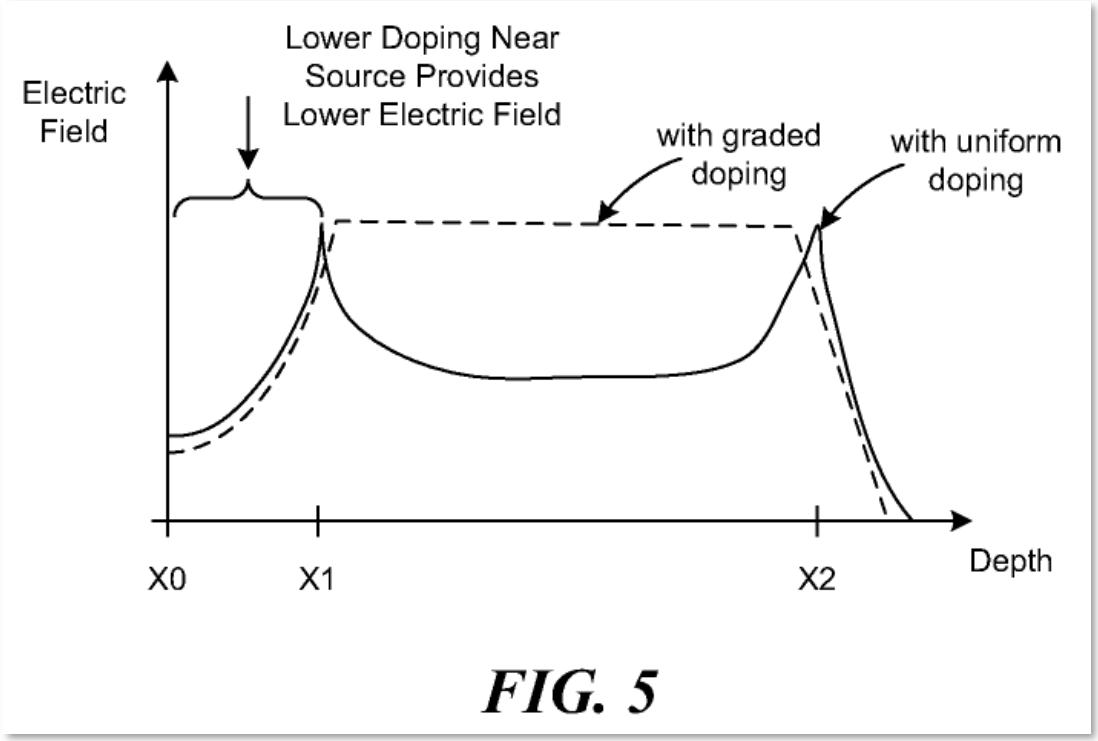
(Zoomed in near active regions on image from page 43)



MP86905 Report at 43.



MP86905 Report at 43.

	Additionally, MPS' annual report states that it seeks patent protection based on its product designs designs: "In general, we have elected to pursue patent protection for aspects of our circuit and device designs that we believe are patentable." *See* MPS "2021 ANNUAL REPORT ON FORM 10-K" at 4. Therefore, the purported inventions described in MPS's patents are an indication of how its products operate. The descriptions of MPS's purported inventions in its patent applications confirm that its products meet this limitation. For example, Figure 5 of MPS U.S. Patent No. 8,704,292 (below) clearly shows the use of graded dopants in active and well regions for the purposes of creating electric fields to aid carrier movement. The patent recites that "The dashed line in FIG.5 shows a uniform electric field distribution associated with an example drift region doping profile."  *FIG. 5*
2. The semiconductor device of claim 1, wherein the substrate is a	Upon information and belief, the substrate of the semiconductor device of the MPS Accused Products is a p-type substance, as discussed above and shown in SCM/sMIM analysis above.

p-type substrate.	
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	Upon information and belief, the substrate of the MPS Accused Products has epitaxial silicon on top of a nonepitaxial substrate. For example, the device summary shown below includes an upper epitaxy layer. **Device Summary** ▪ This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2]. ▪ The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe. ▪ The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region. ▪ One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer. ▪ The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3]. ▪ The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total. ▪ In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions. rary 5 All content © 2022 TechInsights Inc. All rights reserved. Insights Inc **Manufacturer**: Monolithic Power Systems **Part number**: MP86905 **Foundry**: Unknown **Type**: PMIC **Date code**: H39 (week 39 of 2017) **Package type**: 23-pin FC-QFN **Package markings**: MPSH39 / M86905 / 54U403 **Package dimensions**: 3.97 mm × 3.97 mm × 0.88 mm (thick) **Die markings**: MP9502 2013 / <MPS logo> **Die size (whole die)**: 3.38 mm × 3.14 mm (10.61 mm²) **Die size (edge seal)**: 3.36 mm × 3.12 mm (10.48 mm²) **Minimum measured transistor gate length/pitch**: 0.40 µm/0.86 µm **Process generation**: Likely 0.18 µm process generation with relaxed feature dimensions **Feature measured to determine process generation**: Contacted gate pitch, use of CoSi contacts, STI isolation **Maximum voltage [2]**: 18 V Tech Insights
5. The semiconductor device of claim 1, wherein the first active	The MPS Accused Products meet this limitation. *See* above at Claim 2.

region and second active region contain one of either p-channel and n-channel devices.	
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The MPS Accused Products meet this limitation. As shown above, the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. *See* Tech Insights Report images reproduced above at Claim 1, Element 2.
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have graded dopants. *See* Tech Insights Report images reproduced above at Claim 1, Element 2 annotating "n-wells."

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the MPS's Accused Products. MPS's recent patent applications reference forming N regions and P regions by ion implantation. Information about the fabrication process for the MPS Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	The MPS Accused Products meet this limitation. *See* above at Claim 1, Elements 1-3.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.

which transistors can be formed in the surface thereof;	
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5.

concentration to aid carrier movement from the surface to the substrate.	
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and second active region contain	The MPS Accused Products meet this limitation. *See* above at Claim 6.

either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the MPS Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the MPS Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active	The MPS Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.

regions are formed adjacent the first surface of the substrate.	
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The MPS Accused Products meet this limitation. As discussed above for Claim 1, the MPS Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendant and are expected to be obtained through discovery.

U.S. Patent No. 10,734,481	Exemplary Accused Product MPS 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products constitute and are incorporated into semiconductor devices. This chart includes exemplary information regarding a representative example of the MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905"). The 86905 was analyzed in the below referenced report from Tech Insights. MPS MP86905 Intelli-PhaseTM Solution with Integrated HS/LS-FETs and Driver Power Essentials Summary ("MP86905 Report"), *available at* https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2202-801&genealogyCode=MPS-MP9502. The 86905 was also analyzed in a supplemental report from Tech Insights ("MP86905 Supplemental Report"). *See* Exhibit 8 (Supplemental Report for PEF-2202-801). The complete reports are hereby incorporated by reference into each and every claim and claim element discussed. Selected pages are reproduced herein to aid in understanding. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). The claimed invention would have application in numerous types of MPS products, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOFSET drivers, insolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, and current sensors, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. The MPS Accused Products, of which MPS 86905 is one example, are semiconductor devices.

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

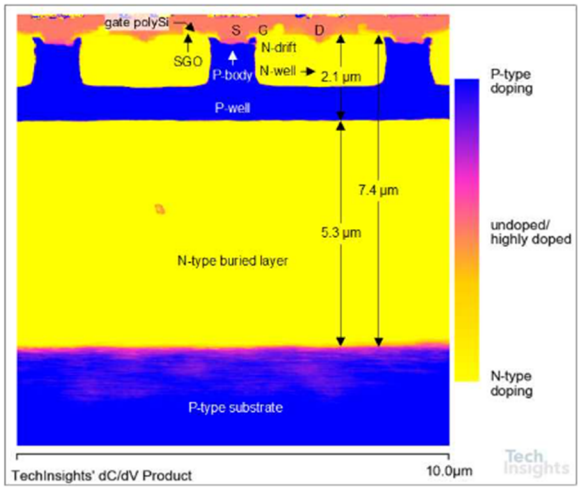
Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm²)
Minimum measured transistor gate length/pitch	0.40 µm/0.86 µm
Process generation	Likely 0.18 µm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Report at 5.

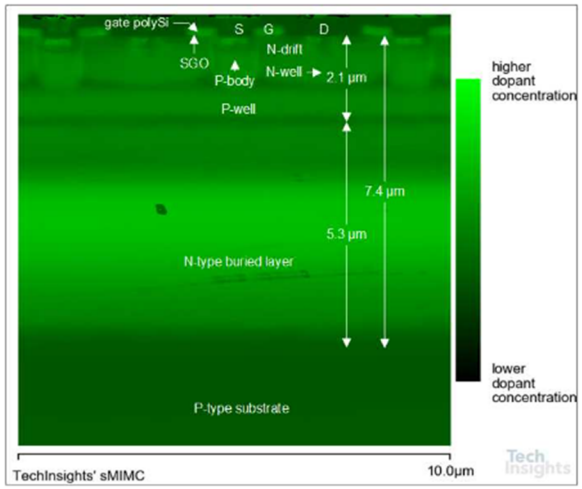
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

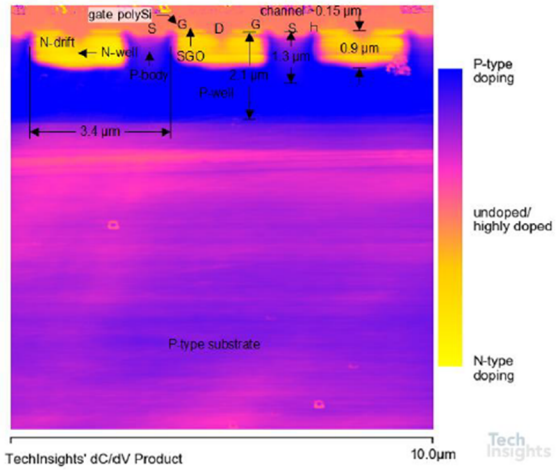
HSFET Array – sMIM-C Cross-Section A-A

All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Report at 42.

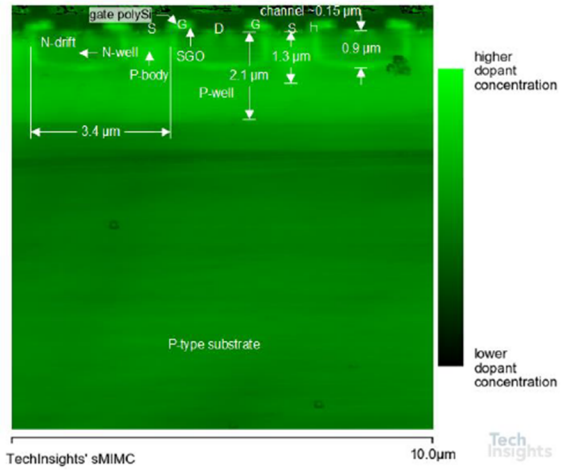
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

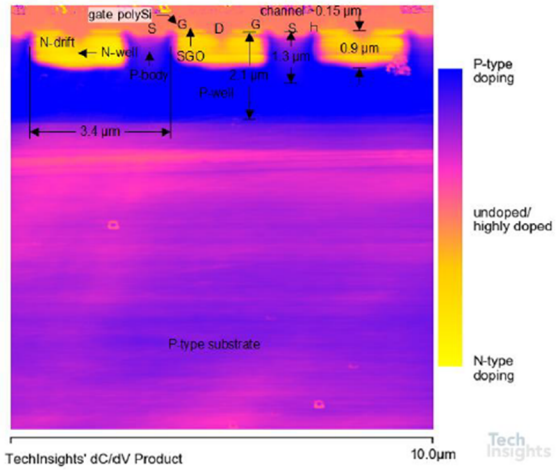
All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Supplemental Report at 2.

	Statement of Measurement Uncertainty and Scope Variation **Statement of Measurement Uncertainty** TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI). Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used. TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the micrometer's 100 µm pitch lines. Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width. TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers. The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration. Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request. **Statement of Scope Variation** Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports. 3 All content © 2022 TechInsights Inc. All rights reserved. TechInsights MP86905 Supplemental Report at 3.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary MPS Accused Product (the MPS 86905 discussed above) reveals the presence of such a substrate. For example, the MPS 86905 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

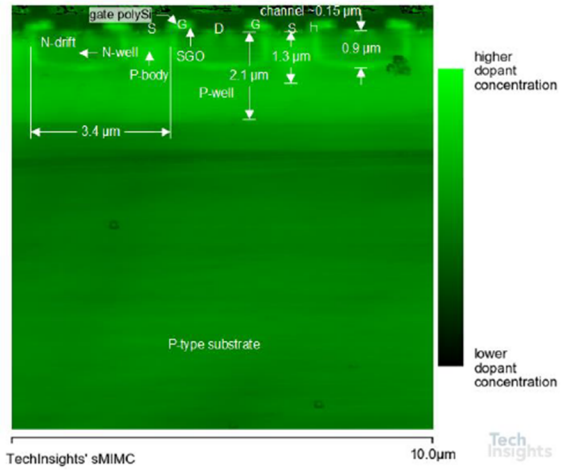
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



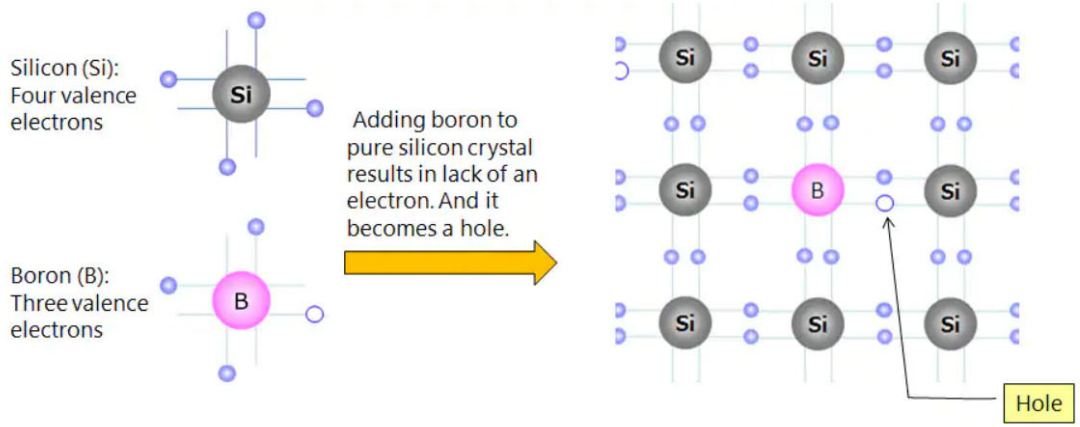
Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

2

All content © 2022 TechInsights Inc. All rights reserved.

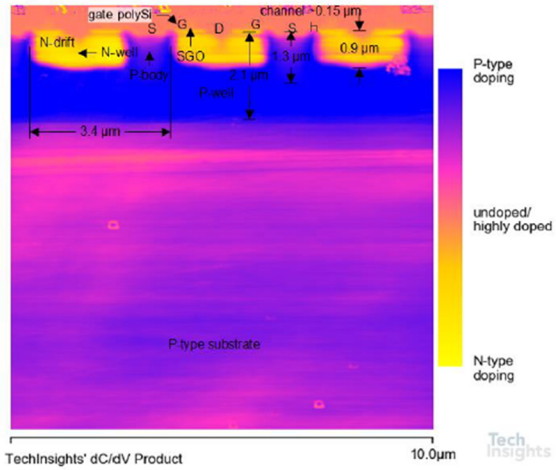
MP86905 Supplemental Report at 2.

	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within	The MPS Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary MPS 86905 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. *See* below showing "HSFET Array," and toward the top the source ("S"), gate ("g") and drain ("drain") where the transistors are, underneath each of the annotations are active regions. *See also* below showing "LSFET Array."

which transistors can be formed;

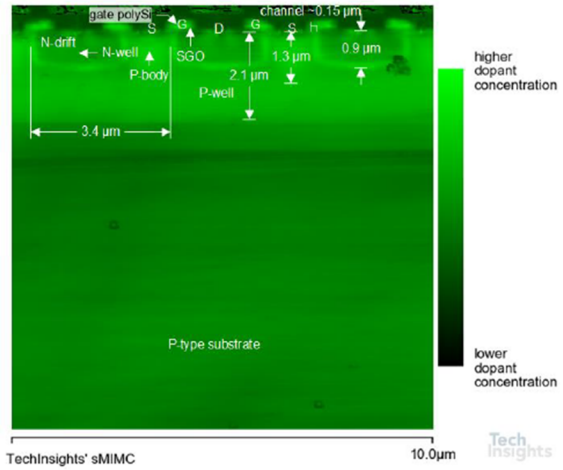
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

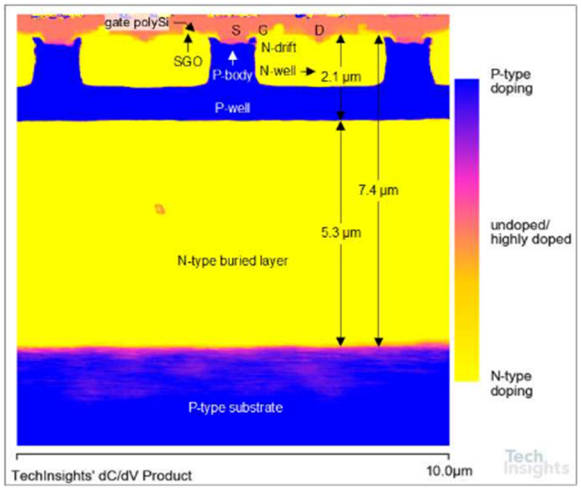
2

All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Supplemental Report at 2.

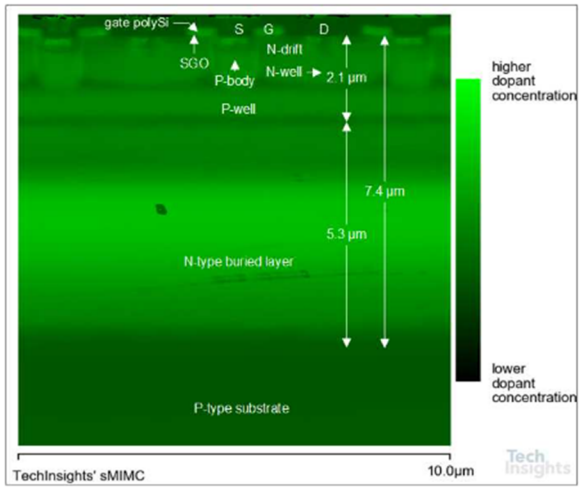
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 µm from the front surface, while the NBL measures ~5.3 µm thick and reaches ~7.4 µm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

ibrary
42 All content © 2022 TechInsights Inc. All rights reserved.
Tech Insights

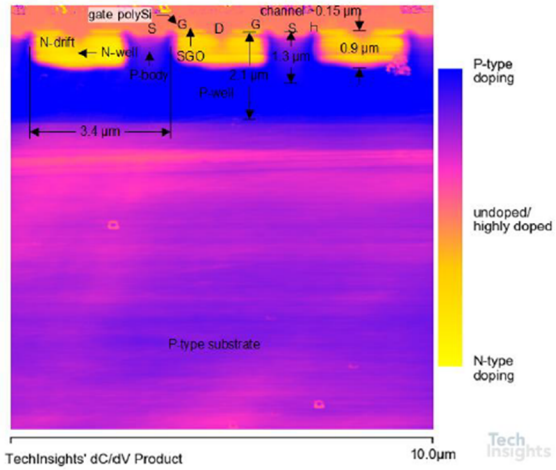
MP86905 Report at 42.

[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the	The MPS Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the HSFET and LSFET arrays shown in the images reproduced at Claim 1, Element 2 shows multiple transistors with active regions.

first active region and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at Preamble, Elements 2-3 (discussing the HSFET AND LSFET arrays).
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The MPS Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps, which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/SMIM maps taken from MPS Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Zooming in on the sMIM-C image taken from page 43 of the Tech Insights report clearly shows vertical dopant grading in the active regions surounding the source, gate, and drain. The image of the LSFET array (reproduced below) also shows grading near the source and drain and in wells.

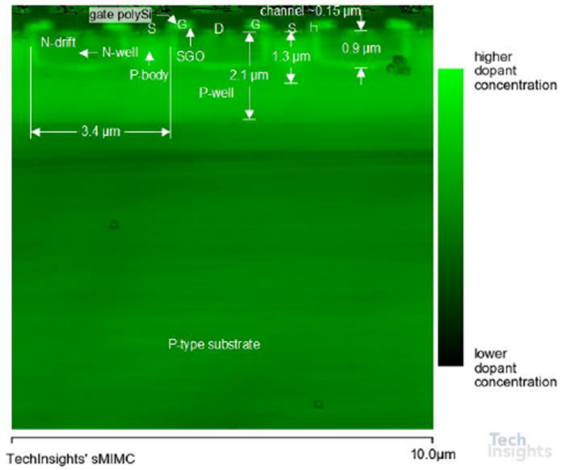
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is ~2.1 µm deep, the P-body is ~1.3 µm deep, while the drain N-drift/N-well is ~0.9 µm deep, shallower than 1.2 µm observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be ~0.15 µm in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

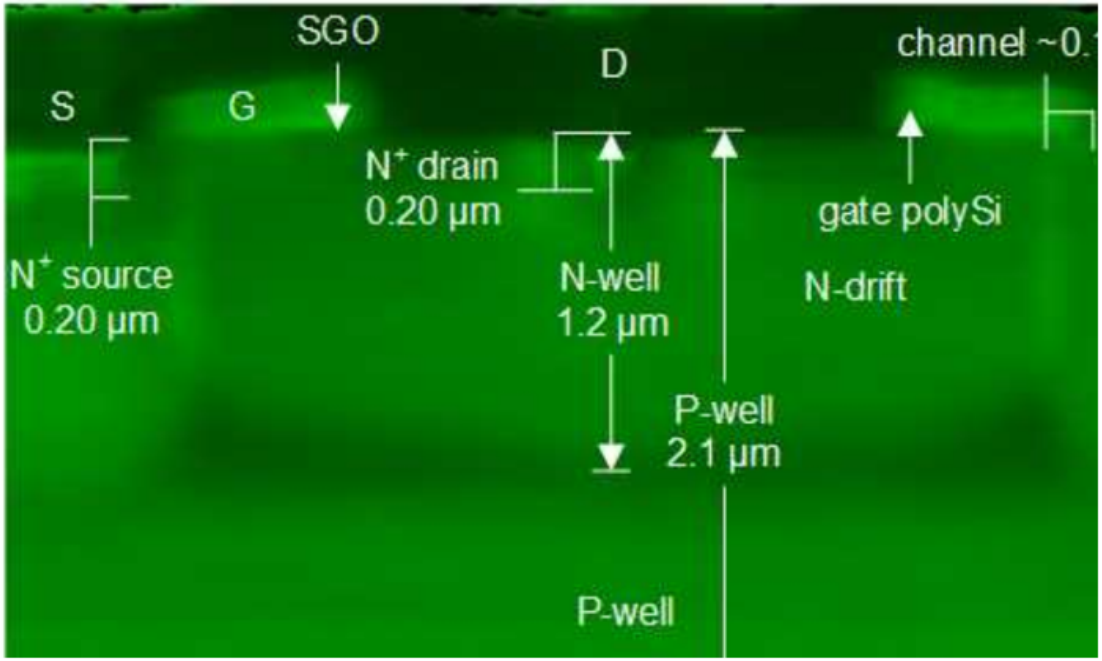
LSFET Array – sMIM-C Cross-Section A-A

2

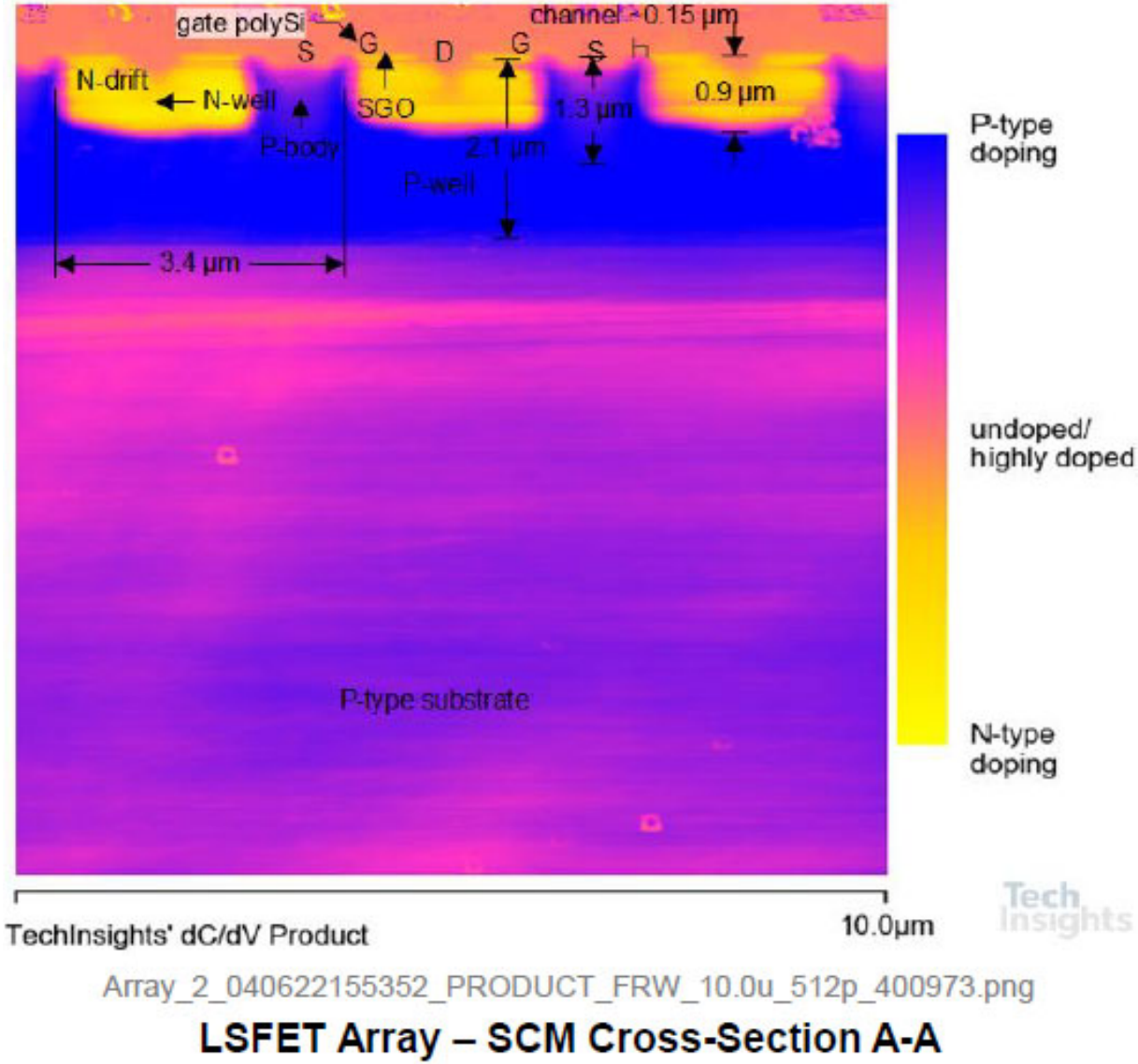
All content © 2022 TechInsights Inc. All rights reserved.

MP86905 Supplemental Report at 2.

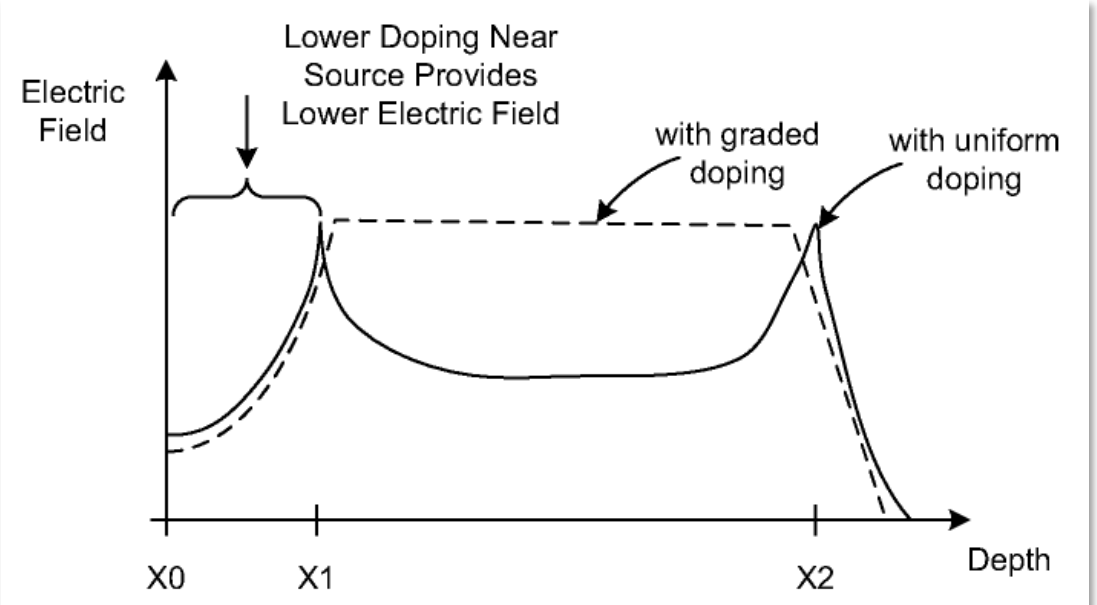
(Zoomed in near active regions on image from page 43)



MP86905 Report at 43.

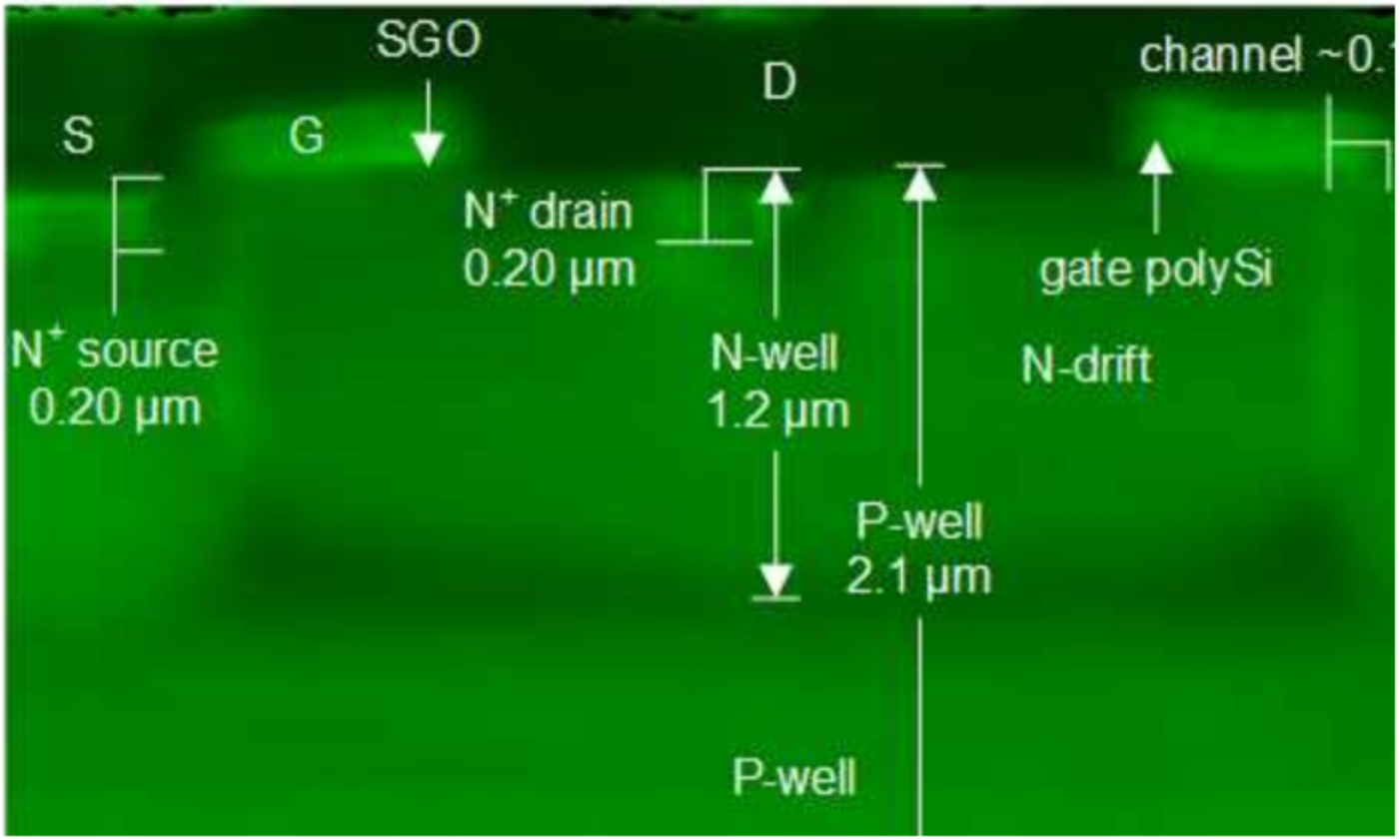


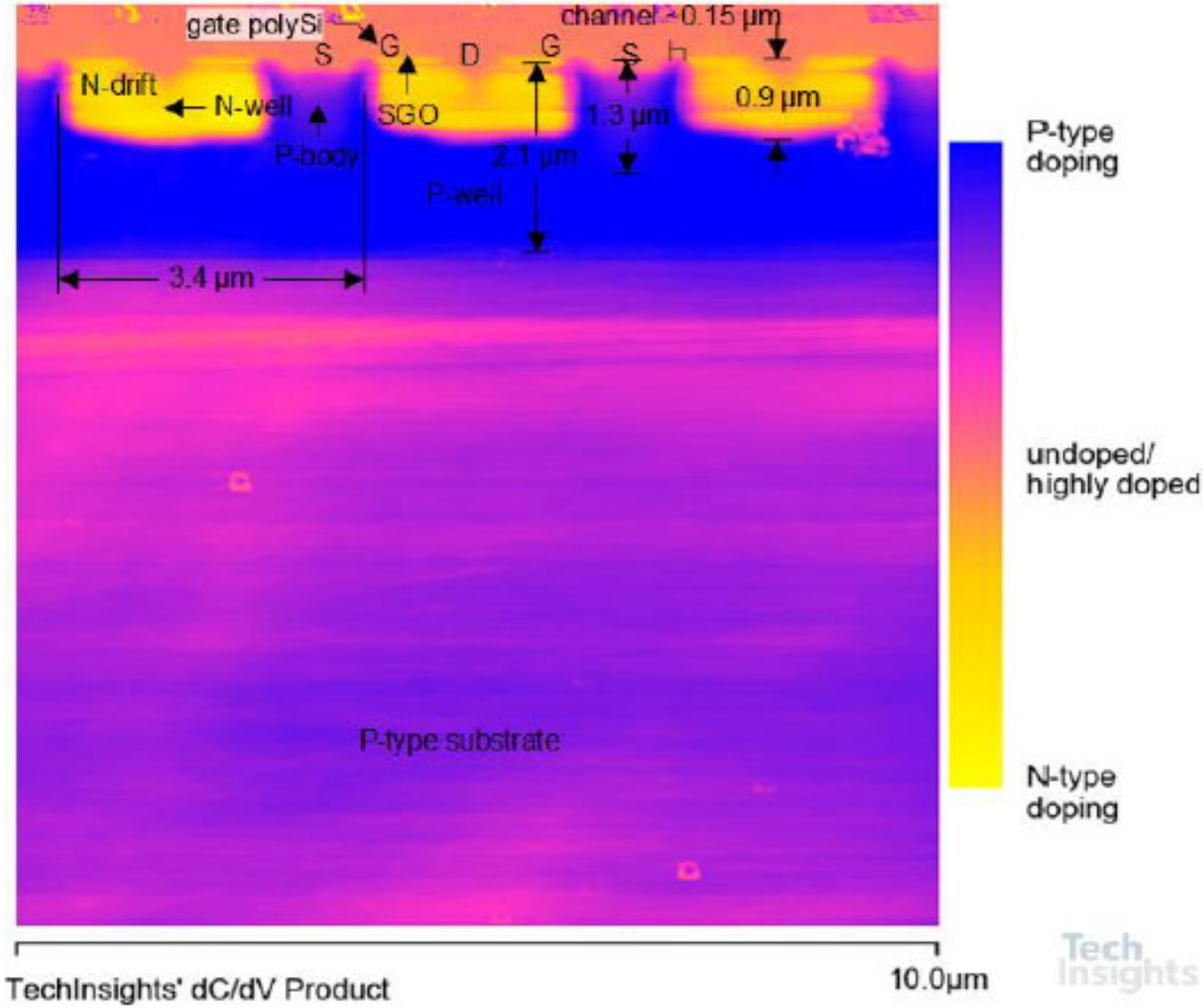
MP86905 Report at 43.

	Additionally, MPS' annual report states that it seeks patent protection based on its product designs designs: "In general, we have elected to pursue patent protection for aspects of our circuit and device designs that we believe are patentable." *See* MPS "2021 ANNUAL REPORT ON FORM 10-K" at 4. Therefore, the purported inventions described in MPS's patents are an indication of how its products operate. The descriptions of MPS's purported inventions in its patent applications confirm that its products meet this limitation. For example, Figure 5 of MPS U.S. Patent No. 8,704,292 (below) clearly shows the use of graded dopants in active and well regions for the purposes of creating electric fields to aid carrier movement. The patent recites that "The dashed line in FIG.5 shows a uniform electric field distribution associated with an example drift region doping profile."  *FIG. 5*
[Claim 1, Element 6] at	The MPS Accused Products include a semiconductor device comprising at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. The images of

least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	the HSFET and LESFET arrays reproduced below (and above) clearly show dopant grading in the well regions. Likewise, Figure 5 from MPS's '292 patent shows grading in a well region.

(Zoomed in near active regions on image from page 43)

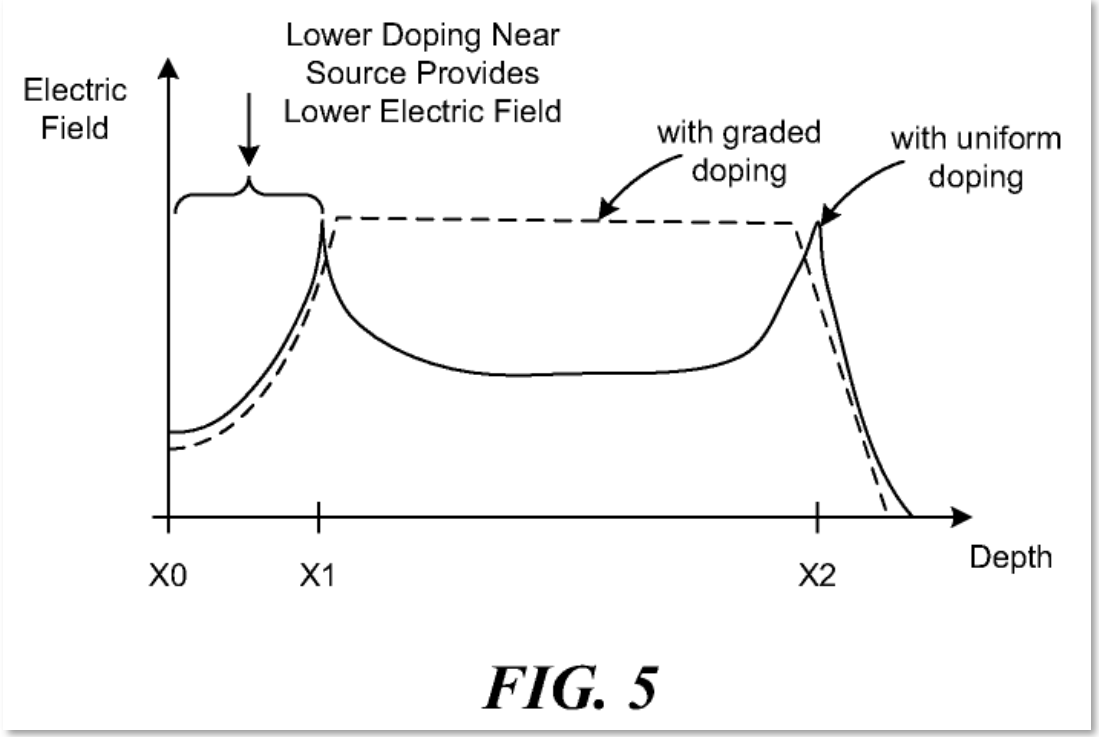




Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

Page 17

	 *FIG. 5*
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	Upon information and belief, the substrate of the semiconductor device of the MPS Accused Products is a p-type substance, as discussed above and shown in SCM/sMIM analysis above.
3. The semiconductor device of claim 1, wherein the	Upon information and belief, the substrate of the MPS Accused Products has epitaxial silicon on top of a nonepitaxial substrate. For example, the device summary shown below includes an upper epitaxy layer.

substrate has epitaxial silicon on top of a nonepitaxial substrate.

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 µm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 µm drain-to-drain pitch and ~0.66 µm total polysilicon gate length, while the LSFET is arranged with ~3.4 µm drain-to-drain pitch and ~0.60 µm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 µm on a 0.86 µm contacted gate pitch, indicating the use of likely 0.18 µm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm²)
Minimum measured transistor gate length/pitch	0.40 µm/0.86 µm
Process generation	Likely 0.18 µm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

5 All content © 2022 TechInsights Inc. All rights reserved.

Tech Insights

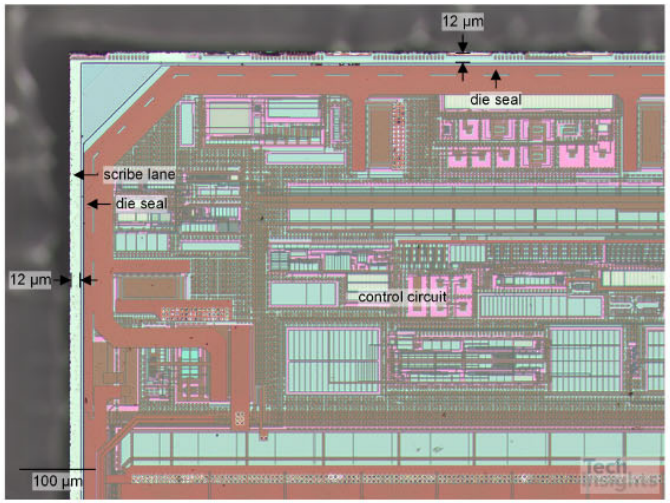
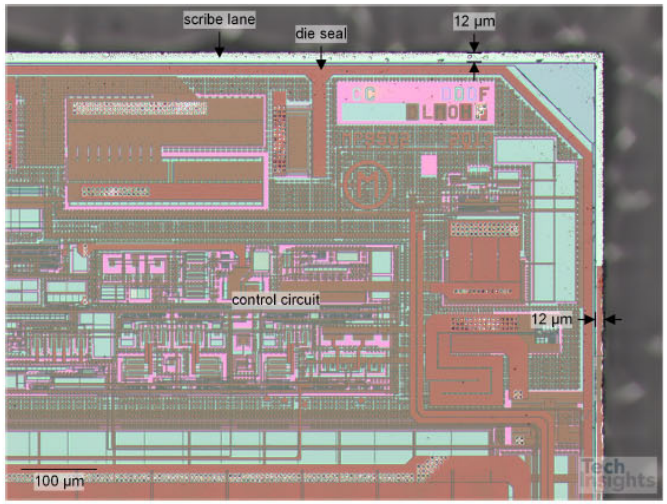
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel

The MPS Accused Products meet this limitation. *See* above at Claim 2.

and n-channel devices.	
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The MPS Accused Products meet this limitation. As shown above, the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. *See* Tech Insights Report images reproduced above at Claim 1, Element 2.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have graded dopants. *See* Tech Insights Report images reproduced above at Claim 1, Element 2 annotating "n-wells."
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the MPS's Accused Products. MPS's recent patent applications reference forming N regions and P regions by ion implantation. Information about the fabrication process for the MPS Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.

8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The MPS Accused Products meet this limitation. *See* above at Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. As shown by the images obtained by SPM/sMIM anlysis (*see* above at Claim 1, Element 5), the MPS Accused Products show blocks of highly n-doped and p-doped wells.
13.The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. As discussed above for Claim 1, the MPS Accused Products include first and second active regions. Upon information and belief, CMOS transistors are formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendant and are expected to be obtained through discovery.

15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* above at Claim 3 (regarding epitaxy) and Claim 13 (regarding CMOS).
17. The semiconductor device of claim 1, wherein the device is a logic device.	Upon information and belief, the MPS's Accused Products comprise a logic device. For example, the image below displays a "control circuit" region.

	MP9502 Die Upper Corners ▪ The scribe lane measures ~12 µm wide all around the die. ▪ The control circuit is at the top portion of the die.  M86908_MP9502_345783_DieCornerA.png  M86908_MP9502_345783_DieCornerB.png 12 All content © 2022 TechInsights Inc. All rights reserved. Tech Insights
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1.

at a first doping level having first and second surfaces;	
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 20, Element 4] transistors formed in at least	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 4.

one of the first active region or second active region;	
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The MPS Accused Products meet this limitation. *See* above at Claim 6.

22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The MPS Accused Products meet this limitation. See above at Claim 1, Element 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. See above at Claim 3.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* above at Claim 4.
25.The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices	The MPS Accused Products meet this limitation. *See* above at Claim 5.

in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* above at Claim 6.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion	The MPS Accused Products meet this limitation. *See* above at Claim 7.

implantation process.	
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The MPS Accused Products meet this limitation. *See* above at Claim 13.
34. The semiconductor device of claim 20, wherein the device is a logic device.	The MPS Accused Products meet this limitation. *See* above at Claim 17.

Exhibit A-3 to Greenthread's Infringement Contentions (U.S. Patent No. 11,121,222))

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a VLSI semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendant and are expected to be obtained through discovery. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5. *See* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the MPS Accused Products are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.

U.S. Patent No. 11,121,222	Accused Products
n−wells or p−wells, respectively, and each well has at least one graded dopant.	
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.
15. The VLSI semiconductor device of claim 1, wherein the	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.

U.S. Patent No. 11,121,222	Accused Products
device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The MPS Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the MPS Accused Products are in the possession of the Defendant and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The MPS Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 3.

U.S. Patent No. 11,121,222	Accused Products
and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. As shown by SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SCM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 5.

U.S. Patent No. 11,121,222	Accused Products
of either p-channel and n-channel devices.	
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 16.

U.S. Patent No. 11,121,222	Accused Products
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to	The MPS Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,121,222	Accused Products
the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,121,222	Accused Products
carrier movement from the first or second active region to at least one substrate area where there is no active region.	
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least	The MPS Accused Products meet this limitation. SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,121,222	Accused Products
one substrate area where there is no active region.	
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a CMOS Semiconductor device. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The MPS Accused Products meet this limitation. *See* above at Claim 21, Element 1.
[Claim 44, Element 2] a substrate;	The MPS Accused Products meet this limitation. *See* above at Claim 44, Element 1.
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* above at Claim 21, Element 5. Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The MPS Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants. Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Infringement Contentions (U.S. Patent No. 8,421,195)

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a CMOS semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-3 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble and Exhibit A-3, Claim 44, Preamble) with transistors, and is a CMOS semiconductor device upon information and belief. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims.
[Claim 1, Element 1] a surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/SMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The MPS Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Infringement Contentions (U.S. Patent No. 9,190,502)

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendant and are expected to be obtained through discovery. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims.
[Claim 7, Element 1] a surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The MPS Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendant and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the MPS Accused Products include an electronic system. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each MPS Accused Product is an electronic system. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The MPS Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 4.
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,316,014	Accused Products
active regions towards an area of the substrate where there are no active regions; and	
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 5.
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 7.

U.S. Patent No. 11,316,014	Accused Products
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 16.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the MPS Accused Products include an electronic system. *See* above at Claim 1, Preamble.

U.S. Patent No. 11,316,014	Accused Products
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error	The MPS Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

U.S. Patent No. 11,316,014	Accused Products
function, or any combination thereof.	
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The MPS Accused Products meet this limitation. *See* Exhibit A-3, Claim 28.