UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MONOLITHIC POWER SYSTEMS, INC.,

Petitioners,

v.

GREENTHREAD, LLC,

Patent Owner.

PTAB Case Nos.: IPR2024-00468 on U.S. Patent No. 8,421,195; IPR2024-00469 on U.S. Patent No. 9,190,502; and IPR2024-00470 on U.S. Patent No. 11,121,222

DECLARATION OF STEPHEN CAMPBELL IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NOS. 8,421,195; 9,190,502; 11,121,222

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I. INTRODUCTION

1. I, Stephen Campbell, have been retained by Petitioner Monolithic Power Systems, Inc. ("Petitioner") to investigate and opine on certain issues relating to United States Patent Nos. 8,421,195; 9,190,502; and 11,121,222 (the "'195 Patent," "'502 Patent," and "'222 Patent," respectively) in its Petitions for *Inter Partes* Reviews. The Petition requests that the Patent Trial and Appeal Board ("PTAB" or "Board") review and cancel claims 1-3 and 5-6 of the '195 Patent, claims 7-8 of the '502 Patent, and claim 44 of the '222 Patent.

2. I have included the analysis of these three patents in a single declaration due to their overlap in claims. I have limited my analysis to the above-identified claims and my lack of analysis with respect to other claims of the '195, '502, and '222 Patents should in no way be interpreted as a concession of their validity. I reserve the right to provide further opinion in other proceedings regarding those claims.

3. The opinions set forth in this declaration are based on my personal knowledge, my professional judgment, and my analysis of the materials and information referenced in this declaration and its exhibits.

4. I am being compensated for consulting services. I am also reimbursed for reasonable and customary expenses associated with my work in this case. I receive no other forms of compensation related to this case. My compensation does

not depend on the outcome of this post-grant review or the co-pending district court litigation, and I have no other financial interest in the post-grant review or the co-pending district court or Petitioner.

5. I understand that the ’195, ’502, and ’222 Patents have been assigned to Greenthread, LLC. I make no opinion on whether this assignment or ownership is correct.

6. This declaration is based on the information currently available to me. To the extent that additional information becomes available, I reserve the right to continue my investigation and study, which may include a review of documents and information that may be produced, as well as testimony from depositions that have not yet been taken.

A. Qualifications

1. Education and Work Experience

7. I received my Bachelor’s degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the

company. This involved a wide variety of process technologies for submicron CMOS.

8. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than $100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200 mm wafers, particle control in CVD systems, and the development of high uniformity wafer cleaning systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as the gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics, micro electromechanical systems (MEMS), and novel materials. The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

9. A brief summary of my work at the University would include:

A. Approximately 200 publications

B. The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.

C. Honors from outside the University such as being named a Presidential Young Investigator by the National Science Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

D. Honors within the University including outstanding service and outstanding teaching.

E. As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new $80M building with a expansive cleanroom facility.

10. Since retiring from the University, I have consulted with semiconductor companies including patent litigation. My work with these companies has been quite successful.

2. Curriculum Vitae

11. A copy of my curriculum vitae is attached as Appendix A to this declaration.

B. Materials Reviewed

12. My opinions expressed in this declaration are based on documents and materials identified in this declaration, including the ’195, ’502, and ’222 Patents, the prior art references and background materials discussed in this declaration, and the other references specifically identified in this declaration. I have considered these materials in their entirety, even if only portions are discussed here.

13. I have also relied on my own experience and expertise in semiconductor fabrication.

C. Level of Ordinary Skill in the Art

14. I am not an attorney and offer no legal opinions. I have been informed about certain aspects of the law for purposes of my analyses and opinions.

15. I understand that in analyzing questions of invalidity and infringement, the perspective of a person having ordinary skill in the art (“POSITA”) is often implicated, and the Court may need assistance in determining that level of skill.

16. I understand that the claims and written description of a patent must be understood from the perspective of a POSITA. I have been informed that the following factors may affect the level of skill of a POSA: (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) the prior-art

solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of active workers in the field. A person of ordinary skill in the art is also a person of ordinary creativity in the art.

17. In my opinion, a POSITA of the subject matter of the ’195, ’502, and ’222 Patents would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for a deficiency in experience, and vice-versa.

D. Summary of Opinions

18. I have reviewed and analyzed the ’195, ’502, and ’222 Patents.

19. Based on my review and analysis, it is my opinion that claims 1-3 and 5-6 of the ’195 Patent, claims 7-8 of the ’502 Patent, and claim 44 of the ’222 Patent are invalid as obvious by: (1) Onoda; (2) Nishizawa; and (3) Kawagoe.

II. OVERVIEW OF THE TECHNOLOGY

A. Priority Date of the Claims

20. I have been informed that a U.S. patent application may claim the benefit of the filing date of an earlier patent application if the earlier patent application disclosed each limitation of the invention claimed in the later-filed U.S. patent application. I have also been informed that priority is determined on a claim-by-claim basis so that certain claims of a patent may be entitled to the priority date

of an earlier-filed patent application even if other claims of the same patent are not entitled to that priority date.

21. I have also been informed that a patented claim is invalid if the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention, or the claimed invention was described in an issued patent or a published patent application that was effectively filed before the effective filing date of the claimed invention.

22. The ’502 and ’222 Patents claim priority to the ’195 Patent, which claims priority to Sept. 3, 2004. All of the ’195, ’502, and ’222 Patent claims claim priority to Sept. 3, 2004.

B. Overview of the ’195, ’502, and ’222 Patents

23. As an initial matter, the independent claims of the ’195, ’502, and ’222 Patents are nearly identical. A table showing the claim language, with highlighted substantive differences, is provided below. Claim 1 of the ’195 and ’502 Patents recite “said” while claim 7 of the ’502 Patent recites “the.”

’195 Patent	**’222 Patent**	**’502 Patent**
Claim 1	**Claim 44**	**Claim 7**
A CMOS Semiconductor device comprising:	A CMOS Semiconductor device comprising:	A semiconductor device comprising:
a surface layer;	a surface layer;	a surface layer;
a substrate;	a substrate;	a substrate;
an active region including a source and a drain,	an active region including a source and a drain,	an active region including a source and a drain,

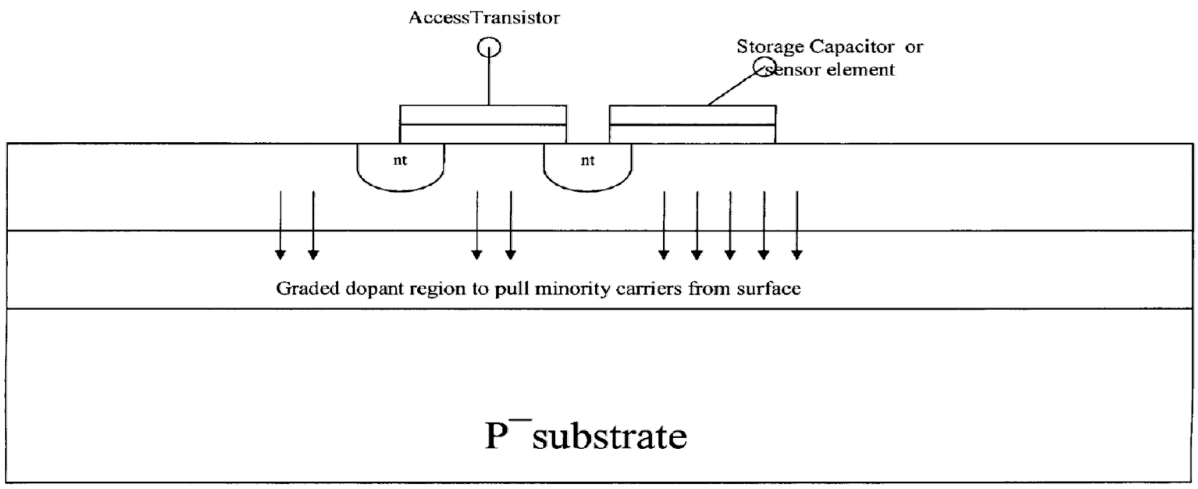
disposed on one surface of said surface layer;	disposed on one surface of the surface layer;	disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate,	a single drift layer disposed between the other surface of the surface layer and the substrate,	a single drift layer disposed between the other surface of said surface layer and said substrate,
said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

24. The ’195, ’502, and ’222 Patents all share a similar specification. The below reference is to the earliest filed application (the ’195 Patent). There are analogous citations to the other patents that describe the same subject matter.

25. The ’195, ’502, and ’222 Patents describe a CMOS semiconductor device that has semiconductor layers that have been doped. (’195 Patent at Abstract & 3:30-33; ’502 Patent at Abstract & 3:38-44; ’222 Patent at Abstract & 3:53-59.) The ’195, ’502, and ’222 Patents state that the doping profile is graded, to enable an electric drift that would sweep minority carriers from semiconductor’s surface to its substrate. (*Id*.)

26. The ’195, ’502, and ’222 Patents acknowledge that graded doping profiles have been used. They state that some prior art bipolar junction transistors employed a graded dopant base to create an “‘aiding drift field’ to enhance the diffusing minority carrier’s speed from emitter to collector.” (’195 Patent at 1:34-36; ’502 Patent at 1:38-40; ’222 Patent at 1:46-48.) The ’195, ’502, and ’222 Patents state that this had deficiencies because “most semiconductor devices … still use a uniformly doped drift epitaxial region in the base.” (’195 Patent at 1:36-40; ’502 Patent at 1:40-44; ’222 Patent at 1:46-53.)

27. The ’195, ’502, and ’222 Patents state that these purported problems of the prior art could be improved by having an epitaxial layer at the surface that has a graded dopant profile. (’195 Patent at 3:30-35; *see also id.* at 4:28-29; 2:51-67; ’502 Patent at 3:38-44 & 2:55-3:17; ’222 Patent at 3:53-59 & 3:4-35.) This would carry minority carriers from the surface to the substrate (indicated by arrows in FIG. 5(b)). (*Id*.)



('195, '502, and '222 Patents at FIG. 5(b).)

28. In my opinion, doping profiles with a gradient (*i.e.*, non-uniform) was well known. It was common in the industry, and widely employed via common techniques. For example, thermally diffusing dopants was a common technique in semiconductor formation, and it provided for a graded dopant profile in the semiconductor layers by the nature of the process. A dopant would be introduced to the surface, and thereafter thermally diffused. There would be a greater concentration at the surface and then a downward gradient where the concentration disperses away from the surface.

29. The '195, '502, and '222 Patents echo the well-matured nature of the field with respect to creating doping profiles. Doping in the art was widely known to be done in order to create various layers where various regions are doped to be N or P type, along with associated drain and source regions, to create PNP or NPN transistors. This is fundamental to forming transistors.

30. It was also well known to use several doping gradients to control electric fields. The ’195, ’502, and ’222 Patents show the doping gradients at the emitter (decreasing as a function of distance) and collector (increasing upward). (’195 Patent at 1:34-36 and FIG. 1; ’502 Patent at 1:38-40 and FIG. 1; ’222 Patent at 1:46-48 and FIG. 1.) In my opinion, the ’195, ’502, and ’222 Patents confirm the well-known nature of various doping profiles by merely listing them by name (*e.g.*, “linear, quasi linear, exponential”). (’195 Patent at 2:40-42; ’502 Patent at 2:44-46; ’222 Patent at 2:60-62.) I consider the first two to have a change in concentration no more than a factor of ten and are usually displayed on a linear-linear plot. The latter has a change in concentration more than a factor of ten and are usually displayed on a log-linear plot. Gaussian and error function curves are examples of exponential profiles.

31. The ’195, ’502, and ’222 Patents also did not provide any new layers to apply those known doping techniques. The layers described are routine and known, and this is confirmed by the ’195, ’502, and ’222 Patents describing various known semiconductor layers when describing the prior art. (’195 Patent at 1:34-36 and FIG. 1; ’502 Patent at 1:38-40 and FIG. 1; ’222 Patent at 1:46-48 and FIG. 1.)

C. Overview of the Technical Concepts

32. My analysis will primarily rely on prior art patents Onoda, Nishizawa, and Kawagoe to show that the ’195, ’502, and ’222 patents are invalid. All three

prior art patents deal with the same technical challenge as the patents being challenged: how to protect electronic circuits from impacts of high energy photons such as x-rays or high energy particles such as alpha particles. When a high-energy collision takes place in a semiconductor, it creates a very large number of negatively charged electrons and positively charged holes. Of particular interest are the minority carriers such as electrons in a p-type region. If enough of these electrons are collected by the circuitry on the surface of the semiconductor, they can introduce faults in the circuit. As will be discussed, these charged species move in response to an electric field, and so an electric field that is properly constructed will push the minority carriers away from the surface, making their collection much less probable. I will also point out that an electric field caused by a doping profile can improve the performance of photosensing devices (Patents from Jastrzebski and from Kamins) by drifting minority carriers into the substrate.

33. Onoda, Nishizawa, and Kawagoe cite latch-up and/or soft errors to motivate the need for the innovation. Soft errors occur when the circuitry collects enough of the minority carriers to change the voltage of that part of the circuit. Thus, a logical "1" becomes a logical "0", or vice versa. It is a soft error in the sense that the circuitry is not damaged, only the stored information is corrupted. Latch-up, on the other hand, can be destructive. The basic element of a CMOS circuit is the inverter consisting of one NMOS transistor and one PMOS transistor. In addition to

the two MOSFETs, parasitic bipolar transistors are automatically formed in the active region of the devices. These bipolar transistors are also inevitably connected so as to create a latch. Once triggered, the latch remains in the state it enters until the circuit forces a change or until the circuit is powered down. In this case the minority carriers collected by part of the circuitry provide the trigger to start the latch-up process.

34. While the exact faults vary slightly from patent to patent, the source of the faults (the collection of excess minority carriers) and the proposed solution (a static electric field to drift excess minority carriers away from the circuit) are identical.

D. Static Unidirectional Electric Drift Fields

35. The ’195, ’502, and ’222 Patents state that a graded doping concentration sweeps minority carriers to the substrate. (’195 Patent at 3:30-33; ’502 Patent 3:38-44; ’222 Patent at 3:53-59.)

> Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate.

36. In my opinion, Patent Owner represented to the Patent and Trademark Office that a graded dopant concentration creates, as an inherent physical property,

a static unidirectional electric drift field. Patent Owner argued this in the '195 Patent prosecution, and the '502 Patent and '222 Patents claim priority to that application. To argue for written description support in the specification of the '195 Patent, the Patent Owner argued that:

> "[T]he graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carriers into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant."
> ('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 7.)

37. Patent Owner stated that:

> "a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way… Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept 'down' … or 'up…'" ('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 6-7.)

38. Patent Owner referenced U.S. Pat. No. 4,481,522 ("Jastrzebski") in support. ('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 7.). Patent Owner stated that:

> "With regard to the existence of a "built-in" electric field created by a graded dopant density, see, e.g., Jastrzebski (US 4,481,522) col. 5, lines 11-13 (cited in Office Action). Applicant respectfully

> submits that this inherent "built-in" unidirectional electric field is the additional parameter for ensuring that all minority carriers are being moved in one direction and which parameter the Office Action deemed to be missing from the disclosure."

(Jastrzebski at FIGS. 1a, 1b.)

39. Jastrzebski confirms this inherent physical property resulting from a graded dopant. It states that a downward-sloping graded-dopant concentration creates an electric drift field that "force[s] most of the charge carriers … deep into the substrate[.]" (Jastrzebski at 5:14-22; *id.* at 2:27-32 ("This is done by creating a field, such as a drift field, in the semiconductor substrate to sweep minority charge carriers…into the bulk [substrate], away from the electrode-bearing surface of the substrate.").).

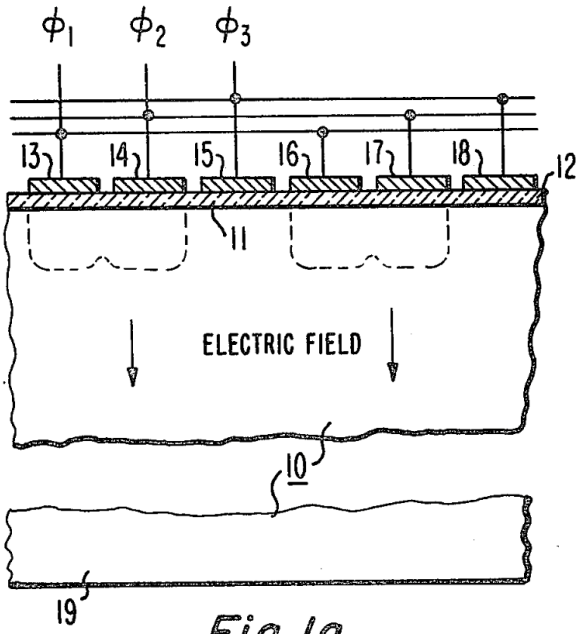


Fig. 1a

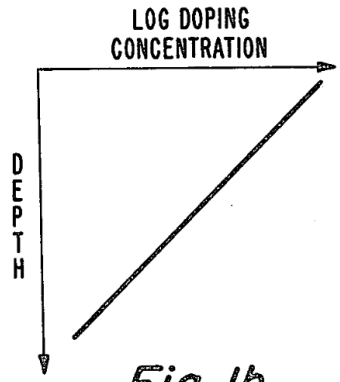


Fig. 1b

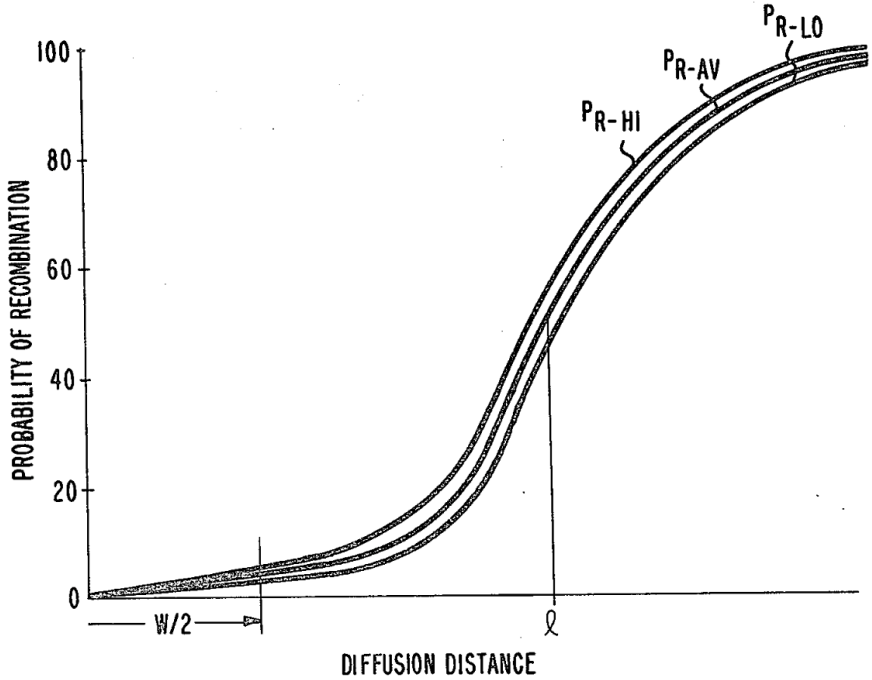


Fig. 2

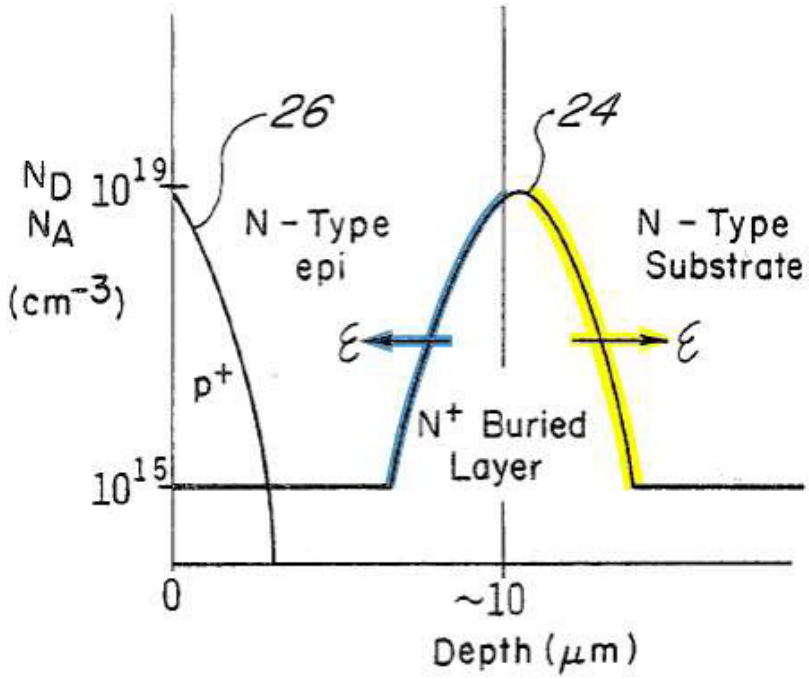
40. Jastrzebski at 5:5-24 discloses:

> These background striation and cross-talk problems are surmounted by constructing CCD shift registers, as exemplified by the FIG. 1a structural segment, in accordance with the present invention, so that there is an electric field normal to the surface 11 that tends to force carriers deeper into the bulk away from the depletion regions induced adjacent to surface 11. This electric field can be a drift field created by a graded concentration of doping in the substrate. In the FIG. 1a structural segment the gradient of doping concentration would be normal, or perpendicular, to the surface 11 of substrate 10, with the doping concentration decreasing with depth from surface 11. The drift field is accordingly directed to force most of the charge carriers generated outside a depletion region deep into the substrate 10 bulk. In these portions of the bulk remote from surface 11 of substrate 10 the charge carriers recombine. Arrangements can also be made to place deep drain structures to dispose of the charge carriers driven into these remote portions of the bulk.

41. Patent Owner made the same representation to the Patent Office regarding U.S. Pat. No. 4,160,985 ("Kamins"). ('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 7.). Patent Owner stated:

> Kamins discloses a photosensing device in which selective doping of a semiconductor substrate of the device produces electric fields in the substrate which accelerate photo generated charge carriers toward or away from the surface of the device. Abstract, Fig. 3.

42. According to Patent Owner, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. (*Id.* at 237, 253 (citing Kamins at 3:6-13, FIGS. 2-3).)



(Kamins at FIG. 3.)

43. Patent Owner argued that:

> In particular, Kamins' disclosure further states that "[t]he carriers therefore tend to be accelerated either toward the nearest photosensor or away from the surface. More specifically, carriers created below the maximum dopant concentration are accelerated into the substrate [...], while carriers created above the maximum dopant concentration are accelerated toward the surface [...]." Col. 3, Lines 6-13, Fig. 2 (showing minority carries accelerated into the substrate and the surface layer, depending on the location

of the carriers relative to the maximum dopant concentration within the "buried layer" 21) and Fig. 3 (showing two electrical fields with opposing directions, away from the area of maximum dopant concentration towards both the surface layer and the substrate, respectively).

44. Kamins at 2:64-3:18 teaches that a graded dopant concentration creates electric fields:

> FIG. 3 schematically illustrates profiles of doping concentration vs. depth into substrate 19. Curve 24 represents the N-type dopants, while curve 26 indicates the P+ -type doping for photosensors 11, 13 etc. The non-uniform dopant concentration in the substrate creates electric fields in the substrate, indicated by arrows labeled "ε" in FIGS. 2 and 3. In devices fabricated as described above, the electric field in the substrate is about 460 V/cm near the surface, decreasing to 60 V/cm at 1 μm above the maximum dopant concentration. The carriers therefore tend to be accelerated either toward the nearest photosensor or away from the surface. More specifically, carriers created below the maximum dopant concentration are accelerated into the substrate where they recombine without contributing to the collected current of any sensor, while carriers created above the maximum dopant concentration are accelerated toward the surface where they increase the collected current of the adjacent photosensor. In either case, the probability of a carrier reaching a distant sensor is reduced. The field also leads to more rapid collection of

photogenerated carriers, thus improving the frequency response of the device.

45. FIG. 3 of Kamins depicts these two electric fields that are inherently created by a graded dopant concentration.

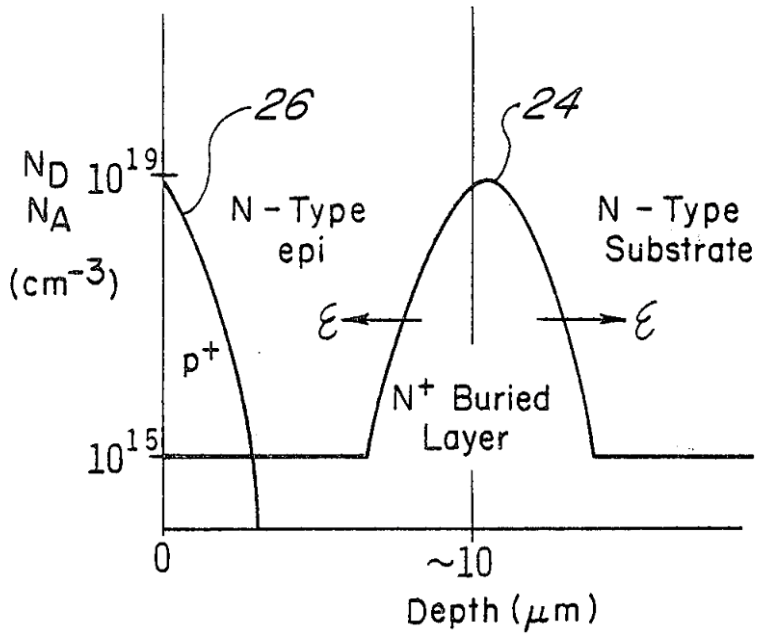


Figure 3

46. Kamins depicts the minority carriers in FIG. 2, stating that it provides "built-in electric fields into the structure so that a directional drift motion is superposed on the random thermal diffusion of the charge carriers." (Kamins at 2:32-36.)

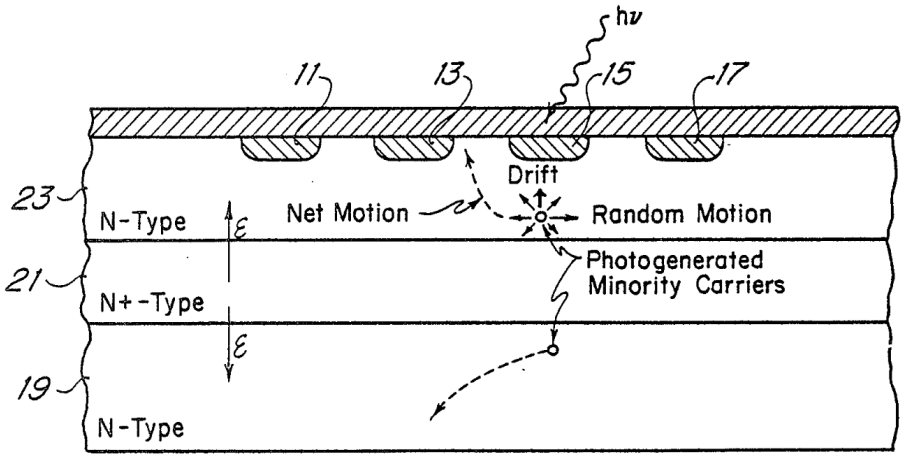


Figure 2

47. Patent Owner also described "static" with respect to Kamins and conceded that it "discloses the presence of a 'static' drift field, 'because the drift field is created by graded concentration of dopants which does not change over time.'" Patent Owner stated ('195 Patent App., App. No. 11/622,496, Oct. 15, 2015 Amendment at 6 (citing Office Action ¶ 4 p.4 lines 1-3, further citing to Kamins, Col. 2, lines 15-16; Col. 2, line 64- Col. 3, line 2; Col. 1, lines 38-46; and Col. 3, lines 8-11.).

E. Claim Construction

48. I understand that claim terms generally are construed in accordance with the ordinary and customary meaning they would have to a POSITA at the time of the invention in light of the claim language, the specification, and the prosecution history. I understand that dictionaries and other extrinsic evidence may be

considered as well, though such evidence is typically regarded as less significant than the intrinsic record in determining the meaning of the claim language

49. For all terms of the challenged claims of the ’195, ’502, and ’222 Patents, I have interpreted them as they would have been understood by a POSA at the time of the asserted priority date, i.e., Sept. 3, 2004.

III. UNPATENTABILITY OF THE ’195, ’502, AND ’222 PATENT CLAIMS

A. Standards for Invalidity

1. Obviousness

50. I am informed and understand that a patent cannot be properly granted for subject matter that would have been obvious to a person of ordinary skill in the art at the time of the alleged invention, and that a patent claim directed to such obvious subject matter is invalid under 35 U.S.C. § 103. It is also my understanding that in assessing the obviousness of claimed subject matter, one should evaluate obviousness in light of the prior art from the perspective of a person having ordinary skill in the art at the time the alleged invention was made (and not from the perspective of either a layman or a genius in that art). It is my further understanding that the question of obviousness is to be determined based on:

- The scope and content of the prior art;
- The difference or differences between the subject matter of the claim and the prior art (whereby in assessing the possibility of

obviousness one should consider the manner in which a patentee and/or a Court has construed the scope of a claim);

- The level of ordinary skill in the art at the time of the alleged invention of the subject matter of the claim; and

- Any relevant objective factors (the "secondary indicia") indicating nonobviousness, including evidence of any of the following: commercial success of the products or methods covered by the patent claims; a long-felt need for the alleged invention; failed attempts by others to make the alleged invention; copying of the alleged invention by others in the field; unexpected results achieved by the alleged invention; praise of the alleged invention by the alleged infringer or others in the field; the taking of licenses under the patent by others and the nature of those licenses; expressions of surprise by experts and those skilled in the art at the subject matter of the claim; and whether the patentee proceeded contrary to accepted wisdom of the prior art.

- Any relevant objective factors (the "secondary indicia") indicating obviousness: independent invention of the claimed invention by others before or at about the same time as the named inventor thought of it; and other evidence tending to show obviousness.

51. Further, I understand that when combining references or modifying a reference, rationales that may support a conclusion of obviousness include: (a) combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain

predictable results; (c) use of a known technique to improve similar devices (methods, or products) in the same way; (d) applying a known technique to a known device (method, or products) in the same way; (e) "obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; (f) known work in the field that may prompt variations of it for use in either the same field or different one based on design incentives, or other market forces; (g) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. And when considering these rationales, one should be careful not to engage in hindsight analysis such that the reconstruction of the alleged invention is only based on the knowledge gleaned from the patent disclosure itself. I have not engaged in hindsight analysis as the prior art references disclose the inherent characteristics that are claimed in the patents and discuss the same benefits of those characteristics.

B. '195 Patent

1. Ground I: Onoda Renders Obvious Claims 1, 2, 3, 5, and 6.

a. Independent Claim 1

52. Onoda discloses a CMOS device. FIG. 8 depicts a cross-sectional where the dopant concentration gradually decreases from the surface of the epitaxial layer (tan), through the well region 105a (green) and into the substrate 101 (grey).

FIGS. 2 and 3 further shows examples of CMOS devices based on both NMOS and PMOS transistors. (Onoda at [Abstract], [0041]-[0047], [0052].)

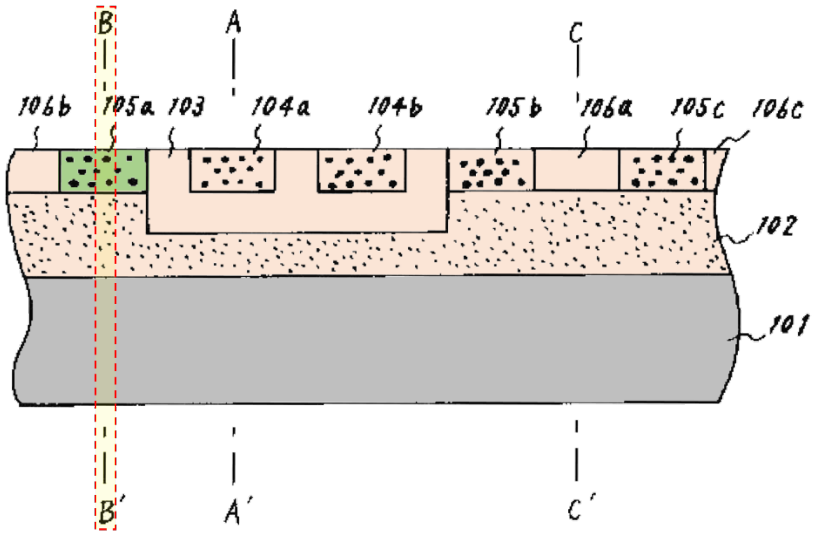
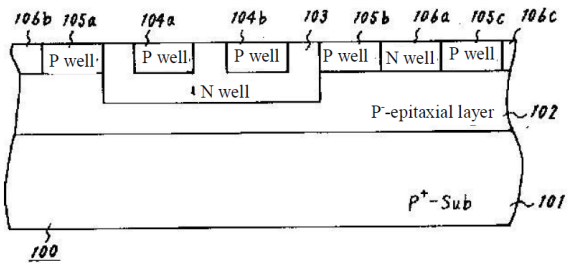
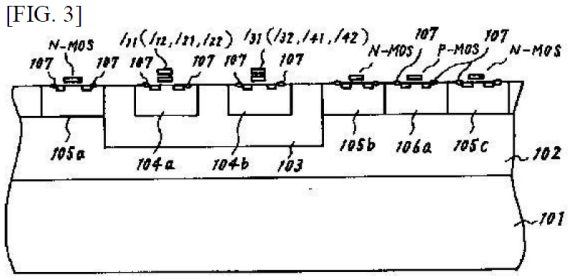


FIG. 8 of Onoda





FIGS. 2 and 3 of Onoda

53. The cross-sectional of B-B' (yellow) is shown below in FIG. 11 with corresponding colors (i.e., the surface of the epitaxial layer (tan), the well region 105a (green), and the substrate 101 (grey)). The X-axis of the figure depicts depth while the Y-axis depicts impurity concentration. As can be seen below, the impurity concentration decreases from the surface to the substrate.

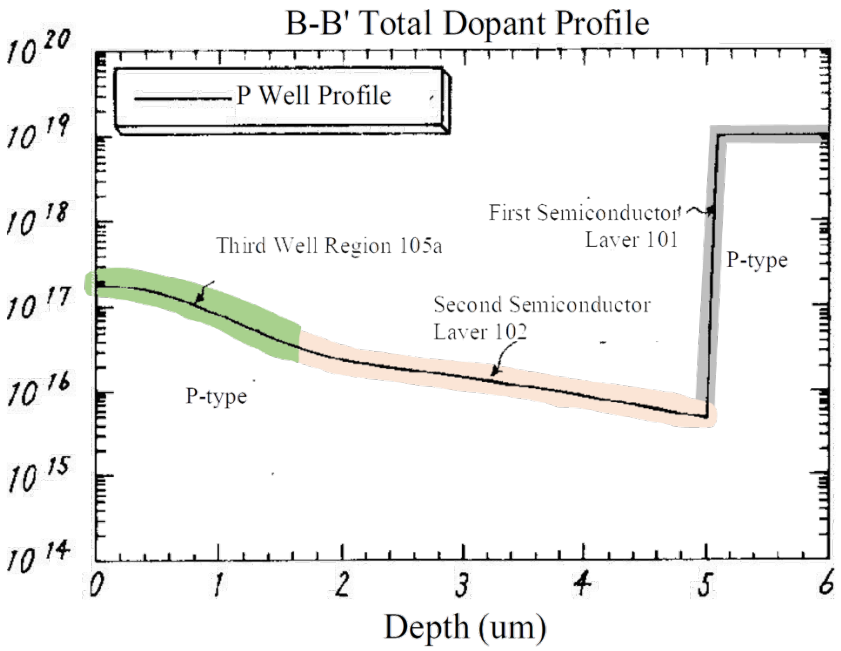


FIG. 11

54. In my opinion, Onoda discloses and/or renders obvious each of the limitations of claims 1, 2, 3, 5, and 6. This is described below.

(i) Preamble: "A CMOS semiconductor device comprising:"

55. Onoda discloses a CMOS semiconductor device. CMOS devices have complimentary pair of NMOS and PMOS transistors. As of the publication of Onoda, and filing of the '195, '502, and '222 Patents, CMOS was the dominant fabrication technology, and it still is. For example, flash devices have been predominantly manufactured with CMOS since the 1980s. In my opinion, a POSITA would have understood that a publication describing NMOS and PMOS transistors to be directed to CMOS for these reasons.

56. Onoda discloses both N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors. (Onoda at FIGS. 2, 3 and 8, [Abstract], [0041]-[0047], [0052], Claim 2.) In my opinion, a POSITA would have understood these teachings to be directed to CMOS circuits. Onoda further mentions that one of the objectives of the invention "is to provide a semiconductor integrated device … with improved resistance to latch-up" (*id.* at [0006]), which a POSITA would have understood to be a problem of CMOS transistors having both NMOS and PMOS transistors as shown in the illustrated circuits in Onoda.

57. In addition, it would have been obvious to employ the teachings of implementing both NMOS and PMOS transistors in the circuits taught by Onoda to CMOS devices. As I have noted above, CMOS was the predominant technology as of the 1980s, and Onoda explicitly describes both NMOS and PMOS transistors on a single device (FIG. 3) which are the ingredients for a CMOS. Applying Onoda's teachings to CMOS would not only have been obvious to do, it would have been expected.

(ii) Element [1.1]: "a surface layer;"

58. Onoda discloses a surface layer that is at the surface of Onoda's semiconductor substrate 101 and is in the region of the NMOS transistor's p-doped well region 105A. The well itself has source and drain regions. (Onoda at [0043] ("105a, 105b, and 105c are P-type [] well regions"); *see also id.* at [0044], Claim 2

("floating gate electrode formed over the second well region, positioned between the source region and the drain region").) As can be seen from the annotated FIG. 1 of Onoda below, Onoda's surface layer is at the surface of semiconductor substrate 100, and the source and drain regions (red) of Onoda's transistors are in that surface layer.

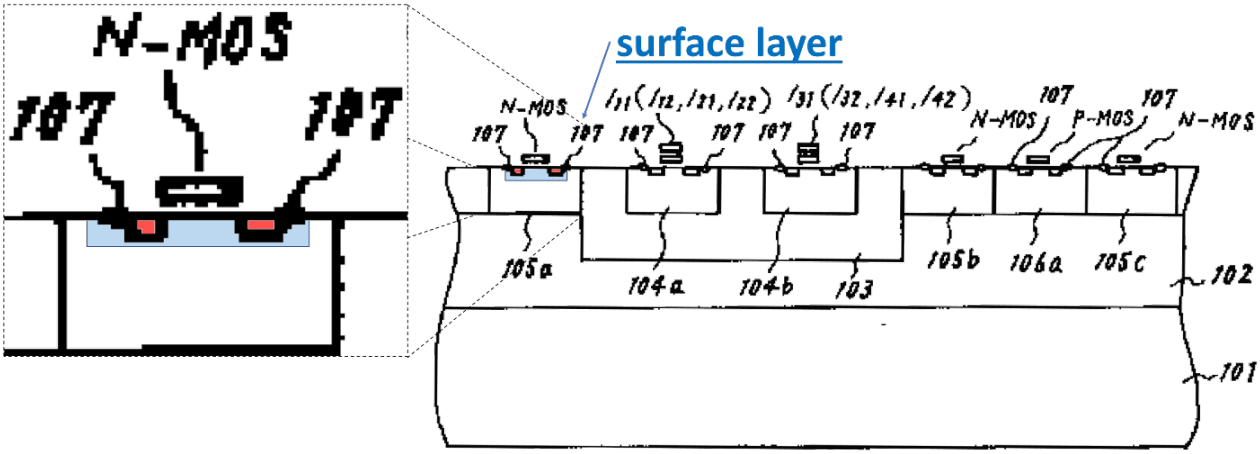
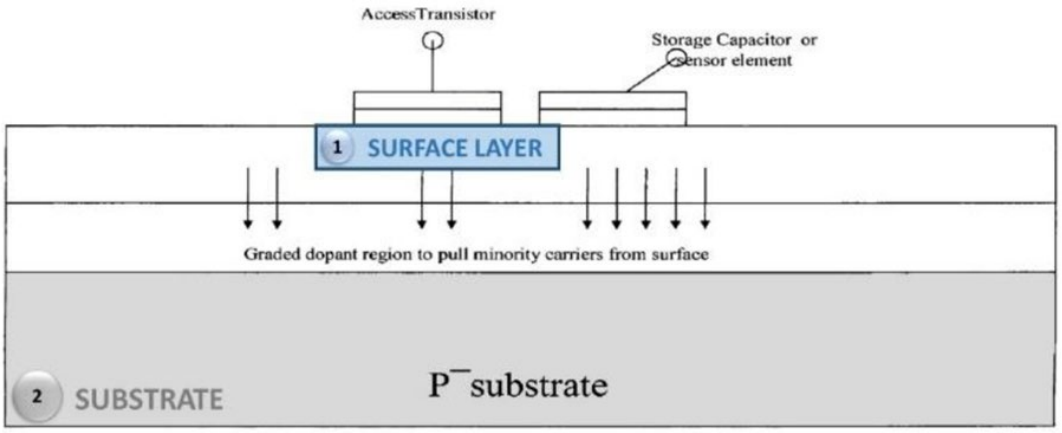


FIG. 3 of Onoda

59. I note that Onoda's teaching of the "surface layer" provides a substantively identical match to how the Patent Owner stated that the '195, '502, and '222 Patents describe it. In court filings, Patent Owner annotated FIG. 5(b) stating that the surface layer is at the device's surface, surrounding the action region. (Patent Owner's Responsive Claim Construction Brief, *Greenthread, LLC v. Intel Corp. et al.*, 6:22-cv-105-ADA ("PO Res. Br.") at 6.)



(iii) Element [1.2]: "a substrate;"

60. Onoda's flash memory has a "a semiconductor substrate 100" in which, after doping, becomes the first substrate layer 101. (Onoda at [0041] ("FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention").) Element 101 in Onoda "is a first semiconductor layer made from a heavily-doped … P-type silicon substrate." (*Id.*; *see also id.* at [0041]; *see also id.* at "Brief Description of the Drawings" describing FIGS. 1 through 14 as describing features of the "first embodiment.") The doped substrate 101 in Onoda is an underlying layer in the devices in Onoda and discloses the claimed substrate.

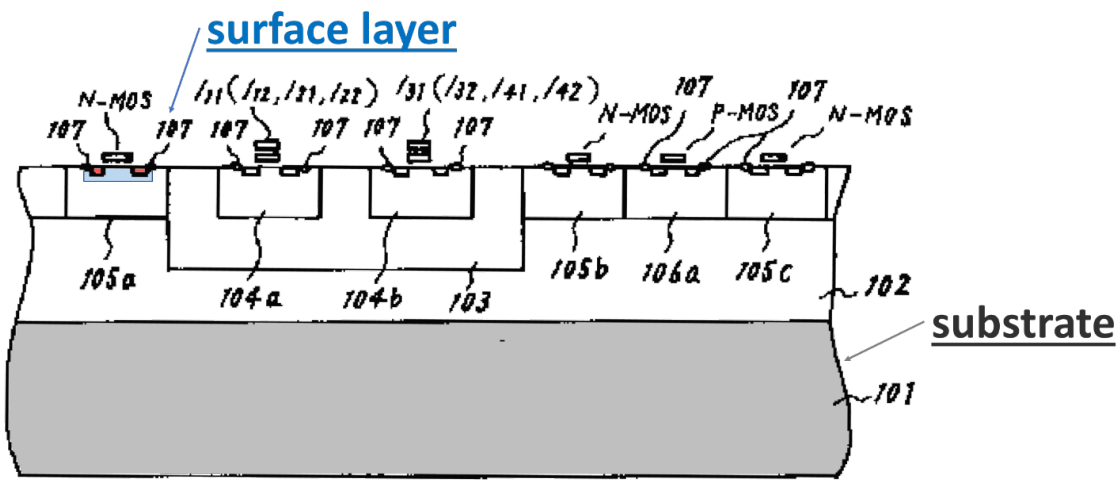
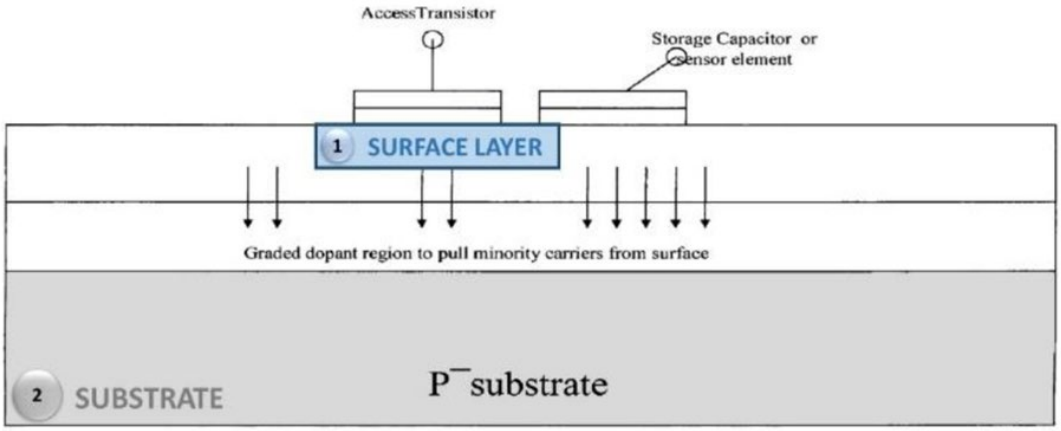


FIG. 3 of Onoda

61. Onoda's teaching of the "substrate" by its doped substrate 101 matches Patent Owner's proposed claim construction in district court, where it stated the term "substrate" should be construed to mean "an underlying layer." (PO Res. Br. at 15.) Patent Owner's annotations to FIG. 5(b) of the '195 Patent are below. (*Id.* at 6.)



(iv) Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

62. Onoda's surface layer includes a region with transistor source and drain regions (red) as illustrated above annotated FIG. 3. This region in the Onoda's surface layer constitutes an active region. (Onoda at [0029] ("each a memory cell having a source region comprising an N-type diffusion layer, a drain region comprising an N-type diffusion layer that is separate from the source region, a floating electrode formed over a channel region that is positioned between the source region and the drain region, with a gate oxide film, comprising a tunnel oxide film, interposed therebetween, and a control gate electrode disposed facing the floating gate electrode with an interlayer insulating films interposed therebetween."), [0043] ("105a, 105b, and 105c are P-type [] well regions"); *see also id.* at [0044], Claim 2 ("floating gate electrode formed over the second well region, positioned between the source region and the drain region").) As shown below, the active region is disposed to the top of the surface layer, *i.e.*, the claimed "one surface on said surface layer." See also *id*. at [0053]-[0055]. In Patent Owner's responsive claim construction brief, Patent Owner also likened this to a room, stating:

> By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the ceiling fan is spinning around like a propeller on the roof of the house. Instead, it means

that the ceiling fan is hanging from the ceiling ***inside*** the room. The same is true about the active region and the surface layer.

PO Res. Br. at 11.

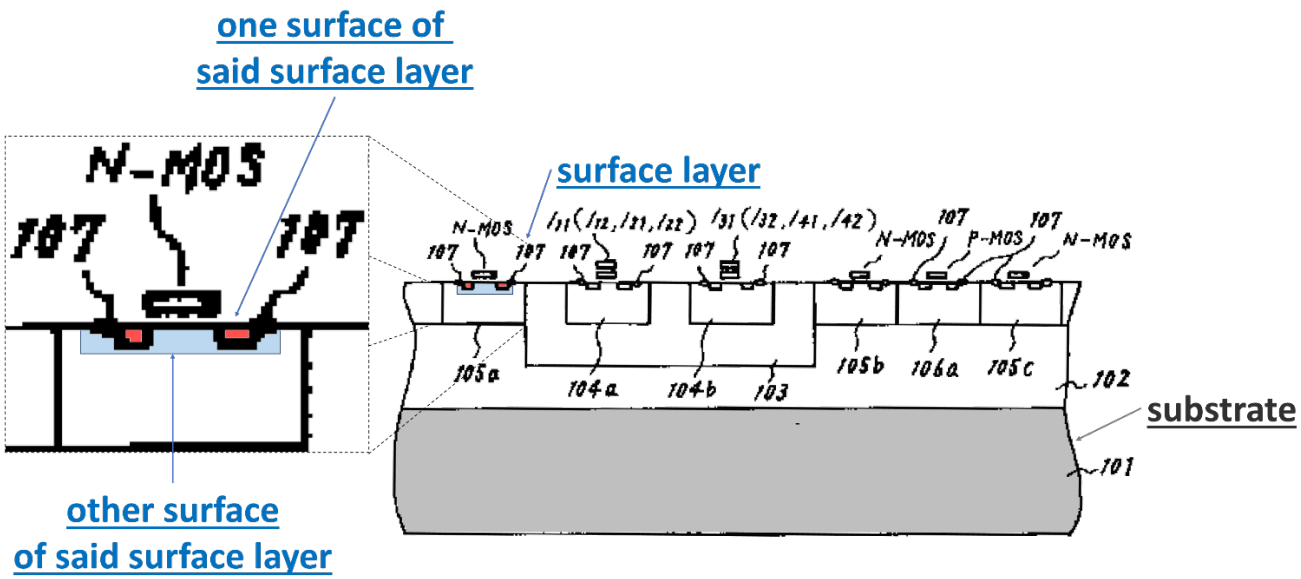
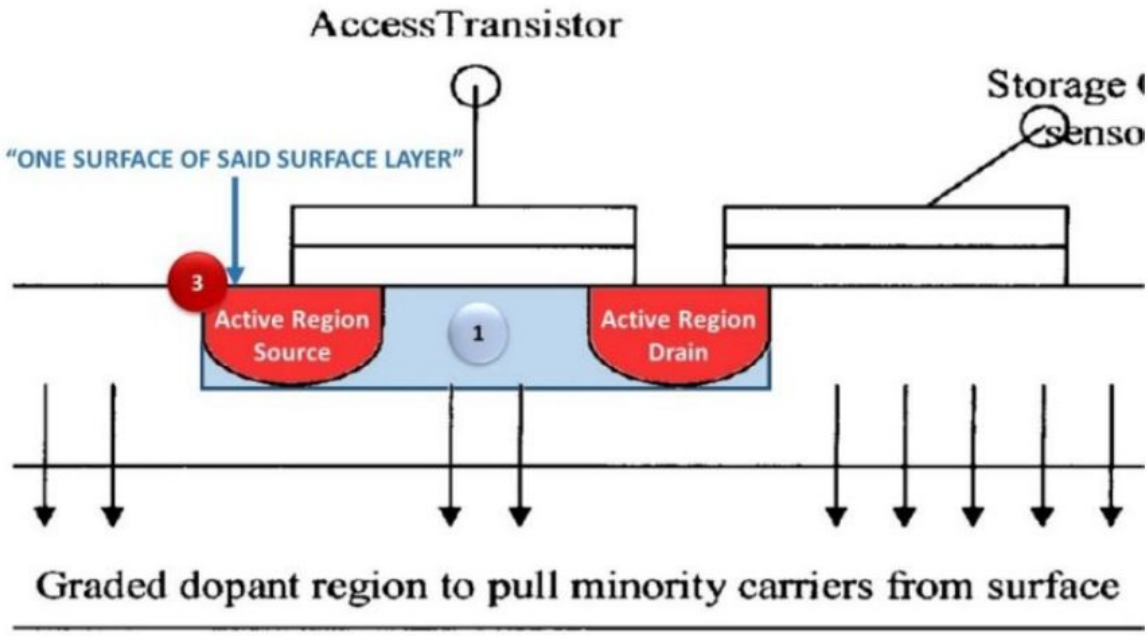
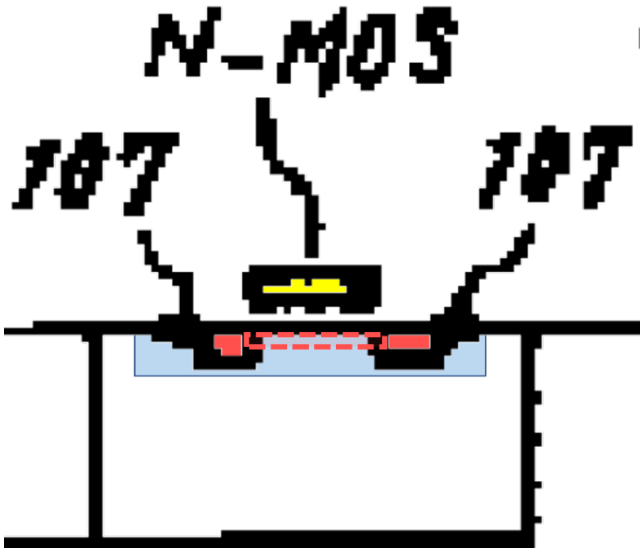


FIG. 3 of Onoda

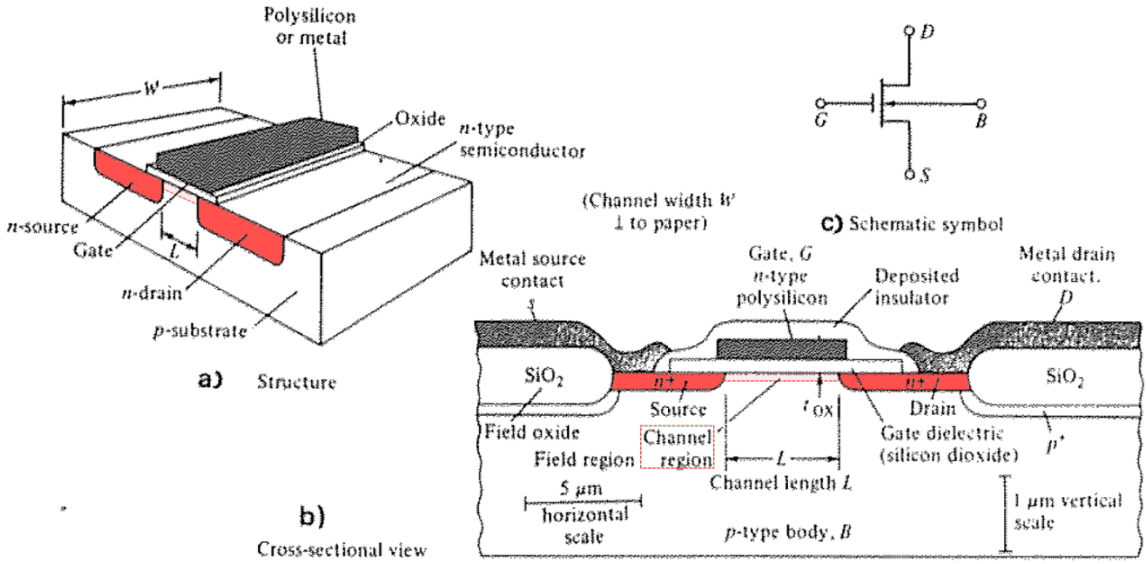
63. Patent Owner also annotated FIG. 5(b) of the '195, '502, and '222 Patents to depict this orientation. PO Res. Br. at 7.



64. Onoda discloses an active region. This is depicted in the enlarged excerpt of FIG. 3 of Onoda, below, in an example of a NMOS transistor. As can be seen from the below, a gate is provided in yellow where a charge applied to it forms a channel across the source and drain region. (*See, e.g.,* Onoda at [0029] ("a floating electrode formed over a channel region that is positioned between the source region and the drain region").)



65. This understanding of source, gate, drain, and transistor operation is confirmed via *Wolf and Tauber*, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions."



(v) Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate,"

66. Onoda discloses a single drift layer. The second semiconductor layer 102, which is annotated tan, is an example of the claimed single drift layer. As can be seen from the annotated FIG. 3 below, the single drift layer 102 in Onoda is "disposed between the "other surface of said surface layer" (the bottom surface) and the underlying substrate 101 as the claimed "substrate." Onoda discloses that the second semiconductor layer 102 is an epitaxial layer. Onoda at [0041] and [0046]-[0047].

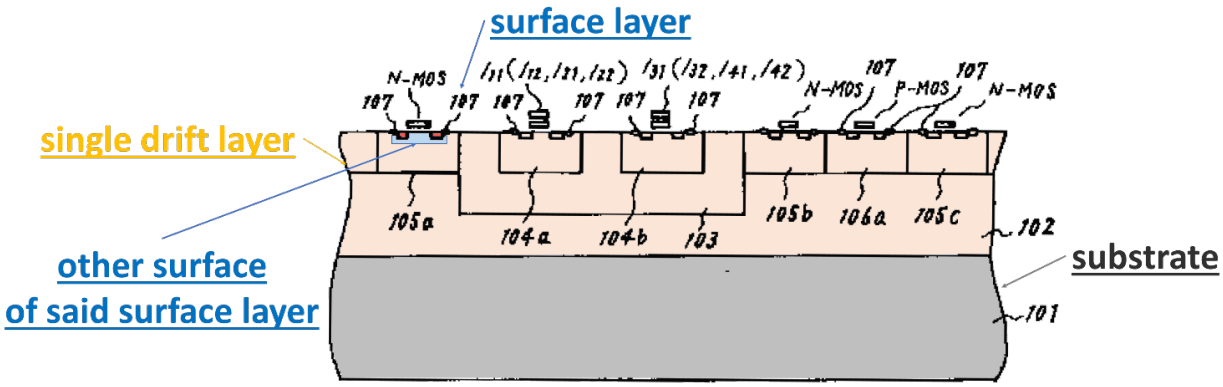
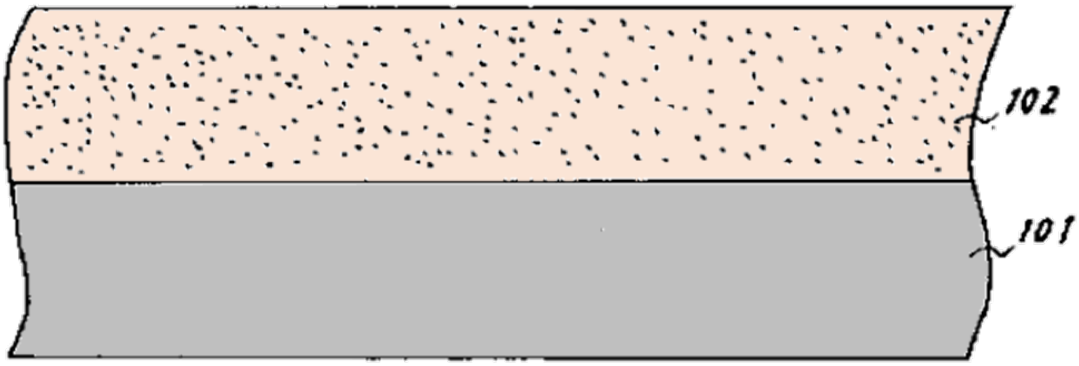
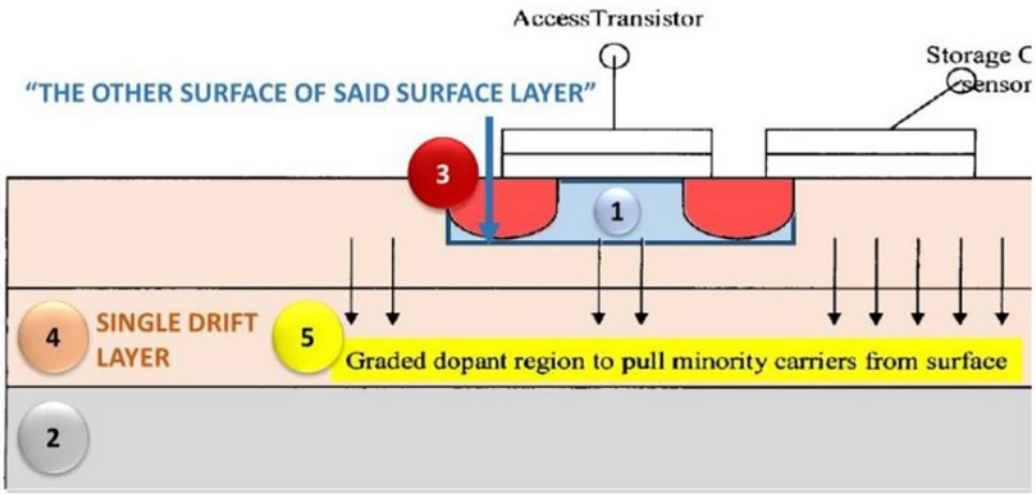


FIG. 3 of Onoda

67. FIG. 5 in Onoda below shows intermediate processing steps, where the substrate 101 and the single drift layer 102 are created. (Onoda at [0047]; *see also id.* at FIGS. 10-12 (showing final dopant profiles); *see also id.* at [0041]-[0051].)



68. Onoda's single drift layer 102 matches Patent Owner's annotations to FIG. 5(b) of the '195, '502, and '222 Patents. As can be seen from the below, Onoda has an identical configuration as identified by Patent Owner.



69. Onoda's single drift layer 102 has a graded concentration of dopants extending between the surface layer and the substrate 101. FIG. 8 depicts the semiconductor device of Onoda, and FIG. 11 demonstrates that device's dopant profile of the portion marked as B-B' (cross-section annotated yellow). (Onoda at [0052].)

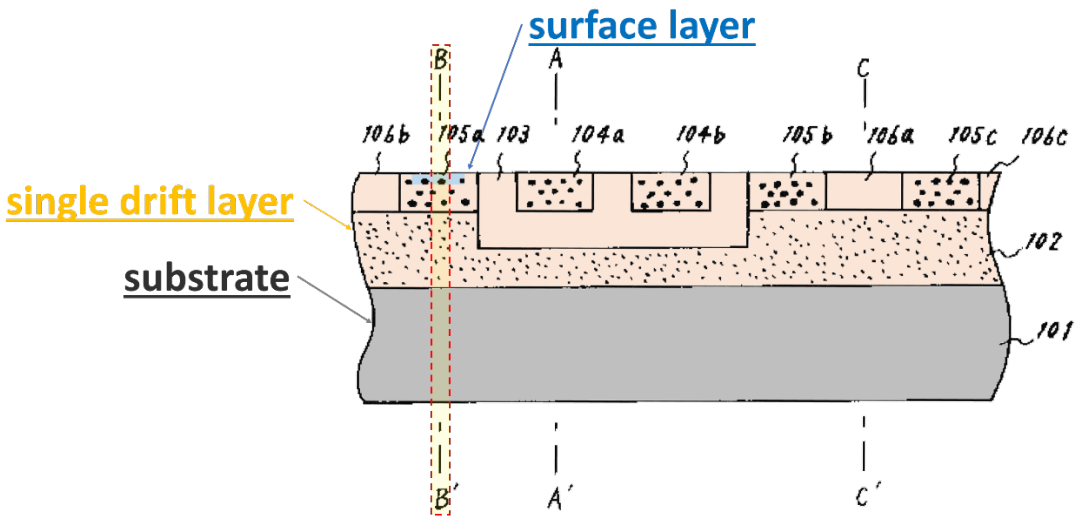

surface layer
single drift layer
substrate
B
A
C
106b
105a
103
104a
104b
105b
106a
105c
106c
102
101
B'
A'
C'

FIG. 8

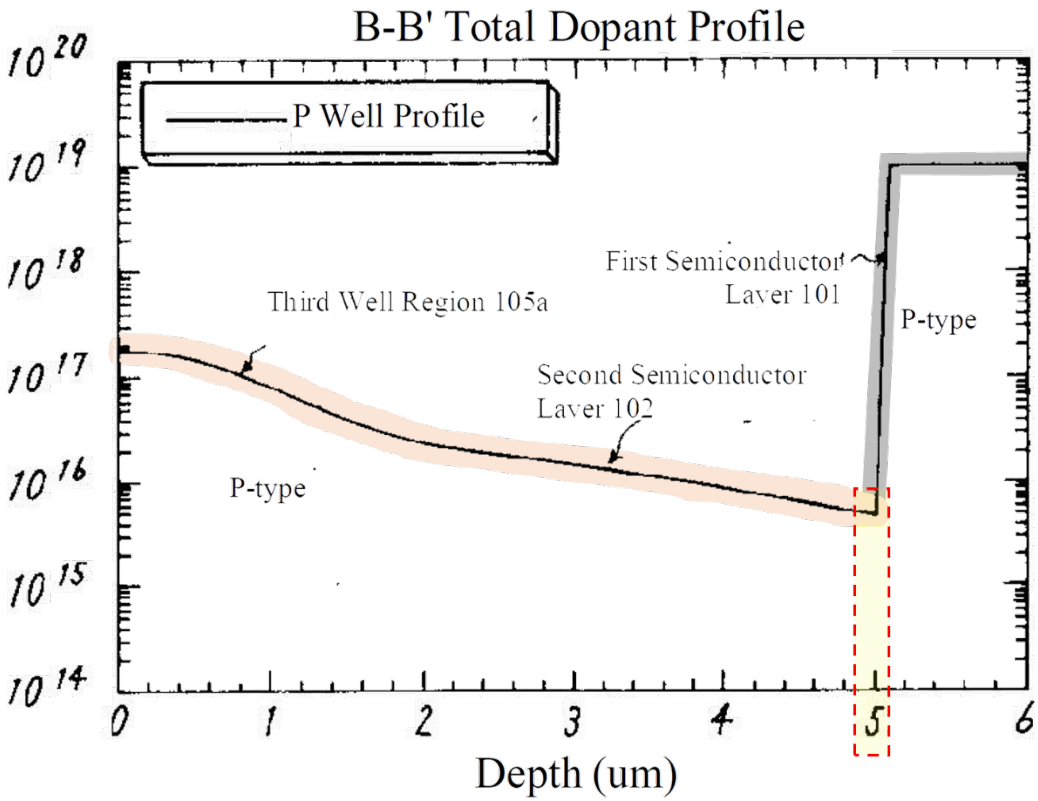

B-B' Total Dopant Profile
P Well Profile
First Semiconductor Layer 101
Third Well Region 105a
P-type
Second Semiconductor Layer 102
P-type
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
0
1
2
3
4
5
6
Depth (um)

FIG. 11

70. Onoda's semiconductor device has a dopant profile whose impurities decrease from the surface, *i.e.*, depth 0, to the substrate, *i.e.*, depth of 5 um. (Onoda at [0046] (stating that the p-type epitaxial layer 102a of the single drift layer 102 has a thickness of about 5um); *see also id.* at [0052] ("both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly"); *see also id.* at [0047] (describing doping layer 102), [0048]-[0050] (stating how wells are created, which is discussed in further detail in Element [1.6]).)

71. Onoda describes implanting dopants and thereafter thermally diffusing them to create the gradient. (Onoda at [0047]-[0050].).

(vi) Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

72. In my opinion, Onoda discloses this limitation. Onoda's drift layer has a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (gray, starting at the 5 μm depth level). Such a dopant concentration profile can be considered a decaying exponential as Onoda's FIG. 11 depicts the carrier concentration as nearly a straight line on a semi-log (log/linear) graph. The below annotation of Onoda's FIGS. 8 and 11 depicts the movement of the minority carriers (purple arrow) due to the first static unidirectional electric drift

field, at a depth corresponding to Onoda's second semiconductor layer 102 (tan) as the single drift layer. The arrow indicates the movement of minority carriers from the surface layer to the substrate. A POSITA would understand that the field would be in the opposite direction.

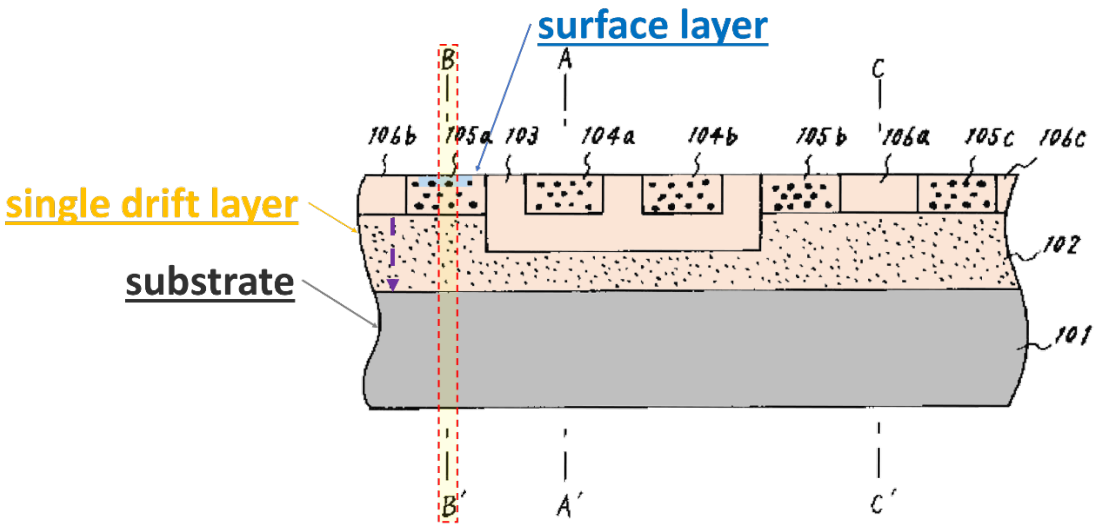


FIG. 8

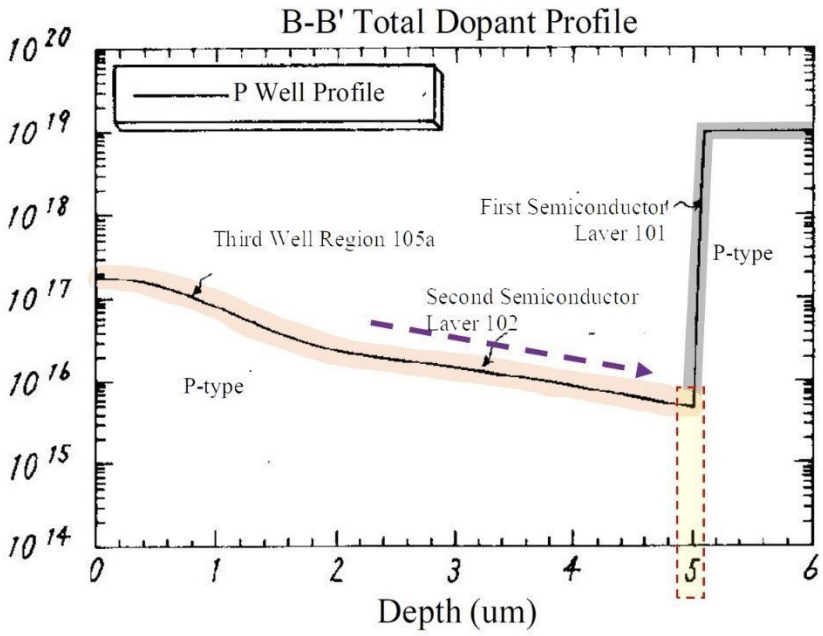


FIG. 11

73. In my opinion, it was well known that having a downward dopant gradient would create an inherent, and static electric drift field to aid the movement of minority carriers down towards the substrate irrespective of whether the doped regions are n-type or p-type. As I have described elsewhere in this declaration, this was a known property that the Patent Owner acknowledged in prosecution, and it was described in the Kamins and Jastrzebski references.

74. In addition, a POSITA would have understood that Onoda's electric drift field would have been static because the graded dopant concentration that causes the Onoda's electric drift field after the completion of the device fabrication is static. Onoda's device is created through ion implantation and thermal diffusion and its dopant profile, and consequently its electric drift field, would have been set after the device is fabricated. (Onoda at [0047]-[0050].)

(vii) Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

75. Onoda discloses a well region (green) in its single drift layer (epitaxial layer 102, tan). (*See* Onoda at FIG. 3, [0045]-[0046].)

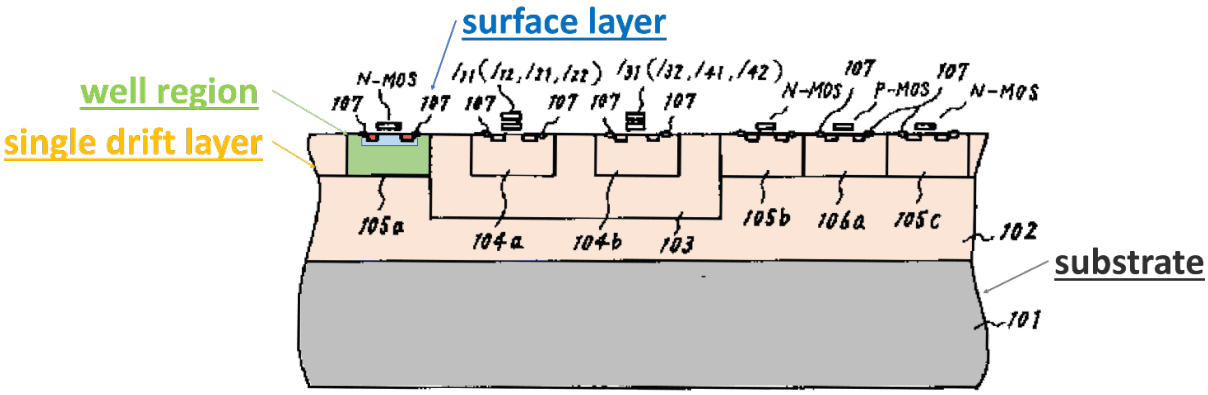


FIG. 3

76. Disposed within that single drift layer 102 in Onoda is a p-type well region (green). (Onoda at [0042] ("105a [is a] P-type third well region[ ] formed in the surface of the second semiconductor layer 102"), FIG. 2 (105a); *see also id.* at [0044] ("the plurality of N-channel MOS transistors is formed in the third well regions 105a, 105b, 105c.").)

77. Onoda discloses the steps to form the P-wells in the lightly-doped semiconductor layer 102 as part of Onoda's single drift layer. (Onoda at [0048]-[0050].) After forming the epitaxial second semiconductor layer 102, a P-type dopant (*e.g.*, boron B) is implanted to form P-type implantation layers 104a, 104b and 105a through 105c, and an N-type dopant is implanted to form N-type implantation layers 106a through 106c. (*Id.* at [0049].) Finally, after carrying out heat treatment, a P-type third well region 105a is formed, among others, in the

second semiconductor layer 102, as illustrated in FIG. 8 below. (*Id.* at [0042], [0048]-[0050].)

78. Onoda discloses that its well region has a graded concentration of dopants (105a) and a second static unidirectional electric drift field (102) to aid the movement of minority carriers from said surface layer to said substrate. FIG. 11 depicts the gradient profile of cross-sectional B-B' of FIG. 8 (annotated in yellow). (*See also* Onoda at [0052].) Both figures are provided below.

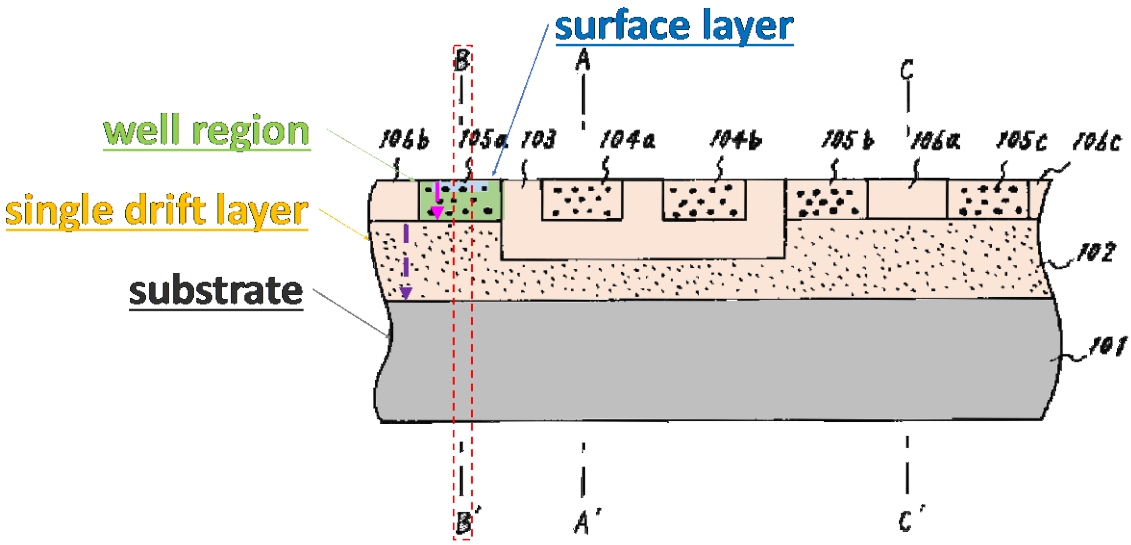


FIG. 3

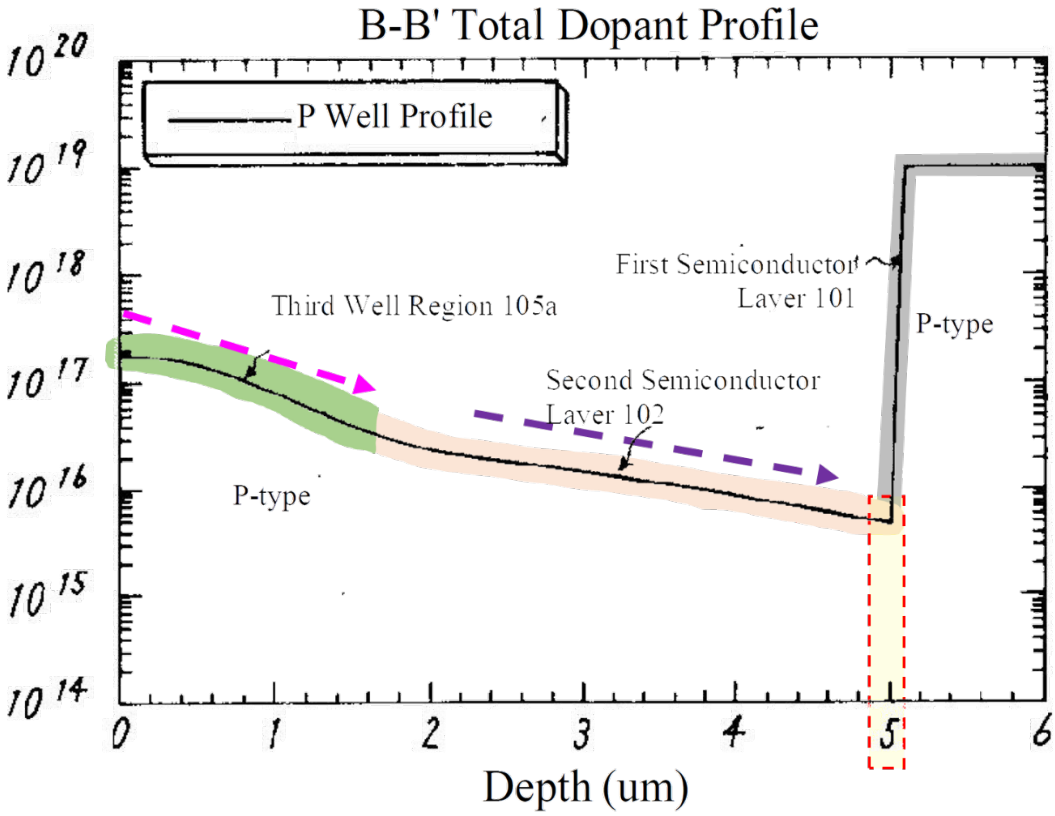


FIG. 11

79. The well region 105a, like the "single drift layer" 102, has a dopant profile that has a downward sloping gradient. (Onoda at [0052].) The well region 105a has the claimed second static unidirectional electric drift field. The pink arrow depicts the direction of minority carrier movement (where the field would be depicted in the opposite direction) to aid the movement of minority carriers from the surface layer to said substrate.

80. In my opinion, it was well known that a downward dopant gradient would create an inherent, and static electric drift field to aid the movement of minority carriers down towards the substrate. As I have described elsewhere in this

declaration, this was a known property that the Patent Owner acknowledged in prosecution, and it was described in the Kamins and Jastrzebski references.

81. In addition, a POSITA would have understood that Onoda's electric drift field over the well region would have been static because the graded dopant concentration after the completion of the device fabrication is static. Onoda's device is created through ion implantation and thermal diffusion and its dopant profile, and consequently its electric drift field, would have been set once the device was fabricated. (Onoda at [0047]-[0050].)

82. Onoda describes other well regions in other embodiments that also meet the claimed well region. For example, FIG. 13 below shows well region 105a as separated from others and depicts well region 105a (dark green, below) encompassed within portions of the epitaxial layer 102 and separated from other well regions (light green). (Onoda at [0087] (stating that "the first well region 103, third well region 105, and fourth well region 106 are separated from each other, that is, wherein the second semiconductor layer 102 is interposed between the well regions, as depicted in FIG. 13"); [0042] (generally describing the well regions 104a, 104b, 105a, 105b, 105c, 106a, 106b, 106c).)

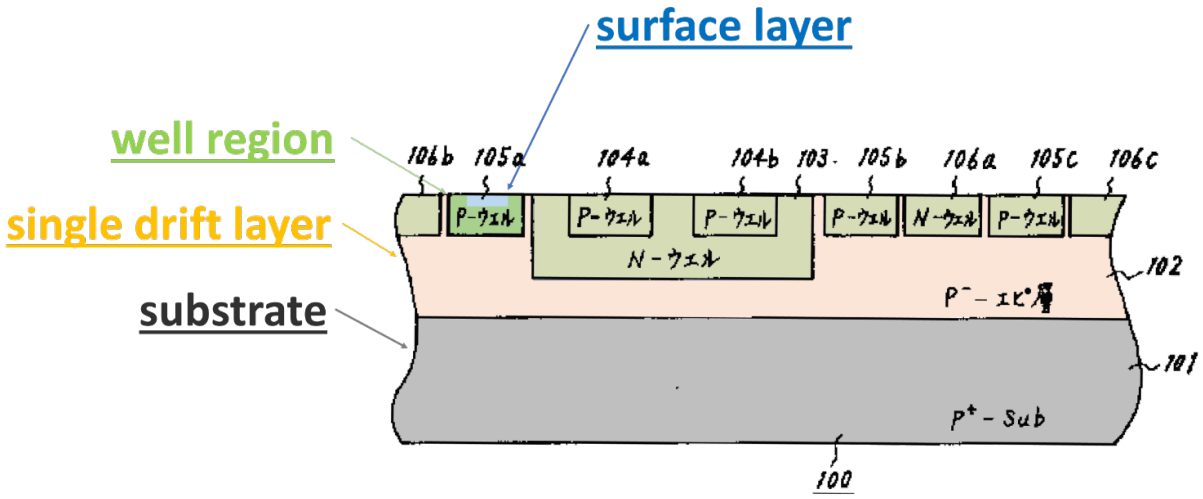


FIG. 2 of Onoda

83. Second, well region 105 (a) is part of a contiguous well structure, where the entire well region teaches the claimed "well region." This is depicted in FIG. 8, below, with the well region 105a annotated in dark green and the other well regions annotated in light green. (*See* Onoda at FIG. 8; [0042] (generally describing the well regions 104a, 104b, 105a, 105b, 105c, 106a, 106b, 106c).)

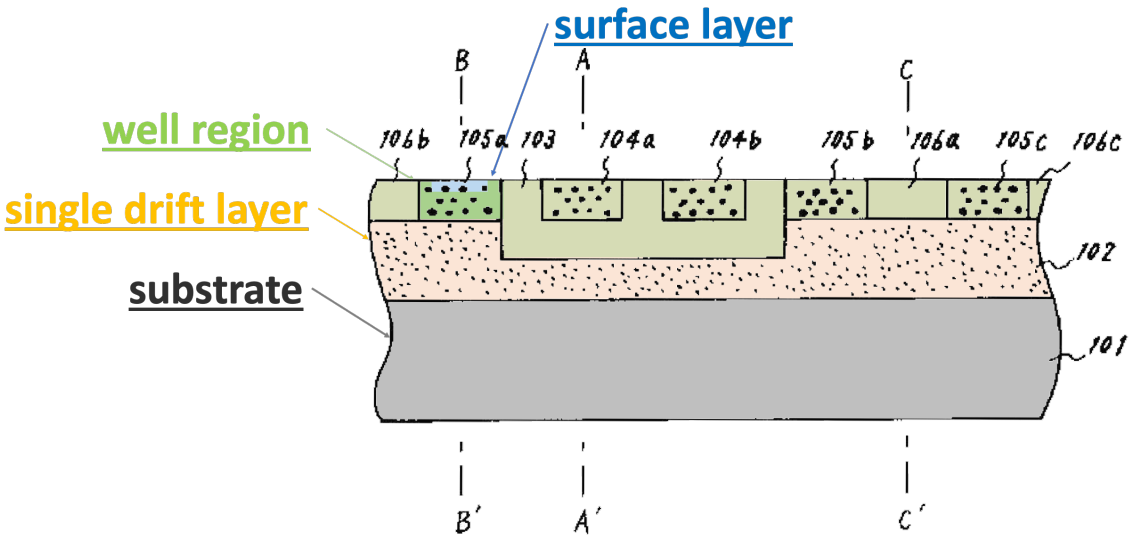
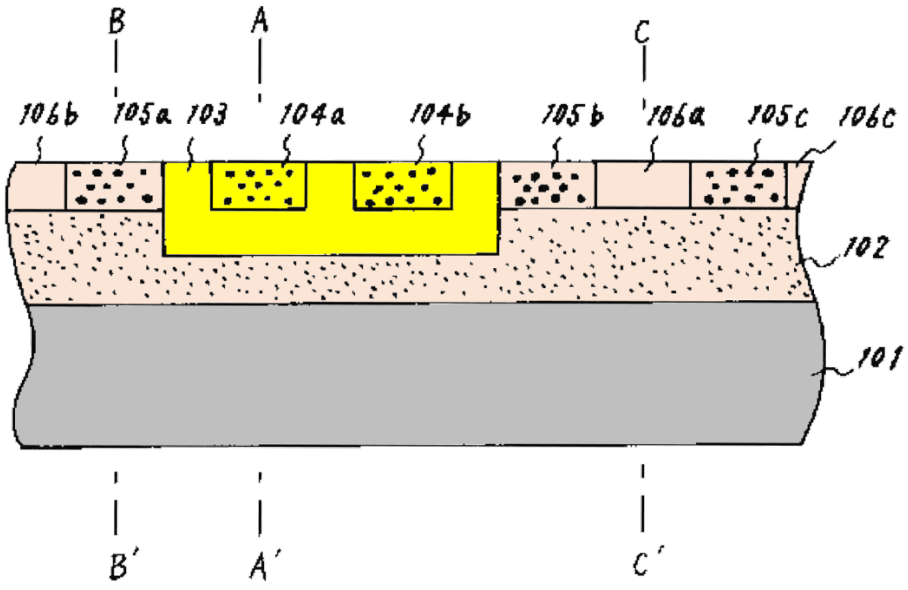


FIG. 8

b. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

84. Onoda teaches that the doped epitaxial semiconductor layer 102 which is fabricated using ion implantation and includes an epitaxial layer 102a with a depth of "about 5 μm." (Onoda at [0046]-[0047].) Further, Onoda teaches forming its well structures with deep wells formed by ion implantation and thermal diffusion, extending 3-5 μm deep. (*Id.* at [0052].) Onoda, moreover, describes its n wells as being "deep" (annotated yellow) and those wells do not go as "deep" as the claimed single drift layer (tan) (*id.* at FIG. 8 (excerpted below)), further demonstrating that the single drift layer 102 in Onoda is a "deeply-implanted layer." (*Id.* at FIG. 11).



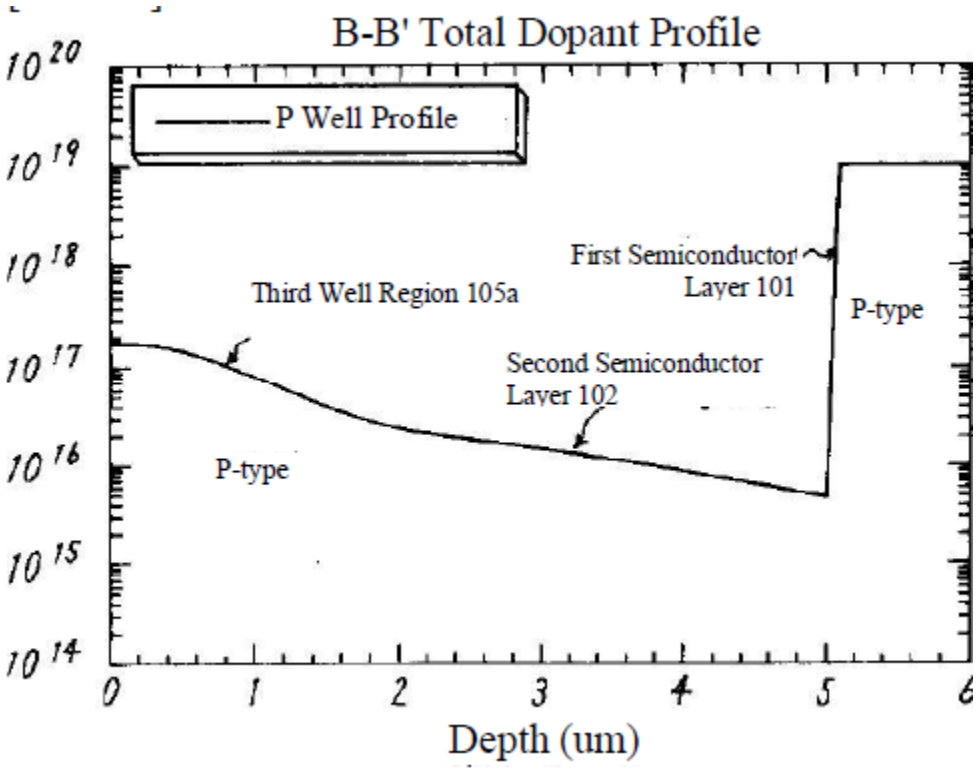


FIG. 11

85. And this would have been an obvious modification to implant the layer deep even if it were argued that the layer was not deep. As noted above, Onoda suggests implanting its layers "deep," and a POSITA would have found it obvious to do so in light of that suggestion. Furthermore, the '195, '502, and '222 Patents provide little guidance as to what is meant by "deep"; it mentions the deeply implanted layer once (*e.g.*, '195 Patent at 3:37-38) and mentions "deep" in another context, sweeping carriers "deep into the substrate." (*Id.* at 3:33-35.) It was well known to deeply implant layers, and the specification itself confirms it.

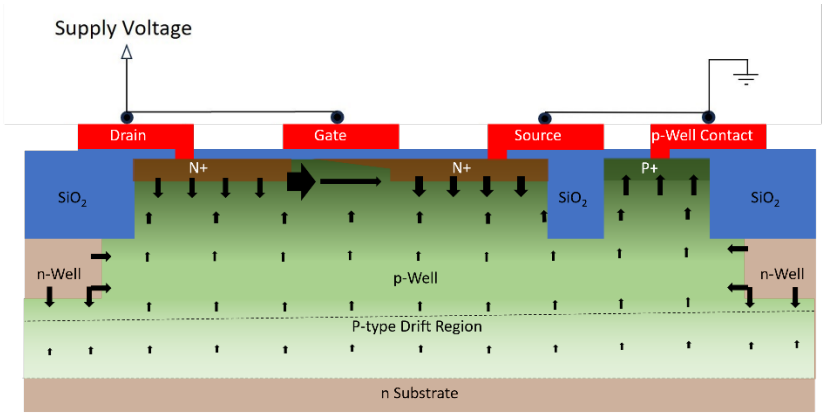
c. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein the said drift layer is an epitaxial layer."

86. Onoda discloses Claim 3. When discussing formation of semiconductor layer 102 (corresponding to the claimed single drift layer), Onoda discloses that it is an epitaxial layer (Onoda at [0041]); that a lightly-doped P-type epitaxial layer 102a with a dopant concentration of 1 x $10^{15}/cm^3$ is formed with a thickness of about 5 μm through epitaxial deposition onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x $10^{19}/cm^3$. (*Id*. at [0046]-[0047].) Subsequent implantation of dopant (*e.g*., boron B) creates an ion implantation layer 102b, which is then subjected to heat treatment to produce a lightly-doped P-type second semiconductor layer 102. Onoda's lightly-doped P-type semiconductor layer 102 is an epitaxial layer.

d. Dependent Claim 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient."

87. Onoda teaches several dopant gradient profiles, in addition to providing graphical depictions of profiles that to a POSITA render a quasi-linear gradient obvious. For instance, Onoda teaches a gaussian distribution of dopants. (Onoda at [0053] ("the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate Gaussian

distributions with the concentrations at maxima near the surface”).) Moreover, providing a quasi-linear gradient was well-known, and this is confirmed by the ’195, ’502, and ’222 Patents describing them amongst a list of known profiles. It would have been obvious to apply a quasi-linear gradient in view of a POSITA’s general knowledge that such a gradient facilitates the movement of minority carriers. It would have further been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile, and would have been readily available as a known option. As shown in the figure below, the unidirectional doping gradient produces a unidirectional electric field.

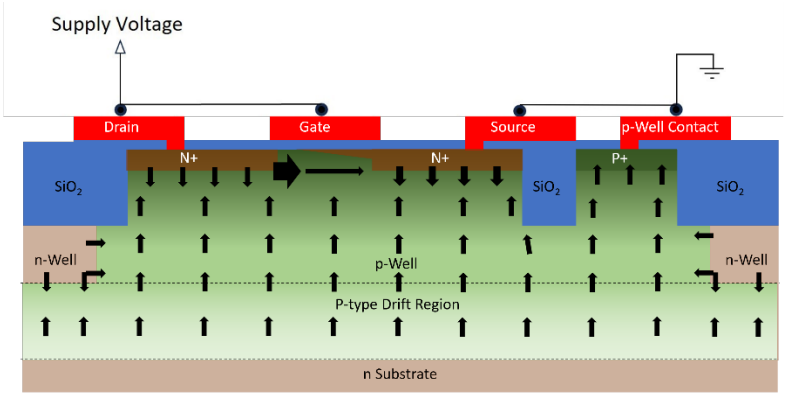


Linearly graded profile with the graded drift region matching the bottom of the well

e. Dependent Claim 6: “The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.”

88. Onoda teaches a gaussian distribution of dopants. (Onoda at [0053].). A POSITA would understand that a gaussian distribution is an exponential gradient and this is confirmed by contemporaneous patents which describe a gaussian

distribution via an exponential. (U.S. Pat. No. 6,900,091 at 23:23-40.) Furthermore, as noted immediately above, Onoda teaches several distributions (Onoda at [0053]) and, moreover, Onoda's FIG. 11, when converted to a linear scale, depicts portions with an exponential gradient. Moreover, a POSITA would understand that, in semiconductor processing, exponential profiles are widely used in semiconductor processing and thus it would be obvious to try. Furthermore, as with the "quasi-linear" gradient limitation, the '195 Patent only mentions "exponential" gradient once in a listing of known dopant profiles ('195 Patent at 2:40-42) and does not illustrate or otherwise describe it, or describe any process steps for obtaining it, thus confirming that it was a well-known alternative. Moreover, Onoda recognizes using downward dopant gradients (Onoda at FIG. 11) and it would have been obvious to apply a POSITA's general knowledge in the art to achieve a known exponential gradient dopant profile because it is one of a finite number of known gradients to use for a downward-sloping graded-dopant and would have also been a simple substitution of one known dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success. As shown in the figure below, the unidirectional doping gradient produces a unidirectional electric field.



Exponentially graded profile with the graded drift region matching the bottom of the well

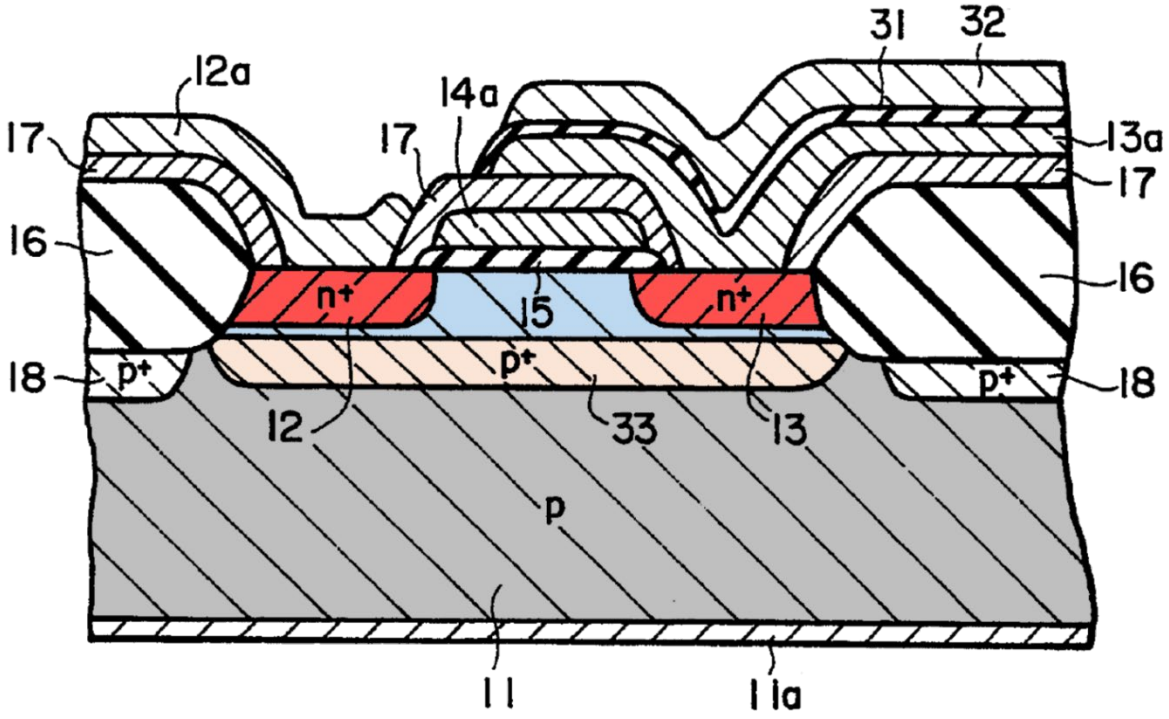
2. Ground II: Onoda in view of Nishizawa Renders Obvious Claims 1, 2, 3, 5, and 6.

89. Onoda and Nishizawa both disclose CMOS devices and are concerned with minority carriers (electrons) moving into the functioning circuitry. Specifically, Nishizawa teaches a CMOS device (*e.g.*, Nishizawa at 7:61-63, FIG. 32) that provides a buried region that has a graded dopant profile (annotated tan, below). (*Id.* at FIG. 16, 18:46-67, 20:25-27.)[1] The graded dopant profile is a p+ type buried region that contains a relatively high impurity concentration at the "top" that progressively decreases as the buried region gets closer to the p type substrate. *Id.* Decreasing the concentration in this manner provides an electric drift field (*id.* at

[1] Nishizawa discloses Figure 32 as a "CMOS arrangement [that] may be termed an ideal circuit arrangement" (15:29-30) and that "the CMOS arrangement [of Figure 32] using the MOS transistor of the present invention is extremely excellent in its high speed operation and low power dissipation," and can "easily" be used to form RAM (15:49-52). Thus the features disclosed in Nishizawa can be used in CMOS technology for both logic and memory. Figure 16, which is pictured, is DRAM that uses the disclosed features of Nishizawa.

18:10-18) that allows minority carriers (electrons) to move from the surface region (blue) having the source and drain (red) to the substrate (gray). (*Id.* at 19:1-9; *see also id.* at 16:19-24 (describing the migration of carriers flowing to the surface as causing errors).)[2] Nishizawa discloses that if the electrons were allowed to "flow" to the circuit rather than down to the substrate, the circuit would not function correctly. (*Id.* at 19:1-9 (Discussing how the electrons contribute to "the extinction of memory.").

FIG. 16



[2] While the discussion in question focuses on FIG. 35, both FIGS. 35 and 16 depict DRAM cells (8:25-27, 63-65) with a buried layer. The buried layer in FIG. 16 extends under both the source and drain regions which a POSITA understands provides for a more effective movement of the electrons to the substrate.

90. Similarly, and as previously discussed, Onoda, discloses a CMOS device in the form of a PMOS and NMOS memory devices combined on one substrate with a graded dopant profile. Onoda teaches that "there is a tendency [for the devices] to become a structure wherein latch-up is inherently likely to occur due to transistors of a parasitic thyristor structure." (Onoda at [004]). Essentially, Onoda is also concerned with electrons moving into the circuit and causing issues as a POSITA would understand that issues with "latch-up" are related to the movement of the minority carrier, which in this case are electrons. Thus, both Nishizawa and Onoda use a graded doping profile to control electron movement.

91. A POSITA would have been motivated to combine the teachings of Onoda with the teachings of Nishizawa as both prior art references focus on CMOS devices with gradient doping such that the impurity concentration intentionally becomes less toward the substrate and effectively controls the movement of minority carriers. Nishizawa's teachings of CMOS and minority carrier diffusion are well known elements which, when combined with Onoda, would yield predictable results. A POSITA would have found it obvious to apply teachings of CMOS—which was well known and described in Nishizawa—and apply it to Onoda's teachings of PMOS and NMOS as it was well known that a CMOS (complementary MOS) is a combination of both PMOS and NMOS devices on the same substrate. Nishizawa states an "object of the present invention is to provide a semiconductor device of the

type described above, which is suitable for use as a CMOS" and describes an NMOS and PMOS pair as being a CMOS (*e.g.*, Nishizawa at FIG. 32) for memory (*id.* at Abstract), while Onoda describes both NMOS and PMOS in a single memory device. (Onoda at FIG. 3.) A POSITA would have been motivated to apply Nishizawa's teachings of minority carrier diffusion based on a downward sloping dopant gradient (*e.g.*, Nishizawa at 18:46-67) to Onoda's teachings of a downward sloping dopant gradient (*e.g.*, Onoda at FIG. 11). Both Nishizawa and Onoda disclose similar structures with a graded dopant, and while Onoda generally confirms issues related to minority carrier movement (*i.e.*, latch-up), Nishizawa makes explicit the concept of an "electric field" that migrates minority carriers to a substrate based on a dopant gradient (Nishizawa at 18:10-18). A POSITA would have been motivated to combine teachings of Nishizawa's explicit discussion of concepts to the structures described in Onoda as confirmation of Onoda's teachings.

92. Making this combination of teachings would have combined known elements to achieve predictable results (*e.g.*, applying Onoda's PMOS and NMOS transistors to CMOS as disclosed by Nishizawa and applying Onoda's downward dopant gradient to Nishizawa's teaching of the electric fields and minority carrier drifts that a downward dopant gradient creates). A POSITA would have seen such combinations as yielding expected results with known prior art elements and would have moreover found it obvious to try.

93. Moreover, both Nishizawa and Onoda are directed to similar devices, which face similar problems, and seek similar solutions. Both are directed to memory devices (Nishizawa at Abstract; Onoda at [0004]), and to reducing punch through. (Nishizawa at Title; Onoda at Object.)

a. Independent Claim 1

(i) Preamble: "A CMOS semiconductor device comprising:"

94. Consistent with Ground I, Onoda discloses a CMOS semiconductor device. Further, Nishizawa teaches CMOS. FIG. 32 depicts using NMOS and PMOS as CMOS (Nishizawa at FIG. 32 and 15:27-52) and further states one of its objects is to provide an improved CMOS device (*id.* at 7:61-63).

(ii) Elements [1.1]-[1.4]

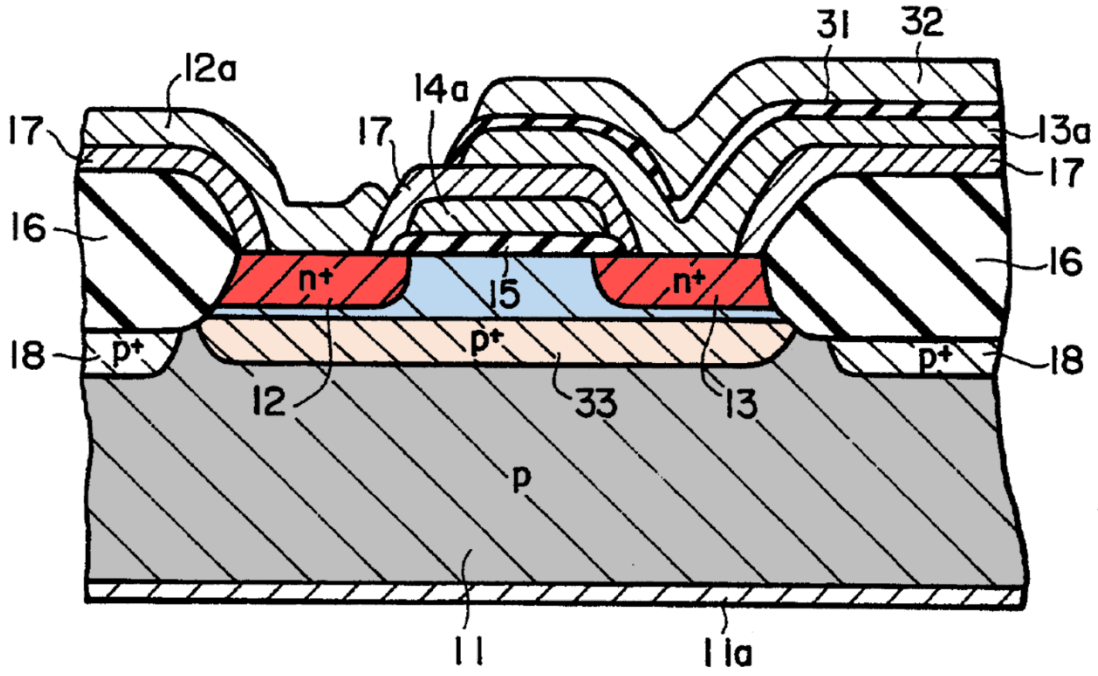
95. Consistent with Ground II, Onoda discloses and/or renders obvious the elements [1.1] through [1.4].

(iii) Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

96. Onoda discloses a drift layer whose dopant concentration has a downward gradient which a POSITA would have recognized as providing a built-in, static, unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate. (III.B.1.a.vi.) Nishizawa makes these elements explicit and explains that it is necessary to form an impurity gradient in the drift

layer to move the minority carriers to the substrate. Nishizawa at 18:10-19:53. Such an impurity gradient will keep the electrons from being captured by the circuitry at the surface and impairing the circuit. (*Id.* at 18:42-50.) FIG. 16 in Nishizawa depicts a source and drain (red, below) at the surface region (blue), where buried region 33 (tan) provides an "impurity concentration gradient … [that is] progressively decreasing toward the p type substrate" (gray). (Nishizawa at 19:4-5; *see also id.* at 18:50-59 ("the impurity concentration of that portion of the p+ type buried region 33a located adjacent the channel region and the n+ type region 13 is set at about $1x10^{17}$ cm^{-3}, with progressively lowered concentration as the portions of the buried region 33a go progressively toward the p type substrate 11, in such manner that the impurity concentration of lowermost portion of the buried region is less than at least one third of that of the highest impurity concentration.") The cited-to text refers to the embodiment of FIG. 35, and Nishizawa states that the discussion is likewise applicable to the structure of FIG. 16 which is illustrated. (Nishizawa at 20:23-27.)

FIG. 16



97. Nishizawa teaches "a drift electric field" that is created when there is a "difference in the degree of impurity concentration," which is used to drift minority carriers to the substrate. (Nishizawa at 18:9-18.) To drift electrons within the p+ buried layer to the substrate, "an impurity concentration gradient in the p+ type buried region 33a in the direction toward the p type substrate" is formed. (*Id.* at 18:35-50; *see also id.* at 18:51-67 (stating that the impurity concentration has a downward gradient to the substrate); *see also id.* at 19:1-9.)

(iv) Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

98. The Onoda-Nishizawa combination makes clear that this well region in Onoda provides a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate for the same reasons described above. (III.B.1.vii.)

b. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

99. Nishizawa further teaches that its layer having a graded dopant profile (e.g., region 33a in FIG. 16) is a deeply implanted layer by referring to it as a "deep semiconductor region." (Nishizawa at 22:17 (describing the layer as "a deep semiconductor region (33)").) Furthermore, the layer is created via implantation. (*see also id.* at 18:64-67 (stating that the gradient can be created via implantation).)

3. Ground III: Kawagoe Renders Obvious Claims 1, 2, 3, 5, and 6.

100. Kawagoe teaches CMOS devices whose surface region (its epitaxial layer) has its "impurity concentration gradually lowered depthwise of said epitaxial layer." (Kawagoe at Abstract; 3:32-38; 8:46-54; 15:37-43; 22:66-23:2; 24:34-50.) The "gradient … is gradually lowered in the depthwise direction from the surface of the epitaxial layer … so that the influence to be caused by the carriers (or electrons)

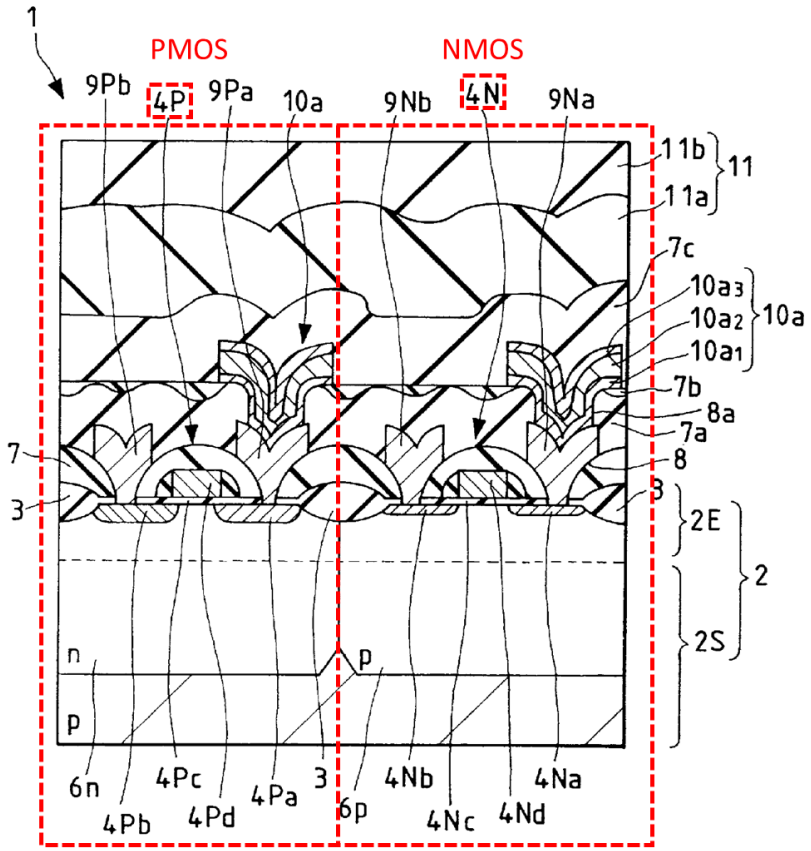
due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient." (*Id.* at 16:3-8.)

a. Independent Claim 1

(i) Preamble: "A CMOS semiconductor device comprising:"

101. Kawagoe discloses a CMOS semiconductor device. (*See, e.g.,* Kawagoe at 15:37-43 (describing the CMOS structure of the embodiment of FIG. 16 having an NMOS 4N and PMOS 4P); *see also id.* at 8:46-54; 22:66-23:2; 24:34-50 (describing CMOS devices).)

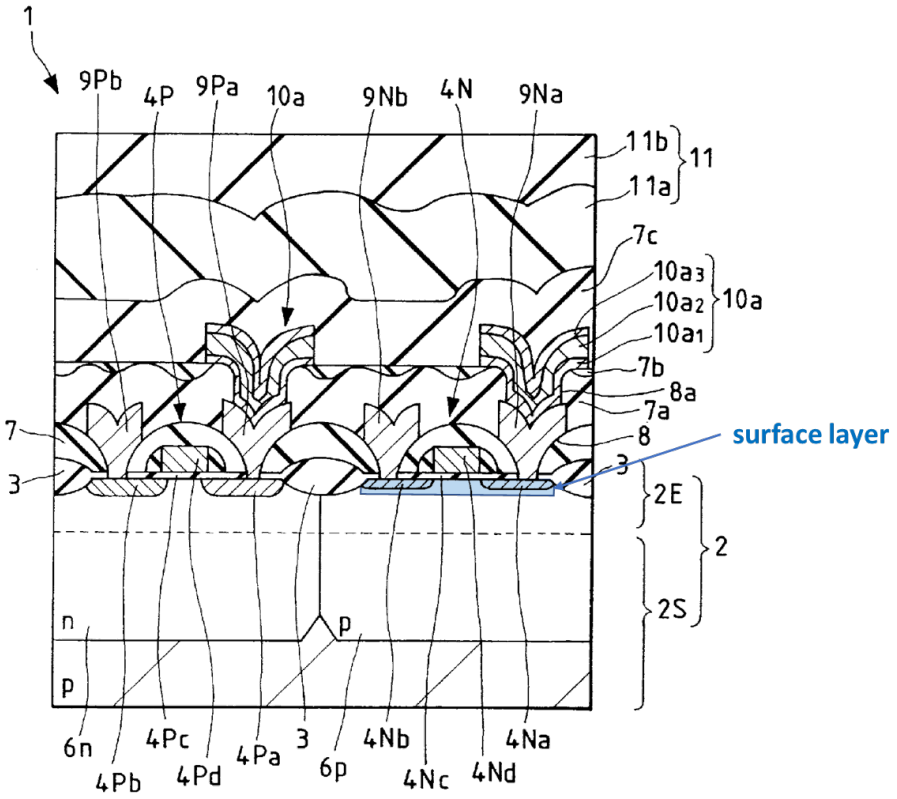
FIG. 16



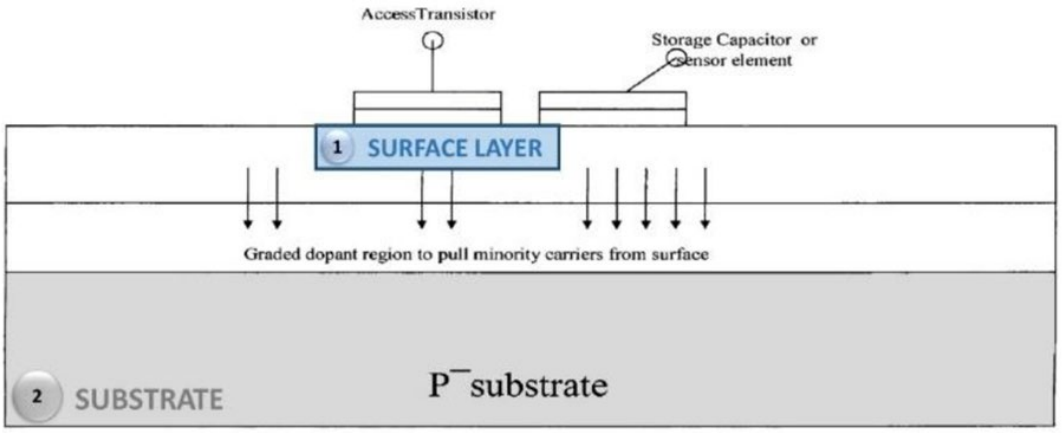
(ii) Element [1.1]: "a surface layer;"

102. Kawagoe teaches a surface layer as depicted below in blue in annotated FIG. 16. Kawagoe's surface layer exists in the epitaxial layer (2E) and the surface layer has an active region with a source and drain formed within it (4Nb and 4Na) (discussed in more detail with respect to Element [1.3]). (Kawagoe at 8:66-9:6; *see also id.* at 15:26-32.) FIG. 16 depicts the finalized devices, with insulating films 7, wirings 10, and protection films 11. (Kawagoe at 15:55-61.) A POSITA would understand that these additional components are not a part of the semiconductor's surface layer because they are, as they state, wirings and insulators for the semiconductor device that is fabricated on the silicon wafer.

FIG. 16



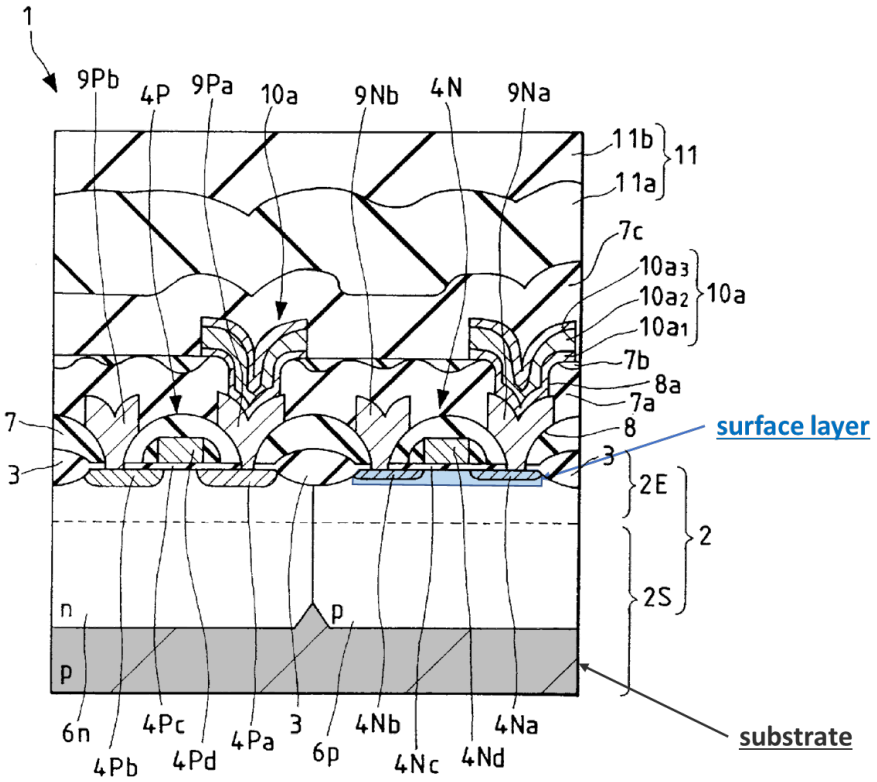
103. Kawagoe's "surface layer" teachings match Patent Owner arguments made in its district court claim construction briefing. Shown below, Patent Owner annotated FIG. 5(b) as support to disclose a "surface layer" (the region surrounding the active region), and Patent Owner further argued in construction that the "surface layer" refers to "a layer at the surface of the silicon." (*Greenthread, LLC v. Intel Corp. et al.*, 6:22-cv-105-ADA at 13.)



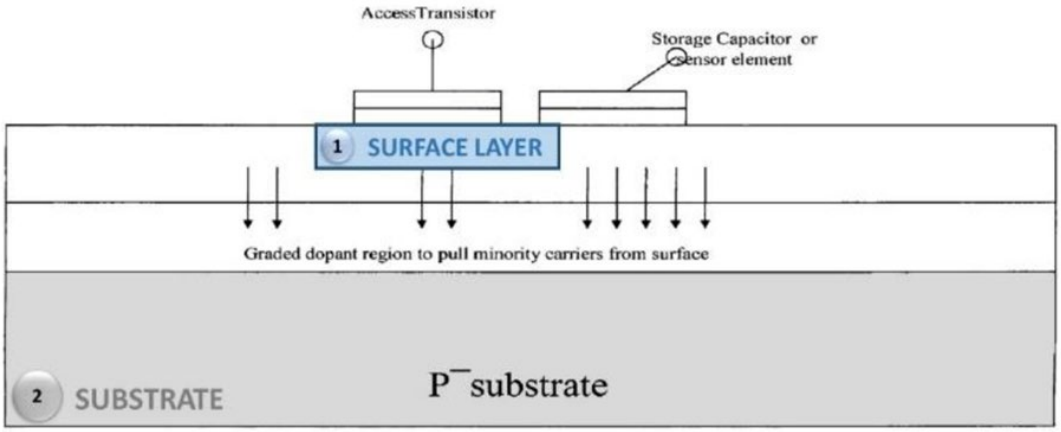
(iii) Element [1.2]: "a substrate;"

104. Kawagoe's substrate is annotated in gray in FIG. 16, below. Kawagoe forms its p-well 6p and n-well 6n in part of the substrate body 2S from the original wafer. (Kawagoe at 15:62-65, 17:50-61, FIG. 21.) A POSITA would understand that at least the portion of the substrate—separate from the well regions—would satisfy the claimed substrate. Moreover, the substrate body 2S by itself further satisfies the "substrate" term because it is, and is identified as, a substrate (*e.g.*, *id.* at 15:7-17; FIG. 1, 6:51-56.)

FIG. 16



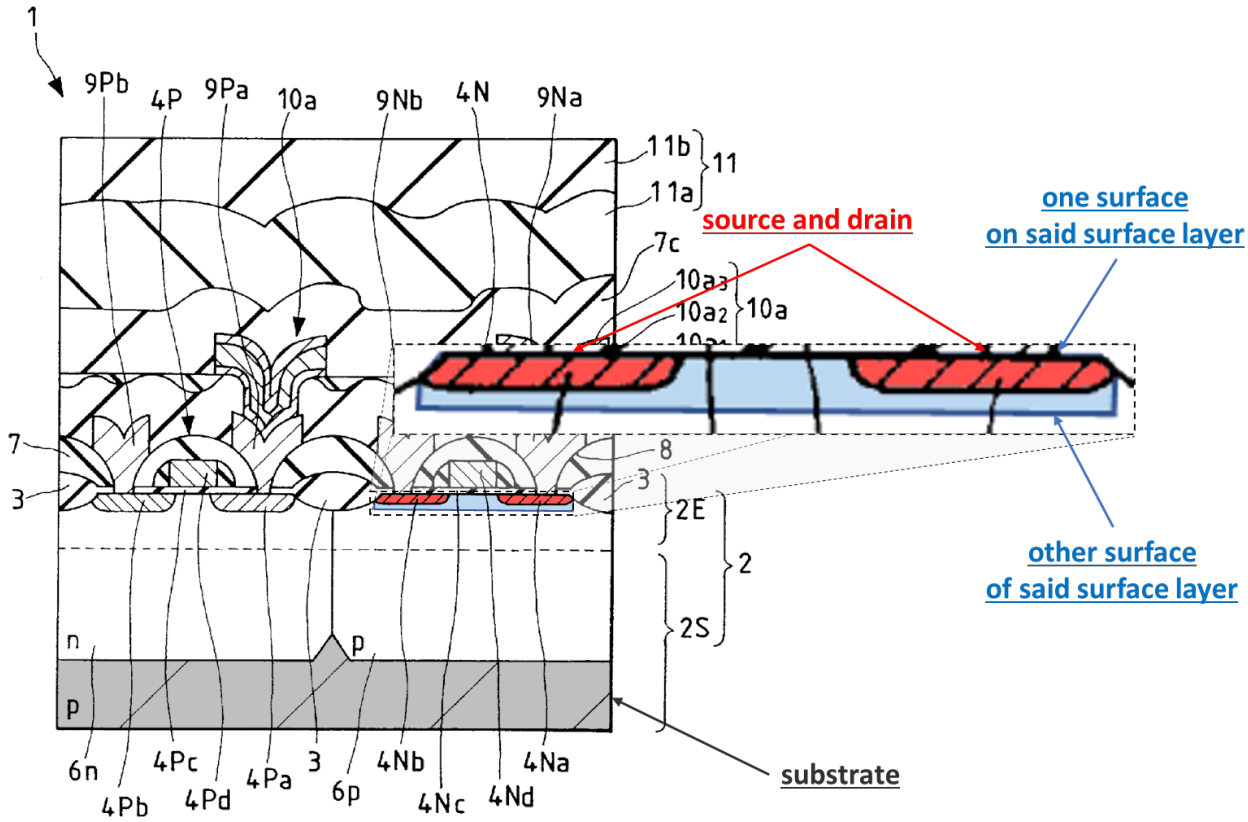
105. Kawagoe's teaching of the "substrate" matches Patent Owner's district court claim construction of "substrate," which was described as "an underlying layer." (*Greenthread, LLC v. Intel Corp. et al.*, 6:22-cv-105-ADA at 15.) Patent Owner's provided annotation to FIG. 5(b) of the '195 Patent is provided below.



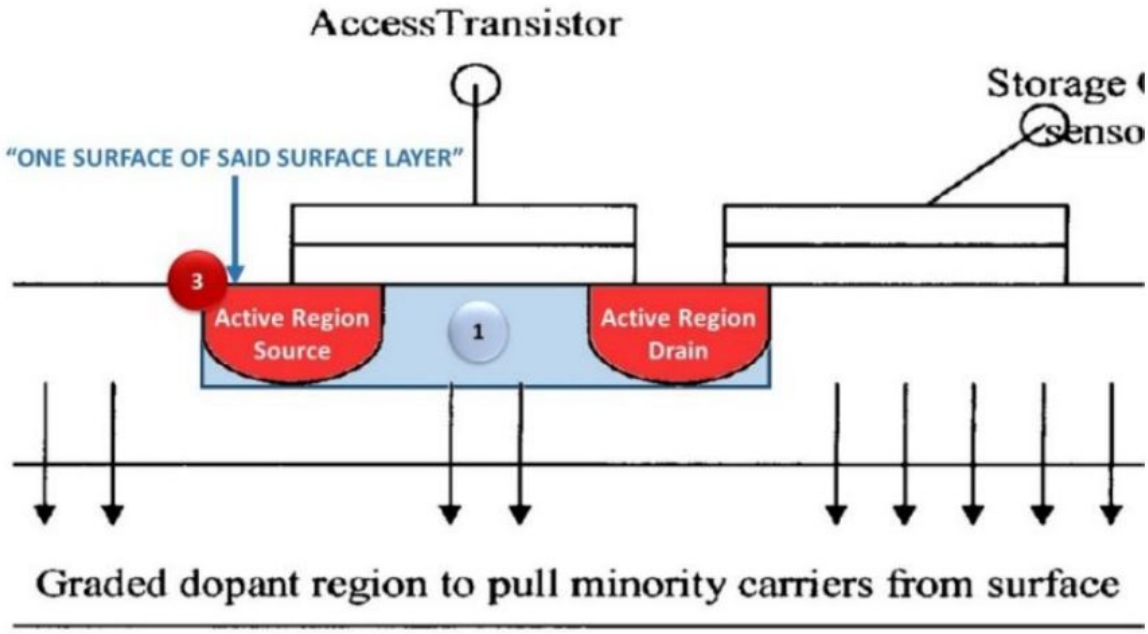
(iv) Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

106. Kawagoe teaches an active region that has a source and a drain disposed on one surface of the surface layer. FIG. 16 below the surface layer contains source and drain 4Nb and 4Na which form an active region. (Kawagoe at FIG. 1, 8:46-9:53, 9:47-53.) Specifically, Kawagoe discloses such an active region with respect to the pMOS 4P part of the active region of Kawagoe's CMOS device in FIG. 1. *Id.*. at 9:41-54 (semiconductor regions 4Pa and 4Pb are formed over the epitaxial layer 2E).

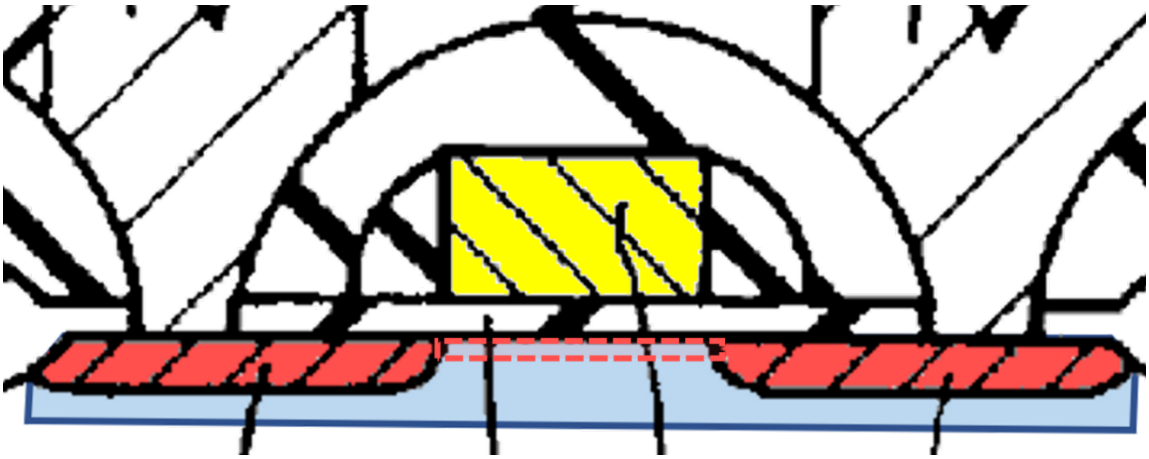
FIG. 16



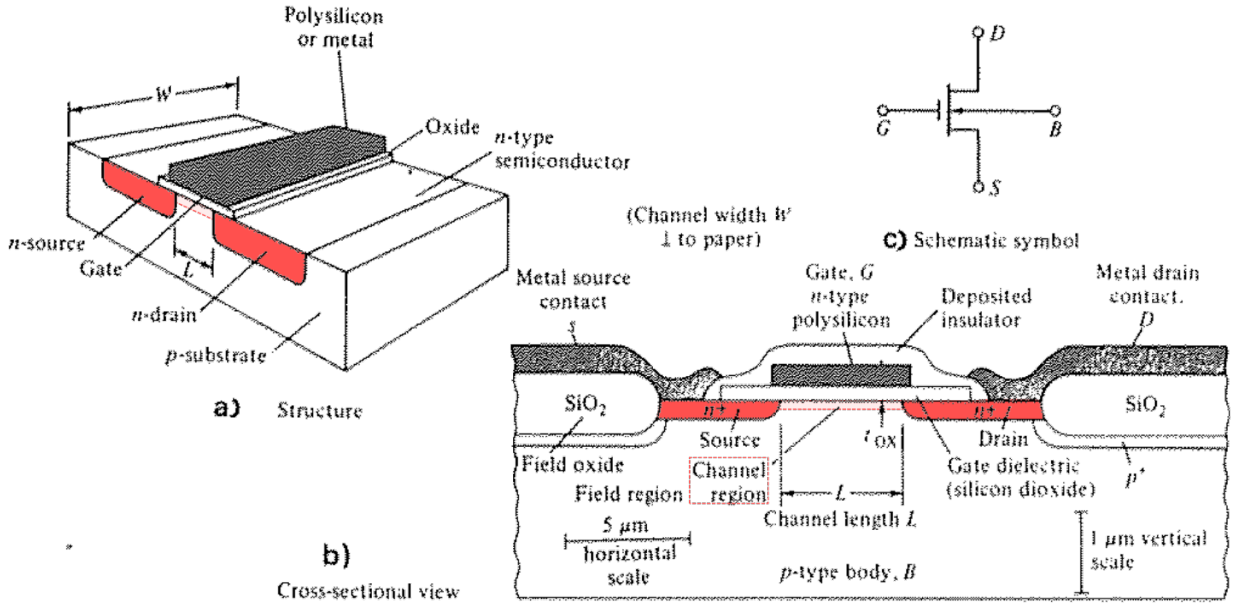
107. The active region is disposed to the top surface of the surface layer, *i.e.*, the claimed "one surface on said surface layer." Patent Owner annotated FIG. 5(b) of the '195 Patent to depict this configuration, where the active region source and drains were disposed on the surface of the surface layer (similar to Kawagoe's FIG. 16).



108. A POSITA would understand that the above-described source and drain configurations of Kawagoe provide an active region. In FIG. 16, below, a charge applied to gate electrode 4Nd (annotated in yellow, *see, e.g.,* Kawagoe at 9:20-26) causes a conductive channel (annotated in dashed-red) to form between the source and drain. A POSITA would understand the source, drain, and channel depicted below to be an active region.



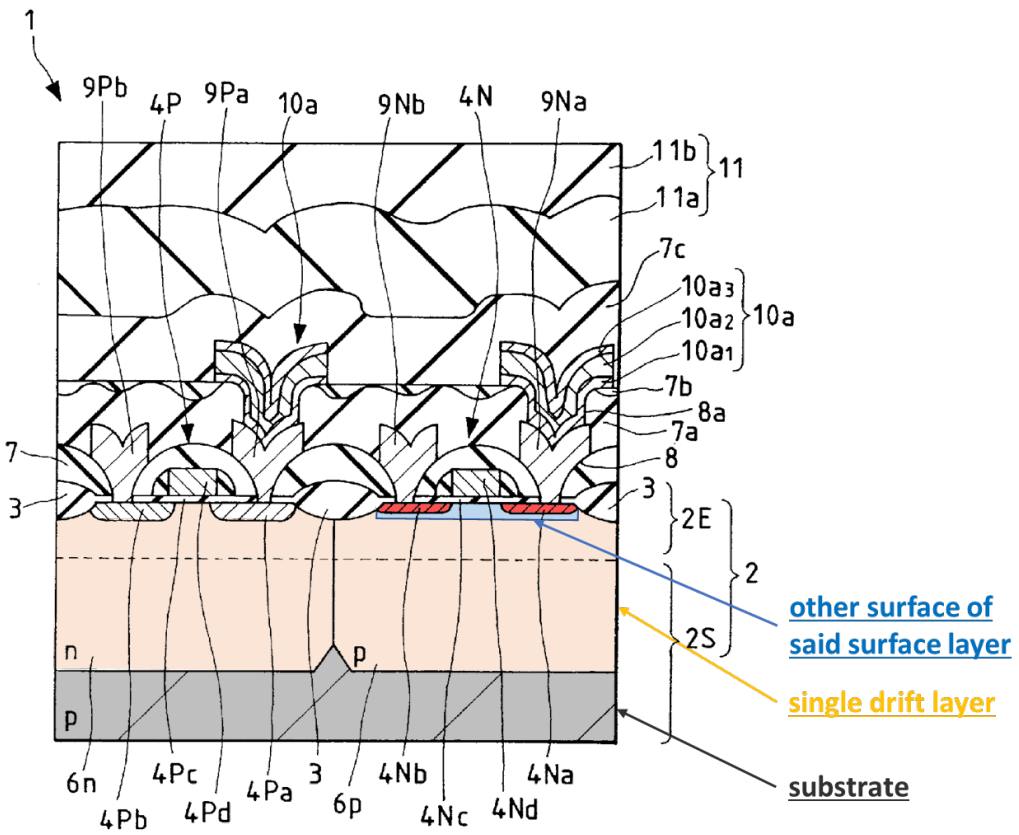
109. This understanding of source, drain, and channel operation in a MOS transistor is confirmed via *Wolf and Tauber*, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor as "[its] channel and [its] heavily doped source and drain regions."



(v) Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate,"

110. Kawagoe teaches the claimed single drift layer (annotated tan, below) disposed between the other surface of said surface layer (blue) and said substrate (gray), and this single drift layer in Kawagoe has a graded concentration of dopants extending between the surface layer and substrate.

FIG. 16



111. Kawagoe's single drift layer (annotated in tan, above) includes the upper portion of the substrate body 2S colored in tan and the epitaxial layer 2E

colored in tan. The epitaxial layer 2E is epitaxially grown on the upper surface of the upper part of the substrate body 2S so that the epitaxial layer 2E and the substrate body 2S constitute an epitaxially integrated single structure with the same single crystal silicon structure and the same p doping. (Kawagoe at FIG. 1 and 6:60-7:3.) As shown in FIG. 16, the upper portion of the substrate body 2S colored in tan is doped to include n-doped and p-doped regions to support PMOS and NMOS transistors for the CMOS device. This single drift layer in Kawagoe is at the surface of the semiconductor device (*see, e.g.,* Kawagoe at 15:62-16:15) and is formed into the CMOS device so that minority carriers (*e.g.*, electrons in the p-well) are attracted to the substrate to reduce errors. (*Id.* at 16:7-11.) The single drift layer in Kawagoe comprises both p-wells and n-wells, where the "impurity concentrations [of those wells are] gradually lowered in the depthwise direction from the principal surface … of the epitaxial layer 2E." (*Id.* at 15:66-16:2.) The depthwise gradient extends from the surface of the semiconductor device into its substrate (*id.* at 16:2-15) and is formed by diffusing impurities in the upper portion of the semiconductor substrate. (*Id.* at 15:26-36). Kawagoe's graded concentration of dopants is depicted in FIG. 17 where the gradient of dopants in the drift layer (tan) extends from the surface of 2E (epitaxial layer of wafer) through the p and n wells (6p and 6n) whose depth is depicted by the annotated yellow), and into a portion of the substrate below the p and n wells (i.e., below depth Ww in FIG. 17).

FIG. 16

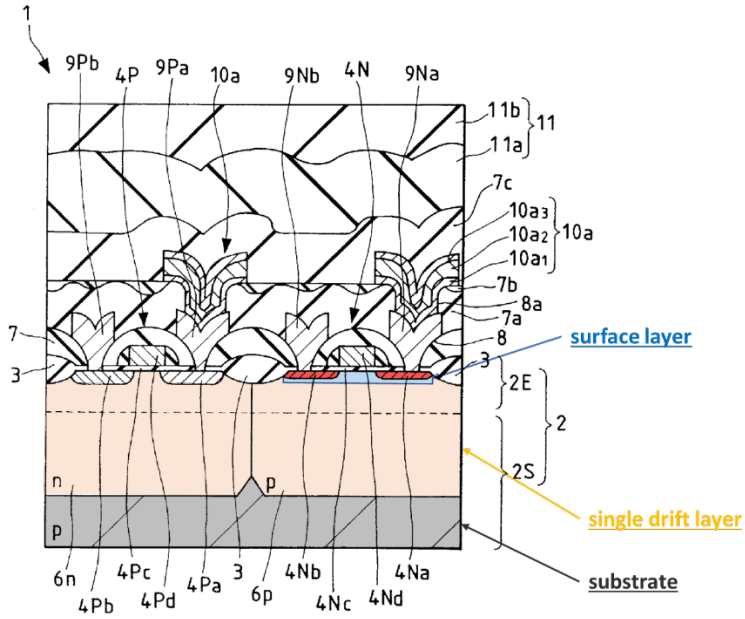
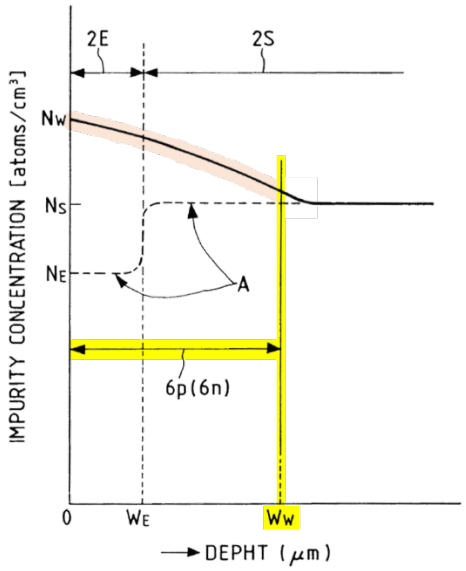
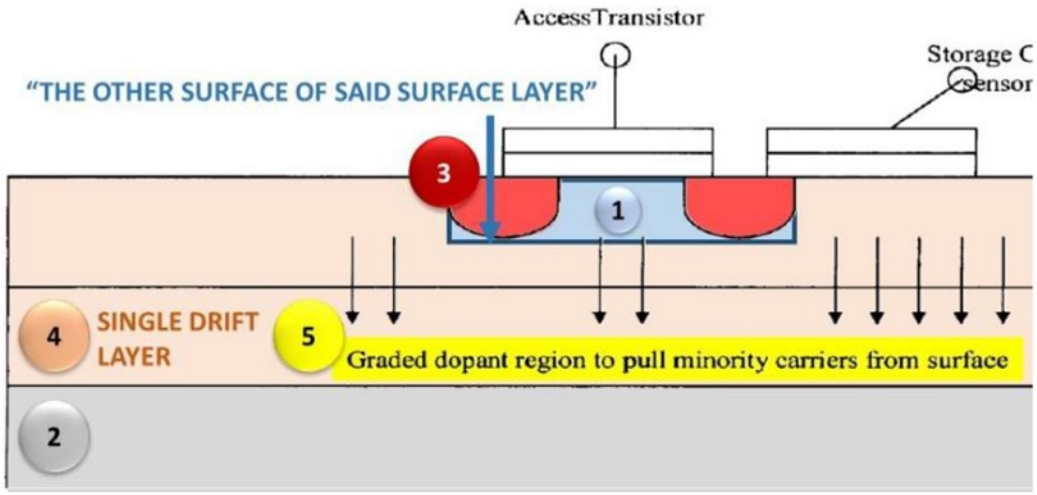


FIG. 17



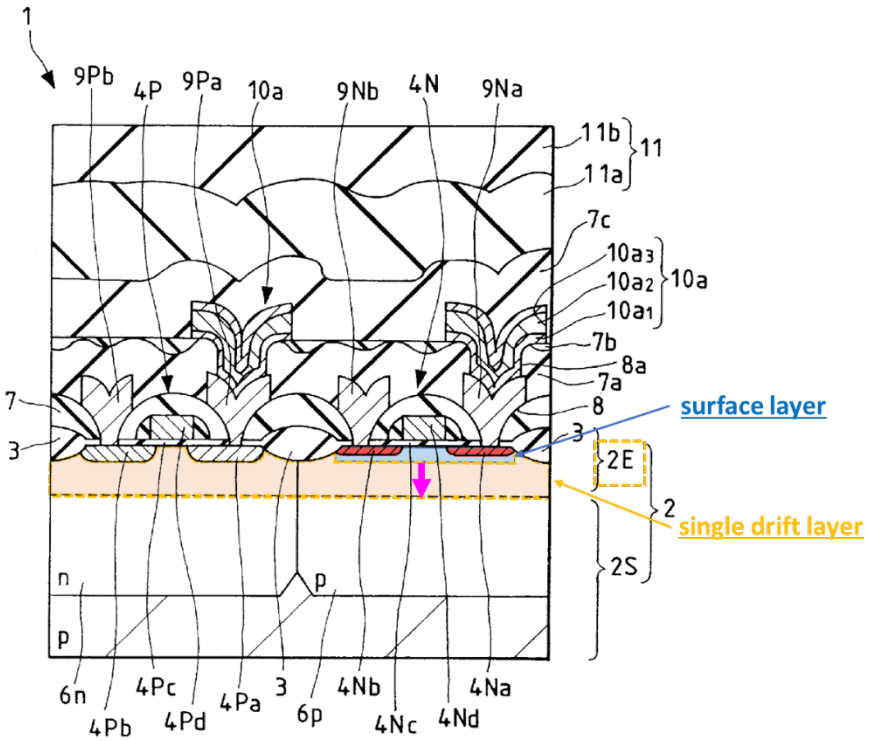
112. Kawagoe describes its impurity gradient region (which was annotated tan, above) as a "diffusion layer." Kawagoe discloses that a "diffusion layer" is created by diffusing impurities into a semiconductor device. (Kawagoe at 2:20-23; *see also id.* at 16:63-17:10 (stating that diffusion of impurities creates a "diffusion layer" when describing the state of the art), 2:21-35, 1:61-65. And, as described above, Kawagoe's drift layer is created by diffusing impurities to create a diffusion layer. (*Id.* at 15:26-36, 17:50-54, 25:27-30.). Finally, the term "drift layer" does not appear in the '195 Patent specification while "drift region" is repeatedly described. (*See, e.g.,* '195 Patent at 2:64-66 and 3:5-6.) For purposes of my analysis, the two terms correspond to identical structures. Moreover, a POSITA would have found the drift layer obvious because Kawagoe itself describes it as a diffusion layer.

113. Kawagoe's teachings match Patent Owner's district court claim construction annotations to FIG. 5(b) of the '195 Patent, where Patent Owner annotated the drift layer.

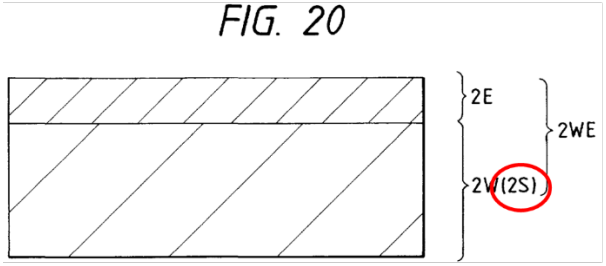


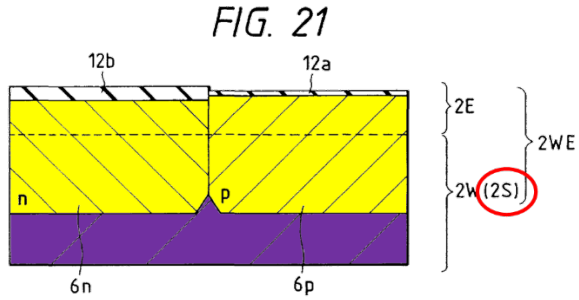
114. Beyond the above, the portion of the diffused impurity gradient that is within the epitaxial layer 2E also is a "single drift layer" and is annotated below in tan within the dashed lines.

FIG. 16

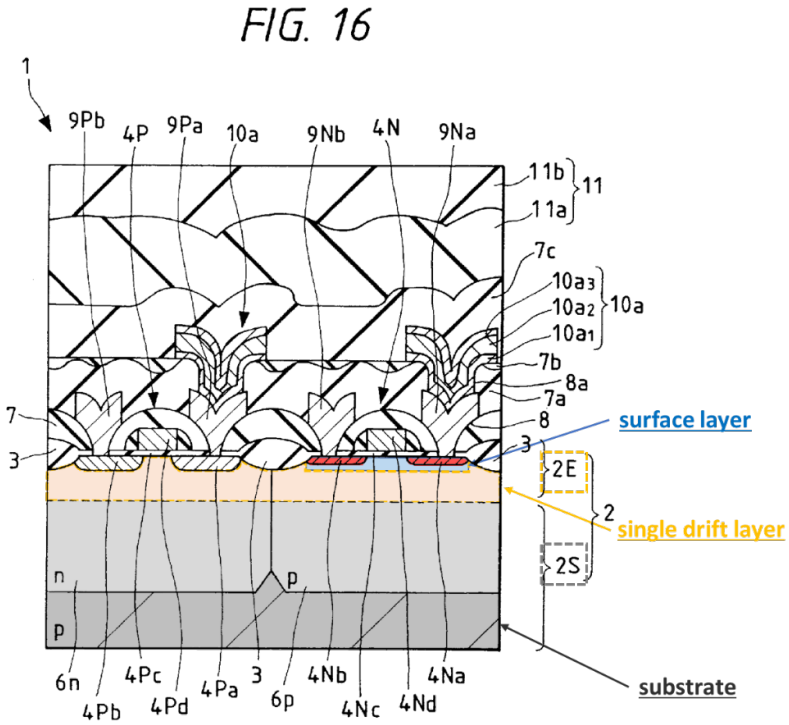


115. Layers 2E and 2S are part of the semiconductor wafer prior to forming the diffusion layer. (*See* Kawagoe at FIGS. 20 and 21.) The substrate 2S is made of a p-type Si single crystal that is initially formed with a p type impurity such as boron and the epitaxial layer 2E is made up of a p-type Si single crystal. (*Id.* at 14:61-15:16.) After the wafer is formed, it is doped with impurities to create the diffusion layer that comprises n and p wells. (*Id.* at 15:26-36.) This process is depicted in FIGS. 20 and 21 where after the diffusion gradient is created (yellow) only a portion of the substrate has a uniform doping profile (purple). (*Id.* at 17:11-21.)





116. Layer 2E has a graded dopant concentration and would also comprise a "single drift layer. Its graded dopant concentration is similarly provided to attract minority carriers to the substrate. (Kawagoe at 15:62-16:11.) Layer 2E is again depicted by the tan-dashed lines below. Layer 2S (substrate body, *e.g.*, *id.* at 15:1-17) as a whole, or merely the uniformly doped portion, further renders obvious the claimed "substrate" (both portions annotated in grey below, with the non-well region after doping in darker grey).



(vi) Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

117. Kawagoe teaches a single drift layer with a graded dopant profile. This graded dopant profile results in "electrons … [being] attracted to the substrate body 2S by that concentration gradient." (Kawagoe at 16:7-11.) A POSITA would understand that electrons are minority carriers in the p-well, and that the electrons are attracted to the substrate due to a static unidirectional electric drift field. A POSITA would understand the field to be static because it is created by doping impurities that are fixed during device fabrication, as depicted in Kawagoe (*see, e.g.,* Kawagoe at 15:26-36, FIGS. 20-21). There are electric fields in separate regions due to the graded doping concentrations, *e.g.*, those depicted by pink and purple arrows in annotated FIG. 17 below, where the pink field would have been understood to be the the first static unidirectional electric drift field. The arrow orientation and direction are depicting the drift of minority carriers (electrons) in the p-well and a POSITA would understand that the electric field would exist in the opposite direction.

FIG. 16

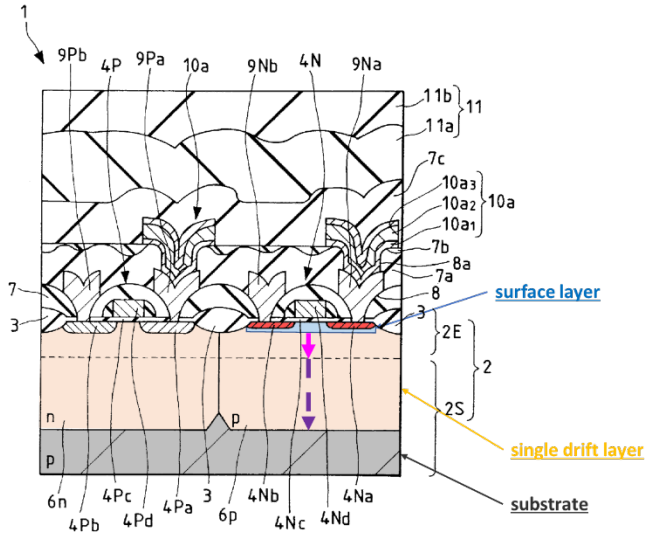
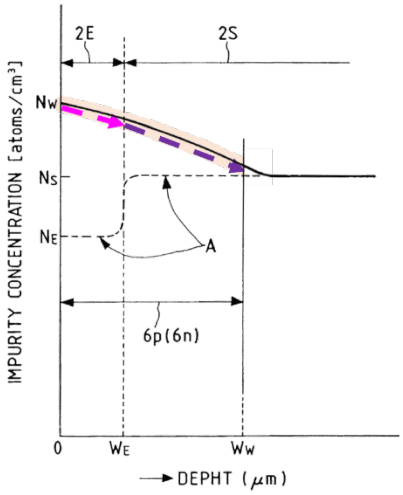


FIG. 17



118. These electric fields are not exhaustive, and a POSITA would understand that numerous fields exist in the diffusion layer to attract minority carriers to the substrate. A POSITA would have understood that Kawagoe's single drift layer has multiple static unidirectional electric drift fields that aid in the movement of minority carriers to the substrate, and that any one of them satisfies the claimed "first static unidirectional electric drift field," *e.g.*, the one depicted in pink over the epitaxial layer.

119. The epitaxial layer (2E) would also have been understood to have the claimed "first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate" because it also has a graded dopant concentration. This is annotated by the pink arrow. For the same reasons described in Kawagoe (Kawagoe at 16:7-11), Kawagoe's graded dopant profile provides a static unidirectional electric field and a POSITA would have understood that a

graded dopant concentration like Kawagoe's provides a first static unidirectional electric drift field.

FIG. 16

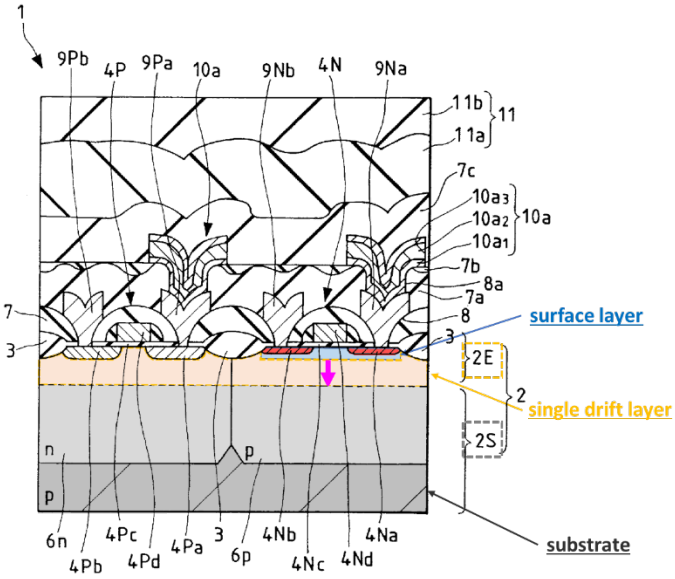
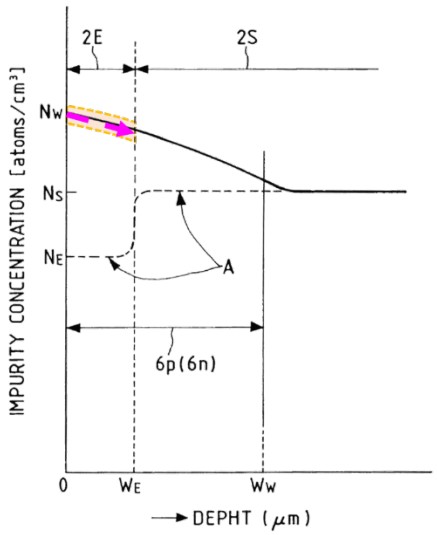


FIG. 17



(vii) Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

120. As depicted below in annotated FIGS. 16 and 17, Kawagoe's single drift layer (the diffusion layer which comprises n and p wells) has at least one well region disposed within it (*e.g.*, the p well). This p-well is part of the diffusion layer and it has a graded dopant concentration. (Kawagoe at 15:62-16:15; *see also id.* at 15:26-36, 17:11-21; *see also id.* at 1:59-2:5, 2:20-23, 15:62-16:15.) And, as described in Element [1.5], this dopant concentration results in static unidirectional electric drift fields. The pink arrow indicates the movement of minority carriers due

to the first static unidirectional electric drift field. The movement of minority carriers due to the second static unidirectional electric drift field is annotated in purple. As depicted below, the well region (green) is disposed within the single drift layer (tan with tanned dashes) and graphically overlaps.

FIG. 16

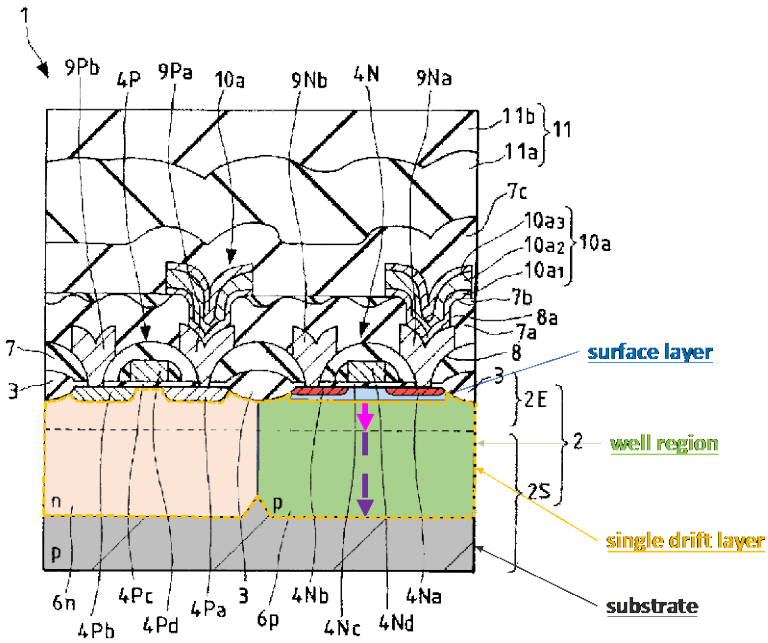
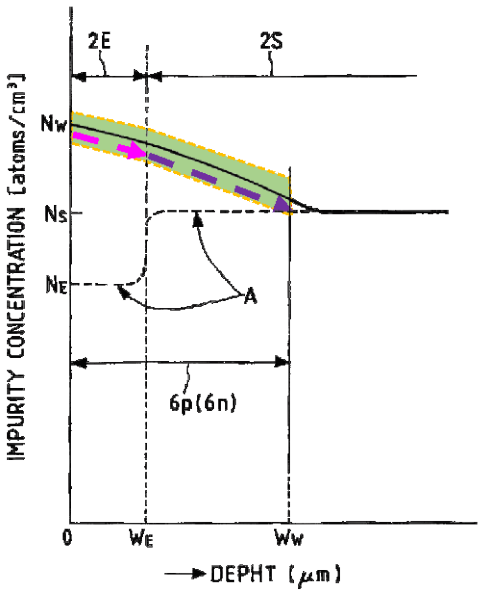


FIG. 17

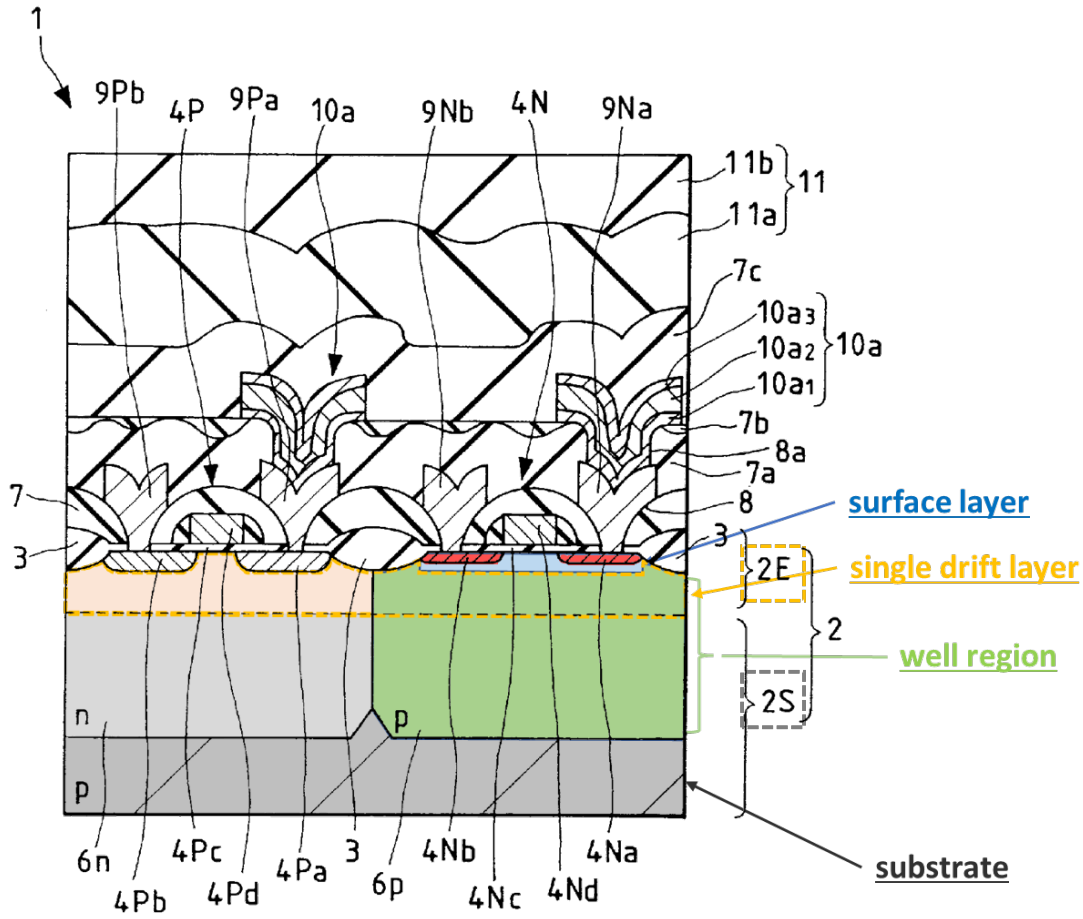


121. In addition, the claimed single drift layer is further rendered obvious even under a narrow construction of that term. This is because Kawagoe's epitaxial layer (2E) by itself renders obvious the claimed "single drift layer" and either the entire substrate layer (2S) or just the portion of layer 2S that does not have a graded doping profile by itself independently renders obvious the "substrate" limitation.

122. The epitaxial layer (2E) has at least one well region that is disposed in it where the "single drift layer" is annotated in tan and, as can be seen below, the

well region (green) is disposed in the single drift layer and goes into the substrate body 2S (light grey, where the undoped portion is in darker grey).

FIG. 16



123. The above comports with the claim language, which requires that the well region be "disposed in" the "single drift layer," and not that the well region be disposed entirely within the single drift layer.

124. Moreover, the well-region similarly provides a static unidirectional electric drift field for the same reasons described in Element [1.5]. (Kawagoe at 16:62-16, FIG. 17. This is depicted below, where the second static unidirectional

electric drift field aids the movement of minority carriers from said surface layer to said substrate (purple arrow).

FIG. 16

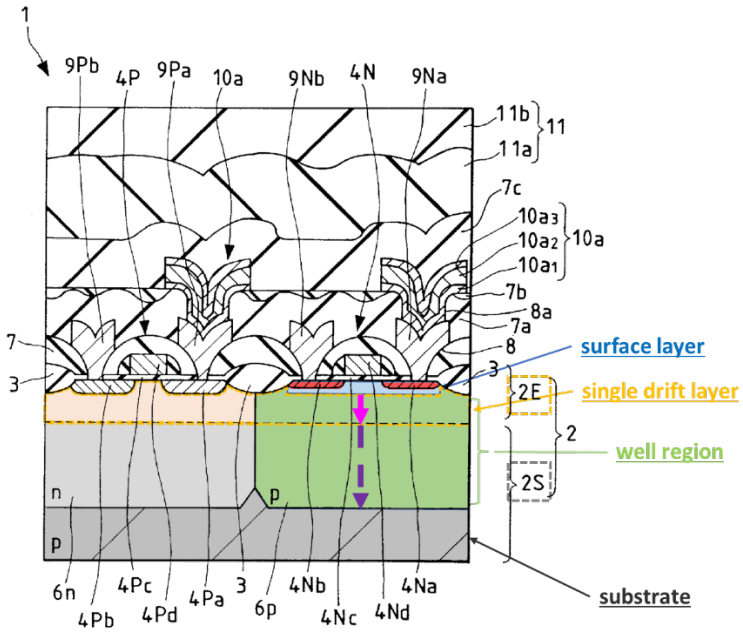
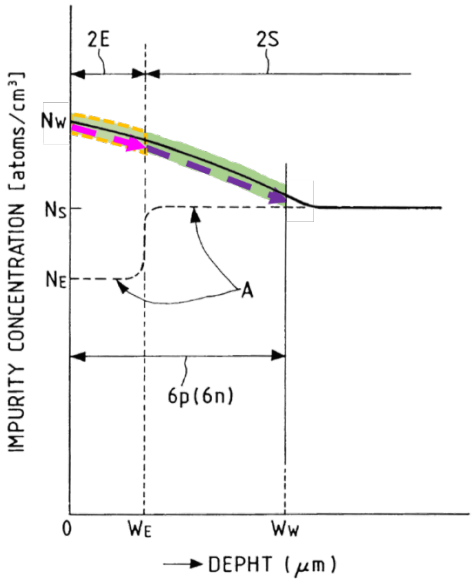
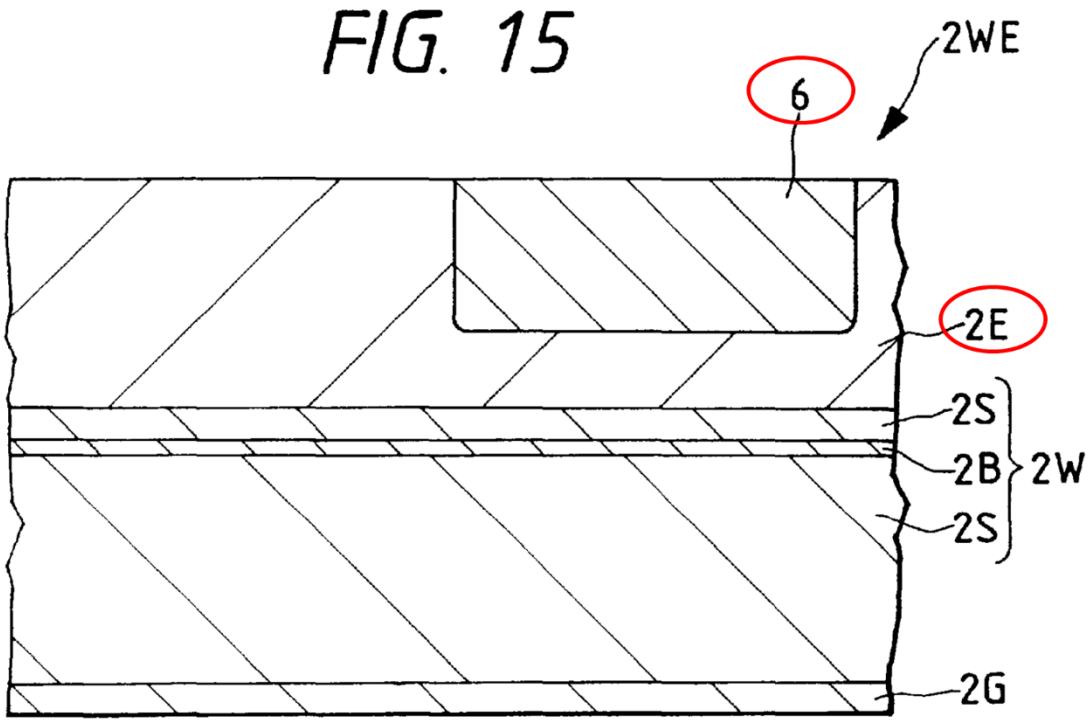


FIG. 17



125. In my opinion, it would have also been obvious for a POSITA to modify Kawagoe's FIG. 16 embodiment to have its well region contained solely within the epitaxial layer, and not extend into the substrate (as is depicted in FIG. 16 and 17). Kawagoe teaches embodiments of thicker epitaxial layers (Kawagoe at 13:49-53) where the n and p well regions are confined within the epitaxial layer, and do not extend to the substrate. (*Id.* at FIG. 15 (excerpted and annotated below).) A POSITA would have known that an epitaxial layer is very commonly grown on a heavily doped substrate which provides a better backside contact. The substrate is typically implanted with a high dose prior to epitaxial growth, however, the heavily doped

wafers are expensive and tend to have higher defect concentrations. Further, if the well doping extended into the heavily doped region on the surface of the substrate, it would be overwhelmed by the substrate doping. Thus, it was beneficial and even more obvious to confine the well regions to the epitaxial layer.



126. Kawagoe further teaches a gradient whose "impurity concentration gradually lowered depthwise of said epitaxial layer" (Kawagoe at Abstract) and that the "impurity concentration [is] gradually lowered ***depthwise of said semiconductor single crystal layer***." (*Id.* at 3:22-23 (emphasis added); *see also id.* at 2:59-61 (making clear that the "semiconductor single crystal layer" is the epitaxial layer over the substrate).) Kawagoe thusly teaches a well region within the epitaxial layer. A POSITA would have found it obvious to apply these teachings to modify the above-

described FIG. 16 of Kawagoe to have the well region exist within the epitaxial layer (and not extend into the substrate), because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. *See, e.g., KSR*, 550 U.S. at 418. It would have been obvious to try; Kawagoe teaches that a POSITA has a degree of freedom for setting the impurity concentration and depth of its layers. (Kawagoe at 25:10-14.) A POSITA would have recognized this degree of freedom in creating layer depths, and would have found it an obvious variant to create the depth of the well region to be confined within the epitaxial layer and not extend into the substrate according to Kawagoe's other embodiments. (*See, e.g., id.* at 2:59-61, 3:22-23, 13:49-53, FIG. 16.) This would have been a simple and beneficial substitution that would have produced better and predictable results: a POSITA would understand that Kawagoe's well region, if it went up to but not into the substrate, would achieve a goal of Kawagoe (*i.e.,* attracting the minority carriers to the substrate without being overwhelmed by the substrate doping, *id.* at 16:7-11) and would work for its intended purpose.

b. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

127. The '195 Patent mentions the deeply implanted layer once (*e.g.*, '195 Patent at 3:37-38) and mentions "deep" in another context, sweeping carriers "deep into the substrate." (*Id.* at 3:33-35.) The specification does not discuss the depth of

the "deeply-planted layer" or the process of forming such a layer. However, a POSITA would understand a diffusion layer that goes into the substrate to be "deeply implanted."

128. Kawagoe teaches that its diffusion layer extends into the substrate. As depicted in FIGS. 16 and 17, the diffusion layer is "formed to extend from the surface of the epitaxial layer 2E to the upper portion of the substrate body … [where its] impurity concentration[] [is] gradually lowered in the depthwise direction." (Kawagoe at 15:62-16:4.) The layers of the wafer are originally formed via "ion implantation" (*id.* at 17:32-49) and are annealed to extend the diffusion. (*Id.* at 17:50-54.) As depicted in FIG. 20, the semiconductor wafer has two layers with one being substrate 2S (annotated red) and, after the fabrication process, the diffusion layer extends into 2S (annotated tan in FIG. 21).

FIG. 20

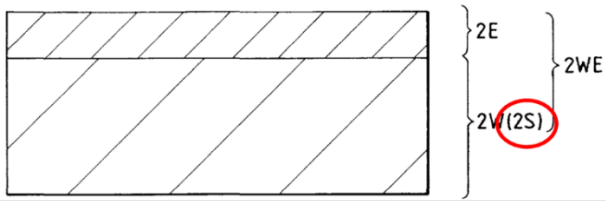
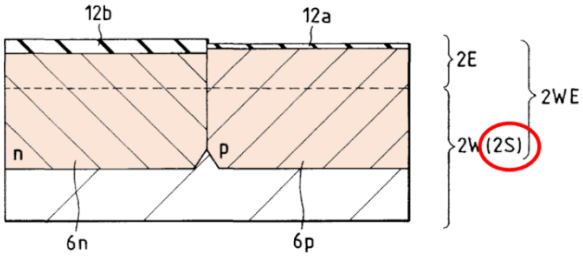


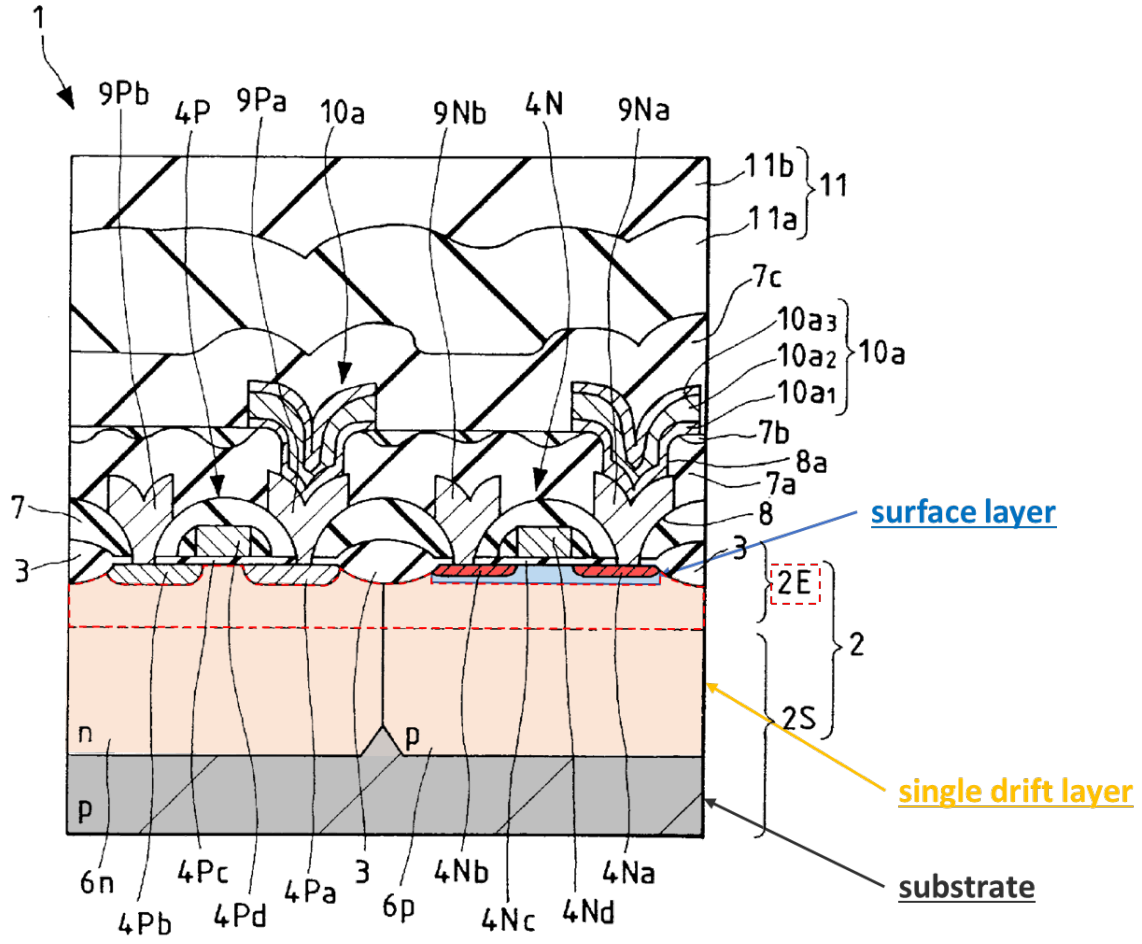
FIG. 21



c. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein the said drift layer is an epitaxial layer."

129. Kawagoe's drift layer includes the epitaxial layer 2E. This is depicted in annotated FIG. 16, below, where the epitaxial layer 2E is depicted as being bounded by the dashed-red border. This teaching renders Claim 3 obvious.

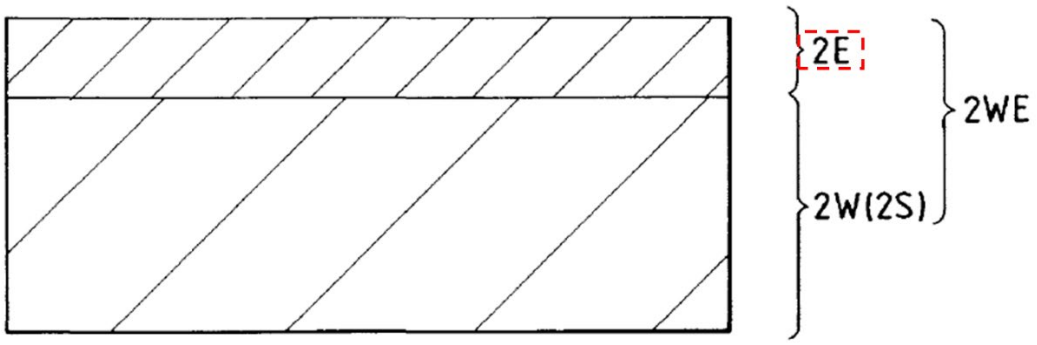
FIG. 16



130. FIG. 20 depicts the epitaxial wafer 2WE (*e.g.*, Kawagoe at 14:23-29 (describing 2WE as the epitaxial wafer)) prior to formation of the graded dopant region. (*Id.* at 14:47-60 (describing FIGS. 20-24 as depicting manufacturing steps

for Embodiment 4.) The epitaxial layer 2E is formed (*id.* at 15:26-36) and thereafter the diffusion layer is formed. (*Id.* at 15:62-16:15.)

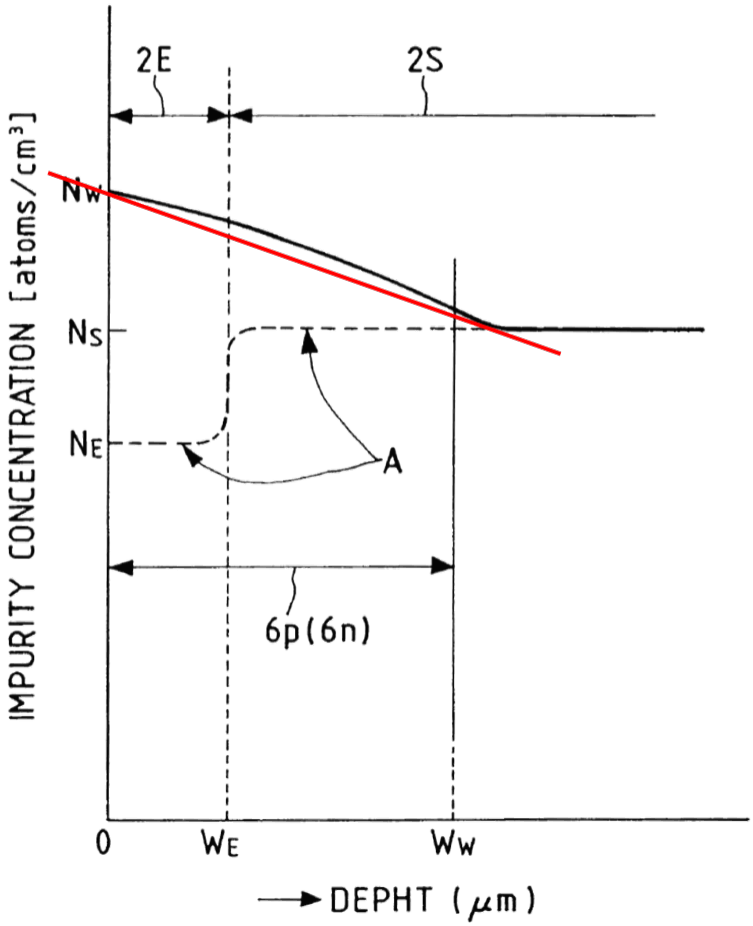
FIG. 20



d. Dependent Claim 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient."

131. FIG. 17 depicts a graded concentration. (Kawagoe at 16:16-40.) However, the vertical axis is not defined. As a result, a POSITA would not be able to discern if FIG. 17 depicts a quasi-linear or exponential gradient. If it is intended to be a linear scale, a linear gradient is depicted in red). As discussed earlier, either type of profile would improve the transport of minority carriers to the substrate.

FIG. 17



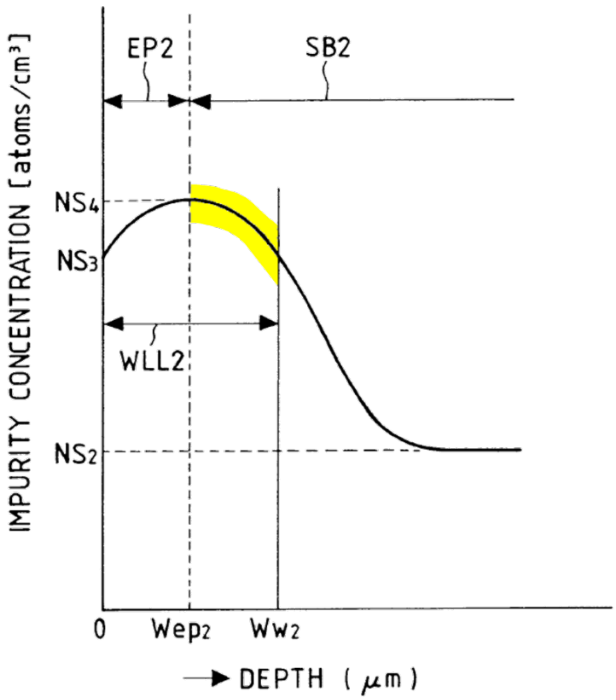
132. Moreover, a POSITA would have also found it obvious to use a quasi-linear gradient because it was a simple usage of one known method. The '195 Patent only mentions quasi-linear gradient once ('195 Patent at 2:40-42) and does not illustrate or otherwise describe it, or describe any process steps for obtaining it confirming that such a gradient was a well-known alternative to a POSITA. It would have been obvious to modify Kawagoe's dopant profile based on the POSITA's

general knowledge in the art to achieve a known quasi-linear gradient. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success.

e. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient."

133. A POSITA would have found it obvious to modify Kawagoe's diffusion profile depicted in FIG. 17 to be exponential in view of Kawagoe's teachings. Kawagoe depicts an exponentially downward dopant gradient for the well region (within the substrate) in FIG. 19. (Kawagoe at 16:62-17:10; *see also id.* at 1:58-65.) As can be seen below, the rate of downward progression starts slowly then increases as depth increases, which a POSITA would understand to be an exponential decrease.

FIG. 19
PRIOR ART



134. Moreover, a POSITA would have found it obvious to use an exponential gradient instead of, for example, a linear or quasi-linear gradient, because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. The '195 Patent only mentions "exponential" gradient once and does not illustrate or otherwise describe it, or describe any process steps for obtaining it, thus confirming that it was a well-known alternative to a POSITA. ('195 Patent at 2:40-42.)

135. Moreover, Kawagoe recognizes an exponential downward gradient as a known technique (Kawagoe at 16:62-17:10), and further recognizes that a downward gradient causes minority carriers to drift from the surface to the substrate.

(*Id.* at 15:62-16:15.) It would have been obvious to modify Kawagoe's graded-dopant profile based on the POSITA's general knowledge in the art to achieve a known exponential gradient. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success.

C. '222 Patent

1. Ground I: Onoda Renders Obvious Claim 44.

a. Independent Claim 44

(i) Preamble: "A CMOS Semiconductor device comprising:"

136. Claim 44, preamble, is substantively identical to claim 1 of the '195 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [44.1]: "a surface layer;"

137. Claim 44, Element [44.1], is substantively identical to claim 1, Element [1.1] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [44.2]: "a substrate;"

138. Claim 44, Element [44.2], is substantively identical to claim 1, Element [1.2] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [44.3]: "an active region including a source and a drain, disposed on one surface of the surface layer;"

139. Claim 44, Element [44.3], is substantively identical to claim 1, Element [1.3] of the '195 Patent and is disclosed for the same reasons I described above for that element.

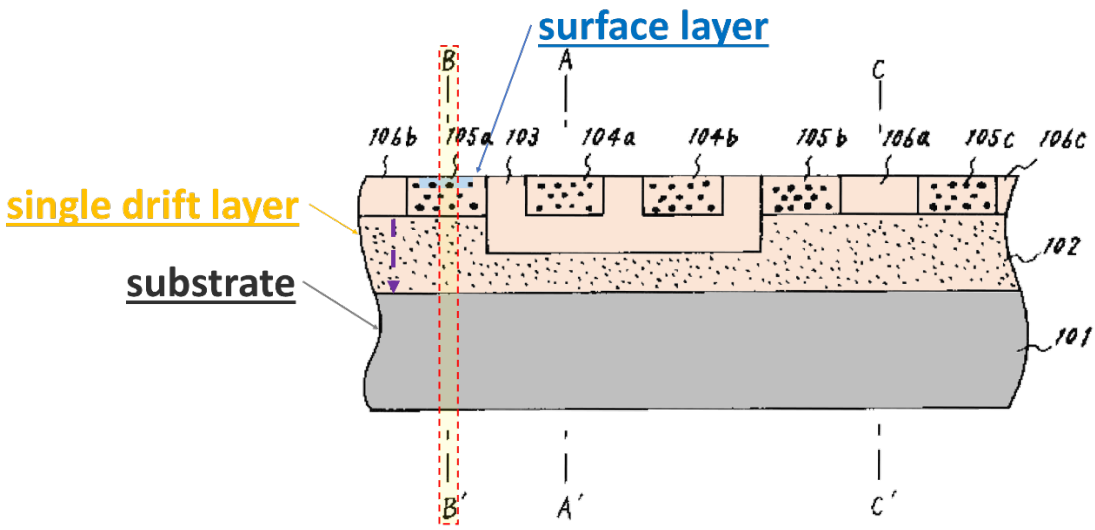
(v) Element [44.4]: "a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,"

140. Claim 44, Element [44.4], is substantively identical to claim 1, Element [1.4] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [44.5]: "the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and"

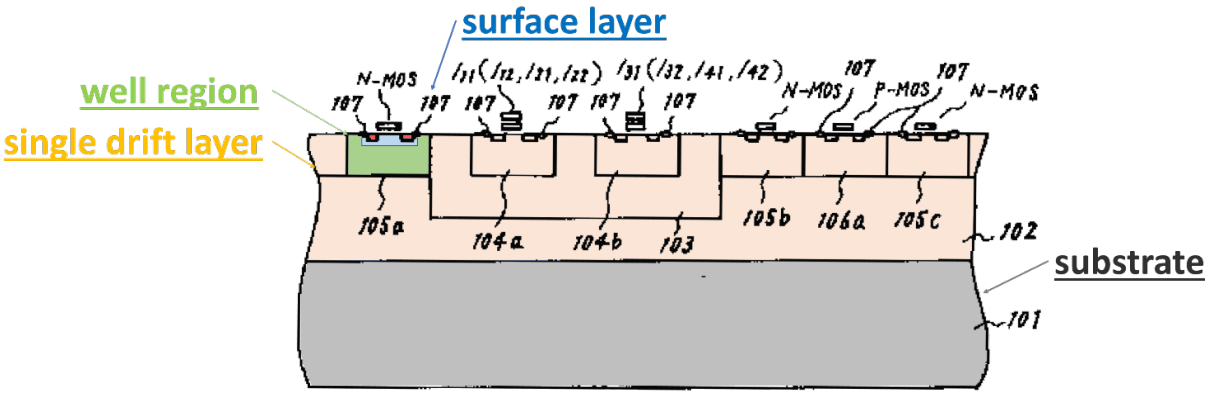
141. Claim 44, Element [44.5], is substantively identical to claim 1, Element [1.5] of the '195 Patent but recites "to an area of the substrate where there are no

active regions" instead of simply "substrate." As can be seen from the below, there are no active regions in the area of the substrate.



(vii) Element [44.6]: "at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions."

142. Claim 44, Element [44.6], is substantively identical to claim 1, Element [1.6] of the '195 Patent but recites "to an area of the substrate where there are no active regions" instead of simply "substrate." As can be seen from the below, there are no active regions in the area of the substrate.



2. Ground II: Onoda in view of Nishizawa Renders Obvious Claim 44.

a. Independent Claim 44

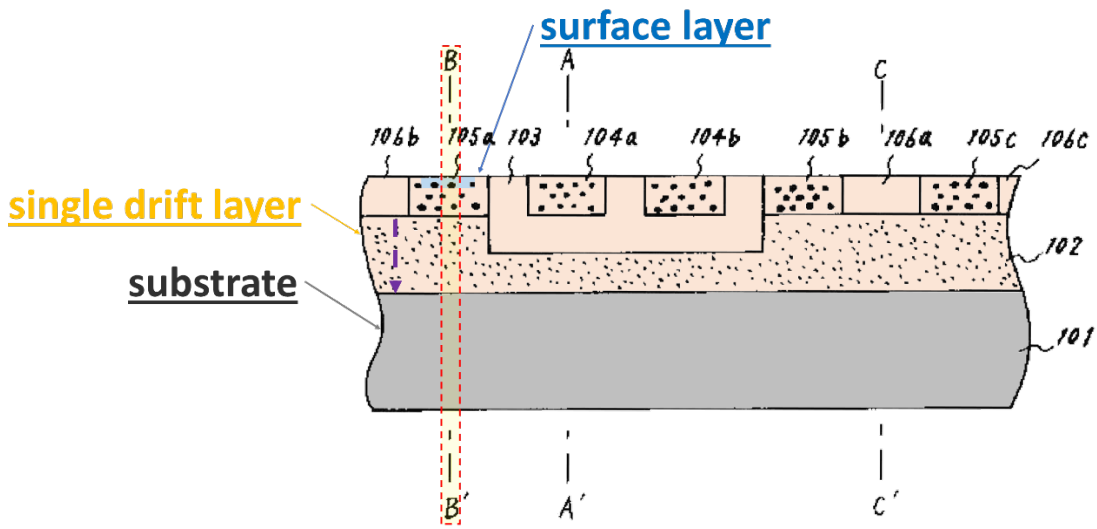
143. I incorporate my analysis regarding the motivation to combine Onoda and Nishizawa as provided for the '195 Patent, Ground II in section III.B.2.

(i) Preamble: "A CMOS Semiconductor device comprising:"

144. Claim 44, preamble, is substantively identical to claim 1 of the '195 Patent and is disclosed for the same reasons I described above for that element.

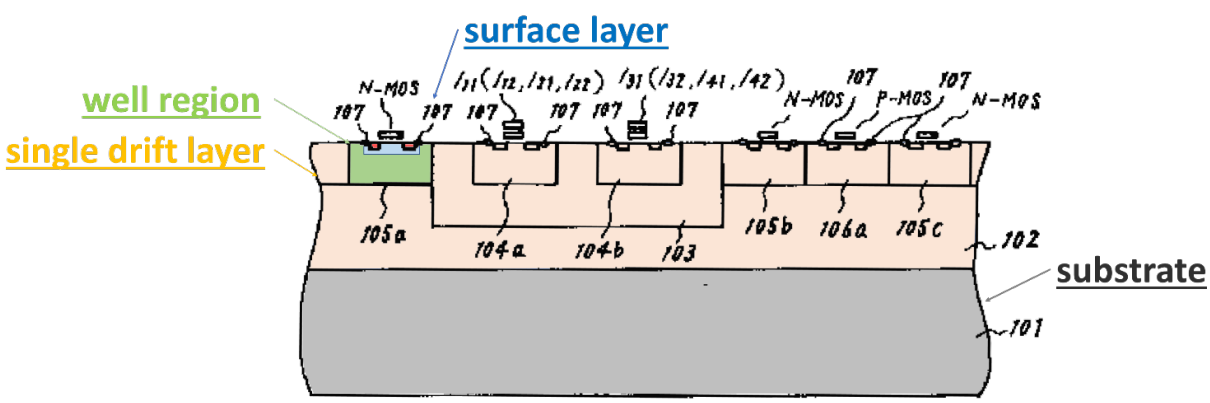
(ii) Element [44.5]: "the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and"

145. Claim 44, Element [44.5], is substantively identical to claim 1, Element [1.5] of the '195 Patent but recites "to an area of the substrate where there are no active regions" instead of simply "substrate." As can be seen from the below, there are no active regions in the area of the substrate.



(iii) Element [44.6]: "at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions."

146. Claim 44, Element [44.6], is substantively identical to claim 1, Element [1.6] of the '195 Patent but recites "to an area of the substrate where there are no active regions" instead of simply "substrate." As can be seen from the below, there are no active regions in the area of the substrate.



3. Ground III: Kawagoe Renders Obvious Claim 44.

a. Independent Claim 44

(i) Preamble: "A CMOS Semiconductor device comprising:"

147. Claim 44, preamble, is substantively identical to claim 1 of the '195 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [44.1]: "a surface layer;"

148. Claim 44, Element [44.1], is substantively identical to claim 1, Element [1.1] of the '195 Patent and is disclosed for the same reasons I described above for that element

(iii) Element [44.2]: "a substrate;"

149. Claim 44, Element [44.2], is substantively identical to claim 1, Element [1.2] of the '195 Patent and is disclosed for the same reasons I described above for that element

(iv) Element [44.3]: "an active region including a source and a drain, disposed on one surface of the surface layer;"

150. Claim 44, Element [44.3], is substantively identical to claim 1, Element [1.3] of the '195 Patent and is disclosed for the same reasons I described above for that element

(v) Element [44.4]: "a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,"

151. Claim 44, Element [44.4], is substantively identical to claim 1, Element [1.4] of the '195 Patent and is disclosed for the same reasons I described above for that element

(vi) Element [44.5]: "the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and"

152. Claim 44, Element [44.5], is substantively identical to claim 1, Element [1.5] of the '195 Patent but recites "to an area of the substrate where there are no active regions" instead of simply "substrate." As can be seen from the below, there are no active regions in the area of the substrate.

FIG. 16

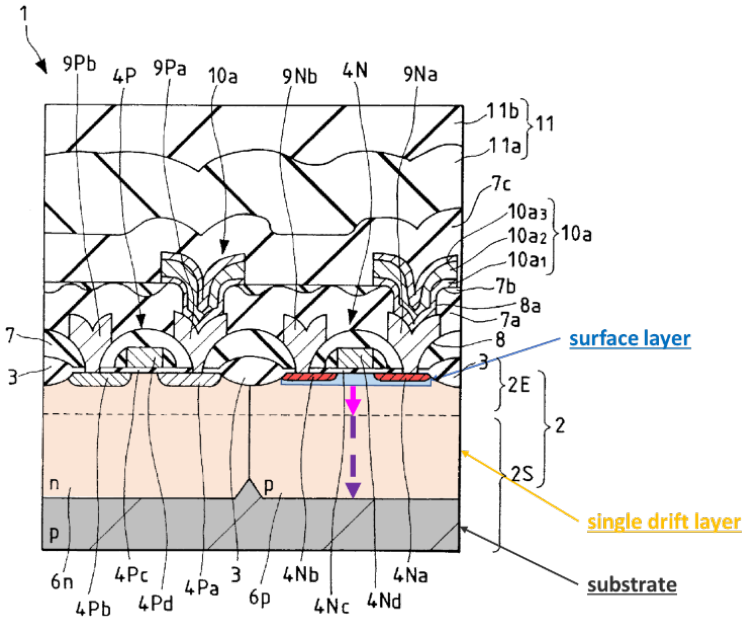
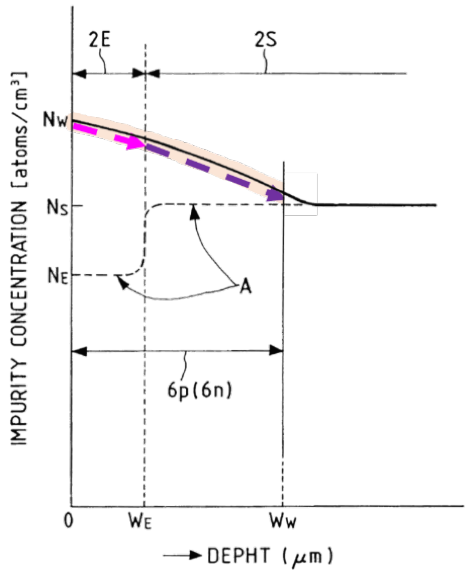


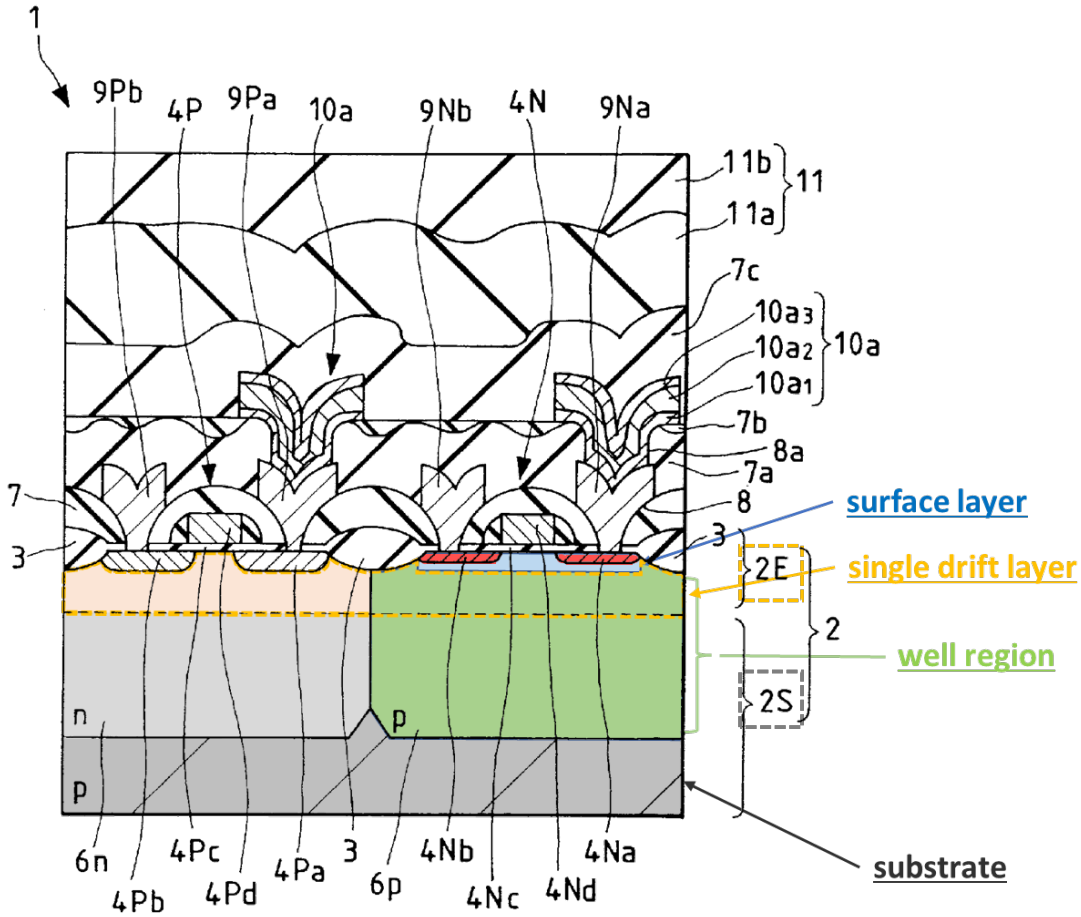
FIG. 17



(vii) Element [44.6]: "at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions."

153. Claim 44, Element [44.6], is substantively identical to claim 1, Element [1.6] of the '195 Patent but recites "to an area of the substrate where there are no active regions" instead of simply "substrate." As can be seen from the below, there are no active regions in the area of the substrate.

FIG. 16



D. '502 Patent

1. Ground I: Onoda Renders Obvious Claims 7-8.

a. Independent Claim 7

(i) Preamble: "A semiconductor device comprising:"

154. Claim 7, preamble, is substantively identical to claim 1 of the '195 Patent and is disclosed for the same reasons I described above for that element. The preamble of the '195 Patent describes a CMOS device, which is a semiconductor device.

(ii) Element [7.1]: "a surface layer;"

155. Claim 7, Element [7.1], is substantively identical to claim 1, Element [1.1] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [7.2]: "a substrate;"

156. Claim 7, Element [7.2], is substantively identical to claim 1, Element [1.2] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [7.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

157. Claim 7, Element [7.3], is substantively identical to claim 1, Element [1.3] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [7.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate,"

158. Claim 7, Element [7.4], is substantively identical to claim 1, Element [1.4] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [7.5]: "said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

159. Claim 7, Element [7.5], is substantively identical to claim 1, Element [1.5] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(vii) Element [7.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

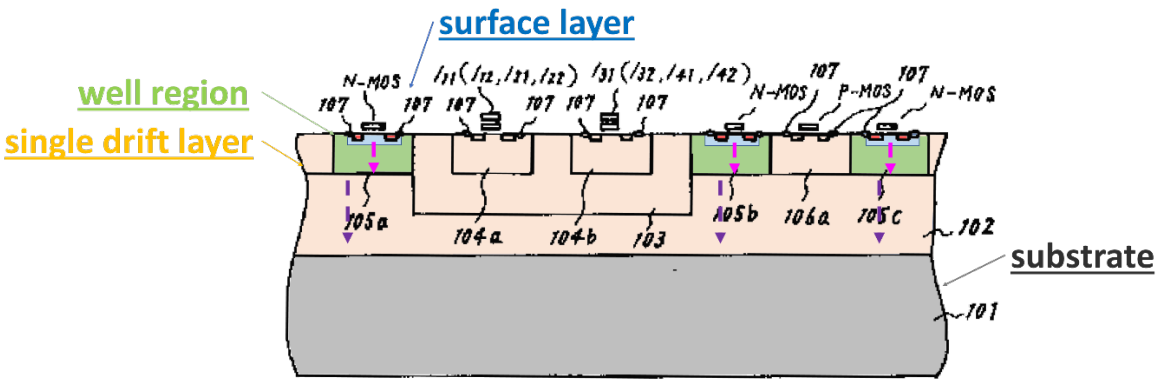
160. Claim 7, Element [7.6], is substantively identical to claim 1, Element [1.6] of the '195 Patent and is disclosed for the same reasons I described above for that element.

b. Dependent Claim 8: "The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions"

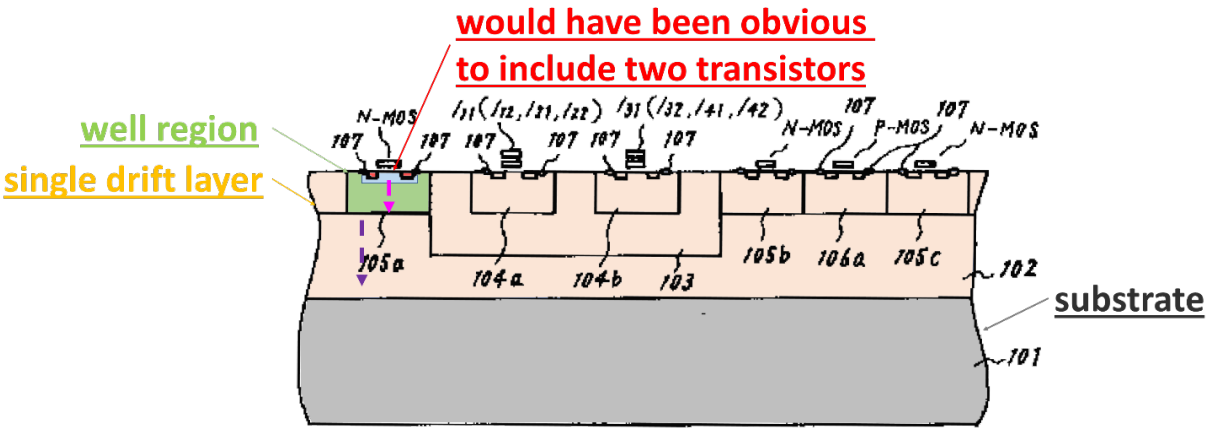
161. Onoda renders obvious this limitation.

162. The second semiconductor layer 102 generates a first static unidirectional electric field that aids the movement of carriers (purple arrow) and well region 105a (dark green) generates a second unidirectional electric field that aids the movement of carriers (pink arrow). This is annotated below in FIG. 3, which

depicts the transistor and active region (red). A POSITA would have understood that each respective well region likewise has a similar doping, and similar electric fields, and would subsequently aid in the movement of carriers for each respective active region.



163. To the extent it is argued that the claims refer to "respective active regions" that must exist in a single well, this would have nonetheless been obvious in view of Onoda. A POSITA would have found it obvious to include two transistors and, consequently, two active regions in a single well region, *e.g.*, well region 105a (green, below).



(Onoda at FIG. 3.)

164. Including multiple transistors—and their associated active regions—in a single well region is suggested by Onoda. Onoda discloses that the "P-type third well region [is] formed in the surface of the second semiconductor layer," and that "at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region." (Onoda at [0009]; *see also id.* at [0054]; (referring to "the plurality of MOS transistors that are formed in" third well region 105a (among other regions)).) P-type well region 105a is a "third well region" (*id.* at Abstract) and Onoda's suggestion to include "some" transistors in that region would have provided a POSITA motivation to include more than one transistor and, consequently, more than one active region in well region 105a (green). Moreover, a POSITA would have been motivated to provide two transistors in a single well region because doing so was well known in the art. A POSITA would have found it commonplace to include multiple active regions in a single well to provide multiple transistors. For example, in a p-type well, a POSITA would have understood that multiple n-p-n transistors could be created by doping n-type regions. Indeed, this is depicted in FIG. 3(d) of the '502 Patent which is labeled as prior art. A POSITA would have accordingly found it obvious to include multiple transistors and active regions in a single well region.

2. Ground II: Onoda in view of Nishizawa Renders Obvious Claims 7-8

165. I incorporate my analysis regarding the motivation to combine Onoda and Nishizawa as provided for the ’195 Patent, Ground II in section III.B.2.

a. Independent Claim 7

(i) Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”

166. Claim 7, Element [7.5], is substantively identical to claim 1, Element [1.5] of the ’195 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [7.6]: “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”

167. Claim 7, Element [7.6], is substantively identical to claim 1, Element [1.6] of the ’195 Patent and is disclosed for the same reasons I described above for that element.

3. Ground III: Kawagoe Renders Obvious Claims 7-8.

a. Independent Claim 7

(i) Preamble: "A semiconductor device:"

168. Claim 7, preamble, is substantively identical to claim 1 of the '195 Patent and is disclosed for the same reasons I described above for that element. The preamble of the '195 Patent describes a CMOS device, which is a semiconductor device.

(ii) Element [7.1]: "a surface layer;"

169. Claim 7, Element [7.1], is substantively identical to claim 1, Element [1.1] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [7.2]: "a substrate;"

170. Claim 7, Element [7.2], is substantively identical to claim 1, Element [1.2] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [7.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

171. Claim 7, Element [7.3], is substantively identical to claim 1, Element [1.3] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [7.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate,"

172. Claim 7, Element [7.4], is substantively identical to claim 1, Element [1.4] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [7.5]: "said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

173. Claim 7, Element [7.5], is substantively identical to claim 1, Element [1.5] of the '195 Patent and is disclosed for the same reasons I described above for that element.

(vii) Element [7.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

174. Claim 7, Element [7.6], is substantively identical to claim 1, Element [1.6] of the '195 Patent and is disclosed for the same reasons I described above for that element.

b. Dependent Claim 8: "The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions."

175. Kawagoe's diffusion layer generates a first static unidirectional electric field that aids the movement of carriers (pink arrow) and well region 105a (dark green) generates a second unidirectional electric field that aids the movement of carriers (purple arrow). This is annotated below in FIG. 3, which depicts the transistor and active region (red). A POSITA would have understood that each respective well region likewise has a similar doping, and similar electric fields, and would subsequently aid in the movement of carriers for each respective active region.

FIG. 16

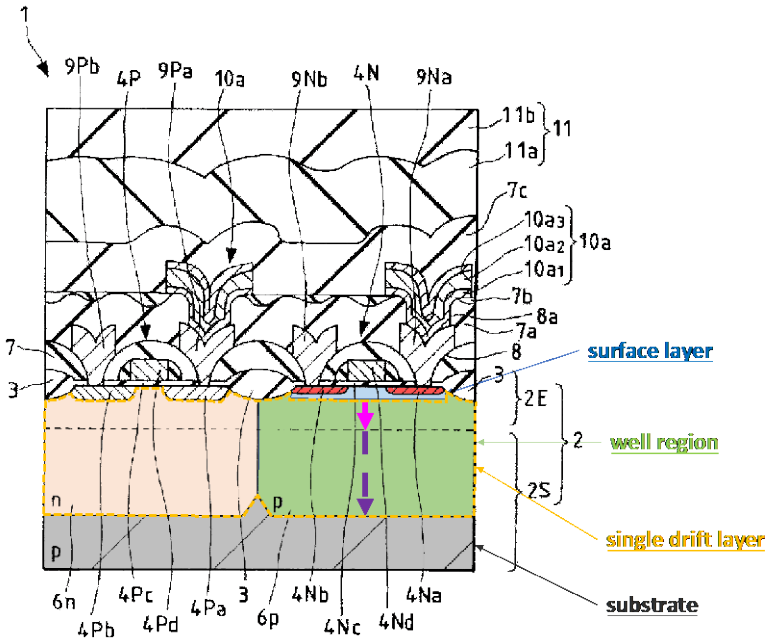
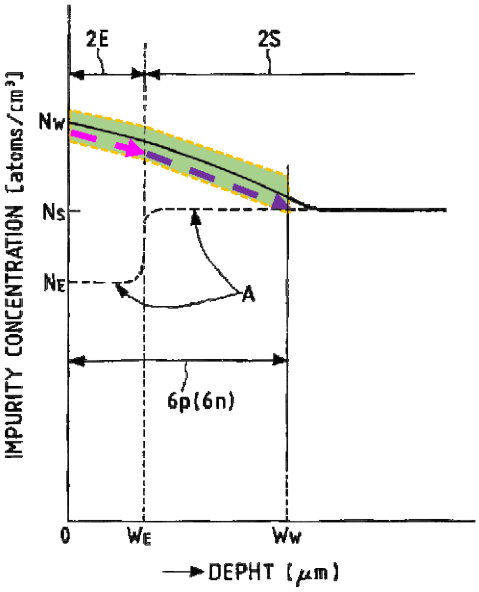
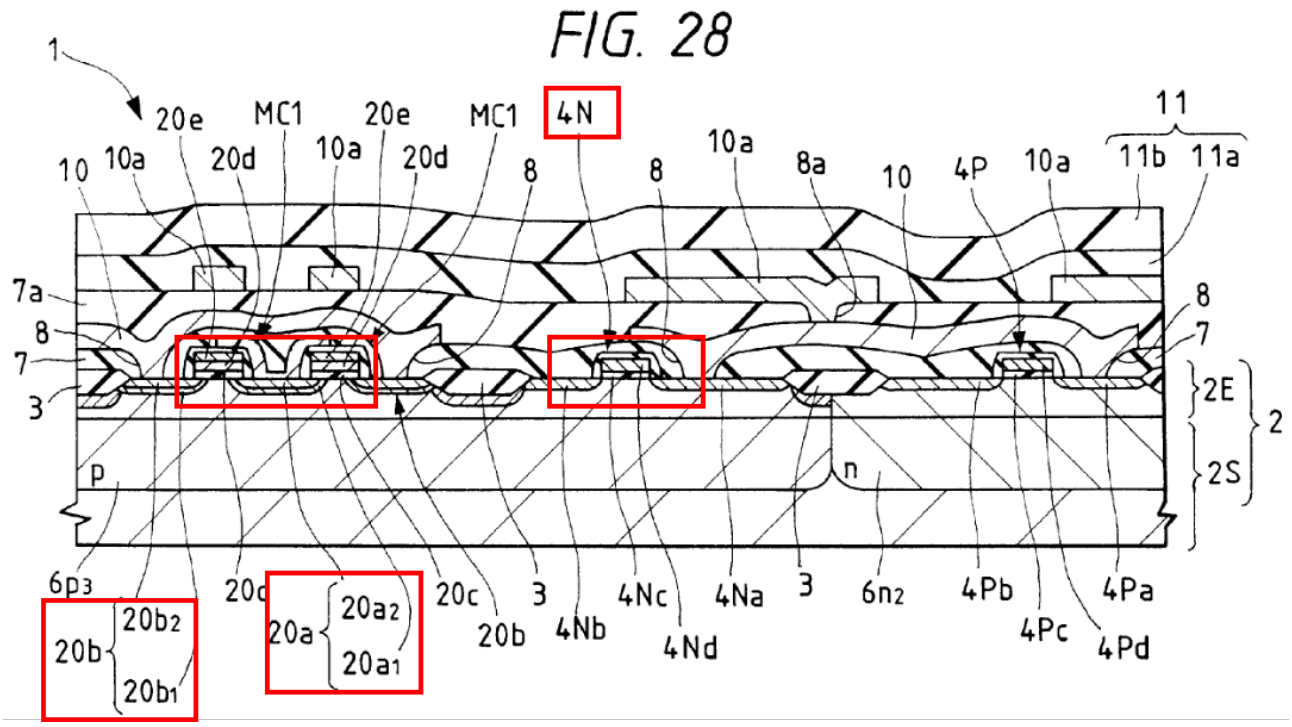


FIG. 17



176. To the extent it is argued that the claims refer to "respective active regions" that must exist a single well, this would have nonetheless been obvious in view of Kawagoe's teachings. Kawagoe teaches an embodiment (*e.g.*, FIG. 28) where multiple active regions (annotated in red) are formed within a single p type layer (p-well 6p3). Like Kawagoe's other embodiments, the "impurity concentrations [of FIG. 28] are made gradually lower depthwise of the semiconductor region 2, as in the foregoing embodiment 4." (Kawagoe at 22:22-29.) This region has several semiconductor regions (20a, 20b, and 4n (all red)) providing associated active regions. (*Id.* at 22:33-38 ("The memory cell MC1 is composed of: a pair of semiconductor regions 20a and 20b formed in the upper portion of the p-well 6p3; a gate insulating film 20c formed over the epitaxial layer 2E.; a floating gate electrode 20d formed over the gate insulating film 20c, a control gate electrode 20e formed over the floating gate electrode 20d through the (not-shown) insulating film."); *see also id.* at 22:51-59.)



(Kawagoe at FIG. 28.)

IV. CONCLUSION

177. Based on my review and analysis, it is my opinion that claims 1-3 and 5-6 of the ’195 Patent, claims 7-8 of the ’502 Patent, and claim 44 of the ’222 Patent are invalid as obvious by: (1) Onoda; (2) Nishizawa; and (3) Kawagoe.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001; and further that such willful false statements may jeopardize the validity of the application or any patent issued thereon. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on ___February 2, 2024_____ in __Arden Hills, Minnesota_____.

Stephen Campbell

Stephen Campbell

Curriculum Vitae
Stephen A. Campbell

Educational History

PhD	Physics	Northwestern University	1981
MS	Physics	Northwestern University	1978
BA	Physics	College of St. Thomas	1975

Employment History

1986 – 2023 University of Minnesota
Emeritus Professor
Director, Minnesota Nano Center (1999 – 2021)
Penrose Professorship in Science and Engineering (2015 – 2021)
Bordeau Chair in Electrical and Computer Engineering (2007 - 2015)
Professor of Electrical and Computer Engineering (1998 - Present)
Associate Professor of Electrical Engineering (1992 - 1998)
Assistant Professor of Electrical Engineering (1986 - 1992)
Presidential Young Investigator

Professor Campbell is very active in education, research, and service to the university. In the first, he leads the University's participation in Nano-Link, an NSF sponsored regional center for nanotechnology education at the AAS level. He has designed and implemented a one-semester capstone experience that is considered to be one of the best in the country. Professor Campbell is the author of *Fabrication Engineering at the Micro and Nanoscale*, one of the most widely used textbook on microfabrication. This text has been used in more than 60 US schools as well as many schools in Europe and Asia. After more than a dozen printings, it is now entering its fourth edition. Professor Campbell's teaching experience includes Microfabrication, Semiconductor Devices, Electromagnetic Fields, Analog Electronics, Linear Circuits, Circuits Lab, Senior Design, and Materials and Devices. In research, Professor Campbell is most well-known for pioneering efforts in high permittivity (aka high-k) materials for the gate insulator in deeply scaled MOSFETs. This revolution in transistor design has now been adopted by most of the leading-edge integrated circuit manufacturers. His other current interests include ultra-high-speed MEMS and efficient thin film photovoltaics. Professor Campbell serves as the Minnesota lead for the National Nanotechnology Coordinated Infrastructure (NNCI) network, established by NSF to support nanotechnology research. He directs the University's Nano Center (www.mnc.umn.edu) where has developed funding for many new pieces of equipment including a 2.5 M$ direct write e-beam lithography. Most recently he has been instrumental in developing support for construction of a new Physics and Nanotechnology Building.

1981-86 Sperry (Unisys), Semiconductor Operations
Device Physicist, 1981-83
Manager, MOS Process Development, 1983-84
Manager, Silicon Research, 1984-86

Dr. Campbell held a variety of positions within Sperry relating to the research and development of high-speed silicon devices. He was the principal architect of Sperry's 1.25 micron CMOS technology. Dr. Campbell managed Sperry's silicon research group where he initiated and directed work in 0.5 micron CMOS, laser photochemical deposition, silicon SOI, super self aligned bipolar devices for high speed ECL, polyimide dielectrics, and novel BiMOS design approaches. He also represented Sperry on the Technical Advisory Board of the Semiconductor Research Corporation.

APPENDIX A

Consulting

2019-2021	Wilmer-Hale, Advanced CMOS Litigation
2008:	3M, Optoelectronic Devices
2005-2007	CIMA Nanotech: Nanoparticle materials
2004-2005:	Precision Press: Thin film devices
2003-2004:	Ennovato, Inc. A startup working on novel transistors for thin film displays
1997-2000:	Offered IC fabrication short courses through UC Berkeley and independently
1997	Fusion Semiconductor Developed a design for radiative heating of 300 mm wafers.
1994-96	FSI Corporation Studied effects of wafer cleaning steps on gate oxide quality
1991-93	AG Associates, Modeling and design of rapid thermal processing equipment.
1992, 94	National Science Board, Naval Studies Board (JAST)
1989-92	Institute for Defense Analysis Participant, Defense Sciences Study Group

Professional Activities and Affiliations

Life Fellow, IEEE

Conference Committee, Semiconductor Interface Specialists Conference (2002-2004)

Associate Editor, Journal of Semiconductor Technology and Science (2002- present)

Symposium Organizer, Gate Stacks, Materials Research Society Spring Meeting (MRS), 2000, 2001

Executive Committee and Technical Committee member, Bipolar Circuits and Technology Meeting (IEEE), 1995, 1996, 1997

Symposium Organizer, GeSi and Related Materials, Materials Research Society Spring Meeting (MRS), 1996

Member, Technical Advisory Board, Semiconductor Research Corp, 1983-86

Reviewer

- IEEE Transactions of Electron Devices
- IEEE Electron Device Letters
- Journal of Applied Physics
- Journal of the Electrochemical Society
- Journal of Vacuum Science and Technology

Awards and Honors

Russell J. Penrose Professorship in Science and Engineering (2015)

George W. Taylor Award for Distinguished Service, 2011

Sanford P. and Lenore Edgerton Bordeau Chair in Electrical and Computer Engineering (2007)

Institute of Electrical and Electronic Engineers (IEEE) Fellow 2007

Institute of Technology Distinguished Professor, 2006

George W. Taylor Award for Distinguished Teaching, 2005

IBM University Partnership Award, 1998

Outstanding EE Instructor Award, Inst of Technology Student Board, 1991

Presidential Young Investigator (National Science Foundation) 1989

Engineering Initiation Award (National Science Foundation) 1987

Sperry Outstanding Technical Achievement Award, 1986

President's Fellow, Northwestern University 1976 - 1977

Argonne National Laboratory Research Participant 1978 -1981

APPENDIX A

Graduate Students Advised - Degrees Completed

PhD

1. Abhimanyu Ravinadrath – "High Density Chronic Neural Probes PhDEE 2023.
2. Nezhueyotl Izquierdo – "Thin Film Growth of Black Phosphorus and Black Arsenic Phosphorus" (MatSci), September 2020.
3. Tim Bontrager – "Optimizing the Interactions Between the Buffer and Barrier Layers for CIGS Based Tandem Photovoltaics", PhDEE February 2019
4. Sehyun Wang – Growth and Characterization of Wide Bandgap CIAGS Solar Cell Material and Devices, PhDEE December 2018
5. Brian Benton – Electronic Transport in Semiconductor Nanocrystal Thin Films – PhDEE May 2018
6. Mandip Sibokati – Electrical Characterization and Device Modeling to Study Degradation Mechanisms in CIAGS Solar Cells– PhDEE June 2017
7. Liyuan Zhang – Earth Abundant CZTS Solar Cells – PhDEE 2016
8. Jun Young Lim – CNT Films and Processing, PhDEE 2015
9. Forrest Johnson – Broken Gap Junctions for Tandem Solar Cells – PhDEE 2015
10. Brijesh Kumar – Modeling of Embedded Quantum Dot Structures PhDEE 2013
11. Sang Ho Song – Characterization and Modeling of PV Devices – PhDEE 2013
12. Dan Yu – Si Nanoparticle Composites – PhDEE 2012
13. Maryam Jalali – An IR Scene Projector – PhDEE 2011
14. Min Woo Jang – Low Mass NEMS Switch – PhDEE 2011
15. Richard Liptak – Passivation of Si Nanoparticles – PhDEE 2009
16. Rebeccah Ligman - Si Nanoparticles in Organic LEDs– PhDEE May, 2007
17. Min Li – "Development and Characterization of Ultrathin Hafnium Titinates and High Permittivity Gate Insulators", Oct, 2005
18. Zhihong Zhang – "Hafnium Oxide gate Dielectrics for Deeply Scaled MOSFETs", Oct 2005
19. Ying Dong – Devices Made on Single Crystal Silicon Nanoparticles" – Sept. 2005
20. Zhe Shen – Nano-sized Silicon Particle Formation in Silane HDP", Sept 2004
21. Noel Hoilien – "Zirconium Based High k Materials", PhDEE, May 2004
22. Fang Chen – "Hafnium Based High k Materials", PhDEE Jan 2004
23. Taesung Kim - "Particle Measurement and Transport in SiO_2 CVD and Si HDPCVD", PhDME, March, 2002 (co-advised with Peter McMurry)
24. Tiezong Ma – High Permittivity Materials, PhDEE, August 2001 (co-advised with Wayne Gladfelter)
25. Boyong He – "High Permittivity FETs", March, 2000
26. Sandeep Nijawan - "Particle Measurement and Control in Silane CVD", PhDME, December, 1998 (co-advised with Peter McMurry)
27. David Gilbert - "The Deposition and Characterization of TiO_2 from Titanium Tetrakis Isopropoxide and from Tetrakis Nitrato Titanium", PhD Chem, May, 1998 (co-advised with Wayne Gladfelter)
28. Hyeong Saug Kim - "Electrical Characteristics and Reliability of High Permittivity FETs", PhDEE, March, 1998
29. Richard Tran - "GeSi Based Microwave ICs", July, 1995
30. Jinhua Yan - "High ε Dielectrics for MOS Transistors", March, 1995
31. John Leighton - "Rapid Thermal Vapor Phase Epitaxy - A Technique for Growing Thin Films of Silicon and Germanium-Silicon on Silicon", April, 1994
32. Karson Knutson - "Modeling of the Thermal Uniformity and Gas Phase Reactions in a Rapid Thermal Epitaxy System", August, 1993
33. Weihua Liu - "Performance of Deep Submicron GeSi Devices", June, 1993
34. Kyungho Lee - "Radiation Damage in Ultra Thin Dielectric Layers", May, 1993

APPENDIX A

MSEE

1. Maryam Jalali – A Restricted Channel Gas Sensor - January 2009
2. Gagan Aggrawal – Optical Transistor – August 2008
3. Richard Liptak – Passivation of Silicon Nanoparticles – August 2006
4. Bek Ligman – Nanoparticle LEDs June 2006
5. Dan Yu – CVD of SrHfO3 – MSEE, May, 2006
6. Niles Graf– Fine Alignment of an E-Beam Lithography System – MSEE, April, 2005
7. Paul Chen – CVD of Ternary High-k Materials MSEE May, 2005
8. Sharon Hilchie – "Si Nanoparticle Processing" MSEE, September 2004
9. Bek Ligman – "A Fine Comb Structure for Integrated Gas Sensors", MSEE, May 2004
10. Ying Dong – "Formation of Single Crystal Si Nanoparticles", MSEE, September 2003
11. Xiaorong Shi – "UHV Nitrides", MSEE, March 2003
12. Fang Chen – "Deposition of Titanium Nitride", MSEE June 2002
13. Henry Utomo – "A Control System for an ALD Reactor", MSEE June, 2001
14. Robert Rassel – "Particle Formation During Low-Pressure Chemical Vapor Deposition Of Silicon Dioxide From Silane And Oxygen: Measurement And Film Properties", MSEE June, 2001
15. Richard Rassel – "A Solenoid Type Microtransformer and Its Fabrication", MSEE June 2001
16. Mark Shriver – "UHV Nitridization", MSEE April, 2001
17. Hans Christianson "High Resistance Silicon Devices", MSEE March, 1999
18. Zhang Wu - Ultrafine Particle Control in Tungsten CVD, MSEE, May, 1998
19. Rongshan Wang - Semi-insulating Silicon, MSEE, April, 1998
20. Ray Tan – "High Resistance Silicon", MSEE, April, 1997
21. Bret Schwab - Effects of Surface Preparation on MOS Reliability, MSEE, July, 1996
22. Jay Meyer - Production and Performance of Semi-Insulating Silicon, MSEE, June, 1996
23. Hyeong Saug Kim - "Reliability of Ultrathin SiO_2", MSEE, May, 1994
24. Kai Ping Liu - Charge Pumping Measurements of Silicon MOSFETs, MSEE, February, 1992
25. Martin Kale - "Spreading Resistance Depth Profiling", MSEE, October 1991
26. Gregory Case - "Detection of Defects in Integrated Circuit Interconnects", MSEE, July, 1991
27. Karson Knutson - "Numerical Analysis of Rapid Thermal Processing", MSEE, April, 1991
28. Kyungho Lee - "Wafer Level Reliability Tests of IC's", MSEE, March, 1991
29. Kaseem Hamze - "Temperature Dependence of GeSi Mobility", January, 1991
30. Ling Shang - Particles in LPCVD Silicon Nitride", October, 1990
31. John Leighton - "Rapid Thermal Vapor Phase Epitaxy", November, 1989
32. Steve Guccione - "DC MOSFET Parameter Extraction", May, 1989

APPENDIX A

Synopsis of Research Accomplishments
Director, Minnesota Nano Center

Over the period 9/99 to the present, Professor Campbell has served as the Director of the MicroTechnology Lab, which changed its name in 2003 to the NanoFabrication Center. With a staff of 14 permanent employees and an annual budget of approximately 1.9 M$, the NFC has as its charter to act as a central resource at the University for all work involving the fabrication of micro and nano structures. The Lab is heavily used by many Departments at the University including EE, CEMS, ME, Physics, Chemistry, Plant Biology, Cellular Biology, and Biomedical Engineering. In addition, the Lab hosts outside users including many companies and researchers from other institutions.

During the period of Professor Campbell's appointment, the Lab upgraded its facilities considerably. One of the major accomplishments was the addition of a nanotechnology capability. Professor Campbell led the acquisition of a direct write electron beam lithography system and ultimately to a state of the art, 6 nm Vistec system. This machine has been widely adopted by academic users and has been augmented by a nano imprint tool. Lithography capabilities have also expanded with an i-line exposure tool. At the same time the Lab upgraded its sputtering capability, replacing a system built in the 1970's with two state of the art tools which are much better suited to the current faculty needs. Professor Campbell has started new Lab initiatives. As a result of this and other innovative incentive programs, usage of the Lab by University faculty has increased by a factor of five over his tenure. The lab conservatively estimates that these facilities enable approximately 10 M$ of research annually. This growth has led to the development of support for a new building, include a 10,000 square foot (5000 under filter) clean room which will be the primary facility for nano research for current and future University researchers. This building was occupied in late 2013.

Professor Campbell has successfully allied the Laboratory with Stanford, Cornell, and 11 other schools in a successful bid to become the National Nanotechnology Infrastructure Network (NNIN). This activity began in April, 2004, and has been renewed to March 2014. In 2015, Professor Campbell successfully led a team to ensure Minnesota participation in the follow-on NSF program, the National Nanotechnology Coordinated Infrastructure (NNCI) program. NNCI will provide support to critical nano facilities until at least 2020 and, if renewed, until 2025. Professor Campbell has also worked with local community colleges to spearhead a successful bid to develop a new nano education initiative at the 2-year level in a 3+1 format, becoming a regional center in nano education at the AAS level.

APPENDIX A

Synopsis of Research Accomplishments
Thin Film Photovoltaics

Our group is active in the area of thin film PV, particularly CIGS and related materials. We have built a molecular beam epitaxy system for depositing these films in an oxygen-free ambient. We are currently working on the development of tandem CIGS devices using the wide bandgap absorber material CIAGS and on improving the efficiency of the earth-abundant absorber CZTS. Supporting this work is 2D device modeling using DESIS, and a wide variety of characterization equipment including DLTS, photocapacitance spectroscopy, and a novel technique that we have developed to distinguish interface from bulk traps in these devices.

Papers (Journal and Conference)

1. Sreejith Karthikeyan, Sehyun Hwang, Mandip Sibakoti, Timothy Bontrager, Richard W. Liptak, Stephen A. Campbell, "Effect of rapid thermal annealing of Copper Indium Aluminium Gallium diSelenide device and its deposition challenges", Applied Surface Science **493**, pp. 105-111 (2019) https://doi.org/10.1016/j.apsusc.2019.06.279.

2. A High Stability Near-Broken Gap Junction for Multijunction Photovoltaics, Forrest Johnson, Joel Pankow, Glenn Teeter, Brian Benton, and Stephen A. Campbell, JVST A **37**(1) 011201 (2019).

3. Sreejith Karthikeyan, Liyuan Zhang, Sehyun Hwang, and Stephen A. Campbell, Experimental scheme for a stable molybdenum bilayer back contacts for photovoltaic applications" Applied Surface Science **449**, Pages 647-653 (2018).

4. Mandip Jung Sibakoti, Sreejith Karthikeyan1, Sehyun Hwang, Timothy Bontrager, Stephen Campbell, "Defects in Copper Indium Gallium Aluminum Diselenide (CIAGS) Films and their Impact on Photovoltaic Device Performance" Proceedings of the Spring 2017 Materials Research Conference.

5. "Interface Characterization and Modeling of CIAGS Devices", Mandip J. Sibakoti, Sreejith Karthikeyan, Sehyun Hwang, Timothy Bontrager and Stephen A. Campbell, Proceedings of the 42nd IEEE Photovoltaic Specialist Conference, Portland (2016).

6. "Cu_2ZnSnS_4 thin film growth optimization and post rapid thermal annealing of solar cells and its influence on device performance", Liyuan Zhang, Sreejith Karthikeyan, Mandip J. Sibakoti, Stephen A. Campbell, Proceedings of the 41st IEEE Photovoltaic Specialist Conference (2015).

7. "Metal Oxide Broken Gap Tunnel Junction for Copper Indium Gallium Diselenide Tandem Solar Cells", Sang Ho Song, Eray Aydil, and Stephen A. Campbell, Solar Energy Materials and Solar Cells Vol. 133C (2015) pp. 133-142 DOI 10.1016/j.solmat.2014.10.046.

8. "Sputtered Metal Oxide Broken Gap Junctions for Tandem Solar Cells", Forrest Johnson, Sang Ho Song, Joel Abrahamson, Richard Liptak, Boris Chernomordik, Eray Aydil, and Stephen A. Campbell, Solar Energy Materials and Solar Cells Vol. 132C (2015) pp. 515 522 DOI 10.1016/j.solmat.2014.09.042.

9. "Atomic Layer Deposition of Tin Oxide and Zinc Tin Oxide Using Tetraethyltin and Ozone", Ellis J Warner, Forrest Johnson , Stephen A. Campbell, and Wayne L.

Gladfelter, J. Vac. Sci. Technol. A 33, pp. 021517-1 to 021517-7 (2015). DOI: 10.1116/1.4907562.

10. "Challenges in deposition of wide band gap copper indium aluminum gallium selenide (CIAGS) thin films for tandem solar cells", Sreejith Karthikeyan, Mandip Sibakoti, Richard Liptak, Sang Ho Song, Joel Abrahamson, Eray S. Aydil and Stephen A. Campbell, 40th IEEE Photovoltaic Specialist Conference (2014).

11. "In-situ stress and thermal stability studies of molybdenum bilayer back contacts for photovoltaic applications", Sreejith Karthikeyan, Liyuan Zhang and Stephen A. Campbell, 40th IEEE Photovoltaic Specialist Conference (2014).

12. "Sputtered Metal Oxide Broken Gap Junctions", Stephen Campbell, Forrest Johnson, Sreejith Karthikeyan, Sang-Ho Song, Richard Liptak, Brian Benton, Proc of the Spring Meeting of the Electrochemical Society Orlando (2014).

13. "In-situ stress and thermal stability studies of molybdenum bilayer back contacts for photovoltaic applications", Sreejith Karthikeyan, Liyuan Zhang and Stephen A. Campbell, accepted for publication, IEEE J. Photovoltaics (2014).

14. "Heteroepitaxy and the performance of CIGS solar cells", Sang Ho Song and Stephen A. Campbell, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

15. "Synthesis and Structural Characterization of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Sreejith Karthikeyan,and Stephen A. Campbell, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

16. "Sputtering of Metal Oxide Tunnel Junctions for Tandem Solar Cells", Forrest Johnson, Sang Ho Song, Richard Liptak, and Stephen A. Campbell, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

17. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher Cheng, Stephen A. Campbell, Eray S. Aydil, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

18. "A low temperature, single step, pulsed d.c magnetron sputtering technique for copper indium gallium diselenide photovoltaic absorber layers", Sreejith Karthikeyan, Kushagra Nagaich, Arthur E Hill, Richard D Pilkington, and Stephen A Campbell, Proceedings of the Spring Meeting of the MRS **1538** (2013) doi.org/10.1557/opl.2013.1008

19. "Tin dioxide as an alternative window layer for improving the Damp-Heat Stability of Copper Indium Gallium Diselenide Solar Cells", Selin Tosun, Rebekah K. Feist, Stephen A. Campbell and Eray S. Aydil, J. Vac. Sci. Techn. A **30**, 04D101 (2012).

20. "Improving the damp-heat stability of copper indium gallium diselenide solar cells with a semicrystalline tin dioxide overlayer", Tosun, B.S.; Feist, R.K.; Gunawan, A.; Mkhoyan, K.A.; Campbell, S.A.; Aydil, E.S. Solar Energy Mat and Solar Cells 101, p 270-6, (2012).

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K.; Gunawan, Aloysius; Mkhoyan, K. Andre; Campbell, Stephen A.; Aydil, Eray S. Thin Solid Films, v 520, n 7, p 2554-2561, January 31, 2012

22. "Structure and composition of ZnxCd1-xS films synthesized through chemical bath deposition", Tosun, B. Selin; Pettit, Chelsea; Campbell, Stephen A.; Aydil, Eray S. ACS Applied Materials and Interfaces, v 4, n 7, p 3676-3684, July25, 2012

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25. B. S. Tosun, C. Pettit, S. A. Campbell and E. S. Aydil, "Structure and Composition of $Zn_xCd_{1-x}S$ Films Synthesized through Chemical Bath Deposition," *ACS Appl. Mater. Interfaces* **4**, 3676-3684 (2012).

26. "Atomic layer deposition of p-type phosphorus-doped zinc oxide films using diethylzinc, ozone and trimethylphosphite", H. Yuan, B. Luo, S. A. Campbell and W. L. Gladfelter, Electrochem. Solid-State Lett., Volume 14, Issue 5, pp. H181-H183 (2011).

27. "Imaging and phase identification of Cu2ZnSnS4 thin films using confocal Raman spectroscopy", A.-J. Cheng, M. Manno, A. Khare, C. Leighton, S. A. Campbell, and E. S. Aydil, J. Vac. Sci. Tech. v 29, n 5, (2011).

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29. "Sputter Deposition of Amorphous and Nanocrystalline Tin Dioxide Films," B. S. Tosun, R. K. L. Feist, S. A. Campbell and E. S. Aydil, Thin Solid Films **520**, pp. 2554-2561 (2011).

30. "Simultaneous Interface And Bulk Trap Characterization in CIGS Solar Cells", S. H. Song, S. Jeong, E. Aydil, B. Todd R. Feist, R. Haley, and S. A. Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference (2011).

31. "Improving the Damp-Heat Stability of Copper Indium Gallium Diselenide Solar Cells with a Semicrystalline Tin Dioxide Overlayer" Selin Tosun, Rebekah Feist, Stephen A. Campbell, and Eray Aydil, accepted for publication, Solar Energy Materials and Solar Cells (2011).

32. "Wide Band-gap CuIn1-xGaxSe2 based chalcopyrite absorbers for Tandem cell applications", Kushagra Nagaich, Eray Aydil, and Stephen Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference (2011).

33. "An analysis of temperature dependent current-voltage characteristics of Cu2O-ZnO heterojunction solar cells", Seong Ho Song, Sang Ho Song, Kushagra Nagaich, Stephen A. Campbell and Eray S. Aydil, Thin Solid Films v 519, n 19, p 6613-6619, July 29 (2011).

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35. "Structure Optimization for a High Efficiency CIGS Solar Cell", S. H. Song, K. Nagaich, E. Aydil, R. Feist, R. Haley, and S. A. Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference, Honolulu (2010).

Patent

1. "Optoelectronic Devices With Thin Barrier Films With Crystalline Characteristics That Are Conformally Coated Onto Complex Surfaces To Provide Protection Against Moisture", U.S. Provisional Patent Application, Attorney Docket No. 71385, Selin Tosun, Stephen Campbell, Eray Aydil, and Rebekah Feist , Dow Chemical (2012).

Talks

1. **Invited Talk** – "PV Technologies and Outlook: Mostly Sunny with Scattered Clouds", Reforming Electric Energy Systems Curriculum with Emphasis on Sustainability Workshop, National Academy of Engineering and NSF, Washington DC (2015).

2. **Invited Talk** – "Solar Outlook for Minnesota", Minnesota Power Systems Conference, Minneapolis (2014).

3. **Invited Talk** – "Transparent Metal Oxides for Tunnel Junctions", Spring Meeting of the Electrochemical Society Orlando (2014).

4. **Invited Talk** – "The Future of Solar Energy", Upper Midwest Power Conference, Pine City Minnesota (2014).

5. "Heteroepitaxy and the performance of CIGS solar cells", Sang Ho Song and Stephen A. Campbell, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

6. "Synthesis and Structural Characterizations of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Sreejith Karthikeyan,and Stephen A. Campbell, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

7. "Sputtering of Metal Oxide Tunnel Junctions for Tandem Solar Cells", Forrest Johnson, Sang Ho Song, Richard Liptak, and Stephen A. Campbell, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

8. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher

Cheng, Stephen A. Campbell, Eray S. Aydil, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

9. "A low temperature, single step, pulsed d.c magnetron sputtering technique for copper indium gallium diselenide photovoltaic absorber layers", Sreejith Karthikeyan, Kushagra Nagaich, Arthur E Hill, Richard D Pilkington, and Stephen A Campbell, Proceedings of the Spring Meeting of the MRS (April, 2013)

10. "Continuous-Flow Chemical Bath Deposition of ZnxCd1-xS Thin Films For Chalcopyrite Solar Cells", Selin Tosun, Joel Abrahamson, Aloysius Gunawan, K. Andre Mkhoyan, Stephen A. Campbell and Eray S. Aydil, AVS Fall Meeting 2013.

11. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher Cheng, Stephen A. Campbell, Eray S. Aydil, 39th IEEE Photovoltaic Specialist Conference (2013).

12. "Copper Indium Aluminum Gallium diSelenide as a Potential Wide band-gap Absorber for CIGS based Tandem Photovoltaic Cells", Kushagra Nagaich*, Sreejith Karthikeyan* and Stephen A. Campbell, Spring meeting of the MRS (2013)

13. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher Cheng, Stephen A. Campbell and Eray S. Aydil. Photo Voltaics Spec Conf (2013).

14. "Synthesis and Structural Characterizations of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Xin Zhang, Sreejith Karthikeyan, Stephen A. Campbell, Photo Voltaics Spec Conf (2013).

15. "Sputtering of Metal Oxide Tunnel Junctions for Tandem Solar Cell Applications", Forrest Johnson, Sang Ho Song, Ricard Liptak, Boris XXX, Eray Aydil, Stephen A. Campbell, Photo Voltaics Spec Conf (2013).

16. "Deposition and Structural Characterizations of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Xin Zhang, Michael Manno, Melissa Johnson, Eray Aydil, Chris Leighton, Stephen Campbell, Minneapolis AVS Sectional Meeting Fall 2012.

17. "Electrical scanning probe microscopy of thin films for CIGS-based solar cells", Joel T. Abrahamson, B. Selin Tosun, Forrest Johnson, Greg Haugstad, Stephen A. Campbell, and Eray S. Aydil, Spring ACS (2013).

18. "Copper Indium Aluminum Gallium diSelenide as a Potential Wide band-gap Absorber for CIGS based Tandem Photovoltaic Cells", Kushagra Nagaich, Sreejith Karthikeyan and Stephen A. Campbell, Spring MRS (2013).

19. "A low temperature, single step, pulsed d.c magnetron sputtering technique for copper indium gallium diselinide photovoltaic absorber layers", Sreejith Karthikeyan, Kushagra Nagaich, Arthur Hill, Richard D Pilkington, and Stephen A. Campbell, Spring MRS (2013).

20. **Invited Talk** "Ozone Assisted ALD of Doped ZnO as a Transparent Metal Oxide", ", Hai Yuan, Bing Luo, Wayne L. Gladfelter, Stephen A. Campbell, Spring ECS meeting Seattle (2012).

21. 60th International AVS Symposium, Long Beach, California, "Continuous-Flow Chemical Bath Deposition of $Zn_xCd_{1-x}S$ Thin Films for Chalcopyrite Solar Cells," B. S. Tosun, J. T. Abrahamson, A. A. Gunawan, K. A. Mkhoyan, S. A. Campbell and E. S. Aydil (speaker), October 2013.

22. 245th American Chemical Society National Meeting, New Orleans, Lousiana, "Synthesis of Compositionally Graded $Zn_xCd_{1-x}S$ Films using Chemical Bath Deposition," B. S. Tosun (speaker), J. T. Abrahamson, A. A. Gunawan, C. Pettit, C. Cheng, K. A. Mkhoyan, S. A. Campbell and E. S. Aydil, April 2013.

23. 245th American Chemical Society National Meeting, New Orleans, Lousiana, "Electrical Scanning Probe Microscopy of Thin Films for CIGS-based Solar Cells," J. T. Abrahamson (speaker), B. S. Tosun, F. Johnson, G. Haugstad, S. A. Campbell and E. S. Aydil, April 2013.

24. 59th International AVS Symposium, Tampa Bay, Florida, "$Zn_xCd_{1-x}S$ Thin Films For Chalcopyrite Solar Cells Deposited Through Batch and Continuous-Flow Chemical Bath Deposition," B. S. Tosun, C. Pettit, S. A. Campbell and E. S. Aydil, October 2012.

25. "Imaging and Phase Identification of Cu2ZnSnS4 Thin Films using Confocal Raman Spectroscopy", A.-J. Cheng,; M. Manno, A.; Ankur Khare, C.; Chris Leighton, S. A. Campbell, and E. S. Aydil, Fall AVS Meeting, Minneapolis (2011).

26. "Sputter Deposition of Amorphous and Nanocrystalline Tin Dioxide Films" Selin Tosun, Rebekah Feist, Steve Campbell and Eray S. Aydil, American Institute of Chemical Engineering Conference, Minneapolis (2011).

27. "p-Type phosphorus-doped zinc oxide films deposited by atomic layer deposition: Microstructural effects", Wayne L. Gladfelter, Hai Yuan, Bing Luo, and; Stephen A. Campbell, ALD Conference, Cambridge MA (2011).

28. "Simultaneous Interface And Bulk Trap Characterization in CIGS Solar Cells", S. H. Song, S. Jeong, E. Aydil, B. Todd R. Feist, R. Haley, and S. A. Campbell, IEEE Photovoltaics Specialists Conference, Seattle (2011).

29. "Wide Band-gap CuIn1-xGaxSe2 based chalcopyrite absorbers for Tandem cell applications", Kushagra Nagaich,; Eray Aydil, and Stephen Campbell, IEEE Photovoltaics Specialists Conference, SeattleAVS 58th Annual International Symposium and Exhibition (2011).

30. "Sulfurization Studies of the Potential Thin Film Solar Absorber Cu_2ZnSnS_4" An-Jen Cheng, Mike Manno, Rachel Frakie, Rachel Hoffman, Chris Leighton, Eray Aydil and Stephen A. Campbell, IEEE Photovoltaics Specialists Conference, Honolulu (2010).

31. "Structure Optimization for a High Efficiency CIGS Solar Cell", S. H. Song, K. Nagaich, E. Aydil, R. Feist, R. Haley, and S. A. Campbell, EEE Photovoltaics Specialists Conference Honolulu (2010).

32. "Solar Cells from Abundant Nontoxic Materials: Copper Zinc Tin Sulfide Photovoltaics", Eray S. Aydil, Ankur Khare, An-Jen Cheng, Michael Manno, Melissa Johnson, David Norris, Chris Leighton and Stephen Campbell", E3 Conference (an IREE sponsored event), 2010.

33. "An Overview of Lab-Scale Fabrication of High Performance PVs", S. A. Campbell, Colorado Workshop on Photovoltaics, Boulder (2010).

APPENDIX A

Semiconductor Nanoparticles

Collaborators in Mechanical Engineering developed particle beam mass spectroscopy (PBMS) as a tool to measure nanoscale particle size distributions in low pressure processing chambers in real-time. We have observed and sized particles as small as 5 nm in diameter with a sensitivity of ~1 cm^{-3}. More working with Professor Kortshagen, have developed techniques for making cubic, single crystal Si nanoparticles. These could have tremendous applications in building three dimensional, multi-material integrated systems on a chip and in low substrate temperature electronic applications. We have built both n- and p- channel devices and are working on optimizing the device structure. We have also developed processes for making light emitting silicon quantum dots, single crystal silicon nanoparticles that emit all colors (depending on size) and have made the first hybrid silicon OLED.

Papers (Journal and Conference)

1. Brian T. Benton, Benjamin L. Greenberg, K. V. Reich, B. I. Shklovskii, Uwe R. Kortshagen, S. A. Campbell, Variable Range Hopping Conduction in ZnO Nanocrystal Thin Films, Nanotechnology **29**(41) 415202 (2018).

2. UV and Air Stability of High-Efficiency Photoluminescent Silicon Nanocrystals, Jihua Yang, Richard Liptak, Stephen Campbell, Uwe Kortshagen, James Casey and Jon Hannington, Applied Surface Science Vol. 323 pp. 54-58 (2014).

3. Modeling Charge Transport in Quantum Dot Light Emitting Devices with NiO and ZnO transport layers and Si Quantum Dots", Brijesh Kumar, Stephen A. Campbell, Paul Ruden, Journal of Applied Physics **114**(4) p. 044507 (2013). http://dx.doi.org/10.1063/1.4816680

4. "Tunneling Conduction in Dense Silicon Quantum Dot/PMMA Composites, "D. Yu, R. W. Liptak, G. Aggarwal, A. –J. Cheng, and S. A. Campbell, Thin Solid Films 527, pp 261-266 (2013). http://dx.doi.org/10.1016/j.tsf.2012.11.056

5. "Environmental Photostability of SF6-Etched Silicon Nanocrystals", Richard W. Liptak, Jihua Yang, Uwe R. Kortshagen, and Stephen A. Campbell, Nanotechnology 23(39), 395205 (7 pp.) (2012).

6. "Comparing Direct Charge Injection and Forster Energy Transfer into Quantum Dots to Maximize Light Output in Hybrid Organic/Inorganic QD-LEDs" Brijesh Kumar, Ryan Hue, Wayne L. Gladfelter, Stephen A. Campbell, J. Applied Physics 112(3), August 2012 (2012).

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11. "Nanoparticles: A Route to Post-Shrink Information Systems", S. A. Campbell, R. Liptak, S. H. Song, R. Ligman, Yongping Ding, Ying Dong, A. Bapat, F. Gali, X. D. Pi, U. Kortshagen, Proceedings of the UGIM (2008).

12. "Air-stable full-visible-spectrum emission from silicon nanocrystals synthesized by an all-gas-phase plasma approach", X. D. Pi, R. W. Liptak, J Deneen Nowak, N. P. Wells, C B Carter, S A Campbell and U Kortshagen, Nanotechnology **19** 245603 (2008).

13. "Doping Efficiency, Dopant Location, and Oxidation of Si nanocrystals", X. D. Pi, R. Gresback , R. W. Liptak , S. A. Campbell , and U. Kortshagen, APL 92, 123102 (2008).

14. "Full Spectrum Emission and Hybrid OLEDs from Silicon Nanoparticles", X. Pi, R. Liptak, R. Ligman, U. Kortshagen, and S. A. Campbell, Proceedings of the 4th International Conference on Group Four Photonics Workshop, IEEE/LEOS, Tokyo (2007).

15. "Nonthermal plasma Synthesis of Faceted Germanium Nanocrystals", Patrizio Cernetti, Ryan Gresback,, Stephen A. Campbell, and Uwe Kortshagen, Chemical Vapor Deposition **13**, Issue 6-7, July, 2007, Pages: 345-350 (2007).

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17. "Electroluminescence from Surface Oxidized Silicon Nanoparticles Randomly Dispersed within a Polymer Matrix", Rebekah K Ligman, Lorenzo Mangolini, Uwe Kortshagen, Stephen A Campbell, proceedings of Nano Science and Technology International, Santa Clara (2007).

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21. Rebekah K. Ligman, Stephen A. Campbell, Lorenzo Mangolini and Uwe Kortshagen "Electroluminescence from Surface Oxidized Silicon Nanoparticles Dispersed Within a Polymer Matrix", Applied Physics Letters **90**, 061116 (2007), also appears in February 19, 2007 issue of Virtual Journal of Nanoscale Science & Technology (APS).

22. Patrizio Cernetti, Ryan Gresback, Stephen A. Campbell and Uwe Kortshagen, ”Nonthermal plasma synthesis of highly oriented Germanium nanocrystals”, Cherm Vap Dep. **13**, pp. 345–350 (2007).

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27. Barry, Chad R. (University of Minnesota); Campbell, Steven; Jacobs, Heiko O. “Nanoxerography: Electrostatic force directed printing of nanomaterials” Digital Fabrication 2005 - Final Program and Proceedings, Digital Fabrication 2005 - Final Program and Proceedings, 2005, p 25

28. S. A. Campbell, Y. Dong, Y. Ding, A. Bapat, J. Deneen, Uwe R. Kortshagen, and C. Barry Carter, “Single Nanoparticle Semiconductor Devices”, Nanofabrication: Technologies, Devices, and Applications II, W. Y. Lai, L. E. Ocola, and S. Pau, Eds., SPIE Boston (2005).

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30. T. J. Belich, Z. Shen, C. Blackwell, S. Campbell and J. Kakalios, “Conductance Fluctuations in Free-Standing Hydrogenated Amorphous Silicon Nanoparticles”, in the Proceedings of the Third SPIE International Symposium on Fluctuations and Noise - Session on Fluctuations and Noise in Materials II 23-26 May, 2005, Austin, Texas

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APPENDIX A

Synopsis of Research Accomplishments
High Permittivity Insulators and Ultrathin SiO_2 for Deeply Scaled CMOS

Our group has played a pioneering role in the developments of high permittivity layers for deeply scaled MOSFETs. We were the first in the rapidly growing area of research. Papers in 1996 and 97 proved seminal and sparked research efforts at many schools and companies into the use of high permittivity materials as gate insulators. Together with Professor Gladfelter, we have developed new precursors for depositing TiO_2, ZrO_2, HfO_2, and other materials, and have demonstrated the formation of, and electrical effects of, a thin interfacial layer. We have measured the effects of charge injection in these composite gate insulator systems, developed techniques for controlling the interfacial layer thickness, and investigated binary oxides. More recently we have also explored the use of high k materials on SiC, producing the highest quality SiC MOSCAPs ever published.

Books

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APPENDIX A

Synopsis of Research Accomplishments
Rapid Thermal Processing and GeSi Technology

Rapid thermal processing, and its application to the growth of epitaxial layers, comprised a significant fraction of my research efforts from 1991-94. Our group was the first to apply computational fluid dynamics, along with conventional radiative transfer, to model the rapid thermal processing chamber. We developed code for 2 and 3 dimensional steady state calculations and 2 dimensional transient analysis of two chambers. The first was an experimental, single side heated system in which we did GeSi epitaxial growth. The other was an industry standard, Heat Pulse, manufactured by AG Associates. We demonstrated with our model the need for multizone heating and the tendency of wafer edges to overheat during thermal transients. In the area of RTCVD, we demonstrated the effect of dopant addition to the growth chemistry. Specifically we demonstrated that arsine poisoned the surface, raising the activation energy for the growth to that of conventional silicon. This provided significant support to the growth rate enhancement model of Sturm, et. al.

Papers (Journal and Conference)

1. "A Critical Review - The Epitaxial Growth of Semiconductors By Rapid Thermal Chemical Vapor Deposition" S. A. Campbell, Materials Science & Engineering R - Reports **20**, pp 1-36 (1997).

2. "Rapid Thermal Processing", in *Computational Modeling in Semiconductor Processing*, M. Meyyappan, Ed., Artech Publishing (1994)

3. "A Kinetics and Transport Model of Dichlorosilane Chemical Vapor Deposition", K. L. Knutson, S. A. Campbell, and R. Carr, J. Crystal Growth **140**, p. 191 (1994).

4. "The Development of an Anisotropic Si Etch Process Selective to GexSi1-x Underlayers", J. Electrochem. Soc. **141**, p. 507 (1994).

5. "Three Dimensional Temperature Uniformity Modeling of a Rapid Thermal Processing Chamber", K. Knutson, S. A. Campbell, and F. Dunn, IEEE Trans. Semicon. Man.**7**, p. 68 (1994).

6. "A Kinetics and Charge Transport Model of Dichlorosilane Chemical Vapor Deposition", K. L. Knutson, R. W. Carr, W. H. Liu, and S. A. Campbell, Proc. Am Chem Soc (1993).

7. "Arsenic Doping of GeSi Epitaxial Layers in the Dichlorosilane/Germane System", W. H. Liu, J. D. Leighton, and S. A. Campbell, Appl Phys Lett. **61** pp 1676-1678 (1992).

8. "Dopings Effects During the CVD Growth of GeSi", W. H. Liu, S. A. Campbell, and J. D. Leighton, Proceedings of the Fall 1992 American Vacuum Society Symposium on GeSi.

9. "Transient Effects in Rapid Thermal Processing", S. A. Campbell and K. L. Knutson, IEEE Trans on Semicon Man. **5**, p. 302 (1992).

10. "Thermal Effects of Gasses in Rapid Thermal Processing", K. L. Knutson and S. A. Campbell in Rapid Thermal and Integrated Processing: Materials Research Society Proceedings, Vol 224 Materials Research Society, (1991).

11. "Steady State Thermal Uniformity and Gas Flow Patterns in a Rapid Thermal Processing Chamber", S. A. Campbell, K. H. Ahn, K. L. Knutson, B. Liu, and J. D. Leighton, IEEE Trans on Semicon Man, 4, (1991).

12. "Modeling of Ge-Si Heterojunction Bipolar Transistors For Use In Silicon Monolithic Millimeterwave Integrated Circuits", S. A. Campbell and A. Gopinath, IEEE Microwave Theory and Tech 37, pp. 2046-2051 (1989).

13. "Very Thin Silicon Epitaxial Layers Grown Using Rapid Thermal Vapor Phase Epitaxy", S. A. Campbell, J. D. Leighton, G. H. Case, and K. Knutson, J Vac Sci and Tech B 7, pp. 1080-1083 (1989).

Presentations

1. "Three Dimensional Temperature Uniformity Modeling of a Rapid Thermal Processing Chamber", K. L. Knutson, S. A. Campbell, and F. Dunn, 1993 Spring Meeting of the Materials Research Society.

2. "A Kinetics and Transport Model of Dichlorosilane Chemical Vapor Deposition", K. L. Knutson, W. H. Liu, S. A. Campbell, and R. W. Carr, The American Institute of Chemical Engineers, Fall Meeting, 1993.

3. "Dopings Effects During the CVD Growth of GeSi", W. H. Liu, S. A. Campbell, and J. D. Leighton, Fall 1992 American Vacuum Society Symposium.

4. "Selective Removal of GeSi Layers", L. Shang, S. A. Campbell, W. H. Liu, and J. D. Leighton, Fall 1992 American Vacuum Society Symposium.

5. "Thermal Effects of Gasses in Rapid Thermal Processing", K. L. Knutson and S. A. Campbell, Spring Meeting of the Materials Research Society, (1991).

6. "Gas Flow Patterns and Thermal Uniformity in Rapid Thermal Processing Equipment", S. A. Campbell, K. L. Knutson, K. H. Ahn, J. D. Leighton, and B. Liu, 1990 International Electron Devices Meeting.

APPENDIX A

Synopsis of Accomplishments
Semiconductor Processing Education and Technology

The Science and Technology of Microelectronic Fabrication, was released in March, 1996 by Oxford University Press. The first edition went through seven printings before the second edition was released in 2001. The third edition is now in preparation. Approximately 50 US institutions have adopted it as a course textbook, including Stanford, Berkeley, Cornell, and UT Austin. Numerous schools in Europe, the Middle East, and the Pacific Rim have also adopted the book, and the book has been translated into Chinese. A major new initiative has been the development of new AAS capstone experience at the University. This was developed in collaboration with Dakota County Technical. Minnesota State College - Southeast Technical recently joined and will be submitting students to the program in 2009. Four other schools have joined with the University and DCTC to create an upper Midwest consortia in nano education. Finally, this section covers several small research projects including MEMS-related work and one project funded by ONR on the formation of semi-insulating silicon wafers by the addition of Au as a Fermi level pinning impurity.

Books

1. S. A. Campbell, *The Science and Technology of Microelectronic Fabrication*, Oxford University Press, New York (1996, 2001).
2. S. A. Campbell, *Fabrication Engineering at the Micro and Nanoscale*, Oxford University Press, New York (2006, 2013).

Papers (Journal and Conference)

1. Nezhueyotl Izquierdo, Jason C. Myers, Prafful Golani, Nicholas C. A. Seaton, Steven J. Koester, and Stephen A. Campbell, "Growth of Black Arsenic Phosphorus Thin Films and its Application for Field-Effect Transistors", Nanotechnology 32 325601 (2021).

2. Sushil K. Pandey (IEEE Member), Nezhueyotl Izquierdo and Stephen A. Campbell, "Growth of very large MoS2 single crystals using out-diffusion transport and their use in field effect transistors", Accepted for publication, IEEE Trans. Nano (2021).

3. Zachary DeGregorio, Jason Myers, Stephen Campbell, "Rational Control of WSe2 Layer Number via Hydrogen-Controlled Chemical Vapor Deposition" Nanotechnology, **31** 315604 (2020).

4. Nezhueyotl Izquierdo, Jason Myers, Nicholas C.A. Seaton, Sushil K. Pandey and Stephen A. Campbell, "Deposition of Surface Passivated Black Phosphorus Thin Films", *ACS Nano* 13(6) pp. 7091-7099 (2019).

5. Sushil Kumar Pandey, Hussain Alsalman, Javad Ghasemi Azadani, Nezhueyotl Izquierdo, Tony Low, and Stephen A. Campbell, Controlled p-type substitutional doping in large-area monolayer WSe2 crystals grown by chemical vapor deposition, *Nanoscale*, 2019, **11**, 365 - 365.

6. Yong-hua Zhang, Stephen A. Campbell, Sreejith Karthikeyan, Finite element analysis of hollow out-of- plane HfO2 microneedles for transdermal drug delivery applications, Biomedical Microdevices (2018) 20:19.

7. Yong-hua Zhang, Stephen A. Campbell, Sreejith Karthikeyan, Preparation of hollow out-of-plane hafnium oxide microneedle arrays for transdermal drug delivery, Microsyst Technol (2017) 23:5887–5892 DOI 10.1007.

8. Yonghua Zhang and Stephen A. Campbell, "Finite element analysis of hollow hafnium oxide microneedles for transdermal drug delivery", Proceedings of the Biomedical Engineering and Informatics Conference, Shanghai (2017).

9. Sushil Kumar Pandey, Nezhueyotl Izquierdo and Stephen Campbell "Use of passivation layer to improve thermal stability and quality of phosphorene/AZO heterojunction diode", RSC Advances **7**, pp. 46201 - 46207 (2017).

10. Yong-hua Zhang, Stephen A. Campbell, Liyuan Zhang, Sreejith Karthikeyan, "Sandwich structure based on back-side etching silicon (100) wafers for flexible electronic technology", Microsyst Technol **23**, pp. 739–743 (2017). DOI 10.1007/s00542-015-2737-7

11. Sushil Pande, Stephen A. Campbell, "Effect of Passivation Layer of the Thermal Stability of a Few-Layer Phosphorene/AZO Heterostructure", Spring Meeting of MRS 2017.

12. Younghua Zhang and Stephen A. Campbell, Preparation of hollow hafnium oxide microneedles for transdermal drug delivery, Proceedings of the 9th International Conference on BioMedical Engineering and Informatics (BMEI), Datong, China (2016).

13. Jie Zhu, Haechan Park, Junyang Chen, Hu Zhang, Sreejith Karthikeyan, Nathaniel Wendel, Stephen A. Campbell, Matthew Dawber, Du Xu, Mo Li, Jianping Wang, and Xiaojia Wang, "Probing the Anisotropic Thermal Conductivity of Black Phosphorous with Time-Resolved Magneto-Optical Kerr Effect", Advanced Materials 2(5) 1600040, (2016).

14. Younghua Zhang and Stephen A. Campbell, Polymer-sandwiched Ultra-thin Silicon(100) Layer for Flexible Electronics', Proceedings of the 8th International Conference on BioMedical Engineering and Informatics (BMEI), Shenyang City, China (2015).

15. "Electromechanical Switches Fabricated by Electrophoretic Deposition of Single Wall Carbon Nanotube Films" Junyoung Lim and Stephen A. Campbell, submitted to Sensors and Actuators A (2015).

16. "Properties of electrophoretically deposited single wall carbon nanotube films" Junyoung Lim, Maryam Jalali, Stephen A. Campbell, *Thin Solid Films* 589 278-285 (2015). doi/10.1016/j.tsf.2015.05.042

17. "A Low-Cost Hands-On Laboratory to Introduce Lithography Concepts", Maryam Jalali , James Marti, Allison Kirchhoff, Frances Lawrenz, and Stephen A. Campbell, IEEE Trans. Education (2012).

18. "Suspended and Highly Aligned Carbon Nanotube Thin-Film Structures Using Open Microfluidic Channel Template", Dongjin Lee, Zhijiang Ye, Stephen A. Campbell, and Tianhong Cui, Sensors and Actuators A: Physical vol 188, pp. 434 - 441 (2012).

19. "A three-terminal single-walled carbon nanotube thin film MEMS switch for digital logic applications", Jang, Min-Woo; Chen, Chia-Ling; Partlo, Walter E; Patil, Shruti R; Lee, Dongjin; Ye, Zhijiang; Lilja, David; Taton, T. Andrew; Cui, Tianhong; Campbell, Stephen A., 2011 16th International Solid-State Sensors, Actuators and Microsystems Conference, TRANSDUCERS'11, p 1705-1708, 16th International Solid-State Sensors, Actuators and Microsystems Conference (2011).

20. "An All Carbon Nanotube Thin Film Based Three Terminal Switch", Min-Woo Jang, Chia-Ling Chen, Walter E Partlo III, Shruti R Patil, Dongjin Lee, Zhijang Ye, David Lilja, T. A. Taton, T. Cui and Stephen A. Campbell, Applied Physics Letters 98, 073502 (2011), also February 28, 2011 issue of Virtual Journal of Nanoscale Science & Technology.).

21. "A Pure Single-Walled Carbon Nanotube Thin Film Based 3-Terminal MEMS Switch", Min-Woo Jang, Chia-Ling Chen, Walter E Partlo III, Shruti R Patil, Dongjin Lee, Zhijang Ye, David Lilja, S. A. Campbell, *Applied Physics Letters*, v 98, n 7, February 14, 2011

22. "Suspended Carbon Nanotube Thin Film Structures with High Degree Of Alignment For NEMS Switch Applications", Dongjin Lee, Zhijiang Ye, Stephen A. Campbell, and Tianhong Cui, Proceedings of the IEEE Transducers Conference, Bejing (2011).

23. "Thermally Enhanced Single-Walled Carbon Nanotube Microfluidic Alignment", Zhijiang Ye, Dongjin Lee, Stephen A. Campbell, and Tianhong Cui1, *Microelectronic Engineering*, v 88, n 9, p 2919-2923, September 2011

24. "Characterization of Carbon Nanotube Nanoswitches with Gigahertz Resonance Frequency and Low Pull-in Voltages Using Electrostatic Force Microscopy", Miao Lu, Xuekun Lu, Min-Woo Jang, Stephen A. Campbell, and Tianhong Cui, Journal of Micromechanics and Microengineering, v 20, n 10 (2010).

25. "Aligned Dense SWNT Beams and Cantilevers for NEMS Applications", Miao Lu, Min-Woo Jang, Stephen A. Campbell, and Tianhong Cui", Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures, v 28, n 3, p 522-526, May 2010

26. Well-Aligned and Suspended Single-Walled Carbon Nanotube Membranes: Directed Self Assembly, Patterning, and Characterization", Miao Lu, Min-Woo Jang, Greg Haugstad, Stephen A. Campbell, and Tianhong Cui1, Applied Physics Letters **94**, p. 261903 (2009).

27. "High Temperature Materials for Resistive IRSPs", Steven Solomon, Robert Ginn, Stephen A. Campbell, Maryam Jalali, and George Goldsmith, in Technologies for Synthetic Environments: Hardware-in-the-Loop Testing XI, part of the SPIE Defense and Security Symposium, Orlando (2006).

28. "Fabrication and Characterization of a Solenoid-Type Microtransformer", R. J. Rassel, F. Hiatt, J. DeCramer, and S. A. Campbell, IEEE Trans. on Magnetics **39** (1) pp. 553-558 (2003).

29. "Semi-insulating Silicon Substrates for Silicon Based RF Integrated Circuits", R. Wang, S. A. Campbell, R. Tan, J. Meyer, and Y. Cai, Proceedings of the Silicon Materials for RF

Integrated Circuits Symposium, IEEE (1998).

30. "Semi-Insulating Silicon", S. A. Campbell and J. Meyer, Proceedings of the 1995 Silicon on Insulator Workshop, IEEE (1995).

31. "Interconnect for Layered Integrated Circuit Assembly", S. Bezuk, T. Gheewala, S. A. Campbell, and R. Baseman, US Patent Number 4,845,542, July 4, 1989.

32. "Mobility Degradation Coefficients in CMOS Devices at Low Temperature", S. A. Campbell and P. Anderson, IEE Proceedings, 135, pp. 17-19 (1988).

33. "Initial Investigations of Transistor FET Logic (TFL)", J. Jorgenson, S.A. Campbell, J. Granger, and T. Gheewala in Proceedings of the 1986 Gull Lake Technical Symposium.

34. "Laser Direct Writing of Semiconductor Structures: High Aspect Ratio Structures for IC-Chip Carrier Connections", R. Baseman, S. Bezuk, S.A. Campbell, and T. Gheewala in Proceedings of the 1986 Gull Lake Technical Symposium.

35. "A New Super Self Aligned Bipolar Technology", J. Seefeldt, D. Gibson, G. Thomes, and S.A. Campbell in Proceedings of the 1985 Gull Lake Technical Symposium.

36. "Design Methodology of a 1.2 um Double-Level-Metal CMOS Technology", N. Prekshot, S.A. Campbell, W. Heikkila, D. Dokos, R. Passow, W. Grant, D. Schultz, and J. Victorey IEEE Transactions and IEEE Electron Devices, February (1984).

37. "MOS III A One Micron CMOS Technology", S.A. Campbell, D. Dokos, W. Grant, and J. Victorey in Proceedings of the 1983 Gull Lake Technical Symposium.

Presentations

1. Nezhueyotl Izquierdo and Stephen A. Campbell, “Single-Step, Direct Silicon-Substrate Growth of Black Phosphorus with in-situ Sn passivation”, Presented at the Fall Meeting of the MRS (2018).

2. Sushil Kumar Pandey, Nezhueyotl Izquierdo and Stephen Campbell, “Effect of Passivation Layer of the Thermal Stability of a Few-Layer Phosphorene/AZO Heterostructure”, presented at spring MRS meeting 2017 (Phoenix).

3. Sushil Kumar Pandey, Nezhueyotl Izquierdo and Stephen Campbell, “Ion bombardment free plasma thinning of black phosphorus for integration of phosphorene/ZnO based optoelectronics devices applications”, presented at fall MRS meeting 2017 (Boston).

4. Yonghua Zhang and Stephen A. Campbell, “Finite element analysis of hollow hafnium oxide microneedles for transdermal drug delivery”, Biomedical Engineering and Informatics Conference, Shanghai (2017)

5. Abhimanyu Ravindranath; Joshua G. Puhl; Morgan Newhoff; Kang Xiong-Hang; Christy L. Haynes; Karen A. Mesce; Stephen A. Campbell. 2016. High Signal-to-Noise Detection of Neuronal Activity Using Novel Mutli-Channel Microfabricated Electrode Arrays.

Institute for Engineering in Medicine, Retreat (poster), University of Minnesota, Minneapolis, 2016.

6. Revealing the Origins of Three-Dimensional Anisotropic Thermal Conductivities of Black Phosphorus submitted to the IMECE2016.

7. Nathaniel Wendel, Ryan J. Wu, Nazila Haratipour, Matthew C. Robbins, K. Andre Mkhoyan, Steven Koester, and Stephen A. Campbell, "Black Phosphorus Synthesis and Characterization Enabling High Performance Phosphorene Transistors", MRS Fall Meeting, 2015, accepted for oral presentation.

8. "Device for quantifying neural response and other conditions by measuring sweat gland function", Jun Young Lim, Ming-Lun Wu, William R. Kennedy, Stephen A. Campbell, Design of Medical Devices Conference (2014).

9. "A Pure Single-Walled Carbon Nanotube Thin Film Based 3-Terminal MEMS Switch", Min-Woo Jang, Chia-Ling Chen, Walter E Partlo III, Shruti R Patil, Dongjin Lee, Zhijang Ye, David Lilja, T. A. Taton, T. Cui and Stephen A. Campbell, Proceedings of the IEEE Transducers Conference, Bejing (2011).

10. "Suspended Carbon Nanotube Thin Film Structures with High Degree Of Alignment For NEMS Switch Applications", Dongjin Lee, Zhijiang Ye, Stephen A. Campbell, and Tianhong Cui, Proceedings of the IEEE Transducers Conference, Bejing (2011).

11. "Functional 1.6ghz MEMS Switch Using Aligned Composite CNT Membrane By Dielectrophoretic Self-Assembly", M.W. Jang, M. Lu, T. Cui and S. A. Campbell, IEEE Transducers Conference (Denver) 2009.

12. "A 1.6 GHz MEMS Switch Using Aligned Composite CNT Membranes", M.W. Jang, M. Lu, T. Cui and S. A. Campbell, IEEE Device Research Conference, 2009.

13. "High Temperature Materials for Resistive IRSPs", Steven Solomon, Robert Ginn, Stephen A. Campbell, Maryam Jalali, and George Goldsmith, at Technologies for Synthetic Environments: Hardware-in-the-Loop Testing XI, part of the SPIE Defense and Security Symposium Symposium, Orlando (2006).

14. "Semi-insulating Silicon Substrates for Silicon Based RF Integrated Circuits", R. Wang, S. A. Campbell, R. Tan, J. Meyer, and Y. Cai, Silicon Materials for RF Integrated Circuits Symposium, IEEE (1998).

15. "Fabrication and Microwave Performance of Semi-Insulating Silicon", S. A. Campbell and J. Meyer, Spring Meeting of the Materials Research Society (1996).

16. "Semi-Insulating Silicon", S. A. Campbell and J. Meyer, 1995 Silicon on Insulator Workshop, Phoenix (1995).

17. Invited Talk "The Possibility of Semi-insulating Silicon Wafers", S. A. Campbell, Silicon RF Technologies Workshop, 1995 Microwave Theories and Techniques Conference, Orlando (1995).

18. Invited Talk "Si-Ge Based Microwave Circuits", S. A. Campbell, A. Gopinath, and S. Taub, IEEE International Workshop on Silicon Based High Frequency Devices and Circuits", Ulm, Germany (1994).

19. "Possibility of Silicon Monolithic Millimeterwave Integrated Circuits", S. A. Campbell and A. Gopinath, 1989 Microwave Theory and Techniques Symposium, Long Beach, Cal.

20. "A 1.2 Micron Double Level Metal CMOS Technology", S.A. Campbell, D. Dokos, W. Grant, J. Victorey in Proceedings of the 1983 Custom Integrated Circuits Conference.

21. "Multiple Layer Techniques in Optical Lithography: Applications to Fine Line MOS Production", M.A. Listvan, M. Swanson, A. Wall and S.A. Campbell, Optical Microlithograhpy III: Technology for the Next Decade, p. 85, SPIE **470** (1983).

APPENDIX A

Additional Publications

Papers (Journal and Conference)

1. "Anisotropy of the Fermi Surface, Fermi Velocity, Many-Body Enhancement and Super Conducting Energy Gap in Nb", G. W. Crabtree, D. H. Dye, D. P. Karim, S.A. Campbell, J. B. Ketterson, Phys. Rev. B, 35, pp. 1728-1741 (1987).

2. "Critical Field Measurements in Superconductors using AC Inductive Techniques", S. A. Campbell, J. B. Ketterson, and G. W. Crabtree, Rev. Sci. Inst. 54, pp. 1191-1198 (1983).

3. "Observation of a First-Order Phase Transition in Single Crystal ErRh4B4 at Hc2", F. Behroozi, G.W. Crabtree, S.A. Campbell, and D.G. Hinks, Phys. Rev. B 27 (1983).

4. "Anisotropic Superconducting and Magnetic Properties of Single Crystal ErRh4B4", G.W. Crabtree, F. Behroozi, S.A. Campbell, and D.G. Hinks Phys. Rev. Letters 49 (1982).

5. "Magnetic Free Energy of ErRh4B4 in Paramagnetic and Superconducting States", G.W. Crabtree, F. Behroozi, S.A. Campbell, D.G. Hinks, and M. Levy, J. Low Temp. Physics, 49 (1982).

6. "Precision Magnetization and Susceptibility Measurements on ErRh4B4 in the Ferromagnetic and Superconducting Phases", F. Behroozi, G.W. Crabtree, S.A. Campbell, D.R. Snider, M. Levy, D.C. Johnston, and B.T. Matthias, in Ternary Superconductors, ed. by G.K. Shenoy, B.D. Dunlop, and F.Y. Fradin (Elsevier North Holland, Amsterdam 1981).

7. "Fermi Surface and Many Body Enhancements in Pd", D.H. Dye, S.A. Campbell, G.W. Crabtree, J.B. Ketterson, N.B. Sandersara, and J.J. Vuillemin, Phys. Rev. B 23 (1981).

Presentations

1. "Experimental Determination of Paramagnetic and Superconducting Free Energies of ErRh4B4", F. Behroozi, G.W. Crabtree, S.A. Campbell, D.R. Snider, M. Levy, and D.C. Johnston, Bull. Am. Phys. Soc. 26 (1981).

2. "Anisotropy of the Fermi Surface and Many Body Effects in Palladium", S.A. Campbell, W.W. Crabtree, D.H. Dye, J.B. Ketterson, N.B. Sandersara, and J.J. Vuillemin, Bull. Am. Phys. Soc. 24 (1978).