

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MONOLITHIC POWER SYSTEMS, INC.,

Petitioner,

v.

GREENTHREAD LLC,

Patent Owner.

U.S. PATENT NO. 11,121,222
PTAB CASE NO. IPR2024-00470

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,121,222
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

TABLE OF CONTENTS

I.	MANDATORY NOTICES.....	1
A.	Real Party-In-Interest	1
B.	Related Matters.....	1
C.	Counsel Service Information	3
D.	37 C.F.R. §42.8(b)(4): Service Information	3
II.	PAYMENT OF FEES UNDER 37 C.F.R. §42.103	3
III.	CERTIFICATION OF GROUNDS FOR STANDING.....	4
IV.	OVERVIEW OF CHALLENGE AND RELIEF REQUESTED	4
A.	Prior Art Printed Publications.....	4
B.	Relief Requested.....	4
V.	PERSON OF ORDINARY SKILL IN THE ART	5
VI.	CLAIM CONSTRUCTION.....	5
VII.	THE '222 PATENT AND BACKGROUND	9
A.	The '222 Patent's Purported Improvements	9
B.	General Background On Static Unidirectional Electric Drift Fields as Related to Semiconductor Layers Having Graded Dopant Profiles.....	11
C.	Patent Owner's Representation of Claim Scope	14
VIII.	SPECIFIC GROUNDS.....	19
A.	Ground I: Onoda Renders Obvious Claim 44.....	19
1.	Independent Claim 44.....	19
a.	Preamble: "A CMOS Semiconductor device comprising:"	21
b.	Element [44.1]: "a surface layer;"	22

c.	Element [44.2]: “a substrate;”	25
d.	Element [44.3]: “an active region including a source and a drain, disposed on one surface of the surface layer;”	26
e.	Element [44.4]: “a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,”	30
f.	Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”	34
g.	Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”	36
B.	Ground II: Onoda in view of Nishizawa Renders Obvious Claim 44. .	42
1.	Independent Claim 44.....	45
a.	Preamble: “A CMOS Semiconductor device comprising:”	45
b.	Elements [1.1]-[1.4]	46
c.	Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”	46
d.	Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”	48
C.	Ground III: Kawagoe Renders Obvious Claim 44.....	49
1.	Independent Claim 44.....	49

a.	Preamble: “A CMOS Semiconductor device comprising:”	49
b.	Element [44.1]: “a surface layer;”	50
c.	Element [44.2]: “a substrate;”	53
d.	Element [44.3]: “an active region including a source and a drain, disposed on one surface of the surface layer;”	54
e.	Element [44.4]: “a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,”	58
f.	Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”	65
g.	Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”	69
IX.	THE BOARD SHOULD INSTITUTE IPR	75
1.	35 U.S.C. § 314(a)	75
2.	35 U.S.C. § 325(d)	76
3.	Prior Petitions Do Not Warrant Denying Institution	78

TABLE OF AUTHORITIES

FEDERAL CASES

<i>Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH,</i> IPR2019- 01469.....	76
<i>Apple Inc. v. Uniloc 2017 LLC,</i> IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020).....	79
<i>Becton, Dickinson, & Co. v. B. Braun Melsungen AG,</i> IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017).....	76
<i>Bowtech Inc. v. MCP IP, LLC,</i> IPR2019-00383, Paper 14 (P.T.A.B. Aug. 6, 2019)	77
<i>Dell Technologies, Inc. et al. v. Greenthread, LLC,</i> IPR2023-00509.....	2
<i>Fasteners for Retail, Inc. v. RTC Indus., Inc.,</i> IPR2019-00994, Paper 9 (P.T.A.B. Nov. 5, 2019)	77
<i>Intel Corp. v. Greenthread, LLC,</i> IPR2023-00420.....	2
<i>Intel Corp. v. Greenthread, LLC,</i> IPR2023-00552.....	2
<i>Phillips v. AWH Corp.,</i> 415 F.3d 1303 (Fed. Cir. 2005) (<i>en banc</i>). 37 C.....	5
<i>PopSockets LLC v. Flygrip, Inc.,</i> IPR2022- 00938.....	76
<i>Samsung Electronics, Co., Ltd., v. Greenthread, LLC,</i> IPR2020-00289.....	2
<i>Sony Group Corp. (Japan) v. Greenthread, LLC,</i> IPR2023-00324.....	2
<i>Xilinx, Inc. v. Arbor Global Strategies, LLC,</i> IPR2020-01568, Paper No. 12 (P.T.A.B. Mar. 5, 2021).....	79

OTHER CASES

<i>Greenthread, LLC v. Cirrus Logic, Inc.</i> , Civil Action No. 1:23-cv-00369.....	1
<i>Greenthread, LLC v. Intel Corp. et al.</i> , Case No. 6:22-cv-00105, Dkt. 96.....	7
<i>Greenthread, LLC v. Intel Corp. et al.</i> , Case No. 6:22-cv-105-ADA.....	14, 15
<i>Greenthread, LLC v. Intel Corporation</i> , Civil Action No. 6:22-cv-01293.....	2
<i>Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.</i> , Civil Action No. 6:22-cv-00105.....	2
<i>Greenthread, LLC v. Micron Technology, Inc. et al.</i> , Civil Action No. 1:23-cv-00333.....	2
<i>Greenthread, LLC v. Monolithic Power Systems, Inc.</i> , Civil Action No. 1:23-cv-00579.....	1
<i>Greenthread, LLC v. OmniVision Technologies, Inc.</i> , Civil Action No. 2:23-cv-00212.....	1
<i>Greenthread, LLC v. ON Semiconductor Corp., et al.</i> Civil Action No. 1-23-cv-00443.....	2
<i>Greenthread, LLC v. OSRAM GmbH et al</i> , Civil Action No. 2:23-cv-00179.....	1
<i>Greenthread, LLC v Texas Instruments Incorporated</i> , Civil Action No. 2:23-cv-00157.....	1
<i>Greenthread, LLC v. Western Digital Corporation et al</i> , Civil Action No. 1:23-cv-00326.....	2

FEDERAL STATUTES

35 U.S.C. § 103.....	4, 5
35 U.S.C. § 314(a)	75, 76

35 U.S.C. § 325(d).....76, 77

pre-America Invents Act.....4

RULES

Rule 42.104(a) 4

REGULATIONS

37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4) and 42.10(a).....3

37 C.F.R. § 42.8(b)(4) 3

37 C.F.R. § 42.10(b) 3

37 C.F.R. § 42.15(a)(1).....3

37 C.F.R. § 42.103.....3

TABLE OF EXHIBITS

Ex. 1001	U.S. Patent No. 11,121,222 (the “’222 Patent”)
Ex. 1002	Prosecution History of the ’195 Patent (“the Prosecution History”)
Ex. 1003	Declaration of Dr. Stephen Campbell
Ex. 1004	Curriculum Vitae of Dr. Stephen Campbell
Ex. 1005	U.S. Patent No. 4,684,971 (“Payne”)
Ex. 1006	U.S. Patent No. 4,907,058 to Sakai (“Sakai”)
Ex. 1007	U.S. Patent No. 6,043,114 to Kawagoe, et al., (“Kawagoe”)
Ex. 1008	Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000)
Ex. 1009	U.S. Patent No. 4,160,985 (“Kamins”)
Ex. 1010	U.S. Patent No. 4,481,522 (“Jastrzebski”)
Ex. 1011	U.S. Patent Application Publication No. 2003/0042511 (“Rhodes”)
Ex. 1012	U.S. Patent Application Publication No. 2002/0102783 (“Fujimoto”)
Ex. 1013	Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21st Intl Conf on VLSI Design, IEEE 2008 (“Wang”)
Ex. 1014	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 (“Resnick Decl.”)
Ex. 1015	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 (“Watters Decl.”)
Ex. 1016	IPR2020-00289, Patent Owner Preliminary Response
Ex. 1017	U.S. Pat. No. 11,121,222 (the “’222 Patent”)
Ex. 1018	U.S. Pat. No. 11,316,014 (the “’014 Patent”)

Ex. 1019	Civil Action No. 2:19-cv-00147-JRG, Dkt. 67 (E.D. Tex. Apr. 20, 2019)
Ex. 1020	Prosecution History of U.S. Pat. No. 11,121,222
Ex. 1021	Prosecution History of U.S. Pat. No. 11,316,014
Ex. 1022	U.S. Patent Application Publication No. 2004/0063288 (“Kenney”)
Ex. 1023	Jaeger, <i>Introduction to Microelectronic Fabrication</i> , Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) (“Jaeger”)
Ex. 1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics , dated June 30, 2023
Ex. 1025	U.S. Patent No. 4,435,896 (“Parrillo”)
Ex. 1026	L.C. Parrillo, R.S. Payne et al., <i>Twin-Tub CMOS - A Technology for VLSI Circuits</i> , IEEE 1980 (“Parrillo2”)
Ex. 1027	U.S. Patent Application Publication No. 2007/0045682 to Hong <i>et al.</i> (“Hong”)
Ex. 1028	The Oxford American Dictionary and Language Guide, Oxford University Press (1996)
Ex. 1029	U.S. Patent No. 11,121,222 File History
Ex. 1030	Patent Owner’s Responsive Claim Construction Brief
Ex. 1031	RESERVED
Ex. 1032	Patent Owner’s Sur-Reply Claim Construction Brief
Ex. 1033	Proposed Claim Constructions in the District Court Case
Ex. 1034	Redacted District Court Case Transfer Order
Ex. 1035	Civil Action No. 2:19-cv-00147-JRG, Dkt. 105 (E.D. Tex. Jul. 9, 2020)
Ex. 1036	Publication Declaration of Sylvia Hall-Ellis for Wolf

Ex. 1037	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105
Ex. 1038	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek (“Wieczorek”)
Ex. 1039	Parrillo IEEE Citation List
Ex. 1040	Dictionary of Engineering, McGraw Hill (2003)
Ex. 1041	Rubin et al., <i>Ranges and Moments of Depth Distributions of Boron and Phosphorus Implanted into Silicon in the Energy Range 1.7 - 5.0 MeV with an Eaton NV-GSD/VHE Implanter</i> , IEEE 1997 (“Rubin”)
Ex. 1042	Certified translation of Japanese Unexamined Patent Application Publication No. H8-279598 (“Onoda”)
Ex. 1043	Japanese Unexamined Patent Application Publication No. H8-279598, published on October 22, 1996
Ex. 1044	IPR2020-289, Termination Order
Ex. 1045	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
Ex. 1046	U.S. Pat. No. 5,384,476 (the “’576 Patent”) (“Nishizawa”)
Ex. 1047	U.S. Pat. No. 6,900,091 (the “’091 Patent”) (“Williams”)

Monolithic Power Systems, Inc. (“Petitioner”) requests *inter partes* review (“IPR”) of claim 44 (the “Challenged Claim”) of U.S. Patent No. 11,121,222 (Ex. 1001, the “’222 Patent”).

I. MANDATORY NOTICES

A. Real Party-In-Interest

Monolithic Power Systems, Inc. is the real party-in-interest.

B. Related Matters

The ’222 Patent is the subject of the following active proceedings:

- *Greenthread, LLC v. Monolithic Power Systems, Inc.*, Civil Action No. 1:23-cv-00579 in the District of Delaware, filed May 26, 2023 (“MPS Litigation”);
- *Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-00369 in the Western District of Texas, filed March 31, 2023;
- *Greenthread, LLC v. Texas Instruments Incorporated*, Civil Action No. 2:23-cv-00157 in the Eastern District of Texas, filed April 6, 2023;
- *Greenthread, LLC v. OSRAM GmbH et al*, Civil Action No. 2:23-cv-00179 in the Eastern District of Texas, filed April 19, 2023; and
- *Greenthread, LLC v. OmniVision Technologies, Inc.*, Civil Action No. 2:23-cv-00212 in the Eastern District of Texas, filed May 10, 2023.

The ’222 Patent was previously subject to the following proceedings, which are no longer pending:

- *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-00105 in the Western District of Texas (“Intel Litigation”), filed January 27, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6:22-cv-01293 in the Western District of Texas, severed December 21, 2022, and transferred to District of Oregon as 3:22-cv-02001;
- *Greenthread, LLC v. Western Digital Corporation et al*, Civil Action No. 1:23-cv-00326 in the District of Delaware, filed March 24, 2023;
- *Greenthread, LLC v. Micron Technology, Inc. et al.*, Civil Action No. 1:23-cv-00333 in the District of Delaware, filed March 24, 2023;
- *Samsung Electronics, Co., Ltd., v. Greenthread, LLC*, IPR2020-00289, filed on December 23, 2019.
- *Greenthread, LLC v. ON Semiconductor Corp., et al.* Civil Action No. 1-23-cv-00443 in the District of Delaware, filed April 21, 2023.
- *Intel Corp. v. Greenthread, LLC*, IPR2023-00552, filed on Feb. 1, 2023.
- *Intel Corp. v. Greenthread, LLC*, IPR2023-00420, filed on Dec. 28, 2022.
- *Dell Technologies, Inc. et al. v. Greenthread, LLC*, IPR2023-00509, filed on Jan. 27, 2023.
- *Sony Group Corp. (Japan) v. Greenthread, LLC*, IPR2023-00324, filed on Dec. 12, 2022.

The '222 Patent is or was involved in the following PTAB proceedings as of today:

AIA review # 2 ↓	Filing date (mm/dd/yyyy) 1 ↓	Institution decision date (mm/dd/yyyy)	Termination date (mm/dd/yyyy)	Petitioner application #	Petitioner patent #	Petitioner	Petitioner tech center	PO/Respondent application #	PO/Respondent patent #	PO/Respondent	PO/Respondent tech center	Status
IPR2024-00021	10/27/2023					Cirrus Logic, Inc. et al.		16947294	11121222	Greenthread, LLC	2800	Pending
IPR2024-00020	10/27/2023					Cirrus Logic, Inc. et al.		16947294	11121222	Greenthread, LLC	2800	Pending
IPR2023-01244	07/27/2023					Semiconductor Com...		16947294	11121222	Greenthread, LLC	2800	Pending
IPR2023-01242	07/27/2023					Semiconductor Com...		16947294	11121222	Greenthread, LLC	2800	Pending
IPR2023-00552	02/01/2023		05/18/2023			Intel Corporation		16947294	11121222	Greenthread, LLC	2800	Terminated-Settled
IPR2023-00509	01/27/2023		05/17/2023			Dell Technologies Inc...		16947294	11121222	Greenthread, LLC	2800	Terminated-Settled
IPR2023-00420	12/28/2022		05/18/2023			Intel Corporation		16947294	11121222	Greenthread, LLC	2800	Terminated-Settled
IPR2023-00324	12/12/2022		05/18/2023			Sony Group Corpora...		16947294	11121222	Greenthread, LLC	2800	Terminated-Settled

C. Counsel Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints Miguel Bombach (Reg. No. 68,636) as its lead counsel, and Bing Ai (Reg. No. 43,312), John D. Esterhay (Reg. No. 73,512), John P. Schnurer (Reg. No. 52,196), Brianna Kadjo (Reg. No. 74,307), and Runkun (Justin) Jiang (Reg. No. 78,118) as its back-up counsel.

D. 37 C.F.R. §42.8(b)(4): Service Information

Petitioner concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address:

PerkinsServiceMPS-GreenthreadIPR@perkinscoie.com

II. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 50-0665. Review of claim 44 is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '222 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Prior Art Printed Publications

The '222 Patent claims priority to September 3, 2004. Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '222 Patent:

- **Onoda** – Japanese Application H8-279598 to Onoda (Ex. 1043, certified translation 1042) published on October 22, 1996 and is prior art under §102(b).¹
- **Kawagoe**: U.S. Patent No. 6,043,114 to Kawagoe et al. (Ex. 1007) issued on March 28, 2000 and is prior art under §102(b).
- **Nishizawa**: U.S. Patent No. 5,384,476 to Nishizawa et al. (Ex. 1046) issued on January 24, 1995 and is prior art under §102(b).

B. Relief Requested

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are

¹ Citations to §§102/103 are to the pre-America Invents Act (pre-AIA) versions.

supported by the declaration of Dr. Campbell (Ex.1003).

Ground	Basis	Challenged Claims	Reference(s)
I	§ 103	44	Onoda
II	§ 103	44	Onoda and Nishizawa
III	§ 103	44	Kawagoe

V. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) of the subject matter of the ’222 Patent would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. (Ex. 1003, ¶ 17.) Additional education might compensate for a deficiency in experience, and vice-versa. *Id.*

VI. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). No terms need to be construed to resolve the issues presented in this Petition.²

² The Eastern District of Texas construed “single drift layer . . . having a graded concentration of dopants . . . said drift layer further having a first static unidirectional electric drift field” as “single drift layer . . . having a concentration of dopants at the interface of the single drift layer and surface layer that is different than the

The ‘222 Patent issued from U.S. Application No. 16/947,294 filed on July 27, 2020 and is the sixth generation child continuation application of U.S. Application No. 11/622,496 filed January 12, 2007 which was issued as U.S. Patent No. 8,421,195 (‘195 Patent) via the following five intermediate continuation applications between the ‘222 Patent and the ‘195 Patent in the sequential order of their filing dates at the USPTO:

1. U.S. Application No. 13/854,319 filed on April 1, 2013, which is a continuation application of U.S. Application No. 11/622,496 for the ‘195 Patent, and was abandoned for failure to responding an office action;

2. U.S. Application No. 14/515,584 filed October 16, 2014 is a continuation application of the above-referenced U.S. Application No. 13/854,319 and is issued as U.S. Patent No. 9,190,502;

3. U.S. Application No. 14/931,636 filed November 3, 2015 is a continuation application of the above-referenced U.S. Application No. 14/515,584 and is issued as U. S. Patent No. 9,647,070;

4. U.S. Application No. 15/590,282 filed May 9, 2017 is a continuation

concentration of dopants at the interface of the single drift layer and the substrate . . . said drift layer further having a first static unidirectional electric drift field.” Ex. 1019 at 17 (*Greenthread, LLC v. Samsung Electronics Co., Ltd.*, et al., Case No. 2:19-cv-00147-JRG (Dkt. 67) (April 20, 2020).) Whether or not this construction is proper is not material to institution, and no construction need be entered.

application of the above-referenced U.S. Application No. 14/931,636 and is issued as U. S. Patent No. 10,510,842; and

5. U.S. Application No. 16/717,950 filed December 17, 2019 is a continuation application of the above-referenced U.S. Application No. 14/931,636 and is issued as U. S. Patent No. 10,734,481.³

In the above chain of priorities, the U.S. Application No. 16/947,294 for the '222 Patent is a continuation application of the above-referenced U.S. Application No. 16/717,950.

The file history of the '195 Patent shows that the originally filed specification of the '195 Patent does not use or mention the claim terms of “surface layer” and “drift layer”/ “single drift layer.” (Ex. 1002 at 8) *See*, for example, the published patent publication No. US20070158790A1 which is the original filed application for the '195 Patent. On May 14, 2010, Patent Owner added new claims to the application of the '195 Patent that became the patented claims in a response to the 4th, final office action dated Dec. 30, 2009 by introducing the above claim terms. The challenged Claim 44 recites “a surface layer” and “a single drift layer” as claim limitations.

In the Intel Litigation, Patent Owner took positions on the meaning of certain claim terms, which are listed below. (*Greenthread, LLC v. Intel Corp. et al.*, Case No. 6:22-cv-00105, Dkt. 96, Ex. Ex. 1030.).

³ Petitioner has also filed an IPR petition against the '195 Patent under PTAB Case No. IPR2024-00468 and an IPR petition against the U.S. Patent No. 9,190,502 under PTAB Case No. IPR2024-00469.

Claim Term	Patent Owner’s Proposed Construction
“surface layer”	Plain and ordinary meaning (“a layer at the surface”) (Ex. 1030 at 9-15.)
“substrate”	Plain and ordinary meaning (“underlying layer”) (Ex. 1030 at 15-18.)
“active region”	Plain and ordinary meaning (“a doped silicon region at the surface of a semiconductor device where a transistor can be formed”) (Ex. 1030 at 19-20.)
“unidirectional electric drift field”	Plain and ordinary meaning (Ex. 1030 at 20-25.)
“to aid carrier movement from ... [to/towards] ...”	Plain and ordinary meaning (Ex. 1030 at 25-30.)
“well region”	Plain and ordinary meaning (“a doped region that surrounds the active region of a semiconductor device”) (Ex. 1030 at 30-31.)

In the Intel Litigation, the Court provided its “preliminary constructions” in advance of the claim construction hearing, in which the Court offered a “preliminary construction” of plain and ordinary meaning as to each of the above-listed terms.⁴ (*See* Ex. 1037 (Intel’s Ex. 1037).) Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition. Petitioner reserves the right to respond to any purported claim constructions that Patent Owner raises.

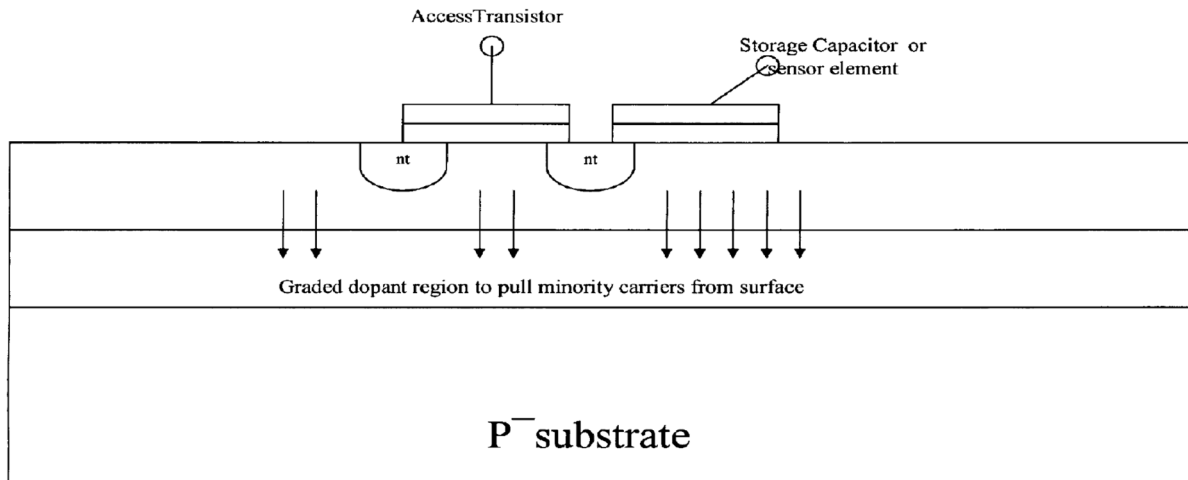
⁴ The court in the Western District of Texas did provide a note that the plain and ordinary meaning of well region does not include portions of a well. (Ex. 1037 at 4 (stating that “portions of a well are not well regions”).)

VII. THE '222 PATENT AND BACKGROUND

A. The '222 Patent's Purported Improvements

The '222 Patent is directed to a CMOS semiconductor device whose semiconductor layers have a graded dopant concentration that creates an electric drift field that sweeps minority carriers from the semiconductor's active region at the surface to its substrate. ('222 Patent at Abstract & 3:52-56.)

The '222 Patent states that some prior art bipolar junction transistors employed a graded dopant base to create an “‘aiding drift field’ to enhance the diffusing minority carrier’s speed from emitter to collector.” ('222 Patent at 1:46-48.) According to the '222 Patent, however, “most semiconductor devices ... still use a uniformly doped drift epitaxial region in the base.” (*Id.* at 1:48-53.) The '222 Patent claims the prior art semiconductor devices could be improved by providing a graded dopant region between the surface and the substrate to carry minority carriers from the surface to the substrate as quickly as possible (indicated by arrows in FIG. 5(b)). (*Id.* at 3:52-56; *see also id.* at 8:26-33; 2:4-35 (stating that the dopant gradient exists in the epitaxial layer).) This purported improvement is illustrated below from FIG. 5(b).)



(’222 Patent at FIG. 5(b).)

The ’222 Patent did not, however, use a new or unknown dopant profile to achieve the purported novelty. Rather, it utilized known doping techniques to known physical layers. (Ex. 1003 at ¶¶ 23, 25-28.). A POSITA would have understood that semiconductor layers and regions are doped to control their conductance and electric drift fields, including by using gradient doping profiles. (Id. at ¶ 27-31.) This was admitted as known by the ’222 Patent, at least with regard to the base portion of some prior art transistors (’222 Patent at 1:46-53; FIG. 1 (illustrating a doping impurity gradient in the base portion of a bipolar junction transistor that varies with depth)). In any event, the existence of, benefits from, and technologies necessary to achieve such gradient doping were known to a POSITA at the time, as the Patent Owner subsequently admitted during prosecution. Furthermore, when describing various dopant profiles that could be used (*e.g.*, “linear, quasi linear, exponential”), the ’222 Patent merely lists them as possible options (*id.* at 2:60), confirming that they were

known and that a POSITA would know how to implement them without further explanation.

The purported novelty in the '222 Patent is merely taking known doping techniques, applied to known layers, to create electric drift fields to diffuse minority carriers to a substrate. (Ex. 1003 at ¶¶ 27-31.) As demonstrated by Petitioner's prior art (Onoda, Nishizawa, and Kawagoe), all of this was well-known and obvious at the time of the purported invention.

B. General Background On Static Unidirectional Electric Drift Fields as Related to Semiconductor Layers Having Graded Dopant Profiles

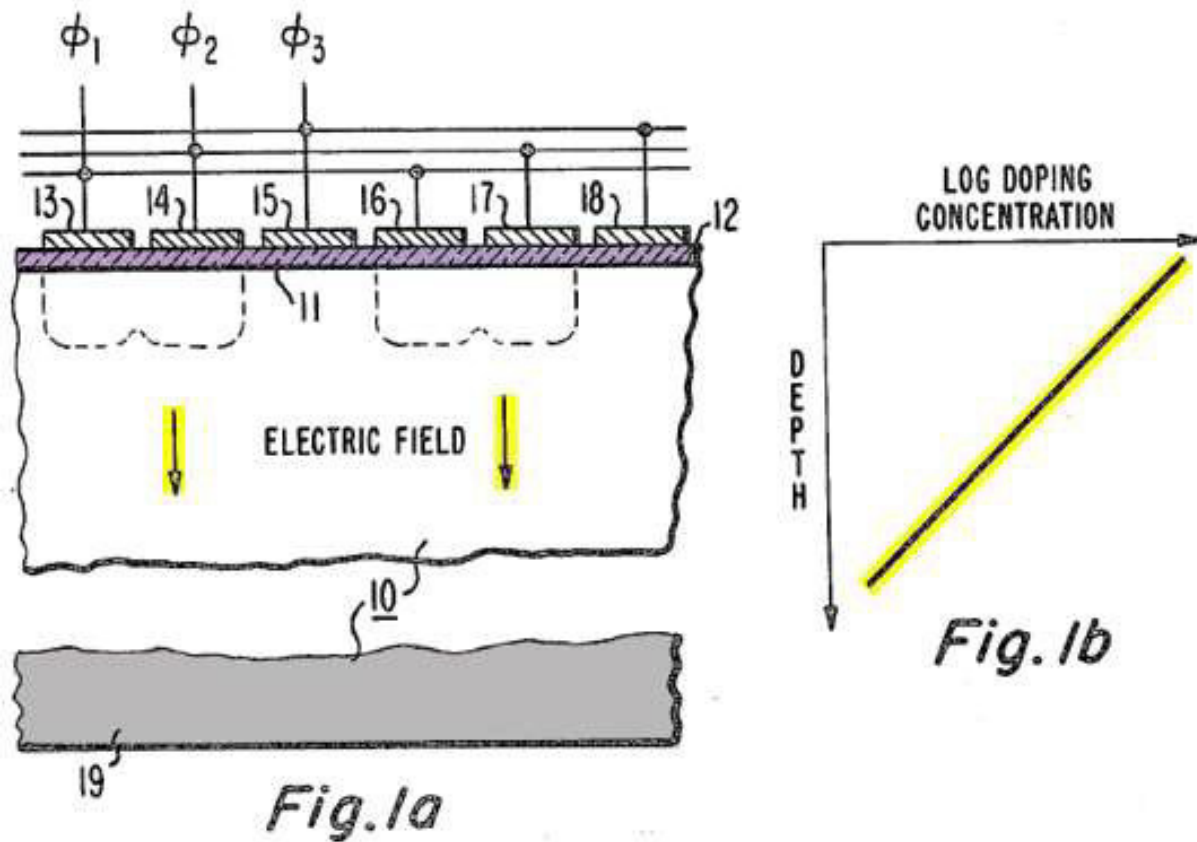
At the time of the alleged invention, Patent Owner represented that it was well-known that a graded dopant concentration creates a static unidirectional electric drift field. During prosecution of the '222 Patent's parent, U.S. Pat. No. 8,421,195, Patent Owner admitted that both upward and downward-sloping graded dopant concentrations were known and created an "inherent 'built-in' unidirectional electric field":

"[T]he graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carriers into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant."

(Ex. 1002 at 289-290 (underlining in original).)

Patent Owner further represented to the USPTO that "a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way...

Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept ‘down’ ... or ‘up...’” (Ex. 1002 at 289.) Patent Owner cited Jastrzebski in support. (*Id.* at 290.) In Jastrzebski, the graded-dopant concentration is “decreasing with depth” from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. (Ex. 1010 at 5:14-22.)

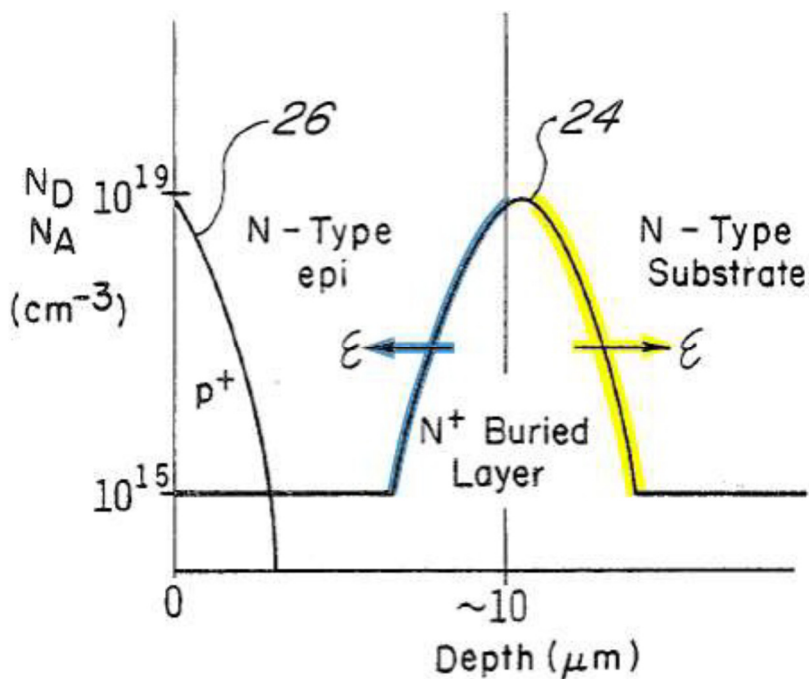


(Ex. 1010 at FIGS. 1a, 1b.)

Jastrzebski teaches that this downward-sloping graded-dopant concentration creates an electric drift field that “force[s] most of the charge carriers ... deep into the substrate[.]” (*Id.* at 5:14-22; *id.* at 2:27-32 (“This is done by creating a field, such as a drift field, in the semiconductor substrate to sweep minority charge carriers...into the

bulk [substrate], away from the electrode-bearing surface of the substrate.”).)

Patent Owner made the same representation to the Patent Office regarding the Kamins prior art. (Ex. 1002 at 237-238, 253-254.) According to Patent Owner, Kamins’ Figure 3 shows “two electrical fields with opposing directions” (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. (*Id.* at 237, 253 (citing Ex. 1009 at 3:6-13, FIGS. 2-3).)



(Ex. 1009 at FIG. 3.)

Patent Owner explained that Kamins “show[s] minority carrier[s] accelerated into the substrate.” (*Id.* (citing Ex. 1009, FIG. 2 and quoting Ex. 1009 at 3:6-13 (“carriers... accelerated... away from the surface... into the substrate”))).) According to Patent Owner, the electric field associated with the downward-sloping graded concentration at depth beyond $\sim 10 \mu\text{m}$ causes “[minority] carriers created [in that

region to be] ... accelerated into the substrate” (*Id.* (citing Ex. 1009 at 3:6-13, FIGS. 2-3); Ex. 1030 at 24 (Kamin’s “bottom electric field [(yellow)] draws a minority carrier from the substrate to a deeper part of the substrate.”); Ex. 1009 at 2:67-3:14 (“The non-uniform dopant concentration in the substrate creates electric fields in the substrate indicated by arrows labeled ‘ ϵ ’ in [Kamins’] FIGS. 2 and 3” such that “[minority] carriers created below the maximum dopant concentration are accelerated into the substrate.”), FIG. 2 (referring to these carriers as “photogenerated minority carriers”), 2:11-16 (same).)

Patent Owner also described “static,” and conceded that “Kamins (US 4,160,985), just like the ’222 Patent, discloses the presence of a ‘static’ drift field: ‘because the drift field is created by graded concentration of dopants which does not change over time.’” (Ex.1002 at 318 (citing Ex.1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and Ex.1002, 302- 03), 333 (same).)

C. Patent Owner’s Representation of Claim Scope

In a prior litigation against Intel, Patent Owner provided a description of the ’195 Patent’s claim terms with reference to its figures, which depict Patent Owner’s perceived claim scope. *See* Ex. 1030 (*Greenthread, LLC v. Intel Corp. et al.*, Case No. 6:22-cv-105-ADA). Provided below is a Patent-Owner-created graphic of claim 1 of the ’195 Patent. Claim 1 of the ’195 Patent is a near-identical match to claim 44 of the ’222 Patent.

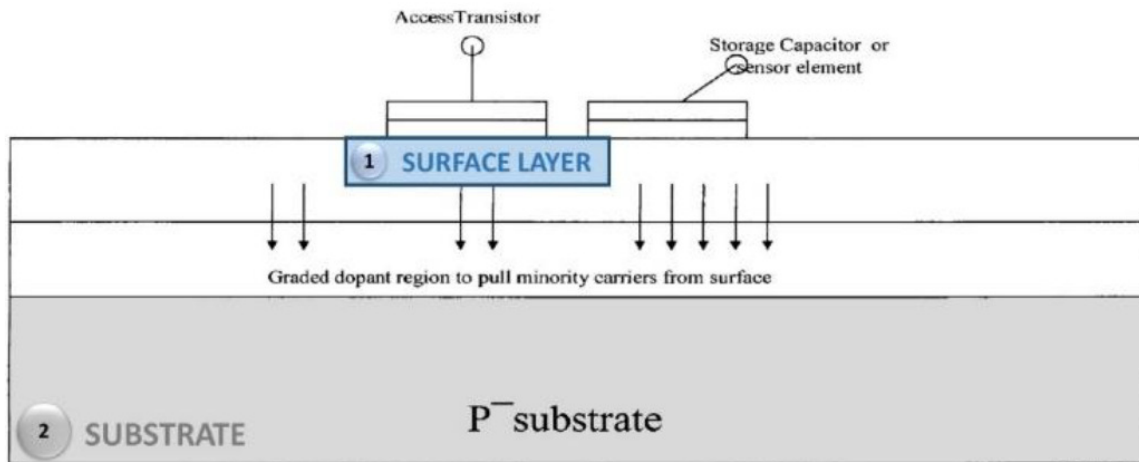
Term	U.S. Patent No. 8,421,195, Claim 1 (195:1)
1	A CMOS Semiconductor device comprising: a <u>surface layer</u> ;
2	a <u>substrate</u> ;
3	an <u>active region</u> including a source and a drain, disposed on one surface of said surface layer;
4	a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static <u>unidirectional electric drift field</u>
5	<u>to aid the movement of minority carriers from said surface layer to said substrate</u> ; and
6	at least one <u>well region</u> disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

(*Id.* at 5 (annotations by Patent Owner).) Shown below is claim 44 of the '222 Patent. The limitation of “said” in '195 Patent, claim 1, was changed to “the” in '222 Patent, Claim 44. Claim 44 further includes the limitation of “to the area of the substrate where there are no active regions” in (6) when claim 1 of the '195 Patent recited only substrate. These claims are substantively identical.

Term	U.S. Patent No. 11, 121,222, Claim 44
1	A CMOS semiconductor device comprising: a <u>surface layer</u> ;
2	a <u>substrate</u> ;
3	an <u>active region</u> including a source and a drain, disposed on one surface of the surface layer;

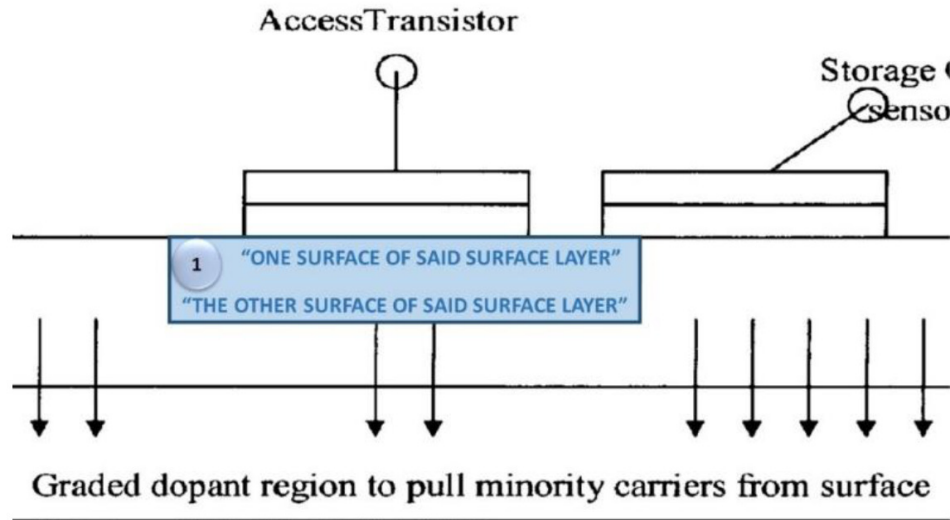
4	a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and
5	
6	at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

Patent Owner also annotated FIG. 5(b) to demonstrate each term's purported support. Shown below, Patent Owner identified a “surface layer” in blue and described it as “a layer at the surface of the silicon.” (*Id.* at 6.)



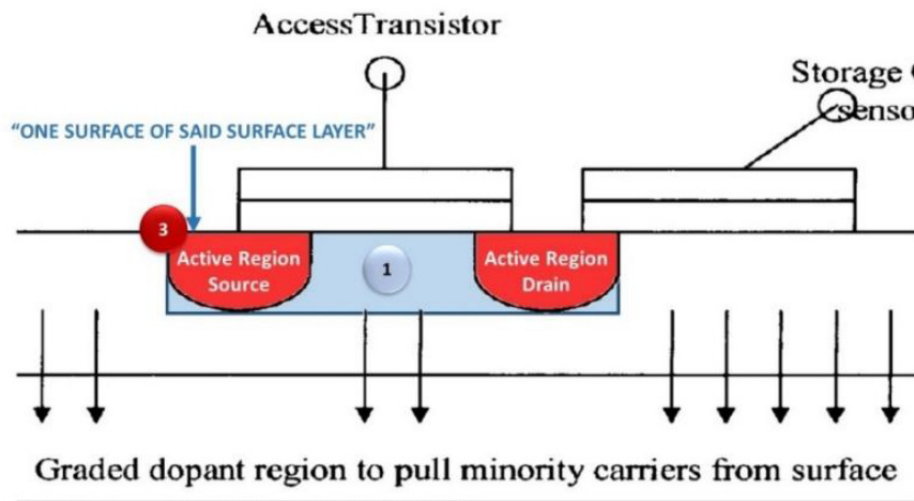
(*Id.* at 6 (annotations by Patent Owner).)

The “surface layer” as described by Patent Owner has two surfaces, “one surface” and “the other surface” each on opposite ends of the “surface layer.”



(*Id.* at 6 (annotations by Patent Owner).)

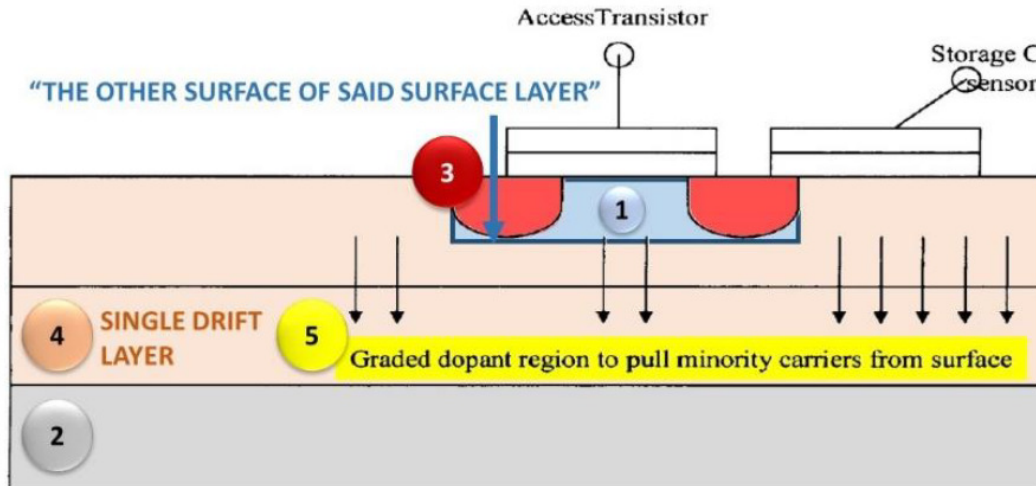
According to Patent Owner, “[t]he ‘active region’ is a doped region where a transistor can be formed” and is disposed on “one surface of said surface layer.” (*Id.* at 6.)



(*Id.* at 6 (annotations by Patent Owner).)

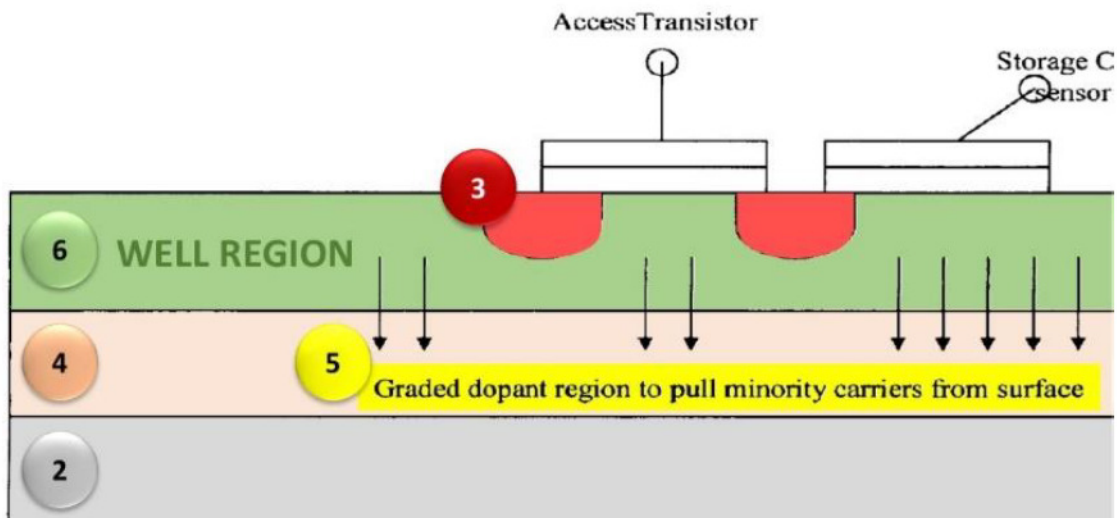
Patent Owner argued in claim construction that the “single drift layer [is] disposed between ‘the other surface of said surface layer’ and the substrate. The single

drift layer has a graded concentration of dopants” that “create an electric field that aids in the movement of minority carriers.” (*Id.* at 7.)



(*Id.* at 7 (annotations by Patent Owner).)

Finally, Patent Owner argued that “there is a well region disposed in the single drift layer.” (*Id.* at 7.) According to Patent Owner, “POSITAs normally use the term ‘well region’ to describe the doped silicon that surrounds the source and drain.” (*Id.* at 4.)



(*Id.* at 7 (annotations by Patent Owner).)

VIII. SPECIFIC GROUNDS⁵

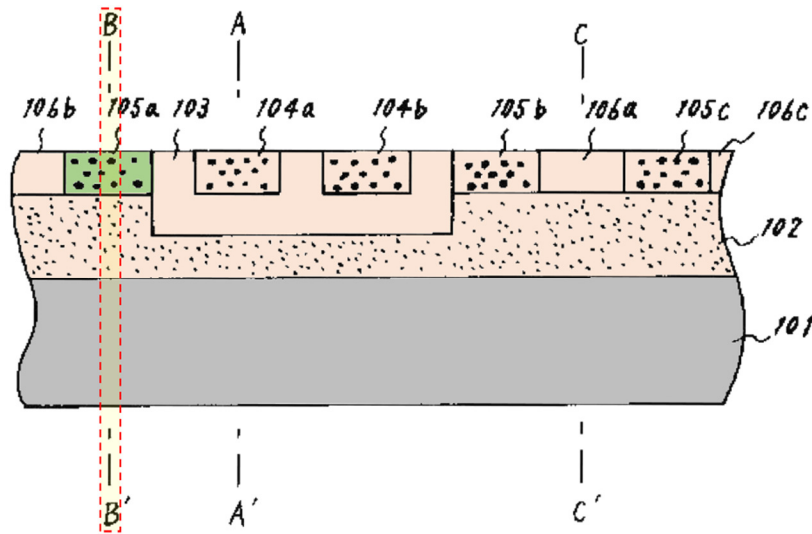
A. Ground I: Onoda Renders Obvious Claim 44.

1. Independent Claim 44

Onoda teaches a CMOS device that has a dopant profile where the dopant concentration gradually decreases from the surface of the device—through the epitaxial layer—to the substrate. This is depicted in the cross-sectional B-B' of FIG. 8 (shown in FIG. 11, both excerpted below), where the dopant gradient decreases from the surface, through the well-region (green),⁶ through the epitaxial layer 102 (tan), to the substrate 101 (grey). (Onoda at [0046]-[0047], [0052].)

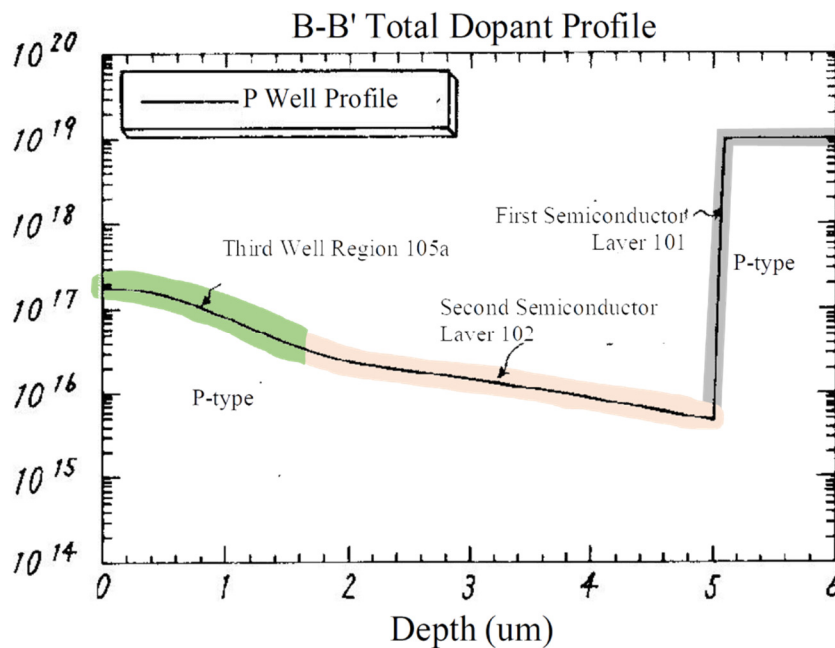
⁵ The specific grounds cite to the corresponding element of the '195 Patent in Dr. Campbell's declaration (Ex. 1003) unless otherwise stated.

⁶ There are several well regions; only a single one is emphasized and discussed in the grounds (*i.e.*, 105a).



(Onoda at FIG. 8.)

As can be seen from the below, the impurity concentration decreases from the surface to the substrate (the X-axis represents depth while the Y-axis represents concentration of impurities).



(Onoda at FIG. 11.)

The purported novelty of the '222 Patent matches Onoda's structure. Onoda's

dopant profile consists of two layers (105a and 102) that create a unidirectional electric field, where such a field would accelerate minority carrier electrons from the surface toward the substrate. (Ex. 1003 at ¶¶ 32-34, 72-83.) This matches the '222 Patent's purported improvement; it claims that the prior art was deficient because it purportedly provided uniformly doped epitaxial regions ('222 Patent at 1:46-53) while the purported invention provided—as an improvement—a graded dopant layer [or region] between the surface layer and the substrate to sweep unwanted minority carriers into the substrate. (*Id.* at 3:52-56.)

Onoda thusly renders obvious claim 44 as detailed below.

a. Preamble: “A CMOS Semiconductor device comprising:”

To the extent the preamble is limiting, Onoda discloses a CMOS semiconductor device.

Onoda discloses both N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the circuitry of its flash memory devices. (Onoda at [0052], [0044]-[0045], FIG. 2, Claim 2.) A POSITA would have understood this to disclose CMOS because: (a) CMOS is a complimentary pair of NMOS and PMOS transistors and (b) CMOS was at the time (and still is) the dominant fabrication technology used in memory devices. (Ex. 1003 at ¶¶ 55-57.) Onoda further mentions that one of the objectives of the invention “is to provide a semiconductor integrated device ... with improved resistance to latch-up” (*id.* at [0006]), which a POSITA would have

understood to be a problem of CMOS transistors. (Ex. 1003 at ¶ 56.)

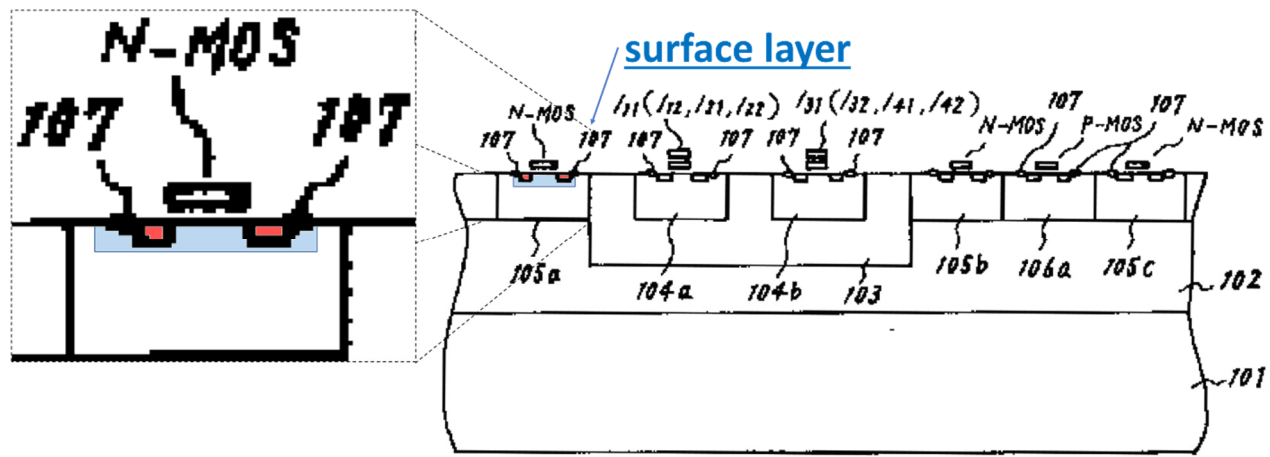
Furthermore, by the 1980s, CMOS had become the dominant IC fabrication technology and has remained so to the present day. (*Id.* at ¶ 55-57.) Flash memory devices have been fabricated almost exclusively with CMOS since at least the late 1980s. (*Id.*). Thus, when Onoda was published, a POSITA would understand its teachings to be directed to CMOS-based fabrication technologies and a POSITA would have thusly understood Onoda to disclose CMOS. (*Id.*)

To the extent Patent Owner argues that Onoda does not teach CMOS and that the preamble is limiting, it would have nonetheless been obvious to employ the teachings of Onoda to CMOS devices. CMOS devices are complimentary MOS devices, which use complimentary NMOS and PMOS transistors, and Onoda teaches a single device with both. (Onoda at FIG. 3.) A POSITA would have found it obvious to apply Onoda's teachings in a well-known CMOS structure, which is almost universally used in memory devices. (Ex. 1003 at ¶ 57.) A POSITA would have found it obvious to try, would have yielded predictable results, and would have been the application of known techniques to achieve those results. (*Id.*)

b. Element [44.1]: “a surface layer;”

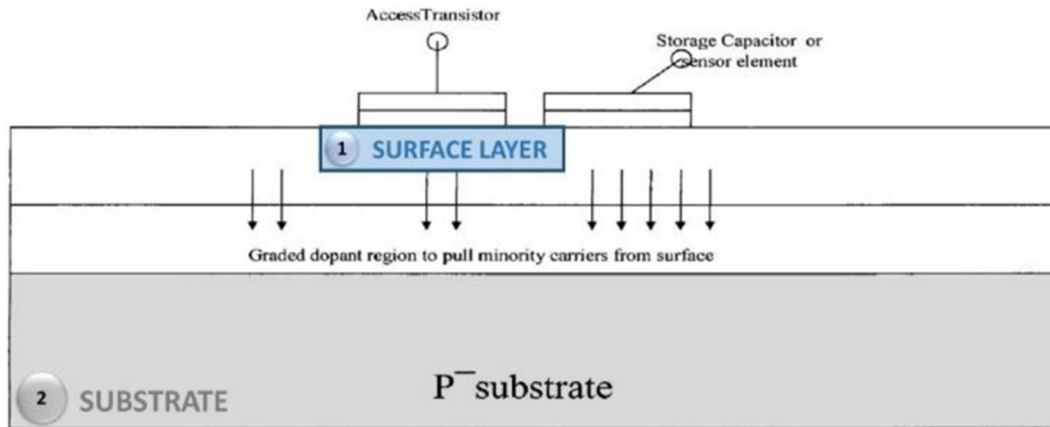
Onoda teaches a surface layer (annotated blue, below). Onoda's surface layer is shown below in a region of the NMOS transistor (excerpted below) within the doped p-well region 105a, where the well has source/drain regions (the active region discussed in more detail in Element [44.3]). (Onoda at [0043] (“105a, 105b, and 105c

are P-type [] well regions”); *see also id.* at [0044], Claim 2 (“floating gate electrode formed over the second well region, positioned between the source region and the drain region”).) As can be seen from the below, Onoda’s surface layer is at the surface of semiconductor substrate 100, and the source and drain regions (red) of Onoda’s transistors are in that layer. (Ex. 1003 at ¶¶ 58-59.)



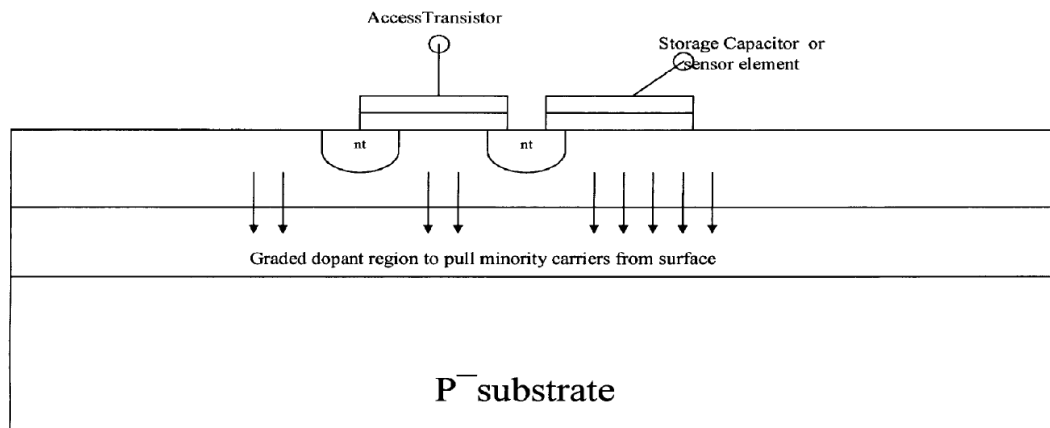
(Onoda at FIG. 3.)

Onoda’s teaching of the “surface layer” matches Patent Owner’s articulation of the ’222 Patent’s claim scope. Patent Owner annotated FIG. 5(b) to depict its purported scope of “surface layer” (the region surrounding the active region), and further argued in construction that the “surface layer” refers to “a layer at the surface of the silicon.” (Ex. 1030 at 13.) This matches Onoda’s teachings.



(Ex. 1030 at 6 (annotations to FIG. 5(b) of the '222 Patent by Patent Owner).)

Patent Owner annotated over FIG. 5(b) obscuring some regions (*e.g.*, the source / drain); a non-annotated version of the '222 Patent is excerpted below, which illustrates the active region.



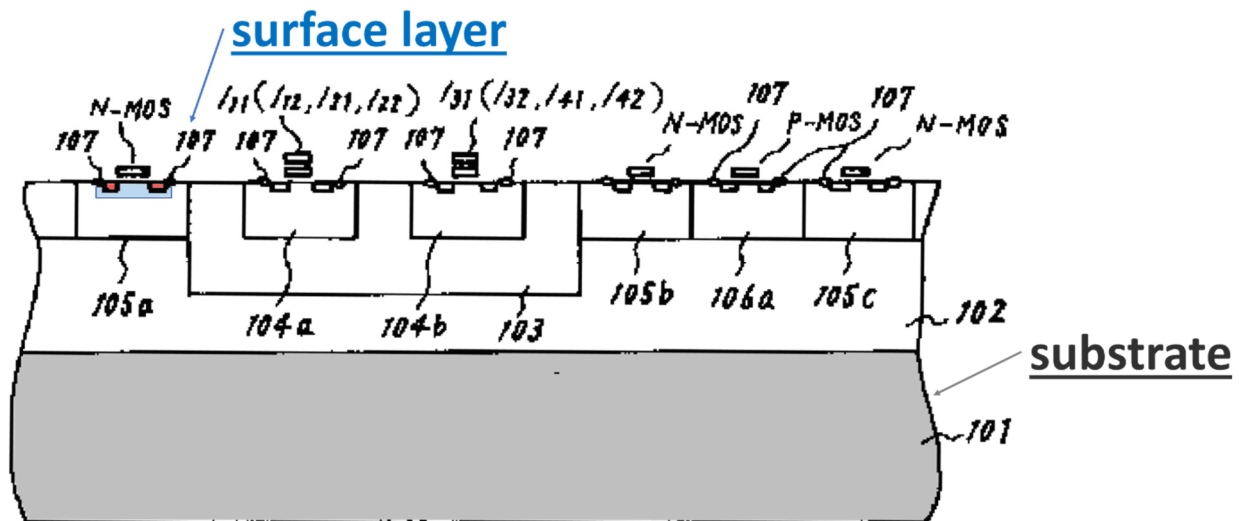
('222 Patent at FIG. 5(b).)

Onoda teaches the “surface layer” in an identical manner as described by the '222 Patent’s purported written description support of this same limitation, and thusly discloses Element [44.1].

c. Element [44.2]: “a substrate;”

Onoda discloses this element.

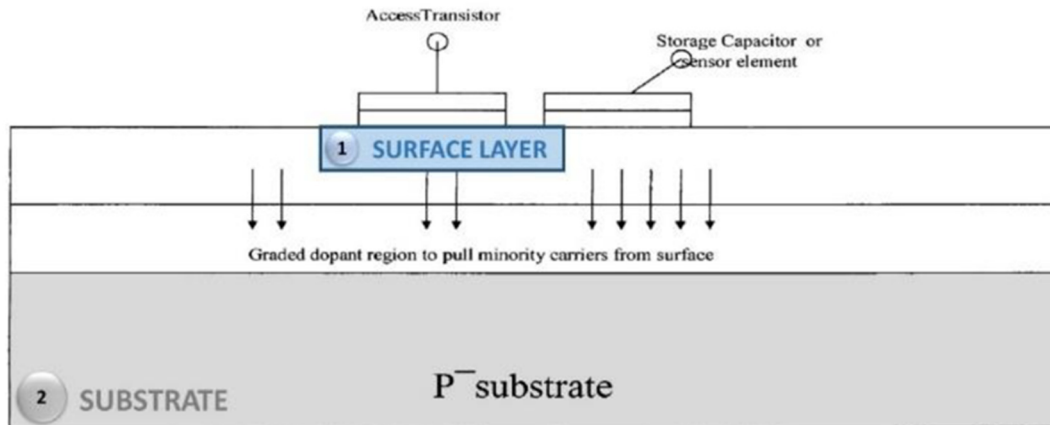
Onoda discloses “a semiconductor substrate 100” on which the flash memory is formed. (Onoda at [0041] (“FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention”).) Within the semiconductor substrate is element 101 (annotated grey, below), which “is a first semiconductor layer made from a heavily-doped ... P-type silicon substrate.” (*Id.*). Shown below is FIG. 3 with element 101, the “p-type silicon substrate” (annotated in grey). (*Id.* at [0041]; *see also id.* at “Brief Description of the Drawings” describing FIGS. 1 through 14 as describing features of the “first embodiment.”)



(Onoda at FIG. 3.)

Similar to the “surface layer,” Onoda’s teaching of the “substrate” matches Patent Owner’s district court claim construction, where it construed the “substrate” as “an underlying layer.” (Ex. 1030 at 15.) Patent Owner’s annotations to FIG. 5(b) of

the '222 Patent are below.



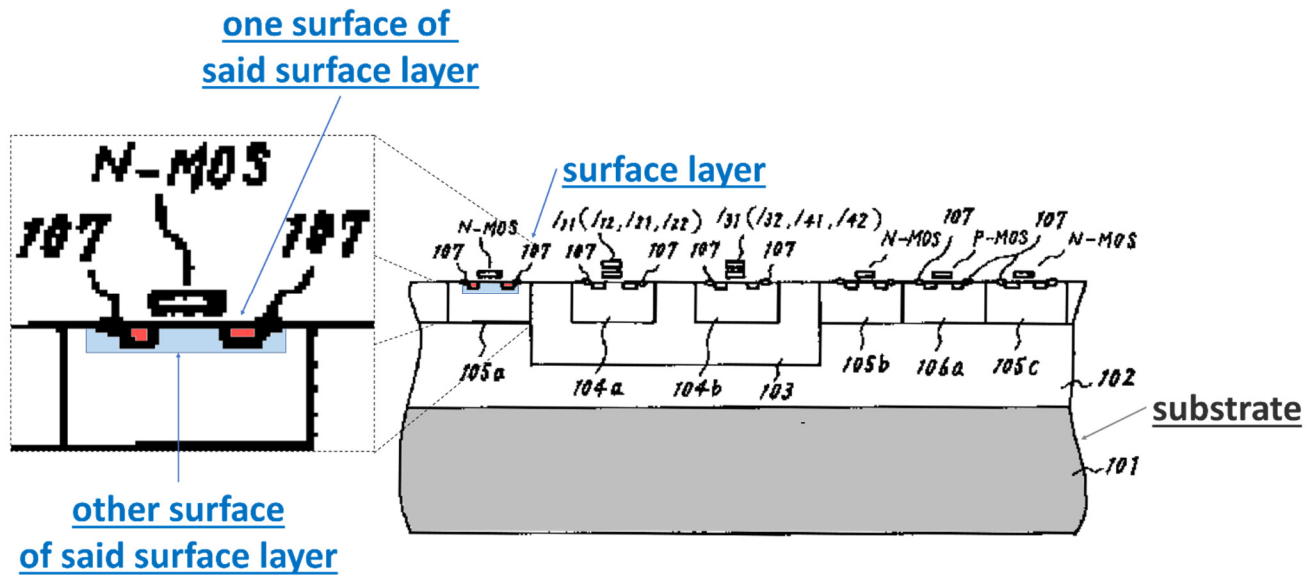
((Ex. 1030 at 6) (annotations by Patent Owner).)

Onoda thusly discloses Element [44.2].

d. Element [44.3]: “an active region including a source and a drain, disposed on one surface of the surface layer;”

Onoda discloses this element.

As depicted in annotated FIG. 3 below, the surface layer contains a source and drain which form an active region. (Onoda at [0029] (“each a memory cell having a source region comprising an N-type diffusion layer, a drain region comprising an N-type diffusion layer that is separate from the source region, a floating electrode formed over a channel region that is positioned between the source region and the drain region, with a gate oxide film, comprising a tunnel oxide film, interposed therebetween, and a control gate electrode disposed facing the floating gate electrode with an interlayer insulating films interposed therebetween.”), [0043] (“105a, 105b, and 105c are P-type [] well regions”); *see also id.* at [0044], Claim 2 (“floating gate electrode formed over the second well region, positioned between the source region and the drain region”).)



other surface
of said surface layer

(Onoda at FIG. 3 (active region called out for greater emphasis).)

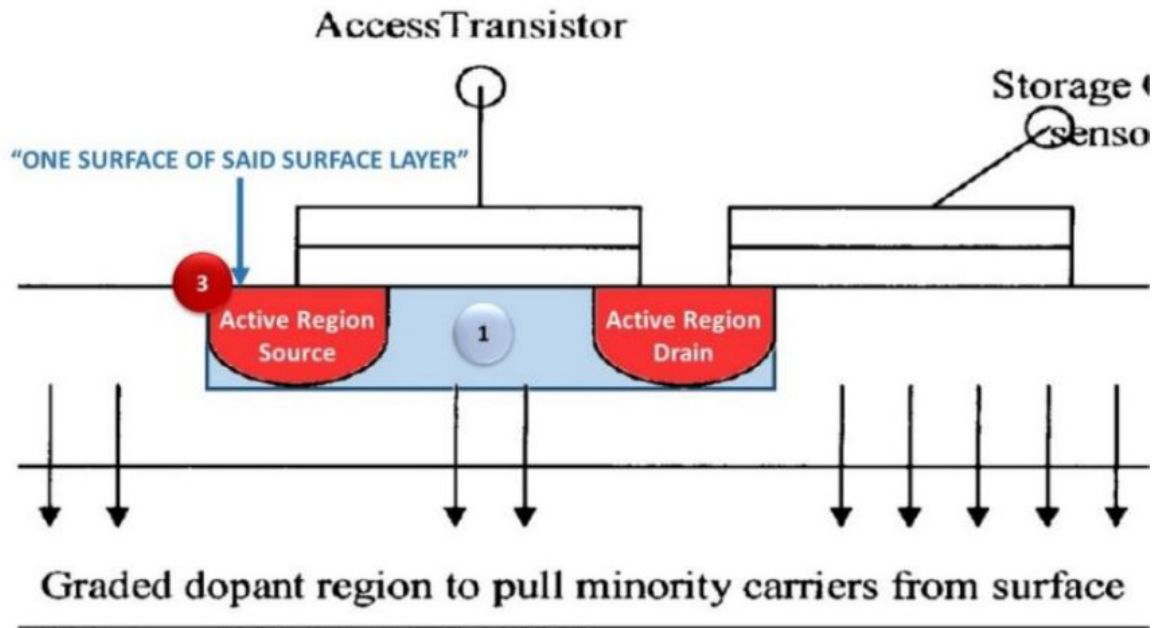
The active region is disposed to the top surface of the surface layer, *i.e.*, the claimed “one surface on the surface layer.” (Ex. 1003 at ¶¶ 62-65.) This orientation—and discussion of each respective region—matches Patent Owner’s articulation during claim construction in the district court. There, Patent Owner likened the orientation to a ceiling fan in a room, stating:

“By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the ceiling fan is spinning around like a propeller on the roof of the house. Instead it means that the ceiling fan is hanging from the ceiling *inside* the room. The same is true about the active region and the surface layer.”

(Ex. 1030 at 11 (emphasis added).)

Patent Owner further annotated FIG. 5(b) of the '222 Patent to depict this

orientation, where the active region source and drains were disposed on the surface of the surface layer (similar to Onoda's FIG. 3). (Ex. 1003 at ¶¶ 63-64.)



((Ex. 1030 at 7) (annotations by Patent Owner).)

Onoda thusly teaches the “an active region including a source and a drain, disposed on one surface of the surface layer.”

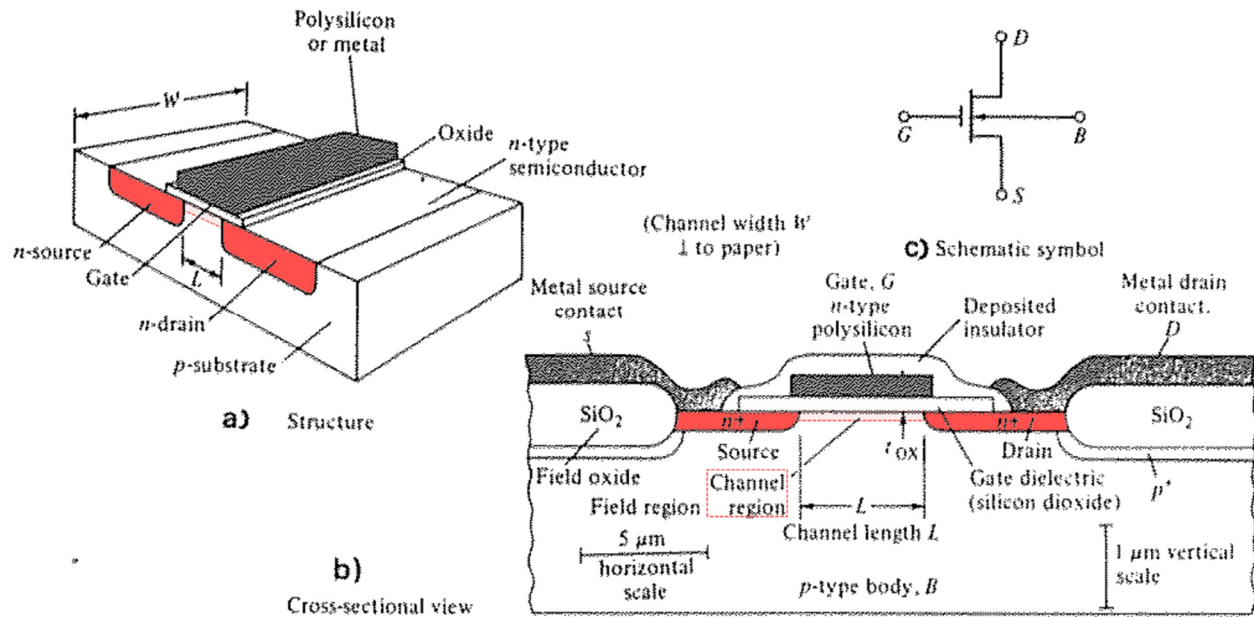
Furthermore, a POSITA would have understood that the above-described source and drain configurations of Onoda disclose an active region. (Ex. 1003 at ¶ 64.) As depicted in the enlarged excerpt of FIG. 3, below, a charge applied to gate electrode (annotated yellow, *see, e.g.*, Onoda at [0029] (“a floating electrode formed over a channel region that is positioned between the source region and the drain region”)) causes a conductive channel (annotated in dashed-red) to form between the source and drain. (Ex. 1003 at ¶¶ 64-65.) A POSITA would understand the source, drain, and

channel to be an active region. (*Id.*)



(Onoda at FIG. 3 (Excerpted).)

This understanding of source, gate, drain, and transistor operation is confirmed via *Wolf and Tauber*, *Silicon Processing For The VLSI Era*, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor is “[its] channel and [its] heavily doped source and drain regions.” (Ex. 1008 at 299; *see also* Ex. 1030 at 4-5 (Patent Owner acknowledging that a channel is formed between a source and drain to form an active region).)



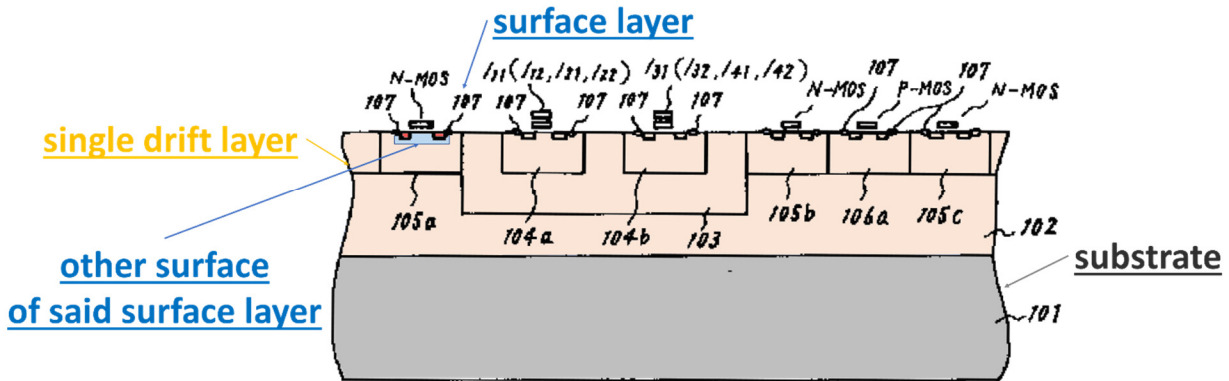
(Ex. 1008B at FIG. 5-1.)

Onoda thusly discloses Element [44.3].

- e. **Element [44.4]: “a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,”**

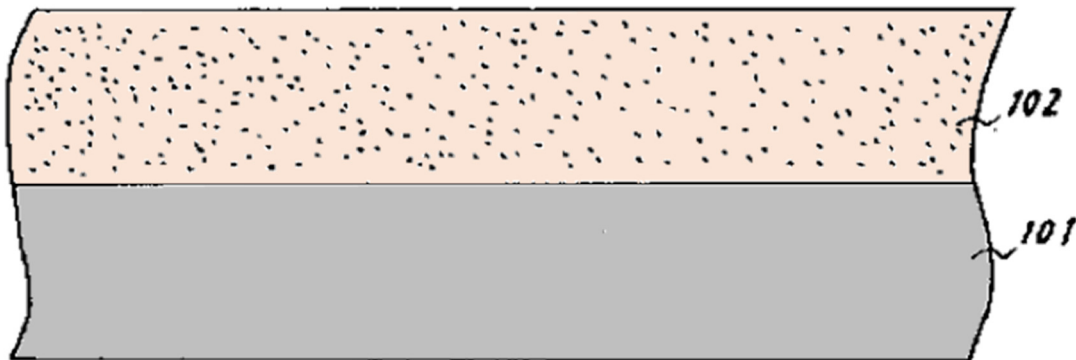
Onoda discloses this limitation.

Onoda discloses a single drift layer. In Onoda’s FIG. 3, the second semiconductor layer 102 is an example of the claimed single drift layer (annotated tan, below). This single drift layer is “disposed between the “other surface of the surface layer” (the bottom surface) and the “substrate.”



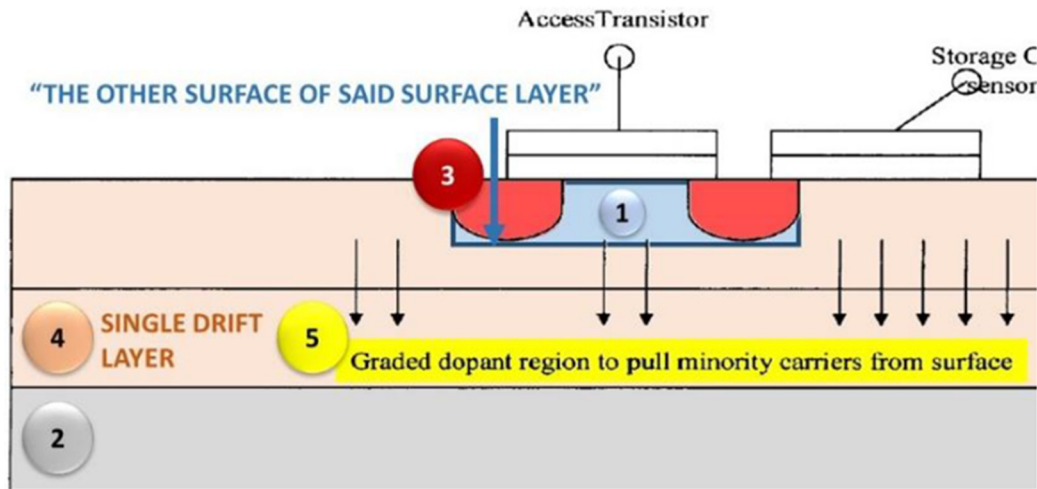
(Onoda at FIG. 3.)

The single drift layer is demonstrated in the intermediate processing step of FIG. 5, below, prior to well formation. (Onoda at [0047]; *see also id.* at FIGS. 10-12 (showing final dopant profiles); *see also id.* at [0041]-[0051].)



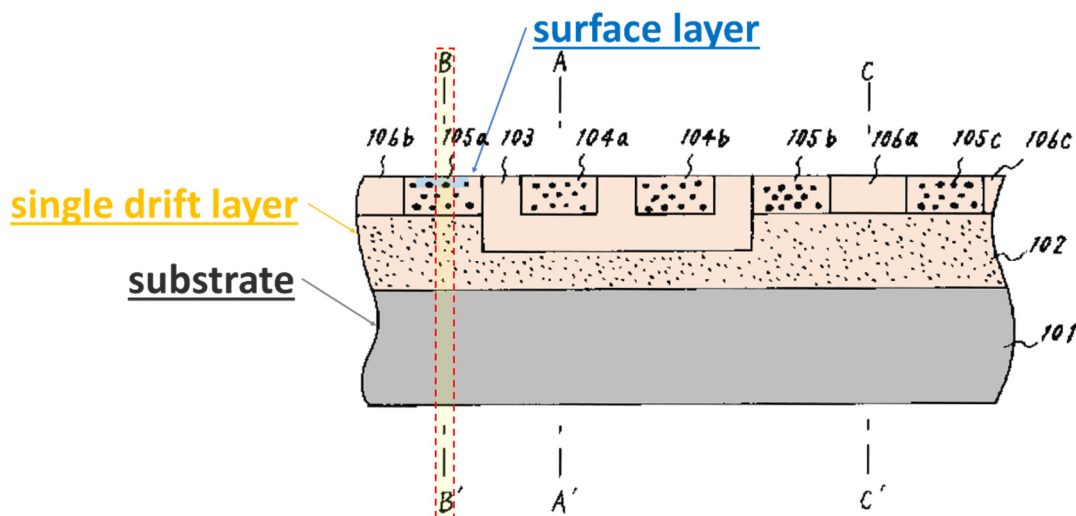
(Onoda at FIG. 5.)

Onoda's teachings further match Patent Owner's district court claim construction annotations to FIG. 5(b) of the '222 Patent. There, Patent Owner provided annotations demonstrating the position of the single drift layer in relationship to the surface layer's other surface and the substrate, where the single drift layer was below the surface layer.

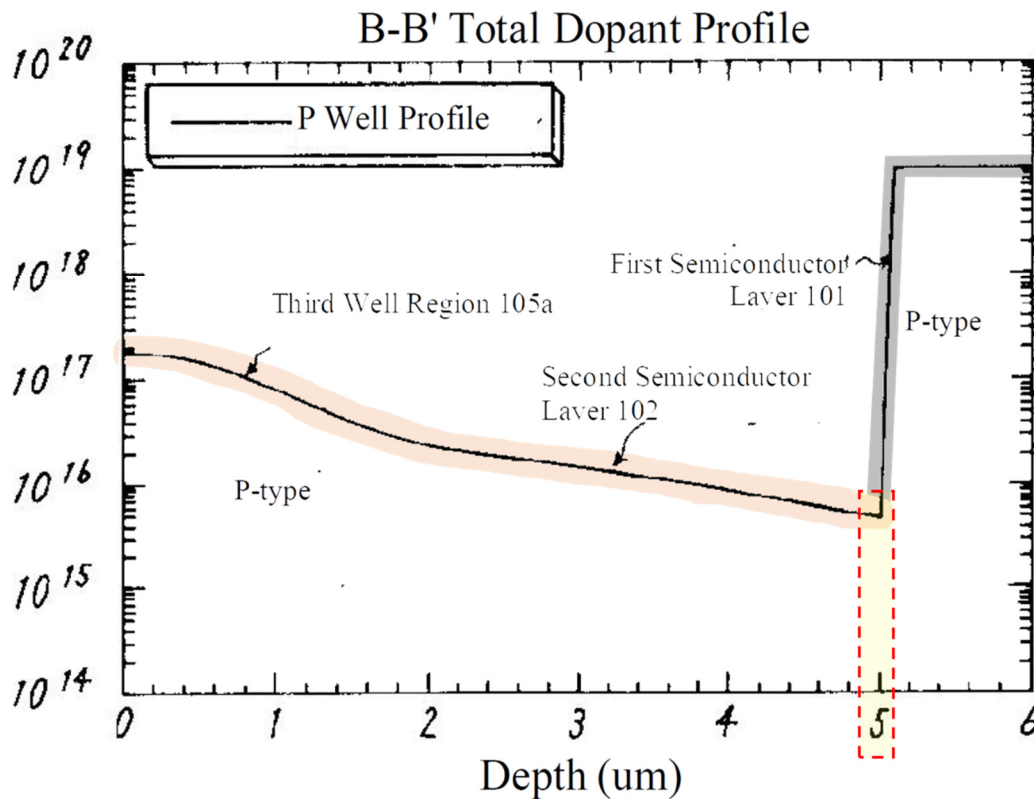


((Ex. 1030 at 7) (annotations by Patent Owner).)

Onoda's single drift layer further has a graded concentration of dopants extending between the surface layer and the substrate. FIG. 8 depicts the semiconductor device of Onoda, and FIG. 11 demonstrates that device's dopant profile of the portion marked as B-B' (cross-section annotated yellow). (Onoda at [0052].)



(Onoda at FIG. 8.)



(Onoda at FIG. 11.)

Comparing the two figures, Onoda's semiconductor device has a dopant profile whose impurities decrease from the surface, *i.e.*, depth 0, to the substrate, *i.e.*, depth of 5 μm . (Onoda at [0046] (stating that the p-type epitaxial layer 102 has a thickness of about 5 μm); *see also id.* at [0052] ("both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly"); *see also id.* at [0047] (describing doping layer 102), [0048]-[0050] (stating how wells are created, which is discussed in further detail in Element [44.6]).) And, to create the gradient, Onoda describes implanting dopants and thereafter thermally diffusing them. (*Id.* at [0047]-

[0050]). Onoda thusly discloses a dopant profile with a downward doping gradient from the surface to the substrate. (Ex. 1003 at ¶¶ 66-71.)

Onoda thusly discloses Element [44.4].

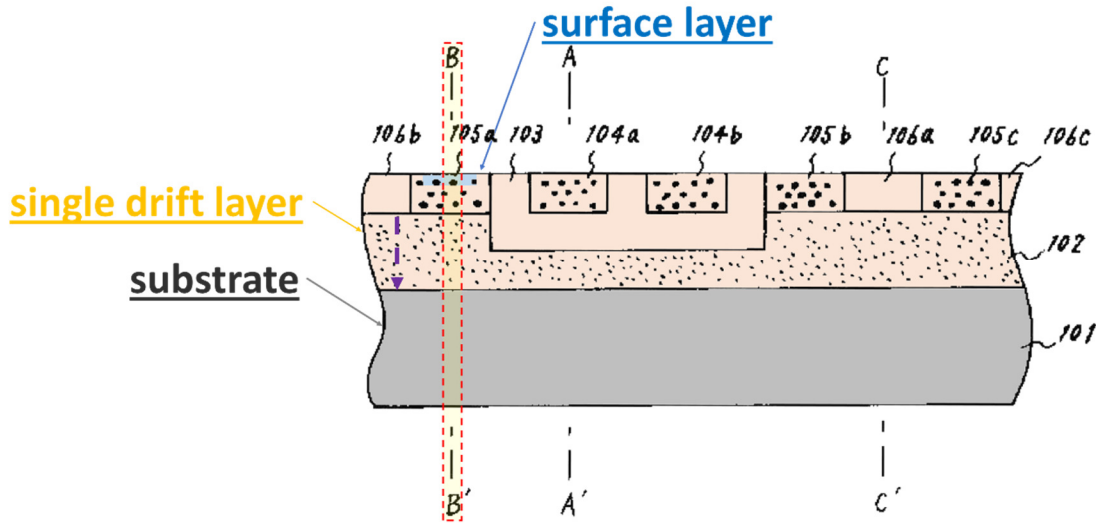
- f. Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”**

Onoda teaches this element.

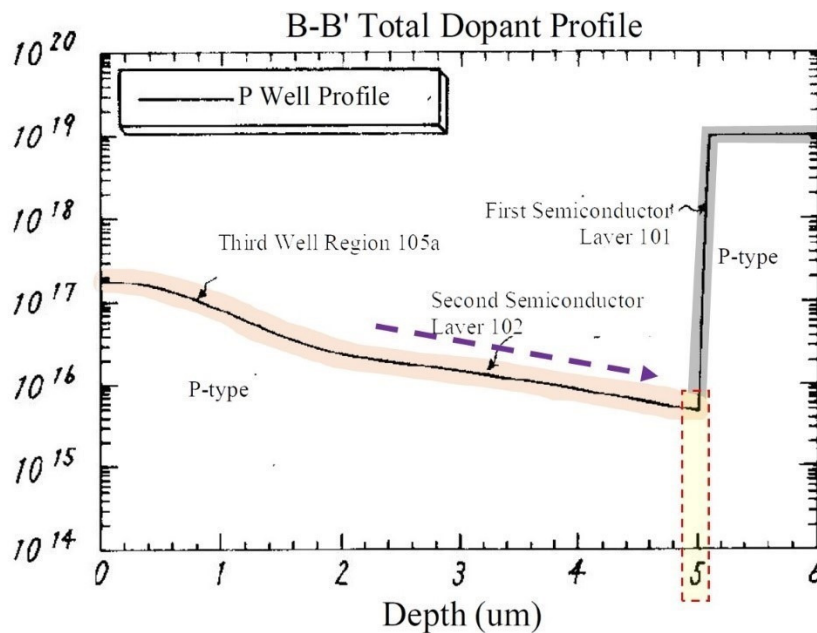
As discussed above with regard to Element [44.4], Onoda discloses a single drift layer (tan) having a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (gray, starting at the 5 μm depth level).

The below annotation of Onoda’s FIGS. 8 and 11 depicts the first static unidirectional electric drift field (purple arrow)⁷ that aids in the movement of minority carriers from the surface to the substrate, at a depth corresponding to Onoda’s second semiconductor layer 102 (tan). As can be seen in FIG.8, there is no active region in the substrate area. (Ex. 1003 at ¶ 141.)

⁷ The arrow indicates the movement of minority carriers from the surface layer to the substrate. (Ex. 1003 at ¶¶ 72-74). A POSITA would understand that the field would be in the opposite direction. (*Id.*)



(Onoda at FIG. 8.)



(Onoda at FIG. 11.)

As Patent Owner conceded during prosecution, a POSITA would have further understood that a downward-sloping graded-dopant concentration creates an inherent built-in unidirectional electric drift field to aid the movement of minority carriers. As detailed in section VII.B at pages 9-13, the Patent Owner in prosecution described a

downward graded dopant profile as providing an “inherent ‘built-in’ unidirectional electric field” that moves carriers into the substrate. (*Supra* 9.) Moreover, a POSITA would have understood this to be an inherent property of a downward sloping doping gradient. (Ex. 1003 at ¶ 73)

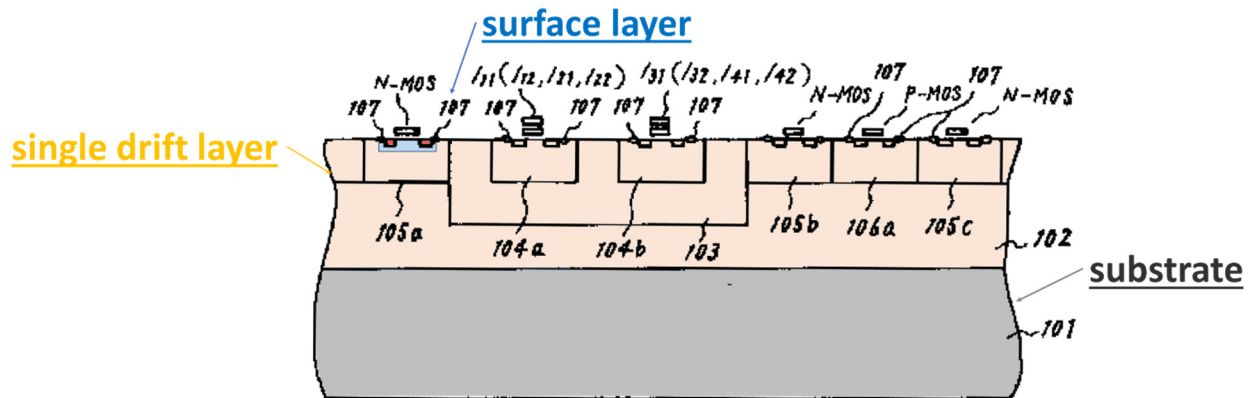
Furthermore, the static unidirectional electric drift field would have been understood to be static. (*Id.* at 74.) As discussed in [44.4], the dopant profile is created through ion implantation and thermal diffusion techniques and is thusly set once the device has been fabricated. (Onoda at [0047]-[0050]; *see also* Ex. 1003 at ¶¶ 66-71, 74.) In other words, this would have understood to be static to a POSITA. (Ex. 1003 at ¶ 74.) Patent Owner also described “static” similarly during prosecution, stating that a semiconductor device with a fabricated dopant profile provides a static unidirectional electric field. (Ex. 1002 at 318 (citing Ex. 1009), 333.) Consequently, A POSITA would have understood Onoda’s downward sloping gradient to provide a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. (Ex. 1003 at ¶¶ 72-74.)

Onoda thusly discloses Element [44.5].

- g. Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”**

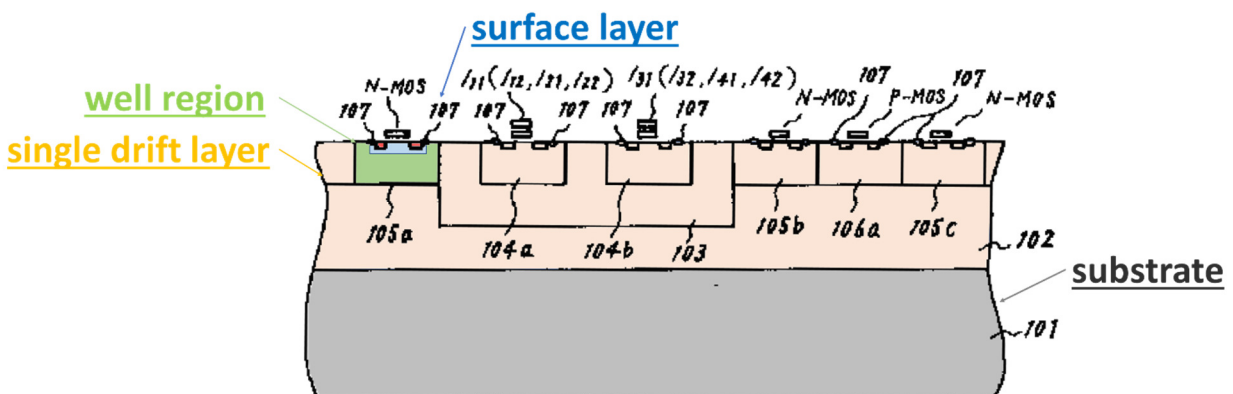
Onoda discloses this element.

Onoda discloses a well region disposed in the single drift layer. As described in Element [44.4], Onoda has a single drift layer (epitaxial layer 102, tan). (*See also* Onoda at [0046].)



(Onoda at FIG. 3.)

As shown below, disposed within that single drift layer is a well region (green) which is within the claimed single drift layer. (Onoda at [0042] (“105a, 105b, and 105c are P-type third well regions formed in the surface of the second semiconductor layer 102”); *see also id.* at [0044] (“the plurality of N-channel MOS transistors is formed in the third well regions 105a, 105b, 105c.”).) Yet there is no active region in the substrate area. (Ex. 1003 ¶ 142)

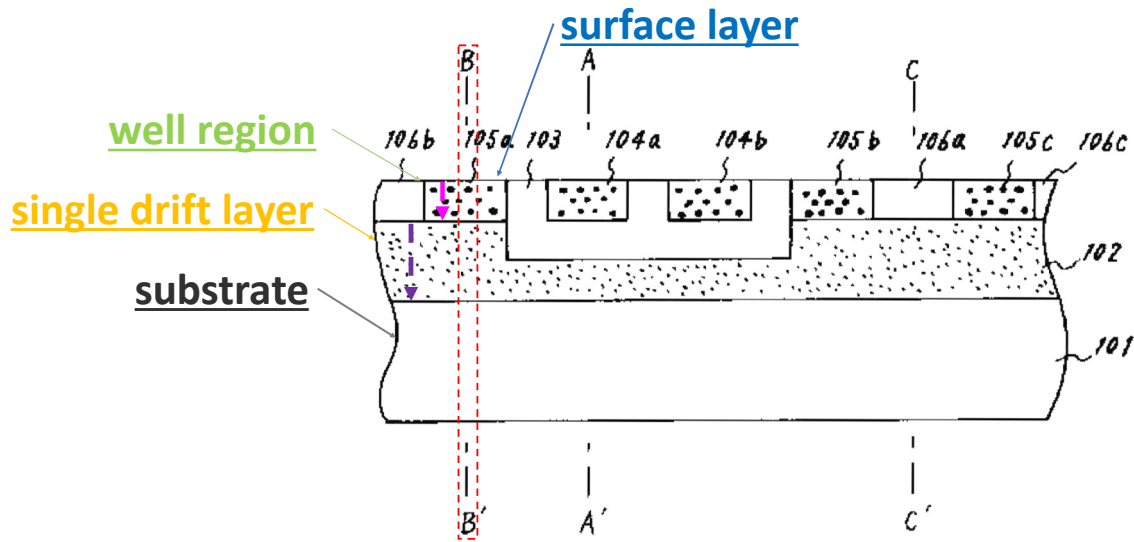


(Onoda at FIG. 3.)

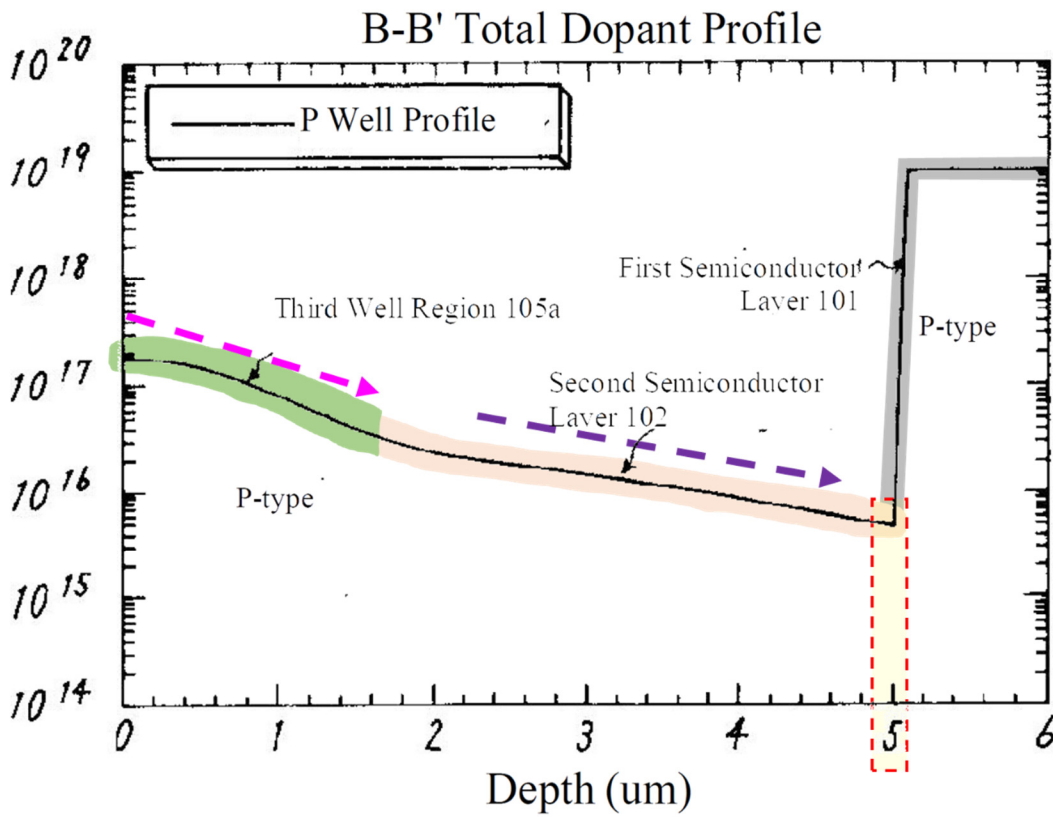
Onoda discloses the steps to form the P-wells and the N-wells (including the exemplary claimed “well region”) in the lightly-doped semiconductor layer 102. (Onoda at [0048]-[0050].) After forming the epitaxial second semiconductor layer 102, an N-type dopant (*e.g.*, phosphorus P) is implanted and heat treatment is carried out to form an N-type first well region 103 with a depth of about 3 μm . (*Id.* at [0048].) Thereafter, a P-type dopant (*e.g.*, boron B) is implanted to form P-type implantation layers 104a, 104b and 105a through 105c, and an N-type dopant is implanted to form N-type implantation layers 106a through 106c. (*Id.* at [0049].) Finally, after carrying out heat treatment, P-type second well regions 104a and 104b, P-type third well regions 105a through 105c, and N-type fourth well regions 106a through 106c are formed in the second semiconductor layer 102, as illustrated in Figure 8 below. (*Id.* at [0050].) The well formation is depicted in FIG. 8, where P-well regions 105a, 105b, 105c, 104a and 104b and N-well regions 103, 106a, 106b and 106c are formed in semiconductor layer 102. (*Id.* at [0042], [0048]-[0050].)

Onoda discloses that its well region has a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. As noted in Element [44.5], FIG. 11 depicts the gradient profile of cross-sectional B-B’ of FIG. 8 (annotated in yellow). (*See also* Onoda at [0052].) As can be seen below, the substrate has no active regions, and Onoda teaches that minority carriers move “to the area of the substrate where there are no

active regions.” Both figures are provided below.



(Onoda at FIG. 8.)



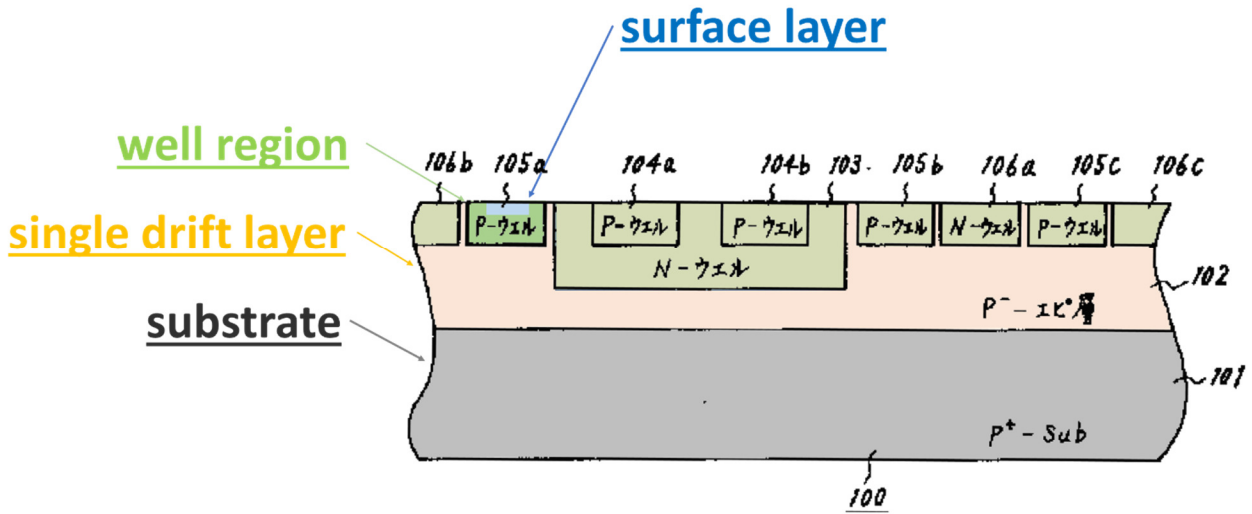
(Onoda at FIG. 11.)

As can be seen in the two figures, the well region 105a, like the “single drift layer” 102, has a dopant profile that has a downward sloping gradient. (Onoda at [0052].) The well region 105a has the claimed second static unidirectional electric drift field (*e.g.*, pink arrow)⁸ to aid the movement of minority carriers from said surface layer to said substrate for the same reasons as described in Element [44.5]. And, as detailed in section VII.B at pages 11-14, Patent Owner in prosecution described a downward graded dopant profile as providing an “inherent ‘built-in’ unidirectional electric field” that moves carriers into the substrate. (*Supra* at 11.) A POSITA would have understood Onoda’s dopant profile over the well region 105a to teach a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. (Ex. 1003 at ¶¶ 75-83.)

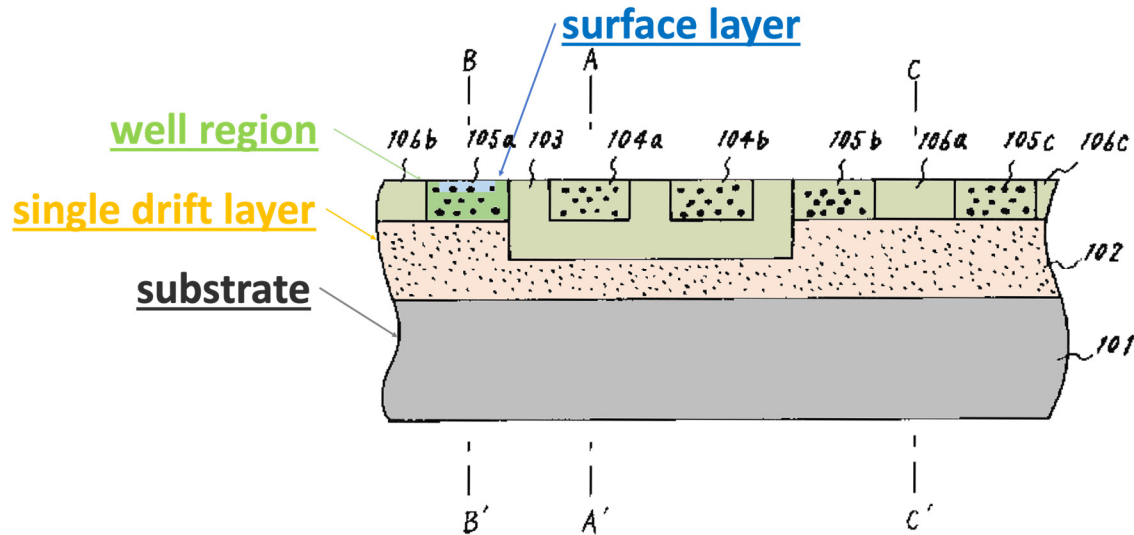
A singular well region (p well 105a) has been identified above. P well 105a is described in separate embodiments as: (1) being separated from other well regions; and (2) being part of a contiguous set of well regions. Under any possible perceived construction argument surrounding “well region,” it is taught by Onoda. First, FIG. 13 shows well region 105a as separated from others; it depicts well region 105a (dark green, below) encompassed within portions of the epitaxial layer 102 and separated from other well regions (light green). (Onoda at [0087] (stating that “the first well

⁸ The arrow denotes the drift of electrons (minority carriers) in the p-well. (Ex. 1003 at ¶ 79.)

region 103, third well region 105, and fourth well region 106 are separated from each other, that is, wherein the second semiconductor layer 102 is interposed between the well regions, as depicted in FIG. 13”); [0042] (generally describing the well regions 104a, 104b, 105a, 105b, 105c, 106a, 106b, 106c).)



(Onoda at FIG. 13.) Second, well region 105 (a) is part of a contiguous well structure, where the entire well region teaches the claimed “well region.” This is depicted in FIG. 8, below, with the well region 105a annotated in dark green and the other well regions annotated in light green. (See Onoda at FIG. 8; [0042] (generally describing the well regions 104a, 104b, 105a, 105b, 105c, 106a, 106b, 106c).)



(Onoda at FIG. 8.)

Finally, for the same reasons as described in Element [44.5], a POSITA would have understood Onoda's graded-dopant profile, including the dopant profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static. (Ex. 1003 at ¶¶ 75-83, 72-74; *see also* Onoda at [0048] (stating that the wells are doped and then dopants thermally diffused).)

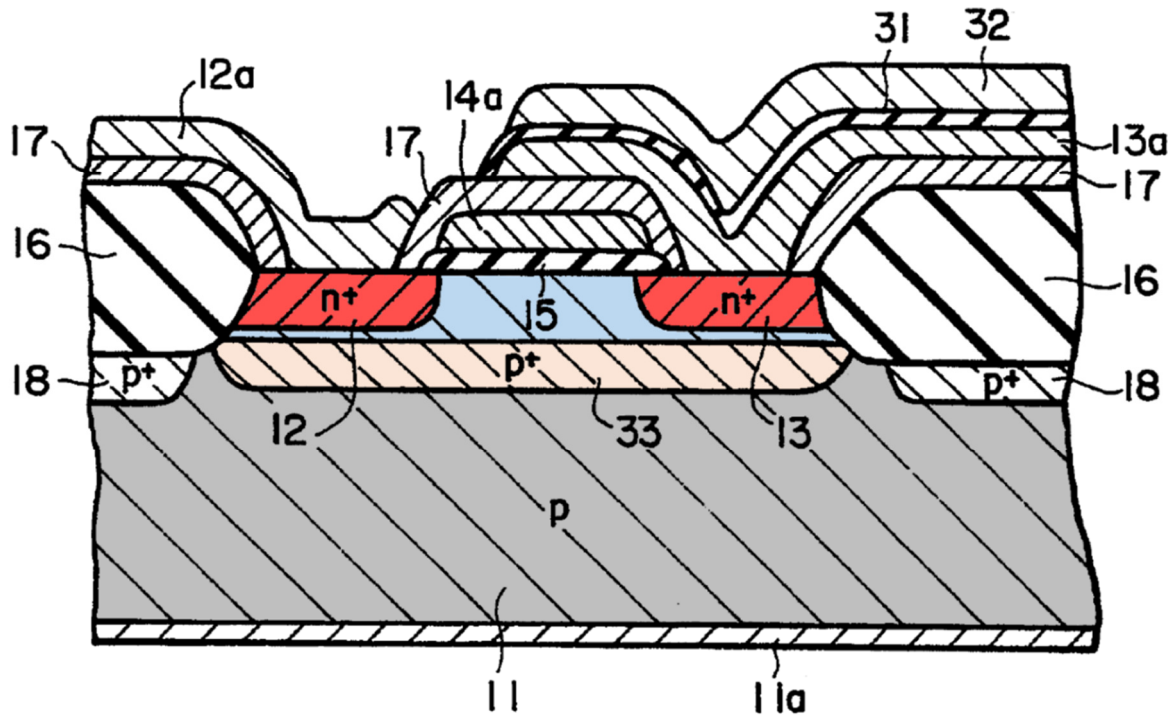
Onoda thusly discloses or, at the very least, renders obvious Claim 44.

B. Ground II: Onoda in view of Nishizawa Renders Obvious Claim 44.

Nishizawa teaches a CMOS device (*e.g.*, Nishizawa at 7:61-63, FIG. 32) that provides a buried region that has a graded dopant profile (annotated tan, below). (Nishizawa at FIG. 16, 18:46-67; *see also id.* at 20:25-27.) The graded dopant profile is provided to create an electric drift field (*id.* at 18:10-18) that flows minority carriers (electrons) from the surface region (blue) having the source and drain (red) to the

substrate (gray) in order to prevent device errors. (*Id.* at 19:1-9; *see also id.* at 16:19-24 (describing the migration of carriers flowing to the surface as causing errors).)

FIG. 16



(Nishizawa at FIG. 16.)

Ground II takes Nishizawa's teachings of CMOS and minority carrier diffusion, and combines it with teachings from Onoda. As described in Ground I, the CMOS and minority carrier diffusion elements are disclosed or, at the very least, rendered obvious by Onoda. Even if Patent Owner were to somehow successfully argue that these limitations were not disclosed by Onoda, Nishizawa nonetheless contains explicit statements about these elements making it clear that they were well-known to a POSITA.

A POSITA would have been motivated to make this combination for several reasons. (Ex. 1003 at ¶¶ 89-93.) Nishizawa’s teachings of CMOS and minority carrier diffusion are well known elements which, when combined with Onoda, would yield predictable results. As depicted in Ground I, Element [Preamble], Onoda discloses CMOS (although not mentioning the word “CMOS” directly). A POSITA would have found it obvious to apply teachings of CMOS—which was well known and described in Nishizawa—and apply it to Onoda. (*Id.*) For example, Nishizawa describes an NMOS and PMOS pair as being a CMOS (*e.g.*, Nishizawa at FIG. 32) for memory (*id.* at Abstract), and Onoda describes both NMOS and PMOS in a single memory device. (Onoda at FIG. 3.)

In a similar vein, a POSITA would have been motivated to apply Nishizawa’s teachings of minority carrier diffusion based on a downward sloping dopant gradient (*e.g.*, Nishizawa at 18:46-67) to Onoda’s teachings of a downward sloping dopant gradient (*e.g.*, Onoda at FIG. 11). (Ex. 1003 at ¶¶ 91-92.) Again, Nishizawa makes explicit concepts in direct words, *e.g.*, “electric field” that migrates minority carriers to a substrate based on a dopant gradient (Nishizawa at 18:10-18), whereas Onoda describes the structure (*e.g.*, the downward dopant gradient, Onoda at FIG. 11), which a POSITA would have understood necessarily creates the specified physical conditions. A POSITA would have been motivated to combine teachings of Nishizawa’s explicit discussion of concepts to the structures described in Onoda. (Ex. 1003 at ¶¶ 92-93.)

Making this combination of teachings would have combined known elements to achieve predictable results (*e.g.*, applying Onoda’s PMOS and NMOS transistors to CMOS as disclosed by Nishizawa and applying Onoda’s downward dopant gradient to Nishizawa’s teaching of the electric fields and minority carrier drifts that a downward dopant gradient creates). A POSITA would have seen such combinations as yielding expected results with known prior art elements and would have moreover found it obvious to try. (*Id.*)

Moreover, both Nishizawa and Onoda are directed to similar devices, which face similar problems, and seek similar solutions. Both are directed to memory devices (Nishizawa at Abstract; Onoda at [0004]), and to reducing punch through. (Nishizawa at Title; Onoda at Object.) (Ex. 1003 at ¶¶ 89-90.)

The Onoda-Nishizawa combination teaches elements from Onoda as described in Ground I, as supplemented by the specific limitations below to render claim 44 obvious.

1. Independent Claim 44

a. Preamble: “A CMOS Semiconductor device comprising:”

As described in Ground I, preamble, a POSITA would have found Onoda to disclose and, at the very least, render obvious CMOS. As described in the motivation to combine section above at VII.B, a POSITA would have further found it obvious to combine Nishizawa’s teachings of CMOS to Onoda’s teachings of NMOS and PMOS.

Nishizawa teaches CMOS. FIG. 32 depicts using NMOS and PMOS as CMOS (Nishizawa at FIG. 32 and 15:27-52) and further states one of its objects is to provide an improved CMOS device (*id.* at 7:61-63).

The Onoda-Nishizawa combination therefore renders obvious the preamble.

b. Elements [1.1]-[1.4]

For the same reasons as in Ground I, Elements 1.1-1.4 are disclosed and/or rendered obvious by the Onoda-Nishizawa combination.

c. Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”

As described in Ground I, Element [44.5], Onoda discloses a drift layer whose dopant concentration has a downward gradient which a POSITA would have recognized as providing a built-in, static, unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate where there is no active region. (Ex. 1003 at ¶ 145.)

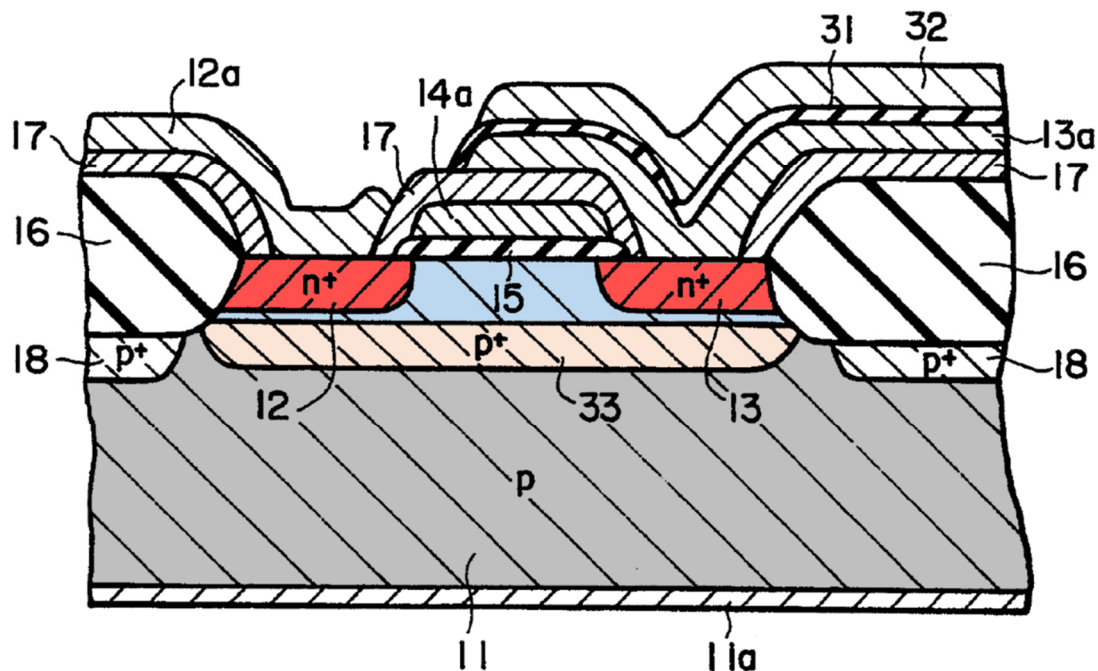
Nishizawa makes these elements explicit. FIG. 16⁹ depicts a source and drain (red, below) at the surface region (blue), where buried region 33 (tan) provides an

⁹ The cited-to text refers to the embodiment of FIG. 35, and Nishizawa states that the discussion is likewise applicable to the structure of FIG. 16 which is illustrated.

(Nishizawa at 20:23-27.) (Ex. 1003 at ¶ 89, fn. 2.)

“impurity concentration gradient ... [that is] progressively decreasing toward the p type substrate” (gray). (Nishizawa at 19:4-5; *see also id.* at 18:50-59 (“the impurity concentration of that portion of the p+ type buried region 33a located adjacent the channel region and the n+ type region 13 is set at about $1 \times 10^{17} \text{ cm}^{-3}$, with progressively lowered concentration as the portions of the buried region 33a go progressively toward the p type substrate 11, in such manner that the impurity concentration of lowermost portion of the buried region is less than at least one third of that of the highest impurity concentration.”))

FIG. 16



(Nishizawa at FIG. 16.)

As recognized by Nishizawa, “a drift electric field” is created when there is a “difference in the degree of impurity concentration,” which is used to drift minority

carriers to the substrate. (Nishizawa at 18:9-18.) To drift electrons within the p+ buried layer to the substrate, “an impurity concentration gradient in the p+ type buried region 33a in the direction toward the p type substrate” is formed. (*Id.* at 18:35-50; *see also id.* at 18:51-67 (stating that the impurity concentration has a downward gradient to the substrate); *see also id.* at 19:1-9.) (Ex. 1003 at ¶¶ 96-97.)

As described in Ground I, Element [44.5], Onoda discloses a drift layer with an impurity dopant profile with a downward gradient. The Onoda-Nishizawa combination makes clear that this drift layer in Onoda provides a static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate. (Ex. 1003 at ¶¶ 96-97.)

The Onoda-Nishizawa combination thusly renders Element [44.5] obvious.

- d. Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”**

As described immediately above, the Onoda-Nishizawa combination renders Element [44.5] obvious. As described in Ground I, Element [44.6], Onoda discloses a drift layer having a well-region with an impurity dopant profile with a downward gradient. The Onoda-Nishizawa combination makes clear that this well region in Onoda provides a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate for the same reasons

described in Ground II, Element [44.5] and that the substrate does not have an active region. (Ex. 1003 at ¶¶ 98, 146.)

C. Ground III: Kawagoe Renders Obvious Claim 44.

Kawagoe teaches a CMOS device whose surface region (its epitaxial layer) has its “impurity concentration gradually lowered depthwise of said epitaxial layer.” (Kawagoe at Abstract.) The “gradient ... is gradually lowered in the depthwise direction from the surface of the epitaxial layer ... so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient.” (*Id.* at 16:3-8.)

Kawagoe’s teachings and purpose of the doping gradient match that of the ’222 Patent. The ’222 Patent states that the prior art was deficient because it purportedly provided uniformly doped epitaxial regions (’222 Patent at 1:46-53), and the ’222 Patent—as an improvement—provided a gradient doping profile at the surface to sweep unwanted minority carriers into the substrate. (*Id.* at 3:52-56.) This purported improvement is described by Kawagoe.

Kawagoe renders obvious claim 44 as detailed below.

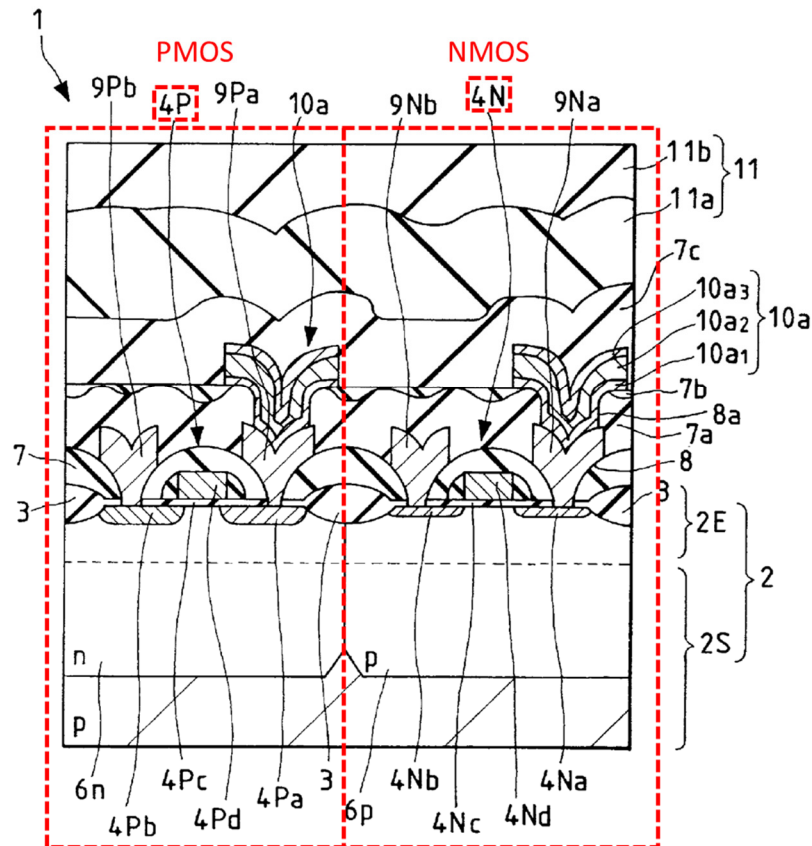
1. Independent Claim 44

a. Preamble: “A CMOS Semiconductor device comprising:”

Kawagoe discloses a CMOS semiconductor device. (*See, e.g.*, Kawagoe at

15:37-40 (describing the CMOS structure of the embodiment of FIG. 16 having an NMOS 4N and PMOS 4P); *see also id.* at 8:46-54 (describing the CMOS).) (Ex. 1003 at ¶ 101.)

FIG. 16



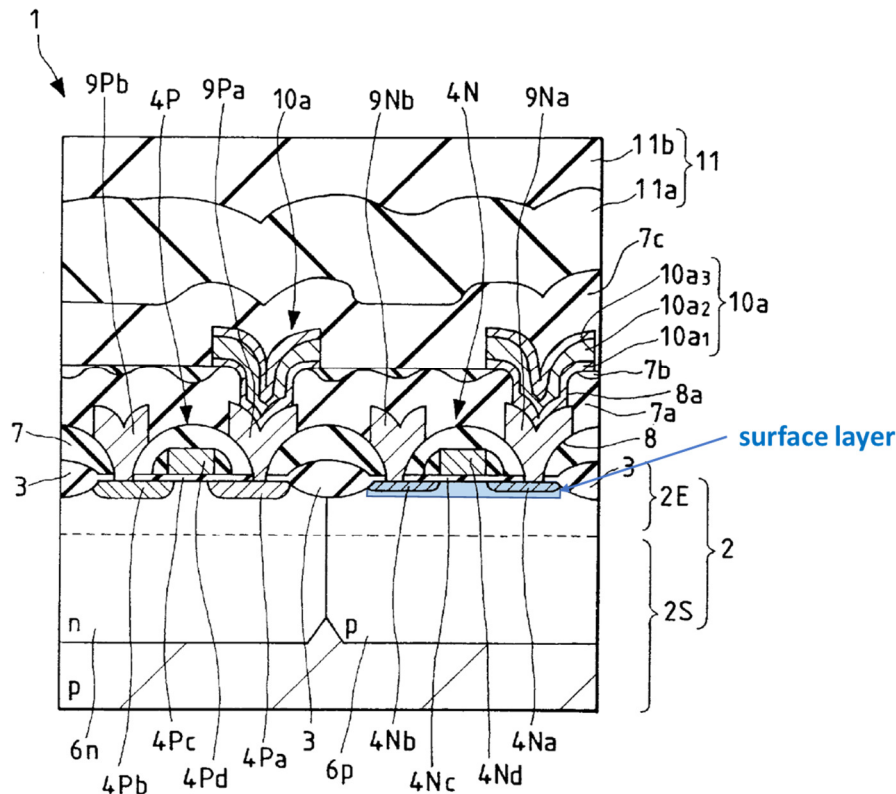
(Kawagoe at FIG. 16.)

b. Element [44.1]: “a surface layer;”

Kawagoe teaches a surface layer as depicted below in blue in annotated FIG. 16. Kawagoe’s surface layer exists in the epitaxial layer (2E) and the surface layer has an active region with a source and drain formed within it (4Nb and 4Na) (discussed in

more detail with respect to Element [44.3]).¹⁰ (Kawagoe at 8:66-9:6; *see also id.* at 15:26-32.) (Ex. 1003 at ¶ 102.)

FIG. 16

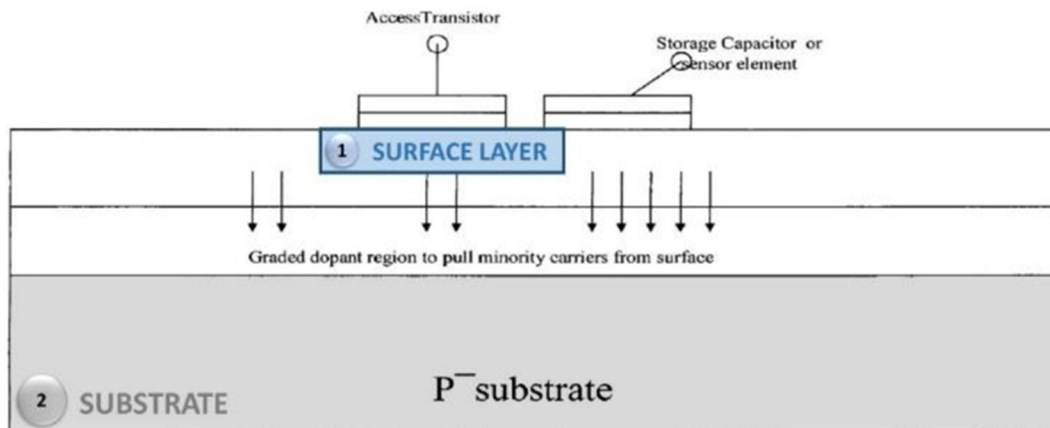


(Kawagoe at FIG. 16.)

Kawagoe’s “surface layer” teachings match Patent Owner arguments made in its

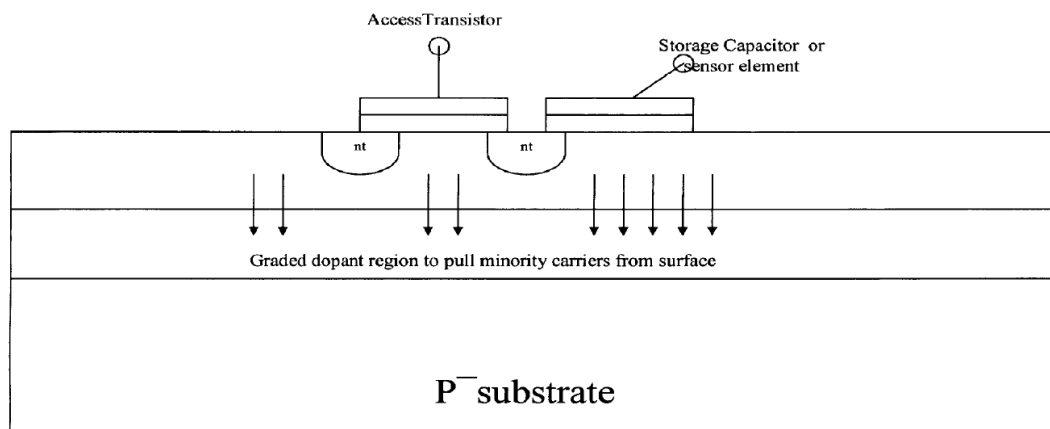
¹⁰ FIG. 16 depicts the finalized devices, with insulating films 7, wirings 10, and protection films 11. (Kawagoe at 15:55-61.) A POSITA would understand that these additional components are not a part of the semiconductor’s surface layer because they are, as they state, wirings and insulators for the semiconductor device that is fabricated on the silicon wafer. (Ex. 1003 at ¶ 102.)

district court claim construction briefing. Shown below, Patent Owner annotated FIG. 5(b) as support to disclose a “surface layer” (the region surrounding the active region), and Patent Owner further argued in construction that the “surface layer” refers to “a layer at the surface of the silicon.” (Ex. 1030 at 13.)



(Ex. 1030 at 6) (annotations to FIG. 5(b) of the '222 Patent by Patent Owner).

Patent Owner annotated over FIG. 5(b). A non-annotated version of FIG. 5(b) of the '222 Patent is excerpted below that more clearly illustrates the active region (the source and drain).



('222 Patent at FIG. 5(b).)

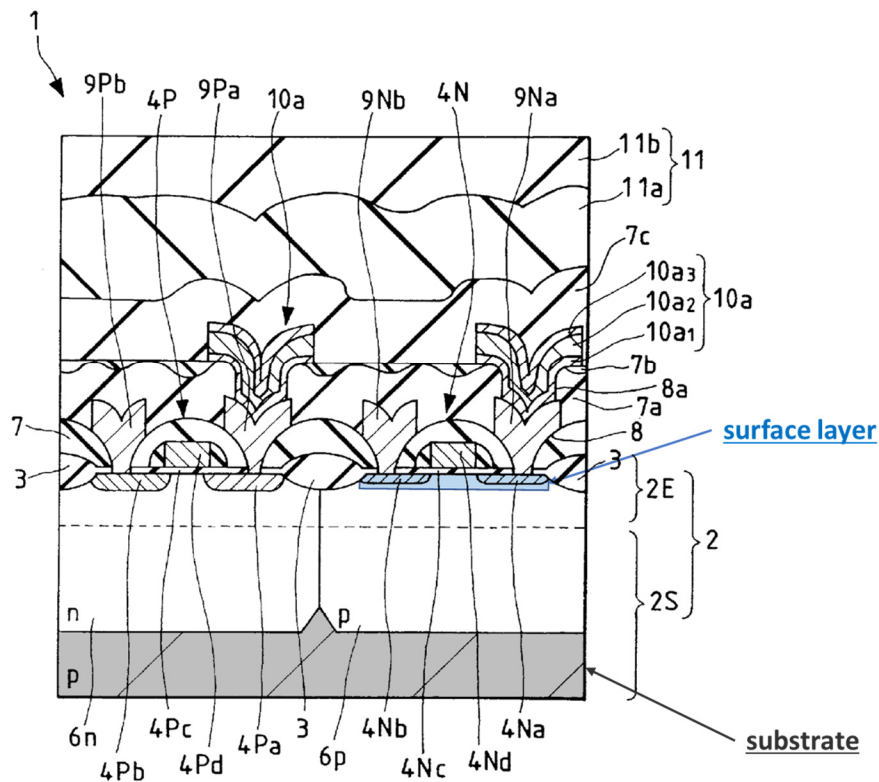
Kawagoe teaches the “surface layer” in an identical manner as described by the ‘222 Patent’s purported written description support of the very same limitation, and thusly renders this limitation obvious.

c. Element [44.2]: “a substrate;”

Kawagoe teaches a substrate.

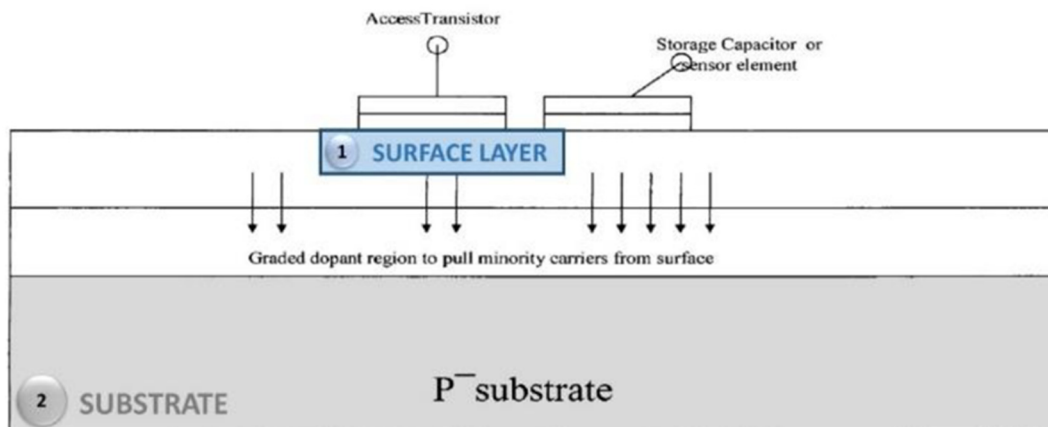
Kawagoe’s substrate is annotated in gray in FIG. 16, below. Kawagoe forms its p-well 6p and n-well 6n in part of the substrate body 2S from the original wafer. (Kawagoe at 15:62-65, 17:50-61, FIG. 21.) A POSITA would understand that at least the portion of the substrate—separate from the well regions—would satisfy the claimed substrate. (Ex. 1003 at ¶ 104.).

FIG. 16



(Kawagoe at FIG. 16.)

Kawagoe’s teaching of the “substrate” matches Patent Owner’s district court claim construction of “substrate,” which was described as “an underlying layer” (Ex. 1030 at 15) and where Patent Owner provided annotation to FIG. 5(b) of the ’222 Patent (excerpted below).¹¹



(Ex. 1030 at 6) (annotations by Patent Owner).

Element [44.2] is accordingly taught by Kawagoe.

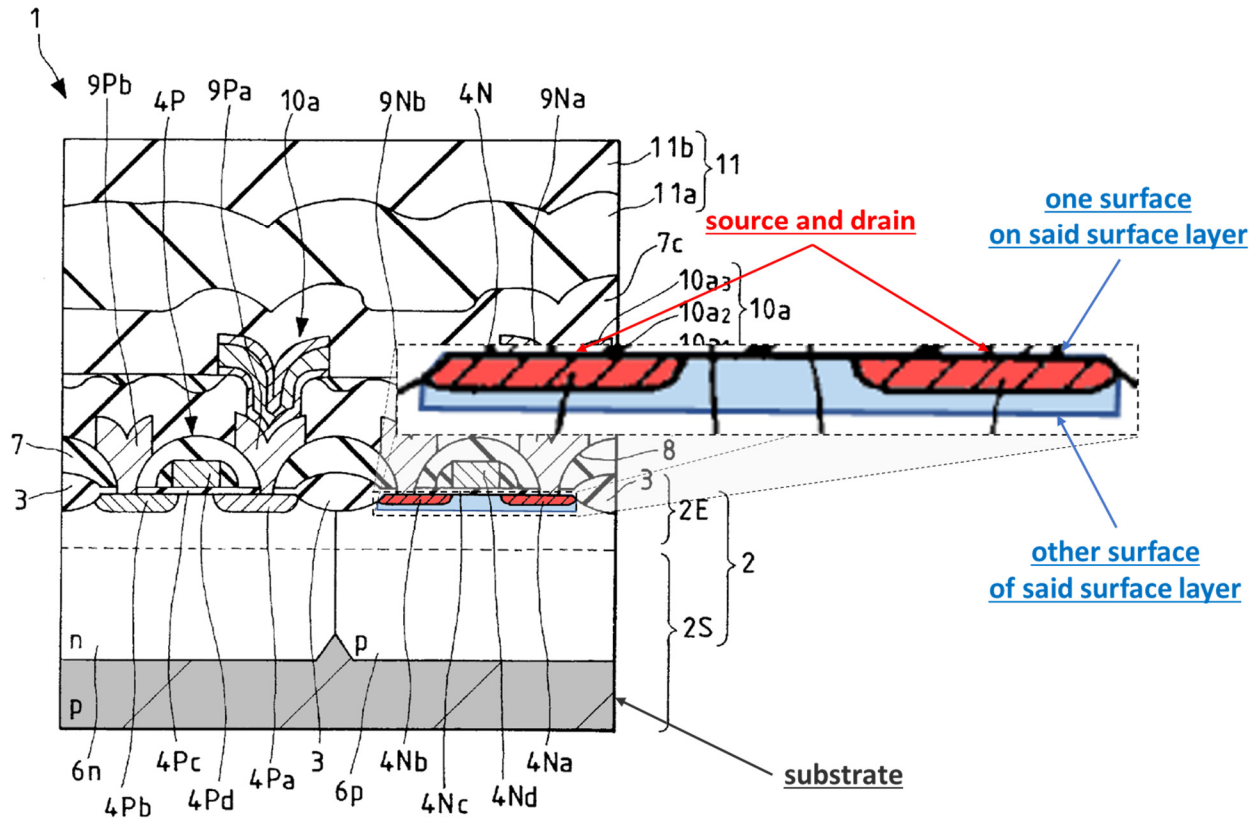
d. Element [44.3]: “an active region including a source and a drain, disposed on one surface of the surface layer;”

Kawagoe teaches an active region that has a source and a drain disposed on one surface of the surface layer. As depicted in annotated FIG. 16 below, the surface layer

¹¹ Moreover, layer 2S by itself further satisfies the “substrate” term (*e.g.*, Kawagoe at 15:7-8 (stating that “the p- -type epitaxial layer 2E is formed over the p-type semiconductor substrate).). This—and its relationship to the claimed “single drift layer”—are discussed in more detail with respect to Elements [44.4]-[44.6] below.

contains source and drain 4Nb and 4Na which form an active region (excerpted out for greater emphasis). (Kawagoe at 8:66-9:6, 9:47-53.) (Ex. 1003 at ¶ 106.)

FIG. 16



(Kawagoe at FIG. 16 (active region excerpted above).)

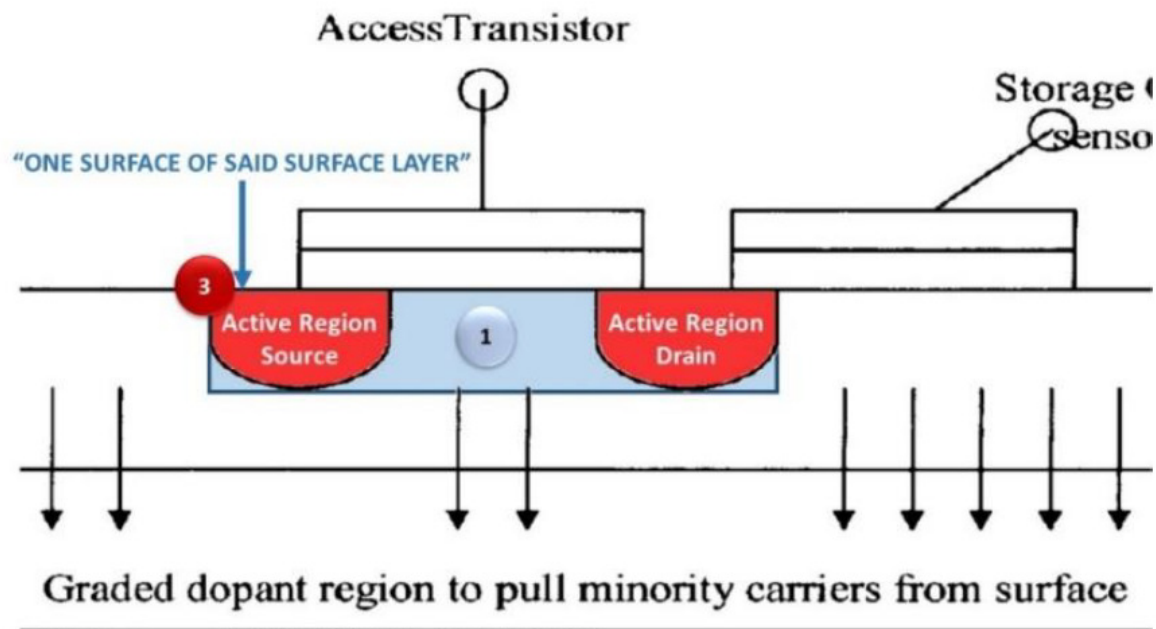
The active region is disposed to the top surface of the surface layer, *i.e.*, the claimed “one surface on said surface layer.” (Ex. 1003 at ¶ 107.). This orientation—and discussion of each respective region—matches Patent Owner’s articulation of this limitation during district court claim construction. There, it had likened the orientation to a ceiling fan in a room, stating:

“By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the

ceiling fan is spinning around like a propeller on the roof of the house. Instead it means that the ceiling fan is hanging from the ceiling *inside* the room. The same is true about the active region and the surface layer.”

(Ex. 1030 at 11 (emphasis in original).)

Patent Owner further annotated FIG. 5(b) of the '222 Patent to depict this configuration, where the active region source and drains were disposed on the surface of the surface layer (similar to Kawagoe's FIG. 16).

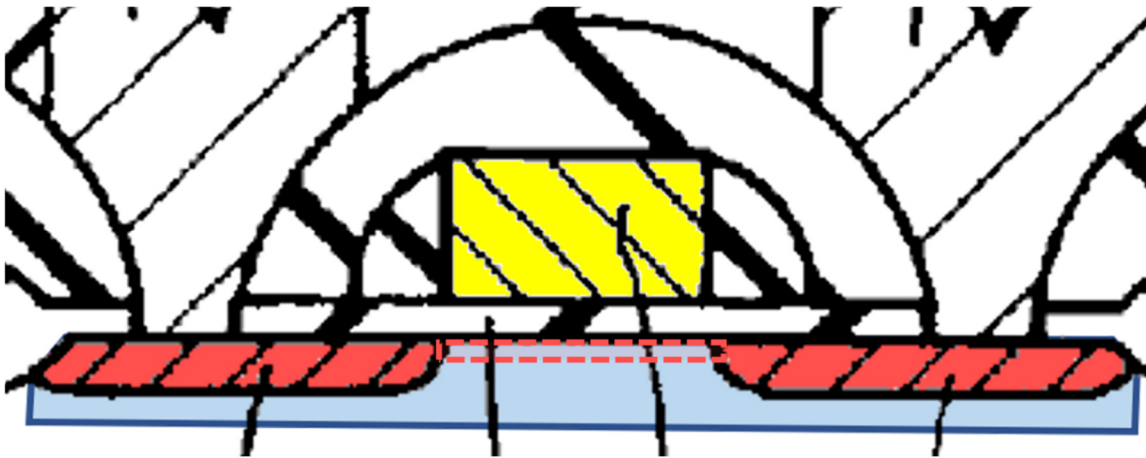


(Ex. 1030 at 7.)

Kawagoe thusly teaches the “an active region including a source and a drain, disposed on one surface of the surface layer,” and moreover teaches it in a manner similarly to Patent Owner’s stated written description support.

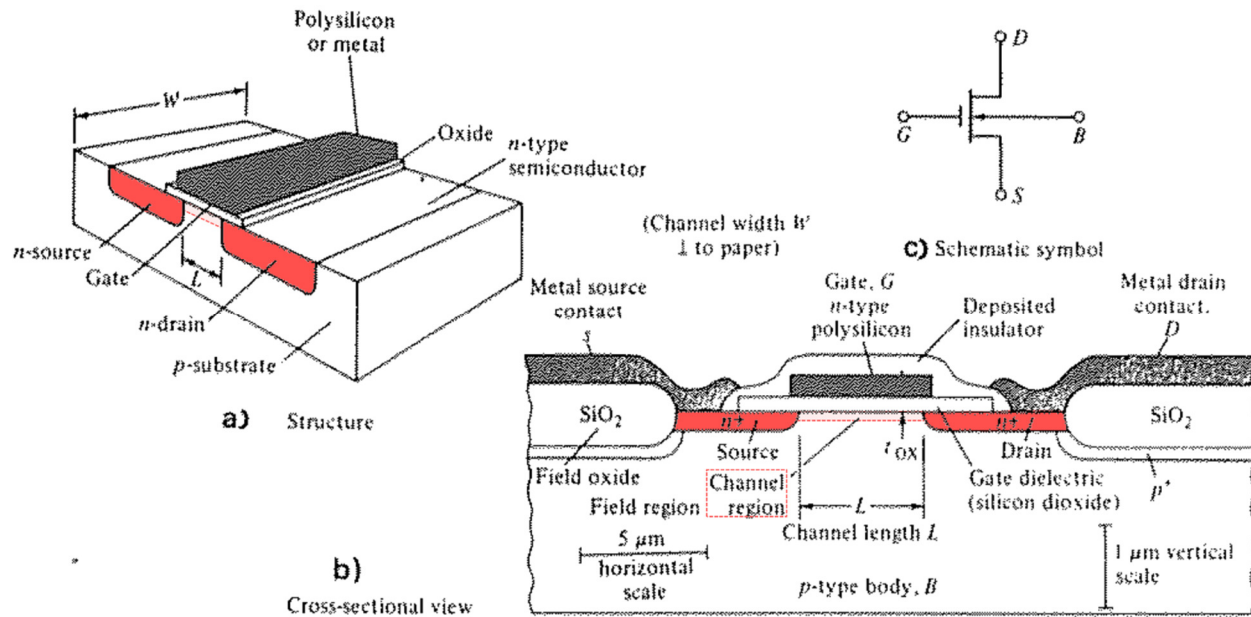
Furthermore, a POSITA would understand that the above-described source and

drain configurations of Kawagoe provide an active region. (Ex. 1003 at ¶ 108.). As depicted in the enlarged excerpt of FIG. 16, below, a charge applied to gate electrode 4Nd (annotated in yellow, *see, e.g.*, Kawagoe at 9:20-26) causes a conductive channel (annotated in dashed-red) to form between the source and drain. (Ex. 1003 at ¶ 108.). A POSITA would understand the source, drain, and channel depicted below to be an active region. *Id.*



(Kawagoe at FIG. 16 (excerpt).)

This understanding of source, drain, and channel operation in a MOS transistor is confirmed via *Wolf and Tauber*, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor as “[its] channel and [its] heavily doped source and drain regions.” (Ex. 1008 at 299; *see also* Ex. 1030 at 4-5 (Patent Owner acknowledging that a channel is formed between a source and drain to form an active region).)



(Ex. 1008B at FIG. 5-1.)

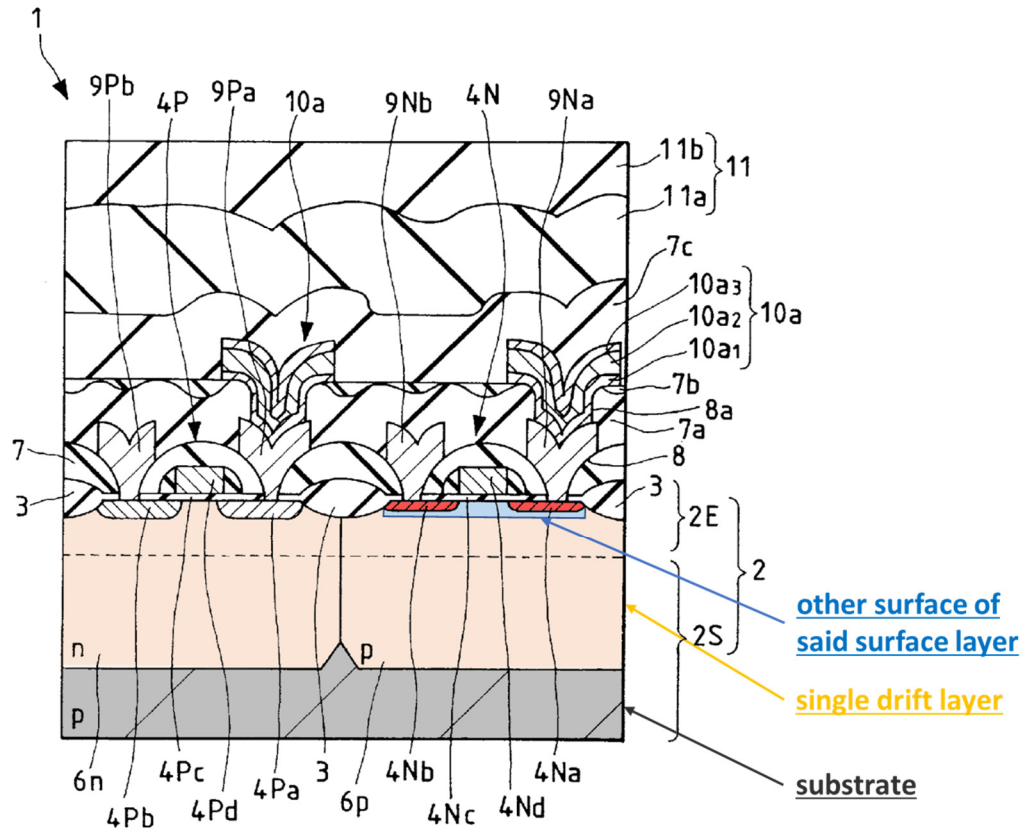
Kawagoe thusly teaches Element [44.3].

- e. **Element [44.4]: “a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,”**

Kawagoe teaches this limitation.

Kawagoe teaches the claimed single drift layer (annotated tan, below) disposed between the other surface of said surface layer (blue) and said substrate (gray), where the drift layer has a graded concentration of dopants extending between the surface layer and substrate. Kawagoe’s single drift layer includes the upper portion of the substrate body 2S colored in tan and the epitaxial layer 2E colored in tan that constitute an epitaxially integrated single structure. (Ex. 1003 at ¶¶110-111.)

FIG. 16

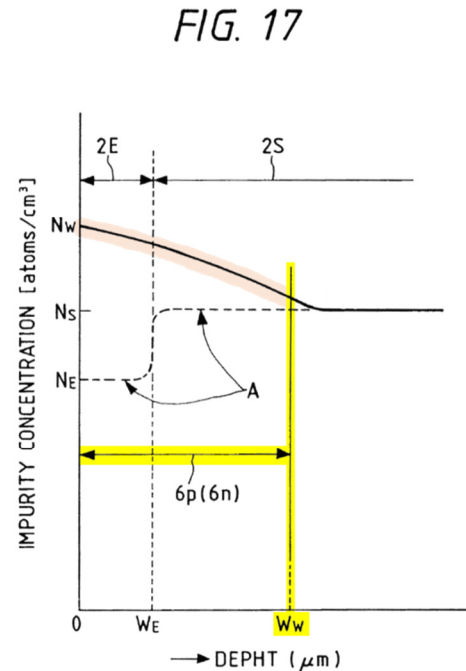
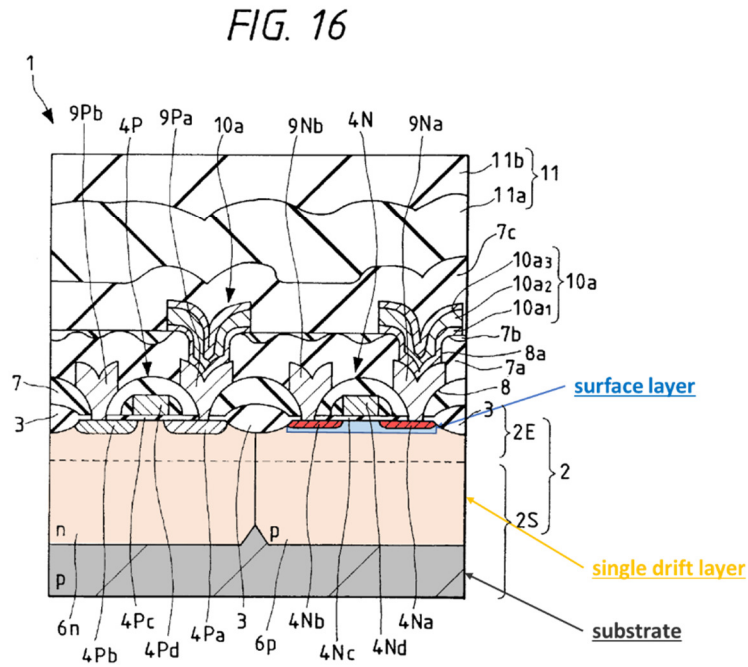


(Kawagoe at FIG. 16.)

Kawagoe’s single drift layer (annotated in tan, above) is at the surface of the semiconductor device (*see, e.g.,* Kawagoe at 15:62-16:15) and is formed into the CMOS device so that minority carriers (*e.g.,* electrons in the p-well) are attracted to the substrate to reduce errors. (Kawagoe at 16:7-11.) (Ex. 1003 at ¶ 111.) The single drift layer comprises both p-wells and n-wells, where the “impurity concentrations [of those wells are] gradually lowered in the depthwise direction from the principal surface ... of the epitaxial layer 2E.” (*Id.* at 15:66-16:2.) The depthwise gradient extends from the surface of the semiconductor device into its substrate (*id.* at 16:2-15) and is formed

by diffusing impurities in the upper portion of the semiconductor substrate. (*Id.* at 15:26-36). Kawagoe’s graded concentration of dopants is depicted in FIG. 17 where the gradient of dopants in the drift layer (tan) extends from the surface of 2E (epitaxial layer of wafer) through the p and n wells (6p and 6n) (with depth depicted in yellow) and a portion of the substrate (substrate of wafer).¹² (Ex. 1003 at ¶ 111.)

¹² Patent Owner has argued in claim construction that the claims cover a drift layer that extends into the substrate. (Ex. 1030 at 17 (Patent Owner arguing in claim construction that “the claim never says the well region and drift layer cannot be part of the substrate. In fact, the specification says the opposite”) (citing ’195 Patent at 2:27-28, which is the ’222 Patent’s parent).) To the extent Patent Owner argues a narrow view of “single drift layer” to be narrowly confined in some manner, that would be inconsistent with Patent Owner’s own argument of claim scope.

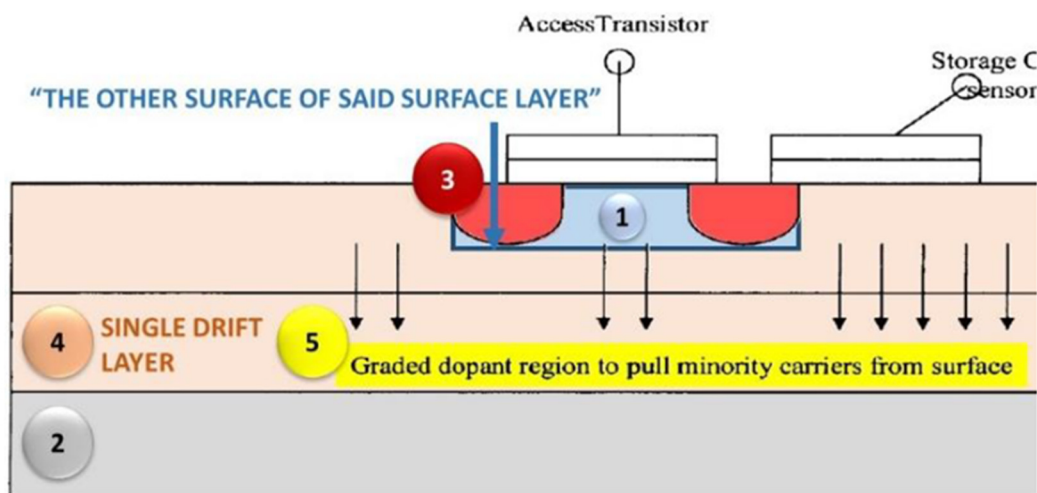


(Kawagoe at FIGS. 16 and 17.)

Kawagoe describes its impurity gradient region (which was annotated tan, above) as a “diffusion layer.” Kawagoe discloses that a “diffusion layer” is created by diffusing impurities into a semiconductor device. (Kawagoe at 2:20-23; *see also id.* at 16:63-17:10 (stating that diffusion of impurities creates a “diffusion layer” when describing the state of the art); *see also id.* at 2:21-35; *see also id.* at 1:61-65 (describing how the referenced Japanese application, likewise describes this as a diffusion layer). And, as described above, diffusing impurities to create a diffusion layer is how Kawagoe’s drift layer is created. (*Id.* at 15:26-36; *see also id.* at 17:50-54; *see also id.* at 25:27-30.). Finally, the term “drift layer” does not appear in the ’222 Patent specification while “drift region” is repeatedly described. (*See, e.g.,* ’222 Patent at 3:18-28.) As a consequence, a POSITA would understand that Kawagoe’s diffusion

layer discloses—or at least renders obvious because it uses similar verbiage as the claims—the claimed “single drift layer.” (Ex. 1003 at ¶ 112.)

Kawagoe’s teachings match Patent Owner’s district court claim construction annotations to FIG. 5(b) of the ’222 Patent, where it demonstrated the position of the single drift layer in relationship to the surface layer’s other surface and the substrate. (Ex. 1003 at ¶ 113.)

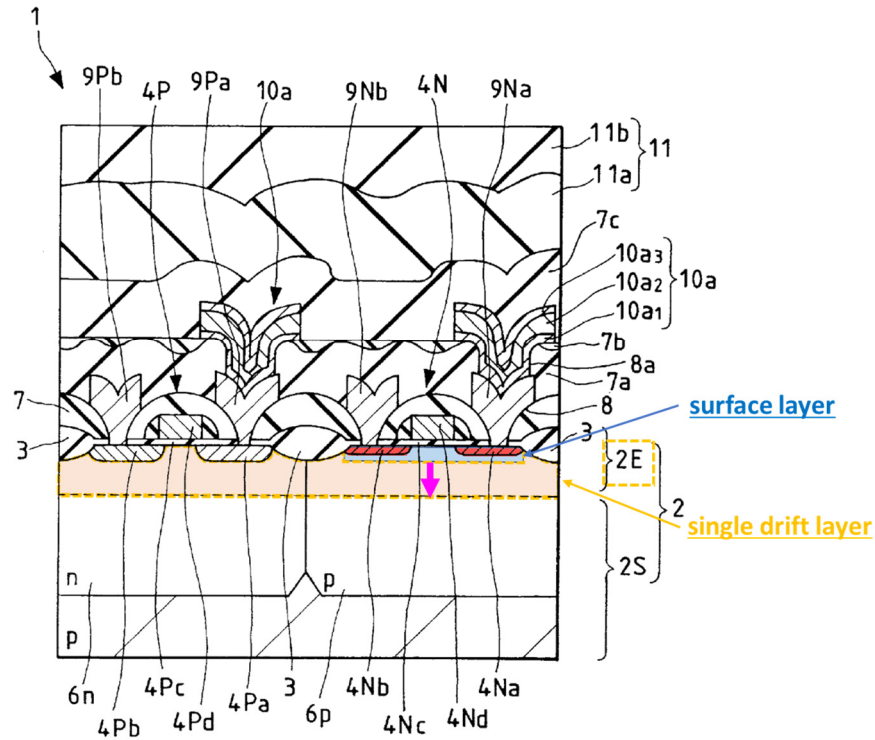


Kawagoe’s diffusion layer thusly satisfies the claim limitations of Element [44.4].

Even if Patent Owner were to argue that Kawagoe’s dopant gradient does not literally disclose Element [44.4] under a narrow interpretation of “single” or “layer” in the claim phrase “single drift layer,” it nevertheless would be obvious because the epitaxial layer (*see* 2E in FIG. 16) itself, which has a graded dopant concentration (*see* line Nw in FIG. 17), is a singular layer that satisfies the claimed “single drift layer.” The portion of the diffused impurity gradient that is within the epitaxial layer 2E—

which satisfies the “single drift layer”—is annotated below in tan within the dashed lines. (Ex. 1003 at ¶¶ 113-16.)

FIG. 16

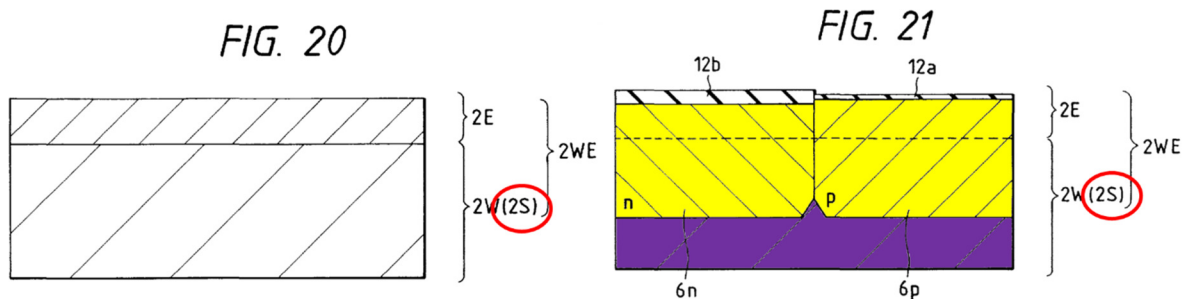


(Kawagoe at FIG. 16.)

Layers 2E and 2S are part of the semiconductor wafer prior to forming the diffusion layer. (*See* Kawagoe at FIGS. 20 and 21.) The substrate 2S is made of a p type Si single crystal which that is initially formed with a p type impurity such as boron and the epitaxial layer 2E is made up of a p- type Si single crystal. (*Id.* at 14:61-15:16.) After the wafer is formed, it is doped with impurities to create the diffusion layer that comprises n and p wells.¹³ (*Id.* at 15:26-36.) This process is depicted in FIGS. 20 and

¹³ 12a and 12b are masks used in the well-forming processes. (*Id.* at 17:40-49.)

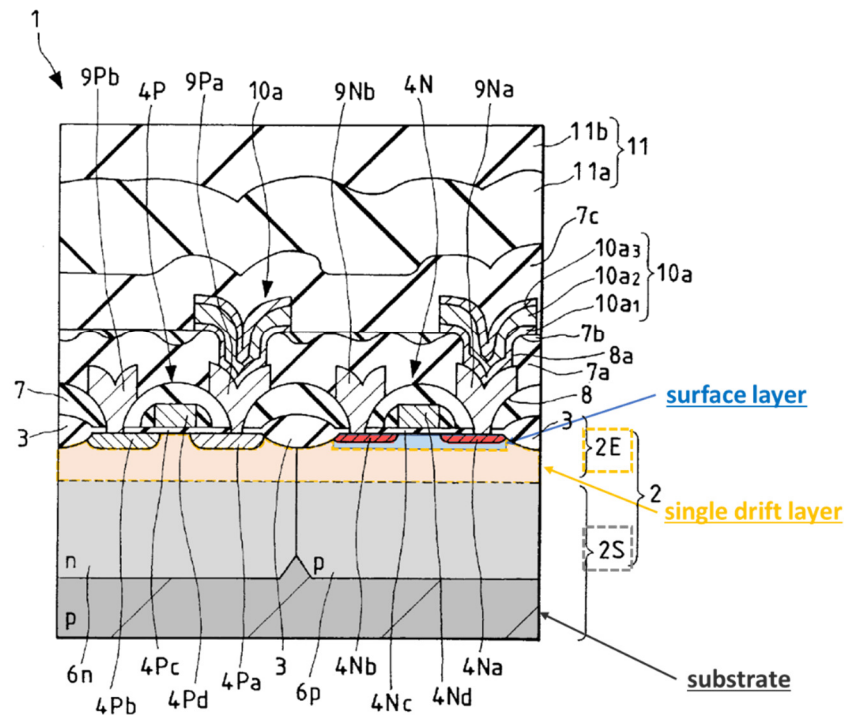
21 where—after the diffusion gradient is created (yellow)—only a portion of the substrate has a uniform doping profile (purple). (*Id.* at 17:11-21.) (Ex. 1003 at ¶¶ 114-16.)



(Kawagoe at FIGS. 20 and 21.)

Layer 2E, if taken as a separate and distinct layer by itself, has a graded dopant concentration and satisfies the claimed “single drift layer.” (Ex. 1003 at ¶ 116.) Its graded dopant concentration is similarly provided to attract minority carriers to the substrate. (Kawagoe at 15:62-16:11.) Layer 2E—which satisfies the “single drift layer”—is again depicted by the tan-dashed lines below. Furthermore, Layer 2S (substrate body, *e.g.*, *id.* at 15:1-17) as a whole, or merely the uniformly doped portion, further renders obvious the claimed “substrate” (both portions annotated in grey below, with the non-well region after doping in darker grey). (*See e.g.*, Element [44.2] discussion at pg. 54 and Fn. 10 (discussing “substrate.”) Even under a narrow construction of Limitation [44.4], the Kawagoe structure still renders it obvious.

FIG. 16



(Kawagoe at FIGS. 16 and 17.)

Thusly, even under a prospective narrow view of Element [44.4]’s “single drift layer,” one that is at odds with Patent Owner’s own position in litigation and the ’222 Patent specification, Kawagoe nonetheless renders Element [44.4] obvious.

Kawagoe accordingly discloses or at the very least renders Element [44.4] obvious.

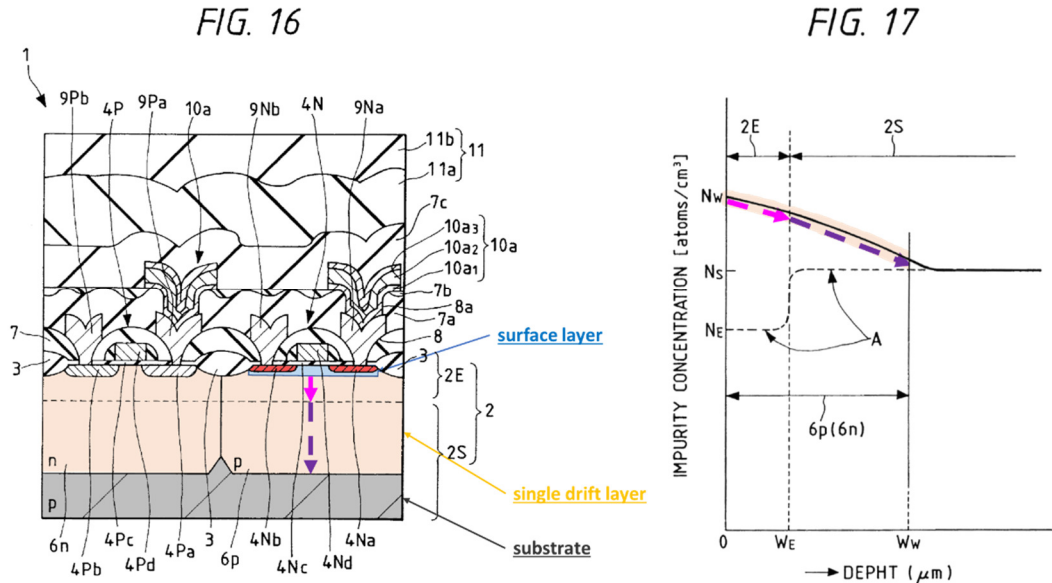
- f. Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”**

Kawagoe teaches this limitation.

As described in Element [44.4], Kawagoe teaches a single drift layer with a

graded dopant profile. This graded dopant profile results in “electrons ... [being] attracted to the substrate body 2S by that concentration gradient.” (Kawagoe at 16:7-11.) A POSITA would understand that electrons refer to minority carriers in the p-well, and that the electrons are attracted to the substrate due to a static unidirectional electric drift field. (Ex. 1003 at ¶ 117) A POSITA would understand the field to be static because it is created by doping impurities that are fixed during device fabrication, as depicted in Kawagoe (*see, e.g.*, Kawagoe at 15:26-36, FIGS. 20-21). (Ex. 1003 at ¶ 117.) This was, moreover, recognized by Patent Owner as a property of a graded dopant profile in the specification of the ’222 Patent and during prosecution. (Ex. 1003 at ¶ 36.) There are electric fields in separate regions due to the graded doping concentrations, *e.g.*, those depicted by pink and purple arrows in annotated FIG. 17 below, where the pink field satisfies the first static unidirectional electric drift field.¹⁴ (Ex. 1003 at ¶ 118.) However, the substrate does not contain an active region as shown below. (Ex. 1003 at ¶ 152.)

¹⁴ The arrow orientation and direction are depicting the drift of minority carriers (electrons) in the p-well. (Ex. 1003 at ¶ 117.) A POSITA would understand that the electric field would exist in the opposite direction. (*Id.*)



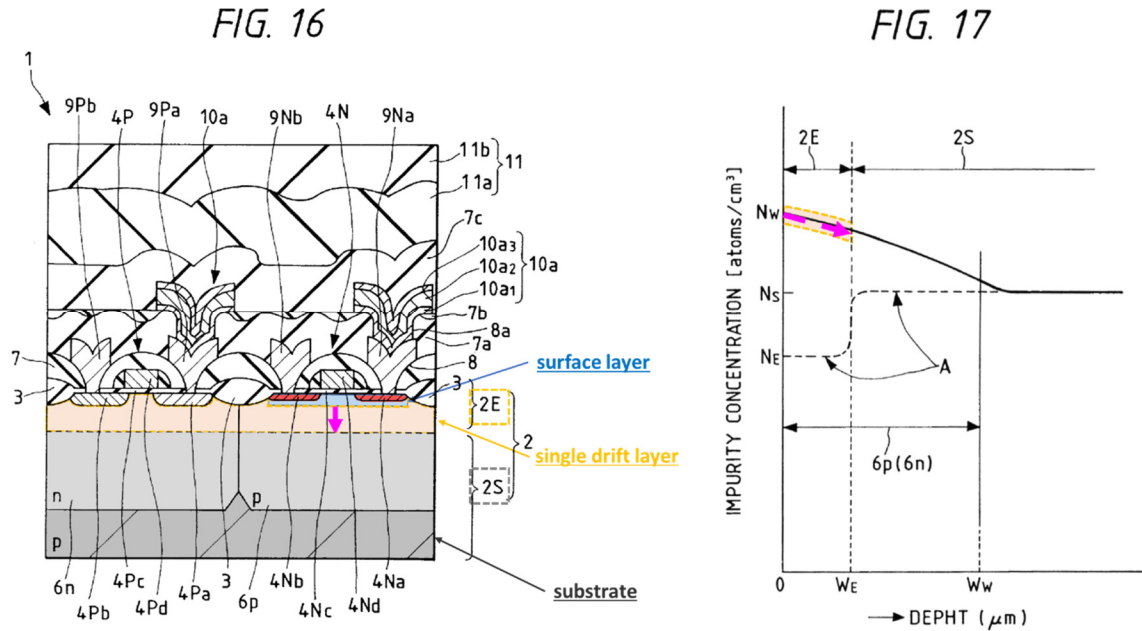
(Kawagoe at FIGS. 16 and 17.)

These electric fields are not exhaustive, and a POSITA would understand that numerous fields exist in the diffusion layer to attract minority carriers to the substrate.¹⁵ (Ex. 1003 at ¶ 118.) A POSITA would understand that Kawagoe’s single drift layer has multiple static unidirectional electric drift fields that aid in the movement of minority carriers to the substrate, and that any one of them satisfies the claimed “first static unidirectional electric drift field,” *e.g.*, the one depicted in pink over the epitaxial layer. (*Id.*)

¹⁵ Indeed, Patent Owner has argued that the limitation is not limited to a drift layer that has only one electric field, and covers the instance where there are multiple such fields. (Ex. 1030 at 21 (stating that “[t]here is nothing in the claim preventing additional electric fields”).)

Kawagoe thusly discloses Element [44.5].

Furthermore, as described in Element [44.4] at pages 58-60, Kawagoe's epitaxial layer (2E), by itself, renders obvious a narrow interpretation of the "single drift layer." And, either the entire substrate layer (2S), or just the non-gradient portion of 2S renders the "substrate" of Element [44.2] obvious. (*Supra* at 53-54.) The epitaxial layer (2E) would similarly have the claimed "first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate" because it also has a graded dopant concentration. This is annotated by the pink arrow, below. (Ex. 1003 at ¶ 119.) For the same reasons described in Kawagoe (Kawagoe at 16:7-11) and as admitted by Patent Owner (Ex. 1030 at pg. 24), Kawagoe's graded dopant profile provides a static unidirectional electric field. (*Id.*). Thusly, a POSITA would have understood that a graded dopant concentration like Kawagoe's provides a first static unidirectional electric drift field.



Element [44.5] is thusly rendered obvious by Kawagoe.

- g. **Element [44.6]:** “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”

Kawagoe teaches Element [44.6].

As depicted below in annotated FIGS. 16 and 17, Kawagoe’s single drift layer (the diffusion layer which comprises n and p wells) has at least one well region disposed within it (*e.g.*, the p well). This p-well is part of the diffusion layer and, like the diffusion layer described in Element [44.4], it has a graded dopant concentration. (Kawagoe at 15:62-16:15; *see also id.* at 15:26-36, 17:11-21; *see also id.* at 1:59-2:5, 2:20-23, 15:62-16:15.) (Ex. 1003 at ¶ 120.) And, as described in Element [44.5], this dopant concentration results in several static unidirectional electric drift fields, where

the pink arrow indicates the first static unidirectional electric drift field. (Ex. 1003 at ¶ 120.) The second static unidirectional electric drift field is annotated in purple. (*Id.*) As depicted below, the well region (green) is disposed within the single drift layer (tan with tanned dashes) and graphically overlaps. But the substrate does not contain an active region. (Ex. 1003 at ¶ 152.)

FIG. 16

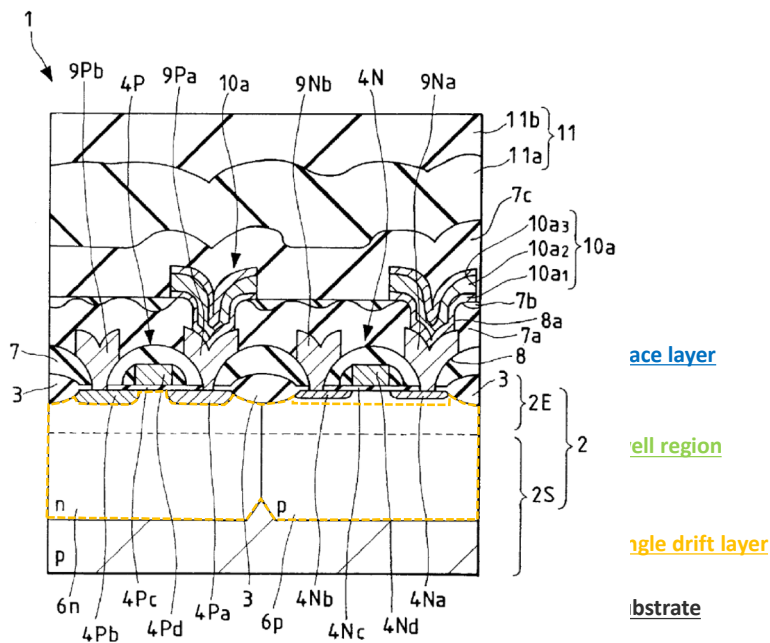
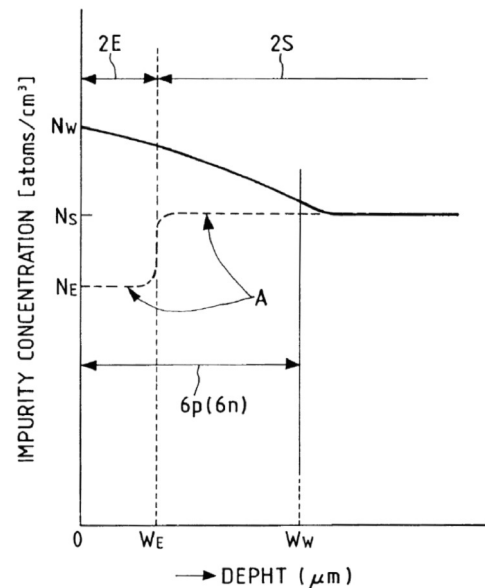


FIG. 17



(Kawagoe at FIGS. 16 and 17.)

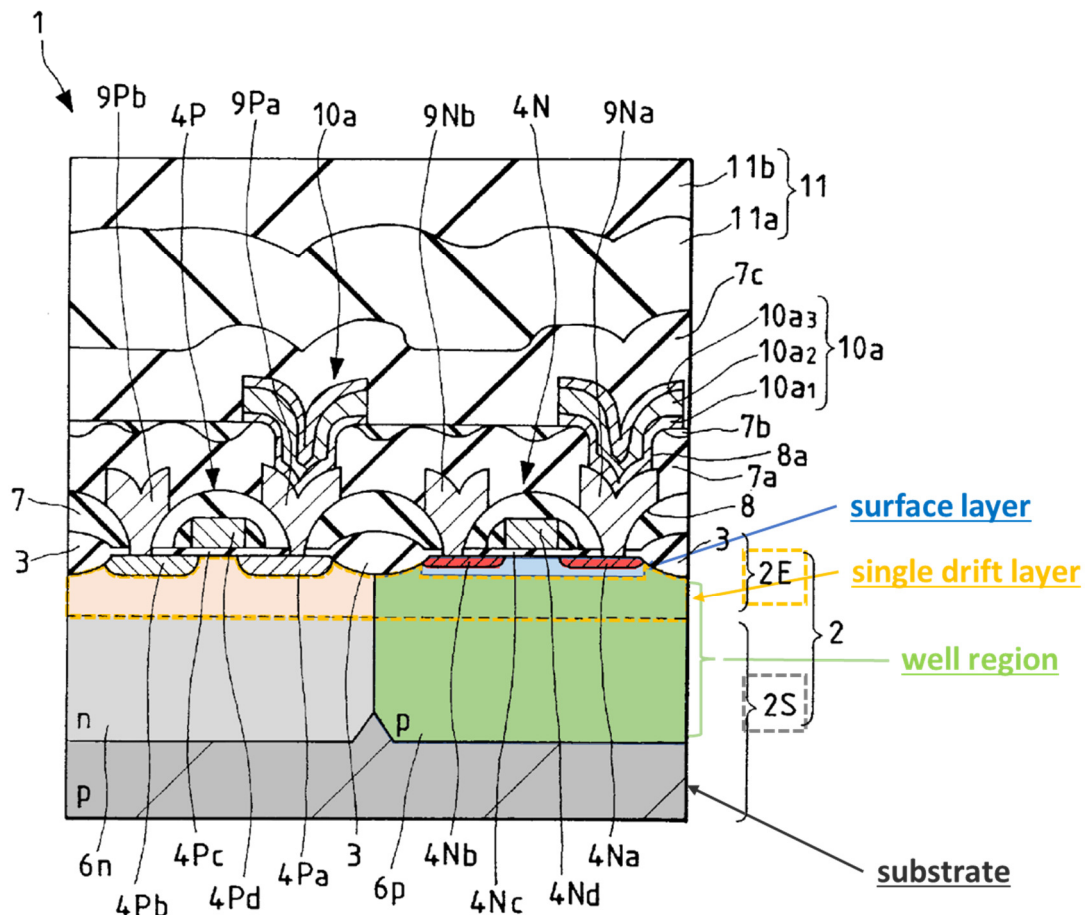
Kawagoe thusly teaches Element [44.6]

Furthermore, as described in Element [44.4], the claimed single drift layer is further rendered obvious even under a narrow construction of that term. This is because Kawagoe’s epitaxial layer (2E) by itself renders obvious the claimed “single drift layer.” (Ex. 1003 at ¶¶ 121-22.) And, either the entire substrate layer (2S) or just the

portion of layer 2S that does not have a graded doping profile by itself independently render obvious the “substrate” limitation. (*Id.*) This is consistent with the limitations of Element [44.6].

The epitaxial layer (2E) has at least one well region that is disposed in it and it thusly satisfies the limitations of Element [44.6]. The “single drift layer” is annotated in tan and, as can be seen below, the well region (green) is disposed in the single drift layer and goes into the substrate body 2S (light grey, where the undoped portion is in darker grey).

FIG. 16



(Kawagoe at FIG. 16.)

The above comports with the claim language, which requires that the well region be “disposed in” the “single drift layer,” and not that the well region be disposed entirely within the single drift layer. To use a real-world example, a finger is “disposed in” a cup of water if the finger is dipped in the water even though a portion of the finger is outside the cup. Similarly, Kawagoe’s well-region is “disposed in” the epitaxial layer 2E (single drift layer) even though portions of it are outside of the single drift layer.

Moreover, the well-region similarly provides a static unidirectional electric drift field for the same reasons described in Element [44.5]. (Kawagoe at 16:62-16, FIG. 17; *see also* Ex. 1003 at ¶ 124.) This is depicted below, where the second static unidirectional electric drift field (purple arrow) aids the movement of minority carriers from said surface layer to said substrate.

FIG. 16

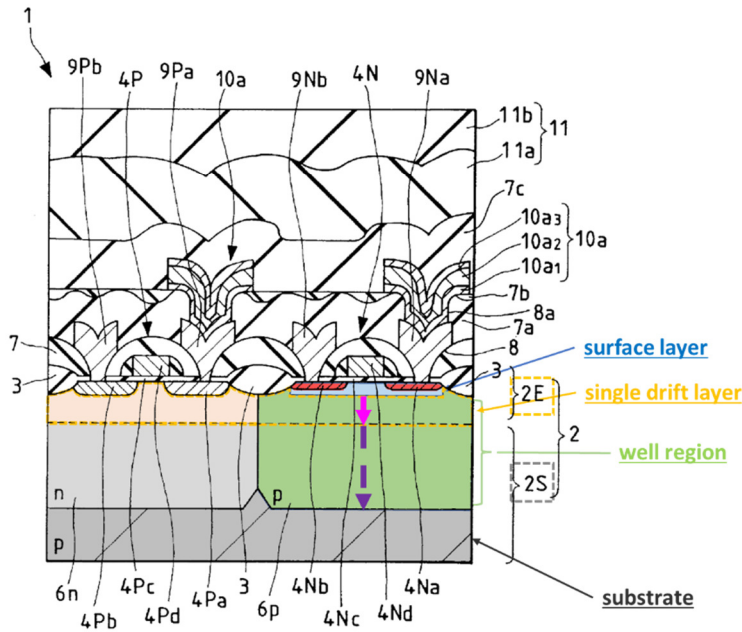
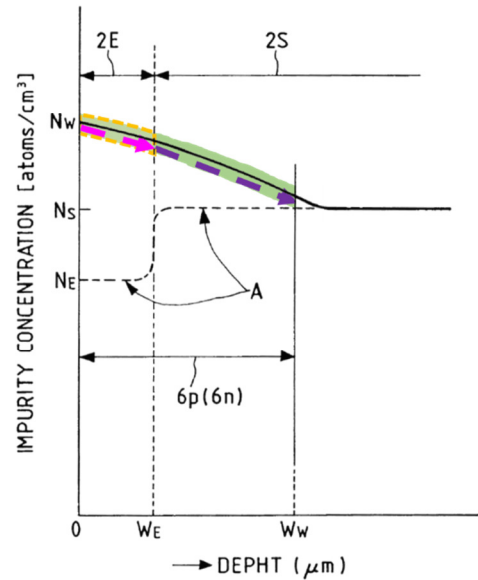
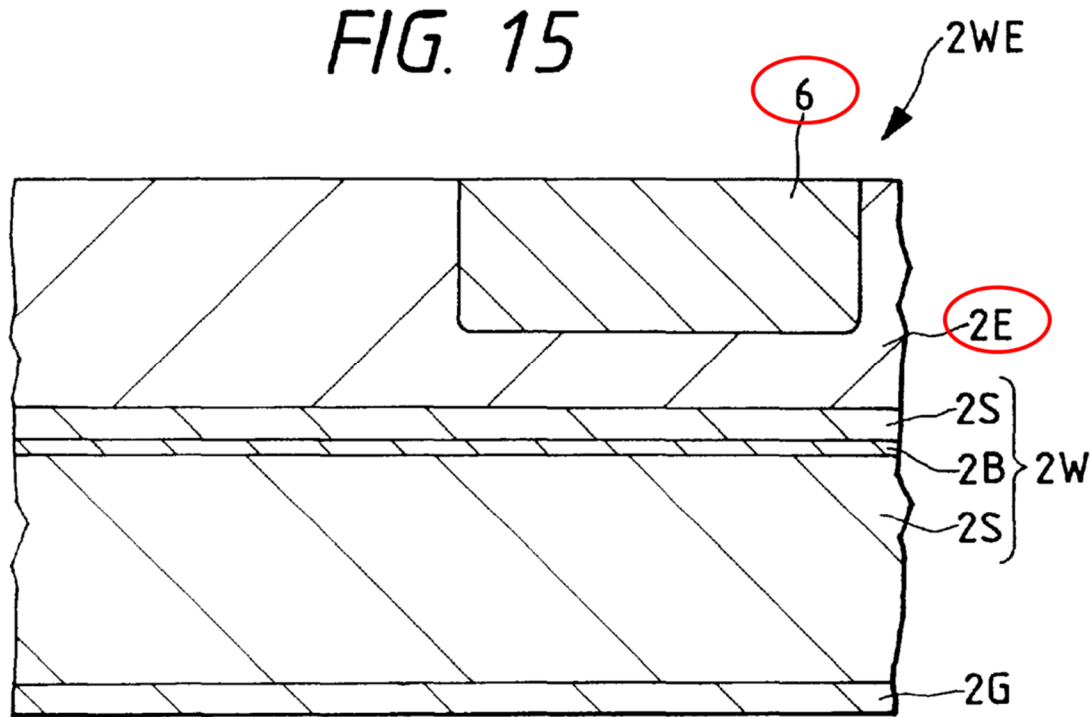


FIG. 17



(Kawagoe at FIGS. 16 and 17.)

Finally, even if “disposed in” were interpreted to require that the well region be disposed entirely within the epitaxial layer, it would have been obvious for a POSITA to modify Kawagoe’s FIG. 16 embodiment to have its well region contained solely within the epitaxial layer, and not extend into the substrate (as is depicted in FIG. 16 and 17). (Ex. 1003 at ¶ 125.) Kawagoe teaches embodiments of thicker epitaxial layers (Kawagoe at 13:49-53) where the n and p well regions are confined within the epitaxial layer, and do not extend to the substrate. (*Id.* at FIG. 15 (excerpted and annotated below).)



(Kawagoe at FIG. 15.)

Kawagoe further teaches a gradient whose “impurity concentration gradually lowered depthwise of said epitaxial layer” (Kawagoe at Abstract) and that the “impurity concentration [is] gradually lowered *depthwise of said semiconductor single crystal layer.*” (*Id.* at 3:22-23 (emphasis added); *see also id.* at 2:59-61 (making clear that the “semiconductor single crystal layer” is the epitaxial layer over the substrate).) (Ex. 1003 at ¶ 126.) Kawagoe thusly teaches a well region within the epitaxial layer.

A POSITA would have found it obvious to apply these teachings to modify the above-described FIG. 16 of Kawagoe to have the well region exist within the epitaxial layer (and not extend into the substrate), because it was a simple substitution of one known method with another to yield predictable results and was obvious to try. *See,*

e.g., *KSR*, 550 U.S. at 418. It would have been obvious to try; Kawagoe teaches that a POSITA has a degree of freedom for setting the impurity concentration and depth of its layers. (Kawagoe at 25:10-14.) A POSITA would have recognized this degree of freedom in creating layer depths, and would have found it an obvious variant to create the depth of the well region to be confined within the epitaxial layer and not extend into the substrate according to Kawagoe's other embodiments. (*See, e.g., id.* at 2:59-61, 3:22-23, 13:49-53, FIG. 16.) This would have been a simple substitution and would have yielded predictable results: a POSITA would understand that Kawagoe's well region, if it went up to but not into the substrate, would achieve a goal of Kawagoe (*i.e.*, attracting the minority carriers to the substrate, *id.* at 16:7-11) and would work for its intended purpose. (Ex. 1003 at ¶ 126.)

Thusly, Kawagoe discloses or at least renders obvious Limitation [44.6].

IX. THE BOARD SHOULD INSTITUTE IPR

1. 35 U.S.C. § 314(a)

On June 21, 2022, the Director issued an interim procedure regarding application of the *Fintiv* factors (Interim Procedure) in which the Director clarified that “the PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling evidence of unpatentability.” Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 9 (June 21, 2022). As just one example of compelling evidence here, Ground I is a single-reference obviousness ground explaining how Onoda discloses or,

at a minimum, renders obvious all of the Challenged Claims. While Onoda is subject to a pending IPR (IPR2024-00020 / IPR2024-00021), it is being presented differently here on new grounds never before examined and also presented in Ground II in combination with never-before-examined Nishizawa. Moreover, IPR2024-00020 and 21 are in their preliminary stages, having not reached preliminary response at the time of this filing. Further, Kawagoe has never before been provided as a single reference obviousness ground, and was never subject to any examination or review by the Board.

None of Petitioner's references (Onoda, Kawagoe, Nishizawa) were examined by the Board or the USPTO during prosecution. And, this evidence, "if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable" (Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," at 4) and the Board must decline to exercise its discretion under §314(a) to deny institution. *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022- 00938, Paper 8 at 9 (P.T.A.B. Nov. 1, 2022).

2. 35 U.S.C. § 325(d)

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020).

The Board has consistently "held that a reference that 'was neither applied

against the claims nor discussed by the Examiner does not weigh in favor of exercising [] discretion under §325(d).” *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7–11 (P.T.A.B. Nov. 5, 2019); *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5-6 (P.T.A.B. Aug. 6, 2019). That is the case here because none of the ground references (Onoda, Kawagoe, Nishizawa) is cited art, and the arguments presented herein were not considered during prosecution of the ’222 Patent.

Patent Owner has previously incorrectly argued that other art not at issue in this Petition was cumulative to already-examined art (U.S. Pat. Pub. No. 2003/0042511, Rhodes) in the ’222 Patent’s parent (’195 Patent). (Ex. 1011 at 21-24.) Patent Owner’s arguments there lack merit, and are similarly inapplicable to Onoda and Kawagoe.

Onoda and Kawagoe are not cumulative with Rhodes. The Examiner relied on Rhodes’ paragraphs [0046], [0047], [0049], and [0049], and FIGS. 5-14 in rejection, stating that well-regions 160/170/180 aid carrier movement from the surface regions to the substrate. (Ex. 1002 at 55-56.) In response, Patent Owner amended the claims to recite “VLSI digital” and that “the active channel regions” aid in carrier movement (Ex. 1002 at 72, 94), and further argued that Rhodes is inapplicable to CMOS image sensors because it only provides a graded dopant concentration in the image sensor. (Ex. 1002 at 74; *see also id.* at 97.) Patent Owner argued:

“Rhodes describes a CMOS image sensor- but, his sensor elements only uses electrons (a CMOS gate, by strict text book definition has a n-channel transistor that conducts electrons and a p-channel transistor that

conducts holes). The ‘graded dopant’ as described by Rhodes, is only in the ‘sensing element.’ Rhodes may have one million sensors (he may have a few CMOS transistors in periphery on non image sensing function). However, that does not make the device in Rhodes VLSI and certainly not CMOS VLSI.”

(*Id.* at 74; *see also id.* at 97.)

The Examiner thereafter dropped rejections based on Rhodes. (*Id.* at 111-115.)

Here, in contrast, both Onoda and Kawagoe describe CMOS and, moreover, provide graded dopants in p wells having active regions that form conductive channels in memory devices. (Ex. 1003 at ¶¶ 32-34) Moreover, Figure 2 of Onoda discloses forming P-type well regions (105a through 105c) and N-type well regions (103, 106a through 106c) in a lightly-doped semiconductor layer 102 that is formed through epitaxial deposition. (Onoda at FIG. 2.) Kawagoe similarly provides well regions doped into an epitaxial layer. (Kawagoe at FIG. 16.) Onoda and Kawagoe describe non-cumulative systems that are relevant to the claims in a manner that Rhodes was not.

Onoda and Kawagoe are not cumulative and, even assuming *arguendo* that they were, the Examiner overlooked Rhodes’ relevance to CMOS devices and downward graded dopant well regions as claimed due to Patent Owner’s arguments regarding Rhodes. In either case, review of the challenged claims is warranted.

3. Prior Petitions Do Not Warrant Denying Institution

While several Petitions have been filed, none of the prior challenges to the ’222

Patent reached an institution decision. In addition, the entity challenging the '222 Patent in this Petition here is a defendant in a district court case and would potentially be severely prejudiced if this Petition is not instituted. *Apple Inc. v. Uniloc 2017 LLC*, IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020). In light of the foregoing, *General Plastic* factors weigh strongly against discretionary denial. *Xilinx, Inc. v. Arbor Global Strategies, LLC*, IPR2020-01568, Paper No. 12 at 10 (P.T.A.B. Mar. 5, 2021).

Dated: February 3, 2024

Respectfully submitted,

/Bing Ai/

Lead Counsel

Miguel Bombach, Reg. No. 68,636

Back-up Counsel

Bing Ai, Reg. No. 43,312

John D. Esterhay, Reg. No. 73,512

John P. Schnurer, Reg. No. 52,196

Brianna Kadjo, Reg. No. 74,307

Runkun (Justin) Jiang, Reg. No. 78,118

Attorneys for Petitioner

PERKINS COIE LLP
11452 El Camino Real, Ste 300
San Diego, California 92130-2080
858.720.5700 (phone)
858.720.5799 (fax)

CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(d)

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this *Petition for Inter Partes Review* totals 12,012, excluding the parts exempted by 37 C.F.R. §42.24(a).

The word count was made using the built-in word count function in the Microsoft 365 software used to prepare this document.

Dated: February 3, 2024

Respectfully submitted,

PERKINS COIE LLP
11452 El Camino Real, Ste 300
San Diego, California 92130-2080
858.720.5700 (phone)
858.720.5799 (fax)

/Bing Ai/
Lead Counsel
Miguel Bombach, Reg. No. 68,636

Back-up Counsel
Bing Ai, Reg. No. 43,312
John D. Esterhay, Reg. No. 73,512
John P. Schnurer, Reg. No. 52,196
Brianna Kadjó, Reg. No. 74,307
Runkun (Justin) Jiang, Reg. No. 78,118

Attorneys for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of this PETITION FOR INTER PARTES REVIEW and supporting materials (Exhibits 1001-1030, 1032-1047 and Power of Attorney) have been electronically served in their entireties on counsel for patent owner as follows:

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

and the attorneys of record for Plaintiff in the concurrent litigation matter:

Brian E. Farnan - bfarnan@farnanlaw.com
Ala L. Whitehurst - awhitehurst@mckoolsmith.com
Archis Ozarkar - nozarkar@mckoolsmith.com
Arvind Jairam - ajairam@mckoolsmith.com
Emily Tate - etate@mckoolsmith.com
John B. Campbell, Jr. - jcampbell@mckoolsmith.com
Kaitlyn M. Dawson - kdawson@mckoolsmith.com
Kaylee Hoffner - khoffner@mckoolsmith.com
Michael J. Farnan - mfarnan@farnanlaw.com
Nicholas T. Matich - nmatich@mckoolsmith.com

In addition, the undersigned certifies that a true copy of the petition and supporting materials have been served on Patent Owner via email to its legal counsel:

Patent Owner Attorney
GHowison@munckwilson.com

Dated: February 3, 2024

Respectfully submitted,

/Bing Ai/

Lead Counsel

Miguel Bombach, Reg. No. 68,636

Back-up Counsel

Bing Ai, Reg. No. 43,312

John D. Esterhay, Reg. No. 73,512

John P. Schnurer, Reg. No. 52,196

Brianna Kadjo, Reg. No. 74,307

Runkun (Justin) Jiang, Reg. No. 78,118

PERKINS COIE LLP
11452 El Camino Real, Ste 300
San Diego, California 92130-2080
858.720.5700 (phone)
858.720.5799 (fax)

Attorneys for Petitioner