The Future of Analog IC Technology®

MP2953B

Digital Multi-Phase Controller with PMBus Interface for VR12.5

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DESCRIPTION

The MP2953B is a digital multi-phase controller that provides power for the core of the INTEL VR12.5 platform. It works with MPS' Intelli-Phase products to complete the multi-phase VR solution with minimal external components. It can be configured for 1 ~ 6 phase operation.

The MP2953B provides on-chip EEPROM to store and restore device configurations. Device configurations and fault parameters are easy to program or monitor using the PMBus interface. The MP2953B monitors and reports the output current through CS output from Intelli-Phase products.

The MP2953B is based on a unique digital multi-phase, non-linear control to provide fast transient response to load transient with minimal output capacitors. With only one power loop control method for both steady state and load transient, the power loop compensation is easily configured.

FEATURES

- 6-Phase Digital PWM Controller
- Intel's VR12.5 Compliant
- PMBus Compliant
- Serial VID Interface for Programming and Monitoring
- Pin Programmable SVID registers
- Built-In EEPROM to Store Custom Configurations
- Automatic Loop Compensation
- Less External Components than Conventional Analog Controllers
- Phase-Shedding at Light Load to Provide High Efficiency
- Phase-to-Phase Active Current Balancing
- Input and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- Open-Drain FAULT# Signal for Fault Notification
- RVP/OVP/UVP/OCP/OTP/UVLO Protection with Options of No Action, Latch, Retry, or Hiccup
- Adjustable Load-Line Regulation
- RoHS Compliant 5mmx5mm QFN-40

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Telecom and Networking Systems
- Base Stations

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TYPICAL APPLICATION

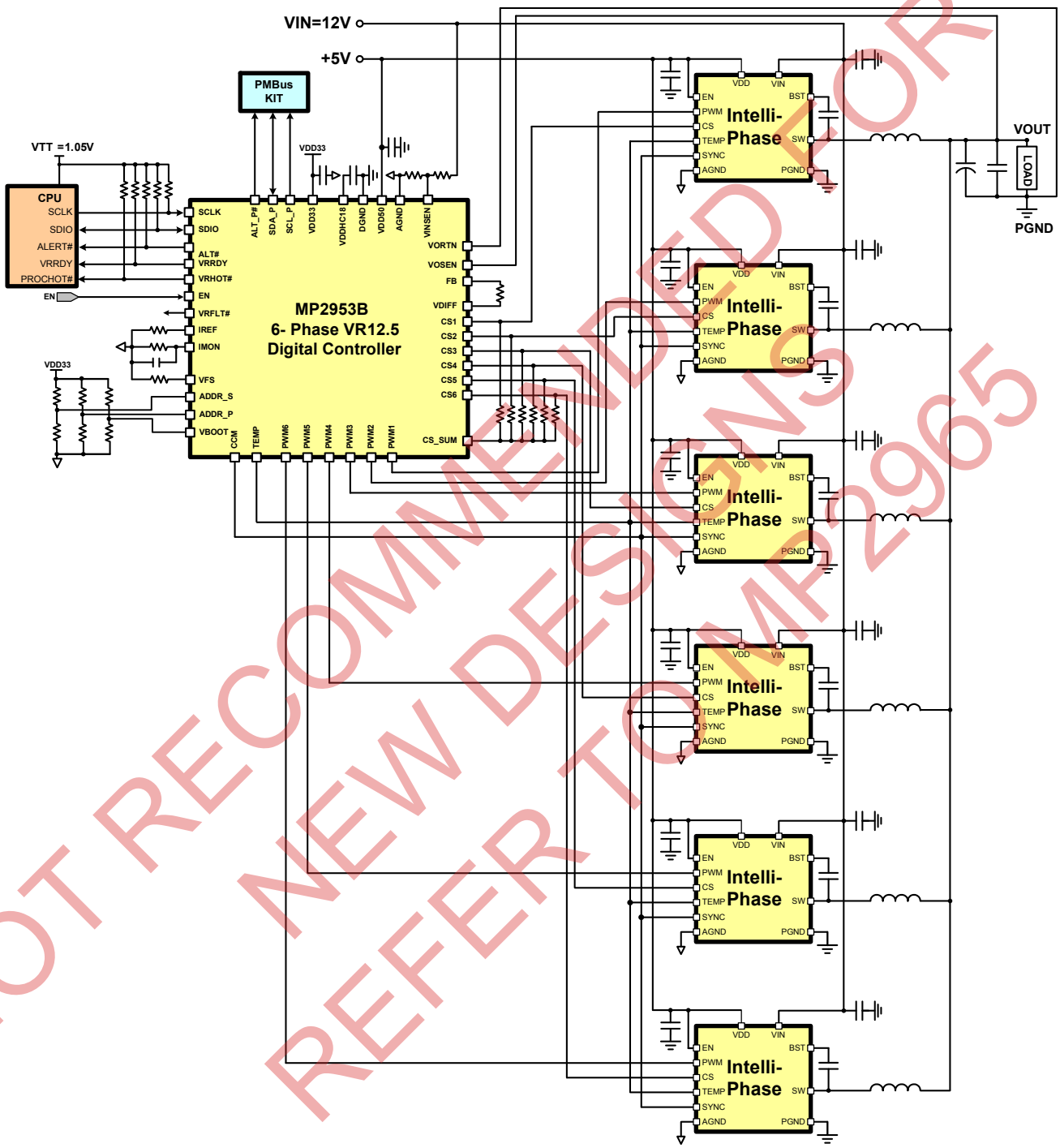

Figure a: 6 Phase application

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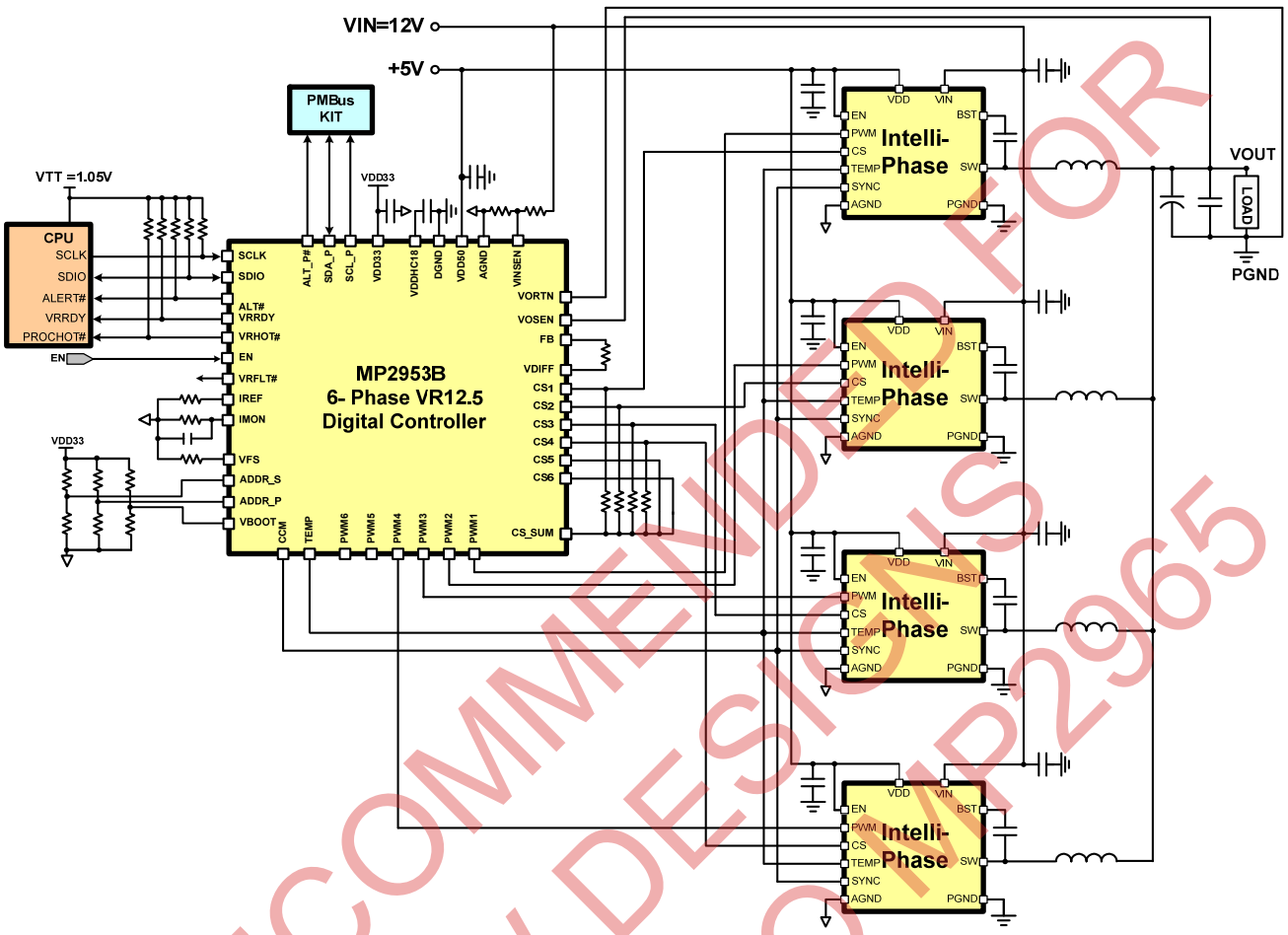

Figure b: 4 Phase application

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ORDERING INFORMATION

Part Number(*)	PACKAGE	Top Marking
MP2953BGU-xxxx(**)	QFN-40 (5mmx5mm)	*See Below*

* For Tape & Reel, add suffix (e.g. MP2953BGU-xxxx(**)-Z).

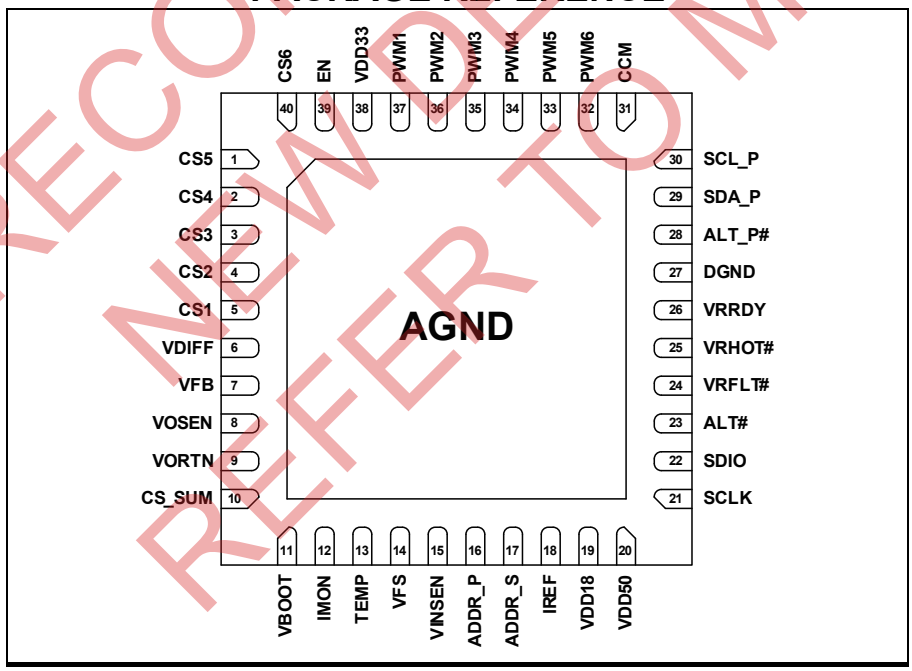
**: "xxxx" is the configuration code identifier for the register settings stored in the EEPROM. For the default case, the number will be "0000." Each "x" could have a hexadecimal value between 0 & F. Please work with the MPS FAE to create this unique number even if ordering the "0000" code.

TOP MARKING

MPSYYWW
MP2953B
LLLLLLL

MPS: MPS Prefix
YY: Year Code
WW: Week Code
MP2953B: Part Number
LLLLLLL: Lot Number

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

VDD50.....–0.3V to +6.5 V
VDD18.....–0.3V to +2.0 V
CS1 to CS6, PWM1 to PWM6, FB, VDIFF, VOSEN, VORTN, SCL_P, SDA_P, ALT_P#, CCM, EN, VDD33.....–0.3V to +3.6 V
All Other Pins.....–0.3V to +1.8 V
Continuous Power Dissipation (T_A = +25°C) (2)
……..…… ..3.4 W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

VDD50..... +5V
Operating Junction Temp. (T_J). -10°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-40 (5mmx5mm)	36	5	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 6-layer PCB.

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ELECTRICAL CHARACTERISTICS

VDD50 = 5 V, EN = 1V, VID = 0.50 V to 2.6 V, Current going into pin is positive, T_J =-10°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
REMOTE SENSE AMPLIFIER						
Bandwidth(5)	$GBW_{(RSA)}$			20		MHz
VORTN Current	I_{RTN}			-70	-400	µA
VOSEN Current	I_{VOSEN}			70	400	µA
OSCILLATOR						
Frequency	f_{OSC}	IREF=1.23V; RIREF=61.9kΩ	1.56			MHz
SYSTEM INTERFACE CONTROL INPUTS						
EN						
Input Low Voltage	$VIL_{(EN)}$				0.4	V
Input High Voltage	$VIH_{(EN)}$		0.8			V
Enable High Leakage	$IIH_{(EN)}$	EN=2V			3.6	µA
Enable Delay	T_A	EN High to SVID Ready		2	5	ms
THERMAL THROTTLING CONTROL						
VRHOT# Low Output Impedance		$I_{VRHOT\#}$ = 20mA, T_A = 25°C		8	12	Ω
VRHOT# High Leakage Current		VRHOT = 1.8V	-3		3	µA
IMON OUTPUT						
Current Gain Accuracy	I_{MON}/I_{CS_SUM}	Measured from I_{CS_SUM} to I_{MON}, I_{CS_SUM} =1.2mA		1:32		A/A
COMPARATOR (VFB & VREF)						
Propagation Delay(5)	t_{PD}			10		ns
Common-Mode Range			0		2.6	V
COMPARATOR (VFB & VREF-20mV)						
Propagation Delay(5)	t_{PD}			10		ns
Common-Mode Range			0		2.6	V
COMPARATOR (Protection)						
Under-Voltage Threshold	V_{DIFF} (UV)	Relative to Reference DAC Voltage		−300		mV
Over-Voltage Threshold	V_{DIFF} (OV)	Relative to Reference DAC Voltage		300		mV
		Relative to Protection DAC Voltage		400		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Reverse Voltage Detection Threshold(5)	$V_{OSEN\ (RV)}$	Relative to RTN, VDIFF is Falling		0		mV
		Relative to RTN, VDIFF is Rising		30		mV
CCM OUTPUT						
Output Low Voltage	V_{OL}	$I_{CCM(SINK)}$ = 400 µA		10	500	mV
Output High Voltage	V_{OH}	$I_{CCM(SOURCE)}$ = -400 µA	3	VDD33-0.02		V
PWM OUTPUTS						
Output Low Voltage	$V_{OL\ (PWM)}$	$I_{PWM(SINK)}$ = 400 µA		10	200	mV
Output High Voltage	$V_{OH\ (PWM)}$	$I_{PWM(SOURCE)}$ = -400 µA	3.15	VDD33-0.02		V
Rise and Fall Time(5)		C = 10pF		10		ns
PWM Tri-State Leakage		PWM = 1.5V; EN = 0V	-1		1	µA
SUPPLY						
Supply Voltage Range	VDD50		4.5	5	5.5	V
Supply Current	I_{VDD50}	EN=High. Both the SVID Bus and the Internal ID Bus are Idle. No-Load Condition. 6-Phase Configuration.		16		mA
UVLO Threshold Voltage	VDD_{UVLO}	VDD50 is Rising		4.13	4.5	V
UVLO Hysteresis(5)	VDD_{UVLO}	VDD50 is Falling		180		mV
1.8V REGULATOR						
1.8V Regulator Output Voltage	VDD18	I_{VDD18} = 0mA		1.8		V
1.8V Regulator Load Capability	I_{VDD18}	VOL = VDD18 - 40mV		30		mA
3.3V REGULATOR						
3.3V Regulator Output Voltage	VDD33	I_{VDD33} = 0mA		3.3		V
3.3V Regulator Load Capability	I_{VDD33}	VOL = VDD33 - 40mV		30		mA

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ELECTRICAL CHARACTERISTICS *(continued)*

VDD50 = 5 V, EN = 1V, VID = 0.50 V to 2.6 V, Current going into pin is positive, T_J =-10°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SVID Interface[5]						
CPU Interface Voltage (SDIO, SCLK)	V_{IL}	Logic Low			0.45	V
	V_{IH}	Logic High	0.65			V
	V_{hyst}	Hysteresis		50		mV
Termination Resistance (SDIO, SCLK, ALT#)[5]	R_{PU}		50	55	TBD	Ω
Leakage Current (SDIO, SCLK, ALT#)	IL	0V to VTT	-10		10	µA
Pad Capacitance (SDIO, SCLK, ALT#)	C_{PAD}				4	pF
Pin Capacitance (SDIO, SCLK, ALT#)[5]	C_{PIN}				5	pF
Buffer On Resistance (SDIO, SCLK, ALT#)[5]	R_{ON}		4		5	Ω
Maximum voltage (SDIO, SCLK, ALT#)	V_{MAX}	Transient Voltage including Ringing	-0.3		2.1	V
Slew Rate (SDIO, SCLK, ALT#)[5]		2nH, 4pF Load	0.5		2	V/ns
VR Clock to Data Delay[5]			4		8.3	ns
Setup Time				7		ns
Hold Time				14		ns
DAC (Reference Voltage)						
Range				2.88		V
Resolution per LSB				10		mV
Output Voltage Slew Rate[5]				100		mV/µs
DAC (Vout Calibration)						
Range				350		mV
Resolution				8		bit
DAC (Protection)						
Range		Adjustable via the PMBus		0.97~3.54		V
Resolution				10		mV

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VDD50 = 5 V, EN = 1V, VID = 0.50 V to 2.6 V, Current going into pin is positive, T_J =-10°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Management Features						
VIN UVLO Turn-On Threshold		Adjustable via the PMBus		10.2		V
VIN UVLO Turn-Off Threshold		Adjustable via the PMBus		9		V
Thermal Protection Threshold		DBh = 961Eh		150		°C
Thermal Protection Hysteresis		DBh = 961Eh		30		°C
PMBus DC Characteristics (ALT_P, SDA_P, SCL_P)						
Input High Voltage	V_{IH}	SCL_P, SDA_P	2.4			V
Input Low Voltage	V_{IL}	SCL_P, SDA_P			0.8	V
Input Leakage Current		SCL_P, SDA_P, ALT_P	-10		10	µA
Output Low Voltage	V_{OL}	ALT_P Sinks 2mA			400	mV
Maximum Voltage	V_{MAX}	Transient Voltage including Ringing	-0.3	3.3	3.6	V
Pin Capacitance(5)	C_{PIN}				10	pF
PMBus Timing characteristics(5)						
Operating Frequency Range			10		400	kHz
Bus Free Time		Period between Stop and Start Condition	4.7			µs
Holding Time			4.0			µs
Repeated Start Condition Setup Time			4.7			µs
Stop Condition Setup Time			4.0			µs
Data Hold Time			300			ns
Data Setup Time			250			ns
Clock Low Time Out			25		35	ms
Clock Low Period			4.7			µs
Clock High Period			4.0		50	µs
Clock/Data Fall Time					300	µs
Clock/Data Rise Time					1000	µs

Notes:

5) Guaranteed by design or characterization data, not tested in production.

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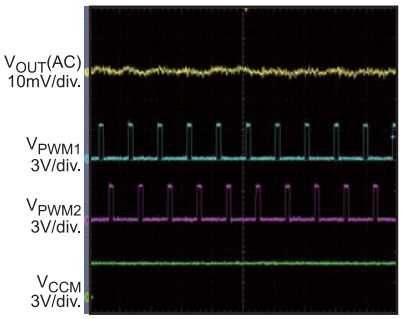
TYPICAL PERFORMANCE CHARACTERISTICS

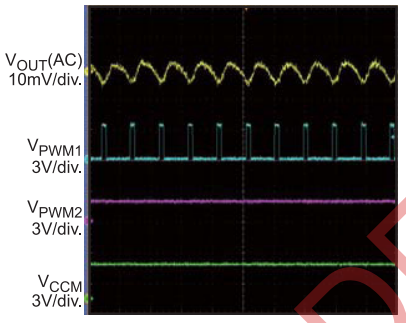
Steady State

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz, I_{OUT} = 160A, PS0



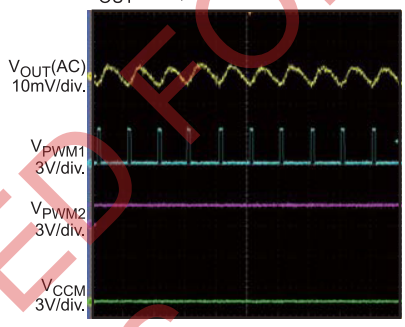
Steady State

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz, I_{OUT} = 20A, PS1



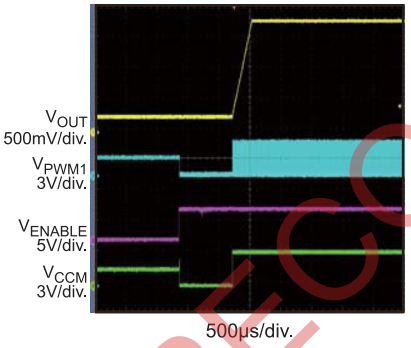
Steady State

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz, I_{OUT} = 5A, PS2



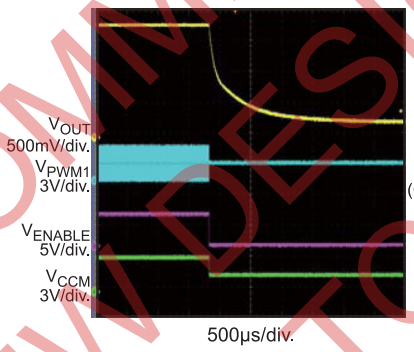
Enable On

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz



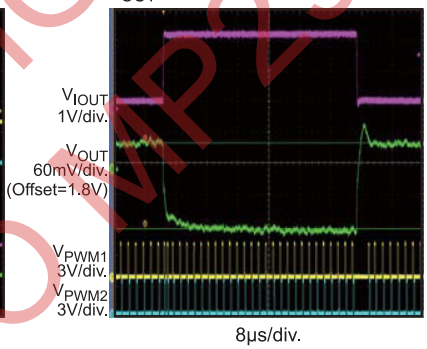
Enable Off

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz



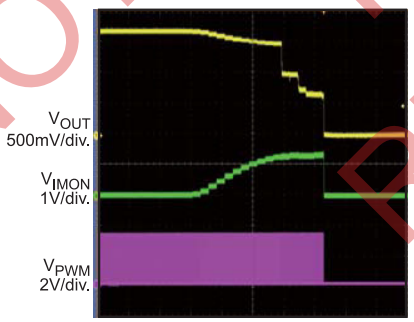
Transient

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz, I_{OUT} = 30 to 181A

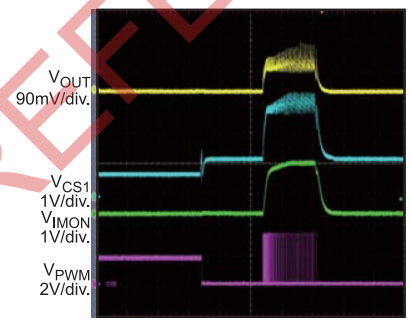


OCP

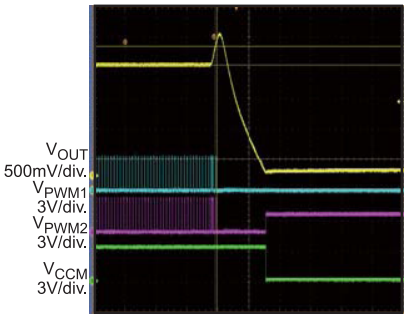
V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH, C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz



SCP @ Enable On



OVP



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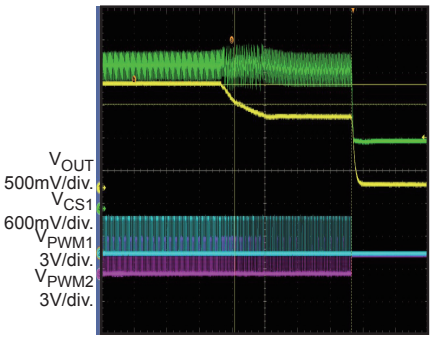
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

UVP

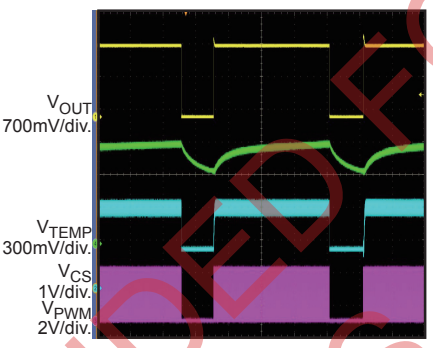
V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH,
C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz,



100µs/div.

OTP

V_{IN} = 12V, V_{OUT} = 1.8V, L = 150nH,
C_{OUT} = 40x47µF+20x22µF, F_{SW} = 500kHz,



1s/div.

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PIN FUNCTIONS

Pin #	Name	I/O	Description
1	CS5	I	**Phase 5 Current Sense Input.** Connect CS of the unused phase to CS_SUM pin.
2	CS4	I	**Phase 4 Current Sense Input**. Connect CS of the unused phase to CS_SUM pin.
3	CS3	I	**Phase 3 Current Sense Input.** Connect CS of the unused phase to CS_SUM pin.
4	CS2	I	**Phase 2 Current Sense Input.** Connect CS of the unused phase to CS_SUM pin.
5	CS1	I	**Phase 1 Current Sense Input.**
6	VDIFF	O	**Differential Remote Sense Amplifier Output.**
7	FB	I/O	**Feedback.** FB sources a current proportional to the sensed output current (Idroop). This current flows through the resistor between FB and VDIFF to create a voltage drop proportional to the load current. Ensure the resistor between VDIFF and FB has a value that will set a proper load line.
8	VOSEN	I	**Positive Remote Voltage Sense Input.** VOSEN is connected directly to the VR output voltage at the load and should be routed differentially with VORTN.
9	VORTN	I	**Remote Voltage Sensing Return Input.** VORTN is connected directly to ground at the load and should be routed differentially with VOSEN.
10	CS_SUM	I	**Total Phase Current, which Monitors AVP.** Connect the active phase CS signal to CS_SUM through current-sense resistors.
11	VBOOT	I/O	**Boot Voltage Setting**.
12	IMON	I/O	**Analog Total Load Current Signal.** IMON sources a current proportional to the sensed total load current from CS_SUM. Connect an external resistor from IMON to GND to program the gain.
13	TEMP	I	**Analog Signal from the VR to the VID Controller to Indicate the Power Stage Temperature.** The MP2953B only supports temperature sensing from Intelli-Phase. Connect all of Intelli-Phase's VTEMP pins together to produce the maximum junction temperature and then connect to TEMP.
14	VFS	I/O	**Switching Frequency Setting.**
15	VINSEN	I	**Input Voltage Sensing**. Connect VINSEN to the system input voltage through a resistor divider.
16	ADDR_P	I/O	**PMBus Address Setting.**
17	ADDR_S	I/O	**SVID Address Setting.**
18	IREF	I	**Internal Bias Current.** Connect an 61.9kΩ resistor from IREF to GND.
19	VDD18	O	**1.8V LDO Output for Current Sense.** Connect a 1μF bypass capacitor to digital ground.
20	VDD50	I	**5V Analog Power Supply.** Connect a 10μF bypass capacitor to digital ground.
21	SCLK	I	**Source Synchronous Clock from the CPU**. Frequency range from 10MHz to 26MHz.
22	SDIO	I/O	**Data Signal between the CPU and VID Controller.**
23	ALT#	O	**Alert**. ALT# is an open-drain output. It is the alert signal from the VID controller to the CPU.

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PIN FUNCTIONS

Pin #	Name	I/O	Description
24	VRFLT#	O	**VR Fault.** VRFLT# is an open-drain output. When Vin or Vout OVP occurs, VRFLT# is asserted to shut down the input power supply.
25	VRHOT#	O	**Voltage Regulator Thermal Throttling Logic Output.** VRHOT# is an open-drain output. VRHOT# pulls low actively if the monitored temperature exceeds the programmed VRHOT# temperature threshold.
26	VRRDY	O	**VR Ready Output.** VRRDY is an open-drain output that signals when the output voltage is outside of the proper operating range. A VTT rail is expected for pull up; however, some systems may pull up to a maximum voltage of 3.3V with an external pull-up circuit.
27	DGND	I/O	**Digital Ground.**
28	ALT_P#	O	**Open-Drain Output that Asserts Low when a Warning has Occurred.**
29	SDA_P	I/O	**Data Signal between the PMBus Controller and the VID Controller.**
30	SCL_P	I	**Source Synchronous Clock from the PMBus Controller.**
31	CCM	O	**Forced CCM Operations Enable.** CCM stays high in power state 0 and 1. It pulls low actively during PS2/3 to enable DCM operation.
32	PWM6	O	**Tri-State Logic-Level PWM Outputs**. Each output is connected to the input of Intelli-Phase's PWM pin. The logic levels are 0V for low logic and 3.3V for high logic. The output is set to tri-state (High-Z) to shut down both the high-side MOSFET and the low-side MOSFET of Intelli-Phase.
33	PWM5	O	
34	PWM4	O	
35	PWM3	O	
36	PWM2	O	
37	PWM1	O	
38	VDD33	O	**3.3V LDO Output for the Internal Digital Power Supply.** Connect a 1μF bypass capacitor to digital ground.
39	EN	I	**Enable Control for the Controller.**
40	CS6	I	**Phase 6 Current Sense Inputs.** Connect CS of the unused phase to CS_SUM pin.
PAD	AGND	I/O	**Analog Ground.**

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OPERATION

The MP2953B is a digital multi-phase VR12.5 compliant controller for Intel microprocessors. It operates in 1-, 2-, 3-, 4-, 5-, or 6-phase. It contains blocks of precision DAC and ADC, differential remote voltage sense amplifier, fast comparators, current sense amplifiers, internal loop compensation, load-line setting, VR_Ready monitor, temperature monitor, PMBus interface, SVID interface, and EEPROM for custom configuration.

Fault protection features include under-voltage lockout (Vin-UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), over-temperature protection (OTP), and reverse-voltage protection (RVP).

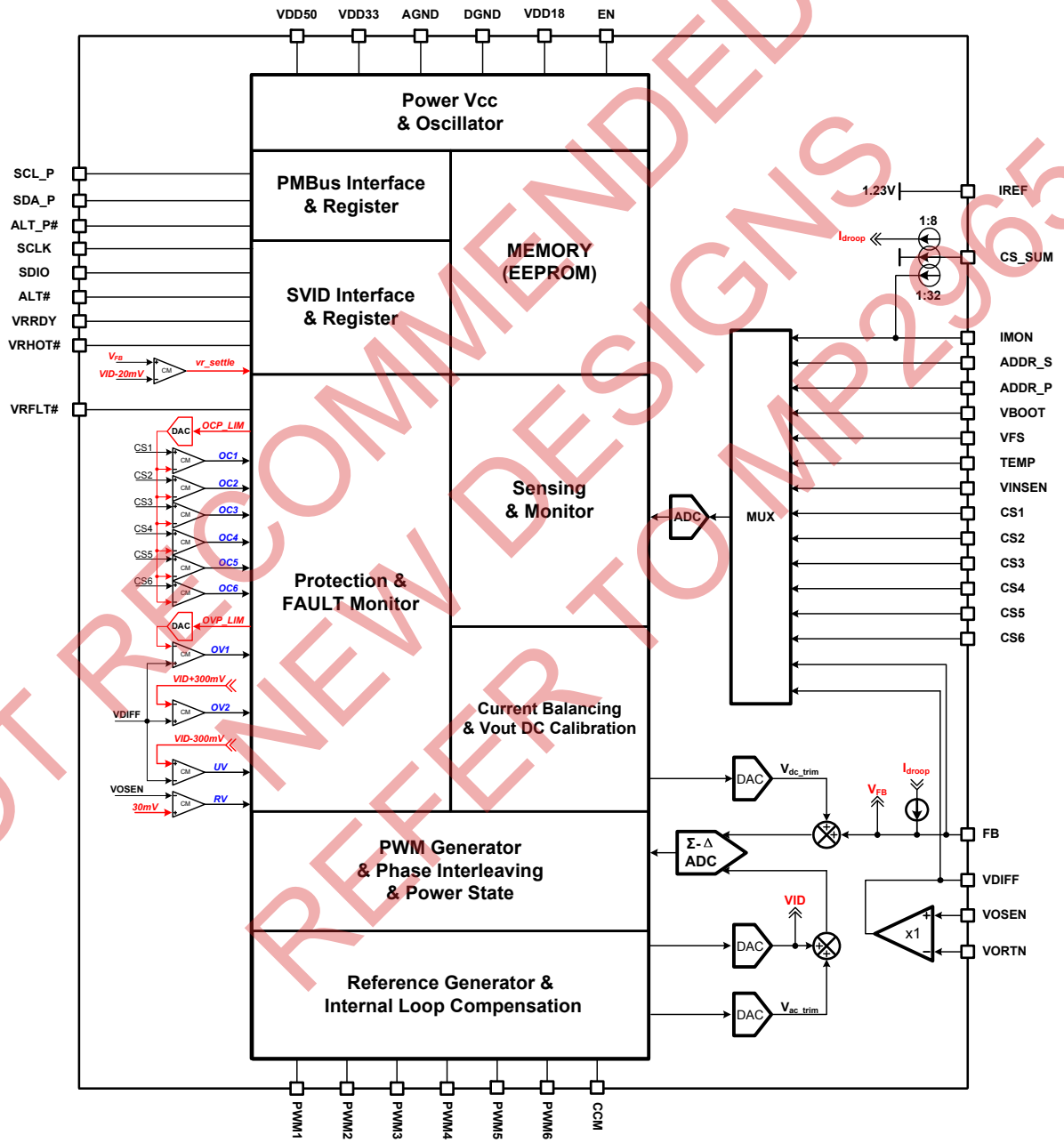

FIGURE 1. System Functional Block

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EEPROM Operation

The MP2953B provides EEPROM for storing application configuration parameters. The default values are pre-programmed at the factory. The data can be programmed again using STORE_USER_ALL command via the PMBus.

EEPROM is read automatically during the power-on sequence or by receiving the RESTORE_USER_ALL command from the PMBus. The state machine of the MP2953B is shown in Fig. 2.

EEPROM operation is accomplished easily with MPS GUI software.

EEPROM is subject to more than 100,000 erase/write cycles.

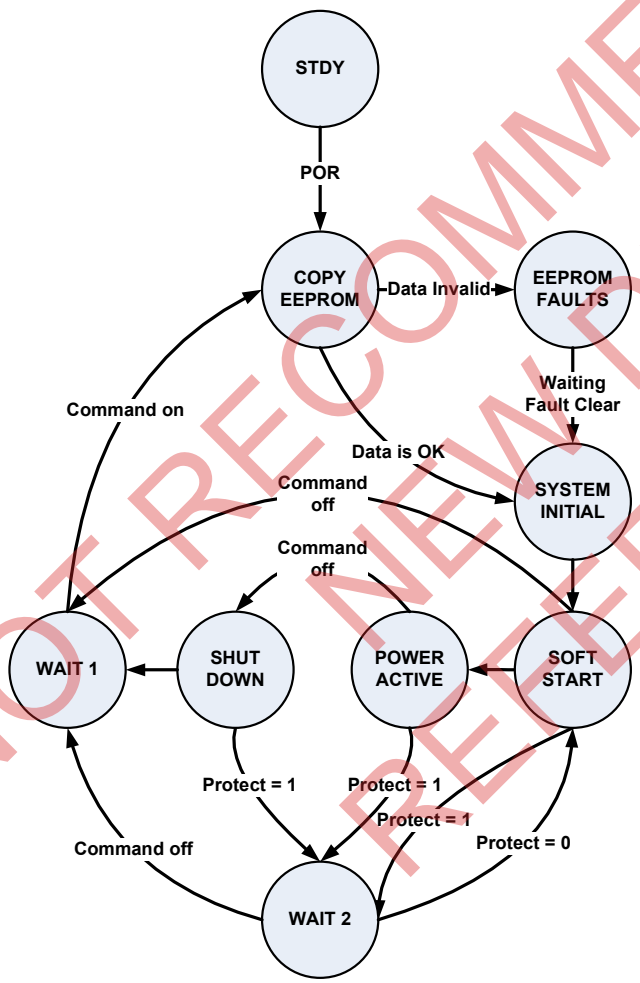

FIGURE 2. System State Machine

System Configuration

The MP2953B provides a differential output voltage sense, an input voltage sense, and an output enable function. Working with the Intelli-Phase (MPS Driver MOS), the MP2953B senses the per-phase current and the maximum temperature among the power MOSFETs with minimal external components. The PWM of the MP2953B outputs 3.3V compatible tri-state signals before outputting power to the load.

The boot voltage, per-phase switching frequency, SVID address, and PMBus slave address can be set using pin configurations or using the registers via the PMBus.

The MP2953B can be configured as a 3~6 phase operation application via the PMBus (see Table 1).

TABLE 1. Phase Configuration and Active PWM Pins

MFR_VR_CONFIG [14:12]	Phase Number	Active PWM Pins
3'b100	2	1, 3
3'b011	3	1, 2, 3
3'b100	4	1, 2, 3, 4
3'b101	5	1, 2, 3, 4, 5
3'b110	6	1, 2, 3, 4, 5, 6

An unused PWM enters tri-state, and the active phase becomes interleaving automatically.

Power-On Configuration

The MP2953B is supplied by +5V voltage, its internal LDOs produce +3.3V voltage for the analog circuit and +1.8V voltage for the digital circuit. The system is re-set by the internal power-on re-set signal (POR). After the system exits POR, the data in the EEPROM loads to the registers to configure the VR operation. If the setting is loaded from pins, then resistors with 1% tolerance must be connected from VBOOT, VFS, ADDR_S, and ADDR_P to ground in order to set the parameters of the controller. The initialization process takes 700µs.

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EEPROM Fault and Wait State

If the data in the EEPROM is invalid, the system enters the EEPROM FAULT state and waits for the error to clear. The data in the EEPROM is ignored if the system detects an EEPROM fault. The following 3 actions clear the EEPROM fault in order to re-set with the default value in the register:

1. Clear the EERPOM FAUTL via the PMBus;
2. Store the register data into the EEPROM via the PMBus and re-start again;
3. Receive the SetVID command and run the VR with default values in the registers.

Once the registers are loaded from the EEPROM, the MP2953B enters a soft-start state. If any of the conditions below occur, the system will remain in the waiting state until the conditions are removed:

1. Protection is triggered (i.e. the sense input voltage is under the VIN_ON threshold), or the sensed temperature is above the OTP_LIMI, OVP1. The system enters the WAIT2 state until the protection signal is re-set.
2. The internal enable command is off, the system enters the WAIT1 state until the enable command is on; the EEPROM will be read again.

Soft-Start (SS)

Before entering the power-active state, the MP2953B executes the soft-start process to charge the output capacitor with the SetVID_Slow slew rate (until the reference reaches the boot voltage).

Fig. 3 shows the soft-start process with a pre-bias function. The CCM signal is low to turn off all phases until the reference voltage rises above the output voltage.

Once the pre-bias is over, the controller sets PWM1 high (with a narrow minimum on pulse). The controller increases the on-time according to the VID and sensed input voltage. In next cycle, the controller triggers phase 2 to turn on and exit tri-state. All other phases will exit tri-state in this manner.

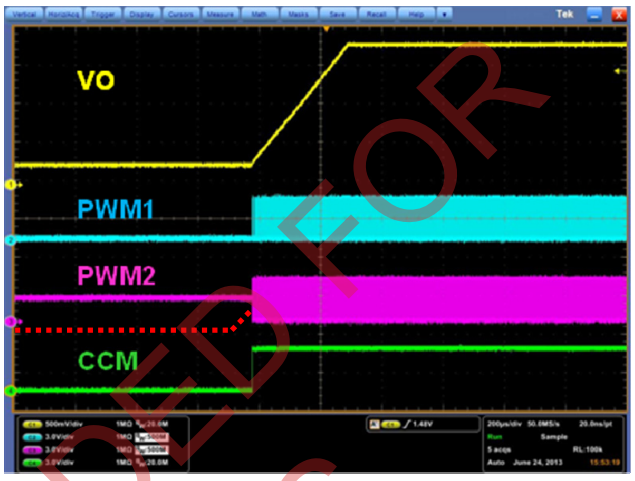

FIGURE 3. Soft-Start with Pre-Bias

If boot voltage is nonzero, the output voltage ramps up to the boot voltage and asserts ALERT#. ALERT# de-asserts after the STATUS1 register is read. When receiving a new SetVID command, the controller ramps to the target voltage with the rate of SVID_Fast or SVID_Slow.

If the boot voltage or the ICC max is set initially to 0, the PWM is kept in tri-state until a valid SVID voltage is received, and the ICC max is set above 0. The controller then ramps the voltage to the target value and asserts ALERT#.

After the controller completes the soft-start process, it is ready to output power to the load and assert VR_READY.

Power Active

The MP2953B applies a digital, non-linear control to provide fast transient response and easy loop compensation. The duty cycle of each phase's PWM updates in real-time, according to the input voltage and reference voltage. Figure 4(a) shows the steady-state performance with load current at 160A.

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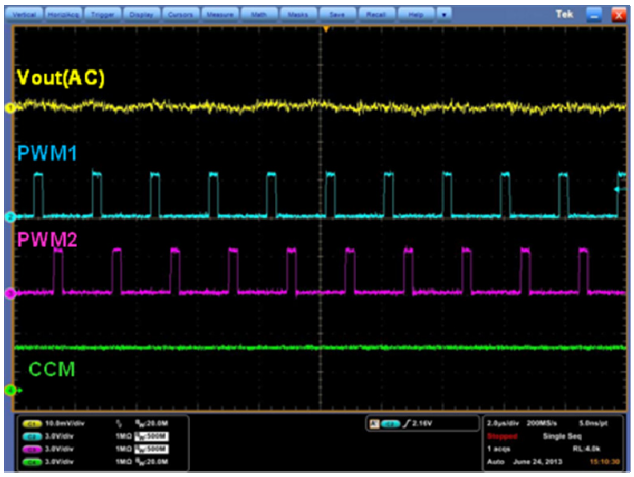

FIGURE 4(a). Steady State with Load @160A

Load transient performance is illustrated in Figures 4(b)—(d). The MP2953B adaptively changes the switching frequency of each individual phase during load transient to achieve fast closed-loop speed. Only one set of loop compensation is needed, so it is very easy to set the loop parameter.

Fig. 4(b) shows no ring-back when the load steps up from 36A to 180A. Fig. 4(c) shows that the overshoot of the output voltage is small during load release. Fig. 4(d) shows the high-load transient rate; the output voltage is stable. The MP2953B meets Intel VR12.5 standards with a minimum number of output capacitors.

FIGURE 4(b). Load Step Up @ 1kHz

FIGURE 4(c). Load Step Down @ 1kHz

FIGURE 4(d). Load Step @1MHz

Power State Change

The SVID bus changes the VR into different power states to achieve high efficiency during light-load conditions. These states are entered by programming the power-state register using SVID's SetPS command. The VR optimizes its power loss to flatten the efficiency curve over the operating current range with the power-state commands issued by the CPU.

In PS0 mode, all phases run in CCM. In PS1 mode (<20A load, typically), only one phase runs with synchronous switching; the other phases are in tri-state. In PS2 mode (<5A load, typically), only one phase runs in the diode emulation mode; the switching frequency decreases automatically due to the light-load condition.

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During the dynamic VID transition issued by the SVID commands of either SetVID_Fast or SetVID_Slow, the power state is changed to PS0 by default and runs in full-phase PWM mode. Once the output is well regulated to the new target voltage, the power state stays in PS0 until the CPU sends a new command to change the power state.

The MP2953B implements the PSI function in the following ways:

1) Tri-state of PWM: When the VR receives the SetPS1 command, it sets PWM2~6 outputs to tri-state (High-Z) or the third level;

2) CCM Control: When the VR receives the SetPS2 command, phase 1 must enter DCM. The VR will set PWM2~6 outputs to tri-state and pull CCM low (which is connected to SYNC of Intelli-Phase). Then phase 1 will enter diode emulation mode. Figures 5(a) and 5(b) show the phase-shedding and phase-adding process when the VR receives the SetPS command.

Three sets of registers are provided to set the loop compensation of the power state. Customers can use the MPS GUI to set these registers automatically. Customers only need to select the fast transient performance loop or the steady-state performance loop.

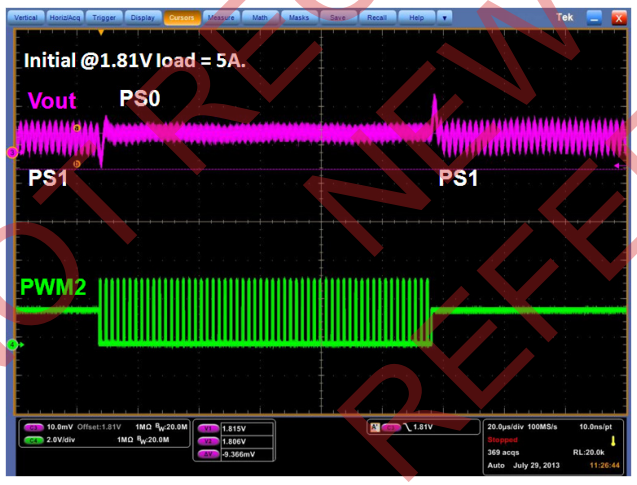

FIGURE 5(a). 1-Phase CCM →6-Phase →1-Phase CCM

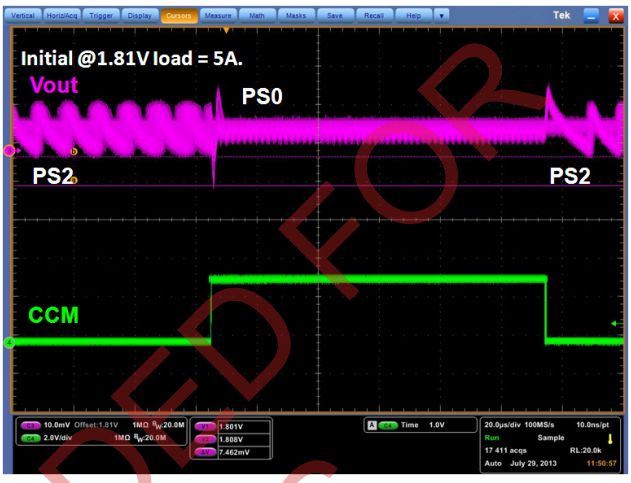

FIGURE 5(b). 1-Phase DCM → 6-Phase →1-Phase DCM

Shutdown

The MP2953B enters shutdown mode in the following ways:

1. When EN pulls low, the VR begins High-Z shutdown.
2. When the operation command is set to soft off, the VR will soft shut down with the rate of SVID_Slow.
3. When the operation command is set to immediate off, all PWM signals will enter tri-state to turn off all phases.
4. UVP, VIN_UVLO, OCP, and OTP turn off all phases immediately by forcing all PWM signals to enter tri-state.
5. OVP1/2 forces all PWM signals low to turn off all high-side MOSFETs and turn on all low-side MOSFETs to discharge the voltage in the output capacitor.

If the VR is shut off by the enable signal, it enters the WAIT1 state after shutdown. The VR can be re-started by setting the enable signal to high. When enable is high, the system will read EEPROM again.
If the VR is shut off by the protection signal, it enters the WAIT2 state after shutdown. The VR can be re-started by re-setting the protection signals. Once the protection signals are re-set, it takes 12.5ms before the soft-start begins. This state occurs when the protection mode is set to hiccup mode or retry mode.

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If the VR is in the WAIT2 state and the enable signal is pulled low, the VR enters the WAIT1 state to wait for the system to re-start. This state occurs if the protection mode is set to latch mode or retry mode.

Output Voltage Sense

The output voltage is remote sensed with the differential amplifier. The sensed output voltage is used for loop compensation, over-voltage protection, under-voltage protection, and monitoring via the PMBus.

The output voltage with the load-line regulation component is compared with the reference voltage from the VID-DAC. The error is converted to a series of high-speed digital signals by the special ADC.

The factory trimmed bandgap voltage reference and differential remote sense amplifier ensures precise setpoint and output voltage accuracy.

Input Voltage Sense

The 12V supply voltage on VINSEN is sampled and used for Vin_UVLO, Vin_OVP fault protection, and monitoring via the PMBus.

A 16:1 attenuation network is connected to VINSEN (see Fig. 6). Recommended values for a 12V system are R_{VIN_1} = 15kΩ and R_{VIN_2} = 1kΩ, with a 1% tolerance or better. Usually, C_{VINSEN} is not required or may be populated up to a maximum of 10nF for noise suppression.

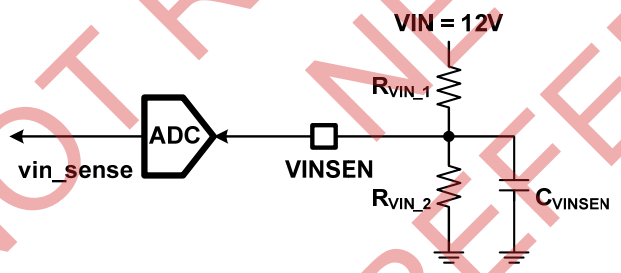

FIGURE 6. VIN Resistor Divider Network

Total Current Sense

The total current is sensed from CS_SUM; a proportional current comes from IMON. Place a resistor from IMON to ground to generate a voltage proportional to the output current. The IMON voltage is sampled and converted by ADC and then converted to the direct format or Iccmax format for the current report. The R_{IMON} is calculated with equation (1).

$$R_{IMON} = \frac{5120}{\alpha I_{CCMAX}} (k\Omega) \quad (1)$$

Where α 1 by default (which can be used to increase the current report resolution).

The current report for the CPU is used to avoid exceeding the thermal design point and maximum current capability of the system. Also, the current report is used for total current fault protection.

The MP2953B contains a user-programmable scaling factor and a programmable current offset. The programmable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of Intel turbo.

Inductor Current Sense

The MP2953B works with MPS Intelli-Phase to sense the phase inductor current and the total current (see Fig. 7). The cycle-by-cycle current information is used for phase-current balancing, over-current protection, and active voltage positioning (output-voltage droop).

The current sense gain is 10μA/A for Intelli-Phase products. The resistor R_{CS} is connected from CS to CS_SUM. CS_SUM is a 1.23V constant voltage, and it is capable of sinking small current to provide voltage shifts that meet the operating voltage range of CS.

Different Intelli-Phase products have different operating voltage ranges of CS, V_{CS_MIN}, and V_{CS_MAX}. Refer to each Intelli-Phase's datasheet to determine the minimum and maximum operating voltage range. Use equation (2) to determine a proper R_{CS} value:

$$V_{CS_MIN} < I_{CS} R_{CS} + 1.23V < V_{CS_MAX}$$
$$I_{CS} = I_L \times 10 \times 10^{-6} \quad (2)$$

Paired with Intelli-Phase, the MP2953B does NOT need temperature compensation

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and impendence matching to achieve accurate current sense.

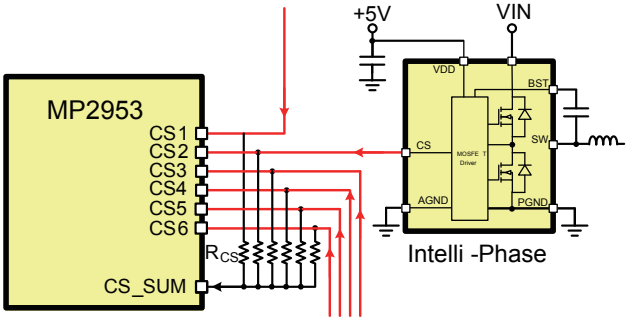

FIGURE 7. Current Sense with Intelli-Phase

Temperature Sense

The MP2953B measures the external temperature by connecting all the Intelli-Phase VTEMP (see Fig. 8). The sensed temperature is used for over-temperature fault protection, and the assert VRHOT# signal is used for the CPU.

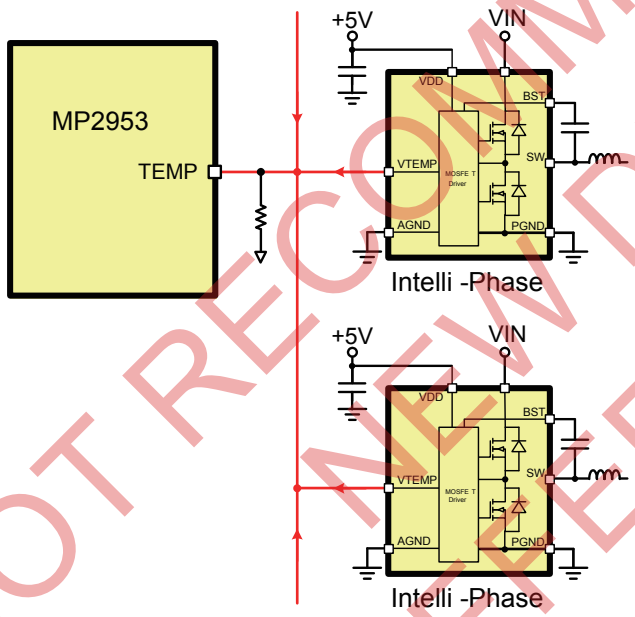

FIGURE 8. External Temperature Sense

VTEMP of Intelli-Phase is a voltage output proportional to the junction temperature. The junction temperature can be calculated from equation (3):

$$T_{JUNCTION} = \frac{V_{TEMP} + 100mV}{10mV/^{o}C} \quad (3)$$

$$\text{for} \quad T_{JUNCTION} > 10^{o}C$$

For example, if the VTEMP voltage is 700mV, the junction temperature of that Intelli-Phase is 80˚C. VTEMP can NOT go below 0V, so it will read 0V for junction temperature lower than 10˚C.

Dynamic Voltage Identification (DVID)

The MP2953B supports Dynamic VID change through three SVID commands: SetVID_Fast, SetVID_Slow, and SetVID_Decay. By default, the slew rate for SetVID_Fast is 20mV/µs; the slew rate for SetVID_Slow is 5mV/µs; the slew rate for SetVID_Decay is determined by the load current and output capacitor bank.

If the VR receives a SetVID_Fast/Slow command in a low-power state (PS1/2/3), the VR will enter PS0 then change voltage, so it will always operate in full-phase PWM mode during a voltage change by SetVID_Fast/Slow.

During dynamic VID, OVP2 (which is VID +300mV) is temporarily disabled. However, OVP1 (which is VOUT_MAX +400mV) remains enabled.

The MP2953B applies an advanced digital control method to improve the output voltage performance during SetVID_Fast/Slow voltage changes.

Ramping Up

When the output voltage is ramping up, the inductor current becomes higher to charge the output capacitors. This current introduces a large positive droop voltage and lowers the output voltage. Once ramping ends, the output voltage may be smaller than the minimum regulation tolerance budget (5µs after Alert#), which is unacceptable.

Ramping Down

When the output voltage is ramping down, the inductor current becomes smaller to discharge the output capacitors (which will continue to discharge the output capacitors when ramping ends and may lead to an output-voltage undershoot.

The MP2953B applies a low-pass filter for the VID-DAC to smooth out the reference voltage when the output voltage is ramping down.

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Fig. 9 shows the output voltage of SetVID_Fast upward following the completion of the previous SetVID_Fast downward (SR = 20mV/µs).

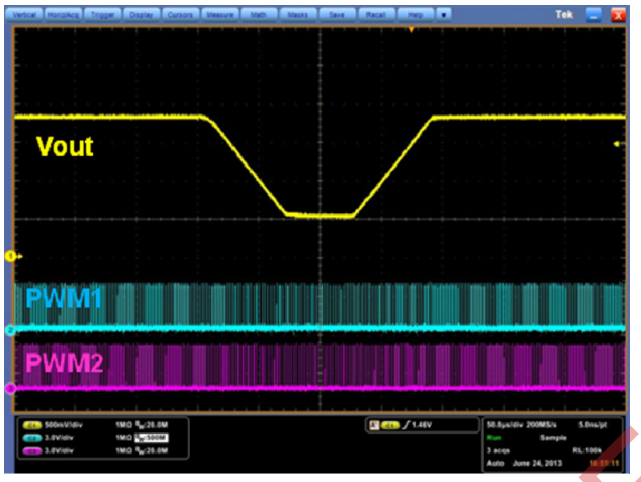

FIGURE 9. SetVID_Fast Downward → SetVID_Fast Upward

If the controller receives a SetPS command while the output voltage is ramping from the previous SetVID command (except for the SetVID_Decay command), then the controller will send a reject response (see Fig. 11(b)) to the SetPS command as an indication that it cannot carry out the command.

Figures 10(a) and 10(b) show different categories of decay preemption. The dynamic VID process is very smooth as there is no undershoot or ringback of the output voltage during the transient.

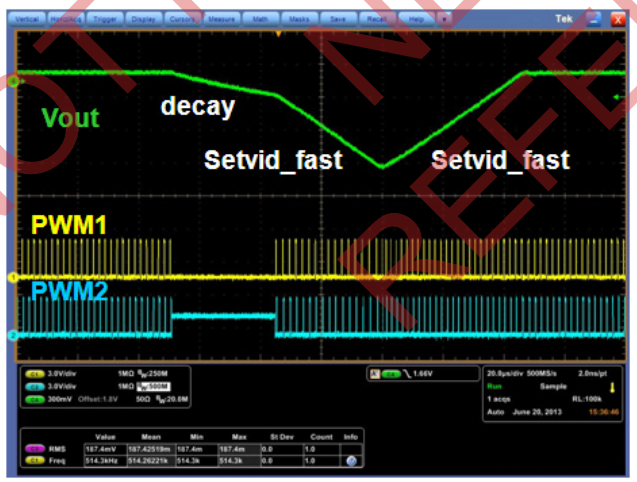

FIGURE 10(a). Decay (Interrupted)→SetVID_Fast (Interrupted)→SetVID_Fast (Finished)

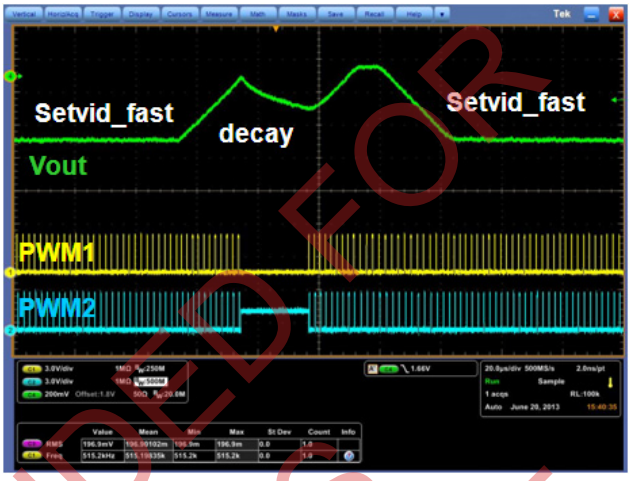

FIGURE 10(b). SetVID_Fast (Interrupted) → Decay (Interrupted) → SetVID_Fast (Finished) → SetVID_Fast (Finished)

PMBus & SVID Communication

The MP2953B supports real-time monitoring for the VR operation parameters and status with the PMBus and SVID interface. Table 2 lists the monitored parameters.

TABLE 2. PMBus & SVID Monitored Parameters

Parameter	PMBus	SVID
Output Voltage	X	X
Output Current	X	X
Output Power	X	X
Temperature	X	X
Input Voltage	X	X
Phase1~6 current	X	
POWERGOOD	X	X
OV	X	
OC	X	X
UV	X	
OT	X	X
CML	X	

Fault Monitoring and Protection Features

The MP2953B supports fault monitoring and the following protection features:

- **Vin UVLO**:
  a) The VR shuts off immediately if the input voltage is below VIN_OFF, and it re-starts when the input voltage is above VIN_ON.

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b) The VR latches if the input voltage is above VIN_OV_FAULT_LIMIT.
c) The VR is warned if the input voltage is below VIN_UV_WARNING_LIMIT.

- **Under Voltage**: When the output voltage is below VID – 300mV for a pre-set time, the VR either latches off or re-starts depending on the user selection via the PMBus.
- **Over Voltage**:
  a) When the output voltage is above VID + 300mV for a pre-set time, the VR latches off (with all the low-side MOSFETs turned on). It can be programmed to re-start after the fault condition clears.
  b) When the output voltage is above Vout_Max + 400mV for another pre-set time, the VR latches off (with all the low-side MOSFETs turned on).
- **Reverse Voltage**: All the low-side MOSFETs turn off if the output voltage is below 30mV.
- **Over Current**: When the total current is above the OCP level for a pre-set time, the VR latches off or re-starts.
- **Over-Temperature Indicator (VRHOT#, Active Low)**: When the temperature is above OTP_LIMIT, the VR latches until the temperature falls below OTP_LIMIT-OTP_HYS.
- **Fault# Signal (CFP)**: When Vin is above VIN_OV_FAULT_LIMIT or the output voltage is above Vout_Max +400mV, then Fault# pulls low actively.
- **CML**: The PMBus communication fault.
- **EEPROM Fault**: The data in the EEPROM is invalid.

All fault conditions can be monitored via the PMBus.

OVP, OCP, and UVP modes have options of no action, latch, retry, or hiccup mode. After the fault condition clears, the MP2953B waits12.5ms before attempting to re-start again. A 12.5ms delay ensures a sufficiently low duty-cycle stress rate to prevent regulator components from being damaged by power cycling.

For latched protection mode, external intervention is required to clear the latch before the VR can re-start again. External intervention includes the enable signal toggle, controller power-supply recycle, or input-voltage supply toggle.

The fault status is record in the registers. Once triggered, the fault registers report faults even if the fault condition no longer exists. Fault registers may be cleared manually by issuing a fault clear command, controller power-supply cycle, or the enable signal toggle (either by EN or command enable toggle).

The following is a brief description of each fault:

Over-Voltage Protection (OVP)

The OVP circuit monitors the output voltage for an over-voltage condition. The over-voltage signal generation is shown in Fig. 11.

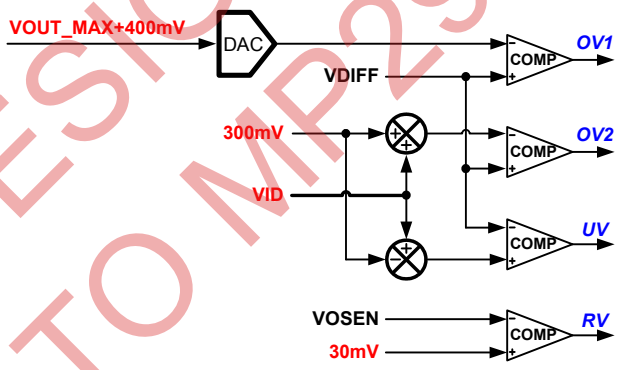

FIGURE 11. OV, UV, and RV Signal Generation

There are two levels of over-voltage protection:

1. OVP2 (VID+300mV) and
2. OVP1 (VOUT_MAX + 400mV).

The OVP2 signal is blanked during the soft-start and soft-shut down process to avoid a false trigger by a pre-bias condition. Also, the OVP2 monitor is disabled during a VID decay transition. It re-activates after finishing the VR settle re-assertion transition.

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Fig. 12 summarizes the blanking conditions for OVP2 monitor. The OVP1 monitor is active when the controller is enabled, regardless of fault conditions. This ensures that the load is protected against high-side MOSFET leakage while the MOSFETs are turned off. In the event of an OVP condition, the PWMs are latched low with CCM=1. This turns off the high-side MOSFETs and turns on the low-side MOSFETs to crowbar the output voltage. The OVP latch can be re-set only by the enable toggle, the VCC toggle, or reverse-voltage protection (RVP). Fig. 13 shows the OVP fault latch for both levels.

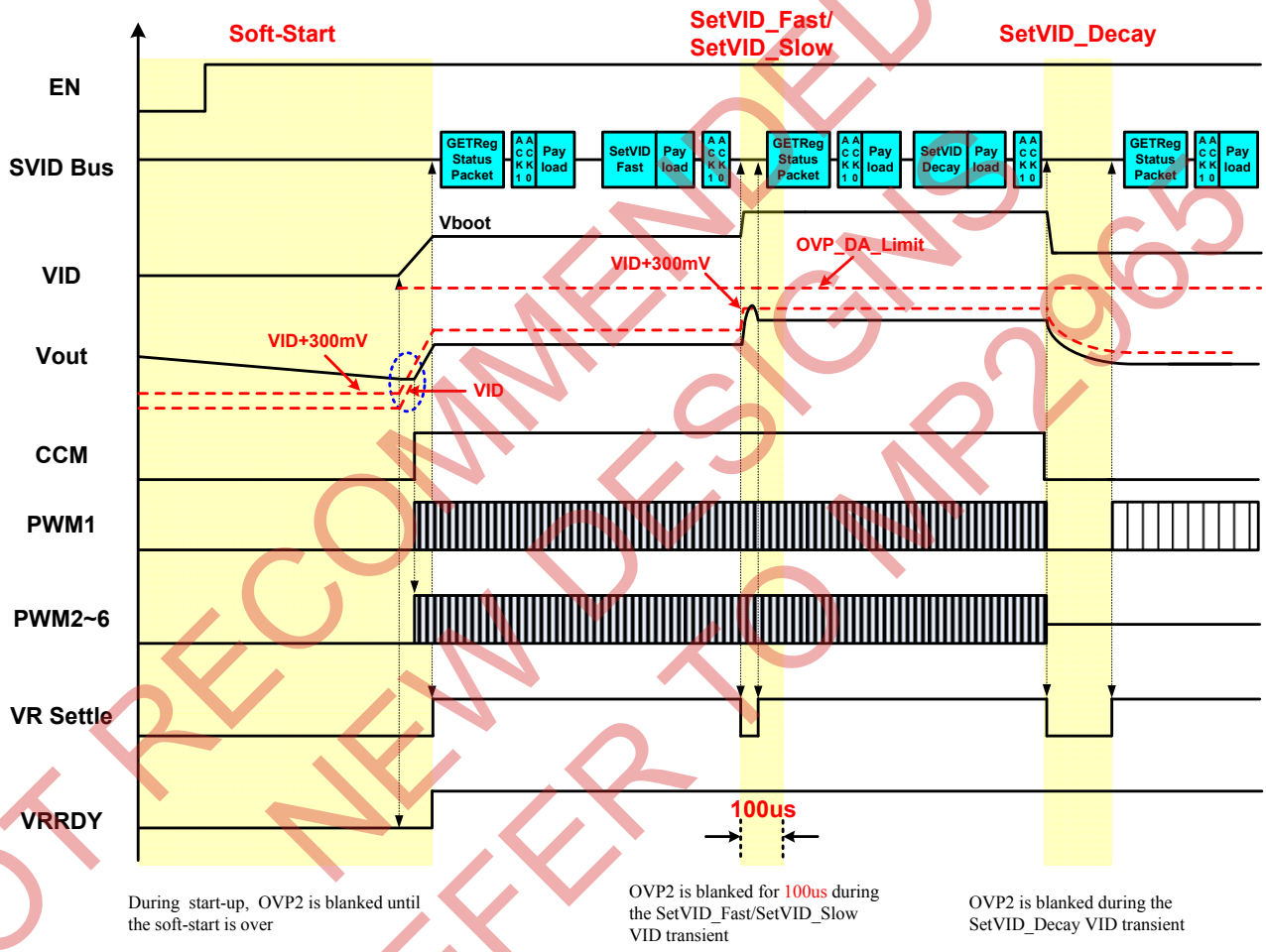

FIGURE 12. OVP Protection Blanking Conditions

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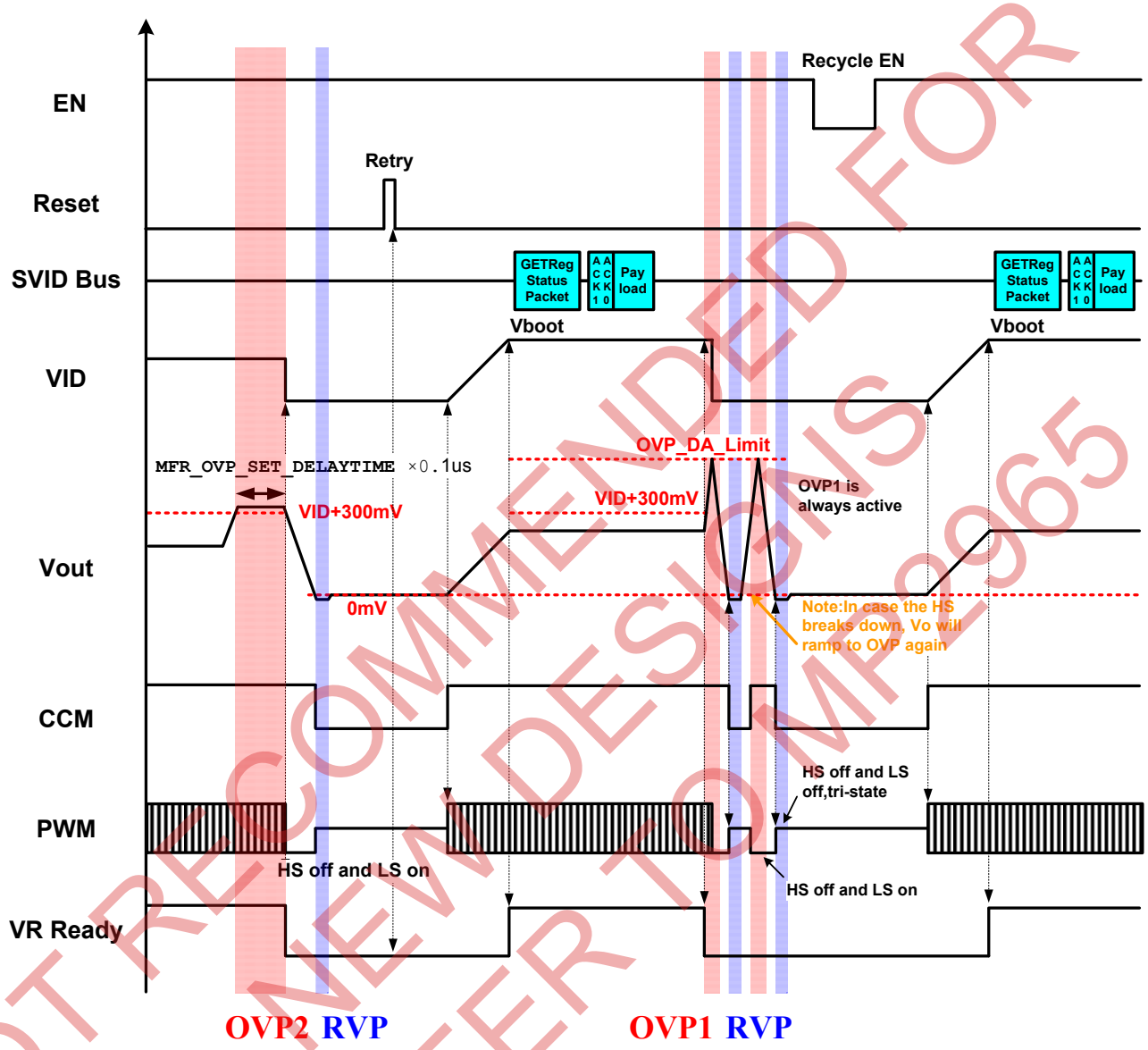

FIGURE 13. OVP and RVP Fault Protection

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Over-Current Protection (OCP)

The MP2953B utilizes the valley point over-current limit method to limit each phase current.

If the present phase current is higher than the setting valley point, then this phase will not turn on until its current falls below the setting level. If the present phase is blocked for 150ns, then the next phase will turn on instead so as to regulate the output voltage at the set point.

The valley point over-current level can be programmed via the PMBus to limit the per-phase current.

The total current protection is triggered if the sensed average total current is higher than the OC threshold.

Since this protection averages the output current over many switching cycles, the average current OCP threshold can be set very close to the expected maximum output load for accurate over-current protection.

Fig. 14 shows the OCP process for total current protection. The total current protection is disabled during the soft-start process, and it is enabled when soft start has finished.

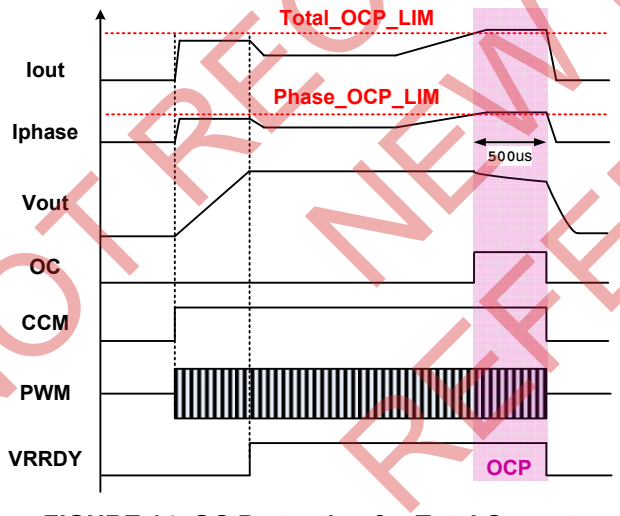

FIGURE 14. OC Protection for Total Current

Fig. 15 shows the process when the output is shorted to ground. During this process, per-phase OCP limits the phase current. After a pre-set time, the VR is shut off by the total current OCP.

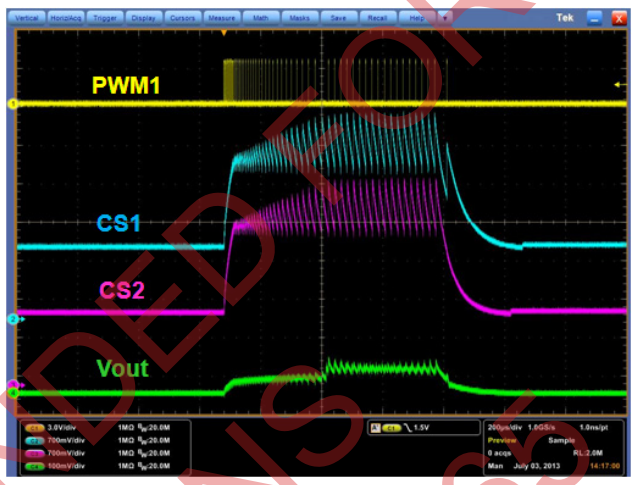

FIGURE 15. OCP with Output Dead Short

Under-Voltage Protection (UVP)

If the output voltage is below VID – 300mV for a given time, the system triggers UVP and immediately shuts down by turning off all phases.

Fig. 16 shows the UVP process.

Normally, UVP is triggered when PWM signals are blocked by the OC signals (when the per-phase current limit is reached) as shown in Fig. 17.

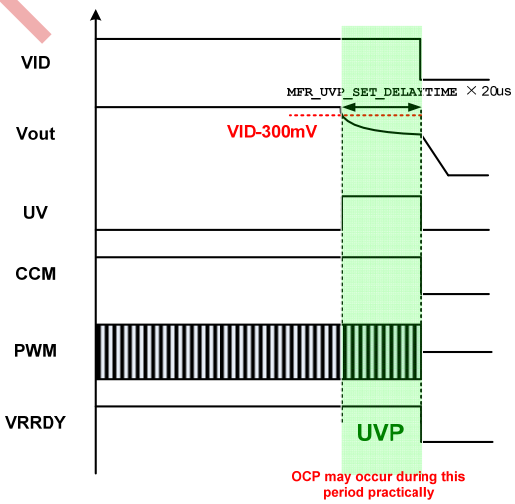

FIGURE 16. Under-Voltage Protection

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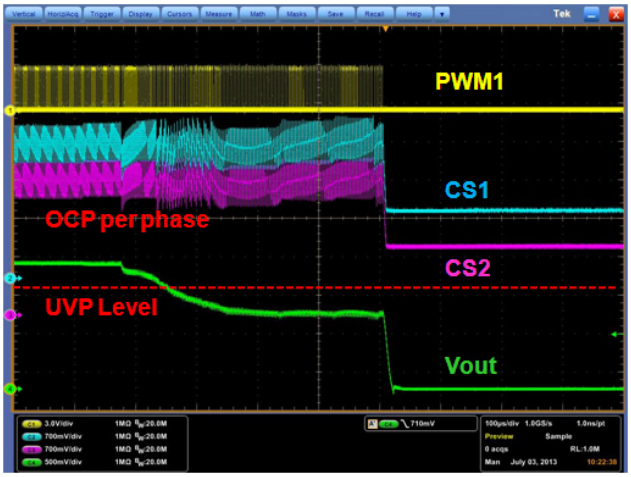

FIGURE17. UVP Triggered when Per-Phase Current is Limited

Reverse -Voltage Protection (RVP)

A large reverse inductor current may cause negative output voltages, which harm the CPU and other output components. The MP2953B provides RVP without additional system costs.

VOSEN monitors the output voltage (see Fig. 10). Any time the VOSEN voltage falls below 30mV, the MP2953B triggers RVP by latching all PWM outputs to High-Z state. The reverse inductor current can re-set quickly to 0A by dissipating the energy in the inductor to the input DC voltage source through a forward-biased body diode of the high-side MOSFETs.

Occasionally, OVP results in negative output voltage because turning on all low-side MOSFETs leads to a very large reverse inductor current. The VR controller's RVP monitoring function remains active even after OVP latch-off to prevent damage to the load by negative voltage.

The RVP latch can only be re-set by toggling enable, power cycling VCC, or when OVP occurs (see Fig. 13).

Catastrophic Failure Protection (CFP)

The MP2953B has a dedicated CFP output which triggers in the event of OVP1 or input voltage above VIN_OV_FAULT_LIMIT.

In server computer systems, this signal is used commonly to shut down immediately the input supply (by firing a shunting SCR in order to blow a fuse or by turning off the AC power supply). This feature is active during the power-on sequence in case a computer shuts down, and the user just recycles the power supply's AC input.

VR_HOT#

The VR_HOT# fault is asserted when the sensed external temperature exceeds the temperature's maximum threshold. It is used for fault reporting only and it can NOT shut down the system. Also, VR_HOT# has a fixed 3°C hysteresis and is enabled after the initialization state. VR_HOT# is initialized in High-Z state upon device power-up.

EEPROM Fault

If the data in the EEPROM is checked as invalid, the system enters the EEPROM FAULT state and waits for the error to clear. It is reported in the fault register.

Communication Failure

A data transmission fault occurs when information is not properly transferred between the devices. Several data transmission faults are listed below:

- Sending too few data
- Reading too few data
- Host sends too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults assert ALT_P#. The CLEAR_FAULTS command de-asserts ALT_P#; however, if the faults still exist, ALT_P# asserts again.

Active Voltage Positioning (AVP)

The MP2953B supports AVP by connecting R_{droop} between V_{FB} and V_{DIFF}. An internal current-sense circuit produces the I_{droop} current source (which is 1/8 of the total current signal) from CS_SUM. I_{droop} injects to R_{droop} from VFB to produce the feedback

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voltage with droop voltage for regulation with the reference voltage.

Given the application's need for RLL load-line regulation, R_{droop} can be calculated according to equation (4):

$$R_{DROOP} = \frac{8R_{LL}}{K_{CS}} \quad (4)$$

Where K_{CS} is the current sense gain of Intelli-Phase.

Phase Current Balancing

The per-phase current is sensed and compared with the average phase current. Each phase's PWM on time is adjusted individually to balance the currents.

The MP2953B applies Σ-Δ Modulation and delay line loop in the current balance modulation so as to increase the resolution of the current balance modulation and greatly reduce the jitter of t_{ON}. The resolution of the time modulation of the digital system is 5ns. By applying Σ-Δ modulation, the digital ton resolution can be increased to 0.08ns.

Figures 18(a) and 18(b) show phase current balance results with and without Σ-Δ modulation.

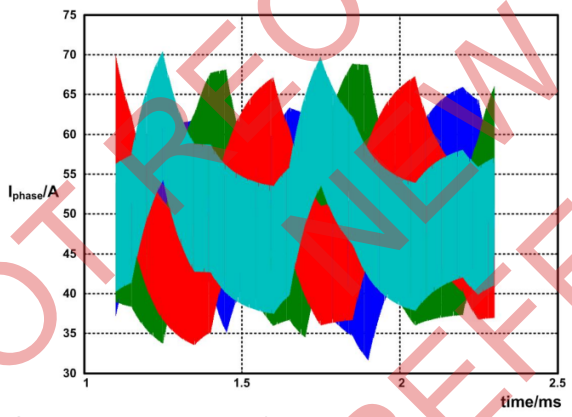

FIGURE 18 (a). Phase Current Balance without Σ-Δ Modulation

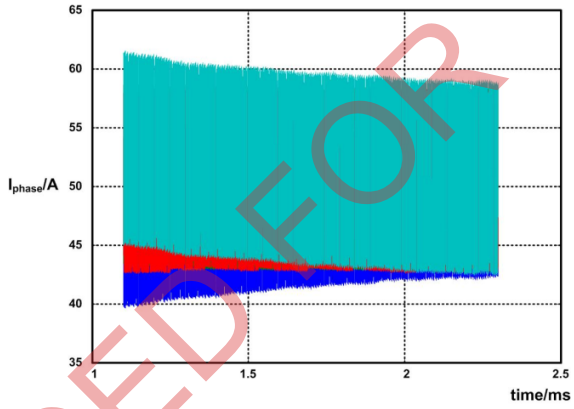

FIGURE 18(b). Phase Current Balance with Σ-Δ Modulation

Test Mode

The MP2953B provides test mode for users to test the chip with open-loop operation. In order to avoid the chip being protected, OVP1/2, UVP, OTP, OCP, and Vin_UVLO should be disabled via the PMBus.

SVID Interface

To support multiple VR devices used on the same SVID bus, the registers MFR_ADDR_SVID or ADDR_S are used to program the SVID address for each VR.

The SVID address is a 4-bit code. There are 14 addresses for up to 14 voltage regulator controllers or voltage rails. The final addresses 0Eh and 0Fh are "All Call" addresses and all the VR controllers respond to these addresses.

The "All Call' address is used only with SetVID or SetPS commands. It can NOT be used with GET, SetRegADR, or SetRegDAT commands. The VR will NAK those commands with an "All Call" address. The VR acknowledges an "All Call" address in the same manner as a single address. To get more accuracy value from the pin configuration, place a 1% tolerance resistor (R_{TOP}) from the pin to 3.3V and a resistor (R_{BOTTOM}) from the pin to ground. Table 3 shows resistor values for different SVID addresses.

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TABLE 3. SVID Address by ADDR_S Pin

SVID Address	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
00H	NS	0
01H	3.32	0.1
02H	3.32	0.178
03H	3.32	0.301
04H	3.32	0.422
05H	3.32	0.562
06H	3.32	0.698
07H	3.32	0.887
08H	3.32	1.1
09H	2.0	0.806
0AH	2.0	0.931
0BH	2.0	1.07
0CH	2.0	1.27
0DH	2.0	1.65

PMBus Interface

To support multiple VR devices used with the same PMBus interface, the registers MFR_ADDR_PMBUS or ADDR_P can be used to program the PMBus address.

The PMBus address is a 7-bit code; 4MSB bit is already fixed to 0100b. The MP2953B supports 8 addresses for up to 8 voltage regulator controllers or voltage rails by placing a 1% tolerance resistor (R_{TOP}) from the pin to 3.3V and a resistor (R_{BOTTOM}) from the pin to ground. The PMBus "All Call" address is 00h.

Table 4 shows the resistor values for different PMBus addresses.

TABLE 4. PMBus Address

PMBus Address	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
20H	3.32	0.0698
21H	NS	0
22H	3.32	0.1
23H	3.32	0.178
24H	3.32	0.301
25H	3.32	0.422
26H	3.32	0.59
27H	2	0.976

VBOOT Setup

The boot voltage of the MP2953B can be set using either the pin or the register via the PMBus.

To set using the pin, place a 1% tolerance resistor (R_{TOP}) from the pin to 3.3V and a resistor (R_{BOTTOM}) from the pin to ground. Table 5 shows 7 resistor values for the 7 boot voltage.

TABLE 5. Boot Voltage Setting by Pin

Vboot (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
1.75	3.32	2.74
1.70	2	1.15
1.65	2	0.953
1.50	2	0.806
1.35	2	0.681
1.20	2	0.316
0	NS	0

To set using the PMBus, the boot voltage can support the entire VID table.

Switching Frequency Setup

The switching frequency of MP2953B can be set using either the pin or the register via the PMBus.

To set using the pin, a 1% tolerance resistor should be connected between VFS and ground. Table 6 shows 9 resistor values for the 9 per-phase switching frequency.

TABLE 6. Frequency Setting by Pin

Resistor (kΩ) 1%	Voltage (V)	Fs (kHz)/phase
0	0	200
4.75	0.095	300
8.45	0.169	400
13.7	0.277	500
19.1	0.378	600
24.0	0.479	700
28.7	0.580	800
34.8	0.703	900
59	1.181	1000

To set using the PMBus, the switching frequency can be programmed from 200kHz to 1MHz with 10kHz step.

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PMBUS COMMANDS

Command Code	Command Name	Type	Bytes	Default Value	Data Formats
01h	OPERATION	r/w	1	80h	Direct
03h	CLEAR_FAULTS	send	0	-	-
15h	STORE_USER_ALL	send	0	-	-
16h	RESTARE_USER_ALL	send	0	-	-
21h	VOUT_COMMAND	r/w	2	007Eh	VID
24h	VOUT_MAX	r/w	2	00FFh	VID
25h	VOUT_MARGIN_HIGH	r/w	2	0000h	VID
26h	VOUT_MARGIN_LOW	r/w	2	0000h	VID
35h	VIN_ON	r/w	2	E850h	Linear
36h	VIN_OFF	r/w	2	E848h	Linear
38h	IOUT_CAL_GAIN	r/w	2	88A8h	Linear
39h	IOUT_CAL_OFFSET	r/w	2	F800h	Linear
55h	VIN_OV_FAULT_LIMIT	r/w	2	E870h	Linear
58h	VIN_UV_WARN_LIMIT	r/w	2	E84Ch	Linear
78h	STATUS_BYTE	r	1	00h	Direct
79h	STATUS_WORD	r	2	0000h	Direct
7Ah	STATUS_VOUT	r	1	00h	VID
7Bh	STATUS_IOUT	r	1	00h	Direct
7Ch	STATUS_ INPUT	r	1	00h	Direct
7Dh	STATUS_ TEMPERATURE	r	1	00h	Direct
7Eh	STATUS_ CML	r	1	00h	Direct
88h	READ_VIN	r	2	E800h	Linear
89h	READ_IIN	r	2	E000h	Linear
8Bh	READ_VOUT	r	2	0000h	VID
8Ch	READ_IOUT	r	2	F000h	Linear
8Dh	READ_TEMPERATURE	r	2	0019h	Linear
96h	READ_POUT	r	2	0000h	Linear
BAh	MFR_SLOPE_SLEWRATE_PS2	r/w	2	01C1H	Direct
BBh	MFR_SLOPE_CNT_PS2	r/w	2	03F0H	Direct
D0h	MFR_VR_CONFIG	r/w	2	EC00h	Direct
D1h	MFR_TEMPERATURE	r/w	2	500Ah	Direct
D2h	MFR_FS_SET	r/w	1	B2h	Direct
D3h	MFR_CUR_GAIN	r/w	2	0159h	Direct
D4h	MFR_OCP_SET	r/w	2	4525h	Direct
D5h	MFR_OVP_UVP_SET	r/w	2	4A54h	Direct
D6h	MFR_OCP_TRG	r/w	1	2Ah	Direct
D8h	MFR_ADDR_PMBUS	r/w	1	8Fh	Direct
D9h	MFR_ADDR_SVID	r/w	1	10h	Direct
DBh	MFR_OTP_SET	r/w	2	961Eh	Direct
DCh	MFR_PSI_TRIM	r/w	2	0D8Bh	Direct
DDh	MFR_CUR_OFFSET	r/w	1	3Ah	Direct
E8h	MFR_BLANK_TIME	r/w	1	18h	Direct
EAh	MFR_VBOOT	r/w	2	017Eh	Direct
EBh	MFR_ICC_MAX	r/w	1	FFh	Direct
ECh	MFR_TEMP_MAX	r/w	1	7Dh	Direct
EDh	MFR_SR	r/w	2	1405h	Direct
EEh	MFR_VR_TOLERANCE	r/w	1	28h	Direct
EFh	VENDOR_ID_VR	r/w	1	00h	Direct
F0h	PRODUCT_ID_VR	r/w	1	00h	Direct

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PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Default Value	Data Formats
F1h	PRODUCT_REV_VR	r/w	1	00h	Direct
F2h	MFR_CONFIGRATION_ID_LSB	r/w	1	00h	Direct
F3h	MFR_CONFIGRATION_ID_MSB	r/w	1	00h	Direct
F4h	PROTOCOL_ID_VR	r/w	1	00h	Direct
F5h	CAPABILITY_VR	r/w	1	7Fh	Direct
F7h	MFR_PLUS_STEP	r/w	1	22h	VID
FAh	MFR_SLOPE_SLEWRATE_PS0	r/w	2	00ECh	Direct
FBh	MFR_SLOPE_CNT_PS0	r/w	1	34h	Direct
FCh	MFR_SLOPE_CNT_PS1	r/w	2	020Eh	Direct
FDh	MFR_SLOPE_SLEWRATE_PS1	r/w	2	01C9h	Direct
FEh	MFR_PROTECT_DIS	r/w	2	3100h	Direct

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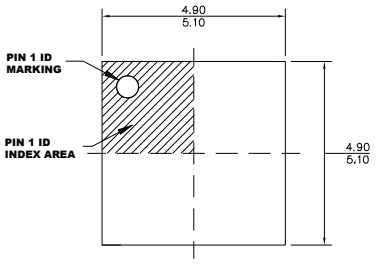
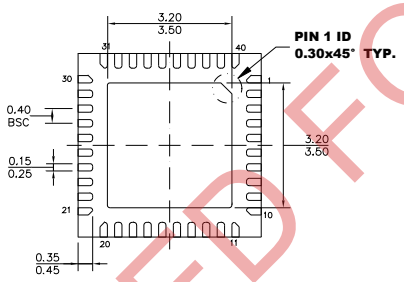
PACKAGE INFORMATION

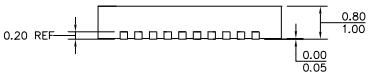
QFN-40 (5mmx5mm)



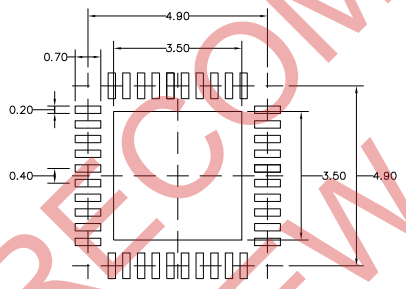
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHE-1
5) DRAWING IS NOT TO SCALE.

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