UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION

Petitioner

v.

GREENTHREAD, LLC

(record) Patent Owner

IPR2023-00324
Patent No. 11,121,222

PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.200 ET. SEQ

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Exhibit No.	Description
1001	U.S. Patent No. 11,121,222 ("**the '222 patent**").
1002	Declaration of R. Michael Guidash.
1003	C.V. of R. Michael Guidash.
1004	U.S. Pat. No. 6,614,560 ("**Silverbrook**").
1005	U.S. Pat. No. 6,420,763 ("**Yamashita**").
1006	File History of U.S. App. Ser. No. 11/622,496 (issued as U.S. Pat. No. 8,421,195).
1007	File History of U.S. App. Ser. No. 16/947,294 (issued as the '222 patent).
1008	U.S. Pat. No. 4,481,522 ("**Jastrzebski**").
1009	Redline comparisons of claim 1 and claims 21, 39, 41, 42, and 43 with other independent claims.
1010	U.S. Pat. Pub. 2004/0063288 A1 ("**Kenney**").
1011	U.S. Pat. Pub. 2001/0032983 A1 ("**Miyagawa**").
1012	Excerpt from Nishi, et al. (eds.) *Handbook of Semiconductor Manufacturing*, Marcel Dekker, Inc., New York (2000) ("**Nishi**").
1013	Defendants' Opening Claim Construction Brief in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. Oct. 10, 2022).
1014	Plaintiffs' Claim Construction Brief in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. Oct. 31, 2022).

1015	Complaint in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. January 27, 2022).
1016	Amended Complaint in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. April 29, 2022).
1017	Exhibit 12 from Amended Complaint in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. April 29, 2022).
1018	U.S. Pat. App. Pub. 2003/0136982A1 ("**Rhodes**").
1019	Scheduling Order in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. May 23, 2022).
1020	United States District Courts — National Judicial Caseload Profile, March 31, 2022, available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1
1021	Scheduling Order in *Topia Tech., Inc. v. Box, Inc., et al.*, Case No. 6:21-cv-01372-ADA (W.D. Tex. May 20, 2022).
1022	Scheduling Order in *Parus Holdings, Inc., v. Apple Inc., et al.*, Case No. 6:21-cv-00968-ADA (W.D. Tex. August 22, 2022).
1023	Scheduling Order in *Lone Star SCM Systems, Ltd. V. Zebra Tech. Corp.*, Case No. 6:21-cv-00842-ADA (W.D. Tex. August 3, 2022).
1024	U.S. Pat. No. 6,483,176 ("**Noguchi**").
1025	U.S. Pat. App. Pub. 2003/0063272A1 ("**Zaidi**").
1026	U.S. Pat. App. Pub. 2003/0081463A1 ("**Bocian**").
1027	U.S. Pat. App. Pub. 2003/0098419A1 ("**Ji**").
1028	Screen capture of https://www.bestbuy.com/site/sony-alpha-a7-iii-mirrorless-4k-video-camera-body-only-black/6213101.p?skuId=6213101

1029	Excerpt from Pierret, *Semiconductor Fundamentals, Vol. I*, Addison-Wesley Publishing Company, Reading, MA, 1983.
1030	Excerpt from Grove, *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, 1967.
1031	Excerpt from Sze, *VLSI Technology*, McGraw-Hill Book Company, 1983.
1032	Excerpt from Wolf and Tauber, *Silicon Processing for the VLSI ERA,* Lattice Press, Sunset Beach, CA, (2000).

Petitioner respectfully requests *inter partes* review under 35 U.S.C. §311 of claims 1-44 of U.S. Pat. No. 11,121,222 ("the '222 patent").

NOTICE OF LEAD AND BACKUP COUNSEL

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NOTICE OF RELATED MATTERS

The '222 patent has been asserted in *Greenthread, LLC v. Intel Corporation et al,* Case No. 6-22-cv-00105 (W.D. Tex.), filed January 27, 2022.

NOTICE OF THE REAL-PARTIES-IN-INTEREST

The real-parties-in-interest ("RPIs") are Sony Group Corporation, Sony Corporation, Sony Semiconductor Solutions Corporation, Sony Semiconductor Manufacturing Corporation, Sony Taiwan Ltd., Sony Corporation of America, Sony Electronics Inc., Dell Inc., and Dell Technologies Inc.

NOTICE OF SERVICE INFORMATION

Please address all correspondence to the lead counsel at the addresses shown above. Petitioner consents to electronic service by email at: smith@smithbaluch.com, baluch@smithbaluch.com.

GROUNDS FOR STANDING

Petitioner hereby certifies that the patent for which review is sought is available for *inter partes* review, and that the Petitioner is not barred or estopped from requesting a *inter partes* review on the grounds identified in the petition.

STATEMENT OF PRECISE RELIEF REQUESTED

Petitioner respectfully requests that claims 1-44 of the ’222 patent be canceled based on the following grounds:

Ground 1: Claims 1-38 were obvious over Silverbrook in view of Yamashita.

Ground 2: Claims 39-43 were obvious over Yamashita.

Ground 3: Claims 1-43 were obvious over Silverbrook, Yamashita, and Nishi.

Ground 4: Claim 44 was obvious over Kenney.

THRESHOLD REQUIREMENT FOR *INTER PARTES* REVIEW

As shown in the Grounds set forth below, the information presented in the instant petition, if unrebutted, demonstrates that “it is more likely than not that at least 1 of the claims challenged in the petition is unpatentable.” 35 U.S.C. § 314(a).

I. INTRODUCTION

A. Technical Background

The ’222 patent relates to semiconductor devices having graded dopant concentrations. Petitioner’s expert, Mr. Guidash, provides an introduction to the technology concepts relevant to the ’222 patent. (Ex. 1002, ¶¶24-68).

II. CLAIM CONSTRUCTION

"In an inter partes review proceeding, a claim of a patent…shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. §42.100(b).

Greenthread LLC and defendants related to Dell and Intel have taken claim construction positions in the co-pending litigation, as reflected in Exhibits 1013 and 1014.

A. Claims 1-38 — "VLSI"

The preambles of claims 1-38 use the term "VLSI". As Mr. Guidash explains, VLSI stands for "Very Large Scale Integration", and was typically understood to describe an integrated circuit with one million active elements, such as transistors. (Ex. 1002, ¶¶71-72). Greenthread's prosecution statements in a related application support this definition. (Ex. 1006, p. 291).

III. DETAILED EXPLANATION OF THE REASONS FOR UNPATENTABILITY

Ground 1. Claims 1-38 were obvious over Silverbrook in view of Yamashita

Claims 1-38 were obvious under 35 U.S.C. §103(a) over U.S. Pat. No.

6,614,560 ("**Silverbrook**")(Ex. 1004) in view of U.S. Pat. No. 6,420,763 ("**Yamashita**")(Ex. 1005).

Neither reference was of record during prosecution of the application leading to the '222 patent.

A. Effective Prior Art Date of Silverbrook and Yamashita

Silverbrook is a U.S. patent that issued on September 2, 2003, from an application filed July 10, 1998, and is thus prior art under pre-AIA 35 U.S.C. §§102(a) and (e).

Yamashita is a U.S. patent that issued on July 16, 2002, and is thus prior art under pre-AIA 35 U.S.C. §102(b).

B. Overview of the Combination

Yamashita teaches semiconductor devices for, *e.g.*, DRAM in integrated circuits. (Ex. 1005, 1:7-15). Yamashita alone teaches almost all claim elements. (Ex. 1002, ¶74). This ground is nonetheless presented as one of obviousness for several reasons. First, Yamashita does not specifically state that its semiconductor devices are part of VLSI devices (as recited by the preambles of independent claims 1 and 21), nor that its semiconductor devices are used in certain applications—such as "central processing units"—specified in dependent claims. (Ex. 1002, ¶74). Silverbrook teaches a VLSI integrated circuit (called an "Image Capture and Processing Chip" or "ICP") having DRAM, a CPU, and an image sensor, in which

it is appropriate to use Yamashita's devices. (Ex. 1004, 6:42-55, Fig. 15)(Ex. 1002, ¶74). This Ground posits that it would have been obvious to use Yamashita in a VLSI DRAM chip for two reasons: (1) it would have been obvious from Yamashita alone to use Yamashita's techniques specifically in a VLSI chip and (2) it would have been obvious to use Yamashita's techniques in Silverbrook's ICP.

Second, Yamashita describes retrograde n-wells and retrograde p-wells. "Retrograde" wells are wells that have a dopant level peak below the surface. (Ex. 1005, Fig. 55, 21:35-41)(Ex. 1002, ¶74). While Yamashita expressly shows a dopant profile concentration having a graded dopant profile in a retrograde p-well, it does not illustrate the corresponding graded dopant concentration profile in a retrograde n-well, which would have been obvious.

Third, Yamashita teaches that graded dopant profiles create potential gradients that aid carrier movement, and the ability to aid carrier movement in the specific Eighth Embodiment, on which the Ground relies, would have been obvious. (Ex. 1002, ¶74).

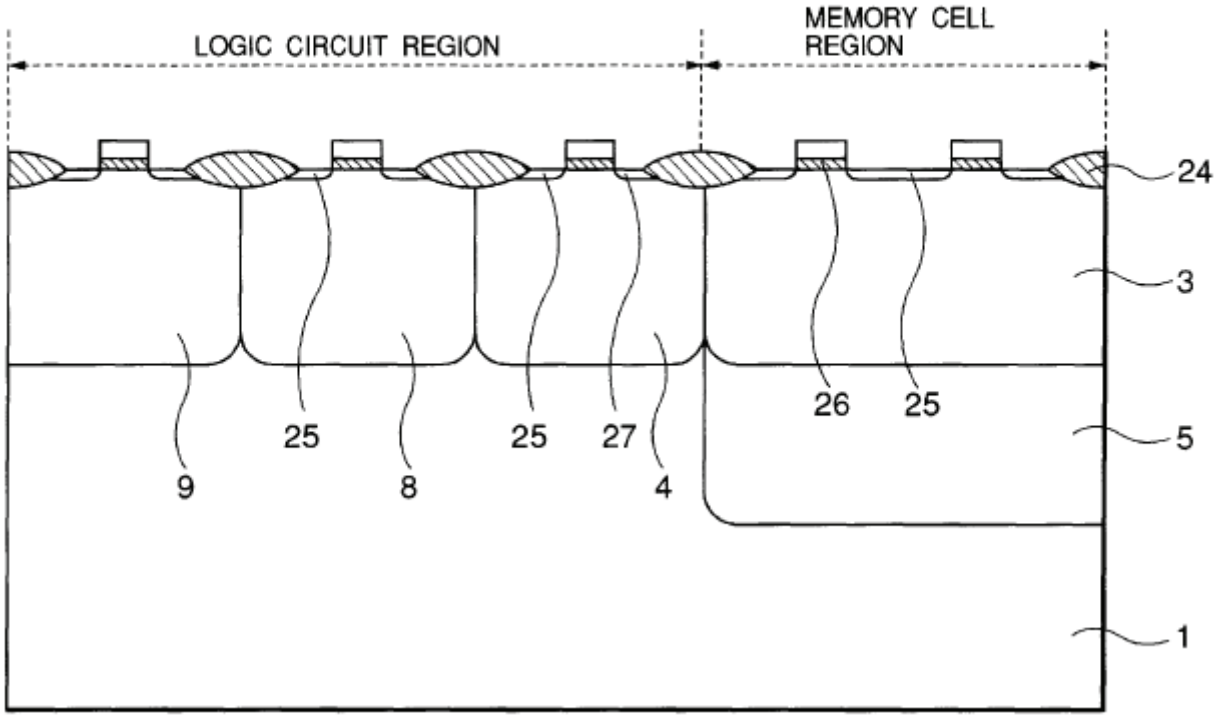
Finally, this Ground also posits obviousness for certain dependent claims, as explained in detail in the claim mapping section where appropriate. The Rationale underpinning other obviousness grounds will be presented in the Claim Mapping section, under each claim element as appropriate.

C. Rationale (Motivation) Supporting Obviousness

It would have been obvious to use Yamashita's devices in a VLSI integrated DRAM circuit and in a VLSI circuit like Silverbrook's ICP. (Ex. 1002, ¶75).

Yamashita teaches semiconductor structures useful for memory (and in particular, DRAM) having both a logic circuit region and a memory cell region, as shown with respect to the Eighth Embodiment in Fig. 53, reproduced here:

FIG.53



(Ex. 1005, Fig. 53, 6:1-2, 21:19-34)(Ex. 1002, ¶76). Yamashita states:

> "The semiconductor device is divided roughly into an element region (a memory cell region) for storing information of large-capacity mainly and an element region (a logic circuit region) for executing

> logical calculations while exchanging information of large-capacity with the memory cell region."

(Ex. 1005, 21:27-33)(Ex. 1002, ¶76).

It would have been obvious from Yamashita alone that it was intended to be used in a VLSI integrated circuit, because in the relevant timeframe, memory chips with built-in logic typically had millions of transistors and memory cells, to process and store large amounts of information. (Ex. 1005, 2:62-67, 21:27-33, 31:27-32)(Ex. 1002, ¶77).

As an example of this, Silverbrook teaches an Image Capture and Processing Chip (ICP) that employs DRAM and logic circuitry. (Ex. 1004, 6:42-10:23)(Ex. 1002, ¶78). The layout of the ICP is shown in Silverbrook's Fig. 15, reproduced here:

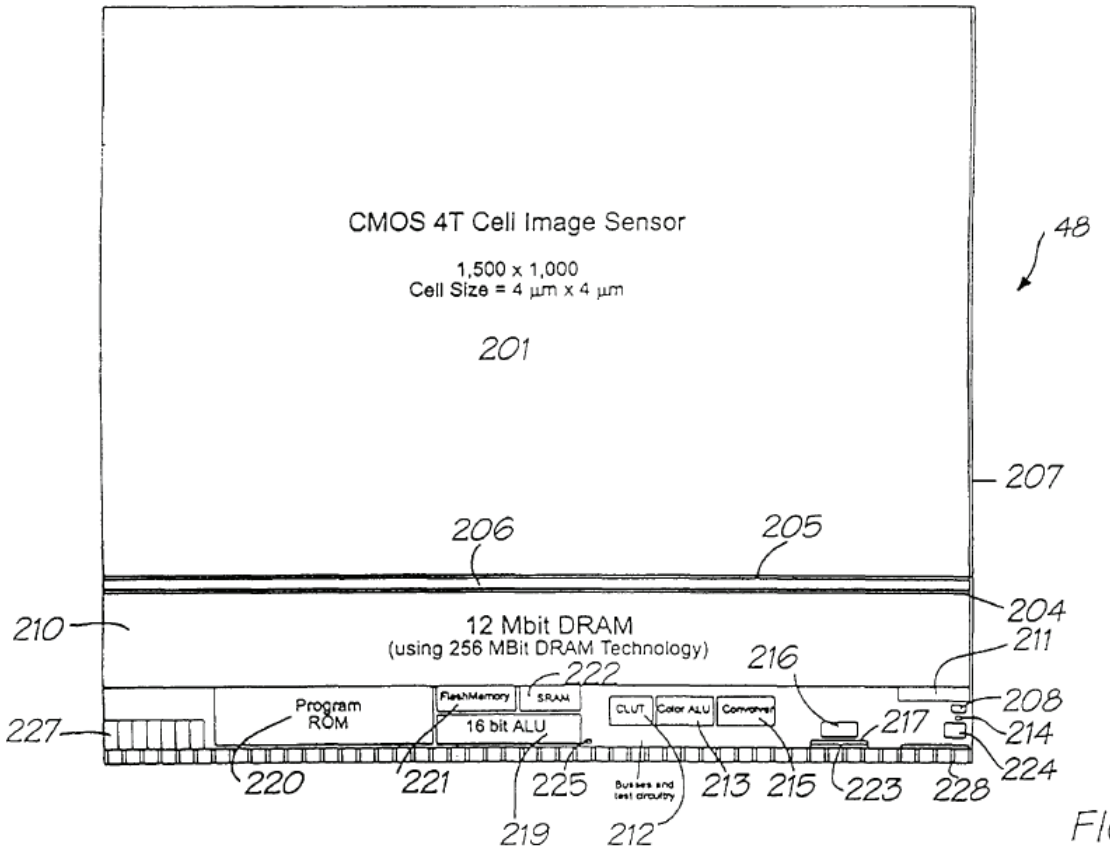


FIG. 15

(Ex. 1004, Fig. 15, 6:42-10:23)(Ex. 1002, ¶78). As seen at the bottom of Fig. 15, the ICP has DRAM and a logic circuit region for executing logical calculations (*e.g.*, the 16 bit ALU 219, the Color ALU 213, and the Convolver 215). (Ex. 1004, 6:46-48, 7:1-27, 10:9-50)(Ex. 1002, ¶78).

Silverbrook does not teach the low-level semiconductor structure of devices that form the DRAM and logic devices, but does state that they "can be vendor-supplied cores" (Ex. 1004, 7:28-30) (Ex. 1002, ¶79). A POSITA would have understood Silverbrook to be teaching that the exact semiconductor techniques used for the DRAM and logic circuit can be obtained from other prior art. (Ex. 1002,

¶79).

A POSITA further would have found it obvious to use the techniques of Yamashita in Silverbrook. (Ex. 1002, ¶80). Yamashita teaches that its techniques can be used to achieve the advantages of:

> "provid[ing] a semiconductor device having a substrate impurity structure that has both soft error resistance and latch up resistance and that prevents faulty circuit operation when the semiconductor device is formed with a fine structure."

(Ex. 1005, 3:15-18; *see also* 23:17-25)(Ex. 1002, ¶80). A POSITA thus would have found the combination obvious based on the advantages of Yamashita.

A POSITA further would have found the combination obvious because Silverbrook represents a known type of integrated circuit that required circuitry for DRAM and logic circuits, and would have been ready for improvement using the known techniques in a predictable manner. (Ex. 1002, ¶81). *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416-21 (2007).

Other aspects of the Rationale supporting obviousness will be explained below in the Claim Mapping section, under the claim limitation to which the obviousness argument pertains.

D. *Graham* Factors

The **level of ordinary skill** encompassed a person having a Bachelor's Degree in electrical engineering, microelectronics engineering or a related field and three

years of experience relating to semiconductor device manufacturing, where a higher level of education may substitute for experience and vice versa. (Ex. 1002, ¶83).

The **scope and content of the prior art** are discussed throughout the Ground.

The **differences between the prior art and the claims** are discussed in the section entitled "Rationale (Motivation) Supporting Obviousness", above, and in the claim mapping, below.

Petitioner is not aware of any **secondary considerations** that would make an inference of non-obviousness more likely.

E. Reasonable Expectation of Success

A person of ordinary skill in the art ("POSITA") in the relevant timeframe would have had a reasonable expectation of success in using the prior art in the manner discussed in this petition. (Ex. 1002, ¶87). As Mr. Guidash explains, the art was relatively predictable in the relevant timeframe (September 2004). (Ex. 1002, ¶87). A POSITA would have been able to make any necessary modifications to implement the Ground, and in particular would have been able to use Yamashita's techniques in a VLSI device and in Silverbrook, and to adjust doping gradients, electric fields created by dopant gradients and carrier movement to effect the purposes of Yamashita. (Ex. 1002, ¶87).

F. Analogous Art

Silverbrook and Yamashita are analogous art because they are directed to the

same field as the ’222 patent (semiconductor devices). (Ex. 1001, Title, Abstract, 1:23-30)(Ex. 1004, Title, 1:9-11, 2:10-16)(Ex. 1005, Title, Abstract). Furthermore, the teachings of Silverbrook and Yamashita would have been reasonably pertinent to the problems facing the named inventors, including the production of integrated circuits including CMOS image sensors and memory. (Ex. 1001, 3:36-55)(Ex. 1004, Title, Fig. 15, 6:41-8:17, 11:14-30)(Ex. 1005, 1:12-3:22)(Ex. 1002, ¶88). *See Wyers v. Master Lock Co.*, 616 F.3d 1231, 1238 (Fed. Cir. 2010)(“The Supreme Court’s decision in *KSR* [cite omitted], directs us to construe the scope of analogous art broadly….”).

G. Claim Mapping

This section maps the challenged claims to the relevant disclosures of Silverbrook and Yamashita, where the claim text appears in bold-italics, and the relevant mapping follows the claim text. The Petitioner has added numbering and lettering in brackets (*e.g.*, 1[a], [1b]) to certain claim elements, to facilitate the discussion.

CLAIM 1

“1[a]. A VLSI semiconductor device, comprising:”

Yamashita alone and the combination with Silverbrook renders obvious a **VLSI semiconductor device**. Silverbrook teaches an Image Capture and Processing Chip or “ICP”. (Ex. 1004, 6:41-60)(Ex. 1002, ¶90). Silverbrook states

that the ICP is

> "a highly integrated system. It combines CMOS image sensing, analog to digital conversion, digital image processing, DRAM storage, ROM, and miscellaneous control functions in a single chip."

(Ex. 1004, 6:46-49)(Ex. 1002, ¶90).

The ICP is a **VLSI semiconductor device** because it is a semiconductor chip that incorporates millions of transistors. (Ex. 1002, ¶91). For example, the ICP includes an "imaging array [that] is a CMOS 4 transistor active pixel design with a resolution of 1,500 x 1,000." (Ex. 1004, 7:35-37)(Ex. 1002, ¶91). As Mr. Guidash explains, this means that the ICP has six million transistors in its CMOS image sensor array alone. (Ex. 1002, ¶91). Furthermore, the ICP includes 12 megabits of DRAM, which would include one transistor per bit, or approximately 12.5 million transistors. (Ex. 1004, 7:12, 8:63-67)(Ex. 1002, ¶91).

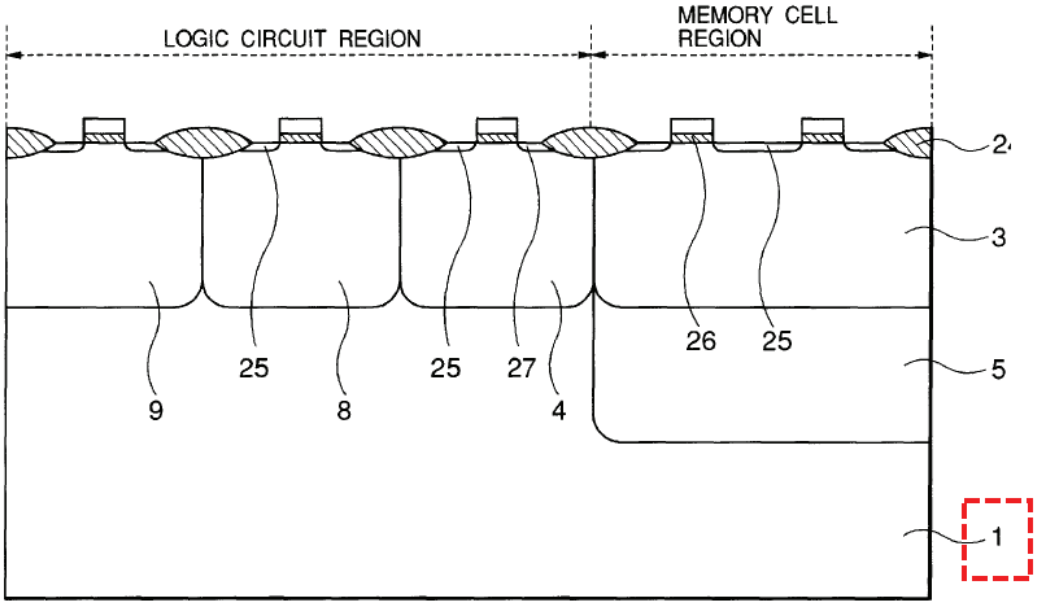
Furthermore, it would have been obvious to a POSITA in the relevant timeframe that Yamashita was intended to be used with VLSI DRAM memory devices, which typically had millions of elements, together with logic circuits capable of "high-capacity" information exchange with the DRAM. (Ex. 1005, 21:27-32)(Ex. 1002, ¶92).

"[1b] a substrate of a first doping type at a first doping level having a surface;"

Yamashita teaches, and the combination renders obvious, **a substrate of a first doping type at a first doping level having a surface**. (Ex. 1002, ¶93).

Yamashita teaches a semiconductor device having a **substrate** 1, as shown below in the reproduction of Fig. 53 of Yamashita, with an added, red-dashed box to show the reference numeral 1 of the substrate:

FIG.53



(Ex. 1005, Fig. 53, 6:1-2, 21:20-24, 22:19-24, 7:19-21)(Ex. 1002, ¶94).

The substrate 1 is "p type semiconductor substrate 1 containing boron of a concentration on the order of $1 \times 10^{16} / cm^3$". (Ex. 1005, 6:1-2, 21:20-24, 22:19-24, 7:19-21)(Ex. 1002, ¶95). Thus, the substrate is **of a first doping type** (p-type) **at a first doping level** ($1 \times 10^{16} / cm^3$). (Ex. 1005, 8;13-14)(Ex. 1002, ¶95). The substrate has a top **surface** (the top surface of the device shown in Fig. 53), as indicated in the

figure. (Ex. 1002, ¶95).

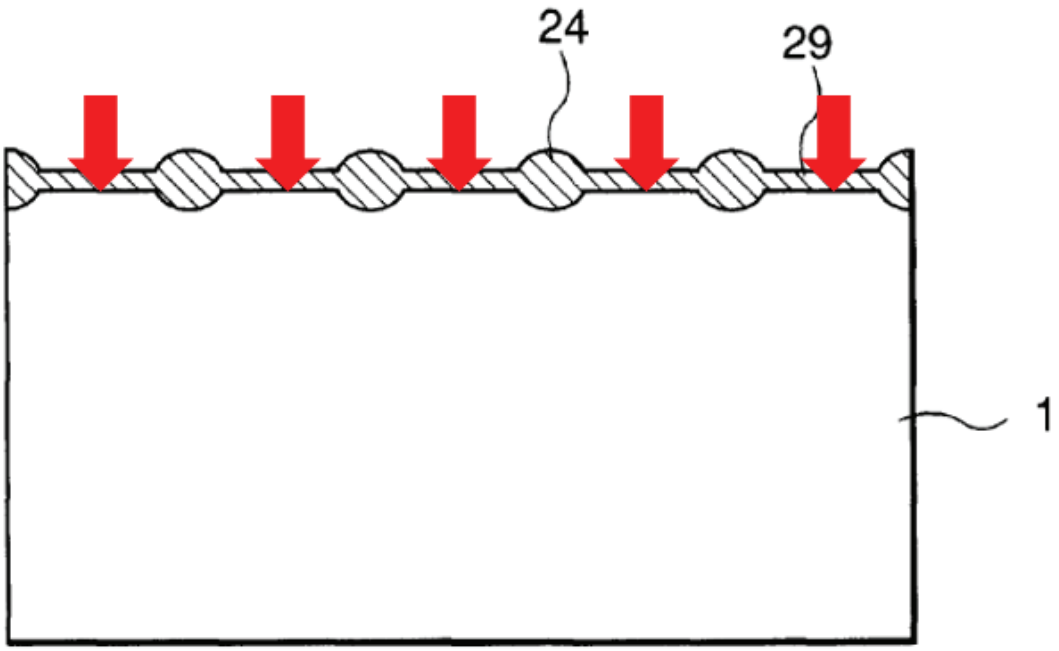
"[1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

Yamashita teaches **a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type** within **which transistors can be formed**. First, Yamashita teaches a series of active regions separated by separation regions:

> "As shown in FIG. 57, **the field oxide film 24 is formed on the separation region** on the main surface of the p type semiconductor substrate 1 containing boron of concentration on the order of 1×10^{16} / cm^3, and **the oxide film 29 for the gate oxide film 26 is formed on the active region**."

(Ex. 1005, 22:33-37)(Emphasis added)(Ex. 1002, ¶96). Figure 57 of Yamashita (referenced in the quote above) is reproduced below, with the location of the eventual active regions indicated with added red arrows:

FIG.57



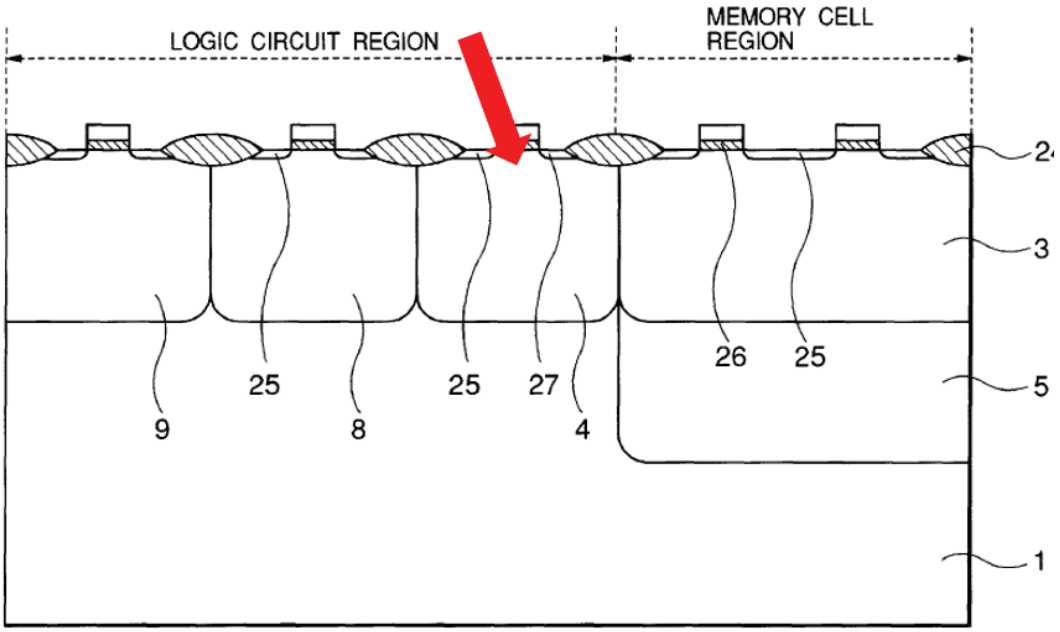
(Ex. 1005, 6:9-10, 22:29-39)(Ex. 1002, ¶96). The active regions at this stage in manufacturing are covered by a thin gate oxide, and separated by thick portions of field oxide 24. (Ex. 1005, 22:33-37)(Ex. 1002, ¶96). The field oxide has the function of isolating active regions from one another. (Ex. 1005, 22:33-37)(Ex. 1002, ¶96). The "gate oxide", after later steps, will become the oxide that separates gate electrodes from transistor channels in MOSFET transistors. (Ex. 1002, ¶96).

The active regions are disposed **adjacent to** the top **surface of the substrate** 1. (Ex. 1005, Fig. 57, 22:33-37)(Ex. 1002, ¶97).

Yamashita teaches that certain active regions will have n-type doping, which is **a second doping type opposite in conductivity to the first doping type** (which

is p-type, as discussed above under claim limitation [1b]). (Ex. 1005, 23:4-16, 21:55-58, 21:66-22:1, 21:20-24, 22:7-9)(Ex. 1002, ¶98). The **first active region** with an n-type doping is indicated by the added red arrow in the reproduction of Fig. 53, reproduced below:

FIG.53



(Ex. 1005, 21:20-24)(Ex. 1002, ¶98).

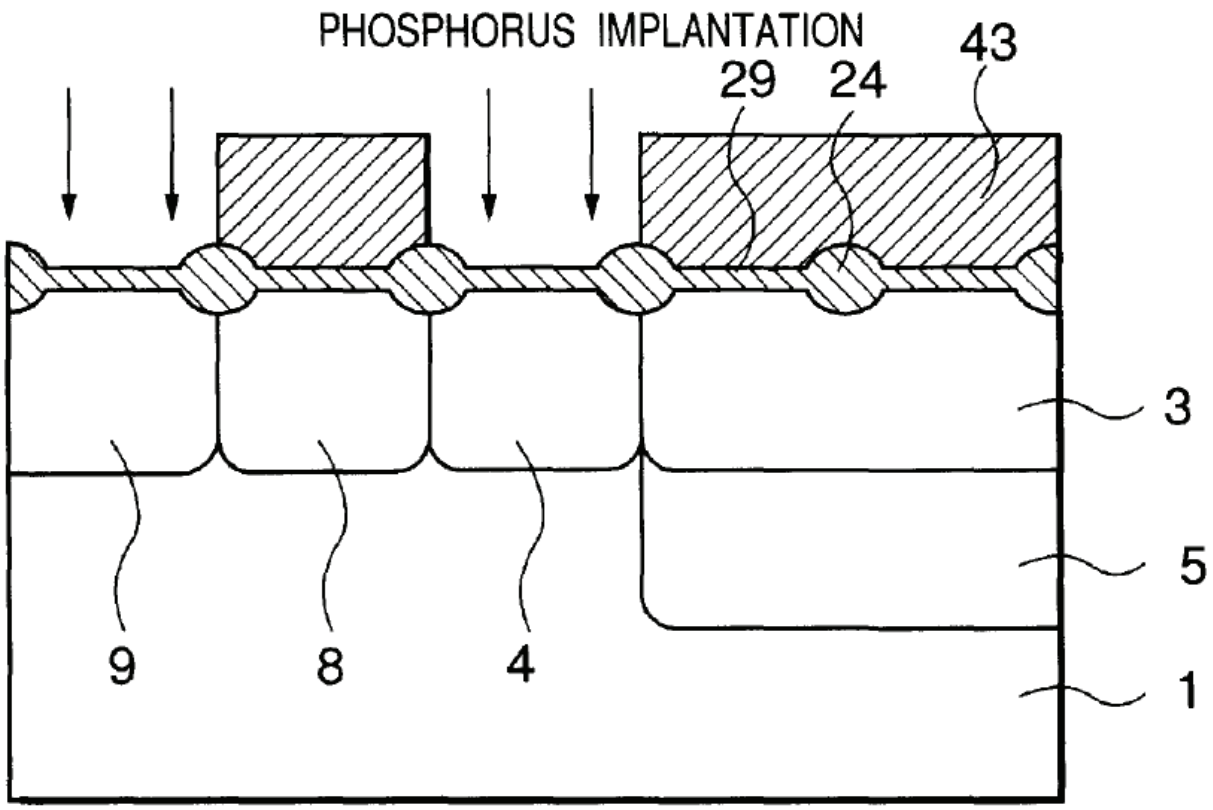
The **first active region** is formed by ion implantation of phosphorous, producing a "retrograde n well 4" extending from the surface of the semiconductor to some depth. Yamashita explains:

> "As shown in FIG. 63, a resist 43 is formed. The resist 43 has an opening portion on a formation region for the PMOSFET in the logic circuit region. **Phosphorus, which is a source of n type impurity**

> ions, **is implanted** through the opening portion in the formation region by conditions of 300 keV - 2.5 MeV, $1 \times 10^{12} - 1 \times 10^{14} / cm^2$, and the **retrograde n wells 4**, 9 **are formed**."

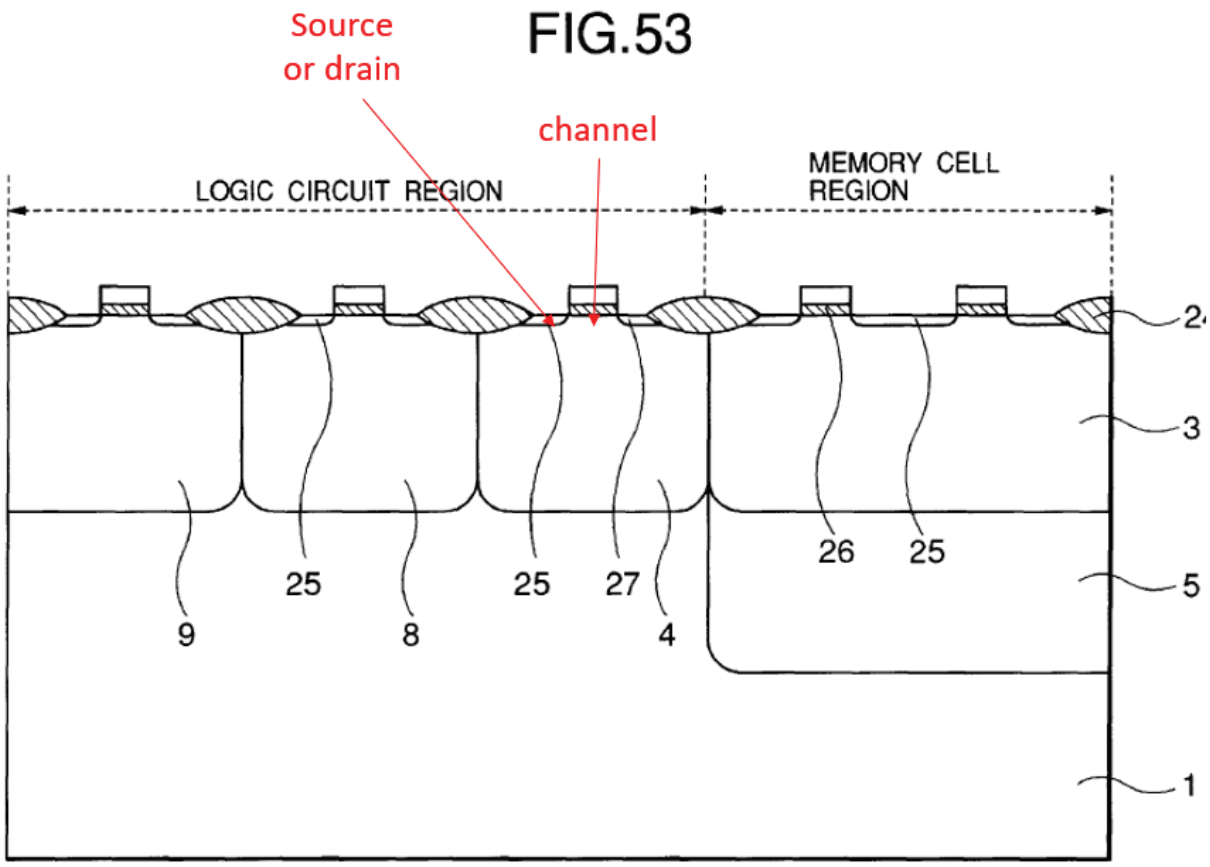
(Ex. 1005, 23:4-10)(Emphasis added)(Ex. 1002, ¶99). Figure 63, discussed in the quote above, is reproduced here:

FIG.63



(Ex. 1005, Fig. 63)(Ex. 1002, ¶99). Petitioner notes that in the semiconductor arts, a substrate typically *contains* active regions, which can in turn *contain* or *be contained in* wells. (Ex. 1002, ¶99).

The first active region is a region **within which transistors can be formed.** Fig. 53, reproduced below with added labels and arrows, depicts the source, drain and channel of a transistor, which meets the claim language under the Patent Owner's interpretation (Ex. 1014, p. 33):



(Ex. 1005, Fig. 53, 6:1-2, 21:55-58)(Ex. 1002, ¶100). Furthermore, Yamashita teaches that additional transistors can be formed in this same region:

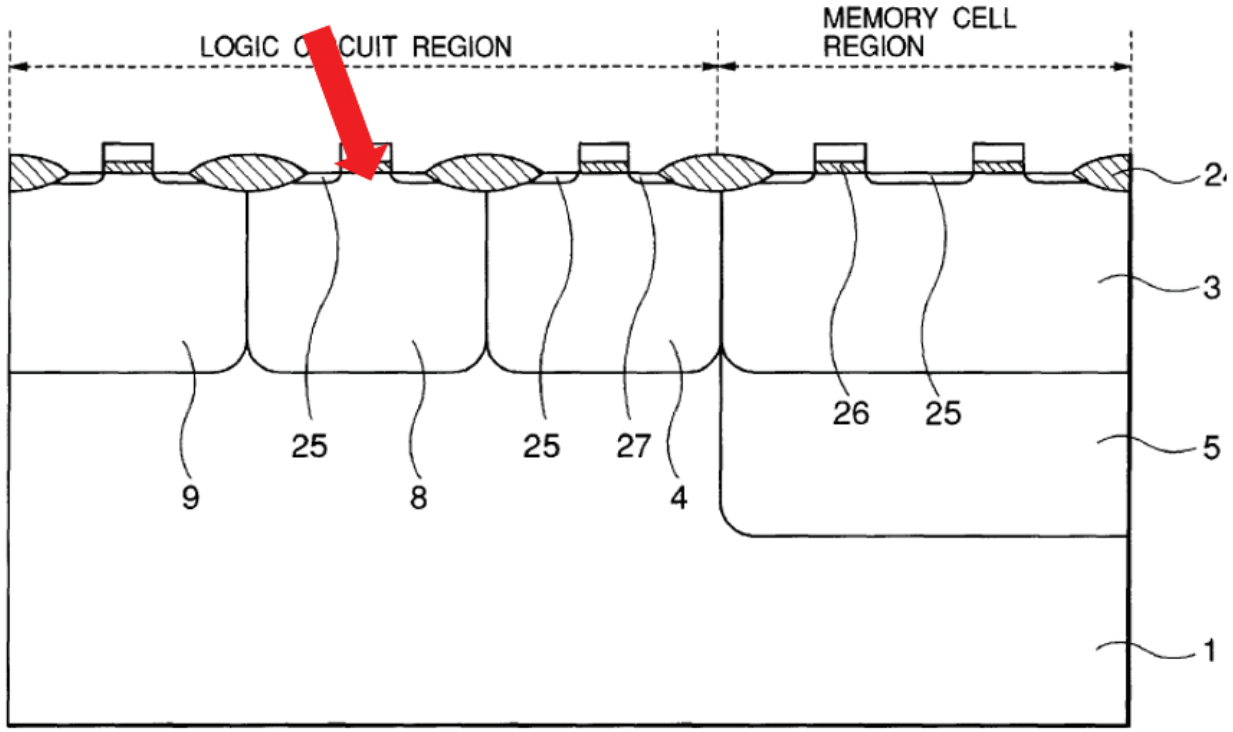
> "**A plurality of transistors** or a single transistor **is formed on the** retrograde p well 8, **the retrograde n well 4** and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region."

(Ex. 1005, 21:55-58)(Emphasis added)(Ex. 1002, ¶100).

> ***"[1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"***

Yamashita teaches **a second active region separate from the first active region disposed adjacent to the first active region** within which transistors can be formed**.** (Ex. 1002, ¶101). The second active region is shown in Fig. 53, reproduced below, with an added red arrow showing the **second active region**:

FIG.53



(Ex. 1005, Fig. 53)(Ex. 1002, ¶101). The second active region has a retrograde p well 8. (Ex. 1005, 21:20-23, 21:55-58, 22:64-23:3, 23:13-14)(Ex. 1002, ¶101).

Petitioners note that in the semiconductor arts, a substrate typically contains active regions, which can in turn contain or be contained in wells. (Ex. 1002, ¶99).

The second active region is **separate[d] from the first active region** by a "separation region", which is comprised of an isolating field oxide layer 24, as explained above under element [1c]. (Ex. 1005, 22:33-37)(Ex. 1002, ¶102). Petitioner notes that the '222 patent also separates active regions by isolation regions. (*e.g.*, Ex. 1001, claim 6)(Ex. 1002, ¶102).

The second active region is also **adjacent to the first active region**, as shown in Fig. 53, above. (Ex. 1002, ¶103). This adjacent nature of the active regions was also obvious from the disclosure of CMOS logic, as Mr. Guidash explains. (Ex. 1002, ¶103).

Finally, Fig. 53 depicts a transistor formed in the second active region, and Yamashita teaches that additional **transistors can be formed in the second active region**:

> "**A plurality of transistors** or a single transistor **is formed on the retrograde p well 8**, **the retrograde n well 4** and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region."

(Ex. 1005, 21:55-58)(Emphasis added)(Ex. 1002, ¶104).

"[1e] transistors formed in at least one of the first active region or second active region;"

As explained above under elements [1c] and [1d], Yamashita teaches that transistors are formed in both the first and second active regions. (Ex. 1005, Fig. 53, 21:55-58)(Ex. 1002, ¶105).

"[1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

Yamashita teaches that both **the first and second active regions** each have **at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions.** Specifically, the first active region contains a retrograde n well 4, and the second active region contains a retrograde p well 8. (Ex. 1005, 21:19-25, 22:7-9)(Ex. 1002, ¶106). As Mr. Guidash explains, a "retrograde well" is an area of a semiconductor device that has a dopant concentration peak below the surface of the device, and thus a graded dopant profile that creates the claimed carrier movement. (Ex. 1002, ¶106)(Ex. 1018, ¶0045). The '222 patent admits that:

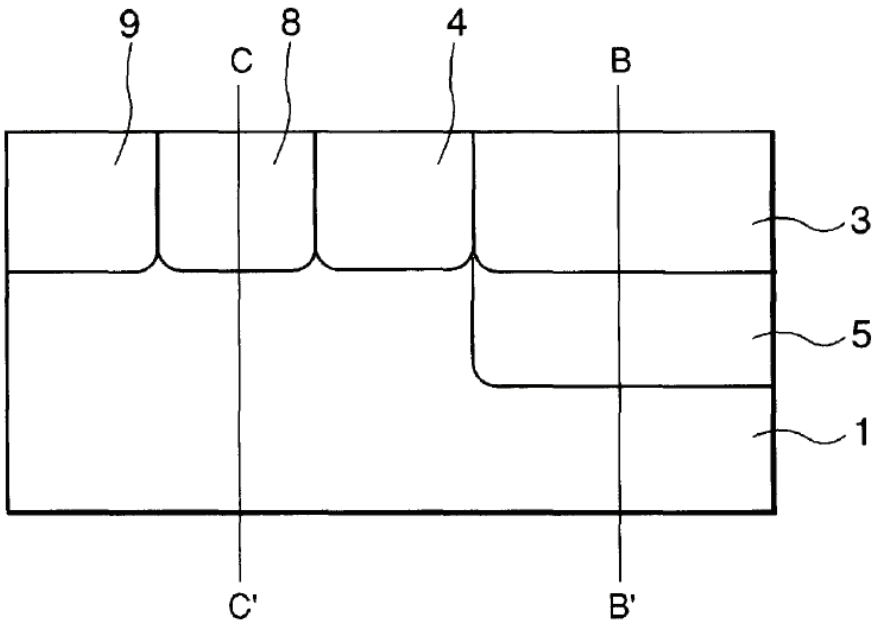
> "As desired, the n-well and p-wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well."

(Ex. 1001, 3:62-64).

With respect to the **second active region** (which has a retrograde p well 8), Yamashita discloses a cross-section in Fig. 54. The cross-section in Fig. 54 is

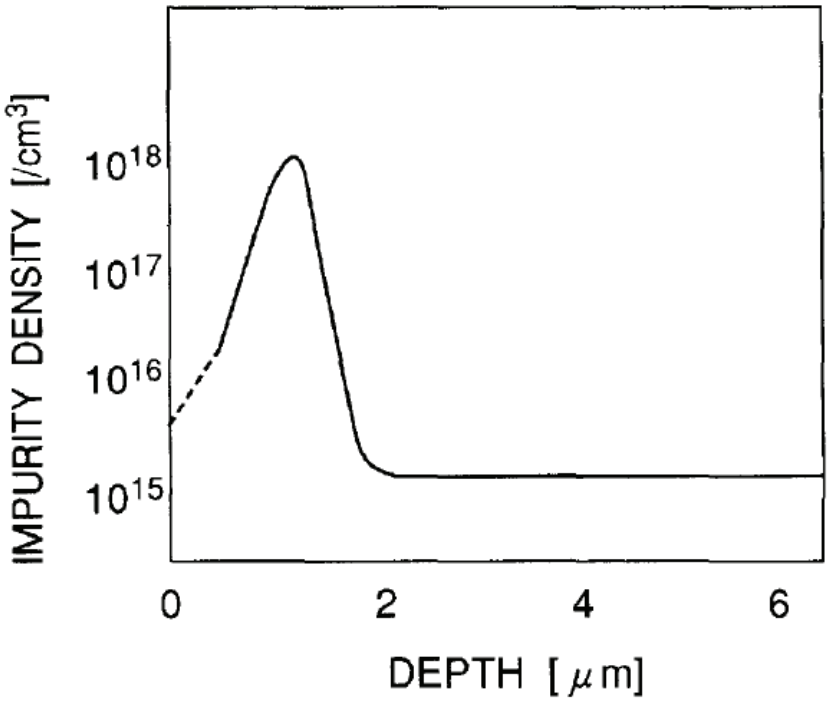
reproduced here:

FIG.54



(Ex. 1005, Fig. 54, 6:3-4, 21:19-26)(Ex. 1002, ¶107). In Fig. 54, Yamashita shows, running through the second active region, a vertical axis C-C' toward the left-hand side. Along that axis, there is the dopant ("impurity") concentration profile shown in Fig. 55, reproduced here:

FIG.55



(Ex. 1005, Fig. 55, 21:35-36, 6:5-6)(Ex. 1002, ¶107). The horizontal axis of Fig. 55 represents the depth from the top surface of the device, where the top surface is at depth zero on the left-hand side. (Ex. 1002, ¶107). The vertical axis represents the dopant concentration (called the "impurity density" here). (Ex. 1002, ¶107). As is visible from the figure, the **dopant concentration is graded**, because it increases from the surface, reaches a peak, and because it then decreases from the peak to a flatter portion at around a depth of two microns. (Ex. 1002, ¶107).

With respect to the first active region, although Yamashita does not provide a

graph similar to the one shown in Fig. 55, Yamashita does disclose that the well 4 is a "retrograde n well". (Ex. 1005, 21:19-25, 21:55-22:1, 22:7-9, 23:4-17)(Ex. 1002, ¶108). This indicates that the n well 4 has a dopant concentration profile with a peak below the surface, similar to the one shown in Fig. 55. (Ex. 1002, ¶108). Furthermore, the ion implantation step described by Yamashita (Ex. 1005, 23:4-12, Fig. 63) would have produced a phosphorus (dopant) profile in the retrograde n well 4 similar to the dopant profile shown in Fig. 55 for boron. (Ex. 1002, ¶108). Thus, it would have been obvious based on the description of well 4 as a "retrograde n well", the corresponding description of the dopant profile of the similarly-labeled retrograde p well 8, and the conditions under which the retrograde n well was created, that the first active region also had a dopant profile with a peak below the surface of the device, and thus a **graded dopant concentration**. (Ex. 1002, ¶108).

Under the Patent Owner's claim construction apparent from both its claim construction briefing and its infringement contentions,[1] the graded dopant profiles

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[1] (Ex. 1014, pp. 26)(patent owner's claim construction briefing, interpreting all claim terms in all asserted patents containing the language "to aid the movement" [of carriers], and stating "[t]he claim even says where the movement occurs: it is in the drift layer, and the carriers move **downward**")(Emphasis added); (Ex. 1017,

would obviously have the effect of **aiding carrier movement from the first and second active regions towards an area of the substrate where there are no active regions**, because graded dopant profiles move carriers downward in the device. (Ex. 1002, ¶109). As explained by Mr. Guidash, a dopant concentration that is graded at some portion along the axis from the top to the bottom of the device will produce an electric field that aids carriers with one type of charge toward the bottom of the device, and carriers with the opposite charge toward the top of the device. (Ex. 1002, ¶109). The carriers that move toward the bottom of the device (an **area of the substrate where there are no active regions**) are carriers that are **aided from the first and second active regions towards an area of the substrate where there are no active regions** under the Patent Owner's construction. (Ex. 1002, ¶109).

The obvious effect of Yamashita's graded dopant profiles is exemplified by Figs. 3 and 4 of Yamashita, shown side-by-side below. (Ex. 1002, ¶110). Fig. 3

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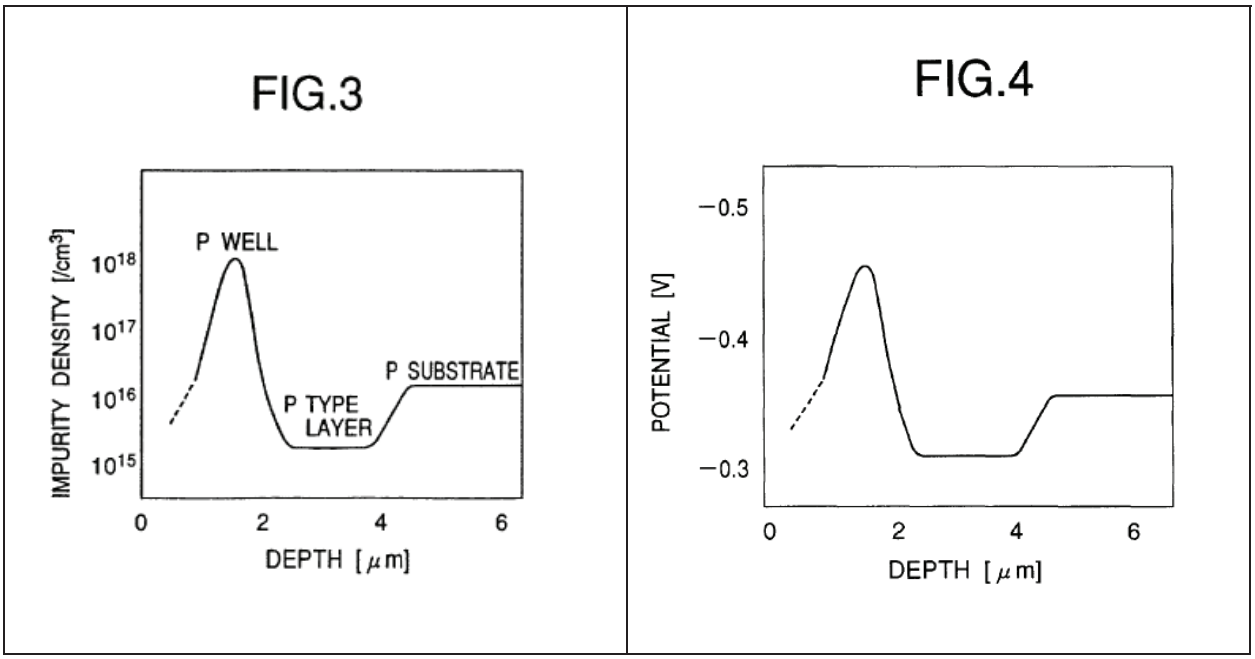
pp. 12-13 (numbers at top))(Patent Owner's infringement contentions directed to a Sony image sensor, describing alleged dopant profiles that aid carrier movement from the surface to the bottom of the substrate, by arguing that "**at least one downward sloped portion** is shown in each of the boron-11 and arsenic plots above, viewed from right (more depth) to left (less depth).")(Emphasis added)(Ex. 1017, pp. 22-23)(applying the same reasoning to the '222 patent).

shows a dopant profile concentration that has a peak between 1 and 2 microns' depth, similar to the peak shown in the dopant concentration profile of Fig. 55. (Ex. 1002, ¶110). That peak produces an electric potential function (the derivative of which is an electric field) as shown in Fig. 4 (right side):



(Ex. 1005, Figs. 3-4, 3:61-64, 7:32-8:5)(Ex. 1002, ¶110). Because of the electric field produced by the retrograde P well, negative carriers (electrons) will move down the slope to the right of the large negative potential peak, while positive carriers (holes) will move up the slope to the left of the positive potential peak, and thus both types of carriers are aided in their movement from the first and second active regions towards an area of the substrate where there are no active regions. (Ex. 1005, 7:32-8:5)(Ex. 1002, ¶111). It would have been obvious to implement, in the Eighth embodiment of Yamashita, a potential gradient similar to the one in Fig. 4 from the

surface to about 2.5 microns in depth using a graded dopant concentration. (Ex. 1002, ¶111). This was obvious because of the similarity of the dopant concentration profiles between 0 and 2.5 microns depth in Figs. 3 and 55, and because the potential gradient of Fig. 4 would fulfill the function of the Eighth Embodiment of Yamashita, namely that "soft error based on electrons can be controlled" by aiding minority carriers toward the bottom of the device. (Ex. 1005, 23:17-26, 7:56-63)(Ex. 1002, ¶111).

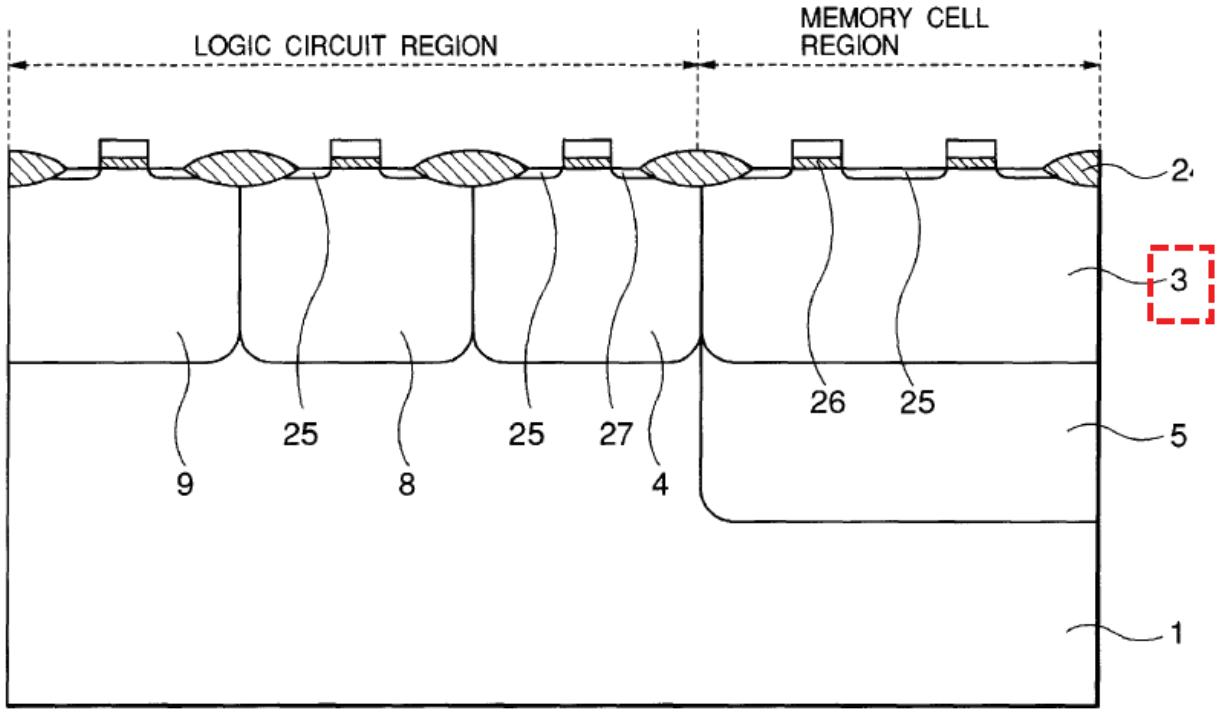
Furthermore, during prosecution of related U.S. Patent No. 8,421,195, the Applicant stated that "a graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carrier into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concertation of dopant." (Ex. 1006, pp. 100-101)(*citing* Ex. 1008, 5:11-13). Accordingly, under Applicant's interpretation, the retrograde wells of Yamashita are sufficient to meet the claim language.

> ***"[1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,"***

Yamashita further teaches **at least one well region adjacent to the first or second active region.** The well region is "retrograde p well 3", which is shown in

Fig. 53. (Ex. 1005, 21:20-22, 21:51-54)(Ex. 1002, ¶112). Figure 53 is reproduced below with an added, red-dashed box around the reference numeral 3 on the right-hand side:

FIG.53



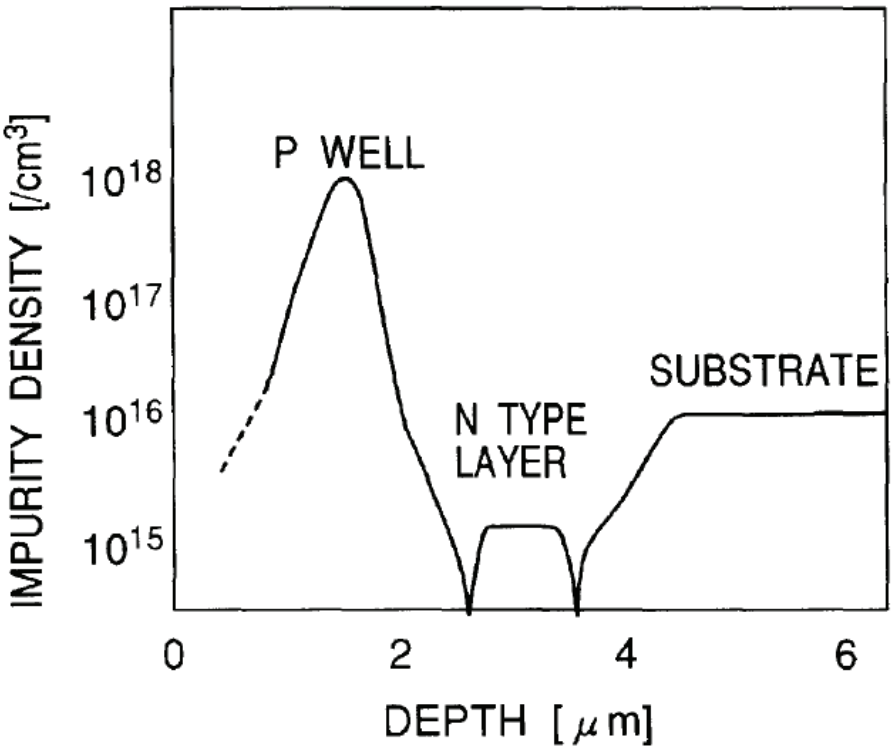
(Ex. 1005, Fig. 53, 21:42-54)(Ex. 1002, ¶112).

The retrograde p-well 3 is a **well region**. (Ex. 1002, ¶113). The well region is **adjacent to the first or second active region**, as shown in Fig. 53. (Ex. 1002, ¶113). It was also obvious to situate the well 3 adjacent to the first active region to have CMOS logic circuits adjacent to a memory area, as suggested by Yamashita. (Ex. 1005, Fig. 53, 21:27-32)(Ex. 1002, ¶113).

The retrograde p-well 3 further **contains at least one graded dopant region.**

The dopant profile is shown in Fig. 10 of Yamashita (Ex. 1005, 21:36-41), reproduced here:

FIG.10



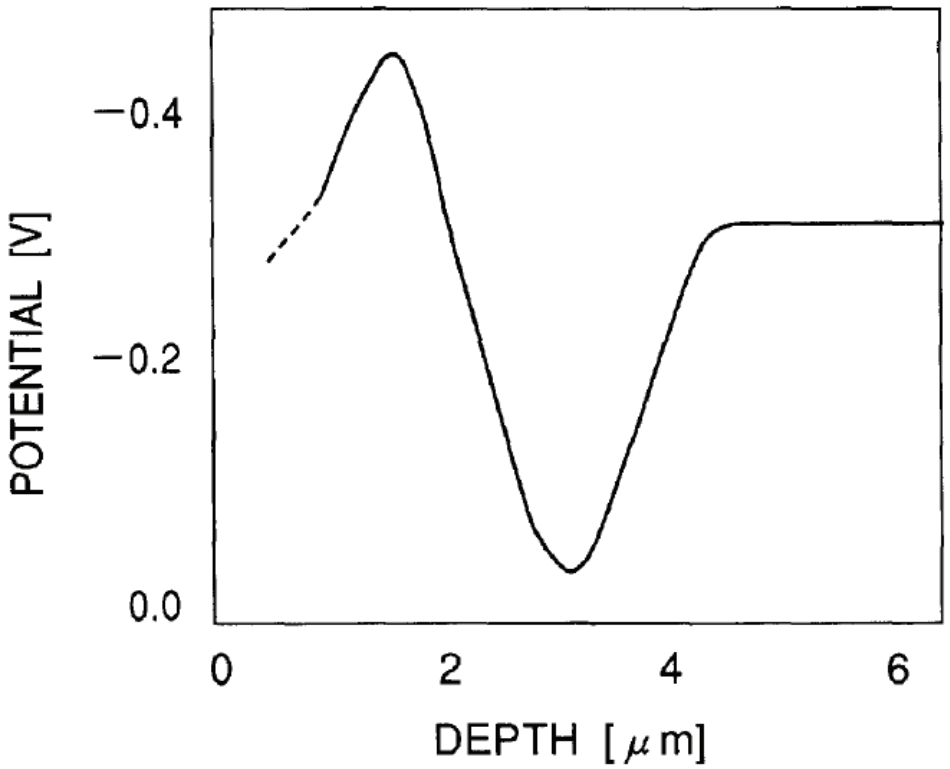
(Ex. 1006, Fig, 10, 21:37-41, 22:10-19)(Ex. 1002, ¶114). Figure 10 shows a dopant concentration ("impurity density") profile similar to the one discussed above under element [1f]. (Ex. 1002, ¶114). The region labeled "p well" corresponds to the retrograde p well 3 and the region labeled "n type layer" corresponds to n type layer 5. (Ex. 1002, ¶114). The Figure shows that the p well has a concentration peak with increasing dopant concentration beginning at the surface and proceeding to a peak,

followed by decreasing dopant concentration to a depth somewhat greater than two microns, where the p well contacts the n type layer below it. (Ex. 1002, ¶114). The well region thus has **at least one graded dopant region.** (Ex. 1002, ¶114).

The graded dopant region is to **aid carrier movement from the surface towards the area of the substrate where there are no active regions**. This is obviously the case under the Patent Owner's claim construction for the same reasons discussed above under claim element [1f]. (Ex. 1002, ¶115).

Furthermore, Yamashita teaches that the graded dopant concentration profile shown in Fig. 10 produces the potential profile shown in Fig. 11, reproduced here:

FIG.11



(Ex. 1005, Fig. 11, 4:14-15, 9:27-34)(Ex. 1002, ¶116). As shown in Fig. 11, the electrical potential (in Volts, in the vertical axis) varies in a manner corresponding to the dopant concentration profile. (Ex. 1002, ¶116). The variation in potential is an electric field. (Ex. 1002, ¶116). The electric field causes movement of charged carriers in opposite directions (toward or away from the bottom of the device, depending on the charge of the carrier and the local direction of the field), and thus **aids carrier movement from the surface towards the area of the substrate where there are no active regions** under the Patent Owner's construction. (Ex. 1002, ¶116).

For example, Yamashita teaches:

> "According to the substrate structure of the memory cell region, as shown in FIG. 10, as in the second embodiment, soft error based on the electron can be controlled, because **the potential barrier of electrons**, generated by α-rays or the like in the p type semiconductor substrate 1, with respect to the upper side of the retrograde p well 3, becomes larger by the existence of the n type impurity layer 5, and **electron flow to the source/drain 25 on the retrograde p well 3 is interrupted**."

(Ex. 1005, 22:10-19)(Emphasis added)(Ex. 1002, ¶117). The potential barrier interrupting electron flow to the source/drain 25 (at the top of the device) indicates that the potential barrier is **aiding** electron (carrier) **movement from the surface** towards the bottom of the device, which is **towards the area of the substrate where**

there are no active regions under the Patent Owner's construction. (Ex. 1002, ¶117).

"[1h] wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

Yamashita teaches that the **transistors** of the first and second active regions **form digital logic**. Yamashita states:

> "A plurality of transistors or a single transistor is formed on the **retrograde p well 8**, the **retrograde n well 4** and the retrograde n well 9 (not shown), and a CMOS is formed on the **logic circuit region**."

(Ex. 1005, 21:55-58)(Emphasis added)(Ex. 1002, ¶118). The logic circuit region is shown in Fig. 53, and encompasses both the first active region (discussed above under element [1c]) and the second active region (discussed above under element [1d]). (Ex. 1005, Fig. 53, 21:55-65, 22:10-18, 22:32-39)(Ex. 1002, ¶118).

As described above in the section entitled "Rationale (Motivation) for the Combination", it would have been obvious to use Yamashita's techniques in a VLSI device and in Silverbrook's ICP, which requires both DRAM and associated processing circuitry. (Ex. 1002, ¶119). In that way, the combination renders obvious that **at least some of the transistors form digital logic of the VLSI semiconductor device.** (Ex. 1002, ¶119).

CLAIM 2

"2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.'

Yamashita teaches **the substrate is a p-type substrate**. (Ex. 1005, 22:10-14, 22:33-35)(Ex. 1002, ¶120).

CLAIM 3

"3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

Yamashita teaches that its **substrates** can have **epitaxial silicon**. Specifically, Yamashita teaches that the p-type layer 2, as well as the n type layer 5, are "formed by epitaxial growth". (Ex. 1005, 8:11-16, 8:50-54, 11:62-64, 12:27-28. 15:56-61, 16:53-57, 18:39-42, 21:20-24, 26:31-36)(Ex. 1002, ¶121). Silicon formed by epitaxial growth is **epitaxial silicon**. Furthermore, these layers are "formed on the p type semiconductor substrate 1". (Ex. 1005, 8:11-15, 10: 50-54, 11:62-67, 21:20-24, Figs. 60, 53)(Ex. 1002, ¶121).

While Yamashita does not expressly state that the substrate of the Eighth Embodiment is epitaxial silicon is **on top of a nonepitaxial substrate**, this was a common practice in the relevant timeframe, as explained by Mr. Guidash. (Ex. 1002, ¶122). In general, epitaxial silicon layers are higher quality for device manufacturing, but slower to grow. (Ex. 1002, ¶122). Therefore, providing a thicker nonepitaxial substrate for handling and stability, topped by a higher-quality epitaxial

substrate, made economic sense in the relevant timeframe. (Ex. 1002, ¶122).

CLAIM 4

"4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices."

See above, claim 1, limitations [1c]-[1e] (discussing the formation of transistors in the first and second active regions, as well as their dopant types), limitation [1h] (discussing the transistors forming digital logic). The transistors in the first and second active region comprise both **p-channel and n-channel** devices. (Ex. 1005, 21:42-65)(Ex. 1002, ¶123).

CLAIM 5

"5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

See above, claim 4 (discussing p-channel and n-channel devices), claim 1, elements [1c] and [1d] (discussing the n-wells (*e.g.*, n well 4) and p-wells (*e.g.*, p well 8) respectively), and claim limitation [1f] (discussing the graded dopant regions in the retrograde n well 4 and the retrograde p well 8). (Ex. 1002, ¶124).

CLAIM 6

"6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

Yamashita teaches that the **first active region and second active region are each separated by at least one isolation region**, specifically field oxide region 24. (Ex. 1002, ¶125). As discussed above under claim 1, element [1c], the active regions under gate oxide 29 in Fig. 57 are separated by "separation regions" in the form of field oxide 24. (Ex. 1005, 22:32-39, 22:57-23:17)(Ex. 1002, ¶125). These separation regions are visible between active regions, including after transistor construction, in Figs. 53 and 57-63. (Ex. 1002, ¶125). Field oxide regions are **isolation regions**. (Ex. 1002, ¶125).

CLAIM 7

"7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process."

Yamashita teaches that the **graded dopant is fabricated with an ion implantation process** in each of retrograde p wells 3 and 8, as well as retrograde n well 4. (Ex. 1005, 22:57-23:17)(Ex. 1002, ¶126).

CLAIM 8

"8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

Yamashita teaches this claim. (Ex. 1002, ¶127). *See* above, claim 1, element [1c], which already requires that the *first* active region be "disposed adjacent to the surface". (Ex. 1002, ¶127). The *second* active region, in turn, is disposed

horizontally adjacent to the first active region (*see* above, claim 1, element [1d]), and is also **adjacent the first** (top) **surface of the substrate**. *See* above, claim 1, element [1d]. (Ex. 1002, ¶127). To the extent that the word "formed" (as opposed to the word "disposed" in claim 1) requires a physical process, the first and second active regions are also "formed" where they are ultimately "disposed". (Ex. 1005, 21:55-22:6, Fig. 53)(Ex. 1002, ¶127).

CLAIM 9

> ***"9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type."***

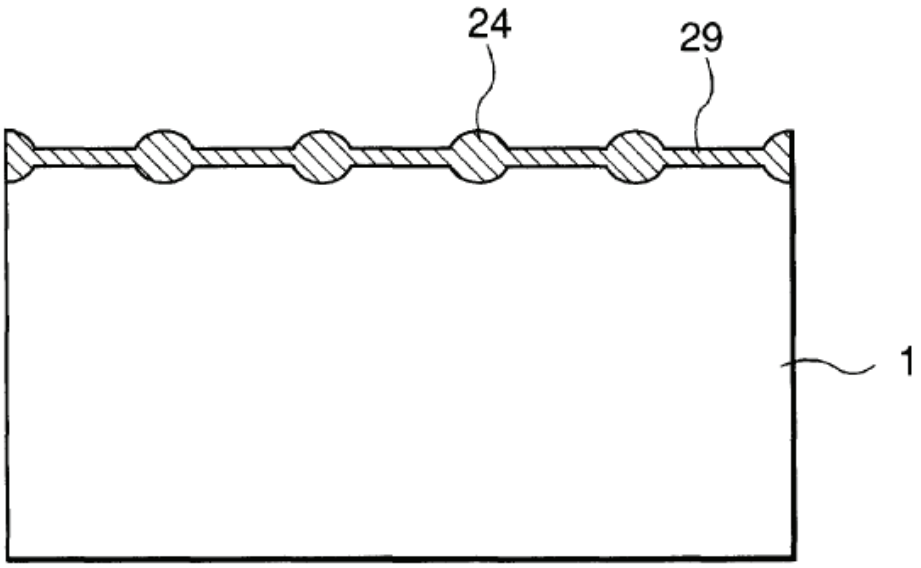
Yamashita teaches this claim. (Ex. 1002, ¶128). *See* above, claim 1, limitations [1c] and [1d] (discussing dopants of the first and second active region) as well as limitation [1f], discussing the graded dopants. (Ex. 1002, ¶128).

CLAIM 10

> ***"10. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type."***

Yamashita teaches claim 10. As discussed above under claim 1, element [1b], Yamashita begins with a "p type semiconductor substrate 1 containing boron of a concentration on the order of $1 \times 10^{16} / cm^3$". (Ex. 1005, 22:33-38, 6:1-2, 21:20-24, 22:19-24, 7:19-21)(Ex. 1002, ¶129). The substrate 1, at an earlier stage in the fabrication process, is shown in Fig. 57, reproduced here:

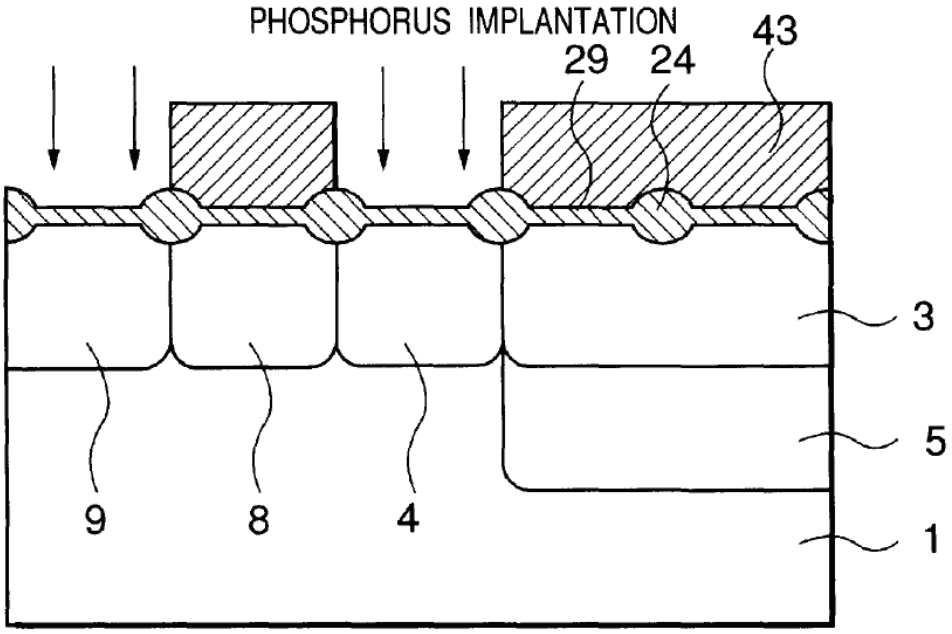
FIG.57



(Ex. 1005, Fig. 57, 22:33-38)(Ex. 1002, ¶129).

As discussed above under claim 1, element [1c], the **first active region** has a retrograde n well 4, which has a graded dopant concentration. The retrograde n well 4 is formed by the ion implantation of phosphorus ions, which are **n-type dopants**, into the already p-type substrate. (Ex. 1005, 23:4-12)(Ex. 1002, ¶130). This implantation is shown in Fig. 63, reproduced again here:

FIG.63



(Ex. 1005, Fig. 63, 23:4-12)(Ex. 1002, ¶130).

Because the n well 4 (which is in the first active region) is formed by the implantation of n-type dopants into substrate 1, which has p-type dopants, and because the implantation of n-type dopants does not remove p-type dopants, Yamashita teaches claim 10. (Ex. 1002, ¶131).

CLAIM 11

"11. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type."

The combination renders claim 11 obvious. As discussed above under claim 1, elements [1d] and [1f], the second active region of Yamashita contains a

retrograde p well 8, which has a **graded dopant region** containing **p-type dopants** (namely, boron). (Ex. 1005, 22:64-23:3)(Ex. 1002, ¶132).

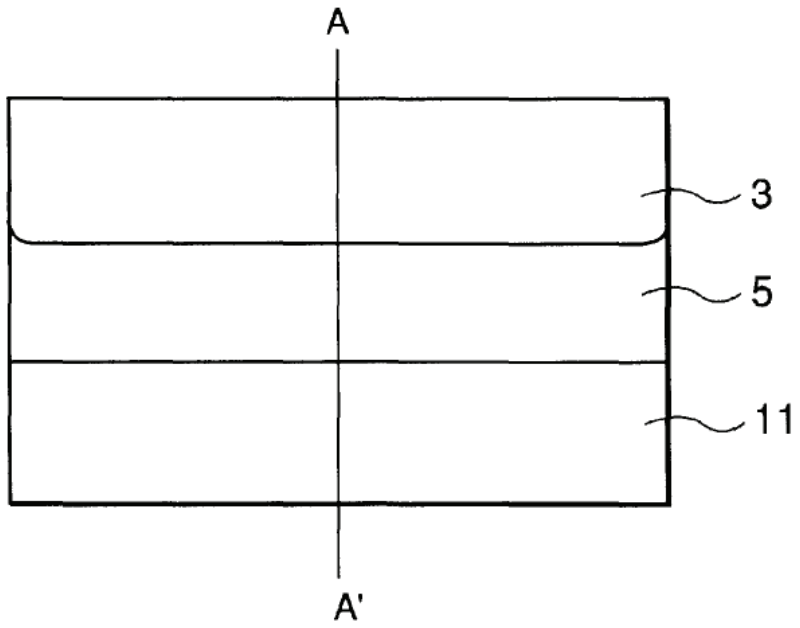
With respect to the required n-type dopants, it would have been obvious to use an n-type substrate, in which the retrograde p well 8 was implanted, thus providing both p-type and n-type dopants. (Ex. 1002, ¶133).

Specifically, Yamashita discloses, in the context of its Seventh Embodiment, an "n type semiconductor substrate 11". (Ex. 1005, 19:57-20:7, 20:31-39, Fig. 48)(Ex. 1002, ¶134). The n-type semiconductor 11 then has a p-type impurity layer 2 and a retrograde p well 3. Yamashita states:

> "A substrate of the semiconductor device, as shown in FIG. 48, comprises the n type semiconductor substrate 11 containing phosphorus of concentration on the order of $1x10^{16}$ /cm^3, the n type impurity layer 5 containing phosphorus of concentration on the order of $1x10^{15}$ /cm^3 and the retrograde p well 3 containing boron of concentration on the order of $1x10^{18}$ /cm^3."

(Ex. 1005, 20:1-7)(Ex. 1002, ¶134). The layers are shown in Fig. 48, reproduced here:

FIG.48



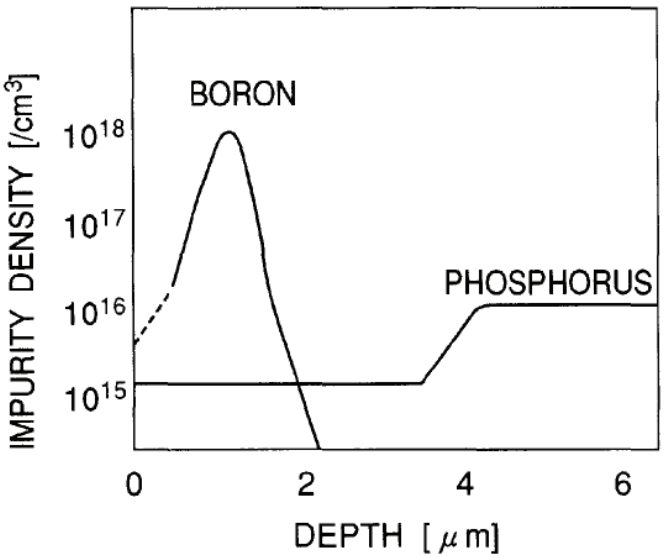
(Ex. 1005, Fig. 48)(Ex. 1002, ¶134).

It would have been obvious to use an n-type substrate, as suggested by the Seventh Embodiment of Yamashita, in the Eighth Embodiment of Yamashita. A POSITA would have recognized that the Eighth Embodiment could have been used with a p-type or an n-type substrate without unpredictable results and with a reasonable expectation of success, as long as the appropriately doped well is implanted for each type of device. (Ex. 1002, ¶135). In the Seventh Embodiment, for example, a retrograde p well 3 is implanted near the surface, which is similar to the retrograde p well implanted for the second active region. (Ex. 1005, 20:1-7, 20:35-39, *compare* Figs. 50 and 54)(Ex. 1002, ¶135). In addition, Yamashita teaches that the structure of the Seventh Embodiment can improve pressure resistance and

prevent degradation of transistor threshold voltage. (Ex. 1005, 20:31-39)(Ex. 1002, ¶135). A POSITA would thus have expected advantages in using the n-type semiconductor substrate and structure of the Seventh Embodiment together with the Eighth Embodiment of Yamashita. (Ex. 1002, ¶135).

With the n-type semiconductor substrate of the Seventh Embodiment, the substrate has a dopant concentration, as required by claim 1, specifically phosphorus of concentration on the order of $1x10^{16}$ /cm^3. (Ex. 1005, 18:59-65)(Ex. 1002, ¶136). The dopant concentration profile along the line A – A' in Fig. 48 is shown in Fig. 50, reproduced here:

FIG.50



(Ex. 1005, Fig. 50, 5:60-62, 19:65-67)(Ex. 1002, ¶136). The profile of Fig. 50 is similar to the profile in the second active region (shown in Fig. 54), as discussed

above under claim 1, element [1f], except that in Fig. 50, the n-type dopant (phosphorous) is present from the n-type substrate. (Ex. 1002, ¶136).

As can be seen from the Figure, the p-type dopant (boron) and n-type dopant (phosphorous) overlap in the region of graded dopant profile. (Ex. 1002, ¶137). Thus, both dopant types obviously would contribute to the dopant level, meaning that **dopants of the graded dopant concentration in the second active region are both p-type and n-type.** (Ex. 1002, ¶137).

CLAIM 12

> ***"12. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type."***

Yamashita teaches claim 12. As discussed above under claim 1, element [1g], the well region with a graded dopant concentration is the p well 3. The p well 3 is formed by boron implantation, and thus has **p-type dopants**. (Ex. 1005, 22:57-63, Fig.)(Ex. 1002, ¶138). The p well 3, however, is formed after the ion implantation and diffusion of phosphorous, which is an n-type dopant, forming layer 5. (Ex. 1005, 22:39-63, Figs. 58-61)(Ex. 1002, ¶138). Because the p well 3 is formed by the implantation of p-type dopants into n-type layer 5, which has n-type dopants, and because the implantation of p-type dopants does not remove n-type dopants, Yamashita teaches claim 12. (Ex. 1002, ¶138).

CLAIM 13

"13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel."

Yamashita teaches that **the transistors which can be formed in the first and second active regions are CMOS digital logic transistors.** The first and second active regions, and their transistors, are discussed above under claim 1, elements [1c]-[1e]. Yamashita states that the transistors can form CMOS digital logic. Yamashita states:

> "**A plurality of transistors** or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a **CMOS** is formed on the logic circuit region."

(Ex. 1005, 21:52-58)(Emphasis added)(Ex. 1002, ¶139). As Mr. Guidash explains, a POSITA would have understood from this description that pMOS transistors are formed in the n well 4, and nMOS transistors are formed in the p well 8, and that these transistors together form CMOS digital logic, and are thus **CMOS digital logic transistors**. (Ex. 1002, ¶139). The MOSFET transistors in Yamashita have sources, drains, channels, and gates. (Ex. 1005, 21:55-65, 22:32-39)(Ex. 1002, ¶139).

CLAIM 14

"14. The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)."

The combination renders claim 14 obvious. (Ex. 1002, ¶140). Specifically, it would have been obvious to use Yamashita in a VLSI DRAM chip, and independently, Silverbrook teaches that its chip has DRAM, and is thus **a dynamic random access memory (DRAM).** (Ex. 1004, 7:28-30, 8:63-67, Fig. 15)(Ex. 1002, ¶140).

CLAIM 15

15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate."

The combination renders claim 15 obvious. (Ex. 1002, ¶141). *See* above, claim 13 (addressing CMOS) and claim 3 (addressing the nonepitaxial substrate). (Ex. 1002, ¶141).

CLAIM 16

"16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory."

The combination renders claim 16 obvious. (Ex. 1002, ¶142). Specifically, Silverbrook teaches that its chip has flash memory, and is thus **a flash memory.** (Ex. 1004, 7:20, 7:28-30, Fig. 15)(Ex. 1002, ¶142).

CLAIM 17

"17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors."

The combination renders claim 17 obvious. (Ex. 1002, ¶143). Yamashita and

Silverbrook both teach and render obvious DRAM, which has individual cells that store individual bits of information as charge in a capacitor. (Ex. 1004, 7:28-30, 8:63-67, Fig. 15)(Ex. 1005, 1:12-15)(Ex. 1002, ¶143). Yamashita also expressly teaches forming capacitors. (Ex. 1005, 23:10-12)(Ex. 1002, ¶143). Yamashita and Silverbrook likewise teach digital logic, as discussed above under claim 1, element [1h]. (Ex. 1002, ¶143).

CLAIM 18

"18. The VLSI semiconductor device of claim 1, wherein the device is central processing unit."

The combination renders claim 14 obvious. (Ex. 1002, ¶144). Specifically, Silverbrook teaches that its chip has a central processing unit, and is thus **a central processing unit.** (Ex. 1004, 7:18, 7:28-30, 11:14-20, Fig. 15)(Ex. 1002, ¶144).

CLAIM 19

"19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor."

The combination renders claim 19 obvious. (Ex. 1002, ¶145). Specifically, Silverbrook teaches that its chip has an image sensor occupying most of the area of the chip**,** and thus **is an image sensor.** (Ex. 1004, 6:56-57, 7:6, 7:28-30, Fig. 15)(Ex. 1002, ¶145).

CLAIM 20

"20. The VLSI semiconductor device of claim 1, wherein each of the

first and second active regions are in the lateral or vertical direction."

See above, claim 1, elements [1c] and [1d]. The first and second active regions laterally next to one another. (Ex. 1005, Fig. 53)(Ex. 1002, ¶146).

CLAIM 21

Claim 21 is similar to claim 1. A comparison (redline) of differences between claims 1 and 21 is provided in Ex. 1009 (p. 5).

"21[a]. A VLSI semiconductor device, comprising:"

See discussion above, claim 1, element 1[a], which has the same language. (Ex. 1002, ¶148)(Ex. 1009, p. 5).

"[21b] a substrate of a first doping type at a first doping level having a surface;"

See discussion above, claim 1, element [1b], which has the same language. (Ex. 1002, ¶149)(Ex. 1009, p. 5).

"[21c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

See discussion above, claim 1, element [1c], which has similar language (Ex. 1002, ¶150)(Ex. 1009, p. 5). The present element [21c] specifies that the "surface" is the "surface of the substrate", and that transistors can be formed "in the surface"

of the first active region. These differences in language do not affect the mapping of the prior art onto the claim, because the transistors in Yamashita's first and second active regions are formed at the surface of the substrate, which is also the surface of the active region. *See* above, claim 1, element [1e]. (Ex. 1002, ¶150).

"[21d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

See discussion above, claim 1, element [1d], which has similar language (Ex. 1002, ¶151)(Ex. 1009, p. 5). The present element [21d] specifies that transistors can be formed "in the surface" of the second active region. This difference in language does not affect the mapping of the prior art onto the claim, because the transistors in Yamashita's first and second active regions are formed at the surface of the substrate, which is also the surface of the active region. *See* above, claim 1, element [1e]. (Ex. 1002, ¶151).

"[21e] transistors formed in at least one of the first active region or second active region;"

See discussion above, claim 1, element [1e], which has the same language. (Ex. 1002, ¶152)(Ex. 1009, p. 5).

"[21f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where

there are no active regions; and"

See discussion above, claim 1, element [1f], which has similar language. (Ex. 1002, ¶153)(Ex. 1009, p. 5). The present claim element [21f] specifies that carrier movement is aided "from the surface" instead of "from the first and second active regions", but this does not affect the mapping of the prior art to the claim, because the first and second active regions are aligned with the surface [of the substrate]. *See* above, claim 1, element [1c]-[1d]. (Ex. 1002, ¶153).

"[21g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and"

See discussion above, claim 1, element [1g], which has similar language. (Ex. 1002, ¶154)(Ex. 1009, p. 5). The present claim element [21g] changes the word "towards" to "to", but this does not affect the mapping of the prior art to the claim. *See* above, claim 1, element [1g]. (Ex. 1002, ¶154)(Ex. 1006, p. 100)(Ex. 1017, pp. 12-13, 22-23)(Ex. 1014, pp. 2, 26, 28)(plaintiff's claim construction brief).

"[21h] wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

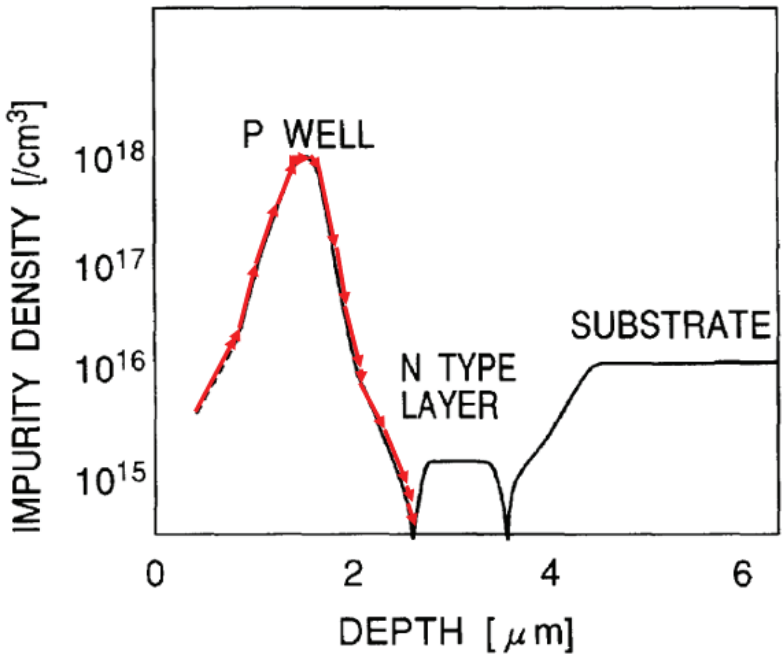
It was obvious from Yamashita's disclosure of the graded dopant concentration in the p well 3 (*see* above, claim 1, element [1g]) that the concentration

profile was linear, **quasilinear, error function, complementary error function, or any combination thereof**. (Ex. 1002, ¶155)

First, the p well 3 was formed by ion implantation, and ion implantation would obviously have resulted in the claimed mathematical profile. This is because, as Mr. Guidash explains, ion implantation (followed by annealing and diffusion) yields a dopant concentration profile that can be modeled using complementary error functions. (Ex. 1002, ¶156). The claim does not specify the value of constants used, and allows for use "in any combination", thus accounting for any departures from the ideal distribution. (Ex. 1002, ¶156).

Furthermore, the clause of the claim that permits "any combination thereof" would cover the dopant profiles of Yamashita. For example, as Mr. Guidash explains, choosing a sequential combination of piece-wise linear functions having tangents to the dopant profiles of Yamashita would allow for a nearly exact reproduction of those profiles. (Ex. 1002, ¶157). This is shown, for example, in the reproduction of Fig. 10 below, which has red arrows added to show a series of linear functions that, when combined, match the profile of Fig. 10. The match between the actual dopant profile and the one formed from tangent lines can be improved to an arbitrary degree, simply by shortening the tangent lines (in the figure, by using a greater number of shorter arrows):

FIG.10



(Ex. 1002, ¶157)(Ex. 1005, Fig. 10). Thus, it would have been obvious from the combination that **the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.** (Ex. 1002, ¶157).

CLAIM 22

> ***"22. The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate."***

See above, claim 11, discussing that it would have been obvious to use an n-type substrate with the Eighth Embodiment of Yamashita. (Ex. 1002, ¶158).

CLAIM 23

"23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate."

See above, claim 2. (Ex. 1002, ¶159).

CLAIM 24

"24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

See above, claim 3. (Ex. 1002, ¶160).

CLAIM 25

"25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices."

See above, claim 4. (Ex. 1002, ¶161).

CLAIM 26

"26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

See above, claim 5. (Ex. 1002, ¶162).

CLAIM 27

"27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region."

See above, claim 6. (Ex. 1002, ¶163).

CLAIM 28

"28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type."

See above, claim 9. (Ex. 1002, ¶164).

CLAIM 29

"29. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type."

See above, claim 10. (Ex. 1002, ¶165).

CLAIM 30

"30. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type."

See above, claim 11. (Ex. 1002, ¶166).

CLAIM 31

"31. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant region in the well region are both p-type and n-type."

See above, claim 12. (Ex. 1002, ¶167).

CLAIM 32

"32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process"

See above, claim 7. (Ex. 1002, ¶168).

CLAIM 33

"33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device."

See above, claim 15. (Ex. 1002, ¶169).

CLAIM 34

"34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory."

See above, claim 16. (Ex. 1002, ¶170).

CLAIM 35

"35. The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions."

See above, claim 1, element [1h], explaining that the device has digital logic and element [1e], explaining that the first and second active regions have transistors. As Mr. Guidash explains, the FET transistors in Yamashita have a gate **capacitor** formed of the gate electrode and the transistor channel, with a gate oxide in between the two. (Ex. 1002, ¶171). The device is thus **a logic device with capacitors in at least some of the first or second active regions**. (Ex. 1002, ¶171).

CLAIM 36

"36. The VLSI semiconductor device of claim 21, wherein the device is central processing unit."

See above, claim 18. (Ex. 1002, ¶172).

CLAIM 37

"37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor."

See above, claim 19. (Ex. 1002, ¶173).

CLAIM 38

"38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction."

See above, claim 20. (Ex. 1002, ¶174).

Ground 2. Claims 39-43 were obvious over Yamashita.

Claims 39-43 are obvious over Yamashita (discussed under Ground 1) alone. The rationale underlying obviousness is explained in the claim mapping section where appropriate. Other considerations relating to obviousness (*Graham* factors, etc.) are the same as in Ground 1.

A. Claim Mapping

CLAIM 39

"39[a]. A semiconductor device, comprising:"

Yamashita teaches a "semiconductor device" (Ex. 1005, Abstract)(Ex. 1002, ¶176).

"[39b] a substrate of a first doping type at a first doping level;"

See above, claim 1, element [1b], which has the same language, except that claim element [1b] additionally recites "having a surface". (Ex. 1002, ¶177)(Ex. 1009, p. 1)(showing a redline comparison between claim 39 and claim 1).

"[39c] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

See above, claim 1, element [1c], which has similar language. (Ex. 1002, ¶178)(Ex. 1009, p. 1). The present claim element [39c], adds that the first active region is disposed adjacent to a surface "of the substrate", but there is no material change, because in claim 1, element [1b] already defined the "surface" as part of the substrate. (Ex. 1002, ¶178)(Ex. 1009, p. 1).

"[39d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

See above, claim 1, element [1d], which has the same language. (Ex. 1002, ¶179)(Ex. 1009, p. 1).

"[39e] transistors formed in at least one of the first active region or second active region; and"

See above, claim 1, element [1d], which has similar language, except that the present claim element [39e] recites "first active region <u>or</u> second active region" instead of "and". This does not have a material effect on the claim mapping. (Ex.

1002, ¶180)(Ex. 1009, p. 1).

> ***"[39f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."***

See above, claim 1, element [1f], which has similar language. (Ex. 1002, ¶181)(Ex. 1009, p. 1). The present claim element [39f] recites "to at least one area" instead of "towards at least one area", but this does not affect the mapping of the prior art to the claim, because Yamashita already teaches aiding carrier movement "to" an area of the substrate where there are no active regions under the Patent Owner's construction. *See* above, claim 1, element [1f]. (Ex. 1002, ¶181).

The present limitation [39f] also uses "first <u>or</u> second active region" instead of the phrase "first and second active regions" in claim 1. This again has no material effect on the mapping of prior art to the claims. (Ex. 1002, ¶182).

<u>CLAIM 40</u>

> ***"40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well."***

See above, claim 1, element [1g]. Claim 40 differs from claim element [1g] by requiring the graded dopant region to aid carrier movement from any region in

the well to the substrate area where there is no well. This language is similarly met by the structure described under claim element [1g] under the Patent Owner's construction, because Yamashita teaches that the graded dopant concentration creates an electric field that moves electrons toward the bottom of the device. (Ex. 1002, ¶183).

CLAIM 41

Claim 41 is identical to claim 39, except that the word "acceptor" has been added in the phrase "graded dopant acceptor concentration". (Ex. 1009, p 2)(Ex. 1002, ¶184). Yamashita teaches this limitation, because the second active region has a retrograde p well 8, as explained above under claim 1, element [1d]. (Ex. 1002, ¶184). The p well 8 has a graded dopant concentration of boron, which is an acceptor. (Ex. 1005, 22:64-23:3, Figs. 53, 61)(Ex. 1002, ¶184).

CLAIM 42

Claim 42 is identical to claim 39, except that the word "donor" has been added in the phrase "graded donor dopant concentration". (Ex. 1009, p. 3)(Ex. 1002, ¶185). Yamashita teaches this limitation, because the first active region has a retrograde n well 4, as explained above under claim 1, element [1c]. (Ex. 1002, ¶185). The n well 4 has a graded dopant concentration of phosphorous, which is a donor. (Ex. 1005, 23:4-12, Figs. 53, 63)(Ex. 1002, ¶185).

CLAIM 43

Claim 43 is identical to claim 39, except that the phrase "at least one graded

acceptor dopant concentration and one graded donor dopant concentration" has been added in the phrase "at least one of the first and second active regions having at least one graded acceptor dopant concentration and one graded donor dopant concentration". (Ex. 1009, p. 4)(Ex. 1002, ¶186). Yamashita teaches this limitation, for the reasons provided under claims 41 and 42. (Ex. 1002, ¶186).

Ground 3. Claims 1-43 were obvious over Silverbrook, Yamashita, and Nishi

Claims 1-43 were obvious over Silverbrook and Yamashita (Grounds 1 and 2) in further view of the Nishi, et al. (eds.) *Handbook of Semiconductor Manufacturing Technology*, Marcel Dekker, Inc., New York (2000)(Ex. 1012).

A. Effective Prior Art Dates

Silverbrook and **Yamashita** are prior art as discussed under Ground 1.

Nishi is a textbook published in the year 2000. (Ex. 1002, ¶188)(*citing* Exs. 1024-1027). It thus qualifies as prior art under pre-AIA 35 U.S.C. §102(b).

B. Overview of the Ground

This ground posits that it would have been obvious to provide for additional graded dopant profile portions to the retrograde wells 4 and 8 of Yamashita, as taught by Nishi. The ground is directed to the possibility that the Patent Owner might argue both that the term "active region" has a particular depth at which it stops, and that Yamashita does not teach a graded dopant profile within that depth.

The combination with Nishi begins with the observation that Nishi teaches a "modulated retrograde well" dopant profile—applicable to CMOS transistors—in its Fig. 11 and surrounding text. (Ex. 1012, p. 086)(Ex. 1002, ¶190). Figure 11 of Nishi is reproduced below, and shows a dopant concentration profile with depth, where the surface of the substrate is on the left side of the figure:

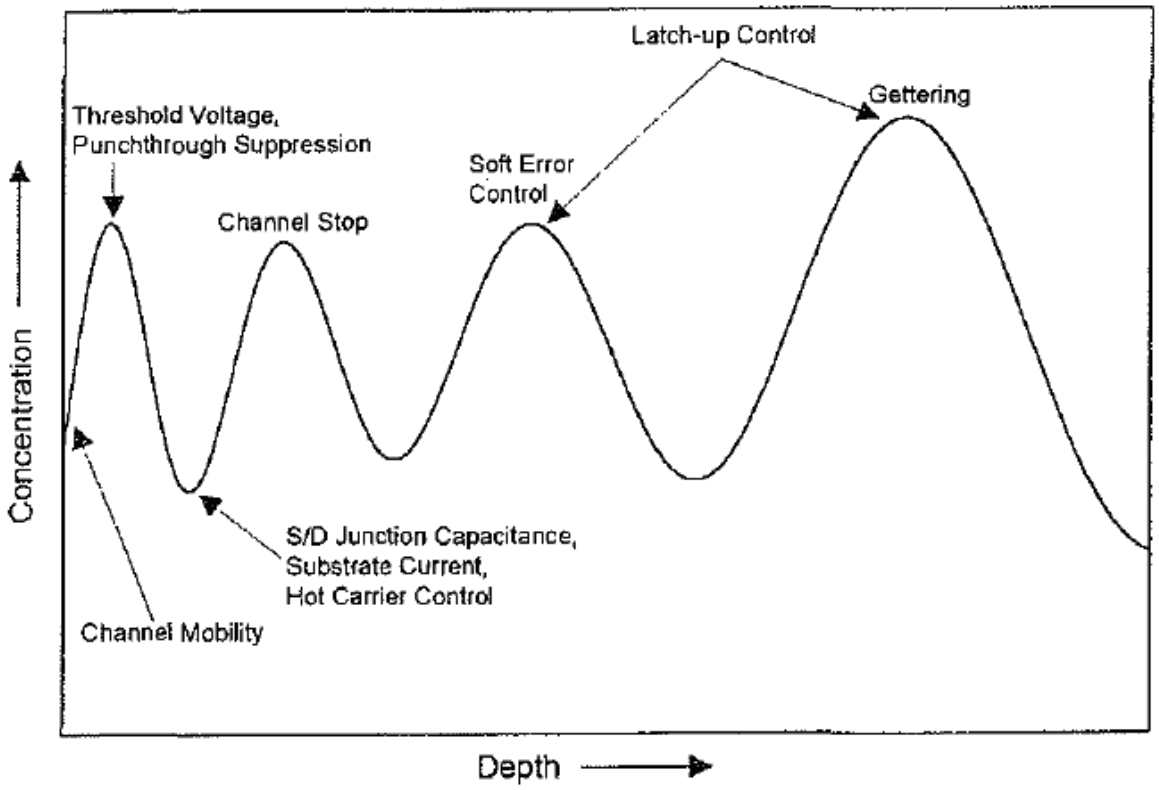
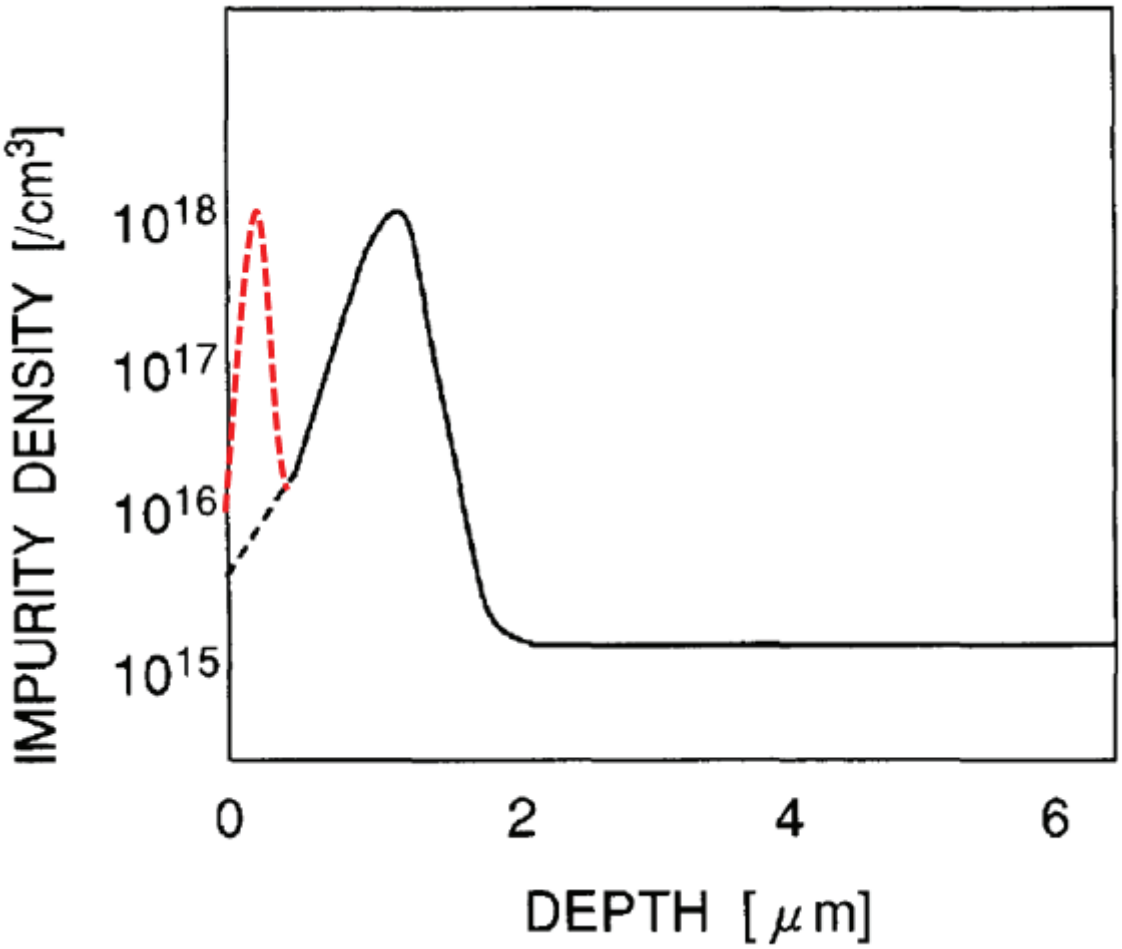


Figure 11 Doping profile of a modulated retrograde well structure, showing the device parameters affected by the doping level at each depth. Adapted from references [40,41].

(Ex. 1012, Fig. 11, p. 086)(Ex. 1002, ¶190).

This ground posits that it would have been obvious to provide for at least the

left-most peak in the Nishi Fig. 11 profile (labeled with "Threshold voltage, Punchthrough Suppression" at the peak and "Channel Mobility" at the left shoulder") in Yamashita's retrograde wells 4 and 8. (Ex. 1012, p. 086)(Ex. 1002, ¶191). This would have provided for a graded dopant profile that is very close to the surface of the device in Yamashita, and within the transistor channel. (Ex. 1002, ¶191). A modified version of Fig. 55 of Yamashita, showing the additional peak from Nishi, is provided below, with an added, red-dashed line indicating the peak from Nishi provided for punch-through suppression and threshold voltage, with adjacent valleys for channel mobility and hot carrier control:



(Ex. 1002, ¶191). A similar modification would be made to the dopant profiles in both wells 4 and 8, using n-type and p-type dopants, respectively. (Ex. 1002, ¶192).

A. Rationale (Motivation) Supporting Obviousness

The modification would have been obvious. (Ex. 1002, ¶193). Yamashita already suggests such a modification, stating:

> "A plurality of transistors or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region. **In this case, in the retrograde wells, the channel implantation layer**

> **for punch-through prevention and threshold control is formed at the depth of 0-0.2 µm from the substrate as needed**."

(Ex. 1005, 21:55-61)(Emphasis added)(Ex. 1002, ¶193). This expressly suggests forming an implantation in the transistor channel region, which would result in a peak of dopant concentration at a depth between 0 and 0.2 µm. (Ex. 1002, ¶193). Furthermore, the purpose of this implantation is for "punch-through prevention and threshold control", which are exactly the purposes shown in Fig. 11 of Nishi for the left-most (shallowest) dopant concentration peak. (Ex. 1002, ¶193). This implantation would make sense in Yamashita's device, as Mr. Guidash explains. (Ex. 1002, ¶193).

Furthermore, Yamashita teaches that the transistors in the Logic Circuit Region (*see* Fig. 53) are MOSFET transistors in a CMOS process. (Ex. 1005, 21:34)(Ex. 1002, ¶194). Nishi teaches that the modulated retrograde well is particularly effective for such transistors, and had, by 2000, replaced other standard well processes. (Ex. 1012, p. 086)(Ex. 1002, ¶194). Nishi explains:

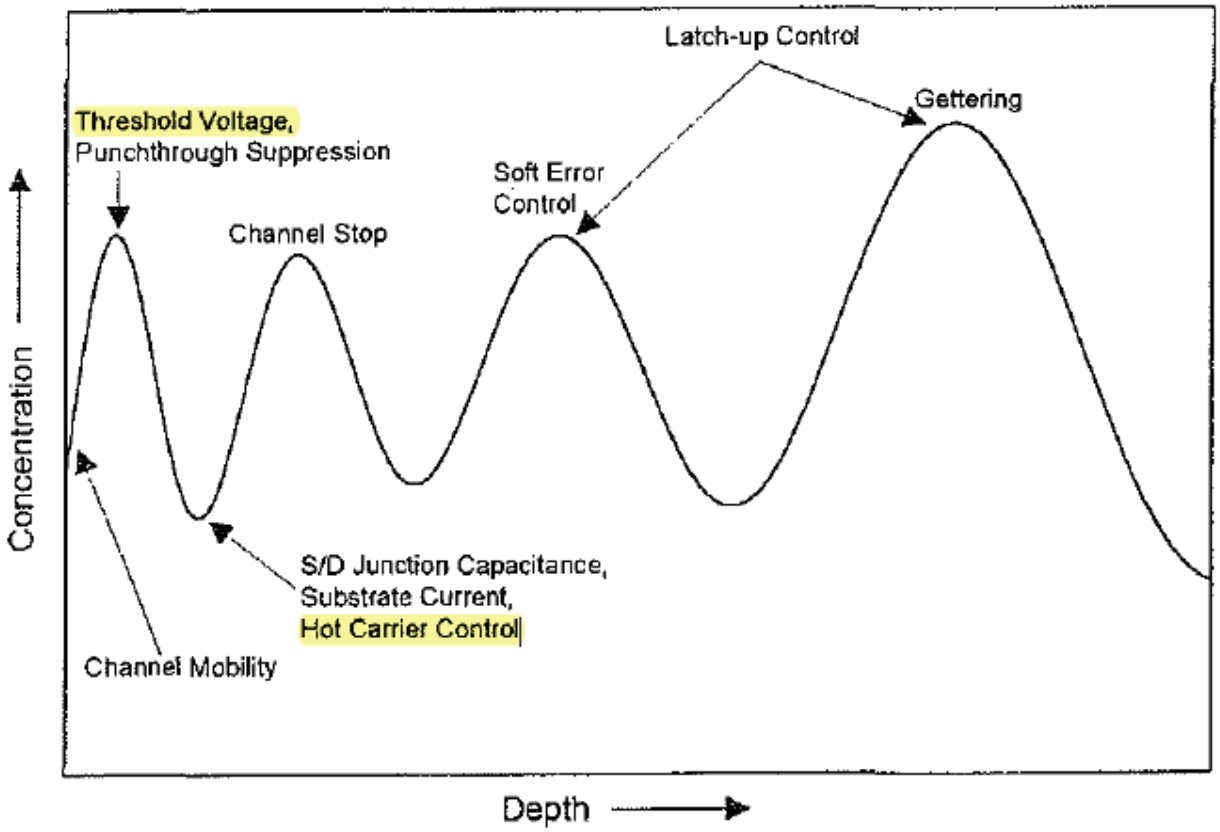
> "Ion implantation is essential for fabricating the twin tub (both p-well and n-well implants) CMOS process. **The modulated well structure (Fig. 11) has replaced the older diffused well process**, **due to its higher processing flexibility and lower cost**. Since the well forms the MOSFET's 'back gate', the well doping will fundamentally affect the transistor's electrical performance. **Engineering the well with multiple implants and minimal**

> **thermal diffusion** allows independent control of dopant levels throughout the depth of the well, and thus **independent optimization of key MOSFET performance characteristics** (Fig. 11)."

(Ex. 1012, p. 086)(Emphasis added)(Ex. 1002, ¶194). Nishi thus teaches to engineer wells "with multiple implants and minimal thermal diffusion", which results in multiple peaks in the dopant profile concentration, as shown in Fig. 11. (Ex. 1012, p. 086)(Ex. 1002, ¶194). Among other things, this allows better control of the threshold voltage of the transistor ("V_T"), allows for punch-through suppression, and allows for hot carrier control, as shown in Nishi Fig. 11 and (as to V_T and punch-through suppression) taught expressly by Yamashita. (Ex. 1005, 21:55-61)(Ex. 1012, pp. 085-086)(Ex. 1002, ¶194). Nishi further teaches that having a lower dopant concentration at shallower depths in the transistor channel "increase[s] mobility and decrease[s] capacitance", while "[h]eavier doping below the surface (retrograde doping) reduces minority carrier collection…." (Ex. 1012, p. 086)(Ex. 1002, ¶194). To the extent desired, a POSITA could have used all four peaks shown in Nishi Fig. 11 in an obvious manner. (Ex. 1002, ¶194). These advantages (the ability to better control the transistor threshold voltage, punch-trough suppression, hot carrier control and increased transistor channel mobility, decreased minority carrier collection and decreased capacitance) would have been seen as valuable by a POSITA in the relevant timeframe, and would have rendered the combination

obvious. (Ex. 1002, ¶194).

Furthermore, it would have been obvious to arrange the doping peak of Nishi in Yamashita specifically to **aid the movement of carriers from the first and second active regions towards an area of the substrate where there are no active regions** (applying the Patent Owner's construction, as explained above under Ground 1, element [1f])**.** (Ex. 1002, ¶195). This would have been obvious to a POSITA in order to achieve the threshold voltage control and hot carrier control, as shown in Fig. 11 of Nishi, reproduced again here with highlighting added:



(Ex. 1012, Fig. 11, p. 086)(Ex. 1002, ¶195). As Mr. Guidash explains, threshold voltage control can be provided by the gradient in the doping profile. (Ex. 1002,

¶195). This allows the designer a way to influence threshold voltage that is less coupled to punchthrough voltage. (Ex. 1012, p. 086)(Ex. 1002, ¶195). Such independent control over design parameters is an express goal of Nishi's modulated well. (Ex. 1012, p. 086)(Ex. 1002, ¶195). Furthermore, hot carriers (which can damage the transistor) are controlled by the right-hand slope of the first peak in Fig. 11, because they are aided away from the surface toward the substrate, where they cannot damage the transistor. (Ex. 1002, ¶195). Thus it would have been obvious to arrange the graded dopant profile in order **to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions**. (Ex. 1002, ¶195).

Finally, the technique suggested by Nishi was, in the relevant timeframe, a well-known (indeed, textbook) technique for improving exactly the type of transistors taught by Yamashita, and could have been used in Yamashita with no unpredictable results, and was thus obvious under *KSR*, 550 U.S. 398, 416-21 (2007). (Ex. 1002, ¶196).

B. *Graham* Factors

The Graham factors are the same as discussed under Ground 1, with the exception that the relationship of the prior art to the claims is altered in this Ground.

C. Reasonable Expectation of Success

A POSITA in the relevant timeframe would have had a reasonable expectation

of success in implementing the transistor channel peak (and any other of Nishi's peaks in Fig. 11, as desired). As Mr. Guidash explained, the dopant profiles shown in Nishi were accomplished by ion implantation, which was a standard, predictable technique in the relevant timeframe. (Ex. 1002, ¶198).

D. Analogous Art

Nishi is analogous art because it is in the same field as the '222 patent (semiconductor devices) and as a handbook on manufacturing such devices, would have been highly relevant to the problems purportedly facing the named inventors. (Ex. 1002, ¶199).

E. Claim Mapping

The claim mapping is the same as described in Ground 1, except that the first and second active regions would have one (or more, if desired) additional **at least one graded dopant concentration to aid carrier movement.** (Ex. 1002, ¶200). These graded regions would be the additional peak as discussed above, present in the channels of transistors formed in both the retrograde p-well 8 and retrograde n-well 4. (Ex. 1002, ¶200). This peak is a **graded dopant profile** in each active region, which would have obviously and necessarily been **to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions** (claim limitations [1f] and [21f]), as explained above in the section entitled Rationale (Motivation) Supporting Obviousness. (Ex. 1002,

¶200). The mapping for other elements of the independent or dependent claims does not change. (Ex. 1002, ¶200). In particular, the mapping for claims 9-12 and 28-31 (the language of which pertains to the graded dopant concentration) does not change if the graded region is at shallower depth. (Ex. 1002, ¶200).

Ground 4. Claim 44 was obvious over Kenney

Claim 44 was obvious over U.S. Pat. Pub. 2004/0063288 A1 ("**Kenney**")(Ex. 1010). Kenney is prior art under pre-AIA 35 U.S.C. §§102(a) and (e).

A. Overview and Rationale Supporting Obviousness.

This ground is presented under Greenthread's apparent claim constructions applied in its infringement contentions. Kenney nearly anticipates claim 44, but renders obvious the claim preamble (a CMOS device) and limitation [44g], which requires "at least one well region disposed in the single drift layer." The rationale underlying obviousness will be discussed in the Claim Mapping section, below.

B. Reasonable Expectation of Success

A POSITA in the relevant timeframe would have had a reasonable expectation of success in making the modifications discussed in the claim mapping section. (Ex. 1002, ¶203).

C. Analogous Art

Kenney is analogous art because it is in the same field as the '222 patent

(semiconductor devices) and relevant to the problems purportedly facing the named inventors. (Ex. 1010, Abstract, ¶¶0065-0067)(Ex. 1002, ¶204).

D. Claim Mapping.

CLAIM 44

"44[a]. A CMOS Semiconductor device comprising:"

To the extent the preamble is limiting, Kenney renders obvious a **CMOS semiconductor device**. First, it is clear that Kenney teaches semiconductor devices. (Ex. 1010, ¶¶0004, 0012, 0073)(Ex. 1002, ¶205).

As was well-known in the art, a "CMOS" device was a **C**omplementary **M**etal **O**xide **S**emiconductor device, meaning that it used both p-channel and n-channel transistors (which are complementary to one another). (Ex. 1002, ¶206). Silicon-based CMOS was a widely used technology for many classes of integrated circuits in the relevant timeframe. (Ex. 1002, ¶206).

Kenney renders obvious a CMOS semiconductor device first because it relates to the construction of transistors, and more specifically, both p-channel and n-channel transistors. (Ex. 1010, ¶0012)("In FIG. 1, the semiconductor material in the source and drain regions 101 and 103 are doped with N-type material which is a different type of material than in the region under the gate, thus an NPN MOSFET; however, but device 100 could be a PNP with P-type source and drain and an N-type gate.")(Ex. 1002, ¶207).

Second, Kenney suggests that that its techniques are useful for chips using complementary devices, stating:

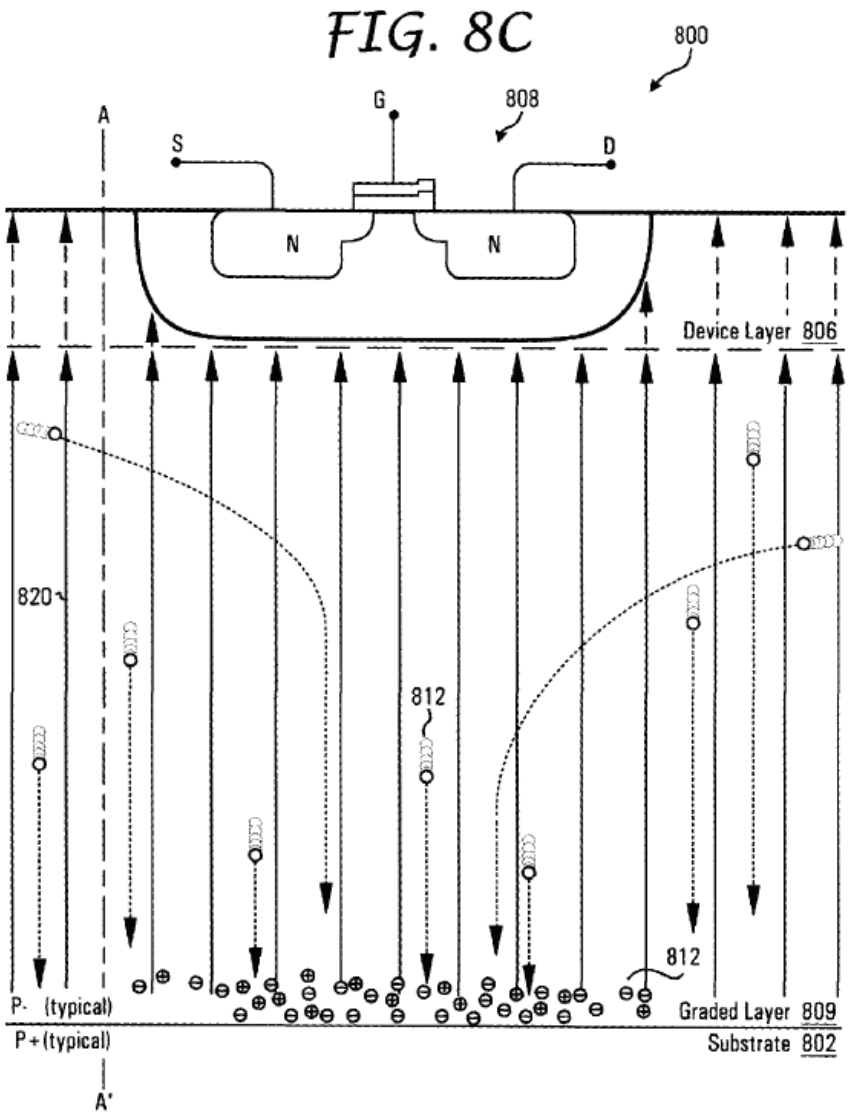
> "[T]he presently described method for fabricating a graded dopant layer for SER reduction is flexible enough to accommodate a wide variety of the device application types and their **complementary** device layer."

(Ex. 1010, ¶0073)(Emphasis added)(Ex. 1002, ¶208).

Because CMOS was a widely-used semiconductor technology in the relevant timeframe involving complementary p-channel and n-channel transistors, because Kenney relates to both p-channel and n-channel transistors, and because Kenney suggests that its techniques "are flexible enough to accommodate a wide variety of the device application types and their complementary device layer", it would have been obvious to a POSITA that Kenney contemplated CMOS semiconductor devices. (Ex. 1002, ¶209).

"[44b] a surface layer;"

Kenney teaches a "surface layer" in the form of a "device layer". The device layer is shown as layer 806 at the top of Fig. 8C of Kenney, reproduced here:



(Ex. 1010, ¶0067, Fig. 8C)(Ex. 1002, ¶210).

Although the device layer is shown as separated from the graded layer 809 below it by a dashed line in Fig. 8C, Kenney makes clear that:

> "…device layer 806 may be defined as a portion of graded layer 809, i.e. the graded portion of the epitaxial layer. Those of ordinary skill in the art will readily understand that a device layer is often merely an extension of, or additional epitaxial layer, comprising materials or electrical properties favorable for the fabrication of a particular class

of device."

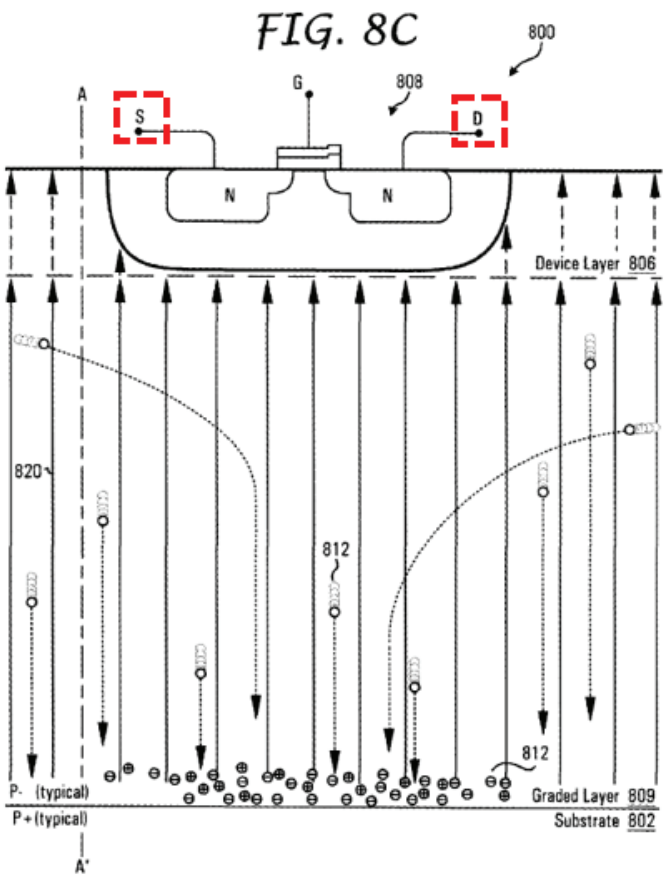
(Ex. 1010, ¶0067)(Ex. 1002, ¶211).

"[44c] a substrate;"

Kenney teaches a substrate (*e.g.*, substrate 802 shown in Fig. 8C, above). (Ex. 1010, ¶0066, Fig. 8C)(Ex. 1002, ¶212).

"[44d] an active region including a source and a drain, disposed on one surface of the surface layer;"

Kenney teaches **an active region including a source and a drain, disposed on one surface of the surface layer.** Figure 8C shows a FET transistor at its top surface with the source labeled "S", and the drain labeled "D". Figure 8C is reproduced here, with added, red-dashed boxes around the labels for the source and drain:



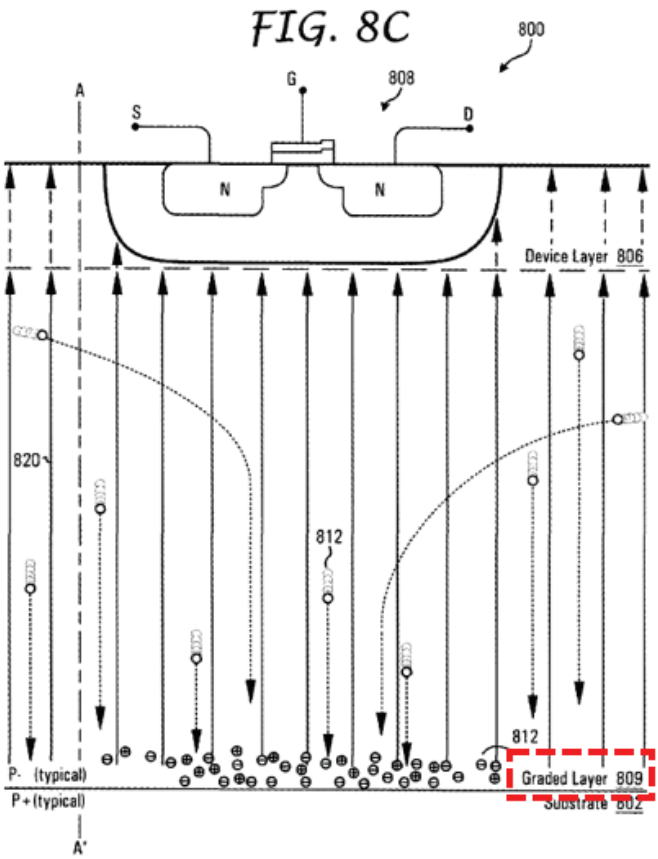
(Ex. 1010, ¶¶0066-0067, 0012)(Ex. 1002, ¶213). The labels for the source and drain are explained with respect to Fig. 1 of Kenney. (Ex. 1010, ¶0012, Fig. 1)(Ex. 1002, ¶213).

As shown in Fig. 8C, the source and drain are **disposed on one surface of the surface layer**. (Ex. 1010, ¶0066-0067, 0012, Figs. 1, 8C)(Ex. 1002, ¶214). The region of the surface on which they are disposed is the **active region** required by the claim. (Ex. 1002, ¶214).

> ***"[44e] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and***

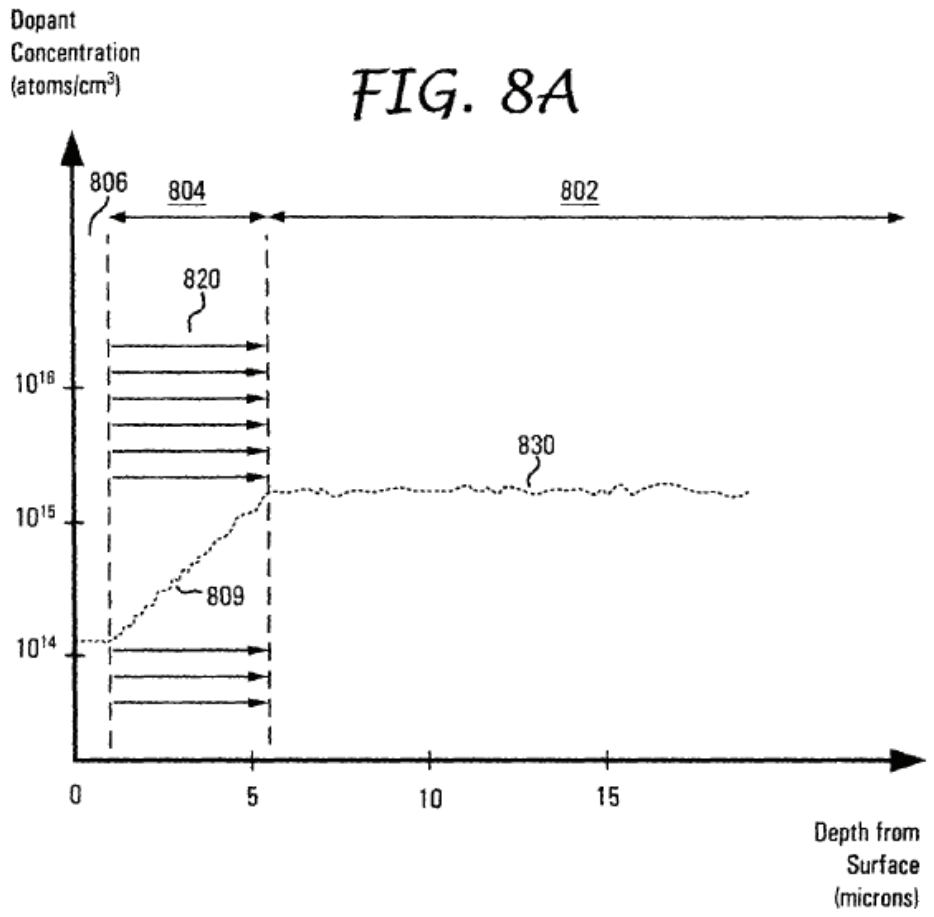
the substrate,"

Kenney teaches **a single drift layer disposed between the other surface of the surface layer and the substrate**, in the form of graded layer 809, as shown in Fig. 8C, reproduced here with an added, red-dashed box around the label Graded Layer 809:



(Ex. 1010, Fig. 8C, ¶¶0066-0067)(Ex. 1002, ¶215). As shown in the Figure, the Graded Layer 809 is situated **between the other surface** (*i.e.*, the bottom surface) **of the surface layer and the substrate** (*i.e.*, substrate 802 below the Graded Layer 809). (Ex. 1010, ¶0066)(Ex. 1002, ¶215).

The Graded Layer 809 (the drift layer) has **a graded concentration of dopants extending between the surface layer and the substrate.** (Ex. 1010, ¶¶0066-0067)("graded layer 809")(Ex. 1002, ¶216). Specifically, the Graded Layer 809 has a graded concentration as shown, for example, in Fig. 8A, reproduced here:



(Ex. 1010, Fig. 8A, ¶0065)(Ex. 1002, ¶216). In Fig. 8A, the dotted line indicates a dopant concentration (vertical axis) as a function of depth from the top surface of the device (horizontal axis). (Ex. 1010, ¶0065)(Ex. 1002, ¶216). As shown by the slope of the dotted line in the region indicated by reference numeral 809, the dopant

profile is graded. (Ex. 1010, ¶¶0065-0066)(Ex. 1002, ¶216). The grading in dopant concentration extends **between the surface layer and the substrate.** (Ex. 1010, Figs. 8A and 8C, ¶¶0065-0067)(Ex. 1002, ¶216). This is also visible from the electric field lines shown Fig. 8C, which indicate the grading. (Ex. 1002, ¶216).

"[44f] the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and"

Kenney teaches that the drift layer has **a first static unidirectional electric drift field.** Kenney states:

> "ε-field 820 is created by, or results from, the gradual concentration changes in dopant across the vertical extent of the epitaxial layer 804. **Electric field 820 traverses the vertical extent of epitaxial layer** from one to six microns in depth rather than merely forming a two-dimensional surface between doped material regions."

(Ex. 1010, ¶0065)(Ex. 1002, ¶217). As shown in both Figs. 8A and 8C, the electric field 820 is **unidirectional**, because it points from the bottom to the top of the device. (Ex. 1010, Figs. 8A and 8C, ¶¶0065-0067)(Ex. 1002, ¶217). The electric field is also plotted in Fig. 8B, showing that the field is unidirectional. (Ex. 1010, ¶0065)(Ex. 1002, ¶217). The field is also **static**, at least because it "is created by, or results from, the gradual concentration changes in dopant across the vertical extent of the epitaxial layer 804." (Ex. 1010, ¶0065)(Ex. 1002, ¶217).

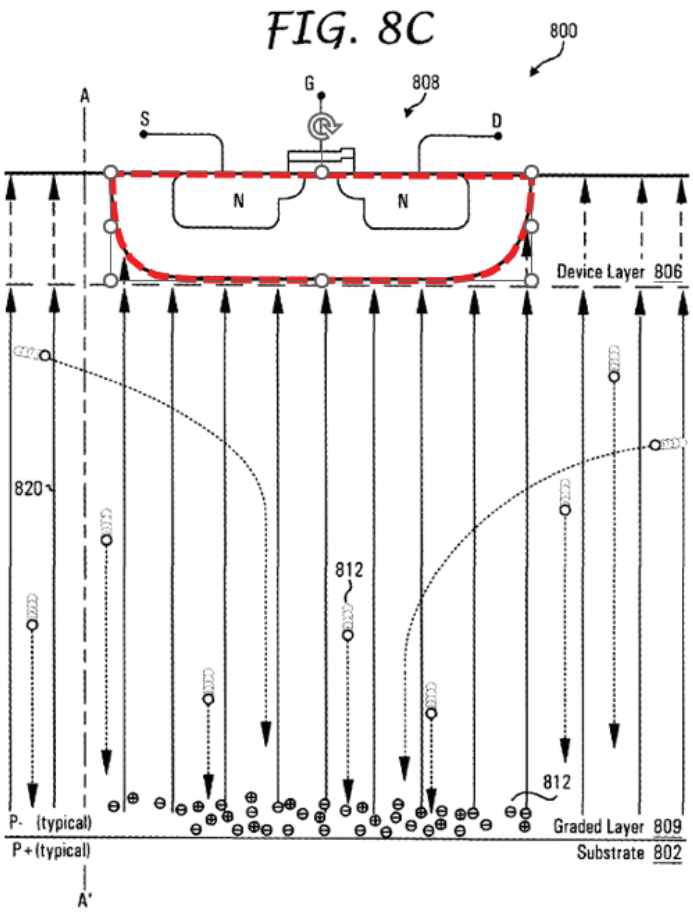
The electric field is a **drift** field, and is **to aid the movement (drift) of carriers from the surface layer to an area of the substrate where there are no active regions**, because it aids negative charges (electrons) to flow from the top of the device to the bottom. Kenney states:

> "Transient charges occurring in epitaxial layer 804 interact with ε-field 820 causing the charges to be swept down, away from active device region 806, toward substrate 802, regardless of where in epitaxial layer 804 the transient charges occur."

(Ex. 1010, ¶0065)(Ex. 1002, ¶218).

"[44g] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions."

Kenney renders this limitation obvious. First, Kenney teaches **well regions**. The well regions consist of both the device layer 806 itself, and the region around the transistor visible in Fig. 8C, reproduced below, with the region around the transistor outlined with an added, red-dashed line:



(Ex. 1010, Fig. 8C, ¶¶0065-0066)(Ex. 1002, ¶219).

Kenney teaches that the regions around active devices such as transistors have special characteristics for forming devices. (Ex. 1010, ¶0067)(Ex. 1002, ¶220). As Mr. Guidash explains, one of the electric properties appropriate for forming transistor channels (the space between the source and drain regions of the transistor, *see* above, element [44d]), was the level of dopant concentration. (Ex. 1010, ¶0067)("Often the device layer is comprised of a different type of semiconducting material than the epitaxial layer, or the same type of semiconducting material as the epitaxial layer, but having different properties, *e.g.*, dopant concentration….")(Ex.

1002, ¶220). Dopant concentration that differed from the substrate was typically, in the prior art, controlled by well formation. (Ex. 1002, ¶220). Thus, A POSITA would have understood and found obvious to use a well region in the device layer 806 and the region in Fig. 8C outlined in red above. (Ex. 1002, ¶220).

Kenney further renders obvious having the well region **disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions**. (Ex. 1002, ¶221). Specifically, Kenney teaches that the graded dopant concentration can extend into the device layer 806, or that the device layer can be part of the graded dopant region. Kenney states:

> "Nonetheless, in accordance with other exemplary embodiments of the present invention **electric field 820 may extend into device layer 806** (depicted in the figure as dashed arrows), or in accordance with still other exemplary embodiments of the present invention, **device 808 may be fabricated entirely within the graded portion** of the epitaxial layer, and thus d**evice layer 806 may be defined as a portion of graded layer 809**, i.e. the graded portion of the epitaxial layer. Those of ordinary skill in the art will readily understand that a device layer is often merely an extension of, or additional epitaxial layer, comprising materials or electrical properties favorable for the fabrication of a particular class of device."

(Ex. 1010, ¶0067)(Emphasis added)(Ex. 1002, ¶221). A POSITA would have understood this teaching to be a recommendation to have a device layer (formed itself by a well or containing a well, as discussed above) in the graded layer 809, and with a graded dopant concentration profile creating **a second static unidirectional electric drift field,** similar to the graded dopant concentration and resultant electric field described above under elements [44e]-[44f] for graded layer 809. A POSITA would have been motivated by the express suggestion of Kenney, quoted above, and by the desire to decrease so-called soft errors, using a gradient that would **aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions**, based on Kenney's express teachings. (Ex. 1010, ¶¶0064-0065)(Ex. 1002, ¶221).

IV. DISCRETIONARY INSTITUTION

A. The Board should not deny the petition under 35 U.S.C. §325(d)

The Board should not exercise its discretion to deny the petition. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte G.m.b.H.*, IPR2019-01469, Paper 6, *8-9 (PTAB Feb. 13, 2020) (precedential).

Three of the principal prior art references, Yamashita, Silverbrook, and Nishi, were not before the Office during the Examination the application leading to the '222 patent. *See id.* While the Kenney reference (the subject of Ground 4) was of

record, it was not examined on the record or discussed. (Ex. 1007). Furthermore, Kenney is asserted in the present petition against only claim 44, and was submitted to the Office together with a large number of other references from a then co-pending litigation concerning related patents. Thus, there is a relatively low degree of overlap between the prior art cited during prosecution and the prior art applied herein, per factors (a) and (b) of *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph). *See Advanced Bionics* at *9, (citing Becton, Dickinson factors).

To the extent the Examiner even considered Kenney when faced with a large number of claims and a large number cited references, the Examiner clearly erred by failing to consider clearly the teachings in Figs. 8C and ¶¶0065-0067 of Kenney, which render obvious claim 44.

Finally, the breadth of the claims in light of the prior art, combined with the strength of the prior art and the additional evidence presented in the petition would "warrant reconsideration of the prior art or arguments". *Becton, Dickinson,* at 17-18.

B. The Board should not deny the petition under 35 U.S.C. §314(a)

Nor should the Board deny the petition under 35 U.S.C. §314(a) in view of the co-pending litigation between Greenthread, Dell, and Intel (hereinafter the "West-Texas Litigation"). *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential)("*Fintiv*").

The *Fintiv* factors weigh in favor of institution, as follows:

***Fintiv* Factor 1** ("*whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*"). None of the parties in the West-Texas Litigation have moved for a stay pending *inter partes* review, and it is unclear whether any party would. This factor is thus neutral.

***Fintiv* Factor 2** ("*proximity of the court's trial date to the Board's projected statutory deadline for a final written decision*"): The trial date in the West-Texas Litigation is only tentatively set for 12/11/23, but the Court expects to revisit that date at the conclusion of the claim construction hearing. (Ex. 1019, p. 3)("[t]he Court expects to set this date [December 11, 2023] at the conclusion of the Markman Hearing"). At least three other *patent* cases have also been assigned the same trial date in the same courtroom before the same judge (Exs. 1021-1023), meaning that the provisional date is unlikely to hold. The district has a median 28.3 months to jury trial in civil cases, which would result in a jury trial in approximately June 2024, approximately concurrent with the Board's likely Final Written Decision in this matter. (Ex. 1020, p. 037). *See Interim Procedure for Discretionary Denials in AIA Postgrant Proceedings with Parallel District Court Litigation*, USPTO, June 21,

2022, p. 8.[2]

This factor thus weighs in favor of institution.

***Fintiv* Factor 3** ("*investment in the parallel proceeding by the court and the parties*"): In the parallel proceeding, discovery has not yet begun (Ex. 1009, p. 2), the parties have begun, but not completed, Markman proceedings, and the parties have not yet filed motions for summary judgment. (Ex. 1019). This factor thus favors institution.

***Fintiv* Factor 4** ("*overlap between issues raised in the petition and in the parallel proceeding*"): Defendants in the West-Texas litigation have asserted a wide variety of prior art in preliminary invalidity contentions, including Yamashita, Nishi and Kenney. However, it is likely that these references would need to be narrowed before trial, and it is thus too early to determine the extent of overlap of any trial. This factor is thus neutral.

***Fintiv* Factor 5** ("*whether the petitioner and the defendant in the parallel proceeding are the same party*"):

While the Dell RPIs are parties to the litigation, the Sony RPIs are not. Moreover, Greenthread made no allegations against Sony Products until April 29,

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[2] https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

2022, several months after filing its action. (Ex. 1015)(Ex. 1016, ¶¶18, 60, 76-81, 102, 110, 118, 126). The Sony RPIs sell accused products to entities other than entities accused in the West-Texas Litigation (*e.g.*, Ex. 1028), and thus have an independent interest in the proceeding. This factor thus weighs in favor of institution.

***Fintiv* Factor 6** ("*other circumstances that impact the Board's exercise of discretion, including the merits*."): The merits of the petition are compelling, and the Board should institute on this basis alone. *See Interim Procedure for Discretionary Denials,* p. 8.

V. CONCLUSION

Petitioner thus respectfully requests that claims 1-44 of the '222 patent be canceled.

Date: December 12, 2022	/Matthew A. Smith/ (RN 49,003) Matthew A. Smith SMITH BALUCH LLP 700 Pennsylvania Ave. SE, 2nd Floor Washington, DC 20003 (202) 669-6207 smith@smithbaluch.com *Counsel for Petitioner*

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing petition for *inter partes* review, together with all exhibits and other documents filed therewith, was served by Priority Mail - Express on December 12, 2022, on the Patent Owner's counsel of record at the United States Patent & Trademark Office having the following address:

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UNITED STATES

Date: December 12, 2022 /Matthew A. Smith/ (RN 49,003)

CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the foregoing petition for *inter partes* review contains 13,976 words according to the word processing program used to prepare it.

Date: December 12, 2022 /Matthew A. Smith/ (RN 49,003)