

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 1:23-cv-00282	DATE FILED 3/14/2023	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF ICPillar LLC		DEFENDANT Arm Ltd. and Arm, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,924,899	12/30/2014	ICPillar LLC
2 9,367,657	6/14/2016	ICPillar LLC
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 1:23-cv-00282	DATE FILED 3/14/2023	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF ICPillar LLC		DEFENDANT Arm Ltd. and Arm, Inc.
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1 8,924,899	12/30/2014	ICPillar LLC
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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK Philip J. Devlin	(BY) DEPUTY CLERK 	DATE 03/15/2023
----------------------------------	---	--------------------

Copy 1—Upon initiation of action, mail this copy to Director. Copy 2—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/901,466	12/30/2014	8924899	101913.0003P	2909

34284 7590 12/10/2014
Rutan & Tucker, LLP.
611 ANTON BLVD
SUITE 1400
COSTA MESA, CA 92626

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Daniel Jakob Seidner, Los Angeles, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/901,466	05/23/2013	Daniel Jakob Seidner	101913.0003P

CONFIRMATION NO. 2909

PUBLICATION NOTICE



OC000000072086210*

34284

Rutan & Tucker, LLP.

611 ANTON BLVD

SUITE 1400

COSTA MESA, CA 92626

Title:SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES

Publication No.US-2014-0351774-A1

Publication Date:11/27/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

RUTAN & TUCKER LLP
611 Anton Boulevard, Suite 1400
Costa Mesa, California 92626

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/901,466	05/23/2013	Daniel Jakob Seidner	101913.0003P	2909

TITLE OF INVENTION: System And Method For Universal Control Of Electronic Devices

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480.00			\$480.00	02/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
Not Yet Assigned	2851	716-102000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- | | |
|---|--------------------|
| 1 | Rutan & Tucker LLP |
| 2 | John K. Fitzgerald |
| 3 | |

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-2191 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☒ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /John K. Fitzgerald/
Typed or printed name John K. Fitzgerald

Date November 21, 2014
Registration No. 38,881

Application No. (if known): 13/901,466

Attorney Docket No.: 101913.0003P

Certificate of Electronic Filing Under 37 C.F.R. § 1.8

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4):

MS Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on November 21, 2014
Date

/John K. Fitzgerald/
Signature



John K. Fitzgerald

Typed or printed name of person signing Certificate

38,881
Registration Number, if applicable

(714) 641-5100
Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

Issue Fee Transmittal (1 page)
Charge \$480.00 to deposit account 50-2191

Electronic Patent Application Fee Transmittal				
Application Number:		13901466		
Filing Date:		23-May-2013		
Title of Invention:		SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		
First Named Inventor/Applicant Name:		Daniel Jakob Seidner		
Filer:		John Kenneth Fitzgerald/Francine Sanders		
Attorney Docket Number:		101913.0003P		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				480

Electronic Acknowledgement Receipt	
EFS ID:	20767727
Application Number:	13901466
International Application Number:	
Confirmation Number:	2909
Title of Invention:	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Daniel Jakob Seidner
Customer Number:	34284
Filer:	John Kenneth Fitzgerald/Francine Sanders
Filer Authorized By:	John Kenneth Fitzgerald
Attorney Docket Number:	101913.0003P
Receipt Date:	21-NOV-2014
Filing Date:	23-MAY-2013
Time Stamp:	14:57:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$480
RAM confirmation Number	1357
Deposit Account	502191
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IssueFee101913-0003P.pdf	65621	no	2
			5c41163fbdd8d6dd360f7997dae69b8851876c		

Warnings:**Information:**

2	Fee Worksheet (SB06)	fee-info.pdf	30578	no	2
			2016f09b2d57a7ce6df396f109f799ff048ae2e1		

Warnings:**Information:**

Total Files Size (in bytes):			96199
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/901,466	05/23/2013	Daniel Jakob Seidner	DSEID-90745

CONFIRMATION NO. 2909

POWER OF ATTORNEY NOTICE

24201
FULWIDER PATTON LLP
HOWARD HUGHES CENTER
6060 CENTER DRIVE, TENTH FLOOR
LOS ANGELES, CA 90045



OC000000071918257*

Date Mailed: 11/20/2014

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/12/2014.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/hachristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/901,466	05/23/2013	Daniel Jakob Seidner	101913.0003P

CONFIRMATION NO. 2909

POA ACCEPTANCE LETTER

34284

Rutan & Tucker, LLP.

611 ANTON BLVD

SUITE 1400

COSTA MESA, CA 92626



OC000000071918278*

Date Mailed: 11/20/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/12/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hachristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Application Number	13/901466		
	Filing Date	May 23, 2013		
	First Named Inventor	Daniel Jakob Seidner		
	Title	System and Method For Universal Control of Electronic Devices		
	Art Unit	2851		
	Examiner Name	Alam, Mohammed		
	Attorney Docket Number	101913.0003P		

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.
OR
☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 34284
OR
☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number	Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number.
OR
☐ The address associated with Customer Number: 34284
OR

☐ Firm or Individual Name

Address

City	State	Zip	
Country			
Telephone	Email		

I am the:

☒ Applicant/Inventor.
OR
☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Applicant or Assignee of Record			
Signature	/ Daniel J. Seidner /	Date	November 12, 2014
Name	Daniel Jakob Seidner	Telephone	310-433-4200
Title and Company	Inventor		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Electronic Acknowledgement Receipt	
EFS ID:	20680429
Application Number:	13901466
International Application Number:	
Confirmation Number:	2909
Title of Invention:	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Daniel Jakob Seidner
Customer Number:	24201
Filer:	John Kenneth Fitzgerald/Francine Sanders
Filer Authorized By:	John Kenneth Fitzgerald
Attorney Docket Number:	DSEID-90745
Receipt Date:	12-NOV-2014
Filing Date:	23-MAY-2013
Time Stamp:	17:55:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA101913-0003P.pdf	38535	no	1
			1f9d01d906a59900de3c901a73b9b4486422fc44		
Warnings:					
Information:					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24201 7590 11/07/2014
FULWIDER PATTON LLP
HOWARD HUGHES CENTER
6060 CENTER DRIVE, TENTH FLOOR
LOS ANGELES, CA 90045

EXAMINER

ALAM, MOHAMMED

ART UNIT

PAPER NUMBER

2851

DATE MAILED: 11/07/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/901,466	05/23/2013	Daniel Jakob Seidner	DSEID-90745	2909

TITLE OF INVENTION: SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	02/09/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24201 7590 11/07/2014
FULWIDER PATTON LLP
HOWARD HUGHES CENTER
6060 CENTER DRIVE, TENTH FLOOR
LOS ANGELES, CA 90045

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/901,466	05/23/2013	Daniel Jakob Seidner	DSEID-90745	2909

TITLE OF INVENTION: SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	02/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
ALAM, MOHAMMED	2851	716-102000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/901,466	05/23/2013	Daniel Jakob Seidner	DSEID-90745	2909
24201 7590 11/07/2014				
FULWIDER PATTON LLP HOWARD HUGHES CENTER 6060 CENTER DRIVE, TENTH FLOOR LOS ANGELES, CA 90045				
EXAMINER ALAM, MOHAMMED				
ART UNIT 2851		PAPER NUMBER		

DATE MAILED: 11/07/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/901,466	Applicant(s) SEIDNER, DANIEL JAKOB	
	Examiner MOHAMMED ALAM	Art Unit 2851	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/28/14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-14. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date <u>10/28/14</u> .	

/MOHAMMED ALAM/ Examiner, Art Unit 2851	/Vuthe Siek/ Primary Examiner, Art Unit 2851
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1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

OFFICE ACTION

App. No.	Office Action Type
13/901466	Allowance

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with:

John K. Fitzgerald on 10/28/14.

AMENDMENTS TO THE CLAIMS

The Application has been amended as follows:

- i. In claim 1, line 10, after "the processor", delete "an" and insert in place "of".
- ii. In claim 8, line 5, after "of a device", delete:

-“; provide [[an IC]] a hardware integrated circuit design based on the selection of input and output characteristics of the device; and

provide software programming commands for controlling the device through the [[IC]] hardware integrated circuit”-- ; and insert in place:

-“into a memory associated with the one or more processors, the logic executed by the one or more processors operable to design a hardware integrated circuit design based on the selection of input and output characteristics of the device, the hardware integrated circuit design including a communication bus, and

output software programming commands to executed by the hardware integrated circuit for controlling the device in accordance with the selection of categorized input and output characteristics of the device using a communication protocol compatible with the device through the communication bus of the hardware integrated circuit” --.

iii. In claim 11, line 2, after “status information”, delete:

-“representing an operating state of the device and is configured by the software programming commands to communicate the status information to the controller”--; and insert in place:

-“from the device through the communication bus of the hardware integrated circuit, the status information representing an operating state of the device, and the hardware integrated circuit is configured by the software programming commands to communicate the status information to the controller through the communication bus of the hardware integrated circuit using the compatible communication protocol”--

Reason for Allowance

The following is an examiner's statement of reasons for allowance:

Regarding to the independent claims:

The Applicant argument was found persuasive and the claimed inventions was found novel over prior art of reference in regards to the claimed limitations:

“analyzing by the processor the selection of categorized input and output characteristics of the electronic device;

outputting by the processor of a hardware integrated circuit design based on the selection of input and output characteristics of the device, hardware integrated circuit including a communication bus for communicating with the electronic device; and

outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device through the communication

bus of the hardware integrated circuit using a communication protocol compatible with the electronic device.”

Regarding to the dependent claims:

Claims are found allowable due to their dependence up on already allowed claims and lacking any technical errors.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMED ALAM whose telephone number is (571) 270-1507 and fax number is (571) 270-2507. The examiner can normally be reached on 10AM to 4PM (EST), Monday to Thursday. If attempts to reach the examiner by telephone are unsuccessful, the Examiner’s Supervisor, JACK CHIANG can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mohammed Alam/ Examiner, Art Unit 2825	/VUTHE SIEK/ Primary Examiner, Art Unit 2851
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	230	((programmable configurable) with ((input adj output) IO interfac\$3 port input/output communication)) and (layout pattern) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/01 10:21
L4	46	((programmable configurable) near ((input adj4 output) IO interfac\$3 port input/output communication)) and (layout pattern) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/01 10:27
S1	2	((("6914551" "8271773" "20110145777" "20120317574" "7991606" "20110145777" "20120019371" "20120317574" "8326962" "20120019371" "20100217967" "7991606" "20100217967" "8271773" "6914551" "8326962").PN.) and "716".clas.	US-PGPUB; USPAT	OR	ON	2014/03/11 14:05
S5	149	(design\$3 with (IC chip device semiconductor controller micro? controller)) and ((input output) with (behavior function functionality characteristic) with (electronic with device)) and (software with control\$5 with (device system)) and ((communicat\$3 interfac\$3) with (register identify) with (device system)) and ((command\$3 control\$3) with (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 09:16
S9	8	("6914551" "8271773" "20110145777" "20120317574" "7991606" "20110145777" "20120019371" "20120317574" "8326962" "20120019371" "20100217967" "7991606" "20100217967" "8271773" "6914551" "8326962").PN.	US-PGPUB; USPAT	OR	ON	2014/04/02 11:31
S10	324	(wireless with communication with chip with design\$3)	US-PGPUB; USPAT	OR	ON	2014/04/02 11:34
S13	43	((wireless remote) with communication) same ((chip IC circuit) with design\$3) and (software with control\$5) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))	US-PGPUB; USPAT	OR	ON	2014/04/02 11:38
S14	75	((appliance wireless remote) with (control\$3 communication)) same ((chip IC circuit) with design\$3) and (software	US-PGPUB; USPAT	OR	ON	2014/04/02 11:41

		with control\$5 with (device system controller)) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))				
S15	3	((("6914551" "8271773" "20110145777" "20120317574" "7991606" "20110145777" "20120019371" "20120317574" "8326962" "20120019371" "20100217967" "7991606" "20100217967" "8271773" "6914551" "8326962").PN.) and "716".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 12:42
S17	8	((IC chip semiconductor circuit) with design\$3) same ((categoriz\$3 group\$3 organizing) with (input) with (output) with (characteristic property)) and ((software instruction code program) with (contrlling controlled driven run))	US-PGPUB; USPAT	OR	ON	2014/04/02 12:48
S19	2	(G06F17/50 G06F17/00 G06F17/30).cpc. and ("8346528" "4065997" "5446555" "5541849" "5544066" "5544070" "5628630" "5838584" "5870308" "6031246" "6077308" "6090151" "6128577" "6140602" "6147674" "6169540" "6259963" "6268228" "6285351" "6343369" "6362641" "6397077" "6473888" "6536017" "6539290" "6546297" "6622289" "6662144" "6714828" "6735488" "6743020" "6772035" "6817004" "6838010" "6877142" "6912439" "6957405" "7047505" "7093205" "7139996" "7159982" "7231374" "7260790" "7353469" "7359645" "7363099" "7369970" "7371067" "7386816" "7412296").pn.	US-PGPUB; USPAT	OR	ON	2014/04/02 12:53
S25	18	(designing with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:18
S26	218	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:18
S27	2	(designing with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2014/04/02 13:18

		functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller)) and "716".clas.	EPO; JPO; DERWENT; IBM_TDB			
S28	2	(designing with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller)) and ("716".clas. (G06F17/50 G06F17/00 G06F17/30).cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:19
S29	47	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) same ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:23
S30	507	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation automatic automatically software user remote) with (control controlled controlling) with (microcontroller controller chip IC)) same ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:32
S31	52	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) same ((automation automatic automatically software user remote) with (control controlled controlling) with (microcontroller controller chip IC)) same ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:33
S32	0	US20010039190	US-PGPUB; USPAT	OR	ON	2014/04/02 15:22
S33	1	"20010039190"	US-PGPUB; USPAT	OR	ON	2014/04/02 15:22
S34	1	("20010039190").DID. and (design\$3 with (controller circuit IC chip))	US-PGPUB; USPAT	OR	ON	2014/04/02 16:18

S36	71	((design with microcontroller with circuit) and (configurable with (IO input output)) and (schematic layout))	US-PGPUB; USPAT	OR	ON	2014/04/02 16:33
S39	13	((design\$3 with microcontroller with circuit) and (configurable with (IO input adj output)) and (schematic and layout))	US-PGPUB; USPAT	OR	ON	2014/04/02 16:34
S42	2	"20020108006"	US-PGPUB; USPAT	OR	ON	2014/04/02 17:00
S46	102	((design\$3 with (microcontroller micro? controller)) and schematic and layout) and ((programmable configurable) with (input near5 output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:08
S50	29	((design designing) with (microcontroller micro?controller)) and (schematic\$3 same (layout mask pattern)) and ((programmable configurable cusomizable) with (input output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:11
S54	111	((design designing) with (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:15
S55	108	((design designing) with (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3)) and ((control with command) instruction)	US-PGPUB; USPAT	OR	ON	2014/04/02 17:16
S56	23	((design designing) with (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3)) and ((control with command) instruction) and (input with output with (characteristic type category))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:17
S57	512	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near3 (input output IO interfac\$3))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:38
S58	143	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input adj output) IO interfac\$3))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:39
S59	22	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3)) and ((software computer user) near3 (controlled controlling))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:40
S60	2	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3)) and ((software computer user) near3 (controlled controlling)) and	US-PGPUB; USPAT	OR	ON	2014/04/03 08:46

		(communication near3 protocol) and (controller near3 status)				
S61	8	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:55
S63	143	((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator))	US-PGPUB; USPAT	OR	ON	2014/04/03 09:00
S64	73	((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT	OR	ON	2014/04/03 09:00
S65	16	(micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT	OR	ON	2014/04/03 09:03
S79	1	("20090113037".did.) and ((controller device) with (ID status mode signature))	US-PGPUB; USPAT	OR	ON	2014/04/03 16:17
S80	16	(micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/04 10:42

		((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)				
S81	3	((micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and (layout) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/04 10:45
S82	24	((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and (layout) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/04 10:46
S85	2	("20090113037") and (communicate identity ID operating state mode)	US-PGPUB; USPAT	OR	ON	2014/04/05 19:25
S86	37	((micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) same (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) with protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/24 19:56
S87	86	((design designing) near8 (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3))	US-PGPUB; USPAT	OR	ON	2014/10/25 10:42
S88	55	((wireless remote) with communication) same ((chip IC circuit integated?circuit) with design\$3) and (software with control\$5) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))	US-PGPUB; USPAT	OR	ON	2014/10/25 10:59
S90	69	((micro?controller microcontroller) near(design\$3)) and ((programmable configurable) with ((input near3 output) IO interfac\$3)) and ((software computer user) with (controlled controlling))	US-PGPUB; USPAT	OR	ON	2014/10/25 11:26
S91	95	((micro?controller microcontroller circuit chip IC) with (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and	US-PGPUB; USPAT	OR	ON	2014/10/25 12:43

		((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)				
S92	111	(schematic layout) and (design\$3 WITH microcontroller with circuit) and (configurable with (IO input output))	US-PGPUB; USPAT	OR	ON	2014/10/25 13:53
S93	97	(schematic layout) and (design\$3 WITH microcontroller with circuit) and (configurable near8 (IO input output))	US-PGPUB; USPAT	OR	ON	2014/10/25 19:43
S101	140	(design\$3 with (IC chip device semiconductor controller micro? controller)) and ((input with output) with (electronic with device)) and (software with control\$5) and ((communicat\$3 interfac\$3) with (register identify) with (device system)) same ((command\$3 control\$3) adj4 (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/25 19:52
S102	54	(design\$3 with (IC chip device semiconductor controller micro? controller)) and ((input with output) near6 (electronic with device)) and (software with control\$5) and ((communicat\$3 interfac\$3) with (register identify) with (device system)) same ((command\$3 control\$3) with (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/25 20:14
S103	69	((wireless remote) with communication) same ((chip IC circuit) with design\$3) and (software same control\$5) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))	US-PGPUB; USPAT	OR	ON	2014/10/25 20:52
S105	77	((IC chip semiconductor circuit) with design\$3) and ((categoriz\$3 group\$3 organizing) with (input) with (output) with (characteristic property)) and ((software instruction code program) same (contrlling controlled driven run))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/25 21:05
S106	129	((IC chip semiconductor circuit) same design\$3) and ((categoriz\$3 group\$3 organizing) with (input) with (output) with (characteristic property)) and ((software instruction code program) same (contrlling controlled driven run))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/25 21:48
S107	82	((micro?controller microcontroller) near (design\$3)) and ((programmable configurable) near ((input adj output) IO interfac\$3))	US-PGPUB; USPAT	OR	ON	2014/10/25 22:33
S108	317	((programmable configurable) same ((input near3 output) IO interfac\$3 port input/output communication)) and (layout) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/26 09:47
S109	93	((programmable configurable) near8	US-PGPUB;	OR	ON	2014/10/26

		((input near3 output) IO interfac\$3 port input/output communication)) and (layout) and (G06F17/50 G06F17/00 G06F17/30).cpc.	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			09:48
S110	45	(schematic layout) and (design\$3 with microcontroller with circuit) and (configurable near (IO input output))	US-PGPUB; USPAT	OR	ON	2014/10/26 13:27
S111	82	(design\$3 with (IC chip device semiconductor controller micro? controller)) and ((input near output) with (electronic with device)) and (software with control\$5) and ((communicat\$3 interfac\$3) with (register identify) with (device system)) same ((command\$3 control\$3) adj4 (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/31 17:14
S112	82	((micro?controller microcontroller) near (design\$3)) and ((programmable configurable) near ((input adj output) IO interfac\$3))	US-PGPUB; USPAT	OR	ON	2014/10/31 17:38
S114	118	(schematic layout pattern) and (design\$3 with microcontroller with circuit) and (configurable with (IO input output))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/31 20:17
S115	69	((wireless remote) with communication) same ((chip IC circuit integated?circuit) with design\$3) and (software same control\$5) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))	US-PGPUB; USPAT	OR	ON	2014/10/31 22:03

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S83	16	(micro?controller microcontroller) and ((micro? controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/04 10:43
S84	2	(selection with categorized with characteristics) and (software with controlling with device)	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/04 10:44

11/ 1/ 2014 10:28:11 AM

C:\Users\malam3\Documents\EAST\Workspaces\182_13901466_SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES.wsp

Issue Classification 	Application/Control No. 13901466	Applicant(s)/Patent Under Reexamination SEIDNER, DANIEL JAKOB
	Examiner MOHAMMED ALAM	Art Unit 2851

☐ Claims renumbered in the same order as presented by applicant																☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original						
1	1		17																		
2	2		18																		
3	3		19																		
4	4		20																		
5	5																				
6	6																				
7	7																				
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9	9																				
10	10																				
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12	12																				
13	13																				
14	14																				
	15																				
	16																				

/MOHAMMED ALAM/ Examiner.Art Unit 2851 (Assistant Examiner)	11/01/2014 (Date)	Total Claims Allowed: 14	
/VUTHE SIEK/ Primary Examiner.Art Unit 2851 (Primary Examiner)	11/03/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 10

Search Notes 	Application/Control No. 13901466	Applicant(s)/Patent Under Reexamination SEIDNER, DANIEL JAKOB
	Examiner MOHAMMED ALAM	Art Unit 2851

CPC- SEARCHED		
Symbol	Date	Examiner
G06F17/30, G06F17/50	4/4/2014	/MA/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
716	102	4/4/2014	/MA/

SEARCH NOTES		
Search Notes	Date	Examiner
Plus Search	4/3/2014	/MA/
Google Search	4/3/2014	/MA/
EAST Search	4/3/2014	/MA/
East	10/30/2014	/MA/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
716	102	4/3/2014	/MA/

/M.A./ Examiner.Art Unit 2851	
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BIB DATA SHEET

CONFIRMATION NO. 2909

SERIAL NUMBER 13/901,466	FILING or 371(c) DATE 05/23/2013 RULE	CLASS 716	GROUP ART UNIT 2851	ATTORNEY DOCKET NO. DSEID-90745		
APPLICANTS INVENTORS Daniel Jakob Seidner, Los Angeles, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 06/15/2013						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/MOHAMMED ALAM/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS FULWIDER PATTON LLP HOWARD HUGHES CENTER 6060 CENTER DRIVE, TENTH FLOOR LOS ANGELES, CA 90045 UNITED STATES						
TITLE SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES						
FILING FEE RECEIVED 730	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

<i>Index of Claims</i> 	Application/Control No. 13901466	Applicant(s)/Patent Under Reexamination SEIDNER, DANIEL JAKOB
	Examiner MOHAMMED ALAM	Art Unit 2851

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	04/04/2014	10/30/2014												
1	1	✓	=												
2	2	✓	=												
3	3	✓	=												
4	4	✓	=												
5	5	✓	=												
6	6	✓	=												
7	7	✓	=												
8	8	✓	=												
9	9	✓	=												
10	10	✓	=												
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	15	✓	-												
	16	✓	-												
	17	✓	-												
	18	✓	-												
	19	✓	-												
	20	✓	-												

EFS-WEB TRANSMISSION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 13/901,466 Confirmation No. : 2909
Applicant : Daniel Jakob Seidner
Filed : 05/23/2013
Title : UNIVERSAL CONTROL ARCHITECTURE
Art Unit : 2851
Examiner : Mohammed Alam
Docket No. : DSEID-90745
Customer No. : 24201

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Sir:

This Amendment is responsive to the Office action of April 11, 2014, the response for which is due July 11, 2014.

Applicant herewith petitions the Director of the United States Patent and Trademark Office to extend the time for reply to the Office Action dated April 11, 2014 for 1 month from July 11, 2014 to August 11, 2014. The extension fees will be paid by credit card with this Electronic Transmission.

Amendments to the Claims begin on page 2

Remarks/Arguments begin on page 5.

AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A computer implemented method for designing [[an IC]] an integrated circuit which controls a device when the integrated circuit integrated into the device comprising:

receiving a selection of categorized input and output characteristics of [[the]] an electronic device into a memory of a processor programmed by software commands to design a hardware integrated circuit and associated operating software for controlling the integrated circuit to control the electronic device;

analyzing by the processor the selection of categorized input and output characteristics of the electronic device;

providing outputting by the processor an [[IC]] a hardware integrated circuit design based on the selection of input and output characteristics of the device; and

providing outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device through an IC based on the IC design.

2. (Currently Amended) The method of claim 1, wherein providing outputting software for controlling the device includes providing a user interface and virtual controls for a controller which allows for controlling the device through the [[IC]] hardware integrated circuit.

3. (Original) The method of claim 2, wherein the user interface is based on the selection of input and output characteristics.

4. (Currently Amended) The method of claim 1, wherein the [[IC]] hardware integrated circuit allows for status input from the device and is capable of reporting the status to a controller.

5. (Currently Amended) The method of claim 1, wherein the [[IC]] hardware integrated circuit design is based on at least one predetermined [[IC]] hardware integrated circuit component which is able to control one of the input or output characteristics.

6. (Currently Amended) The method of claim 5, wherein the [[IC]] hardware integrated circuit design is provided as a software schematic, layout, or both.

7. (Currently Amended) The method of claim 1, wherein the [[IC]] hardware integrated circuit is configured by the software programming commands to communicate an identity and an operating state of the device to a controller and wherein the controller is configured to register the identity of the device, and based on the identity of the device, communicate control commands to the device to alter the operating state of the device.

8. (Currently Amended) A system comprising:

one or more processors;

logic encoded in one or more non-transitory computer-readable media that, when executed by the one or more processors, is operable to:

receive a selection of categorized input and output characteristics of a device;

provide [[an IC]] a hardware integrated circuit design based on the selection of input and output characteristics of the device; and

provide software programming commands for controlling the device through the [[IC]] hardware integrated circuit .

9. (Currently Amended) The system of claim 8, wherein the provided [[IC]] hardware integrated circuit design includes:

a user interface for communicating with a controller which provides a virtual control for the device through the [[IC]] hardware integrated circuit .

10. (Original) The system of claim 9, wherein the user interface is based on the selection of input and output characteristics.

11. (Currently Amended) The system of claim 9, wherein the [[IC]] hardware integrated circuit includes an input for receiving status information representing an operating state of the device and is configured by the software programming commands to communicate the status information to the controller.

12. (Currently Amended) The system of claim 9, wherein the [[IC]] hardware integrated circuit design is based on at least one predetermined [[IC]] hardware integrated circuit component which is able to control one of the input or output characteristics.

13. (Currently Amended) The system of claim 12, wherein the [[IC]] hardware integrated circuit design is provided as a software schematic, layout, or both.

14. (Currently Amended) The system of claim 8, wherein the one or more non-transitory computer-readable media further comprises logic that, when executed by the one or more processors, is further operable to~~[[:]]~~ simulate the [[IC]] hardware integrated circuit's functionality based on the [[IC]] hardware integrated circuit design.

15-20. Canceled

REMARKS/ARGUMENTS

Applicants have carefully reviewed the arguments presented in the Office Action and respectfully request entry of the amendment and reconsideration of the claims in view of the remarks presented below.

Claims 1-2, 4-9 and 11-14 have been amended and claims 15-20 were canceled without prejudice. Thus, claims 1-14 are pending in the application. No new matter was added.

Rejections under 35 U.S.C. § 101

Claims 1-7 and 15-20 were rejected as being directed to non-statutory subject matter. Specifically, the Examiner states that the claims are claiming an abstract idea and/or statement(s) of concept, based on the Examiner's position that the claims recite steps that have no recitation of a machine or transformation. Applicant respectfully traverses these rejections.

The Examiner appears to be applying a strict "machine or transformation" test to determine eligible subject matter. Even under Bilsky v. Kappos, 561 US 2010, this is incorrect. The Supreme Court held that "machine or transformation" is just one factor to be considered, not the only factor used to determine patent eligibility.

Even under the recent holding of Alice v. CLS Bank, and the guidance issued by the USPTO on June 25, 2014, the rejection is still incorrect. First, there is no identification of what the abstract idea is that the claims are directed to, and second, there is no analysis as to whether the elements of the claim, taken alone or in combination, are sufficient to ensure that the claim amount to significantly more than the abstract idea itself.

Applicant has amended claim 1 to recite that a selection of categorized input and output characteristics of an electronic device are received into a memory of a processor programmed by software commands to design a hardware integrated circuit and associated operating software for controlling the integrated circuit to control the electronic device. Claim 1 was also amended to recite that the processor outputs both a hardware integrated circuit design based on the received characteristics, and software programming commands to be executed by the hardware integrated

circuit for controlling the electronic device in accordance with the received characteristics. Independent claim 8 was similarly amended.

Applicant submits that the claims are directed to eligible subject matter in that they are not directed to an abstract idea. The claims are not directed to fundamental economic practices nor methods of organizing human activities. Nor are they directed laws of nature or natural phenomena.

Rather, the claims are directed to producing and output based on certain inputs, using a processor that is programmed to do so. The claims are eligible even under the "machine or transformation" test, because the processor transforms certain received characteristics into both hardware and software programming commands to be executed by the software.

This is significantly more than a mere instruction to apply an abstract idea (which has never been identified), it is significantly more than merely using a generic computer to perform functions that are well-understood, routine or conventional activities previously known in the industry.

Accordingly, Applicant respectfully requests that the rejections under 35 U.S.C. § 101 be withdrawn and that amended claims 1-14 be allowed.

Rejections under AIA 35 U.S.C. § 102(a)(1)

Claims 1-20 were rejected as being anticipated by Pouchak (US Pub. No. 2009/0113037). Applicant respectfully traverses these rejections.

It is axiomatic that, for a reference to anticipate a claim, the reference must show each and every element of the claim arranged as in the claim. Pouchak fails to satisfy this test.

As stated above, independent claim 1 has been amended recite that a selection of categorized input and output characteristics of an electronic device are received into a memory of a processor programmed by software commands to design a hardware integrated circuit and associated operating software for controlling the integrated circuit to control the electronic device. Claim 1 was also amended to recite that the processor outputs both a hardware integrated circuit design based on the received characteristics, and software programming

commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the received characteristics. Independent claim 8 was similarly amended.

In contrast, Pouchak only teaches a software system that can be used to develop software operating commands on a computer, and to use that computer to simulate how the software will operate when applied to control an HVAC system. While Pouchak does discuss various "modules" and "blocks", those modules and blocks are no more than software programs; they are not hardware integrated circuits or designs. Indeed, Pouchak describes designing "circuits", but those "circuits" are not hardware circuits, but rather simulations of a collection of hardware components, the virtual nature of which are then used to test the software "blocks" and "modules" to determine if the software works.

Nowhere does Pouchak even suggest outputting a hardware integrated circuit and software programming to be executed on the hardware integrated circuit to control an electronic device in accordance with a selected set of input and output characteristics of the electronic device, as is claimed in amended claims 1 and 8.

Moreover, since Pouchak fails to teach each and every element of claims 1 and 8, as amended, Pouchak also fails to render those claims obvious, as absence of an element is strong evidence of non-obviousness. No would one skilled in the art, using nothing more than common knowledge or common sense be able to obtain the inventions of amended claim 1 and 8, as Pouchak provides nothing more than a process for developing and testing software, and mentions nothing related to designing a hardware integrated circuit.

For all of the reasons set forth above, Applicant respectfully submits that independent claims 1 and 8 as amended are patentable over the cited art. Thus, Applicant requests that the rejections be withdrawn and that amended independent claims 1 and 8, and the claims dependent therefrom, be allowed.

CONCLUSION

Applicant has carefully reviewed the arguments presented in the Office Action and respectfully requests entry of the amendment and reconsideration of the claims in view of the remarks presented. In light of the above amendments and remarks, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Should the Examiner have any questions concerning the above amendments and arguments, or any suggestions for further amending the claims to obtain allowance, Applicant requests that the Examiner contact Applicant's attorney, John K. Fitzgerald, at (310) 242-2667.

The Commissioner is authorized to charge any additional fees or credit any overpayment in this matter to our Deposit Account No. 06-2425.

Date: August 11, 2014

Respectfully submitted,

FULWIDER PATTON LLP

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John K. Fitzgerald
Registration No. 38,881

Howard Hughes Center
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Los Angeles, CA 90045
Telephone: (310) 824-5555
Facsimile: (310) 824-9696

Electronic Patent Application Fee Transmittal				
Application Number:		13901466		
Filing Date:		23-May-2013		
Title of Invention:		SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		
First Named Inventor/Applicant Name:		Daniel Jakob Seidner		
Filer:		John Kenneth Fitzgerald/Joanna Morris		
Attorney Docket Number:		DSEID-90745		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt	
EFS ID:	19836378
Application Number:	13901466
International Application Number:	
Confirmation Number:	2909
Title of Invention:	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Daniel Jakob Seidner
Customer Number:	24201
Filer:	John Kenneth Fitzgerald/Joanna Morris
Filer Authorized By:	John Kenneth Fitzgerald
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Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		90745-AMENDMENT-TO- OA-4-11-2014.pdf	40693 b908f0e0a1710f50bbf22c865eb37a872cf1b6a9	yes	8
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	4	
	Applicant Arguments/Remarks Made in an Amendment		5	8	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30331 ddb2ba29959e1684c4e09b847afc7951f7ba590d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			71024		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/901,466		Filing Date 05/23/2013		☐ To be Mailed	
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	08/11/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X \$40 =		0	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$210 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/901,466	05/23/2013	Daniel Jakob Seidner	DSEID-90745	2909
24201 7590 04/11/2014 FULWIDER PATTON LLP HOWARD HUGHES CENTER 6060 CENTER DRIVE, TENTH FLOOR LOS ANGELES, CA 90045			EXAMINER ALAM, MOHAMMED	
			ART UNIT 2851	PAPER NUMBER
			NOTIFICATION DATE 04/11/2014	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketla@fulpat.com
eOfficeAction@fulpat.com

Office Action Summary	Application No. 13/901,466	Applicant(s) SEIDNER, DANIEL JAKOB	
	Examiner MOHAMMED ALAM	Art Unit 2851	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 08/22/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☒ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 05/23/2013 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some** c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 08/22/2013.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

OFFICE ACTION

App. No.	Office Action Type
13/901466	Non-Final (1 st Action)

2. This Office Action responds to the Application filed on 05/23/2013 and IDS filed on 08/22/2013.

Claims 1-20 are pending.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

4. The following claims are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Based upon consideration of all of the relevant factors with respect to the claims as a whole, claims mentioned are held to claiming an abstract idea and/or statement(s) of concept, therefore rejected as ineligible subject matter under 35 U.S.C. 101. The rationale for this finding is explained below:

Claims 1-7, 15-20, recite a series of method (or process) steps including: receiving, providing, reporting, operating, communicating, and etc.; but the steps have no recitation of a machine or transformation (either express or inherent). Thus, the subject matter of claimed invention is non-statutory and not patent eligible.

In view of the decision by the United States Supreme Court in *Bilski v. Kappos*, 561 US 2010 (*Bilski*), the claims mentioned are non-statutory because a § 101 process claim must (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing. If neither of these requirements are met by the claim, the method is not a patent eligible process under § 101. A § 101 process claim that would not qualify as a statutory process would be a claim that recites purely mental step(s) that can be performed manually or merely manipulating an abstract idea without the use of a specific structure. Thus, to qualify as a § 101 statutory process, the claimed step(s) must explicitly recite the other statutory class, i.e., the computer, the structure, the equipment, the thing, to which it is tied, for example by identifying the computer, the processor that accomplishes the step(s) and providing transformation underlying subject matter to a different state or thing.

The examiner acknowledges that the preamble of claim 1 comprises "computer implemented method" and claim 15 comprises "non-transitory computer-readable medium". However, as to MPEP 2106.B, and particularly for factor (a), it does not appear that the computer is performing any steps, instead, it is just used in the implementation somehow.

To qualify as a particular machine under the test, the claim must clearly convey that the computer is programmed to perform the steps of the method because such programming, in effect, creates a special purpose computer limited to the use of the

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particularly claimed combination of elements (i.e., the programmed instructions) performing the particularly claimed combination of functions.

In order to overcome this rejection, (i) at least one or more steps that define the essence of the invention should be meaningfully tied to a particular machine (for example: by a computer or by a processor or as applicable), or (ii) transform underlying subject matter (such as an article or material) to a different state or thing.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

6. Claims 1-20, are rejected under AIA 35 U.S.C. 102(a)(1) as being anticipated by the prior art of record **Pouchak** (US-PGPUB-NO: **US20090113037**).

7. (As to claim 1, **Pouchak** discloses):

A computer implemented method for **designing an IC** which **controls a device when integrated into the device** comprising [refer to "**designing circuit**", in Para. 4, in conjunction with Fig. 12, where a **microcontroller (111)** integrated to control other device (interface 112-123 for connecting other devices)]:

receiving **a selection of categorized input and output characteristics** of the electronic device [refer to Fig. 11 depicting selection of **categorized (84- 86, 87-91)** IO types having **different characteristics** (resistive, digital and etc.)];

providing an **IC design** based on the selection of **input and output characteristics** of the device [refer to Fig. 10, the IO blocks (622, 623) taking **different IO type for IC design consideration**]; and

providing **software for controlling the device** through an IC based on the IC design [refer to Para. 41 “system to be **controlled**...effectively all in conveyable **software**”; also refer to Fig. 18 depicting software (variables 356) controlling input and output (372, 384) sets].

8. (As to claim 2, **Pouchak** further discloses):

The method of claim 1, wherein providing software for controlling the device includes providing **a user interface** and **virtual controls** for a **controller** which allows for controlling the device through the IC [refer to Para. 41, at “**remote monitoring and control...touch screen, voice command**”, via remote **user interface** (here touch screen, voice command and etc.); also note that as to applicant disclosure in Para. 37, remote control is disclosed as a type of virtual control].

9. (As to claim 3, **Pouchak** further discloses):

The method of claim 2, wherein the **user interface** is based on the **selection of input and output characteristics** [refer to Para. 109 “**user interface** (402)...output...input”; also Fig. 34 depicting user interface information (App Data 835) is based on **IO selection (831)**; meaning IO selection based on their **characteristics**].

10. (As to claim 4, **Pouchak** further discloses):

The method of claim 1, wherein the IC allows for **status input** from the device and is capable of **reporting the status to a controller** [refer to Fig. 32 “nvo_Status” for reporting **status to controller** and “nvi_Request” for **input receiving status** representing the operation status and configure the controller accordingly; also refer to Para. 158 “receive node...sending node” and “**error flag**” whereas the “error flag” of **Pouchak** is functionally equivalent to “reporting status to the controller” of the applicant, since both reports the operating status to the controller].

11. (As to claim 5, **Pouchak** further discloses):

The method of claim 1, wherein the IC design is based on at least one predetermined **IC component** which is able to **control one of the input or output characteristics** [refer to Para. 92 at “**configure input**”, “**configure output**” wherein configuring input and output are based on **predetermined IC component** (IO design is predetermined such as: input, output, analog, digital and etc.) that changes the characteristic of input and output].

12. (As to claim 6, **Pouchak** further discloses):

The method of claim 5, wherein the **IC design** is provided as a software **schematic, layout** or both [refer to Para. 52 at “FIG. 10 shows a portion of the **layout**” and, Para. 71, at “FIG. 17 is a **schematic** diagram” as part of the microcontroller chip (**IC**) design].

13. (As to claim 7, **Pouchak** further discloses):

The method of claim 1, wherein the IC is configured to **communicate an identity** and an **operating state** of the device to a controller and wherein the controller is configured to **register the identity of the device** [refer to Para. 99 at “to **configure** the controller ...**ID number** ... on the controller ... **mark** the controller...”, note that the “ID number” of **Pouchak** is functionally equivalent to “the identity of the device” of the applicant that is utilized to **resister** (configure the controller as of Pouchak) the identity

of the device operating state (mark the controller of **Pouchak**)], and based on the identity of the device, communicate **control commands** to the device **to alter the operating state** of the device [refer to Para. 241 at “**command**” and “controller would **lay out** the entire structure...data following the signature”, wherein “lay out” (or reprogram) is functionally equivalent **to alter the operating state** by reprogramming].

14. (As to claim 8, **Pouchak** further discloses):

A system comprising:

one or more processors [refer to Fig. 30 at “processor”];

logic encoded in one or more non-transitory **computer-readable media** that, when executed by the one or more **processors**, is operable to [refer to Fig. 30, at “stack” (i.e. memory), and “processor”]:

receiving a **selection of categorized input and output characteristics** of a device [refer to Fig. 11 depicting selection of categorized (84- 86, 87-91) IO types having different characteristics (resistive, digital and etc.)];

providing an **IC design** based on the selection of **input and output characteristics** of the device [refer to Fig. 10, the IO blocks (622, 623) taking different IO type for **IC design consideration**]; and

providing **software for controlling the device** through the IC [refer to Para. 41 “system to be controlled...effectively all in conveyable software”; also refer to Fig. 18 depicting software (variables 356) controlling input and output (372, 384) sets].

15. (As to claim 9, **Pouchak** further discloses):

The system of claim 8, wherein the provided IC design includes:

a **user interface** for communicating with a controller which provides a **virtual control** for the device through the IC [refer to Para. 41, at “**remote monitoring and control...touch screen, voice command**”, via remote **user interface** (here touch screen, voice command and etc.); also note that as to applicant disclosure in Para. 37, remote control is disclosed as a type of virtual control].

16. (As to claim 10, **Pouchak** further discloses):

The system of claim 9, wherein the **user interface** is based on the **selection of input and output characteristics** [refer to Para. 109 “**user interface** (402)...output...input”; also Fig. 34 depicting user interface information (App Data 835) is based on **IO selection (831)**; meaning IO selection based on their **characteristics**].

17. (As to claim 11, **Pouchak** discloses):

The system of claim 9, wherein the IC includes an **input for receiving status** information representing an operating state of the device and is configured to **communicate the status information to the controller** [refer to Fig. 32 “**nvo__Status**” for reporting **status to controller** and “**nvi_Request**” for **input receiving status** representing the operation status and configure the controller accordingly; also refer to Para. 158 “receive node...sending node” and “**error flag**” whereas the “error flag” of **Pouchak** is functionally equivalent to “reporting status to the controller” of the applicant, since both reports the operating status to the controller].

18. (As to claim 12, **Pouchak** also discloses):

The system of claim 9, wherein the IC design is based on at least one predetermined **IC component** which is able to **control one of the input or output characteristics** [refer to Para. 92 at “**configure input**”, “**configure output**” wherein configuring input and output are based on predetermined IC component (IO design is predetermined such as: input, output, analog, digital and etc.) that changes the characteristic of input and output].

19. (As to claim 13, **Pouchak** also discloses):

The system of claim 12, wherein the **IC design** is provided as a software **schematic, layout** or both [refer to Para. 52 at “FIG. 10 shows a portion of the **layout**” and, Para. 71, at “FIG. 17 is a **schematic** diagram” as part of the microcontroller chip **(IC) design**].

20. (As to claim 14, **Pouchak** discloses):

The system of claim 8, wherein the one or more non-transitory computer-readable media further comprises logic that, when executed by the one or more processors, is further operable to: **simulate the IC's functionality based on the IC design** [refer to Para. 50, at “**simulate mode**...controller...**designed circuit**” functionally equivalent teaching].

21. (As to claim 15, **Pouchak** discloses):

A non-transitory computer readable medium **storing instruction** that, when executed by a **processor**, perform method comprising [refer to Fig. 30, at “stack” (memory), and “processor”]:

receiving **a selection of categorized input and output characteristics** of the device [refer to Fig. 11 depicting selection of **categorized (84- 86, 87-91)** IO types having **different characteristics** (resistive, digital and etc.)];

providing an **IC design** based on the selection of **input and output characteristics** of the device [refer to Fig. 10, the IO blocks (622, 623) taking **different IO type for IC design consideration**]; and

providing **software for controlling the device** through the IC [refer to Para. 41 “system to be **controlled**...effectively all in conveyable **software**”; also refer to Fig. 18 depicting software (variables 356) controlling input and output (372, 384) sets].

22. (As to claim 16, **Pouchak** discloses):

The method of claim 15, further comprising:

communicating a **user interface** to a **remote controller** which provides a **virtual control** for the device through the IC [refer to Para. 41, at “**remote monitoring and control...touch screen, voice command**”, via remote **user interface** (here touch screen, voice command and etc.); also note that as to applicant disclosure in Para. 37, remote control is disclosed as a type of virtual control].

23. (As to claim 17, **Pouchak** discloses):

The method of claim 16, wherein the **user interface** is based on the **selection of input and output characteristics** [refer to Para. 109 “**user interface** (402)...output...input”; also Fig. 34 depicting user interface information (App Data 835) is based on **IO selection (831)**; meaning IO selection based on their **characteristics**].

24. (As to claim 18, **Pouchak** discloses):

The method of claim 15, wherein the IC allows for **status input** from the device and is capable of **reporting the status to a controller** [refer to Fig. 32 “**nvo_Status**” for reporting **status to controller** and “**nvi_Request**” for **input receiving status** representing the operation status and configure the controller accordingly; also refer to Para. 158 “receive node...sending node” and “**error flag**” whereas the “error flag” of **Pouchak** is functionally equivalent to “reporting status to the controller” of the applicant, since both reports the operating status to the controller].

25. (As to claim 19, **Pouchak** also discloses):

The method of claim 15, wherein the IC design is based on at least one predetermined **IC component** which is able to **control one of the input or output characteristics** [refer to Para. 92 at “**configure input**”, “**configure output**” wherein configuring input and output are based on predetermined IC component (IO design is

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predetermined such as: input, output, analog, digital and etc.) that changes the characteristic of input and output].

26. (As to claim 20, **Pouchak** discloses):

The method of claim 19, wherein the IC design is provided as a software schematic, layout, or both [refer to Para. 52 at “FIG. 10 shows a portion of the **layout**” and, Para. 71, at “FIG. 17 is a **schematic** diagram” as part of the microcontroller chip **(IC) design**].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMED ALAM whose telephone number is (571) 270-1507, email address mohammed.alam@uspto.gov and fax number (571) 270-2507. The examiner can normally be reached on 10AM to 4PM (EST), Monday to Thursday. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, JACK CHIANG can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mohammed Alam/ Examiner, Art Unit 2825	
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Notice of References Cited	Application/Control No. 13/901,466	Applicant(s)/Patent Under Reexamination SEIDNER, DANIEL JAKOB	
	Examiner MOHAMMED ALAM	Art Unit 2851	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2001/0039190 A1	11-2001	Bhatnagar, Rajiv	455/450
*	B	US-2002/0108006 A1	08-2002	Snyder, Warren	710/100
*	C	US-2009/0113037 A1	04-2009	Pouchak, Michael A.	709/224
*	D	US-2011/0260752 A1	10-2011	Jouin et al.	326/41
*	E	US-8,555,032 B2	10-2013	Snyder, Warren	712/32
	F	US-			
	G	US-			
	H	US-			
	I	US-			
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	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	((micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/04 10:42
L5	3	((micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and (layout) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/04 10:45
L6	24	((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and (layout) and (G06F17/50 G06F17/00 G06F17/30).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/04 10:46
S1	2	((("6914551" "8271773" "20110145777" "20120317574" "7991606" "20110145777" "20120019371" "20120317574" "8326962" "20120019371" "20100217967" "7991606" "20100217967" "8271773" "6914551" "8326962").PN.) and "716".clas.	US-PGPUB; USPAT	OR	ON	2014/03/11 14:05
S4	942	(design\$3 with (IC chip device semiconductor controller micro?controller)) and ((input with output) same (electronic with device)) and (software with control\$5) and ((communicat\$3 interfac\$3) with (register identify) with (device system)) and ((command\$3 control\$3) with (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 09:14
S5	149	(design\$3 with (IC chip device semiconductor controller micro?controller)) and ((input output) with (behavior function functionality characteristic) with (electronic with device)) and (software with control\$5 with (device system)) and ((communicat\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/04/02 09:16

		interfac\$3) with (register identify) with (device system)) and ((command\$3 control\$3) with (device system))	IBM_TDB			
S6	28	(design\$3 with (IC chip device semiconductor controller micro?controller)) and ((input output) with (behavior function functionality characteristic) with (electronic with device)) and (software with control\$5 with (device system)) and ((communicat\$3 interfac\$3) with (register identify) with (controller)) and ((command\$3 control\$3) with (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 09:17
S7	16	(design\$3 with (IC semiconductor device) with (controller micro?controller)) and ((input output) with (behavior function functionality characteristic) with (electronic with device)) and (software with control\$5 with (device system)) and ((communicat\$3 interfac\$3) with (register identify) with (controller)) and ((command\$3 control\$3) with (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 09:25
S8	1	(design\$3 with (IC circuit chip (integrated adj circuit) (semiconductor adj device)) with (controller micro?controller)) and ((input adj5 output) with (behavior function functionality characteristic) with (electronic adj5 device)) and (software with control\$5 with (device system)) and ((communicat\$3 interfac\$3) with (register) with (controller microcontroller micro?controller)) and ((command\$3 control\$3) with (device system))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 11:28
S9	8	("6914551" "8271773" "20110145777" "20120317574" "7991606" "20110145777" "20120019371" "20120317574" "8326962" "20120019371" "20100217967" "7991606" "20100217967" "8271773" "6914551" "8326962").PN.	US-PGPUB; USPAT	OR	ON	2014/04/02 11:31
S10	324	(wireless with communication with chip with design\$3)	US-PGPUB; USPAT	OR	ON	2014/04/02 11:34
S13	43	((wireless remote) with communication) same ((chip IC circuit) with design\$3) and (software with control\$5) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))	US-PGPUB; USPAT	OR	ON	2014/04/02 11:38
S14	75	((appliance wireless remote) with (control\$3 communication)) same ((chip IC circuit) with design\$3) and (software with control\$5 with (device system controller)) and ((group\$3 category categorized) same (input with output) same (feature behavior characteristics))	US-PGPUB; USPAT	OR	ON	2014/04/02 11:41
S15	3	((("6914551" "8271773" "20110145777" "20120317574" "7991606" "20110145777" "20120019371" "20120317574" "8326962" "20120019371" "20100217967" "7991606" "20100217967" "8271773" "6914551" "8326962").PN.) and	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 12:42

		"716".clas.				
S17	8	((IC chip semiconductor circuit) with design\$3 same ((categoriz\$3 group\$3 organizing) with (input) with (output) with (characteristic property)) and ((software instruction code program) with (contrlling controlled driven run))	US-PGPUB; USPAT	OR	ON	2014/04/02 12:48
S19	2	(G06F17/50 G06F17/00 G06F17/30).qpc. and ("8346528" "4065997" "5446555" "5541849" "5544066" "5544070" "5628630" "5838584" "5870308" "6031246" "6077308" "6090151" "6128577" "6140602" "6147674" "6169540" "6259963" "6268228" "6285351" "6343369" "6362641" "6397077" "6473888" "6536017" "6539290" "6546297" "6622289" "6662144" "6714828" "6735488" "6743020" "6772035" "6817004" "6838010" "6877142" "6912439" "6957405" "7047505" "7093205" "7139996" "7159982" "7231374" "7260790" "7353469" "7359645" "7363099" "7369970" "7371067" "7386816" "7412296").pn.	US-PGPUB; USPAT	OR	ON	2014/04/02 12:53
S25	18	(designing with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:18
S26	218	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:18
S27	2	(designing with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller)) and "716".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:18
S28	2	(designing with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:19

		controlling) with (microcontroller chip IC)) and ((communicat\$3 interfac\$3) with (controller microcontroller)) and ("716".clas. (G06F17/50 G06F17/00 G06F17/30).cpc.)				
S29	47	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation software user remote) with (control controlled controlling) with (microcontroller chip IC)) same ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:23
S30	507	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) and ((automation automatic automatically software user remote) with (control controlled controlling) with (microcontroller controller chip IC)) same ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:32
S31	52	(design\$3 with (IC chip circuit semiconductor)) and ((group\$3 categorizing organizing) with (input output port interface) with (type function functionality operation behavior characteristics)) same ((automation automatic automatically software user remote) with (control controlled controlling) with (microcontroller controller chip IC)) same ((communicat\$3 interfac\$3) with (controller microcontroller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 13:33
S32	0	US20010039190	US-PGPUB; USPAT	OR	ON	2014/04/02 15:22
S33	1	"20010039190"	US-PGPUB; USPAT	OR	ON	2014/04/02 15:22
S34	1	("20010039190").DID. and (design\$3 with (controller circuit IC chip))	US-PGPUB; USPAT	OR	ON	2014/04/02 16:18
S36	71	(design with microcontroller with circuit) and (configurable with (IO input output)) and (schematic layout)	US-PGPUB; USPAT	OR	ON	2014/04/02 16:33
S39	13	(design\$3 with microcontroller with circuit) and (configurable with (IO input adj output)) and (schematic and layout)	US-PGPUB; USPAT	OR	ON	2014/04/02 16:34
S40	2	(design\$3 with microcontroller with circuit) and (configurable with (IO input adj output)) same ((design\$3) with (input parameter))and (schematic and layout)	US-PGPUB; USPAT	OR	ON	2014/04/02 16:42
S41	2	(microcontroller with design\$3 with (automation EDA tool)) and ((configurable programmable) with (input adj output)) same ((design\$3) with (input parameter))and (schematic and layout)	US-PGPUB; USPAT	OR	ON	2014/04/02 16:57
S42	2	"20020108006"	US-PGPUB; USPAT	OR	ON	2014/04/02 17:00

S46	102	((design\$3 with (microcontroller micro? controller)) and schematic and layout) and ((programmable configurable) with (input near5 output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:08
S47	5	((design\$3 with (microcontroller micro? controller)) and (schematic same layout)) and ((programmable configurable) with (input near5 output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:08
S48	4	((design designing) with (microcontroller micro?controller)) and (schematic same layout)) and ((programmable configurable) with (input near5 output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:09
S49	4	((design designing) with (microcontroller micro?controller)) and (schematic same layout) and ((programmable configurable) with (input near5 output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:10
S50	29	((design designing) with (microcontroller micro?controller)) and (schematic\$3 same (layout mask pattern)) and ((programmable configurable customizable) with (input output)) and ((software code automation auto automatically automatic) with (control controlling))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:11
S54	111	((design designing) with (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:15
S55	108	((design designing) with (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3)) and ((control with command) instruction)	US-PGPUB; USPAT	OR	ON	2014/04/02 17:16
S56	23	((design designing) with (microcontroller micro?controller)) and ((programmable configurable) with (input interface)) and ((software) with (control controlling controlled)) and (status with (bit report\$3)) and ((control with command) instruction) and (input with output with (characteristic type category))	US-PGPUB; USPAT	OR	ON	2014/04/02 17:17
S57	512	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near3 (input output IO interfac\$3))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:38
S58	143	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input adj output) IO interfac\$3))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:39
S59	22	((micro?controller microcontroller) near3	US-PGPUB; USPAT	OR	ON	2014/04/03

		((design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3)) and ((software computer user) near3 (controlled controlling))	USPAT			08:40
S60	2	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3)) and ((software computer user) near3 (controlled controlling)) and ((communication near3 protocol) and (controller near3 status))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:46
S61	8	((micro?controller microcontroller) near3 (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator))	US-PGPUB; USPAT	OR	ON	2014/04/03 08:55
S63	143	((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator))	US-PGPUB; USPAT	OR	ON	2014/04/03 09:00
S64	73	((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT	OR	ON	2014/04/03 09:00
S65	16	((micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and ((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT	OR	ON	2014/04/03 09:03
S79	1	("20090113037".did.) and ((controller	US-PGPUB;	OR	ON	2014/04/03

		device) with (ID status mode signature))	USPAT			16:17
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EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	16	(micro?controller microcontroller) and ((micro?controller microcontroller circuit chip IC) near (design\$3)) and ((programmable configurable) near ((input near3 output) IO interfac\$3 port input/output communication)) and ((software computer user) near3 (controlled controlling)) and ((communication interfac\$3 interconnect control controlling) near3 protocol) and (((controller communication interfac\$3 interconnect control controlling) with (status indicator)) and (schematic) and (layout)	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/04 10:43
L3	2	(selection with categorized with characteristics) and (software with controlling with device)	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/04 10:44

4/ 4/ 2014 10:48:55 AM

C:\ Users\ malam3\ Documents\ EAST\ Workspaces\ 182_13901466_SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES.wsp

Receipt date: 08/22/2013

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13901466	
	Filing Date		2013-05-23	
	First Named Inventor	Daniel Jakob Seidner		
	Art Unit	~~2484~~ 2851		
	Examiner Name	/Mohammed Alam/		
	Attorney Docket Number	DSEID-90745		

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8326962	B2	2012-12-04	Lo	
	2	8271773	B2	2012-09-18	Grittke et al.	
	3	7991606	B1	2011-08-02	D'Souza et al.	
	4	6914551	B2	2005-07-05	Vidal	
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	1	20120317574	A1	2012-12-13	Eckardt	
	2	20120019371	A1	2012-01-26	Vidal	

Receipt date: 08/22/2013 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13901466	
	Filing Date		2013-05-23	
	First Named Inventor	Daniel Jakob Seidner		
	Art Unit	2184		
	Examiner Name	/Mohammed Alam/		
	Attorney Docket Number	DSEID-90745		

	3	20110145777	A1	2011-06-16	Iyer et al.	
	4	20100217967	A1	2010-08-26	Viswanathan et al.	

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EXAMINER SIGNATURE			
Examiner Signature	/Mohammed Alam/	Date Considered	04/04/2014

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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Receipt date: 08/22/2013 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13901466
	Filing Date		2013-05-23
	First Named Inventor	Daniel Jakob Seidner	
	Art Unit	2184	
	Examiner Name	/Mohammed Alam/	
	Attorney Docket Number	DSEID-90745	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/john k. fitzgerald/	Date (YYYY-MM-DD)	2013-08-22
Name/Print	John K. Fitzgerald	Registration Number	38881

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.A./

<i>Index of Claims</i> 	Application/Control No. 13901466	Applicant(s)/Patent Under Reexamination SEIDNER, DANIEL JAKOB
	Examiner MOHAMMED ALAM	Art Unit 2851

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	04/04/2014								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
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	15	✓								
	16	✓								
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	18	✓								
	19	✓								
	20	✓								



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BIB DATA SHEET

CONFIRMATION NO. 2909

SERIAL NUMBER 13/901,466	FILING or 371(c) DATE 05/23/2013 RULE	CLASS 716	GROUP ART UNIT 2851	ATTORNEY DOCKET NO. DSEID-90745		
APPLICANTS INVENTORS Daniel Jakob Seidner, Los Angeles, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 06/15/2013						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/MOHAMMED ALAM/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS FULWIDER PATTON LLP HOWARD HUGHES CENTER 6060 CENTER DRIVE, TENTH FLOOR LOS ANGELES, CA 90045 UNITED STATES						
TITLE SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES						
FILING FEE RECEIVED 730	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

Search Notes 	Application/Control No. 13901466	Applicant(s)/Patent Under Reexamination SEIDNER, DANIEL JAKOB
	Examiner MOHAMMED ALAM	Art Unit 2851

CPC- SEARCHED		
Symbol	Date	Examiner
G06F	4/4/2014	/MA/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
G06F 17/30, 17/50	4/4/2014	/MA/

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
716	102	4/4/2014	/MA/

SEARCH NOTES		
Search Notes	Date	Examiner
Plus Search	4/3/2014	/MA/
Google Search	4/3/2014	/MA/
EAST Search	4/3/2014	/MA/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
716	102	4/3/2014	/MA/
G06F	17/30, 17/50	4/4/2014	/MA/

/M.A./ Examiner.Art Unit 2851	
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PLUS Search Results for S/N 13901466, Searched Mon Mar 10 08:46:11 EDT 2014
The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

8346528 99	7412296 97
4065997 97	
5446555 97	
5541849 97	
5544066 97	
5544070 97	
5628630 97	
5838584 97	
5870308 97	
6031246 97	
6077308 97	
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7353469 97	
7359645 97	
7363099 97	
7369970 97	
7371067 97	
7386816 97	

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13901466
	Filing Date		2013-05-23
	First Named Inventor	Daniel Jakob Seidner	
	Art Unit	2184	
	Examiner Name		
	Attorney Docket Number	DSEID-90745	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8326962	B2	2012-12-04	Lo	
	2	8271773	B2	2012-09-18	Grittke et al.	
	3	7991606	B1	2011-08-02	D'Souza et al.	
	4	6914551	B2	2005-07-05	Vidal	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add
U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120317574	A1	2012-12-13	Eckardt	
	2	20120019371	A1	2012-01-26	Vidal	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13901466	
	Filing Date		2013-05-23	
	First Named Inventor	Daniel Jakob Seidner		
	Art Unit	2184		
	Examiner Name			
	Attorney Docket Number	DSEID-90745		

	3	20110145777	A1	2011-06-16	Iyer et al.	
	4	20100217967	A1	2010-08-26	Viswanathan et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. **Add**

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

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EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13901466
	Filing Date	2013-05-23
	First Named Inventor	Daniel Jakob Seidner
	Art Unit	2184
	Examiner Name	
	Attorney Docket Number	DSEID-90745

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/john k. fitzgerald/	Date (YYYY-MM-DD)	2013-08-22
Name/Print	John K. Fitzgerald	Registration Number	38881

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	16662950
Application Number:	13901466
International Application Number:	
Confirmation Number:	2909
Title of Invention:	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Daniel Jakob Seidner
Customer Number:	24201
Filer:	John Kenneth Fitzgerald/V. Monica Mandel
Filer Authorized By:	John Kenneth Fitzgerald
Attorney Docket Number:	DSEID-90745
Receipt Date:	22-AUG-2013
Filing Date:	23-MAY-2013
Time Stamp:	17:03:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ustpto_ids_DSEID_90745.pdf	612653	no	4
			1d42ab06c60816faf9997bd6cb22bfd1baf81203		
Warnings:					
Information:					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/901,466				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA		RATE(\$)	FEE(\$)	RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	70	N/A				
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	300	N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	360	N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 =	*	x 40 =	0.00	OR				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 =	*	x 210 =	0.00	OR				
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				0.00	OR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					0.00	OR				
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	730	TOTAL				
APPLICATION AS AMENDED - PART II										
AMENDMENT A	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	OR OTHER THAN SMALL ENTITY		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
AMENDMENT B	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	OR OTHER THAN SMALL ENTITY		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/901,466	05/23/2013	2184	730	DSEID	20	3

CONFIRMATION NO. 2909

24201
FULWIDER PATTON LLP
HOWARD HUGHES CENTER
6060 CENTER DRIVE, TENTH FLOOR
LOS ANGELES, CA 90045

FILING RECEIPT



OC000000061999902

Date Mailed: 06/21/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Daniel Jakob Seidner, Los Angeles, CA;

Applicant(s)

Daniel Jakob Seidner, Los Angeles, CA;

Power of Attorney: The patent practitioners associated with Customer Number 24201

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 06/15/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/901,466**

Projected Publication Date: 11/27/2014

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/901,466	05/23/2013	Daniel Jakob Seidner	DSEID

24201
FULWIDER PATTON LLP
HOWARD HUGHES CENTER
6060 CENTER DRIVE, TENTH FLOOR
LOS ANGELES, CA 90045

CONFIRMATION NO. 2909
POA ACCEPTANCE LETTER



OC000000061999938*

Date Mailed: 06/21/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/23/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hngo/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: <u>Daniel Jakob Seidner</u> Date (Optional) : <u>May 23, 2013</u> Signature: <u>/Daniel Jakob Seidner/</u>	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	DSEID
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor 1					Remove		
Legal Name							
Prefix	Given Name		Middle Name		Family Name		Suffix
	Daniel		Jakob		Seidner		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Los Angeles		State/Province	CA	Country of Residence i	US	
Mailing Address of Inventor:							
Address 1		10260 Constellation Boulevard					
Address 2		Suite 2810					
City	Los Angeles			State/Province	CA		
Postal Code	90067			Country i	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.							
Add							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	24201		
Email Address	docketla@fulpat.com	Add Email	Remove Email
Email Address	jfitzgerald@fulpat.com	Add Email	Remove Email

Application Information:

Title of the Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		
Attorney Docket Number	DSEID	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	DSEID
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	24201		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) ^h the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).			
Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	DSEID
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
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Authorization to Permit Access:

☒	Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	DSEID
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		

Applicant 1			Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
Clear			
☐ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor :			
If the Applicant is an Organization check here. ☐			

Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button. Add				

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.	
Assignee 1	
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).	
Remove	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	DSEID
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		

If the Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee Data may be generated within this form by selecting the Add button. Add				

Signature:Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications				
Signature	/john k. fitzgerald/		Date (YYYY-MM-DD)	2013-05-23
First Name	John K.	Last Name	Fitzgerald	Registration Number
				38881
Additional Signature may be generated within this form by selecting the Add button. Add				

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82A (07-12)

Approved for use through 11/30/2014. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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**TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE
REGISTERED PRACTITIONERS**

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	
Filing Date	05/23/2013
First Named Inventor	Daniel Jakob Seidner
Title	SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES
Art Unit	
Examiner Name	
Attorney Docket Number	DSEID-90745

SIGNATURE of Applicant or Patent Practitioner

Signature	/john k. fitzgerald/	Date	05/23/2013
Name	John K. Fitzgerald	Telephone	310-824-5555
Registration Number	38,881		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

- ☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

24201

OR

- ☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

- ☒ The address associated with the above-mentioned Customer Number.

OR

- ☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

I am the Applicant:

- ☒ Inventor or Joint Inventor
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature	/Daniel Jakob Seidner/	Date	May 23, 2013
Name	Daniel Jakob Seider	Telephone	310-433-4200
Title and Company			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

- ☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES		
First Named Inventor/Applicant Name:		Daniel Jakob Seidner		
Filer:		John Kenneth Fitzgerald/V. Monica Mandel		
Attorney Docket Number:		DSEID-90745		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				730

Electronic Acknowledgement Receipt	
EFS ID:	15860502
Application Number:	13901466
International Application Number:	
Confirmation Number:	2909
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SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES

BACKGROUND

[0001] For some time now, technology has advanced to the point where developers and manufacturers have had the ability to provide remote control over their products. A very simple example is a television and its remote controller. A remote controller uses a wireless signal, usually infrared, to send user provided control instructions to a television set. The television set then executes those instructions, such as turning off the television or changing the channel. In the case of the TV and the remote controller, manufacturers had to design, develop and program the remote controller such that it could interact with the proprietary specifications of their television system. A remote controller setup for one television system would not work for another television system or a different system all together, such as a DVD player.

[0002] With the wide proliferation of the devices connected to the internet, developers have had the ability to develop software and controllers to control devices connected to the internet. One example is a personal computer with remote desktop software. This software enables a personal computer (with the correct software) to control another personal computer which is connected to the internet and running the remote desktop software. Another example is a mechanical device which is fitted with integrated circuits (ICs) that can be controlled by smartphones such as AR.Drone, Sphero and iHelicopter. For situations like these, developers currently have to create or develop proprietary software to provide control functionality of proprietary hardware.

[0003] Control has also gone beyond the personal computer. Developers have designed and built micro control units (MCUs) integrated with remote communication devices and programmed them to receive instructions both locally and remotely.

[0004] In the past, the controlling device that sent the instructions to host devices may have been specifically manufactured and designed by the host device manufacturers. However, new devices, such as smart phones, remove the necessity of manufacturing the controlling device because these devices are very flexible and common place. These handheld devices are smaller than the traditional television remote controllers and can be configured with software to provide

instructions to any object with a receiver. The only limitations are that an object has proper hardware and that the controlling device has the proper software.

[0005] A developer who wishes to provide remote controllability to an object or product they may also create, must spend time and expenses in developing the software and hardware for this remote controllability functionality. For example, a developer might have to fit their product with an application specific integrated circuit (ASIC) specifically designed to receive remote communications. The ASIC may have a proprietary set of commands and instructions that need to be programmed into a controller to remotely control and communicate with the ASIC and control the product. Additionally, for every different type of computer or operating system, a different program or application has to be created to ensure compatibility. Furthermore, the developer has to fabricate and test the ASIC to ensure that it is working properly. All of this deters manpower from the development of the host product itself. Furthermore, the developer has to develop software specific to the ASIC and any remote controlling device. Many times, devices that could be fitted with an ASIC to allow remote control are not because of the time and costs for implementation.

[0006] All currently available automation, integration and control products and technologies are nothing more than hardware and software acting as figurative ropes and pulleys designed to manipulate devices and constructs with abstraction for the actual state of the device itself. Consequently, these existing solutions require considerable customization and development on a case by case basis for the establishment of individual/closed automation and control ecosystems. These solutions are neither universal nor capable of ad-hoc deployment scenarios. From complex proprietary based control and automation systems to low cost, Do-It-Yourself (DIY) approaches, all currently available solutions require varying degrees of hardware and software abstraction to accomplish their respective deployment goals.

[0007] In general, all competing solutions fail to offer universal control as they all are predicated upon deployment through an abstraction layer and are geared towards specific markets of which there is no cross-communication or service. For the most part, competing solutions to the above described problems introduce automation of devices as “after thoughts” and attempt to enable integration through a “bolt on” metaphor. No competing technology has

yet produced a universal “plug and play” model for any third party device manufacture to employ.

[0008] Current automation and control management systems and components are mired with complex controls, proprietary commands and non-intuitive interfaces. Entry level systems which attempt to empower the end user with some degree of management of the automation device are limited to very simplistic binary states such as a “preference list.” This limitation exists because there is no established mechanism for broadcasting the capabilities of the component or device.

[0009] True, universal automation and control is predicated upon the development of the integrated technology piece which will deliver plug and play for all devices and constructs that can be envisioned within an automated ecosystem. Historically, we have accepted that information and its movement through the internet have been viewed as unrestricted through the establishment of communication, messaging and interaction standards such as TCP, SMTP, and HTTP and we have viewed access to the same as commonplace due to the ubiquity of the web browser. These standards and related technologies not only assure access to information but are largely taken for granted as being available anywhere and through anything at any time.

[0010] Access to control however presents considerably greater challenges and to this day no single solution allows for the complete ad-hoc establishment and expansion of an automation plant without imposing the requirement of complex iterative development of said environment. Simply put, the seemingly contradictory expectation exists that while a printer added to a network should automatically be accessible to computers within the same network, it is also expected and accepted that a device added to an automation plant requires the reconfiguration of the totality of the automation systems for the specific recognition and operation of that singular new device.

[0011] The ideal connected world allows for equal access to information and control. The technology architects of the information age have achieved universal access to information set within this ideal yet they have only created successive obstacles to equal access to control. Each development within the automation and control space has been predicated upon the use of complex and proprietary interconnects creating virtual ropes and pulleys to the devices they intend to operate and manipulate. At no point in time have the endpoints been given the

fundamental abilities to maintain their unique presence and identity in a networked infrastructure and present their modes of being for open access and manipulation. The existence of abstraction layers within the modes of address between end users and automation systems from automation systems and their endpoints assures that at no point may an end user alter, add or remove an endpoint without modifying the system that is to manage it. In effect, while access to information is always direct, the middleman in access to control becomes its liability and greatest detraction.

[0012] Additionally it is important to note that most automation invention in the “post PC revolution” has been product-centric, not technology centric. Constructs come into being through the amalgamation of a host of existing technologies and introduce very little that is “new.” In doing so, these developments effectively add complexity to the landscape they ostensibly intended to simplify.

[0013] Thus, a need has been developed for a system and method that simplifies and vertically integrates the development of the hardware and software for a universal control system. Such a system and method provides solutions to the above described problems by delivering integration from within a construct to be controlled rather than via an external abstraction layer. Moreover, such a system and method should imbue the integrated construct or device with an ability to broadcast its existence, its identity, its functionality as well as its current state and reciprocally receive instruction in parallel with its traditional I/O mechanisms. The present invention satisfies these and other needs.

SUMMARY OF THE INVENTION

[0014] In its most general aspect, the invention includes a system and method for providing universal and integrated control to constructs and devices which may be controlled by micro control units (MCU) or other controlling hardware.

[0015] In another general aspect, the invention provides a mechanism and methodology for delivering true universal automation and control of any device or construct that can be imagined within an automation and control ecosystem. Any device that can be envisioned within an automation and control ecosystem, once imbued with the various aspects of the invention on a

pre-fabrication/manufacturing basis, can be easily integrated into an automation and control ecosystem in a “plug and play” manner requiring no modification or alteration to the ecosystem.

[0016] In still another general aspect, the invention also provides for integration and control by providing, native connectivity from within the construct rather than through an abstraction layer apart and exterior to the construct. These capabilities are entirely new and offer a complete departure from pre-existing automation, integration and control products and technologies.

[0017] In another aspect, the system and method of the present invention provide for the development of a super horizontal imbedded solution which offers network identity, location resolution, mode and state awareness and access to the range of parameters for device use or configuration irrespective of the nature of the device which would allow consumer and industrial electronics manufacturers, appliance and machine designers and device and apparatus creators to easily and effectively bring universal access and control to their unique products.

[0018] In yet another aspect, the system and method of the present invention provide for the development of an exceptionally low cost, low power and extremely low profile component such as an ASIC which is to be made available for inclusion in a parent device. This ASIC includes both core services for inclusion of the parent device within the automation ecosystem along with extensible services made available to the parent device designer and/or manufacturer for integration to the range of functionality and configurations associated with the parent device.

[0019] In yet another aspect, the system and method of the present invention provide for the development of a hierarchal class system for establishing definitions of behavior, operation and modification for any parent device.

[0020] In still another aspect, the system and method of the present invention provide for the development of a User Interface (UI) model for dynamic awareness of end point existence and operation.

[0021] In another aspect, the system and method of the present invention provide for the development of a management layer, not to obfuscate and insulate the end user from the end point but rather to maintain concurrency of environment awareness and simplify processes for variable device access.

[0022] In still another aspect, the system and method of the present invention provide a Fabless Development Kit (FDK) that enables device manufacturers to embed unique ASIC functionality within their micro-controller (MCU) design process and integration.

[0023] In yet another aspect, the present invention includes a system providing a common interface for devices to be controlled. Analogous to the simple act of “getting in a car and driving,” such an interface and control system allows a user to simply get the job done without having to relearn how to drive for every different car that the user drives; thus providing a user with a standardized interface with which to control the various devices that are a part of the user’s daily life.

[0024] In one aspect, the invention includes a system and method for designing integrated circuits (IC) to integrate into an electronic device for control using IC components that are developed for generic characteristics of electronic devices. This way, IC devices components may be standardized and designed based on functionality thus removing the necessity of designing a proprietary device in house. A developer can select the functionality of their device and an IC can be designed off the standard components. Furthermore, because standard IC components are used, standard software can be used to control and run on the IC devices.

[0025] In another aspect of the invention, a user interface (UI) standard is developed and through the deployment of this UI standard, a UI control interface may be coupled with each IC component. This allows for an intuitive user experience because the controls function similarly across multiple devices.

[0026] In yet another aspect of the invention, the designed IC is provided in a software representation. The software representation may be in layout and/or schematic format. This would allow for developers to make simple tweaks, simulate, and/or test the IC design. Furthermore, the layout and/or schematic can be sent to a manufacturer for manufacturing the IC. Having a fabless IC reduces IC development costs.

[0027] Furthermore, in another aspect of the invention, the ICs may be designed with fail safes for handling loss of connection or manual control overrides.

[0028] In another aspect, the present invention includes a computer implemented method for designing an IC which controls a device when integrated into the device comprising: receiving a selection of categorized input and output characteristics of the electronic device; providing an IC design based on the selection of input and output characteristics of the device; and providing software for controlling the device through an IC based on the IC design.

[0029] In still another aspect, the invention includes providing software for controlling the device includes providing a user interface and virtual controls for a controller which allows for controlling the device through the IC. In an alternative aspect, the user interface is based on the selection of input and output characteristics. In yet another alternative aspect, IC allows for status input from the device and is capable of reporting the status to a controller.

[0030] In yet another aspect, the IC design is based on at least one predetermined IC component which is able to control one of the input or output characteristics. In still another aspect, the IC design is provided as a software schematic, layout, or both.

[0031] In another aspect, the IC may be configured to communicate an identity and an operating state of the device to a controller and wherein the controller is configured to register the identity of the device, and based on the identity of the device, communicate control commands to the device to alter the operating state of the device.

[0032] In yet another aspect, the invention includes a system comprising: one or more processors; logic encoded in one or more non-transitory computer-readable media that, when executed by the one or more processors, is operable to: receive a selection of categorized input and output characteristics of a device; provide an IC design based on the selection of input and output characteristics of the device; and provide software for controlling the device through the IC. In one alternative aspect, the provided IC design includes: a user interface for communicating with a controller which provides a virtual control for the device through the IC. In another alternative aspect, the user interface is based on the selection of input and output characteristics.

[0033] In a further aspect, the IC includes an input for receiving status information representing an operating state of the device and is configured to communicate the status information to the controller.

[0034] In yet a further aspect, the IC design is based on at least one predetermined IC component which is able to control one of the input or output characteristics. In another aspect, the IC design is provided as a software schematic, layout, or both.

[0035] In still another aspect the one or more non-transitory computer-readable media further comprises logic that, when executed by the one or more processors, is further operable to: simulate the IC's functionality based on the IC design.

[0036] In yet another aspect, the invention includes a non-transitory computer-readable medium storing instructions that, when executed by a processor, perform a method comprising: receiving a selection of categorized input and output characteristics of the device; providing an IC design based on the selection of input and output characteristics of the device; and providing software for controlling the device through the IC.

[0037] In a further aspect, the invention includes communicating a user interface to a remote controller which provides a virtual control for the device through the IC. In one alternative, the user interface is based on the selection of input and output characteristics. In still a further aspect, the IC allows for status input from the device and is capable of reporting the status to the controller. In another aspect, the IC design is based on at least one predetermined IC component which is able to control one of the input or output characteristics. In still another aspect, the IC design is provided as a software schematic, layout, or both.

[0038] Other features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] FIGURE 1 is a frontal view of a device that may be controlled using various embodiments of the present invention.

[0040] FIG. 2 is an exemplary depiction of a top-level hierarchal classification scheme in accordance with one embodiment of the invention.

[0041] FIG. 3 is an exemplary depiction of sub-level of the hierarchal classification scheme of FIG. 2.

[0042] FIG. 4 is a flow chart of one embodiment of the invention depicting an exemplary method for using an FDK to design an ASIC.

[0043] FIG. 5 is an exemplary Integrated Device Control System wherein a Device Management System is used.

[0044] FIG. 6 is an exemplary Integrated Device Control System wherein device management software is held on the controlling device.

[0045] FIG. 7 is an another exemplary Integrated Device Control System wherein device management software is held on the IC.

[0046] FIG. 8 is a flow chart of an exemplary implementation of a system which allows for developers to implement remote controllability to a device without developing integrated circuits and controlling software in-house.

[0047] FIG. 9 is an exemplary block diagram of an IC designed using a fabless design kit.

[0048] FIG. 10 is a flowchart of exemplary management software for managing interoperability between a computer system and an IC in an electronic device.

[0049] FIG. 11 illustrates an exemplary computer system architecture.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0050] As will be described hereinafter in greater detail, the various embodiments of the present invention relates to a device control system and method with uniform IC and UI development. For purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. Description of specific applications and methods are provided only as examples. Various modifications to the embodiments will be

readily apparent to those skilled in the art and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and steps disclosed herein.

[0051] The various embodiments of the invention provide a mechanism for delivering true universal automation and control of any device or construct that can be imagined within an automation and control ecosystem. Any device that can be envisioned within an automation and control ecosystem, once imbued with the invention on a pre-fabrication/manufacturing basis, can be easily integrated into an automation and control ecosystem in a “plug and play” manner requiring no modification or alteration to the ecosystem. The embodiments of the invention provide for integration and control by providing native connectivity from within the construct rather than through an abstraction layer apart and exterior to the construct.

[0052] All currently available automation, integration and control products and technologies are nothing more than hardware and software acting as figurative ropes and pulleys designed to manipulate devices and constructs with abstraction from the actual state of the device itself. Consequently, these existing solutions require considerable customization and development on a case by case basis for the establishment of individual/closed automation and control ecosystems. These solutions are neither universal nor capable of ad-hoc deployment scenarios. From complex proprietary based control and automation systems to low cost, DIY approaches, all currently available solutions require varying degrees of hardware and software abstraction to accomplish their respective deployment goals. The embodiments of the invention provide a direct, non-abstracted interface for the inclusion of any construct or device within an automation ecosystem.

[0053] Currently realized and envisioned integration, control and automation technologies fail to offer seamless deployment and management of their endpoints due to the many abstractions that exist between the automation management system and the endpoint. The various embodiments of present invention overcomes this failure by providing the mechanism by which any device and/or construct may be imbued with the capability of being seamlessly added to a network of like-kind devices and/or constructs and managed within an integration, control and

automation system that has real time awareness of the device and/or construct. The net result of the implementation of these various embodiments of the invention is the realization of the standardization of universal integration, control and automation through an interface that is as ubiquitous as the standardization of the web server and web browser are for information distribution.

[0054] In general, the invention is embodied in four core components which work together to produce a system by which discrete devices may be seamlessly added to a network of like-kind equipped devices producing an ecosystem that may be fully controlled and automated. The four core components are: 1) An ASIC or like-kind construct which is to be made available for inclusion in a parent device. This ASIC component includes both core services for inclusion of the parent device within the automation ecosystem along with extensible services made available to the parent device designer and/or manufacturer for integration to the range of functionality and configurations associated with the parent device; 2) a hierarchal class system for establishing definitions of behavior, operation and modification for any parent device; 3) a UI model for dynamic awareness of end point existence as well as modes of operation; and 4) a management layer for maintaining concurrency of environment awareness and for simplification of control of the aforementioned device.

[0055] As will be discussed more fully below, the ASIC is typically imbedded within a device and/or construct intended for inclusion within an automation ecosystem. This imbedding, in some embodiments, takes place at time of device manufacturing and is part of the finished good design of the device. In other embodiments, the ASIC may be added to the circuitry supporting the MCU of the device, rather than being imbedded within the MCU itself.

[0056] In the various embodiments of the invention, the ASIC is created with data provided by the device manufacturer through the use of an FDK (Fabless Development Kit) which provides a database of specific information which can be used to define the operation of the device. The FDK may be a software application or program, which may take the form of an Integrated Development Environment (IDE). The FDK may be specifically designed to assist a developer in designing and manufacturing control circuitry and programming. The FDK will typically access a database of structured information derived from the hierarchal class system defining the

behavior, operation and communication characteristics of the device into which the ASIC is to be imbedded.

[0057] The various embodiments of the invention permit each device in which the ASIC is imbedded to present itself autonomously to an automation ecosystem's management layer and/or controller device without any configuration or customization of the device, management layer and/or controller device and without any abstraction components or related communications technologies. Discrete device manufacturers of any type will have the ability to make their constructs "automation ready" with no limitation on device type or function. Much as the World Wide Web with the advent of the web server and web browser along with their core protocols of HTTP and HTTPS and core languages HTML and XML (via CSS) enabled ubiquity for the movement of information, the various embodiments of the invention will, for the first time, offer ubiquity for control and create a true universally accessible mechanism for integration and automation.

[0058] One of the key aspects of the various embodiments of the present invention is the observation by the inventor that the control systems applicable to the majority, if not all, of devices is that an individual device may be defined by four parameters: 1) control type; 2) display type; 3) input type; and 4) output type. FIG. 1 illustrates this using a common household appliance, namely, a blender 10.

[0059] A blender is a common kitchen appliance. It includes a motor, circuitry to operate the motor, one or more inputs 20, typically buttons of some type, and a display, which may be individual lights 15, as shown in FIG. 1, or may be a single panel display. Older blenders may use a rotatable dial with one or more positions assigned to providing one or more speeds or functions, and the use of dots, words or other graphic elements to display the state of the blender. Utilizing the principles described herein in reference to the various embodiment of the invention, it is possible to define the blender with parameters included in a hierarchal database, and thus the principles of the invention apply to any device. However, it will be understood that the various embodiments of the invention are particularly applicable to devices that include MCUs to provide for control of the device through natively interfacing with and/or addressing the MCU. It will also be understood that control functions described below may, through the use of the

embodiments of the invention, be built into the MCU, or may be provided through an IC that has been added to the circuitry of the device to provide for control of the device in parallel with the MCU.

[0060] FIG. 2 illustrates one embodiment such a hierarchal database. In this illustration, the hierarchal database contains data directed to particular aspects of a device. For example, such hierarchal databases are used by the United States Patent and Trademark Office as classification aids for classifying inventions into one or more fields of technology. The exemplary database of FIG. 2 will typically have a high level list of devices, divided into such categories as aerospace, automotive, maritime, rail, and the like. As shown, the upper level rail category can be further divided into sub-categories of amusement, industrial, and light rail. A further sub-categorization provides classes for diesel and electric engines, further sub-categorized by specifications and functions. The function sub-category is finally categorized again into control types, display types, input types and output types.

[0061] FIG. 3 illustrates a categorization scheme similar to that shown in FIG. 2 for consumer appliances. In this example, the top-level category of consumer appliances is divided into sub-categories such as cleaning devices, cooking devices, and food preparation devices. Food preparation devices are further categorized as either hand-held or stationary. One example of a stationary food preparation device is a blender like that described with reference to FIG. 1. Diving further into the classification library provides a category describing the functions of the blender, which functions may be further categorized by control type, display type, input type, and output type. For example, a blender may be controlled by a rotary dial, with a display that amounts to a word or graphic or symbol that displays the state of the blender when the input type is actuated. In another example, the input device may be push buttons or touch sensitive elements, and the display type may be a LCD or other type of electronic display that informs the user what state the blender is in when an input type is actuated. The output of the input may also be discerned from the display type, as well as experientially, such as by hearing the increase or decrease of sound generated by the blender as the speed of the motor is increased or decreased, pulsed, or stopped upon actuation of the input type. As one skilled in the art will immediately understand, any device, such as a blender, can be defined by defining its control type, display type, input type, and output type.

[0062] FIG. 4 is a graphical representation of one embodiment 50 of a system and method for designing and programming an ASIC that may either be incorporated directly into a device's MCU design, or may be a separate integrated circuit that is in operational communication with a device's MCU. In this exemplary embodiment, the circuit designer of the ASIC uses a Fabless Development Kit (FDK) 65 to design the circuitry of an ASIC that will provide native control and communications capability to a device, such as the blender described above. In this example, the FDK is embodied in software, or a combination of software and hardware and includes a hierarchal classification database 55 and an appropriate user interface (not shown). The ASIC designer interacts with the user interface of the FDK to access the hierarchal classification database using various menus or other input schemes of the FDK user interface. For example, it is contemplated that designer will may use a series of cascading menus corresponding to the classification scheme of the hierarchal classification scheme described with reference to FIGS. 2-3. Once the designer has reached the desired classification level, such as level 3.2.1.1.1 shown in FIG. 3 for the blender, the designer chooses a particular control type to be included in the operation of the circuitry. The designer may also edit the parameters associated with that particular entry as needed for the particular device for which the ASIC is being designed.

[0063] The process is continued until the control type 57, display type 59, input type 61 and output type 63 for the blender are defined. The parameters associated with the designers choices are then input into the FDK engine 65. Once input into the FDK engine 65, compiler 67 of the FDK engine 65 may access a library of circuits and embedded programming suitable for creating ASIC design 69 and its associated ASIC Programming 71. The software of the FDK may access a library of circuits and embedded programming suitable for carrying out the functions required for creation of an ASIC that will carry out the functions desired by the designer. It is also intended that the FDK may also include specifications for circuitry allowing for the ASIC to broadcast the identity and control functions to a controller, allowing the controller to seamlessly register the device in a plug and play manner. ASIC design 69 may be a circuit design such as a layout or a schematic that can be sent out to a manufacturer for fabrication. ASIC Programming 71 may be software to be programmed and/or stored in a fabricated ASIC and/or a controller to establish interoperability between the controller, ASIC, and/or a device that the ASIC is integrated with.

[0064] Fabless design of ICs and MCUs is well known in the art. In general, the term fabless design is applied to process where the design of the IC is accomplished separately from the manufacture of the device itself, rather than past methods which relied upon vertical integration of design and manufacture. Accordingly, a fabless process within the scope of the various embodiments of the present invention are particularly advantageous, in that the FDK may be used by a device maker, such as a blender manufacturer, to design and manufacture into the control circuitry of a device all of the functions the manufacturer desires, including the addition of a standardized communication scheme that would allow a controller to sense the presence of a device incorporating an ASIC designed in accordance with the embodiments of the present invention, and to register the device and communicate with the device without requiring an extensive set up or programming of the device or the controller.

[0065] It will be apparent to those skilled in the art that in many ways, the FDK of the various embodiments described herein may function similarly to a so called software development kit or an IDE. A software development kit has similar functionality, that is, a software development kit is typically a set of software development tools that allows for the creation of applications for a certain software package, software framework, hardware platform, computer system, video game console, operating system, or similar development platform. The inventor has realized that such a framework may also be applied in the fabless design of ICs, in concert with a hierarchal classification database that allows for the classification of the control type, display type, input type and output type of any control system required to control a device. In this manner, using the FDK and hierarchal classification device of the embodiments of the invention, an ASIC designer may build in native control functionality to be incorporated into any device capable of communicating with and being controlled by a controller. In essence, the hierarchal classification database and FDK system may provide a standardized system of programming control functionality into any controllable device. Such a control scheme would eliminate the need to perform custom “set up” or installation changes into a controller or a device to enable the device and controller to communicate with each other.

[0066] FIG. 5 illustrates an exemplary Integrated Device Control System 100 according to one embodiment of the present invention. Integrated Device Control System 100 may have one or more Integrated Device Controllers 101 which may be one or more computer systems and/or

may include, by way of example, wireless or wired controllers, including controllers that are remote from the one or more devices being controlled which may connect to Network Cloud 102. Network Cloud 102 generally represents a network or collection of networks (such as the Internet, private intranet, wide area networks, internal networks, personal area networks, or a combination thereof) over which one or more Integrated Device Controllers 101, Control Management System 103, and/or Controllable Devices 104 may interact with each other. In another embodiment the system may use a mesh network or any other suitable network. In still another embodiment, the system may use a pseudo-network, such as a peripheral bus, which may be considered an ad hoc network, or any other non-traditional form of a communication scheme that provides for communication between devices or components. In yet another embodiment, Control Management Systems 103 may be imbedded within Integrated Device Controllers 101 and/or Controllable Devices 104.

[0067] Control Management System 103 may contain one or more databases 113 which stores data and/or computer instructions for controlling one or more IC Components 114 within IC 124. Databases 113 may also include data and/or UI configurations for Integrated Device Controllers 101, instructions for Integrated Device Controllers 101 to interact with Control Management System 103 and/or Controllable Devices 104 and/or user access settings/security. For example, in one embodiment, the IC may include all autonomous logic and data necessary to carry out the control functions of present invention; or the IC may only include a portion of the autonomous logic and data necessary, and be configured to access a separate data source or processor to obtain any other logic or data necessary to carry out the control functions of the invention.

[0068] Control Management System 103 may also be a Web Server which may be used to provide one or more Integrated Device Controllers 101 the ability to interact with Control Management System 103 and/or Controllable Devices 104 through a webpage or other interfaces.

[0069] According to one embodiment, Control Management System 103 may be a unitary server or may be a distributed server spanning multiple computers or multiple data centers. The term server may refer to various types of servers, such as, for example and without limitation, a

web server, news server, mail server, message server, advertising server, file server, application server, exchange server, database server, proxy server, and the like.

[0070] Integrated Device Controllers 101 may be device incorporating a computer or processor system which runs one or more operating systems, such as, for example, OS X, iOS, Windows, Android, Unix, Linux, and the like, and executes one or more applications, such as a web browser, for example, Safari, Internet Explorer, Firefox, Chrome, Opera, and the like. Integrated Device Controllers 101 may have users using the Integrated Device Controllers 101. A user may enter a Uniform Resource Locator (URL) or other address directing a web browser to a server, and the web browser may generate a Hyper Text Transfer Protocol (HTTP) request and communicate the HTTP request to a server. A server may accept the HTTP request. Integrated Device Controllers 101 may render a web page based on the HTML files from a server, a thick client, or the like. As an example and not by way of limitation, web pages may render from one or more combinations of HTML, XHTML, XML, Java Script, Java, Microsoft Silverlight, AJAX, and the like. In another embodiment, Integrated Device Controllers 101 may run computer instructions which provides a UI for the client to interact with. The user's interaction with Integrated Device Controllers 101 may instigate communications between Integrated Device Controllers 101, Control Management System 103 and Controllable Devices 104. In one embodiment, a user's interaction with a UI may provide real time control over Controllable Devices 104. Control Management System 103, and/or Controllable devices 104 may also be made of one or more computer or processor systems.

[0071] Controllable Devices 104 may be any electronic device including but not limited to a light switch, a lamp, automobile, kitchen appliance, home theatre appliance, computer system, phone, or the like.

[0072] FIG. 6 illustrates an exemplary Integrated Device Control System 100B according to another embodiment of the invention. Integrated Device Control System 100B may have one or more Integrated Device Controllers 101B which may be one or more computer systems and may connect to one or more Controllable Devices 104. Integrated Device Controllers 101B may be connected to Controllable Devices 104B through Connection 102B which may be connected through the Internet, wired connection, private intranet, wide area networks, internal networks,

personal area networks, or a combination thereof. Alternatively, the connection between Integrated Device Controllers 101B and Controllable Devices 104B may be a direct wired or wireless connection. Wireless connectivity may be obtained using RF, Infrared, Wi-Fi, Bluetooth or other suitable technologies.

[0073] Integrated Device Controllers 101B may have a memory or data storage 103B which contains Control Management Software. The Control Management Software may allow the Integrated Device Controllers 101B to interact with Controllable Devices 104B through a webpage, software application, or other interfaces as described above.

[0074] An Integrated Device Controller (IDC) running appropriate Control Management Software in accordance with the principles of the present invention may be configured to either actively query the ecosystem in which the IDC is used to find and register Controllable Devices residing within a predefined area (which may be limited by the range of a transmitter incorporated within the IDC) or addressable network range, or the Control Management Software may control the IDC to passively listen for signals emitted by Controllable Devices within the range of the IDC. In this manner, the Control Management Software enables the IDC to cooperate with a Controllable Device that includes an IC (which may be an ASIC) in accordance with the various embodiments of the present invention to automatically register the Controllable Device with the IDC in a plug and play manner. As has been discussed above, the IC of the various embodiments of the invention, incorporated into the Controllable device, is configured to natively provide the identity, operational state and communication mode of the Controllable Device to the IDC during the registration process.

[0075] Integrated Device Control System 100B may have one or more Integrated Device Controllers 101B which may be one or more computer systems and may connect to Connection 102B. Integrated Device Control System 100B may also Integrated Device Controllers 101B may have a memory or data storage 103B which contains Control Management Software. The Control Management Software may allow for the Integrated Device Controllers 101B to provide one more Integrated Device Controllers 101B the ability to interact with Controllable Devices 104B either directly, or where appropriate connection to a network is available, through a webpage, software application, or other interfaces.

[0076] FIG. 7 illustrates yet another exemplary Integrated Device Control System 100C according to another embodiment. Integrated Device Control System 100C may have one or more Integrated Device Controllers 101C which may be one or more computer systems and may connect to one or more Controllable Devices 104C. Integrated Device Controllers 101C may be connected to Controllable Devices 104C through connection 102C which may be the Internet, private intranet, wide area networks, physical connection, wired connection, wireless connection, wired network, internal networks, personal area networks, or a combination thereof.

[0077] Controllable Devices 104C may have a memory or data storage 103C which contains Control Management Software. The Control Management Software may allow for the Controllable Devices 104C to provide one more Controlling Devices 101C the ability to interact with Controllable Devices 104C through a webpage, software application, or other interfaces. In another embodiment, Controllable Devices 104C may send the Control Management Software for installation and/or execution by Controlling Devices 101C which enables interactions between the two through a webpage, software application, or other interfaces.

[0078] FIG. 8 is a flow chart of an exemplary implementation of a system 2000 which allows for developers to implement remote controllability to a device without developing integrated circuits and controlling software in-house.

[0079] At step 2001, system 2000 may provide a developer a fabless integrated circuit (IC) development kit. The FDK may be software which, when executed on a computer system, allows for a developers to input interface attributes of a device which a developer intends to enable a user to remotely control the device. The FDK may provide a software representations of a complete IC design. In one embodiment, the software representation may be a schematic and/or layout. The user may have the ability to edit the software representation of the IC or the software representation may be locked and only allow for testing. The software representation may also provide simulation and debugging capabilities through proprietary software and/or design automation software. Design automation software may include but, is not limited to, computer aided design software developed by Synopsis, Inc.; Cadence Design Systems, Inc.; Magma Design Automation, Inc.; and the like.

[0080] The IC, when manufactured, may be integrated with the developer's device and provide capabilities to remotely control the product with a computer. In one embodiment, the FDK may also provide accompanying software to run with the IC (assuming it is a programmable IC) and/or on a computer to enable remote control.

[0081] At step 2002 a developer may send the fabless IC design provided by the FDK to a manufacturer for manufacturing. A developer may implement the manufactured IC into the developer's product. In this way, much of the costs for designing, testing, and developing is reduced. System 2000 also provides at step 2002, access to management application software that manages the interoperability between an integrated device controller and the IC. This may include, identity, user interface cues, feedback from the IC, instructions, communications, security, and the like.

[0082] A developer may send the IC design created using the FDK to a IC manufacturer to manufacture the integrated circuit for integration with a product. In one embodiment, a program provided by the FDK is programmed into the IC for pairing with one or more computers to be used as a controller.

[0083] At step 2003 The developer may install the IC into their device and integrate it with the control aspects of the device. For example, if the device were a microwave, the IC may integrate with the microwave controls such that the IC could completely or partially manipulate the microwave. The IC may be directly connected to the device's internal bus such that it directly manipulates the device, and/or provides instruction to a native controller.

[0084] At step 2004 the device may connect to management software which syncs with the device. The management software may provide interoperability between the IC and an integrated device controller. The management software may control access, provide control instructions, identify the device and/or controller. The management software may provide software to allow the IC and an integrated device controller to be plug and play. An integrated device controller may also sync with the management software and may indicate a request to control the device. The management software may have a security protocol that prevents unauthorized connections to the device. Connection to the device may be password protected.

[0085] At step 2005 a UI is provided to the integrated device controller which matches the controlled device and provides virtual controls which may manipulate the device. The management software may also provide status information of the device, such as whether the device is on or off.

[0086] At step 2006 the integrated device controller is given control. Any user manipulations of the UI controls are relayed to the IC to control the device. The management software may also update the integrated device controller with any data provided in response to the control of the device. Furthermore the IC may provide redundancy and responses that informs the management software and integrated device whether commands have been accepted, whether the connection is still intact, quality of the connection, and the like.

[0087] The IC may also provide fail safes for when a connection is lost or when manual control is being conducted. In one embodiment, the IC may shut off or enter a safety mode when a connection to an integrated device controller is lost. The IC may also provide priority to manual control commands which may automatically override and/or disconnect an integrated device controller. In the various embodiments of the present invention, the IC also provides data representative of the state of the IC and/or device to a controlling device, and thus may have an inherent awareness of such state, which is useful in determining the control command necessary to alter the state of the IC or device.

[0088] Referring again to FIGS. 2-4, additional details of an embodiment of a method using the FDK to design an ASIC in accordance with the principles of the invention when executed by a computer is described. As described previously, the FDK may provide a menu of categorized devices for a user to select from. In one embodiment, the menu may start with a limited number of broad categories of devices which drills down into a more specified category of a device with each selection until a final device is selected. By way of example and not limitation, a menu may have, for example, the classes: appliance, automotive, environment. Selecting the class appliance, may provide the additional categories: kitchen appliance, office appliance, entertainment appliance. Once selecting kitchen appliance, a menu of kitchen appliances may be provided such as blender, coffee machine, stove, etc. Once the user selects a device, the user may be provided with a selectable set of characteristics of the user's device. By way of

example, the type of characteristics may include control, display, input and output, communications.

[0089] Characteristics may include multiple types within each characteristic. For example, types of control may include wheel, joystick, button, knob, switch, etc. Display type references the form of visual communication, such as for example, alpha numeric, base ASCII, extended ASCII, bitmap, or even more complex displays such as HTML decoding engines. These display types may be communicated to a user of the device by LCD, LED, OLED, and the like. In other embodiments input and output of the device may be audio, video, etc. For example, the blender's display references an "output" of the vendor (what it is doing) and the blender's buttons references an "input," a command or instruction to modify or initiate a new action on the blender.

[0090] Communications may include Wi-Fi, Bluetooth, serial, public switch telephone network, WiMax, LTE, etc. In other embodiments the FDK may include more or less characteristics and/or use different categorizations.

[0091] A user may choose multiples of each characteristics and/or types within each characteristic. In some cases, a user may be able to add additional specifications related to the environment which the IC would be connected into. These specifications may include, for example, real estate (chip size and dimensions), clock speed; interrupts; operating voltages, current, power; communication types such as HDL; and the like. In some embodiments, the FDK may dictate the minimum necessary elements for the designed IC to run properly.

[0092] Each characteristic and/or type may be linked with a predetermined standardized IC for performing and controlling those characteristics and types on a device. The FDK may design and develop a complete IC design layout and/or schematic that could be sent to a IC manufacturer for manufacturing. The FDK may have a library of standard IC parts which each selection is linked to. Once all selections are made the FDK may combine the standardized IC parts and provide a CAD design of a resulting IC. Similar to how CAD software may provide a library of standard cells or blocks when designing an IC, the FDK may provide standardized IC components that fully function and can control a device based on the user's chosen characteristics.

[0093] In one embodiment, the FDK may combine combinations of unmodified standard IC components based on the user's choices. In another embodiment, the FDK may alter one or more standard IC components chosen by a user to increase efficiency, reduce redundant parts, fit a certain size, and/or compensate for certain specifications chosen by a user. The FDK may be expandable with additional IC components as they are developed and each iteration may be backwards compatible.

[0094] FIG. 9 is an exemplary block diagram of an IC 300 designed using an FDK. IC 300 may have one or more standard IC components 1 through N. IC 300 may receive input from either the device it is integrated with through internal bus 301 or from an integrated device controller through a network connection 302. In one embodiment, one or more of the IC components may be configured to receive information from a network interface controller. In another embodiment, a Network Interface Controller (NIC) may be integrated with IC 300 through one or more standard IC components. IC 300 may also be configured for providing output to control the device or provide feedback to a controller.

[0095] According to an embodiment, an application management software may manage the interoperability between an integrated device controller and a controlled device containing an IC designed through an FDK. This management software may be installed on a computer which is being used as an integrated device controller, held on a server, held on the device's IC or a combination of thereof. The management software may determine the identity of the object, the input output capabilities, UI settings, security, drivers, firmware and communications.

[0096] FIG. 10 is a flowchart of Management software 400 according to an embodiment. At step 401 management software 400 may receive a request from a computer requesting control of a particular object that is integrated with an IC designed through the FDK. In one embodiment, a request may be made using a unique identifier of the object. In another embodiment, the object may broadcast its existence over a network, such that any potential computer on the same network may request access or control.

[0097] At 402, Management software 400 may receive an identifier associated with the IC and object. The identifier may provide the Management software with control parameters for the IC. It may also provide drivers or firmware necessary to operate the IC. In one embodiment, drivers

and firmware would be part integrated with the management software. The IC may also provide user interface cues, which would provide the management software indications on which user interface controls would be used on an integrated device controller.

[0098] At 403, Management software 400 receives information regarding which IC components were chosen through the FDK, and determine what inputs, outputs, status updates and UI controls are enabled for the IC/device.

[0099] At 404, Management software 400 may set up a user interface on an integrated device controller based on the IC components. In one embodiment the user interface may be displayed in a web browser or other like-kind client interface. In another embodiment, the management software may instruct which UI controls are to be displayed on the integrated device controller, through a native program installed on the integrated device controller. In yet another embodiment, the management software may provide an executable file which installs software specific to the IC/device controls for installation and use on the controller.

[0100] At 405, Management software may receive instructions or status updates from either a user manipulating the integrated device controller or the IC. For example, a user may manipulate controls in the UI that requests a device to be turned off. The user's action may be sent to Management software 400. In response, Management software 400 may relay a corresponding instruction to the IC to turn off the device. Similarly, the IC may send a status information such as whether the devices is on or off to Management software 400. The management software may relay periodic updates regarding the status and/or whenever a status has changed. The UI may reflect the current status and/or any status changes from the device.

[0101] According to an embodiment, the UI controls and status updates may be predetermined and standardized based on the IC components used. The UI controls may be consistent over all devices which use the same IC component in its IC. For example, an IC implemented in a car used an IC component for turning a steering wheel, the integrated device controller may display a virtual steering wheel to allow a user to steer. If the same IC component was used in an IC for steering a motor boat steering wheel, the virtual display may be identical on the integrated device controller display. In one embodiment, a developer or integrated device control user may choose among several standardized UI controls for each IC component.

[0102] In yet another embodiment, a developer or user may be able to customize the UI controls. Some UI controls may be unique specific to certain IC components, category group, and/or device defined in an FDK. In one embodiment, the UI may be a replica of the device's native display. For example, a device may have a small LCD display and/or LED display. The IC may output the display data to the integrated device controller, and the integrated device controller may display an identical replica. In some cases, the device may have a touch screen and the integrated device controller may replicate the touch screen controls on its own display and allows for remote interaction through the replicated touch screen controls.

[0103] FIG. 11 illustrates an exemplary computer system 500 which may be used with some embodiments of the present invention. Computer system 500 may take any suitable form, including but not limited to, an embedded computer system, a system-on-chip (SOC), a single-board computer system (SBC) (such as, for example, a computer-on-module (COM) or system-on-module (SOM)), a laptop or notebook computer system, a smart phone, a personal digital assistant (PDA), a server, a tablet computer system, a kiosk, a terminal, a mainframe, a mesh of computer systems, etc. Computer system 500 may be a combination of multiple forms. Computer system 500 may include one or more computer systems 500, be unitary or distributed, span multiple locations, span multiple systems, or reside in a cloud (which may include one or more cloud components in one or more networks).

[0104] In one embodiment, computer system 500 may include one or more processors 501, memory 502, storage 503, an input/output (I/O) interface 504, a communication interface 505, and a bus 506. Although this disclosure describes and illustrates a particular computer system having a particular number of particular components in a particular arrangements, this disclosure contemplates other forms of computer systems having any suitable number of components in any suitable arrangement.

[0105] In one embodiment, processor 501 includes hardware for executing instructions, such as those making up software. Herein, reference to software may encompass one or more applications, byte code, one or more computer programs, one or more executable, one or more instructions, logic, machine code, one or more scripts, or source code, and vice versa, where appropriate. As an example and not by way of limitation, to execute instructions, processor 501

may retrieve the instructions from an internal register, an internal cache, memory 502 or storage 503; decode and execute them; and then write one or more results to an internal register, an internal cache, memory 502, or storage 503. In one embodiment, processor 501 may include one or more internal caches for data, instructions, or addresses. Memory 503 may be random access memory (RAM), static RAM, dynamic RAM or any other suitable memory. Storage 505 may be a hard drive, a floppy disk drive, flash memory, an optical disk, magnetic tape, or any other form of storage device that can store data (including instructions for execution by a processor).

[0106] In one embodiment, storage 503 may be mass storage for data or instructions which may include, but not limited to, a HDD, solid state drive, disk drive, flash memory, optical disc (such as a DVD, CD, Blu-ray, and the like), magneto optical disc, magnetic tape, or any other hardware device which stores may store computer readable media, data and/or combinations thereof. Storage 503 may be internal or external to computer system 500.

[0107] In one embodiment, input/output (I/O) interface 504, includes hardware, software, or both for providing one or more interfaces for communication between computer system 500 and one or more I/O devices. Computer system 500 may have one or more of these I/O devices, where appropriate. As an example but not by way of limitation, an I/O device may include one or more mice, keyboards, keypads, cameras, microphones, monitors, display, printers, scanners, speakers, cameras, touch screens, trackball, trackpad, biometric input device or sensor, or the like.

[0108] In still another embodiment, a communication interface 505 includes hardware, software, or both providing one or more interfaces for communication between one or more computer systems or one or more networks. Communication interface 505 may include a network interface controller (NIC) or a network adapter for communicating with an Ethernet or other wired-based network or a wireless NIC or wireless adapter for communications with a wireless network, such as a Wi-Fi network. In one embodiment, bus 506 includes any hardware, software, or both coupling components of a computer system 500 to each other.

[0109] The various embodiments of the present invention provide for the development of an exceptionally low cost, low power and extremely low profile component such as an ASIC which is to be made available for the inclusion in a parent device, such as the blender described above.

The ASIC, or child component, will include both core services for inclusion of the parent device within the automation ecosystem along with extensible services made available to the parent device designer and/or manufacturer for integration to the range of functionality and configurations associated with the parent device. Moreover, the embodiments include the development of a hierarchal class system for establishing definitions of behavior, operation and modification for any parent device, the development of a UI model for dynamic awareness of end point existence and operation, and the development of a management layer, not to obfuscate and insulate the end user from the end point but rather to maintain concurrency of environment awareness and simplify process for variable device access. The core services introduced with the operating system present modes of access and interpretation the management application for interoperability with any device that includes an ASIC in accordance with the present invention.

[0110] Any conceivable permutation of any device, known or unknown, can be accommodated by the third party submission model made possible through the advent of the embodiments incorporating the above described FDK system and method. Management and control of any component within the ecosystem is manifest through a homogeneous approach made possible through a combination of data sets submitted within the FDK work-product along with defined parameters established within the class system contained within the logic of the imbedded element.

[0111] The various embodiments of the invention also offer revenue opportunities, including but not limited to: a licensing model for the distribution of the FDK, a commercialized goods sale made possible by Build-To-Order manufacturing and distribution of the imbedded element, such as an ASIC, a royalty model for the proliferation of the imbedded element, a professional services revenue system established for support and guidance of FDK use, and a commercial goods sales and licensing model for the deployment of the management system. The embodiments of the invention thus become both a super vertically and super horizontally integrated technology piece that may penetrate every industrial sector and enter into every manufactured construct or device that employs integrated circuits.

[0112] While particular embodiments of the present invention have been described, it is understood that various different modifications within the scope and spirit of the invention are possible. The invention is limited only by the scope of the appended claims.

I Claim:

1. A computer implemented method for designing an IC which controls a device when integrated into the device comprising:

receiving a selection of categorized input and output characteristics of the electronic device;

providing an IC design based on the selection of input and output characteristics of the device; and

providing software for controlling the device through an IC based on the IC design.

2. The method of claim 1, wherein providing software for controlling the device includes providing a user interface and virtual controls for a controller which allows for controlling the device through the IC.

3. The method of claim 2, wherein the user interface is based on the selection of input and output characteristics.

4. The method of claim 1, wherein the IC allows for status input from the device and is capable of reporting the status to a controller.

5. The method of claim 1, wherein the IC design is based on at least one predetermined IC component which is able to control one of the input or output characteristics.

6. The method of claim 5, wherein the IC design is provided as a software schematic, layout, or both.

7. The method of claim 1, wherein the IC is configured to communicate an identity and an operating state of the device to a controller and wherein the controller is configured to register the identity of the device, and based on the identity of the device, communicate control commands to the device to alter the operating state of the device.

8. A system comprising:

one or more processors;

logic encoded in one or more non-transitory computer-readable media that, when executed by the one or more processors, is operable to:

receive a selection of categorized input and output characteristics of a device;

provide an IC design based on the selection of input and output characteristics of the device; and

provide software for controlling the device through the IC.

9. The system of claim 8, wherein the provided IC design includes:

a user interface for communicating with a controller which provides a virtual control for the device through the IC.

10. The system of claim 9, wherein the user interface is based on the selection of input and output characteristics.

11. The system of claim 9, wherein the IC includes an input for receiving status information representing an operating state of the device and is configured to communicate the status information to the controller.

12. The system of claim 9, wherein the IC design is based on at least one predetermined IC component which is able to control one of the input or output characteristics.

13. The system of claim 12, wherein the IC design is provided as a software schematic, layout, or both.

14. The system of claim 8, wherein the one or more non-transitory computer-readable media further comprises logic that, when executed by the one or more processors, is further operable to: simulate the IC's functionality based on the IC design.

15. A non-transitory computer-readable medium storing instructions that, when executed by a processor, perform a method comprising:
- receiving a selection of categorized input and output characteristics of the device;
 - providing an IC design based on the selection of input and output characteristics of the device; and
 - providing software for controlling the device through the IC.
16. The method of claim 15, further comprising:
- communicating a user interface to a remote controller which provides a virtual control for the device through the IC.
17. The method of claim 16, wherein the user interface is based on the selection of input and output characteristics.
18. The method of claim 15, wherein the IC allows for status input from the device and is capable of reporting the status to the controller.
19. The method of claim 15, wherein the IC design is based on at least one predetermined IC component which is able to control one of the input or output characteristics.
20. The method of claim 19, wherein the IC design is provided as a software schematic, layout, or both.

SYSTEM AND METHOD FOR UNIVERSAL CONTROL OF ELECTRONIC DEVICES

ABSTRACT OF THE DISCLOSURE

A system and method for providing an integrated circuit that integrates with and controls a device wherein the integrated circuit design is developed based on a selection of characteristics of the device. The system and method also provide software for establishing interoperability between the integrated circuit and a controller.

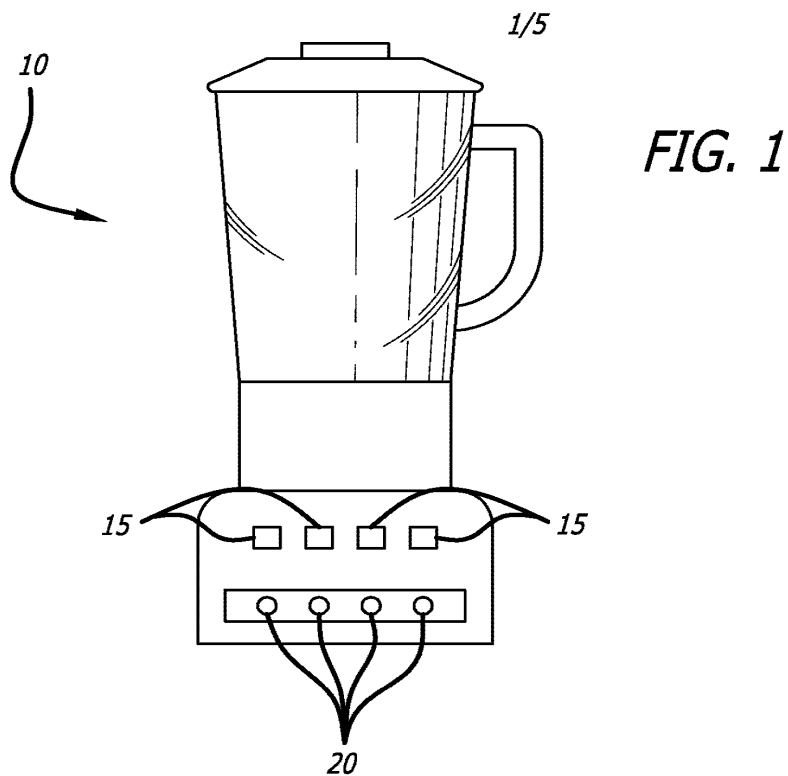


FIG. 2

INTERNATIONAL STANDARD INDUSTRIAL CLASSIFICATION

A. Transportation

- 1.0 Aerospace
- 2.0 Automotive
- 3.0 Maritime
- 4.0 Rail

- 4.1 Amusement
- 4.2 Industrial
- 4.3 Light Rail

4.3.1 Engine Type

4.3.1.1 Diesel

4.3.1.2 Electric

4.3.1.2.1 Specification

4.3.1.2.2 Functions

4.3.1.2.2.1 Control Types

4.3.1.2.2.2 Display Types

4.3.1.2.2.3 Input Types

4.3.1.2.2.4 Output Types

FIG. 3

2/5

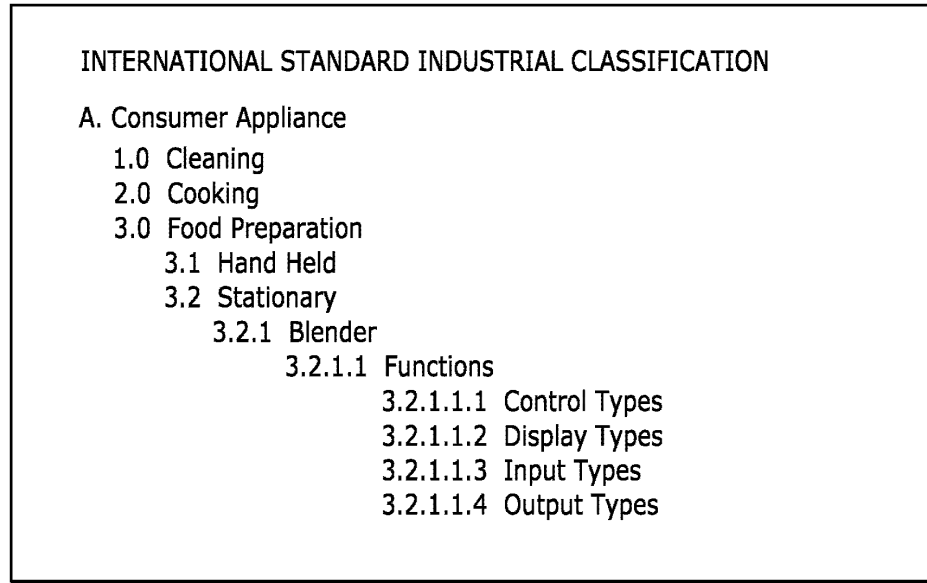
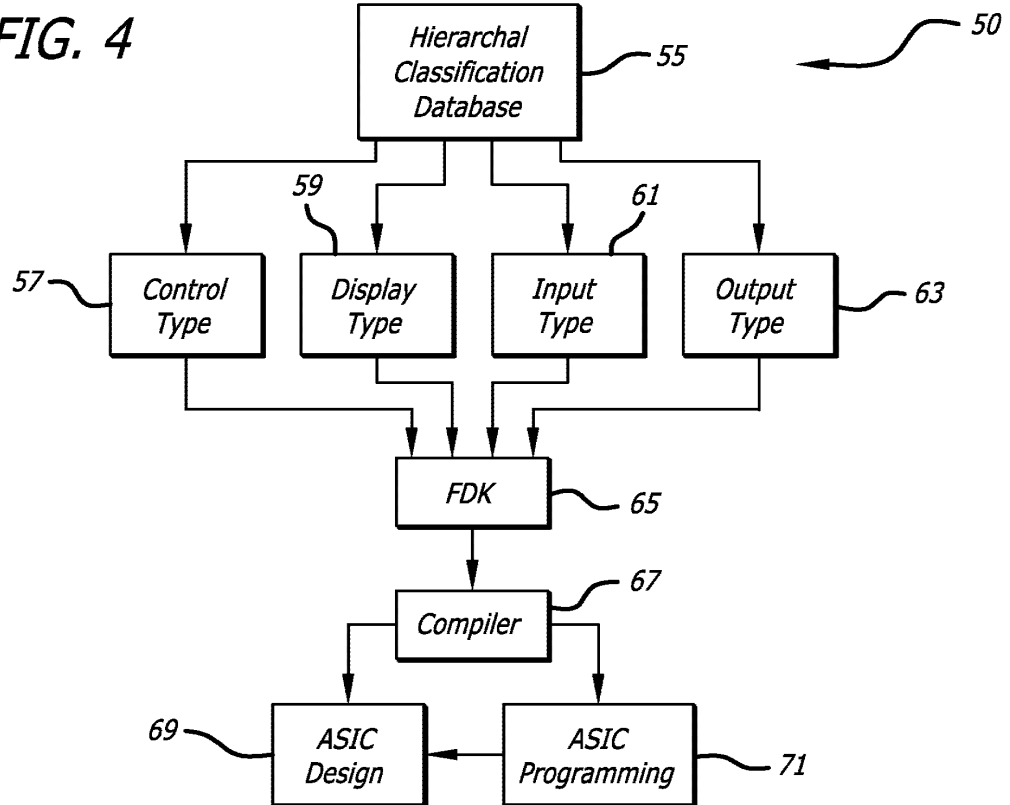
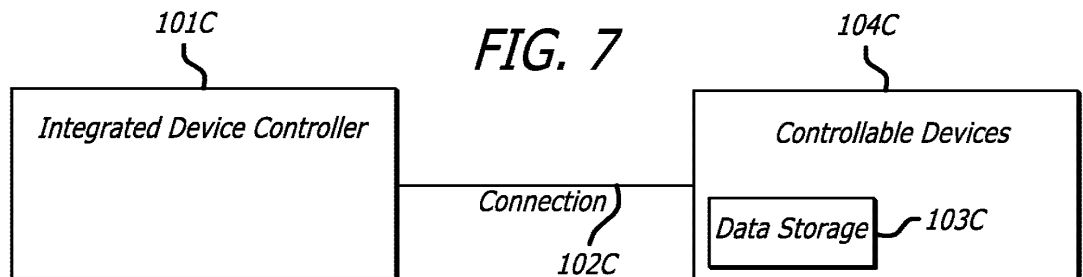
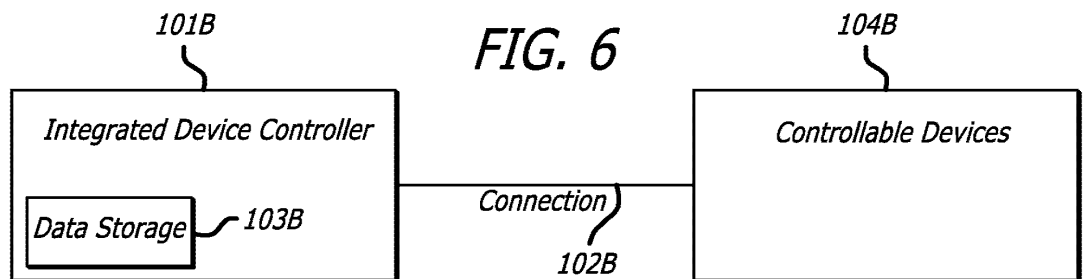
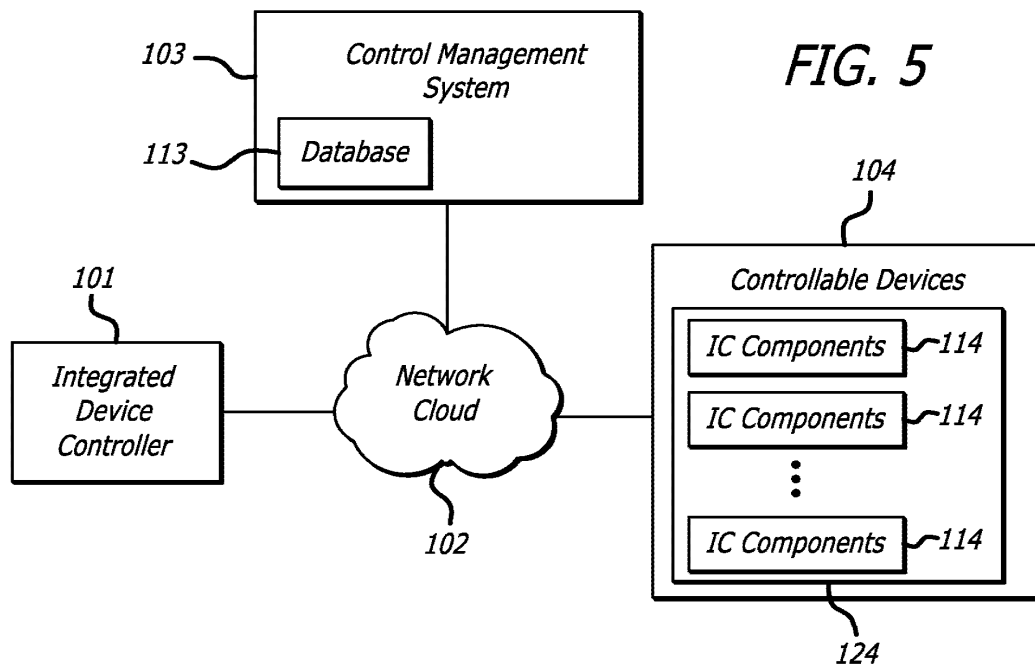
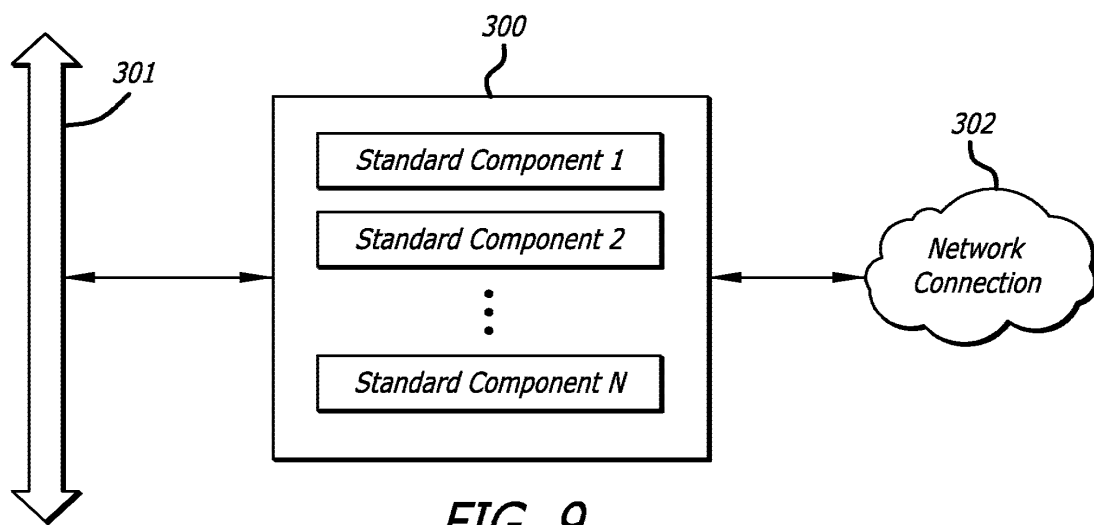
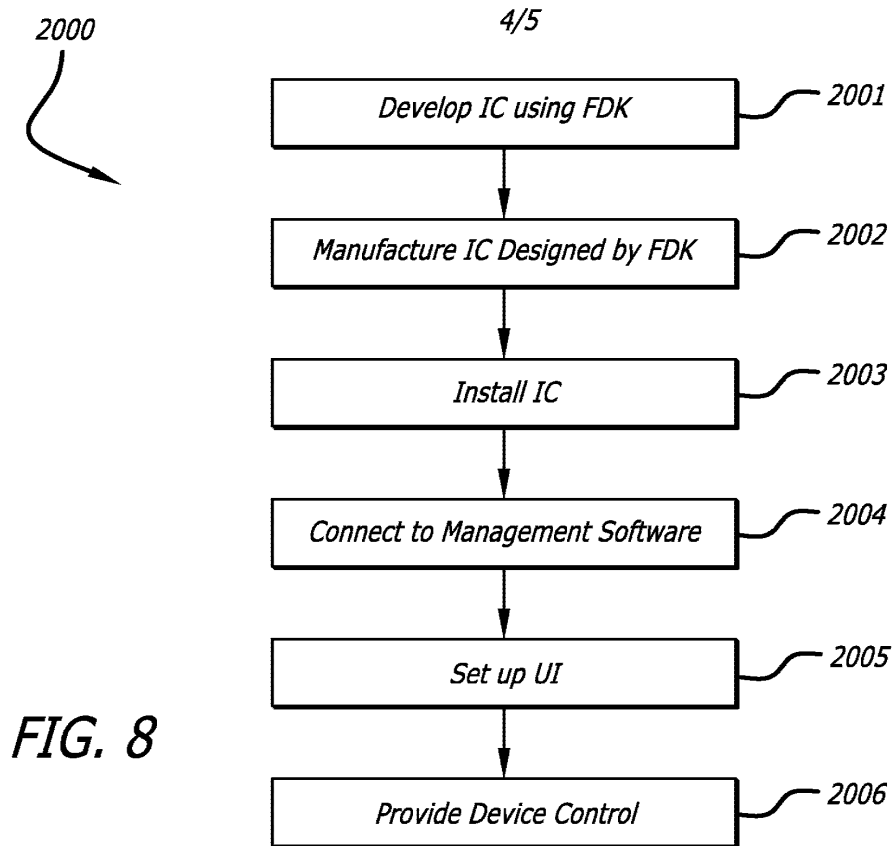


FIG. 4







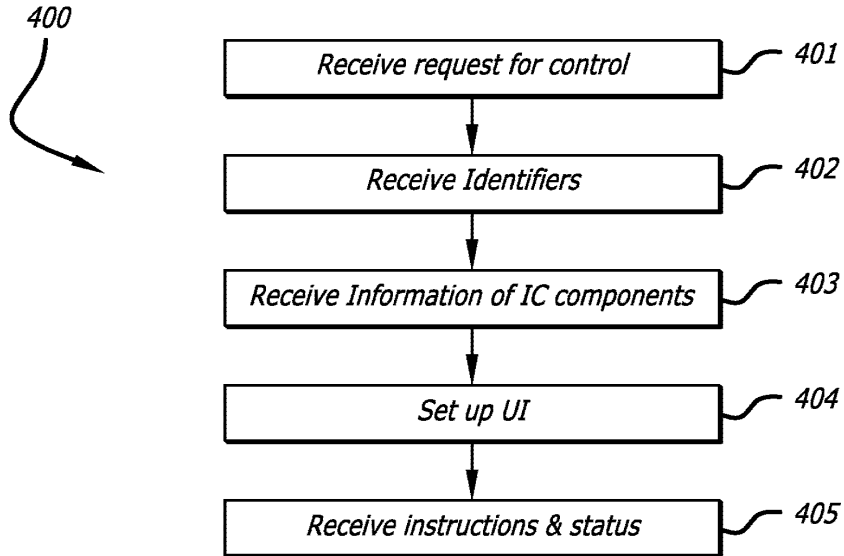


FIG. 10

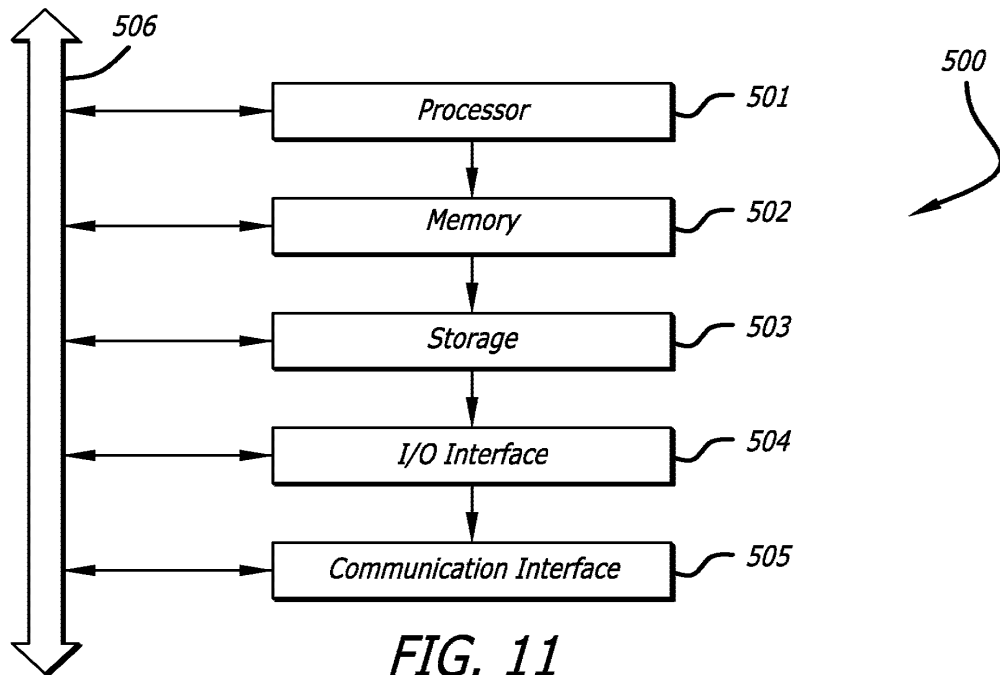


FIG. 11