

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ARM LIMITED,
Petitioner,

v.

ICPILLAR LLC,
Patent Owner.

Case IPR2024-00476
Patent 8,924,899

EXHIBIT 2001

DECLARATION OF JOSEPH C. MCALEXANDER III, P.E.

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I. INTRODUCTION

1. My name is Joseph C. McAlexander ^{III}. I have been retained as an expert witness to provide my independent opinion regarding the matters at issue in *inter partes* review of U.S. Patent No. 8,924,899 (“the ’899 Patent”), IPR2024-00476. I have been retained by ICPillar LLC (“ICP”), the Patent Owner in the above proceedings. Petitioner is ARM Limited. (“ARM” or “Petitioner”).

2. I am being compensated \$625 per hour for my time spent working in connection with this case. My compensation is in no way related to the outcome of this litigation. If called as a witness, I would testify as to the statements and opinions contained in this report.

3. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

II. QUALIFICATIONS

4. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I am a member of a number of professional organizations, including the Institute of Electrical and Electronics Engineers, Inc. (IEEE) and the National Society of Professional Engineers. I have been associated with the integrated circuit and electronics industry as a designer and

consultant for the past fifty-two (52) years. I am a named inventor on thirty-one (31) U.S. patents and a number of foreign patents, including patents directed to current sensors, motion sensors, timing and voltage/current control, signal generation and detection, and conditional response circuits.

5. My skills and experience are in areas of circuit design, simulation, layout and analysis, device fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed and managed development, testing, and evaluation of devices including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant, parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs applications;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control;
- performed testing, analysis, and control involving use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase

contrast and Fast Fourier Transform (FFT) for High Aspect Ratio Inspection (HARI) applications; audio and video system design and installation;

- taught courses in solid state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, pressure sensors, and other); provided nuclear radiation hardness testing services for military and space clients; managed the design and installation of audio sound and video systems for private and commercial enterprises.

6. I also have experience performing intellectual property valuation and patent portfolio work for companies. For example, when I worked at RMC Management, I conducted numerous patent portfolio valuations and negotiated licenses. Also, I was part of a consultant team with ST Microelectronics that performed patent portfolio valuations and negotiated licenses on behalf of ST Microelectronics.

7. Because of my background, training, and experience, I am qualified to provide the expert opinions within this declaration regarding the technology

described and claimed in the '899 Patent. A more detailed record of my professional qualifications is set forth in the attached Exhibit A, which is my *curriculum vitae*, including a list of publications, awards, research grants, and professional activities.

III. BASES OF OPINIONS

8. In the course of conducting my analysis and forming my opinions, I have reviewed materials including those listed below:

- i. The Petition by ARM in IPR2024-00476;
- ii. U.S. Patent No. 8,924,899 (Ex. 1001) (“the '899 Patent” or “'899”);
- iii. The prosecution history of the '899 Patent (Ex. 1002);
- iv. The Declaration signed by Dr. Henry Houh in IPR2024-00476 (Ex. 1003) (the “Houh Declaration”);
- v. U.S. Patent No. 5,870,588 (“Rompaey”) (Ex. 1004);
- vi. U.S. Pat. Appl. No. 2008/0222581 A1 (“Banerjee”) (Ex. 1005);
- vii. *CoWare—a design environment for heterogeneous hardware/software systems*, K. Van Rompaey, D. Verkest, I. Bolsens and H. De Man, Proceedings EURO-DAC '96, Geneva, Switzerland, pp. 252-257 (1996) (Ex. 1006);
- viii. *CoWare—A design environment for heterogeneous hardware/software systems*, Verkest, D., Van Rompaey, K., Bolsens, I. et al. Des Autom Embed Syst 1, 357–386 (1996) (Ex. 1007);

- ix. ICPillar Preliminary Infringement Contentions, '899 Patent (Ex. 1008);
- x. U.S Pat. No. 5,197,016 (“Sugimoto”) (Ex. 1009);
- xii. U.S. Patent No. 4,922,432 (“Kobayashi”) (Ex. 1010);
- xii. Fletcher, William I., *An Engineering Approach to Digital Design*, Prentice-Hall, Inc., pp. 491-505 (1984) (excerpts) (Ex. 1011);
- xiii. ICPillar Opening Claim Construction Brief (Ex. 1012);
- xiv. Arm Opening Claim Construction Brief (Ex. 1013);
- xv. Complaint in *ICPillar v. ARM Ltd. et al*, 1:23-cv-282 (WDTX) (Ex. 1014);
- xvi. Scheduling Order in *ICPillar v. ARM Ltd. et al*, 1:23-cv-282 (WDTX) (Ex. 1015);
- xvii. The exhibits and other documents cited herein.

IV. APPLICABLE LEGAL STANDARDS

A. Level Of Ordinary Skill In The Art

9. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” or “PHOSITA,” as of the time of the invention, which I understand is here assumed to be the effective filing date (May 23, 2013) of the '899 Patent application from which the '899 Patent issued. I

understand that the person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. By “relevant,” I mean relevant to the challenged claims of the ’899 Patent.

10. I understand that factual indicators of the level of ordinary skill in the art include the various prior art approaches employed, the types of problems encountered in the art, the rapidity with which innovations are made, the sophistication of the technology involved, and the educational background of those actively working in the field. I understand that, in assessing the level of skill of a person of ordinary skill in the art, one should consider the type of problems encountered in the art, the prior solutions to those problems found in the prior art references, the rapidity with which innovations are made, the sophistication of the technology, the level of education of active workers in the field, and my own experience working with those of skill in the art at the time of the invention.

11. In this case, Dr. Houh has asserted in his declaration that a person of ordinary skill in the art as of the time of the ’899 Patent would have had:

a Bachelor’s or Master’s Degree in computer science, electrical engineering, or a related field, with at least three years of practical experience in circuit design, digital design, and/or automation tools. Additional experience could substitute for the advanced degree.

Ex. 1003 [Houh-Decl.] ¶ 47.

12. For the purposes of this declaration, I accept Dr. Houh's proposed qualifications of a POSITA. I may, however, revisit the issue, and consider whether I agree with the correctness of Dr. Houh's proposed qualifications for a POSITA, should this case continue.

13. As further discussed below, my opinions, as stated in this declaration, do not depend on whether the Board adopts this or a slightly different level of ordinary skill in the art. For example, as will be discussed throughout my report, even a person with the level of knowledge or experience described by Dr. Houh or adopted by the Board would not have a reasonable expectation of success in implementing certain aspects of the proposed combination as of the priority date of the '899 Patent.

B. My Understanding Of Legal Standards

14. When considering the '899 Patent and stating my opinions, I rely on the following legal standards as described to me by the attorneys for ICP.

15. I understand that a patent claim is unpatentable if the claimed invention was anticipated by a prior art reference or would have been obvious to a person of ordinary skill in the art at the time of the purported invention.

16. I understand that anticipation requires that every limitation of the claim at issue be disclosed, either expressly or under principles of inherency, in a single prior art reference.

17. I understand that inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, it must be proved that the claim limitation not expressly found in the reference necessarily follows from what is found there.

18. I understand that an obviousness analysis involves comparing a claim to the prior art to determine whether the claimed invention would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art and in light of the general knowledge in the art as a whole. I also understand that obviousness is ultimately a legal conclusion based on underlying facts of four general types, all of which must be considered: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness, including any praise of the invention.

19. I also understand that obviousness may be established under certain circumstances by combining or modifying the teachings of the prior art. Specific teachings, suggestions, or motivations to combine any first prior art reference with a second prior art reference can be explicit or implicit but must have existed before the date of purported invention. I understand that prior art references themselves may be one source of a specific teaching or suggestion to combine features of the

prior art, but that such suggestions or motivations to combine art may come from the knowledge that a person of ordinary skill in the art would have had.

20. I understand that a reference may be relied upon for all that it teaches, including uses beyond its primary purpose, but also including teachings that lead away from the invention. I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, although the mere disclosure of alternative designs does not teach away.

21. I further understand that whether there is a reasonable expectation of success in combining references in a particular way is also relevant to the analysis.

22. I understand that it is improper to use hindsight to combine references or elements of references to reconstruct the invention using the claims as a guide. My analysis of the prior art is made from the perspective of a person of ordinary skill in the art at the time of the invention.

23. I am not offering any legal opinions in this declaration nor am I qualified to do so. I only consider such legal standards in framing my opinions and conclusions as well as placing assertions made by Petitioner in the Petition into the proper context. Additionally, from a subject matter perspective, I understand that the petitioner always has the burden of persuasion regarding a challenge of patentability of an invention under an inter partes review.

V. CLAIMS-AT-ISSUE (CLAIMS 1, 5, 6, 8, 14)

24. I understand that Petitioner has challenged independent claim 1, its dependent claims 5 and 6, and independent claim 8, as well as its dependent claim 14, based on obviousness over Rompaey alone or in combination with CoWare I (Ground 1) and obviousness over Banerjee alone (Ground 2).

VI. OPINIONS

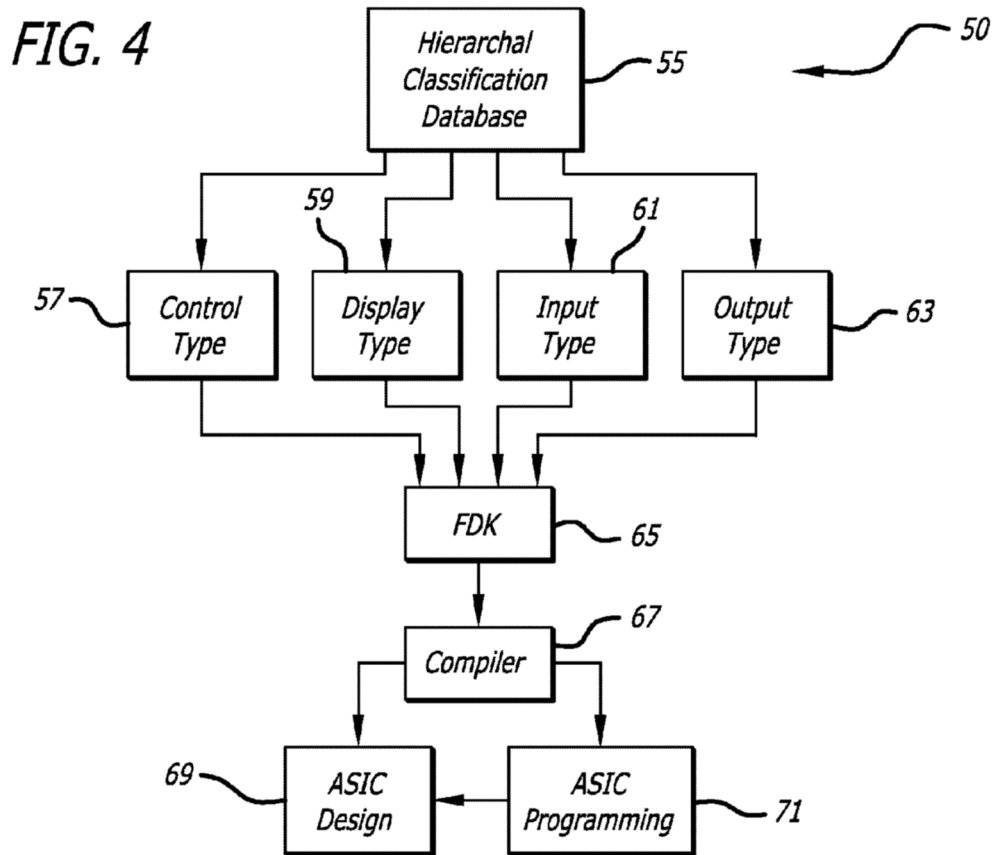
A. Petitioner's Banerjee Ground (All Claims, Ground 2).

1. The '899 Patent and Banerjee.

25. I understand that Petitioner's second ground argues that the claims are disclosed and/or rendered obvious by Banerjee alone. Pet., 57-84. In my opinion, the Petition does not show that Banerjee discloses, or renders it obvious to add, at least claim limitation 1[d] requiring "outputting software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device." Ex. 1001 ['899] cl. 1. Claim limitation 8[e], similarly worded, is also not disclosed or rendered obvious, requiring "output software programming commands to executed by the hardware integrated circuit for controlling the device in accordance with the selection of categorized input and output characteristics of the device using a communication protocol compatible with the device through the communication bus of the hardware integrated circuit." Ex.

1001 ['899] cl. 8. These limitations require outputting software programming commands to be executed by the hardware IC for controlling the device. Banerjee at best discloses intermediate processing steps that only pass between internal modules of Banerjee's design tool, rather than outputting software programming commands to be executed by the hardware IC. Therefore, Banerjee's teachings only address hardware IC design rather than outputting any executable software from the design tool.

26. The '899 Patent's claims are directed toward designing an integrated circuit and associated software to be executed on that integrated circuit. First, as part of a system or a method to design a hardware integrated circuit and associated software programming commands executed by the integrated circuit to control an electronic device, a memory of a processor receives a selection of categorized input and output characteristics of that device. *See, e.g.*, Ex. 1001, cl. 1, limitation 1[a]. After analysis, based on this selection, the processor outputs a hardware integrated circuit design and software programming commands. *Id., e.g.*, cl. 1, limitations 1[b]-[c]; cl. 6; *see id., e.g.*, FIG. 4, 9:19-10:14; *see also, e.g., id.*, 13:6-13:17 ("The FDK may provide a software representation[] of a complete IC design. In one embodiment, the software representation may be a schematic and/or layout."); cl. 8.



'899 Patent FIG. 4 (showing, e.g., outputs 69, 71)

27. The '899 Patent is directed towards an invention “that simplifies and vertically integrates the development of the hardware and software for a universal control system,” performing unified design of integrated circuit hardware and software, including to “provide an IC design based on the selection of input and output characteristics of the device; and provide software for controlling the device through the IC,” and “providing an IC design based on the selection of input and output characteristics of the device; and providing software for controlling the device through the IC.” Ex. 1001 [’899] 3:21-3:22, 5:26-5:28, 5:50-5:52.

28. Specifically, the '899 Patent describes and claims a method and system for designing and outputting a hardware integrated circuit design and software that controls an electronic device when the integrated circuit is integrated into the device. Ex. 1001 ['899], *e.g.*, 18:38-18:40; *see, e.g., id.*, 5:3-5:4 (“In still another aspect, the invention includes providing software for controlling the device . . .”), 9:61-9:64 (“ASIC Programming 71 may be software to be programmed and/or stored in a fabricated ASIC and/or a controller to establish interoperability between the controller, ASIC, and/or a device that the ASIC is integrated with.”), 13:20-13:23 (“the FDK may also provide accompanying software to run with the IC (assuming it is a programmable IC) and/or on a computer to enable remote control.”), 13:36-13:38 (“A developer may send the IC design created using the FDK to a IC manufacturer to manufacture the integrated circuit for integration with a product. In one embodiment, a program provided by the FDK is programmed into the IC for pairing with one or more computers to be used as a controller.”).

29. The '899 Patent's approach renders multiple benefits, such as, *inter alia*, significantly reducing the time needed to design such an integrated circuit by standardizing and designing an integrated circuit using standard components based on device functionality and associated software to run on the resulting integrated circuits. Ex. 1001 ['899], *e.g.*, 4:39-4:45 (“This way, IC devices components may be standardized and designed based on functionality thus removing the necessity of

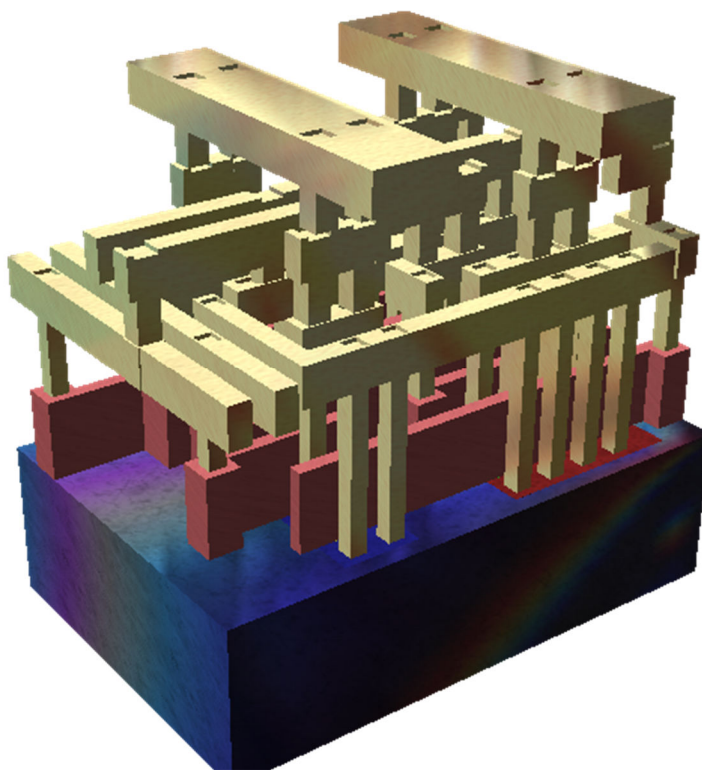
designing a proprietary device in house. A developer can select the functionality of their device and an IC can be designed off the standard components. Furthermore, because standard IC components are used, standard software can be used to control and run on the IC devices.”).

30. The claimed inventions are directed to computer implemented design of an integrated circuit which controls a device when that integrated circuit is integrated into that device, including both a hardware integrated circuit, which may be represented by software, and software programming commands to be executed by the hardware integrated circuit, for controlling that device in accordance with the received selection of the device’s characteristics. Ex. 1001 [’899], *e.g.*, 2:49-2:60, 3:20-3:26, 4:17-4:45; *see, e.g., id.*, cl. 1, limitation 1[d].

31. Banerjee does not disclose the same tool as the ’899 Patent because it only outputs a hardware design but does not output software for executing on that hardware to allow control of a device, much less software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device.

32. Rather, Banerjee describes a design tool “to automatically produce a hardened GDSII description or other representation of” an integrated circuit (IC). Ex. 1005 [Banerjee] Abstract. “Designers select contractual terms for incorporating

third party intellectual property and then design and initiate manufacture of the IC by way of a network portal.” *Id.* This reference to a “hardened GDSII description” of an IC refers to a hardware description file describing the IC design, not software that could be executed on the resulting IC. (As an ordinary artisan at the time of the invention would have known, GDSII, which currently is a de facto industry standard for electronic design automation data exchange of IC or IC layout artwork, is a binary database file format, representing in hierarchical form information about the IC layout such as text labels or shapes such as planar geometric shapes, which may be used for creating photomasks, transferring artwork between tools, reconstructing in whole or in part the artwork when sharing layouts. See Exs. 2002 [GDSI-Data Format], 2003 [GDSII-Layout Editor]), 2004 [Wikipedia-GDSII].) Banerjee describes a system that outputs this “hardened” IC design in the form of a hardware IC description file but says nothing about the creation of software to be executed on the hardware of the IC. *Id.*



Example of GDSII hardware design (source: Wikipedia (Ex. 2004))

33. Banerjee discloses a design tool that “a designer can use to develop the [hardware IC] description file.” Ex. 1005 [Banerjee] [0033], Figure 2. Banerjee’s tool includes functional description module 21, parameter description module 22, workload analysis module 23, OS optimization module 24, and tools (simulation, formal verification) module 25.

34. The functional description module 21 of Banerjee’s tool guides the user, via a user interface, to develop a functional description of the IC to be designed, and also allows the user to upload design scripts for customized elements. *Id.*, [0033], Figures 2-3. Parameter description module 22 guides the user in defining

performance parameters for the functional blocks, which module 21 uses “to optimize the selection of [hardware] functional block components.” *Id.*, [0034].

35. Banerjee’s workload analysis module 23 accepts algorithms or other specifications that describe the workload targets for the IC the user is designing. *Id.*, [0036]. It then performs an analysis of workload targets to analyze the algorithm’s processing loads and identify potential bottlenecks. *Id.*, [0036]-[0037]. This “[i]nformation from module 23 is passed to module 21 and module 22 to optimize the selection of the [hardware] functional block components.” *Id.*, [0036].

36. The workload target algorithm, loosely referred to in Banerjee as “application programming code” more precisely is a script or algorithm containing workload targets used by module 23 for workload analysis in designing an IC. *Id.* The format used by Banerjee to describe the algorithm can be a flowchart, a script written in C or C++ or other format to specify the IC workload targets. *Id.* The result of the workload analysis module is passed to modules 21 and 22 for optimizing the hardware IC design and is never outputted from the design tool. *Id.*; Figure 2. In short, this workload target algorithm is not an output from the Banerjee design tool. It is a data point used within Banerjee’s design tool for optimization of the hardware IC design. More particularly, it certainly is not software programming commands to be executed by the hardware integrated circuit for controlling the

electronic device, like the output software commands expressly required by the '899 Patent's claims' language.

37. Banerjee's OS optimization module 24 is used to optimize the footprint and performance of the operating system by analyzing the workload from the perspective of the operating system. *Id.*, [0038]; Figure 2. Banerjee's module 24 is also used to analyze what the "typical[]" operating system storage and other footprint needs will be for the IC that is being designed, so that these typical requirements can guide the design of the hardware IC. *Id.*, [0072]. Said another way, module 24, "based on a prototype description," compiles the characteristics of the typical or "baseline" "operating system configuration," in order to analyze its expected "footprint" on the IC and how it is expected to be instantiated on the device. *Id.*, [0072]-[0074], [0083]. As Banerjee puts it: "Module 24 enables the configuration of the operating system to minimize its footprint in memory in the finished product," to avoid "inefficient use of memory resources" in the IC design. *Id.*, [0073].

38. As Banerjee explains, module 24's intermediate analysis is not an output from its tool, contrary to what the Petition repeatedly suggests. Module 24 "interfaces with modules 23-21 to determine whether it is preferable to implement certain functions [of the IC] in software rather than hardware." *Id.*, [0038]. For example, if a function requires performing a significant number of multiplication operations, then a hardware multiplication implementation may be deemed preferred

to minimize the need for the operating system to include a software multiplication implementation. Conversely, if multiplication is seldom performed, then it may be area and power efficient to implement the multiplication function in software, even though it will take longer to perform the multiplication. *Id.*, [0039]. As illustrated in Figure 2, the result of analysis of module 24 is passed back to modules 21-23. Banerjee's module 24 does not provide any output from Banerjee's design tool.

39. The tool's module 25 (simulation, formal verification) assembles and outputs a hardware description file. Ex. 1005 [Banerjee] [0040], Figure 2. It specifies the hardware components and operational characteristics in RTL ("Register Transfer Level"). *Id.*, [0040]. As an ordinary artisan would have understood at the time of the '899 Patent invention, RTL refers to a "design abstraction" which models a synchronous digital circuit in terms of the flow of digital signals (data) "between hardware registers," and logical "operations performed on" those signals. Ex. 2005 [RTL Design], 1-2. "Module 25 also performs logic synthesis to compile and optimize the ... circuit description and generate a gate-level netlist representation" of the IC design. Ex. 1005 [Banerjee], [0044].

40. In sum, the Banerjee design tool (computer program 15, *see id.*, [0045]) gathers information regarding the functional description and design parameters of the IC, optimizes the hardware IC design through workload targets and tradeoff analyses between hardware and software implementation and then, outputs an HDL

file descriptive of the hardware IC design. *Id.*, [0045], Figure 2, *see, e.g., id.*, Figure 6 (showing step of “Send netlist to foundry” (67) if “Design acceptable” (66)).

41. In this way, according to Banerjee’s teachings, expected characteristics of an operating system may be used to output a more optimal design for the hardware IC; the operating system “software,” referred to in the cited portions of Banerjee, is an optional input in the hardware design. Banerjee does not disclose outputting software for execution on the newly designed IC. Nor does Banerjee disclose writing or outputting software programming commands for controlling any device with the designed IC.

42. It is my opinion that Banerjee does not disclose outputting software for execution on the newly designed IC. Nor does Banerjee disclose writing or outputting software programming commands for controlling any device with the designed IC.

2. Banerjee Is Not Shown To Disclose Or Render Obvious Claim Limitation 1[d].

43. Claim limitation 1[d] requires:

Outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device.

44. Banerjee’s teachings differ from the ’899 Patent in a number of ways. One of note is that Banerjee’s tool outputs only a hardware description file. It does

not output software programming commands to be executed on the described hardware IC, to control the electronic device into which it is integrated. Where limitation 1[d] (and limitation 8[e]) are concerned, the Petition points to internal analyses of Banerjee’s tool, during the hardware design process, of attributes of the software that might run on the hardware being designed. But the Petition’s citations to Banerjee do not show this; these intermediate analyses do not output executable software commands from the tool, nor do they output executable software commands.

a. Banerjee Does Not Disclose Claim Limitations 1[d]/8[e].

45. The Petition asserts that Banerjee discloses the “software programming commands” of limitations 1[d] or 8[e] because Banerjee supposedly “outputs the hardware circuit design and the related software to implement the designed system.” Pet., 8; *see also, e.g., id.*, 78-80, 83-84. The Petition asserts that limitation 1[d] is met because:

Banerjee’s tool outputs the software specific to the designed system and application thereof and based on the selections identified in 1[a]. EX-1003, ¶¶375-380. The output software includes: (1) the operating system; (2) application software; (3) application specific instruction extensions; and (4) “middleware” (such as I/O device driver software).

Pet., 78. The Petition cites Banerjee at [0038], [0039],[0045], [0046], [0056], [0067], [0078], and [0084] in support, as well as Figure 5, asserting that “Fig. 5

exemplifies how the operating system software is compiled and output,” and that “OS software is generated *and output*” (emphasis added), citing Banerjee at [0075], [0081], and [0083]. Pet., 78-79. Finally, the Petition cites Banerjee at [0038] and [0086] for the proposition that “Banerjee’s tool generates and outputs software instructions related to the application specific instructions.” *Id.*, 79-80.

46. It is my opinion that none of the Petition’s cited portions of Banerjee disclose the output of software, as required by the claims. Instead, the cited disclosures only describe Banerjee’s process of using the desired attributes of what software will be typically executed on the desired IC design in order to optimize the outputted design of the IC, *without* writing software to run on that IC after it is fabricated. Even assuming, for the sake of argument, that Banerjee outputs a hardware IC design that may meet the recited output in claim limitation 1[c], Banerjee does not output any software that meets claim limitation 1[d].

47. The descriptions of the use of application software and operating system software in Banerjee may address the attributes and requirements of executing such software on the resulting IC, but they do not describe any software *output* by Banerjee that is “executed on the hardware integrated circuit for controlling the electronic device[.]” The only output described in Banerjee is a hardware description file: in other words, a file containing the hardware IC design.

Banerjee does not disclose, or render obvious, the output of software executable on the designed IC to control the device.

48. Therefore, it is my opinion that Banerjee does not disclose, or render obvious, the output of software executable on the designed IC to control the device.

i. Banerjee Is Not Shown To Deliver Software

49. The Petition characterizes Banerjee as providing “output software” that is “specific to the designed system and application thereof,” including “the operating system” and “application software” for the IC being designed. Pet., 58-59, 78, 79. This appears to be a misapprehension of Banerjee’s functions.

50. The Petition quotes the following statement in Banerjee as supposedly disclosing outputting software as claimed:

[M]odule 24 outputs C or C++ code that configures the Windows, Linux or RTOS operating system by outputting header files, switches, and a modified makefile. ... Module 24 then determines the optimal configuration for the design by selecting the processor that most closely matches the specified parameters and providing any additional functionality in software either at the application, middleware or operating system level.

Pet., 78 (quoting Ex. 1005 [Banerjee] [0078]). This disclosure in Banerjee does not describe outputting any software programming commands executable on the designed IC recited in the claims.

51. The claims require (referring specifically here to claim 1) not only “outputting by the processor of a hardware integrated circuit design” (claim limitation 1[c]), but also “outputting . . . software programming commands to be executed by the hardware integrated circuit for controlling the electronic device” (claim limitation 1[d]). Ex. 1001 [’899] cls. 1, 8. In contrast, and as discussed previously, Banerjee only delivers a hardware description file, but not software to be executed on that IC. *See* Ex. 1005 [Banerjee], *e.g.*, [0040]; Figures 2 and 6.

52. Banerjee’s descriptions of outputting its IC design are never accompanied by any suggestion that Banerjee is also, with that hardware design, outputting executable software for that designed hardware IC. Banerjee’s disclosure of what it outputs includes only a hardware description file or “netlist,” and does not output any software.

53. For example, Banerjee describes at [0044] module 25 of Figure 2 compiling and optimizing to “generate a gate-level netlist representation of the device.” (Here, “the device” clearly refers to the IC being designed by the tool: it is not referring to an integrated circuit that will be integrated into the designed IC device to control that device.). Notably, Banerjee’s description “of a generalized method of the” tool in Banerjee, at Figure 6 and [0085]-[0093], does not mention outputting software. *Id.*, [0086], [0093]. When Banerjee here states that “the design process is completed,” it has described only a hardware “device” design that is

suitable to be sent “to a foundry.” *Id.*, [0091] (“Preferably, only a hardened design is exported to a foundry at the conclusion of the design process as indicated at 67.”), [0093].

54. The Petition quotes Banerjee’s statement that Banerjee’s “module 24 outputs C or C++ code that configures the Windows, Linux or RTOS operating system by outputting header files, switches, and a modified makefile.” Pet., 78. But this statement in Banerjee merely confirms in even more specific terms that what Banerjee’s module 24 produces—for internal use in the tool only, in any event—is not software, as the Petition appears to mistakenly assume. As the ordinary artisan at the time of the ’899 Patent invention would have recognized, Banerjee’s references here to “header files,” “switches” and “makefiles” are not references to software, because “header files,” “switches,” and “makefiles” do not refer to software. Rather, they refer to information to facilitate developing software. To summarize these briefly:

55. “**Header files**”—Header files contain information that is needed by several different files or functions. A header file contains C-language definitions and structures. Centralizing information into a header file facilitates the creation and update of programs. *See, e.g.*, Ex. 2006 [IBM-Header Files] 1.

56. “**Switches**”— “Switches” here refers to switch statements, which transfer control to different statements within a switch body depending on the value

of the switch expression. They may be thought of as a concept or piece of information akin to an “if...else...if” ladder. *See, e.g.*, Ex. 2007 [IBM-SWITCH] 1.

57. “***Makefile***”—A makefile sets rules, typically a set of rules, to determine which parts of a program need to be recompiled, and issues commands to recompile them. Such a makefile is a way to automate software building procedures and other complex tasks with dependencies. *See, e.g.*, Ex. 2008 [UND-Makefile] 1 (“Makefiles are used to help decide which parts of a large program need to be recompiled.”).

ii. Banerjee’s “Output” Is Data Transmitted Between Internal Modules Of Banerjee’s Tool, Not Executable Software Outputted From Its Tool.

58. I understand that when the Petition quotes Banerjee’s use of the term “outputs,” it appears to be trying to suggest that Banerjee thereby discloses “output[ting]” software alongside the hardware design, as recited in the claims. *E.g.*, Pet., 78 (““Module 24 outputs C or C++ code . . .””) (quoting Ex. 1005 [Banerjee] [0078]). However, such “outputs” in Banerjee refer to information produced in Banerjee’s optimization process that is never output from the tool and is “output” only from one internal module into other internal modules as part of the hardware IC design process.

59. Banerjee’s statement that “module 24 outputs C or C++ code” (emphasis altered from Petition) refers to the optimization module itself during the

process of designing the hardware IC. Banerjee specifically says (and is even quoted in the Petition as saying) that *after* this module “outputs” this “code,” Module 24 “*then* determines the optimal configuration for the design by selecting the processor that most closely matches the specified parameters and providing any additional functionality in software either at the application, middleware or operating system level.” Ex. 1005 [Banerjee] [0078]. Here, “the design” refers specifically to the IC for which the hardware description file is being created, as shown by Banerjee’s statement that it is using these “specified parameters” of a functional specification in “selecting the processor,” which is hardware, not software.

60. To repeat, the claims of the ’899 Patent require, in summary, outputting *both* (i) a hardware IC design, *and* (ii) software programming commands executable on the designed IC to control the electronic device whose characteristics formed a basis for the IC’s design. *See* Ex. 1001 [’899] cls. 1, 8; *see also id.*, 5:3-5:8, 5:13-5:14, 9:61-9:62; 13:20-13:23. In contrast, Banerjee does not disclose outputting or delivering any executable software.

61. The reference in Banerjee to outputting “code” does not mean that Banerjee is disclosing outputting from its tool executable software programming commands as recited in and required by the claims. Rather, it is a reference to, specifically, “outputting header files, switches, and a modified makefile” corresponding to the “operating system.” Ex. 1005 [Banerjee] [0078]. These files

contain information to facilitate the creation of programs in the future. They are not software programs themselves. It is a reference to establishing the necessary “parameters” for the software functionality that the IC must be designed to support, as part of “the optimization process” for designing the IC. *Id.*

62. This is further confirmed by Banerjee’s next paragraph, which clarifies that this is a hardware design selection process, not an outputting of executable software for the IC. As Banerjee explains in the next paragraph, this “optimization process” is based on parameters of an “operating system footprint” used to optimize the IC design:

To illustrate the optimization process, consider the process of multiplying two numbers. In one design, the processor can include a high performance hardware multiply unit. In another embodiment, the design may simply bring in a floating point emulation repository that the user could explicitly access by selecting a floating point unit or not. In yet another embodiment the designer may simply specify performance (rate of megaflop), or go a step farther and give computer program 15 an application to profile and to select the optimal configuration.

Ex. 1005 [Banerjee] [0079]; *see also id.*, [0078] (“By way of illustration, the designer can provide module 24 with a range of possibilities such as 1 megabyte of memory, restrict the processor to be no bigger than 3 mm² while meeting certain performance metrics.”). Each of these descriptions in Banerjee concern optimizing

the IC's hardware design, not writing or outputting software that will run on the IC to control a device after the IC is fabricated.

63. The Petition's citations to Banerjee at [0038], [0045], [0046], [0056], [0067], [0075], [0081], [0083], and [0086], Pet., 78-79, do not change this conclusion, but, rather, confirm and reinforce it. Banerjee at [0038] and [0086] describes how to optimize *hardware* "processor design" (such as "reduc[ing] the processor die size and gate count") based on desired hardware and software characteristics, such as "determin[ing] whether it is preferable to implement certain functions in software rather than hardware." It does not describe writing, or outputting from its tool, software programming commands.

64. Meanwhile, Banerjee at [0045]-[0046] and [0056] describes hardware design choices such as "cache line size" and generating an "HDL file descriptive of the design," where the "H" stands for hardware, not software, *id.*, [0004], and modifying this HDL file based on the desired "features and functionality" and "storage requirements" of the expected "application" software and operating system code. Here too, there is no description of outputting software to execute on the IC thus designed. Banerjee at [0067], [0075], and [0081] describes how Banerjee's optimization process "provides quantitative information on the application software including code structure, critical components, risk areas etc." by selecting attributes based on the configuration of software which the hardware will need to "operate in

conjunction with”; again, existing software requirements are quantified or characterized for optimization purposes, but no creation or producing of a tool output of software for execution on the new IC is disclosed. At [0067]-[0069], Banerjee further refers to workload analysis for identifying “instructions” that may be executed by the to-be-designed processor to, for example, “achieve the intended results quickly and efficiently.” Yet Banerjee makes clear that this “identif[ication]” of such “instructions” is not the generation or outputting of executable software programming commands; rather, this simply describes an analysis of “the optimal configuration” of the hardware, such as its DSP “blocks,” to achieve potential “savings in power and die area,” reflected in “the description file” in hardware description language. *Id.*, [0069].

65. Next, Banerjee at [0083], describes how Banerjee’s optimization module, “based on a prototype description,” compiles the characteristics of the typical or “baseline” “operating system configuration,” to be executed on the IC once it is fabricated, in order to analyze its expected “footprint” on the IC and how it is expected to be instantiated on the device. Ex. 1005 [Banerjee] [0083]; *see also id.*, [0072]-[0074].

66. Petitioner’s characterization of these disclosures, as output of software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized

input and output characteristics of the electronic device, is not correct. Pet., 78-80. Banerjee uses the attributes and requirements of software that is expected to be run on the IC under design to optimize that design prior to outputting the hardware related design. But Banerjee only outputs a hardware description file. See Ex. 1005 [Banerjee], e.g., [0044], [0069]. It does not output newly written (or rewritten) software. See *id.*, [0084] (explaining that Banerjee’s tool helps avoid “having to rewrite” software that is already available).

67. Based on my analysis, it is my opinion that Banerjee does not disclose the claims of the ’899 Patent.

b. Banerjee Does Not Render Obvious Claim Limitations 1[d] or 8[e].

68. Again, Petitioner relies upon Banerjee alone to render the claims of the ’899 Patent obvious under Ground 2. Pet., 57-60 (contending that “Banerjee discloses all features of the Challenged Claims” and “discloses, and/or renders obvious, the Challenged Claims”) (capitalization altered). I see no argument in the Petition that it would be obvious to modify Banerjee, alone, to add claim limitations 1[d]/8[e]. Pet., 78-80. As shown above, Banerjee does not disclose these claim limitations. Instead, Petitioner only contends that limitations 1[a], 1[b], and 8[a] would be obvious. *Id.*, 69-72 (alleging that claim limitation 1[a] is “obvious”), 76-77 (same, 1[b]), 80 (same, 6), 81 (same, 8[a]).

69. Therefore, I do not see any showing by the Petition that Banerjee renders obvious claim limitations 1[d] or 8[e].

B. Petitioner's Rompaey And CoWare I Ground (All Claims, Ground 1).

1. The '899, Rompaey, and CoWare I.

70. I understand that Petitioner's first ground argues that the claims are disclosed and/or rendered obvious by either Rompaey alone, or in the alternative solely as to the preamble of Claim 1, obvious in view of Rompaey in combination with CoWare I. Pet., 16-60; *see id.*, 37-40 (citing CoWare I as to cl. 1 preamble). In my opinion, similar to Banerjee in Ground 2, the '899 Patent and Rompaey disclose different tools. In ways similar to Banerjee, Rompaey is not shown to output by its tool software programming commands to be executed on an outputted hardware design, as claimed.

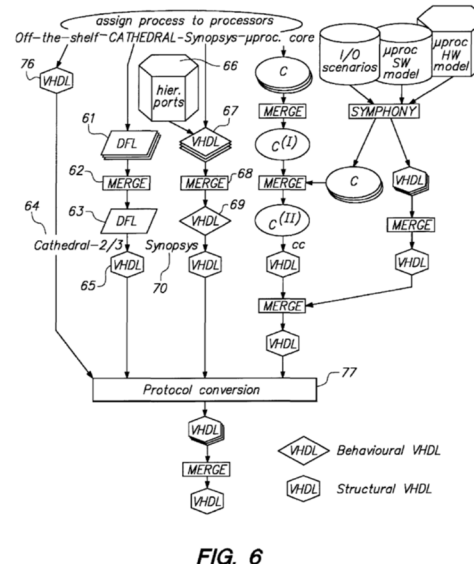
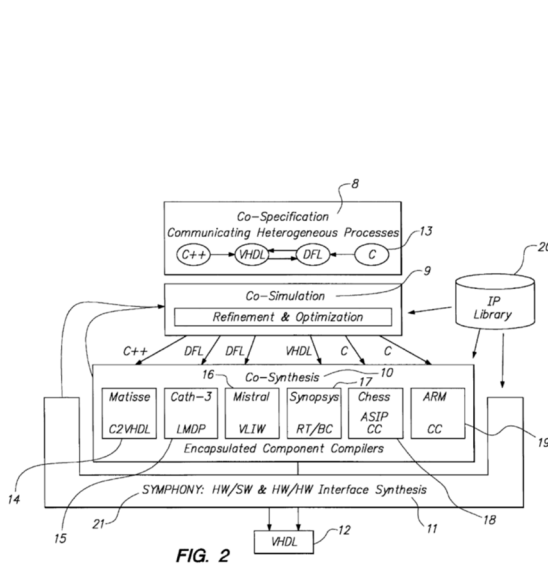
71. Rompaey is a reference from 1996, nearly two decades before the '899 Patent, and contains no description of now-common types of ICs such as SoCs. As I discussed previously, the '899 Patent describes and claims a method for designing a hardware integrated circuit, which controls an electronic device when integrated into the device, and associated software executed by the integrated circuit to control the device. *Id.*, *e.g.*, cls. 1, 8.

72. Rompaey discloses a design tool that fundamentally differs from the '899 Patent. Rompaey's design tool outputs a hardware design, based on a different

design methodology than the '899 Patent. Rompaey's design tool does not output software, including software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device, as recited in and required by the claims.

73. Rompaey discloses a design tool that uses a (convoluted) “encapsulation” scheme in connection with “a data-model” and outputs a “VHDL” file, which is a hardware description file that describes a hardware integrated circuit. Ex. 1004 [Rompaey] Figures 2, 6, 1:54-60, 2:42-46, 6:9-18 (“A hardware/software co-design environment and design methodology based on a data-model that allows one to specify, simulate, and synthesize heterogeneous hardware/software architectures from a heterogeneous specification is disclosed. The environment and methodology of the present invention are based on the principle of encapsulation of existing hardware and software compilers and allow for the interactive synthesis of hardware/software and hardware/hardware interfaces.”). This reference in Rompaey to a “VHDL” type of file refers to a hardware description file describing the IC design. Rompaey expressly states that “VHDL” refers to “Very High Speed Integrated Circuit (VHSIC) Hardware Description Language,” which, Rompaey correctly notes, is a “hardware description language”. *Id.*, 1:54-60. Multiple figures

of Rompaey depict this “VHDL” as the sole output from the design tool. Two such figures are shown below.



Ex. 1004 [Rompaey] Figures 2, 6.

74. Rompaey defines a hardware/software co-design as a digital system containing both high and low data-rate blocks in the signal path, where the high data-rate blocks are synthesized in hardware and low data-rate blocks are implemented on programmable processors. Ex. 1004 [Rompaey] 4:9-14. Rompaey also discloses that “hardware subsystems comprise any one or more of processor cores, off-the-shelf components, custom components, ASIC, processors, and boards.” *Id.*, 6:49-53. The software subsystems comprise machine instructions for the off-the-shelf programmable processors. *Id.*, 5:35-37, 6:49-53, 18:25-27. Machine instruction or machine code is an instruction for the processor to perform a specific task in a digital binary form, *e.g.*, long sequence of zeros and ones. Thus, throughout Rompaey’s

disclosure, references to software subsystems and software generally concern machine instructions or codes for off-the-shelf programmable processors.

75. Rompaey explains that hardware and software may be “designed separately” or else “co-design[ed],” and that when they are, the “hardware components” may be designed “in a specific hardware description language such as Very High Speed Integrated (VHSIC) Hardware Description Language (VHDL) or VERILOG for the hardware components and a software description language such as C or assembler for the software components.” *Id.*, 1:12-16, 1:54-62. Rompaey is directed to a “hardware/software co-design environment” involving “a simulation of the digital system” to assist creation of a “specification” for “an heterogeneous essentially digital system,” “the specification having hardware and software aspects.” *Id.*, 6:6-9, 6:18-36, 8:48-58, 9:14-15. Rompaey further discloses that its “design environment . . . includes means for creating processor models of the hardware components as objects in the database, the models comprising software models representing the software views on the hardware components and hardware models representing the hardware views on the hardware components.” *Id.*, 8:4-10. Rompaey explains that in its system it continues to be true that “[d]ifferent description languages are needed to allow each system component to be described with the most appropriate paradigm.” *Id.*, 5:58-61.

76. Rompaey describes a “specification having hardware and software aspects,” in which “the implementation comprises hardware and software subsystems of the system, where the software subsystems are executed on one or more of the hardware subsystems.” *Id.*, 8:48-58, 9:16-24. Here, the “software subsystems” do not refer to application software, operating system, or software programming commands, but to machine instructions to program a programmable processor, which is a type of processor having hardware that is programmable by machine instructions to operate in different ways. *Id.*, 6:51-53, 9:25-33. While Rompaey notes that this “implementation comprises hardware and software subsystems,” Rompaey’s tool does not output both a hardware design and software executable on that hardware, as the claimed invention requires. Rather, Rompaey outputs only “a net list comprising the layout information of the implementation”—which refers to a hardware IC design, rather than software that may be executed on a designed IC to control a device. *Id.*, 9:16-24.

77. I understand that the Petition repeatedly cites “SYMPHONY” in connection with Rompaey’s tool supposedly outputting software programming commands. Pet., *e.g.*, 48 (asserting that “The discussion in [*sic*] element 1[b] above regarding “SYMPHONY” highlights this output of software specific to the designed software [*sic*].”), 49.

78. Rompaey discloses that, where the processor is “a programmable processor, the implementation of inter-process communication comprises the steps of generating device drivers and of generating hardware interfaces. A software tool is used to achieve this. This tool is called SYMPHONY[.]” *Id.*, 17:59-63. SYMPHONY runs a “model” of “the target processor and a library of I/O scenarios ... for that processor,” allowing the processor to be simulated. *Id.*, 17:65-18:12. Rompaey teaches that this software modeling tool, by supplying “performance figures,” “will allow the designer or SYMPHONY to make a decision about what I/O scenario to use for which port.” *Id.*, 19:13-16. In other words, SYMPHONY will model the software subsystem and I/O scenarios to provide performance figures that can help inform the hardware design of the IC, although, as Rompaey explains, “the user can always override the proposed assignment.” *Id.*, 19:54-55. Further, “[t]he result of SYMPHONY is a refinement of the original host language encapsulation into a CoWare encapsulation of which the behavioral interface is identical to that of the original encapsulation. SYMPHONY effectively replaces a software encapsulation by a hardware encapsulation that has equivalent functionality.” Rompaey, 20:26-31, Figure 7.

79. Rompaey’s cited mentions of “software” do not suggest, contrary to what the Petition seems to assert, that Rompaey outputs software to execute on a new hardware IC design. Rompaey outputs a hardware IC design in, for example,

VHDL. All that the cited teachings of Rompaey describe is delivering a hardware description. The references to “software” are not references to generating software programming commands executable on a designed hardware IC.

80. Contrary to what the Petition suggests, Rompaey does not disclose outputting software for execution on a newly designed IC. Nor does Rompaey disclose writing or outputting software programming commands for controlling any device with the designed IC.

81. Based on my analysis, Rompaey delivers to its users only a hardware description, rather than a hardware IC design and software programming commands executable on that IC.

2. Rompaey Is Not Shown To Disclose Or Render Obvious Limitations 1[d] or 8[e].

82. Claim Limitation 1[d] requires:

Outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device.

Claim limitation 8[e] is similar, as I have already discussed above.

a. Rompaey Does Not Disclose Claim Limitations 1[d]/8[e].

83. The Petition asserts that Rompaey discloses the output “software programming commands” of limitations 1[d] and 8[e] because supposedly “Rompaey discloses that CoWare outputs software programming commands to be

executed by the hardware circuit,” referring to the “SYMPHONY” software tool discussed in Rompaey. Pet., 48-49. It appears to me that the Petition misapprehends Rompaey’s cited disclosures. Furthermore, even if Rompaey outputs a hardware IC design that may meet the recited IC design output, Rompaey does not output any software that would meet claim limitations 1[d] and 8[e].

84. The descriptions of the use of “SYMPHONY” in Rompaey are not referring to the output of the design process, but the “modeling,” partway through the hardware design process, which is intended by Rompaey to inform decisions how to assign, *e.g.*, the ports of programmable processors.

85. Although the Petition contains partial quotations of Rompaey that refer, for example, to “software,” Pet., 49 (quoting Ex. 1004 [Rompaey] 25:29-26:49), when these portions of Rompaey are read in full, they make it perfectly clear to artisans that when Rompaey refers to the “software” on the chip to be designed, it is referring to such “software” in the context of what is “in” a “model.” *See* Ex. 1004 [Rompaey] at, *e.g.*, 11:12-35.

86. Rompaey’s “model” includes, *inter alia*, “processes,” providing “modularity” in the model, which “are used to describe the system components.” *Id.*; *see also, e.g., id.*, 8:4-8:38. “A process is a container for a number of host language encapsulations of a component.” *Id.*, 11:40-11:41. Rompaey’s use of software-sounding terms such as “processes,” are not references to executable

software programming commands, like the claims require; rather, they refer to parts of a “model” that Rompaey teaches can create, at an abstract level, “a description of the component,” facilitating among other things simulation of “the communication behavior of the system,” including modeling of the programming of these components in particular programming “languages,” such as “C”, and how they will communicate using so-called “ports.” *See, e.g., id.*, 8:4-8:38, 11:39-11:57, 12:57-61, 14:41-14:46, 16:61-16:65, 17:3-17:7.

87. Rompaey teaches:

By using primitive channels, ports, and protocols, the designer first concentrates on the functionality of the system while abstracting from terminals, signals, and handshakes. Once the designer is convinced that the processes of the system are functionally correct, the communication behavior of the system can be refined.

Id., 14:41-46; *see also id.*, 16:42-65. In sum, Rompaey’s references to “channels,” “ports,” “protocols,” and “processes” are all references to what is being modeled in Rompaey partway through its design process, and not to actual hardware or executable software.

88. In the model, these “ports” are not actual physical ports any more than the “processes” are actual software processes. Rather, in Rompaey’s model, the “[p]orts are objects through which processes communicate. *Id.*, 12:57; *see, e.g., id.*, 8:4-8:14 (describing Rompaey’s “design environment” as including “processor

models of the hardware components as objects in the database,” with “I/O scenario models of the ports as objects in the database, the I/O scenario models representing the implementation of the ports on the hardware components”). “A primitive port is characterized by a protocol and a data type parameter.” *Id.*, 12:57-59; *see also id.*, 12:64-67 (“Protocols define the communication semantics of a port. . . . Each primitive protocol indicates another way of data transport.”). “For example, the primitive protocol used to model the memory port of a processor will have an index to model the address of the data that is put on the memory port.” *Id.*, 13:15-18; *see also, e.g., id.*, 15:31-37 (“A primitive protocol determines the communication semantics, but not the communication implementation; it does not fix the timing diagram used in the communication. . . . Hierarchical protocols are high level models for alternative implementations of a primitive protocol: they preserve both data direction and control direction of the primitive protocol.”). And, for example, “[a] channel is a point-to-point connection of a master port and a slave port.” *Id.*, 13:41-42; *see also id.*, Figure 7, 17:65-18:46 (further describing Rompaey’s use of SYMPHONY “software model,” discussed further below).

b. Rompaey Models Software, But Does Not Output It.

89. I do not see any indication that any of Rompaey’s modeling of designs lead to any output of executable software, let alone software programming commands to be executed on a designed hardware IC to control a device.

90. Rompaey’s “model” can be used to create “a representation of the system” and its results can be used “to analyze, manipulate, and refine the system description.” Ex. 1004 [Rompaey] 15:50-57. Once this modeling, simulation, or “synthesis” of the hardware and software behavior is complete, “[t]he final step is to link all the synthesis and hardware descriptions to drive commercial back-end tools to generate layout.” *Id.*, 12:44-49. “Layout” denotes hardware description, not software programming commands. This final step is shown in Rompaey’s Figure 2: the output deliverable is an IC design in hardware description language (feature 12).

91. This modeling in Rompaey’s design process is a “model,” not the real thing. *See id.*, e.g., 13:42-51 (“Two ports that are connected by a channel can exchange data. . . . A primitive channel provides for unbuffered communication. . . . In software it is implemented with a (possibly in-lined) function call. In this way, primitive channels model the basic communication primitives found back in software”). Rompaey does not output or deliver any software programming commands executable by a hardware IC being designed by the system.

92. The Petition cites to several disclosures in Rompaey for support that Rompaey meets limitations 1[d] and 8[e]. Pet., 48-49. It is my opinion, however, that the Petition’s citations to Rompaey are descriptions of software modeling or hardware description language, not executable software as required in claim limitations 1[d] and 8[e].

93. Leaving aside for the moment the Petition’s references to Rompaey’s “SYMPHONY” tool, which I will discuss below, the disclosures in Rompaey that the Petition, at 48-49, cites as supposedly describing the output of executable software programming commands, as recited in the claims, all refer to either hardware descriptions or models of potential characteristics of software that might be used on the IC that is to be designed. None of them refers to executable software delivered as an output from the tool.

94. For example, I will list specific citations the Petition makes to Rompaey, and what they actually describe:

i. “Fig. 7” and “6:45-53” (Pet., 48).

95. Figure 7 of Rompaey literally shows a software (“SW”) “model.” As for “6:45-53,” it describes the tool or tools disclosed by Rompaey, which includes “hardware subsystems and software subsystems,” which may include “machine instructions,” or binary programming for programmable processors. But this does not describe what outputs the tool delivers and does not change the fact that Rompaey ultimately outputs only a hardware description file. Ex. 1004 [Rompaey] at *e.g.*, Figures, 2, 6.

iii. “8:4-38; 26:14-30; claims 6-8, 27-37; TITLE; Abstract” (Pet., 49)

97. Rompaey at 8:4-38 describes modeling of ports, not executable software outputs. Rompaey at 26:14-30 is discussed above. Rompaey’s cited claims are describing Rompaey’s tool, not the *outputs* of that tool. Rompaey’s title and abstract, like the rest of its written description, nowhere state that Rompaey generates or outputs software programming commands executable on the hardware designed in light of Rompaey’s modeling and simulation of what that hardware might be used for.

98. It is my opinion that none of the citations from Rompaey relied upon by the Petition disclose claim limitation 1[d]’s requirement of outputting software programming commands to be executed on the hardware designed in Rompaey’s process, let alone for controlling a device whose characteristics formed a basis for that design.

c. “SYMPHONY” Does Not Output The Claimed Software.

99. I understand that the Petition asserts that Rompaey’s discussions of its “co-design” software tool, “SYMPHONY,” “highlight[] this output of software specific to the designed software.” Pet., 48. However, no such “output of software” occurs. The claimed limitation concerns outputting software executable on the IC, not the “designed software,” and so there is no indication Rompaey teaches the limitation. Even if the Petitioner had meant to say the “designed hardware” rather

than “designed software,” that assertion is equally unsupported by Rompaey’s disclosure. Rompaey’s disclosures do not describe any output software programming commands by Rompaey that could be executed on the designed IC. The only output described in Rompaey is a hardware description file: in other words, a file describing the hardware IC design.

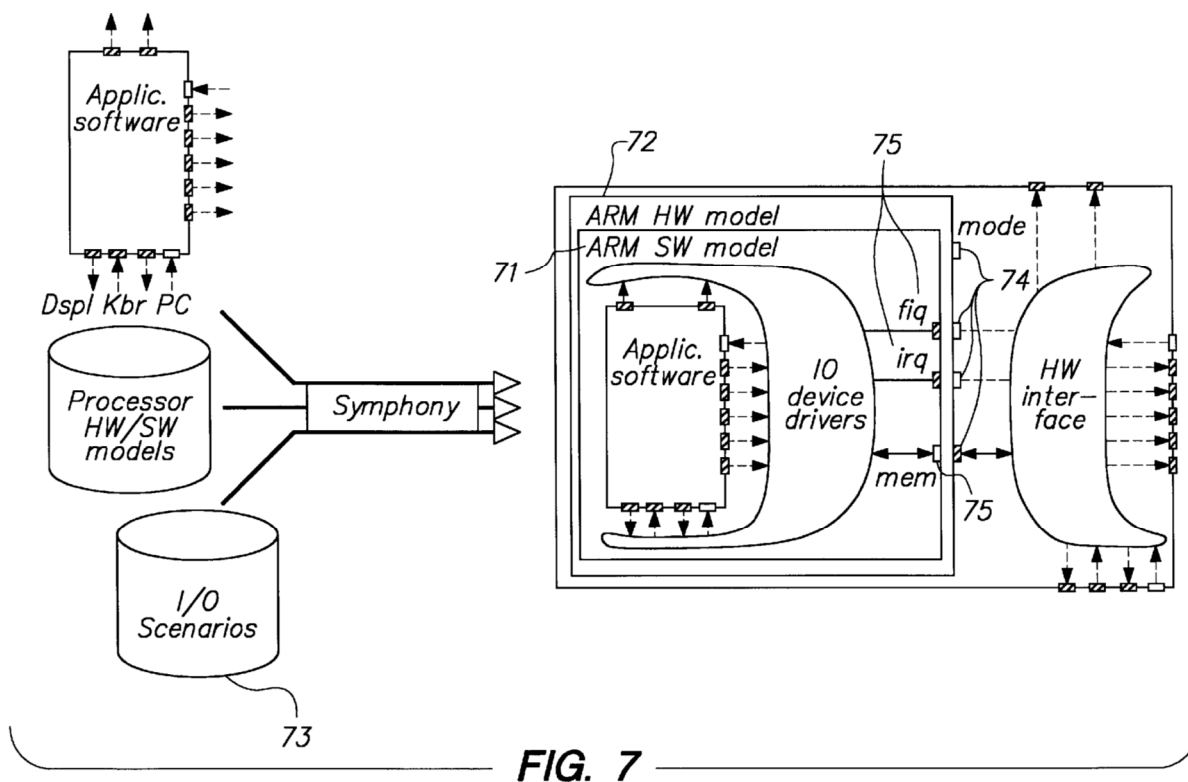
100. The Petition quotes Rompaey’s statement that “In addition, SYMPHONY, adds RAM and ROM blocks to store the program code and data”. Pet. 48 (quoting Ex. 1004 [Rompaey] 20:22-25). This disclosure in Rompaey describes the use of SYMPHONY, partway through the hardware design process, to make decisions about adding hardware components; it says nothing about outputting software. “RAM and ROM blocks to store the program code and data” can store information, but they are *hardware*, not software programming commands.

101. Nowhere does Rompaey say that it specifies or outputs “the program code and data” that will actually be stored in these components once the described designed IC has been fabricated. Nor could it: the only output described by Rompaey of this design process is a file in *hardware* design language, which could not specify such *software* program code and data even if that were desired.

102. The Petition further points to Rompaey’s Figure 7, which it erroneously asserts “shows the output of hardware and the associated ‘applic. Software’ and ‘IO device drivers’ to interface with the display, keyboard, and program controls.” Pet.,

48. This interpretation of Rompaey's Figure 7 is not correct and seems to confirm that the Petition has misapprehended Rompaey's disclosure of modeling to refer to actual software.

103. Figure 7 of Rompaey clearly depicts these features as being within, and part of, the Rompaey process's "SYMPHONY" "modeling":



104. As already mentioned above, Section II.B.2, this "software modeling" in Rompaey is performed to supply "performance figures" that "will allow the designer or SYMPHONY to make a decision about what I/O scenario to use for which port." Ex. 1004 [Rompaey] 19:13-16. The result of SYMPHONY is to replace the software encapsulation with a hardware encapsulation that has the same

functionality. *Id.*, 20:26-31. In other words, SYMPHONY models the system and provides performance figures that can help inform the hardware design of the IC. It is not the end or output of the design process, and this is a model of the system, not the actual executable software itself.

105. The same goes for Rompaey's statement cited in the Petition of concerning "I/O device driver software." Pet., 49. Contrary to the Petition's insinuation, this is only a step toward generating what is actually the output of the tool: the hardware description file. It is not generated software programming commands to be executed on the described, designed IC for controlling a device.

106. In sum, for each of the reasons above, the Petition's assertions that these disclosures in Rompaey are directed to outputted software that may be executed on the designed IC to control an electronic device are contrary to Rompaey's disclosure.

d. Rompaey Does Not Render Obvious Limitations 1[d]/8[e].

107. The Petition asserts that if "Rompaey does not expressly disclose this element, Rompaey renders obvious this element" because "Rompaey's teachings are devoted to converting the design of an 'application' (such as the 'pager application') into the hardware integrated circuits and software implementing that design." Pet., 49. I note that the Petition does not include CoWare I in its alternative obviousness argument. Regardless of CoWare I's inclusion, I disagree with Petitioner.

108. Rompaey does not disclose any outputting by the design tool of any software at all, let alone any software that is to be executed by the fabricated IC that is being designed. And more specifically, Rompaey neither discloses nor suggests outputting by the processor, as claimed, software programming commands to be executed by the hardware IC being designed for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device.

109. Thus, in my opinion, Rompaey neither discloses nor renders obvious claim limitations 1[d] or 8[e].

110. My opinions herein are current as of this stage of this proceeding. I may further develop these opinions or offer additional opinions after a decision to institute, should the Board decide to do so.

VII. CONCLUSION

111. Although my complete opinions are set forth above, for convenience I summarize several points of my opinions in conclusion. For the foregoing reasons, based on my expertise and experience and the record of this case that I have reviewed, it is my opinion that:

- '899 Patent Claims 1 and 8, as well as their dependent claims 5, 6, and 14, are not disclosed by or rendered obvious over Banerjee;

- '899 Patent Claims 1 and 8, as well as their dependent claims 5, 6, and 14, are not disclosed by or rendered obvious over Rompaey alone or in combination with CoWare I.

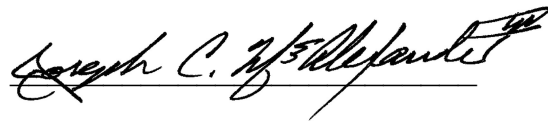
112. I understand that my opinions discussed above support a legal conclusion that claims 1, 5, 6, 8, and 14 are nonobvious and not anticipated.

In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Respectfully submitted,

Dated: May 9, 2024

A handwritten signature in black ink, reading "Joseph C. McAlexander III", written over a horizontal line.

Joseph C. McAlexander^{III}, P.E.

EXHIBIT A

PROFESSIONAL SUMMARY

Currently a Registered Professional Engineer (#79454) and recognized as an inventor on 31 US and a number of foreign patents, I am President of McAlexander Sound, Inc., and the Managing Director of McAlexander Sound Pte Ltd. I have focused my expertise to support a number of clients in product, process, and operations analysis and investigation. Forty-eight years of experience in microcircuit and semiconductor technologies has developed my skills in areas of circuit design and analysis, device fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations and respective areas of quality, reliability, and defect / failure analysis. I am also the President and CEO of MDFHoldings, Inc., an IP holding company currently engaged in the field of GPS Tracking, and was formerly, among others, a Manager with QM Partners, LP, supporting clients in IP management and licensing. I have:

- designed and managed development, testing, and evaluation of devices including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant, parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs applications;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involving use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and Fast Fourier Transform (FFT) for High Aspect Ratio Inspection (HARI) applications; audio and video system design and installation;
- taught courses in solid state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other);
- provided nuclear radiation hardness testing services for military and space clients; and
- managed the design and installation of audio sound and video systems for private and commercial enterprises.

PROFESSIONAL SUMMARY

From 1986-1990, I was Executive Vice President of EPI Technologies, Inc., prior to joining the staff at Cochran Consulting, Inc. where I served as senior managing consultant from 1991-2002. From 1972 to 1986, I was employed by Texas Instruments Incorporated.

EXPERIENCE PROFILE

1988-present

McAlexander Sound, Inc. (McASI) - Richardson, TX
President

- o System, Product, and Process investigation, expert witness services for protection of intellectual property;
- o Patent portfolio development and valuation;
- o Product liability and insurance claim investigation, expert witness services for matters involving such claims;
- o Quality Systems consulting and engineering;
- o Radiation Hardness Testing Technical Representative;
- o Acoustic system design/installation
- o Technical Advisor in High Aspect Ratio and Surface Contour Measurement using Direct-to-Digital Holography.

2005-present

McAlexander Sound Pte Ltd - Singapore
Managing Director

- o System, Product, and Process investigation, expert witness services for protection of intellectual property;
- o Patent portfolio development and valuation;
- o Contract consultation;
- o Not assigned any patents and is not engaged in any IP related licensing or litigation activities.

2002-present

MDFHoldings, Inc. – Las Vegas, NV
CEO

- o IP holding and licensing company;
- o Assigned U.S. Patent Nos. 7,340,260 and 7,657,265 and EP 1 557 058 B1, each related to an object locating system;
- o Has not been and is not engaged in any IP related litigation or licensing activities.

2006-2020

QM Partners, L.P. – Texas
Manager

- o Management of development, licensing, prosecution and exploitation of assigned intellectual property;
- o Not assigned any patents and is not engaged in any IP related licensing or litigation activities.

EXPERIENCE PROFILE (continued)

2006-2020

Guardian Technologies, LLC – Texas
Manager

- o IP holding and licensing company;
- o Litigated U.S. Patent No. 5,657,076 related to security surveillance 2009-2011 (patent expired 2015);
- o Assigned U.S. Patent No. 8,334,775 related to RFID tracking (reassigned 2020 to personal);
- o Not engaged in any IP related licensing or litigation activities.

2006-2020

Appropriate Holdings, LLC – Delaware
Manager

- o IP holding company;
- o Not assigned any patents, has not been and is not engaged in any IP related licensing or litigation activities.

1996-2010

RMC Management, LLP - Plano, TX
Partner

- o Asset management.

1991-2002

Cochran Consulting, Inc. (CCI) - Richardson, TX
Managing Consultant

- o System, Product, and Process investigation, expert witness services for protection of intellectual property;
- o Design, process, and product reliability;
- o Defect and failure analysis.

1986-Nov'90

EPI Technologies, Inc. - Richardson, TX
Executive Vice President and Company Officer

- o Managed Advanced Technology Div., QA, and Engineering, including software program development;
- o Developed strategic, space/energy market growth plans;
- o Negotiated the acquisition of and managed a radiation company;
- o Designed and managed physical analysis, radiation effects, and environmental stress laboratories, including optical and e-beam measurement;
- o Achieved > 30% annual revenue growth and profitability for each laboratory the first 12 months;

EXPERIENCE PROFILE (continued)

- o Product and Process investigation services for protection of intellectual property.

1972 – 1986 **Texas Instruments, Inc.** - Dallas/Houston, TX; Singapore

'84 - '86 **Quality/Reliability Assurance Manager, TI Dallas** Advanced DRAM semiconductor wafer fabrication facility

- o Developed/implemented on-line, computerized SPC software tools for dimensioning analysis and control and pattern recognition;
- o Coordinated people development, design-of-experiments;
- o Managed chemical and physical analysis laboratories;
- o Implemented control systems to assure product, process, material, equipment, and facility compliance, including Cost of Quality analysis.

'82 - '84 **Quality/Reliability Assurance and Engineering Manager, TI Singapore** assembly/test facility

- o Developed, implemented, and operated an effective Quality/Reliability Assurance program for assembly processing including optical pattern recognition for equipment registration;
- o Supervised 225 people for 7 day/week operation, including QRA, Computer Systems software development, and Training;
- o Trained engineers in Solid State Physics, device fabrication, and statistical process control.

'81 - '82 **Engineering Operations Manager, TI Houston**

- o Managed DRAM memory product cost center;
- o Responsible for division test software generation, product assembly and test quality / yield, cost reduction and quality improvement;
- o Provided technical customer interface for marketing;
- o Coordinated TI Singapore engineering test/assembly.

'79 - '81 **Product Engineering Manager, TI Houston**

- o Responsible for yield improvement, technical customer interface, quality improvement, design evaluation, and device characterization for DRAM and CCD products;
- o Developed device specifications and test software.

EXPERIENCE PROFILE (continued)

'72 - '79

Design Section Manager / Engineer, TI Houston

- o Responsible for design and development, process compatibility, production introduction of Dynamic Ram products;
- o Activities included electrical and physical layout, SPICE model simulation, test program generation, and product implementation for MOS Dynamic Ram products.

1969 - 1972

U. S. Army - Coventry, Rhode Island; Seoul, Korea
Captain, Air Defense Artillery

- o Served one year as Communications Officer in Korea;
- o Served two years as Tactical Officer, New England Defense.

ORGANIZATIONS, PUBLICATIONS, EDUCATION**PROFESSIONAL ORGANIZATIONS AND AWARDS**

- 1 - Institute of Electrical and Electronics Engineers, Inc. (IEEE), Senior Member. Societies:
Computer, Electron Devices, Solid State Circuits
- 2 - Licensing Executives Society (LES)
- 3 - National Society of Professional Engineers
- 4 - Texas Board of Professional Engineers, Registered License #79454
- 5 - Society of Flight Test Engineers
- 6 - American Society of Civil Engineers
- 7- Architectural Engineering Institute
- 8 - 2000/2001 Nationwide Register's Who's Who in Executives and Businesses
- 9 - 1996/1997 Strathmore's Who's Who Registry of Business Leaders

PUBLICATIONS

- 1- NUS Proceedings of Engineering Convention '83, Aug '83, pgs. 139-142, The Memory Challenge.
- 2- Archives of Biochemistry and Biophysics, Dec'81, Vol. 212, No. 2, Equilibrium Constants under Physiological Conditions for the Reactions of D-3-Phosphoglycerate Dehydrogenase and L-Phosphoserine Aminotransferase.
- 3- International Electron Devices Meeting, Dec '79, pgs. 355-357, Sub 100ns 16K x 1 MOS Dynamic RAM Using a Grounded Substrate.

EDUCATION PROFILE

- | | |
|-------------|--|
| 1980 - 1985 | Taught Solid State Device Physics, Semiconductor Processing, Circuit Design Techniques, and Statistical Quality Control Methods

Effectiveness Training and Japanese Manufacturing Techniques, Participative Problem Solving courses |
| 1975 - 1976 | 1.5 years Graduate Study in Neural Science, the University of Texas Graduate School of Biomedical Science |
| 1965 - 1969 | BSEE, North Carolina State University |

PATENTS (US-31, Foreign-8)

4,239,993	(1980) High Performance Dynamic Sense Amplifier with Active Loads
4,280,070	(1981) Balanced Input Buffer Circuit for Semiconductor Memory
4,288,706	(1981) Noise Immunity in Input Buffer Circuit for Semiconductor Memory
4,370,575	(1983) High Performance Dynamic Sense Amplifier with Active Loads
4,418,293	(1983) High Performance Dynamic Sense Amplifier with Multiple Column Outputs
4,533,843	(1985) High Performance Dynamic Sense Amplifier with Voltage Boost for Row Address Lines
4,543,500	(1985) High Performance Dynamic Sense Amplifier Voltage Boost for Row Address Lines
4,543,501	(1985) High Performance Dynamic Sense Amplifier with Dual Channel Grounding Transistor
4,748,349	(1988) High Performance Dynamic Sense Amplifier with Voltage Boost for Row Address Lines
6,172,640 B1	(2001) Pet Locator
6,236,358 B1	(2001) Mobile Object Locator
6,421,001 B1	(2002) Object Locator
6,441,778 B1	(2002) Pet Locator
6,480,147 B2	(2002) Portable Position Determining Device
6,518,919 B1	(2003) Mobile Object Locator
6,771,213 B2	(2004) Object Locator
6,859,171 B2	(2005) Mobile Object Locator

PATENTS (continued)

7,113,126 B2	(2006) Portable Positioning Determining Device
7,179,674 B2	(2007) Bi-Directional Released-Beam Sensor
7,209,075 B2	(2007) Mobile Object Locator
7,324,044 B2	(2008) Object Locator
7,336,227 B2	(2008) Portable Position Determining Device
7,340,260 B2	(2008) System and Method for Tracking the Location of Multiple Mobile Radio Transceiver Units (assigned to MDFHoldings, Inc.)
7,353,706 B2	(2008) Weighted Released-Beam Sensor
7,397,097 B2	(2008) Integrated Released Beam Layer Structure Fabricated in Trenches and Manufacturing Method Thereof
7,564,405 B2	(2009) Object Locator
7,657,265 B2	(2010) System and Method for Tracking the Location of Multiple Mobile Radio Transceiver Units (assigned to MDFHoldings, Inc.)
7,760,137 B2	(2010) Portable Positioning Determining Device
7,764,228 B2	(2010) Portable Positioning Determining Device
7,989,906 B2	(2011) Bi-Directional released-Beam Sensor
8,334,775 B2	(2012) RFID-Based Asset Security and Tracking System, Apparatus and Method (assigned to personal)
JP 55-053640 B4	(1980) Defect Resistant Semiconductor Memory Cell
JP 59-044720 B4	(1984) Semiconductor High Speed Read/Write Memory Unit
DE2935121 C2	(1980) Clock Voltage Generator for Semiconductor Memory with Reduced Power Dissipation
DE3043651 A1	(1981) Clock Voltage Generator for Semiconductor Memory with Reduced Power Dissipation

PATENTS (continued)

GB2032211 B2	(1980) High Performance Dynamic MOS Read/Write Memory
EP 1 557 058 B1	(2011) System and method for tracking the location of multiple mobile radio transceiver units (assigned to MDFHoldings, Inc.) [States: AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR]
EP 1 676 809 B1	(2010) Weighted released-beam sensor [States: DE FR GB IT]
EP 1 676 810 B1	(2010) Bi-directional released-beam sensor [States: DE FR GB IT]

CASES

Cases over at least the past 7 years, either active or closed, in which I have signed a Protective Order, have testified as an expert either at a trial, hearing, or deposition, or have submitted statements / opinions by declaration, affidavit, or report, are:

CASE¹	CASE NUMBER	LOCATION	YEAR	TYPE²
Kangaroo Media* v. Immersion Entertainment (*firm: Kenyon & Kenyon)	2:12-cv-00382-JFC, 2:14-cv-01536-JFC	WD PA	2012 - 2016	P,t
(Audio/Video Entertainment System patent)				
Securus* v. Global (*firm: Gruber)	3:13-CV-03009-K	ND TX	2014 - 2017	P,t
(Patents related to telecom systems)				
Global v. Securus* (*firm: Gruber)	3:14-CV-0829-K, 3:13-CV-00713-JRS	ND TX / ED VA	2014 - 2017	P
(Patents related to telecom systems)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01155	USPTO PTAB	2014 - 2016	P,t
(Patent 7,289,393 related to music jukebox)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01156	USPTO PTAB	2014 - 2016	P,t
(Patent 7,817,502 related to a personal digital stereo player)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01157	USPTO PTAB	2014 - 2016	P,t
(Patent 7,933,171 related to a personal digital stereo player)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01158	USPTO PTAB	2014 - 2016	P,t
(Patent 8,400,888 related to a personal digital stereo player)				

¹ * = Client

² P=Patent, C=Contract, ©=Copyright, TS=Trade Secret, AT=Antitrust; CA=Class Action; t=testified, TH=Trial/Hearing

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
One-E-Way* v. Sony, Sennheiser, BlueAnt, Creative Tech, Beats, Jawbone, Jabra (*firm: Knobbe Marten, Olson & Bear)	337-TA-943	ITC (Pender)	2014 - 2018	P,t
(Patents related to bluetooth configured headphones)				
Omega* v. Calamp	6:13-cv-1950-Orl-31DAB	MD, FL	2015 - 2016	P,t,TH
(Patents related to vehicular control systems and tracking)				
AVM* v. Intel (*firm: Boies, Schiller & Flexner)	1:15-cv-00033-RGA	DE	2015 - 2016	P,t,TH
(Patent related to dynamic logic circuits)				
Allure Energy* v. Honeywell (*firm: McKool Smith)	1:15-cv-00079-RP	WDTX, Austin	2015 - 2017	P
(Smart Thermostat)				
IV* v. Toshiba (*firm: Desmarais)	13-cv-453-SLR-SRF	DE	2015 - 2017	P,t,TH
(NAND Flash)				
IMS v. Micron* (*Weil Gotchal/ Orrick)	1:14-cv-01480-RGA	DE	2015 - 2022	P,t
(Patents related to flash memory)				
Honeywell v. Allure* (*firm: Dickinson Wright)	IPR201501248, 01251,01253	USPTO PTAB	2015 - 2017	P
(Smart Thermostat)				
Blitzsafe* v Honda (*firm: Brown Rudnick)	2:15-cv-01274-JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v Hyundai (*firm: Brown Rudnick)	2:15-cv-01275-JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Blitzsafe* v Nissan (*firm: Brown Rudnick)	2:15-cv-01276- JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v Toyota (*firm: Brown Rudnick)	2:15-cv-01277- JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v VW (*firm: Brown Rudnick)	2:15-cv-01278- JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
3rd Eye Surveillance* v Stealth (*firm: Kennedy Law)	6:14-cv-00162 JDL	EDTX, Tyler	2015 - 2016	P
(Patents related to real-time image processing to response agency)				
3rd Eye Surveillance* v Vision Video (*firm: Kennedy Law)	6:14-cv-00161- JDL	EDTX, Tyler	2015 - 2016	P
(Patents related to real-time image processing to response agency)				
3rd Eye Surveillance* v Ft Worth / e-Watch (*firm: Kennedy Law)	6:14-cv-00725	EDTX, Tyler	2015 - 2017	P,t,TH
(Patents related to real-time image processing to response agency)				
3rd Eye Surveillance* v United States (*firm: Kennedy Law)	1:15-cv-00501- CFL	Court of Federal Claims, DC	2015 -	P,t,TH
(Patents related to real-time image processing to response agency)				
Hitachi v TPV* (*firm: O'Melveny & Myers)	2:14-cv-1121- JRG-RSP	EDTX, Marshall	2015 - 2016	P
(Patent related to LCD power and signal board arrangement)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Nidec Motor v Broad Ocean Motor* (*firm: Locke Lord)	2:15-cv-00443	EDTX, Marshall	2016	P
(Patent related to blower motor control for HVAC)				
TracBeam* v T-Mobile (*firm: Dovel & Luner)	6:14-cv-678-RWS	EDTX, Tyler	2016	P,t
(Patents related to geographic location estimates)				
SMS v Emerson* (*firm: Davidson Berquist)	2:15-cv-00032-RWS-RSP	EDTX, Marshall	2016	P
(Patent related to a method of monitoring a protected space)				
Prong v Sorias* (*firm: Gottlieb, Rackman & Reisman)	IPR2015-01317	USPTO PTAB	2016	P
(Patent related to attachable mobile charger)				
Skyline Software Systems v Duane Morris* (*firm: Venable)	2015-08868	Circuit Court Fairfax County	2016	P
(3D mapping technology)				
SignalQuest v Oncque* (*firm: Duane Morris)	11-cv-00392-JL	NH	2016	P
(Patents related to vibration switches)				
TiVo v Samsung* (*firm: Fish & Richardson)	2:15-CV-1503	EDTX, Marshall	2016	P
(Patent related to multimedia signal processing)				
Richtek v uPi* (*firm: Hogan Lovells)	C 09-05659 WHA LB	NDCA, SF	2016	P
(Patents related to converter channel current balance and PWM circuit)				
Paice* v VW, Porsche, Audi (*firm: Fish & Richardson)	337-TA-998	ITC	2016 – 2017	P
(Patents related to hybrid vehicle technology)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Biosonix v Hydrowave* (*firm: Bradley)	4:16-cv-00139-RC	EDTX, Sherman	2016 - 2017	P
(Patent related to underwater sound listening and generation)				
Univ of S FL* v Fujifilm (*firm: Dickinson Wright)	8:16-cv-01194-MSS-TGW	MDFL, Tampa	2017	P
(Patent related to Workstation Interface – Digital Mammography)				
Univ of S FL * v BRIT (*firm: Dickinson Wright)	8:16-cv-03109-MSS-TGW	MDFL, Tampa	2017	P,t
(Patent related to Workstation Interface – Digital Mammography)				
Nokia v Apple	337-TA-1038	ITC	2017	P
(Patent related to controllable bias mode oscillator)				
Univ of IL v Micron* (*firm: Fish & Richardson)	2:11-cv-02288-SLD-JAG	CDIL, Rock Falls	2017	P, C
(Patents and contract related to use of deuterium in semiconductor processing)				
ZiiLabs v AMD* (*firm: O'Melveny & Myers)	337-TA-1037	ITC-Shaw	2017	P
(Patents related to graphics processors)				
MTL* v Sandisk (*firm: Tensegrity)	337-TA-1034	ITC-Lord	2017	P,t
(Patents related to flash memory)				
Razberi v Dynacolor* (*firm: McDole Williams)	01-16-0003-3734	AAA	2017 - 2018	C,TS,t, TH
(Arbitration related to contractual obligations)				
Seed Spring* v Microsoft (*firm: Dovel)	6:17-cv-427-RWS	EDTX, Tyler	2017	P
(Patents related to Wirelss Location)				
TracBeam* v Microsoft (*firm: Dovel)	6:17-cv-426-RWS	EDTX, Tyler	2017	P
(Patents related to Wirelss Location)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
TracBeam* v Cisco (*firm: Dovel)	6:17-cv-525-RWS	EDTX, Tyler	2017 - 2018	P
(Patents related to Wirelss Location)				
Arris* v Sony (*firm: Fish & Richardson)	337-TA-1060	ITC-Lord	2017	P,t
(Patent related to Broadcast Signals)				
Vivint* v Alarm.com (*firm: Weil)	2:15-cv-00392- CW-BCW	UT	2017 - 2023	P,t
(Patents related to Electronic Message Delivery)				
Blitzsafe* v Bosch (*firm: Brown Rudnick)	2:17-cv-00105- JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v Daimler & Mercedes (*firm: Brown Rudnick)	2:17-cv-00422- JRG	EDTX, Marshall	2017 – 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v BMW (*firm: Brown Rudnick)	2:17-cv-00418- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Mazda (*firm: Brown Rudnick)	2:17-cv-00423- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Mitsubishi (*firm: Brown Rudnick)	2:17-cv-00430- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Subaru (*firm: Brown Rudnick)	2:17-cv-00421- JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to audio device integration systems)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Blitzsafe* v Tata & Jaguar (*firm: Brown Rudnick)	2:17-cv-00424-JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Volvo (*firm: Brown Rudnick)	2:17-cv-00420-JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
AGIS* v Huawei (*firm: Brown Rudnick)	2:17-00513-JRG	EDTX, Marshall	2017 - 2018	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v HTC (*firm: Brown Rudnick)	2:17-00514-JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v LG (*firm: Brown Rudnick)	2:17-00515-JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v Apple (*firm: Brown Rudnick)	2:17-00516-JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v ZTE (*firm: Brown Rudnick)	2:17-00517-JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to Patents related to interactive remote communications)				
Arya v Dufossat* (*firm: Robert Sueiro)	4:16-cv-03595	SDYX, Houston	2017 -	TS,C,t
(Dispute related to Trade Secrets)				
Seven Networks v Samsung* (*firm: Fish & Richardson)	2:17-cv-00441-JRG	EDTX, Marshall	2017 - 2018	P,t
(Patents related to Power Management of Mobile Networks)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
ZF Micro Solutions* v. Tat Investment (*firm: Berger)	1-09-CV-134970	Santa Clara County	2018	C,t,TH
(Business tort, unfair practice)				
Univ of S FL* v Fujifilm (*firm: Dickinson Wright)	3:18-cv-00215-AVC	Connecticut	2018	P,t
(Patent related to Workstation Interface – Digital Mammography)				
Univ of S FL* v BRIT (*firm: Dickinson Wright)	3:18-CV-0250-K	NDTX, Dallas	2018 - 2019	P,t
(Patent related to Workstation Interface – Digital Mammography)				
Cypress Insurance v Hynix* (*firm: Bird Marella)	C17-467 RAJ	WDWA, Seattle	2018 - 2019	C,t,TH
(Contract dispute related to product delivery)				
Belliveau* v BARCO (*firm: McKool)	1:17-CV-00379-SS	WDTX, Austin	2018	C,t
(Patent portfolio licensing dispute)				
MPS* v Intersil (*firm: Perkins)	16-1125-LPS	DE	2018 - 2021	TS,t
(Trade Secret dispute)				
GoGo v Squire Patton Boggs* (*firm: Cozen O'Connor)	2016-L-007789	Cook County, IL	2018 - 2019	P
(Patent Malpractice claim)				
X2Y* v Intel (*firm: Dovel)	3:18-cv-1394-HZ	DOR, Portland	2018 - 2020	P
(Patents related to package layer metalization)				
Power Integration* v ON Semi (*firm: Fish & Richardson)	5:16-cv-06371-BLF	NDCA, San Jose	2019	P,t
(Patents related to power converter regulation)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
ON Semi v Power Integration* (*firm: Fish & Richardson)	1:17-cv-00247-LPS-CJB	DE	2019	P,t
(Patents related to power converter regulation)				
Semcon* v Amazon (*firm: Brown Rudnick)	2:18-CV-00192-JRG	EDTX, Marshall	2019	P
(Patent related to Adaptive Power Control)				
Semcon* v Asustek (*firm: Brown Rudnick)	2:18-CV-00193-JRG	EDTX, Marshall	2019	P
(Patent related to adaptive power control)				
Semcon* v Kyocera (*firm: Brown Rudnick)	2:18-CV-00197-JRG	EDTX, Marshall	2019	P
(Patent related to adaptive power control)				
Innovation Sciences* v Amazon (*firm: Davidson Berquist)	4:18-cv-00474-ALM	EDTX, Sherman	2019 - 2020	P,t,TH
(Patent related to Internet communication)				
Innovation Sciences* v HTC (*firm: Davidson Berquist)	4:18-cv-00476-ALM	EDTX, Sherman	2019 - 2020	P,t
(Patent related to Internet communication)				
Innovation Sciences* v Resideo (*firm: Davidson Berquist)	4:18-cv-00475-ALM	EDTX, Sherman	2019 - 2020	P,t
(Patent related to Internet communication)				
Innovation Sciences* v Vector (*firm: Davidson Berquist)	4:18-cv-00477-ALM	EDTX, Sherman	2019	P
(Patent related to Internet communication)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
CXT* v JC Penny (*firm: Brown Rudnick)	2:18-cv-00171-RWS-RSP (lead) 2:18-CV-233-RWS-RSP	EDTX, Marshall	2019 - 2020	P,t
(Patents related to storage management and information distribution)				
Photonics* v Lenovo (*firm: Brown Rudnick)	1:18-cv-00489-MN	DE	2019	P
(Patents related to GDS-II Layout)				
Quest NetTech Corp* v Apple (*firm: Brown Rudnick)	2:19-CV-00118-JRG	EDTX, Marshall	2019 - 2020	P
(Patent related to programmable credit card system)				
Pilot, Inc.* v Schumacher (*firm: Bradford)	1:19-cv-05982-EEC	NDIL, Eastern Div	2019 - 2921	P
(Patents related to battery chargers)				
Vocalife* v Amazon (*firm: Brown Rudnick)	2:19-cv-00123-JRG	EDTX, Marshall	2019 - 2020	P,t,TH
(Patent related to microphone array)				
Semcon* v Vuitton (*firm: Brown Rudnick)	2:19-CV-00122-JRG	EDTX, Marshall	2019	P,t
(Patent related to adaptive power control)				
Semcon* v Shenzhen (*firm: Brown Rudnick)	2:18-CV-00196-JRG	EDTX, Marshall	2019	P,t
(Patent related to adaptive power control)				
Ultravision* v GoVision (*firm: Brown Rudnick)	2:18-cv-00100-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Shenzhen (*firm: Brown Rudnick)	2:18-cv-00103-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Ultravision* v Aoto (*firm: Brown Rudnick)	2:18-cv-00113-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Leyard (*firm: Brown Rudnick)	2:18-cv-00102-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v NEC (*firm: Brown Rudnick)	2:18-cv-00150-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to Modular Display Panels and LED lighting)				
Ultravision* v Prismaflex (*firm: Brown Rudnick)	2:18-cv-00108-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Unilumin (*firm: Brown Rudnick)	2:18-cv-00116-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Yaham (*firm: Brown Rudnick)	2:18-cv-00118-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Absen (*firm: Brown Rudnick)	2:18-cv-00112-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Birchett* v City of Fort Worth (*firm: Kennedy Law)	DC-19-06941	Dallas County	2019	C,t
(Whistleblower)				
Innovation Sciences* v HTC (*firm: Davidson Berquist)	337-TA-1180	ITC	2020 - 2021	P,t
(Patent related to wireless communication)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Innovation Sciences* v Resideo (*firm: Davidson Berquist)	337-TA-1180	ITC	2020	P,t
(Patent related to Internet communication)				
CXT* v Neiman Marcus (*firm: Brown Rudnick)	2:19-cv-00270-RWS-RSP	EDTX, Marshall	2020	P
(Patents related to storage management and information distribution)				
CXT* v General Nutrition (*firm: Brown Rudnick)	2:19-cv-00271-RWS-RSP	EDTX, Marshall	2020	P
(Patents related to storage management and information distribution)				
CXT* v Steven Madden (*firm: Brown Rudnick)	2:19-cv-00272-RWS-RSP	EDTX, Marshall	2020	P
(Patents related to storage management and information distribution)				
Consolidated* v Amazon (*firm: Devlin Law)	1:19-cv-01715-RGA	DE	2020 – 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v Ford (*firm: Devlin Law)	1:19-cv-01916-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v JC Penney (*firm: Devlin Law)	1:19-cv-01918-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v Ebay (*firm: Devlin Law)	1:19-cv-01580-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v Walmart (*firm: Devlin Law)	1:19-cv-01581-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Semcon* v TCT Mobile (*firm: Brown Rudnick)	2:18-CV-00194-JRG	EDTX, Marshall	2020	P
(Patent related to adaptive power control)				
BNR v Samsung* (*firm: Fish & Richardson)	2:19-cv-00286-JRG	EDTX, Marshall	2020	P
(Patents related to portable communication devices)				
AGIS* v Google (*firm: BRudnick, Fabricant)	2:19-cv-00361-JRG	EDTX, Marshall	2020 - 2022	P,t
(Patents related to interactive remote communications)				
AGIS* v Waze (*firm: BRudnick, Fabricant)	2:19-cv-00359-JRG	EDTX, Marshall	2020 - 2022	P,t
(Patents related to interactive remote communications)				
Burke* v City of Fort Worth (*firm: Kennedy Law)	DC-19-07239	Dallas County	2020 -	C,t
(Whistleblower)				
Infinera v Oyster Optics* (*firm: Davidson Berquist)	IPR2020-00325	PTAB	2020	P,t
(Patent related to fiber optic telecommunications)				
Blitzsafe* v GM (*firm: Fabricant)	2:19-cv-00377-JRG	EDTX, Marshall	2020	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v FCA (*firm: Fabricant)	2:19-cv-00378-JRG	EDTX, Marshall	2020	P,t
(Patents related to audio device integration systems)				
Kuster v Western Digital* (*firm: Shearman & Sterling)	6:20-cv-00563	WDTX, Waco	2020 -	P,t
(Patent related to memory stack storage)				
TruSun* v Eaton (*firm: Duane Morris)	6:19-cv-00656-ADA	WDTX, Waco	2020 - 2022	P,t
(Patent related to a light-generating system)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
RJR v PMI* (*firm: Latham Watkins)	1:20-cv-00393- LO-TCB	EDVA, Alexandria	2020 - 2022	P,t,TH
(Patents related to e-cigarette controls)				
Koss* v Apple et al (*firm: K L Gates)	6:20-cv-00665	WDTX, Waco	2020 - 2022	P,t
(Patents related to Wireless Headphones)				
Koss* v Bose (*firm: K L Gates)	6:20-cv-00661	WDTX, Waco	2020 -	P
(Patents related to Wireless Headphones)				
Ipcom v Sprint et al (Nokia*) (*Alston Bird)	2:20-cv-321	EDTX, Marshall	2020 - 2022	P
(Patents related to CDMA communication)				
Ipcom v Verizon et al (Nokia*) (*Alston Bird)	2:20-cv-323	EDTX, Marshall	2020 - 2022	P
(Patents related to CDMA communication)				
Pilot* v CarKu (*firm: Bradford / Sheridan)	7131799991	Amazon Arbitration	2020	P,t
(Patent related to jump starters)				
MPS* v Meraki (*firm: Perkins Coie)	6:2020cv00876- ADA	WDTX, Waco	2020 - 2022	P,TS,C
(Patents related to synchronous rectifier control)				
AGIS* v Uber (*firm: Fabricant)	2:21-cv-00026- JRG-RSP)	EDTX, Marshall	2021	P
(Patents related to interactive remote communications)				
AGIS* v WhatsApp (*firm: Fabricant)	2:21-cv-00029- JRG-RSP)	EDTX, Marshall	2021	P
(Patents related to interactive remote communications)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
One E-Way* v Apple (*firm: Knobbe Martin)	2:20-cv-06339- JSK-PD	CDCA	2021 - 2023	P,t
(Patent related to Bluetooth Headphones)				
BMW v Omega Patents* (*firm: Allen Dyer)	IPR2021-00181	PTAB	2021 -	P,t
(Patent related to remote start)				
Pilot* v The NOCO Co (*firm: Bradford / Sheridan)	2:20-cv-01452- SRB	AZ	2021 -	P,t
(Patents related to auto chargers)				
Express Mobile* v Atlassian (*firm: Mololamken)	6:20-cv-00805- ADA	WDTX, Austin	2021 -	P
(Patents related to browser-based web site generation)				
AGIS* v Lyft (*firm: Fabricant)	2:21-cv-00024- JRG-RSP	EDTX, Marshall NDCA	2021 - 2022	P
(Patents related to interactive remote communications)				
AGIS* v T-Mobile (*firm: Fabricant)	2:21-cv-00072- JRG-RSP	EDTX, Marshall	2021	P
(Patents related to interactive remote communications)				
Altria* v RJR (*firm: Weil Gotshal)	1:20-cv-00472	MDNC	2021 - 2022	P,t,TH
(Patents related to e-cig)				
Altria* v RJR (*firm: Weil Gotshal)	IPR2021-00650 IPR2021-00652 IPR2021-00725 IPR2021-00744 IPR2021-00745 IPR2021-00746 IPR2021-00747 IPR2021-00793	PTAB	2021 - 2022	P,t,TH
(Patents related to e-cig control)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
One E-Way* v Apple (*firm: Knobbe Martin)	IPR2021-00283 IPR2021-00286	PTAB	2021 - 2022	P,t
(Patent related to Bluetooth Headphones)				
Kiwi Connection* v Anker (*firm: Bradford)	8519300821	Amazon Arbitration	2021	P,t
(Patent related to bidirectional connector)				
Kiwi Connection* v JBL (*firm: Bradford)	8674855301	Amazon Arbitration	2021	P,t
(Patent related to bidirectional connector)				
Platform Science v Omnitracs* (*firm: Kirkland & Ellis)	IPR2020-0187 IPR2020-1517 IPR2020-1518	PTAB	2021 – 2022	P,t
(Patent related to critical event reporting)				
Netlist v Samsung* (*firm: Bird Marella)	8:20-cv-993-MCS	CDCA, Southern	2021	C,t
(Contract dispute)				
Monterey Research* v (*firm: Desmarais)	IPR 2021-00119 IPR 2021-00120 IPR 2021-00172	PTAB	2021 - 2022	P,t
(Patents related to semiconductor processing)				
Apple / Bose v Koss* (*firm: K L Gates)	IPR2021-00255 IPR2021-00297 IPR2021-00305 IPR2021-00381 IPR2021-00592	PTAB	2021 - 2022	P,t
(Patents related to Wireless Headphones)				
Vocalife* v Amazon2 (*firm: Fabricant)	2 :20-cv-00401- JRG-RSP	EDTX, Marshall	2021 - 2023	P,t
(Patent related to microphone array)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Vocalife* v Google (*firm: Fabricant)	2 :21-cv-00124-JRG-RSP	EDTX, Marshall	2021 - 2023	P,t
(Patent related to microphone array)				
Luxshare* v Amphenol (*firm: K L Gates)	IPR2022-00132	PTAB	2021 - 2022	P,t
(Patent related to high performance connector)				
Vervain v Micron* (*firm: Orrick)	6:20-cv-487-ADA	WDTX, Waco	2021 - 2023	P,t
(Patents related to MLC & SLC endurance)				
Express Mobile* v Dropbox (*firm: Mololamken)	3:21-cv-01145	NDCA	2021 -	P
(Patents related to browser-based web site generation)				
Lexmark v Universal Imaging* (*firm: Allen Dyer)	8:18-cv-1047-T-17AEP	MDFL, Tampa	2021 - 2023	P
(Patents related to printer cartridge authentication)				
Pilot* v The NOCO Co (*firm: Bradford / Sheridan)	IPR2021-00777 IPR2021-01232 IPR2023-00167 IPR2023-00810	PTAB	2021 -	P,t
(Patents related to auto chargers)				
Delta T* v MacroAir (*firm: Latham/VedderPrice)	5:20-cv-00728-GW-GJS	CDCA, LA	2022 - 2023	P
(Patents related to fan sensors and control)				
MPS* v Dong & Sheng (*firm: Perkins Coie)	4 :20-cv-6752-JSW	NCCA, Oakland	2022 - 2023	P, TS
(Patents related to synchronous rectifier control)				
Vocalife* v Sonos (*firm: Fabricant)	2 :21-cv-00129-JRG	EDTX, Marshall	2022	P,t
(Patent related to microphone array)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Vocalife* v Bose (*firm: Fabricant)	2 :21-cv-00128-JRG	EDTX, Marshall	2022	P,t
(Patent related to microphone array)				
Enovsys* v T-Mobile (*firm: Eichmann)	2:21-cv-00368-JRG	EDTX, Marshall	2022	P,t
(Patents related to precise location determination and secure disclosure)				
Enovsys* v Verizon (*firm: Eichmann)	2:21-cv-00315-JRG-RSP	EDTX, Marshall	2022	P,t
(Patents related to precise location determination and secure disclosure)				
Lyft v AGIS* (*firm: Fabricant)	5 :21-cv-04653-BLF	NDCA, San Jose	2022 - 2023	P
(Patents related to interactive remote communications)				
Vocalife* v Amazon (*firm: Fabricant)	IPR2021-01331	PTAB	2022	P,t
(Patent related to microphone array)				
MPS* v Meraki (*firm: Perkins Coie)	4:22-cv-01986 JSW	NDCA, Oakland	2022 - 2023	P,TS,C
(Patents related to synchronous rectifier control)				
Signode v Polychem* (*firm: Latham)	1 :22-cv-00519-UNA	DE	2022 -	P
(Patents related to a strapping apparatus)				
Pilot* v Hulkman (*firm: BRADFORD)	10427111251	Amazon Arbitration	2022	P,t
(Patent related to jump starters)				
Netlist v Samsung* (*firm: Fish & Richardson)	2:21-cv-463	EDTX, Marshall	2022 -	P
(Patents related to DIMM DDR3 signal timing, power management, and rank multiplication)				
Orange* v Autel (*firm: Sughrue Mion)	2 :21-cv-240	EDTX, Marshall	2022 - 2023	P
(Patent related to Tire Pressure Monitoring Systems)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Bell Power v MPS* (*firm: Perkins Coie)	6 :21-cv-00655- ADA	WDTX, Waco	2022 -	P
(Patents related to power converter/regulator control)				
VPR v Jupiter* (*firm: Noroozi PC)	2:20-CV-02185- DJH	AZ	2023 -	P
(Patent related to electronic vape device with air flow sensor)				
Multimodal* v Guangdong (*firm: Fabricant)	2:21-cv-00436- JRG-RSP	EDTX, Marshall	2023 -	P
(Patents related to communication over a network, call completion)				
Multimodal v ZTE (*firm: Fabricant)	2:21-cv-00437- JRG-RSP	EDTX, Marshall	2023 -	P
(Patents related to communication over a network, call completion)				
Entropic* v Charter Communications et al. (*firm: K L Gates)	2 :22-cv-00125- JRG	EDTX, Marshall	2022 -	P
(Patents related to modems and broadband content distribution)				
Oasis Tooling* v Global Foundries U.S. (*firm: Kramer Levin)	22-00312-CJB	DE	2022 -	P
(Patents related to chip design process workflow)				
Oasis Tooling* v Siemens Industry Software (*firm: Kramer Levin)	22-00151-CJB	DE	2022 -	P
(Patents related to chip design process workflow)				
AGIS* ITC (*firm: Fabricant)	337-TA-1347	ITC	2023	P
(Patents related to Location-Sharing Systems)				
Monterey* v Nanya (*firm: Desmarais)	19-2090-NIQA- LAS	DE	2023 – 2024M	P
(Patents directed to semiconductor technology)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Geotab v Omega* (*firm: Allen Dyer)	IPR2023-00504	PTAB	2023	P
(Patent related to vehicle tracking)				
Adv Lighting Concepts* v mate (*firm: Munsch)	IPR2023-01264	PTAB	2023 -	P
(Patent related to LED drivers)				
SitePro* v Waterbridge (*firm: Perkins Coie)	6:23-cv-00115- ADA-DTG	WDTX, Waco	2023 -	P,TS,C
(Patents and Trade Secrets related to remote delivery control)				
Nanya v Monterey* (*firm: Botos Churchill)	EPR 6,825,526C1 EPR 6,680,516	USPTO	2023 -	P
(Patents directed to semiconductor technology)				
ICPillar* v ARM (*firm: Eichmann)	6_23-cv-00115- ADA-DTG	WDTX, Austin	2023 -	P
(Patents related to computer method for IC design)				
GoTV Streaming v Netflix* (*firm: Wilkie Farr)	EPR 8478245 EPR 8989715	USPTO	2023 -	P
(Patent related to rendering content on a wireless device)				
Greenthread v MPS* (*firm: Perkins Coie)	23-579-RGA	DE	2024 -	P
(Patents related to semiconductor structure with graded doping)				

Cases (continued)

I have worked with other clients in various areas of my expertise, including “system, product, and process investigation,” “patent valuation,” “product liability and insurance claim investigation,” “quality systems consulting and engineering,” and “IP licensing.” This work generally relates to patents and may involve analysis of products either defensively or offensively. In no case does any of the work involve design of circuits, processes, packaging, software, or systems.

Non-confidentially, I have represented a radiation effects testing company, ICS Radiation Technology. Further, I have worked with investment companies, such as Hatcreek Partners, reviewing potential investment opportunities, and have participated as a technical advisor to nLine Corporation, a company that developed a product for semiconductor wafer inspection using holographic High Aspect Ratio Inspection (HARI) technology. Work associated with each of these matters occurred more than 10 years ago.

These and other non-confidentially related companies are:

The Aspire International Foundation (2019-present)

- Partner;
- Rediscovering and redefining identity and purpose through experiential equine learning programs;
- Not assigned any patents and not engaged in any IP related activities.

Casualty Consulting Group of America (2013-present)

- Partner;
- Assessment of structural damage caused by extreme weather events;
- Not assigned any patents and not engaged in any IP related activities.

VCSY (2013-2020)

- Advisory board Member;
- Technology related to encrypted communication.

Bethel Cannon Group / Bethel Cannon Holdings (2011-present)

- Partner;
- Counseling / Event / Retreat Center / Hunting Lodge;
- Not assigned any patents and not engaged in any IP related activities.

Spirit Song Youth Equestrian Academy / Spirit Song Holdings (2011-present)

- CEO;
- Equine Assisted Learning Program for abused / traumatized youth, families, corporations, and churches;
- Not assigned any patents and not engaged in any IP related activities.

Cases (continued)E³A (2016-present)

- President;
- Certification training of Equine Practitioners;
- Not assigned any patents and not engaged in any IP related activities.

Novo Tellus Capital Partners (2016-2017)

- Novo Tellus is an investment firm. I served as a technical advisor in reviewing the technology and contracts of investment opportunities.

UTAC (2008-2016)

- Technical consultant in matters related to packaging test and assembly, patents, and contracts.

ICS Radiation Technology (1988-2009)

- Consulting work related to nuclear radiation effects testing.

Creative Management Consultants (CMC) (2003-2004)

- Consulting work related to Internet services, such as access service to clients and web site hosting services; providing business co-op services and internet product purchasing sites.

Hatcreek Partners (1999-2003)

- Hatcreek Partners is an investment firm. I served as a technical advisor in reviewing the technology of investment opportunities.

nLine Corporation (1999-2003)

- Member of Technical Advisory Board;
- nLine Corp.'s business related to semiconductor holographic High Aspect Ratio Inspection (HARI) technology.

Texas Instruments (pre 2002)

- Patent evaluation and application consulting.

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