UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ARM LIMITED,
Petitioner,

v.

ICPILLAR LLC,
Patent Owner.

Case IPR2024-00476
Patent 8,924,899

PATENT OWNER'S AUTHORIZED PRELIMINARY SUR-REPLY

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I. Petitioner's New Unpatentability Arguments Should Be Rejected.

Petitioner Arm Ltd. misuses its brief to add untimely arguments "missing from the petition" and "go[ing] beyond what Petitioner argued" there. Ex. 2020, 9:16, 31:3-4; *see id.*, 17:5-8, 27:8-12. The Board authorized merits briefing only on "the proper claim construction of" "outputting" limitation (1[d]) and its "impact" "on understanding the asserted…references." *Id.*, 22:15-23:2, 24:5-13; Paper 7, 3-4. Yet after devoting just 2 pages to a strained new claim construction, ignoring the claim language, Arm proceeds to spend most of the brief rehashing arguments and evidence irrelevant to that construction. The Petition cannot overcome the simple fact that Banjeree and Rompaey do not output software programming commands to be executed on a hardware IC. The Reply's belated arguments do no better.

A. *Petitioner's New Claim Construction Position Is Wrong.*

Responding to the POPR showing that Banerjee and Rompaey do not output software programming commands executable on a hardware IC for controlling a device, Arm presents a broad new 1[d] interpretation that sweeps in "(1) internal outputs from 'compilers' that are then used by other portions of the design" tool and (2) "software…within the 'layout sent out to a manufacturer for fabrication.'" PReply, 2. The Petition never raised this construction—nor argued that so-called "internal outputs" or "software within the layout" met 1[d]. It argued that Banerjee and Rompaey "output" software as they "output" hardware designs: externally, not

internally or within the hardware design. POPR, 14-15 & 19-20 (Banerjee), 33-43 (Rompaey). This was unfounded, as is the belated proposed construction.

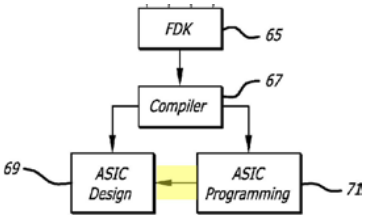
None of the claim language supports Arm's new construction. "*[O]utputting … software programming commands to be executed by the hardware integrated circuit for controlling the electronic device*" does not suggest "internal" software for use by the design tool, nor that the second recited "output[]" could be part of the first. *See, e.g., Becton, Dickinson & Co. v. Tyco Healthcare Group, LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) ("Where a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention."). Arm focuses on generic "software" shorn of context, PReply, *e.g.*, 2-3 (arguing that '899 "defines software broadly"). Arm's citation is misplaced: this is from a description of an exemplary computer system, not of the invention's outputs. The Patent explains that the "exemplary computer system" of Fig. 11 includes processor 501 for "executing instructions, such as those making up software," then lists "software" instruction types such generic computers might execute. Ex. 1001, 16:47-17:10. This describes software types an exemplary computer could execute. It is not, as Arm asserts, a definition of the "software programming commands" recited in 1[d]. *See* Ex. 1002, 48-49.

Nor does the '899 specification support the proposed construction. The '899 patent describes tools and methods for, *e.g.*, "providing an IC design based on the

selection of input and output characteristics of the device; and providing software for controlling the device through an IC based on the IC design." Ex. 1001, 4:66-5:2; *see id.*, Abstract; *see also id.*, 1:66-2:3 (noting that prior art ASIC design tools failed to "develop software" for the ASICs and devices they controlled). As usual, Arm truncates and snips essential and qualifying text from around its preferred isolated word, "software." *E.g.*, PReply, 1 (quoting '899 specification at 5:1-4 as "providing software," omitting "for controlling the device through the IC based on the IC design"), *id.* (similarly truncating '899 disclosure at 5:27, 5:52, 13:21).

As Arm does not dispute, the '899 written description does not describe internal outputted software to use for optimization. Nor does it describe "software stored in 'layouts,'" as Arm alleges (PReply, 2)—oddly, because there is no such thing. Arm seems to misapprehend that a "layout," as the term is used in the patent (and Banerjee and Rompaey) is merely a ***description of physical hardware for fabrication***. Ex. 2001 [McAlexander-Decl.] ¶¶32, 76, 90. It is impossible for "software programming commands" to be "stored in 'layouts.'"" Layouts may describe physical memory. But software cannot be stored in such a description, any more than shipped goods can be stored in a photograph of a shipping container.

Unable to find support in the '899's written description, Arm points to a sliver of alleged support in the drawings, but cannot substantiate its convoluted



theory. Arm asserts that a lone arrow in FIG. 4 must be seen "as an input into the layout" because the arrow points from the "ASIC Programming" box to the "ASIC Design" box. PReply, 1-2 (Arm's emphases). Even if Arm had substantiated its allegation that this is the sole embodiment with output as claimed, which it has not, it's unclear how the arrow could suggest that Programming 71 must be an "internal output" for internal use, when Design 69 and Programming 71 are both shown as outputs, not inputs, of the compiler. The arrow is more reasonably interpreted to refer to the express disclosure, which the Reply ignores, that "ASIC programming 71" is ***"associated" with "ASIC design 69."*** Or that box 71 can "be programmed and/or stored in a fabricated ASIC" based on design 69, once it is "sent out to a manufacturer for fabrication" and "fabricated." Ex. 1001, 9:47-51, 9:59-64.

Arm falsely suggests that Mr. McAlexander agrees with its view of FIG. 4's arrow. PReply 1-2. But McAlexander does not even mention the arrow: he simply notes that FIG. 4 shows programming 71 as an output of the tool, as accompanying written description at 9:59-61 indicates. Ex. 2001, ¶¶26-28. That programming 71 is expressly described as being programmed and stored "in a ***fabricated*** ASIC" is more than sufficient to dispel any notion that this arrow ***must*** be " an input into the layout"—which, as seen above, can't "store" or "be[] programmed" with software.

B. *Petitioner Improperly And Belatedly Refashions Its Prior Arguments.*

The Board found no cause for further merits briefing, except "limited to: (1)

the proper claim construction of the term 'outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device,'" and "(2) the impact that the asserted claim construction has on understanding the asserted prior art references," Paper 7, 3-4; Ex. 2020, 21:10-13 ("we agree with Patent Owner that on…the substantive issues, that Petitioner hasn't really shown good cause to file a reply"). Yet Arm devotes most of the Reply to attempting to augment its substantive briefing on 1[d] in ways not addressing the impact of its asserted construction. Indeed, the Reply arguments that 1[d] is met are over twice as long as the Petition arguments that 1[d] is met.

For example, after briefly addressing the impact of its proposed construction to sweep "internal outputs" into 1[d], PReply, 3-4, Arm pivots to attempting to rehabilitate the Petition's arguments that Banerjee outputs "software" "to be executed on the hardware (SoC)" that Banerjee supposedly "create[s]." PReply, 3; *compare id. with* Pet. 78-80 (arguing that Banerjee "outputs," among other things, "the operating system" and "application software"). As the POPR explained (at 15-24), "[t]he only output described in Banerjee is a hardware description file" and "descriptions of the use of application software and operating system in Banerjee may address the attributes and requirements of executing such software on the resulting IC, but they do not describe any software output by Banerjee that is 'executed on the hardware integrated circuit for controlling the electronic device.'"

In response, the Reply doubles down on the Petition's arguments (at 79) that Banerjee teaches software "'compiled' and '<u>instantiated in the device</u>'" it designs. PReply, 3-4 (Arm's emphasis). Most of these redoubled arguments—which remain based on cropped language or outright misapprehensions of Banerjee and continue to misread Banerjee's "instantiat[ion]" as referring to physical hardware instead of characterizations of how Banerjee performs optimization, *but see* POPR, 11, 23—are not impacted by Arm's new proposal to construe 1[d] to sweep in "internal outputs" and "software stored in 'layouts.'" Arm also says its view of Banerjee is required by Banerjee's "configur[ation] [of] software to efficiently use available hardware resources," "match[ing]" of "compiled features of the operating system," "'optimiz[ing]'" of "software such as the OS and device drivers," and "purpose," because "discard[ing]" any "tailored and specialized software" would supposedly "render[] Barnerjee's entire hardware/software optimization a nullity." PReply, 4-5. These arguments are meritless—among other things, Banerjee ***does*** use what it teaches to accomplish its purpose, of ***optimizing hardware designs***. POPR, 9-12. But these arguments weren't in the Petition, so can't be rebutted by evidence here.

Similarly, the Reply (at 7-9) revisits and expands the Petition's arguments that Rompaey meets 1[d], including those based on Rompaey's alleged output of "machine code" and "software drivers." PReply, 7-9. Arm makes new arguments that Rompaey's "essential" steps, "matching" software drivers to hardware, and

co-design "for efficiency" show that 1[d] is met. And it now argues that Rompaey "output[s]" "simulation," a "'database,'" and even a "software model." *Id.*, 8-10. These arguments are not shown to be impacted by the proposed construction, and ICPillar is barred from rebutting them with evidence here. Arm's untimely and unsubstantiated arguments should be disregarded under both §314(a) and *Fintiv*.

C. *Under The New Claim Construction, Neither Banerjee Nor Rompaey Outputs Software Programming Commands As 1[d] Claims.*

Arm argues Banerjee's disclosure of "compil[ing]" and "instantiat[ing]" an "operating system" is "virtually identical" to supposed disclosure of "output[ting]" '899's "ASIC Programming 71" "by a 'compiler'" as an "input into ASIC Design 69." PReply, 3. This argument is based on a misinterpretation of the arrow between box 69 and "associated" box 71 of '899 FIG. 2, and is wrong. Section I.A, *supra*.

As for Rompaey, Arm primarily focuses on Rompaey's "'output preferably compris[ing] *** machine code,'" PReply, 1, 7; Ex. 1004, 11:12-20). As usual, Arm is cropping what the actual text says. As the POPR notes, Rompaey's figures show outputting "hardware description language" from the model. POPR, 27-28, 31; Ex. 1004, Figs. 2, 6. As to Fig. 2, Rompaey states it outputs a "net list," which as McAlexander explains, "'refers to a hardware IC design, rather than software that may be executed on a designed IC to control a device.'" POPR, 30 (quoting Ex. 2001 ¶76). Rompaey goes on to say that "[t]his output preferably comprises structural VHDL ***or*** Verilog and machine code for the programmable processors."

Ex. 1004, 11:12-20. This "output" can therefore take two forms— depending on whether it is destined for the foundry or for Rompaey's simulator:

1) "structural VHDL," *id.*, Fig. 6, 9:58-59, 10:3-5; "***or***"
2) "Verilog and machine code for the programmable processors," *see id.*, 11:14, 5:31-39, 6:35-43, 9:14-15, 20:39-44.

The "VHDL" option corresponds to VHDL 12 on Figure 2, and is necessarily a hardware design such as for a foundry. POPR, 27, 29, 31. The "Verilog" option corresponds to the arrow from SYMPHONY 11 to Co-Simulator 9 on Figure 2, and is necessarily for simulation, such as to test or "debug[]" Rompaey's design. Ex. 1004, 5:31-39, 11:14. As a few minutes on Wikipedia will readily confirm, Verilog hardware descriptions were suitable only for simulation at the time of Rompaey (1995-96). And to simulate the hardware design, Rompaey would have needed both Verilog description and "machine code" to program its "instruction set simulator for [each] programmable processor." *Id.*, 21:7-18. None of this output is software programming commands to be executed on a hardware IC, as 1[d] recites.

Arm now argues that Rompaey's claims 6, 8 and 36 "generate and output" a "'database.'" PReply, 9. To borrow language from the Reply (*id.*, 6), this argument is nonsensical. Rompaey could not be any clearer that this "database" is ***part*** of its "design environment" and "co-design tool." Ex. 1004, 7:32-35, 9:62. It is where Rompaey "I/O scenarios" are stored. *Id.*, 6:18-34, 8:5-38, 10:9-11, 26:50-60, Figs.

8, 18. If this really were an "output" it's hard to think of anything that wouldn't be.

Finally, Arm argues Rompaey's RAM/ROM blocks "stor[ing] … program code" meet 1[d] because they "fall within" Arm's interpretation of '899 FIG. 4, so Rompaey's "stat[ement] that [these blocks] 'store the program code' teaches outputting 'the program code' to be stored." PReply, 10. To the contrary, these disclosures merely describe hardware blocks that are part of Rompaey's "hardware IC design," and, when fabricated, can store program code. POPR, 40.

II. Petitioner's Change To The Scope Of Its *Fintiv* Stipulation Is Untimely.

The Related Litigation will resolve the '899's validity nearly a half-year before this IPR can. POPR, 56. The Petition, trying to make *Fintiv* factor 4 "weigh[] against discretionary denial" despite a looming court trial, offered a "*Sand Revolution*" stipulation limited to "the grounds in this Petition." Pet., 87. ICPillar relied on that position to devote over 5,000 words of the POPR to *Fintiv*. After the POPR, Arm now changes position and offers a conditional "*Sotera*" stipulation covering, if instituted, "any ground that "could have been reasonably raised" in IPR.

The Director's 6/21/2022 Memo stated that "the PTAB will not discretionarily deny institution of an IPR…where a petitioner stipulates not to pursue in a parallel… proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition," but she has since clarified that that is so only if the stipulation is timely. *See NXP USA v. Impinj, Inc.*, IPR2021-01556, #13

(9/7/2022) (precedential). *NXP* addressed the "limited question of whether the Board may reconsider a decision to deny institution based on a stipulation filed after the institution decision" and answered it in the affirmative—"hold[ing] that the only appropriate time for a petitioner to offer a stipulation related to the *Fintiv* factor 4 analysis is prior to the Board's decision of whether to institute." *Id.*, 3, 4. *NXP* leaves to the Board's discretion whether to accept pre-institution, post-POPR stipulations, as the Board has often held. *E.g.*, IPR2024-00064; IPR2023-01024, 00571. Whether to accept it depends on, *e.g.*, "gamesmanship," *NXP*, 4, and whether patent owners are "prejudiced by the timing of the stipulation," IPR2024-00083 #13, 20 (5/17/24).

Arm's change of position should be rejected. Unlike other cases where such belated stipulations have been accepted, this is Arm's second stipulation—it already took a position on Factor 4 stipulation in its Petition. Now, post-POPR, it's changing the scope of its offer to stipulate. This greatly prejudices ICPillar, which irreversibly committed over 1/3 of its POPR to *Fintiv* in reliance on Arm's initial stipulation. Arm offers no justification whatever for its delayed bait-and-switch. To accept it on these facts "would open the door to gamesmanship," *NXP*, 4, and frustrate *Fintiv*'s goals of avoiding duplication and waste (since the Court will decide validity almost half a year earlier) as well as Congress's goal of simple cost-effective proceedings—proceedings Arm itself is making more complex by belatedly changing its positions.

With or without Arm's belated new stances, institution should be denied.

Respectfully submitted,

____/ Kenneth J. Weatherwax /_____

Kenneth J. Weatherwax, Reg. No. 54,528
LOWENSTEIN & WEATHERWAX LLP

Date: June 20, 2024

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Patent Owner Preliminary Response (the "POPR") consists of 10 pages, excluding tables of contents, authorities and exhibits, signature block, certificate of service, and this certificate. The POPR complies with the type-volume limitation of 10 pages as mandated in Paper 7.

Respectfully submitted,

/ Kenneth J. Weatherwax /

Date: June 20, 2024

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the following documents were served by electronic service, by consent between the parties (Pet. at 90), on the date signed below:

PATENT OWNER'S AUTHORIZED PRELIMINARY SUR-REPLY

The names and address of the parties being served are as follows:

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Respectfully submitted,

/ Robert Pistone /

Date: June 20, 2024