AFFIDAVIT OF NATHANIEL E FRANK-WHITE

1. I am a Records Request Processor at the Internet Archive. I make this declaration of my own personal knowledge.

2. The Internet Archive is a website that provides access to a digital library of Internet sites and other cultural artifacts in digital form. Like a paper library, we provide free access to researchers, historians, scholars, and the general public. The Internet Archive has partnered with and receives support from various institutions, including the Library of Congress.

3. The Internet Archive has created a service known as the Wayback Machine. The Wayback Machine makes it possible to browse more than 450 billion pages stored in the Internet Archive's web archive. Visitors to the Wayback Machine can search archives by URL (i.e., a website address). If archived records for a URL are available, the visitor will be presented with a display of available dates. The visitor may select one of those dates, and begin browsing an archived version of the Web. Links on archived files in the Wayback Machine point to other archived files (whether HTML pages or other file types), if any are found for the URL indicated by a given link. For instance, the Wayback Machine is designed such that when a visitor clicks on a hyperlink on an archived page that points to another URL, the visitor will be served the archived file found for the hyperlink's URL with the closest available date to the initial file containing the hyperlink.

4. The archived data made viewable and browsable by the Wayback Machine is obtained by use of web archiving software that automatically stores copies of files available via the Internet, each file preserved as it existed at a particular point in time.

5. The Internet Archive assigns a URL on its site to the archived files in the format http://web.archive.org/web/[Year in yyyy][Month in mm][Day in dd][Time code in hh:mm:ss]/[Archived URL] aka an "extended URL". Thus, the extended URL http://web.archive.org/web/19970126045828/http://www.archive.org/ would be the URL for the record of the Internet Archive home page HTML file (http://www.archive.org/) archived on January 26, 1997 at 4:58 a.m. and 28 seconds (1997/01/26 at 04:58:28). The date indicated by an extended URL applies to a preserved instance of a file for a given URL, but not necessarily to any other files linked therein. Thus, in the case of a page constituted by a primary HTML file and other separate files (e.g., files with images, audio, multimedia, design elements, or other embedded content) linked within that primary HTML file, the primary HTML file and the other files will each have their own respective extended URLs and may not have been archived on the same dates.

6. Attached hereto as Exhibit A are true and accurate copies of browser screenshots of the Internet Archive's records of the archived files for the URLs and the dates specified in the attached coversheet of each printout.

7. Attached hereto as Exhibit B are true and accurate copies of the Internet Archive's records of the archived files for the URLs and the dates specified in the attached coversheet of each file.

8. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

DATE: 12/11/2023

Nathaniel Frank-White

Nathaniel E Frank-White

Please see attached All Purpose Jurat form for additional Notary Events

Microchip Ex. 1065, p. 2
Microchip v. Aptiv
IPR2024-00494

EXHIBIT A

https://web.archive.org/web/20130813011121/https://www.gsmarena.com/asus_google_nexus_7_2_2013-review-964p8.php

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REVIEWS

Asus Google Nexus 7 (2013) review: The magnificent seven

GSMArena team, 09 August 2013.

Asus Google Nexus 7 (2013) specs | User opinions and reviews | Comments (27)

Pages: « 1 2 3 4 5 6 7 8 9 10 » 8. Connectivity, web browser

Tags: Asus, Google, Android

Tons of local connectivity

The Nexus 7 tablet comes in two versions - 16GB/32GB. The version with LTE data connectivity will ship only with 32GB on board. For local connectivity, you get dual-band Wi-Fi a/b/g/n along with Wi-Fi Direct and Bluetooth 4.0.

The Nexus 7 supports NFC along with the latest version of Android Beam. This enables simple transfer of images between two NFC-enabled phones and you can pair a Bluetooth speaker with a simple tap (if it supports NFC, of course).

Wireless charging is also supported out of the box. It uses the popular Qi standard.

The tablet also comes with a built-in A-GPS receiver. User reports have emerged that the tablet would regularly lose GPS signal, though we are yet to experience such an event. Google however, is reportedly investigating the matter so if it's more than an isolated problem, a fix should be around the corner.

The microUSB port handles both charging and computer connections. You should note that there's no mass storage mode available, you'll have to use MTP instead. It works just as well for transferring most files but some files are a problem (e.g. a ZIP file we needed to offload from the device didn't show up in the explorer).

The Nexus 7 supports USB OTG out of the box unlike the previous generation Nexus 7. A standard adapter needed for the feature to work can be purchased separately.

Google Chrome keeps evolving

The tablet version of Google Chrome has tabs on the top - it all looks a lot like the desktop Chrome browser, complete with the new tab button. You can also use sideway swipes to switch between them.

Google Chrome on the Nexus 7

When you open a new tab, you're greeted with a list of the most visited sites. You can also access your bookmarks from here or even tabs you have open on any other device you have Chrome running on (your computer, your phone, even other tablets). Incognito tabs are available.

New tab options

The URL bar has a couple of handy shortcuts - one allows you to perform a voice search, which is quicker than typing, and the other is the star, which allows you to add a site to your bookmarks (this one should be familiar from desktop Chrome).

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The settings menu includes some really interesting options. For example, you can set your search provider to be Yahoo or Bing or request the desktop version of a site. You can also allow the browser to preload links from search results it's certain you're going to open, but you can also opt for enabling this over Wi-Fi only to preserve your data allowance.

Flash is, of course, not supported but as the web moves towards HTML5, Flash becomes less and less relevant. Still, if it's that important to you, you should know that we manage to side-load the Flash Player and enable it on some of the alternative browsers available at the Play Store. So if Flash is a must, you can have it.

NEXT PAGE »

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Pages: « 1 2 3 4 5 6 7 8 9 10 » 8. Connectivity, web browser

Asus Google Nexus 7 (2013) specs User opinions and reviews Comments (27)

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VOTING RESULTS

Design 6.0

Features 6.3

Performance 6.5

5 5 5

Votes: 13 Login

Like 0

Tablet with no support for GSM voice communication, SMS, and MMS.

This is not a GSM device, it will not work on any GSM network worldwide.

GENERAL	2G Network	N/A
	SIM	No
	Announced	2012, Q3
	Status	Available. Released 2012, November
BODY	Dimensions	259.1 x 175.3 x 12.2 mm (10.20 x 6.90 x 0.48 in)
	Weight	685 g (1.51 lb)
DISPLAY	Type	TFT capacitive touchscreen, 256K colors
	Size	800 x 1280 pixels, 10.1 inches (~149 ppi pixel density)
	Multitouch	Yes - Acer UI
SOUND	Alert types	N/A
	Loudspeaker	Yes, with stereo speakers
	3.5mm jack	Yes - Stereo sound
MEMORY	Card slot	microSD, up to 32 GB
	Internal	8/16 GB storage, 1 GB RAM
DATA	GPRS	No
	EDGE	No
	WLAN	Wi-Fi 802.11 b/g/n, Wi-Fi hotspot
	Bluetooth	Yes, v2.1 with EDR
	USB	Yes, microUSB v2.0, USB v2.0, USB On-the-go
CAMERA	Primary	2 MP, 1600x1200 pixels
	Features	Touch focus, face detection
	Video	Yes
	Secondary	No
FEATURES	OS	Android OS, v4.0 (Ice Cream Sandwich), upgradable to v4.1 (Jelly Bean)
	Chipset	Nvidia Tegra 3
	CPU	Quad-core 1.2 GHz
	GPU	ULP GeForce
	Sensors	Accelerometer, gyro
	Messaging	Email, Push Email, IM
	Browser	HTML5
	Radio	No
	GPS	Yes, with GLONASS
	Java	Yes, via Java MIDP emulator
	Colors	Titanium Gray - SNS integration - Google Search, Maps, Gmail - YouTube, Google Talk, Picasa - MP3/WAV/WMA/eAAC+ player - XviD/MP4/H.264/H.263 player - Organizer - Document viewer - Photo viewer/editor - Predictive text input
BATTERY		Non-removable Li-Po 3260 mAh battery
	Stand-by	
	Talk time	Up to 8 h (multimedia)
MISC	Price group	

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ACER PHONES
- Acer Liquid E2
- Acer Iconia Tab B1-A71
- Acer Liquid Z2
- Acer Iconia Tab A1-810
- Acer Liquid S1
- Acer Liquid Z110
- Acer CloudMobile

more phones

ACER ICONIA TAB A210 - USER OPINIONS AND REVIEWS

papu

nice tab frm other tab

2013-06-05 11:39 Y)K4 U Reply

Nigam-prasad

This is a very nice tab in budget. I use this from last 3-months. no problem. completely handy for use. good battery, nice touch, superb HD quality video. N with android 4.1 its just amaze. 1 thing negative is colors its 256k. But in this price u ne...

2013-02-27 05:09 uwmt C Reply

Tech_Chase

On paper it's a good tablet but it falls short of comparing with other tablets in

comparable price ranges. The battery life is somewhat of a hindrance when you consider my previous point. It's not that it's not advertised it's just overshadowed. But ...

2013-02-04 06:11 0dbj R Reply

Read all opinions | Post your opinion | Total user opinions: **5**

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Samsung I9500 Galaxy S4

SAMSUNG

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Samsung Galaxy S4 vs Galaxy S III: Advanced fence-sitting
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VOTING RESULTS
Design 6.5
Features 7.4
Performance 7.4
5 5 5
Votes: 3837 Login

Like 6.5k

GENERAL	2G Network	GSM 850 / 900 / 1800 / 1900
	3G Network	HSDPA 850 / 900 / 1900 / 2100
	4G Network	LTE (market dependent)
	SIM	Micro-SIM
	Announced	2013, March
	Status	Available. Released 2013, April
BODY	Dimensions	136.6 x 69.8 x 7.9 mm (5.38 x 2.75 x 0.31 in)
	Weight	130 g (4.59 oz)
DISPLAY	Type	Super AMOLED capacitive touchscreen, 16M colors
	Size	1080 x 1920 pixels, 5.0 inches (~441 ppi pixel density)
	Multitouch	Yes
	Protection	Corning Gorilla Glass 3
		- TouchWiz UI
SOUND	Alert types	Vibration; MP3, WAV ringtones
	Loudspeaker	Yes
	3.5mm jack	Yes
MEMORY	Card slot	microSD, up to 64 GB
	Internal	16/32/64 GB storage, 2 GB RAM
DATA	GPRS	Yes
	EDGE	Yes
	Speed	HSDPA, 42.2 Mbps; HSUPA, 5.76 Mbps
	WLAN	Wi-Fi 802.11 a/b/g/n/ac, dual-band, DLNA, Wi-Fi Direct, Wi-Fi hotspot
	Bluetooth	Yes, v4.0 with A2DP, EDR, LE
	NFC	Yes
	Infrared port	Yes
	USB	Yes, microUSB v2.0 (MHL 2), USB On-the-go, USB Host
CAMERA	Primary	13 MP, 4128 x 3096 pixels, autofocus, LED flash, check quality
	Features	Dual Shot, Simultaneous HD video and image recording, geo-tagging, touch focus, face and smile detection, image stabilization, HDR
	Video	Yes, 1080p@30fps, dual-video rec., check quality
	Secondary	Yes, 2 MP,1080p@30fps, dual video call
FEATURES	OS	Android OS, v4.2.2 (Jelly Bean)
	Chipset	Exynos 5 Octa 5410
	CPU	Quad-core 1.6 GHz Cortex-A15 & quad-core 1.2 GHz Cortex-A7
	GPU	PowerVR SGX 544MP3
	Sensors	Accelerometer, gyro, proximity, compass, barometer, temperature, humidity, gesture
	Messaging	SMS(threaded view), MMS, Email, Push Mail, IM, RSS
	Browser	HTML5
	Radio	No
	GPS	Yes, with A-GPS support and GLONASS
	Java	Yes, via Java MIDP emulator
	Colors	White Frost, Black Mist
		- Wireless charging (market dependent) - S-Voice natural language commands and dictation - Smart stay, Smart pause, Smart scroll - Air gestures - Dropbox (50 GB storage) - Active noise cancellation with dedicated mic - TV-out (via MHL 2 A/V link) - SNS integration - MP4/DivX/XviD/WMV/H.264/H.263 player - MP3/WAV/eAAC+/AC3/FLAC player - Organizer - Image/video editor - Document viewer (Word, Excel, PowerPoint, PDF) - Google Search, Maps, Gmail, YouTube, Calendar, Google Talk, Picasa - Voice memo/dial/commands - Predictive text input (Swype)
BATTERY		Li-Ion 2600 mAh battery
	Stand-by	(2G) / Up to 370 h (3G)
	Talk time	(2G) / Up to 17 h (3G)
	Music play	Up to 62 h
MISC	SAR US	0.85 W/kg (head) 1.55 W/kg (body)
	SAR EU	0.42 W/kg (head) 0.54 W/kg (body)
	Price group	
TESTS	Display	Contrast ratio: Infinite (nominal) / 3.352:1 (sunlight)

Samsung I9500 Galaxy S
Price history in EURO

cell:pex WHOLESALE TRADING BOARD

SAMSUNG PHONES
- Samsung I9500 Galaxy S4
- Samsung I9300 Galaxy S III
- Samsung Galaxy S Duos S7562
- Samsung Galaxy Mega 6.3 I9200
- Samsung Galaxy Grand I9082
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Loudspeaker	Voice 70dB / Noise 66dB / Ring 77dB
Audio quality	Noise -95.9dB / Crosstalk -96.4dB
Camera	Photo / Video

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SAMSUNG I9500 GALAXY S4 - USER OPINIONS AND REVIEWS

gopal

samsung is really no 1 phone

2013-07-01 22:22 vwes U Reply

raul

I have a samsung galaxy S4 in Honduras, with Tigo. Is very fast and smooth, awesome camera. Just a wonderful phone. I have read a lot of comments saying that GS4 is very slow and laggy. Based on my phone i said, IMPOSSIBLE! But i checked a GS4 bought...

2013-07-01 21:29 PbJu H Reply

Nik Vel

Hey all... I need to update 28mb new firmware update.. due to some issues wifi is nt connecting. . can someone guide me on how to get the same done through samsung kies pls.

2013-07-01 19:47 UjLr Q Reply

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Name	Last modified	Size	Description
Parent Directory			
FS6M12653RTC.pdf	09-Jul-2011 07:57	549K	
FS6S1265RE.pdf	09-Jul-2011 07:57	598K	
FSA110.pdf	09-Jul-2011 07:57	613K	
FSA1156.pdf	09-Jul-2011 07:57	769K	
FSA1157.pdf	09-Jul-2011 07:57	769K	
FSA1208.pdf	09-Jul-2011 07:57	456K	
FSA1211.pdf	09-Jul-2011 07:57	508K	
FSA1256.pdf	09-Jul-2011 07:57	503K	
FSA1256A.pdf	09-Jul-2011 07:57	503K	
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FSA203.pdf	09-Jul-2011 07:57	658K	
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FSA2156.pdf	09-Jul-2011 07:57	695K	
FSA221.pdf	09-Jul-2011 07:57	440K	
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FSA2258.pdf	09-Jul-2011 07:57	622K	
FSA2259.pdf	09-Jul-2011 07:57	597K	
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FSA2267A.pdf	09-Jul-2011 07:57	1M	
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FSA2467.pdf	09-Jul-2011 07:57	787K	
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FSA266.pdf	09-Jul-2011 07:57	209K	
FSA2866.pdf	09-Jul-2011 07:57	615K	
FSA3000.pdf	09-Jul-2011 07:57	456K	
FSA3157.pdf	09-Jul-2011 07:57	1M	
FSA3157B.pdf	09-Jul-2011 07:57	467K	
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FSA321.pdf	09-Jul-2011 07:57	524K	
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FSA5157.pdf	09-Jul-2011 07:57	542K	
FSA6157.pdf	09-Jul-2011 07:57	524K	

FSA641.pdf	09-Jul-2011 07:57	531K
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FSA66.pdf	09-Jul-2011 07:57	749K
FSA800.pdf	09-Jul-2011 07:57	621K
FSA8008.pdf	09-Jul-2011 07:57	639K
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FSA8009.pdf	09-Jul-2011 07:57	637K
FSA801.pdf	09-Jul-2011 07:57	242K
FSA8029.pdf	09-Jul-2011 07:57	638K
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FSA839.pdf	09-Jul-2011 07:57	562K
FSA859.pdf	09-Jul-2011 07:57	565K
FSA880.pdf	09-Jul-2011 07:57	312K
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FSA9280A.pdf	09-Jul-2011 07:57	720K
FSA9288A.pdf	09-Jul-2011 07:57	720K
FSAL200.pdf	09-Jul-2011 07:57	254K
FSAM10SH60A.pdf	09-Jul-2011 07:57	1M
FSAM15SH60A.pdf	09-Jul-2011 07:57	1M
FSAM15SM60A.pdf	09-Jul-2011 07:57	2M
FSAM20SH60A.pdf	09-Jul-2011 07:57	1M
FSAM20SM60A.pdf	09-Jul-2011 07:57	2M
FSAM30SH60A.pdf	09-Jul-2011 07:57	1M
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FSAR001B.pdf	09-Jul-2011 07:57	494K
FSAV330.pdf	09-Jul-2011 07:57	578K
FSAV331.pdf	09-Jul-2011 07:57	603K
FSAV430.pdf	09-Jul-2011 07:57	895K
FSAV433.pdf	09-Jul-2011 07:57	1023K
FSAV450.pdf	09-Jul-2011 07:57	995K
FSB32560.pdf	09-Jul-2011 07:57	268K
FSB50250.pdf	09-Jul-2011 07:57	433K
FSB50250S.pdf	09-Jul-2011 07:57	410K
FSB50250UD.pdf	09-Jul-2011 07:57	863K
FSB50250US.pdf	09-Jul-2011 07:57	298K
FSB50250UTD.pdf	09-Jul-2011 07:57	889K
FSB50325T.pdf	09-Jul-2011 07:57	413K
FSB50325TD.pdf	09-Jul-2011 07:57	897K
FSB50450.pdf	09-Jul-2011 07:57	417K
FSB50450S.pdf	09-Jul-2011 07:57	410K
FSB50450T.pdf	09-Jul-2011 07:57	398K
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FSB50450US.pdf	09-Jul-2011 07:57	298K
FSB50550T.pdf	09-Jul-2011 07:57	397K
FSB50550U.pdf	09-Jul-2011 07:57	343K
FSB50550US.pdf	09-Jul-2011 07:57	298K
FSB50550UTD.pdf	09-Jul-2011 07:57	893K
FSB50825US.pdf	09-Jul-2011 07:57	297K
FSB52006S.pdf	09-Jul-2011 07:57	236K
FSB560.pdf	09-Jul-2011 07:57	184K
FSB560A.pdf	09-Jul-2011 07:57	184K
FSB619.pdf	09-Jul-2011 07:57	33K
FSB649.pdf	09-Jul-2011 07:57	30K
FSB660A.pdf	09-Jul-2011 07:57	53K
FSB749.pdf	09-Jul-2011 07:57	29K
FSBB15CH60.pdf	09-Jul-2011 07:57	545K
FSBB15CH60C.pdf	09-Jul-2011 07:57	394K
FSBB15CH60F.pdf	09-Jul-2011 07:57	319K
FSBB20CH60.pdf	09-Jul-2011 07:57	544K
FSBB20CH60C.pdf	09-Jul-2011 07:57	514K

FSBB20CH60CL.pdf	09-Jul-2011 07:57	693K
FSBB20CH60CT.pdf	09-Jul-2011 07:57	408K
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FSBB30CH60.pdf	09-Jul-2011 07:57	563K
FSBB30CH60C.pdf	09-Jul-2011 07:57	517K
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FSBF15CH60BTL.pdf	09-Jul-2011 07:57	645K
FSBF3CH60B.pdf	09-Jul-2011 07:57	399K
FSBF5CH60B.pdf	09-Jul-2011 07:57	451K
FSBH0170.pdf	09-Jul-2011 07:57	795K
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FSBH0170_F116.pdf	09-Jul-2011 07:57	938K
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FSBH0270_F116.pdf	09-Jul-2011 07:57	938K
FSBH0370.pdf	09-Jul-2011 07:57	795K
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FST3253.pdf	09-Jul-2011 07:57	141K
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FSUSB45.pdf	09-Jul-2011 07:57	710K
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Part #, Keyword, Cross-reference

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Function
- Multimedia Switch (8)
- USB Switch (26)

Package Type
- DQFN (5)
- MicroPak (13)
- MLP (1)
- MSOP (6)
- QSOP (1)
- TSSOP (2)
- UMLP (17)
- US8 (2)
- WL-CSP (1)

Crosstalk
- -120 dB - -100 dB (1)
- -100 dB - -80 dB (1)
- -80 dB - -60 dB (10)
- -60 dB - -40 dB (18)
- -40 dB - -20 dB (5)

ESD
- 2 kV - 4 kV (8)
- 4 kV - 6 kV (7)
- 6 kV - 8 kV (11)
- 8 kV - 10 kV (6)
- 14 kV - 16 kV (5)

Leakage Current
- 0.05 uA (1)
- 0.1 uA (1)
- 0.5 uA (1)
- 1 uA (10)
- 2 uA (4)
- 3 uA (1)
- 10 uA (8)

Number of Switches
- 1 (14)
- 2 (8)
- 3 (2)
- 4 (1)
- 5 (1)

On Resistance
- 0 Ohm - 2 Ohm (2)
- 2 Ohm - 4 Ohm (7)
- 4 Ohm - 6 Ohm (3)
- 6 Ohm - 8 Ohm (12)
- 8 Ohm - 10 Ohm (6)

Product Family
- USB Switches (26)

Supply Voltage Range
- 1.65 - 5.5 (1)
- 2.5 - 4.4 (2)
- 2.7 - 4.3 (2)
- 2.7 - 4.5 (1)
- 2.7 - 5.5 (1)
- 3 - 4.4 (3)
- 3.0 - 3.4 (1)
- 3.0 - 3.6 (4)
- 3.0 - 4.3 (8)
- 3.0 - 4.4 (2)
- 4.0 - 6.0 (1)

Switches Configuration
- 2:1 (2)
- 3:1 (2)
- 3:1 with Charge D... (2)
- 3PDT (1)
- 4:1 (1)
- DCP CDP Charge De... (1)
- DPDT (12)
- DPST (1)
- SPDT (1)
- SPDT (NO/NC) (1)
- SPST (1)
- USB and Headphone... (1)

Off Isolation
- -100 dB - -80 dB (3)
- -80 dB - -60 dB (6)
- -60 dB - -40 dB (9)
- -40 dB - -20 dB (13)

TTL Control Inputs
- No (7)
- Yes (15)

Undershoot Protection
- No (18)
- Yes (4)

Bandwidth
- 250 MHz (1)
- 350 MHz (1)

Search | Search within the current results | Start Over!

Function = USB Switch

Your request so far: **Function** USB Switch (26)

Product Parametric Data

COMPARE

USB Switches (26) | View All Parameters | Download to Excel | Download to PDF

Part Number	Switches Configuration	Number of Switches	Bandwidth	ESD	Package Type	Function	Select All/None
NEW FSA9285 MCPC Compliant USB Port Multimedia Switch with Accessory Detection	3PDT	5		5.0	WL-CSP	Multimedia Switch USB Switch	
NEW FSA880 USB Port 2:1 Switch with Accessory and Charger Detection	2:1	1		15.0	UMLP	USB Switch	
NEW FSUSB74 High Speed USB 2.0 Switch/Multiplexer	4:1	1		2.0	MLP, UMLP	USB Switch	
NEW FSA831 USB2.0 High-Speed (480Mbps) Charger Detection with Isolation Switch	DCP CDP Charge Detection	2		15.0	MicroPak	USB Switch	
NEW FSUSB73 High Speed USB 2.0 Switch/Multiplexer	3:1	1		2.0	UMLP	USB Switch	
NEW FSA881 USB Port 2:1 Switch with Accessory and Charger Detection	2:1	1		15.0	UMLP	USB Switch	
FSUSB42 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	MSOP, UMLP	USB Switch	
FSUSB30 Low Power 2-Port Hi-Speed USB 2.0 (480 Mbps) Switch	DPDT	1	720.0	8.0	DQFN, MSOP, MicroPak, UMLP	USB Switch	
FSA221 Multimedia and USB 2.0 Hi-Speed and Audio Switches w/ Negative Signal Capability	DPDT	1	720.0	7.0	MSOP, MicroPak, UMLP	Multimedia Switch USB Switch	
FSA223 Multimedia and USB 2.0 Hi-Speed and Audio Switches w/ Negative Signal Capability	DPDT	1	720.0	7.5	MSOP, MicroPak, UMLP	Multimedia Switch USB Switch	
FSUSB31 Low Power Dual SPST Hi-Speed USB 2.0 (480 Mbps) Switch	SPST	2	720.0	7.5	MicroPak, UMLP, US8	USB Switch	
FSUSB63 3:1 HS - USB Switch / Multiplexer	3:1	1	830.0	16.0	UMLP	USB Switch	
FSA9280A USB 2.0 Accessory Detection Switch w/ 28V FET	3:1 with Charge Detection	3	720.0	4.0	UMLP	Multimedia Switch USB Switch	
FSUSB45 Hi-Speed USB2.0 (480Mbps) Switch w/Dedicated Charger Port Detect	DPDT	2	720.0	8.0	MicroPak, UMLP	USB Switch	
FSUSB11 Low Power Full Speed USB Switch	SPDT (NO/NC)	2	350.0	8.0	MicroPak, TSSOP	USB Switch	
FSUSB46 Hi-Speed USB2.0 (480Mbps) DPST Switch with Dedicated Charger Port Detection	DPST	2	720.0	16.0	MicroPak, UMLP, US8	USB Switch	
FSA9288A USB 2.0 Accessory Detection Switch w/ 28V FET	3:1 with Charge Detection	3	720.0	4.0	UMLP	Multimedia Switch USB Switch	
FSUSB20 Low Power 1 Port Hi-Speed USB (480Mbps) Switch	DPDT	2	750.0	4.0	DQFN, MSOP, MicroPak	USB Switch	
FSUSB22 Low Power 2 Port Hi-Speed USB 2.0 (480Mbps) Switch	SPDT	4	800.0	4.0	DQFN, QSOP, TSSOP	USB Switch	
FSUSB23 Low Power Hi-Speed USB 2.0 (480 Mbps) Switch	DPDT	1	750.0	7.0	DQFN, MicroPak	USB Switch	
FSA201 Multimedia, USB 2.0 and Audio Switch	DPDT	2	250.0	2.0	MSOP, MicroPak	Multimedia Switch USB Switch	
FSUSB40 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	7.0	MicroPak, UMLP	USB Switch	
FSA2000 Auto Selecting HS-USB Switch with Cap-Free Headphone Audio Amplifier	USB and Headphone Amp	2	720.0	4.0	UMLP	Multimedia Switch USB Switch	
FSA203 Multimedia, Hi-Speed USB, Video, and Negative Swing Audio Switch with Video Amp/Filter	DPDT	1	780.0	5.5	DQFN	Multimedia Switch USB Switch	
FSUSB43 Low Power, Two-Port, Hi-Speed, USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	MicroPak	USB Switch	
FSUSB104 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	UMLP	USB Switch	

1 - 26 of 26 [Part Number]

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720 MHz (13)
750 MHz (2)
780 MHz (1)
800 MHz (1)
830 MHz (1)

Max T Off

0 ns - 100 ns (15)
900 ns - 1000 ns (1)
1000 ns - 1100 ns (1)
1900 ns - 2000 ns (1)
2000 ns - 2100 ns (1)
9900 ns - 10000 ns (1)

Max T On

0 ns - 500 ns (15)
500 ns - 1000 ns (1)
1000 ns - 1500 ns (1)
1500 ns - 2000 ns (1)
2000 ns - 2500 ns (1)
9500 ns - 10000 ns (1)

R On Flatness

0 Ohm - 0.5 Ohm (7)
0.5 Ohm - 1 Ohm (7)
1 Ohm - 1.5 Ohm (3)
1.5 Ohm - 2 Ohm (4)
2 Ohm - 2.5 Ohm (4)

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Function
- Multimedia Switch (7)
- USB Switch (24)

Package Type
- DQFN (5)
- MicroPak (12)
- MLP (1)
- MSOP (6)
- QSOP (1)
- TSSOP (2)
- UMLP (17)
- US8 (2)

Crosstalk
- -120 dB - -100 dB (1)
- -100 dB - -80 dB (1)
- -80 dB - -60 dB (8)
- -60 dB - -40 dB (17)
- -40 dB - -20 dB (5)

ESD
- 2 kV - 4 kV (8)
- 4 kV - 6 kV (6)
- 6 kV - 8 kV (11)
- 8 kV - 10 kV (6)
- 14 kV - 16 kV (4)

Leakage Current
- 0.05 uA (1)
- 0.5 uA (1)
- 1 uA (10)
- 2 uA (4)
- 3 uA (1)
- 10 uA (7)

Number of Switches
- 1 (14)
- 2 (7)
- 3 (2)
- 4 (1)

On Resistance
- 0 Ohm - 2 Ohm (2)
- 2 Ohm - 4 Ohm (6)
- 4 Ohm - 6 Ohm (3)
- 6 Ohm - 8 Ohm (11)
- 8 Ohm - 10 Ohm (6)

Product Family
- USB Switches (24)

Supply Voltage Range
- 1.65 - 5.5 (1)
- 2.5 - 4.4 (2)
- 2.7 - 4.3 (2)
- 2.7 - 4.5 (1)
- 2.7 - 5.5 (1)
- 3 - 4.4 (2)
- 3.0 - 3.4 (1)
- 3.0 - 3.6 (4)
- 3.0 - 4.3 (8)
- 3.0 - 4.4 (2)

Switches Configuration
- 2:1 (2)
- 3:1 (2)
- 3:1 with Charge D... (2)
- 4:1 (1)
- DPDT (12)
- DPST (1)
- SPDT (1)
- SPDT (NO/NC) (1)
- SPST (1)
- USB and Headphone... (1)

Off Isolation
- -100 dB - -90 dB (1)
- -80 dB - -70 dB (1)
- -70 dB - -60 dB (6)
- -60 dB - -50 dB (6)
- -50 dB - -40 dB (4)
- -40 dB - -30 dB (12)
- -30 dB - -20 dB (9)

Bandwidth
- 250 MHz (1)
- 350 MHz (1)
- 720 MHz (13)
- 750 MHz (2)
- 780 MHz (1)
- 800 MHz (1)
- 830 MHz (1)

TTL Control Inputs
- No (6)
- Yes (14)

Undershoot Protection

Search ☐ Search within the current results Start Over!

Function = USB Switch

Your request so far: **Function** USB Switch (24) ✕

Product Parametric Data

COMPARE

USB Switches (24) View All Parameters Download to Excel Download to PDF

Part Number	Switches Configuration	Number of Switches	Bandwidth	ESD	Package Type	Function	Select All/None
NEW FSUSB73 High Speed USB 2.0 Switch/Multiplexer	3:1	1		2.0	UMLP	USB Switch	☐
NEW FSA881 USB Port 2:1 Switch with Accessory and Charger Detection	2:1	1		15.0	UMLP	USB Switch	☐
NEW FSUSB74 High Speed USB 2.0 Switch/Multiplexer	4:1	1		2.0	MLP, UMLP	USB Switch	☐
NEW FSA880 USB Port 2:1 Switch with Accessory and Charger Detection	2:1	1		15.0	UMLP	USB Switch	☐
FSUSB42 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	MSOP, UMLP	USB Switch	☐
FSUSB30 Low Power 2-Port Hi-Speed USB 2.0 (480 Mbps) Switch	DPDT	1	720.0	8.0	DQFN, MSOP, MicroPak, UMLP	USB Switch	☐
FSA9280A USB 2.0 Accessory Detection Switch w/ 28V FET	3:1 with Charge Detection	3	720.0	4.0	UMLP	Multimedia Switch USB Switch	☐
FSA223 Multimedia and USB 2.0 Hi-Speed and Audio Switches w/ Negative Signal Capability	DPDT	1	720.0	7.5	MSOP, MicroPak, UMLP	Multimedia Switch USB Switch	☐
FSA221 Multimedia and USB 2.0 Hi-Speed and Audio Switches w/ Negative Signal Capability	DPDT	1	720.0	7.0	MSOP, MicroPak, UMLP	Multimedia Switch USB Switch	☐
FSUSB31 Low Power Dual SPST Hi-Speed USB 2.0 (480 Mbps) Switch	SPST	2	720.0	7.5	MicroPak, UMLP, US8	USB Switch	☐
FSUSB63 3:1 HS - USB Switch / Multiplexer	3:1	1	830.0	16.0	UMLP	USB Switch	☐
FSA9288A USB 2.0 Accessory Detection Switch w/ 28V FET	3:1 with Charge Detection	3	720.0	4.0	UMLP	Multimedia Switch USB Switch	☐
FSUSB11 Low Power Full Speed USB Switch	SPDT (NO/NC)	2	350.0	8.0	MicroPak, TSSOP	USB Switch	☐
FSUSB45 Hi-Speed USB2.0 (480Mbps) Switch w/Dedicated Charger Port Detect	DPDT	2	720.0	8.0	MicroPak, UMLP	USB Switch	☐
FSUSB20 Low Power 1 Port Hi-Speed USB (480Mbps) Switch	DPDT	2	750.0	4.0	DQFN, MSOP, MicroPak	USB Switch	☐
FSUSB46 Hi-Speed USB2.0 (480Mbps) DPST Switch with Dedicated Charger Port Detection	DPST	2	720.0	16.0	MicroPak, UMLP, US8	USB Switch	☐
FSUSB22 Low Power 2 Port Hi-Speed USB 2.0 (480Mbps) Switch	SPDT	4	800.0	4.0	DQFN, QSOP, TSSOP	USB Switch	☐
FSA201 Multimedia, USB 2.0 and Audio Switch	DPDT	2	250.0	2.0	MSOP, MicroPak	Multimedia Switch USB Switch	☐
FSUSB23 Low Power Hi-Speed USB 2.0 (480 Mbps) Switch	DPDT	1	750.0	7.0	DQFN, MicroPak	USB Switch	☐
FSUSB40 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	7.0	MicroPak, UMLP	USB Switch	☐
FSA2000 Auto Selecting HS-USB Switch with Cap-Free Headphone Audio Amplifier	USB and Headphone Amp	2	720.0	4.0	UMLP	Multimedia Switch USB Switch	☐
FSUSB43 Low Power, Two-Port, Hi-Speed, USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	MicroPak	USB Switch	☐
FSUSB104 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	UMLP	USB Switch	☐
FSA203 Multimedia, Hi-Speed USB, Video, and Negative Swing Audio Switch with Video Amp/Filter	DPDT	1	780.0	5.5	DQFN	Multimedia Switch USB Switch	☐

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No (17)
Yes (3)

Max T Off

0 ns - 100 ns (15)
900 ns - 1000 ns (1)
1000 ns - 1100 ns (1)
1900 ns - 2000 ns (1)
2000 ns - 2100 ns (1)
9900 ns - 10000 ns (1)

Max T On

0 ns - 500 ns (15)
500 ns - 1000 ns (1)
1000 ns - 1500 ns (1)
1500 ns - 2000 ns (1)
2000 ns - 2500 ns (1)
9500 ns - 10000 ns (1)

R On Flatness

0 Ohm - 0.5 Ohm (6)
0.5 Ohm - 1 Ohm (7)
1 Ohm - 1.5 Ohm (3)
1.5 Ohm - 2 Ohm (4)
2 Ohm - 2.5 Ohm (4)

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FSUSB30

Low Power 2-Port Hi-Speed USB 2.0 (480 Mbps) Switch

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General description

The FSUSB30 is a low power, two--port high-speed USB 2.0 switch. This part is configured as a double-pole double-throw (DPDT) switch and is optimized for switching between two high-speed (480Mbps) sources or a Hi-Speed and Full Speed (12Mbps) source. The FSUSB30 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.7pF. The wide bandwidth of this device (720MHz), exceeds the bandwidth needed to pass the 3rd harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB30 contains special circuitry on the D+/D- pins which allows the device to withstand an overvoltage condition when powered off. This device is also designed to minimize current consumption even when the control voltage applied to the S pin, is lower than the supply voltage (V_{CC}). This feature is especially valuable to ultra-portable applications such as cell phones, allowing for direct interface with the general purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

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Features

- Low On Capacitance, 3.7pF (typical)
- Low On Resistance, 6.5Ω (typical)
- Low power consumption (1μA maximum)
- 10μA maximum I_{CCT} over and expanded control voltage range (V_{IN} = 2.6V, V_{CC} = 4.3V)
- Wide -3dB bandwidth, >720MHz
- 8KV ESD protection
- Power OFF protection when V_{CC} = 0V, D+/D- pins can tolerate up to 5.25V
- Packaged in:
  - Pb-Free 10-lead MicroPak™ (1.6 x 2.1mm)
  - Pb-Free 14-lead DQFN
  - Pb-Free 10-lead MSOP
  - Pb-Free 10-lead UMLP (1.4 x 1.8mm)

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Applications

- Cell phone, PDA, Digital Camera, and Notebook LCD Monitor, TV, and Set-top Box

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Product status/pricing/packaging BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FSUSB30BQX	Full Production	Full Production	$0.86	DQFN	14	TAPE REEL	Line 1: **$Y** (Fairchild logo) **&Z** (Asm. Plant Code) **&2** (2-Digit Date Code) **&T** (Die Trace Code) Line 2: USB30
FSUSB30L10X	Full Production	Full Production	$0.86	MicroPak	10	TAPE REEL	Line 1: FJ
FSUSB30MUX	Full Production	Full Production	$1.10	MSOP	10	TAPE REEL	Line 1: **$Y** (Fairchild logo) **&Z** (Asm. Plant Code) **&2** (2-Digit Date Code) **&T** (Die Trace Code) Line 2: FSUSB Line 3: 30
FSUSB30UMX	Full Production	Full Production	$1.10	UMLP	10	TAPE REEL	Line 1: GJ

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FSUSB30 is available. Click here for more information .

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Models

Package & leads	Condition	Temperature range	Vcc range	Software version	Revision date

HSPICE					
DQFN-14	slow	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
	typical	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
	fast	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
MSOP-10	slow	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
	typical	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
	fast	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
MicroPak-10	fast	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
	typical	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
	slow	-40°C to 85°C	3V to 4.3V	2001.4	Jan 24, 2006
UMLP-10	TYPICAL	-40°C to 85°C	3V to 4V	2001.4	Feb 21, 2007
	FAST	-40°C to 85°C	3V to 4V	2001.4	Feb 21, 2007
hspice					
UMLP-10	SLOW	-40°C to 85°C	3V to 4.3V	2001.4	Feb 21, 2007

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Application notes

AN-6018: Fairchild USB Switch Advantage (155 K) Mar 30, 2007
AN-6019: AN-6019 Fairchild Analog Switch Products ESD Test Methodology Overview (67 K) Mar 30, 2007
AN-6019C: AN-6019C Fairchild Analog Switch Products ESD Test Methodology Overview - Simplified Chinese (116 K) Mar 30, 2007
AN-6022: AN-6022 Using the FSUSB30 to Comply with USB 2.0 Fault Condition Requirements (57 K) Mar 30, 2007
AN-6022SC: Simplified Chinese - AN-6022SC Using the FSUSB30/31 to Comply with USB 2.0 Fault Condition Requirements (116 K) Mar 30, 2007
AN-6022TC: Traditional Chinese - AN-6022TC - Using the FSUSB30/31 to Comply with USB 2.0 Fault Condition Requirements (123 K) Mar 30, 2007

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Qualification Support

Click on a product for detailed qualification data

Product
FSUSB30BQX
FSUSB30L10X
FSUSB30MUX
FSUSB30UMX

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AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers

Last Updated: Jun 08, 2015

Version: **

AN96527 explains technological advances introduced by the USB-IF Type-C Specification and the Power Delivery Specification and how they can be designed into practical products using Cypress CCG1 Controllers. Four application areas are explored: host design, cable design, peripheral design, and power adapter design. Working prototype reference designs are presented for each application area, along with design and debug tools.

Related Files

File Title	Language	Size	Last Updated
AN96527.pdf	English	3.89 MB	06/08/2015

Need help? Ask a question and find answers in the Cypress Developer Community Forums.

Low/intermittent bandwidth users tip: Firefox and Chrome browsers will allow downloads to be resumed if your connection is lost during download.

Related Resources

Application Notes	
AN94150 - Designing a SuperSpeed Hub Using HX3 with Optimized BOM	02/09/2015

Development Kits/Boards	
CY4501 CCG1 Development Kit	07/16/2015
CY8CKIT-040 PSoC 4000 Pioneer Development Kit	06/24/2015

RELATED RESOURCES

Application Notes (1)
Development Kits/Boards (2)

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High-Speed, 2-of-4 Crosspoint Switch Handles USB 2.0 Data Rates

Note to Editor:

- The MAX4989 is a bidirectional, 2-of-4, USB 2.0 crosspoint switch.
- This device allows any 2 out of 4 combinations of USB pairs to be switched at one time, thus enabling multiple USB host devices to be switched simultaneously.
- This performance is enabled by the MAX4989's low-on-resistance and low-on-capacitance switching architecture.
- The MAX4989 is an ideal solution for notebook and cell phone applications.

Bidirectional, 2-of-4 Crosspoint Switch Supports Hi-Speed USB
Bidirectional, 2-of-4 Crosspoint Switch Supports Hi-Speed USB
[High-Resolution Images]

SUNNYVALE, CA—October 23, 2008—Maxim Integrated Products (NASDAQ: MXIM) introduces the **MAX4989**, a bidirectional, 2-of-4, USB 2.0 crosspoint switch. This device switches any 2 of 4 USB pairs while supporting data rates up to 480Mbps, thus enabling multiple USB host devices to be switched simultaneously. To enable this performance, the MAX4989 features 5.0Ω (typ) on-resistance and low, 6.0pF (typ) on-capacitance switching architecture. Additionally, an integrated charge pump improves performance, providing the full rail-to-rail swing necessary to support Hi-Speed USB applications, making it also compatible with Original USB. This combination of features makes the MAX4989 ideal for applications such as notebooks and cell phones.

To minimize power consumption, the MAX4989 provides three control-logic inputs that can all be driven high or low to place the device in shutdown mode. Shutdown mode reduces the supply current to less than 0.5µA and places all switch terminals in high impedance.

The MAX4989 operates from a single 2.7V to 5.5V supply, and is fully specified over the -40°C to +85°C extended temperature range. The device is available in an ultra-small, 3mm x 3mm, 14-pin TDFN package. Prices start at $1.50 (1000-up, FOB USA).

Maxim Integrated Products is a publicly traded company that designs, manufactures, and sells over $2 billion of high-performance semiconductor products annually. It was founded over 25 years ago with the mission to deliver innovative analog and mixed-signal engineering solutions that add value to its customers' products. To date, Maxim has developed over 5800 products serving the industrial, communications, consumer, and computing markets. For more information, go to www.maxim-ic.com.

Editors Contact: PR-USA@maxim-ic.com
Customer Service: 1-800-998-8800
Additional Information: MAX4989
- QuickView Data Sheet
- Full Data Sheet (PDF)

High-Resolution Images: - Download RGB: (TIF.ZIP) (JPG)
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We introduce an average of one new IC every day! Stay up to date:

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RESOURCE	LINKS	DESCRIPTION
2008-11-04		
Data Sheets	QV DS	**REVISED:** MAX3580 Direct-Conversion TV Tuner
Data Sheets	QV DS	**REVISED:** DS2413 1-Wire Dual Channel Addressable Switch
Data Sheets	QV DS	**NEW:** MAX5963 Dual, 7.5V to 76V, Hot-Swap and Diode ORing Controller
Data Sheets	QV DS	**NEW:** MAX15031 80V, 300mW Boost Converter and Current Monitor for APD Bias Applications
Data Sheets	QV DS	**NEW:** DS1862A XFP Laser Control and Digital Diagnostic IC
2008-11-03		
App Notes	AN	How to Add Margining Capability to a DC-DC Converter
New Products	PR	MAX19985A Highest Linearity, Dual, SiGe Downconversion Mixer for 2.5G, 3G, and 4G Base Stations
Data Sheets	QV DS	**NEW:** MAX4810, MAX4811, MAX4812 Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers
2008-10-31		
Data Sheets	QV DS	**NEW:** DS33M30, DS33M31, DS33M33 Ethernet Over SONET/SDH Mapper
2008-10-30		
New Products	PR	DS8024 Smart-Card Interface IC Provides Superior ESD Protection
Data Sheets	QV DS	**REVISED:** DS1875 PON Triplexer and SFP Controller
Data Sheets	QV DS	**REVISED:** MAX9655, MAX9656 Low-Power Video Switches for Dual SCART Connectors
Data Sheets	QV DS	**NEW:** MAX19505 Dual-Channel, 8-Bit, 65Msps ADC
Data Sheets	QV DS	**REVISED:** MAX16052, MAX16053 High-Voltage, Adjustable Sequencing/Supervisory Circuits
Data Sheets	QV DS	**NEW:** MAX4885E Ultra Low-Capacitance VGA Switch with ±15kv ESD
Data Sheets	QV DS	**NEW:** MAX17031 Dual Quick-PWM, Step-Down Controller with Low-Power LDO and RTC Regulator for MAIN Supplies
Data Sheets	QV DS	**REVISED:** DS3514 I²C Gamma and V_{COM} Buffer with EEPROM
2008-10-29		
Business Press Releases	BPR	Maxim Announces First Quarter Fiscal 2009 Results
New Products	PR	MAX3678 Frequency Synthesizer with Intelligent Dynamic Switching Provides Sub-Picosecond Jitter for High-End Servers
Data Sheets	QV DS	**REVISED:** DS1922E High-Temperature Logger iButton® with 8KB Data-Log Memory
2008-10-28		
Data Sheets	QV DS	**REVISED:** DS4402, DS4404 Two/Four-Channel, I²C Adjustable Current DAC
Data Sheets	QV DS	**REVISED:** DS4412 Dual-Channel, I²C Adjustable Sink/Source Current DAC
Data Sheets	QV DS	**REVISED:** MAX8610, MAX8611, MAX8611V, MAX8612, MAX8613 8-Channel PMICs for Digital Camera Power Supplies
Data Sheets	QV DS	**NEW:** MAX17000A Complete DDR2 and DDR3 Memory Power-Management Solution
2008-10-27		
Design Guides	DG	MICROPROCESSOR SUPERVISORY - English (26th edition)
New Products	PR	MAX19517 Industry's Lowest Power, Dual-Channel, 10-Bit ADCs Offer Superior Dynamic Performance
New Products	PR	MAX19516 Industry's Lowest Power, Dual-Channel, 10-Bit ADCs Offer Superior Dynamic Performance
New Products	PR	MAX19515 Industry's Lowest Power, Dual-Channel, 10-Bit ADCs Offer Superior Dynamic Performance
Data Sheets	QV DS	**REVISED:** DS34T101, DS34T102, DS34T104, DS34T108 Single/Dual/Quad/Octal TDM-Over-Packet Chip
Data Sheets	QV DS	**NEW:** DS4266 DDR Clock Oscillator
Data Sheets	QV DS	**NEW:** MAX9892 Shunt Mode Audio Click-and-Pop Eliminator
Data Sheets	QV DS	**NEW:** MAX8857A Smallest, All-Internal MOSFET, 7-Channel 2 AA DSC PMIC

2008-10-24		
Data Sheets	QV DS	**NEW:** MAX8680 Smallest, All-Internal MOSFET, 7-Channel DSC PMIC in Tiny 5mm x 5mm Thin QFN
Data Sheets	QV DS	**NEW:** MAX8858 Smallest, All-Internal MOSFET, 6-Channel DSC PMIC in a 5mm x 5mm TQFN
2008-10-23		
New Products	PR	MAX4989 High-Speed, 2-of-4 Crosspoint Switch Handles USB 2.0 Data Rates
2008-10-22		
New Products	PR	MAX16826 Dynamically Programmable, Four-String HB LED Driver Maximizes System Flexibility
Data Sheets	QV DS	**REVISED:** MAX3785 6.25Gbps, 1.8V PC Board Equalizer
2008-10-21		
Data Sheets	QV DS	**REVISED:** DS1992, DS1993 1Kb/4Kb Memory iButton®
Data Sheets	QV DS	**NEW:** DS8500 HART Modem
2008-10-20		
New Products	PR	DS2726 Single-Chip Lithium-Ion Protector Provides Comprehensive Protection and Cell Balancing for 5- to 10-Cell Battery Packs
Data Sheets	QV DS	**NEW:** DS26514 4-Port T1/E1/J1 Transceiver
Data Sheets	QV DS	**REVISED:** MAX8625A High-Efficiency, Seamless Transition, Step-Up/Down DC-DC Converter
2008-10-17		
App Notes	AN	Getting Started with the MAXQ1850 Evaluation Kit (EV Kit) and the CrossWorks Compiler for the MAXQ30
Data Sheets	QV DS	**REVISED:** DS1388 I²C RTC/Supervisor with Trickle Charger and 512 Bytes EEPROM
Data Sheets	QV DS	**REVISED:** MAX17007A, MAX17008 Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers
Data Sheets	QV DS	**NEW:** DS2741 Current Monitor and Accumulator with Integrated Sense Resistor
2008-10-16		
New Products	PR	MAX14752, MAX14753 High-Voltage Multiplexers Eliminate the Need for External Protection on Switch Inputs
Data Sheets	QV DS	**REVISED:** DS1307 64 x 8, Serial, I²C Real-Time Clock
Data Sheets	QV DS	**REVISED:** MAX1165, MAX1166 Low-Power, 16-Bit Analog-to-Digital Converters with Parallel Interface
Data Sheets	QV DS	**REVISED:** DS1375 I²C Digital Input RTC with Alarm
2008-10-15		
New Products	PR	MAX8819A, MAX8819B, MAX8819C, MAX8819D Industry's Smallest Power-Management Solution for Portable Media Players
Data Sheets	QV DS	**REVISED:** DS1990A Serial Number iButton
2008-10-14		
Business Press Releases	BPR	Maxim Integrated Products Announces Acquisition of Digital Video Leader Mobilygen
Data Sheets	QV DS	**NEW:** DS3645 4KB Secure Memory with Tamper Protection and RTC for Network Server Applications
2008-10-13		
Design Guides	DG	HIGH-SPEED ADCs, DACs, & AFEs - Chinese (11th edition)
Business Press Releases	BPR	Maxim Announces Preliminary First Quarter 2009 Results and $750 Million Share Repurchase Authorization; Aggregate Repurchase Authorization May Be Increased to $1.5 Billion
New Products	PR	MAX9655, MAX9656 3.3V, Video-Only, Dual-SCART Switches Reduce Cost and Complexity in European STB Designs
Data Sheets	QV DS	**REVISED:** MAX667 +5V Programmable, Low-Dropout Voltage Regulator
Data Sheets	QV DS	**REVISED:** MAX882, MAX883, MAX884 5V/3.3V or Adjustable, Low-Dropout, Low-I_Q, 200mA Linear Regulator with Standby Mode
Data Sheets	QV DS	**REVISED:** MAX4193, MAX630 CMOS Micropower Step-Up Switching Regulator
Data Sheets	QV DS	**REVISED:** MAX3643 155Mbps to 2.5Gbps Burst-Mode Laser Driver
Data Sheets	QV DS	**REVISED:** MAX9650, MAX9651 High-Current VCOM Drive Op Amps for TFT LCDs
2008-10-10		
Design Guides	DG	HIGH-SPEED ADCs, DACs, & AFEs - Japanese (11th edition)
Data Sheets	QV DS	**NEW:** MAX8879 Charge Pump for Backlight/Flash/RGB LEDs with Safety Timer
2008-10-09		
Data Sheets	QV DS	**REVISED:** DS2431 1024-Bit 1-Wire EEPROM
Data Sheets	QV DS	**REVISED:** MAX16016, MAX16020, MAX16021 Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating
Data Sheets	QV DS	**NEW:** MAXQ610 16-Bit Microcontroller with Infrared Module
2008-10-08		
New Products	PR	MAX5961 Quad Hot-Swap Controller Integrates Most Advanced System-Monitoring Features
2008-10-07		
App Notes	AN	Optimization of the MAX4990 High-Voltage DC-AC Converter for EL Lamps
2008-10-06		
Business Press Releases	BPR	Maxim Appoints Bruce E. Kiddoo as Chief Financial Officer

New Products	PR	MAX1377, MAX1379, MAX1383 Dual SPI Interface Maximizes Data Transfer for Dual, 12-Bit, 1.25Msps, Simultaneous-Sampling ADCs
Data Sheets	QV DS	**NEW:** MAX8856 USB/AC Adapter, Li+ Linear Battery Charger with Integrated 50mΩ Battery Switch in TDFN
App Notes	AN	A Filter Primer

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MAX4989

USB 2.0 Hi-Speed 2 of 4 Crosspoint Switch

The MAX4989 Features a Low On-Resistance and Low On-Capacitance Switching- Architecture Ideal for Notebook Applications

QuickView | Technical Documents | Ordering Info | More Information | All

Description

The MAX4989 is a bidirectional 2-of-4 USB 2.0 crosspoint switch. The MAX4989 features the low on-capacitance and low on-resistance necessary to switch USB 2.0 low-/full-/Hi-Speed signals at data rates up to 480Mbps. This device allows any 2-of-4 USB pairs to be connected together and is configured through a simple 3-input control logic interface.

FULL DATA SHEET (PDF, 112kB)
Download E-Mail

The MAX4989 operates from a single +2.7V to +5.5V supply and features an internal charge pump to permit full rail-to-rail swing. This device also features a high-impedance shutdown mode to reduce supply current to 100nA (typ).

The MAX4989 is available in a 14-pin, 3mm x 3mm TDFN package and operates over the extended -40°C to +85°C temperature range.

Key Features

- Single +2.7V to +5.5V Supply Voltage
- Low 1µA (typ) Supply Current
- -3dB Bandwidth: 1GHz (typ)
- Low 5Ω (typ) R_{ON}
- High-Impedance Shutdown Mode
- Logic Inputs Control Signal Routing
- +1.8V CMOS-Logic Compatible
- Ultra-Small 14-Pin, 3mm x 3mm, TDFN Package

Applications/Uses

- Notebook Computers

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Filter results

Function
- Multimedia Switch (8)
- USB Switch (26)

Package Type
- DQFN (5)
- MicroPak (13)
- MLP (1)
- MSOP (6)
- QSOP (1)
- TSSOP (2)
- UMLP (17)
- US8 (2)
- WL-CSP (1)

Crosstalk
- -120 dB - -100 dB (1)
- -100 dB - -80 dB (1)
- -80 dB - -60 dB (10)
- -60 dB - -40 dB (18)
- -40 dB - -20 dB (5)

ESD
- 2 kV - 4 kV (8)
- 4 kV - 6 kV (7)
- 6 kV - 8 kV (11)
- 8 kV - 10 kV (6)
- 14 kV - 16 kV (5)

Leakage Current
- 0.05 uA (1)
- 0.1 uA (1)
- 0.5 uA (1)
- 1 uA (10)
- 2 uA (4)
- 3 uA (1)
- 10 uA (8)

Number of Switches
- 1 (14)
- 2 (8)
- 3 (2)
- 4 (1)
- 5 (1)

On Resistance
- 0 Ohm - 2 Ohm (2)
- 2 Ohm - 4 Ohm (7)
- 4 Ohm - 6 Ohm (3)
- 6 Ohm - 8 Ohm (12)
- 8 Ohm - 10 Ohm (6)

Product Family
- USB Switches (26)

Supply Voltage Range
- 1.65 - 5.5 (1)
- 2.5 - 4.4 (2)
- 2.7 - 4.3 (2)
- 2.7 - 4.5 (1)
- 2.7 - 5.5 (1)
- 3 - 4.4 (3)
- 3.0 - 3.4 (1)
- 3.0 - 3.6 (4)
- 3.0 - 4.3 (8)
- 3.0 - 4.4 (2)
- 4.0 - 6.0 (1)

Switches Configuration
- 2:1 (2)
- 3:1 (2)
- 3:1 with Charge D... (2)
- 3PDT (1)
- 4:1 (1)
- DCP CDP Charge De... (1)
- DPDT (12)
- DPST (1)
- SPDT (1)
- SPDT (NO/NC) (1)
- SPST (1)
- USB and Headphone... (1)

Off Isolation
- -100 dB - -80 dB (3)
- -80 dB - -60 dB (6)
- -60 dB - -40 dB (9)
- -40 dB - -20 dB (13)

TTL Control Inputs
- No (7)
- Yes (15)

Undershoot Protection
- No (18)
- Yes (4)

Bandwidth
- 250 MHz (1)
- 350 MHz (1)

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Function = USB Switch

Your request so far: **Function** USB Switch (26) ✕

Product Parametric Data

COMPARE

USB Switches (26) View All Parameters Download to Excel Download to PDF

Part Number	Switches Configuration	Number of Switches	Bandwidth	ESD	Package Type	Function	Select All/None
NEW FSA9285 MCPC Compliant USB Port Multimedia Switch with Accessory Detection	3PDT	5		5.0	WL-CSP	Multimedia Switch USB Switch	☐
NEW FSA880 USB Port 2:1 Switch with Accessory and Charger Detection	2:1	1		15.0	UMLP	USB Switch	☐
NEW FSUSB74 High Speed USB 2.0 Switch/Multiplexer	4:1	1		2.0	MLP, UMLP	USB Switch	☐
NEW FSUSB73 High Speed USB 2.0 Switch/Multiplexer	3:1	1		2.0	UMLP	USB Switch	☐
NEW FSA831 USB2.0 High-Speed (480Mbps) Charger Detection with Isolation Switch	DCP CDP Charge Detection	2		15.0	MicroPak	USB Switch	☐
NEW FSA881 USB Port 2:1 Switch with Accessory and Charger Detection	2:1	1		15.0	UMLP	USB Switch	☐
FSUSB42 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	MSOP, UMLP	USB Switch	☐
FSUSB30 Low Power 2-Port Hi-Speed USB 2.0 (480 Mbps) Switch	DPDT	1	720.0	8.0	DQFN, MSOP, MicroPak, UMLP	USB Switch	☐
FSA221 Multimedia and USB 2.0 Hi-Speed and Audio Switches w/ Negative Signal Capability	DPDT	1	720.0	7.0	MSOP, MicroPak, UMLP	Multimedia Switch USB Switch	☐
FSA223 Multimedia and USB 2.0 Hi-Speed and Audio Switches w/ Negative Signal Capability	DPDT	1	720.0	7.5	MSOP, MicroPak, UMLP	Multimedia Switch USB Switch	☐
FSA9280A USB 2.0 Accessory Detection Switch w/ 28V FET	3:1 with Charge Detection	3	720.0	4.0	UMLP	Multimedia Switch USB Switch	☐
FSUSB31 Low Power Dual SPST Hi-Speed USB 2.0 (480 Mbps) Switch	SPST	2	720.0	7.5	MicroPak, UMLP, US8	USB Switch	☐
FSUSB63 3:1 HS - USB Switch / Multiplexer	3:1	1	830.0	16.0	UMLP	USB Switch	☐
FSUSB11 Low Power Full Speed USB Switch	SPDT (NO/NC)	2	350.0	8.0	MicroPak, TSSOP	USB Switch	☐
FSUSB45 Hi-Speed USB2.0 (480Mbps) Switch w/Dedicated Charger Port Detect	DPDT	2	720.0	8.0	MicroPak, UMLP	USB Switch	☐
FSA9288A USB 2.0 Accessory Detection Switch w/ 28V FET	3:1 with Charge Detection	3	720.0	4.0	UMLP	Multimedia Switch USB Switch	☐
FSUSB20 Low Power 1 Port Hi-Speed USB (480Mbps) Switch	DPDT	2	750.0	4.0	DQFN, MSOP, MicroPak	USB Switch	☐
FSUSB22 Low Power 2 Port Hi-Speed USB 2.0 (480Mbps) Switch	SPDT	4	800.0	4.0	DQFN, QSOP, TSSOP	USB Switch	☐
FSUSB46 Hi-Speed USB2.0 (480Mbps) DPST Switch with Dedicated Charger Port Detection	DPST	2	720.0	16.0	MicroPak, UMLP, US8	USB Switch	☐
FSUSB23 Low Power Hi-Speed USB 2.0 (480 Mbps) Switch	DPDT	1	750.0	7.0	DQFN, MicroPak	USB Switch	☐
FSUSB40 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	7.0	MicroPak, UMLP	USB Switch	☐
FSA201 Multimedia, USB 2.0 and Audio Switch	DPDT	2	250.0	2.0	MSOP, MicroPak	Multimedia Switch USB Switch	☐
FSA2000 Auto Selecting HS-USB Switch with Cap-Free Headphone Audio Amplifier	USB and Headphone Amp	2	720.0	4.0	UMLP	Multimedia Switch USB Switch	☐
FSA203 Multimedia, Hi-Speed USB, Video, and Negative Swing Audio Switch with Video Amp/Filter	DPDT	1	780.0	5.5	DQFN	Multimedia Switch USB Switch	☐
FSUSB43 Low Power, Two-Port, Hi-Speed, USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	MicroPak	USB Switch	☐
FSUSB104 Low Power, Two-Port, Hi-Speed USB2.0 (480Mbps) Switch	DPDT	1	720.0	8.0	UMLP	USB Switch	☐

1 - 26 of 26 [Part Number] Page : 1

720 MHz (13)
750 MHz (2)
780 MHz (1)
800 MHz (1)
830 MHz (1)

Max T Off

0 ns - 100 ns (15)
900 ns - 1000 ns (1)
1000 ns - 1100 ns (1)
1900 ns - 2000 ns (1)
2000 ns - 2100 ns (1)
9900 ns - 10000 ns (1)

Max T On

0 ns - 500 ns (15)
500 ns - 1000 ns (1)
1000 ns - 1500 ns (1)
1500 ns - 2000 ns (1)
2000 ns - 2500 ns (1)
9500 ns - 10000 ns (1)

R On Flatness

0 Ohm - 0.5 Ohm (7)
0.5 Ohm - 1 Ohm (7)
1 Ohm - 1.5 Ohm (3)
1.5 Ohm - 2 Ohm (4)
2 Ohm - 2.5 Ohm (4)

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EXHIBIT B

https://web.archive.org/web/20070508122710/http://www.fairchildsemi.com:80/ds/FS/FSUSB30.pdf

Click to see this datasheet in Simplified Chinese!

FAIRCHILD SEMICONDUCTOR®

January 2007

FSUSB30
Low-Power 2-Port Hi-Speed USB 2.0 (480Mbps) Switch

Features

- Low On Capacitance, 3.7pF (typical)
- Low On Resistance, 6.5Ohm (typical)
- Low power consumption (1µA maximum)
  - 10µA maximum I_{CCT} over an expanded control voltage range (V_{IN} = 2.6V, V_{CC} = 4.3V)
- Wide -3dB bandwidth, >720MHz
- 8KV ESD protection
- Power-Off protection when V_{CC} = 0V; D+/D- pins can tolerate up to 5.25V
- Packaged in:
  - Pb-Free 10-lead MicroPak™ (1.6 x 2.1mm)
  - Pb-Free 14-lead DQFN
  - Pb-Free 10-lead MSOP
  - Pb-Free 10-lead UMLP (1.4 x 1.8mm)

Applications

- Cell phone, PDA, Digital Camera, and Notebook LCD Monitor, TV, and Set-top Box

Related Application Notes

- *AN-6022 Using the FSUSB30 / FSUSB31 to Comply with USB 2.0 Fault Condition Requirements*

General Description

The FSUSB30 is a low-power, two-port, high-speed USB 2.0 switch. Configured as a double-pole double-throw (DPDT) switch, it is optimized for switching between two high-speed (480Mbps) sources or a Hi-Speed and Full-Speed (12Mbps) source. The FSUSB30 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.7pF. The wide bandwidth of this device (720MHz), exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk minimizes interference.

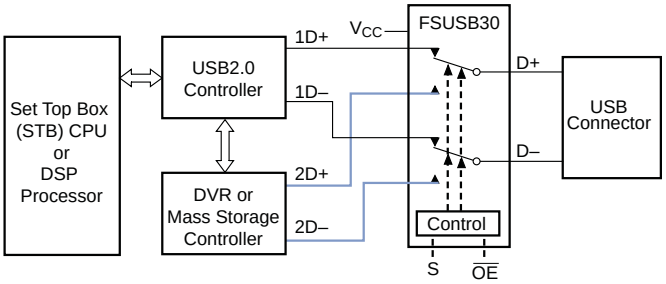
The FSUSB30 contains special circuitry on the D+/D- pins which allows the device to withstand an overvoltage condition when powered off. This device is also designed to minimize current consumption even when the control voltage applied to the S pin, is lower than the supply voltage (V_{CC}). This feature is especially valuable to ultra-portable applications such as cell phones, allowing for direct interface with the general purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Ordering Information

Order Number	Package Number	Product Code Top Mark	Pb-Free	Package Description
FSUSB30L10X	MAC010A	FJ	Yes	10-Lead MicroPak, 1.6 x 2.1mm
FSUSB30BQX	MLP014A	USB30	Yes	14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
FSUSB30MUX	MUA10A	FSUSB30	Yes	10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
FSUSB30UMX	MLP010A	GJ	Yes	10-Lead, Quad, Ultrathin, MLP (UMLP) 1.4 x 1.8mm

Pb-Free package per JEDEC J-STD-020B.

Application Diagram



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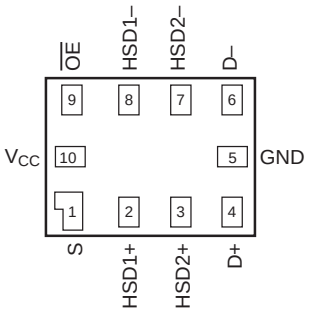
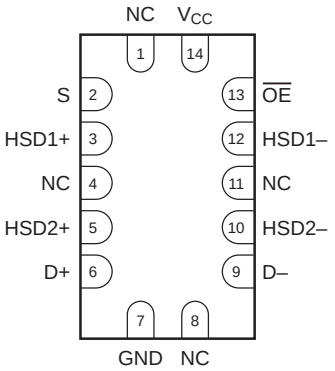
Connection Diagrams

Pad Assignments for MicroPak



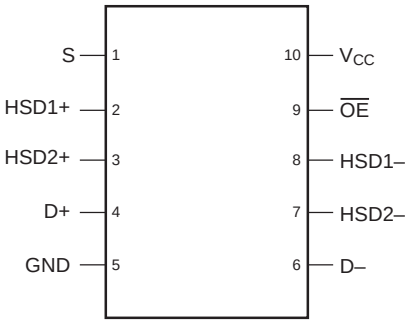
(Top View)

Pad Assignments for DQFN



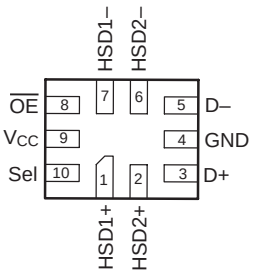
(Top Through View)

Pin Assignment for MSOP



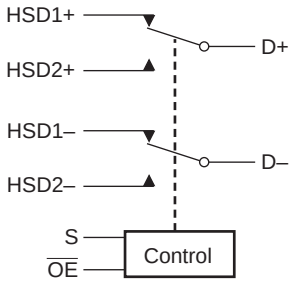
(Top Through View)

Pad Assignments for µMLP



(Top Through View)

Analog Symbol



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
D+, D–, HSDn+, HSDn–	Data Ports
NC	No Connect

Truth Table

S	$\overline{OE}$	Function
X	HIGH	Disconnect
LOW	LOW	D+, D– = $HSD1_n$
HIGH	LOW	D+, D– = $HSD2_n$

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Minimum	Maximum	Unit
V_{CC}	Supply Voltage		-0.5	+4.6	V
V_{CNTRL}	DC Input Voltage(1)		-0.5	+4.6	V
V_{SW}	DC Switch Voltage(1)	HSDnX	0.5	V_{CC} + 0.3	V
		D+,D- when V_{CC} > 0	0.5	V_{CC} + 0.3	V
		D+,D- when V_{CC} = 0	-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model	All Pins		8	kV
		I/O to GND		8	kV

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed. DC switch voltage may never exceed 4.6V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.(2)

Symbol	Parameter	Minimum	Maximum	Unit
V_{CC}	Supply Voltage	3.0	4.3	V
V_{IN}	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C
ΘJ_A	Thermal Resistance, 10 MicroPak		250	°C/W

Note:

2. Control input must be held HIGH or LOW and it must not float.

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DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = –40°C to +85°C			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN} = -18mA	3.0			-1.2	V
V_{IH}	Input Voltage HIGH		3.0 to 3.6	1.3			V
			4.3	1.7			V
V_{IL}	Input Voltage LOW		3.0 to 3.6			0.5	V
			4.3			0.7	V
I_{IN}	Control Input Leakage	V_{SW} = 0.0V to V_{CC}	4.3	-1.0		1.0	µA
I_{OZ}	OFF State Leakage	0 ≤ Dn, $HSD1_n$, $HSD2_n$ ≤ V_{CC}	4.3	-2.0		2.0	µA
I_{OFF}	Power OFF Leakage Current (D+, D–)	V_{SW} = 0V to 4.3V, V_{CC} = 0V	0	-2.0		2.0	µA
R_{ON}	Switch On Resistance(3)	V_{SW} = 0.4V, I_{ON} = -8mA	3.0		6.5	10.0	Ω
		V_{SW} = 0V, I_O = 30mA at 25°C	3.6			7.0	Ω
ΔR_{ON}	Delta R_{ON}(4)	V_{SW} = 0.4V, I_{ON} = -8mA	3.0		0.35		Ω
R_{ON} Flatness	R_{ON} Flatness(3)	V_{SW} = 0.0V - 1.0V, I_{ON} = -8mA	3.0		2.0		Ω
I_{CC}	Quiescent Supply Current	V_{CNTRL} = 0.0V or V_{CC}, I_{OUT} = 0	4.3			1.0	µA
I_{CCT}	Increase in I_{CC} Current per Control Voltage	V_{CNTRL} (control input) = 2.6V	4.3			10.0	µA

Notes:

3. Measured by the voltage drop between Dn, $HSD1_n$, $HSD2_n$ pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two ports.
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = –40°C to +85°C			Unit	Figure Number
				Min.	Typ.	Max.		
t_{ON}	Turn-On Time S, $\overline{OE}$ to Output	$HD1_n$, $HD2_n$ = 0.8V, R_L = 50Ω, C_L = 5pF	3.0 to 3.6		13.0	30.0	ns	Figure 8
t_{OFF}	Turn-Off Time S, $\overline{OE}$ to Output	$HD1_n$, $HD2_n$ = 0.8V, R_L = 50Ω, C_L = 5pF	3.0 to 3.6		12.0	25.0	ns	Figure 8
t_{PD}	Propagation Delay(4)	R_L = 50Ω, C_L = 5pF	3.3		0.25		ns	Figure 6 Figure 7
t_{BBM}	Break-Before-Make	R_L = 50Ω, C_L = 5pF, V_{IN} = 0.8V	3.0 to 3.6	2.0		6.5	ns	Figure 9
O_{IRR}	Off Isolation (Non-Adjacent)	f = 240MHz, R_T = 50Ω	3.0 to 3.6		-30.0		dB	Figure 12
Xtalk	Non-Adjacent Channel Crosstalk	R_T = 50Ω, f = 240MHz	3.0 to 3.6		-45.0		dB	Figure 13
BW	–3dB Bandwidth	R_T = 50Ω, C_L = 0pF	3.0 to 3.6		720		MHz	Figure 11
		R_T = 50Ω, C_L = 5pF			550			

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USB Hi-Speed Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = –40°C to +85°C			Units	Figure Number
				Min.	Typ.	Max.		
$t_{SK(O)}$	Channel-to-Channel Skew(5)	R_L = 50Ω, C_L = 5pF	3.0 to 3.6		50		ps	Figure 6 Figure 10
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(5)	R_L = 50Ω, C_L = 5pF	3.0 to 3.6		20		ps	Figure 6 Figure 10
t_J	Total Jitter(5)	R_L = 50Ω, C_L = 5pF, t_R = t_F = 500ps at 480 Mbps (PRBS = 2^{15} – 1)	3.0 to 3.6		200		ps	

Note:

5. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A = –40°C to +85°C			Units	Figure Number
			Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0V		1.5		pF	Figure 15
C_{ON}	$D1_n$, $D2_n$, Dn On Capacitance	V_{CC} = 3.3, $\overline{OE}$ = 0V		3.7		pF	Figure 14
C_{OFF}	$D1_n$, $D2_n$ Off Capacitance	V_{CC} and $\overline{OE}$ = 3.3		2.5		pF	Figure 15

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Typical Characteristics

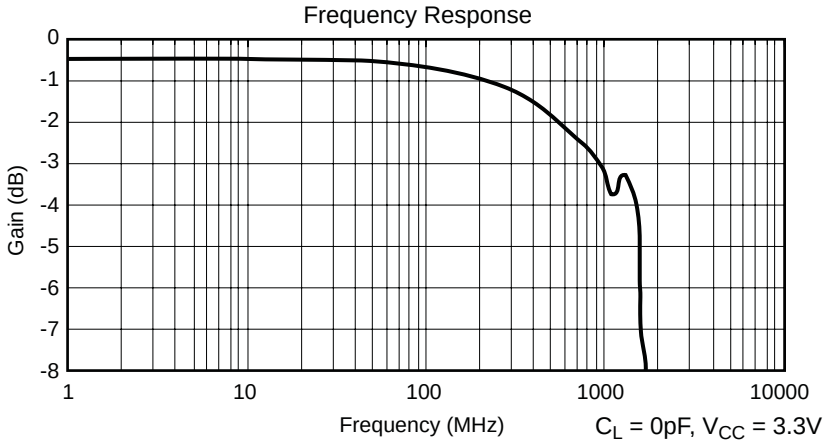

Figure 1. Gain vs. Frequency

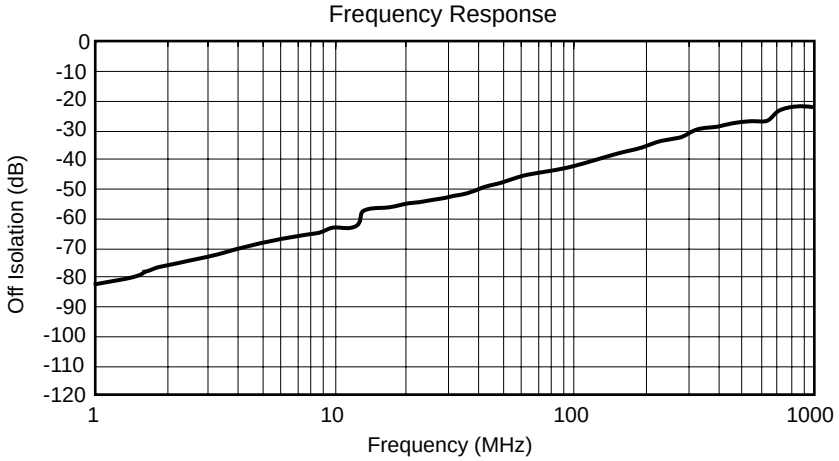

Figure 2. Off Isolation

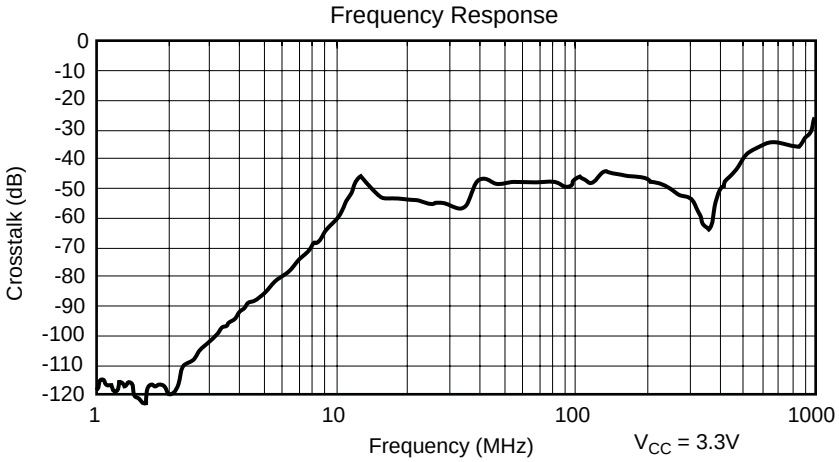

Figure 3. Crosstalk

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Test Diagrams

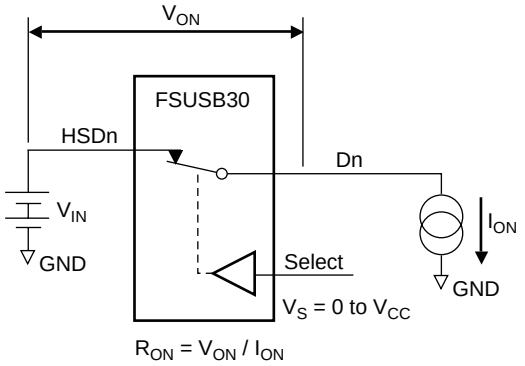
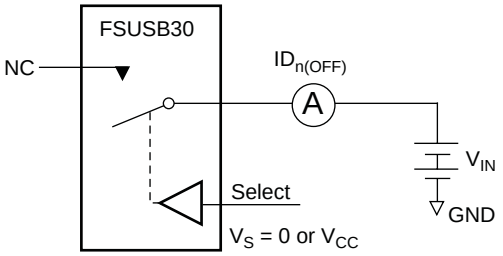
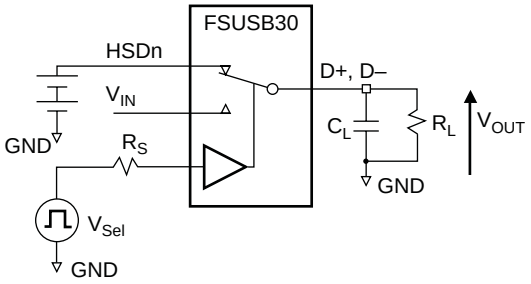


Figure 4. On Resistance



Each switch port is tested separately.

Figure 5. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Electrical tables for specific values).

C_L includes test fixture and stray capacitance.

Figure 6. AC Test Circuit Load

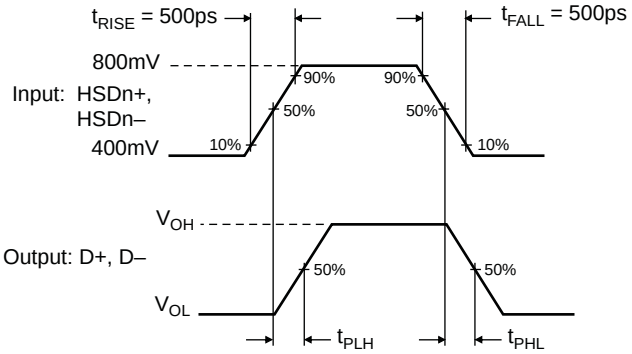


Figure 7. Switch Propagation Delay Waveforms

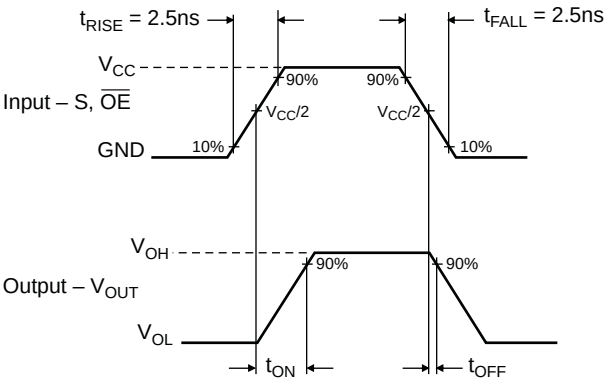


Figure 8. Turn-On / Turn-Off Waveform

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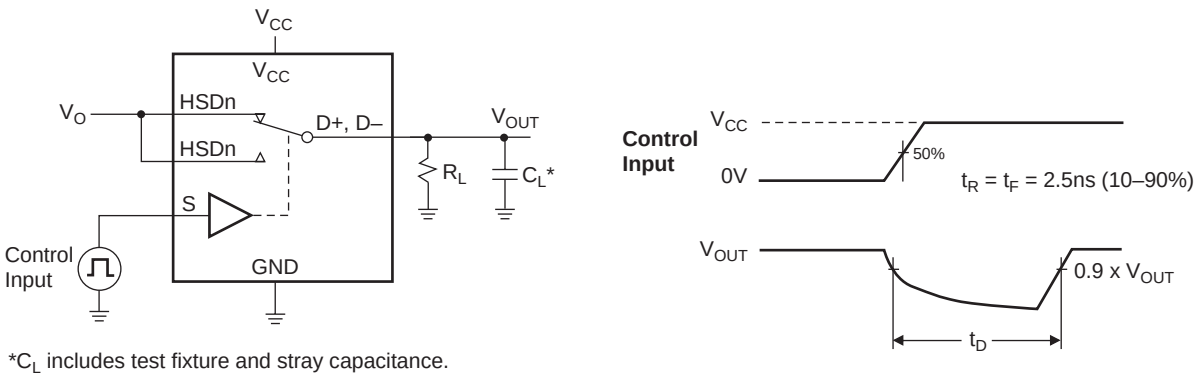

Figure 9. Break-Before-Make (t_{BBM})

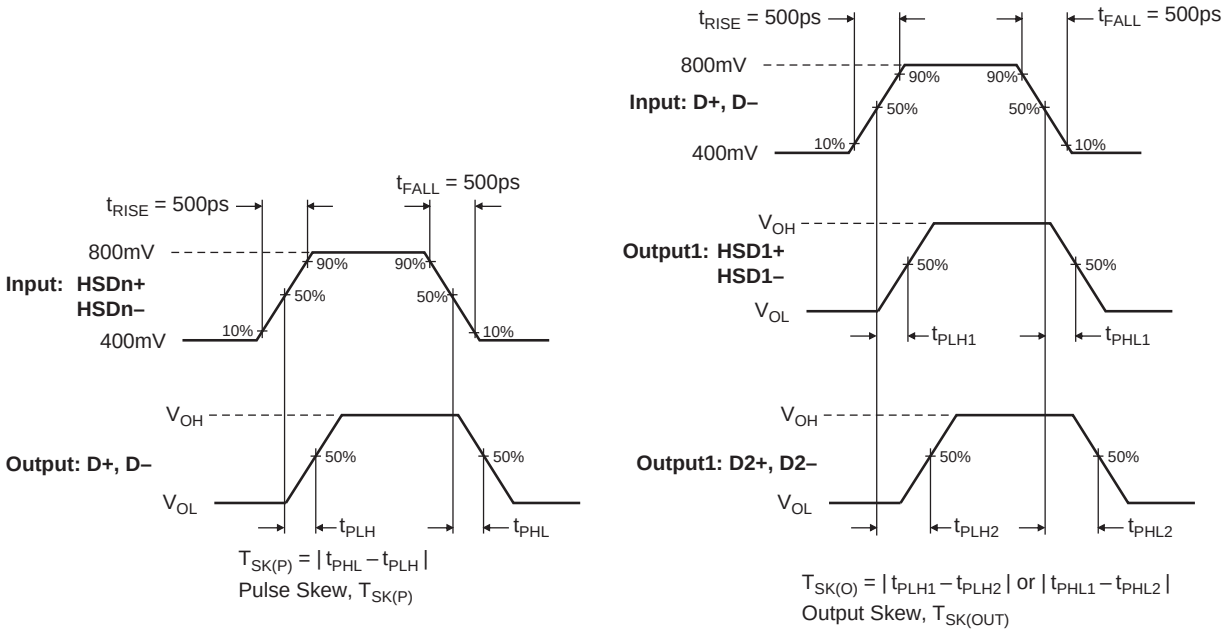

Figure 10. Switch Skew Tests

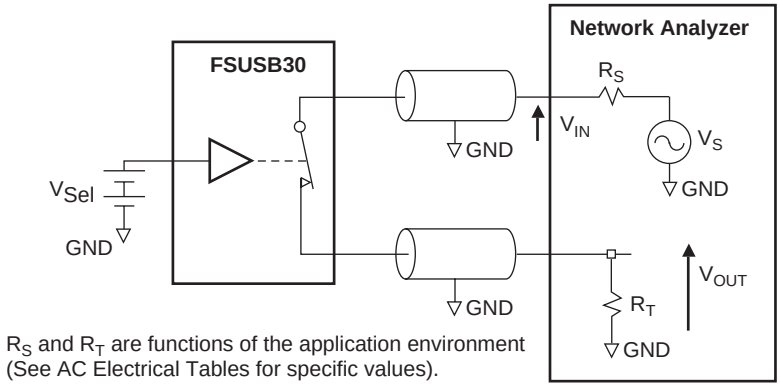

Figure 11. Bandwidth

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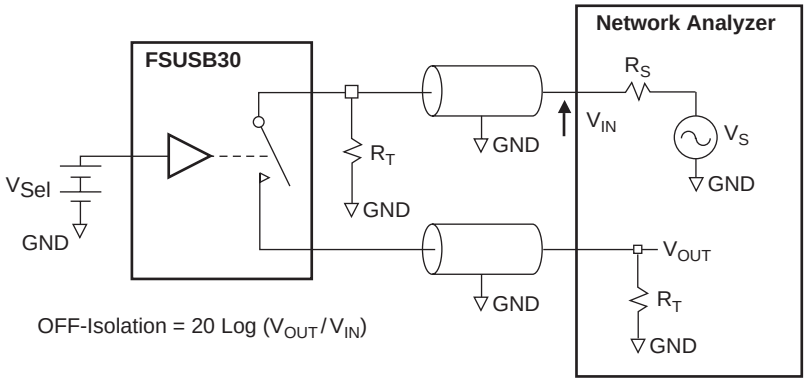

Figure 12. Channel Off Isolation

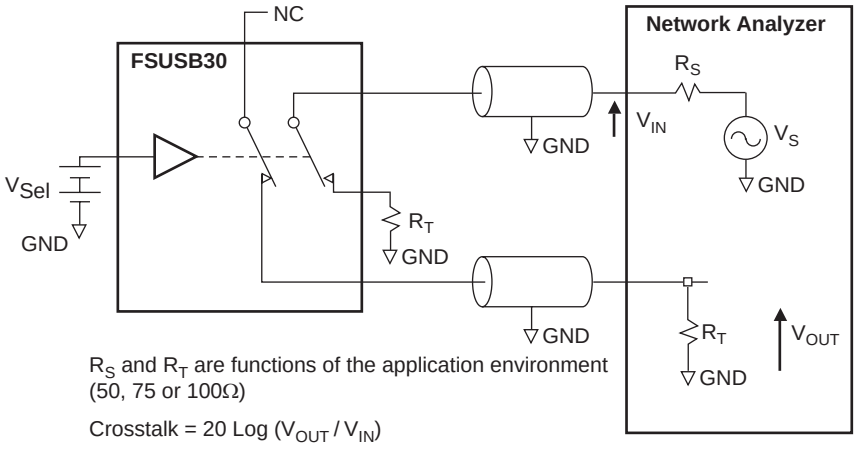

Figure 13. Non-Adjacent Channel-to-Channel Crosstalk

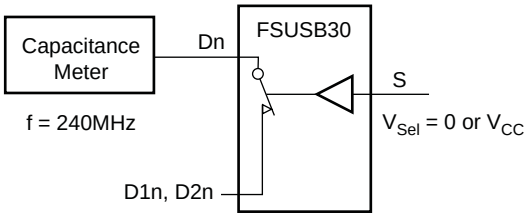

Figure 14. Channel On Capacitance

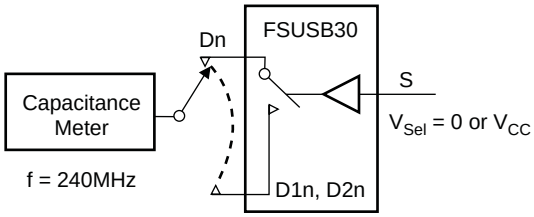

Figure 15. Channel Off Capacitance

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Application Guidance: Meeting USB 2.0 Vbus Short Requirements

In section 7.1.1 of the USB 2.0 specification, it notes that USB devices must be able to withstand a Vbus short to D+ or D- when the USB devices is either powered off or powered on. The FSUSB30 can be successfully configured to meet both these requirements.

Power-Off Protection

For a Vbus short circuit, the switch is expected to withstand such a condition for at least 24 hours. The FSUSB30 has specially designed circuitry which prevents unintended signal bleed through as well as guaranteed system reliability during a power-down, over-voltage condition. The protection has been added to the common pins (D+, D-).

Power-On Protection

The USB 2.0 specification also notes that the USB device should be capable of withstanding a Vbus short during transmission of data. Fairchild recommends adding a 100Ω series resister between the switch VCC pin and supply rail to protect against this case. This modification works by limiting current flow back into the V_{CC} rail during the over-voltage event so current remains within the safe operating range. In this application, the switch passes the full 5.25V input signal through to the selected output, while maintaining specified off isolation on the un-selected pins.

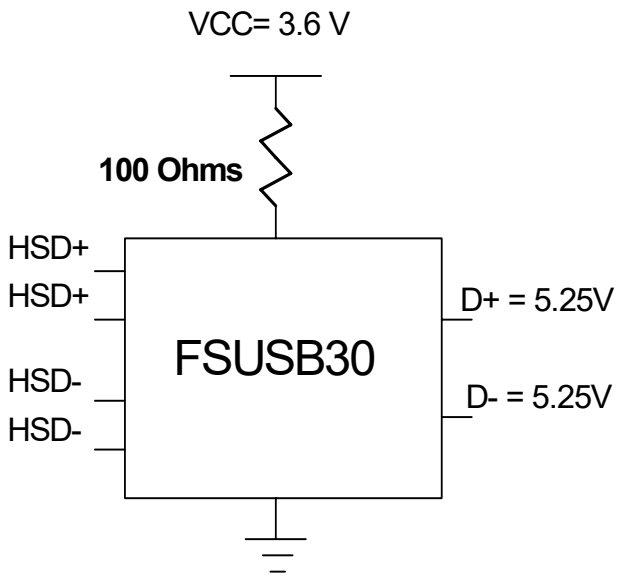

Figure 16. Adding 100Ω resistor in series with the V_{CC} supply allows the FSUSB30 to withstand a Vbus short when powered up

For more information, see Applications Note *AN-6022 Using the FSUSB30 to Comply with USB 2.0 Fault Condition Requirements* at www.fairchildsemi.com

Microchip Ex. 1065, p. 53
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IPR2024-00494

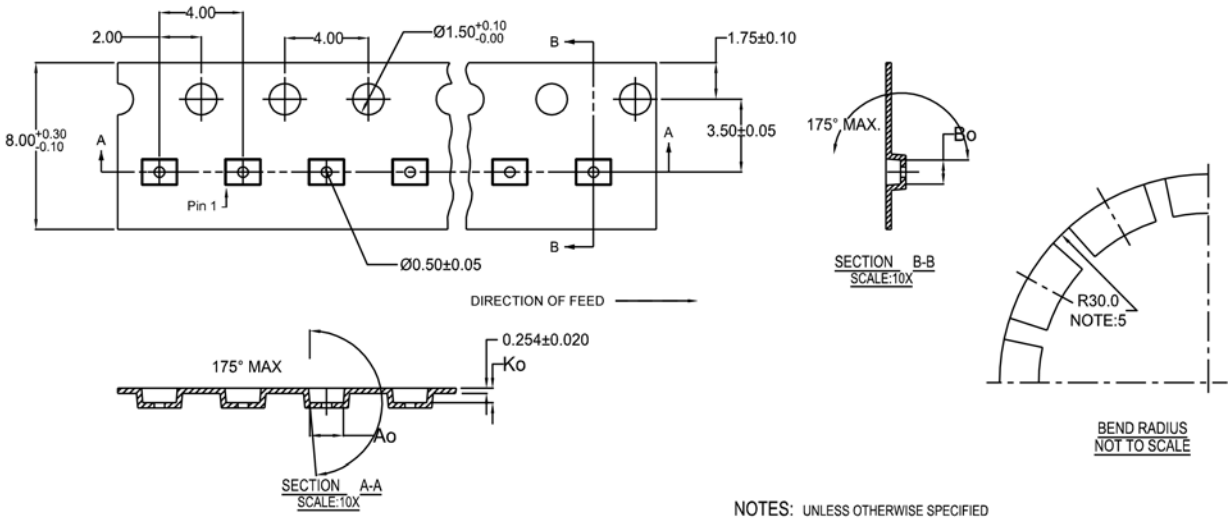
Tape and Reel Specifications

Tape Format for MircoPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L10X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimension

Dimensions are in millimeters unless otherwise specified.



10	300056	2.30± 0.05	1.78±0.05	0.68 ± 0.05
8	300038	1.78± 0.05	1.78±0.05	0.68 ± 0.05
6	300033	1.60± 0.05	1.15±0.05	0.70 ± 0.05

NOTES: UNLESS OTHERWISE SPECIFIED

1. ACCUMULATED 50 SPROCKETS, SPROCKET HOLE PITCH IS 200.00 ±0.30MM
2. NO INDICATED CORNER RADIUS IS 0.127MM
3. CAMBER NOT TO EXCEED 1MM IN 100MM
4. SMALLEST ALLOWABLE BENDING RADIUS
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

SCALE: 6X

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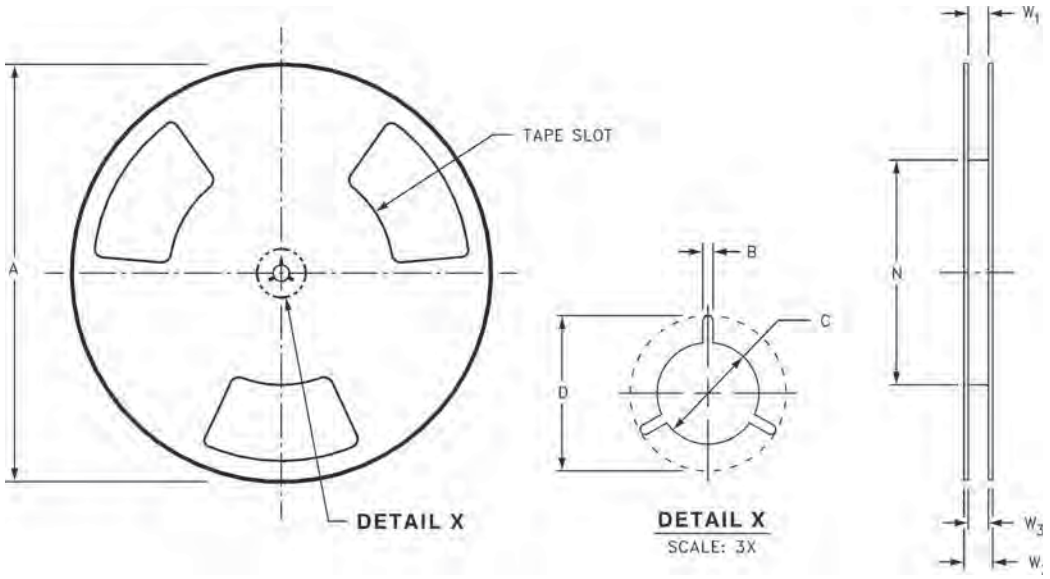
Reel Dimension for MircoPak

Dimensions are in inches (millimeters) unless otherwise specified.



Tape Size	A	B	C	D	N	W1	W2	W3
(8mm)	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

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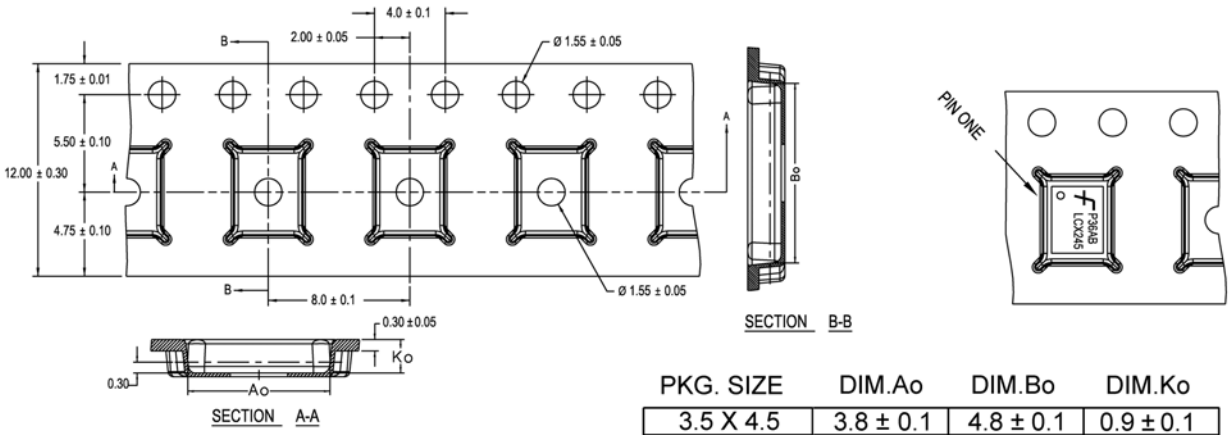
Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions

Dimenions are in millimeters unless otherwise specified.



PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

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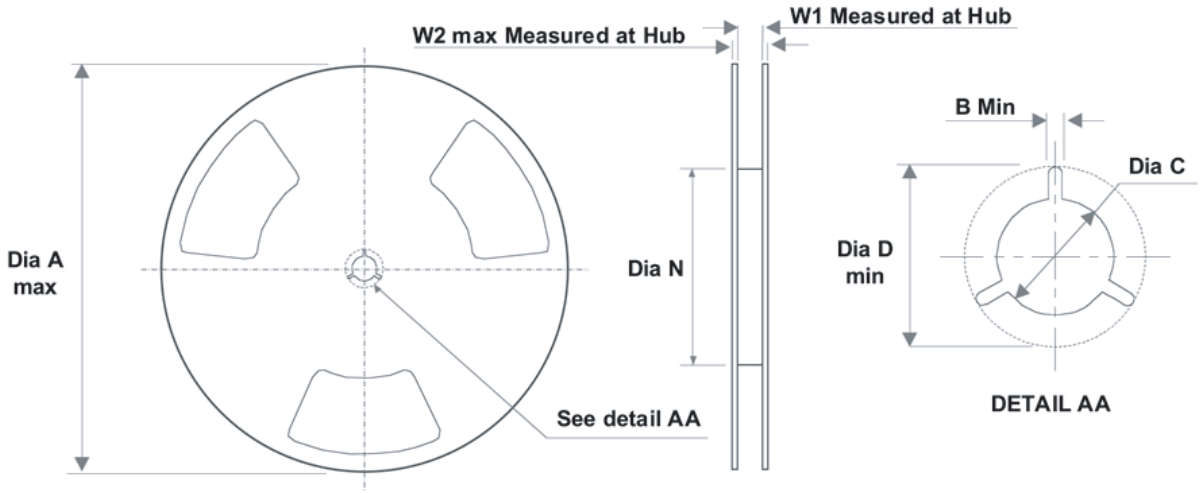
IPR2024-00494

Reel Dimensions for DQFN

Dimensions are in inches (millimeters) unless otherwise specified.



Tape Size	A	B	C	D	N	W1	W2
(12mm)	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

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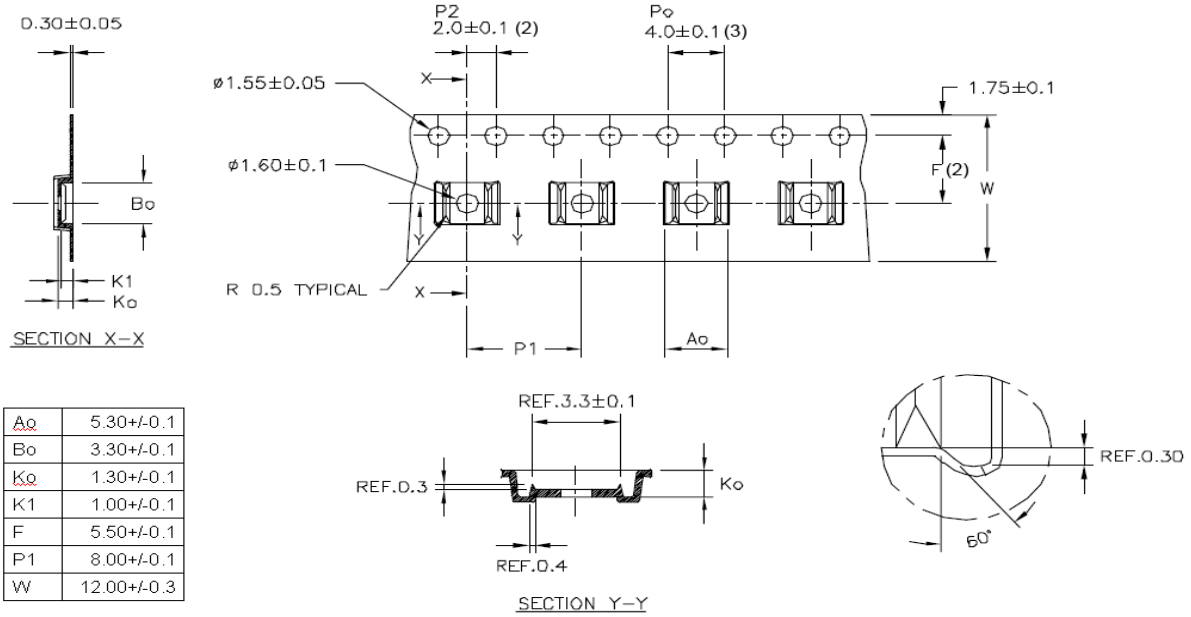
Tape Dimensions for MSOP

Dimensions are in inches (millimeters) unless otherwise specified.



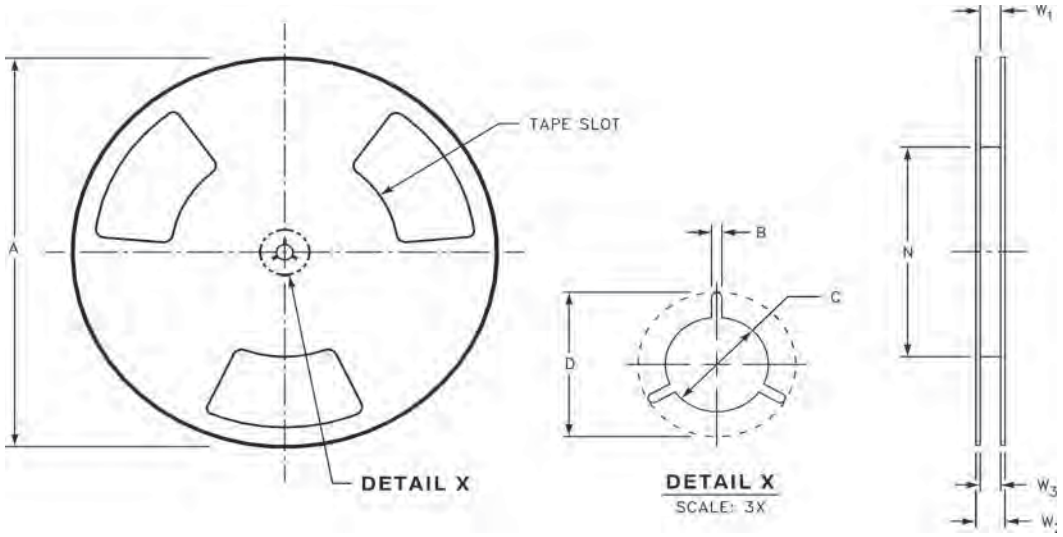
Ao	5.30+/-0.1
Bo	3.30+/-0.1
Ko	1.30+/-0.1
K1	1.00+/-0.1
F	5.50+/-0.1
P1	8.00+/-0.1
W	12.00+/-0.3

Notes:

1. All dimensions are in millimeters.
2. Measured from centerline of sprocket hole to centerline of pocket.
3. Cumulative tolerance of ten sprocket holes is ±0.20mm.
4. Other material available.

Reel Dimensions for MSOP

Dimensions are in inches (millimeters) unless otherwise specified



Tape Size	A	B	C	D	N	W1	W2	W3
(12mm)	13 (330)	0.059 (1.5)	0.512 (13)	0.795 (20.2)	7.008 (178)	0.448 (12.4)	0.724 (18.4)	0.468-0.606 (11.9 -15.4)

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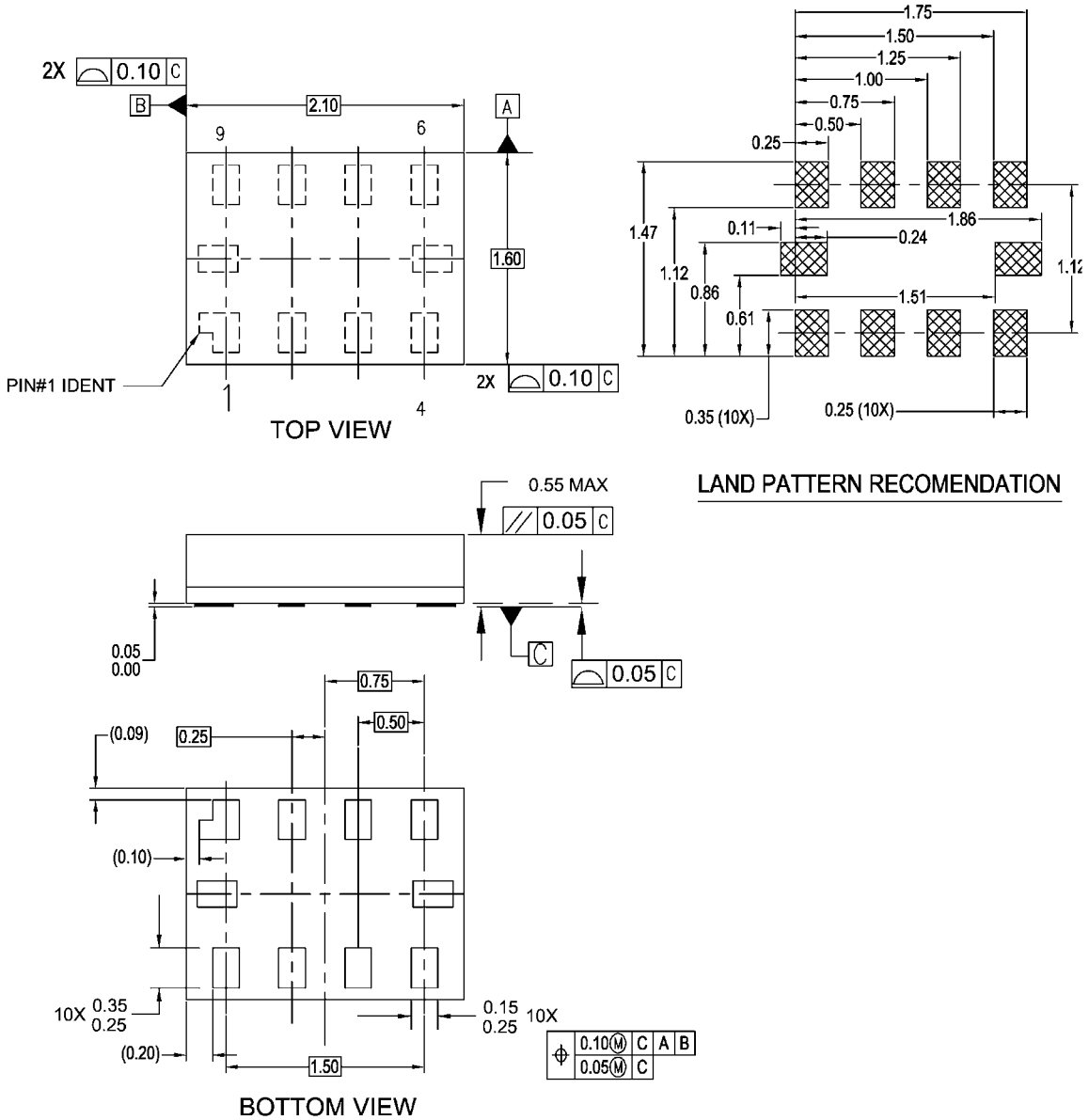
Physical Dimensions

Dimensions are in millimeters unless otherwise specified.



NOTES:

A. PACKAGE CONFORMS TO JEDEC MO255, VARIATION UABD

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES CONFORMS TO ASME Y14.5M, 1994.

MAC010ARevC

Figure 17. 10-Lead MicroPak, 1.6 x 2.1mm

Microchip Ex. 1065, p. 59
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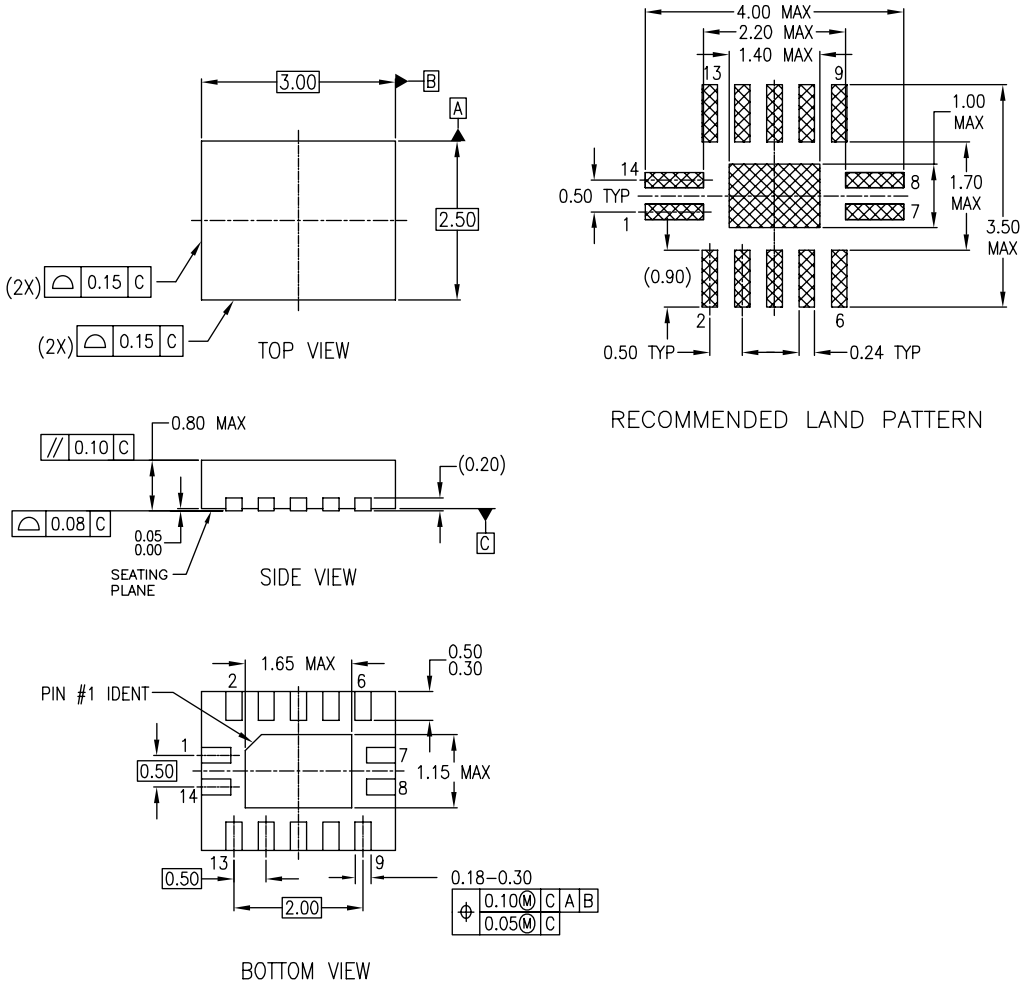
Physical Dimensions

Dimensions are in millimeters unless otherwise specified.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AA
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

Figure 18. 14-Terminal De-populated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm

Microchip Ex. 1065, p. 60
Microchip v. Aptiv
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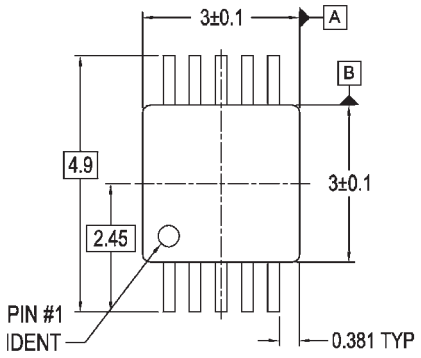
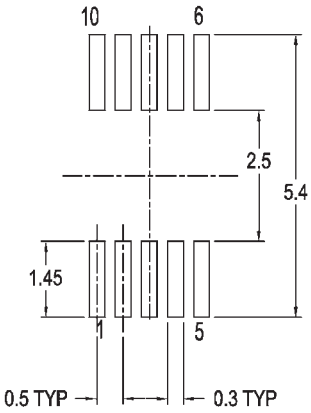
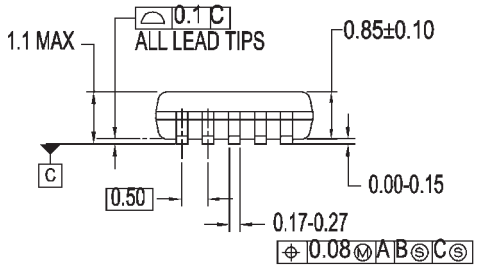
Physical Dimensions

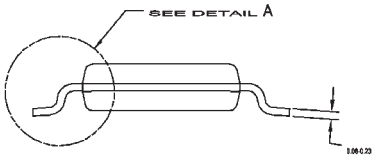
Dimensions are in millimeters unless otherwise specified.

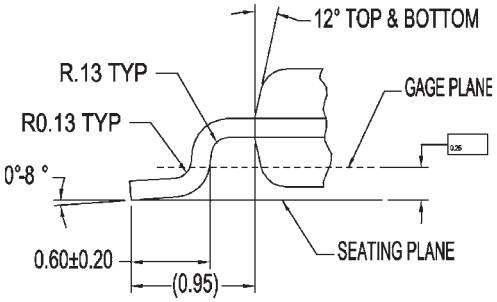




LAND PATTERN RECOMENDATION







DIMENSIONS ARE IN MILLIMETERS

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187, VARIATION BA, REF NOTE 6, DATE 11/00.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

MUA10AREVA

Figure 19. 10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

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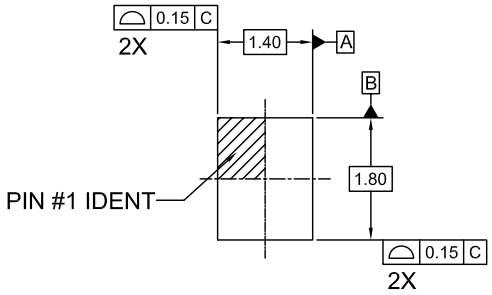
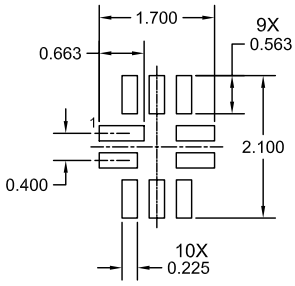
Physical Dimensions

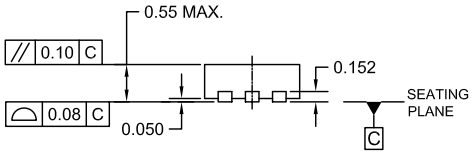
Dimensions are in millimeters unless otherwise specified.



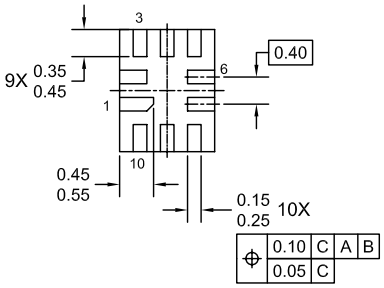
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DIMENSIONS ARE IN MILLIMETERS.

B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

UMLP10Arev1

Figure 20. 10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm

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E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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https://web.archive.org/web/20151221011631/http://www.cypress.com/file/175706/download

AN96527

Designing USB Type-C Products Using Cypress's CCG1 Controllers

Authors: John Hyde, Vihang Trivedi

Associated Project: No

Associated Part Family: CYPD11xx

Related Documents: For a complete list, see Related Documents

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN96527.

AN96527 explains technological advances introduced by the USB-IF Type-C Specification and the Power Delivery Specification and how they can be designed into practical products using Cypress CCG1 Controllers. Four application areas are explored: host design, cable design, peripheral design, and power adapter design. Working prototype reference designs are presented for each application area, along with design and debug tools.

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1 Introduction

In August 2014, the USB Implementers' Forum (USB-IF) introduced two separate but complementary specifications. The USB Power Delivery (PD) Specification Revision 2.0, Version 1.1 details how a USB link can be transformed from a 4.5-W power source (900 mA at 5 V) to a 100-W power source or consumer (up to 5 A at 20 V). The USB Type-C Cable and Connector Specification Revision 1.1 details a reversible, slim connector system with high-speed USB 2.0 signals and two SuperSpeed lanes at up to 10 Gbps that can be repurposed to support Alternate Modes. Power Delivery can be implemented independent of Type-C, and Type-C implementations need not include Power Delivery.

This application note explains a range of USB solutions that can be implemented with both Power Delivery and Type-C within the context of several reference designs: host, cable, client, power adapter, and docking station.

This application note first looks at Power Delivery (PD) and how it is architected and implemented. All USB products, at all speeds, can take advantage of Power Delivery as a power provider, power consumer, or sometimes both, including dynamically changing roles. Up to 100 W can be distributed on a Type-C cable, meaning that even a tablet or notebook can be bus-powered.

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Most Type-C cables will implement all of the Type-C and Power Delivery features and will therefore need to be electronically marked, making a cable an "electronically marked cable assembly" (EMCA). This document covers an EMCA design implemented as a PCB that uses two Cypress CCG1 devices, one at each end of the cable. It also describes a practical EMCA design that can be built inside a Type-C plug.

The application note then looks at Alternate Modes, which allow the USB differential pairs defined by the Type-C Specification to be repurposed for other serial protocols such as DisplayPort, PCIe, Mobile High-Definition Link, and eSATA. This reduces the diversity of connectors on a USB product, because USB Type-C connectors can replace all previous USB connectors, power connector, and connectors for other uses.

Finally, this application note examines a docking station design that performs power aggregation and sharing among multiple Type-C (and a few Type-A) ports.

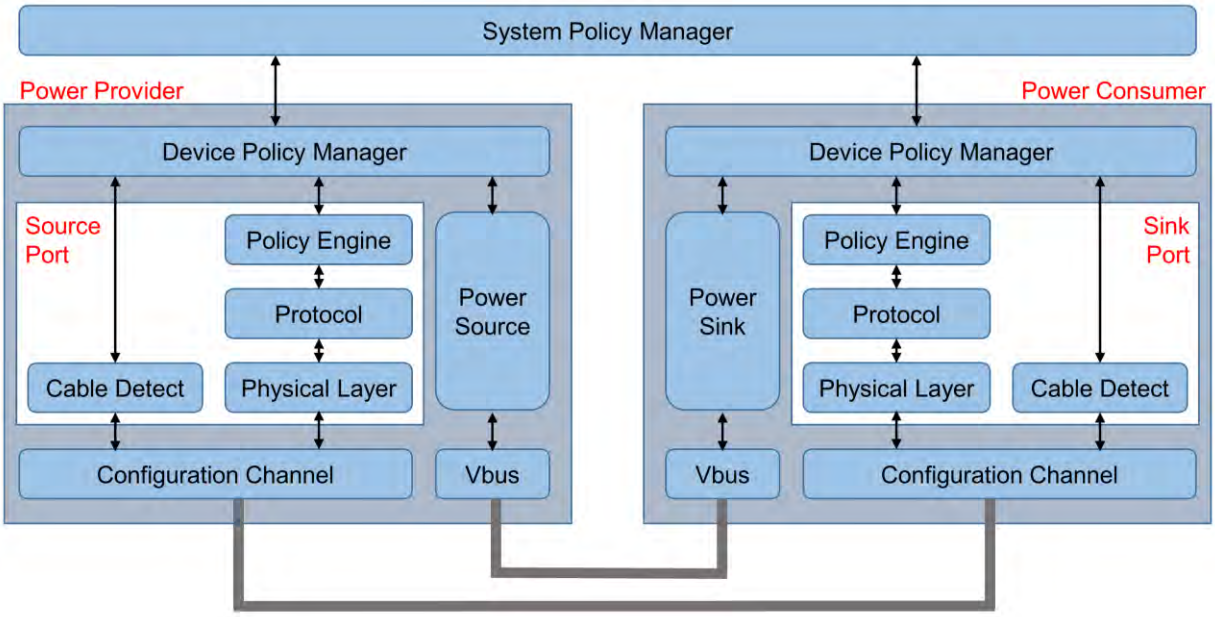
Note: This application note references the Cypress CCG1 (Type-**C** **C**ontroller **G**eneration **1**), a Cypress USB Type-C port controller compliant with the latest USB Type-C and PD standards. This device provides a programmable hardware and firmware solution with field upgradability to adapt to changes in Type-C spec. CCG1 devices integrate Type-C Transceivers. For power delivery applications, it integrates the Over Current Protection (OCP) and Over Voltage Protection (OVP) features. It provides a complete solution to add USB Type-C and PD support to power adapters, cables, notebooks, tablets, and monitors.

This application note also references the Cypress CY4501 CCG1 Development Kit and is intended as supplemental information to the CY4501 CCG1 Development Kit Guide. We recommend that you have the kit and this guide available to implement the example designs. Readers without the kit, however, will still learn a great deal from the USB Type-C theory sections and example designs.

2 Implementing Type-C and Power Delivery Systems

Before discussing specific applications, it is beneficial to review some essential theory. Figure 1 shows the USB Power Delivery architecture for a Type-C system. Derived from the PD Specification, Figure 1 shows only the biphase mark code (BMC) operation with the Type-C connector (this is described in the Configuration Channel: Message Passing section). Note that the PD spec includes support for the previous generation solution using the binary frequency shift keying (BFSK) method over Vbus on legacy (Type-A/B) connectors but this is not considered in this application note.

Figure 1. Type-C Power Delivery Architecture



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Before the PD Specification, the host computer (a laptop, for example) was always the power provider and the peripheral device was always a power consumer. Charging the battery of the host computer was considered a separate action. The PD Specification greatly improves the USB ecosystem and defines power roles that are independent of "host" and "peripheral" and includes ability for swapping power roles. An example for such versatile behavior is that a powered peripheral such as a monitor can charge the battery of a host such as Notebook or PC. This will dramatically reduce the number of cables used in new USB systems.

The PD Specification defines a power provider as the device that provides power onto Vbus and a power consumer as a device that consumes power from Vbus. Here 'device' is 'host' or 'peripheral' and they take on the role of being a power provider or a power consumer. This role may be swapped under program control. Note that these new power roles are independent of the USB data transfers between a host and a peripheral.

The PD Specification defines a System Policy Manager that would be implemented on the USB Host running as an operating system task. This topic is beyond the scope of this application note; the reference designs discussed in this document operate with no involvement of the host operating system. For more details and insight to System Policy, please refer to the PD Specification.

When a USB Host and USB device are interconnected, they form a USB link pair, and each link partner has a configuration channel (CC) controller. Messages are then logically exchanged among Device Policy Managers within each controller. These messages are physically transferred over the CC and a power delivery (PD) contract is set up between the link pair, and then power is delivered over Vbus.

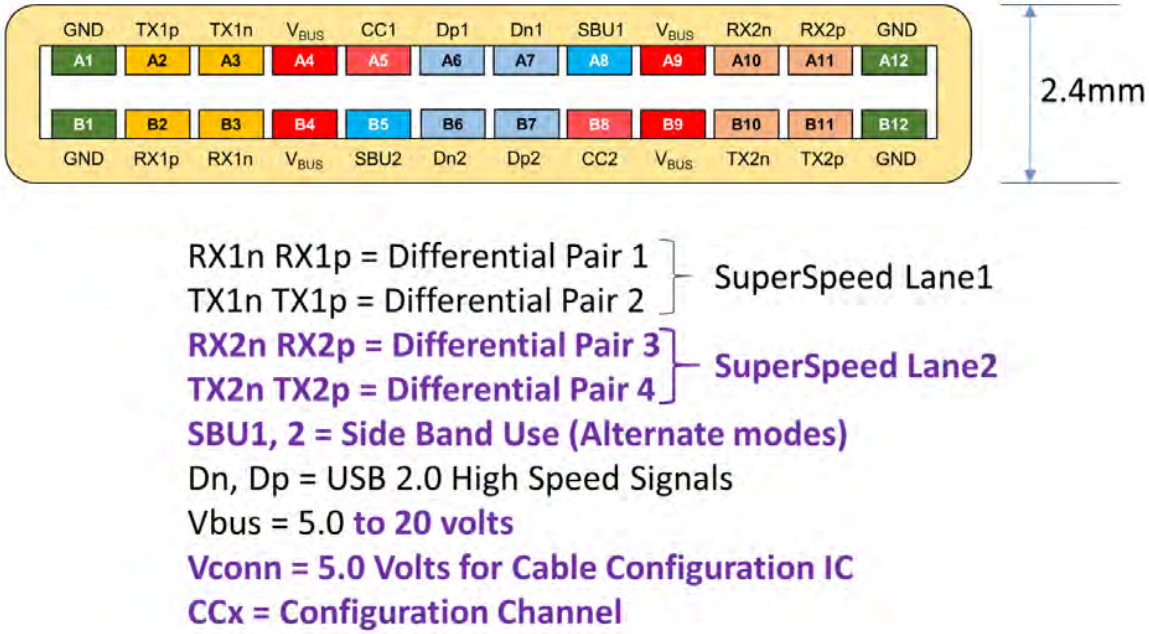
A CCG1 is used to implement the Power Delivery architecture within all of the presented reference designs. The policy protocol layer is implemented in firmware, and the reference designs include solutions for the USB Host (PC, Laptop, Notebook, Smartphone), EMCA (Cable), power adapter, and USB peripheral (Monitor, Hard Disk). The CCG1 device also implements the cable detect mechanism and the messaging physical layer.

The configuration channel is a new signal pair within the Type-C signal definition, so this is described next.

2.1 Type-C Signal Definition

Figure 2 shows the connections of a Type-C receptacle. For reference, the new Type-C signals are shown in bold text below the figure and signal names found in a USB Type-A receptacle are shown in normal text. The Type-C receptacle has two rows of 12 connections arranged symmetrically, both horizontally and vertically to facilitate plugging in a cable right-side up and right-side down. The USB IF did a great deal of simulation and modeling to derive this arrangement of distributed signals and grounds to enable a reliable signal transfer rate of 10 Gbps and beyond.

Figure 2. Type-C Signal Definition of a Receptacle



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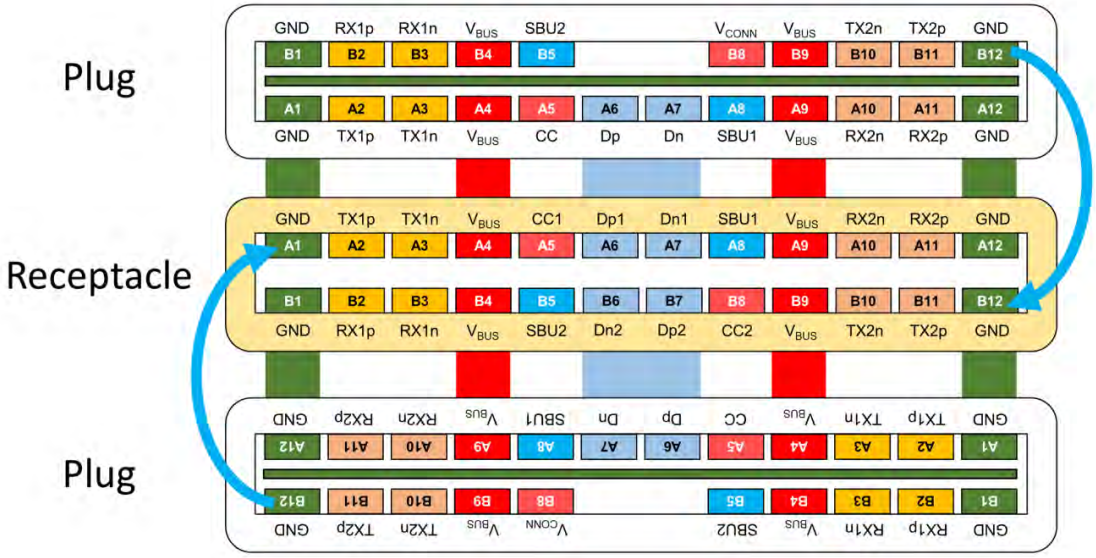
As shown in Figure 2, there are four ground signals and four Vbus signals. Their relative position remains the same when a plug is connected in any orientation.

There are two USB SuperSpeed lanes (four pairs of signals). One or both of these lanes can be repurposed for use in an Alternate Mode to transport other data for other serial protocol buses such as DisplayPort. Alternate Modes are described in the Type-C Alternate Modes section. When an Alternate Mode is active, two additional signals – SideBandUse (SBU1/2) – may also be utilized to carry the control signals.

A USB 2.0 pair of signals, Dp and Dn, is always present, which means that USB data transfers up to high speed (480Mb/s) will always be available even if both USB SuperSpeed lanes have been reassigned for Alternate modes. Two sets of USB 2.0 signals are defined (one in the top row and one in the bottom row) on a Type-C receptacle. It is expected that they are connected together in the PCB that hosts the receptacle. Dp1 should be shorted to Dp2 and Dn1 should be shorted to Dn2. This ensures that the USB 2.0 connection will be in place when a plug is connected in any orientation.

The configuration channel is defined using two signals, Vconn and CC on a plug and CC1 and CC2 on a receptacle, as shown in Figure 3.

Figure 3. Type-C Plug, Receptacle, and Flipped Plug



Because the plug can be inserted right-side up or right-side down, Vconn on the plug will be connected to either CC1 or CC2 on the receptacle, and CC on the plug will be connected to either CC2 or CC1 on the receptacle. The first task then is to determine the orientation of the cable.

This application note only discusses the power delivery aspect of the reference designs; it does not discuss anything about the USB data delivery over the Type-C cable. This is an important point to note because the configuration channel is implemented as a totally separate subsystem to the USB data delivery channels; it does not rely on any USB signaling.

The Type-C Specification introduces a variety of new terms and acronyms (see Appendix A: USB and Type-C Acronyms). These will be explained as they are introduced in this application note.

Figure 4 shows the power delivery signals of a downstream facing port (DFP), which would be a host or a hub and is typically a power provider, and a directly connected (no intervening cable) upstream facing port (UFP), which would be a peripheral device such as thumb drive and is typically a power consumer. Only power signals are shown. USB signals will be added later in the application note, and, as explained previously, their operation is independent of the power signals.

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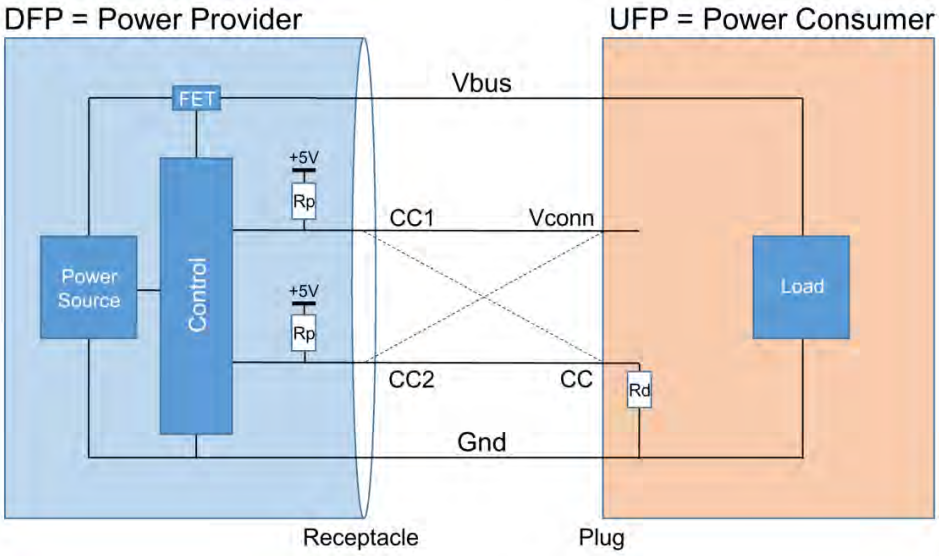
Figure 4. Direct Connection of a Power Provider and Power Consumer



2.2 Configuration Channel: Cable Detect

A typical cable connection detection goes through the following sequence:

- By Default, DFP (power provider) sets Vbus to 0 V.
- DFP (power provider) has two pull-up resistors (Rp) connected to CC1 and CC2.
- UFP (power consumer) is connected to Vbus, waiting for power.
- UFP (power consumer) has Vconn open.
- UFP (power consumer) has a pull-down resistor Rd connected to CC.
- On connection, Rd pulls CC1 or CC2 LOW depending on the orientation.
- DFP (power provider) determines whether CC1 or CC2 was pulled LOW and therefore knows the orientation of the cable.
- DFP (power provider) provides 5 V on Vbus.
- UFP (power consumer), on seeing 5 V on Vbus, responds to the enumeration of its USB data channel, if it has one. Most peripherals will have a USB data channel but the PD Specification permits a power adapter to be designed without a USB data channel.

The value of Rp determines the initial power limit of the DFP, as shown in Table 1. A higher current may be negotiated using USB-PD later as described in Power Provider Design. The CC voltage shown is a typical value because Rp and Rd are specified with ±20 percent tolerance components (additionally, the table assumes that Rp is connected to +5 V; the PD Specification actually defines this connection in terms of current flow through Rd and describes other implementation methods).

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Table 1. Rp Determines Initial Vbus Current Limit

Rp	Rd	CC Voltage	VBUS Current Limit
56 KΩ	5.1 KΩ	0.42V	Default USB Current
22 KΩ	5.1 KΩ	0.94V	1.5 A @ 5V
10 KΩ	5.1 KΩ	1.67V	3.0 A @ 5V

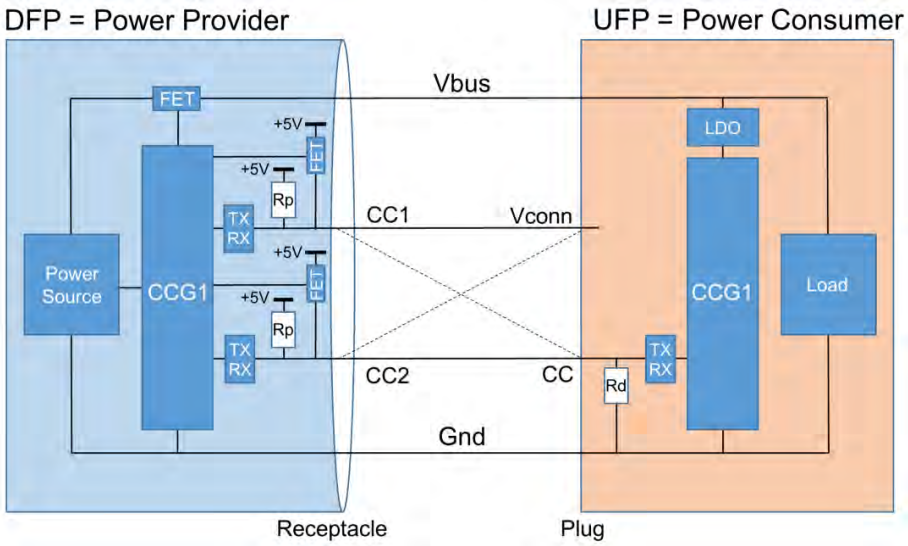
Other resistor values are also valid; refer to Appendix B: Accessories for a description of the accessories.

2.3 Configuration Channel: Messaging Physical Layer

If the UFP peripheral needs only up to 15 W of power (3 A at 5 V), then a PD controller is not needed. If the power provider has an Rp value of 10 kΩ as shown in Table 1, it can source up to 3 A of current. Note that this is twice as much as that provided by the Battery Charging Specification 1.2.

Most new applications will want more power, however. Figure 5 shows the same power source and power consumer of Figure 4 with a configuration channel controller (a CCG1 device) implemented within each link partner so that advanced features such as power delivery can be negotiated.

Figure 5. Type-C Configuration Channel implementation with CCG1



When connected, either CC1 or CC2 will be connected to the plug's CC line (UFP side). The CCG1 (DFP side) will disconnect Rp from the CCx pin, which is not connected to the CC line (UFP side) and instead connects a +5 V Vconn supply to it. This Vconn supply is not used by the example implementation shown in Figure 5. Refer to the Adding a Type-C Cable section to understand how Vconn supply is used.

In the implementation shown in Figure 5, UFP and DFP are directly connected (without a cable). UFP uses a plug, where Vconn and CC are fixed. Another example of a directly connected device is a mouse with a captive cable. It will also have Vconn and CC in a fixed position. Figure 5 highlights TX+RX transceivers that are used to implement the configuration channel; these are actually embedded within the CCG1.

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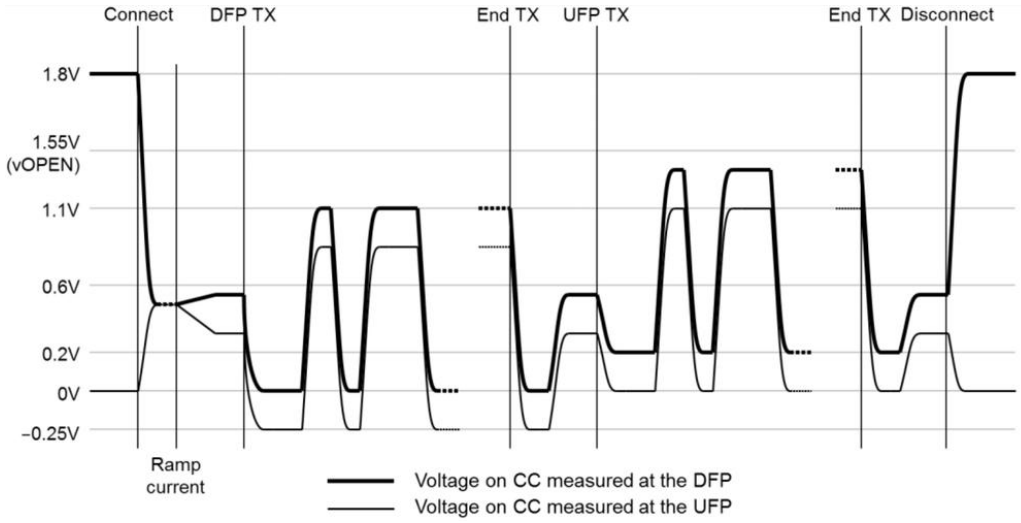
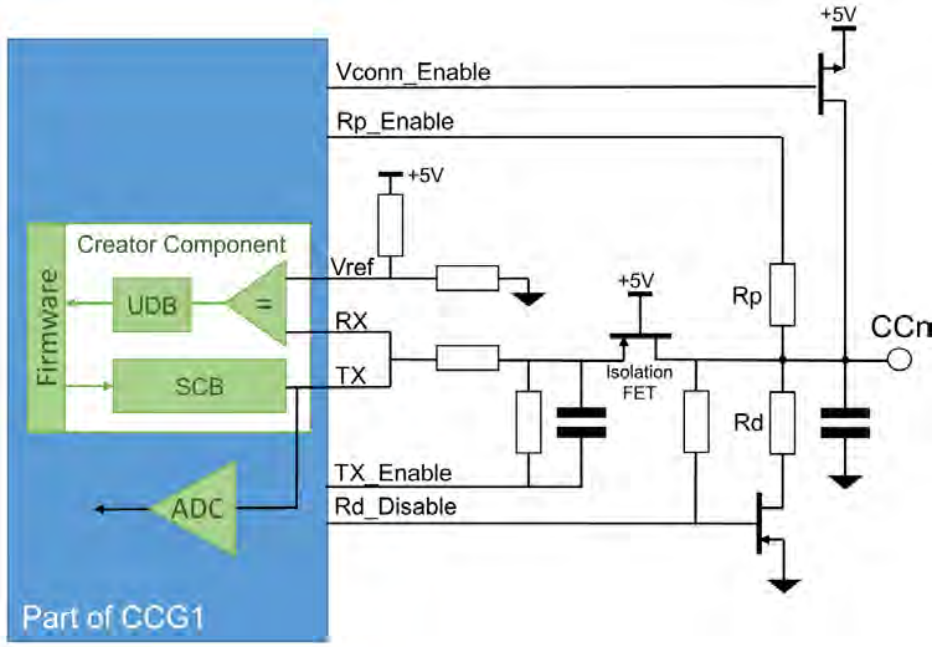
The configuration channel uses half-duplex biphase mark coding (BMC) to transmit and receive messages. BMC is often called "Differential Manchester encoding" and is an extension of Manchester encoding, wherein the output signal toggles on both rising clock edge and falling clock edge if the data bit is HIGH. If the data bit is LOW, the output transitions only every rising edge. Because there are transitions for both LOW and HIGH data bits, BMC is effectively DC-balanced, making it suitable for superimposing on the DC level set by Rp and Rd on the CC line as shown in Figure 6. More details can be found in the Type-C specification from the USB-IF website.

Figure 6. CC Messages (BMC Superimposed on the DC Level of the CC Wire)



CCG1 is based on PSoC® 4, and uses UDB, SCB, and analog blocks and firmware to implement the BMC encoding and decoding scheme. As shown in Figure 7, external resistors Rp and Rd are used to set the correct biasing values (connection detection). If you are not familiar with the PSoC 4 architecture and related terms, refer to the PSoC home page for a wealth of technical documentation, videos, and other training materials.

Figure 7. Detail of One of the Two Configuration Channel Physical Layers on a DRP



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2.4 Dual-Role and Dead-Battery Provision

Many USB products (a laptop, for example) operate as a power provider and a power consumer at different times. The Type-C Specification calls this operation a dual-role port (DRP). (Note that this term has no relationship to the USB OTG ability to swap data host and data peripheral roles).

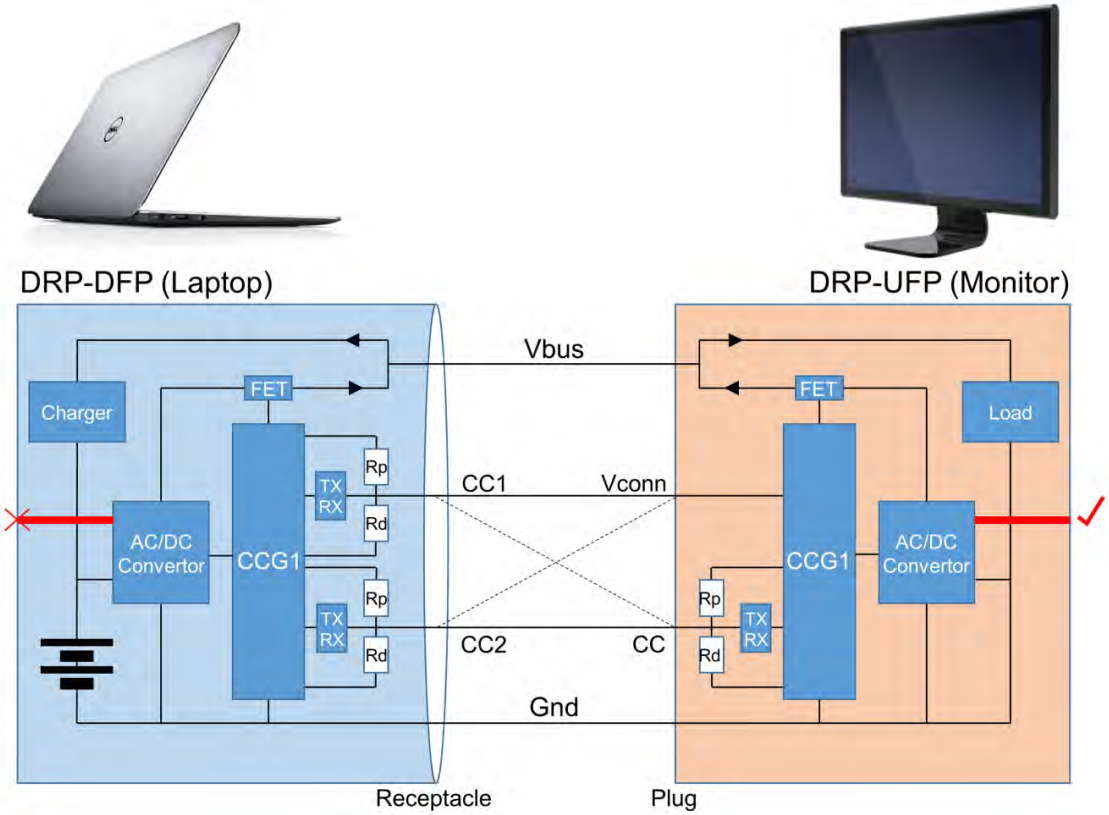
A laptop with DRP capabilities will be a power provider when running from its internal battery and a power consumer when being charged from the Type-C connector. DRP devices have the ability to connect and disconnect either Rp, Rd, or both to and from the CC lines. Upon detecting a Type-C connection, DRP devices will toggle their state between trying to be a DFP (by connecting Rp and disconnecting Rd) and trying to be an UFP (by disconnecting Rp and connecting Rd). When a DRP device (like a laptop) is connected to an UFP device like a mouse, after toggling to the DFP state, the laptop will detect a UFP attached and will settle its power state as a DFP. Then the laptop will provide power to the mouse.

On the other hand, when a DRP device (like a laptop) is connected to a DFP device like a power adapter, after toggling to the UFP state, the laptop will detect a DFP attached and will settle its power state as a UFP. Then the power adapter will provide power to the laptop.

A DFP will have Rp connected to a local +5 V supply, and a UFP will have Rd connected to ground. Consider what happens in Figure 7 if the DRP does not inject power into the system; that is, its local +5-V supply is, in fact, floating. An example is a laptop with a dead battery. A requirement for a power provider is that it should be a DRP and present Rd to ground on both CC lines when it is not providing power. This will make the DRP look like a UFP.

Figure 8 extends Figure 7, with both sides augmented to be DRPs. In this example, consider that a laptop is connected to a powered monitor. The laptop battery is dead, so Rp is floating and Rd is present.

Figure 8. Two Interconnecting DRPs Example – Laptop and Powered Monitor



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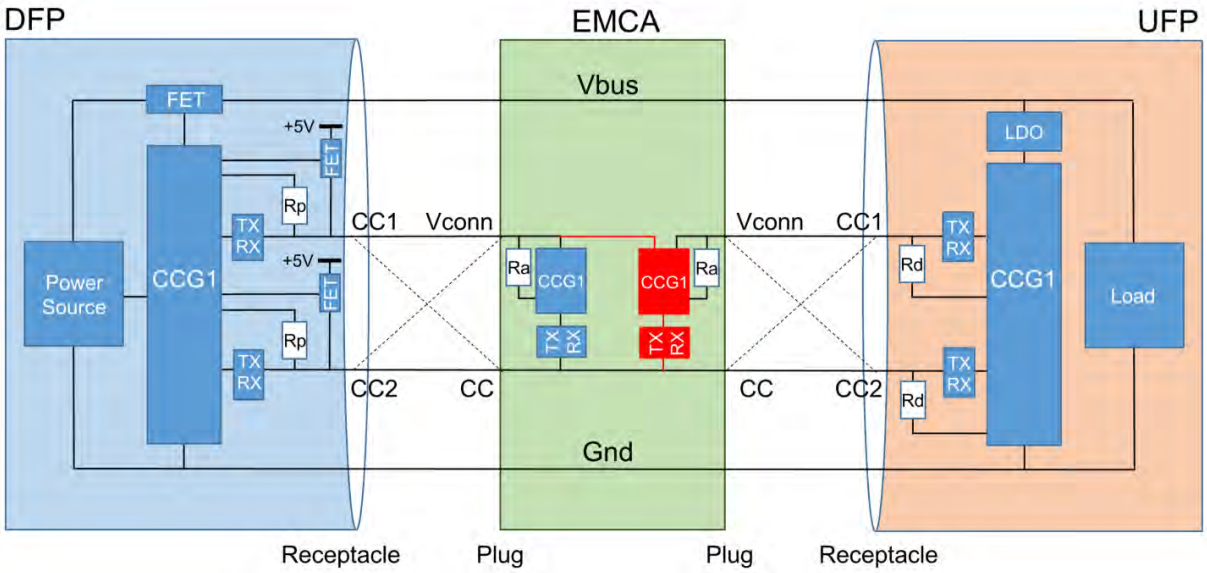
The DRP-UFP (powered monitor in this example) will initially present Rd on its CC line, and the DRP-DFP will not be recognized because the laptop battery is dead and the CC line is not pulled up. The DRP-UFP periodically swaps roles to detect a connection. The DRP-UFP's CCG1 will disconnect Rd and then connect Rp; this CCG1 will then detect the voltage on the CC line and apply 5 V to Vbus with the current rating as defined in Table 1. With the DRP-DFP CCG1 in the laptop now powered, the two CCG1 devices will negotiate a higher Vbus so that the laptop battery can be charged more quickly, as described in Power Provider Design.

2.5 Adding a Type-C Cable

The example in Figure 5 used a directly connected UFP, making the explanation of the configuration channel simpler. Figure 9 shows the more common implementation of interconnecting a DFP and a UFP using an EMCA.

Two types of cables are defined in the USB specifications: a full-featured cable that supports all the Type-C signals shown in Figure 2, and a USB 2.0 cable that does not implement the SuperSpeed or sideband signals. The USB 2.0 Type-C cable, which has fewer wires, would be cheaper and more flexible.

Figure 9. Connecting a DFP and UPF With an EMCA



There are two plugs in the EMCA solution shown in Figure 9, which provide four possible ways of interconnecting the DFP and the UFP. This implementation is slightly more complex compared to the direct connection shown in Figure 5. Now the UFP also has to take care of the cable twist. The Vconn signal is terminated at one end of the cable electronics and is not connected to other end of the cable. This Vconn isolation allows the simple Rp and Rd cable detect mechanism on the CC line to continue to operate.

Vconn in the cable plug has a resistor, Ra, connected to ground. This enables the DFP to determine that it is connected to a cable rather than a directly connected device. Therefore, the DFP will supply +5 V on Vconn to power the cable electronics. It is recommended that the DFP disconnects Rp and the EMCA disconnects Ra once the PD negotiation is complete to conserve power. The EMCA reference design described in the CY4501 CCG1 Development Kit Guide allows three different implementations of an EMCA to be evaluated. Please refer to the Design Files on the CY4501 CCG1 Development Kit webpage.

An EMCA needs a configuration channel controller (a CCG1) mounted in the cable. The CCG1 device is available in three packages, as shown in Figure 10, one small enough to fit into the plug of an EMCA cable. Therefore, whether you are building hosts, clients, EMCAs, or power adapters, you can choose the one best suited to your design project.

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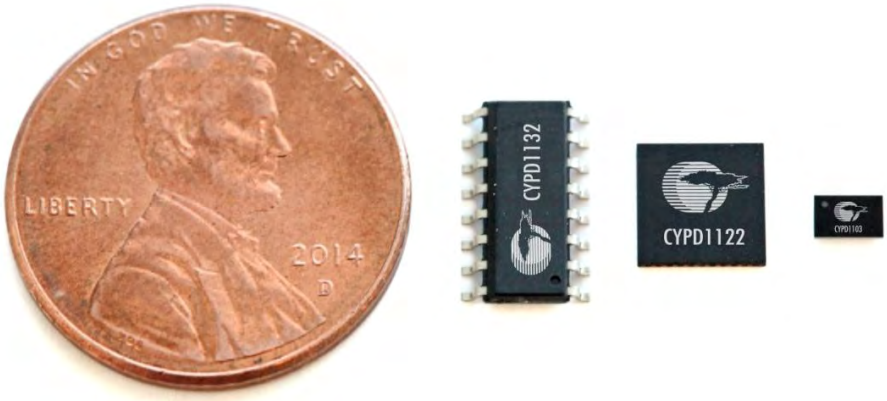
Figure 10. CCG1 Package Types



The Figure 11 shows the image of a CCG1 cable paddle card. The CCG1 device is powered by Vconn. Vconn is supplied from either or both the ends of the cable (and can be swapped), and the cable vendor has the option of using a single CCG1 or two CCG1 devices, one at each end of the cable. Figure 9 shows the second CCG1 device in red.

Figure 11. Type-C EMCA Plug with CCG1

2.6 Configuration Channel: Message Passing

Power Delivery parameters are exchanged between CCG1 devices by passing messages. Up to four CCG1 devices are connected to the CC wire, and the Type-C scheme to uniquely address a destination CCG1 device. The addressing scheme is shown in Figure 12.

Assuming that the DFP is the message source, then the CCG1 device closest to the DFP is called SOP' (SOP prime). The CCG1 device at the other end of the cable, if it exists, is called SOP'' (SOP double prime), and the CCG1 device in the port partner UFP is called SOP. The Type-C Specification also uses SOP* to refer to SOP, SOP' or SOP''. When the UFP is the message source, then the CCG1 device in the cable closest to it is SOP', and the far-end CCG1 device is SOP''. The CCG1 device in the link partner is always SOP.

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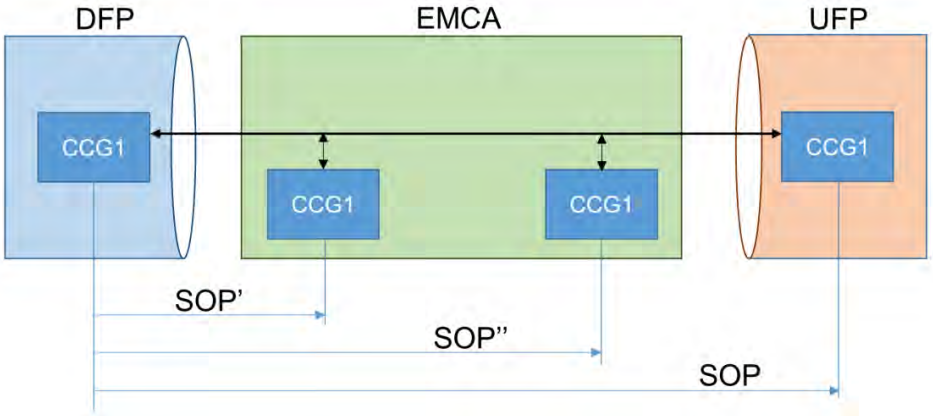
Figure 12. DFP and UFP connection with EMCA (using 4 CCG1)



You do not need to know all the details of the messaging because the CCG1 device implements the Power Delivery (and Alternate Modes) messages in firmware, and a high-level Host Processor Interface (HPI) is presented to users who would like to add messages at run time. The reference designs implement the feature set defined by the PD Specification (and the VESA DisplayPort on Type-C Specification). Should the USB specifications change, then a new firmware will be updated and released.

Messages are sent half-duplex and in the format as shown in Figure 13. Also included is a first-level decoder ring that explains some of the fields. The preamble is 64 bits of alternating 0s and 1s, which allow the receiver to sync with the actual data rate of the transmitter (300 ±30 kHz). All other data is transmitted with 4b5b encoding to improve reliability.

The CCG1 device decodes and extracts the data bytes to send to the protocol layer (refer to Figure 1). A 16-bit address/type field (which the PD Specification calls "SOP") is encoded as 20 bits as a result of the 4b5b encoding. This is always followed by a 16-bit header field, also encoded as 20 bits. The header field includes a data object count; if it is 0, then the message type is "control." If it is 1 through 7, then up to seven 32-bit data objects follow, and the message type is called "data." A 40-bit CRC is transmitted; a 5-bit end of packet (EOP) token completes the message. If the calculated CRC is the same as the received CRC, then the CCG1 device passes the decoded message up to its protocol layer, where it is processed (refer to Figure 1).

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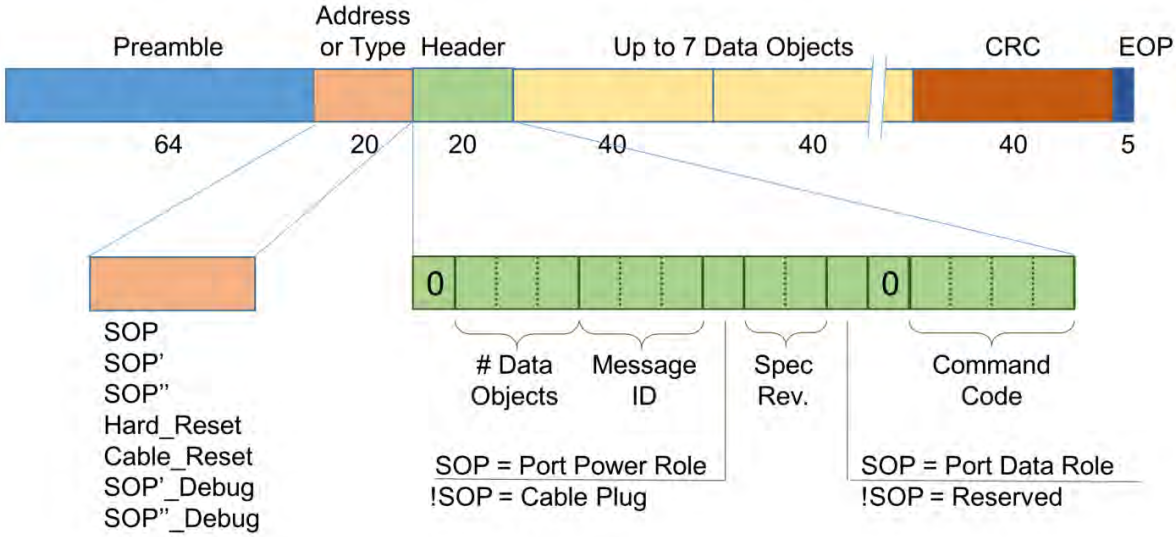
Figure 13. CC Message Format



Code	Control Message	Data Message
0000	Reserved	Reserved
0001	GoodCRC	SourceCapabilities
0010	GotoMin	Request
0011	Accept	BIST
0100	Reject	SinkCapabilities
0101	Ping	Reserved
0110	PS_RDY	Reserved
0111	Get_Source_Cap	Reserved
1000	Get_Sink_Cap	Reserved
1001	DR_Swap	Reserved
1010	PR_Swap	Reserved
1011	Vconn_Swap	Reserved
1100	Wait	Reserved
1101	SoftReset	Reserved
1110	Reserved	Reserved
1111	Reserved	VendorDefined

The names of most of the messages are self-explanatory. The CCG1 device also implements the built-in self-test (BIST) message format designed to characterize the BMC data transfer channel. The USB PD specification also includes eye diagrams, which can be used to test compliance.

A block diagram of the architecture of a CCG1 device is shown in Figure 14.

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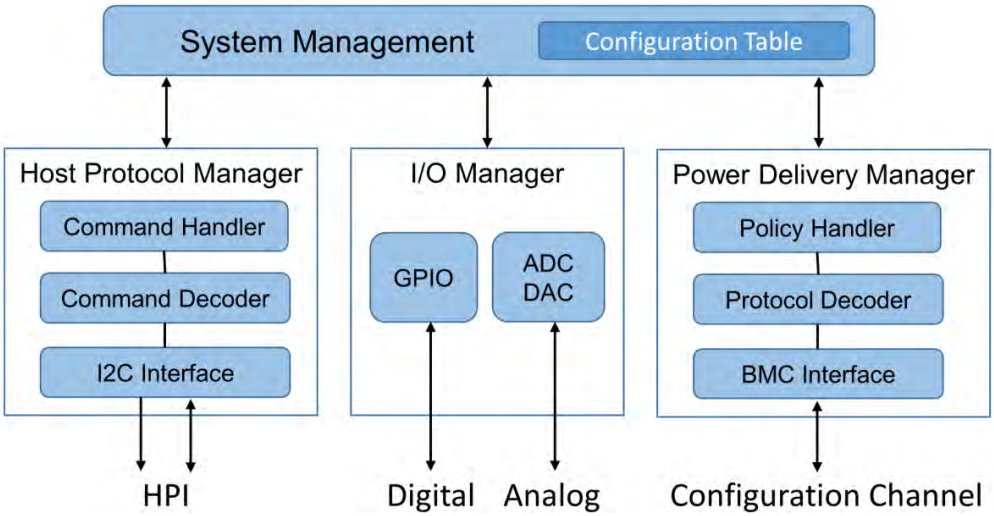
Figure 14. CCG1 Architecture Block Diagram



The CCG1 device monitors digital and analog I/O signals to create configuration channel (CC) messages. The main processor of the target host or client sends and receives the CC messages through the Host Processor Interface (HPI) included in host and client designs. The CCG1 firmware can be configured or updated over either I^2C or the CC channel (depending on the type of application) using a Cypress-supplied flash utility (described in KBA96466).

The HPI interface is a 400-kHz I^2C slave interface with an interrupt line implementing a defined command/response protocol to change configurations, monitor statuses, update firmware, or transparently interact with other CCGx devices using unstructured vendor-defined messages (VDMs).

3 Application Example Overview

Previous sections have covered enough theory to work through a Power Delivery example. The USB data paths are explained in the Adding USB Data Paths section. Figure 15 shows a before-and-after overview of what will be achieved with the first few examples. At the top of the figure is a "today" host computer with three cables attached to it: power, USB, and display. They are connected to various devices. Cypress provides the CY4501 CCG1 Development Kit that can "instantly add USB Type-C" to a today system to demonstrate the features of "tomorrow's" Type-C system. The lower half of the figure shows the same equipment, but now they are connected with a host board, an EMCA board, and a client board. The result is a single Type-C cable serving all three functions of power, USB data and display.

The CY4501 CCG1 Development Kit board designs are comprehensive, containing more features than are needed for each example that will be discussed. This enables you to select features that you need from each design. In the future, it is expected that the host design will be absorbed into the host and the client design will probably be absorbed into a display.

A Chromebox desktop PC is used as an example host, but any SuperSpeed-aware tablet or laptop can also be used.

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Figure 15. Goal of the Reference Designs

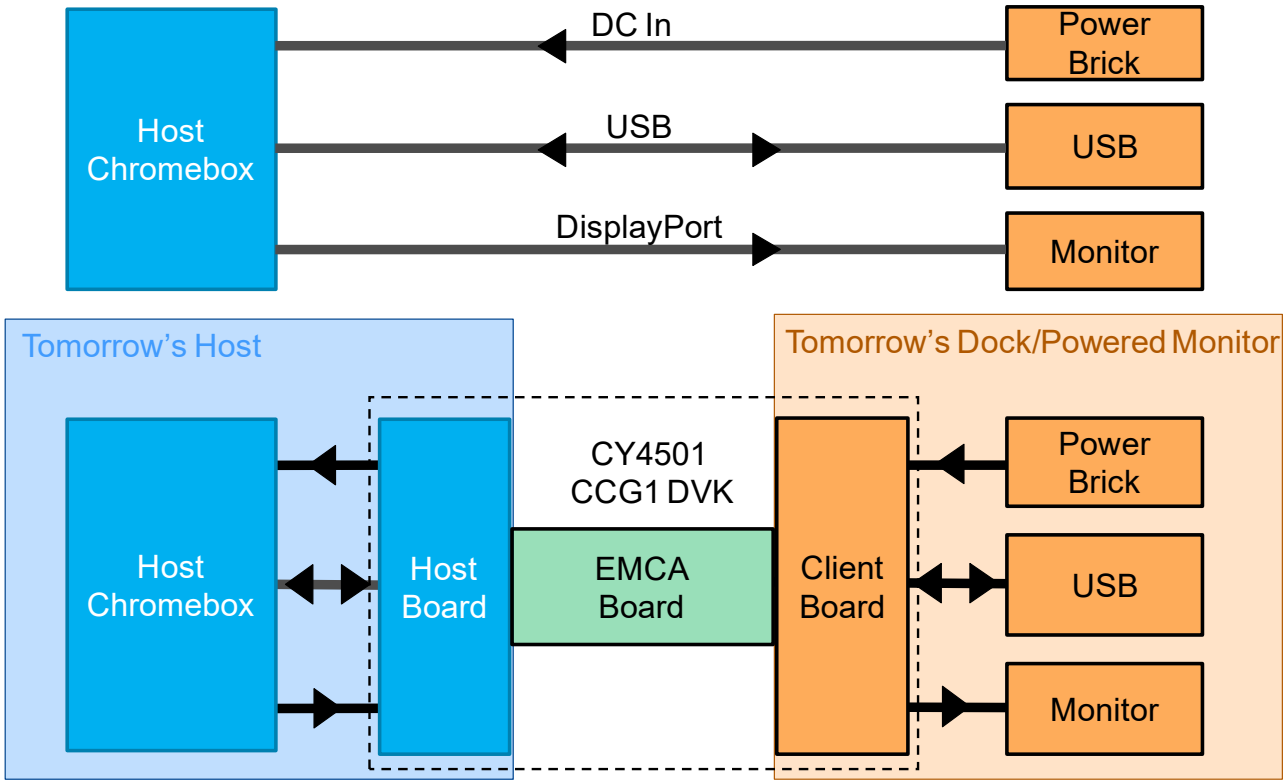

Figure 16 shows a photo of the final system setup including the three CY4501 CCG1 Development Kit boards. A full description of each board is included in the CY4501 CCG1 Development Kit User Guide. The same boards will be used in all the examples in this application note, but not every feature of each board will be used in every example.

Figure 16. Chromebox PC and Three CY4501 CCG1 Development Kit Boards with Debug Laptop

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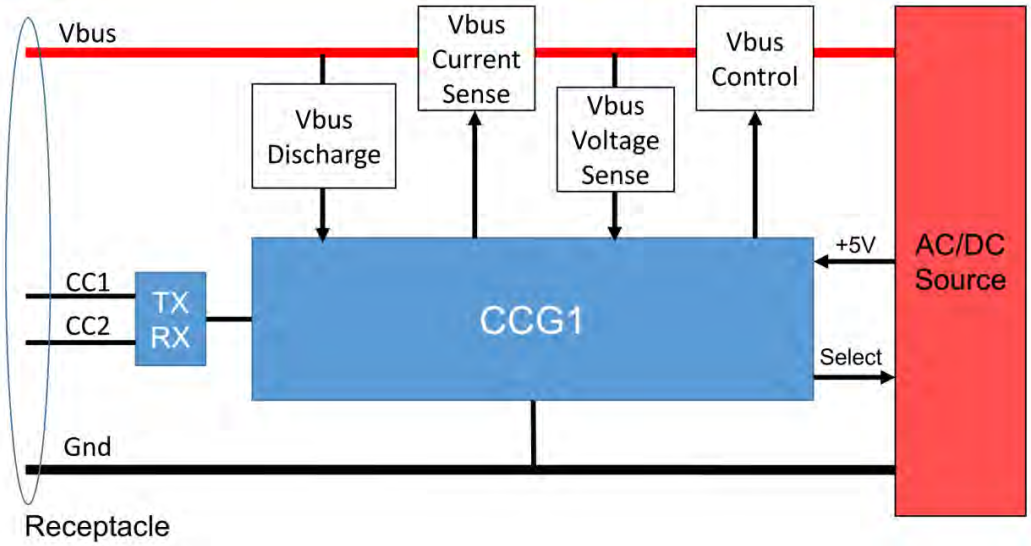
3.1 Power Provider Design

Many considerations are involved in how 100 W of power, 20 V at 5 A, can be safely delivered via a Type-C connector. Figure 17 shows additional circuit elements that must be considered. The CCG1 device includes capabilities to manage this complete power delivery path.

In this example, the client board will operate as a power adapter. It expects a 24-V input that it will regulate down to 20 V, 13 V, 12 V, or 5 V at up to 5 A as commanded by the CCG1 device. The schematics in the CY4501 CCG1 Development Kit User Guide show details of the connections and part numbers used in the reference design.

Figure 17. Safe Delivery of 100 W Must Include Protection Circuits



At power on, the CCG1 device waits for a connection, as described in the Configuration Channel: Cable Detect section. On initial connection, the CCG1 device selects Vbus at 5 V from the DC/DC converter and sets its overvoltage detection circuit to +5 V + 20 percent and its overcurrent detection to 3 A + 50 percent (assuming Rp is 10 kΩ). The Vbus discharge block is required by the USB PD specification to safely discharge the power supply when the connection is terminated, thus resetting the Vbus voltage on the Type-C connector to 0 V.

Set up the jumper settings on the CY4501 CCG1 Development Kit boards as described in the CY4501 CCG1 Development Kit User Guide and then connect them to the host and a power brick, as shown in Figure 18. Note that two USB cables are connected to the mini-B connector of the client board and mini-B connector of the host board. They are only used to supply +5 V to each of the boards.

Also connected to the "debug" laptop is the CC sniffer. The sniffer has a single CC probe wire and a ground wire. The easiest place to attach it is on the EMCA board; TP8 = CC and pin 18 on J9 and J10 = ground (you will probably solder a stake pin onto TP8 so that the sniffer is pluggable).

This example uses a spare PC power brick with the DC cable cut to implement Figure 18. These connections are labeled "DC." The power brick provides power to the client board, and the host board provides power to the Chromebox PC.

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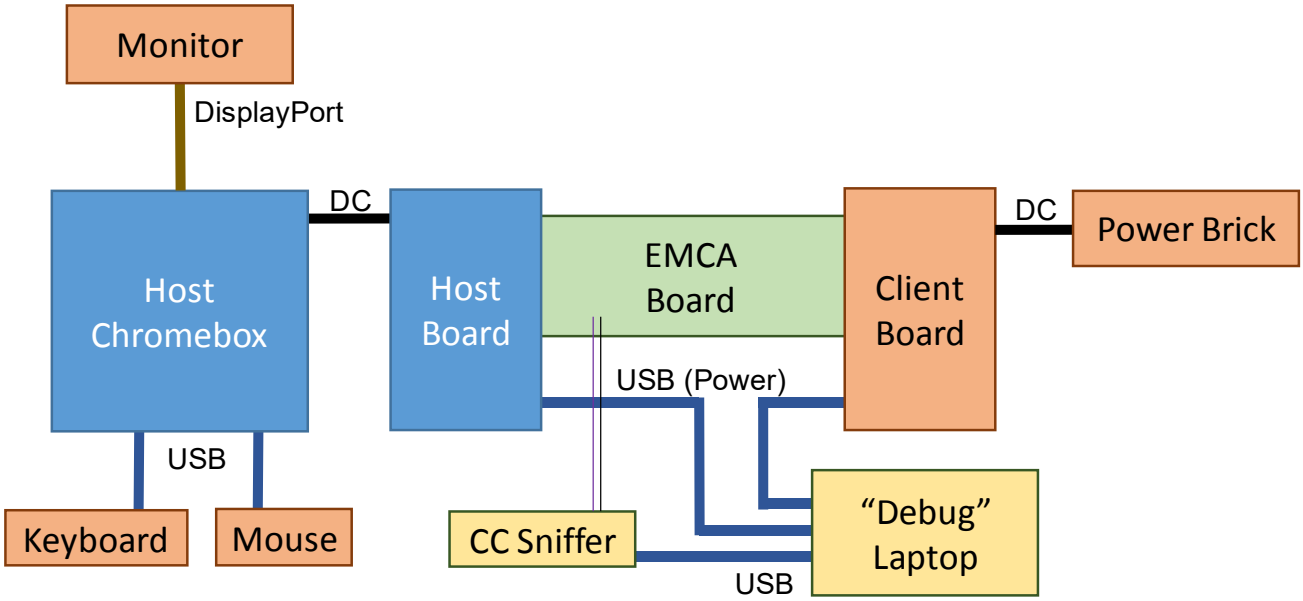
Figure 18. Hardware Setup for Power Delivery Example



On power up, both the host board and the client board have the default state as DRPs and will periodically switch roles until they decide between themselves as to which is the DFP and which is the UFP. Upon connecting the UFP and DFP with each other, the host board would come up as the DFP. The reason is that the PD Specification allows you to set a bias for a DRP (or a UFP). The host board firmware implements the Try.DFP portion of the Power Delivery state machine, and this bias causes the host board to always be a DFP. Figure 19 shows a partial state machine of two interconnected DRPs (extracted from the Type-C Specification, section 4.5.2).

Figure 19. Two DRPs Resolving DFP and UFP Roles

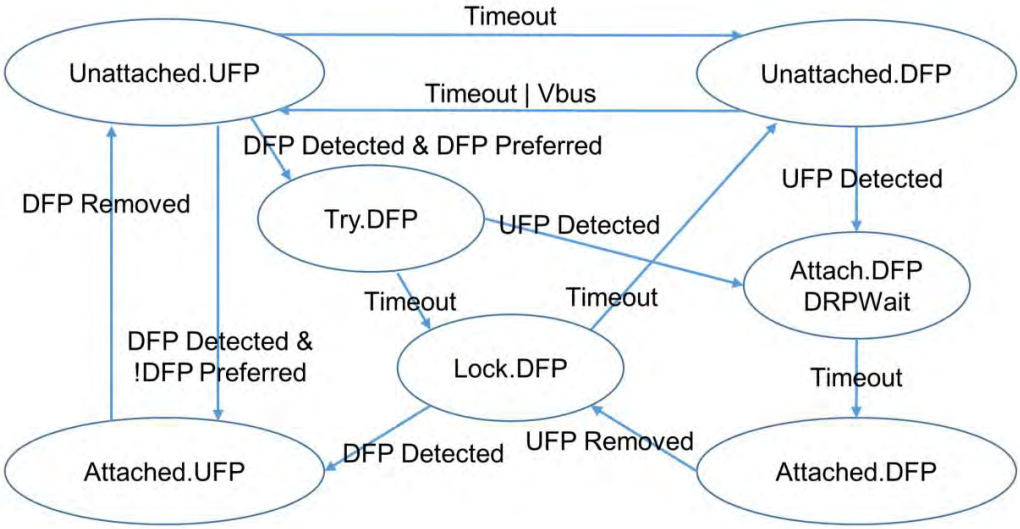


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Figure 20 shows the message flow during initial connection. The DRP discovers that an EMCA is attached due to the presence of Ra, so it discovers the characteristics of the cable via the DiscoverACK response message. Note that each command and data message is acknowledged by the receiver, which sends a GoodCRC response back to the initiator. The initiator starts a timer for each message it sends, and if a GoodCRC message is not received within a timeout (the PD Specification lists all of them), then an error recovery is started. The message could be lost due to a failed CRC, for example, and it is the responsibility of the initiator to take corrective action. Only the first GoodCRC message is labeled in the figure. All others are colored purple.

The DFP detects the presence of a UFP due to the Rp resistor, so it sends it a capabilities message. Within this message is the ability to source 5 V at 900 mA, and the UFP makes a request for 500 mA of it. The DFP accepts and then turns on Vbus. The UFP, on detecting Vbus, could start enumeration if it had USB data channels. The comments in the figure explain the flow, and the vertical red line is Vbus.

Figure 20. Flow of CC Messages at Power On

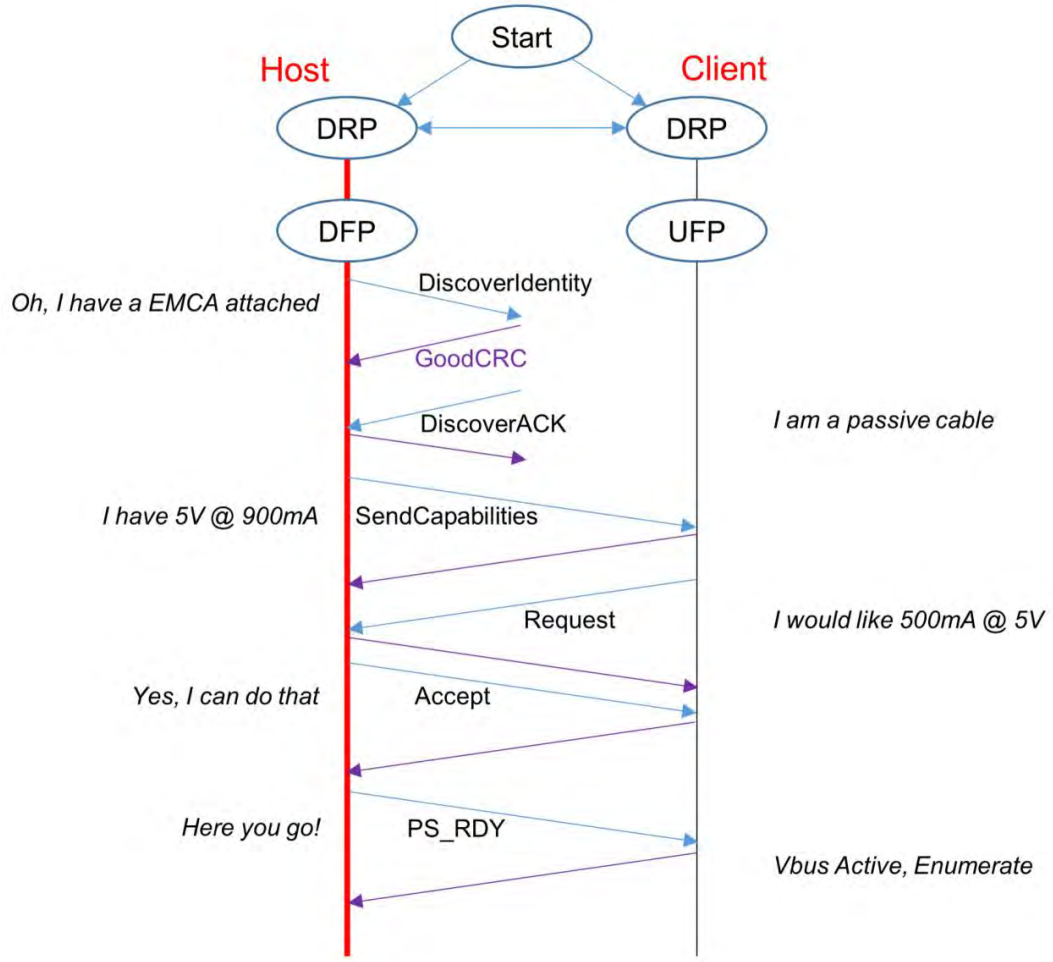

Figure 20 hides some of the complexity that the CCG1 devices are implementing. Each generated message has a MessageID inserted and a CRC added. The conversation between CCG1 devices typically entails a request followed by a response. Each CCG1 device will check that all messages have the correct CRC and that response MessageIDs match request MessageIDs. All actions are also timed and counted, and the PD Specification details a great number of constraints and what to do if any are violated. The CCG1 reference designs implement all the requirements of the PD Specification. The CCG1 firmware will be updated as necessary so that all compliance tests, when available, will be passed.

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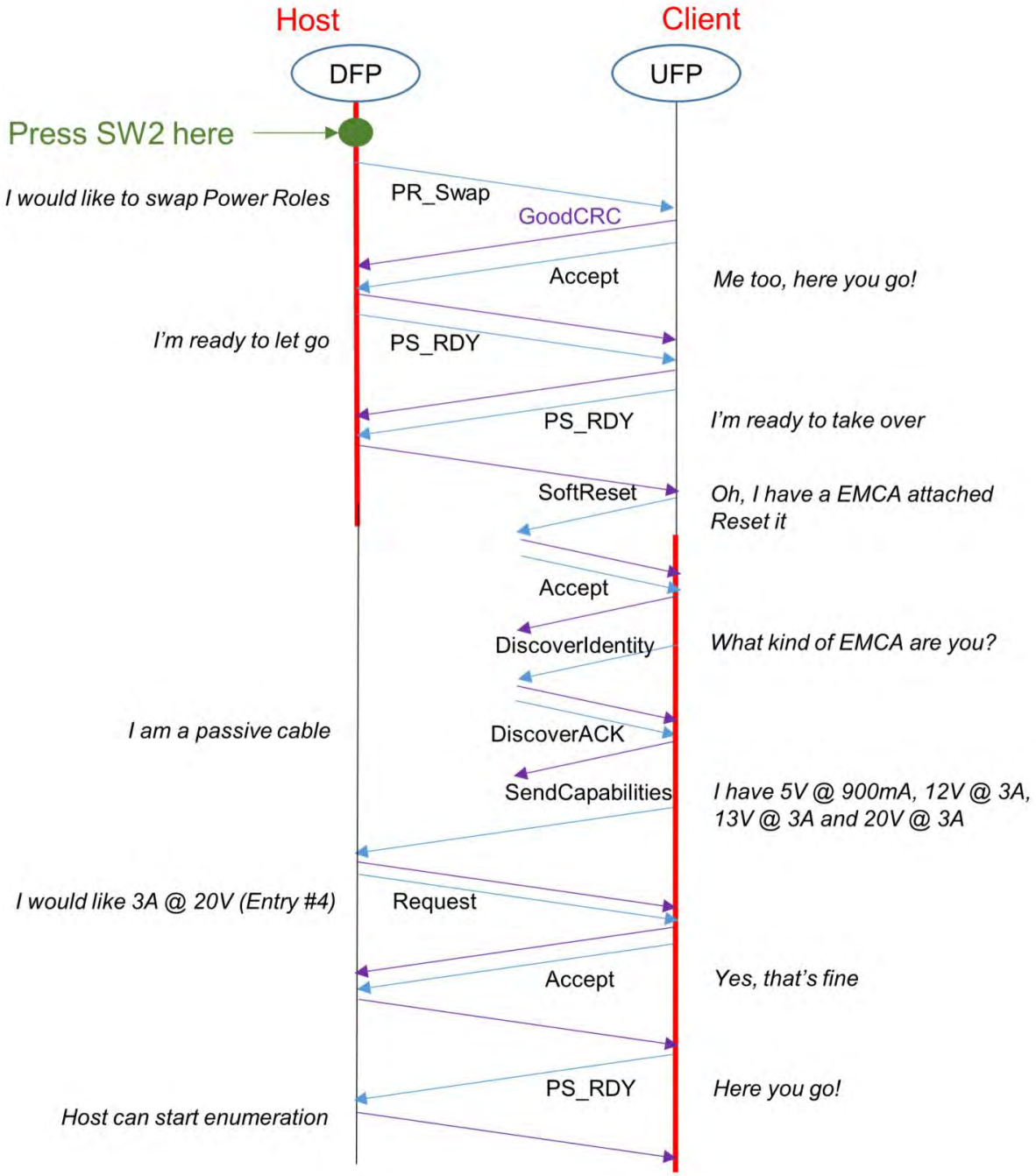
To demonstrate the power adapter capabilities, press SW2 on the host board to initiate a power role swap (PR_Swap). Figure 21 shows the messages that are exchanged. They are similar to the initial power-on messages except that the client board is the new initiator. The client board has a power brick attached, so it can offer more power options. The host board chooses 3 A at 20 V, and the client board delivers it over Vbus to be available at the host board's DC out connector. The vertical red lines show the transfer of ownership of the Vbus line.

The host computer is now being powered by the power brick via the Type-C cable.

Figure 21. Flow of CC Messages in Power Delivery Example



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The PD Specification makes power delivery seem complex, because a specification must cover all conceivable cases. This Type-C–only example demonstrated the essence of power delivery. It is straightforward because all the heavy lifting has been done by the CCG1 firmware.

3.2 Adding USB Data Paths

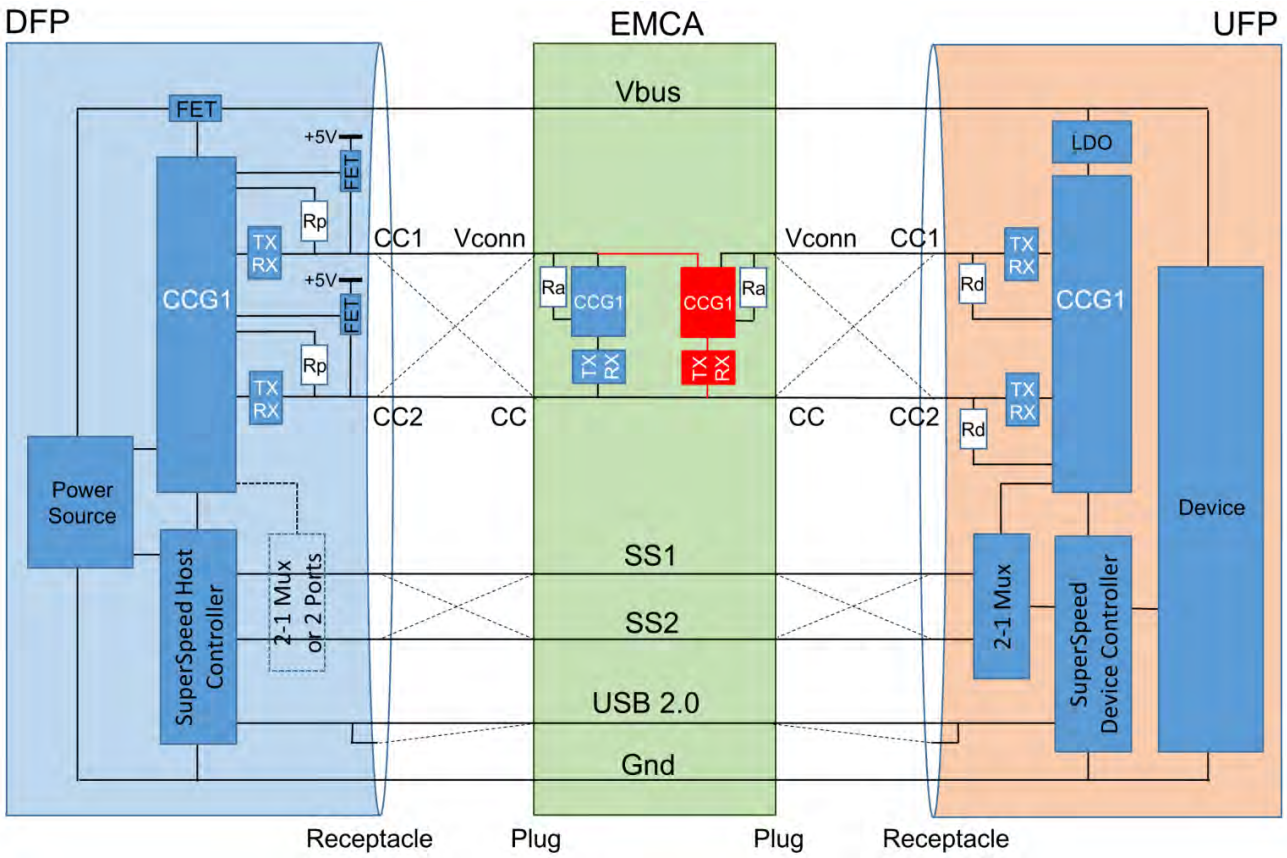
This document has covered only the power delivery aspect of a Type-C design thus far. The reversible connector has implications on the data path too. As shown in Figure 2, the SuperSpeed data lanes can be swapped; however, the USB 2.0 signals, Dp and Dn, are not swapped because Dp1 and Dp2 are connected and Dn1 and Dn2 are connected in the receptacle.

Figure 22 extends Figure 9 to include the USB data paths. A data multiplexer (MUX) must now be included in a UFP so that it can select the SuperSpeed lane, SS1 or SS2, which is carrying the data. The DFP needs the same logical switch, which could be implemented as a MUX or two host ports on the SuperSpeed host controller. The CCG1 devices control these switches.

It is technically possible to have both SuperSpeed lanes active in a Type-C cable. This would be easy for the Host, but the peripheral would need to implement two independent SuperSpeed device controllers.

The schematics of the CY4501 CCG1 Development Kit show details of the 5-Gbps MUXes used in both designs. Data switching circuitry is also included for Alternate Modes, as described in the following section.

Figure 22. Routing Is Required on the SuperSpeed Data Lanes



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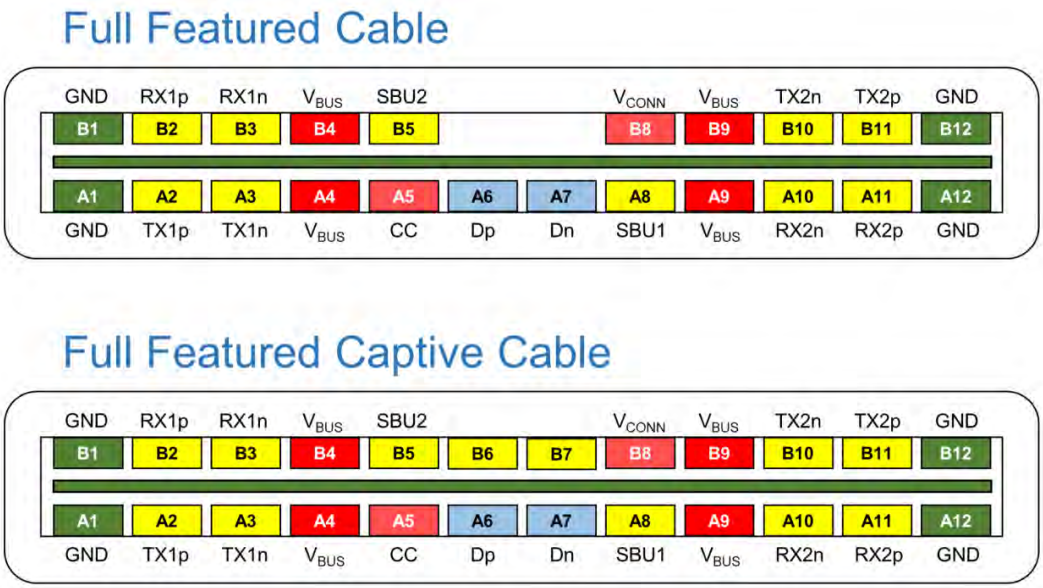
3.3 Type-C Alternate Modes

The Type-C Specification designates several signals that can be repurposed within a Type-C interconnect. Figure 23 shows these signals in yellow. The two SuperSpeed lanes (four differential pairs), two sideband signals, and if the peripheral is directly connected (no intervening cable between UFP and DFP), Vconn and the two unallocated plug pins, B6 and B7, can also be used. A dock or a dongle with a captive cable would be examples of directly connected devices.

Figure 23. Up to 9 Signals (4 pairs + 5) Can Be Repurposed



Before the signals can be reassigned, the DFP and UFP must have a conversation to agree on the new mode in which the signals will now operate. Basically, the DFP asks the UFP which modes it supports, and if the DFP also supports this mode, it will enter it. However, the DFP must check that any intervening cable also supports this new mode. Hubs are not required to propagate Alternate Mode signals, so Alternate Mode operation is defined only between a DFP and a connected (via cable or directly) UFP.

If the UFP does not support the mode that the DFP desires, then it must not fail silently. The Type-C Specification uses the USB 2.0 channel, which is always present, as the mechanism to report and resolve Alternate Mode conflicts. A USB device that supports the Billboard class must be present on the UFP attached to the Dp and Dn lines.

A popular example of using a Type-C interconnection in Alternate Mode is DisplayPort. Figure 24 is a block diagram of the host and client boards showing data MUXes that the CCG1 devices control to switch the use of both SuperSpeed pairs and the sideband signals for DisplayPort use. The CY4501 CCG1 Development Kit design hardware supports four lanes of DisplayPort at the host and client end. The design files for these boards can be found here. Other examples of Alternate Mode signals that could be implemented include PCIe, Mobile High-Definition Link, and eSATA.

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Figure 24. Block Diagram of Data Path Switching for Alternate Mode Example

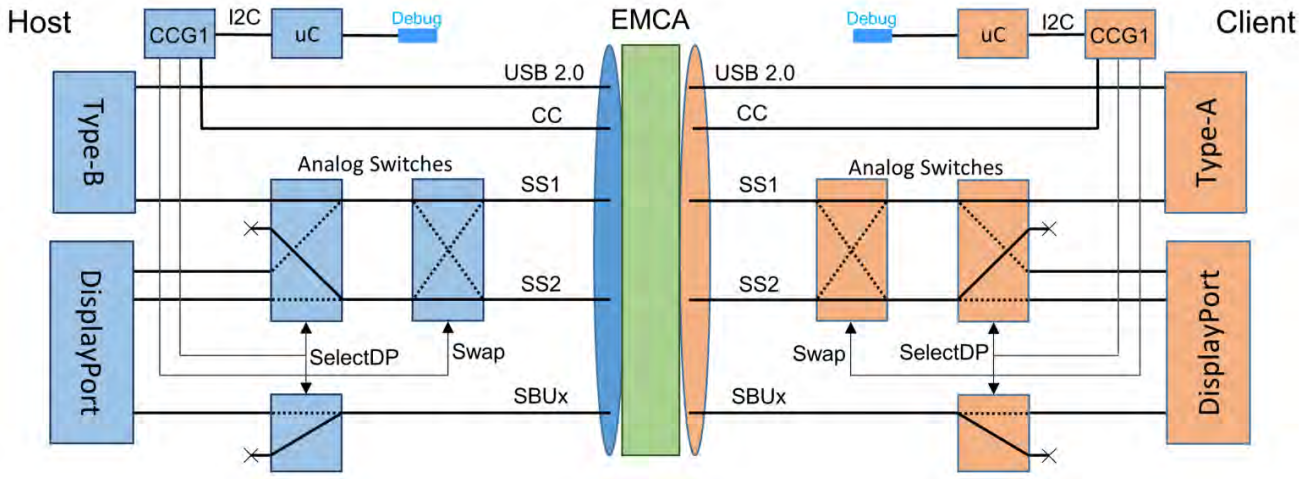
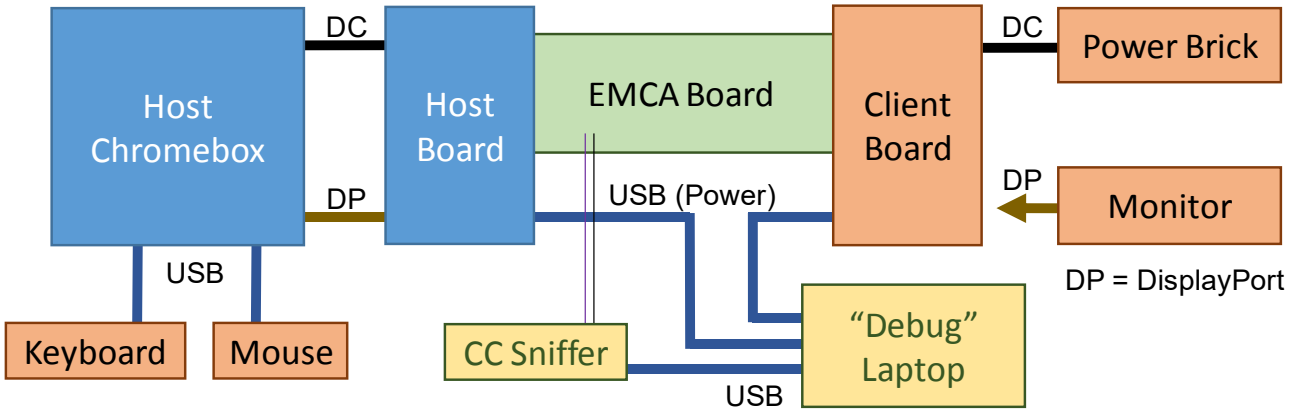


Figure 25 shows a configuration of the hardware for the Alternate Mode Example. The power brick is still connected, and the DisplayPort monitor has been moved from the Chromebox PC. It will be connected to the client board. The Chromebox PC is now connected to the host board with a standard DisplayPort cable. Note that the debug computer connections are still present.

Figure 25. Setup for Alternate Mode Example



The boards power up as before, and the client board provides power to the host board. Figure 26 shows the startup conversation between the host and client, with the GoodCRC messages shown in purple.

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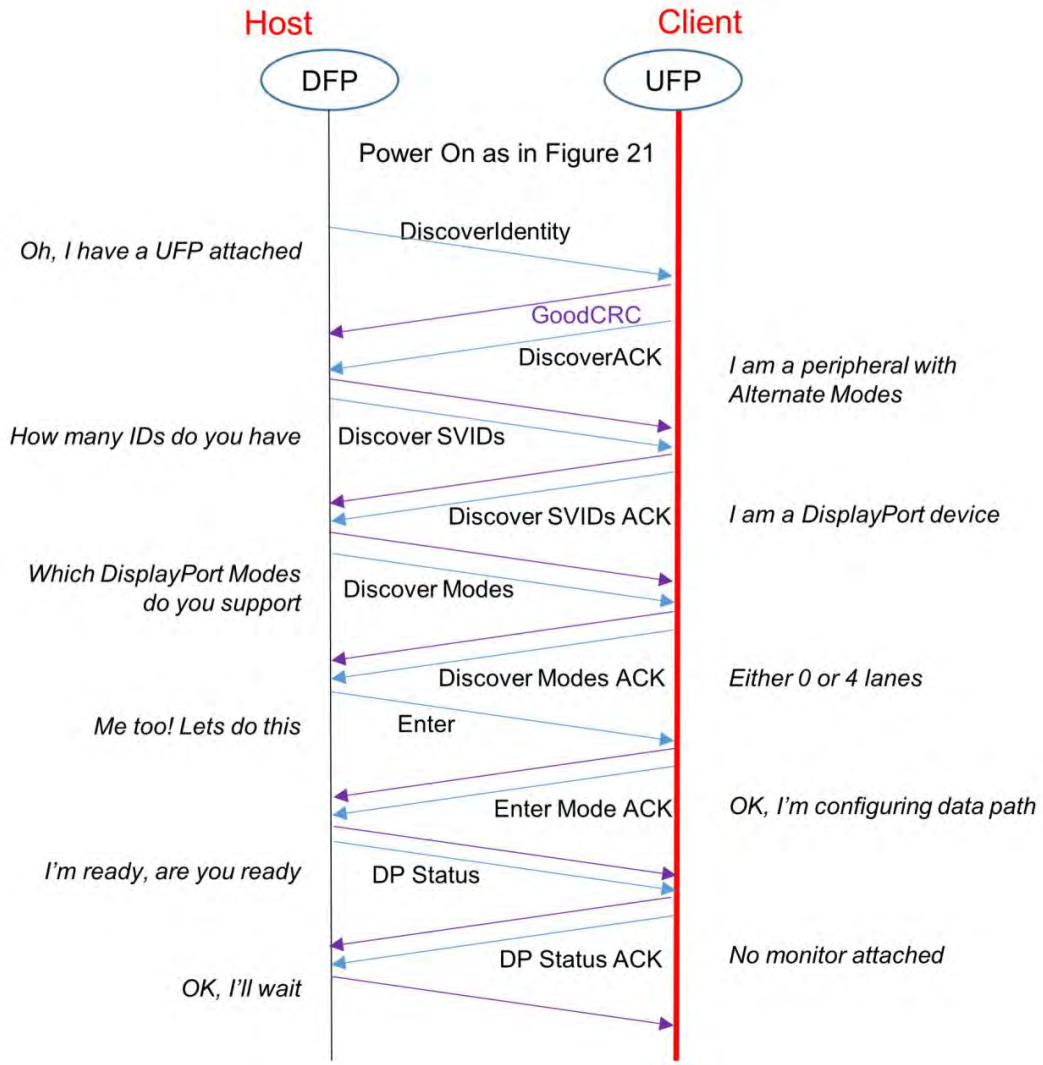
Figure 26. CC Messages Exchanged During Alternate Mode Initialization



The host board discovers that it has an Alternate Mode device attached, so it discovers its Type-C Specification defined Standard ID (SID) or Vendor ID (VID) (so SVID = SID or VID). The client board reports an SVID of 0xFF01, which is an ID assigned to a DisplayPort connection. This is fully documented in the VESA specification, DisplayPort Alt Mode on USB Type-C Standard, which is available only to VESA members. This example uses key information extracted from the specification for annotation purposes.

The client board reports that it supports four DisplayPort lanes. The host also supports the four-lane mode, so it enters this mode, as does the client (signaled by its positive ACK). The host now checks the DisplayPort status, and the client board reports that no display is attached.

Now, attach the DisplayPort monitor to the client board. The client CCG1 device recognizes the connection, via an I/O pin connected to the Hot Plug Detect (HPD) pin, and initiates an Alternate Mode sequence by sending an Attention message to the host, as shown in Figure 27. The host rechecks the status and, since all is good, it sends a DisplayPort Configure message to the client. Both CCG1 devices switch over their MUXes so that the Chromebox PC display appears on the monitor.

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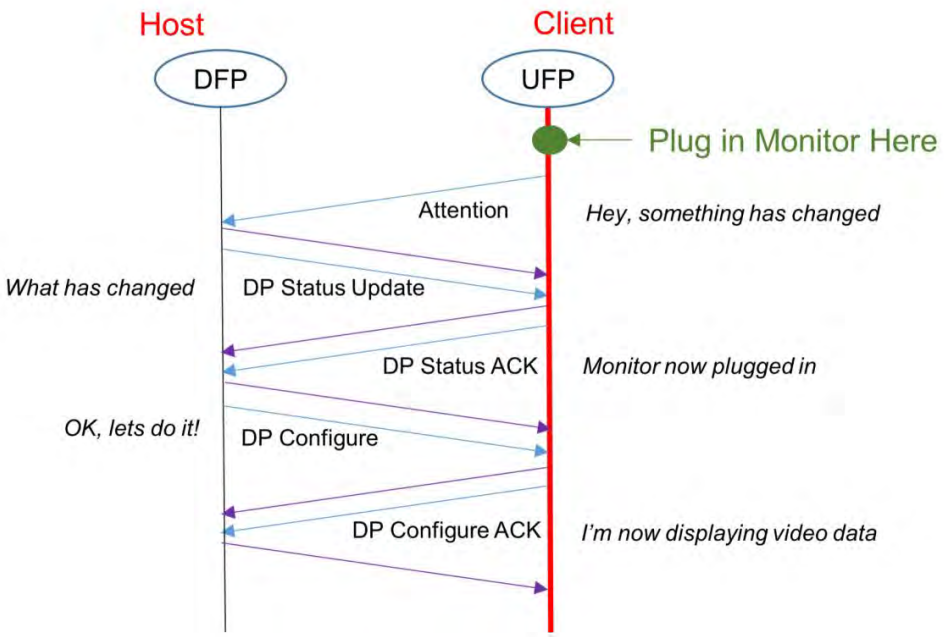
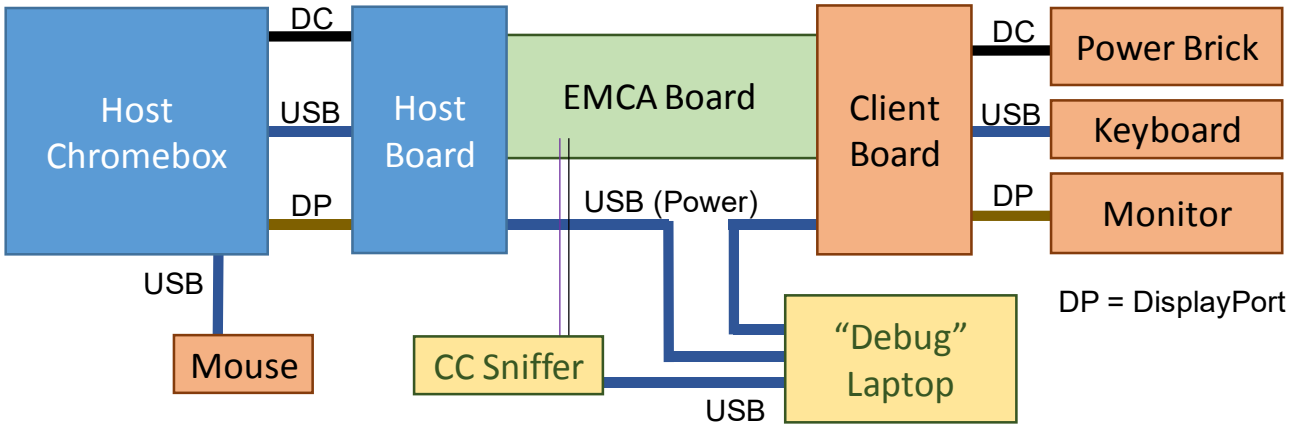
Figure 27. Host and Client Negotiate to Support DisplayPort



As a final experiment, you could disconnect the keyboard from the Chromebox PC and connect it to the USB Type-A connector on the client board, as shown in Figure 28. The Host PC will be connected to keyboard here too as expected.

Figure 28. Setup for DisplayPort plus USB Example



You now have power, display, and USB all running over the single USB Type-C cable.

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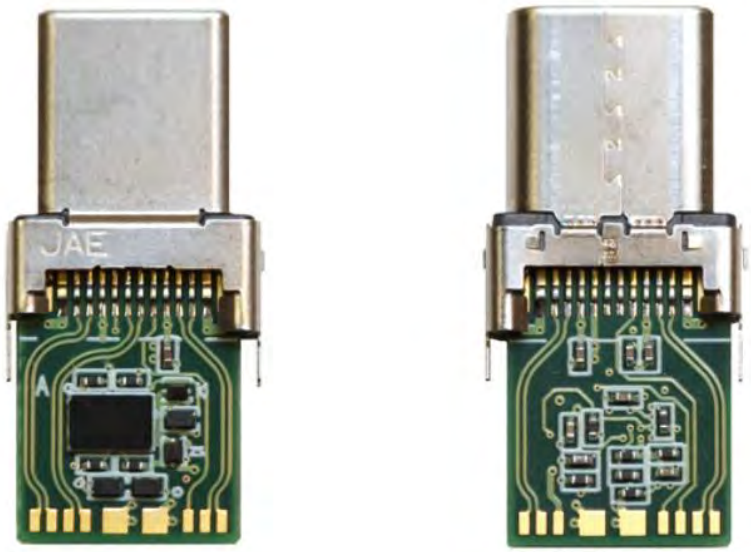
4 Designing a Type-C EMCA

The CCG1 EMCA board of the CY4501 CCG1 Development Kit implemented a cable as a PCB with many jumpers and probe points so that various solutions using one or two CCG1 devices could be explored. The paddle card design shown in Figure 11 is a full reference design. Schematics are downloadable from the CCG1 EMCA Paddle Card Reference Design web page. Figure 29 shows the front and back of the paddle board without wires or plastics.

Figure 29. Complete CCG1-Based Cable Paddle Board Reference Design



4.1 Hardware Design Guidelines

Within a paddle card design, CCG1 devices are powered from the Vconn supply of the DFP. Consider the following while designing the power system network:

1. Placement of bulk and decoupling capacitors
2. Placement of power and ground planes

Placement of Bulk and Decoupling Capacitors

Place decoupling capacitors for high-frequency noise filtering close to the Vconn, Vddd, and Vccd pins as shown in Reference Schematics. Place the bulk capacitor, which acts as a local power supply to the power pin, close to the Vddd pin of CCG1. The Vbus connections need bulk decoupling close to the connector; a 10-nF bypass capacitor per Vbus pin is recommended.

Make the power trace width the same as the power pad width. To connect the power pins to the power plane, keep vias very close to the power pads. This helps minimize stray inductance and IR drop on the line.

Placement of Power and Ground Planes

Place the power plane close to the ground plane for good planar capacitance. Planar capacitance between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing electromagnetic radiation.

The USB data lines, both SuperSpeed lanes and USB 2.0 signals, although not connected to the CCG1, are always close to it in a paddle card design. The USB data lines are most critical to achieve good signal quality and reduce emission. Follow the guidelines below while designing a paddle card:

1. Use a high-performance substrate material for paddle cards.
2. Keep USB SuperSpeed traces as short as possible. Ensure that these traces have a nominal differential characteristic impedance of 90 ohms.

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3. Match the differential SS pair trace lengths within 0.12 mm (5 mils).
4. Match the high-speed (Dp and Dn) signal trace lengths within 1.25 mm (50 mils).
5. Ensure that the differential pairs have a minimum pair-to-pair separation of 0.5 mm.
6. Adjust the high-speed signal trace lengths near the USB receptacle, if necessary.
7. Make adjustments for SS RX signal trace lengths near the USB receptacle. Make adjustments for SS TX signal trace lengths near the device if necessary.

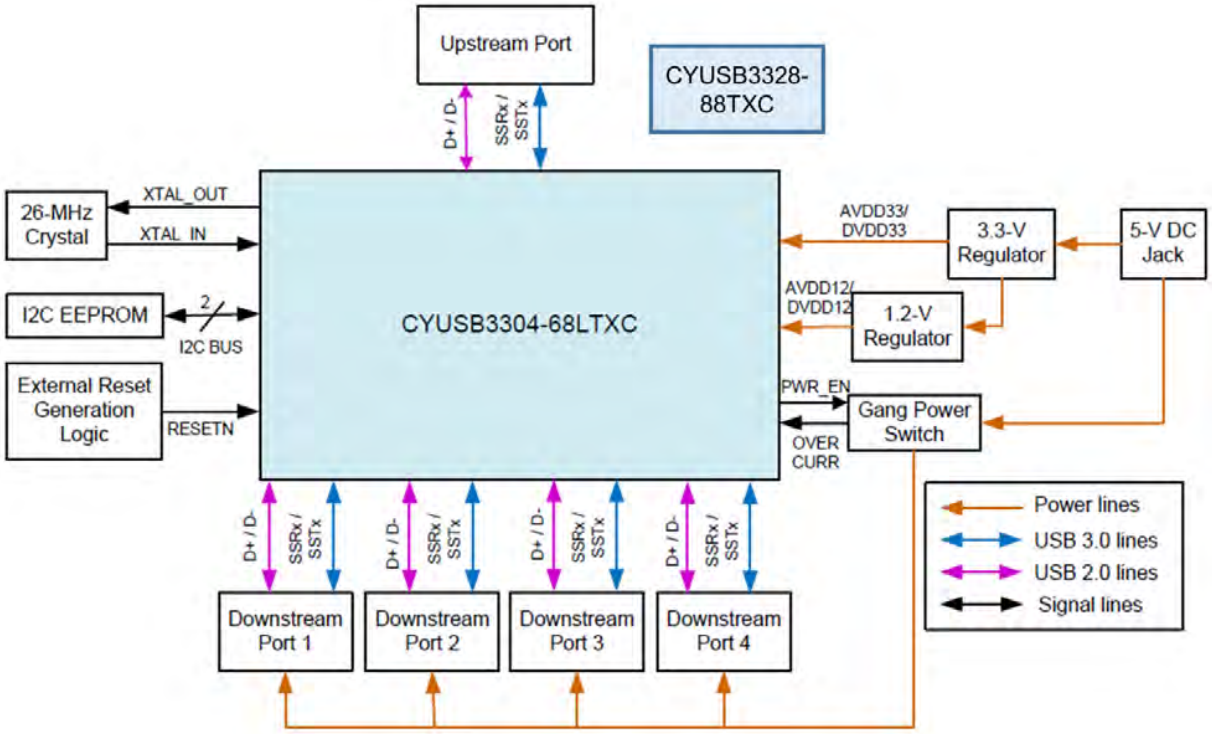
These guidelines should be followed with the layout of host and peripheral CCG1 designs but typically these are less critical because a larger-package CCG1 may be used and it is located further from the USB data lines. In these designs, an I^2C bus is connected to the CCG1 and this should be pulled up with 2.2-kΩ resistors to the CCG1 Vddd supply. The CY4501 CCG1 Development Kit includes reference layout material for these designs.

A compact Type-C to DisplayPort Adapter Reference Design is also available for study.

5 Designing a Docking Station

This section extends the design of the client board and adds a hub and a collection of other devices that would be found in a docking station. Designs using a hub were straightforward prior to the introduction of the PD Specification, as shown in Figure 30. This is a figure from AN94150 – Designing a SuperSpeed Hub Using HX3 with Optimized BOM in which a self-powered hub distributed 900 mA at 5 V to four downstream ports (a total of 18 W). The major design decisions were whether to support ganged or distributed overcurrent detection and which indicator LEDs to include.

Figure 30. Hub Design Before Power Delivery Specification



A hub now plays a much more important role because it can manage and distribute up to 100 W of power for each Type-C port. Each port can be a power provider or power consumer, and it is now feasible for a docking station or powered monitor to power and/or charge a laptop or tablet using the same single Type-C cable used for data.

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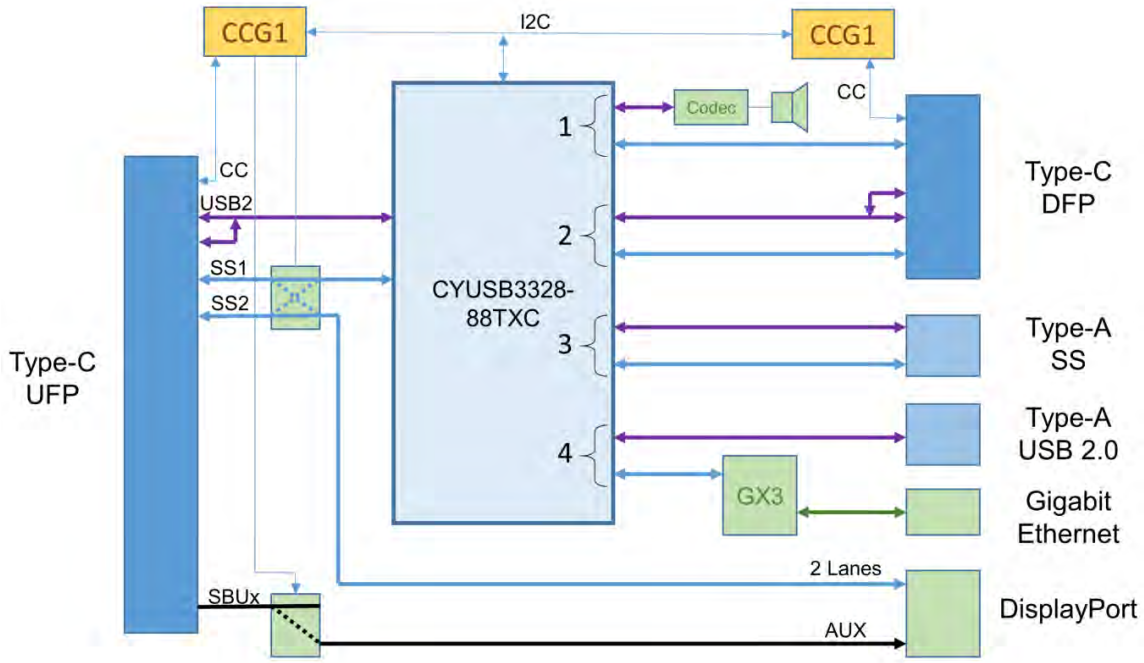
The HX3 also has some unique features that are showcased in this design. A USB 3.1 bus is, in fact, two separate and independent buses, a SuperSpeed bus and a high-speed USB 2.0 bus packaged in a single cable, but only one of these buses is usually active. The HX3 contains additional circuitry that enables both buses to be active if embedded devices are implemented. Figure 31 shows the data paths within a docking station/powered monitor design. Note that the HX3's Shared Link™ technology allows more downstream capability than a typical hub component.

Downstream ports 1 and 2 are both routed to a Type-C connector. Because both SS1 and SS2 are driven, the cost and complexity of a data switch is saved. Also, there is a "spare" USB 2.0 channel, which is used to drive an audio codec. HX3 Downstream Port 3 is connected to a Type-A connector for the attachment of flash drives, backup hard drives, or similar SuperSpeed peripherals. The SuperSpeed lines of the HX3 Downstream Port 4 are connected to a Gigabit Ethernet controller, the GX3. Because the USB 2.0 lines are not needed for this embedded device, they are connected to a Type-A connector for a mouse, keyboard, or wireless dongle that would support both the mouse and keyboard.

Also shown is a two-lane DisplayPort Alternate Mode device, implemented on SuperSpeed lane 2. A switch would not be needed if the dock was a directly connected device and the host knew how to send DisplayPort data on lane 2 (that is, the host and docking station are manufactured by the same vendor).

Figure 31. Data Paths of a Type-C Hub Design



6 Summary

This application note showed that all forms of Type-C design can be implemented with the CCG1 controller. The reference designs, including full schematics and application software, will get you off to a running start. The examples are based on SuperSpeed, but remember that Type-C Power Delivery is also applicable to USB 2.0 high-speed systems.

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7 Related Documents

User Guides

- CY4501 CCG1 Development Kit Guide
- CY8CKIT-040 – PSoC 4000 Pioneer Development Kit Guide

Application Note

- AN94150 – Designing a SuperSpeed Hub Using HX3 with Optimized BOM

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Title: Applications Engineer Sr

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8 Appendix A: USB and Type-C Acronyms

BMC	biphase mark code
CC	configuration channel
CCGx	configuration channel controller generation 1 or 2
CDP	charging downstream port
CRC	cyclic redundancy check
DCP	dedicated charging port
DFP	downstream facing port
DRP	dual-role port
EMCA	electronically marked cable assembly
I^2C	inter-integrated circuit
OCP	overcurrent protection
OVP	overvoltage protection
PD	power Delivery
PD Specification	USB Power Delivery Specification Revision 2.0, Version V1.0, a free download from www.usb.org/developers
PDO	power delivery object
PHY	physical Layer
SCB	serial communication block
SDP	standard downstream port
SOP	Start of Packet symbol directed at USB-PD Port Partner.
SOP'	Start of Packet symbol directed at CCGx at the near end of the EMCA
SOP''	Start of Packet symbol directed at CCGx at the far end of the EMCA
SOP*	Collectively denoting the Start of Packet symbol (SOP, SOP', and SOP'')
SWD	serial wire debug
Type-C Specification	USB Type-C Cable and Connector Specification Revision 1.0, a free download from www.usb.org/developers
UFP	upstream facing port
USB	Universal Serial Bus
USB-IF	USB Implementers' Forum, a non-profit organization chartered with promoting USB
USB-PD	USB Power Delivery

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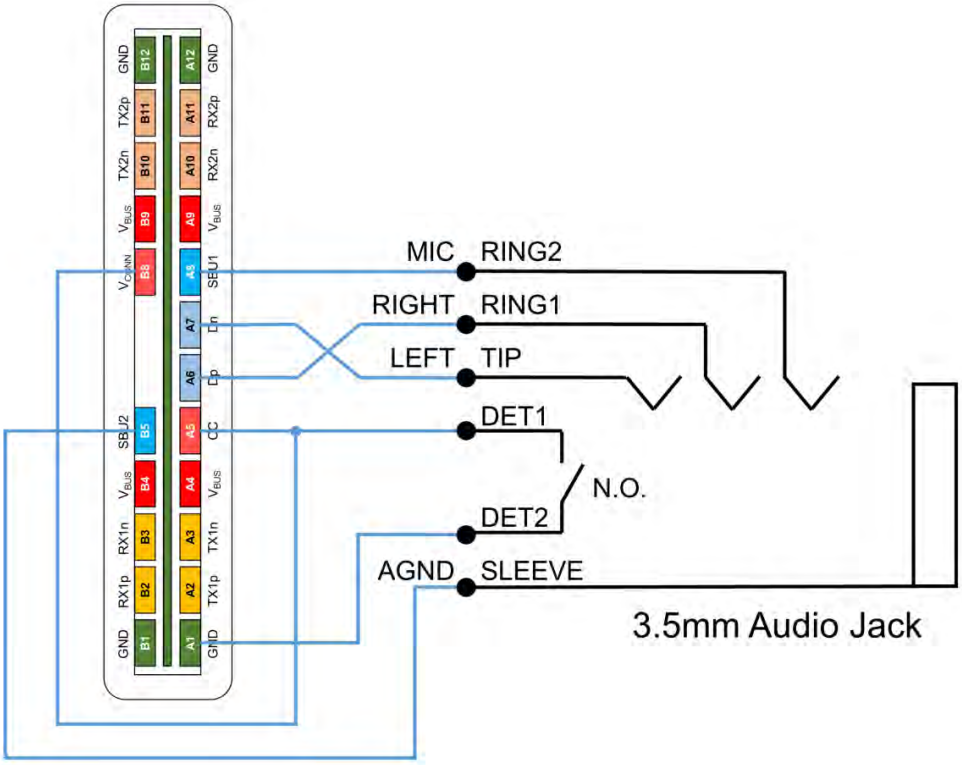
9 Appendix B: Accessories

A UFP is defined as having an Rd on its CC lines. If Rd is less than Ra (Ra = 1 kΩ ± 20 percent), then the DFP would recognize this device as an audio accessory, as shown in Figure 32. Note that Vconn and CC are connected together and then connected to DET1 on the audio jack. When an audio plug is inserted, the switch is closed, and DET1 is shorted to ground (a short is less than 1 kΩ). The DFP will see this as a connection event. It is essential that the DFP does not apply +5 V to Vconn on this audio accessory, since it is connected directly to ground.

Figure 32. Connection of an Audio Jack to Type-C Plug



The simplicity of this design is that it contains only wires. There are no active or passive components. In this way, headphones could be made with a Type-C plug instead of an audio jack with little cost added.

The Type-C Specification also describes a debug accessory, but no details have been disclosed.

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