Universal Serial Bus Type-C Cable and Connector Specification

Revision 1.2
March 25, 2016

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 1
Microchip v. Aptiv
IPR2024-00496

Copyright © 2014-2016, USB 3.0 Promoter Group:
Hewlett-Packard Company, Intel Corporation, Microsoft Corporation,
Renesas, STMicroelectronics, and Texas Instruments
All rights reserved.

NOTE: Adopters may only use the USB Type-C™ cable and connector to implement USB or third party functionality as expressly described in this Specification; all other uses are prohibited.

LIMITED COPYRIGHT LICENSE: The USB 3.0 Promoters grant a conditional copyright license under the copyrights embodied in the USB Type-C Cable and Connector Specification to use and reproduce the Specification for the sole purpose of, and solely to the extent necessary for, evaluating whether to implement the Specification in products that would comply with the specification. Without limiting the foregoing, use of the Specification for the purpose of filing or modifying any patent application to target the Specification or USB compliant products is not authorized. Except for this express copyright license, no other rights or licenses are granted, including without limitation any patent licenses. In order to obtain any additional intellectual property licenses or licensing commitments associated with the Specification a party must execute the USB 3.0 Adopters Agreement. NOTE: By using the Specification, you accept these license terms on your own behalf and, in the case where you are doing this as an employee, on behalf of your employer.

INTELLECTUAL PROPERTY DISCLAIMER

THIS SPECIFICATION IS PROVIDED TO YOU "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE AUTHORS OF THIS SPECIFICATION DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OF INFORMATION IN THIS SPECIFICATION. THE PROVISION OF THIS SPECIFICATION TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

All implementation examples and reference designs contained within this Specification are included as part of the limited patent license for those companies that execute the USB 3.0 Adopters Agreement.

USB Type-C™ and USB-C™ are trademarks of the Universal Serial Bus Implementers Forum (USB-IF). All product names are trademarks, registered trademarks, or service marks of their respective owners.

 Microchip Ex. 1019, p. 2
Microchip v. Aptiv
IPR2024-00496

CONTENTS

Specification Work Group Chairs / Specification Editors 11
Specification Work Group Contributors 11
Pre-Release Draft Industry Reviewing Companies That Provided Feedback 13
Revision History 14
1 Introduction 15
1.1 Purpose 15
1.2 Scope 15
1.3 Related Documents 16
1.4 Conventions 16
1.4.1 Precedence 16
1.4.2 Keywords 16
1.4.3 Numbering 17
1.5 Terms and Abbreviations 17
2 Overview 20
2.1 Introduction 20
2.2 USB Type-C Receptacles, Plugs and Cables 21
2.3 Configuration Process 22
2.3.1 Source-to-Sink Attach/Detach Detection 23
2.3.2 Plug Orientation/Cable Twist Detection 23
2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship 23
2.3.4 USB Type-C VBUS Current Detection and Usage 24
2.3.5 USB PD Communication 24
2.3.6 Functional Extensions 25
2.4 VBUS 25
2.5 VCONN 25
2.6 Hubs 26
3 Mechanical 27
3.1 Overview 27
3.1.1 Compliant Connectors 27
3.1.2 Compliant Cable Assemblies 27
3.1.3 Compliant USB Type-C to Legacy Cable Assemblies 27
3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies 28
3.2 USB Type-C Connector Mating Interfaces 28
3.2.1 Interface Definition 28
3.2.2 Reference Designs 48
3.2.3 Pin Assignments and Descriptions 55
3.3 Cable Construction and Wire Assignments 56
3.3.1 Cable Construction (Informative) 56
3.3.2 Wire Assignments 58
3.3.3 Wire Gauges and Cable Diameters (Informative) 59

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved. Microchip Ex. 1019, p. 3
Microchip v. Aptiv
IPR2024-00496

3.4 Standard USB Type-C Cable Assemblies 61
3.4.1 USB Full-Featured Type-C Cable Assembly 61
3.4.2 USB 2.0 Type-C Cable Assembly 62
3.4.3 USB Type-C Captive Cable Assemblies 63
3.5 Legacy Cable Assemblies 63
3.5.1 USB Type-C to *USB 3.1* Standard-A Cable Assembly 64
3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly 65
3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly 66
3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly 67
3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly 68
3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly 69
3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly 70
3.6 Legacy Adapter Assemblies 70
3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly 71
3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly 72
3.7 Electrical Characteristics 74
3.7.1 Raw Cable (Informative) 74
3.7.2 USB Type-C to Type-C Passive Cable Assemblies (Normative) 75
3.7.3 Mated Connector (Informative) 88
3.7.4 USB Type-C to Legacy Cable Assemblies (Normative) 91
3.7.5 USB Type-C to USB Legacy Adapter Assemblies (Normative) 95
3.7.6 Shielding Effectiveness Requirements (Normative) 97
3.7.7 DC Electrical Requirements (Normative) 99
3.8 Mechanical and Environmental Requirements (Normative) 102
3.8.1 Mechanical Requirements 102
3.8.2 Environmental Requirements 108
3.9 Docking Applications (Informative) 109
3.10 Implementation Notes and Design Guides 110
3.10.1 EMC Management (Informative) 110
3.10.2 Stacked and Side-by-Side Connector Physical Spacing (Informative) 113
3.10.3 Cable Mating Considerations (Informative) 113
4 Functional 115
4.1 Signal Summary 115
4.2 Signal Pin Descriptions 115
4.2.1 SuperSpeed USB Pins 115
4.2.2 USB 2.0 Pins 116
4.2.3 Auxiliary Signal Pins 116
4.2.4 Power and Ground Pins 116
4.2.5 Configuration Pins 116
4.3 Sideband Use (SBU) 116
4.4 Power and Ground 116
4.4.1 IR Drop 116
4.4.2 VBUS 117

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.4.3 VCONN ... 118
4.5 Configuration Channel (CC) ... 120
4.5.1 Architectural Overview ... 120
4.5.2 CC Functional and Behavioral Requirements ... 133
4.5.3 USB Port Interoperability Behavior ... 155
4.6 Power ... 166
4.6.1 Power Requirements during USB Suspend ... 167
4.6.2 VBUS Power Provided Over a USB Type-C Cable ... 168
4.7 USB Hubs ... 171
4.8 Chargers ... 171
4.8.1 DFP as a Power Source ... 171
4.8.2 Non-USB Charging Methods ... 174
4.8.3 Sinking Host ... 174
4.8.4 Sourcing Device ... 174
4.8.5 Charging a System with a Dead Battery ... 174
4.9 Electronically Marked Cables ... 175
4.10 VCONN-Powered Accessories ... 176
4.11 Parameter Values ... 177
4.11.1 Termination Parameters ... 177
4.11.2 Timing Parameters ... 179
4.11.3 Voltage Parameters ... 181
5 Functional Extensions ... 183
5.1 Alternate Modes ... 183
5.1.1 Alternate Mode Architecture ... 183
5.1.2 Alternate Mode Requirements ... 183
5.1.3 Parameter Values ... 187
5.1.4 Example Alternate Mode – USB DisplayPort™ Dock ... 188
5.2 Managed Active Cables ... 190
5.2.1 Requirements for Managed Active Cables that respond to SOP' and SOP" ... 190
5.2.2 Cable Message Structure ... 192
5.2.3 Modal Cable Management ... 192
A Audio Adapter Accessory Mode ... 194
A.1. Overview ... 194
A.2. Detail ... 194
A.3. Electrical Requirements ... 195
A.4. Example Implementations ... 197
A.4.1. Passive 3.5 mm to USB Type-C Adapter – Single Pole Detection Switch ... 197
A.4.2. 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through ... 197
B Debug Accessory Mode ... 199
B.1. Overview ... 199
B.2. Functional ... 199

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

B.2.1. Signal Summary 200
B.2.2. Port Interoperability 200
B.2.3. Debug Accessory Mode Entry 200
B.2.4. Connection State Diagrams 201
B.2.5. DTS Port Interoperability Behavior 210
B.2.6. Orientation Detection 219
B.3. Security/Privacy Requirements: 220
C USB Type-C Digital Audio 221

FIGURES

Figure 2-1 USB Type-C Receptacle Interface (Front View) 20
Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View) 21
Figure 3-1 USB Type-C Receptacle Interface Dimensions 31
Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones 34
Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions 35
Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative) 38
Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right Angle Receptacle (Informative) 39
Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (Informative) 40
Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (Informative) 41
Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative) 42
Figure 3-9 *USB 2.0* Type-C Plug Interface Dimensions 44
Figure 3-10 USB Type-C Plug EMC Shielding Spring Tip Requirements 47
Figure 3-11 Reference Design of Receptacle Mid-Plate 48
Figure 3-12 Reference Design of the Retention Latch 49
Figure 3-13 Illustration of the Latch Soldered to the Paddle Card Ground 49
Figure 3-14 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring 50
Figure 3-15 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring 51
Figure 3-16 Reference Design of Internal EMC Pad 52
Figure 3-17 Reference Design of a USB Type-C Receptacle with External EMC Springs 53
Figure 3-18 Reference Design for a USB Full-Featured Type-C Plug Paddle Card 54
Figure 3-19 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN 57
Figure 3-20 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN 57
Figure 3-21 USB Full-Featured Type-C Standard Cable Assembly 61
Figure 3-22 USB Type-C to USB 3.1 Standard-A Cable Assembly 64
Figure 3-23 USB Type-C to *USB 2.0* Standard-A Cable Assembly 65
Figure 3-24 USB Type-C to *USB 3.1* Standard-B Cable Assembly 66
Figure 3-25 USB Type-C to *USB 2.0* Standard-B Cable Assembly 67
Figure 3-26 USB Type-C to *USB 2.0* Mini-B Cable Assembly 68
Figure 3-27 USB Type-C to *USB 3.1* Micro-B Cable Assembly 69
Figure 3-28 USB Type-C to *USB 2.0* Micro-B Cable Assembly 70
Figure 3-29 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly 71
Figure 3-30 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly 72
Figure 3-31 Illustration of Test Points for a Mated Cable Assembly 75
Figure 3-32 Recommended Differential Insertion Loss Requirement 76
Figure 3-33 Recommended Differential Return Loss Requirement 76
Figure 3-34 Recommended Differential Crosstalk Requirement 77

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-35 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D− Pair and USB SuperSpeed Pair 77
Figure 3-36 Illustration of Insertion Loss Fit at Nyquist Frequency 78
Figure 3-37 Input Pulse Spectrum 79
Figure 3-38 IMR Limit as Function of ILfitatNq 80
Figure 3-39 IRL Limit as Function of ILfitatNq 82
Figure 3-40 Differential-to-Common-Mode Conversion Requirement 82
Figure 3-41 Requirement for Differential Coupling between CC and D+/D− 83
Figure 3-42 Requirement for Single-Ended Coupling between CC and D− in USB 2.0 Type-C Cables 84
Figure 3-43 Requirement for Single-Ended Coupling between CC and D− in USB Full-Featured Type-C Cables 84
Figure 3-44 Requirement for Differential Coupling between VBUS and D+/D− 85
Figure 3-45 Requirement for Single-Ended Coupling between SBU_A and SBU_B 86
Figure 3-46 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC 86
Figure 3-47 Requirement for Coupling between SBU_A and differential D+/D−, and SBU_B and differential D+/D− 87
Figure 3-48 Illustration of USB Type-C Mated Connector 88
Figure 3-49 Recommended Impedance Limits of a USB Type-C Mated Connector 88
Figure 3-50 Recommended Ground Void Dimensions for USB Type-C Receptacle 89
Figure 3-51 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D− Pair and SuperSpeed Pairs 91
Figure 3-52 Recommended Limits for Differential-to-Common-Mode Conversion 91
Figure 3-53 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly 94
Figure 3-54 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly 94
Figure 3-55 Cable Assembly Shielding Effectiveness Testing 98
Figure 3-56 Shielding Effectiveness Pass/Fail Criteria 98
Figure 3-57 LLCR Measurement Diagram 99
Figure 3-58 Temperature Measurement Point 101
Figure 3-59 Example Current Rating Test Fixture Trace Configuration 102
Figure 3-60 Example of 4-Axis Continuity Test Fixture 104
Figure 3-61 Example Wrenching Strength Test Fixture for Plugs without Overmold 106
Figure 3-62 Reference Wrenching Strength Continuity Test Fixture 107
Figure 3-63 Example of Wrenching Strength Test Mechanical Failure Point 107
Figure 3-64 Wrenching Strength Test with Cable in Fixture 108
Figure 3-65 USB Type-C Cable Receptacle Flange Example 110
Figure 3-66 EMC Guidelines for Side Latch and Mid-plate 111
Figure 3-67 EMC Finger Connections to Plug Shell 111
Figure 3-68 EMC Pad Connections to Receptacle Shell 112
Figure 3-69 Examples of Connector Apertures 112
Figure 3-70 Recommended Minimum Spacing between Connectors 113
Figure 3-71 Recommended Minimum Plug Overmold Clearance 113
Figure 3-72 Cable Plug Overmold and an Angled Surface 114
Figure 4-1 Cable IR Drop 117
Figure 4-2 Cable IR Drop for powered cables 117
Figure 4-3 Logical Model for Data Bus Routing across USB Type-C-based Ports 121
Figure 4-4 Logical Model for USB Type-C-based Ports for the Direct Connect Device 121
Figure 4-5 Pull-Up/Pull-Down CC Model 123
Figure 4-6 Current Source/Pull-Down CC Model 123
Figure 4-7 Source Functional Model for CC1 and CC2 126
Figure 4-8 Source Functional Model Supporting USB PD PR_Swap 127
Figure 4-9 Sink Functional Model for CC1 and CC2 128
Figure 4-10 UFP Functional Model Supporting USB PD PR_Swap and VCONN_Swap 129
Figure 4-11 DRP Functional Model for CC1 and CC2 129
Figure 4-12 Connection State Diagram: Source 134
Figure 4-13 Connection State Diagram: Sink 135

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-14 Connection State Diagram: Sink with Accessory Support 136
Figure 4-15 Connection State Diagram: DRP 137
Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support 138
Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support 139
Figure 4-18 Sink Power Sub-States 152
Figure 4-19 Source to Sink Functional Model 155
Figure 4-20 Source to DRP Functional Model 156
Figure 4-21 DRP to Sink Functional Model 157
Figure 4-22 DRP to DRP Functional Model – CASE 1 158
Figure 4-23 DRP to DRP Functional Model – CASE 2 & 3 159
Figure 4-24 Source to Source Functional Model 161
Figure 4-25 Sink to Sink Functional Model 162
Figure 4-26 Source to Legacy Device Port Functional Model 163
Figure 4-27 Legacy Host Port to Sink Functional Model 164
Figure 4-28 DRP to Legacy Device Port Functional Model 165
Figure 4-29 Legacy Host Port to DRP Functional Model 166
Figure 4-30 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model 169
Figure 4-31 Sink Monitoring for Current in Current Source/Pull-Down CC Model 169
Figure 4-32 USB PD over CC Pins 170
Figure 4-33 USB PD BMC Signaling over CC 170
Figure 4-34 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging 172
Figure 4-35 0 – 3 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load 173
Figure 4-36 3 – 5 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load 173
Figure 4-37 Electronically Marked Cable with VCONN connected through the cable 175
Figure 4-38 Electronically Marked Cable with SOP' at both ends 176
Figure 4-39 DRP Timing 180
Figure 5-1 Pins Available for Reconfiguration over the Full-Featured Cable 184
Figure 5-2 Pins Available for Reconfiguration for Direct Connect Applications 184
Figure 5-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable 185
Figure 5-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device 186
Figure 5-5 USB DisplayPort Dock Example 188
Figure 5-6 Managed Active Cable Plug SOP' and SOP" Assignment 191
Figure 5-7 Managed Active Cable 192
Figure A-1 Example Passive 3.5 mm to USB Type-C Adapter 197
Figure A-2 Example 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through 198
Figure B-1 USB Type-C Debug Accessory Layered Behavior 199
Figure B-2 DTS Plug Interface 200
Figure B-3 Connection State Diagram: DTS Source 201
Figure B-4 Connection State Diagram: DTS Sink 202
Figure B-5 Connection State Diagram: DTS DRP 203
Figure B-6 TS Sink Power Sub-States 208

TABLES

Table 2-1 Summary of power supply options 25
Table 3-1 USB Type-C Standard Cable Assemblies 27
Table 3-2 USB Type-C Legacy Cable Assemblies 28
Table 3-3 USB Type-C Legacy Adapter Assemblies 28
Table 3-4 USB Type-C Receptacle Interface Pin Assignments 55
Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support 56
Table 3-6 USB Type-C Standard Cable Wire Assignments 58
Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters 59

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies....60
Table 3-9 Reference Wire Gauges for USB Type-C to Legacy Cable Assemblies....60
Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring....62
Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring....63
Table 3-12 USB Type-C to *USB 3.1* Standard-A Cable Assembly Wiring....64
Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring....65
Table 3-14 USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring....66
Table 3-15 USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring....67
Table 3-16 USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring....68
Table 3-17 USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring....69
Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring....70
Table 3-19 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Wiring....72
Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring....73
Table 3-21 Differential Insertion Loss Examples for USB SuperSpeed with Twisted Pair Construction 74
Table 3-22 Differential Insertion Loss Examples for USB SuperSpeed with Coaxial Construction....75
Table 3-23 Electrical Requirements for CC and SBU wires....83
Table 3-24 Coupling Matrix for Low Speed Signals....83
Table 3-24 USB D+/D− Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies....87
Table 3-25 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (Informative)....89
Table 3-26 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies....92
Table 3-27 Design Targets for USB Type-C to *USB 3.1* Gen 2 Legacy Cable Assemblies (Informative)93
Table 3-28 USB Type-C to *USB 3.1* Gen 2 Legacy Cable Assembly Signal Integrity Requirements (Normative)....93
Table 3-29 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (Normative)....95
Table 3-30 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (Informative) 96
Table 3-31 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (Normative)....97
Table 3-32 Current Rating Test PCB....101
Table 3-33 Force and Moment Requirements....105
Table 3-34 Environmental Test Conditions....108
Table 3-35 Reference Materials....109
Table 4-1 USB Type-C List of Signals....115
Table 4-2 VBUS Source Characteristics....118
Table 4-3 USB Type-C Source Port's VCONN Requirements Summary....118
Table 4-4 VCONN Source Characteristics....119
Table 4-5 VCONN Sink Characteristics....119
Table 4-6 USB Type-C-based Port Interoperability....122
Table 4-7 Source Perspective....124
Table 4-8 Source (Host) and Sink (Device) Behaviors by State....125
Table 4-9 USB PD Swapping Port Behavior Summary....131
Table 4-10 Power Role Behavioral Model Summary....132
Table 4-11 Source Port CC Pin State....140
Table 4-12 Sink Port CC Pin State....140
Table 4-13 Mandatory and Optional States....154
Table 4-14 Precedence of power source usage....167
Table 4-15 Source CC Termination (Rp) Requirements....177
Table 4-16 Sink CC Termination (Rd) Requirements....177
Table 4-17 Powered Cable Termination Requirements....177
Table 4-18 Sink CC Termination Requirements....178

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 4-19 SBU Termination Requirements 178
Table 4-20 VBUS and VCONN Timing Parameters 179
Table 4-21 DRP Timing Parameters 180
Table 4-22 CC Timing 181
Table 4-23 CC Voltages on Source Side – Default USB 181
Table 4-24 CC Voltages on Source Side – 1.5 A @ 5 V 181
Table 4-25 CC Voltages on Source Side – 3.0 A @ 5 V 182
Table 4-26 Voltage on Sink CC Pins (Default USB Type-C Current only) 182
Table 4-27 Voltage on Sink CC pins (Multiple Source Current Advertisements) 182
Table 5-1 USB Safe State Electrical Requirements 187
Table 5-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure 187
Table 5-3 Alternate Mode Signal Noise Ingression Requirements 187
Table 5-4 SOP' and SOP" Timing 192
Table A-1 USB Type-C Analog Audio Pin Assignments 195
Table A-2 USB Type-C Analog Audio Pin Electrical Parameter Ratings 196
Table B-1 DTS to TS Port Interoperability 200
Table B-2 Rp/Rp Charging Current Values for a DTS Source 208
Table B-3 Mandatory and Optional States 210

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Specification Work Group Chairs / Specification Editors

Intel Corporation (USB 3.0 Promoter company)	Yun Ling – Mechanical WG co-chair, Mechanical Chapter Co-editor Bob Dunstan – Functional WG co-chair, Specification Co-author Brad Saunders – Plenary/Functional WG chair, Specification Co-author
Seagate	Alvin Cox, Mechanical WG co-chair, Mechanical Chapter Co-editor

Specification Work Group Contributors

Advanced-Connectek, Inc. (ACON)	Glen Chandler	Vicky Chuang	Alan Tsai
	Jeff Chien	Aven Kao	Stephen Yang
	Lee (Dick Lee) Ching	Danny Liao	
	Conrad Choy	Alan MacDougall	
Advanced Micro Devices	Steve Capezza	Walter Fry	Will Harris
Agilent Technologies, Inc.	James Choate		
Analogix Semiconductor, Inc.	Mehran Badii	Greg Stewart	
Apple	Mahmoud Amini	Zheng Gao	Keith Porthouse
	Sree Anantharaman	Girault Jones	Sascha Tietz
	Paul Baker	Keong Kam	Jennifer Tsai
	Jason Chung	Min Kim	Colin Whitby-Strevens
	David Conroy	Chris Ligtenberg	Dennis Yarak
	Bill Cornelius	Nathan Ng	
	William Ferry	James Orr	
Cypress Semiconductor	Mark Fu	Anup Nayak	Sanjay Sancheti
	Rushil Kadakia	Jagadeesan Raj	Subu Sankaran
Dell	Mohammed Hijazi	Sean O'Neal	Thomas Voor
	David Meyers	Ernesto Ramirez	
DisplayLink (UK) Ltd.	Pete Burgers	Richard Petrie	
Electronics Testing Center, Taiwan	Sophia Liu		
Foxconn	Asroc Chen	Chien-Ping Kao	Pei Tsao
	Allen Cheng	Ji Li	AJ Yang
	Jason Chou	Ann Liu	Yuan Zhang
	Edmond Choy	Terry Little	Jessica Zheng
	Bob Hall	Steve Sedio	Andy Yao
Foxlink/Cheng Uei Precision Industry Co., Ltd.	Robert Chen	Armando Lee	Steve Tsai
	Sunny Chou	Dennis Lee	Wen Yang
	Carrie Chuang	Justin Lin	Wiley Yang
	Wen-Chuan Hsu	Tse Wu Ting	Junjie Yu
	Alex Hsue		
Google	Joshua Boilard	Mark Hayter	Adam Rodriguez
	Alec Berg	Nithya Jagannathan	David Schneider
	Todd Broch	Lawrence Lam	Ken Wu
	Jim Guerin	Ingrid Lin	
	Jeffrey Hayashida	Richard Palatin	
Granite River Labs	Mike Engbretson	Johnson Tan	
Hewlett Packard (USB 3.0 Promoter company)	Alan Berkema	Michael Krause	Linden McClure
	Robin Castell	Jim Mann	Mike Pescetto

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Hirose Electric Co., Ltd.	Jeremy Buan William MacKillop	Gourgen Oganessyan	Sid Tono
Intel Corporation (USB 3.0 Promoter company)	Dave Ackelson Mike Bell Kuan-Yu Chen Hengju Cheng Bob Dunstan Paul Durley Howard Heck Hao-Han Hsu Abdul (Rahman) Ismail	James Jaussi Luke Johnson Jerzy Kolinski Rolf Kuhnis Christine Krause Henrik Leegaard Yun Ling Xiang Li Guobin Liu Steve McGowan	Sankaran Menon Chee Lim Nge Sridharan Ranganathan Brad Saunders Amit Srivastava Ron Swartz Karthi Vadivelu Rafal Wielicki
Japan Aviation Electronics Industry Ltd. (JAE)	Kenji Hagiwara Masaki Kimura Toshio Masumoto Joe Motojima Ron Muir Tadashi Okubo Kazuhiro Saito	Kimiaki Saito Yuichi Saito Mark Saubert Toshio Shimoyama Tatsuya Shioda Atsuo Tago Masaaki Takaku	Jussi Takaneva Tomohiko Tamada Kentaro Toda Kouhei Ueda Takakazu Usami Masahide Watanabe Youhei Yokoyama
JPC/Main Super Inc.	Sam Tseng	Ray Yang	
LeCroy Corporation	Daniel H. Jacobs		
Lenovo	Rob Bowser Tomoki Harada	Wei Liu	Howard Locker
Lotes Co., Ltd.	Ariel Delos Reyes Ernest Han Mark Ho	Regina Liu-Hwang Max Lo Charles Kaun	JinYi Tu Jason Yang
LSI Corporation	Dave Thompson		
Luxshare-ICT	Josue Castillo Daniel Chen Lisen Chen	CY Hsu Alan Kinningham John Lin	Stone Lin Pat Young
MegaChips Corporation	Alan Kobayashi		
Microchip (SMSC)	Josh Averyt Mark Bohm	Donald Perkins	Mohammed Rahman
Microsoft Corporation (USB 3.0 Promoter company)	Randy Aull Fred Bhesania Anthony Chen Marty Evans Vivek Gupta Robbie Harris	Robert Hollyer Kai Inha Jayson Kastens Andrea Keating Eric Lee	Ivan McCracken Toby Nixon Gene Obie Srivatsan Ravindran David Voth
MQP Electronics Ltd.	Sten Carlsen	Pat Crowe	
Nokia Corporation	Daniel Gratiot Pekka Leinonen	Samuli Makinen Pekka Talmola	Timo Toivola Panu Ylihaavisto
NXP Semiconductors	Vijendra Kuroodi	Guru Prasad	
Renesas Electronics Corp. (USB 3.0 Promoter company)	Nobuo Furuya	Philip Leung	Kiichi Muto

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Rohm Co., Ltd.	Mark Aaldering Kris Bahar Yusuke Kondo	Arun Kumar Chris Lin	Takashi Sato Hiroshi Yoshimura
Samsung Electronics Co., Ltd.	Soondo Kim Woonki Kim	Jagoun Koo Cheolho Lee	Jun Bum Lee
Seagate	Alvin Cox Tony Priborsky	Tom Skaar	Dan Smith
STMicroelectronics (USB 3.0 Promoter company)	Nathalie Ballot Nicolas Florenchie Joel Huloux	Christophe Lorin Patrizia Milazzo	Federico Musarra Pascal Legrand
Tektronics, Inc.	Randy White		
Texas Instruments (USB 3.0 Promoter company)	Jawaid Ahmad Richard Hubbard Scott Jackson Yoon Lee Grant Ley	Win Maung Lauren Moore Martin Patoka Brian Quach Wes Ray	Anwar Sadat Sue Vining Deric Waters
Tyco Electronics Corp. (TE Connectivity Ltd.)	Max Chao Robert E. Cid Kengo Ijiro Eiji Ikematsu Joan Leu Clark Li Mike Lockyer	Jim McGrath Takeshi Nakashima Luis A. Navarro Masako Saito Yoshiaki Sakuma Gavin Shih Hiroshi Shirai	Scott Shuey Hidenori Taguchi Bernard Vetten Ryan Yu Sjoerd Zwartkruis
VIA Technologies Inc.	Terrance Shih	Jay Tseng	Fong-Jim Wang

Pre-Release Draft Industry Reviewing Companies That Provided Feedback

Aces
Allion Labs, Inc.
BizLink International Corp.
Corning Optical Communications LLC
Cypress Semiconductor
Etron Technology Inc.
Fairchild Semiconductor
Fujitsu Ltd.
Industrial Technology Research Institute (ITRI)
Joinsoon Electronics Mfg. Co. Ltd.
JST Mfg. Co., Ltd.
Korea Electric Terminal
Marvell Semiconductor
Motorola Mobility LLC
NEC
Newnex Technology Corp.
NXP Semiconductors
PalCONN/PalNova (Palpilot International Corp.)
Parade Technology
Pericom
Qualcomm
Semtech Corporation
Shenzhen Deren Electronic Co., Ltd.
Silicon Image
Simula Technology Corp.
SMK Corporation
Sony Corporation
Sumitomo Electric Industries
Toshiba Corporation

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Revision History

Revision	Date	Description
1.0	August 11, 2014	Initial Release
1.1	April 3, 2015	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.2	March 25, 2016	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

1 Introduction

With the continued success of the USB interface, there exists a need to adapt USB technology to serve newer computing platforms and devices as they trend toward smaller, thinner and lighter form-factors. Many of these newer platforms and devices are reaching a point where existing USB receptacles and plugs are inhibiting innovation, especially given the relatively large size and internal volume constraints of the Standard-A and Standard-B versions of USB connectors. Additionally, as platform usage models have evolved, usability and robustness requirements have advanced and the existing set of USB connectors were not originally designed for some of these newer requirements. This specification is to establish a new USB connector ecosystem that addresses the evolving needs of platforms and devices while retaining all of the functional benefits of USB that form the basis for this most popular of computing device interconnects.

1.1 Purpose

This specification defines the USB Type-C™ receptacles, plug and cables.

The USB Type-C Cable and Connector Specification is guided by the following principles:

- Enable new and exciting host and device form-factors where size, industrial design and style are important parameters
- Work seamlessly with existing USB host and device silicon solutions
- Enhance ease of use for connecting USB devices with a focus on minimizing user confusion for plug and cable orientation

The USB Type-C Cable and Connector Specification defines a new receptacle, plug, cable and detection mechanisms that are compatible with existing USB interface electrical and functional specifications. This specification covers the following aspects that are needed to produce and use this new USB cable/connector solution in newer platforms and devices, and that interoperate with existing platforms and devices:

- USB Type-C receptacles, including electro-mechanical definition and performance requirements
- USB Type-C plugs and cable assemblies, including electro-mechanical definition and performance requirements
- USB Type-C to legacy cable assemblies and adapters
- USB Type-C-based device detection and interface configuration, including support for legacy connections
- USB Power Delivery optimized for the USB Type-C connector

The USB Type-C Cable and Connector Specification defines a standardized mechanism that supports Alternate Modes, such as repurposing the connector for docking-specific applications.

1.2 Scope

This specification is intended as a supplement to the existing *USB 2.0*, *USB 3.1* and *USB Power Delivery* specifications. It addresses only the elements required to implement and support the USB Type-C receptacles, plugs and cables.

Normative information is provided to allow interoperability of components designed to this specification. Informative information, when provided, may illustrate possible design implementations.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

1.3 Related Documents

USB 2.0 *Universal Serial Bus Revision 2.0 Specification*
This includes the entire document release package.
http://www.usb.org/developers/docs

USB 3.1 *Universal Serial Bus Revision 3.1 Specification*
This includes the entire document release package.
http://www.usb.org/developers/docs

USB PD *USB Power Delivery Specification, Revision 2.0, Version 1.2, March 25, 2016*
USB Power Delivery Specification, Revision 3.0, Version 1.0a, March 25, 2016
http://www.usb.org/developers/docs

USB BB *USB Billboard Device Class Specification, Revision 1.0, August 11, 2014*
http://www.usb.org/developers/docs

USB BC *Battery Charging Specification, Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012*
http://www.usb.org/developers/docs

1.4 Conventions

1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

1.4.2 Keywords

The following keywords differentiate between the levels of requirements and options.

1.4.2.1 Informative

Informative is a keyword that describes information with this specification that intends to discuss and clarify requirements and features as opposed to mandating them.

1.4.2.2 May

May is a keyword that indicates a choice with no implied preference.

1.4.2.3 N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and shall not be checked or used by the recipient.

1.4.2.4 Normative

Normative is a keyword that describes features that are mandated by this specification.

1.4.2.5 Optional

Optional is a keyword that describes features not mandated by this specification. However, if an optional feature is implemented, the feature shall be implemented as defined by this specification (optional normative).

1.4.2.6 Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this specification and, unless otherwise stated, shall not be utilized or adapted by vendor implementation. A reserved bit, byte, word, or field shall be set to zero by the

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

sender and shall be ignored by the receiver. Reserved field values shall not be sent by the sender and, if received, shall be ignored by the receiver.

1.4.2.7 Shall

Shall is a keyword indicating a mandatory (normative) requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant Devices.

1.4.2.8 Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase "it is recommended that".

1.4.3 Numbering

Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase "B" are byte values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values. Numbers not immediately followed by either a "b", "B", or "h" are decimal values.

1.5 Terms and Abbreviations

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of Rd/Rd or Ra/Ra on CC1/CC2, respectively.
Active cable	An Electronically Marked Cable with additional electronics to condition the data path signals.
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the USB-IF. Entry and exit into and from an Alternate Mode is controlled by the *USB PD* Structured VDM Enter Mode and Exit Mode commands.
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of Ra/Ra on CC1/CC2, respectively. See Appendix A.
BFSK	Binary Frequency Shift Keying used for *USB PD* communication over VBUS.
BMC	Biphase Mark Coding used for *USB PD* communication over the CC wire.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.
CC	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Debug Accessory Mode (DAM)	The Accessory Mode defined by the presence of Rd/Rd or Rp/Rp on CC1/CC2, respectively. See Appendix B.
Debug and Test System (DTS)	The combined hardware and software system that provides a system developer debug visibility and control when connected to a Target System in Debug Accessory Mode.
Default VBUS	VBUS voltage as defined by the *USB 2.0* and *USB 3.1* specifications. Note: where used, 5 V connotes the same meaning.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Term	Description
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect	The host's DFP is connected directly with no USB hub in between, either via a cable or without (e.g., thumb drive), to the device's UFP.
DRD (Dual-Role-Data)	The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role may be changed dynamically using *USB PD* Data Role Swap.
DRP (Dual-Role-Power)	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers may be fixed to either a Source or Sink or may alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role may be changed dynamically using *USB PD* Power Role Swap.
DR_Swap	*USB PD* Data Role Swap.
Electronically Marked Cable	A USB Type-C cable that uses *USB PD* to provide the cable's characteristics.
eMarker	The element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable may or may not be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of Ra between the VCONN pin and ground.
PR_Swap	*USB PD* Power Role Swap.
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.
SBU	Sideband Use.
SID	A Standard ID (SID) is a unique 16-bit value assigned by the USB-IF to identify an industry standard.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Term	Description
Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
Source	Port asserting Rp on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.
SVID	General reference to either a SID or a VID. Used by *USB PD* Structured VDMs when requesting SIDs and VIDs from a device.
Target System (TS)	The system being debugged in Debug Accessory Mode.
Type-A	A general reference to all versions of USB "A" plugs and receptacles.
Type-B	A general reference to all versions of USB "B" plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports USB 2.0 data operation. This cable does not include USB 3.1 or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the USB 2.0 Type-C cable.
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports USB 2.0 and USB 3.1 data operation. This cable includes SBU wires.
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
VCONN-powered accessory	An accessory that is powered from VCONN to operate in an Alternate Mode.
VCONN_Swap	*USB PD* VCONN Swap.
VDM	Vendor Defined Message as defined by the *USB PD* specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the USB-IF to identify a vendor.
vSafe0V	VBUS "0 volts" as defined by the *USB PD* specification.
vSafe5V	VBUS "5 volts" as defined by the *USB PD* specification.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

2 Overview

2.1 Introduction

The USB Type-C™ receptacle, plug and cable provide a smaller, thinner and more robust alternative to existing *USB 3.1* interconnect (Standard and Micro USB cables and connectors). This new solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices

While the USB Type-C interconnect no longer physically differentiates plugs on a cable by being an A-type or B-type, the USB interface still maintains such a host-to-device logical relationship. Determination of this host-to-device relationship is accomplished through a Configuration Channel (CC) that is connected through the cable. In addition, the Configuration Channel is used to set up and manage power and Alternate/Accessory Modes.

Using the Configuration Channel, the USB Type-C interconnect defines a simplified 5 volt VBUS-based power delivery and charging solution that supplements what is already defined in the *USB 3.1 Specification*. More advanced power delivery and battery charging features over the USB Type-C interconnect are based on the *USB Power Delivery Specification*. As a product implementation improvement, the USB Type-C interconnect shifts the *USB PD* communication protocol from being communicated over VBUS to being delivered across the USB Type-C Configuration Channel.

The USB Type-C receptacle, plug and cable designs are intended to support future USB functional extensions. As such, consideration was given to frequency scaling performance, pin-out arrangement and the configuration mechanisms when developing this solution. The definition of future USB functional extensions is not in the scope of this specification but rather will be provided in future releases of the base USB Specification, i.e., beyond the existing *USB 3.1 Specification*.

Figure 2-1 illustrates the comprehensive functional signal plan for the USB Type-C receptacle, not all signals shown are required in all platforms or devices. As shown, the receptacle signal list functionally delivers both *USB 2.0* (D+ and D−) and *USB 3.1* (TX and RX pairs) data buses, USB power (VBUS) and ground (GND), Configuration Channel signals (CC1 and CC2), and two Sideband Use (SBU) signal pins. Multiple sets of USB data bus signal locations in this layout facilitate being able to functionally map the USB signals independent of plug orientation in the receptacle. For reference, the signal pins are labeled.

Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 2-2 illustrates the comprehensive functional signal plan for the USB Type-C plug. Only one CC pin is connected through the cable to establish signal orientation and the other CC pin is repurposed as VCONN for powering electronics in the USB Type-C plug. Also, only one set of *USB 2.0* D+/D− wires are implemented in a USB Type-C cable. For USB Type-C cables that only intend to support *USB 2.0* functionality, the *USB 3.1* and SBU signals are not implemented.

Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View)

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

2.2 USB Type-C Receptacles, Plugs and Cables

Cables and connectors, including USB Type-C to USB legacy cables and adapters, are explicitly defined within this specification. These are the only connectors and cables that are authorized by the licensing terms of this specification. All licensed cables and connectors are required to comply with the compliance and certification requirements that are developed and maintained by the USB-IF.

The following USB Type-C receptacles and plugs are defined.

- USB Type-C receptacle for *USB 2.0*, *USB 3.1* and full-featured platforms and devices
- USB Full-Featured Type-C plug
- *USB 2.0* Type-C plug

The following USB Type-C cables are defined.

- USB Full-Featured Type-C cable with a USB Full-Featured Type-C plug at both ends for *USB 3.1* and full-featured applications
- *USB 2.0* Type-C cable with a *USB 2.0* Type-C plug at both ends for *USB 2.0* applications
- Captive cable with either a USB Full-Featured Type-C plug or *USB 2.0* Type-C plug at one end

All of the defined USB Type-C receptacles, plugs and cables support USB charging applications, including support for the optional USB Type-C-specific implementation of the *USB Power Delivery Specification* (See Section 4.6.2.4).

All USB Full-Featured Type-C cables are electronically marked. *USB 2.0* Type-C cables may be electronically marked. See Section 4.9 for the requirements of Electronically Marked Cables.

The following USB Type-C to USB legacy cables and adapters are defined.

- *USB 3.1* Type-C to Legacy Host cable with a USB Full-Featured Type-C plug at one end and a *USB 3.1* Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB host*

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- *USB 2.0* Type-C to Legacy Host cable with a *USB 2.0* Type-C plug at one end and a *USB 2.0* Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB 2.0 host (primarily for mobile charging and sync applications)*
- *USB 3.1* Type-C to Legacy Device cable with a USB Full-Featured Type-C plug at one end and a *USB 3.1* Standard-B plug at the other end – *this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host*
- *USB 2.0* Type-C to Legacy Device cable with a *USB 2.0* Type-C plug at one end and a *USB 2.0* Standard-B plug at the other end – *this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host*
- *USB 2.0* Type-C to Legacy Mini Device cable with a *USB 2.0* Type-C plug at one end and a *USB 2.0* Mini-B plug at the other end – *this cable supports use of legacy devices with a USB 2.0 Type-C-based host*
- *USB 3.1* Type-C to Legacy Micro Device cable with a USB Full-Featured Type-C plug at one end and a *USB 3.1* Micro-B plug at the other end – *this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host*
- *USB 2.0* Type-C to Legacy Micro Device cable with a *USB 2.0* Type-C plug at one end and a *USB 2.0* Micro-B plug at the other end – *this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host*
- *USB 3.1* Type-C to Legacy Standard-A adapter with a USB Full-Featured Type-C plug at one end and a *USB 3.1* Standard-A receptacle at the other end – *this adapter supports use of a legacy USB "thumb drive" style device or a legacy USB ThinCard device with a USB 3.1 Type-C-based host*
- *USB 2.0* Type-C to Legacy Micro-B adapter with a *USB 2.0* Type-C plug at one end and a *USB 2.0* Micro-B receptacle at the other end – *this adapter supports charging a USB Type-C-based mobile device using a legacy USB Micro-B-based chargers, either captive cable-based or used in conjunction with a legacy USB 2.0 Standard-A to Micro-B cable*

USB Type-C receptacle to USB legacy adapters are explicitly not defined or allowed. Such adapters would allow many invalid and potentially unsafe cable connections to be constructed by users.

2.3 Configuration Process

The USB Type-C receptacle, plug and cable solution incorporates a configuration process to detect a downstream facing port to upstream facing port (Source-to-Sink) connection for VBUS management and host-to-device connected relationship determination.

The configuration process is used for the following:

- Source-to-Sink attach/detach detection
- Plug orientation/cable twist detection
- Initial power (Source-to-Sink) detection and establishing the data (Host-to-Device) relationship
- USB Type-C VBUS current detection and usage
- *USB PD* communication
- Discovery and configuration of functional extensions

Two pins on the USB Type-C receptacle, CC1 and CC2, are used for this purpose. Within a standard USB Type-C cable, only a single CC pin position within each plug of the cable is connected through the cable.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

2.3.1 Source-to-Sink Attach/Detach Detection

Initially, Source-to-Sink attach is detected by a host or hub port (Source) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, Source-to-Sink detach is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer terminated to GND.

Power is not applied to the USB Type-C host or hub receptacle (V_{BUS} or V_{CONN}) until the Source detects the presence of an attached device (Sink) port. When a Source-to-Sink attach is detected, the Source is expected to enable power to the receptacle and proceed to normal USB operation with the attached device. When a Source-to-Sink detach is detected, the port sourcing V_{BUS} removes power.

2.3.2 Plug Orientation/Cable Twist Detection

The USB Type-C plug can be inserted into a receptacle in either one of two orientations, therefore the CC pins enable a method for detecting plug orientation in order to determine which SuperSpeed USB data signal pairs are functionally connected through the cable. This allows for signal routing, if needed, within a host or device to be established for a successful connection.

2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship

Unlike existing USB Type-A and USB Type-B receptacles and plugs, the mechanical characteristics of the USB Type-C receptacle and plug do not inherently establish the relationship of USB host and device ports. The CC pins on the receptacle also serve to establish an initial power (Source-to-Sink) and data (Host-to-Device) relationships prior to the normal USB enumeration process.

For the purpose of defining how the CC pins are used to establish the initial power relationship, the following port power behavior modes are defined.

1. Source-only – for this mode, the port exclusively behaves as a Source
2. Sink-only – for this mode, the port exclusively behaves as a Sink
3. Dual-Role-Power (DRP) – for this mode, the port can behave either as a Source or Sink

Additionally, when a port supports USB data operation, a port's data behavior modes are defined.

1. DFP-only – for this mode, the port exclusively behaves as a DFP
2. UFP-only – for this mode, the port exclusively behaves as a UFP
3. Dual-Role-Data (DRD) – for this mode, the port can behave either as a DFP or UFP

The DFP-only and UFP-only ports behaviorally map to traditional USB host ports and USB device ports, respectively but may not necessarily do USB data communication. When a host-only port is attached to a device-only port, the behavior from the user's perspective follows the traditional USB host-to-device port model. However, the USB Type-C connector solution does not physically prevent host-to-host or device-to-device connections. In this case, the resulting host-to-host or device-to-device connection results in a safe but non-functional situation.

Once initially established, the Source supplies V_{BUS} and behaves as a DFP, and the Sink consumes V_{BUS} and behaves as a UFP. *USB PD*, when supported by both ports, may then be used to independently swap both the power and data roles of the ports.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

A port that supports dual-role operation by being able to shift to the appropriate connected mode when attached to either a Source-only or Sink-only port is a DRP. In the special case of a DRP being attached to another DRP, an initialization protocol across the CC pins is used to establish the initial host-to-device relationship. Given no role-swapping intervention, the determination of which is DFP or UFP is random from the user's perspective.

Two independent set of mechanisms are defined to allow a USB Type-C DRP to functionally swap power and data roles. When *USB PD* is supported, power and data role swapping is performed as a subsequent step following the initial connection process. For non-PD implementations, power/data role swapping can optionally be dealt with as part of the initial connection process. To improve the user's experience when connecting devices that are of categorically different types, products may be implemented to strongly prefer being a DFP or a UFP, such that the DFP/UFP determination becomes predictable when connecting two DRPs of differing categories. See Section 4.5.1.4 for more on available swapping mechanisms.

As an alternative to role swapping, a USB Type-C DRP may provide useful functionality by when operating as a host, exposing a CDC/network (preferably TCP/IP) stack or when operating as a device, exposing a CDC/network interface.

USB hubs have two types of ports, a UFP that is connected up to a DFP (host or another hub) that initially functions as a Sink, and one or more DFPs for connecting other devices that initially function as Sources.

2.3.4 USB Type-C VBUS Current Detection and Usage

With the USB Type-C connector solution, a Source (host or downstream hub port) may implement higher source current over VBUS to enable faster charging of mobile devices or powering devices that require more current than is specified in the *USB 3.1 Specification*. All USB host and hub ports advertise via the CC pins the level of current that is presently available. The USB device port is required to manage its load to stay within the current level offered by the host or hub, including dynamically scaling back the load if the host or hub port changes its advertisement to a lower level as indicated over the CC pins.

Three current levels at default VBUS are defined by USB Type-C Current:

- Default values as defined by a USB Specification
  (500 mA for USB 2.0 ports, 900 mA for USB 3.1 ports)
- 1.5 A
- 3.0 A

The higher USB Type-C Current levels that can be advertised allows hosts and devices that do not implement *USB PD* to take advantage of higher charging current.

2.3.5 USB PD Communication

USB Power Delivery is a feature on products (hosts, hubs and devices). *USB PD* communications is used to:

- Establish power contracts that allow voltage and current outside that defined by the *USB 2.0* and *USB 3.1* specifications.
- Change the port sourcing VBUS.
- Change the port sourcing VCONN.
- Swap DFP and UFP roles.
- Communicate with cables.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The *USB PD* Bi-phase Mark Coded (BMC) communications are carried on the CC wire of the USB Type-C cable.

2.3.6 Functional Extensions

Functional extensions (see Chapter 5) are enabled via a communications channel across CC using methods defined by the *USB Power Delivery Specification*.

2.4 VBUS

VBUS provides a path to deliver power between a host and a device, and between a USB power charger and a host/device. A simplified high-current supply capability is defined for hosts and chargers that optionally support current levels beyond the *USB 2.0* and *USB 3.1* specifications. The *USB Power Delivery Specification* is supported.

Table 2-1 summarizes the power supply options available from the perspective of a device with the USB Type-C connector. Not all options will be available to the device from all host or hub ports – only the first two listed options are mandated by the base USB specifications and form the basis of USB Type-C Current at the Default USB Power level.

Table 2-1 Summary of power supply options

Mode of Operation	Nominal Voltage	Maximum Current	Notes
USB 2.0	5 V	See *USB 2.0*	
USB 3.1	5 V	See *USB 3.1*	
USB BC 1.2	5 V	Up to 1.5 A[1]	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 20 V	Configurable up to 5 A	Directional control and power level management

Notes:

1. *USB BC 1.2* permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A. If the *USB BC 1.2* power provider does not support 1.5 A, then it is required to follow power droop requirements. A *USB BC 1.2* power consumer may consume up to 1.5 A provided that the voltage does not drop below 2 V, which may occur at any level of power above 0.5 A.

The USB Type-C receptacle is specified for current capability of 5 A whereas standard USB Type-C cable assemblies are rated for 3 A. The higher rating of the receptacle enables systems to deliver more power over directly attached docking solutions or using appropriately designed chargers with captive cables when implementing *USB PD*. Also, USB Type-C cable assemblies designed for *USB PD* and appropriately identified via electronic marking are allowed to support up to 5 A.

2.5 VCONN

Once the connection between host and device is established, the CC pin (CC1 or CC2) in the receptacle that is not connected via the CC wire through the standard cable is repurposed to source VCONN to power circuits in the plug needed to implement Electronically Marked

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Cables (see Section 4.9). Initially, the source supplies VCONN and the source of VCONN may be swapped using *USB PD* VCONN_Swap.

Electronically marked cables may use VBUS instead of VCONN as VBUS is available across the cable. VCONN functionally differs from VBUS in that it is isolated from the other end of the cable. VCONN is independent of VBUS and, unlike VBUS which can use *USB PD* to support higher voltages, VCONN voltage is fixed at 5 V.

2.6 Hubs

USB hubs implemented with USB Type-C receptacles are required to clearly identify the upstream facing port. This requirement is needed because a user can no longer know which port on a hub is the upstream facing port and which ports are the downstream facing ports by the type of receptacles that are exposed, i.e., USB Type-B is the upstream facing port and USB Type-A is a downstream facing port.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3 Mechanical

3.1 Overview

3.1.1 Compliant Connectors

The USB Type-C™ specification defines the following standard connectors:

- USB Type-C receptacle
- USB Full-Featured Type-C plug
- USB 2.0 Type-C plug

3.1.2 Compliant Cable Assemblies

Table 3-1 summarizes the USB Type-C standard cable assemblies along with the primary differentiating characteristics. All USB Full-Featured Type-C cables shall support simultaneous, independent signal transmission on both *USB 3.1* (TX and RX pairs) data buses. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. All cables that are either full-featured and/or are rated at more than 3 A current are Electronically Marked Cables.

Table 3-1 USB Type-C Standard Cable Assemblies

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length	Current Rating	USB Power Delivery (BMC)	USB Type-C Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3 A	Supported	Optional
CC2-5					5 A		Required
CC3G1-3	C	C	USB 3.1 Gen1	≤ 2 m	3 A	Supported	Required
CC3G1-5					5 A		
CC3G2-3	C	C	USB 3.1 Gen2	≤ 1 m	3 A	Supported	Required
CC3G2-5					5 A		

USB Type-C products are also allowed to have a captive cable. See Section 3.4.3.

3.1.3 Compliant USB Type-C to Legacy Cable Assemblies

Table 3-2 summarizes the USB Type-C legacy cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. *USB 3.1* Type-C legacy cables assemblies that only offer performance up to *USB 3.1* Gen1 are not allowed by this specification.

For USB Type-C legacy cable assemblies that incorporate Rp termination, the value of this termination is required to be specified to the Default setting of USB Type-C Current even though the cable assemblies are rated for 3 A. The Rp termination in these cables is intended to represent the maximum current of a compliant legacy USB host port, not the current rating of the cable itself. The cable current rating is intentionally set to a higher level given that there are numerous non-standard power chargers that offer more than the Default levels established by the *USB 2.0* and *USB 3.1* specifications.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-2 USB Type-C Legacy Cable Assemblies

Cable Ref	Plug 1[4]	Plug 2[4]	USB Version	Cable Length	Current Rating
AC2-3	USB 2.0 Standard-A	USB 2.0 Type-C[1]	USB 2.0	≤ 4 m	3 A
AC3G2-3	USB 3.1 Standard-A	USB Full-Featured Type-C[1]	USB 3.1 Gen2	≤ 1 m	3 A
CB2-3	USB 2.0 Type-C[2]	USB 2.0 Standard-B	USB 2.0	≤ 4 m	3 A
CB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-B	USB 3.1 Gen2	≤ 1 m	3 A
CmB2	USB 2.0 Type-C[2]	USB 2.0 Mini-B	USB 2.0	≤ 4 m	500 mA
CμB2-3	USB 2.0 Type-C[2]	USB 2.0 Micro-B	USB 2.0	≤ 2 m	3 A
CμB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Micro-B	USB 3.1 Gen2	≤ 1 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter cable are required to have Rp (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter cable are required to have Rd (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.4.3 for the mated resistance and temperature rise required for the legacy plugs.

3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies

Table 3-3 summarizes the USB Type-C legacy adapter assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements.

Table 3-3 USB Type-C Legacy Adapter Assemblies

Adapter Ref	Plug	Receptacle[3]	USB Version	Cable Length	Current Rating
CμBR2-3	USB 2.0 Type-C[1]	USB 2.0 Micro-B	USB 2.0	≤ 0.15 m	3 A
CAR3G1-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-A	USB 3.1 Gen1	≤ 0.15 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter are required to have Rp (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter are required to have Rd (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.5.3 for the mated resistance and temperature rise required for the legacy receptacles.

3.2 USB Type-C Connector Mating Interfaces

This section defines the connector mating interfaces, including the connector interface drawings, pin assignments, and descriptions. All dimensions in figures are in millimeters

3.2.1 Interface Definition

Figure 3-1 and Figure 3-3 show, respectively, the USB Type-C receptacle and USB Full-Featured Type-C plug interface dimensions.

Figure 3-9 shows the *USB 2.0* Type-C plug interface dimensions. The dimensions that govern the mating interoperability are specified. All the REF dimensions are provided for reference only, not hard requirements.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Key features, configuration options, and design areas that need attention:

1. Figure 3-1 shows a vertical-mount receptacle. Other PCB mounting types such as right-angle mount and mid-mount are allowed.
2. A mid-plate is required between the top and bottom signals inside the receptacle tongue to manage crosstalk in full-featured applications. The mid-plate shall be connected to the PCB ground with at least two grounding points. A reference design of the mid-plate is provided in Section 3.2.2.1.
3. Retention of the cable assembly in the receptacle is achieved by the side-latches in the plug and features on the sides of the receptacle tongue. Side latches are required for all plugs except plugs used for docking with no cable attached. Side latches shall be connected to ground inside the plug. A reference design of the side latches is provided in Section 3.2.2.2 along with its grounding scheme. Docking applications may not have side latches, requiring special consideration regarding EMC (Electromagnetic Compatibility).
4. The EMC shielding springs are required inside the cable plug. The shielding spring shall be connected to the plug shell. No EMC shielding spring finger tip of the USB Full-Featured Type-C plug or USB 2.0 Type-C plug shall be exposed in the plug housing opening of the unmated USB Type-C plug (see Figure 3-10). Section 3.2.2.3 shows reference designs of the EMC spring.
5. Shorting of any signal or power contact spring to the plug metal shell is not allowed. The spring in the deflected state should not touch the plug shell. An isolation layer (e.g., Kapton tape placed on the plug shell) is recommended to prevent accidental shorting due to plug shell deformation.
6. The USB Type-C receptacle shall provide an EMC ground return path through one of the following options:
   - Fingers in the receptacle outer shell
   - Internal EMC pads
   - Both external fingers in the shell and internal EMC pads

   If fingers in the receptacle outer shell are used, then the receptacle springs shall contact the mated plug within the zones defined in Figure 3-2. A minimum of four separate contact points are required. Additional fingers and points of contact are allowed. See Section 3.2.2.4 for a reference design of receptacle outer shell fingers.

   If internal EMC pads are present in the receptacle, then they shall comply with the requirements defined in Figure 3-1. The shielding pads shall be connected to the receptacle shell. If no receptacle shell is present, then the receptacle shall provide a means to connect the shielding pad to ground. See Section 3.2.2.3 for a reference design of the shielding pad and ground connection.
7. This specification defines the USB Type-C receptacle shell length of 6.20 mm as a reference dimension. The USB Type-C receptacle is designed to have shell length of 6.20 ± 0.20 mm to provide proper mechanical and electrical mating of the plug to the receptacle (e.g., full seating of the plug in the receptacle and protection of the receptacle tongue during insertion/withdrawal). The USB Type-C receptacle at the system level should be implemented such that the USB Type-C receptacle connector mounted in the associated system hardware has an effective shell length equal to 6.20 ± 0.20 mm.
8. The USB Type-C connector mating interface is defined so that the electrical connection may be established without the receptacle shell. To prevent excessive misalignment of the plug when it enters or exits the receptacle, the enclosure should have features to guide the plug for insertion and withdrawal when a modified

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

receptacle shell is present. If the USB Type-C receptacle shell is modified from the specified dimension, then the recommended lead in from the receptacle tongue to the plug point of entry is 1.5 mm minimum when mounted in the system.

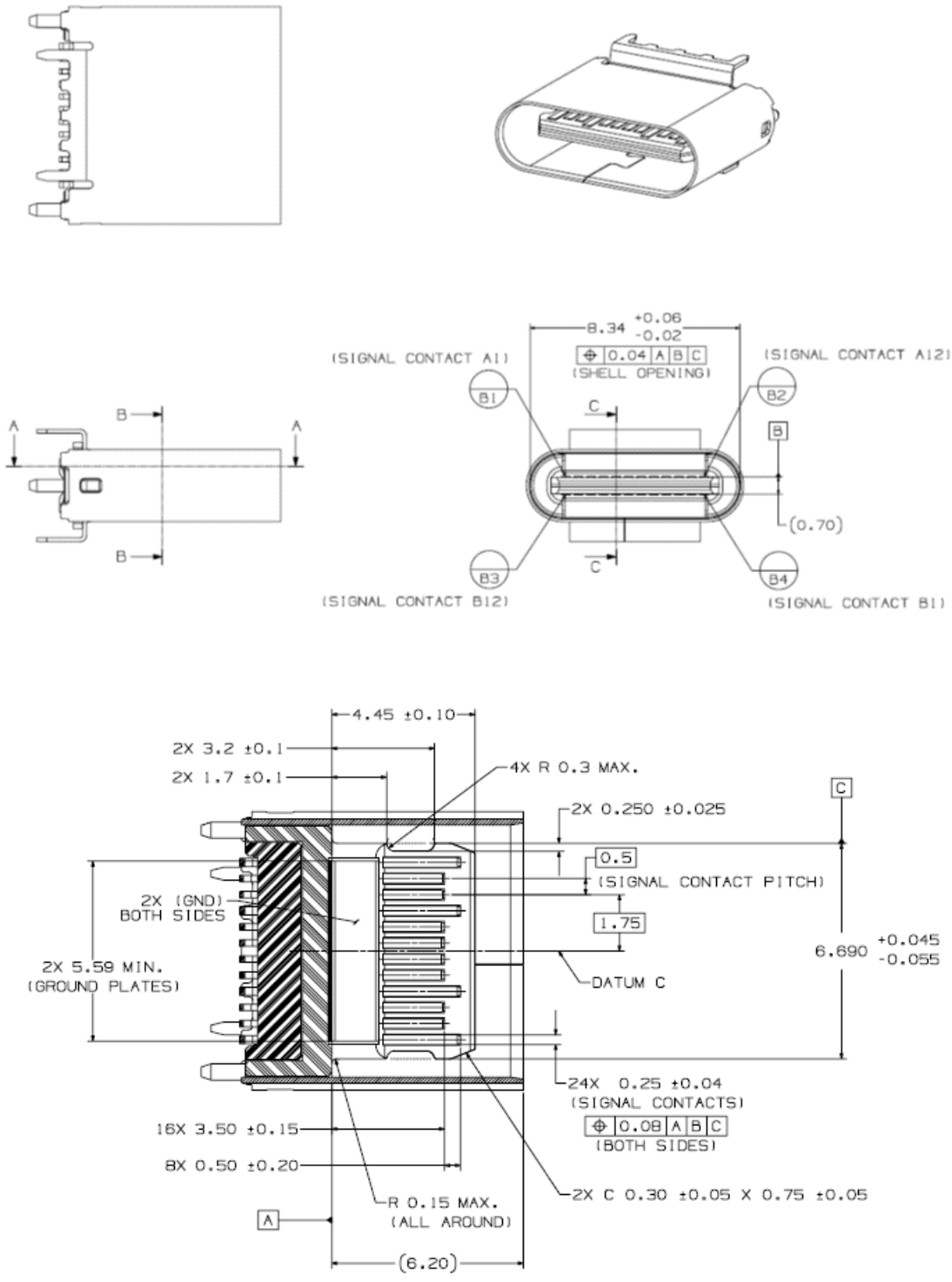
This specification allows receptacle configurations with a conductive shell, a non-conductive shell, or no shell. The following requirements apply to the receptacle contact dimensions shown in SECTION A-A and ALTERNATE SECTION A-A shown in Figure 3-1:

- If the receptacle shell is conductive, then the receptacle contact dimensions of SECTION A-A shown in Figure 3-1 shall be used. The contact dimensions of ALTERNATE SECTION A-A are not allowed.
- If the receptacle shell is non-conductive, then the receptacle contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. The contact dimensions of SECTION A-A are not allowed.
- If there is no receptacle shell, then the receptacle contact dimensions of either SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 may be used. If there is no receptacle shell and the receptacle is used in an implementation that does not effectively provide a conductive shell, then a receptacle with the contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 should be used.

9. A paddle card (e.g., PCB) may be used in the USB Type-C plug to manage wire termination and electrical performance. Section 3.2.2.5 includes the guidelines and a design example for a paddle card.
10. This specification does not define standard footprints. Figure 3-4 shows an example SMT (surface mount) footprint for the vertical receptacle shown in Figure 3-1. Additional reference footprints and mounting configurations are shown in Figure 3-5, Figure 3-6, Figure 3-7, and Figure 3-8.
11. The receptacle shell shall be connected to the PCB ground plane.
12. All VBUS pins shall be connected together in the USB Type-C plug.
13. All Ground return pins shall be connected together in the USB Type-C plug.
14. All VBUS pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all VBUS pins bussed together in the PCB).
15. All Ground return pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all Ground return pins bussed together in the PCB).

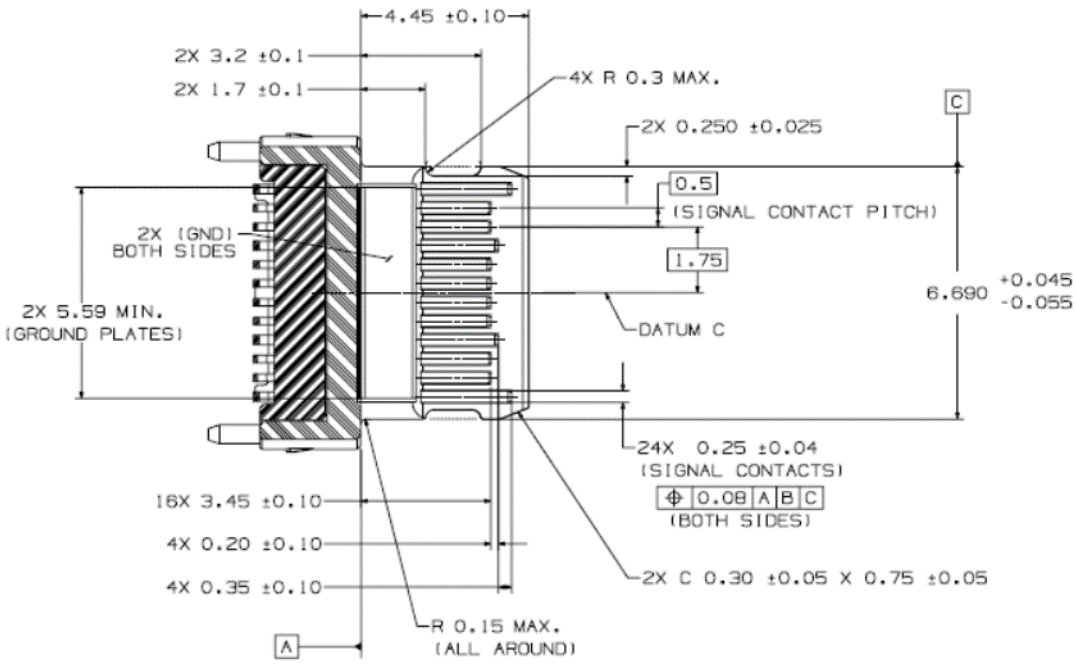
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-1 USB Type-C Receptacle Interface Dimensions



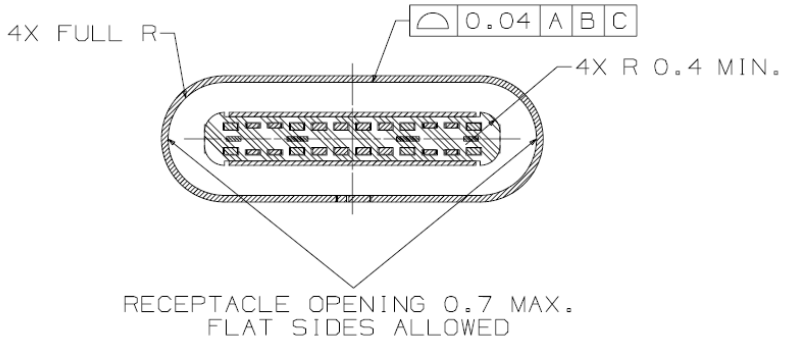
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



ALTERNATE SECTION A-A dimensions for use if the receptacle shell is non-conductive or there is no receptacle shell. This configuration is not allowed for receptacles with a conductive shell. See text for full requirements.

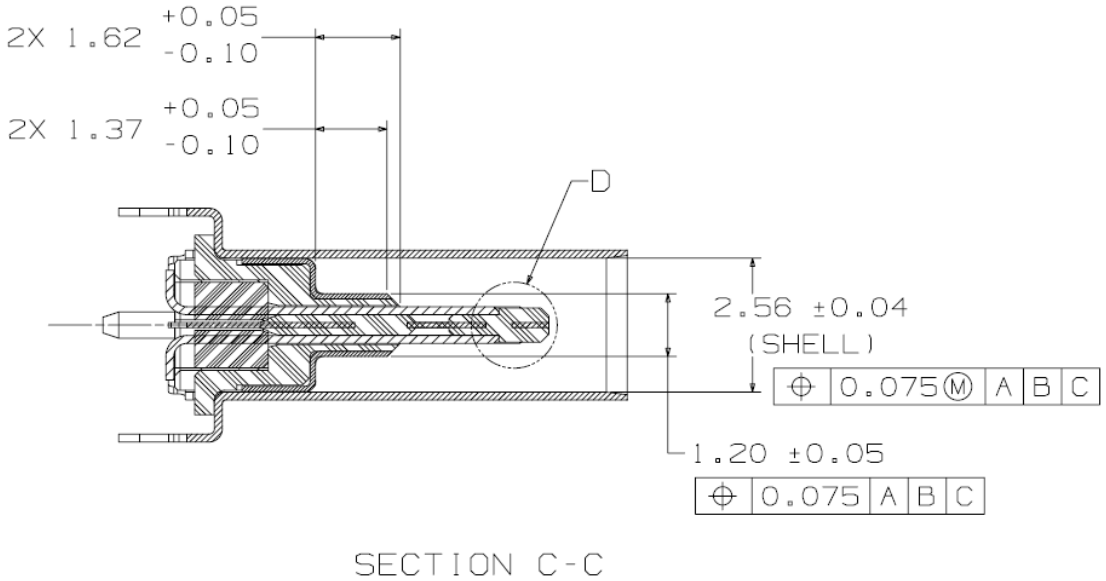
ALTERNATE SECTION A-A

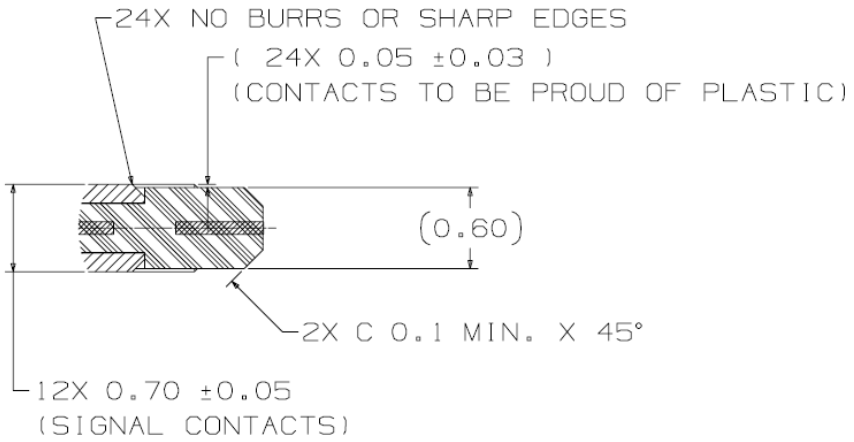


SECTION B-B

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

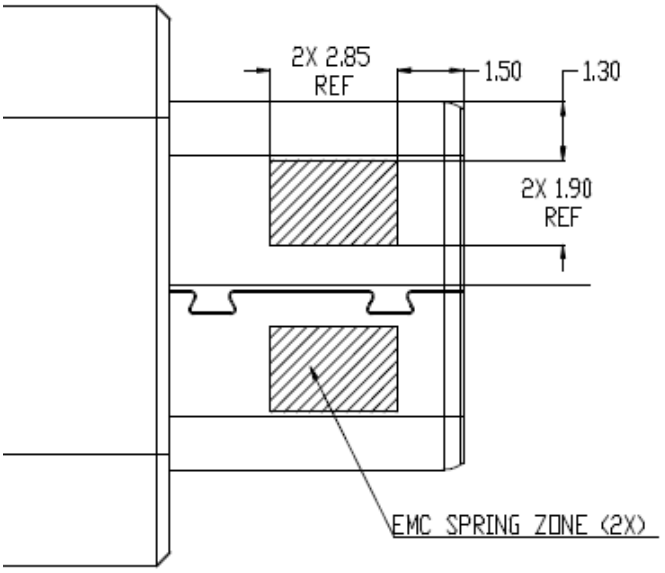
Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.

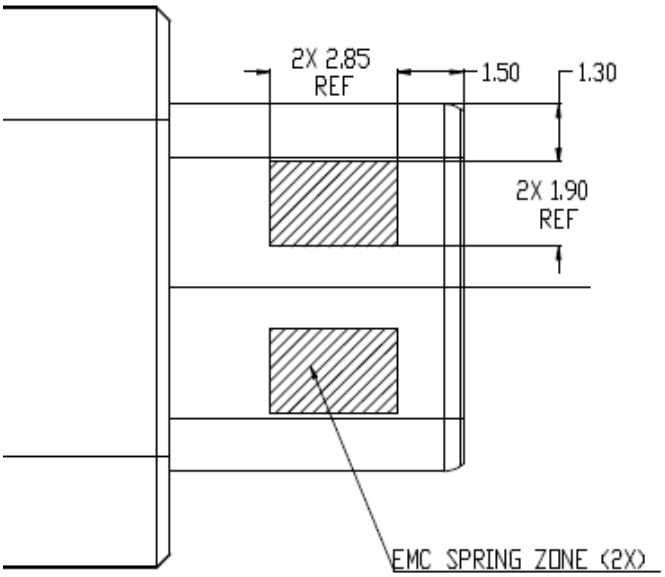




Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

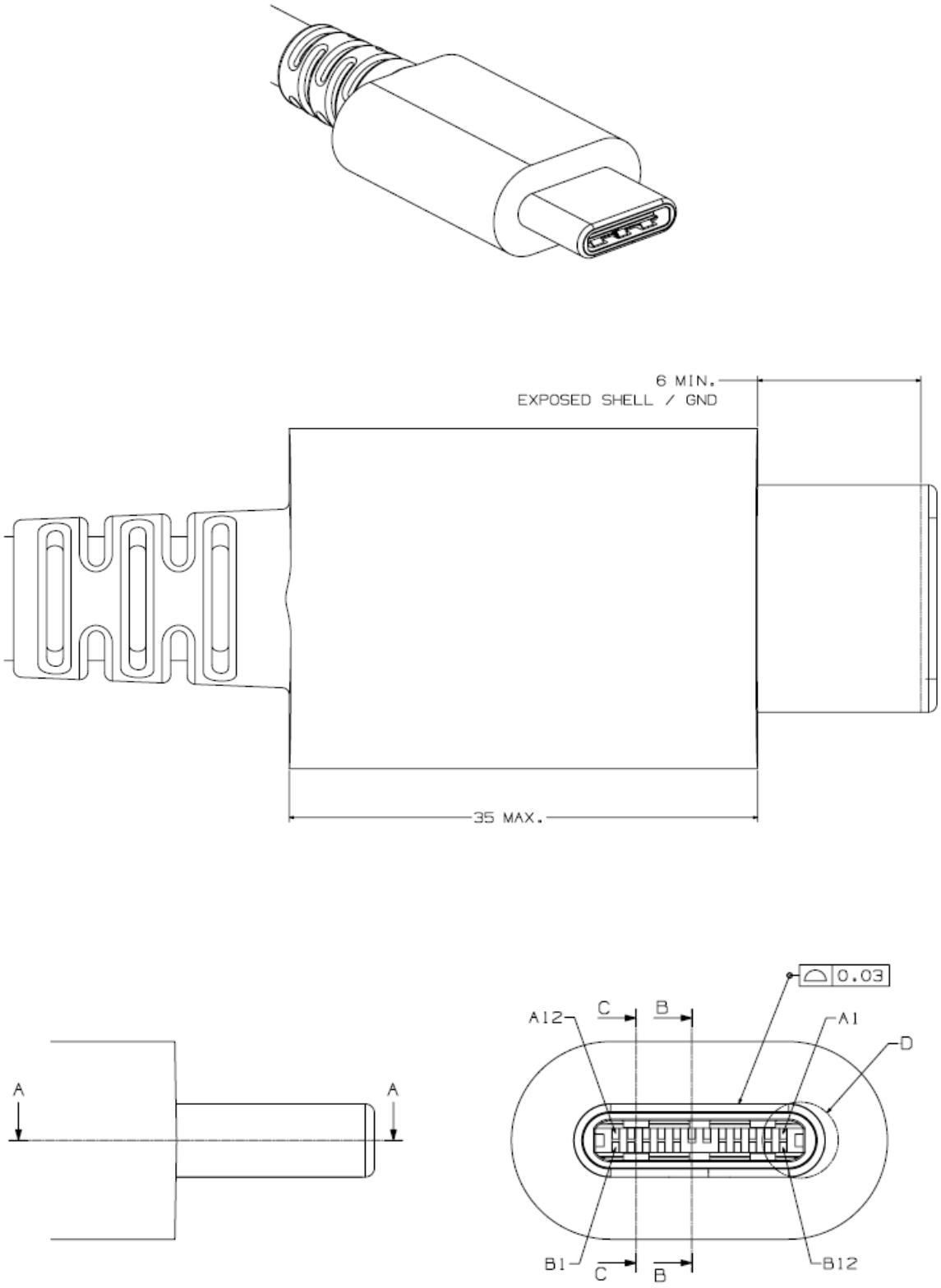
Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones





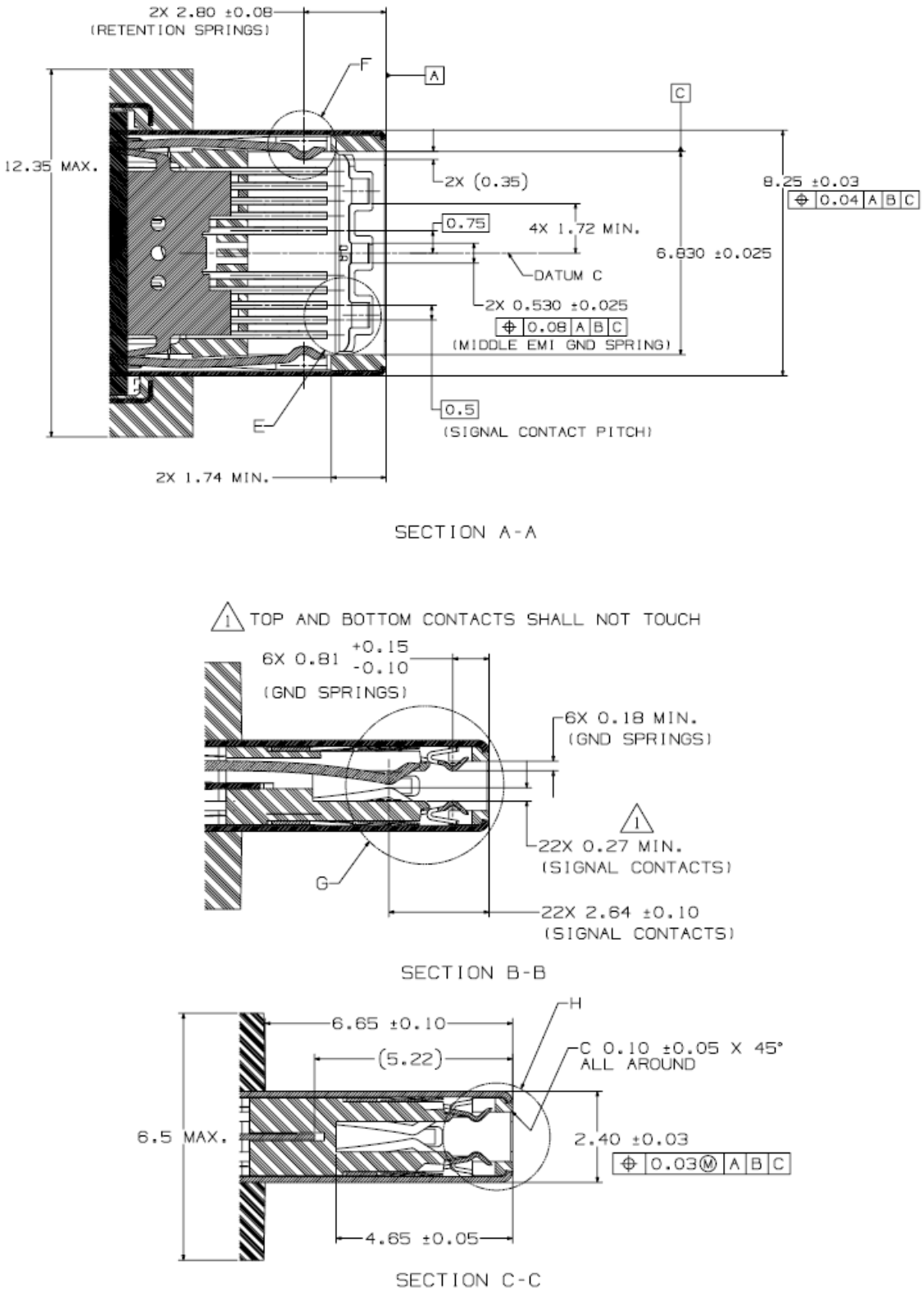
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions



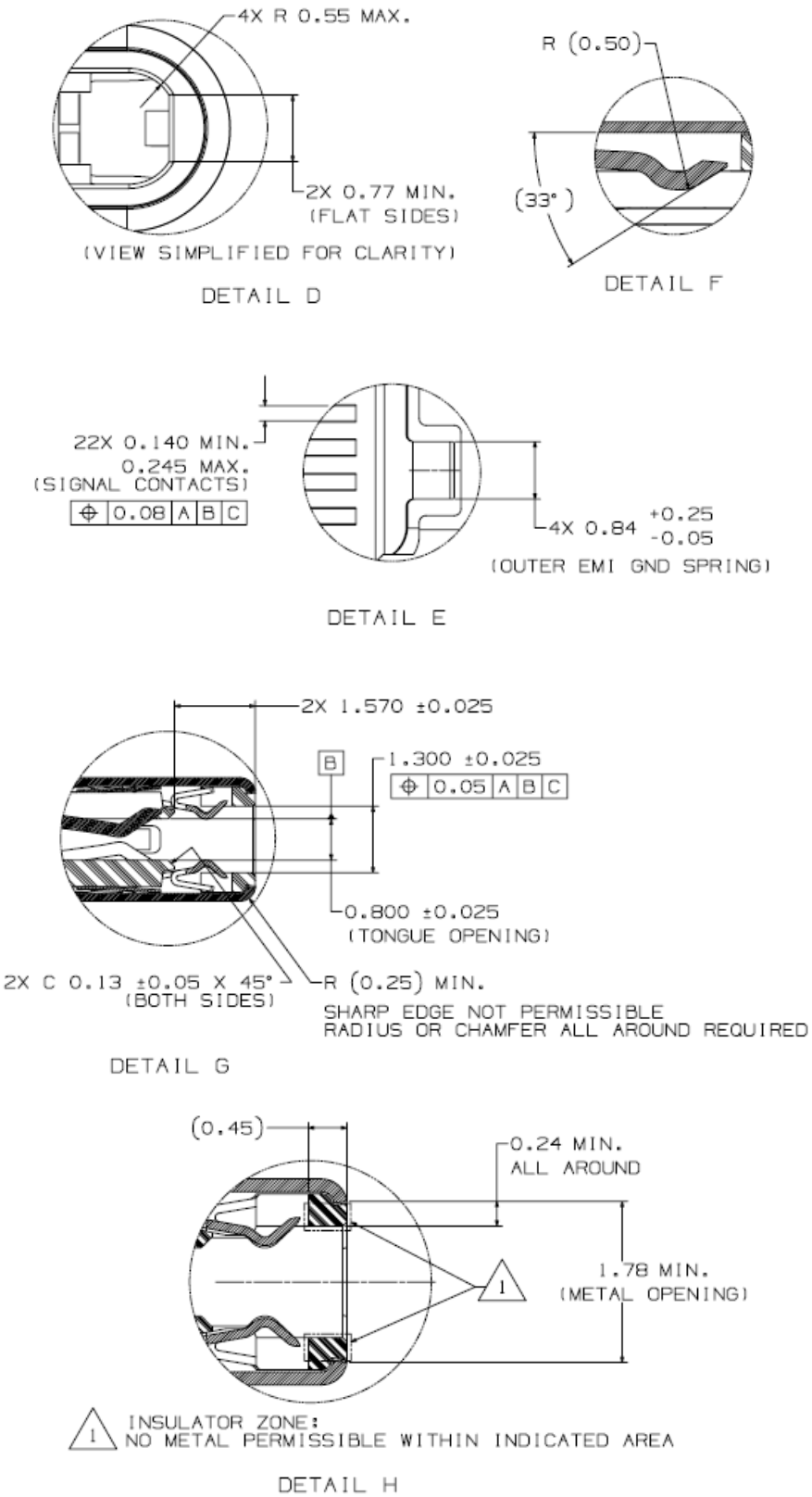
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



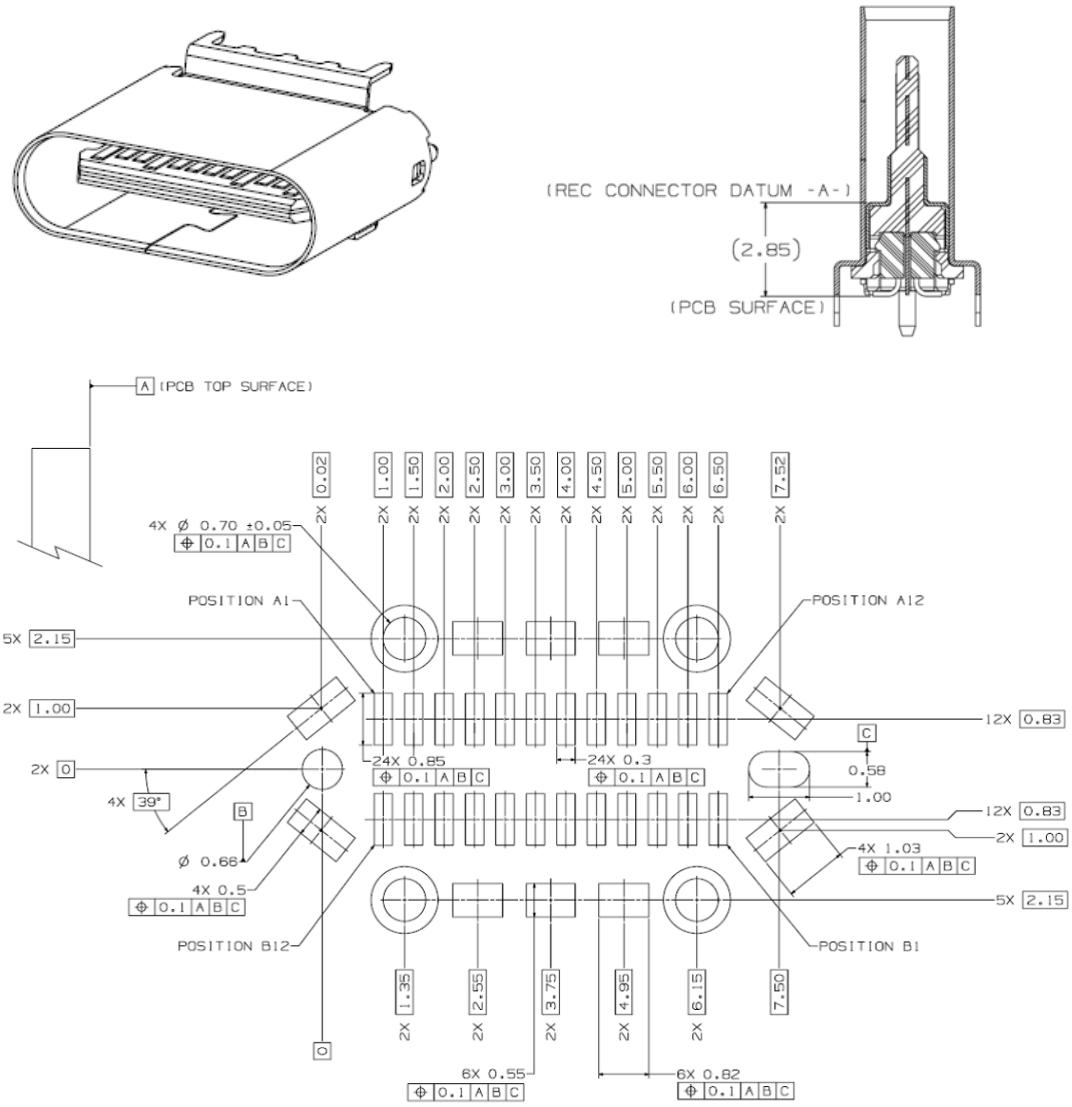
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



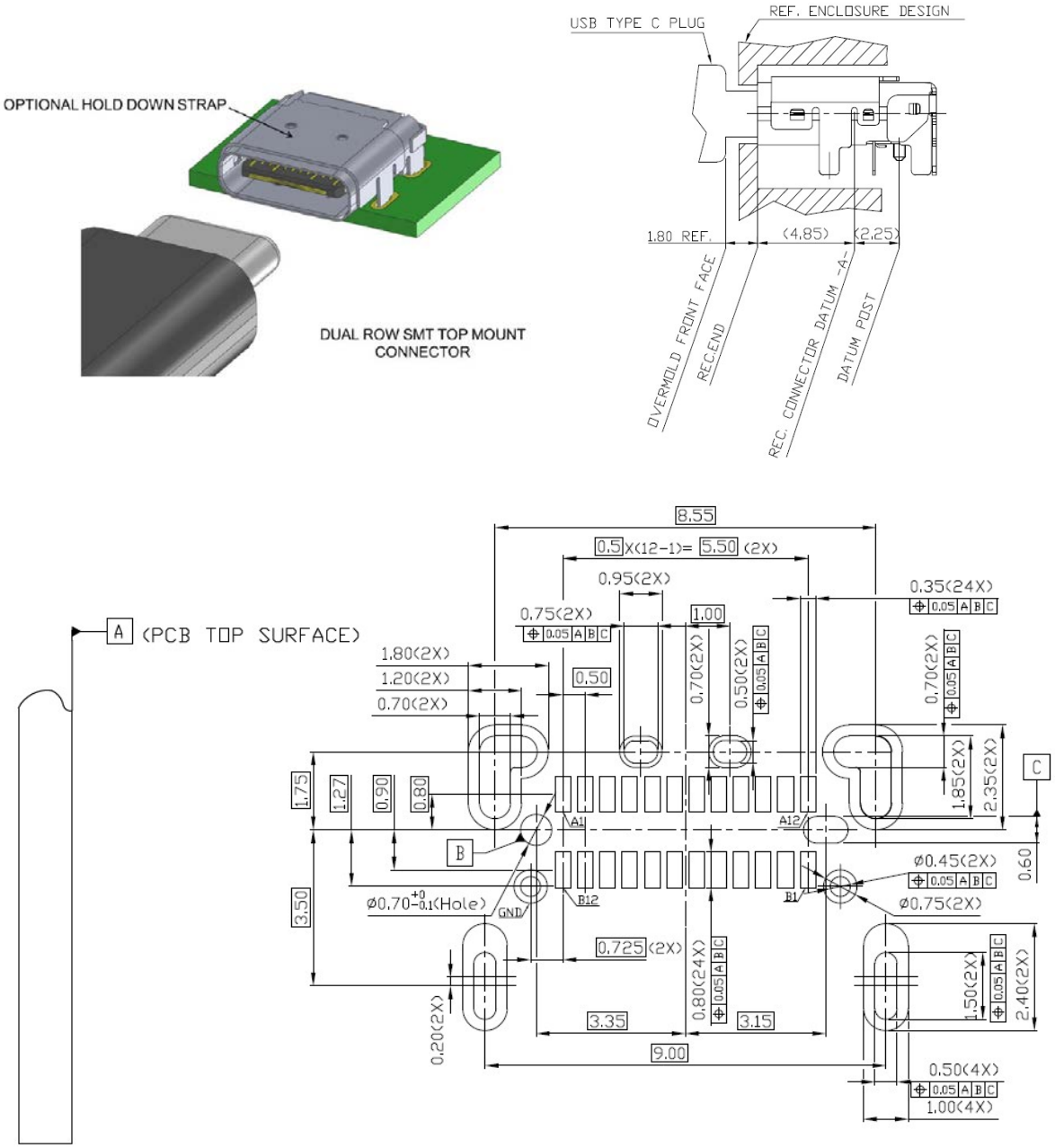
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative)



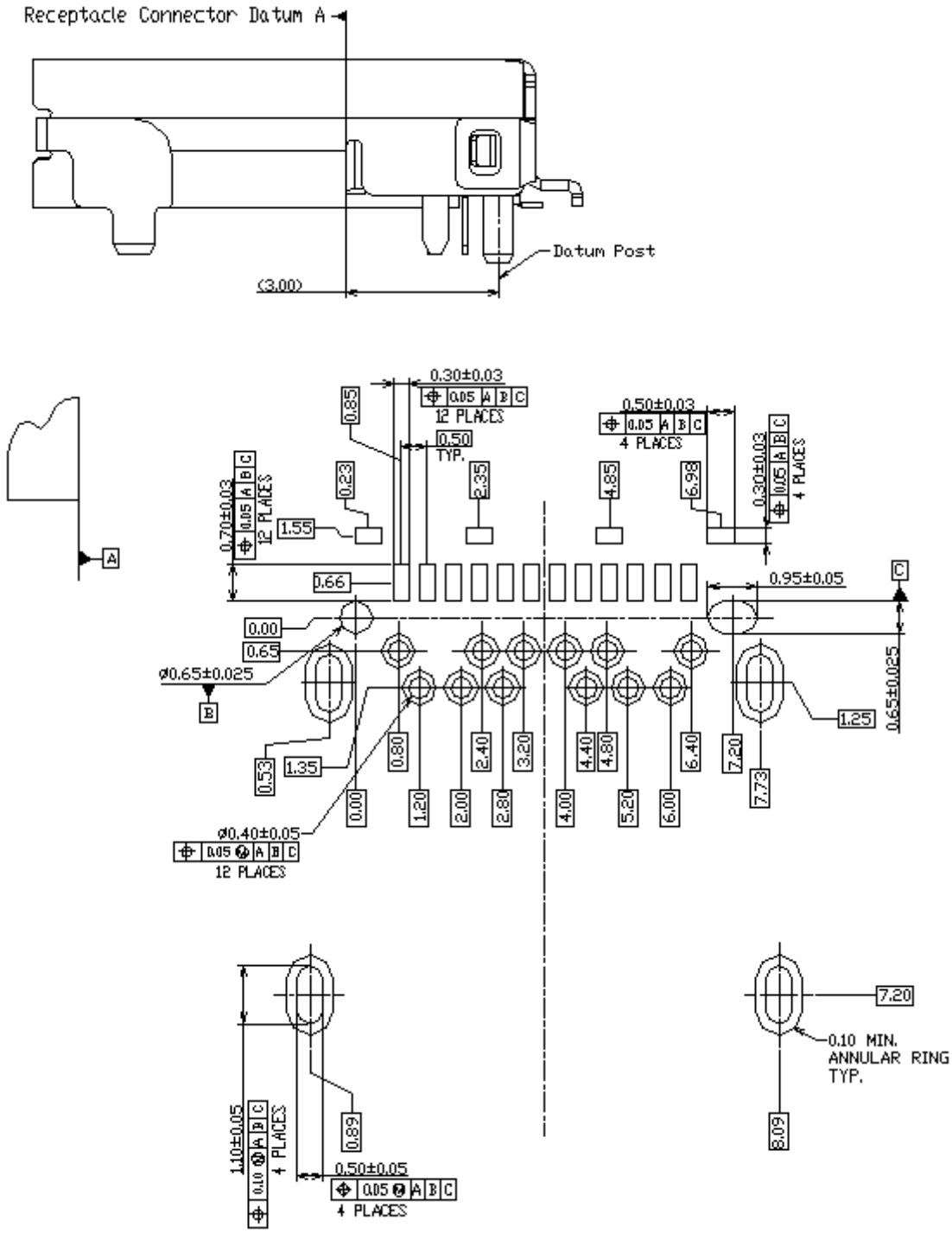
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right Angle Receptacle (Informative)



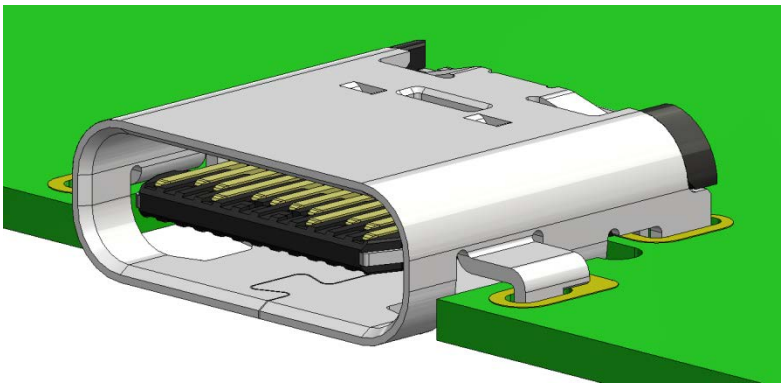
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

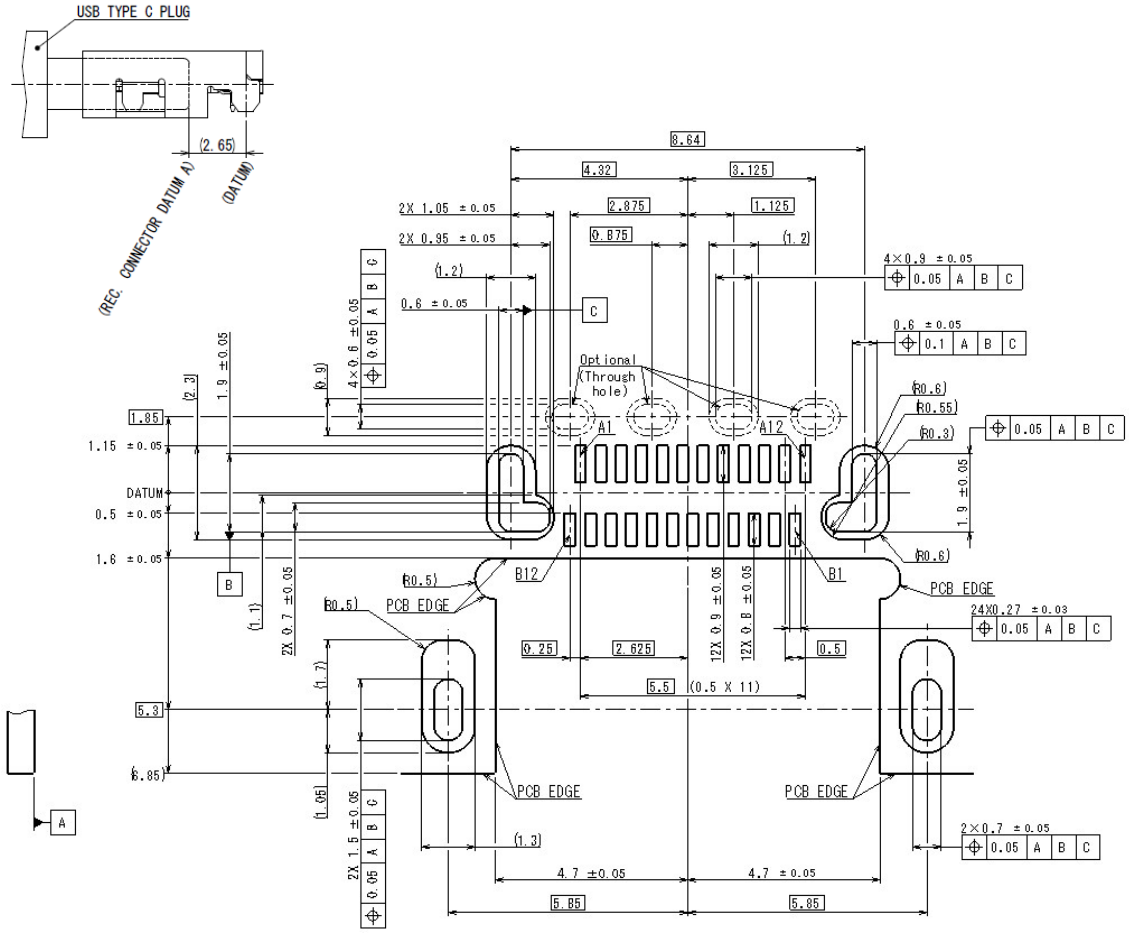
Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (Informative)



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

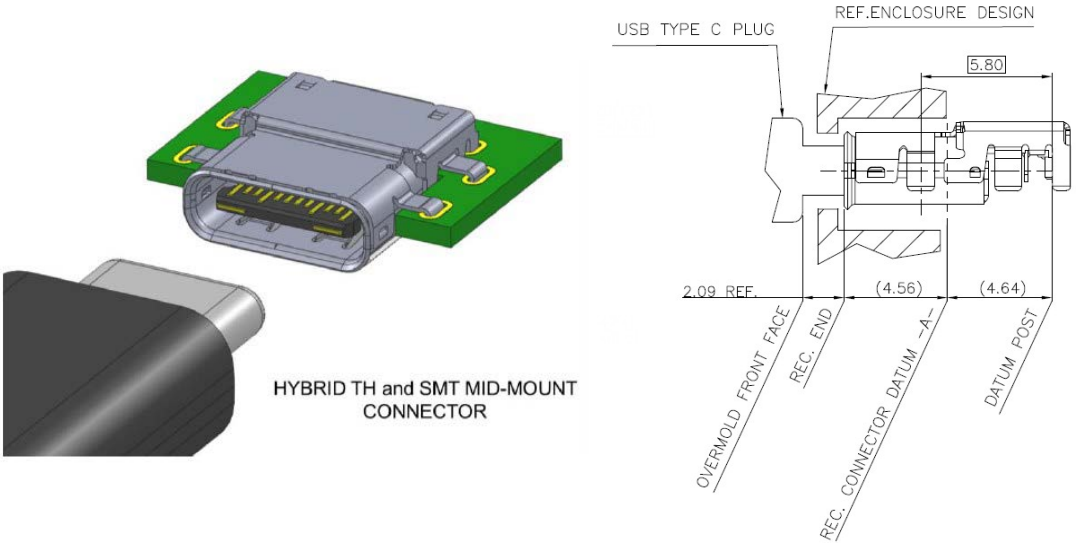
Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (Informative)

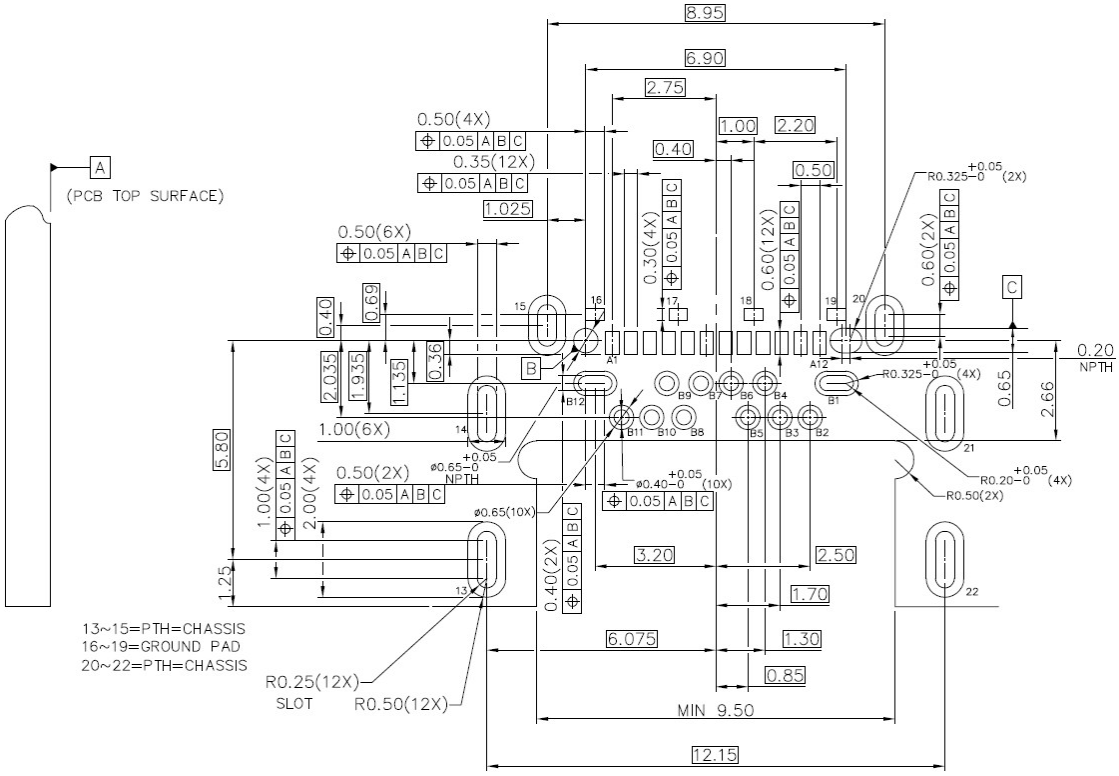




Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 41
Microchip v. Aptiv
IPR2024-00496

Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative)





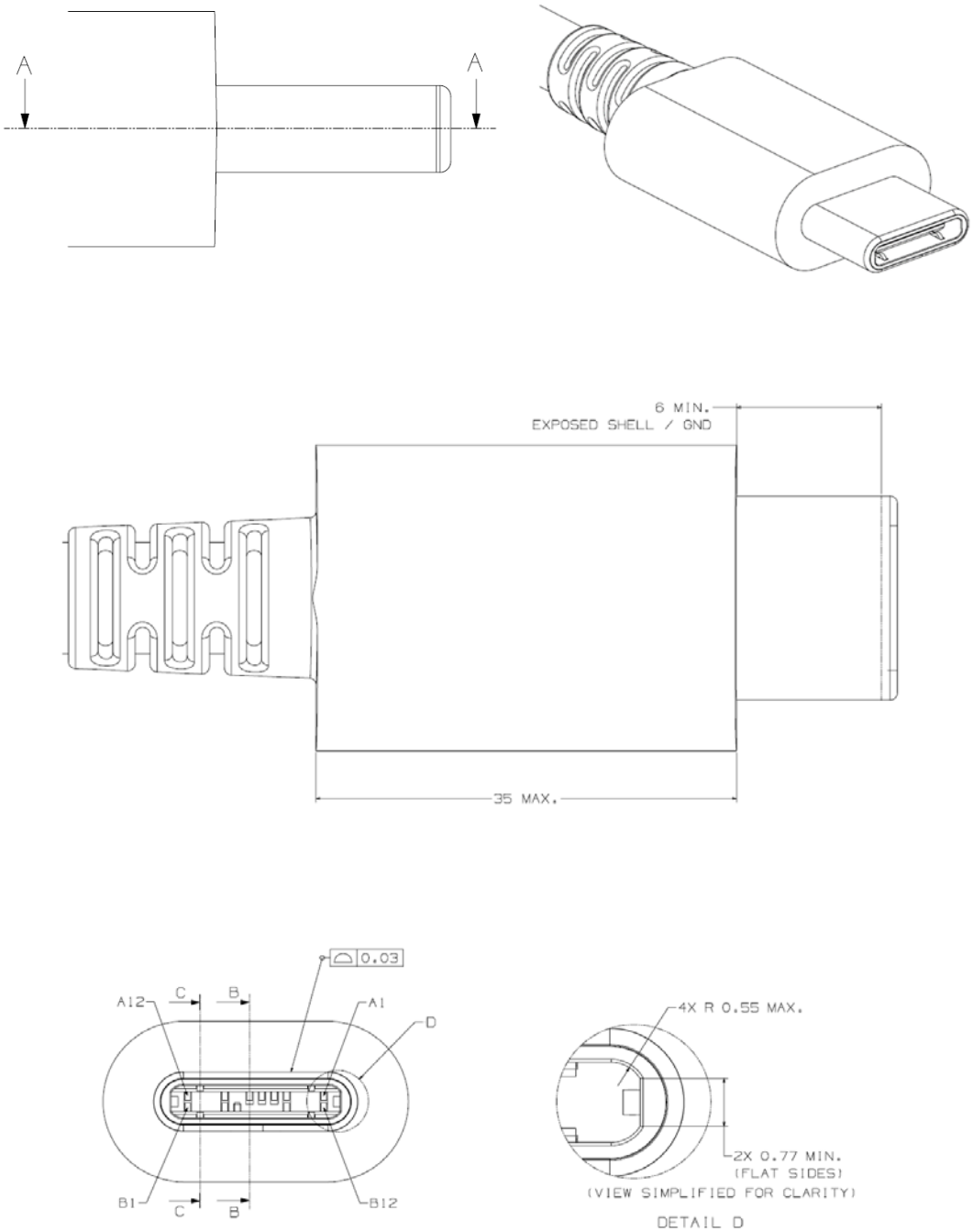
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

This specification requires that all contacts be present in the mating interface of the USB Type-C receptacle connector, but allows the plug to include only the contacts required for *USB PD* and *USB 2.0* functionality for applications that only support *USB 2.0*. The *USB 2.0* Type-C plug is shown in Figure 3-9. The following design simplifications may be made when only *USB 2.0* is supported:

- Only the contacts necessary to support *USB PD* and *USB 2.0* are required in the plug. All other pin locations may be unpopulated. See Table 3-5. All contacts are required to be present in the mating interface of the USB Type-C receptacle connector.
- Unlike the USB Full-Featured Type-C plug, the internal EMC springs may be formed from the same strip as the signal, power, and ground contacts. The internal EMC springs contact the inner surface of the plug shell and mate with the receptacle EMC pads when the plug is seated in the receptacle. Alternately, the *USB 2.0* Type-C plug may use the same EMC spring configuration as defined for the USB Full-Featured Type-C plug. The *USB 2.0* Type-C plug four EMC spring locations are defined in Figure 3-9. The alternate configuration using the six spring locations is defined in Figure 3-1. Also refer to the reference designs in 3.2.2.3 for further clarification.
- A paddle card inside the plug may not be necessary if wires are directly attached to the contact pins.

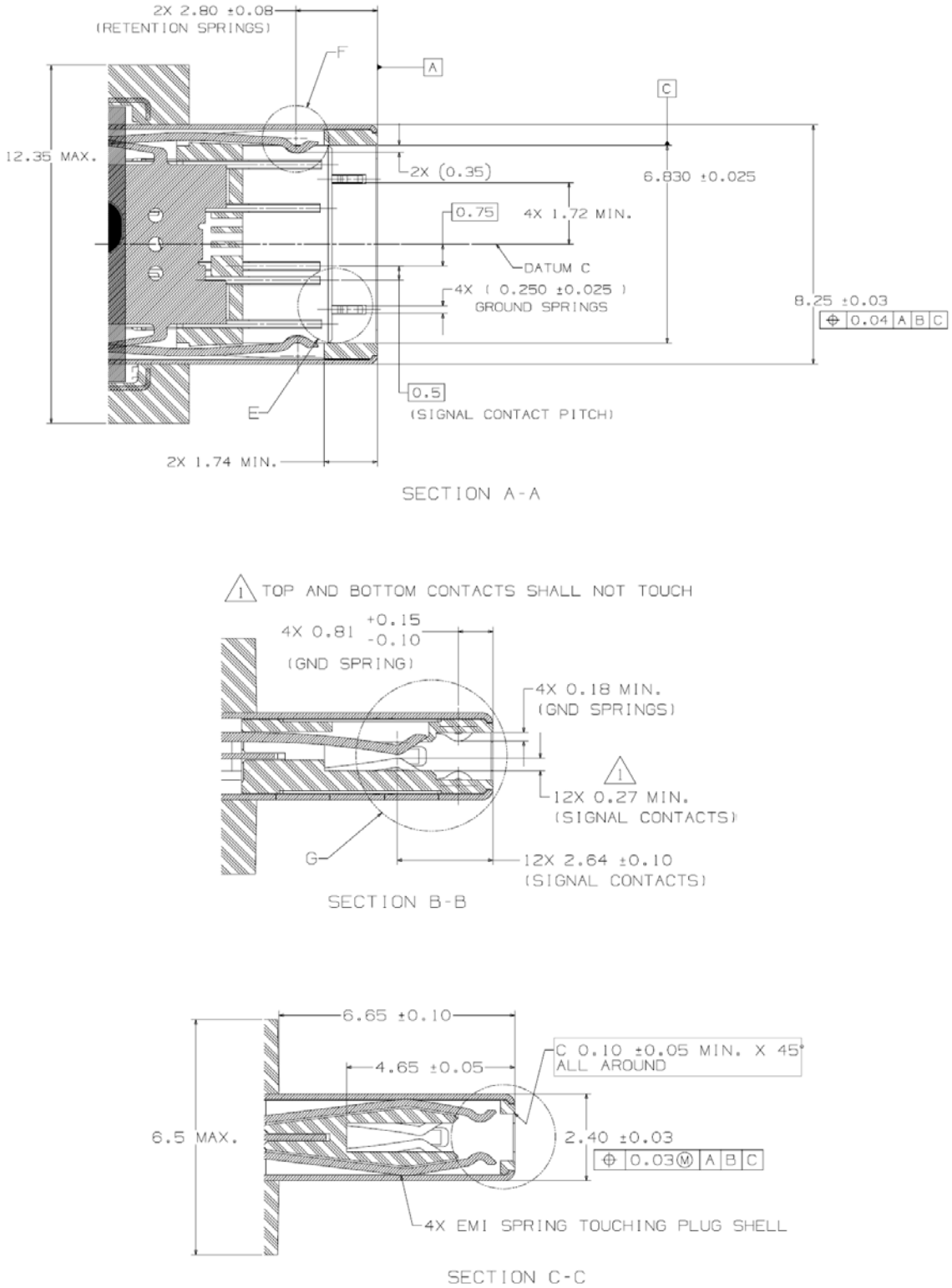
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-9 *USB 2.0* Type-C Plug Interface Dimensions



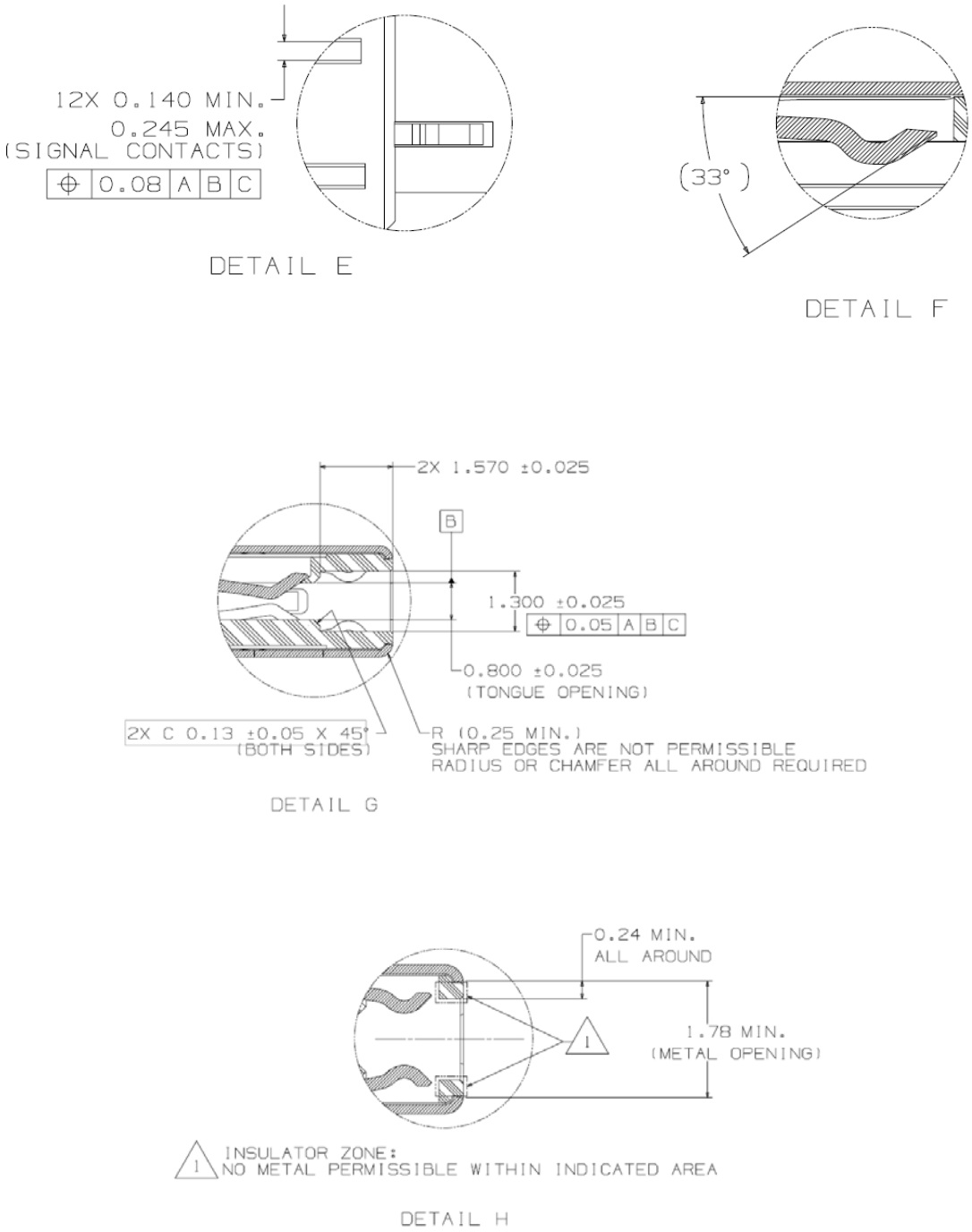
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-9 *USB 2.0* Type-C Plug Interface Dimensions, cont.



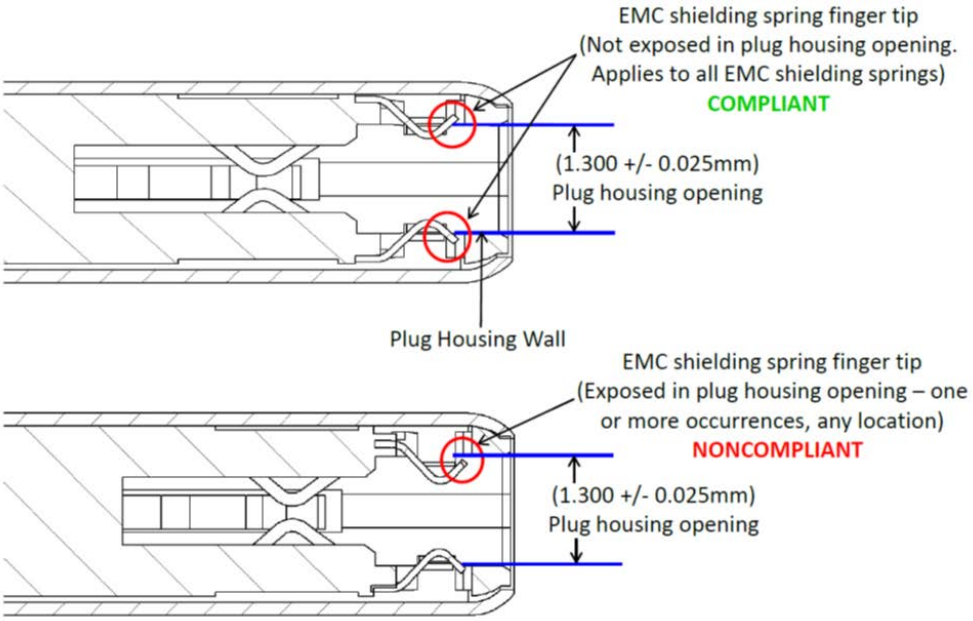
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-9 *USB 2.0* Type-C Plug Interface Dimensions, cont.



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-10 USB Type-C Plug EMC Shielding Spring Tip Requirements



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.2.2 Reference Designs

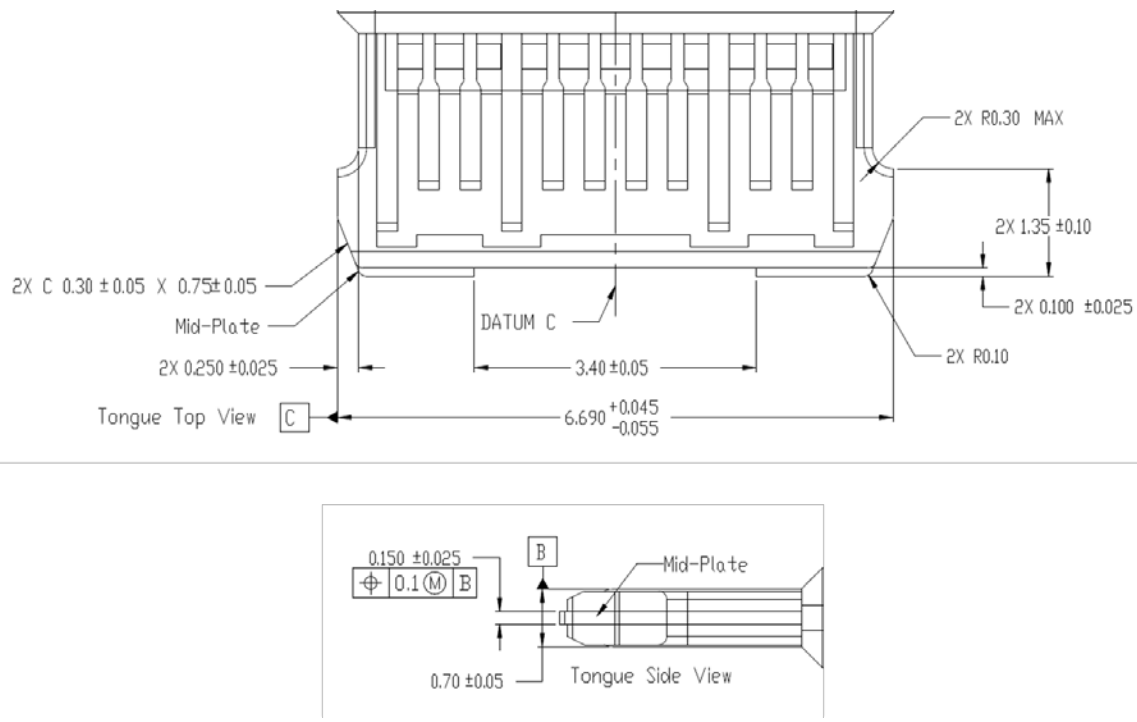
This section provides reference designs for a few key features of the USB Type-C connector. The reference designs are provided as acceptable design examples. They are not normative.

3.2.2.1 Receptacle Mid-Plate (Informative)

The signals between the top and bottom of the receptacle tongue are isolated by a mid-plate inside the tongue. Figure 3-11 shows a reference design of the mid-plate. It is important to pay attention to the following features of the middle plate:

- The distance between the signal contacts and the mid-plate should be accurately controlled since the variation of this distance may significantly impact impedance of the connector.
- The mid-plate in this particular design protrudes slightly beyond the front surface of the tongue. This is to protect the tongue front surface from damage caused by miss-insertion of small objects into the receptacle.
- The mid-plate is required to be directly connected to the PCB ground with at least two grounding points.
- The sides of the mid-plate mate with the plug side latches, making ground connections to reduce EMC. Proper surface finishes are necessary in the areas where the side latches and mid-plate connections occur.

Figure 3-11 Reference Design of Receptacle Mid-Plate



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.2.2.2 Side Latch (informative)

The side latches (retention latches) are located in the plug. Figure 3-12 shows a reference design of a blanked side latch. The plug side latches should contact the receptacle mid-plate to provide an additional ground return path.

Figure 3-12 Reference Design of the Retention Latch

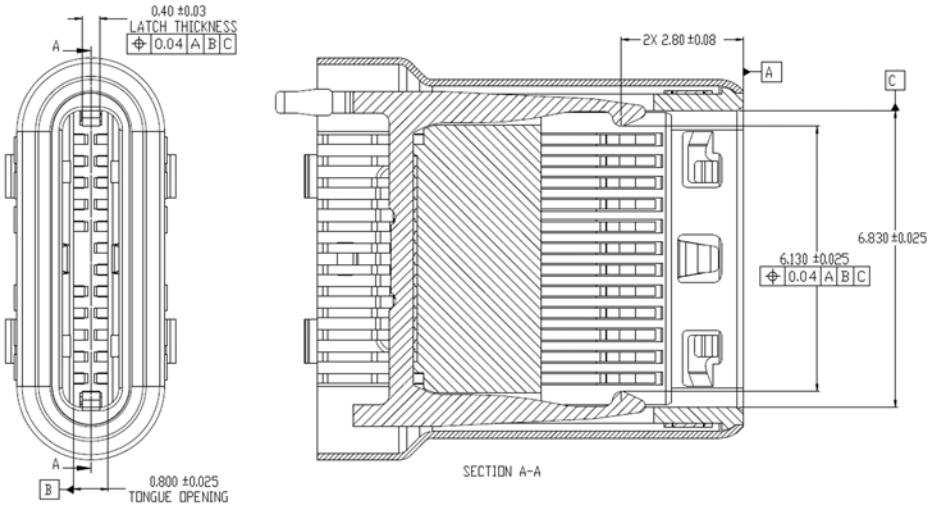
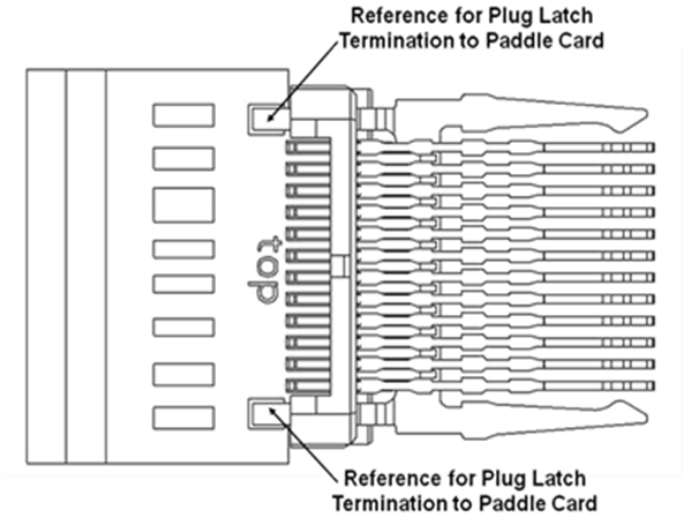


Figure 3-13 Illustration of the Latch Soldered to the Paddle Card Ground

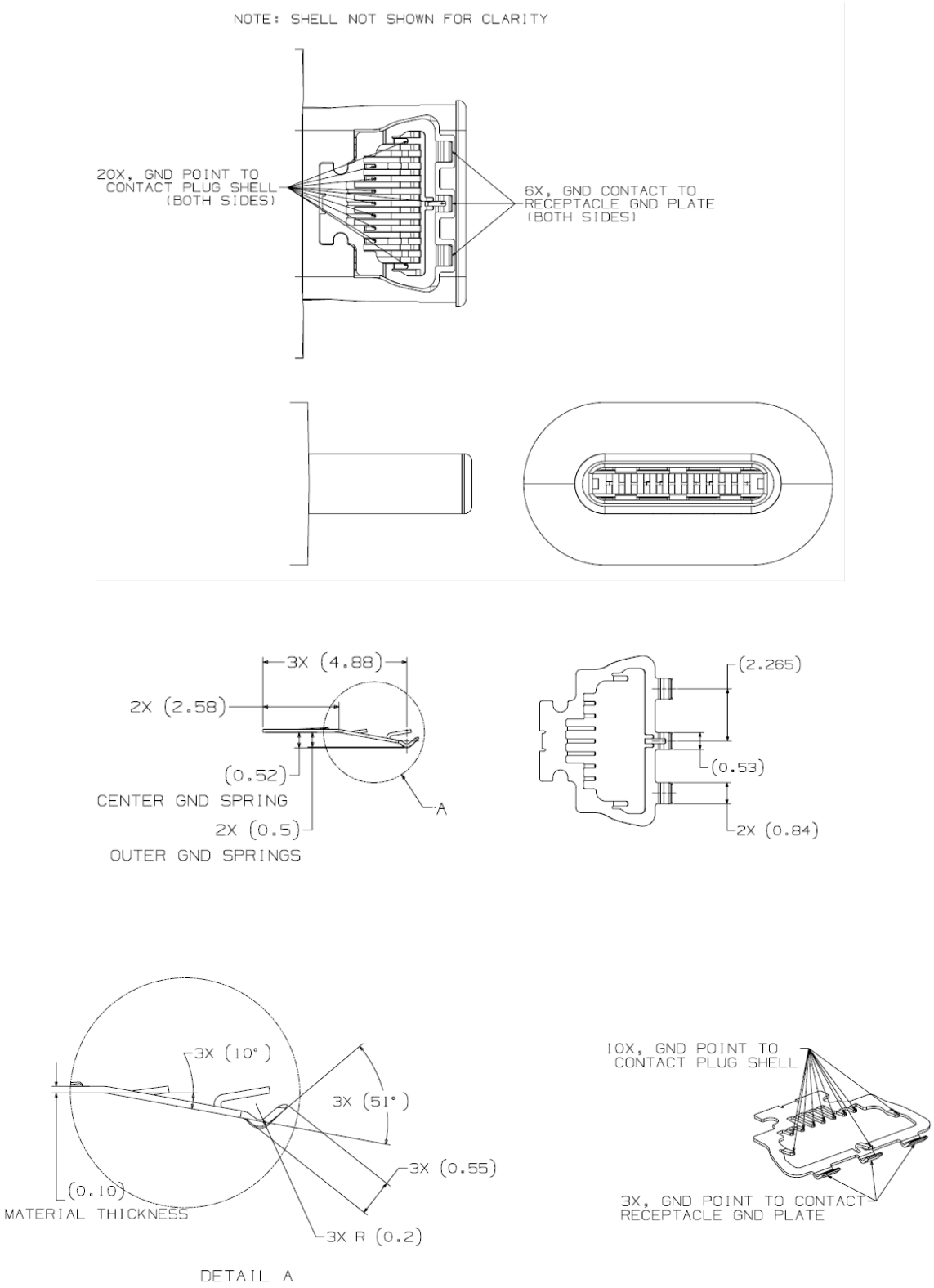


3.2.2.3 Internal EMC Springs and Pads (Informative)

Figure 3-14 is a reference design of the internal EMC spring located inside the USB Full-Featured Type-C plug. Figure 3-15 is a reference design of the internal EMC spring located inside the *USB 2.0* Type-C plug.

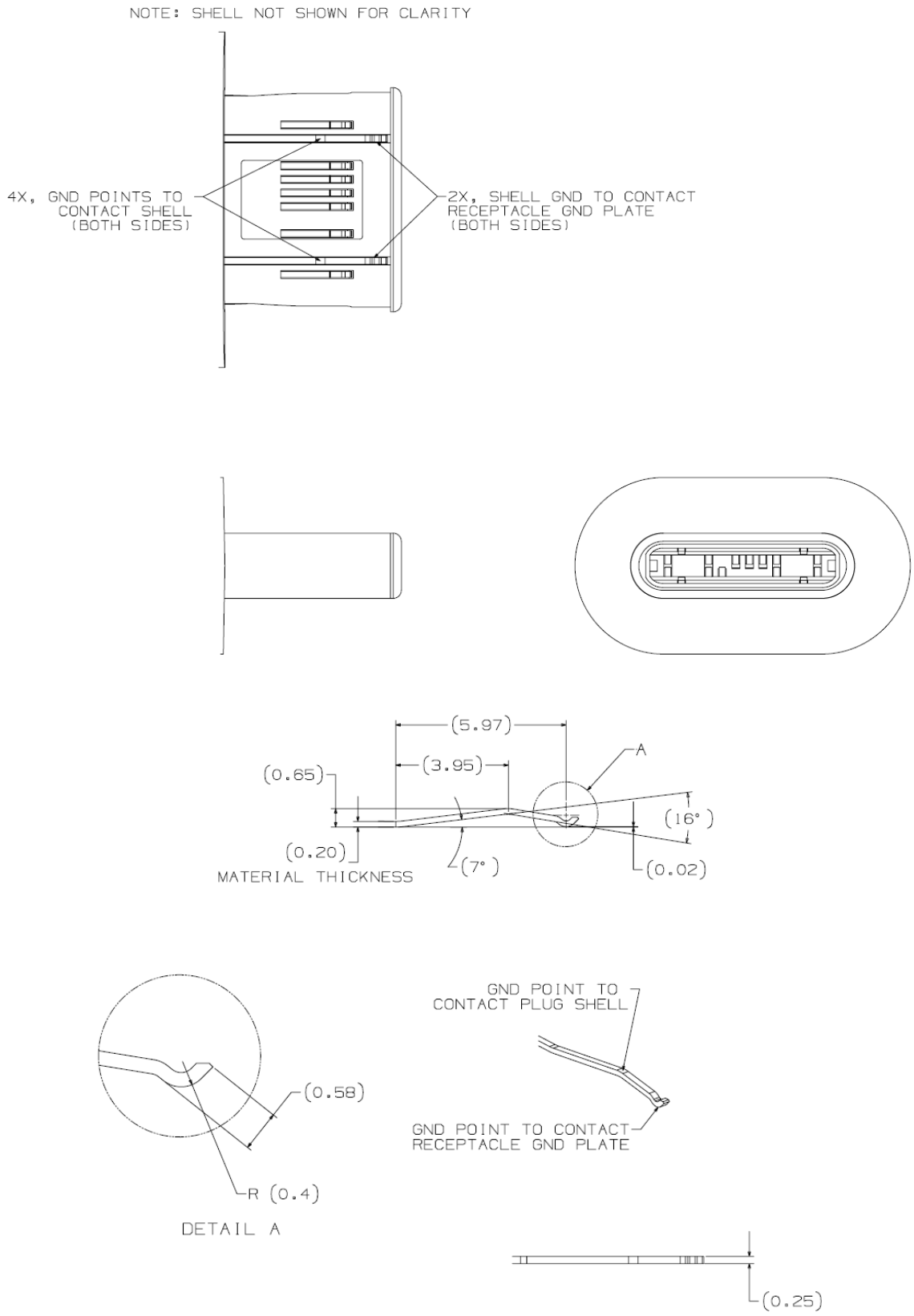
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-14 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-15 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring

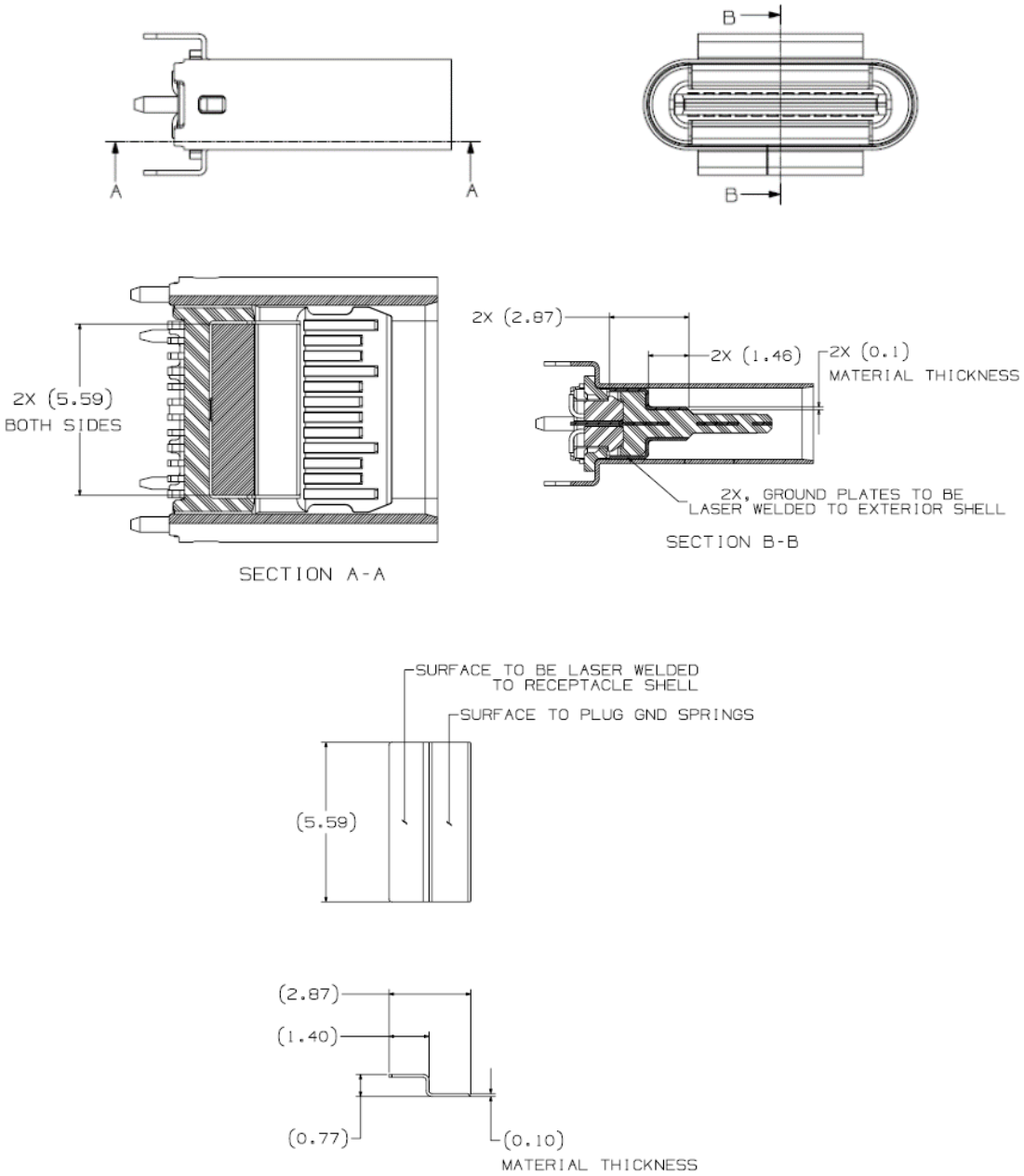


Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

It is critical that the internal EMC spring contacts the plug shell as close to the EMC spring mating interface as possible to minimize the length of the return path.

The internal EMC pad (i.e., ground plate) shown in Figure 3-16 is inside the receptacle. It mates with the EMC spring in the plug. To provide an effective ground return, the EMC pads should have multiple connections with the receptacle shell.

Figure 3-16 Reference Design of Internal EMC Pad

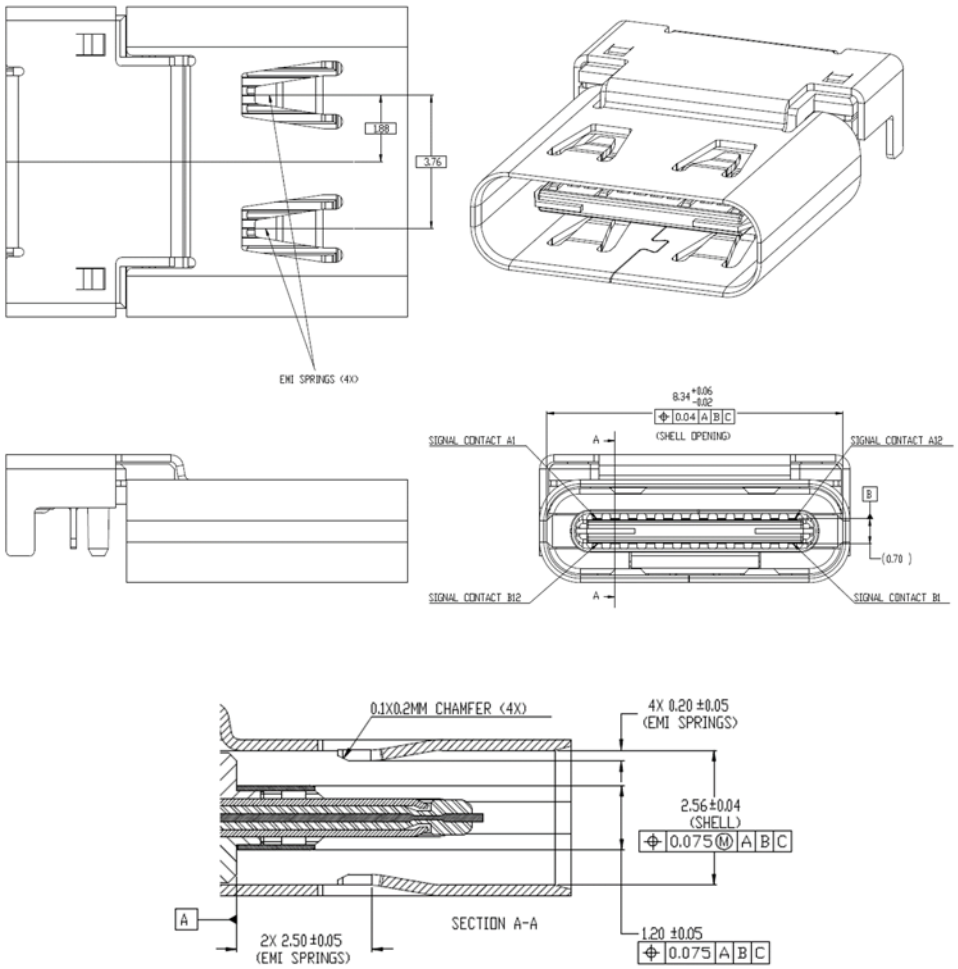


Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.2.2.4 Optional External Receptacle EMC Springs (Informative)

Some applications may use receptacles with EMC springs that contact the outside of the plug shell. Figure 3-17 shows a reference receptacle design with external EMC springs. The EMC spring contact landing zones for the fully mated condition are normative and defined in Section 3.2.1.

Figure 3-17 Reference Design of a USB Type-C Receptacle with External EMC Springs



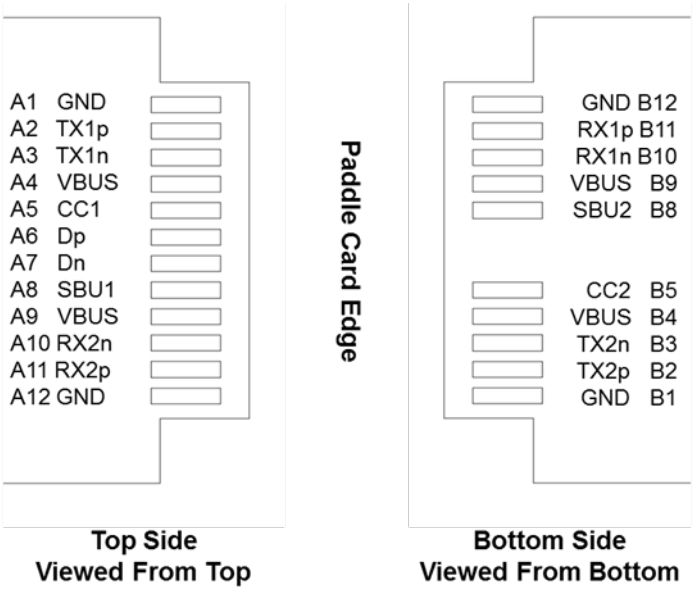
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.2.2.5 USB Full-Featured Type-C Plug Paddle Card (Informative)

The use of a paddle card is expected in the USB Full-Featured Type-C Plug. Figure 3-18 illustrates the paddle card pin assignment and contact spring connection location for a USB Full-Featured Type-C plug. The following guidelines are provided for the paddle card design:

- The paddle card should use high performance substrate material. The recommended paddle card thickness should have a tolerance less than or equal to ± 10%.
- The USB SuperSpeed traces should be as short as possible and have a nominal differential characteristic impedance of 85 Ω.
- The wire attach should have two high speed differential pairs on one side and two other high speed differential pairs on the other side, separated as far as practically allowed.
- It is recommended that a grounded coplanar waveguide (CPWG) system be selected as a transmission line method.
- Use of vias should be minimized.
- VBUS pins should be bussed together on the paddle card.
- GND pins should be bussed together on the paddle card.

Figure 3-18 Reference Design for a USB Full-Featured Type-C Plug Paddle Card



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.2.3 Pin Assignments and Descriptions

The usage and assignments of the 24 pins for the USB Type-C receptacle interface are defined in Table 3-4.

Table 3-4 USB Type-C Receptacle Interface Pin Assignments

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	SSTXp1	Positive half of first SuperSpeed TX differential pair	Second	B11	SSRXp1	Positive half of first SuperSpeed RX differential pair	Second
A3	SSTXn1	Negative half of first SuperSpeed TX differential pair	Second	B10	SSRXn1	Negative half of first SuperSpeed RX differential pair	Second
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10	SSRXn2	Negative half of second SuperSpeed RX differential pair	Second	B3	SSTXn2	Negative half of second SuperSpeed TX differential pair	Second
A11	SSRXp2	Positive half of second SuperSpeed RX differential pair	Second	B2	SSTXp2	Positive half of second SuperSpeed TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the *USB 2.0* differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3.5 mm.
2. All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
3. All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
4. If the contact dimensions shown in Figure 3-1 ALTERNATE SECTION A-A are used, then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A2, A3, A5, A6, A7, A8, A10, A11, B2, B3, B5, B6, B7, B8, B10 and B11) mate third.

The usage and assignments of the signals necessary for the support of only *USB 2.0* with the USB Type-C mating interface are defined in Table 3-5.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. The unused contacts shall not be physically depopulated in the USB Type-C receptacle. Unused contact locations shall be electrically isolated from power, ground or signaling (i.e., not connected).
2. Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the *USB 2.0* differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3.5 mm.
3. Contacts A8 and B8 (SBU1 and SBU2) shall be not connected unless required for a specified purpose (e.g., Audio Adapter Accessory Mode).
4. All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
5. All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
6. If the contact dimensions shown in Figure 3-1 ALTERNATE SECTION A-A are used then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A5, A6, A7, A8, B5, B6, B7 and B8) mate third.

3.3 Cable Construction and Wire Assignments

This section discusses the USB Type-C cables, including cable construction, wire assignments, and wire gauges.

3.3.1 Cable Construction (Informative)

Figure 3-19 illustrates an example of USB Full-Featured Type-C cable cross-section, using micro-coaxial wires for USB SuperSpeed. There are four groups of wires: USB D+/D− (typically unshielded twisted pairs (UTP)), USB SuperSpeed signal pairs (coaxial wires, twin-axial or shielded twisted pairs), sideband signal wires, and power and ground wires. In this example, the optional VCONN wire is shown whereas in Figure 3-20 the example is shown

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

with the VCONN wire removed – the inclusion of VCONN or not relates to the implementation approach chosen for electronically marked cables (See Section 4.9).

Figure 3-19 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN

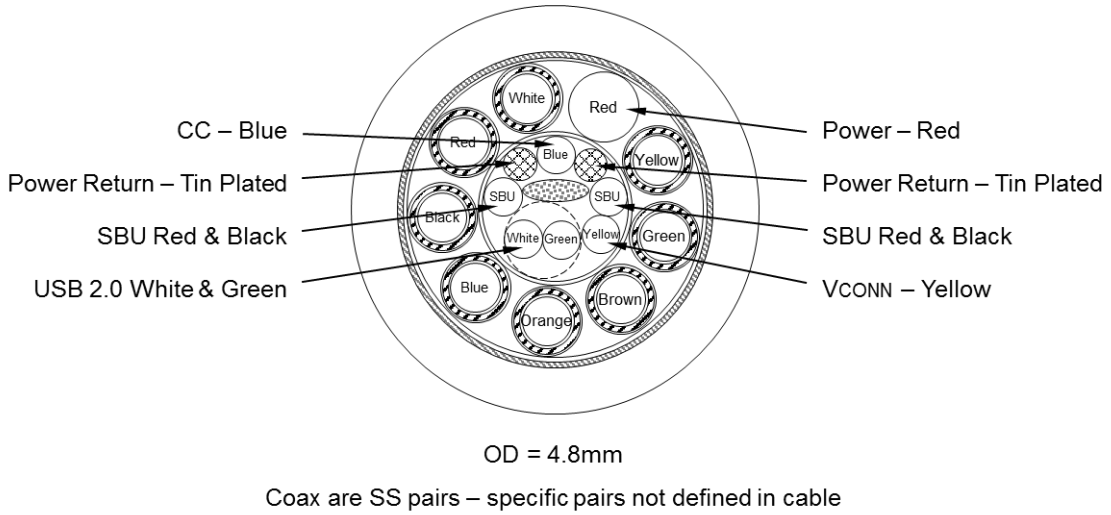
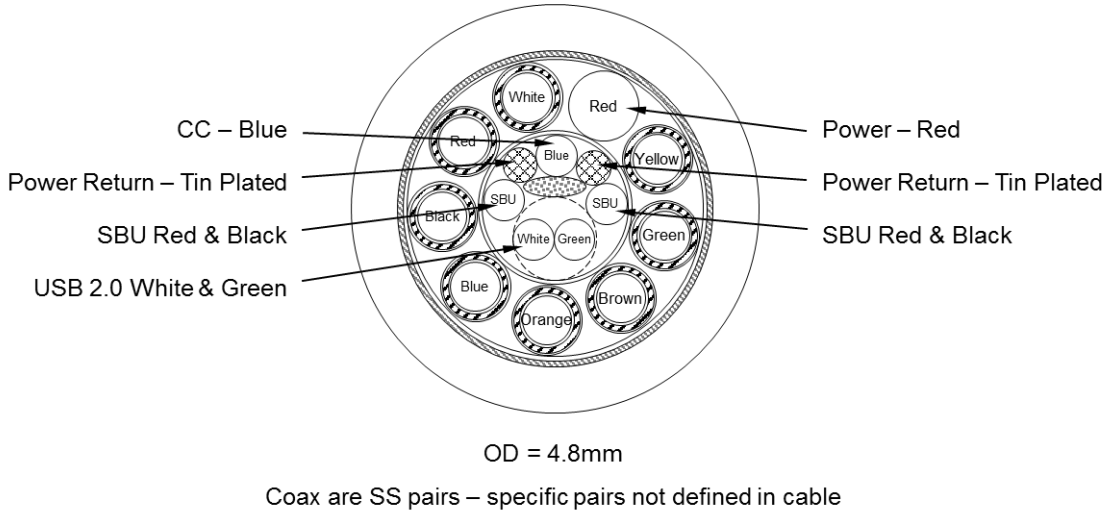


Figure 3-20 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN



The USB D+/D− signal pair is intended to transmit the *USB 2.0* Low-Speed, Full-Speed and High-Speed signaling while the SuperSpeed signal pairs are used for *USB 3.1* SuperSpeed signaling. Shielding is needed for the SuperSpeed differential pairs for signal integrity and EMC performance.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.3.2 Wire Assignments

Table 3-6 defines the full set of possible wires needed to produce all standard USB Type-C cables assemblies. For some cable assemblies, not all of these wires are used. For example, a USB Type-C cable that only provides *USB 2.0* functionality will not include wires 6–15.

Table 3-6 USB Type-C Standard Cable Wire Assignments

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	CC	Configuration Channel
4	UTP_Dp	Unshielded twist pair, positive
5	UTP_Dn	Unshielded twist pair, negative
6	SDPp1	Shielded differential pair #1, positive
7	SDPn1	Shielded differential pair #1, negative
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDPp3	Shielded differential pair #3, positive
11	SDPn3	Shielded differential pair #3, negative
12	SDPp4	Shielded differential pair #4, positive
13	SDPn4	Shielded differential pair #4, negative
14	SBU_A	Sideband Use
15	SBU_B	Sideband Use
16	GND_PWRrt2	Ground for power return (optional)
17	PWR_VBUS2	VBUS power (optional)
18	PWR_VCONN	VCONN power (optional, see Section 4.9)
Braid	Shield	Cable external braid

Note:

1. This table is based on the assumption that coaxial wire construction is used for all SDP's and there are no drain wires. The signal ground return is through the shields of the coaxial wires. If shielded twisted or twin-axial pairs are used, then drain wires are needed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-7 defines the full set of possible wires needed to produce USB Type-C to legacy cable assemblies. For some cable assemblies, not all of these wires are needed. For example, a USB Type-C to *USB 2.0* Standard-B cable will not include wires 5–10.

Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	UTP_Dp	Unshielded twist pair, positive
4	UTP_Dn	Unshielded twist pair, negative
5	SDPp1	Shielded differential pair #1, positive
6	SDPn1	Shielded differential pair #1, negative
7	SDP1_Drain	Drain wire for SDPp1 and SDPn1
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDP2_Drain	Drain wire for SDPp2 and SDPn2
Braid	Shield	Cable external braid

Note:

a. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are needed and the signal ground return is through the shields of the coaxial wires.

3.3.3 Wire Gauges and Cable Diameters (Informative)

This specification does not specify wire gauge. Table 3-8 and Table 3-9 list typical wire gauges for reference purposes only. A large gauge wire incurs less loss, but at the cost of cable diameter and flexibility. Multiple wires may be used for a single wire such as for VBUS or Ground. It is recommended to use the smallest possible wire gauges that meet the cable assembly electrical and mechanical requirements.

To maximize cable flexibility, all wires should be stranded and the cable outer diameter should be minimized as much as possible. A typical USB Full-Featured Type-C cable outer diameter may range from 4 mm to 6 mm while a typical *USB 2.0* Type-C cable outer diameter may range from 2 mm to 4 mm. A typical USB Type-C to *USB 3.1* legacy cable outer diameter may range from 3 mm to 5 mm.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28-34
5	UTP_Dn	28-34
6	SDPp1	26-34
7	SDPn1	26-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDPp3	26-34
11	SDPn3	26-34
12	SDPp4	26-34
13	SDPn4	26-34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

Table 3-9 Reference Wire Gauges for USB Type-C to Legacy Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28-34
4	UTP_Dn	28-34
5	SDPp1	26-34
6	SDPn1	26-34
7	SDP1_Drain	28-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDP2_Drain	28-34

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.4 Standard USB Type-C Cable Assemblies

Two standard USB Type-C cable assemblies are defined and allowed by this specification. In addition, captive cables are allowed (see Section 3.4.3). Shielding (braid) is required to enclose all the wires in the USB Type-C cable. The shield shall be terminated to the plug metal shells. The shield should be physically connected to the plug metal shell as close to 360° as possible, to control EMC.

3.4.1 USB Full-Featured Type-C Cable Assembly

Figure 3-21 shows a USB Full-Featured Type-C standard cable assembly.

Figure 3-21 USB Full-Featured Type-C Standard Cable Assembly

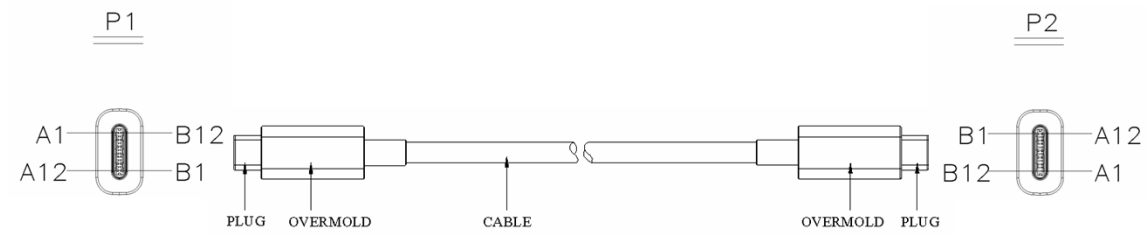


Table 3-10 defines the wire connections for the USB Full-Featured Type-C standard cable assembly.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	SSTXp1	6	SDPp1	B11	SSRXp1
A3	SSTXn1	7	SDPn1	B10	SSRXn1
B11	SSRXp1	8	SDPp2	A2	SSTXp1
B10	SSRXn1	9	SDPn2	A3	SSTXn1
B2	SSTXp2	10	SDPp3	A11	SSRXp2
B3	SSTXn2	11	SDPn3	A10	SSRXn2
A11	SSRXp2	12	SDPp4	B2	SSTXp2
A10	SSRXn2	13	SDPn4	B3	SSTXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. This table is based on the assumption that coaxial wire construction is used for all SDP's and there are no drain wires. The shields of the coaxial wires are connected to the ground pins. If shielded twisted pair is used, then drain wires are needed and shall be connected to the GND pins.
2. Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor (minimum voltage rating of 30 V) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad.
5. All GND pins shall be connected together within the USB Type-C plug.

3.4.2 USB 2.0 Type-C Cable Assembly

A *USB 2.0* Type-C standard cable assembly has the same form factor shown in Figure 3-21.

Table 3-11 defines the wire connections for the *USB 2.0* Type-C standard cable assembly.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is not required for the VBUS pin in the *USB 2.0* Type-C cable.
4. All GND pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.4.3 USB Type-C Captive Cable Assemblies

A captive cable assembly is a cable assembly that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end. The cable assembly that is hardwired is not detachable from the device.

The assembly wiring for captive USB Type-C cables follow the same wiring assignments as the standard cable assemblies (see Table 3-10 and Table 3-11) with the exception that the hardwired attachment on the device side substitutes for the USB Type-C Plug #2 end.

The CC wire in a captive cable shall be terminated and behave as appropriate to the function of the product to which it is captive (e.g. host or device).

This specification does not define how the hardwired attachment is physically done on the device side.

3.5 Legacy Cable Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy cable assemblies are defined. Only the cables defined within this specification are allowed.

Legacy cable assemblies that source power to a USB Type-C connector (e.g. a USB Type-C to USB Standard-A plug cable assembly and a USB Type-C plug to USB Micro-B receptacle adapter assembly) are required to use the Default USB Type-C Current Rp resistor (56 kΩ). The value of Rp is used to inform the Sink how much current the Source can provide. Since the legacy cable assembly does not comprehend the capability of the Source it is connected to, it is only allowed to advertise Default USB Type-C Current as defined by the *USB 2.0*, *USB 3.1* and *BC 1.2* specifications. No other Rp values are permitted because these may cause a USB Type-C Sink to overload a legacy power supply.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.1 USB Type-C to *USB 3.1* Standard-A Cable Assembly

Figure 3-22 shows a USB Type-C to *USB 3.1* Standard-A cable assembly.

Figure 3-22 USB Type-C to USB 3.1 Standard-A Cable Assembly

Table 3-12 defines the wire connections for the USB Type-C to *USB 3.1* Standard-A cable assembly.

Table 3-12 USB Type-C to *USB 3.1* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 2			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
A2	SSTXp1	5	SDPp1	6	StdA_SSRX+
A3	SSTXn1	6	SDPn1	5	StdA_SSRX–
B11	SSRXp1	8	SDPp2	9	StdA_SSTX+
B10	SSRXn1	9	SDPn2	8	StdA_SSTX–
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
2. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-15 for the functional description and value of Rp.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Standard-A plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly

Figure 3-23 shows a USB Type-C to *USB 2.0* Standard-A cable assembly.

Figure 3-23 USB Type-C to *USB 2.0* Standard-A Cable Assembly

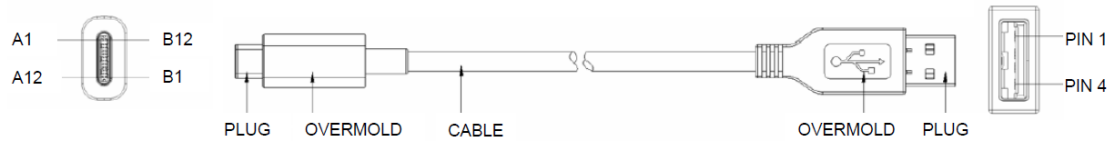


Table 3-13 defines the wire connections for the USB Type-C to *USB 2.0* Standard-A cable assembly.

Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-15 for the functional description and value of Rp.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly

Figure 3-24 shows a USB Type-C to *USB 3.1* Standard-B cable assembly.

Figure 3-24 USB Type-C to *USB 3.1* Standard-B Cable Assembly

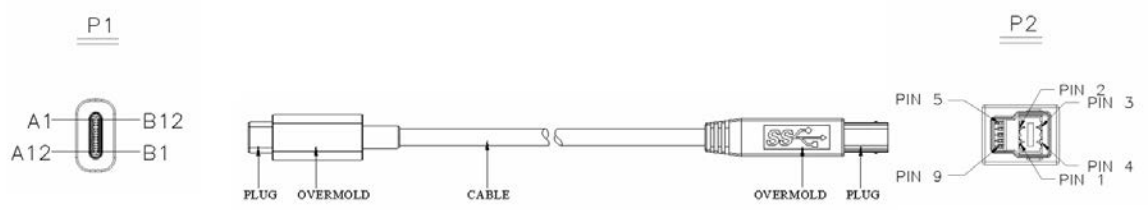


Table 3-14 defines the wire connections for the USB Type-C to *USB 3.1* Standard-B cable assembly.

Table 3-14 USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
A2	SSTXp1	5	SDPp1	9	StdB_SSRX+
A3	SSTXn1	6	SDPn1	8	StdB_SSRX–
B11	SSRXp1	8	SDPp2	6	StdB_SSTX+
B10	SSRXn1	9	SDPn2	5	StdB_SSTX–
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-16 for the functional description and value of Rd.
2. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Standard-B plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly

Figure 3-25 shows a USB Type-C to *USB 2.0* Standard-B cable assembly.

Figure 3-25 USB Type-C to *USB 2.0* Standard-B Cable Assembly

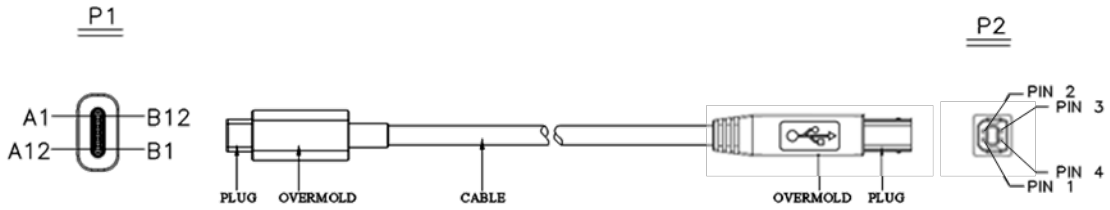


Table 3-15 defines the wire connections for the USB Type-C to *USB 2.0* Standard-B cable assembly.

Table 3-15 USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-16 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly

Figure 3-26 shows a USB Type-C to *USB 2.0* Mini-B cable assembly.

Figure 3-26 USB Type-C to *USB 2.0* Mini-B Cable Assembly

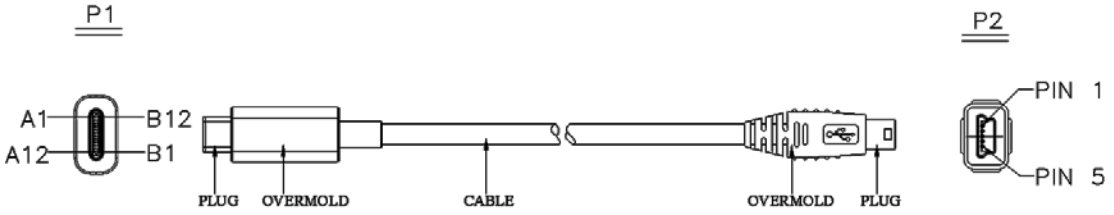


Table 3-16 defines the wire connections for the USB Type-C to *USB 2.0* Mini-B cable assembly.

Table 3-16 USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Mini-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
				4	ID
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin A5 of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-16 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the *USB 2.0* Mini-B plug shall be terminated as defined in the applicable specification for the cable type.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly

Figure 3-27 shows a USB Type-C to *USB 3.1* Micro-B cable assembly.

Figure 3-27 USB Type-C to *USB 3.1* Micro-B Cable Assembly

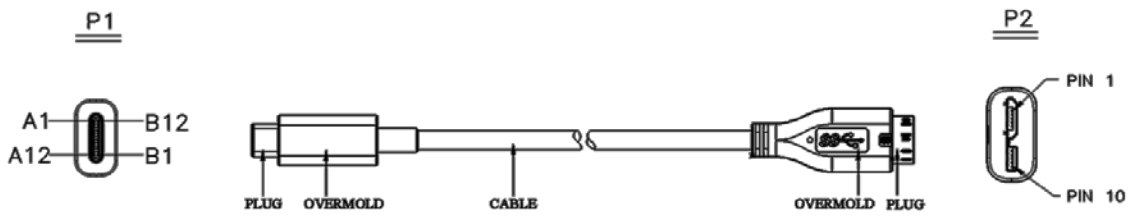


Table 3-17 defines the wire connections for the USB Type-C to *USB 3.1* Micro-B cable assembly.

Table 3-17 USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
A2	SSTXp1	5	SDPp1	10	MicB_SSRX+
A3	SSTXn1	6	SDPn1	9	MicB_SSRX–
B11	SSRXp1	8	SDPp2	7	MicB_SSTX+
B10	SSRXn1	9	SDPn2	6	MicB_SSTX–
				4	ID
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-16 for the functional description and value of Rd.
2. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Micro-B plug. The bypass capacitor should be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Pin 4 (ID) of the *USB 3.1* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly

Figure 3-28 shows a USB Type-C to *USB 2.0* Micro-B cable assembly.

Figure 3-28 USB Type-C to *USB 2.0* Micro-B Cable Assembly

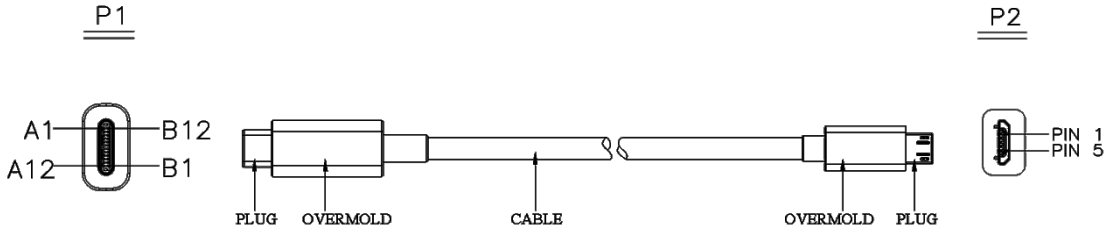


Table 3-18 defines the wire connections for the USB Type-C to *USB 2.0* Micro-B cable assembly.

Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-16 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the *USB 2.0* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.6 Legacy Adapter Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy adapter assemblies are defined. Only the adapter assemblies defined in this specification are allowed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

Figure 3-29 shows a USB Type-C to *USB 3.1* Standard-A receptacle adapter assembly. This cable assembly is defined for direct connect to a USB device (e.g., a thumb drive). System functionality of using this adaptor assembly together with another USB cable assembly is not guaranteed.

Figure 3-29 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

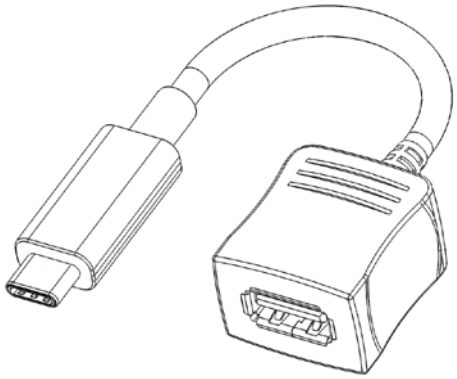


Table 3-19 defines the wire connections for the USB Type-C to *USB 3.1* Standard-A receptacle adapter assembly.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-19 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Wiring

USB Type-C Plug		USB 3.1 Standard-A receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
B5	VCONN		
A6	Dp1	3	D+
A7	Dn1	2	D–
A2	SSTXp1	9	StdA_SSTX+
A3	SSTXn1	8	StdA_SSTX–
B11	SSRXp1	6	StdA_SSRX+
B10	SSRXn1	5	StdA_SSRX–
Shell	Shield	Shell	Shield

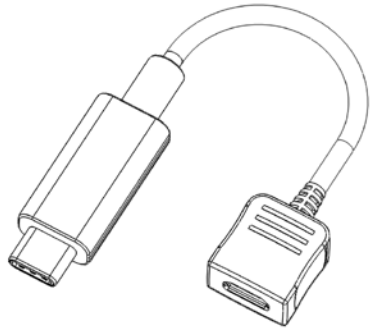
Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-16 for the functional description and value of Rd.
2. This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor is required for the VBUS pin in the USB Type-C plug end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad. A bypass capacitor is not required for the VBUS pin in the Standard-A receptacle.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

Figure 3-29 shows a USB Type-C to *USB 2.0* Micro-B receptacle adapter assembly.

Figure 3-30 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-19 defines the wire connections for the USB Type-C to *USB 2.0* Micro-B receptacle adapter assembly.

Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring

USB Type-C Plug		USB 2.0 Micro-B receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	5	GND
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
A6	Dp1	3	D+
A7	Dn1	2	D–
		4	ID
Shell	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-15 for the functional description and value of Rp.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins at the Micro-B receptacle end of this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.7 Electrical Characteristics

This section defines the USB Type-C raw cable, connector, and cable assembly electrical requirements, including signal integrity, shielding effectiveness, and DC requirements. Chapter 4 defines additional requirements regarding functional signal definition, host/device discovery and configuration, and power delivery.

Unless otherwise specified, all measurements are made at a temperature of 15° to 35° C, a relative humidity of 25% to 85%, and an atmospheric pressure of 86 to 106 kPa and all S-parameters are normalized with an 85 Ω differential impedance.

3.7.1 Raw Cable (Informative)

Informative raw cable electrical performance targets are provided to help cable assembly manufacturers manage the procurement of raw cable. These targets are not part of the USB Type-C compliance requirements. The normative requirement is that the cable assembly meets the performance characteristics specified in Sections 3.7.2, 3.7.4, and 3.7.4.3.

The differential characteristic impedance for shielded differential pairs is recommended to be 90 Ω ± 5 Ω. The single-ended characteristic impedance of coaxial wires is recommended to be 45 Ω ± 3 Ω. The impedance should be evaluated using a 200 ps (10%-90%) rise time; a faster rise time is not necessary for raw cable since it will make cable test fixture discontinuities more prominent.

3.7.1.1 Intra-Pair Skew (Informative)

The intra-pair skew for a differential pair is recommended to be less than 10 ps/m. It should be measured with a Time Domain Transmission (TDT) in a differential mode using a 200 ps (10%-90%) rise time with a crossing at 50% of the input voltage.

3.7.1.2 Differential Insertion Loss (Informative)

Cable loss depends on wire gauges, plating and dielectric materials. Table 3-21 and Table 3-22 show examples of differential insertion losses.

Table 3-21 Differential Insertion Loss Examples for USB SuperSpeed with Twisted Pair Construction

Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.4 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.5 dB/m	−2.0 dB/m	−1.7 dB/m	−1.4 dB/m
2.50 GHz	−3.7 dB/m	−2.9 dB/m	−2.5 dB/m	−2.1 dB/m
5.00 GHz	−5.5 dB/m	−4.5 dB/m	−3.9 dB/m	−3.1 dB/m
7.50 GHz	−7.0 dB/m	−5.9 dB/m	−5.0 dB/m	−4.1 dB/m
10.00 GHz	−8.4 dB/m	−7.2 dB/m	−6.1 dB/m	−4.8 dB/m
12.50 GHz	−9.5 dB/m	−8.2 dB/m	−7.3 dB/m	−5.5 dB/m
15.00 GHz	−11.0 dB/m	−9.5 dB/m	−8.7 dB/m	−6.5 dB/m

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-22 Differential Insertion Loss Examples for USB SuperSpeed with Coaxial Construction

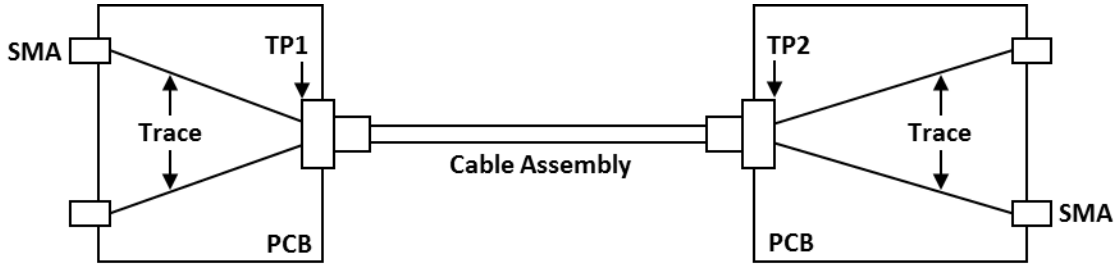
Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.5 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.8 dB/m	−2.2 dB/m	−1.8 dB/m	−1.3 dB/m
2.50 GHz	−4.2 dB/m	−3.4 dB/m	−2.7 dB/m	−1.9 dB/m
5.00 GHz	−6.1 dB/m	−4.9 dB/m	−4.0 dB/m	−3.1 dB/m
7.50 GHz	−7.6 dB/m	−6.5 dB/m	−5.2 dB/m	−4.2 dB/m
10.0 GHz	−8.8 dB/m	−7.6 dB/m	−6.1 dB/m	−4.9 dB/m
12.5 GHz	−9.9 dB/m	−8.6 dB/m	−7.1 dB/m	−5.7 dB/m
15.0 GHz	−12.1 dB/m	−10.9 dB/m	−9.0 dB/m	−6.5 dB/m

3.7.2 USB Type-C to Type-C Passive Cable Assemblies (Normative)

A USB Type-C to Type-C cable assembly shall be tested using a test fixture with the receptacle tongue fabricated in the test fixture. This is illustrated in Figure 3-31. The USB Type-C receptacles are not present in the test fixture. Hosts and devices should account for the additional signal degradation the receptacle introduces.

The requirements are for the entire signal path of the cable assembly mated with the fixture PCB tongues, not including lead-in PCB traces. As illustrated in Figure 3-31, the measurement is between TP1 (test point 1) and TP2 (test point 2). Refer to documentation located at Cable Assembly and Connector Test Requirements page on the USB-IF website for a detailed description of a standardized test fixture.

Figure 3-31 Illustration of Test Points for a Mated Cable Assembly



The cable assembly requirements are divided into informative and normative requirements. The informative requirements are provided as design targets for cable assembly manufacturers. The normative requirements are the pass/failure criteria for cable assembly compliance.

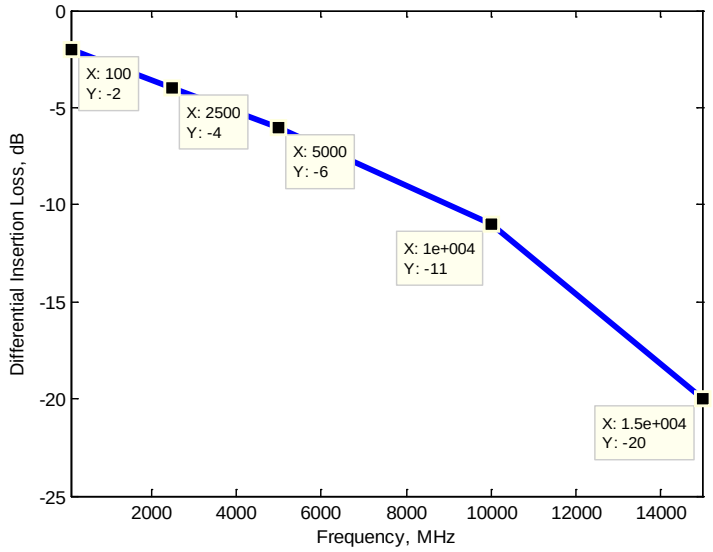
3.7.2.1 Recommended USB SuperSpeed Passive Cable Assembly Characteristics

3.7.2.1.1 Differential Insertion Loss (Informative)

Figure 3-32 shows the differential insertion loss limit for a *USB 3.1* Gen 2 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −2 dB), (2.5 GHz, −4 dB), (5.0 GHz, −6 dB), (10 GHz, −11 dB) and (15 GHz, −20 dB).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

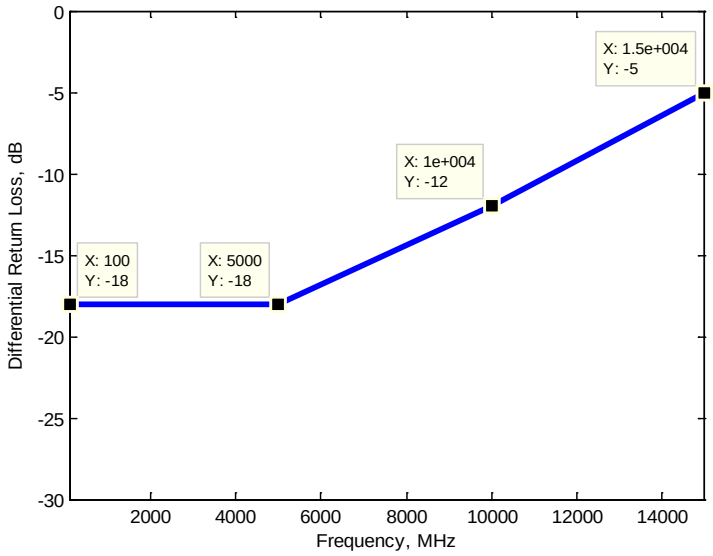
Figure 3-32 Recommended Differential Insertion Loss Requirement



3.7.2.1.2 Differential Return Loss (Informative)

Figure 3-33 shows the differential return loss limit, which is defined by the following points: (100 MHz, -18 dB), (5 GHz, -18 dB), (10 GHz, -12 dB), and (15 GHz, -5 dB).

Figure 3-33 Recommended Differential Return Loss Requirement

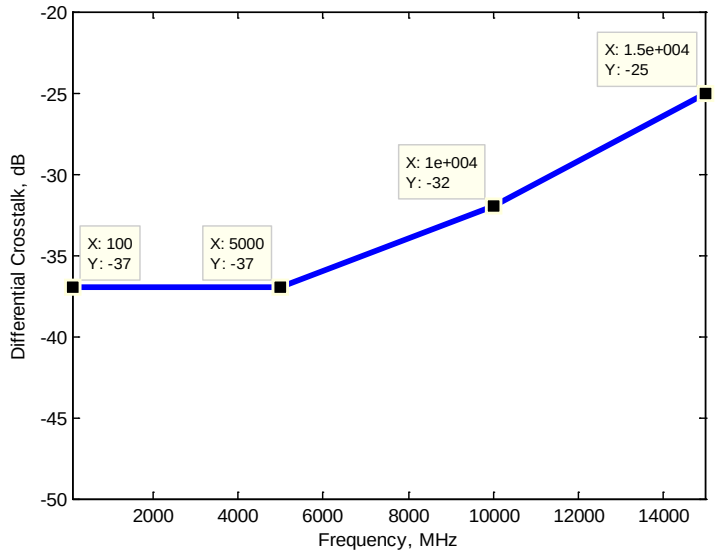


3.7.2.1.3 Differential Near-End and Far-End Crosstalk between SuperSpeed Pairs (Informative)

Both the near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are specified, as shown in Figure 3-34. The DDNEXT/DDFEXT limits are defined by the following vertices: (100 MHz, -37 dB), (5 GHz, -37 dB), (10 GHz, -32 dB), and (15 GHz, -25 dB).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

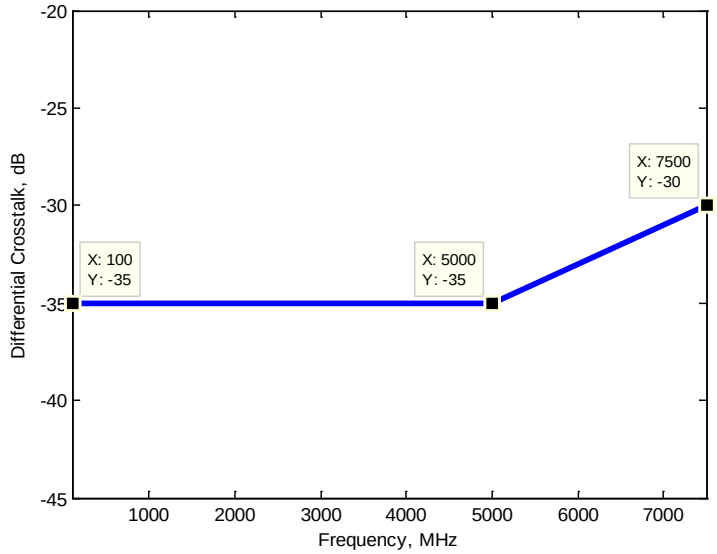
Figure 3-34 Recommended Differential Crosstalk Requirement



3.7.2.1.4 Differential Crosstalk between USB D+/D– and USB SuperSpeed Pairs (Informative)

The differential near-end and far-end crosstalk between the USB D+/D– pair and the USB SuperSpeed pairs should be managed not to exceed the limits shown in Figure 3-35. The limits are defined by the following points: (100 MHz, -35 dB), (5 GHz, -35 dB), and (7.5 GHz, -30 dB).

Figure 3-35 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D– Pair and USB SuperSpeed Pair



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

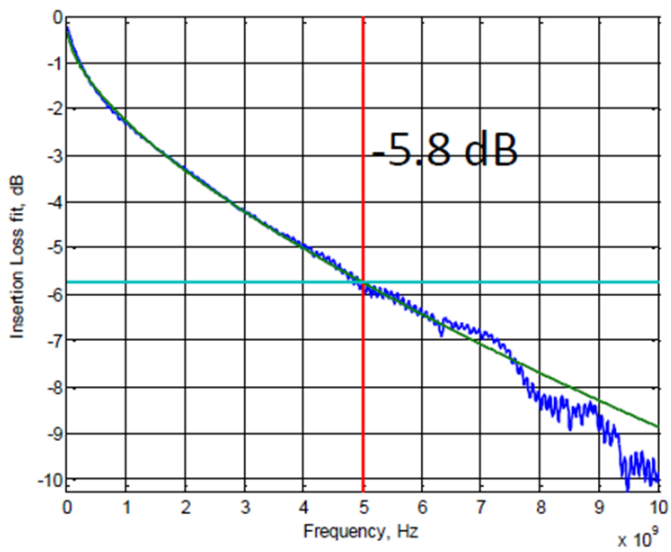
3.7.2.2 Normative SuperSpeed Passive Cable Assembly Requirements

The integrated parameters are used for cable assembly compliance (except for insertion loss and differential-to-common-mode conversion) to avoid potential rejection of a functioning cable assembly that may fail the traditional S-parameters spec at a few frequencies.

3.7.2.2.1 Insertion Loss Fit at Nyquist Frequencies (Normative)

The insertion loss fit at Nyquist frequency measures the attenuation of the cable assembly. To obtain the insertion loss fit at Nyquist frequency, the measured cable assembly differential insertion loss is fitted with a smooth function. A standard fitting algorithm and tool shall be used to extract the insertion loss fit at Nyquist frequencies. Refer to documentation located at Cable Assembly and Connector Test Requirements page on the USB-IF website for a more detailed description about insertion loss fit. Figure 3-36 illustrates an example of a measured cable assembly insertion loss fitted with a smooth function; the insertion loss fit at the Nyquist frequency of USB SuperSpeed Gen 2 (5.0 GHz) is −5.8 dB.

Figure 3-36 Illustration of Insertion Loss Fit at Nyquist Frequency



The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

- ≥ −4 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz, and
- ≥ −11 dB at 10 GHz.

2.5 GHz, 5.0 GHz and 10 GHz are the Nyquist frequencies for USB SuperSpeed Gen 1, USB SuperSpeed Gen 2, and a possible future 20 Gbps USB data rate, respectively.

The USB SuperSpeed Gen 1-only Type-C to Type-C cable assembly is allowed by this specification and shall comply with the following insertion loss fit at Nyquist frequency requirements:

- ≥ −7.0 dB at 2.5 GHz, and
- > −12 dB at 5 GHz.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

This insertion fit at Nyquist frequency allows the USB SuperSpeed Gen 1-only Type-C to Type-C cable assembly to achieve an overall length of approximately 2 meters.

3.7.2.2.2 Integrated Multi-reflection (Normative)

The insertion loss deviation, ILD, is defined as

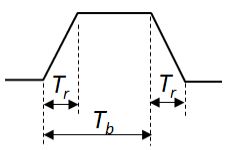
$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of *ILD(f)* is called the integrated multi-reflection (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{fmax}|ILD(f)|^2|Vin(f)|^2df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

where *fmax* = 12.5 GHz and *Vin(f)* is the input trapezoidal pulse spectrum, defined in Figure 3-37.

Figure 3-37 Input Pulse Spectrum



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

T_b=Unit interval=100 ps
T_r=0 to 100% rise time = 0.4T_b

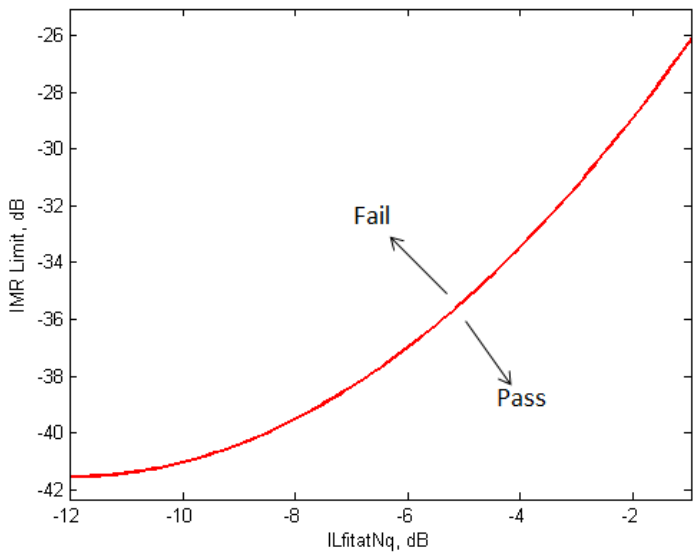
IMR has dependency on ILfitatNq. More IMR may be tolerated when ILfitatNq decreases. The IMR limit is specified as a function of ILfitatNq:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392.$$

This is plotted in Figure 3-38.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-38 IMR Limit as Function of ILfitatNq



3.7.2.2.3 Integrated Crosstalk between SuperSpeed Pairs (Normative)

The integrated crosstalk between all USB SuperSpeed pairs is calculated with the following equations:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 (|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) df + |Vdd(f)|^2 \, |NEXTd(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 (|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) df + |Vdd(f)|^2 \, |FEXTd(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where *NEXT(f)*, *FEXT(f)*, and *C2D(f)* are the measured near-end and far-end crosstalk between USB SuperSpeed pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. *NEXTd(f)* and *FEXTd(f)* are, respectively, the near-end and far-end crosstalk from the D+/D− pair to SuperSpeed pairs. *Vdd(f)* is the input pulse spectrum evaluated using the equation in Figure 3-37 with Tb=2.08 ns.

The integration shall be done for each NEXT and FEXT between all differential pairs. The largest values of INEXT and IFEXT shall meet the following requirements:

- INEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,
- IFEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.

The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four SuperSpeed pairs transmit or receive signals simultaneously, for example in an Alternate Mode.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Crosstalk from the USB SuperSpeed pairs to USB 2.0 D+/D− shall be controlled to ensure the robustness of the USB 2.0 link. Since USB Type-C to Type-C Full-Featured cable assemblies may support the usage of USB SuperSpeed or an alternate mode (e.g., DisplayPort), the crosstalk from the four high speed differential pairs to D+/D− may be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D− is calculated with the following equations:

$$\text{IDDXT_1NEXT + FEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |Vin(f)|^2\,|FEXT(f)|^2 df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

where:

NEXT = Near-end crosstalk from USB SuperSpeed TX pair to D+/D−

FEXT = Far-end crosstalk from USB SuperSpeed RX pair to D+/D−

fmax = 1.2 GHz

$$\text{IDDXT_2NEXT } = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |Vin(f)|^2\,|NEXT2(f)|^2 df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

where:

NEXT1 = Near-end crosstalk from USB SuperSpeed TX pair to D+/D−

NEXT2 = Near-end crosstalk from USB SuperSpeed RX (the RX functioning in TX mode) pair to D+/D−

fmax = 1.2 GHz

The integration shall be done for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement. The integrated differential crosstalk on D+/D− shall meet the following requirements:

- IDDXT_1NEXT + FEXT ≤ −34.5 dB,
- IDDXT_2NEXT ≤ −33 dB.

3.7.2.2.4 Integrated Return Loss (Normative)

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB\left(\sqrt{\frac{\int_0^{fmax}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2 + |SDD22(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

where *SDD21(f)* is the measured cable assembly differential insertion loss, *SDD11(f)* and *SDD22(f)* are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

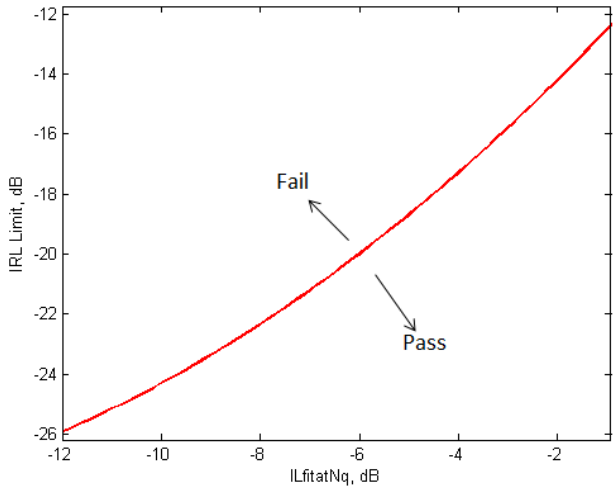
The IRL also has a strong dependency on ILfitatNq, and its limit is specified as a function of ILfitatNq:

$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 10.784.$

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

It is shown in Figure 3-39.

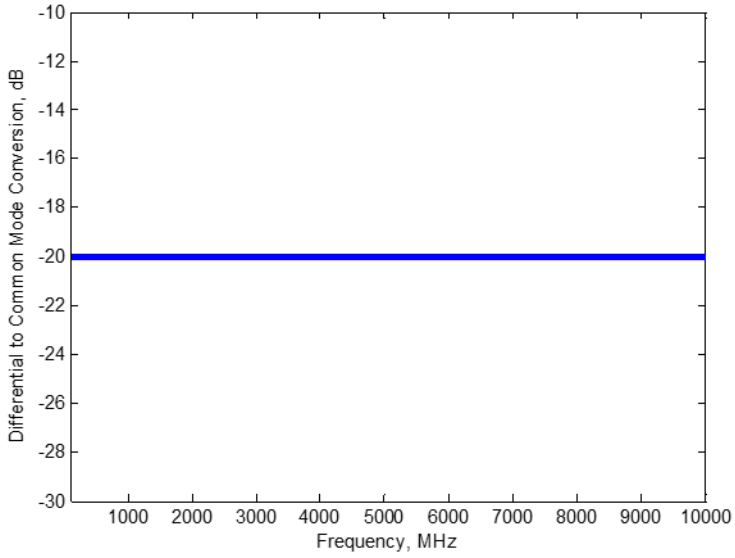
Figure 3-39 IRL Limit as Function of ILfitatNq



3.7.2.2.5 Differential-to-Common-Mode Conversion (Normative)

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Figure 3-40 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −20 dB from 100 MHz to 10 GHz.

Figure 3-40 Differential-to-Common-Mode Conversion Requirement



3.7.2.3 Low-Speed Signal Requirements (Normative)

This section specifies the electrical requirements for CC and SBU wires and the coupling among CC, USB D+/D−, VBUS and SBU.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The CC and SBU wires may be unshielded or shielded, and shall have the properties specified in Table 3-23.

Table 3-23 Electrical Requirements for CC and SBU wires

Name	Description	Min	Max	Units
zCable_CC	Cable characteristic impedance on the CC wire	32	93	Ω
rCable_CC	Cable DC resistance on the CC wire		15	Ω
tCableDelay_CC	Cable propagation delay on the CC wire		26	ns
cCablePlug_CC	Capacitance for each cable plug on the CC wire		25	pF
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wires		26	ns

Coupling or crosstalk, both near-end and far-end, among the low speed signals shall be controlled. Table 3-24 shows the matrix of couplings specified.

Table 3-24 Coupling Matrix for Low Speed Signals

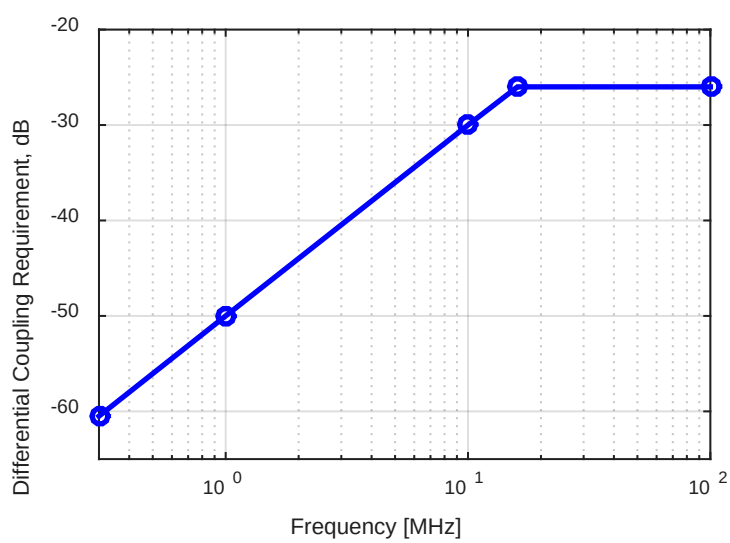
Coupling Matrix	D− (SE)	D+/D− (DF)	VBUS	SBU_B/SBU_A (SE)
CC	FF, CT	FF, CT	FF, CT	FF
D+/D− (DF)	N/A	N/A	FF, CT	FF
SBU_A/SBU_B	N/A	FF	FF	FF

DF: Differential; FF: Full-featured cable; CT: Charge-through cable (including USB 2.0 function).

3.7.2.3.1 CC to USB D+/D− (Normative)

The differential coupling between the CC and D+/D− shall be below the limit shown in Figure 3-41. The limit is defined with the vertices of (0.3 MHz, -60.5 dB), (1 MHz, −50 dB), (10 MHz, −30 dB), (16 MHz, −26 dB) and (100 MHz, −26 dB).

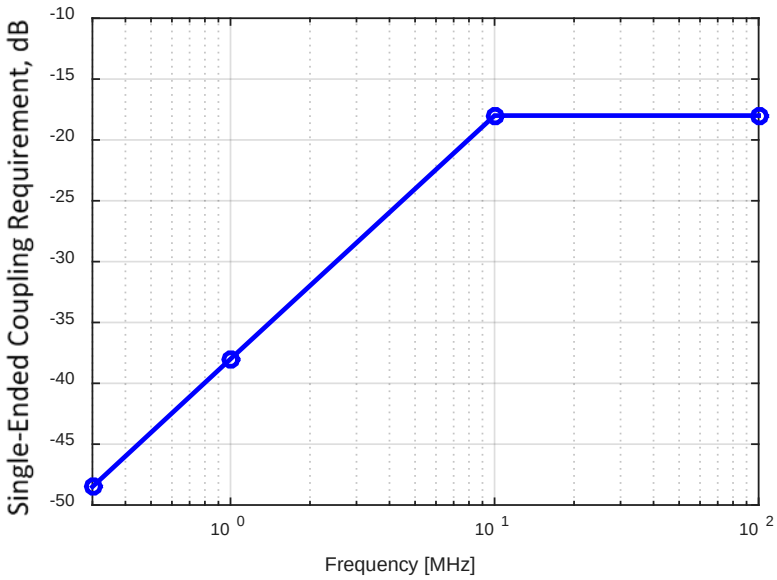
Figure 3-41 Requirement for Differential Coupling between CC and D+/D−



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

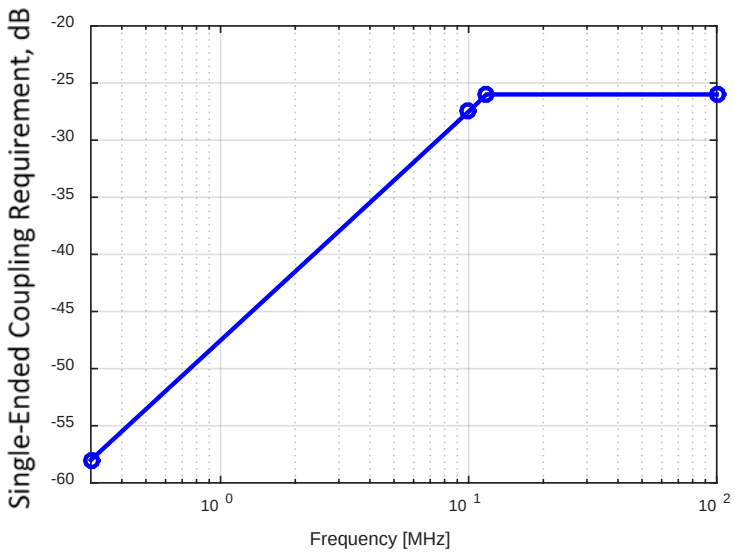
For USB 2.0 Type-C cables, the singled-ended coupling between the CC and D− shall be below the limit shown in Figure 3-42. The limit is defined with the vertices of (0.3 MHz, −48.5 dB), (1 MHz, −38 dB), (10 MHz, −18 dB) and (100 MHz, −18 dB).

Figure 3-42 Requirement for Single-Ended Coupling between CC and D− in USB 2.0 Type-C Cables



For USB Full-Featured Type-C cables, the singled-ended coupling between the CC and D− shall be below the limit shown in Figure 3-43. The limit is defined with the vertices of (0.3 MHz, −8 dB), (10 MHz, −27.5 dB), (11.8 MHz, −26 dB) and (100 MHz, −26 dB).

Figure 3-43 Requirement for Single-Ended Coupling between CC and D− in USB Full-Featured Type-C Cables

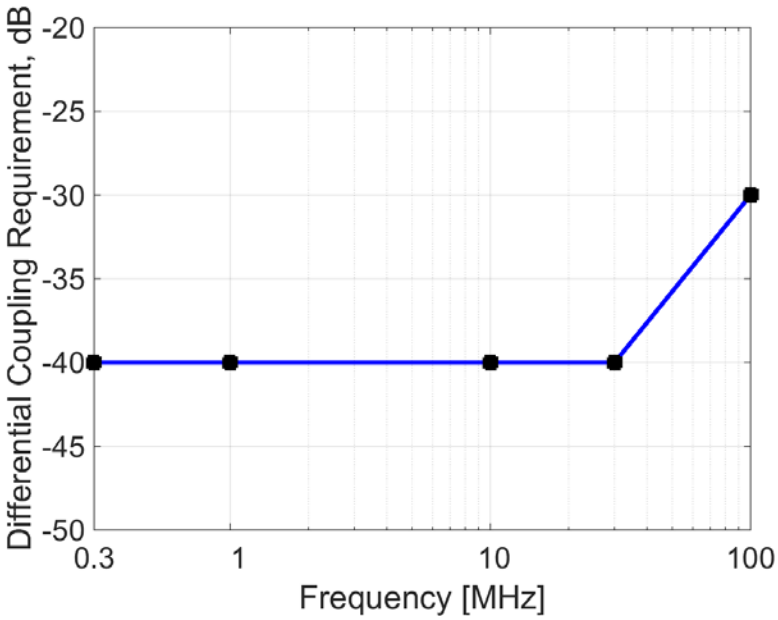


Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.7.2.3.2 VBUS Coupling to SBU_A/SBU_B, CC, and USB D+/D− (Normative)

The differential coupling between VBUS and USB D+/D− shall be less than the limit shown in Figure 3-44. The limit is defined by the following vertices: (0.3 MHz, −40 dB), (1 MHz, −40 dB), (30 MHz, −40 dB), and (100 MHz, −30 dB).

Figure 3-44 Requirement for Differential Coupling between VBUS and D+/D−



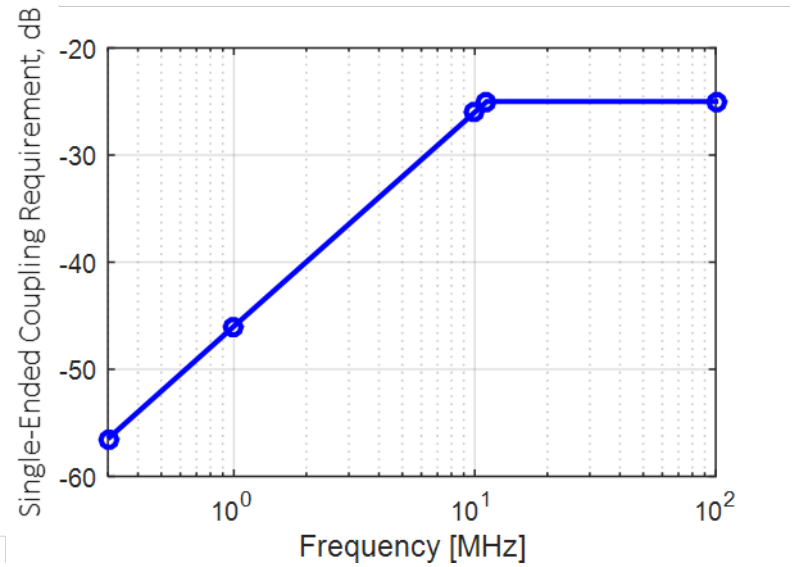
The loop inductance of VBUS and its coupling factor to low speed lines is controlled to limit noise induced on low speed signaling lines. The maximum loop inductance of VBUS shall be 900 nH and the maximum mutual inductance coupling factor (k) between VBUS and low speed signal lines (CC, SBU_A, SBU_B, D+, D−) shall be 0.3. For fully featured cables, the range of VBUS bypass capacitance shall be 8nF up to 500nF as any of the values in the range is equally effective for high-speed return-path bypassing.

3.7.2.3.3 Coupling between SBU_A and SBU_B (Normative)

The single-ended coupling between SBU_A and SBU_B shall be less than the limit shown in Figure 3-45. The limit is defined with the vertices of (0.3 MHz, −56.5 dB), (1 MHz, −46 dB), (10 MHz, −26 dB), (11.2 MHz, −25 dB), and (100 MHz, −25 dB).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

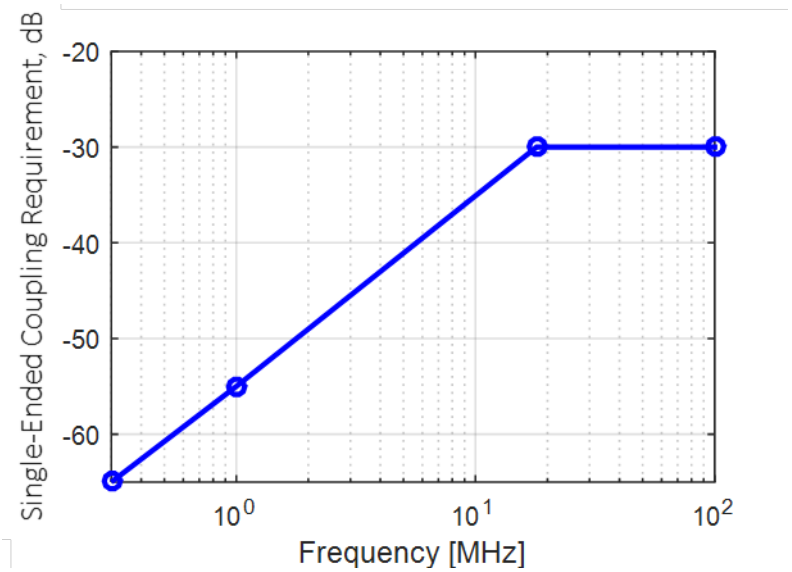
Figure 3-45 Requirement for Single-Ended Coupling between SBU_A and SBU_B



3.7.2.3.4 Coupling between SBU_A/SBU_B and CC (Normative)

The single-ended coupling between SBU_A and CC, and between SBU_B and CC shall be less than the limit shown in Figure 3-46. The limit is defined with the vertices of (0.3 MHz, -65 dB), (1 MHz, −55 dB), (18 MHz, −30 dB), and (100 MHz, −30 dB).

Figure 3-46 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC

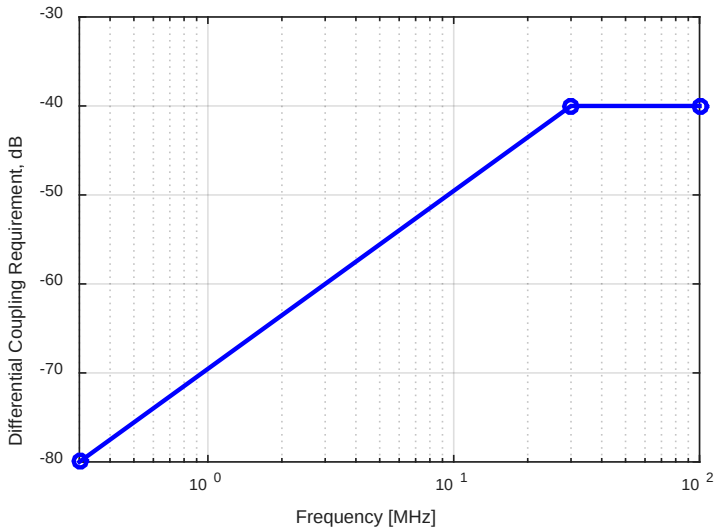


3.7.2.3.5 Coupling between SBU_A/SBU_B and USB D+/D− (Normative)

The coupling between SBU_A and differential D+/D−, and between SBU_B and differential D+/D− shall be less than the limit shown in Figure 3-47. The limit is defined with the vertices of (0.3 MHz, -80 dB), (30 MHz, −40 dB), and (100 MHz, −40 dB).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-47 Requirement for Coupling between SBU_A and differential D+/D−, and SBU_B and differential D+/D−



3.7.2.4 USB D+/D− Signal Requirements (Normative)

The USB D+/D− lines of the USB Type-C to USB Type-C passive cable assembly shall meet the requirements defined in Table 3-25.

Table 3-25 USB D+/D− Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	26 ns max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz

3.7.2.5 VBUS DC Voltage Tolerance (Normative)

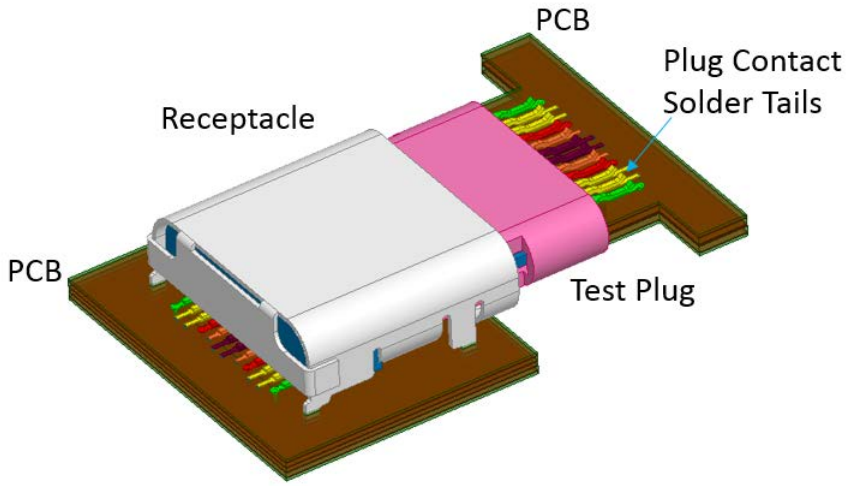
A USB Type-C to USB Type-C cable assembly shall tolerate a VBUS voltage of 21 V DC at the cable rated current (i.e. 3 A or 5 A) applied for one hour as a pre-condition of the testing of the electrical aspects of the cable assembly.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.7.3 Mated Connector (Informative)

The mated connector as defined in this specification for USB Type-C consists of a receptacle mounted on a PCB, representing how the receptacle is used in a product, and a test plug also mounted on a PCB (paddle card) without cable. This is illustrated in Figure 3-48. Note that the test plug is used in host/device TX/RX testing also.

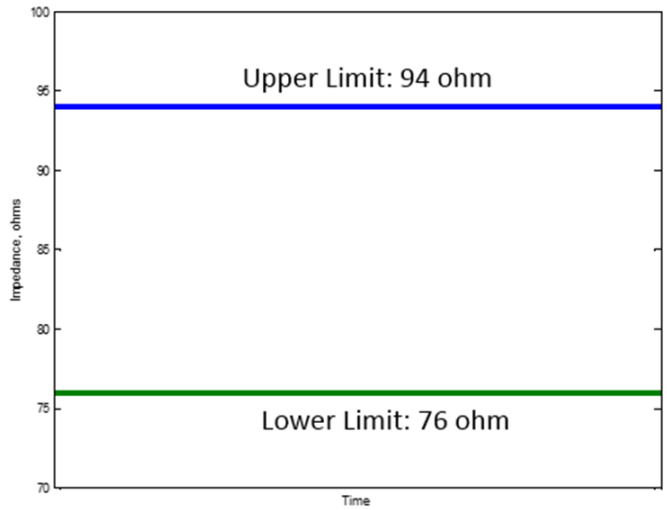
Figure 3-48 Illustration of USB Type-C Mated Connector



3.7.3.1 Differential Impedance (Informative)

The mated connector impedance target is specified to minimize reflection from the connector. The differential impedance of a mated connector should be within 85 Ω ± 9 Ω, as seen from a 40 ps (20% – 80%) rise time. The impedance profile of a mated connector should fall within the limits shown in Figure 3-49.

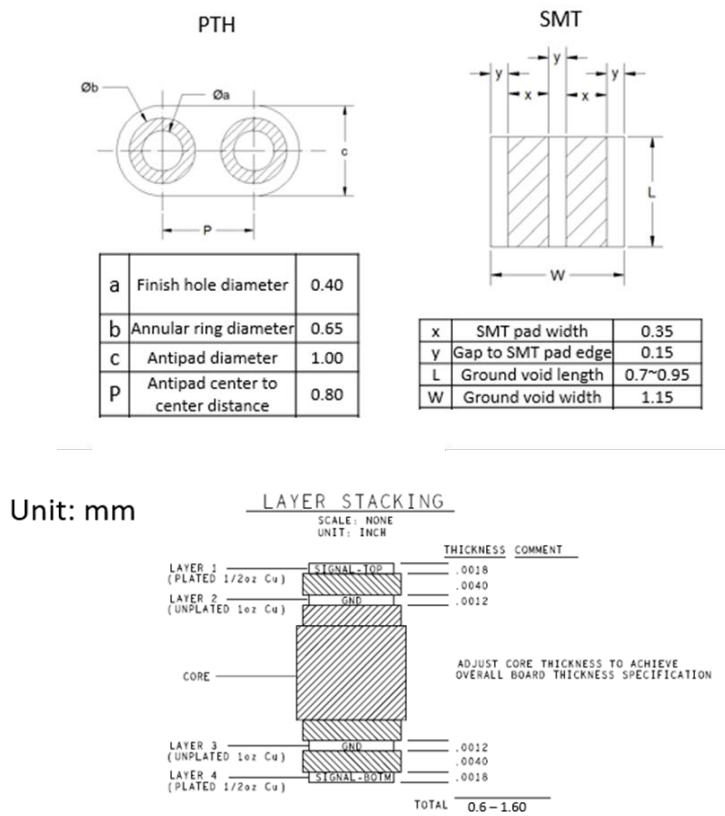
Figure 3-49 Recommended Impedance Limits of a USB Type-C Mated Connector



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The PCB stack up, lead geometry, and solder pad geometry should be modeled in 3D field-solver to optimize electrical performance. Example ground voids under signal pads are shown in Figure 3-50 based on pad geometry, mounting type, and PCB stack-up shown.

Figure 3-50 Recommended Ground Void Dimensions for USB Type-C Receptacle



3.7.3.2 Mated Connector Recommended Differential S-Parameter and Signal Integrity Characteristics (Informative)

The recommended signal integrity characteristics of USB Type-C mated connector pair are listed in Table 3-26.

Table 3-26 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (Informative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen 1, Gen 2 and future 20 Gbps generation Nyquist frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB at 5.0 GHz ≥ −1.0 dB @ 10 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −40 dB

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 89
Microchip v. Aptiv
IPR2024-00496

Items	Descriptions and Procedures	Requirements
Integrated Differential Near-end Crosstalk on SuperSpeed (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \lvert Vdd(f)\rvert^2 \lvert NEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = NEXT between SuperSpeed pairs $NEXTd$ = NEXT between D+/D− and SuperSpeed pairs	≤ −44 dB
Integrated Differential Far-end Crosstalk on SuperSpeed (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 + 0.125^2 \cdot \lvert C2D(f)\rvert^2)df + \lvert Vdd(f)\rvert^2 \lvert FEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: $FEXT$ = NEXT between SuperSpeed pairs $FEXTd$ = NEXT between D+/D− and SuperSpeed pairs	≤ −44 dB
Differential Crosstalk on D+/D-	The differential near-end and far-end crosstalk between the D+/D− pair and the SuperSpeed pairs in mated connectors.	See Figure 3-51
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2 + \lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −18 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	See Figure 3-52

Note: *fmax* = 12.5 GHz (unless otherwise specified);

Vin(f) is defined in Figure 3-37 with Tb (UI) = 100 ps;

Vdd(f) is also defined in Figure 3-37 with Tb (UI) = 2.08 ns.

C2D(f) =measured near-end and far-end crosstalk between USB SuperSpeed pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-51 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D– Pair and SuperSpeed Pairs

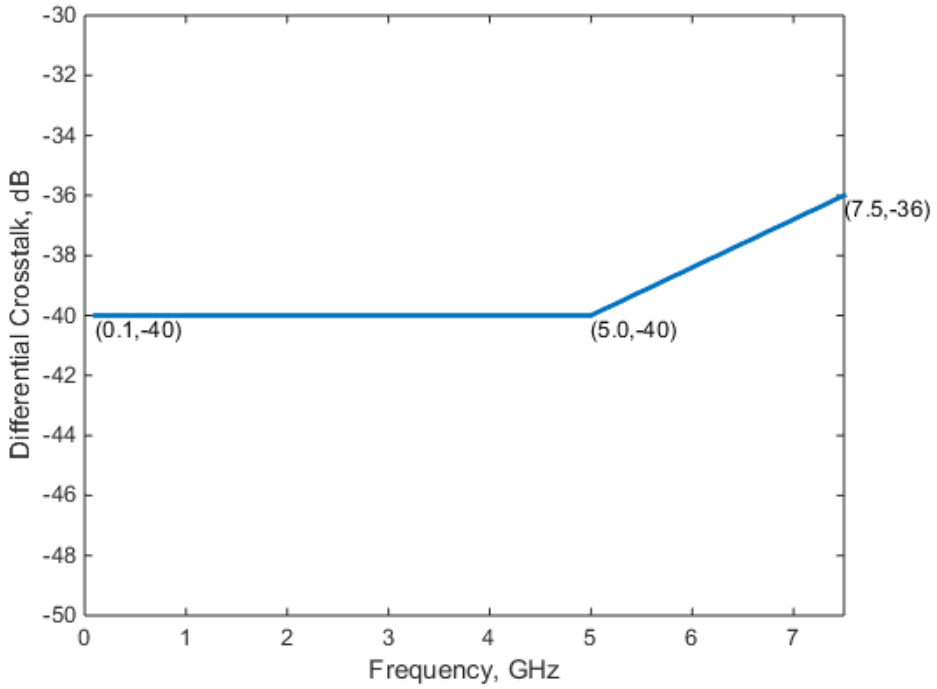
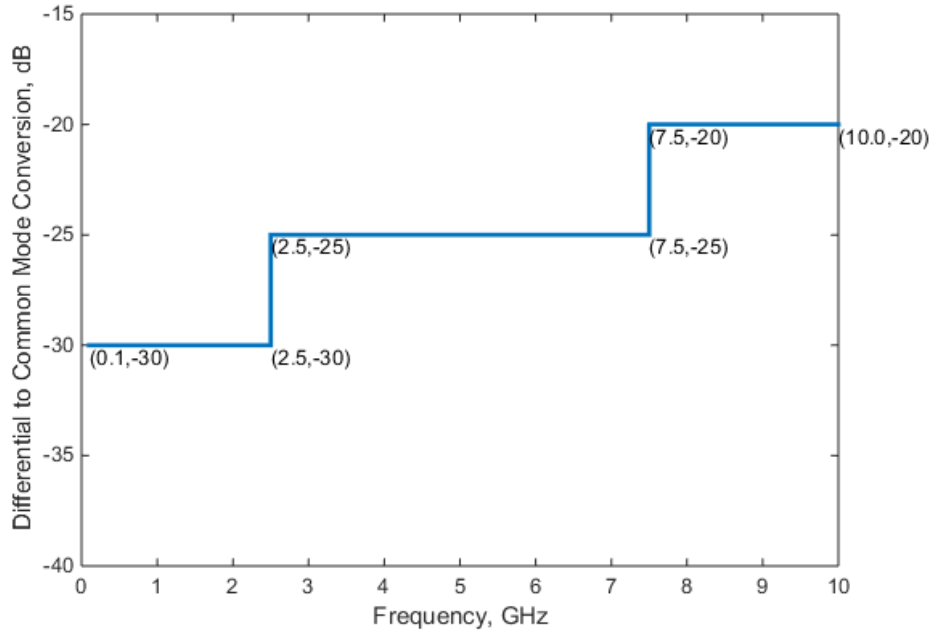


Figure 3-52 Recommended Limits for Differential-to-Common-Mode Conversion



3.7.4 USB Type-C to Legacy Cable Assemblies (Normative)

The USB Type-C to legacy cable assemblies may support *USB 2.0* only or *USB 3.1* Gen 2; *USB 3.1* Gen 1-only Type-C to legacy cable assemblies are not allowed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.7.4.1 USB 2.0-only Cable Assemblies (Normative)

The *USB 2.0*-only Type-C to legacy USB cable assemblies include:

- USB Type-C plug to *USB 2.0* Standard-A plug
- USB Type-C plug to *USB 2.0* Standard-B plug
- USB Type-C plug to *USB 2.0* Micro-B plug
- USB Type-C plug to *USB 2.0* Mini-B plug

The USB D+/D− signal integrity requirements are specified in Table 3-27.

Table 3-27 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	10 ns max for USB Type-C to Micro-B cable assembly; 20 ns max for all other USB Type-C to legacy USB cable assemblies. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz

3.7.4.2 *USB 3.1* Gen 2 Cable Assemblies (Normative)

The USB Type-C to *USB 3.1* Gen 2 legacy cable assemblies include:

- USB Type-C plug to *USB 3.1* Standard-A plug
- USB Type-C plug to *USB 3.1* Standard-B plug
- USB Type-C plug to *USB 3.1* Micro-B plug

The informative design targets for these cables are provided in Table 3-28.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-28 Design Targets for USB Type-C to *USB 3.1* Gen 2 Legacy Cable Assemblies (Informative)

Items	Design Targets
Differential Impedance	76 ohms min and 96 ohms max. 40 ps rise time (20%-80%).
Differential Insertion Loss	≥ −2 dB @ 100 MHz ≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥−3.5 dB @ 2.5 GHz −6.0 dB max @ 5.0 GHz
Differential NEXT between SuperSpeed Pairs	≤ −34 dB to 5 GHz
Differential NEXT and FEXT between D+/D- and SuperSpeed Pairs	≤ −30 dB to 5 GHz

The normative requirements include the USB D+/D− signaling as specified in Table 3-27, and the USB SuperSpeed parameters specified in Table 3-29.

Table 3-29 USB Type-C to *USB 3.1* Gen 2 Legacy Cable Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen 1 and Gen 2 Nyquist frequencies.	≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥ −3.5 dB @ 2.5 GHz ≥ −6.0 dB at 5.0 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 21.392$ See Figure 3-53.
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXTs* = NEXT between SuperSpeed pairs *NEXTd* = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-37 with Tb (UI) = 2.08 ns.	≤ −38 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXT(f)\rvert^2 + \lvert Vin(f)\rvert^2\lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = Near-end crosstalk from SuperSpeed to D+/D− *FEXT* = Far-end crosstalk from SuperSpeed to D+/D− *fmax* = 7.5 GHz	≤ −28.5 dB

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Items	Descriptions and Procedures	Requirements
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.046\cdot ILfitatNq^2 + 1.812\cdot ILfitatNq - 9.784$ See Figure 3-54.
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

Note: *fmax* = 10 GHz (unless otherwise specified); *Vin(f)* is defined in Figure 3-37 with Tb (UI) = 100 ps; and *Vdd(f)* is also defined in Figure 3-37 with Tb (UI) = 2.08 ns.

Figure 3-53 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly

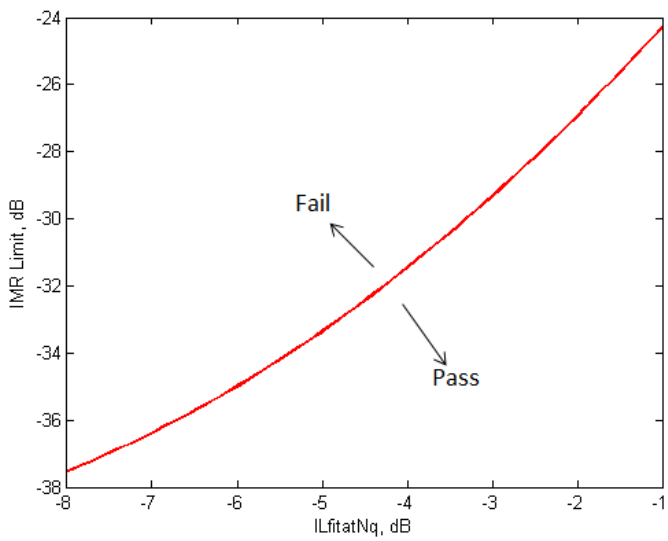
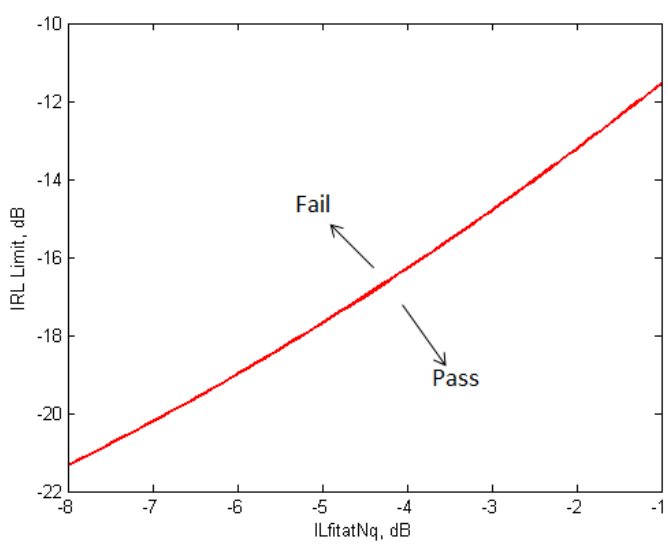


Figure 3-54 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.7.4.3 Compliant USB Legacy Plugs used in USB Type-C to Legacy Cable Assemblies

The following requirements are incremental to the existing requirements for legacy connectors when used in compliant USB Type-C to legacy cable assemblies.

3.7.4.3.1 Contact Material Requirements for USB Type-C to USB Micro-B Assemblies

For USB Type-C to USB Micro-B assemblies, change the contact material in the USB Micro-B connector to achieve the following Low Level Contact Resistance (EIA 364-23B):

- 20 milliohms (Max) initial for VBUS and GND contacts,
- Maximum change (delta) of +10 milliohms after environmental stresses.

3.7.4.3.2 Contact Current Ratings for USB Standard-A, USB Standard-B and USB Micro-B Connector Mated Pairs (EIA 364-70, Method 2)

When a current of 3 A is applied to the VBUS pin and its corresponding GND pin (i.e., pins 1 and 4 in a USB Standard-A or USB Standard-B connector or pins 1 and 5 in a USB Micro-B connector), the delta temperature shall not exceed +30° C at any point on the connectors under test, when measured at an ambient temperature of 25° C.

3.7.5 USB Type-C to USB Legacy Adapter Assemblies (Normative)

Only the following standard legacy adapter assemblies are defined:

- *USB 2.0* Type-C plug to *USB 2.0* Micro-B receptacle
- USB Full-Featured Type-C plug to *USB 3.1* Standard-A receptacle

3.7.5.1 USB 2.0 Type-C Plug to *USB 2.0* Micro-B Receptacle Adapter Assembly (Normative)

This adapter assembly supports only the *USB 2.0* signaling. It shall not exceed 150 mm total length, measured from end to end. Table 3-30 defines the electrical requirements.

Table 3-30 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (Normative)

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the adapter assembly have the proper impedance. For the entire adaptor assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of adapter assembly arrive at the receiver at the same time.	20 ps max. 400 ps rise time (20%-80%).
Differential Insertion Loss	EIA 364 – 101 This test ensures the D+/D− pair of an adapter assembly can provide adequate signal strength to the receiver.	−0.7 dB max @ 400 MHz

3.7.5.2 USB Full-Featured Type-C Plug to *USB 3.1* Standard-A Receptacle Adapter Assembly (Normative)

The USB Full-Featured Type-C plug to *USB 3.1* Standard–A receptacle adapter assembly is intended to be used with a direct-attach device (e.g., USB thumb drive). A system is not guaranteed to function when using an adapter assembly together with a Standard USB cable assembly.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

To minimize the impact of the adapter assembly to system signal integrity, the adapter assembly should meet the informative design targets in Table 3-31.

Table 3-31 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (Informative)

Items	Design Targets
Differential Return Loss	≤ −15 dB to 5 GHz Normalized with 85 ohms.
Differential Insertion Loss	≥ −2.4 dB to 2.5 GHz, ≥ −3.5 dB to 5 GHz
Differential NEXT between SuperSpeed Pairs	≤ −40 dB to 2.5 GHz ≤ −34 dB at 5 GHz
Differential NEXT and FEXT between D+/D− and SuperSpeed Pairs	≤ −30 dB to 2.5 GHz

The normative requirements for the adapter assembly are defined in Table 3-30 and Table 3-32. The adapter assembly total length is limited to 150 mm max.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 3-32 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequency (ILfitatNq)	ILfitatNq is evaluated at the SuperSpeed Gen 1 Nyquist frequency.	≥ −2.4 dB at 2.5 GHz ≥ −3.5 dB at 5 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −38 dB, Tb = 200 ps ≤ −27 dB, Tb = 100 ps
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXTs* = NEXT between SuperSpeed pairs *NEXTd* = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-37 with Tb (UI) = 2.08 ns.	≤ −37 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXT(f)\rvert^2 + \lvert Vin(f)\rvert^2\lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = Near-end crosstalk from SuperSpeed to D+/D− *FEXT* = Far-end crosstalk from SuperSpeed to D+/D− f_{max} = 1.2 GHz	≤ −30 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −14.5 dB, Tb = 200 ps ≤ −12.0 dB, Tb = 100 ps
Diff to Comm mode	Differential to Common Mode conversion (SCD12, SCD21)	≤ −15 dB

Note: *fmax* = 7.5 GHz; *Vin(f)* is defined in Figure 3-37 with Tb (UI) = 200 ps; and *Vdd(f)* is also specified in Figure 3-37 with Tb (UI) = 2.08 ns.

3.7.5.3 Compliant USB Legacy Receptacles used in USB Type-C to Legacy Adapter Assemblies

3.7.5.3.1 Contact Material Requirements

Refer to Section 3.7.4.3.1 for contact material requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

3.7.5.3.2 Contact Current Ratings

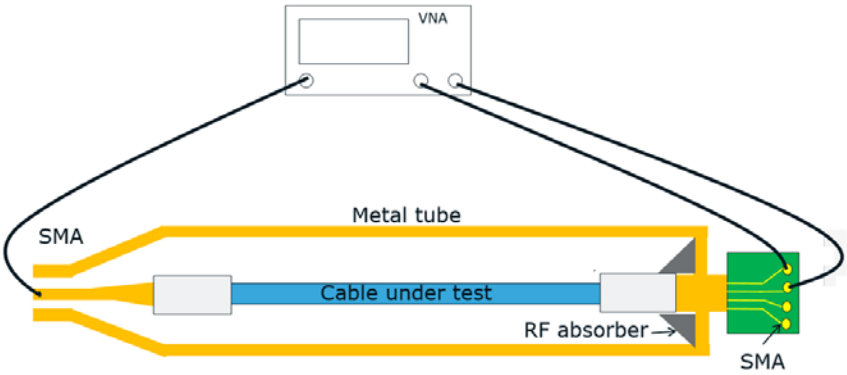
Refer to Section 3.7.4.3.2 for contact current rating requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

3.7.6 Shielding Effectiveness Requirements (Normative)

The cable assembly shielding effectiveness (SE) test measures the EMI and RFI levels from the cable assembly. To perform the measurement, the cable assembly shall be installed in the cable SE test fixture as shown in Figure 3-55. The coupling factors from the cable to the fixture are characterized with a VNA.

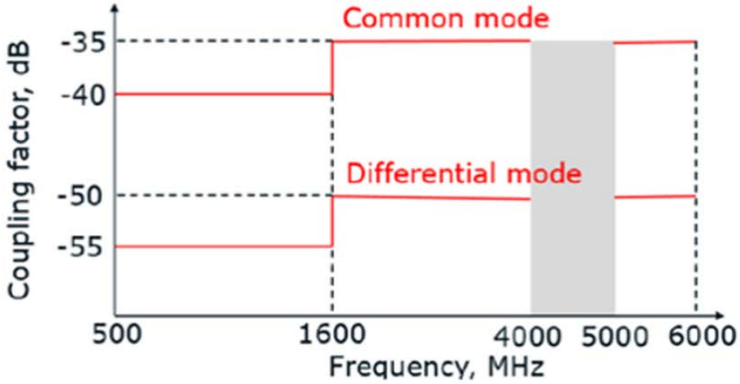
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-55 Cable Assembly Shielding Effectiveness Testing

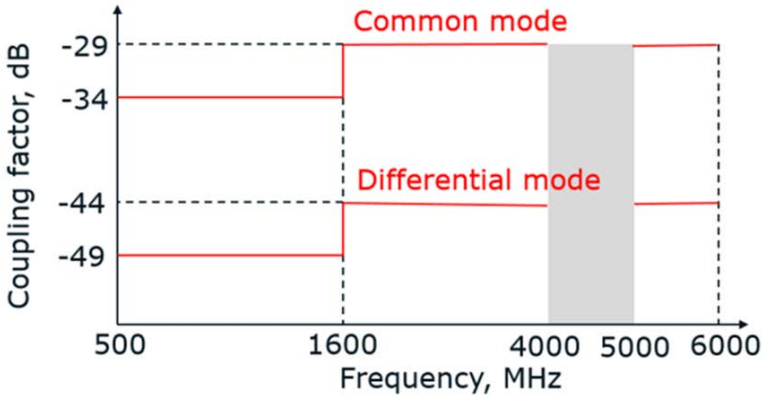


All USB Type-C cable assemblies shall pass the shielding effectiveness test for compliance. The pass/fail criteria for the USB Type-C to USB Type-C cable assemblies is shown in Figure 3-56a while the pass/fail criteria for the USB Type-C to legacy USB cable assemblies is shown in Figure 3-56b. Note that the shielding effectiveness for the frequency band from 4 GHz to 5 GHz is not specified since there is no antenna operating in this frequency range.

Figure 3-56 Shielding Effectiveness Pass/Fail Criteria



(a) For USB Type-C to USB Type-C Cable Assemblies



(b) For USB Type-C to legacy USB cable assemblies

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.7.7 DC Electrical Requirements (Normative)

Unless otherwise stated, the tests in this section are performed on mated connector pairs.

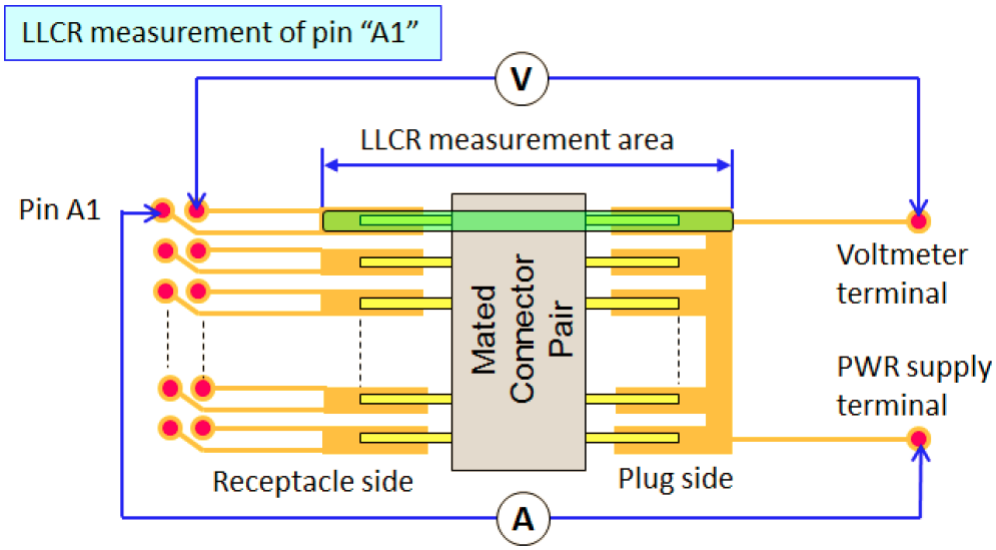
3.7.7.1 Low Level Contact Resistance (EIA 364-23B)

The low level contact resistance (LLCR) measurement is made across the plug and receptacle mated contacts and does not include any internal paddle cards or substrates of the plug or receptacle. See Figure 3-57. The following apply to the power and signal contacts:

- 40 mΩ (Max) initial for VBUS, GND and all other contacts.
- 50 mΩ (Max) after environmental stresses.
- Measure at 20 mV (Max) open circuit at 100 mA.

Refer to Section 3.8 for environmental requirements and test sequences.

Figure 3-57 LLCR Measurement Diagram



3.7.7.2 Dielectric Strength (EIA 364-20)

No breakdown shall occur when 100 Volts AC (RMS) is applied between adjacent contacts of unmated and mated connectors.

3.7.7.3 Insulation Resistance (EIA 364-21)

A minimum of 100 MΩ insulation resistance is required between adjacent contacts of unmated and mated connectors.

3.7.7.4 Contact Current Rating

The current rating testing for the USB Type-C connector (plug and receptacle) shall be conducted per the following set up and procedures:

- A current of 5 A shall be applied collectively to VBUS pins (i.e., pins A4, A9, B4, and B9) and 1.25 A shall be applied to the VCONN pin (i.e., B5) as applicable, terminated through the corresponding GND pins (i.e., pins A1, A12, B1, and B12). A minimum current of 0.25 A shall also be applied individually to all the other contacts, as

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

applicable. When current is applied to the contacts, the temperature of the connector pair shall be allowed to stabilize. The temperature rise of the outside shell surface of the mated pair above the VBUS and GND contacts shall not exceed 30 °C above the ambient temperature. Figure 3-58 provides an illustration of the measurement location.

- The measurement shall be done in still air.
- The connectors shall be oriented such that the accessible outer shell surface is on top and horizontal to the ground.
- The plug and receptacle may require modification to access solder tails or cable attachment points.
- Either thermocouple or thermo-imaging (preferred) method may be used for temperature measurement
- For certification, the connector manufacturer shall provide the receptacle and plug samples under test mounted on a current rating test PCB with no copper planes. A cable plug may use short wires to attach the cable attachment points together rather than using a current rating test PCB.
    - The current rating test PCBs shall be of a 2-layer construction. If 2-layer construction is not possible due to the solder tail configuration, VBUS and ground traces shall be located on the outer layers with the inner layers reserved for signal traces, as required; VCONN traces may be routed either on internal or external layers. Table 3-33 defines the requirements for the test PCB thickness and traces. The trace length applies to each PCB (receptacle PCB and plug PCB) and is from the contact terminal to the current source tie point. Figure 3-59 provides an informative partial trace illustration of the current rating test PCB.
    - If short wires are used instead of a current rating test PCB, the wire length shall not exceed 70 mm, measured from the plug contact solder point to the other end of the wire. There shall be no paddle card or overmold included in the test set-up. Each plug solder tail shall be attached with a wire with the wire gauge of AWG 36 for signals, AWG 32 for power (VBUS and VCONN), and AWG 30 for ground.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-58 Temperature Measurement Point

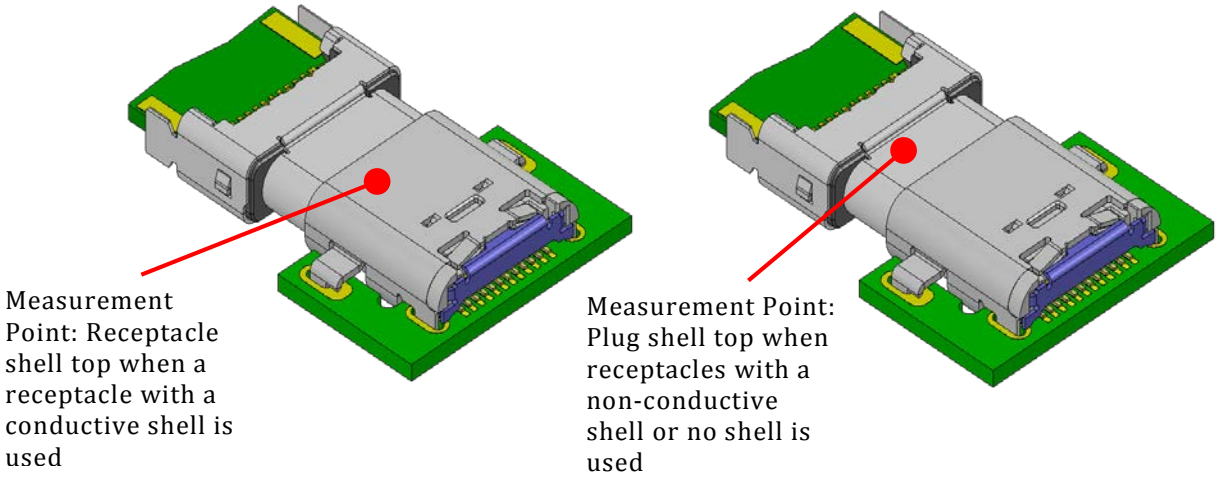
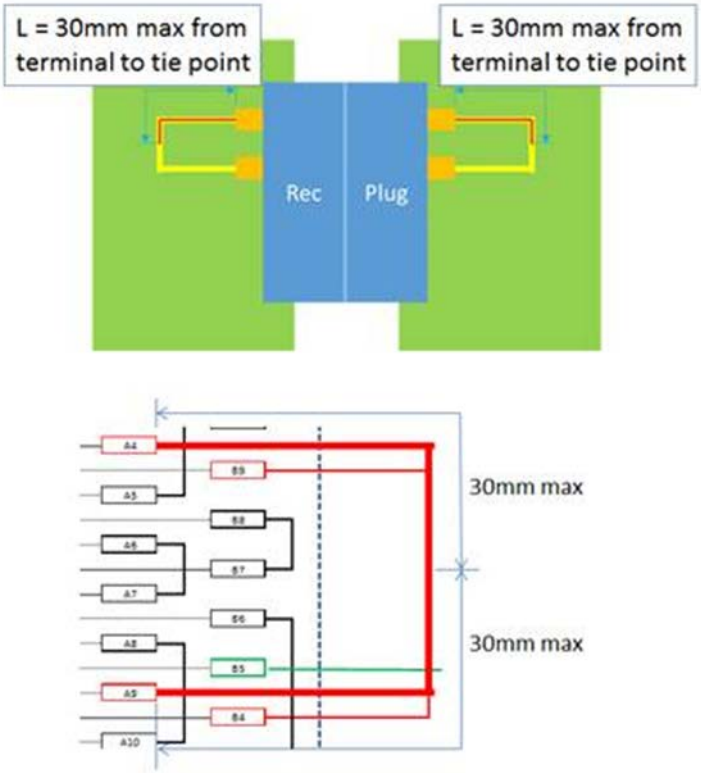


Table 3-33 Current Rating Test PCB

Item	Trace width (mm)	Trace length (mm) on each PCB	Thickness
Signal trace	0.25 max.	13 max.	35 µm (1 oz. copper)
Ground trace	1.57 max.	38 max.	35 µm (1 oz. copper)
VBUS and VCONN	1.25 max.	30 max.	35 µm (1 oz. copper)
PCB	N/A	N/A	0.80 – 1.20 mm

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-59 Example Current Rating Test Fixture Trace Configuration



3.8 Mechanical and Environmental Requirements (Normative)

The requirements in this section apply to all USB Type-C connectors and/or cable assemblies unless otherwise specified. For USB Type-C plug connectors and cable assemblies, the test methods are based on an assumption that the cable exits the overmold in line with mating direction to a USB Type-C receptacle (i.e., straight out the back of the overmold). For USB Type-C plug connectors and cable assemblies with the cable exiting the overmold in a different direction than straight out the back (e.g., right angle to the mating direction), test fixtures and procedures shall be modified as required to accomplish the measurement.

3.8.1 Mechanical Requirements

3.8.1.1 Insertion Force (EIA 364-13)

The initial connector insertion force shall be within the range from 5 N to 20 N at a maximum rate of 12.5 mm (0.492") per minute. This requirement does not apply when the connectors are used in a docking application.

It is recommended to use a non-silicone based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.2 Extraction Force (EIA 364-13)

The initial connector extraction force shall be within the range of 8 N to 20 N, measured after a preconditioning of five insertion/extraction cycles (i.e., the sixth extraction). After an additional twenty-five insertion/extraction cycles, the extraction force shall be measured again (i.e., the thirty-second extraction) and the extraction force shall be:

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

a. within 33% of the initial reading, and
b. within the range of 8 N to 20 N.

The extraction force shall be within the range of 6 N to 20 N after 10,000 insertion/ extraction cycles. The extraction force measurement shall be performed at a maximum speed of 12.5 mm (0.492") per minute. The extraction force requirement does not apply when the connectors are used in a mechanical docking application.

It is recommended to use a non-silicone based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.3 Durability or Insertion/Extraction Cycles (EIA 364-09)

The durability rating shall be 10,000 cycles minimum for the USB Type-C connector family. The durability test shall be done at a rate of 500 ± 50 cycles per hour and no physical damage to any part of the connector and cable assembly shall occur.

3.8.1.4 Cable Flexing (EIA 364-41, Condition 1)

No physical damage or discontinuity over 1ms during flexing shall occur to the cable assembly with Dimension X = 3.7 times the cable diameter and 100 cycles in each of two planes.

3.8.1.5 Cable Pull-Out (EIA 364-38, Method A)

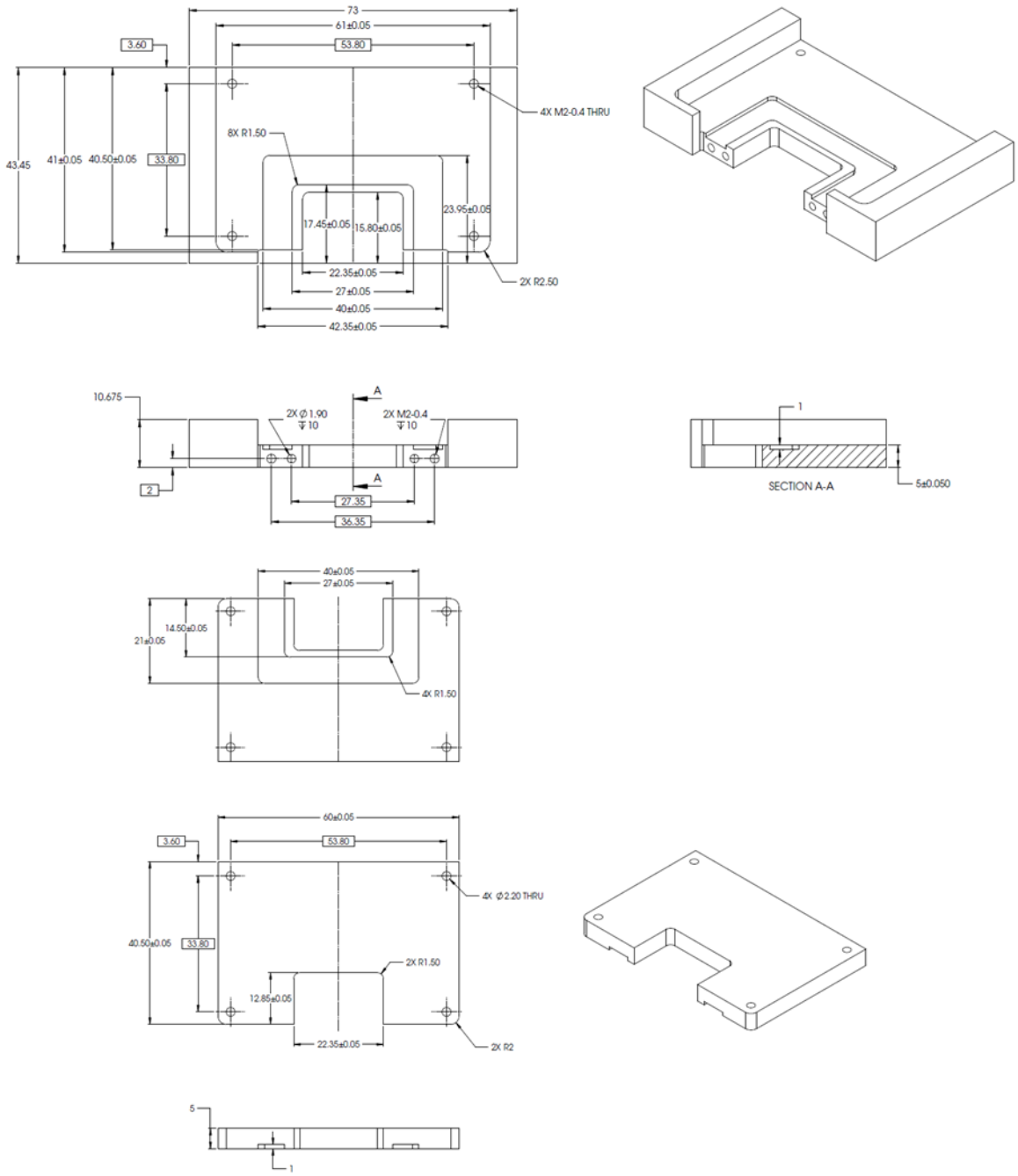
No physical damage to the cable assembly shall occur when it is subjected to a 40 N axial load for a minimum of 1 minute while clamping one end of the cable plug.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 103
Microchip v. Aptiv
IPR2024-00496

3.8.1.6 4-Axis Continuity Test

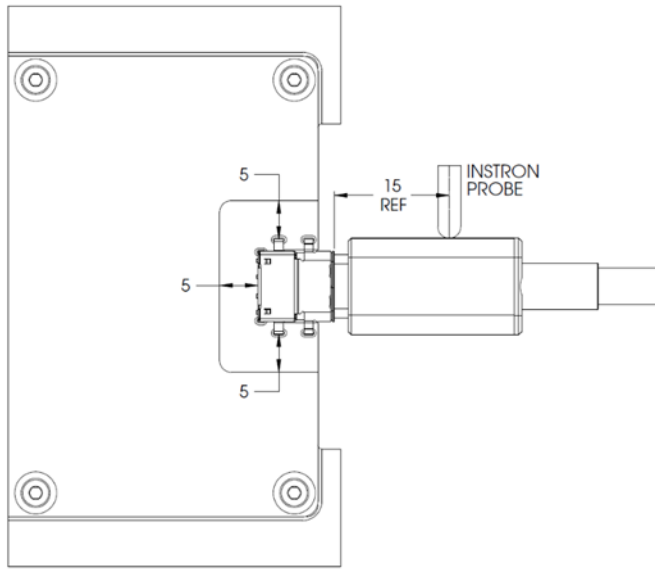
The USB Type-C connector family shall be tested for continuity under stress using a test fixture shown in Figure 3-60 or equivalent.

Figure 3-60 Example of 4-Axis Continuity Test Fixture



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-60 Example of 4-Axis Continuity Test Fixture, cont.



Plugs shall be supplied with a representative overmold or mounted on a 2 layer printed circuit board (PCB) between 0.8 mm and 1.0 mm thickness as applicable. A USB Type-C receptacle shall be mounted on a 2 layer PCB between 0.8 mm and 1.0 mm thickness. The PCB shall be clamped on three sides of the receptacle no further than 5 mm away from the receptacle outline. The receptacle PCB shall initially be placed in a horizontal plane, and a perpendicular moment shall be applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds at a distance of 15 mm from the mating edge of the receptacle shell in a downward direction, perpendicular to the axis of insertion. See Table 3-34 for the force and moment to be applied.

Table 3-34 Force and Moment Requirements

Receptacle configuration with respect to mounting surface	Force at 15 mm from receptacle shell mating edge (N)	Moment with respect to receptacle shell mating edge (Nm)
Right angle	20	0.30
Vertical	8	0.12

The continuity across each contact shall be measured throughout the application of the tensile force. Each non-ground contact shall also be tested to confirm that it does not short to the shell during the stresses. The PCB shall then be rotated 90 degrees such that the cable is still inserted horizontally and the tensile force in Table 3-34 shall be applied again in the downward direction and continuity measured as before. This test is repeated for 180 degree and 270 degree rotations. Passing parts shall not exhibit any discontinuities or shorting to the shell greater than 1 µs duration in any of the four orientations.

One method for measuring the continuity through the contacts is to short all the wires at the end of the cable pigtail and apply a voltage through a pull-up to each of V_{BUS}, USB D+, USB D−, SBU, CC, and USB SuperSpeed pins, with the GND pins connected to ground.

Alternate methods are allowed to verify continuity through all pins.

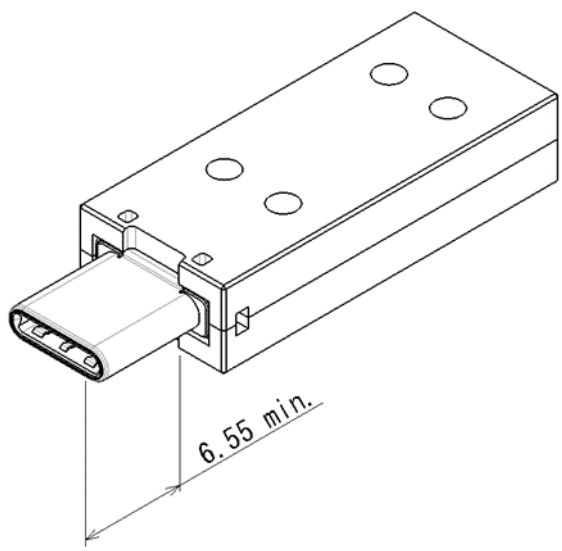
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.8.1.7 Wrenching Strength

USB Type-C plugs on cable assemblies and fixture plugs without overmold (including PCB-mount USB Type-C plugs) shall be tested using the mechanical wrenching test fixture defined in the Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. For plug without overmold, the supplier shall provide a plug test fixture that conforms to the specified plug overmold dimensions for the USB Type-C plug (see Figure 3-61). The fixture may be metal or other suitable material. Perpendicular moments are applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds when inserted in the test fixture to achieve the defined moments in four directions of up or down (i.e., perpendicular to the long axis of the plug opening) and left or right (i.e., in the plane of the plug opening). Compliant connectors shall meet the following force thresholds:

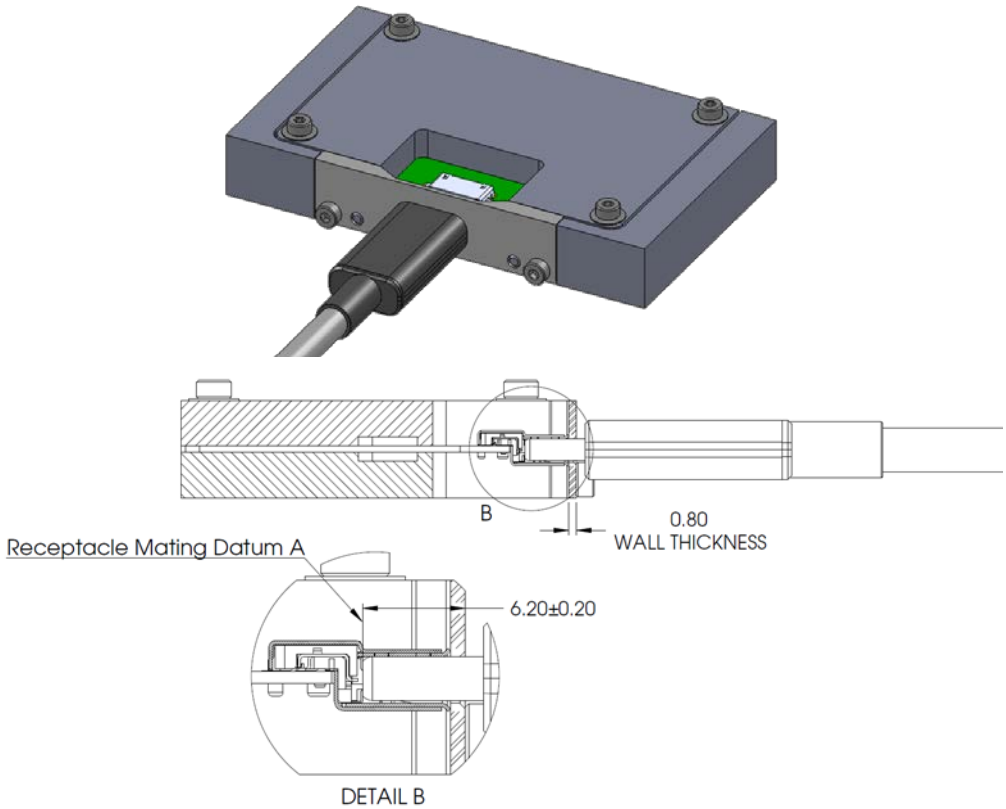
- A moment of 0-0.75 Nm (e.g., 50 N at 15 mm from the edge of the receptacle) is applied to a plug inserted in the test fixture in each of the four directions. A single plug shall be used for this test. Some mechanical deformation may occur. The plug shall be mated with the continuity test fixture after the test forces have been applied to verify no damage has occurred that causes discontinuity or shorting. The continuity test fixture shall provide a planar surface on the mating side located 6.20 ± 0.20 mm from the receptacle Datum A, perpendicular to the direction of insertion. No moment forces are applied to the plug during this continuity test. Figure 3-62 illustrates an example continuity test fixture to perform the continuity test. The Dielectric Withstanding Voltage test shall be conducted after the continuity test to verify plug compliance.

Figure 3-61 Example Wrenching Strength Test Fixture for Plugs without Overmold



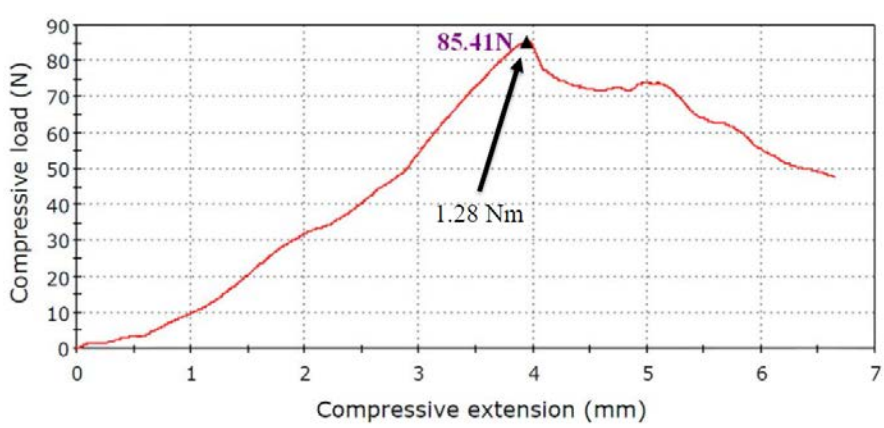
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-62 Reference Wrenching Strength Continuity Test Fixture



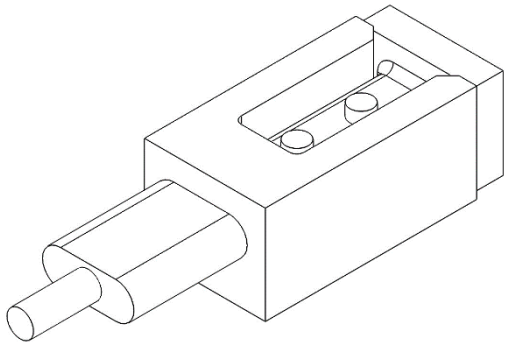
- The plug shall disengage from the test fixture or demonstrate mechanical failure (i.e., the force applied during the test procedure peaks and drops off) when a moment of 2.0 Nm is applied to the plug in the up and down directions and a moment 3.5 Nm is applied to the plug in the left and right directions. A new plug is required for each of the four test directions. An example of the mechanical failure point and an illustration of the wrenching test fixture are shown in Figure 3-63 and Figure 3-64, respectively.

Figure 3-63 Example of Wrenching Strength Test Mechanical Failure Point



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-64 Wrenching Strength Test with Cable in Fixture



3.8.1.8 Restriction of Hazardous Substances

It is recommended that components be RoHS compliant.

3.8.2 Environmental Requirements

The connector interface environmental tests shall follow EIA 364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications.

Since the connector defined has more than 0.127 mm wipe length, Test Group 6 in EIA 364-1000.01 is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature per the following.

Table 3-35 Environmental Test Conditions

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

The pass/fail criterion for the low level contact resistance (LLCR) is as defined in Section 3.7.7.1. The durability ratings are defined in Section 3.8.1.3.

3.8.2.1 Reference Materials (Informative)

This specification does not specify materials for connectors and cables. Connector and cable manufacturers should select appropriate materials based on performance requirements. The information below is provided for reference only.

Note: Connector and cable manufacturers should comply with contact plating requirements per the following options:

Option I

Receptacle

Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Plug

Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Option II

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Receptacle

Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Plug

Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Other reference materials that connector and cable manufacturers select based on performance parameters listed in Table 3-36 are for reference only.

Table 3-36 Reference Materials

Component	Materials
Cable	Conductor: copper with tin or silver plating
	SDP Shield: AL foil or AL/mylar foil
	Coaxial shield: copper strand
	Braid: Tin plated copper or aluminum
	Jacket: PVC or halogen free substitute material
Cable Overmold	Thermoset or thermoplastic
Connector Shells	Stainless steel or phosphor bronze
Plug Side Latches	Stainless steel
Receptacle Mid-Plate	Stainless steel
Plug Internal EMC Spring	Stainless steel or high yield strength copper alloy
Receptacle EMC Pad	Stainless steel or phosphor bronze
Receptacle Shell	Stainless steel or phosphor bronze
Receptacle Tongue	Glass-filled nylon
Housing	Thermoplastics capable of withstanding lead-free soldering temperature

Note: Halogen-free materials should be considered for all plastics

3.9 Docking Applications (Informative)

In this specification, docking refers to plugging a device directly into a dock without using a cable assembly. The USB Type-C connector is defined to support such applications.

The connector is only part of a docking solution. A complete docking solution at the system level may also include retention or locking mechanisms, alignment mechanisms, docking plug mounting solutions, and protocols supported through the connector. This specification does not attempt to standardize system docking solutions, therefore there is no interoperability requirement for docking solutions.

The following list includes the requirements and guidelines when using the USB Type-C connector for docking:

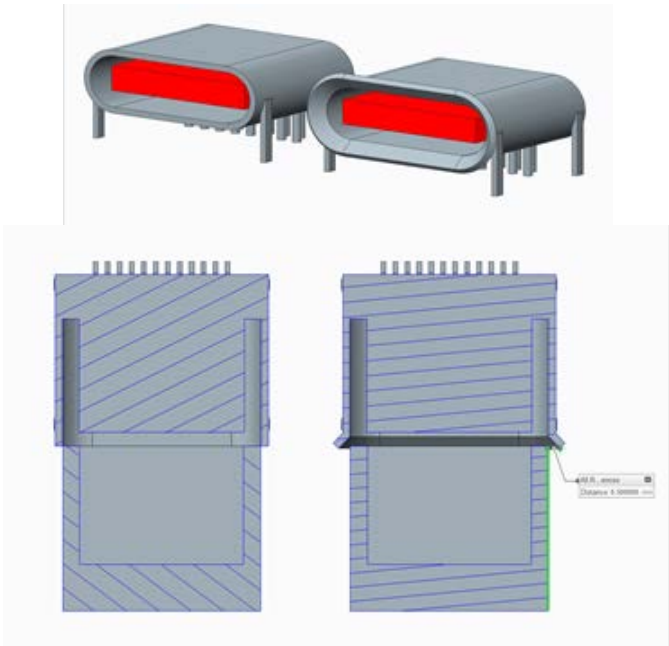
1. The USB Type-C plug used for docking shall work with compliant USB Type-C receptacle. It shall comply with all dimensional, electrical and mechanical requirements.
2. If the plug on the dock does not include the side latches, then the dock should provide a retention or locking mechanism to secure the device to the plug. The retention latches also serve as one of the ground return paths for EMC. The docking

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

design should ensure adequate EMC performance without the side latches if they are not present.

3. The internal EMC fingers are not required for the docking plug as long as the receptacle and plug shells have adequate electrical connection.
4. Alignment is critical for docking. Depending on system design, standard USB Type-C connectors alone may not provide adequate alignment for mating. System level alignment is highly recommended. Alignment solutions are implementation-specific.
5. Fine alignment is provided by the connector. The receptacle front face may have lead-in features for fine alignment. Figure 3-65 shows an example of a USB Type-C receptacle with a lead-in flange compared to a receptacle without the flange.

Figure 3-65 USB Type-C Cable Receptacle Flange Example



3.10 Implementation Notes and Design Guides

This section discusses a few implementation notes and design guides to help users design and use the USB Type-C connectors and cables.

3.10.1 EMC Management (Informative)

Connector and cable assembly designers, as well as system implementers should pay attention to receptacle and cable assembly shielding to ensure a low-impedance grounding path. The following are guidelines for EMC management:

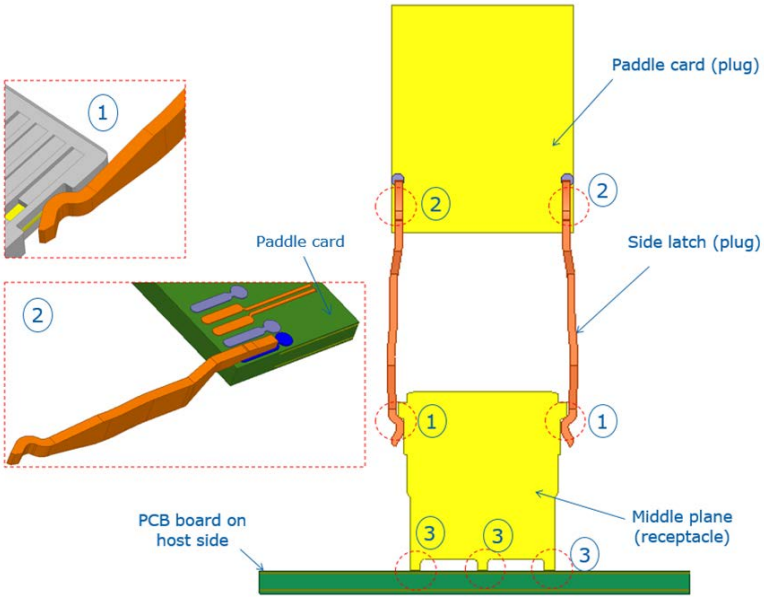
- The quality of raw cables should be ensured. The intra-pair skew or the differential to common mode conversion of the SuperSpeed pairs has a significant impact on cable EMC and should be controlled within the limits of this specification.
- The cable external braid should be physically connected to the plug metal shell as close to 360° as possible to control EMC. Without appropriate shielding termination, even a perfect cable with zero intra-pair skew may not meet EMC requirements. Copper tape may be needed to shield off the braid termination area.
- The wire termination contributes to common-mode noise. The breakout distance for the wire termination should be kept as small as possible to optimize EMC and signal

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

integrity performance. If possible, symmetry should be maintained for the two lines within a differential pair.

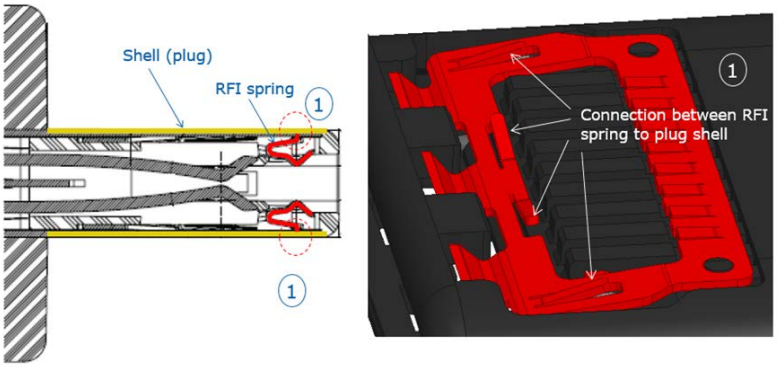
- Besides the mechanical function, the side latches on the plug and the mid-plate in the receptacle also play a role for EMC. This is illustrated in Figure 3-66:
    1. The side latch should have electrical connection to the receptacle mid-plate (a docking plug may not have side latches).
    2. The side latches should be terminated to the paddle card GND plane inside the plug.
    3. The mid-plate should be directly connected to system PCB GND plane with 3 or more solder leads/tails.

Figure 3-66 EMC Guidelines for Side Latch and Mid-plate



- The internal RFI finger inside the plug should have adequate connection points to the inner surface of the plug shell. Four or more connection points are recommended as illustrated in Figure 3-67.

Figure 3-67 EMC Finger Connections to Plug Shell

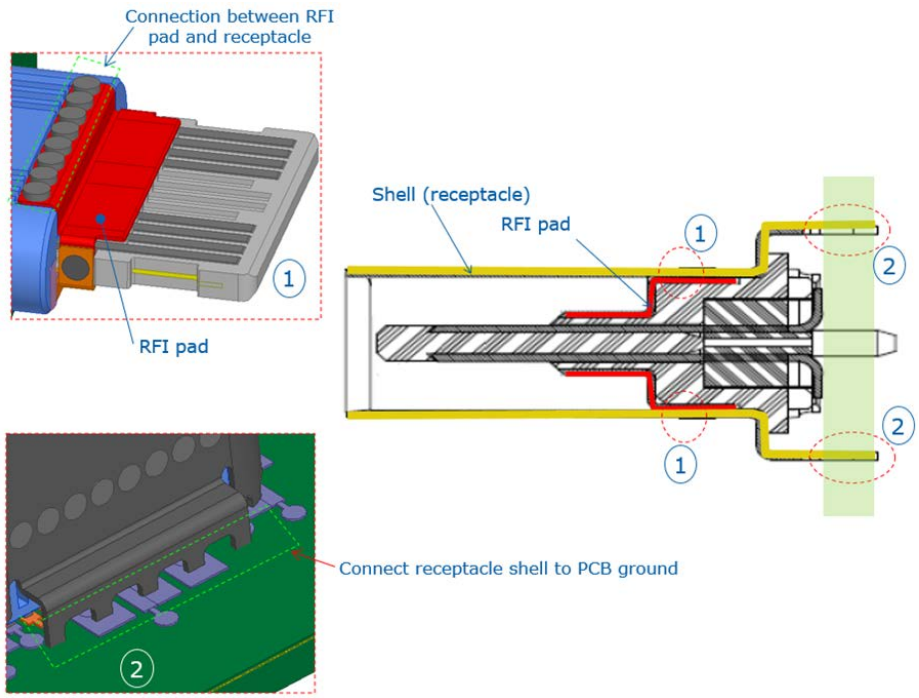


Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- The EMC fingers inside the plug mates with the EMC pad in the receptacle. It is important for the EMC pad to have adequate connections to the receptacle shell. As illustrated in Figure 3-68, there are multiple laser welding points between the EMC pads and the receptacle shell, top and bottom.

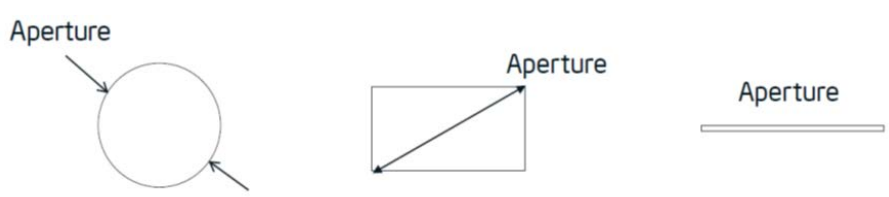
- The receptacle shell should have sufficient connection points to the system PCB GND plane with apertures as small as possible. Figure 3-68 illustrates an example with multiple solder tails to connect the receptacle shell to system PCB GND.

Figure 3-68 EMC Pad Connections to Receptacle Shell



- Apertures in the receptacle and plug shells should be minimized. If apertures are unavoidable, a maximum aperture size of 1.5 mm is recommended. See Figure 3-69 for aperture illustrations. Copper tape may be applied to seal the apertures inside the cable plug.

Figure 3-69 Examples of Connector Apertures



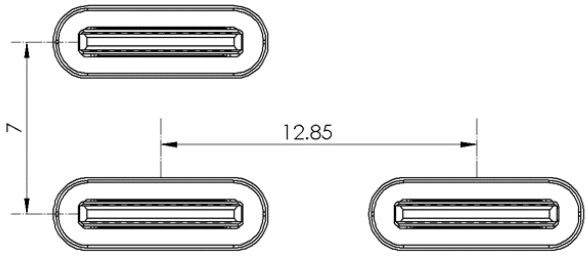
- The receptacle connectors should be connected to metal chassis or enclosures through grounding fingers, screws, or any other way to manage EMC.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3.10.2 Stacked and Side-by-Side Connector Physical Spacing (Informative)

Stacked and side-by-side USB connectors are commonly used in PC systems. Figure 3-70 illustrates the recommended spacing between connectors for stacked and side-by-side configurations.

Figure 3-70 Recommended Minimum Spacing between Connectors



3.10.3 Cable Mating Considerations (Informative)

The receptacle mounting location, exterior product surfaces, cable overmold, and plug mating length need to be considered to ensure the USB Type-C plug is allowed to fully engage the USB Type-C receptacle. Figure 3-71 illustrates the recommended minimum plug overmold clearance to allow the cable plug to fully seat in the product receptacle.

Figure 3-71 Recommended Minimum Plug Overmold Clearance

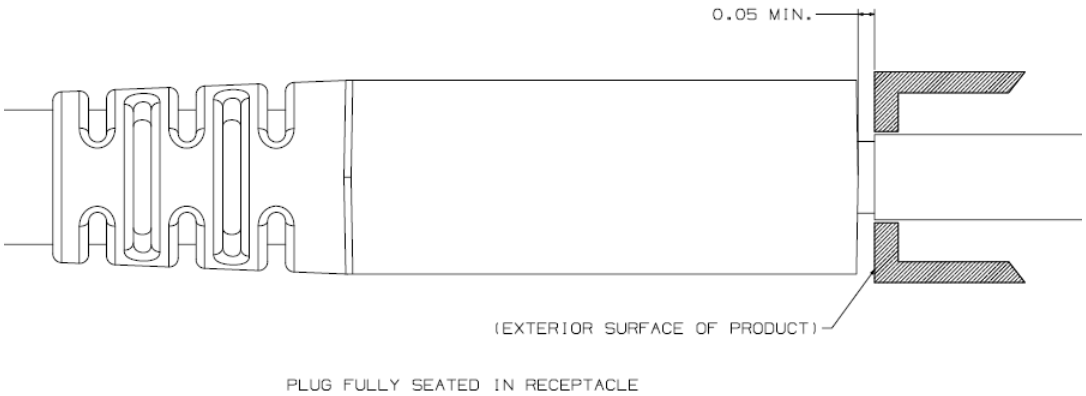
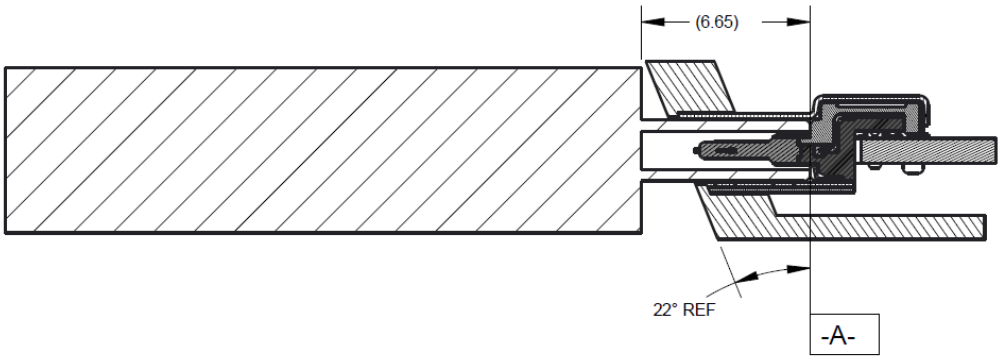


Figure 3-72 illustrates special considerations required when external walls are angled. For such applications, the USB Type-C receptacle shell may not provide as much mechanical alignment protection to the receptacle tongue as in the full shell design. Design options to allow the receptacle to pass mechanical test requirements include relief in the exterior wall surface to allow use of a full shell receptacle or use of a receptacle specifically designed for the application.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 3-72 Cable Plug Overmold and an Angled Surface



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4 Functional

This chapter covers the functional requirements for the signaling across the USB Type-C™ cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.

Chapter 5 defines functional extensions that are optional.

4.1 Signal Summary

Table 4-1 summarizes the list of signals used on the USB Type-C connectors.

Table 4-1 USB Type-C List of Signals

Signal Group	Signal	Description
USB 3.1	**SSTXp1, SSTXn1** **SSRXp1, SSRXn1** **SSTXp2, SSTXn2** **SSRXp2, SSRXn2**	SuperSpeed USB serial data interface defines 1 differential transmit pair and 1 differential receive pair. On a USB Type-C receptacle, two sets of SuperSpeed USB signal pins are defined to enable plug flipping feature
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	*USB 2.0* serial data interface defines a differential pair. On a USB Type-C receptacle, two set of *USB 2.0* signal pins are defined to enable plug flipping feature
Configuration	**CC1, CC2** (receptacle) **CC** (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN
Auxiliary signals	**SBU1, SBU2**	Sideband Use
Power	**VBUS**	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2 Signal Pin Descriptions

4.2.1 SuperSpeed USB Pins

SSTXp1, SSTXn1 (SSTXp2, SSTXn2)

These pins are required to implement the system's transmit path of a *USB 3.1* SuperSpeed interface. The transmitter differential pair in a port are routed to the receiver differential pair in the port at the opposite end of the path. The *USB 3.1 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

SSRXp1, SSRXn1 (SSRXp2, SSRXn2)

These pins are required to implement the system's receive path of a *USB 3.1* SuperSpeed interface. The receiver differential pair in a port are routed to the transmitter differential pair in the port at the opposite end of the path. The *USB 3.1 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.2.2 USB 2.0 Pins

Dp1, Dn1 (Dp2, Dn2) These pins are required to implement *USB 2.0* functionality. *USB 2.0* in all three modes (LS, FS, and HS) is supported. The *USB 2.0 Specification* defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.3 Auxiliary Signal Pins

SBU1, SBU2 These pins are assigned to sideband use. Refer to Section 4.3 for the functional requirements.

4.2.4 Power and Ground Pins

VBUS These pins are for USB cable bus power as defined by the USB specifications. VBUS is only present when a Source-to-Sink connection across the CC channel is present – see Section 4.5.1.2.1. Refer to Section 4.4.2 for the functional requirements for VBUS.

VCONN VCONN is applied to the unused CC pin to supply power to the local plug. Refer to Section 4.4.3 for the functional requirements for VCONN.

GND Return current path.

4.2.5 Configuration Pins

CC1, CC2, CC These pins are used to detect connections and configure the interface across the USB Type-C cables and connectors. Refer to Section 4.5 for the functional definition. Once a connection is established, CC1 or CC2 will be reassigned for providing power over the VCONN pin of the plug – see Section 4.5.1.2.1.

4.3 Sideband Use (SBU)

The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality will be defined in future versions of the USB specifications. See Section 5.1 and Appendix A for use of the SBU pins in Alternate Modes and Audio Adapter Accessory Mode.

The SBU pins on a port shall either be open circuit or have a weak pull-down to ground no stronger than zSBUTermination.

These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.

4.4 Power and Ground

4.4.1 IR Drop

The maximum allowable cable IR drop for ground (including ground on a captive cable) shall be 250 mV and for VBUS shall be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN is being sourced, the IR drop for the ground shall still be met considering any additional VCONN return current.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-1 illustrates what parameters contribute to the IR drop and where it shall be measured. The IR drop includes the contact resistance of the mated plug and receptacles at each end.

Figure 4-1 Cable IR Drop

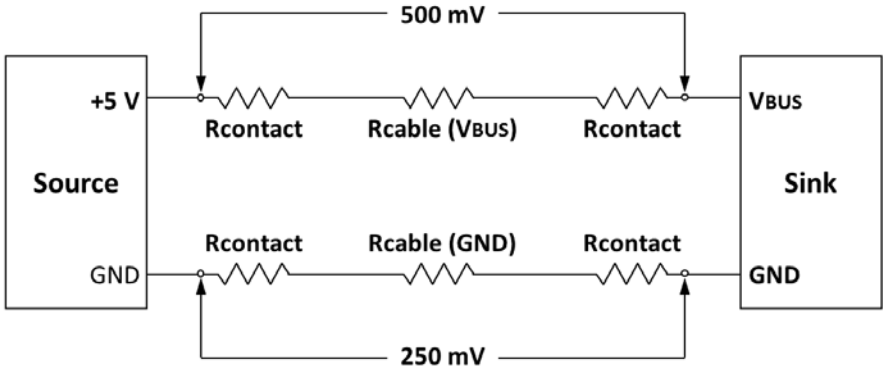
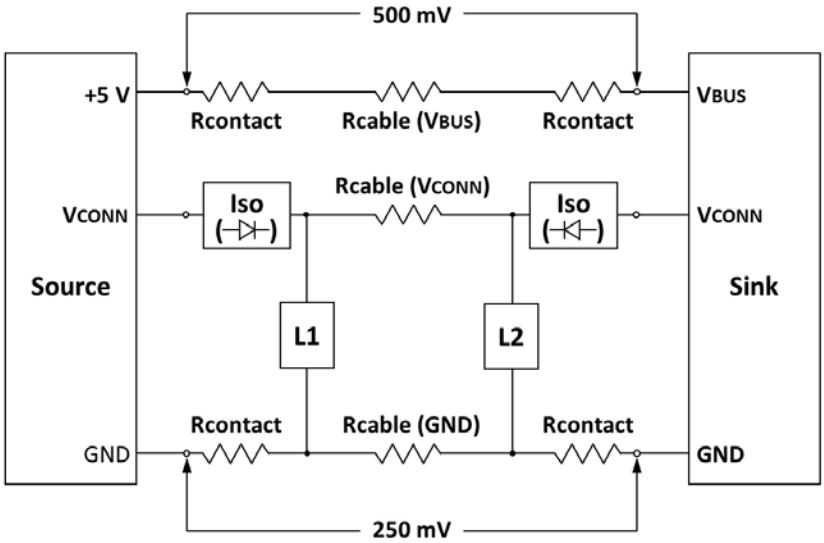


Figure 4-2 illustrates what parameters contribute to the IR drop for a powered cable and where it shall be measured. Note that the powered cable includes isolation elements (Iso) and loads (L1 and L2) for the functions in the powered cable such as *USB PD* controllers. The IR drop shall remain below 250 mV in all cases.

Figure 4-2 Cable IR Drop for powered cables



4.4.2 VBUS

The allowable default range for VBUS as measured at the Source receptacle shall be as defined by the *USB 2.0 Specification* and *USB 3.1 Specification*. Note that due to higher currents allowed, legacy devices may experience a higher voltage (up to 5.5V maximum) at light loads.

The Source's USB Type-C receptacle VBUS pin shall remain unpowered and shall limit the capacitance between VBUS and GND as specified in Table 4-2 until a Sink is attached. The VBUS pin shall return to the unpowered state when the Sink is detached. See Table 4-20 for VBUS timing values. Legacy hosts/chargers that by default source VBUS when connected

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.

A DRP or Source (or device with Accessory Support) implementing an Rp pull-up as its method of connection detection shall provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states Unattached.SRC or Unattached.Accessory).

Table 4-2 VBUS Source Characteristics

	Minimum	Maximum	Notes
VBUS Leakage Impedance	72.4 kΩ		Leakage between VBUS pins and GND pins on receptacle when VBUS is not being sourced.
VBUS Capacitance		10 µF	Capacitance between VBUS and GND pins on receptacle when VBUS is not being sourced.

4.4.3 VCONN

VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.

Initially, VCONN shall be sourced by all USB Type-C receptacles that source VBUS and utilize the SSTX and SSRX pins during specific connection states as described in Section 4.5.2.2. Subsequently, VCONN may be removed under some circumstances as described in Table 4-3. VCONN may also be sourced by USB Type-C receptacles that do not utilize the SSTX and SSRX pins as described in Section 4.5.2.2. *USB PD* VCONN_Swap command also provides the Source a means to request that the attached Sink supply VCONN.

Table 4-3 USB Type-C Source Port's VCONN Requirements Summary

D+/D−	SSTX/SSRX	> 3 A	VCONN Requirements
No	No	No	Not required to source VCONN
Yes	No	No	Not required to source VCONN
Yes	Yes	No	Required to source 1 W. VCONN power may be removed after the source has read the cable's eMarker and has determined that it is not an active cable.
No	No	Yes	Required to source 1 W. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	No	Yes	Required to source 1 W. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	Yes	Yes	Required to source 1 W. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity and that it is not an active cable.

Table 4-4 provides the voltage and power requirements that shall be met for VCONN. See Section 4.9 for more details about Electronically Marked Cables. See Section 4.10 for a wider

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

VCONN voltage operating range for VCONN-powered accessories. See Section 5.1 regarding optional support for an increased VCONN power range in Alternate Modes.

Table 4-4 VCONN Source Characteristics

	Minimum	Maximum	Notes
Voltage	4.75 V	5.5 V	Ports that support VCONN-powered accessories are allowed to supply at a lower minimum of 2.7 V when operating in the PoweredAccessory state.
Power	1.0 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and wattage.
Bulk Capacitance	10 µF	220 µF	The VCONN source shall disconnect the bulk capacitance from the receptacle when VCONN is powered off.

To aid in reducing the power associated with supplying VCONN, a Source is allowed to either not source VCONN or turn off Vconn under any of the following conditions:

- Ra is not detected on the CC pin after tCCDebounce when the other CC pin is in the SRC.Rd state
- Ra is not detected on the CC pin after tCCDebounce when the other CC pin is in the SRC.Open state and the port supports VCONN-powered accessories
- If there is no GoodCRC response to *USB PD* Discover Identity messages

Table 4-5 provides the requirements that shall be met for cables that consume VCONN power.

Table 4-5 VCONN Sink Characteristics

	Minimum	Maximum	Notes
Inrush Capacitance		10 µF	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Cables		70 mW	See Section 4.9.
Power for Active Cables		1.0 W	See Section 5.2.
tVCONNDischarge		250 ms	The time from the point that the cable is detached until vVCONNDischarge shall be met.
vVCONNDischarge		150 mV	The VCONN voltage following cable detach and self-discharge.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The cable may remove or weaken Ra when VCONN is above 1.0 V as long as the other requirements are met. See Section 4.5.1.2.1.

4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. Note that in this section, "direct connect" is used to refer to a device connected directly to a host (e.g., a thumb drive). When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*
- Configure VCONN
- Discover and configure optional Alternate and Accessory modes

4.5.1.1 USB Data Bus Interface and USB Type-C Plug Flip-ability

Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of USB 2.0, this is done by shorting together the two D+ signal pins and the two D− signal pins in the host and device receptacles. In the case of USB SuperSpeed signals, it requires the functional equivalent of a switch in both the host and device to appropriately route the SuperSpeed TX and RX signal pairs to the connected path through the cable.

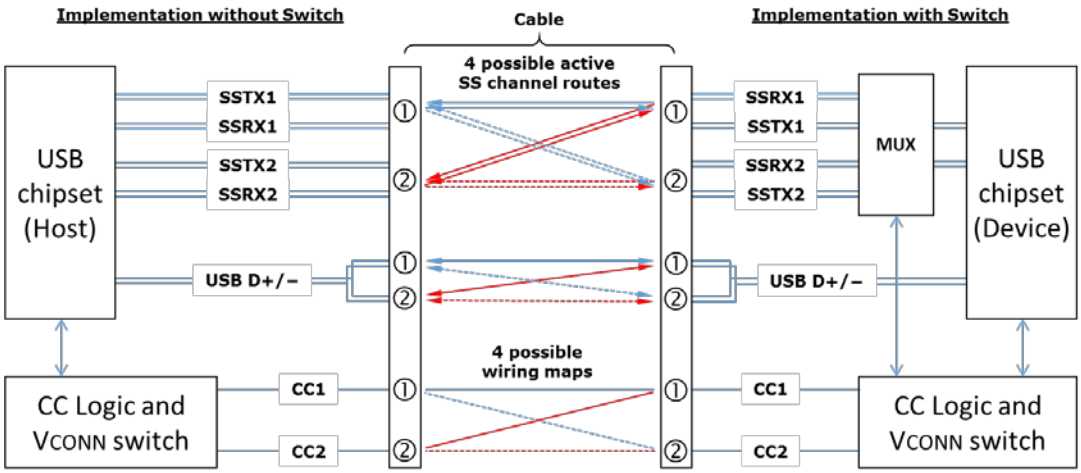
Figure 4-3 illustrates the logical data bus model for a USB Type-C-based Host connected to a USB Type-C-based Device. The USB cable that sits between a host and device can be in one of four possible connected states when viewed by the host:

- Un-flipped straight through – Position ① ⇔ Position ①
- Un-flipped twisted through – Position ① ⇔ Position ②
- Flipped straight through – Position ② ⇔ Position ②
- Flipped twisted through – Position ② ⇔ Position ①

To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first USB SuperSpeed signal pairs (SSTXp1/SSTXn1 and SSRXp1/SSRXn1) – in this way, the CC wire and USB SuperSpeed data bus wires that are used for signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which SuperSpeed USB signals are to be used for the connection and the host can use this to control the functional switch for routing the SuperSpeed USB signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its SuperSpeed USB signal pairs.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

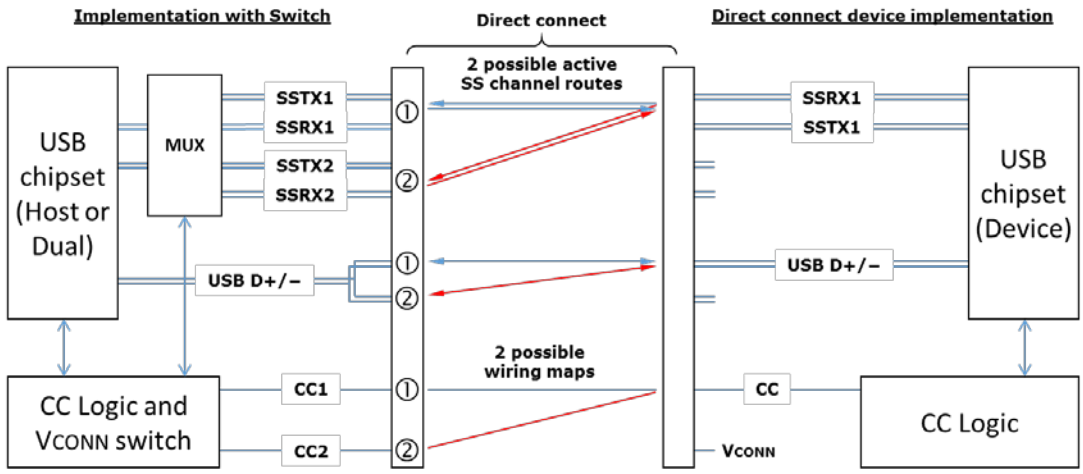
Figure 4-3 Logical Model for Data Bus Routing across USB Type-C-based Ports



While Figure 4-3 illustrates the functional model as a host connected to a device, this model equally applies to a USB hub's downstream ports as well.

Figure 4-4 illustrates the logical data bus model for a USB Type-C-based Device (implemented with a USB Type-C plug either physically incorporated into the device or permanently attached as a captive cable) connected directly to a USB Type-C-based Host. For the device, the location of the USB SuperSpeed data bus, *USB 2.0* data bus, CC and VCONN pins are fixed by design. Given that the device pin locations are fixed, only two possible connected states exist when viewed by the host.

Figure 4-4 Logical Model for USB Type-C-based Ports for the Direct Connect Device



The functional requirements for implementing SuperSpeed USB data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other USB 3.1 design elements, e.g. a bus repeater.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.1.2 Connecting Sources and Sinks

Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-6 summarizes the expected results when interconnecting Source, Sink and DRP ports.

Table 4-6 USB Type-C-based Port Interoperability

	Source-only	Sink-only	DRP (Dual-Role-Power)
Source-only	Non-functional	Functional	Functional
Sink-only	Functional	Non-functional	Functional
DRP (Dual-Role-Power)	Functional	Functional	Functional*

* Resolution of roles may be automatic or manually driven

In the cases where no function results, neither port shall be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where host-to-host and device-to-device connections are not intended to work, the non-keyed USB Type-C solution does not prevent the user from attempting such interconnects. VBUS and VCONN shall not be applied by a Source (host) in these cases.

The typical flow for the configuration of the interface in the general USB case of a Source (Host) to a Sink (Device) is as follows:

1. Detect a valid connection between the ports (including determining cable orientation, Source/Sink and DFP/UFP relationship)
2. Optionally discover the cable's capabilities
3. Optionally establish alternatives to traditional USB power (See Section 4.6.2)
    a. *USB PD* communication over CC for advanced power delivery negotiation
    b. USB Type-C Current modes
    c. USB BC 1.2
4. USB Device Enumeration

For cases of Dual-Role-Power (DRP) ports connecting to either Source-only, Sink-only or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a Source for detecting an attached Sink and presenting as a Sink to be detected by an attached Source. Ultimately this results in a Source-to-Sink connection.

4.5.1.2.1 Detecting a Valid Source-to-Sink Connection

The general concept for setting up a valid connection between a Source and Sink is based on being able to detect terminations residing in the product being attached.

To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd) termination model is used – actual implementation in hosts and devices may vary, for

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

example, the pull-up termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the Source and the second replacing this with a current source.

Figure 4-5 Pull-Up/Pull-Down CC Model

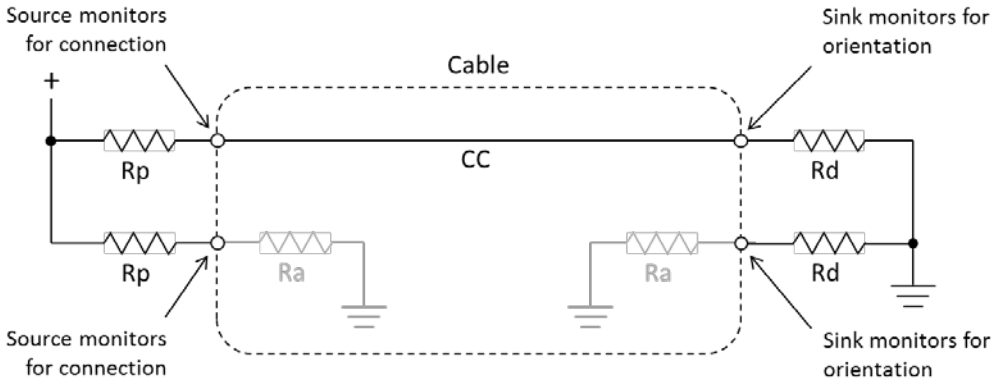
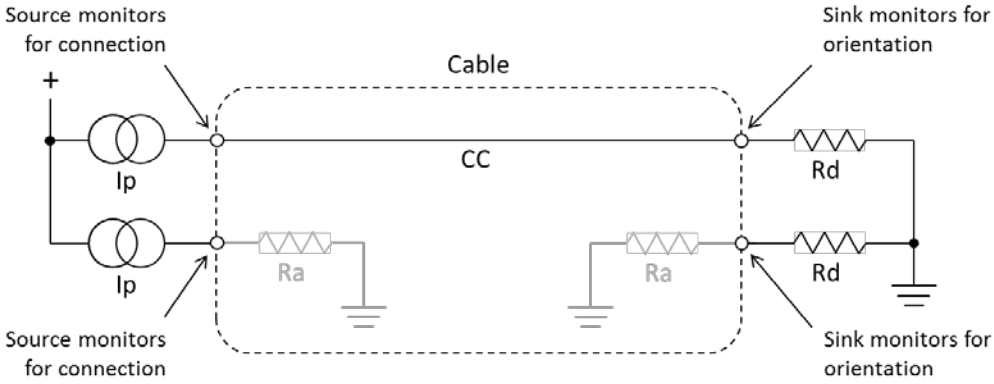


Figure 4-6 Current Source/Pull-Down CC Model



Initially, a Source exposes independent Rp terminations on its CC1 and CC2 pins, and a Sink exposes independent Rd terminations on its CC1 and CC2 pins, the Source-to-Sink combination of this circuit configuration represents a valid connection. To detect this, the Source monitors CC1 and CC2 for a voltage lower than its unterminated voltage – the choice of Rp is a function of the pull-up termination voltage and the Source's detection circuit. This indicates that either a Sink, a powered cable, or a Sink connected via a powered cable has been attached.

Prior to application of VCONN, a powered cable exposes Ra on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be a pure resistance and in others it may be simply the load.

The Source has to be able to differentiate between the presence of Rd and Ra to know whether there is a Sink attached and where to apply VCONN. The Source is not required to source VCONN unless Ra is detected.

Two special termination combinations on the CC pins as seen by a Source are defined for directly attached Accessory Modes: Ra/Ra for Audio Adapter Accessory Mode (Appendix A) and Rd/Rd for Debug Accessory Mode (Appendix B).

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The Source uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (tCCDebounce), and hide *USB PD* BMC communications (tPDDebounce).

Table 4-7 summarizes the port state from the Source's perspective.

Table 4-7 Source Perspective

CC1	CC2	State	Position
Open	**Open**	Nothing attached	N/A
Rd	**Open**	Sink attached	①
Open	**Rd**		②
Open	**Ra**	Powered cable without Sink attached	①
Ra	**Open**		②
Rd	**Ra**	Powered cable with Sink or VCONN-powered Accessory attached	①
Ra	**Rd**		②
Rd	**Rd**	Debug Accessory Mode attached (Appendix B)	N/A
Ra	**Ra**	Audio Adapter Accessory Mode attached (Appendix A)	N/A

Once the Sink is powered, the Sink monitors CC1 and CC2 for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e. pulled up by Rp in the Source) indicates the orientation of the plug.

Table 4-8 summarizes the typical behaviors for simple Sources (Hosts) and Sinks (Devices) for each state in Table 4-7.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 4-8 Source (Host) and Sink (Device) Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Sink attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• Sense CC pins for orientation • Sense loss of VBUS for detach
Powered cable without Sink attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Powered cable with Sink or VCONN-powered Accessory attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• If accessories are supported, see Source Behavior with exception that VBUS is not applied., otherwise, N/A.
Debug Accessory Mode attached	• Sense CC pins for detach • Reconfigure for debug	• Sense VBUS for detach • Reconfigure for debug
Audio Adapter Accessory Mode attached	• Sense CC pins for detach • Reconfigure for analog audio	• If accessories are supported, see Source Behavior, otherwise, N/A

Figure 4-3 shows how the inserted plug orientation is detected at the Source's receptacle by noting on which of the two CC pins in the receptacle an Rd termination is sensed. Now that the Source (Host) has recognized that a Sink (Device) is attached and the plug orientation is determined, it configures the SuperSpeed USB data bus routing to the receptacle.

The Source (Host) then turns on VBUS. For the CC pin that does not connect Source-to-Sink through the cable, the Source supplies VCONN and may remove the termination. With the Sink (Device) now powered, it configures the USB data path. This completes the Host-to-Device connection.

The Source monitors the CC wire for the loss of pull-down termination to detect detach. If the Sink is removed, the Source port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new Sink attach.

Once a valid Source-to-Sink connection is established, alternatives to traditional USB power (VBUS as defined by either *USB 2.0* or *USB 3.1* specifications) may be available depending on the capabilities of the host and device. These include USB Type-C Current, USB Power Delivery, and *USB Battery Charging 1.2*.

In the case where *USB PD* PR_Swap is used to swap the Source and Sink of VBUS, the supplier of VCONN remains unchanged during and after the VBUS power swap. The new Source monitors the CC wire and the new Sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.

In the case where *USB PD* DR_Swap is used to swap the data roles (DFP and UFP), the source of VBUS and VCONN do not change after the data role swap.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

In the case where *USB PD* VCONN_Swap is used to swap the VCONN source, the VBUS Source/Sink and DFP/UFP roles are maintained during and after the VCONN swap.

The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard *USB 2.0* and *USB 3.1* processes.

4.5.1.3 Configuration Channel Functional Models

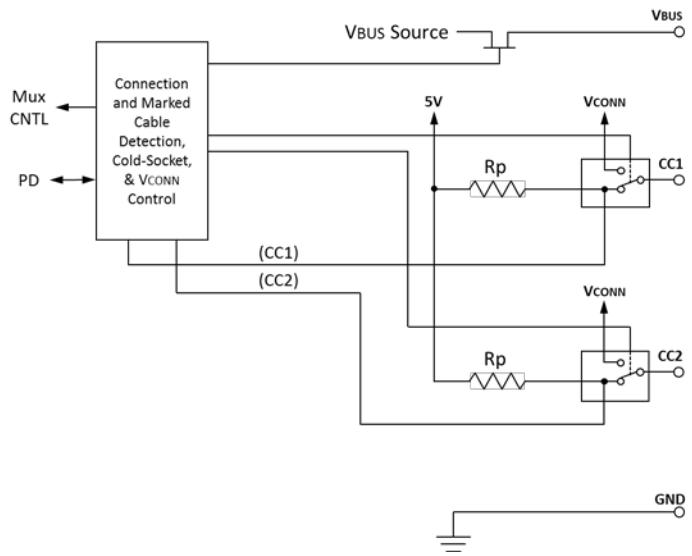
The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: Source, Sink and Dual-Role-Power (DRP).

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN may or may not actually be available.

4.5.1.3.1 Source Configuration Channel Functional Model

Figure 4-7 illustrates the functional model for CC1 and CC2 for a Source port prior to attach. This illustration includes consideration for *USB PD*.

Figure 4-7 Source Functional Model for CC1 and CC2



Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

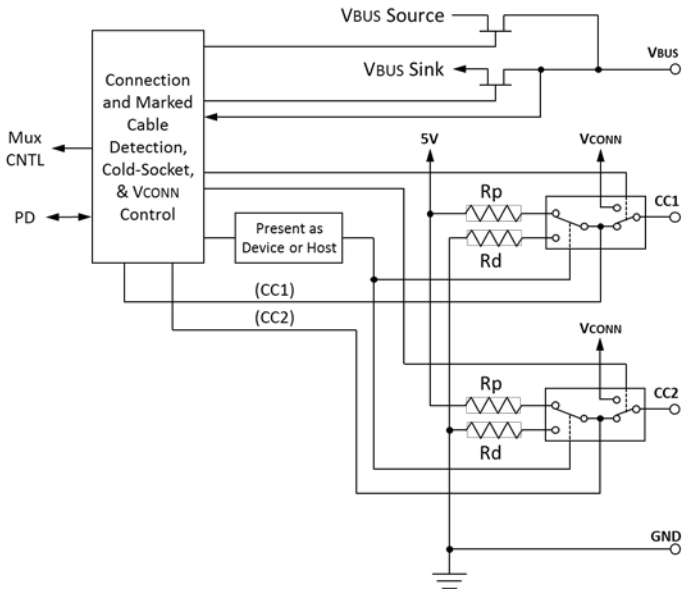
1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the USB SuperSpeed data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

5. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.
6. The Source monitors the continued presence of Rd to detect Sink detach. When a detach event is detected, the Source removes, if supplied, VBUS and VCONN, and returns to step 2.
7. If the Source supports advanced functions (USB Power Delivery and/or Alternate Modes), *USB PD* communication is required.

Figure 4-8 illustrates the functional model for CC1 and CC2 for a Source that supports *USB PD* PR_Swap.

Figure 4-8 Source Functional Model Supporting USB PD PR_Swap

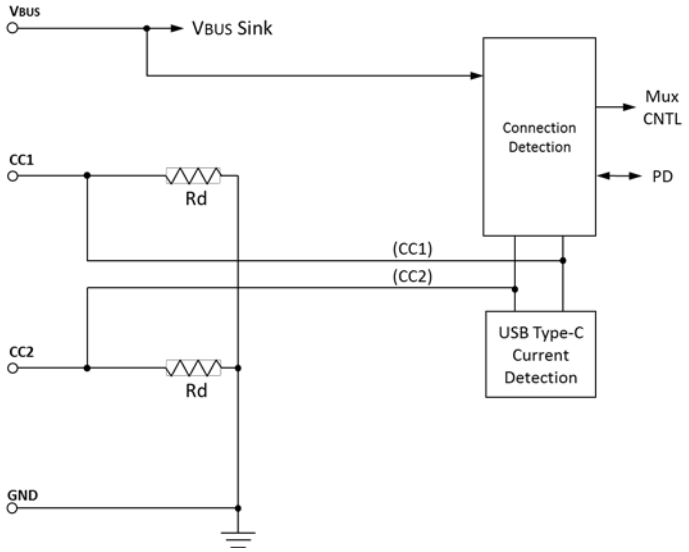


4.5.1.3.2 Sink Configuration Channel Functional Model

Figure 4-9 illustrates the functional model for CC1 and CC2 for a Sink. This illustration includes consideration for both USB Type-C Current and *USB PD*.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-9 Sink Functional Model for CC1 and CC2



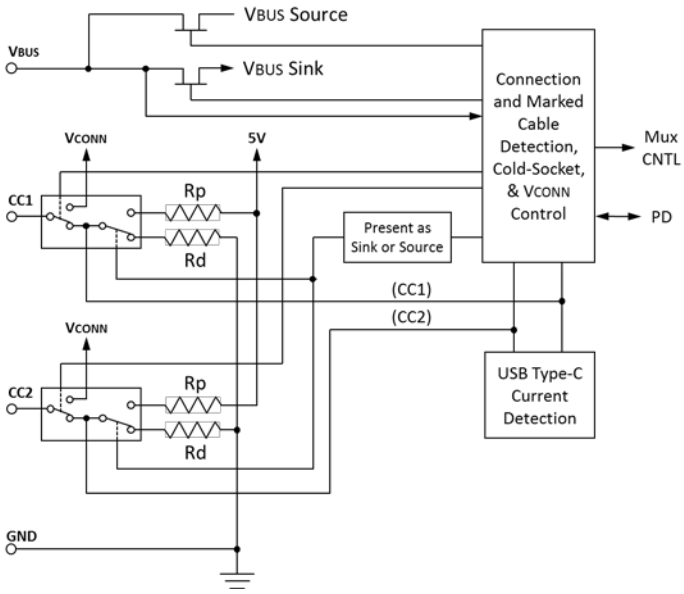
Referring to Figure 4-9, a port that behaves as a Sink has the following functional characteristics:

1. The Sink terminates both CC1 and CC2 to GND using pull-down resistors.
2. The Sink determines that a Source is attached by the presence of power on VBUS.
3. The Sink uses the CC pin pull-up characteristic to detect and establish the correct routing for the USB SuperSpeed data path.
4. The Sink can optionally monitor CC to detect an available higher USB Type-C Current from the Source. The Sink shall manage its load to stay within the detected Source current limit.
5. If the Sink supports advanced functions (USB Power Delivery and/or Alternate Modes), *USB PD* communication is required.

Figure 4-10 illustrates the functional model for CC1 and CC2 for a Sink that supports *USB PD* PR_Swap and supports *USB PD* VCONN_Swap prior to attach.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

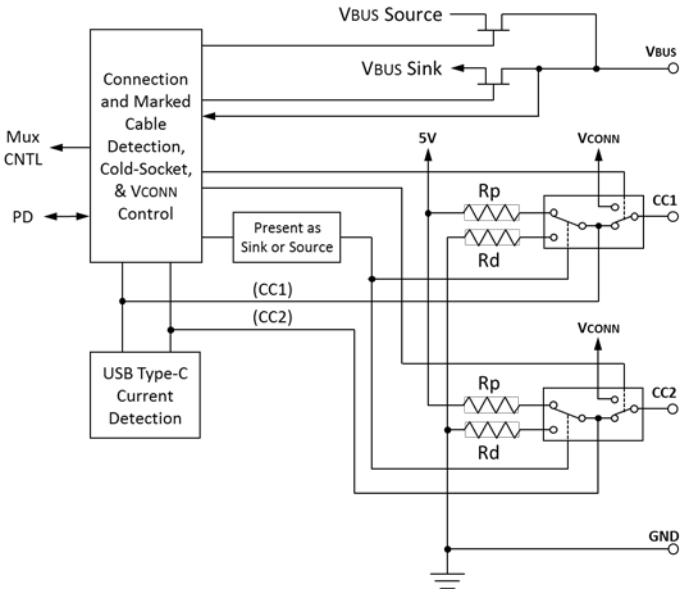
Figure 4-10 UFP Functional Model Supporting USB PD PR_Swap and VCONN_Swap



4.5.1.3.3 Dual-Role-Power (DRP) Configuration Channel Functional Model

Figure 4-11 illustrates the functional model for CC1 and CC2 for a DRP presenting as a Source prior to attach. This illustration includes consideration for both the USB Type-C Current and the *USB PD* features.

Figure 4-11 DRP Functional Model for CC1 and CC2



Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:

1. The DRP uses a FET to enable/disable power delivery across VBUS and initially when in Source mode has VBUS disabled.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

2. The DRP uses switches for presenting as a Source or Sink.
3. The DRP has logic used during initial attach to toggle between Source and Sink operation:
    a. Until a specific stable state is established, the DRP alternates between exposing itself as a Source and Sink. The timing of this process is dictated by a period (tDRP), percentage of time that a DRP exposes Rp (dcSRC.DRP) and role transition time (tDRPTransition).
    b. When the DRP is presenting as a Source, it follows Source operation to detect an attached Sink – if a Sink is detected, it applies VBUS, VCONN, and continues to operate as a Source for a minimum of tDRPHold (e.g., cease alternating).
    c. When the DRP is presenting as a Sink, it monitors VBUS to detect that it is attached to a Source – if a Source is detected, it continues to operate as a Sink (cease alternating).
4. If the DRP supports advanced functions (USB Power Delivery and/or Alternate Modes), *USB PD* communication is required.

4.5.1.4 USB Type-C Port Power Roles and Role Swapping Mechanisms

USB Type-C ports on products (USB hosts, USB devices, USB chargers, etc.) can be generally characterized as implementing one of seven power role behavioral models:

- Source-only
- Source (Default) – strong preference toward being a Source but subsequently capable of becoming a Sink using USB PD swap mechanisms.
- Sink-only
- Sink (Default) – strong preference toward being a Sink but subsequently capable of becoming a Source using USB PD swap mechanisms.
- DRP: Toggling (Source/Sink)
- DRP: Sourcing Device
- DRP: Sinking Host

Two independent sets of swapping mechanisms are defined for USB Type-C port implementations, one based on role swapping within the initial state machine connection process and the other based on subsequent use of *USB PD*-based swapping mechanisms.

4.5.1.4.1 USB Type-C State-Machine-Based Role Swapping

During the initial USB Type-C state machine connection process, the products being connected end up in one of the two following roles associated with the termination of its port:

- Rp → VBUS and VCONN source and behaving as a downstream facing port (USB Host)
- Rd → VBUS sink and behaving as an upstream facing port (USB Device)

A USB Type-C DRP-based product may incorporate either or both the Try.SRC and Try.SNK swap mechanisms to affect the resulting role. Try.SRC allows a DRP that has a policy-based preference to be a Source when connecting to another DRP to effect a transition from a destined Sink role to the Source role. Alternately, Try.SNK allows a DRP that has a policy-based preference to be a Sink when connecting to another DRP to effect a transition from a destined Source role to the Sink role. Connection timing and other factors are involved in this process as defined in the USB Type-C state machine operation (see Section 4.5.2). It is

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

important to note that these mechanisms, Try.SRC and Try.SNK, can only be used once as part of the initial connection process.

Try.SRC and Try.SNK are intended for lower-complexity products that may have a need to swap functional roles when connecting to another multi-role product but otherwise doesn't benefit from implementing *USB PD*, e.g. connecting two phones together for exchanging data and establishing the phone with active user input in the "host" role.

4.5.1.4.2 USB PD-based Power Role, Data Role and VCONN Swapping

Following the completion of the initial USB Type-C state machine connection process, products may use *USB PD*-based swapping mechanisms to command a change power roles, data roles and which end of the cable will supply VCONN. These mechanisms are:

- *USB PD* PR_Swap : swaps Source (Rp) and Sink (Rd)
- *USB PD* DR_Swap : swaps DFP (host data) and UFP (device data) roles
- *USB PD* VCONN_Swap : swaps which port supplies VCONN

Table 4-9 summarizes the behaviors of a port in response to the three *USB PD* swap commands.

Table 4-9 USB PD Swapping Port Behavior Summary

	DFP/UFP Data Roles	Rp/Rd	VBUS Source/Sink	VCONN Source
PR_Swap	Unchanged	Swapped	Swapped	Unchanged
DR_Swap	Swapped	Unchanged	Unchanged	Unchanged
VCONN_Swap	Unchanged	Unchanged	Unchanged	Swapped*

* Swapping of VCONN source port

4.5.1.4.3 Power Role Behavioral Model Summary

Table 4-10 provides a summary of the defining characteristics of the seven fundamental power roles.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 4-10 Power Role Behavioral Model Summary

Power Role		Toggles	PR_Swap	USB Host	USB Device	DFP	UFP	DR_Swap	Try.SRC/ Try.SNK	Connects with
Source-Only		No	NA	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink/ DRP
Source (Default)		No	Req.	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink/ DRP
Sink-Only		No	NA	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source/ DRP
Sink (Default)		No	Req.	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source/ DRP
DRP	**Toggling (Source/Sink)**	Req.	Req.	Opt.	Opt.	Req.	Req.	Req.	Opt. if no PD support NA if PD supported	Source/ Sink/ DRP
	Sourcing Device	Req.	Req.	NA	Req.	Req.	Req.	Req.	NA	
	Sinking Host	Req.	Req.	Req.	NA	Req.	Req.	Req.	NA	

Note: 1. Requires use of DR_Swap

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Microchip Ex. 1019, p. 132
Microchip v. Aptiv
IPR2024-00496

4.5.2 CC Functional and Behavioral Requirements

This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining sub-sections.

The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual-Role-Power) port is capable of acting as either a Source or Sink. Typically Sources are found on hosts and supply VBUS while a Sink is found on a device and consumes power from VBUS. When a connection is initially made, the port's initial power state and data role are established. *USB PD* introduces three swap commands that may alter a port's power or data role:

- The PR_Swap command changes the port's power state as reflected in the following state machines. PR_Swap does not change the port sourcing VCONN.
- The DR_Swap command has no effect on the following state machines or VCONN as it only changes the port's data role.
- VCONN_Swap command changes the port sourcing VCONN. The PR_Swap command and DR_Swap command have no effect on the port sourcing VCONN.

Note: *USB PD* defines another optional swapping mechanism (FR_Swap) that is used in a special case where a user interaction could inadvertently trigger a need to change the source of VBUS. A variant of PR_Swap, FR_Swap similarly swaps Source (Rp) and Sink (Rd) between two connected ports. For purposes of this specification, only PR_Swap is explicitly considered in the behavior requirements and implementations that support FR_Swap should, where applicable, apply PR_Swap-related behaviors to FR_Swap. See the *USB PD* specification for further details regarding FR_Swap.

The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable shall behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle, These devices shall apply and sense CC voltage levels on pin A5 only and pin B5 shall have an impedance above zOPEN, unless it is a Powered Accessory, in which case B5 shall have an impedance Ra.

4.5.2.1 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors.

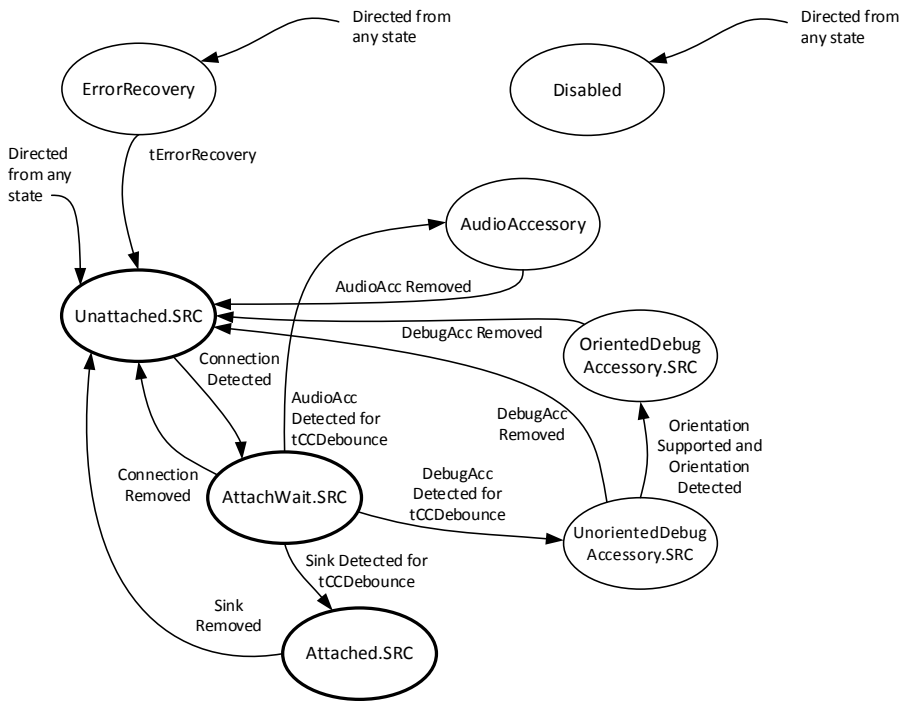
Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section 4.5.2.4 for a description of which states are mandatory for each port type, and a list of states where *USB PD* communication is permitted.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-12 illustrates a connection state diagram for a Source (Host/Hub DFP).

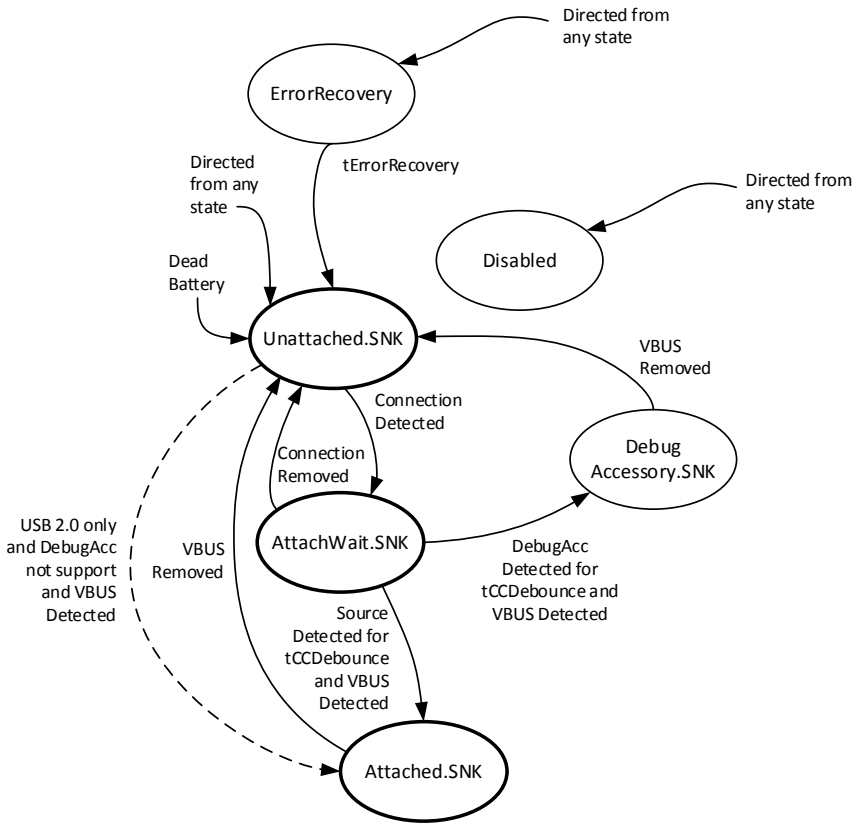
Figure 4-12 Connection State Diagram: Source



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-13 illustrates a connection state diagram for a simple Sink (Device/Hub UFP).

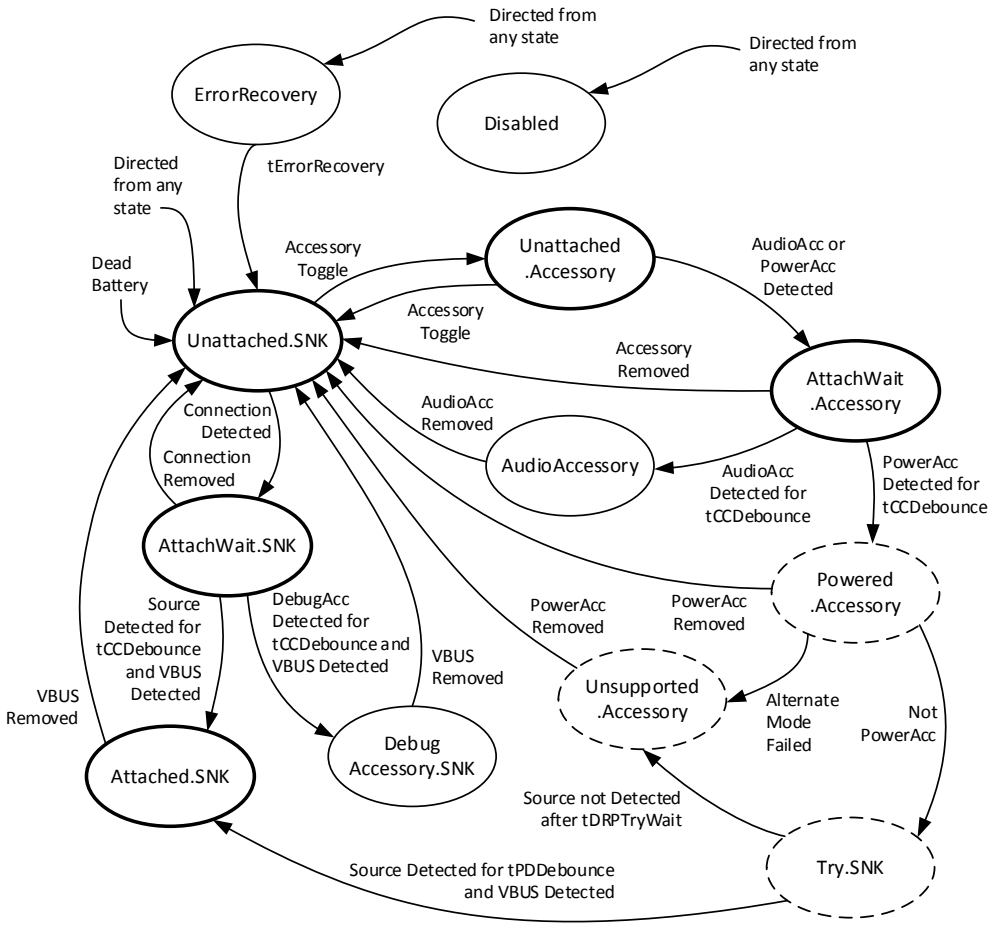
Figure 4-13 Connection State Diagram: Sink



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

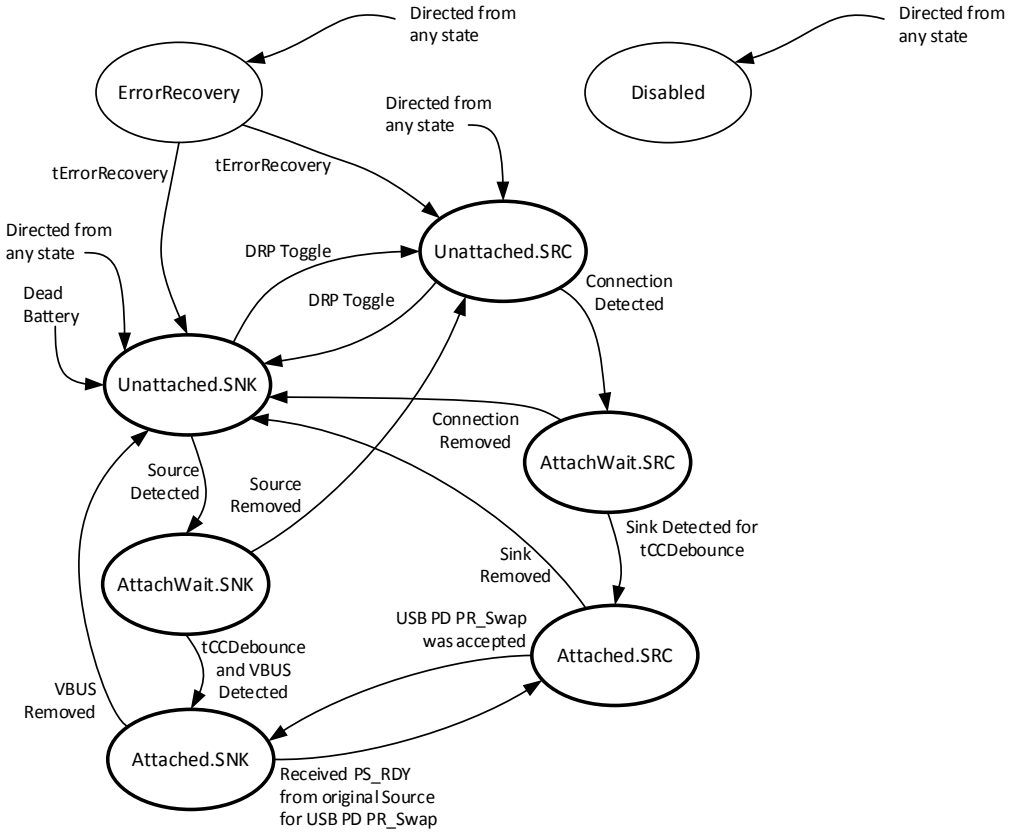
Figure 4-14 Connection State Diagram: Sink with Accessory Support



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-15 illustrates a connection state diagram for a simple DRP (Dual-Role-Power) port.

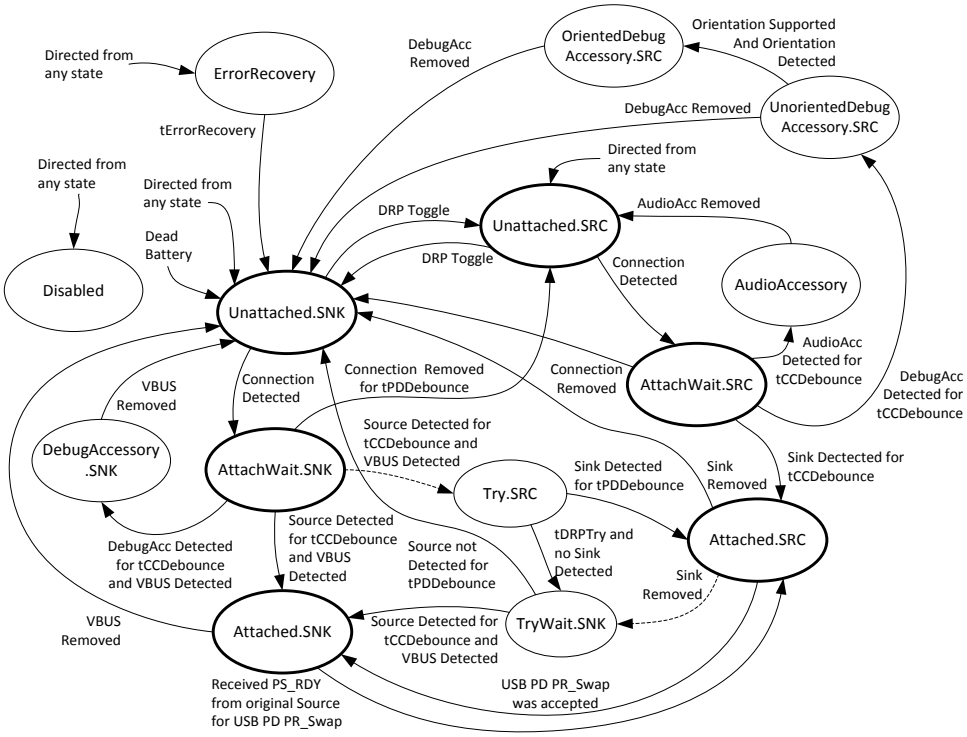
Figure 4-15 Connection State Diagram: DRP



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-16 illustrates a connection state diagram for a DRP that supports Try.SRC and Accessory Modes.

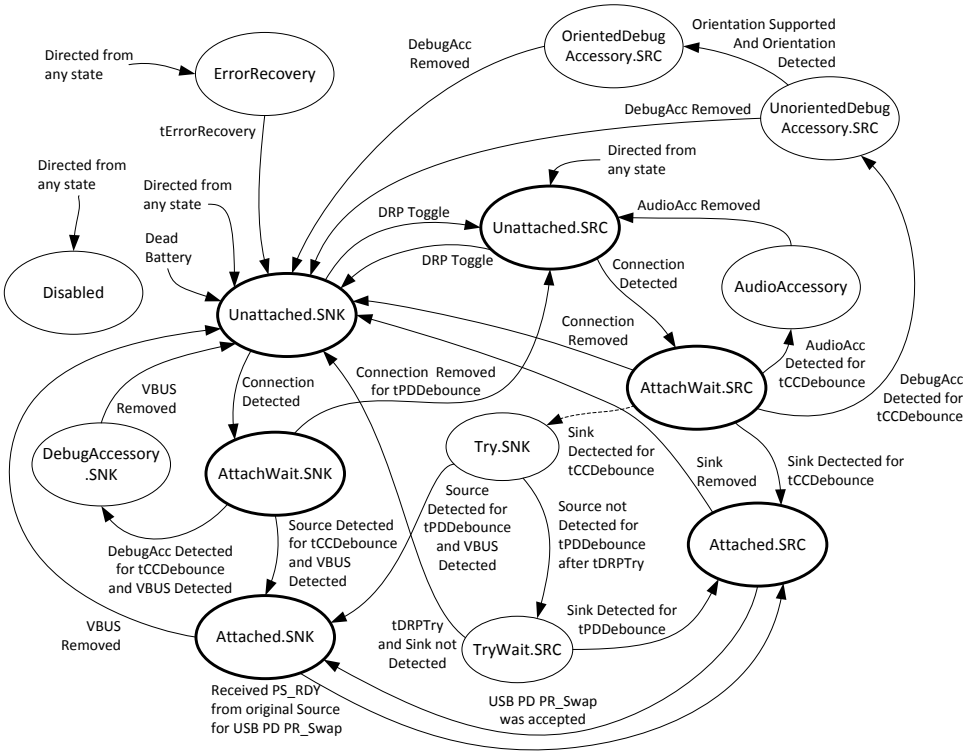
Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-17 illustrates a connection state diagram for a DRP that supports Try.SNK and Accessory Modes.

Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.

Table 4-11 Source Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	**Open, Rp**	Above vOPEN
SRC.Rd	**Rd**	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	**Ra**	Below maximum vRa

Table 4-12 Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	**Rp**	Above minimum vRd-Connect
SNK.Open	**Open, Ra, Rd**	Below maximum vRa

4.5.2.2.1 Disabled State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

The Disabled state is where the port prevents connection from occurring by removing all terminations from the CC pins.

The port should transition to the Disabled state from any other state when directed.

A port may choose not to support the Disabled state. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states after power-on.

4.5.2.2.1.1 Disabled State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.

4.5.2.2.1.2 Exiting From Disabled State

A Sink shall transition to Unattached.SNK when directed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

A Source shall transition to Unattached.SRC when directed.

A DRP shall transition to either Unattached.SNK or Unattached.SRC when directed.

4.5.2.2.2 ErrorRecovery State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

The ErrorRecovery state is where the port removes the terminations from the CC1 and CC2 pins for tErrorRecovery followed by transitioning to the appropriate Unattached.SNK or Unattached.SRC state based on port type. This is the equivalent of forcing a detach event and looking for a new attach.

The port should transition to the ErrorRecovery state from any other state when directed.

A port may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the port shall be directed to the Disabled state if supported. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states.

4.5.2.2.2.1 ErrorRecovery State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.

4.5.2.2.2.2 Exiting From ErrorRecovery State

A Sink shall transition to Unattached.SNK after tErrorRecovery.

A Source shall transition to Unattached.SRC after tErrorRecovery.

A DRP shall transition to either Unattached.SNK or Unattached.SRC after tErrorRecovery.

4.5.2.2.3 Unattached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

When in the Unattached.SNK state, the port is waiting to detect the presence of a Source.

A port with a dead battery shall enter this state while unpowered.

4.5.2.2.3.1 Unattached.SNK Requirements

The port shall not drive VBUS or VCONN.

Both CC1 and CC2 pins shall be independently terminated to ground through Rd.

4.5.2.2.3.2 Exiting from Unattached.SNK State

If the port supports *USB PD* or accessories, the port shall transition to AttachWait.SNK when a Source connection is detected, as indicated by the SNK.Rp state on at least one of its CC pins.

A USB 2.0 only Sink that doesn't support accessories and is self-powered or requires only default power and does not support *USB PD* may transition directly to Attached.SNK when VBUS is detected.

A DRP shall transition to Unattached.SRC within tDRPTransition after the state of both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

A Sink with Accessory support shall transition to Unattached.Accessory within tDRPTransition after the state of both the CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

4.5.2.2.4 AttachWait.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

When in the AttachWait.SNK state, the port has detected the SNK.Rp state on at least one of its CC pins and is waiting for VBUS.

4.5.2.2.4.1 AttachWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

It is strongly recommended that a USB 3.1 SuperSpeed device hold off VBUS detection to the device controller until the Attached.SNK state or the DebugAccessory.SNK state is reached, i.e. at least one CC pin is in the SNK.Rp state. Otherwise, it may connect as USB 2.0 when attached to a legacy host or hub's DFP.

4.5.2.2.4.2 Exiting from AttachWait.SNK State

A Sink shall transition to Unattached.SNK when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

A DRP shall transition to Unattached.SRC when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

The port shall transition to Attached.SNK after the state of only one of the CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.

If the port supports Debug Accessory Mode, the port shall transition to DebugAccessory.SNK if the state of both the CC1 and CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the DAM Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Rp, but this event will not exceed tPDDebounce.

A DRP that strongly prefers the Source role may optionally transition to Try.SRC instead of Attached.SNK when the state of only one CC pin has been SNK.Rp for at least tCCDebounce and VBUS is detected.

4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using *USB PD* commands.

A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use *USB PD*.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 142
Microchip v. Aptiv
IPR2024-00496

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).

If the port supports signaling on USB SuperSpeed pairs, it shall functionally connect the USB SuperSpeed pairs and maintain the connection during and after a *USB PD* PR_Swap.

If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.

If the port has entered the Attached.SNK state from the Attached.SRC state following a *USB PD* PR_Swap, the port shall terminate the connected CC pin to ground through Rd.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.3.

The port may negotiate a *USB PD* PR_Swap, DR_Swap or VCONN_Swap.

By default, upon entry from AttachWait.SNK or Unattached.SNK, VCONN shall not be supplied in the Attached.SNK state. If Attached.SNK is entered from Attached.SRC as a result of a *USB PD* PR_Swap, it shall maintain VCONN supply state, whether on or off, and its data role/connections. A *USB PD* DR_Swap has no effect on which port sources VCONN.

The port may negotiate a *USB PD* VCONN_Swap. When the port successfully executes *USB PD* VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes *USB PD* VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF.

4.5.2.2.5.2 Exiting from Attached.SNK State

A port that is not in the process of a *USB PD* PR_Swap or a *USB PD* Hard Reset shall transition to Unattached.SNK when VBUS falls below 3.67 V. Note if VBUS has been adjusted by *USB PD* to operate above 5 V, then the port shall transition to Unattached.SNK when VBUS falls below 80% of the negotiated value. If supplying VCONN, the port shall cease to supply it within tVCONNOFF of exiting Attached.SNK.

After receiving a *USB PD* PS_RDY from the original Source during a *USB PD* PR_Swap, the port shall transition directly to the Attached.SRC state (i.e., remove Rd from CC, assert Rp on CC and supply VBUS), but shall maintain its VCONN supply state, whether off or on, and its data role/connections.

4.5.2.2.6 Unattached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16 and Figure 4-17.

When in the Unattached.SRC state, the port is waiting to detect the presence of a Sink or an Accessory.

4.5.2.2.6.1 Unattached.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The port shall provide a separate Rp termination on the CC1 and CC2 pins as specified in Table 4-15. Note: A direct-connected Source (e.g. a captive cabled product) presents a single Rp termination on its CC pin (A5).

4.5.2.2.6.2 Exiting from Unattached.SRC State

The port shall transition to AttachWait.SRC when VBUS is vSafe0V and:

- The SRC.Rd state is detected on either CC1 or CC2 pin or
- The SRC.Ra state is detected on both the CC1 and CC2 pins.

Note: A cable without an attached device can be detected, when the SRC.Ra state is detected on one of the CC1 or CC2 pins and the other CC pin is SRC.Open. However in this case, the port shall not transition to AttachWait.SRC.

A DRP shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

4.5.2.2.7 AttachWait.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16 and Figure 4-17.

The AttachWait.SRC state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a Sink is connected.

4.5.2.2.7.1 AttachWait.SRC Requirements

The requirements for this state are identical to Unattached.SRC.

4.5.2.2.7.2 Exiting from AttachWait.SRC State

The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.

If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the SRC.Ra state is detected on both the CC1 and CC2 pins for at least tCCDebounce.

If the port supports Debug Accessory Mode, it shall transition to UnorientedDebugAccessory.SRC when the SRC.Rd state is detected on both the CC1 and CC2 pins for at least tCCDebounce.

A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on both the CC1 and CC2 pins.

A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin and the other CC pin is SRC.Ra.

A DRP that strongly prefers the Sink role may optionally transition to Try.SNK instead of Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.

4.5.2.2.8 Attached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16 and Figure 4-17.

When in the Attached.SRC state, the port is attached and operating as a Source. When the port initially enters this state it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using *USB PD* commands.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.2.2.8.1 Attached.SRC Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the Attached.SRC state by detecting which of the CC1 or CC2 pins is connected through the cable, i.e., which CC pin is in the SRC.Rd state.

If the port has entered this state from the AttachWait.SRC state or the Try.SRC state, the SRC.Rd state will be on only one of the CC1 or CC2 pins. The port shall source current on this CC pin and monitor its state.

If the port has entered this state from the Attached.SNK state as the result of a *USB PD* PR_Swap, the port shall source current on the connected CC pin and monitor its state.

The port shall provide an Rp as specified in Table 4-15.

The port shall supply VBUS current at the level it advertises on Rp.

The port shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.

The port shall not initiate any *USB PD* communications until VBUS reaches vSafe5V.

If the port supports signaling on USB SuperSpeed pairs, it shall:

- Functionally connect the USB SuperSpeed pairs
- For VCONN, do one of two things:
  - Apply VCONN unconditionally to the CC pin not in the SRC.Rd state, or
  - Apply VCONN to the CC pin in the SRC.Ra state.

A port that does not support signaling on USB SuperSpeed pairs may supply VCONN in the same manner described above.

The port may negotiate a *USB PD* PR_Swap, DR_Swap or VCONN_Swap.

If the port supplies VCONN, it shall do so within tVCONNON.

The port shall not supply VCONN if it has entered this state as a result of a *USB PD* PR_Swap and was not previously supplying VCONN. A *USB PD* DR_Swap has no effect on which port sources VCONN.

The port may negotiate a *USB PD* VCONN_Swap. When the port successfully executes *USB PD* VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes *USB PD* VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON.

4.5.2.2.8.2 Exiting from Attached.SRC State

A Source shall transition to Unattached.SRC when the SRC.Open state is detected on the monitored CC pin.

When the SRC.Open state is detected on the monitored CC pin, a DRP shall transition to Unattached.SNK unless it strongly prefers the Source role. In that case, it shall transition to TryWait.SNK. This transition to TryWait.SNK is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

would enter Try.SRC from AttachWait.SNK shall enter TryWait.SNK for a Sink detach from Attached.SRC.

A port shall cease to supply VBUS within tVBUSOFF of exiting Attached.SRC.

A port that is supplying VCONN shall cease to supply it within tVCONNOFF of exiting Attached.SRC, unless it is exiting as a result of a *USB PD* PR_Swap.

After a *USB PD* PR_Swap is accepted (i.e., either an Accept message is received or acknowledged), a DRP shall transition directly to the Attached.SNK state (i.e., remove Rp from CC, assert Rd on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.

4.5.2.2.9 Try.SRC State

This state appears in Figure 4-16.

When in the Try.SRC state, the port is querying to determine if the port partner supports the Sink role.

Note: if both Try.SRC and Try.SNK mechanisms are implemented, only one shall be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.9.1 Try.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide an Rp as specified in Table 4-15.

4.5.2.2.9.2 Exiting from Try.SRC State

The port shall transition to Attached.SRC when the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tPDDebounce.

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected.

4.5.2.2.10 TryWait.SNK State

This state appears in Figure 4-16.

When in the TryWait.SNK state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively the port is responding to the Sink being removed while in the Attached.SRC state.

4.5.2.2.10.1 TryWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

4.5.2.2.10.2 Exiting from TryWait.SNK State

The port shall transition to Attached.SNK after tCCDebounce if or when VBUS is detected. Note the Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tPDDebounce.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The port shall transition to Unattached.SNK when the state of both of the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

4.5.2.2.11 Try.SNK State

This state appears in Figure 4-14 and Figure 4-17.

When in the Try.SNK state, the port is querying to determine if the port partner supports the Source role.

Note: if both Try.SRC and Try.SNK mechanisms are implemented, only one shall be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.11.1 Try.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

4.5.2.2.11.2 Exiting from Try.SNK State

The port shall wait for tDRPTry and only then begin monitoring the CC1 and CC2 pins for the SNK.Rp state.

The port shall then transition to Attached.SNK when the SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tPDDebounce and VBUS is detected.

Alternatively, the port shall transition to TryWait.SRC if SNK.Rp state is not detected for tPDDebounce. A Sink with Accessory Support shall transition to Unsupported.Accessory if SNK.Rp state is not detected for tDRPTryWait.

Note: The Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tPDDebounce.

4.5.2.2.12 TryWait.SRC State

This state appears in Figure 4-17.

When in the TryWait.SRC state, the port has failed to become a Sink and is waiting to attach as a Source.

4.5.2.2.12.1 TryWait.SRC Requirements

The requirements for this state are identical to Unattached.SRC.

4.5.2.2.12.2 Exiting from TryWait.SRC State

The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC pins for at least tCCDebounce.

The port shall transition to Unattached.SNK after tDRPTry if neither of the CC1 or CC2 pins are in the SRC.Rd state.

4.5.2.2.13 Unattached.Accessory State

This state appears in Figure 4-14.

The Unattached.Accessory state allows accessory-supporting Sinks to connect to audio or VCONN-powered accessories.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

This state is functionally equivalent to the Unattached.SRC state in a DRP, except that Attached.SRC is not supported.

4.5.2.2.13.1 Unattached.Accessory Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide an Rp as specified in Table 4-15.

4.5.2.2.13.2 Exiting from Unattached.Accessory State

The port shall transition to AttachWait.Accessory when the state of both the CC1 and CC2 pins is SRC.Ra or SRC.Rd.

A port that supports VCONN-powered accessories also shall transition to AttachWait.Accessory when the state of either CC1 or CC2 pin is SRC.Ra and the other CC pin is SRC.Rd.

Otherwise, the port shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

4.5.2.2.14 AttachWait.Accessory State

This state appears in Figure 4-14.

The AttachWait.Accessory state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a cable is plugged in.

4.5.2.2.14.1 AttachWait.Accessory Requirements

The requirements for this state are identical to Unattached.Accessory.

4.5.2.2.14.2 Exiting from AttachWait.Accessory State

If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.

The port shall transition to Unattached.SNK when the state of either the CC1 or CC2 pin is SRC.Open for at least tCCDebounce.

If the port supports VCONN-powered accessories, it shall transition to PoweredAccessory state if the state of either the CC1 or CC2 pin is SRC.Rd and the other CC pin is SRC.Ra concurrently for at least tCCDebounce.

4.5.2.2.15 AudioAccessory State

This state appears in Figure 4-12, Figure 4-14, Figure 4-16 and Figure 4-17.

The AudioAccessory state is used for the Audio Adapter Accessory Mode specified in Appendix A.

4.5.2.2.15.1 AudioAccessory Requirements

The port shall reconfigure its pins as detailed in Appendix A.

The port shall not drive VBUS or VCONN. A port that sinks current from the audio accessory over VBUS shall not draw more than 500 mA.

The port shall provide an Rp as specified in Table 4-15.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The port shall source current on at least one of the CC1 or CC2 pins and monitor to detect when the state is no longer SRC.Ra. If the port sources and monitors only one of CC1 or CC2, then it shall ensure that the termination on the unmonitored CC pin does not affect the monitored signal when the port is connected to an Audio Accessory that may short both CC1 and CC2 pins together.

4.5.2.2.15.2 Exiting from AudioAccessory State

If the port is a Sink, the port shall transition to Unattached.SNK when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.

If the port is a Source or DRP, the port shall transition to Unattached.SRC when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.

4.5.2.2.16 UnorientedDebugAccessory.SRC

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The UnorientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.16.1 UnorientedDebugAccessory.SRC Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall provide an Rp as specified in Table 4-15 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.

The port may connect any non-orientation specific debug signals for Debug Accessory Mode operation only after entry to this state.

4.5.2.2.16.2 Exiting from UnorientedDebugAccessory.SRC State

If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.

The port shall transition to OrientedDebugAccessory.SRC state if orientation is required and detected as described in Section B.2.6.1.2.

4.5.2.2.17 OrientedDebugAccessory.SRC State

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The OrientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.17.1 OrientedDebugAccessory.SRC State Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall provide an Rp as specified in Table 4-15 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.

The port shall connect any orientation specific debug signals for Debug Accessory Mode operation only after entry to this state. Any non-orientation specific debug signals for Debug Accessory Mode operation shall be connected or remain connected in this state.

If the port needs to establish *USB PD* communications, it shall do so only after entry to this state. The port shall not initiate any *USB PD* communications until VBUS reaches vSafe5V. In this state, the port takes on the initial *USB PD* role of DFP/Source.

4.5.2.2.17.2 Exiting from OrientedDebugAccessory.SRC State

If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.

4.5.2.2.18 DebugAccessory.SNK

This state appears in Figure 4-13, Figure 4-14, Figure 4-16 and Figure 4-17.

The DebugAccessory.SNK state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.18.1 DebugAccessory.SNK Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall not drive VBUS or VCONN.

The port shall provide an Rd as specified in Table 4-16 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

If supported, orientation is determined as outlined in Section B.2.6.1.1. The port shall connect any debug signals for Debug Accessory Mode operation only after entry to this state.

4.5.2.2.18.2 Exiting from DebugAccessory.SNK State

The port shall transition to Unattached.SNK when VBUS is no longer present.

4.5.2.2.19 PoweredAccessory State

This state appears in Figure 4-14.

When in the PoweredAccessory state, the port is powering a VCONN–Powered Accessory.

4.5.2.2.19.1 PoweredAccessory Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the PoweredAccessory state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., which CC pin is in the SRC.Rd state).

The SRC.Rd state is detected on only one of the CC1 or CC2 pins. The port shall advertise either 1.5 A or 3.0 A (see Table 4-15) on this CC pin and monitor its state.

The port shall supply VCONN (2.7 V minimum) on the unused CC pin within tVconnON-PA of entering the PoweredAccessory state.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The port shall not drive VBUS.

When the port initially enters the PoweredAccessory state it shall operate as a DFP.

The port shall use *USB Power Delivery* Structured Vendor Defined Messages (Structured VDMs) to identify the accessory and enter an Alternate Mode.

4.5.2.2.19.2 Exiting from PoweredAccessory State

The port shall transition to Unattached.SNK when the SRC.Open state is detected on the monitored CC pin.

The port shall transition to Try.SNK if the attached device is not a VCONN–Powered Accessory. For example, the attached device does not support *USB PD* or does not respond to *USB PD* commands required for a VCONN–Powered Accessory (e.g., Discover SVIDs, Discover Modes, etc.) or is a Sink or DRP attached through a Powered Cable.

The port shall transition to Unsupported.Accessory if the attached device is a VCONN–Powered Accessory but the port has not successfully entered an Alternate Mode within tAMETimeout (see Section 5.1).

The port shall cease to supply VCONN within tVCONNOFF of exiting the PoweredAccessory state.

4.5.2.2.20 Unsupported.Accessory State

This state appears in Figure 4-14.

If a VCONN–powered accessory does not enter an Alternate Mode, the Unsupported.Accessory state is used to wait until the accessory is unplugged before continuing.

4.5.2.2.20.1 Unsupported.Accessory Requirements

Only one of the CC1 or CC2 pins shall be in the SRC.Rd state. The port shall advertise Default USB Power (see Table 4-15) on this CC pin and monitor its voltage.

The port shall not drive VBUS or VCONN.

4.5.2.2.20.2 Exiting from Unsupported.Accessory

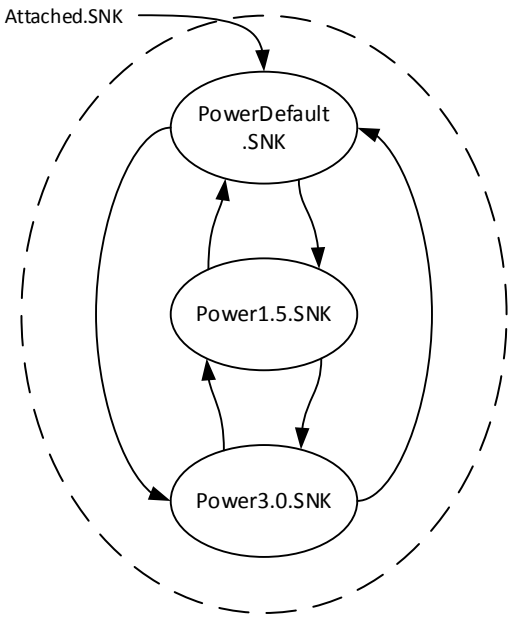
The port shall transition to Unattached.SNK when the SRC.Open state is detected on the monitored CC pin.

4.5.2.3 Sink Power Sub-State Requirements

When in the Attached.SNK state and the Source is supplying default VBUS, the port shall operate in one of the sub-states shown in Figure 4-18. The initial Sink Power Sub-State is PowerDefault.SNK. Subsequently, the Sink Power Sub-State is determined by Source's USB Type-C current advertisement. The port in Attached.SNK shall remain within the Sink Power Sub-States until either VBUS is removed or a *USB PD* contract is established with the Source.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-18 Sink Power Sub-States



The Sink is only required to implement Sink Power Sub-State transitions if the Sink wants to consume more than default USB current.

4.5.2.3.1 PowerDefault.SNK Sub-State

This sub-state supports Sinks consuming current within the lowest range (default) of Source-supplied current.

4.5.2.3.1.1 PowerDefault.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the port wants to consume more than the default USB power, it shall monitor vRd to determine if more current is available from the Source.

4.5.2.3.1.2 Exiting from PowerDefault.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tPDDebounce.

For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State.

For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.

4.5.2.3.2 Power1.5.SNK Sub-State

This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.

4.5.2.3.2.1 Power1.5.SNK Requirements

The port shall draw no more than 1.5 A from VBUS.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 152
Microchip v. Aptiv
IPR2024-00496

The port shall monitor vRd while it is in this sub-state.

4.5.2.3.2.2 Exiting from Power1.5.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tPDDebounce.

For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.

4.5.2.3.3 Power3.0.SNK Sub-State

This sub-state supports Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of Source-supplied current.

4.5.2.3.3.1 Power3.0.SNK Requirements

The port shall draw no more than 3.0 A from VBUS.

The port shall monitor vRd while it is in this sub-state.

4.5.2.3.3.2 Exiting from Power3.0.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tPDDebounce.

For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.2.4 Connection States Summary

Table 4-13 defines the mandatory and optional states for each type of port.

Table 4-13 Mandatory and Optional States

	SOURCE	SINK	DRP	USB PD Communication
Disabled	Optional	Optional	Optional	Not Permitted
ErrorRecovery	Optional	Optional	Optional	Not Permitted
Unattached.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWait.SNK	N/A	Mandatory[1]	Mandatory	Not Permitted
Attached.SNK	N/A	Mandatory	Mandatory	Permitted
Unattached.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWait.SRC	Mandatory	N/A	Mandatory	Not Permitted
Attached.SRC	Mandatory	N/A	Mandatory	Permitted
Try.SRC[4]	N/A	N/A	Optional	Not Permitted
TryWait.SNK[2]	N/A	N/A	Optional	Not Permitted
Try.SNK[4]	N/A	N/A	Optional	Not Permitted
TryWait.SRC[5]	N/A	N/A	Optional	Not Permitted
AudioAccessory	Optional	Optional	Optional	Not Permitted
UnorientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Not Permitted
OrientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Permitted
DebugAccessory.SNK	N/A	Optional	Optional	Permitted
Unattached.Accessory	N/A	Optional	N/A	Not Permitted
AttachWait.Accessory	N/A	Optional	N/A	Not Permitted
PoweredAccessory	N/A	Optional	N/A	Permitted
Unsupported.Accessory[3]	N/A	Optional	N/A	Not Permitted
PowerDefault.SNK	N/A	Mandatory	Mandatory	Permitted
Power1.5.SNK	N/A	Optional	Optional	Permitted
Power3.0.SNK	N/A	Optional	Optional	Permitted

Note:

1. Optional for UFP applications that are USB 2.0-only, consume USB Default Power and do not support *USB PD* or accessories.
2. TryWait.SNK is mandatory when Try.SRC is supported.
3. Unsupported.Accessory is mandatory when PoweredAccessory is supported.
4. Try.SRC and Try.SNK shall not be supported at the same time, although an unattached device may dynamically choose between Try.SRC and Try.SNK state machines based on external factors.
5. TryWait.SRC is mandatory when Try.SNK is supported.
6. UnorientedDebugAccessory.SRC is required for any Source or DRP that supports Debug Accessory Mode. OrientedDebugAccessory.SRC is only required if orientation detection is necessary in Debug Accessory Mode.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.3 USB Port Interoperability Behavior

This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.

4.5.3.1 USB Type-C Port to USB Type-C Port Interoperability Behaviors

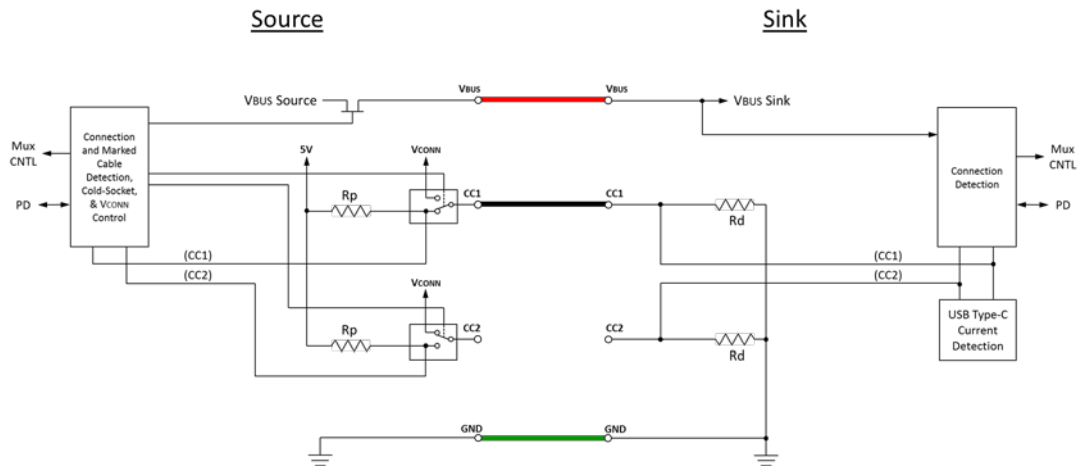
The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs as presented in Table 4-6. In all of the described behaviors, the impact of *USB PD*-based swaps (PR_Swap, DR_Swap or VCONN_Swap) are not considered.

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.

4.5.3.1.1 Source to Sink Behavior

Figure 4-19 illustrates the functional model for a Source connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-19 Source to Sink Functional Model



The following describes the behavior when a Source is connected to a Sink.

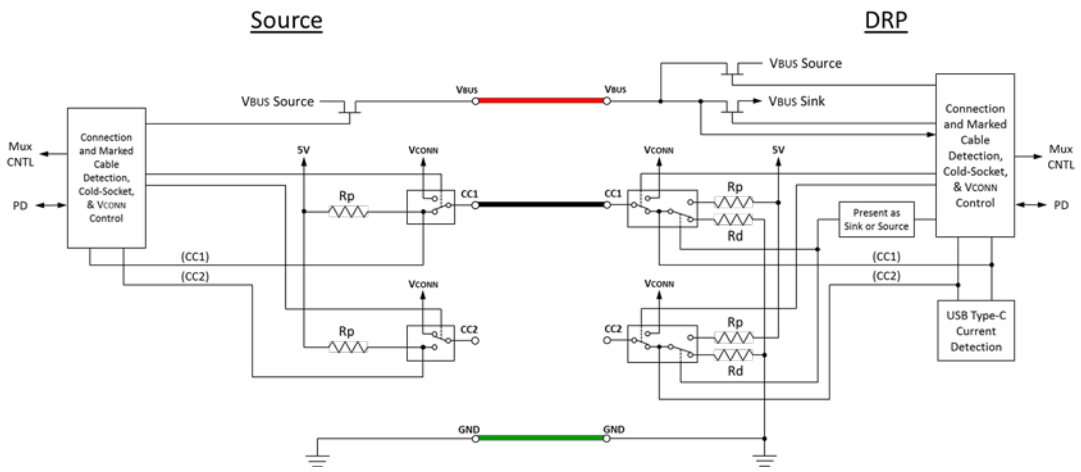
1. Source and Sink in the unattached state
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the Sink's pull-down on CC and enters Attached.SRC through AttachWait.SRC
   - Source turns on VBUS and VCONN
3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK. Sink may skip AttachWait.SNK if it is USB 2.0 only and does not support accessories.
   - Sink detects VBUS and enters Attached.SNK through AttachWait.SNK
4. While the Source and Sink are in the attached state:
   - Source adjusts Rp as needed to limit the current the Sink may draw
   - Sink detects and monitors vRd for available current on VBUS
   - Source monitors CC for detach and when detected, enters Unattached.SRC
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 155
Microchip v. Aptiv
IPR2024-00496

4.5.3.1.2 Source to DRP Behavior

Figure 4-20 illustrates the functional model for a Source connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-20 Source to DRP Functional Model



The following describes the behavior when a Source is connected to a DRP.

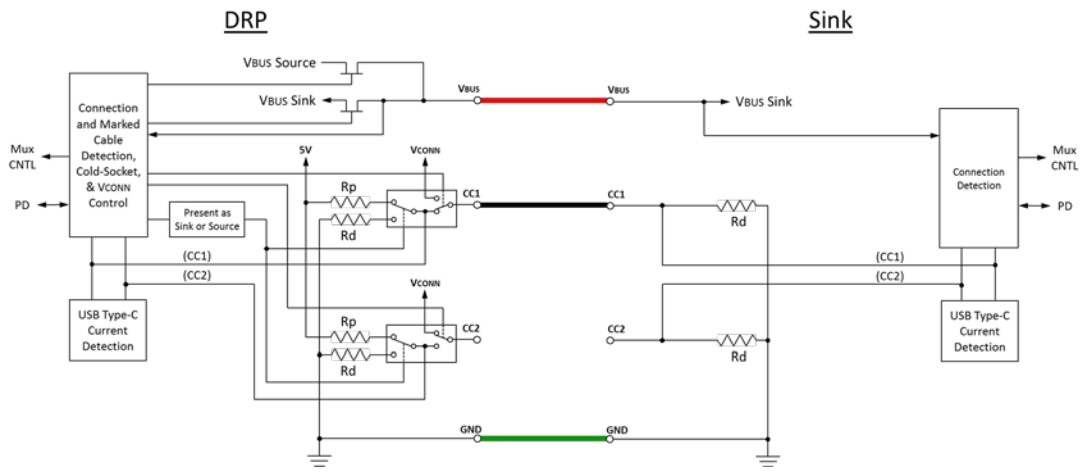
1. Source and DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the DRP's pull-down on CC and enters AttachWait.SRC. After tCCDebounce it then enters Attached.SRC.
   - Source turns on VBUS and VCONN
3. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   - DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters Attached.SNK.
4. While the Source and DRP are in their respective attached states:
   - Source adjusts Rp as needed to limit the current the DRP (as Sink) may draw
   - DRP (as Sink) detects and monitors vRd for available current on VBUS
   - Source monitors CC for detach and when detected, enters Unattached.SRC
   - DRP (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 156
Microchip v. Aptiv
IPR2024-00496

4.5.3.1.3 DRP to Sink Behavior

Figure 4-21 illustrates the functional model for a DRP connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-21 DRP to Sink Functional Model



The following describes the behavior when a DRP is connected to a Sink.

1. DRP and Sink in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to AttachWait.SRC to Attached.SRC
   - DRP in Unattached.SRC detects one of the CC pull-downs of Sink which is in Unattached.SNK and DRP enters AttachWait.SRC
   - DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN
3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if required.
   - Sink detects VBUS and enters Attached.SNK
4. While the DRP and Sink are in their respective attached states:
   - DRP (as Source) adjusts Rp as needed to limit the current the Sink may draw
   - Sink detects and monitors vRd for available current on VBUS
   - DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

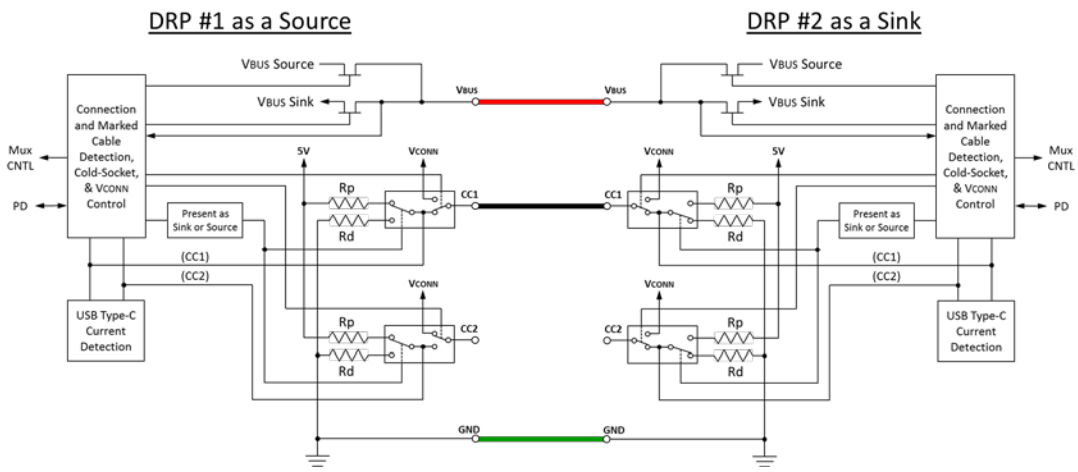
4.5.3.1.4 DRP to DRP Behavior

Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-22 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-22 DRP to DRP Functional Model – CASE 1



CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly.

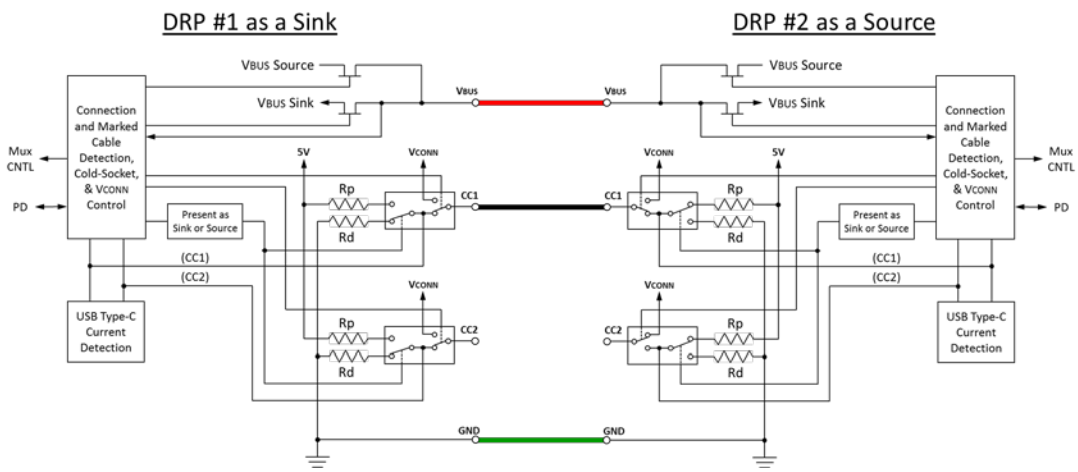
1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Attached.SRC
   - DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
5. DRP #2 transitions from AttachWait.SNK to Attached.SNK.
   - DRP #2 after having been in AttachWait.SNK for tCCDebounce and having detected VBUS, enters Attached.SNK
6. While the DRPs are in their respective attached states:
   - DRP #1 (as Source) adjusts Rp as needed to limit the current DRP #2 (as Sink) may draw
   - DRP #2 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #1 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- DRP #2 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Figure 4-23 illustrates the functional model for a DRP connected to a DRP in the second case described.

Figure 4-23 DRP to DRP Functional Model – CASE 2 & 3



CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Attached.SRC
   - DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
5. DRP #2 transitions from AttachWait.SNK to Try.SRC.
   - DRP #2 in AttachWait.SNK has been in this state for tCCDebounce and detects VBUS but strongly prefers the Source role, so transitions to Try.SRC
   - DRP #2 in Try.SRC asserts a pull-up on CC and waits
6. DRP #1 transitions from Attached.SRC to Unattached.SNK to AttachWait.SNK
   - DRP #1 in Attached.SRC no longer detects DRP #2's pull-down on CC and transitions to Unattached.SNK.
   - DRP #1 in Unattached.SNK turns off VBUS and VCONN and applies a pull-down on CC

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 159
Microchip v. Aptiv
IPR2024-00496

- DRP #1 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK

7. DRP #2 transitions from Try.SRC to Attached.SRC via AttachWait.SRC
   - DRP #2 in Try.SRC detects the DRP #1 in Unattached.SNK's pull-down on CC and enters AttachWait.SRC
   - DRP #2 in Attached.SRC turns on VBUS and VCONN
8. DRP #1 transitions from AttachWait.SNK to Attached.SNK
   - DRP #1 in AttachWait.SNK after tCCDebounce and detecting VBUS, enters Attached.SNK
9. While the DRPs are in their respective attached states:
   - DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw
   - DRP #1 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SRC (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

CASE 3: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #1 chooses to drive the random result to the opposite result using the Try.SNK mechanism.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Try.SNK
   - DRP #1 in AttachWait.SRC has been in this state for tCCDebounce and detects DRP #2's pull-down on CC but strongly prefers the Sink role, so transitions to Try.SNK
   - DRP #1 in Try.SNK asserts a pull down on CC and waits
5. DRP #2 transitions from AttachWait.SNK to Unattached.SRC to AttachWait.SRC.
   - DRP #2 in AttachWait.SNK no longer detects DRP #1's pull up on CC and transitions to Unattached.SRC
   - DRP #2 in Unattached.SRC applies a pull up on CC
   - DRP #2 in Unattached.SRC detects a pull down on a CC pin and enters AttachWait.SRC
   - DRP #1 detects DRP #2's pull up on CC and remains in Try.SNK
6. DRP #2 transitions from AttachWait.SRC to Attached.SRC

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

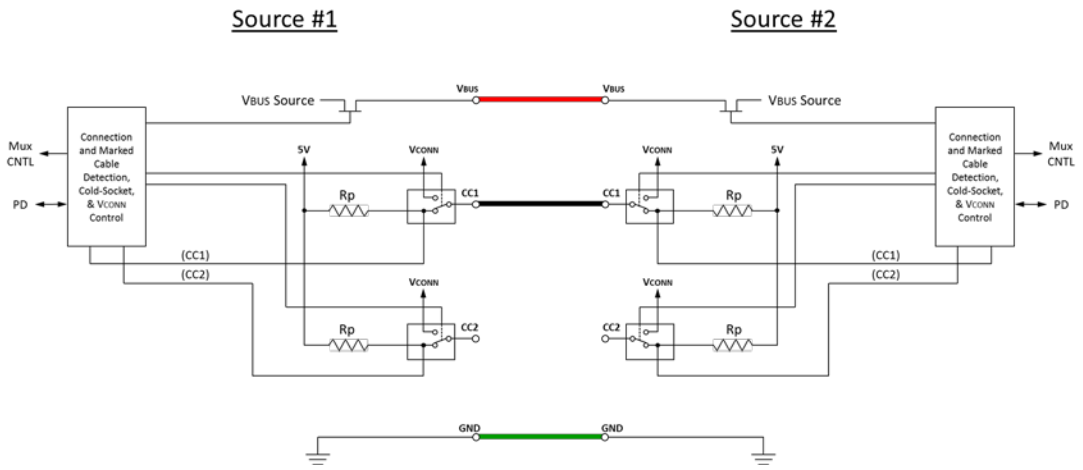
- DRP #2 in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC
- DRP #2 in Attached.SRC turns on VBUS and VCONN

7. DRP #1 transitions from Try.SNK to Attached.SNK
   - DRP #1 in Try.SNK after detecting VBUS, enters Attached.SNK
8. While the DRPs are in their respective attached states:
   - DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw
   - DRP #1 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SRC (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.5.3.1.5 Source to Source Behavior

Figure 4-24 illustrates the functional model for a Source connected to a Source. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-24 Source to Source Functional Model



The following describes the behavior when a Source is connected to another Source.

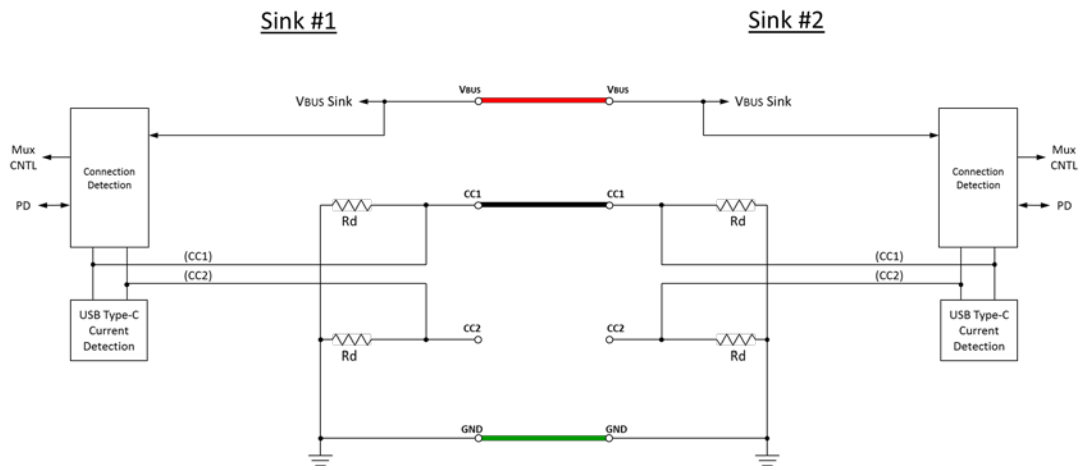
1. Both Sources in the unattached state
   - Source #1 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC
   - Source #2 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 161
Microchip v. Aptiv
IPR2024-00496

4.5.3.1.6 Sink to Sink Behavior

Figure 4-25 illustrates the functional model for a Sink connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-25 Sink to Sink Functional Model



The following describes the behavior when a Sink is connected to another Sink.

1. Both Sinks in the unattached state
   - Sink #1 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK
   - Sink #2 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK

4.5.3.2 USB Type-C port to Legacy Port Interoperability Behaviors

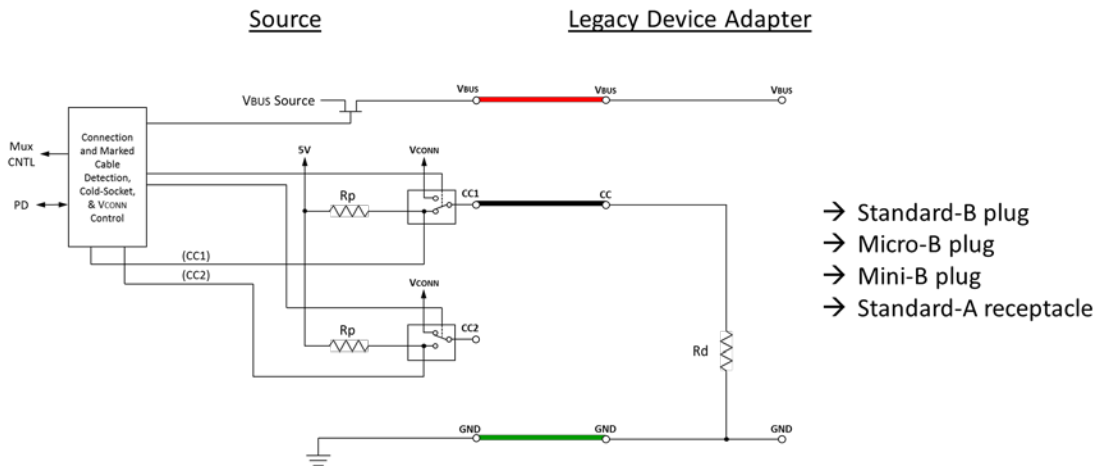
The following sub-sections describe port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs and legacy USB ports.

4.5.3.2.1 Source to Legacy Device Port Behavior

Figure 4-26 illustrates the functional model for a Source connected to a legacy device port. This model is based on having an adapter present as a Sink to the Source. This adapter has a USB Type-C plug on one end plugged into the Source and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-26 Source to Legacy Device Port Functional Model



The following describes the behavior when a Source is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.

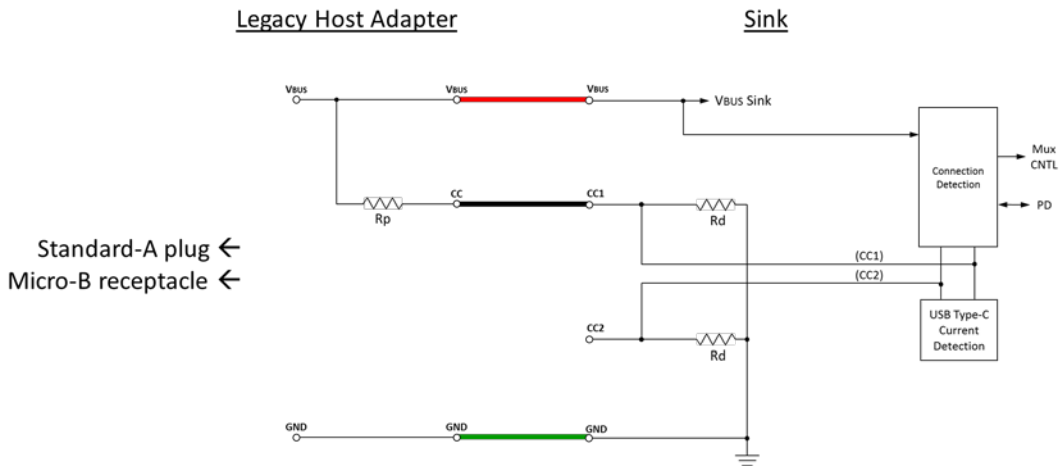
1. Source in the unattached state
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the Sink's pull-down on CC and enters AttachWait.SRC. After tCCDebounce, it enters Attached.SRC.
   - Source turns on VBUS and VCONN
3. While the Source is in the attached state:
   - Source monitors CC for detach and when detected, enters Unattached.SRC

4.5.3.2.2 Legacy Host Port to Sink Behavior

Figure 4-27 illustrates the functional model for a legacy host port connected to a Sink. This model is based on having an adapter that presents itself as a Source to the Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a Sink.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-27 Legacy Host Port to Sink Functional Model



The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source that is connected to a Sink. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-15), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via *USB BC 1.2* or by proprietary means.

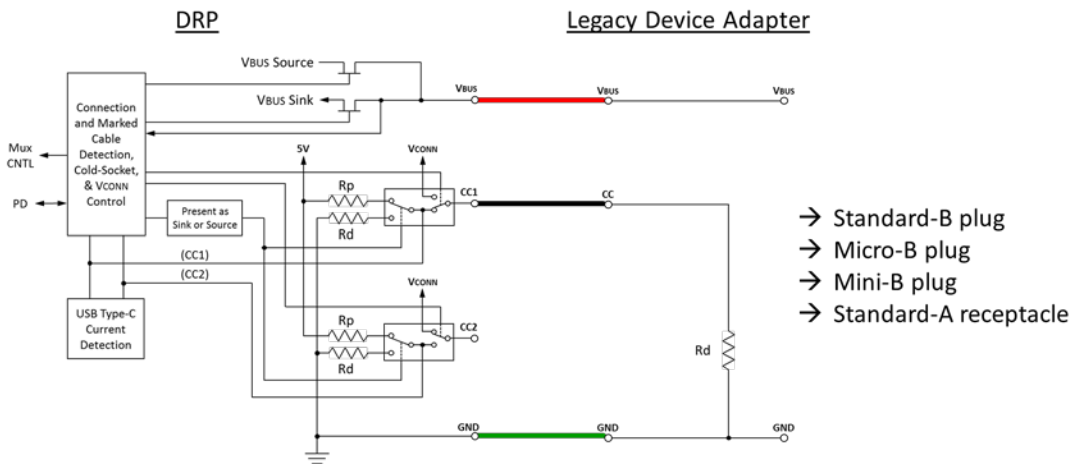
1. Sink in the unattached state
2. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if needed.
   - While in Unattached.SNK, if device is not USB 2.0 only, supports accessories or requires more than default power, it enters AttachWait.SNK when it detects a pull up on CC and ignores VBUS. Otherwise, it may enter Attached.SNK directly when VBUS is detected.
   - Sink detects VBUS and enters Attached.SNK
3. While the Sink is in the attached state:
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.3.2.3 DRP to Legacy Device Port Behavior

Figure 4-28 illustrates the functional model for a DRP connected to a legacy device port. This model is based on having an adapter present as a Sink (Device) to the DRP. This adapter has a USB Type-C plug on one end plugged into a DRP and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Figure 4-28 DRP to Legacy Device Port Functional Model



The following describes the behavior when a DRP is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.

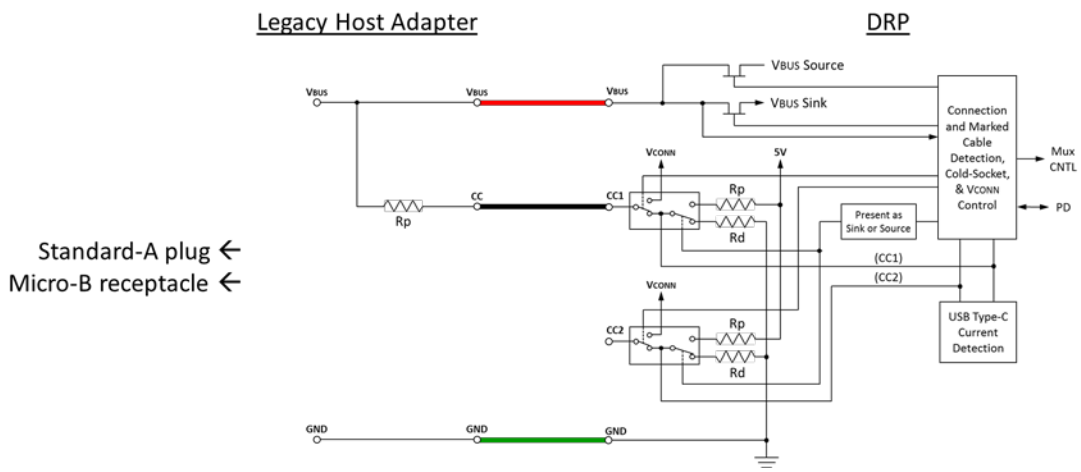
1. DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to Attached.SRC
   - DRP in Unattached.SRC detects the adapter's pull-down on CC and enters AttachWait.SRC
   - DRP in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC
   - DRP in Attached.SRC turns on VBUS and VCONN
   - DRP in AttachWait.SRC may support Try.SNK and if so, may transition through Try.SNK and TryWait.SRC prior to entering Attached.SRC
3. While the DRP is in the attached state:
   - DRP monitors CC for detach and when detected, enters Unattached.SRC (and resumes toggling between Unattached.SNK and Unattached.SRC)

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.5.3.2.4 Legacy Host Port to DRP Behavior

Figure 4-29 illustrates the functional model for a legacy host port connected to a DRP operating as a Sink. This model is based on having an adapter that presents itself as a Source (Host) to the DRP operating as a Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a DRP.

Figure 4-29 Legacy Host Port to DRP Functional Model



The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source is connected to a DRP. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-15), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via *USB BC 1.2* or by proprietary means.

1. DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SNK to AttachWait.SNK to Attached.SNK
   - DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK.
   - DRP in AttachWait.SNK detects VBUS and enters Attached.SNK
   - DRP in AttachWait.SNK may support Try.SRC and if so, may transition through Try.SRC and TryWait.SNK prior to entering Attached.SNK
3. While the DRP is in the attached state:
   - DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.6 Power

Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by: the *USB 2.0* and *USB 3.1* specifications, the *USB BC 1.2* specification and the *USB Power Delivery* specification. The USB Type-C Current mechanism allows the Source to offer more current than defined by the *USB BC 1.2* specification. A USB power source shall not provide more than 20 V nominal on VBUS. *USB PD* power sources that deliver power over a USB Type-C connector shall follow the power rules as defined in Section 10 of the *USB Power Delivery* specification.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

All USB Type-C-based devices shall support USB Type-C Current and may support other USB-defined methods for power. The following order of precedence of power negotiation shall be followed: *USB BC 1.2* supersedes the *USB 2.0* and *USB 3.1* specifications, USB Type-C Current at 1.5 A and 3.0 A supersedes *USB BC 1.2*, and *USB Power Delivery* supersedes USB Type-C Current. Table 4-14 summarizes this order of precedence of power source usage.

Table 4-14 Precedence of power source usage

Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	*USB PD*		Configurable	5 A
	USB Type-C Current @ 3.0 A		5 V	3.0 A
↓	USB Type-C Current @ 1.5 A		5 V	1.5 A
	USB BC 1.2		5 V	Up to 1.5 A[1]
	Default USB Power	*USB 3.1*	5 V	See USB 3.1
Lowest		*USB 2.0*	5 V	See USB 2.0

Notes:

1. *USB BC 1.2* permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A. If the *USB BC 1.2* power provider does not support 1.5 A, then it is required to follow power droop requirements. A *USB BC 1.2* power consumer may consume up to 1.5 A provided that the voltage does not drop below 2 V, which may occur at any level of power above 0.5 A.

For example, once the PD mode (e.g. a power contract has been negotiated) has been entered, the device shall abide by that power contract ignoring any other previously made or offered by the USB Type-C Current, *USB BC 1.2* or *USB 2.0* and *USB 3.1* specifications. When the PD mode is exited, the device shall fallback in order to the USB Type-C Current, *USB BC 1.2* or *USB 2.0* and *USB 3.1* specification power levels.

All USB Type-C ports shall tolerate being connected to USB power source supplying default USB power, e.g. a host being connected to a legacy USB charger that always supplies VBUS.

4.6.1 Power Requirements during USB Suspend

USB Type-C implementations with USB Type-C Current, *USB PD* and VCONN, along with active cables, requires the need to expand the traditional USB suspend definition.

4.6.1.1 VBUS Requirements during USB Suspend

The *USB 2.0* and *USB 3.1* specifications define the amount of current a Sink is allowed to consume during suspend.

USB suspend power rules shall apply when the USB Type-C Current is at the Default USB Power level or when *USB PD* is being used and the Suspend bit is set appropriately.

When USB Type-C Current is set at 1.5 A or 3.0 A, the Sink is allowed to continue to draw current from VBUS during USB suspend. During USB suspend, the Sink's requirement to track and meet the USB Type-C Current advertisement remains in force (See Section 4.5.2.3).

USB PD provides a method for the Source to communicate to the Sink whether or not the Sink has to follow the USB power rules for suspend.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.6.1.2 VCONN Requirements during USB Suspend

If the Source supplies VBUS power during USB suspend, it shall also supply at least 7.5 mA to VCONN.

Electronically marked cables shall draw no more than 7.5 mA from VCONN during USB suspend.

4.6.2 VBUS Power Provided Over a USB Type-C Cable

The minimum requirement for VBUS power supplied over the USB Type-C cable assembly matches the existing requirement for VBUS supplied over existing legacy USB cable assemblies. *USB Power Delivery* is an optional capability that is intended to work over un-modified USB Type-C to USB Type-C cables, therefore any USB Type-C cable assembly that incorporates electrical components or electronics shall ensure that it tolerate, or be protected from, a VBUS voltage of 21 V.

4.6.2.1 USB Type-C Current

Default USB voltage and current are defined by the *USB 2.0* and *USB 3.1* specifications. All USB Type-C Current advertisements are at the USB VBUS voltage defined by these specifications.

The USB Type-C Current feature provides the following extensions:

- Higher current than defined by the *USB 2.0*, the *USB 3.1* or the *BC 1.2* specifications
- Allows the power source to manage the current it provides

The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it can supply:

- Default values defined by the USB Specification
  (500 mA for USB 2.0 ports, 900 mA for USB 3.1 ports)
- 1.5 A
- 3.0 A

A Sink that takes advantage of the additional current offered (e.g., 1.5 A or 3.0 A) shall monitor the CC pins and shall adjust its current consumption within tSinkAdj to remain within the value advertised by the Source. While a *USB PD* contract is in place, a Sink is not required to monitor USB Type-C current advertisements and shall not respond to USB Type-C current advertisements.

The Source shall supply VBUS to the Sink within tVBUSON. VBUS shall be in the specified voltage range at the advertised current.

A Source (port supplying VBUS) shall protect itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement.

The Source adjusts Rp (or current source) to advertise which of the three current levels it supports. See Table 4-15 for the termination requirements for the Source to advertise currents.

The value of Rp establishes a voltage (vRd) on CC that is used by the Sink to determine the maximum current it may draw.

Table 4-26 defines the CC voltage range observed by the Sink that only support default USB current.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

If the Sink wants to consume more than the default USB current, it shall track vRd to determine the maximum current it may draw. See Table 4-27.

Figure 4-30 and Figure 4-31 illustrate where the Sink monitors CC for vRd to detect if the host advertises more than the default USB current.

Figure 4-30 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model

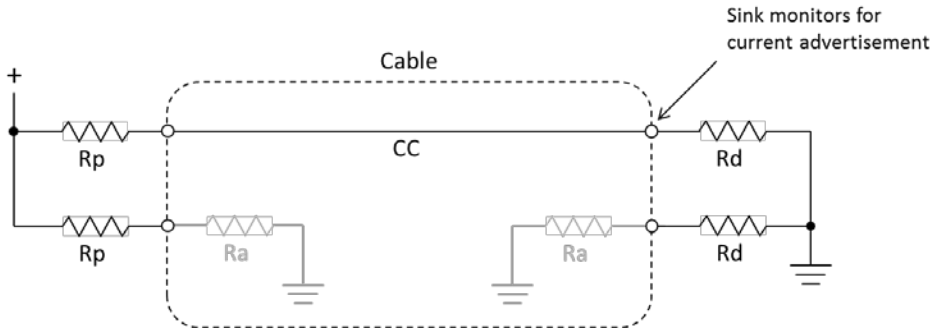
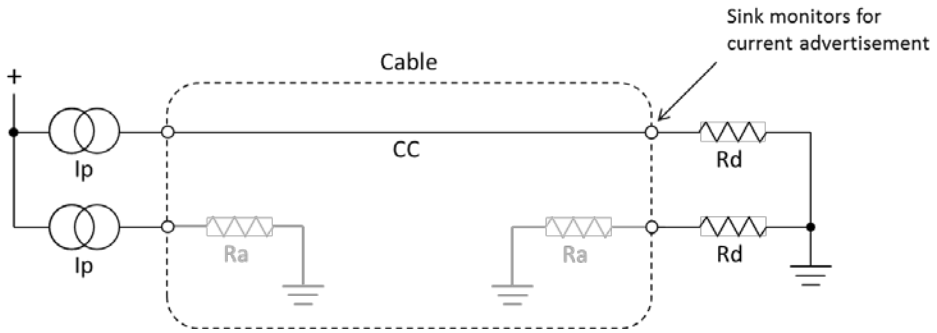


Figure 4-31 Sink Monitoring for Current in Current Source/Pull-Down CC Model



4.6.2.2 USB Battery Charging 1.2

USB Battery Charging Specification, Revision 1.2 defines a method that uses the USB 2.0 D+ and D− pins to advertise VBUS can supply up to 1.5 A. Support for *USB BC 1.2* charging is optional.

USB Type-C-based *BC 1.2* chargers that are capable of supplying at least 1.5 A shall advertise USB Type-C Current at the 1.5 A level, otherwise the charger shall advertise USB Type-C Current at the Default USB Power level. A USB Type-C-based *BC 1.2* charger that also supports USB Type-C Current at 3.0 A may advertise USB Type-C Current at 3.0 A.

4.6.2.3 Proprietary Power Source

A proprietary power source (i.e., battery charger) with a USB Type-C-captive cable or a USB Type-C receptacle that is capable of supplying at least 1.5 A and less than 3.0 A shall advertise USB Type-C Current at least at the 1.5 A level.

A proprietary power source with a USB Type-C-captive cable or a USB Type-C receptacle that is capable of supplying at least 3.0 A shall advertise USB Type-C Current at least at the 3.0 A level.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.6.2.4 USB Power Delivery

USB Power Delivery is a feature on the USB Type-C connector. When *USB PD* is implemented, *USB PD* Bi-phase Mark Coded (BMC) carried on the CC wire shall be used for *USB PD* communications between USB Type-C ports.

At attach, VBUS shall be operationally stable prior to initiating *USB PD* communications.

Figure 4-32 illustrates how the *USB PD* BMC signaling is carried over the USB Type-C cable's CC wire.

Figure 4-32 USB PD over CC Pins

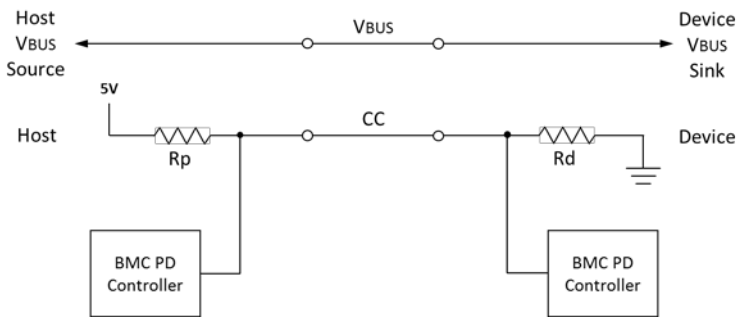
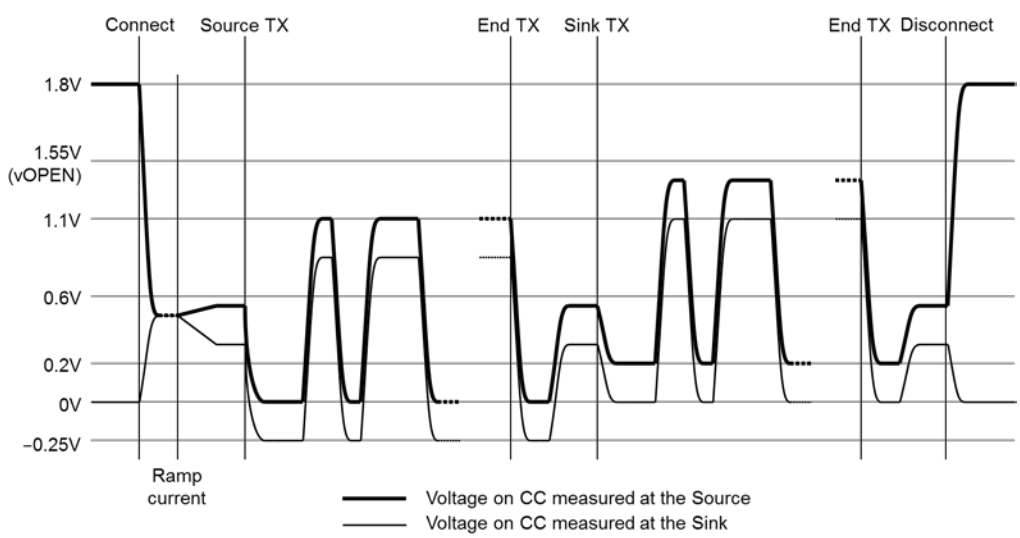


Figure 4-33 illustrates *USB PD* BMC signaling as seen on CC from both the perspective of the Source and Sink. The breaks in the signaling are intended to represent the passage of time.

Figure 4-33 USB PD BMC Signaling over CC



While an *USB PD* Explicit Contract is in place, the Source shall advertise a USB Type-C Current of either 1.5 A or 3.0 A. The Source upon entry into an Explicit Contract shall advertise an Rp value of 1.5 A or 3.0 A after it receives the GoodCRC in response to the first PS_RDY Message and before it sends any other messages. Refer to Section 1.6 of the *USB Power Delivery* specification for a definition of an Explicit Contract.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 170
Microchip v. Aptiv
IPR2024-00496

4.7 USB Hubs

USB hubs are defined by the *USB 2.0* and *USB 3.1* specifications. USB hubs implemented with one or more USB Type-C connectors shall comply with the *USB 3.1 Specification*.

USB hubs shall have an upstream facing port (to connect to a host or hub higher in the USB tree) that may be a Sourcing Device (See Section 4.8.4). The hub shall clearly identify to the user its upstream facing port. This may be accomplished by physical isolation, labeling or a combination of both.

USB hub's downstream facing ports shall not have Dual-Role-Data (DRD) capabilities. However, these ports may have Dual-Role-Power (DRP) capabilities.

CC pins are used for port-to-port connections and shall be supported on all USB Type-C connections on the hub.

USB hub ports shall not implement or pass-through Alternate or Accessory Modes. SBU pins shall not be connected (zSBUTermination) on any USB hub port.

The USB hub's DFPs shall support power source requirements for a Source. See Section 4.8.1.

4.8 Chargers

4.8.1 DFP as a Power Source

Sources (e.g. battery chargers, hub downstream ports and hosts) may all be used for battery charging. When a charger is implemented with a USB Type-C receptacle or a USB Type-C captive cable, it shall follow all the applicable requirements.

- A Source shall expose its power capabilities using the USB Type-C Current method and it may additionally support other USB-standard methods (*USB BC 1.2* or *USB-PD*).
- A Source may also expose its identity and/or power capabilities using a proprietary (e.g. non-USB-standard) method. A proprietary method may source up to 5 A if it has a captive cable capable of carrying that level of current. See Section 4.6.2.3 for additional requirements.
- A Source advertising its current capability using *USB BC 1.2* shall meet the requirements in Section 4.6.2.2 regarding USB Type-C Current advertisement.
- A Source that has negotiated a *USB-PD* contract shall meet the requirements in Section 4.6.2.4 regarding USB Type-C Current advertisement.
- If a Source is capable of supplying a voltage greater than default VBUS, it shall fully conform to the *USB-PD* specification, and shall negotiate its power contracts using only *USB-PD*.
- If a Source is capable of reversing source and sink power roles, it shall fully conform to the *USB-PD* specification, and shall negotiate its power contracts using only *USB-PD*.
- If a Source is capable of supplying a current greater than 3.0 A, it shall use the *USB-PD* Discover Identity to determine the current carrying capacity of the cable.

4.8.1.1 USB-based Chargers with USB Type-C Receptacles

- A USB-based charger with a USB Type-C receptacle (Source) shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).

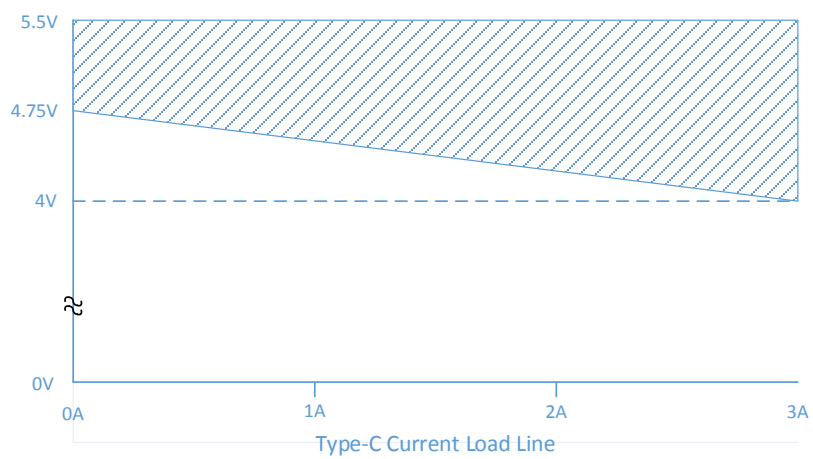
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- A USB-based charger with a USB Type-C receptacle shall not advertise current exceeding 3.0 A except when it uses the *USB-PD* Discover Identity mechanism to determine the cable's actual current carrying capability and then it shall limit the advertised current accordingly.

4.8.1.2 USB-based Chargers with USB Type-C Captive Cables

- A USB-based charger with a USB Type-C captive cable that supports USB PD shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).
- A USB-based charger with a USB Type-C captive cable that does not support USB PD may supply VBUS at any time. It is recommended that such a charger only apply power to VBUS when it detects a Sink is present and remove power from VBUS when it detects the Sink is not present (vOPEN).
- A USB-based charger with a USB Type-C captive cable shall limit its current advertisement so as not to exceed the current capability of the cable (up to 5 A).
- The voltage as measured at the plug of a USB-based charger with a USB Type-C captive cable may be up to 0.75 × I / 3 V (0 < I ≤ 3 A), or 0.75 × I / 5 V (0 < I ≤ 5 A) lower than the standard tolerance range for the chosen voltage, where I is the actual current being drawn.
    - A USB-based charger that advertises USB Type-C Current shall output a voltage in the range of 4.75 V – 5.5 V when no current is being drawn and between 4.0 V – 5.5 V at 3 A. The output voltage as a function of load up to the advertised USB Type-C Current (default, 1.5 A and 3 A) shall remain within the cross-hatched area shown in Figure 4-34.

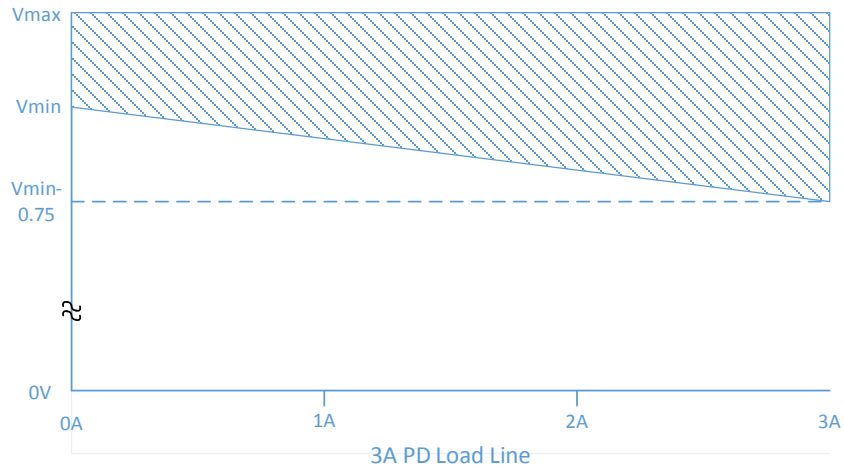
Figure 4-34 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging



    - A USB PD-based charger that has negotiated a voltage V at ≤ 3 A shall output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 3 A. Under all loads, the output voltage shall remain within the cross-hatched area shown in Figure 4-35.

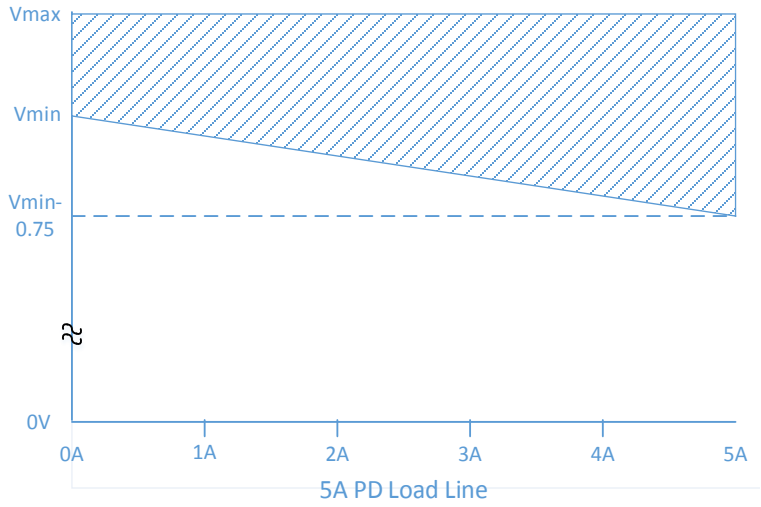
Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-35 0 – 3 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load



- A USB PD-based charger that has negotiated a voltage V at between 3 A and 5 A shall output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 5 A. Under all loads, the output voltage shall remain within the cross hatched area shown in Figure 4-36.

Figure 4-36 3 – 5 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load



- Note: The maximum allowable cable IR drop for ground is 250 mV (see Section 4.4.1). This is to ensure the signal integrity of the CC wire when used for connection detection and *USB PD* BMC signaling.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.8.2 Non-USB Charging Methods

A charger with a USB Type-C connector may employ additional proprietary charging methods to source power beyond what is allowed by the USB defined methods. When implemented, proprietary methods must meet the following requirements:

- The method shall only be used to establish identity and/or a current level at default VBUS voltage in a manner not defined by the USB methods
- The method shall only define the current level and shall not change the voltage delivered on VBUS
- The method shall not alter the Source's role to supply VBUS or the Sink's role to consume VBUS
- See Section 4.6.2.3 for additional requirements regarding USB Type-C Current advertisement.

A product with a USB Type-C connector that consumes power may support proprietary charging methods, these products shall not support methods that redefine VBUS voltage beyond what is defined by the *USB 2.0* and *USB 3.1* specifications.

4.8.3 Sinking Host

A Sinking Host is a special sub-class of a DRP that is capable of consuming power, but is not capable of acting as a USB device. For example a hub's DFP or a notebook's DFP that operates as a host but not as a device.

The Sinking Host shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). The Sinking DFP shall support *USB PD* and shall support the DR_Swap command in order to get the Sink into the UFP data role.

4.8.4 Sourcing Device

A Sourcing Device is a special sub-class of a DRP that is capable of supplying power, but is not capable of acting as a USB host. For example a hub's UFP or a monitor's UFP that operates as a device but not as a host.

The Sourcing Device shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). It shall also follow the requirements for the Source as Power Source (See Section 4.8.1). The Sourcing Device shall support *USB PD* and shall support the DR_Swap command in order to enable the Source to assume the UFP data role.

4.8.5 Charging a System with a Dead Battery

A system that supports being charged by USB whose battery is dead shall apply Rd to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS. It may use any allowed method to increase the amount of power it can use to charge its battery.

Circuitry to present Rd in a dead battery case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of Rd in order for a Source to recognize the Sink and provide VBUS. For example, a 20% resistor of value Rd in series with a FET with VGTH(max) < VCLAMP(max) with the gate weakly pulled to CC would guarantee detection and be removable upon power up.

When the system with a dead battery has sufficient charge, it may use the *USB PD* DR_Swap message to become the DFP.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.9 Electronically Marked Cables

All USB Full-Featured Type-C cables shall be electronically marked. USB 2.0 Type-C cables may be electronically marked.

Electronically marked cables shall support *USB Power Delivery* Structured VDM Discover Identity command directed to SOP'. This provides a method to determine the characteristics of the cable, e.g. its current carrying capability, its performance, vendor identification, etc. This may be referred to as the USB Type-C Cable ID function.

Prior to an explicit *USB PD* contract, a Sourcing Device is allowed to use SOP' to discover the cable's identity. After an explicit *USB PD* contract has been negotiated, only the Source shall communicate with SOP' and SOP" (see Section 5.2.2).

An electronically marked cable incorporates electronics that require VCONN, although VBUS or another source may be used. Electronically marked cables that do not incorporate data bus signal conditioning circuits shall consume no more than 70 mW from VCONN. During USB suspend, electronically marked cables shall not draw more than 7.5 mA from VCONN, see Section 4.6.1.2.

Figure 4-37 illustrates a typical electronically marked cable. The isolation elements (Iso) shall prevent VCONN from traversing end-to-end through the cable. Ra is required in the cable to allow the Source to determine that VCONN is needed.

Figure 4-37 Electronically Marked Cable with VCONN connected through the cable

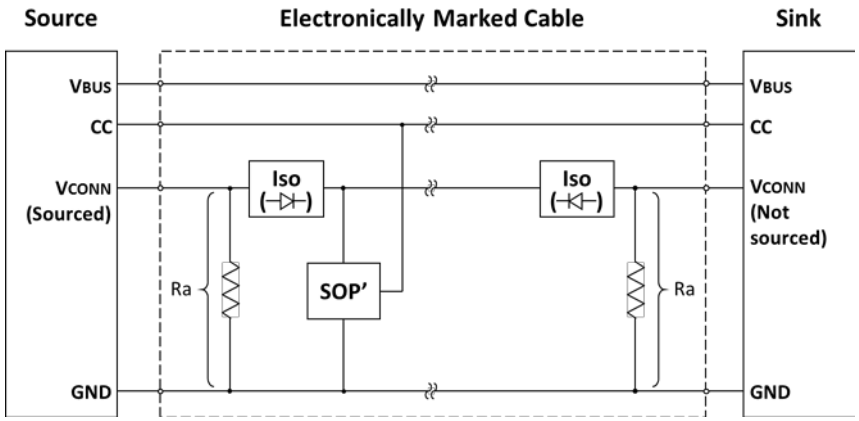
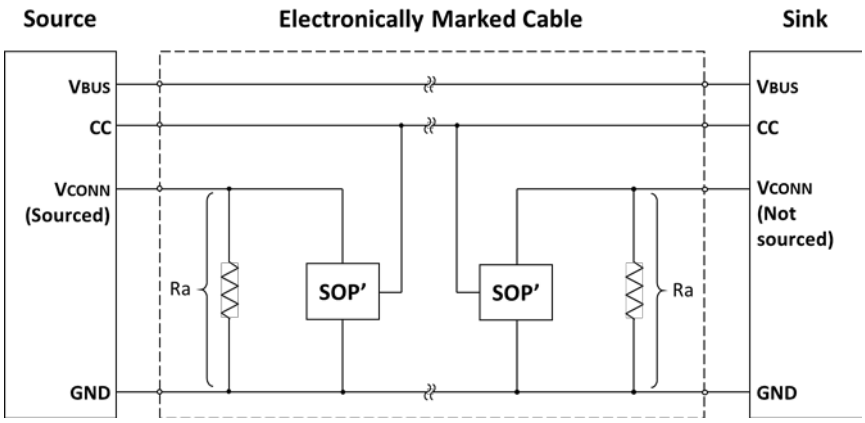


Figure 4-38 illustrates an electronically marked cable where the VCONN wire does not extend through the cable, therefore an SOP' element is required at each end of the cable. In this case, no isolation elements are needed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-38 Electronically Marked Cable with SOP' at both ends



For cables that only respond to SOP', the location of the responder is not relevant.

An active cable is an electronically marked cable that incorporates data bus signal conditioning circuits, for example to allow for implementing longer cables. Active cables shall not draw more than 1 W from VCONN, see Section 4.4.3.

Active cables may or may not require configuration management. Requirements for active cables that require configuration management are provided in Section 5.2.

Refer to Section 4.4.3 for the requirements of a Source to supply VCONN. When VCONN is not present, a powered cable shall not interfere with normal CC operation including Sink detection, current advertisement and *USB PD* operation.

4.10 VCONN-Powered Accessories

A VCONN-powered accessory is a direct-attach Sink that implements an Alternate Mode (See Section 5.1) and can operate with just VCONN.

The VCONN-powered accessory exposes a maximum impedance to ground of Ra on the VCONN pin and Rd on the CC pin.

When operating in the UFP role and when VBUS is not present, VCONN-powered accessories shall treat the application of VCONN as an attach signal, and shall respond to *USB Power Delivery* messages.

When powered by only VCONN, a VCONN-powered accessory shall negotiate an Alternate Mode. If it fails to negotiate an Alternate Mode within tAMETimeout, its port partner removes VCONN.

VCONN-powered accessories shall be able to operate over a range of 2.7 V to 5.5 V on VCONN.

The removal of VCONN when VBUS is not present shall be treated as a detach event.

When VBUS is supplied, a VCONN-powered accessory is subject to all of the requirements for Alternate Modes, including presenting a *USB Billboard Device Class* interface if negotiation for an Alternate Mode fails.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 176
Microchip v. Aptiv
IPR2024-00496

4.11 Parameter Values

4.11.1 Termination Parameters

Table 4-15 provides the values that shall be used for the Source's Rp or current source. Other pull-up voltages shall be allowed if they remain less than 5.5 V and fall within the correct voltage ranges on the Sink side – see Table 4-23, Table 4-24 and Table 4-25. Note: when two Sources are connected together, they may use different termination methods which could result in unexpected current flow.

Table 4-15 Source CC Termination (Rp) Requirements

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

Notes:

1. For Rp when implemented in the USB Type-C plug on a USB Type-C to *USB 3.1* Standard-A Cable Assembly, a USB Type-C to *USB 2.0* Standard-A Cable Assembly, a USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly or a USB Type-C captive cable connected to a USB host, a value of 56 kΩ ± 5% shall be used, in order to provide tolerance to IR drop on VBUS and GND in the cable assembly.

The Sink may find it convenient to implement Rd in multiple ways simultaneously (a wide range Rd when unpowered and a trimmed Rd when powered). Transitions between Rd implementations that do not exceed tCCDebounce shall not be interpreted as exceeding the wider Rd range. Table 4-16 provides the methods and values that shall be used for the Sink's Rd implementation.

Table 4-16 Sink CC Termination (Rd) Requirements

Rd Implementation	Nominal value	Can detect power capability?	Max voltage on pin
± 20% voltage clamp[1]	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V

Note:

1. The clamp implementation inhibits *USB PD* communication although the system can start with the clamp and transition to the resistor once it is able to do *USB PD*.

Table 4-17 provides the impedance value to ground on VCONN in powered cables.

Table 4-17 Powered Cable Termination Requirements

	Minimum Impedance	Maximum Impedance
Ra	800 Ω[1]	1.2 kΩ

Note:

1. The minimum impedance may be less when powering active circuitry.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 4-18 provides the minimum impedance value to ground on CC for a self-powered device (Sink) or a device that supports the Disabled state or ErrorRecovery state to be undetected by a Source.

Table 4-18 Sink CC Termination Requirements

	Minimum Impedance to GND
zOPEN	126 kΩ

Table 4-19 provides the impedance value for an SBU to appear open.

Table 4-19 SBU Termination Requirements

	Termination	Notes
zSBUTermination	≥ 950 kΩ	Functional equivalent to an open circuit

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4.11.2 Timing Parameters

Table 4-20 provides the timing values that shall be met for delivering power over VBUS and VCONN.

Table 4-20 VBUS and VCONN Timing Parameters

	Minimum	Maximum	Description
tVBUSON	0 ms	275 ms	From entry to Attached.SRC until VBUS reaches the minimum vSafe5V threshold as measured at the source's receptacle.
tVBUSOFF	0 ms	650 ms	From the time the Sink is detached until the Source removes VBUS and reaches vSafe0V (See *USB PD*).
tVCONNON	Note 1	2 ms	From the time the Source supplied VBUS in the Attached.SRC state. Measured from vSafe5V to the minimum VCONN voltage (see Table 4-4)
tVCONNON-PA	0 ms	100 ms	From the time a Sink with accessory support enters the PoweredAccessory state until the Sink sources minimum VCONN voltage (see Table 4-4)
tVCONNOFF	0 ms	35 ms	From the time that a Sink is detached or as directed until the VCONN supply is disconnected and bulk capacitance is removed.
tSinkAdj	tPDDebounce	60 ms	Response time for a Sink to adjust its current consumption to be in the specified range due to a change in USB Type-C Current advertisement

Note:

1. VCONN may be applied prior to the application of VBUS

Figure 4-39 illustrates the timing parameters associated with the DRP toggling process. The tDRP parameter represents the overall period for a single cycle during which the port is exposed as both a Source and a Sink. The portion of the period where the DRP is exposed as a Source is established by dcSRC.DRP and the maximum transition time between the exposed states is dictated by tDRPTransition.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 4-39 DRP Timing

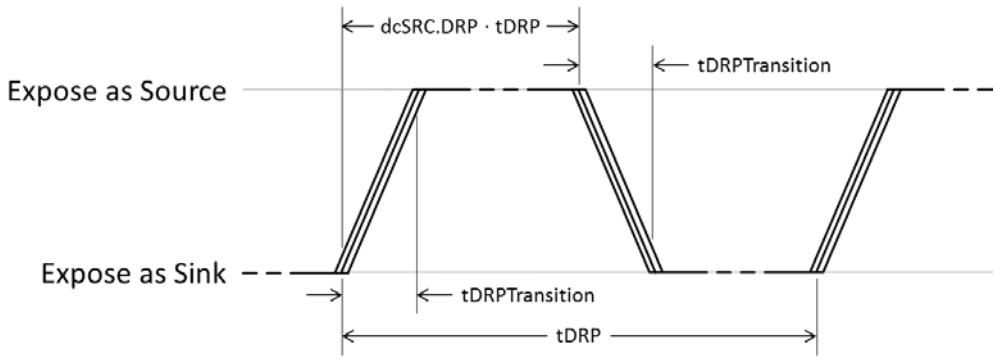


Table 4-21 provides the timing values that shall be met for DRPs. The clock used to control DRP swap should not be derived from a precision timing source such as a crystal, ceramic resonator, etc. to help minimize the probability of two DRP devices indefinitely failing to resolve into a Source-to-Sink relationship. Similarly, the percentage of time that a DRP spends advertising Source not be derived from a precision timing source.

Table 4-21 DRP Timing Parameters

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
dcSRC.DRP	30%	70%	The percent of time that a DRP shall advertise Source during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between Source and Sink roles during role resolution
tDRPTry	75 ms	150 ms	Wait time associated with the Try.SRC state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the Try.SNK state.

Table 4-22 provides the timing requirement for CC connection behaviors.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 4-22 CC Timing

	Minimum	Maximum	Description
tCCDebounce	100 ms	200 ms	Time a port shall wait before it can determine it is attached
tPDDebounce	10 ms	20 ms	Time a port shall wait before it can determine it is either detached or there has been a change in USB Type-C current due to the potential for *USB PD* BMC signaling on CC as described in the state definitions. The exit condition for the Attached.SRC state may not apply this timer.
tErrorRecovery	25 ms		Time a self-powered port shall remain in the ErrorRecovery state.

4.11.3 Voltage Parameters

Table 4-23, Table 4-24 and Table 4-25 provide the CC voltage values that a Source shall use to detect what is attached based on the USB Type-C Current advertisement (Default USB, 1.5 A @ 5 V, or 3.0 A @ 5 V) that the Source is offering.

Table 4-23 CC Voltages on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.15 V	0.20 V
Sink (vRd)	0.25 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 4-24 CC Voltages on Source Side – 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.35 V	0.40 V
Sink (vRd)	0.45 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 4-25 CC Voltages on Source Side – 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.75 V	0.80 V
Sink (vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V		

Table 4-26 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that does not support higher than default USB Type-C Current Source advertisements.

Table 4-26 Voltage on Sink CC Pins (Default USB Type-C Current only)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.18 V	

Table 4-27 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that implements detection of higher than default USB Type-C Current Source advertisements. This table includes consideration for the effect that the IR drop across the cable GND has on the voltage across the Sink's Rd.

Table 4-27 Voltage on Sink CC pins (Multiple Source Current Advertisements)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

5 Functional Extensions

5.1 Alternate Modes

All hosts and devices (except chargers) using a USB Type-C™ receptacle shall expose a USB interface. In the case where the host or device optionally supports Alternate Modes:

- The host and device shall use *USB Power Delivery* Structured Vendor Defined Messages (Structured VDMs) to discover, configure and enter/exit modes to enable Alternate Modes.
- The device is strongly encouraged to provide equivalent USB functionality where such exists for best user experience.
- Where no equivalent USB functionality is implemented, the device shall provide a USB interface exposing a *USB Billboard Device Class* used to provide information needed to identify the device. A device is not required to provide a USB interface exposing a *USB Billboard Device Class* for non-user facing modes (e.g., diagnostic modes).

As Alternate Modes do not traverse the USB hub topology, they shall only be used between a directly connected host and device.

5.1.1 Alternate Mode Architecture

The *USB Power Delivery* Structured VDMs are defined to extend the functionality a device exposes. Only Structured VDMs shall be used to alter the USB functionality or reconfigure the pins the USB Type-C Connector exposes. Structured VDMs provide a standard method to identify the modes a device supports and to command the device to enter and exit a mode. The use of Structured VDMs are in addition to the normal *USB PD* messages used to manage power. Structured VDMs may be interspersed within the normal *USB PD* messaging stream, however they shall not be inserted in the middle of an ongoing PD power negotiation.

The Structured VDMs consist of a request followed by a response. The response is either a successful completion of the request (ACK), an indication that the device needs time before it can service a request (BUSY), or a rejection of the request (NAK). A host and device do not enter a mode when either a NAK or BUSY is returned.

Multiple modes may exist and/or function concurrently. For example, a Structured VDM may be used to manage an active cable at the same time that another Structured VDM is used to manage the device so that both the cable and device are operating in a compatible mode.

5.1.2 Alternate Mode Requirements

The host and device shall negotiate a *USB PD* Explicit Contract before Structured VDMs may be used to discover or enter an Alternate Mode.

The ACK shall be sent after switching to the Alternate Mode has been completed by the UFP for Enter Mode and Exit Mode requests. See Section 6.4.4 in the *USB Power Delivery Specification*.

If a device fails to successfully enter an Alternate Mode within tAMETimeout then the device shall minimally expose a *USB 2.0* interface (*USB Billboard Device Class*) that is powered by V_{BUS}.

When a device offers multiple modes, especially where multiple Alternate Mode definitions are needed in order to be compatible with multiple host-side implementations, successfully entering an Alternate Mode may be predicated on only one of the available modes being successfully recognized by a host. In this case, the device is not required to expose but may

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

still expose a *USB Billboard Device Class* interface to indicate to the host the availability and status of the modes it supports.

The host may send an Enter Mode after tAMETimeout. If the device enters the mode, it shall respond with an ACK and discontinue exposing the *USB Billboard Device Class* interface. The device may expose the *USB Billboard Device Class* interface again with updated capabilities.

The current supplied over VCONN may be redefined by a specific Alternate Mode but the power shall not exceed the current rating of the pin (See Section 3.7.7.4).

5.1.2.1 Alternate Mode Pin Reassignment

Figure 5-1 illustrates the only pins that shall be available for functional reconfiguration in a full-featured cable. The pins highlighted in yellow are the only pins that shall be reconfigured.

Figure 5-1 Pins Available for Reconfiguration over the Full-Featured Cable

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure 5-2 illustrates the only pins that shall be available for functional reconfiguration in direct connect applications such as a cradle dock, captive cable or a detachable notebook. The pins highlighted in yellow are the only pins that shall be reconfigured. Three additional pins are available because this configuration is not limited by the cable wiring.

Figure 5-2 Pins Available for Reconfiguration for Direct Connect Applications

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The USB 2.0 data pins (A6, A7) shall remain connected to the USB host controller during entry, while in and during exit of an Alternate Mode.

5.1.2.2 Alternate Mode Electrical Requirements

Signaling during the use of Alternate Modes shall comply with all relevant cable assembly, adapter assembly and electrical requirements of Chapter 3.

Two requirements are specified in order to minimize risk of damage to the USB SuperSpeed transmitters and receivers in a USB host or device:

- When operating in an Alternate Mode and pin pairs A11, A10 (RX1) and B11, B10 (RX2) are used, these shall be AC coupled in or before the USB Type-C plug.
- When operating in an Alternate Mode and pin pairs A2, A3 (TX1) and B2, B3 (TX2) are used, the DC blocking capacitors in the system used on these pin pairs for USB SuperSpeed signaling shall also be used for Alt Mode signaling.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- Alternate Mode signals being received at the USB Type-C receptacle shall not exceed the value specified for VTX-DIFF-PP in Table 6-17 of the *USB 3.1* specification.

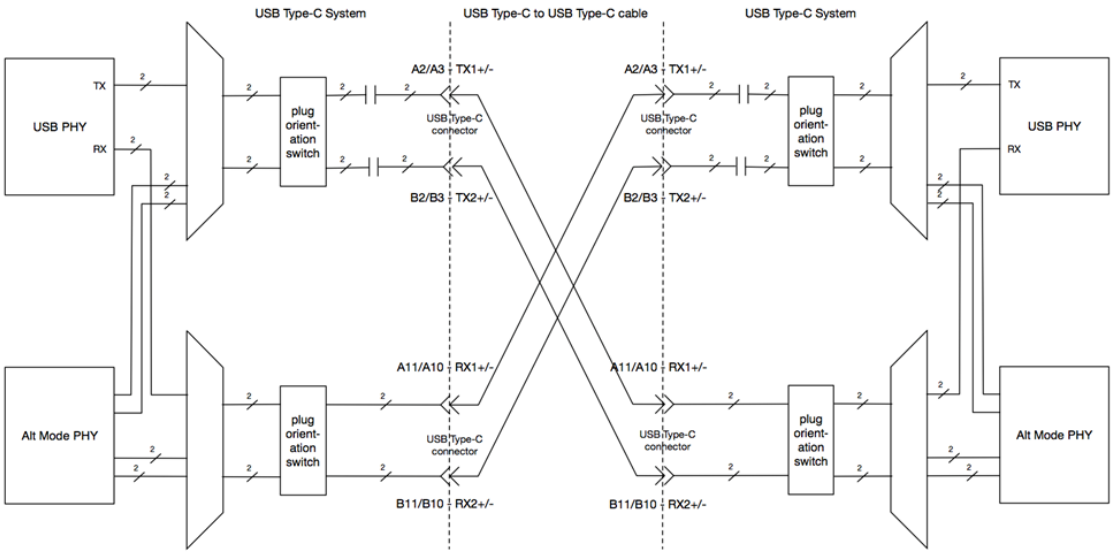
Direct connect applications shall ensure that any stubs introduced by repurposing the extra D+/D− pair do not interfere with USB communication with compliant hosts that short the pairs of pins together on the receptacle. This can be ensured by placing the Alternate Mode switch close to the plug, by adding inductors to eliminate the stubs at USB 2.0 frequencies, by AC-terminating the long stubs to remove reflections at the cost of attenuated signal, or by other means.

When in an Alternate Mode, activity on the SBU lines shall not interfere with *USB PD* BMC communications or interfere with detach detection.

The AC coupling requirement results from the use of AC coupling in the *USB 3.1* specification. This requires that the TX signals are AC coupled within the system before the physical connector, but that the RX signals are DC coupled within the system. There is thus just one DC blocking capacitor in each connection between the SuperSpeed transmitter PHY and the SuperSpeed receiver PHY.

Figure 5-3 shows the key components in a typical Alternate Mode implementation using a USB Type-C to USB Type-C full featured cable. This implementation meets the AC coupling requirements, as the capacitors required to be in or before the USB Type-C plug are implemented behind the TX pins in the port partner.

Figure 5-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable



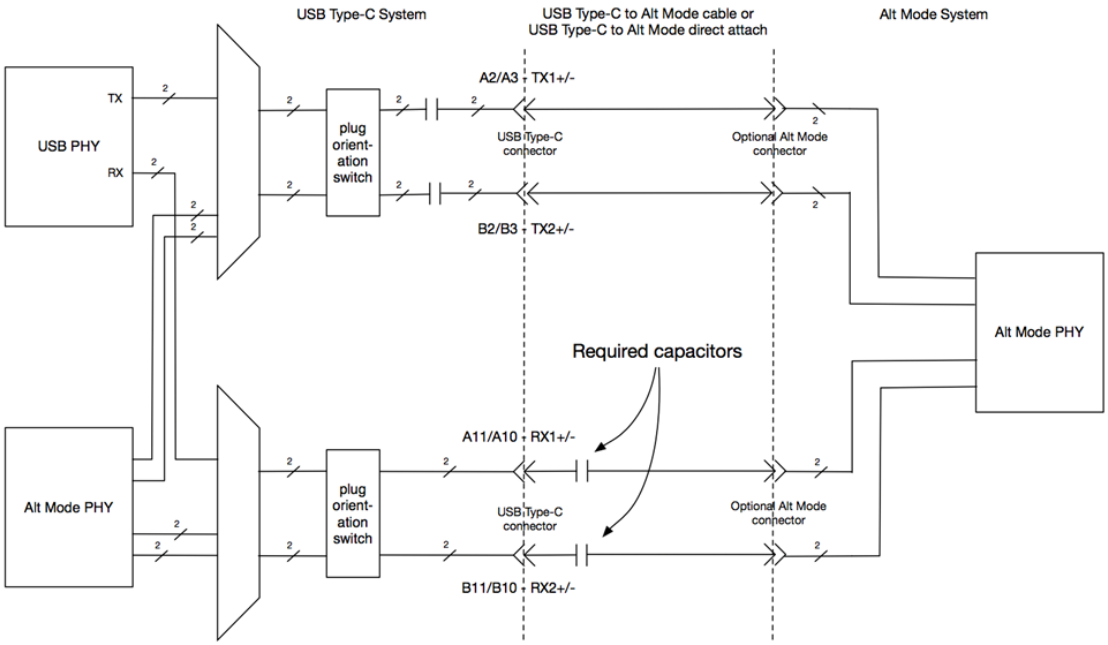
It should be noted that the AC capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the Alternate Mode selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the USB SuperSpeed operation, to both the transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC cap that is implemented on the TX path in the port partner.

Figure 5-4 shows the key components in a typical Alternate Mode implementation using either a USB Type-C to Alternate Mode connector cable, or a USB Type-C Alternate Mode

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Direct Attach device. In both cases it is necessary that the system path behind the RX pins on the USB receptacle be isolated from external common mode. This requirement is met by incorporating capacitors in or behind the USB Type-C plug on the Alternate Mode cable or Alternate Mode device.

Figure 5-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device



In the case where the Alt Mode System is required to implement DC blocking capacitors within the system between active system components and the Alt Mode connector, then this provides the necessary isolation and further capacitors in the USB Type-C to Alt Mode adapter cable are not necessary, and may indeed impair signal integrity.

The USB Safe State is defined by the *USB PD* specification. The USB Safe State defines an electrical state for the SBU1/2 and SSTX/SSRX for DFPs, UFPs, and Active Cables when transitioning between USB and an Alternate Mode. SBU1/2 and SSTX/SSRX must transition to the USB Safe State before entering to or exiting from an Alternate Mode. Table 5-1 defines the electrical requirements for the USB Safe State. See the *USB-PD* Specification for more detail on entry/exit mechanisms to the USB Safe State.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table 5-1 USB Safe State Electrical Requirements

	SBU1/2	SSTX[1,2]	SSRX[2]	B6/B7[4]
Common-mode voltage	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V
Impedance to ground[3]	< 4 MΩ	< 4 MΩ	25 KΩ – 4 MΩ	< 4 MΩ

Notes:

1. SSTX common-mode voltage is defined on the integrated circuit side of the AC coupling capacitors.
2. Unused SSTX and SSRX signals should transition to USB Safe State if wired to the connector but not used.
3. The DFP and UFP shall provide a discharge path to ground in USB Safe State when a connection to the USB Type-C receptacle is present.
4. Applies to docking solutions that redefine pins B6 and B7.

5.1.3 Parameter Values

Table 5-2 provides the timeout requirement for a device that supports Alternate Modes to enable a *USB Billboard Device Class* interface when none of the modes supported by the device are successfully recognized and configured by the DFP to which the device is attached.

Table 5-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure

	Maximum	Description
tAMETimeout	1000 ms	The time between a Sink attach until a *USB Billboard Device Class* interface is exposed when an Alternate Mode is not successfully entered

While operating in an Alternate Mode, the signaling shall not cause noise ingression onto USB signals operating concurrently that exceeds the Vnoise parameters given in Table 5-3.

Table 5-3 Alternate Mode Signal Noise Ingression Requirements

	Limit	Bandwidth
Vnoise on BMC during BMC Active	30 mV	100 ns time constant filter
Vnoise on BMC during BMC Idle	100 mV	100 ns time constant filter
Vnoise on D+/D− (Single-ended)	40 mV	500 MHz
Vnoise on D+/D− (Differential)	10 mV	500 MHz

Note: Each Vnoise parameter is the max noise ingression level allowed onto the respective interface that is due to two SBU aggressors from the Alternate Mode signaling, under respective worse case scenarios. The coupling between SBU_A/SBU_B and CC within a USB Type-C cable shall meet the requirement described in Section 3.7.2.3.4. The coupling between SBU_A/SBU_B and USB D+/D− within a USB Type-C cable shall meet the requirement described in Section 3.7.2.3.5.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

5.1.4 Example Alternate Mode – USB DisplayPort™ Dock

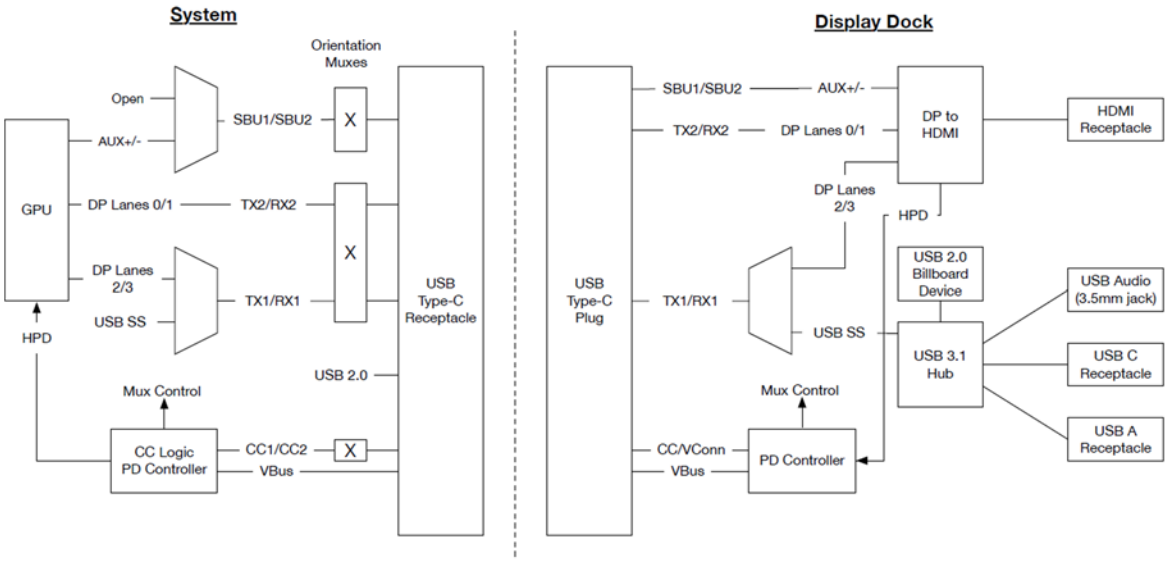
This example illustrates the use of Structured VDMs to expose and access functionality beyond the basic functionality defined by the USB Type-C Connector. The device uses its USB Type-C connector to make connection when placed in a cradle dock. This example only illustrates the functional connections.

5.1.4.1 USB DisplayPort Dock Example

- The cradle dock provides mechanical alignment and attachment in addition to those provided by the USB Type C connector allowing for only one orientation eliminating the need for an orientation MUX in the dock.
- The dock and system use *USB PD* to manage charging and power.
- The dock uses DisplayPort to drive a DisplayPort-to-HDMI adapter to support connecting an HDMI monitor.
- The dock has a USB hub that exposes two external USB ports and attached internal USB Devices, e.g. a USB audio Device (a 3.5 mm audio jack), and a USB Billboard Device.

Figure 5-5 illustrates the USB DisplayPort Dock example in a block diagram form.

Figure 5-5 USB DisplayPort Dock Example



The system uses *USB PD* Structured VDMs to communicate with the dock to discover that it supports a compatible Alternate Mode. The system then uses a Structured VDM to enter the dock mode. Since *USB PD* is used, it may also be used to negotiate power for the system and dock. In this example, the USB SuperSpeed signals allow the dock to work as a USB-only dock when attached to a system that does not fully support the dock or even *USB PD*.

5.1.4.2 Functional Overview

The following summarizes the behavior resulting from attaching the example USB DisplayPort Dock for three likely host system cases.

1. Host system does not support *USB PD* or supports *USB PD* without Structured VDMs

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- The host does not support *USB PD*, or supports *USB PD* but not Structured VDMs, so it will not look for SVIDs using the Structured VDM method.
- The host will discover the USB hub and operates as it would when connected to any USB hub.
- Since the host will not send an Enter Mode command, after tAMETimeout the dock will expose a *USB Billboard Device Class* interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the *USB Billboard Device Class* information.

2. Host system supports *USB PD* and Structured VDMs but does not support this specific USB DisplayPort Dock
   - The host discovers the USB hub and operates as it would when connected to any USB hub.
   - The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock may or may not be recognized by the Host.
   - If that VID is recognized by the Host, the Host then requests the modes associated with this VID. The mode associated with this USB DisplayPort Dock is not recognized by the Host.
   - Since the host does not recognize the mode as being supported hence will not send the Enter Mode command, after tAMETimeout the dock will expose a *USB Billboard Device Class* interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the *USB Billboard Device Class* information.
3. Host system supports this specific USB DisplayPort Dock
   - The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock is recognized by the Host.
   - The Host then requests the modes associated with this VID. The mode associated with this USB/Display Dock is recognized by the Host.
   - Since this mode is recognized as supported, the Host uses the Enter Mode command to reconfigure the USB Type-C receptacle and enter the USB DisplayPort Dock mode.
   - The USB DisplayPort Dock may optionally expose the *USB Billboard Device Class* interface to provide additional information to the OS.

5.1.4.3 Operational Summary

The following summarizes the basic process of discovery through configuration when the USB DisplayPort Dock is attached to the Host.

1. Host detects presence of a device (CC pins) and connector orientation
2. Host applies default VBUS
3. Host applies VCONN because the dock presents Ra
4. Host uses *USB PD* to make power contract with the USB DisplayPort Dock
5. Host runs the Discover Identify process
   a. Sends Discover Identity message
   b. Receives an ACK message with information identifying the cable

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

6. Host runs the Discover SVIDs process
    a. Sends Discover SVID message
    b. Receives an ACK message with list of SVIDs for which the Dock device has modes
7. Host runs the Discover Modes process
    a. Sends Discover Modes VDM for the VIDs previously discovered
    b. Receives an ACK message with a list of modes associated with each VID
    c. If USB DisplayPort Dock mode not found, dock will timeout and present the *USB Billboard Device Class* interface and the OS will inform the user of the error - done
    d. Else
8. Host runs the Enter Mode process
    a. Sends Enter Mode VDM with VID and USB DisplayPort Dock mode
    b. Receives an ACK message – Host is now attached to the USB DisplayPort Dock and supports DisplayPort signaling to interface additional functions in combination with USB signaling
9. Host stays in the USB DisplayPort Dock mode until
    a. Explicitly exited by an Exit Mode VDM
    b. System physically disconnected from the USB DisplayPort Dock
    c. Hard Reset on *USB PD*
    d. VBUS is removed

5.2 Managed Active Cables

Active cables that require configuration (managed active cable) shall use *USB Power Delivery* Structured VDMs to discover and configure the cable.

USB Power Delivery Structured VDMs provide a standardized mechanism for identifying and managing the functionality of active cables.

Some managed active cables only have a single *USB PD* controller in the cable that responds to *USB PD* Structured VDMs sent to SOP'.

When a managed active cable requires independent management at each end of the cable, separate *USB PD* controllers responding to *USB PD* Structured VDMs sent to SOP' and SOP" can be located in each plug.

5.2.1 Requirements for Managed Active Cables that respond to SOP' and SOP"

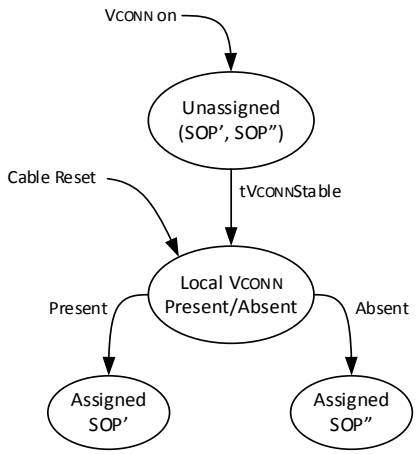
After a power-on reset event or a *USB PD* Hard Reset, the *USB PD* controller attached to the Source is assigned SOP' and the *USB PD* controller attached to the Sink is assigned SOP". After a *USB PD* Cable Reset, the plug being supplied VCONN responds to SOP' independent of whether it is the plug attached to the Source or Sink. The controllers can sense whether they are SOP' or SOP" based on the presence of VCONN at the plug's VCONN pin as only one port supplies VCONN.

Figure 5-6 illustrates the process that shall be followed to assign SOP' and SOP" to the ends attached to the Source and Sink, respectively, at power on. In the Unassigned state, the

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

active cable will not respond to any *USB PD* communication sent to SOP' or SOP". The parameter tVCONNStable allows time for the active cable to set up to communicate.

Figure 5-6 Managed Active Cable Plug SOP' and SOP" Assignment



When VCONN is removed, the plug's local VCONN shall discharge to below its SOP' detection threshold within 20 ms.

A managed active cable shall assure that the two *USB PD* controllers are uniquely assigned via the mechanism described here, one as SOP' and the other as SOP".

USB PD supports three types of USB Type-C-related swaps that may or may not impact VCONN:

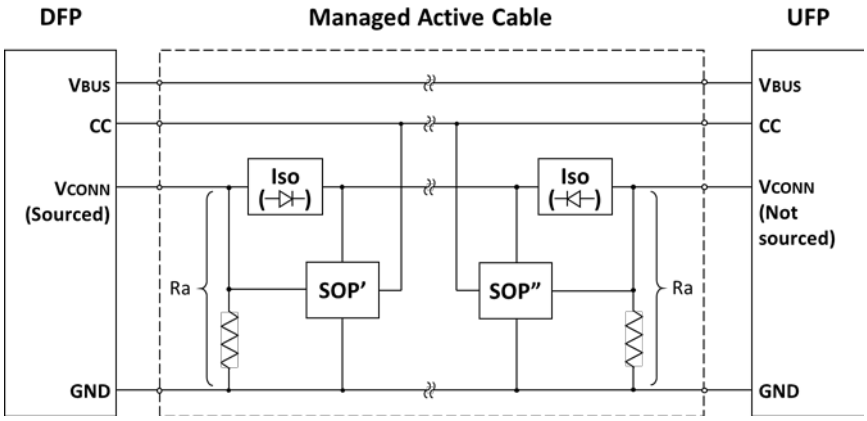
- *USB PD* VCONN_Swap – The port previously not supplying VCONN sources VCONN and the assignment of SOP' and SOP" remain unchanged.
- *USB PD* DR_Swap – The assignment of SOP' and SOP" remain unchanged.
- *USB PD* PR_Swap – The assignment of SOP' and SOP" remain unchanged.

Managed active USB Type-C to USB Type-C cables shall by default support USB operation. Multi-modal cables (e.g., an active cable that supports an Alternate Mode in addition to USB SuperSpeed) that use the TX/RX signal pairs shall minimally support *USB 3.1* Gen 1 operation. They are encouraged to support both Gen 1 and Gen 2 operation.

Figure 5-7 illustrates a typical managed active cable. The isolation elements (Iso) shall prevent VCONN from traversing end-to-end through the cable. Ra is required in the cable to allow the DFP to determine that VCONN is needed.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure 5-7 Managed Active Cable



5.2.1.1 Parameter Values

Table 5-2 provides the power on timing requirements for SOP' and SOP" to be ready to communicate.

Table 5-4 SOP' and SOP" Timing

	Maximum	Description
tVCONNStable	50 ms	The time between the application of VCONN until SOP' and SOP" shall be ready for communication.

5.2.2 Cable Message Structure

USB PD Structured VDMs shall be used to identify and manage active cables. Cables that require additional functionality, for example to program parameters in the active electronics, may define proprietary Structured VDMs to provide the necessary functionality. In all cases, these messages shall only use SOP' and SOP". They shall not use SOP.

SOP' and SOP" are defined to allow a vendor to communicate individually with each end the cable.

For active cables that support both SOP' and SOP", after attach or a *USB PD* Cable Reset, the plug directly connected to the Source shall only respond to SOP' and the plug directly connected to the Sink shall only respond to SOP".

The assignment of SOP' and SOP" to each plug remains persistent until VCONN is removed or a subsequent *USB PD* Cable Reset.

The Discover Identity message shall start with SOP'.

5.2.3 Modal Cable Management

In addition to supporting the Discover Identity message, managed active cables shall support the following *USB Power Delivery* Structured VDMs. These VDMs shall start with SOP'.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 192
Microchip v. Aptiv
IPR2024-00496

5.2.3.1 Discover SVIDs

The managed active cable shall return a list of SVIDs that it supports.

5.2.3.2 Discover Modes

The managed active cable shall return a list of Alternate Modes it supports for each SVID.

5.2.3.3 Enter Mode

The managed active cable shall use the Enter Mode command to enter an Alternate Mode. The behavior of the cable following Enter Mode is vendor specific.

5.2.3.4 Exit Mode

The managed active cable shall use the Exit Mode command to exit an Alternate Mode previously entered. Exit Mode shall return the cable to its default USB operation.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

A Audio Adapter Accessory Mode

A.1. Overview

Analog audio headsets are supported by multiplexing four analog audio signals onto pins on the USB Type-C™ connector when in the Audio Adapter Accessory Mode. The four analog audio signals are the same as those used by a traditional 3.5 mm headset jack. This makes it possible to use existing analog headsets with a 3.5 mm to USB Type-C adapter. The audio adapter architecture allows for an audio peripheral to provide up to 500 mA back to the system for charging.

An analog audio adapter could be a very basic USB Type-C adapter that only has a 3.5 mm jack or it could be an analog audio adapter with a 3.5 mm jack and a USB Type-C receptacle to enable charge-through. The headset shall not use a USB Type-C plug to replace the 3.5 mm plug.

A.2. Detail

An analog audio adapter shall use a captive cable with a USB Type-C plug or include an integrated USB Type-C plug.

The analog audio adapter shall identify itself by presenting a resistance to GND of ≤ Ra on both A5 (CC) and B5 (V_{CONN}) of the USB Type-C plug. If pins A5 and B5 are shorted together, the effective resistance to GND shall be less than Ra/2.

A DFP that supports analog audio adapters shall detect the presence of an analog audio adapter by detecting a resistance to GND of less than Ra on both A5 (CC) and B5 (VCONN).

Table A-1 shows the pin assignments at the USB Type-C plug that shall be used to support analog audio.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Table A-1 USB Type-C Analog Audio Pin Assignments

Plug Pin	USB Name	Analog Audio Function	Location on 3.5 mm Jack	Notes
A5	CC			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
B5	VCONN			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
A6/B6	Dp	Right	Ring 1	Analog audio right channel A6 and B6 shall be shorted together in the adapter.
A7/B7	Dn	Left	Tip	Analog audio left channel A7 and B7 shall be shorted together in the adapter.
A8	SBU1	Mic/AGND	Ring 2	Analog audio microphone (OMTP & YD/T) or Audio GND (CTIA).
B8	SBU2	AGND/Mic	Sleeve	Audio GND (OMTP & YD/T or analog audio microphone (CTIA).
A1/A12 B1/B12	GND			Digital GND (DGND) used as the ground reference and current return for CC1, CC2, and VBUS.
A4/A9 B4/B9	VBUS			Not connected unless the audio adapter uses this connection to provide 5 V @ 500 mA for charging the system's battery.
Others				Other pins shall not be connected.

The analog audio signaling presented by the headset on the 3.5 mm jack is expected to comply with at least one of the following:

- The traditional American headset jack pin assignment, with the jack sleeve used for the microphone signal, supported by CTIA-The Wireless Association
- "Local Connectivity: Wired Analogue Audio" from the Open Mobile Terminal Forum (OMTP) forum
- "Technical Requirements and Test Methods for Wired Headset Interface of Mobile Communication Terminal" (YT/D 1885-2009) from the China Communications Standards Association

When in the Audio Adapter Accessory Mode, the system shall not provide VCONN power on either CC1 or CC2. Failure to do this may result in VCONN being shorted to GND when an analog audio peripheral is present.

The system shall connect A6/B6, A7/B7, A8 and B8 to an appropriate audio codec upon entry into the Audio Adapter Accessory Mode. The connections for A8 (SBU1) and B8 (SBU2) pins are dependent on the adapter's orientation. Depending on the orientation, the microphone and analog ground pins may be swapped. These pins are already reversed between the two major standards for headset jacks and support for this is built into the headset connection of many codecs or can be implemented using an autonomous audio headset switch. The system shall work correctly with either configuration.

A.3. Electrical Requirements

The maximum ratings for pin voltages are referenced to GND (pins A1, A12, B1, and B12). The non-GND pins on the plug shall be isolated from GND on the USB Type-C connector and shall be isolated from the USB plug shell. To minimize the possibility of ground loops

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

between systems, AGND shall be connected to GND only within the system containing the USB Type-C receptacle. Both the system and audio device implementations shall be able to tolerate the Right, Left, Mic, and AGND signals being shorted to GND. The current provided by the amplifier driving the Right and Left signals shall not exceed ±150 mA per audio channel, even when driving a 0 Ω load.

Table A-2 shows allowable voltage ranges on the pins in the USB Type-C plug that shall be met.

Table A-2 USB Type-C Analog Audio Pin Electrical Parameter Ratings

Plug Pin	USB Name	Analog Audio Function	Min	Max	Units	Notes
A6/B6	Dp	Right	−3.0	3.0	V	A6 and B6 shall be shorted together in the analog audio adapter
A7/B7	Dn	Left	−3.0	3.0	V	A7 and B7 shall be shorted together in the analog audio adapter
A8	SBU1	Mic/AGND	−0.4	3.3	V	
B8	SBU2	AGND/Mic	−0.4	3.3	V	

The maximum voltage ratings for Left and Right signals are selected to encompass a 2 Vrms sine wave (2.828 Vp = 5.657 Vpp = 6 dBV) which is a common full-scale voltage for headset audio output.

Headset microphones operate on a positive bias voltage provided by the system's audio codec and AC-couple the audio signal onto it. Some headsets may produce an audio signal level up to 0.5 Vrms (0.707 Vp = 1.414 Vpp = -6 dBV) but this is biased so that the voltage does not swing below GND. The bias voltage during operation is typically around 1.25 V but it varies quite a bit depending on the specifics of the manufacturer's design, therefore the maximum voltage rating for the SBU pins is selected to allow a variety of existing solutions.

While one SBU pin carries the Mic signal, the other SBU pin serves as AGND carrying the return current for Left, Right, and Mic. If we assume a worst-case headset speaker impedance of 16 Ω per speaker, then the worst-case return current for the speakers is ± 0.2 A. If we assume that the worst-case resistance from the AGND pin to GND within the USB Type-C system is 1 Ω (due to FET R_{ON} within the signal multiplexer, contact, and trace resistances), then the voltage of the AGND pin with respect to USB Type-C GND can vary between ± 0.2 V. The minimum voltage rating for the SBU pins has been selected to allow for this scenario with some additional margin to account for Mic signal return current and tolerances.

The system shall exhibit no more than -48 dB linear crosstalk between the Left and Right audio channels and exhibit no more than -51 dB linear crosstalk from the Left or Right channel to the Mic channel. Crosstalk measurements shall be made using a measurement adapter plug that supports USB Type-C analog audio connections according to Table A-1. In the measurement adapter, the Left and Right channels are terminated with 32 Ω resistors to AGND, the Mic channel is terminated with 2k Ω resistor to AGND; AGND is connected to USB Type-C Plug Pin A8, and the Mic channel is connected to USB Type-C Plug Pin B8.

Crosstalk shall be measured by using the system to drive a sine wave signal to the Left output channel and zero signal to the Right output channel. The system shall configure the Mic channel according to the default Mic operating mode supported by the system. AC voltage levels at the Left, Right and Mic channels are measured across the corresponding termination resistors using a third-octave filter at the sine signal frequency. Left – Right

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

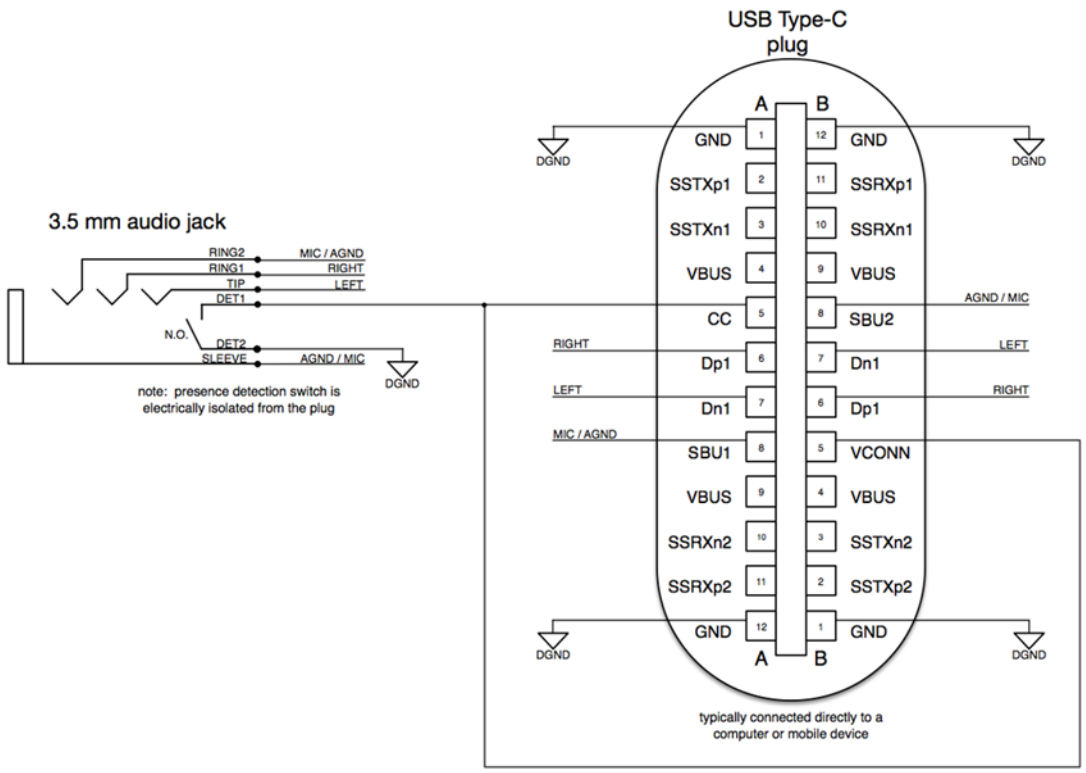
crosstalk is reported as ratio of the Right channel voltage to the Left channel voltage expressed in decibels. Similarly, the Left – Mic crosstalk is reported. The measurements shall be conducted at 31.5, 63, 125, 250, 500, 1000, 2000, 4000, 8000 and 16000 Hz frequencies. The measurements shall be repeated so that the sine wave signal is driven to the Right channel and Right – Left and Right – Mic crosstalk results are obtained. Both USB Type-C plug orientations shall be measured."

A.4. Example Implementations

A.4.1. Passive 3.5 mm to USB Type-C Adapter – Single Pole Detection Switch

Figure A-1 illustrates how a simple 3.5 mm analog audio adapter can be made. In this design, there is an audio plug that contains a single-pole detection switch that is used to completely disconnect the CC and VCONN pins from digital GND when no 3.5 mm plug is inserted. This has the effect of triggering the USB Type-C presence detect logic upon insertion or removal of either the 3.5 mm plug or the audio adapter itself.

Figure A-1 Example Passive 3.5 mm to USB Type-C Adapter



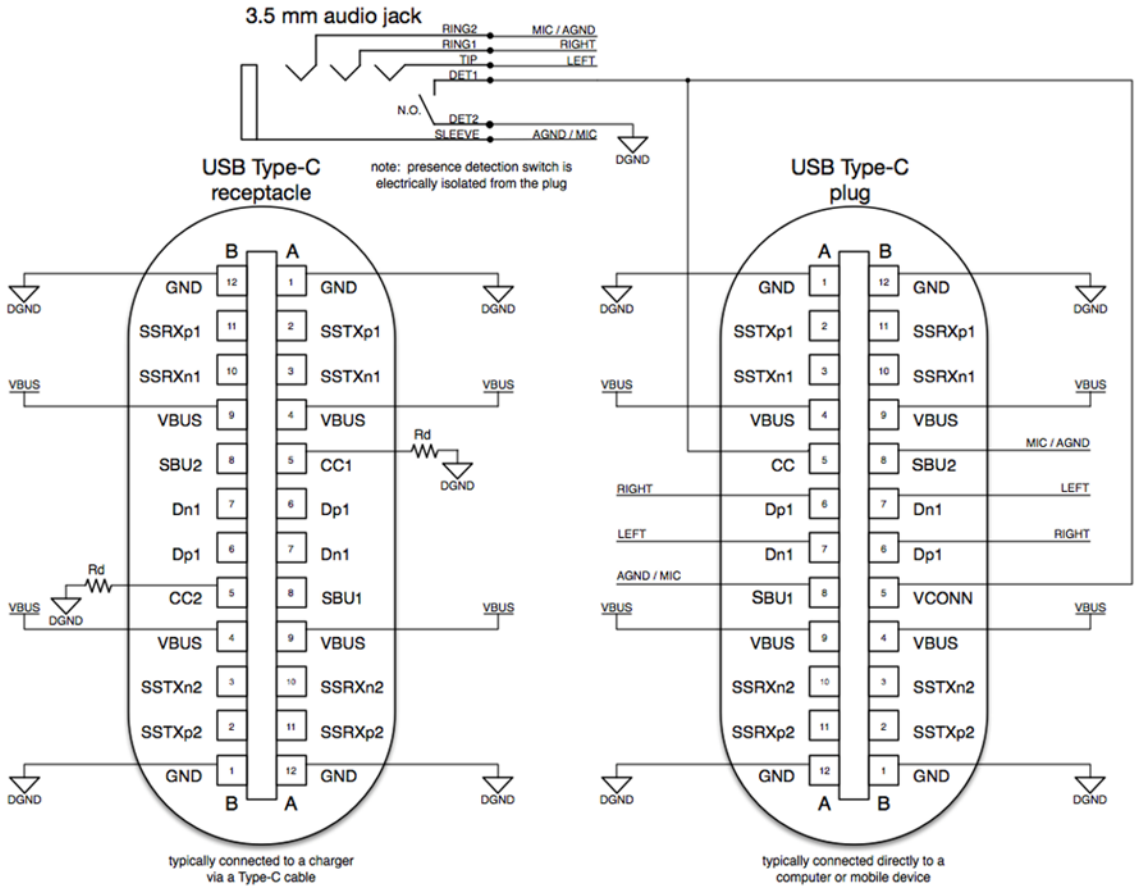
A.4.2. 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through

Figure A-2 illustrates a 3.5 mm analog audio adapter that supports charge-through operation. Charging power comes into the adapter through a USB Type-C receptacle and is routed directly to the adapter's USB Type-C plug, which is plugged into the device being charged. This design is limited to providing 500 mA of charge-through current since it has no way to advertise greater current-sourcing capability. The USB Type-C receptacle presents Rd on both of its CC pins because a CC pull-down must be present for the receptacle to indicate that it wants to consume VBUS current. USB Type-C systems that support analog audio should ensure that charging is not interrupted by insertion or removal of the 3.5 mm

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

audio plug and that audio is not interrupted by insertion or removal of the cable connected to the audio adapter's USB Type-C receptacle by using the system's presence detection logic monitoring the states of both the CC1 and CC2 pins and VBUS.

Figure A-2 Example 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

B Debug Accessory Mode

B.1. Overview

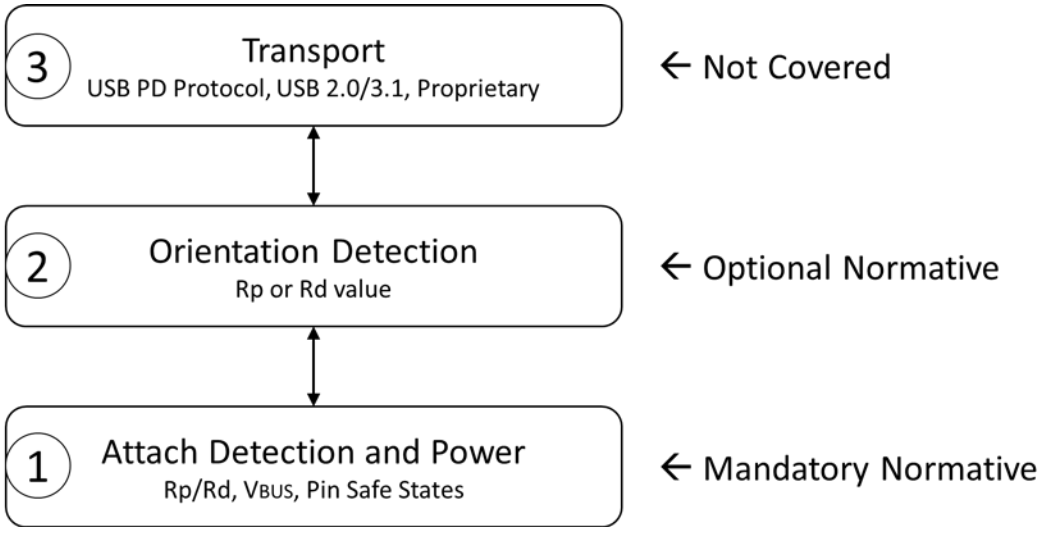
This appendix covers the functional requirements for the USB Type-C Debug Accessory Mode (DAM), Debug and Test System (DTS), and Target System (TS). The USB Type-C connector is ideal for debug of closed-chassis, form-factor devices. Debug covers many areas, ranging from detailed JTAG Test Access Port (TAP)-level debug in a lab to high-level debug of software applications in production. Lab debug requires early debug access to hardware registers soon after reset, whereas software debug uses kernel debuggers, etc. to access software state. Debug Accessory Mode in USB Type-C enables debug of closed-chassis, form-factor devices by re-defining the USB Type-C ports for debug purposes.

Basic debug requirements are defined as a standard feature, and additional debug features may be added as per vendor specifications.

B.2. Functional

The USB Type-C Debug Accessory Mode follows a layered structure as shown in Figure B-1, defining the minimum physical layer for Attach, Detection and Power. Orientation detection is optional normative. The transport layer is left proprietary and is not covered in this document.

Figure B-1 USB Type-C Debug Accessory Layered Behavior



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

B.2.1. Signal Summary

Figure B-2 shows the pin assignments of the DTS plug that are used to support DAM. The pins highlighted in yellow are those available to be configured for debug signals. Both CC1 and CC2 are used for current advertisement and optional orientation detection.

Figure B-2 DTS Plug Interface

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC1	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	CC2	D+	D-	SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The DTS and TS must follow the USB Safe State detailed in Section 5.1.2.2 at all times (whether in DAM or not).

B.2.2. Port Interoperability

Table B-1 summarizes the expected results when interconnecting a DTS Source, Sink or DRP port to a TS Source, Sink or DRP port.

Table B-1 DTS to TS Port Interoperability

	DTS Source	DTS Sink	DTS DRP
TS Sink	Functional	Non-functional[1]	Functional
TS Sink w/ Accessory Support	Functional	Non-functional[1]	Functional
TS DRP	Functional	Functional	Functional
TS Source	Non-functional[1]	Functional	Functional

1. In the cases where no function results, neither port shall be harmed by this connection. Following the USB Safe State ensures this.

B.2.3. Debug Accessory Mode Entry

The typical flow for the configuration of the interface in the general case of a DTS to a TS is as follows:

1. Detect a valid connection between the DTS (Source, Sink, or DRP) and TS (Source, Sink, or DRP)
2. Optionally determine orientation of the plug in the receptacle
3. Optionally establish *USB PD* communication over CC for advanced power delivery negotiation and alternate modes. *USB PD* communication is allowed only if the optional orientation of the plug is determined.
4. Establish test access connections with the available USB Type-C signals

The DTS DRP will connect as either a Source or a Sink, but its state diagram gives preference to the Source role.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

B.2.3.1. Detecting a Valid DTS-to-TS Connection

The general concept for setting up a valid connection between a DTS and TS is based on being able to detect the typical USB Type-C termination resistances. However, detecting a Debug Accessory Mode connection requires that both CC pins must detect a pull-up (Rp) or pull-down (Rd) termination. A USB Type-C Cable does not pass both CC wires so a receptacle to receptacle Debug Accessory Mode connection cannot be detected.

A DTS is only allowed to connect to a TS that is presenting either Rp/Rp or Rd/Rd. Otherwise, the TS does not support Debug Accessory Mode.

To detect either an Rp/Rp or Rd/Rd, the DTS must be a captive cable or a direct-attach device with a USB Type-C plug and the TS must have a USB Type-C receptacle.

B.2.4. Connection State Diagrams

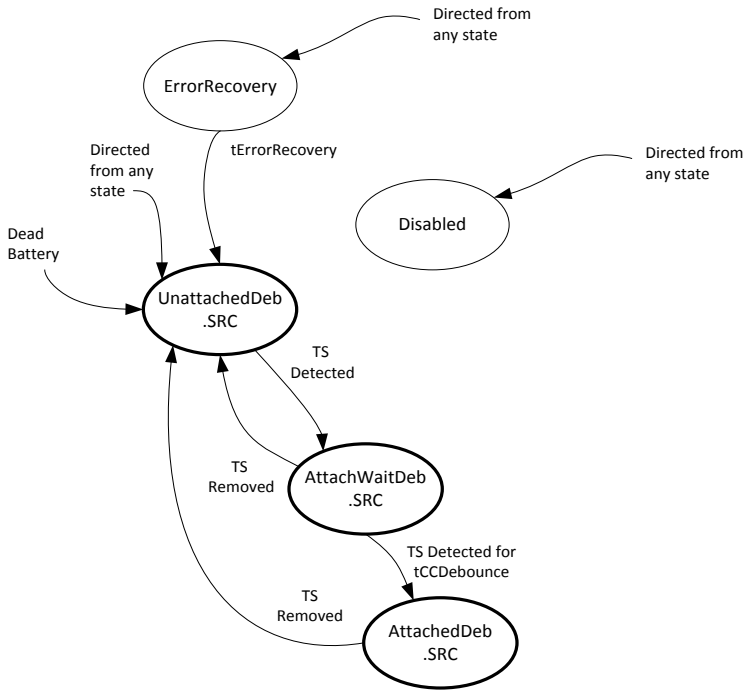
This section provides reference connection state diagrams for CC-based behaviors of the DTS. The TS connection state diagrams are found in Section 4.5.2.

Refer to Section B.2.4.1 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section B.2.4.3 for a description of which states are mandatory for each port type and a list of states where *USB PD* communication is permitted.

Figure B-3 illustrates a connection state diagram for a DTS Source.

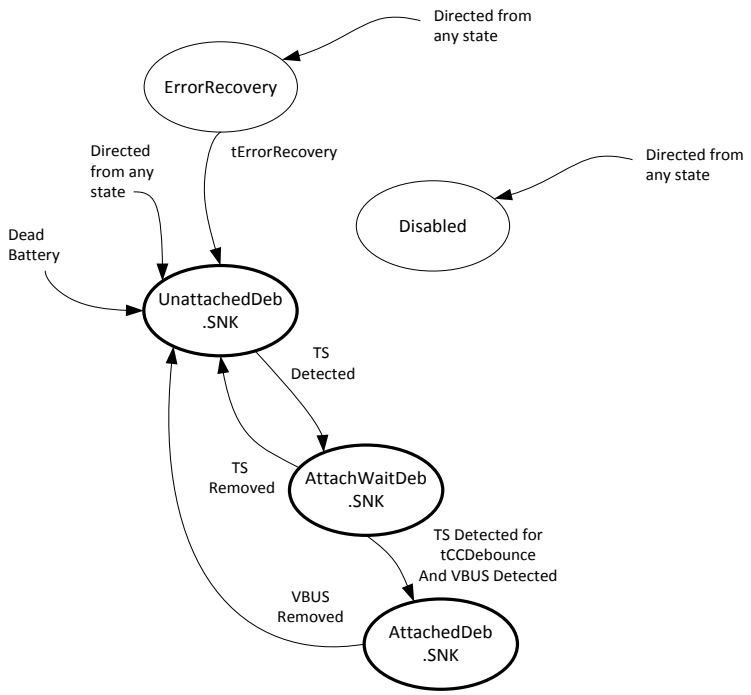
Figure B-3 Connection State Diagram: DTS Source



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure B-4 illustrates a connection state diagram for a simple DTS Sink.

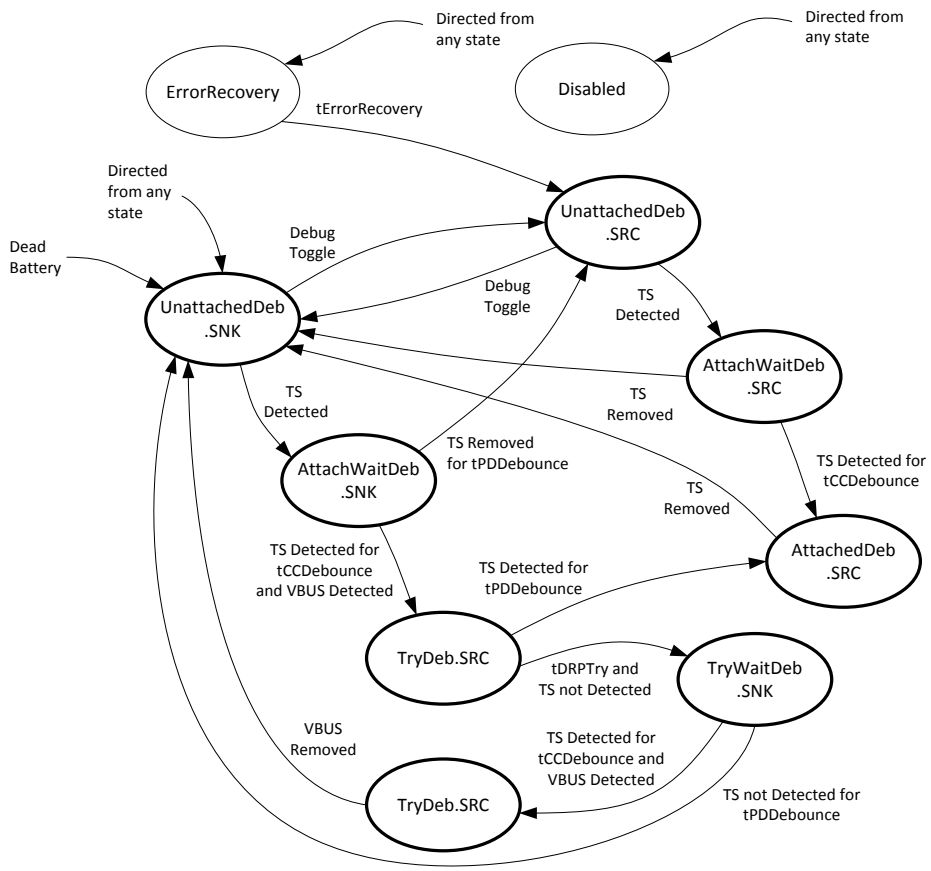
Figure B-4 Connection State Diagram: DTS Sink



Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure B-5 illustrates a connection state diagram for a DTS DRP.

Figure B-5 Connection State Diagram: DTS DRP



B.2.4.1. Connection State Machine Requirements

The DTS state machine requirements follow those outlined in Section 4.5.2.2 for the general USB Type-C state machines with the additional following states defined.

Note, VCONN shall not be driven by any DTS or TS port in any state.

B.2.4.1.1. Exiting From ErrorRecovery State

This state appears in Figure B-3, Figure B-4, and Figure B-5.

The ErrorRecovery state is where the DTS cycles its connection by removing all terminations from the CC pins for tErrorRecovery followed by transitioning to the appropriate UnattachedDeb.SNK or UnattachedDeb.SRC state based on DTS type.

The DTS should transition to the ErrorRecovery state from any other state when directed.

A DTS may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the DTS shall be directed to the Disabled state if supported. If the Disabled state

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

is not supported, the DTS shall be directed to either the UnattachedDeb.SNK or UnattachedDeb.SRC states.

A DTS Sink shall transition to UnattachedDeb.SNK after tErrorRecovery.

A DTS Source shall transition to UnattachedDeb.SRC after tErrorRecovery.

A DTS DRP shall transition to UnattachedDeb.SRC after tErrorRecovery.

B.2.4.1.2. UnattachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the UnattachedDeb.SNK state, the DTS is waiting to detect the presence of a TS Source.

A DTS with a dead battery shall enter this state while unpowered.

B.2.4.1.2.1 UnattachedDeb.SNK Requirements

The DTS shall not drive VBUS.

Both CC pins shall be independently terminated to ground through Rd.

B.2.4.1.2.2 Exiting from UnattachedDeb.SNK State

The DTS shall transition to AttachWaitDeb.SNK when a TS Source connection is detected, as indicated by the SNK.Rp state on both of its CC pins.

A DTS DRP shall transition to UnattachedDeb.SRC within tDRPTransition after the state of one or both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

B.2.4.1.3. AttachWaitDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the AttachWaitDeb.SNK state, the DTS has detected the SNK.Rp state on both CC pins and is waiting for VBUS.

B.2.4.1.3.1 AttachWaitDeb.SNK Requirements

The requirements for this state are identical to UnattachedDeb.SNK.

B.2.4.1.3.2 Exiting from AttachWaitDeb.SNK State

A DTS Sink shall transition to UnattachedDeb.SNK when the state of one or both CC pins is SNK.Open for at least tPDDebounce.

A DTS DRP shall transition to UnattachedDeb.SRC when the state of one or both CC pins is SNK.Open for at least tPDDebounce.

A DTS Sink shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

A DTS DRP shall transition to TryDeb.SRC when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

B.2.4.1.4. AttachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the AttachedDeb.SNK state, the DTS is attached and operating as a DTS Sink.

B.2.4.1.4.1 AttachedDeb.SNK Requirements

This mode is for debug only

The port shall not drive VBUS.

The port shall provide an Rd as specified in Table 4-12 on both CC pins if orientation is not needed. See Section B.2.6 for orientation detection.

The port shall source current on both CC pins and monitor to detect when VBUS is removed.

If the DTS needs to establish a *USB PD* communications, it shall do so only after entry to this state. In this state, the DTS takes on the initial *USB PD* role of UFP/Sink.

The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.

The DTS may follow the DAM Sink Power Sub-State behavior specified in Section 4.5.2.3

B.2.4.1.4.2 Exiting from AttachedDeb.SNK State

A DTS shall transition to UnattachedDeb.SNK when VBUS is no longer present

B.2.4.1.5. UnattachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the UnattachedDeb.SRC state, the DTS is waiting to detect the presence of a TS Sink

B.2.4.1.5.1 UnattachedDeb.SRC Requirements

The DTS shall not drive VBUS.

The DTS shall source current on both CC pins independently.

The DTS shall provide a unique Rp value on each CC pin as specified in Section 4.5.2.3

B.2.4.1.5.2 Exiting from UnattachedDeb.SRC State

The DTS shall transition to AttachWaitDeb.SRC when the SRC.Rd state is detected on both CC pins.

A DTS DRP shall transition to UnattachedDeb.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

B.2.4.1.6. AttachWaitDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

The AttachWaitDeb.SRC state is used to ensure that the state of both of the CC pins is stable after a TS Sink is connected.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 205
Microchip v. Aptiv
IPR2024-00496

B.2.4.1.6.1 AttachWaitDeb.SRC Requirements

The requirements for this state are identical to UnattachedDeb.SRC.

B.2.4.1.6.2 Exiting from AttachWaitDeb.SRC State

The DTS shall transition to AttachedDeb.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both of the CC pins for at least tCCDebounce.

A DTS Source shall transition to UnattachedDeb.SRC and a DTS DRP to UnattachedDeb.SNK when the SRC.Open state is detected on either of the CC pins.

B.2.4.1.7. AttachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the AttachedDeb.SRC state, the DTS is attached and operating as a DTS Source.

B.2.4.1.7.1 AttachedDeb.SRC Requirements

The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.

The DTS shall supply VBUS current at the level it advertises. See Section B.2.6.1.1 for advertising current level.

The DTS shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.

If the DTS needs to establish *USB PD* communications, it shall do so only after entry to this state. The DTS shall not initiate any *USB PD* communications until VBUS reaches vSafe5V. In this state, the DTS takes on the initial *USB PD* role of DFP/Source.

The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.

B.2.4.1.7.2 Exiting from AttachedDeb.SRC State

A DTS Source shall transition to UnattachedDeb.SRC when the SRC.Open state is detected on either CC pin.

A DTS DRP shall transition to UnattachedDeb.SNK when SRC.Open is detected on either CC pin.

A DTS shall cease to supply VBUS within tVBUSOFF of exiting AttachedDeb.SRC.

B.2.4.1.8. TryDeb.SRC State

This state appears in Figure B-5.

When in the TryDeb.SRC state, the DTS DRP is querying to determine if the TS is also a DRP, to favor the DTS taking the Source role.

B.2.4.1.8.1 TryDeb.SRC Requirements

The DTS shall not drive VBUS.

The DTS shall source current on both CC pins independently.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.

B.2.4.1.8.2 Exiting from TryDeb.SRC State

The DTS shall transition to AttachedDeb.SRC when the SRC.Rd state is detected on both CC pins for at least tPDDebounce.

The DTS shall transition to TryWaitDeb.SNK after tDRPTry if the state of both CC pins is not SRC.Rd.

B.2.4.1.9. TryWaitDeb.SNK State

This state appears in Figure B-5.

When in the TryWaitDeb.SNK state, the DTS has failed to become a DTS Source and is waiting to attach as a DTS Sink.

B.2.4.1.9.1 TryWaitDeb.SNK Requirements

The DTS shall not drive VBUS.

Both CC pins shall be independently terminated to ground through Rd.

B.2.4.1.9.2 Exiting from TryWaitDeb.SNK State

The DTS shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

The DTS shall transition to UnattachedDeb.SNK when the state of one of the CC pins is SNK.Open for at least tPDDebounce or if VBUS is not detected within tPDDebounce.

B.2.4.2. Power Sub-State Requirements

B.2.4.2.1. TS Sink Power Sub-State Requirements

When in the DebugAccessory.SNK state and the DTS Source is supplying default VBUS, the TS Sink shall operate in one of the sub-states shown in Figure B-6. The initial TS Sink Power Sub-State is PowerDefaultDeb.SNK. Subsequently, the TS Sink Power Sub-State is determined by the DTS Source's USB Type-C current advertisement determined by the Rp value on each CC pin as shown in Table B-2. The TS Sink in the attached state shall remain within the TS Sink Power Sub-States until either VBUS is removed or a *USB PD* contract is established with the Source.

The TS Sink is only required to implement TS Sink Power Sub-State transitions if the TS Sink wants to consume more than default USB current.

Note, a TS Source will not use the values in Table B-2. A TS Source will present the same Rp on each CC pin using the standard Rp value for the desired current advertisement.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

Figure B-6 TS Sink Power Sub-States

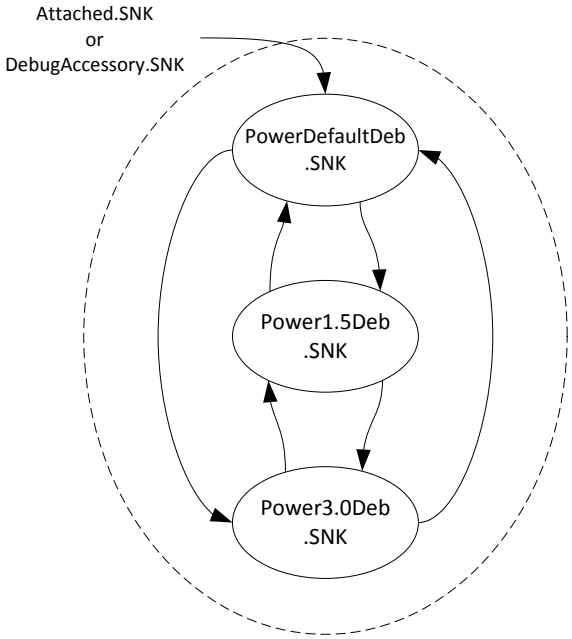


Table B-2 Rp/Rp Charging Current Values for a DTS Source

Mode of Operation	CC1	CC2
Default USB Power	Rp for 3 A	Rp for 1.5 A
USB Type-C Current @ 1.5 A	Rp for 1.5 A	Rp for Default
USB Type-C Current @ 3 A	Rp for 3 A	Rp for Default

B.2.4.2.2. PowerDefaultDeb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the lowest range (default) of Source-supplied current.

B.2.4.2.2.1 PowerDefaultDeb.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the DTS Sink wants to consume more than the default USB power, it shall monitor vRd on both CC pins to determine if more current is available from the Source.

B.2.4.2.2.2 Exiting from PowerDefaultDeb.SNK

For any change on CC indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on each CC pin have been stable for at least tPDDebounce.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 208
Microchip v. Aptiv
IPR2024-00496

For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.

For vRd voltages on the CC pins indicating 3 A mode, the DAM Sink shall transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.3. Power1.5Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the two lower ranges (default and 1.5 A) of DAM Source-supplied current.

B.2.4.2.3.1 Power1.5Deb.SNK Requirements

The DAM Sink shall draw no more than 1.5 A from VBUS.

The DAM Sink shall monitor both vRd voltages while it is in this sub-state.

B.2.4.2.3.2 Exiting from Power1.5Deb.SNK

For any change on the CC pins indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on both CC pins have been stable for at least tPDDebounce.

For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For vRd voltages on the CC pins indicating 3 A mode, the port shall transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.4. Power3.0Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of DAM Source-supplied current.

B.2.4.2.4.1 Power3.0Deb.SNK Requirements

The port shall draw no more than 3.0 A from VBUS.

The port shall monitor both vRd voltages while it is in this sub-state.

B.2.4.2.4.2 Exiting from Power3.0Deb.SNK

For any change on the CC pins indicating a change in allowable power, the port shall not transition until the new vRd voltages on both CC pins have been stable for at least tPDDebounce.

For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.

B.2.4.2.5. DTS Sink Power Sub-State Requirements

A DTS Sink follows the same power sub-states defined in Section 4.5.2.3. The TS Source will be advertising current with a standard Rp value that is the same for each CC pin. If optional

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 209
Microchip v. Aptiv
IPR2024-00496

orientation detection is performed, the DTS Sink will only be able to determine the Rp value from the CC pin that is set for *USB PD* communication.

B.2.4.3. Connection States Summary

Table B-3 defines the mandatory and optional states for each type of port. For states allowing *USB PD* communication, DAM connections requiring *USB PD* communication shall determine orientation by the steps described in Section B.2.6.

Table B-3 Mandatory and Optional States

	DTS Source	DTS SINK	DTS DRP	USB PD Communication and/or Debug Signal Activity
UnattachedDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWaitDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachedDeb.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWaitDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachedDeb.SRC	Mandatory	N/A	Mandatory	Permitted
TryDeb.SRC	N/A	N/A	Mandatory	Not Permitted
TryWaitDeb.SNK	N/A	N/A	Mandatory	Not Permitted

B.2.5. DTS Port Interoperability Behavior

This section describes interoperability behavior between DTS ports and TS ports.

B.2.5.1. DTS Port to TS Port Interoperability Behaviors

The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks and DRPs as presented in Table B-1.

B.2.5.1.1. DTS Source to TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a TS Sink.

1. DTS Source and TS Sink in the unattached state
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 210
Microchip v. Aptiv
IPR2024-00496

- TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK

4. While the DTS Source and TS Sink are in the attached state:
   - DTS Source adjusts both Rp values as needed for offered current
   - TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
   - DTS Source monitors both CC pins for detach and when detected on either pin, enters UnattachedDeb.SRC
   - TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.2. DTS Source to TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a TS DRP.

1. DTS Source and TS DRP in the unattached state
   - TS DRP alternates between Unattached.SRC and Unattached.SNK
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the TS DRP's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. TS DRP transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK
4. While the DTS Source and TS DRP are in their respective attached states:
   - DTS Source adjusts both Rp values as needed for offered current
   - TS DRP detects and monitors vRd on both CC pins for available current on VBUS and performs any orientation required
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

B.2.5.1.3. DTS Sink to TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a TS Source.

1. TS Source and DTS Sink in the unattached state
2. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC. After tCCDebounce, it enters UnorientedDebugAccessory.SRC.
   - TS Source turns on VBUS

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK.
   - DTS Sink in AttachWaitDeb.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters AttachedDeb.SNK
   - DTS sink determines advertised current from vRd on either CC pin.
4. If orientation supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.
5. If orientation supported, TS Source detects change in vRd of one of the CC pins and transitions from UnorientedDebugAccessory.SRC to OrientedDebugAccessory.SRC and performs any orientation required.
6. While the TS Source and DTS Sink are in the attached state:
   - If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
   - TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.1.4. DTS Sink to TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a TS DRP.

1. DTS Sink and TS DRP in the unattached state
   - TS DRP alternates between Unattached.SRC and Unattached.SNK
2. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS DRP in Unattached.SRC detects both CC pull-downs of DTS Sink in UnattachedDeb.SNK and enters AttachWait.SRC
   - TS DRP in AttachWait.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters UnorientedDebugAccessory.SRC and turns on VBUS
3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters AttachedDeb.SNK
   - DTS sink determines advertised current from vRd on either CC pin.
7. If orientation is supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.
8. If orientation supported, TS DRP detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.
9. While the TS DRP and DTS Sink are in the attached state:
   - If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK
- DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.1.5. DTS DRP to TS Sink Behavior

The following describes the behavior when a DTS DRP is connected to a TS Sink.

1. DTS DRP and TS Sink in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
2. DTS DRP transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS DRP in UnattachedDeb.SRC detects both of the CC pull-downs of TS Sink enters AttachWaitDeb.SRC
   - DTS DRP in AttachWaitDeb.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters AttachedDeb.SRC
   - DTS DRP turns on VBUS
3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS Sink in Unattached.SNK detects the DTS DRP's pull-ups on both CC pins and enters AttachWait.SNK
   - TS Sink in AttachWait.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters DebugAccessory.SNK
4. While the DTS DRP and TS Sink are in their respective attached states:
   - DTS DRP adjusts Rp as needed for offered current
   - TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
   - DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK
   - TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.6. DTS DRP to TS DRP Behavior

The following describes the behavior when a DTS DRP is connected to TS DRP.

Case #1:

1. Both DRPs in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS DRP alternate between Unattached.SRC and Unattached.SNK
2. DTS DRP transitions from UnattachedDeb.SRC to AttachWaitDeb.SRC
   - DTS DRP in UnattachedDeb.SRC detects both CC pull-downs of TS DRP in Unattached.SNK and enters AttachWaitDeb.SRC
3. TS DRP transitions from Unattached.SNK to AttachWait.SNK
   - TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

4. DTS DRP transitions from AttachWaitDeb.SRC to AttachedDeb.SRC
   - DTS DRP in AttachWaitDeb.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters AttachedDeb.SRC and turns on VBUS
5. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK
   - TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK
   - TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
6. While the TS DRP and DTS DRP are in the attached state:
   - TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK
   - DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK

Case #2:

1. Both DRPs in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS DRP alternate between Unattached.SRC and Unattached.SNK
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects both CC pull-ups of TS DRP in Unattached.SRC and enters AttachWaitDeb.SNK
3. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS DRP in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC
   - TS DRP in AttachWait.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS
4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC
   - DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC
5. TS DRP transitions from UnorientedDebugAccessory.SRC to Unattached.SNK
   - TS DRP in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SNK
6. TS DRP transitions from Unattached.SNK to AttachWait.SNK
   - TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK
7. DTS DRP transitions from TryDeb.SRC to AttachedDeb.SRC
   - DTS DRP in TryDeb.SRC detects both CC pull-downs of TS DRP for tPDDebounce and enters AttachedDeb.SRC
   - DTS DRP turns on VBUS
8. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK
   - TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK
9. While the DTS DRP and TS DRP are in their respective attached states:

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- DTS DRP adjusts Rp as needed for offered current
- TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
- DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK
- TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.7. DTS DRP to TS Source Behavior

The following describes the behavior when a DTS DRP is connected to TS Source.

1. DTS DRP and TS Source in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS Source in Unattached.SRC
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK
3. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS Source in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC
   - TS Source in AttachWait.SRC continues to see both CC pull-downs of DTS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS
4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC
   - DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC
5. TS Source transitions from UnorientedDebugAccessory.SRC to Unattached.SRC
   - TS Source in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SRC
6. DTS DRP transitions from TryDeb.SRC to TryWaitDeb.SNK
   - After tDRPTry, DTS DRP does not see pull-downs on both CC pin and enters TryWaitDeb.SNK
7. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC
   - TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC
   - TS Source continues to detect pull-downs on both CC pins for tCCDebounce and enters UnorientedDebugAccessory.SRC and outputs VBUS
8. DTS DRP transitions from TryWaitDeb.SNK to AttachedDeb.SNK
   - DTS DRP sees pull-ups on both CC pins for tCCDebounce and detects VBUS and enters AttachedDeb.SNK
   - If orientation required, DTS DRP adjusts Rd on the non-CC communication pin as needed for orientation detection
9. If orientation supported, TS Source detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.
10. While the TS Source and DTS DRP are in the attached state:

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.
Microchip Ex. 1019, p. 215
Microchip v. Aptiv
IPR2024-00496

- If orientation is supported, DTS DRP determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
- TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
- DTS DRP monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.2. DTS Port to non-DAM TS Port Interoperability Behaviors

The following sub-sections describe the non-functional port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks, and DRPs that do not support DAM.

B.2.5.2.1. DTS Source to non-DAM TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS Sink.

1. DTS Source and TS Sink in the unattached state
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. Non-DAM TS Sink transitions from Unattached.SNK to AttachWait.SNK.
   - Non-DAM TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.
   - Non-DAM TS Sink continues to detect pull-ups on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)
4. While the DTS Source and non-DAM TS Sink are in their final state:
   - DTS Source adjusts Rp as needed for offered current
   - Non-DAM TS Sink may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK

B.2.5.2.2. DTS Source to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS DRP.

1. DTS Source and non-DAM TS DRP in the unattached state
   - Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

3. Non-DAM TS DRP transitions from Unattached.SNK to AttachWait.SNK.
   - Non-DAM TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.
   - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)
4. While the DTS Source and non-DAM TS DRP are in their final state:
   - DTS Source adjusts Rp as needed for offered current
   - Non-DAM TS DRP may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SRC

B.2.5.2.3. DTS Sink to non-DAM TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS Source.

1. Non-DAM TS Source and DTS Sink in the unattached state
2. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.
   - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS Source and DTS Sink are in their final state:
   - Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open

B.2.5.2.4. DTS Sink to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS DRP.

1. DTS Sink and non-DAM TS DRP in the unattached state
   - Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK
   - DTS Sink in UnattachedDeb.SNK
2. Non-DAM TS DRP transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS DRP detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

- Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)

3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS DRP and DTS Sink are in their final state:
   - Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK
   - DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pin go to SNK.Open

B.2.5.2.5. DTS DRP to non-DAM TS Sink Behavior

The DTS DRP to non-DAM TS Sink behavior follows the flow in Section B.2.5.2.1

B.2.5.2.6. DTS DRP to non-DAM TS DRP Behavior

The DTS DRP to non-DAM TS DRP behavior follows the flows in Section B.2.5.2.2 and Section B.2.5.2.4 depending on the role forced by the non-DAM TS DRP

B.2.5.2.7. DTS DRP to non-DAM TS Source Behavior

The following describes the behavior when a DTS DRP is connected to non-DAM TS Source.

1. DTS DRP and non-DAM TS Source in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - Non-DAM TS Source in Unattached.SRC
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK
3. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC
   - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
5. While the non-DAM TS Source and DTS DRP are in their final state:
   - Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS DRP monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SRC when both CC pin go to SNK.Open

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

B.2.5.2.8. DTS Sink to non-DAM TS Sink with Accessory Support Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM USB Type-C TS Sink with Accessory Support.

1. DTS Sink and non-DAM TS Sink with Accessory Support ("non-DAM TS Sink" for the remainder of this flow) in the unattached state
   - Non-DAM TS Sink alternates between Unattached.SNK and Unattached.Accessory
   - DTS Sink in UnattachedDeb.SNK
2. Non-DAM TS Sink transitions from Unattached.Accessory to AttachWait.Accessory
   - Non-DAM TS Sink detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.Accessory
   - Non-DAM TS Sink continues to detect pull-downs on both CC pins and enters USB Type-C Debug Accessory Mode
3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Sinks pull-ups on both CC pins and enters AttachWaitDeb.SNK
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS DRP and DTS Sink are in their final state:
   - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK
   - DTS Sink monitors both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open

B.2.6. Orientation Detection

Orientation detection is optional normative. A USB Type-C port supporting Debug Accessory Mode is not required to perform orientation detection. If orientation detection is required, this method shall be followed.

B.2.6.1. Orientation Detection using Rd and/or Rp Values

In this optional normative flow, the DTS shall always initiate an orientation detection sequence, independent of its role as Source, Sink, or DRP. This means that the TS must detect this orientation sequence and perform multiplexing to orient and connect the port signals to the proper channels as well as determine the proper CC pin for *USB-PD* communication.

B.2.6.1.1. Orientation Detection with DTS as a Source

When the DTS is presenting an Rp, it shall present asymmetric Rp values (Rp1/Rp2) on CC1/CC2 to indicate orientation to the TS. The DTS as a source shall indicate a weaker resistive value on CC2. Table B-2 shows the values of Rp resistance on each CC pin to indicate orientation and advertise the USB Type-C current available on VBUS. See Table 4-15 for the Rp resistance ranges.

Once the TS sink enters the DebugAccessory.SNK state, after the vRd on both CC pins is stable for tPDDebounce, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the *USB-PD* CC communication wire. The TS Sink cannot

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

perform *USB-PD* communication or connect any orientation-sensitive debug signals until orientation is determined.

B.2.6.1.2. Orientation Detection with DTS as a Sink

When the DTS is a sink, it shall follow a two-step approach.

1. The DTS sink shall present Rd/Rd on the CC pins of the debug accessory plug. This will put the system into debug accessory mode

2. Once the DTS sink enters AttachedDeb.SNK state, it shall present a resistance to GND of ≤ Ra on B5 (CC2)

The asymmetric signaling is detected by the TS Source in the UnorientedDebugAccessory.SRC state. Once Detected, the TS Source will move to the OrientedDebugAccessory.SRC. Once the TS source enters the OrientedDebugAccessory.SRC state, after the SRC.Ra level is detected on one of the CC pins, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the *USB-PD* CC communication wire. The TS Source cannot perform *USB-PD* communication or connect any orientation-sensitive debug signals until orientation is determined.

B.3. Security/Privacy Requirements:

Debug port(s) typically provide system access beyond the normal operation of USB hardware and protocol. Additional protection against unintended use is needed. The design must incorporate appropriate measures to prohibit unauthorized access or modification of the unit under test and to prevent exposure of private user data on the unit under test. The method of protection is not explicitly defined in this specification.

The vendor shall assert as part of USB compliance certification that:

- The device has met the requirement to protect the system's security and user's privacy in its vendor-specific implementation of the port, and

- The device requires the user to take an explicit action to authorize access to or modification of the unit.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.

C USB Type-C Digital Audio

This appendix is reserved for the future definition of the USB Type-C Digital Audio support.

Copyright © 2016 USB 3.0 Promoter Group. All rights reserved.