

# PCD Dressers for Chemical Mechanical Planarization with Uniform Polishing

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## Abstract:

Instead of attaching individual diamond grits to a metal substrate as all pad conditioners are made today, a revolutionary design by carving the structure out of a strong polycrystalline diamond (PCD) matrix. Such Advanced Diamond Disks (ADD) are manufactured by electro discharge machining (EDM) of PCD to form cutting pyramids of a specific size with a designed shape. ADD can produce a much higher density of pad asperities for polishing wafers at high efficiency and with high uniformity. This is a paradigm shift that low pressure CMP is not necessary to avoid damaging of delicate copper circuitry supported by ultra low dielectric constant material.

**Keywords:** CMP, Diamond dresser, Polycrystalline diamond, Pad conditioner

## 1. Chemical Mechanical Planarization

The semiconductor chips (e.g. ULSI) has been progressing by following the so-called Moore's Law. As a result, the number of transistor numbers on a CPU has been doubling about every 18 months since the Law was predicted in 1965. Due to the relentless miniaturization of transistors, the circuitry for the chip must be down sized continually. The line wide of the circuitry (node) is now encroaching upon the virus domain (10-100nm). In addition, more layers of circuitry must be laid down to meet the increasing demand of logic designs. In order to deposit layers for making nanometer-sized features, each layer must be extremely flat and smooth during the semiconductor fabrication. Consequently, chemical mechanical planarization (CMP) has been employed by the industry to manufacture semiconductor devices (Fig.1).

The CMP is accomplished by polishing the wafer with a polymer pad (e.g. polyurethane). The pad is mounted on a rotating platen with controlled speed. A slurry is introduced to the pad that will spread across the pad surface by spinning of the pad and by pushing around with both wafer and pad conditioner. The slurry contains nanometer (e.g. 100 nm) sized abrasive particles (e.g. ceria) that are dispersed in a chemical solution (e.g. hydrogen peroxide). During the polishing action, chemical reactants (e.g. copper oxide) from the surface of the circuitry will be abraded away by free moving abrasive particles suspended in the slurry.

During the CMP process, the polished debris must be removed periodically, otherwise, the pad top will be loaded with dirt known as glazing. In order to get rid of the accumulation of the removed materials, a diamond pad

conditioner is used to push the waste around and eventually discharge the debris along the pad periphery. In addition to the elimination of contaminants deposited on the pad top, pressure must be increased locally on the pad asperities to cause the abrasion at the contact points between wafer and pad. In order to create the pressurized points, the contact area must be reduced. Hence, the same diamond pad conditioner must groove the pad top to create asperities. The size and distribution of these asperities actually determine the efficiency of the polishing and the quality of the polished wafer (Fig.2).

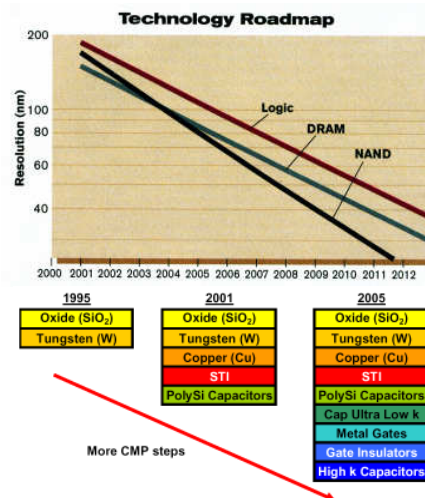


Fig. 1: The progression of Moore's Law for logic and memory devices of semiconductors with the increasing complexity of IC architecture along with the decreasing of the node size.

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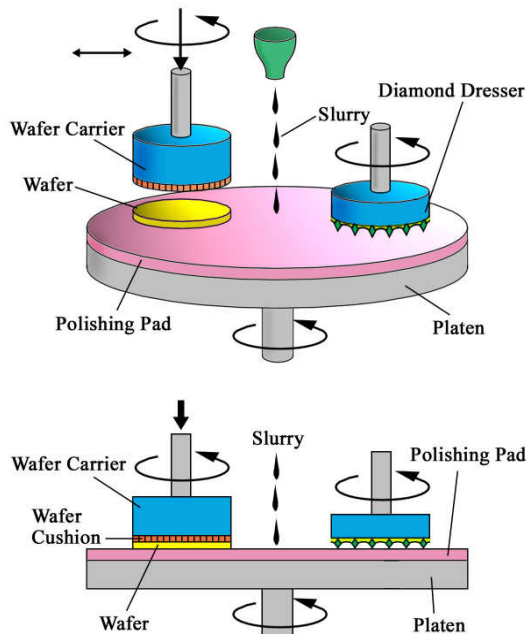


Fig. 2: The CMP layout includes a rotating pad, a feeding slurry, and a rotating pad conditioner.

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The CMP complexity will increase further with the introduction of 450 mm silicon wafers. The pizza-sized wafer will be loaded with virus sized (e.g. 45 nm) transistors. This scale difference of ten million times must be processed by CMP with precision and efficiency. Such a challenge awaits for the refinements of slurry, pad, and pad conditioner (Fig. 3).

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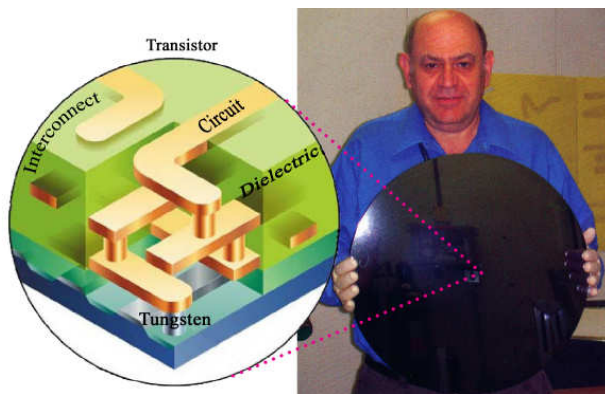


Fig. 3: The size of future 450 mm (16 inches) silicon wafer is 10 million times ( $10^7 \times$ ) larger than the node size (45 nm) of the transistors. In order to polish the soft copper layer buried in the delicate low-k dielectric matrix, the contact pressure between the IC and the tips of pad asperities for ECMP must be one order of magnitude lower than that for conventional CMP. Consequently, only pad conditioners that can generate very uniform pad asperities may be used.

In order to polish fragile wafers more and more gently, the pad asperities must be reduced. On the other hand, to prevent the polishing rate from declining, more contact points must be created. Consequently, the pad asperities need to be finer in size but more in number. However, the more delicate the polishing becomes, the higher risk for causing scratching on the wafer. In order to avoid this risk, the highest tips of all asperities must be fully leveled.

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Otherwise, the protrusion of a few “killer asperities” can ruin the polished wafer. The diamond tips on the current pad conditioners vary more than 50 microns in heights so they cannot avoid forming killer asperities on the pad.

## 2. The Diamond Orientation Problem

Conventional diamond disks are made by attaching already made diamond grits onto a stainless steel substrate. The process of addition cannot alter the shape of diamond, nor adjust the height of grits. As a result, the pad is dressed by irregular shaped diamond at variable depths. Such a chaotic dressing cannot form uniform asperities (Fig. 4).

The orientation of diamond grit has a dramatic effect in plowing the pad, a sharp point of diamond can do more cutting than pushing on the plastic pad. On the other hand, a dull diamond tip may press more on the pad than removing material. Hence, the grooves generated by a conventional diamond pad conditioner are all different, not only in size, but also in geometry. All such variations can cause polishing anomalies of the wafer (Fig. 5).

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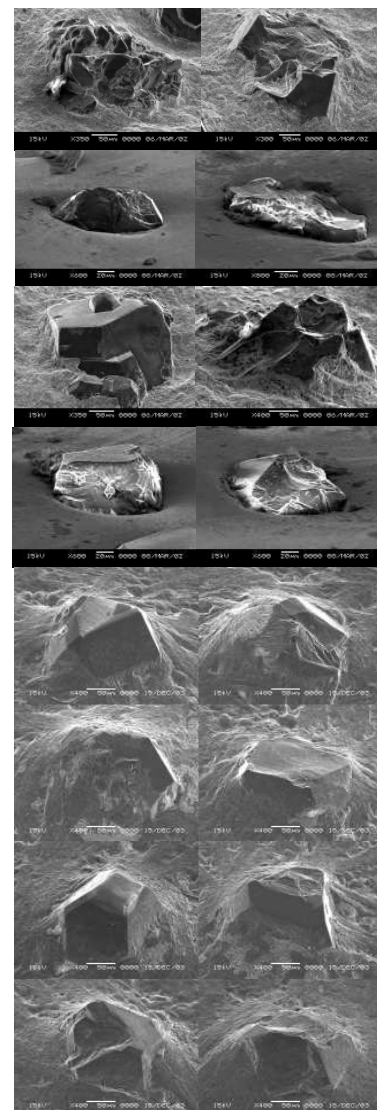


Fig. 4: Conventional diamond pad conditioners contain diamond grits with different shapes and every crystal has a unique orientation. The top rows show electroplated diamond grits; the bottom rows, brazed grits.

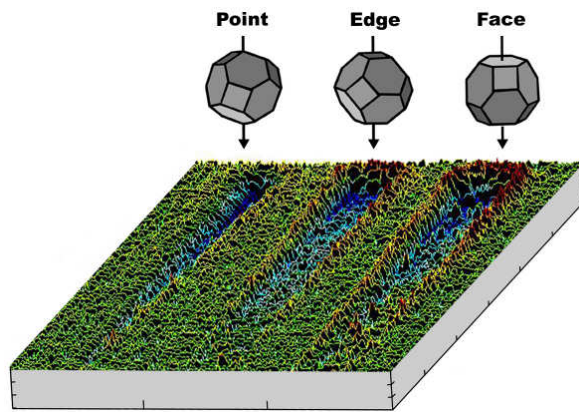


Fig. 5: The cutting grooves traversed by a descending diamond tip down to about 100 microns below the contact level. The diamond was oriented with the point (left), edge (middle) and face toward the pad. Note that with the increase of contact surface area during the cutting action, more and more plastic deformation of the pad was formed (data of Ming-Yi Tsai).

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### 3. Advanced Diamond Pad Conditioner

A revolutionary new design of diamond pad conditioner is now available, this advanced diamond disk (ADD) has identical cutting pyramids with tips extended to the same height. Consequently, ADD can dress pads to achieve unprecedented uniformity in asperities. The furrows are more evenly spaced, the grooves have similar shapes, and there are no killer asperities. All these unique features are needed to achieve uniform polishing of delicate wafers of the future (Fig. 6).

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Fig. 6: The commercial ADD samples for ECMP in the front and the state-of-the-art CMP pad conditioner DiaGrid® disks lying in the backside.

In order to improving the diamond tip leveling of a conventional diamond pad conditioner, smaller diamond grits must be used to reduce their spread in size distribution. However, smaller size diamond has a much lower

protrusion that can impair the flow of slurry. The narrow gaps between diamonds may also trap dirt, a potential cause of wafer defectively. The conventional pad conditioner can only select either fine diamond size or low crystal protrusion, but not both. In contrast, ADD can possess both attributes. In other words, the diamond tips can be leveled without sacrificing their protrusions.

Another great advantage of using ADD is that the cutting elements are formed, so they can be designed with structures, such as by forming terraces. In this way, the high level pyramids can cut into the pad while the cutting depth is gauged by the stopper of the lower terrace. In this way, not only the killer asperities are avoided, but also each asperity has the same length. Consequently, the polishing behavior can be controlled for each and every asperity.

One immediate application of ADD is to dress pads for polishing hard drives of computer memories. In this case, the pad conditioners are not fastened to a fixed handle, but they are encircled in a gear wheel that turns relative the pad on both sides (top and down). As the diamond becomes very small (e.g. 40 microns) for the pad conditioners, they tend to stick to the pad above and below. This problem can be solved by using ADD with tight tip spacing but with much higher tip protrusion. In this case, the “lotus effect” for perching water droplets is used to separate rotating polishing pads (Fig. 7).

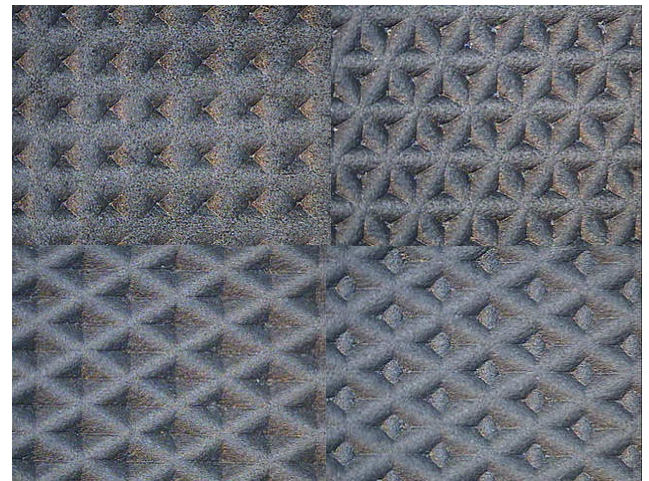


Fig. 7: The cutting tips of ADD can be tailor made in shape and in distribution. This flexibility makes ADD the unique pad conditioners for ECMP manufacture of future Moore’s Law semiconductors with node sizes of 45 nm, 32 nm, and 22 nm.

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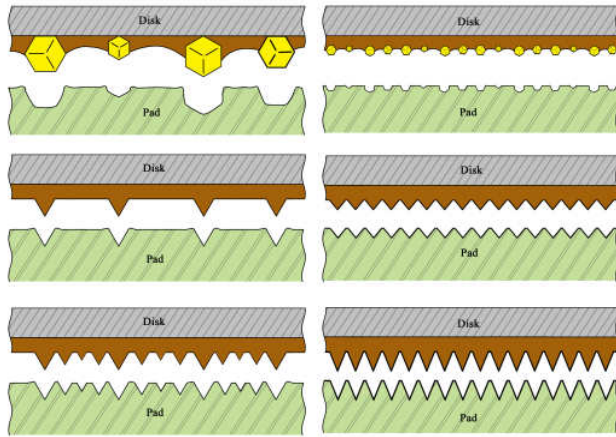


Fig. 8: With the current designs of pad conditioners, diamond tip heights vary significantly due to the differences of diamond size, shape and orientation (top diagrams). As a result, the dressed pad asperities will vary greatly in depth and in shape. In contrast, ADD has leveled diamond tips and identical shapes. So the dressed pads have much more uniform asperities (middle diagrams). In addition, the size and shape of ADD's cutting pyramids can be designed. Hence, the dressed pad asperities may have structured asperities to achieve special results of polishing.

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#### 4. The Versatile Design of ADD

ADD's surface can be tailor designed to form cutting elements of different sizes and shapes. They may be tailor made to exhibit a predetermined structure (Fig. 9).

A combination of sizes and shapes of cutting pyramids may be designed to occupy the same surface of ADD. For example, two set of cutting pyramids may be used to achieve opposite functions, one for cutting; and the other for stopping. In this case, the cut grooves on the pad are not only uniform in shape, but also they have a fixed depth (Fig. 10).

For the conventional application of ADD in CMP, cutting elements of simple pyramids are used. Such ADD can outperform conventional pad conditioners in dressing efficiency and service durability.

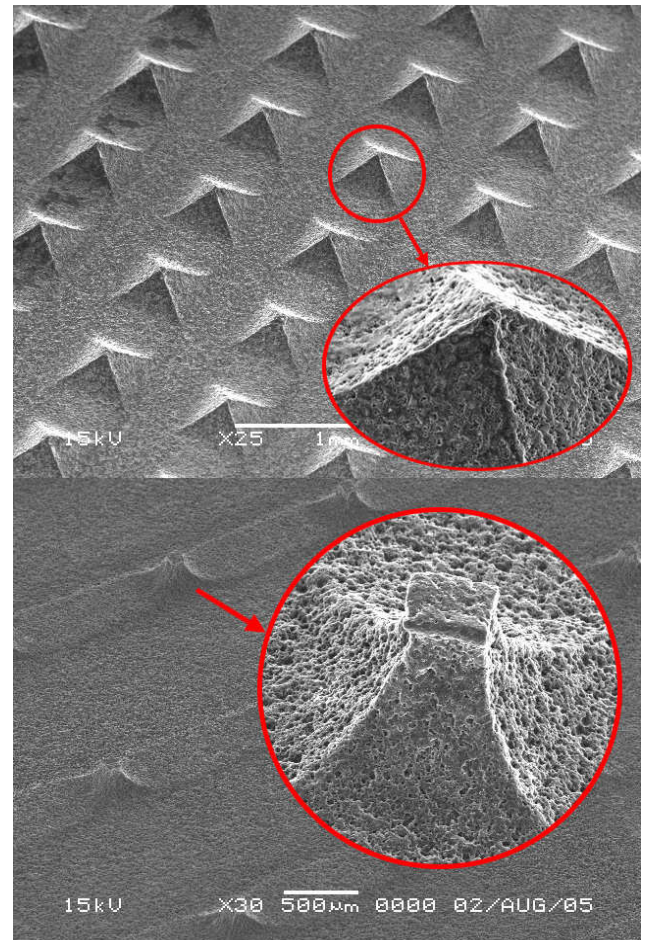


Fig. 9: ADD's cutting pyramids can be designed to suit specific applications.

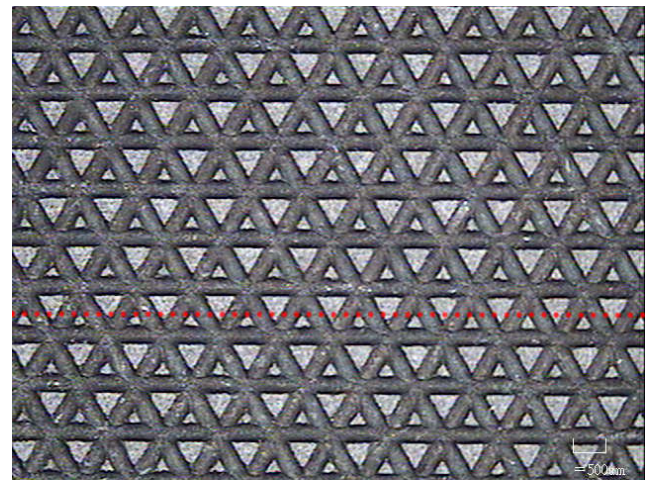


Fig. 10: A novel design of ADD that possesses sharp cutting edges and flat penetration stoppers in between, slurry moving tunnels are also created to facilitate the removal of cutting debris.

## 5. The Performance of ADD

The contrast between ADD and DiaGrid® pad conditioner is dramatic in the global view of optical microscopy, and in the detailed layout of the array as well as the profiling of the cutting tips as revealed below (Fig. 11).

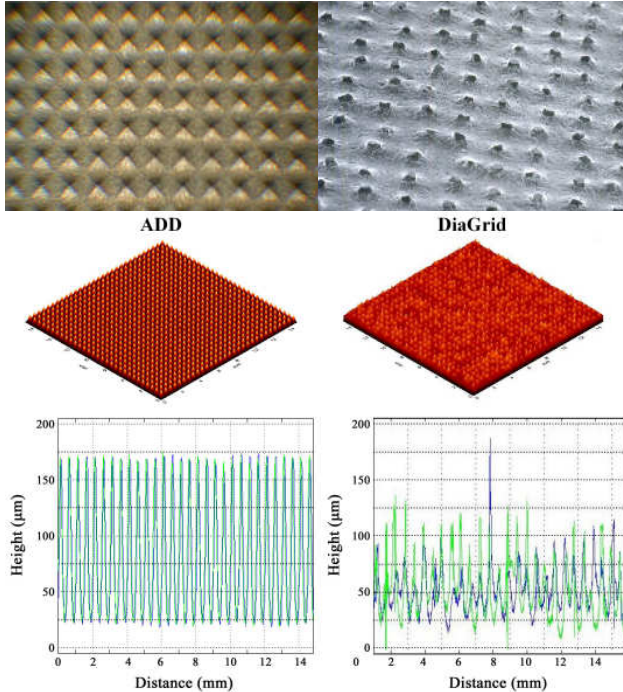


Fig. 11: The vivid comparison of the cutting tips between ADD and DiaGrid® pad conditioner confirms that the former is far superior than the latter in dressing the pad for making semiconductors with virus sized transistors.

The performance of pad conditioners can be measured by two most critical parameters, the longevity of the pad conditioner and the pad; and the effectiveness of the pad dressing. The longevity can be improved by leveling of cutting tips that increases the number of working crystals on the pad conditioner. The effectiveness of the pad dressing may be improved by the sharpness of the cutting tips, the sharper, the faster to create the density of pad asperity as required for polishing.

Due to the even loading of the pad and the uniformity of asperities, wafer polishing can be much more uniform. Moreover, because the polishing can only be achieved by the contact between wafer and pad, ADD with more polishing points generated on the pad may polish at a higher removal rate even if the individual polishing rate is low at each contact point. The low-pressure contact at each polishing point will also assure the uniformity of the polish performance (Fig. 12).

Due to the seriated feature of PCD surfaces and edges, ADD can cut pads cleaner with less tearing. Moreover, the pad dressed has a higher specific surface area than that dressed by a conventional pad conditioner. The more textured pad surface can trap more abrasive particles on asperities. Consequently, a higher polishing rate of wafer or a reduced usage of slurry may be achieved.

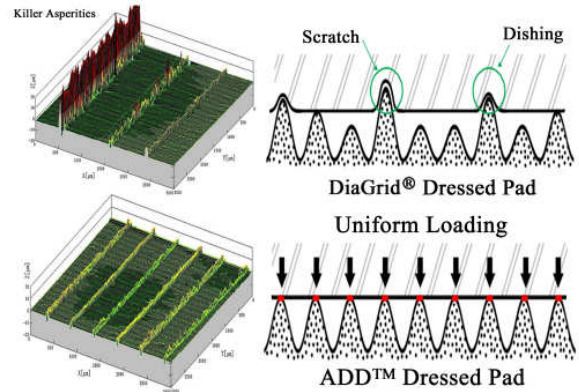


Fig. 12: The contrast of polishing behaviors between ADD and conventional pad conditioners. Note that ADD can achieve the same polishing efficiency with improved wafer quality. Note that ADD dressed pads do not contain “killer asperities” that may ruin the soft copper circuit, if not the layer of vulnerable dielectric layer.

## 6. The Advantages of ADD

The asperities may resemble waves with amplitudes as the height and frequency as the density. Hence, the pad may be dressed to exhibit various wave patterns with harmonic and noisy characteristics. The amplitude of asperities often determines the polishing rate of the wafer; and the frequency, the uniformity of the wafer.

Because ADD has all cutting pyramids leveled, it can create asperities with low amplitude and high frequency. As a result, the wafer can be polished uniformly at high removal rate. Moreover, because every cutting tip is used during dressing, ADD’s life will be much longer than conventional pad conditioners. The experiments confirmed that ADD can be extremely durable as demonstrated in the following figure.

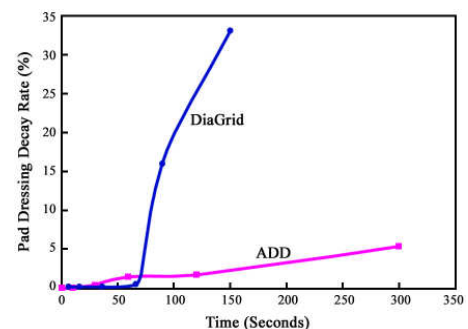


Fig. 13: The relative decay rates of pad dressing rates during an accelerated testing protocol. Note that DiaGrid showed a catastrophic failure after a certain time. Hence, ADD cutting pyramids can last much longer than conventional diamond pad conditioners. The ordinate shows the percentage decline of pad dressing rate. The abscissa shows the time for the pad conditioner to cut an aluminum plate as the means to accelerate the dulling process of cutting tips.

In summary, ADD has the potential to consume less pad to achieve higher polishing rates of wafers. In addition, with the further progression of Moore’s Law, ADD can be the enabler of future CMP for making devices with node sizes smaller than 65 nm.

As a result of the durability of ADD and its ability to minimize the pad wear, the number of wafers polished per installation of pad and pad conditioner combination will be much more. The machine down time saved due to the long ADD life can reduce the overall cost of ownership (CoO) significantly for the manufacture of complex semiconductors (Fig. 14).

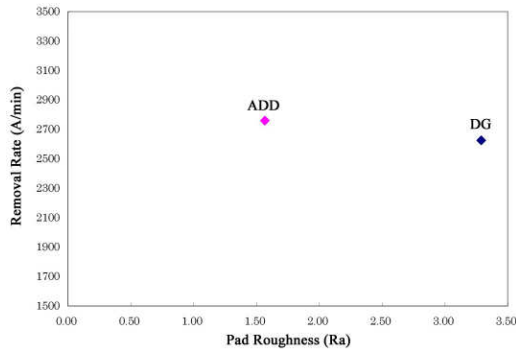


Fig. 14: ADD is uniquely capable to achieve the high polishing rate of wafers with the low dressing rate of pads. It is actually a pad savor for CMP manufacture of semiconductors.

## 7. The High Pressure CMP

The average contact pressure of asperities on the delicate wafer can be two orders of magnitude higher than the average pressure. Moreover, the contact pressure of “killer asperities” is much higher than the average contact pressure. Hence, low average pressure CMP is envisaged as the solution to avoid the damage of the wafer. However, ADD can form dense asperities without the “killer asperities.” Consequently, high average pressure CMP can be exercised to achieve fast polishing to boost the productivity of CMP.

The CMP pad is made of porous polyurethane. The pores are used to store slurry for polishing. With the trend of polishing ever delicate circuitry on IC wafers, the pores are getting smaller (e.g. 20 microns) and their volume fraction is reduced (e.g. 20 V%). Since the polishing is performed on the two dimensional surface, the longevity of the pad life is determined by the dressing rate. ADD can minimize the excessive cutting of the pad, hence, it is actually a pad saver (Fig. 15).

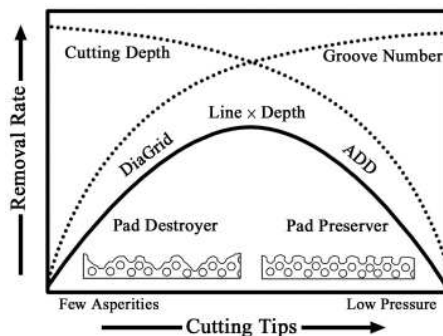


Fig. 15: The removal rate of the wafer is determined by the product of polishing asperities and their cutting depths. Large asperities is formed by excessive dressing. Small asperities can allow more polishing facse to be produced from the same pad.

The uniform dressing of pad can improve the CMP performance with a lower cost of ownership (CoO). ADD is designed to achieve both objectives for the future manufacture of semiconductor (Fig. 16).

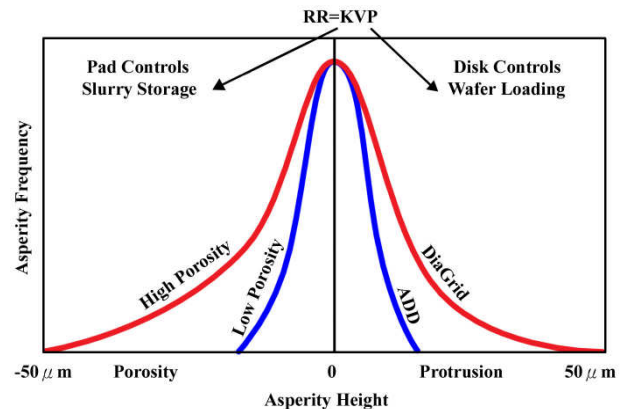


Fig. 16: The pressure distribution under wafer is determined by the uniformity of asperities' tip heights. ADD is uniquely capable to form dense, but uniform polishing points that can expedite the CMP process without causing damage.

As ADD can minimize the pressure distribution on the polishing contact (Fig 17), the necessity of electrolytic oxidation of copper before polishing may be eliminated. That means the conventional CMP can advance to make IC with 32 nm or smaller.

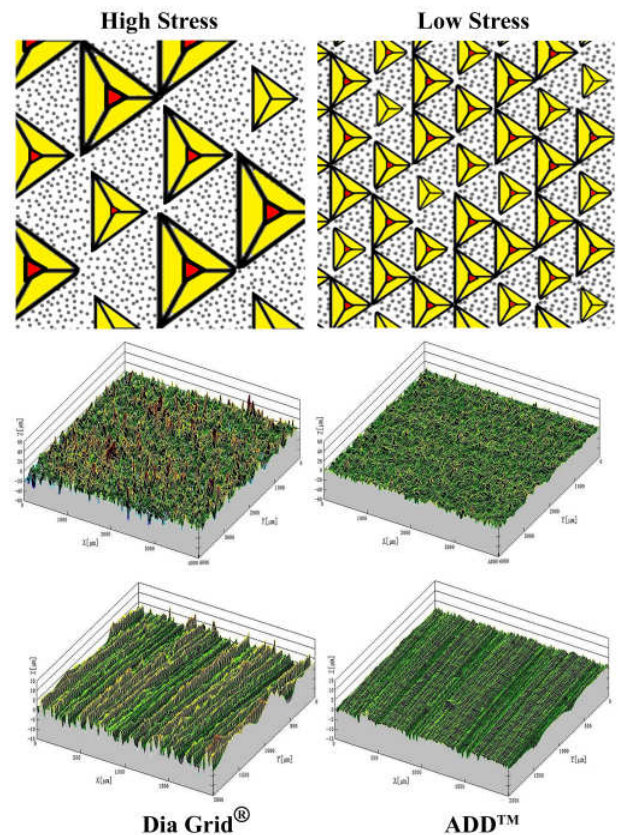


Fig. 17: The contrast of pad surfaces dressed by single crystal diamond grits and polycrystalline diamond pyramids. The latter can allow fast but uniform removal of excess copper materials on IC wafers.