

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Nichia Corp.,
Petitioner

v.

BX LED LLC,
Patent Owner

Case No. IPR2024-00542
Patent No. 8,567,988

Petition for *Inter Partes* Review

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LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 8,567,988
1002	File History of U.S. Patent No. 8,567,988
1003	Declaration of Dr. Nan Jokerst
1004	<i>Curriculum Vitae</i> of Dr. Nan Jokerst
1005	U.S. Patent App. Pub. No. 2005/0174753 (“Cao753”)
1006	U.S. Patent App. Pub. No. 2007/0075325 (“Baek”)
1007	U.S. Patent App. Pub. No. 2004/0256630 (“Cao630”)
1008	Patent Owner’s Responsive Claim Construction Brief, Dkt. 28, dated Feb. 17, 2023, in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.) (<i>excerpted</i>)
1009	Patent Owner’s Sur-Reply Claim Construction Brief, Dkt. 32, dated Mar. 24, 2023, in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.) (<i>excerpted</i>)
1010	Declaration of John K. Roberts in Support of Patent Owner’s Responsive Claim Construction Brief, Dkt. 28-1, dated Feb. 17, 2023, in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.) (<i>excerpted</i>)
1011	U.S. Patent No. 6,969,253 to Cao (“Cao253”)
1012	Graf, Rudolf, <u>Modern Dictionary of Electronics</u> , 7th Ed. (1999) (<i>excerpted</i>)
1013	Zukauskas, Arturas, <u>Introduction to Solid-State Lighting</u> , John Wiley & Sons, Inc. (2002) (<i>excerpted</i>)
1014	U.S. Patent App. Pub. No. 2004/0119975 to Cao (“Cao975”)
1015	U.S. Patent App. Pub. No. 2008/0055901 to Sanpei (“Sanpei”)

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1016	Thomas, N., <u>High Reflectivity of Silver Extended Down to 200 NM</u> , <i>Optical Interference Coatings</i> , OSA Technical Digest Series, Optica Publishing Group (2001)
1017	Bartek, M., <u>Silver-based reflective coatings for micromachined optical filters</u> , J. Micromech. Microeng. 9 (1999)
1018	Pecht, Michael, <u>Electronic Packaging: Materials and Their Properties</u> , CRC Press (1999) (<i>excerpted</i>)
1019	Fink, Donald, <u>Standard Handbook for Electrical Engineers</u> , 14th Ed., McGraw-Hill Book Co. (2000) (<i>excerpted</i>)
1020	U.S. Patent App. Pub. No. 2005/0023538 to Ishii (“Ishii”)
1021	U.S. Patent App. Pub. No. 2004/0065894 to Hashimoto (“Hashimoto”)
1022	Fischer, T., <u>Materials Science for Engineering Students</u> , Academic Press (2009) (<i>excerpted</i>)
1023	Infringement Contentions in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (<i>excerpted</i>)
1024	Bridgelux’s Opening Claim Construction Brief in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (<i>excerpted</i>)
1025	Bridgelux’s Reply Claim Construction Brief in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (<i>excerpted</i>)
1026	Everlight’s Responsive Claim Construction Brief in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (<i>excerpted</i>)

Exhibit	Description
1027	Ohring, Milton, <u>The Materials Science of Thin Films</u> , Academic Press (1992) (<i>excerpted</i>)
1028	Amended Claim Construction Order in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.)

LISTING OF CLAIMS

Element	Claim Language
Claim 1	
1[pre]	A light emitting diode (LED) apparatus comprising:
1[a]	a metal substrate having a reflective surface; and
1[b]	a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path and
1[c]	at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and
1[d]	an electrical path formed by connecting the LED chips in a chip to chip fashion.
Claim 2	
2	The apparatus of claim 1, wherein the reflective surface comprises polished aluminum.
Claim 3	
3	The apparatus of claim 1, wherein the reflective surface comprises silver plating.
Claim 4	
4	The apparatus of claim 1, wherein the reflective surface has a reflectivity of 70% or greater.
Claim 5	
5	The apparatus of claim 1, wherein the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater.
Claim 6	
6	The apparatus of claim 1, wherein the plurality of LED chips provide separate thermal and electrical paths.
Claim 7	
7	The apparatus of claim 1 wherein the plurality of LED chips have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface.
Claim 8	
8	The apparatus of claim 1, wherein the metal substrate is mounted directly to a heat sink.

Element	Claim Language
Claim 9	
9	The apparatus of claim 1, wherein the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface.

Nichia Corporation (“Petitioner”) requests *inter partes* review of claims 1-9 of U.S. Patent No. 8,567,988 (EX1001, the “’988 patent”), assigned to BX LED LLC (“Patent Owner”). There is a reasonable likelihood Petitioner will prevail on at least one challenged claim.

I. Introduction

The ’988 patent discloses and claims simple concepts that were well known in the LED packaging field at the time of the patent’s filing in September 2008. The focus of the claims is directly mounting well-known, conventional LED chips to a reflective surface of a metal substrate and wiring the chips together to improve light efficiency and heat dissipation. But such an LED package construction pre-dated the ’988 patent’s filing.

The prior art in this Petition already addressed the same problems in the same way—with the same LED package construction—rendering the challenged claims anticipated and/or obvious. For example, two patent application publications from an inventor named Cao (“*Cao753*” and “*Cao630*”) were published years before the ’988 patent’s filing. These publications have strikingly similar figures and disclosures to the ’988 patent and disclose the very same claimed concepts—including chip-to-chip wire-bonded LED chips directly mounted to a reflective surface of a metal substrate resulting in a light-reflecting-and-heat-efficient LED package. Similarly, a patent application publication to *Baek* also discloses the same

claimed concepts and renders obvious the challenged claims, both alone and when combined with Cao630.

As explained below and in the declaration of Dr. Jokerst, there is nothing inventive about the challenged claims. The Board should institute this petition and cancel the challenged claims.

II. Mandatory Notices (37 C.F.R. §42.8)

A. Real Parties in Interest (37 C.F.R. §42.8(b)(1))

Nichia Corporation is the sole real party in interest.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The '988 patent is currently being asserted by Patent Owner in *BX LED LLC v. Current Lighting Solutions, LLC*, No. 6:24-cv-00095 (W.D. Tex., filed Feb. 19, 2024) and *BX LED LLC v. Keystone Technologies, LLC*, No. 3:23-cv-02862 (N.D. Tex., filed Dec. 27, 2023).

The '988 patent was also asserted by Patent Owner in *BX LED LLC v. Lowe's Companies, Inc.*, No. 6:23-cv-00451 (W.D. Tex., filed June 13, 2023). While the case remains pending, on February 15, 2024, the parties jointly moved to stay the case because they had “reached an agreement in principle that would resolve all claims and defenses,” which stay was granted by the Court pending finalizing settlement.

The '988 patent was also previously asserted by Patent Owner or a prior assignee in cases that have been voluntarily dismissed: (i) *Everlight Electronics Co., Ltd. v. Bridgelux, Inc.*, No. 4:17-cv-03363 (N.D. Cal., filed June 10, 2017; dismissed

Dec. 14, 2018); (ii) *BX LED LLC v. Wayfair LLC*, No. 6:22-cv-00446 (W.D. Tex., filed May 2, 2022; dismissed Feb. 27, 2023); (iii) *BX LED LLC v. Walmart Inc.*, No. 6:22-cv-00445 (W.D. Tex., filed May 2, 2022; dismissed Aug. 31, 2023); (iv) *BX LED LLC v. Home Depot USA, Inc.*, No. 6:22-cv-00444 (W.D. Tex., filed May 2, 2022; dismissed Dec. 22, 2022); and (v) *BX LED LLC v. RAB Lighting Inc.*, No. 3:23-cv-01323 (N.D. Tex., filed June 13, 2023; dismissed Sept. 1, 2023).

The '988 patent was previously subject to a petition for *inter partes* review, *Everlight Electronics Co., Ltd. v. Bridgelux, Inc.*, IPR2018-01483 (filed July 31, 2018), which was terminated prior to an institution decision (Paper 10, Dec. 10, 2018).

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3)-(4))

Petitioner designates the following lead and back-up counsel:

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III. Requirements for *Inter Partes* Review (37 C.F.R. §42.104)

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies the '988 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR challenging the claims on the identified grounds.

B. Identification of Challenge (37 C.F.R. §42.104(b)(1)-(2)) and Relief Requested (37 C.F.R. §42.22(a)(1))

Petitioner requests the Board institute IPR because the challenged claims are anticipated and/or obvious under pre-AIA 35 U.S.C. §§102 and 103 based on the following grounds:

Ground	Prior Art	Basis	Claims
1	U.S. Patent App. Pub. No. 2005/0174753 ("Cao753")	§102	1, 4-9

Ground	Prior Art	Basis	Claims
2	Cao753	§103	1, 4-9
3	Cao753 alone or in view of U.S. Patent App. Pub. No. 2004/0256630 (“Cao630”)	§103	2-4
4	U.S. Patent App. Pub. No. 2007/0075325 (“Baek”) alone or in view of Cao630	§103	1-9

IV. Relevant Information Concerning the Contested Patent

A. ’988 Patent Overview

The ’988 patent “relates generally to light emitting diodes, and more particularly, to an efficient LED array.” EX1001, 1:6-7. It was filed September 29, 2008, and claims no earlier priority. *Id.*, Cover Page.

Per the patent, prior art devices often had multiple LED chips mounted closely together on a ceramic substrate, which could cause chips to “interfere with each other and result in reduced light output.” *Id.*, 1:33-36. Additionally, because “an LED chip may have electrical contacts on both top and bottom surfaces,” both heat and electricity could pass through to the substrate, causing “thermal and electrical paths that come in contact with each other.” *Id.*, 1:37-42. As a result, ceramic substrates were used to provide “electrical insulating properties while allowing some heat to pass,” but this arrangement “doesn’t provide a very efficient thermal path” and could reduce light output. *Id.*, 1:42-46.

The patent states that one way to improve heat dissipation was to mount the ceramic substrate to an “aluminum heat spreader, which i[n] turn is mounted to an additional heat sink.” *Id.*, 1:46-49. However, the patent explains this “is costly and results in more complicated manufacture.” *Id.*, 1:49-50.

Thus, per the patent, there was a need “for improvements in LED devices to increase light output, provide efficient heat dissipation, and simplify manufacture.” *Id.*, 1:51-53.

The patent purports to provide these improvements by disclosing an LED apparatus with “a metal substrate having a reflective surface, and a plurality of LED chips mounted directly to the reflective surface of the metal substrate to allow for thermal dissipation, and wherein at least a portion of the LED chips are spaced apart from each other to allow light to reflect from a portion of the reflective surface that is located between the portion of the LED chips.” *Id.*, 1:57-64. Figure 3¹ generally illustrates this arrangement:

¹ Unless otherwise noted, all emphasis and coloring has been added and case citations have been cleaned up.

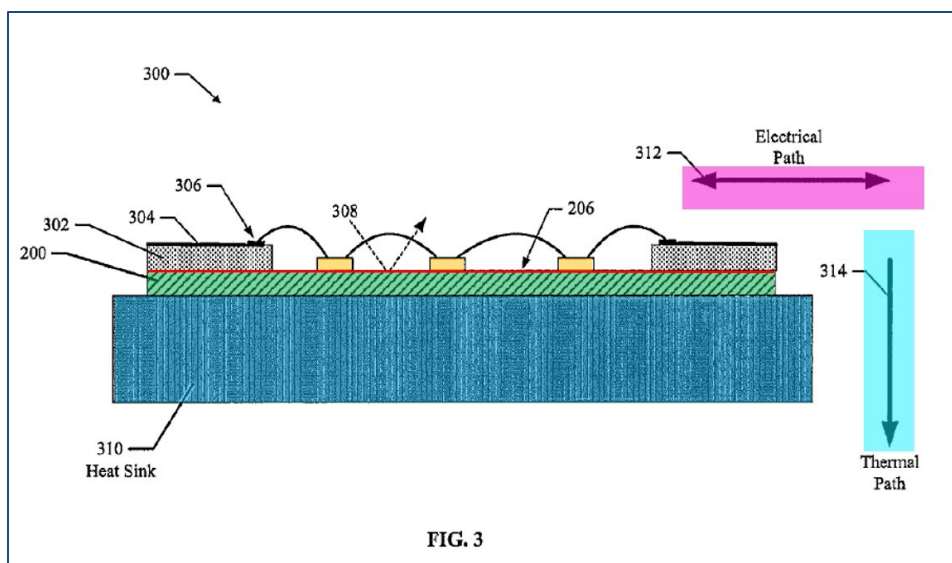


Figure 3 shows LED array 200 with **metal substrate 204** having a **reflective surface 206** whereby “**LED chips (i.e., LED 100)** [are] mounted directly to the **reflective surface 206** at a pre-determined spacing to expose regions of the reflective surface to allow light to reflect from the reflective surface located between the LED chips as illustrated at 308.”² *Id.*, 5:30-37; *see also id.*, 4:60-5:29, FIG. 2 (top view of LED array 200). The patent states that the reflective surface “may be formed from any suitable material and formed upon the substrate 204 in any suitable way,” and provides examples, *e.g.*, an aluminum substrate with a bare or polished aluminum reflective surface, or silver plating. *Id.*, 4:60-5:2. It further states that, in

² Metal substrate 204 and LED chips 100 are labeled in Figure 2 (top view) but unlabeled in Figure 3 (side view). EX1001, 4:60-5:62; FIGs. 2-3.

certain aspects, the reflective surface can have a “reflectivity index of 70% or greater,” *id.*, 5:2-3, *i.e.*, inherent for the disclosed metals such as silver or aluminum in the visible spectrum, *see* EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1016, 3, FIG. 1; EX1017, 162, FIG. 1.

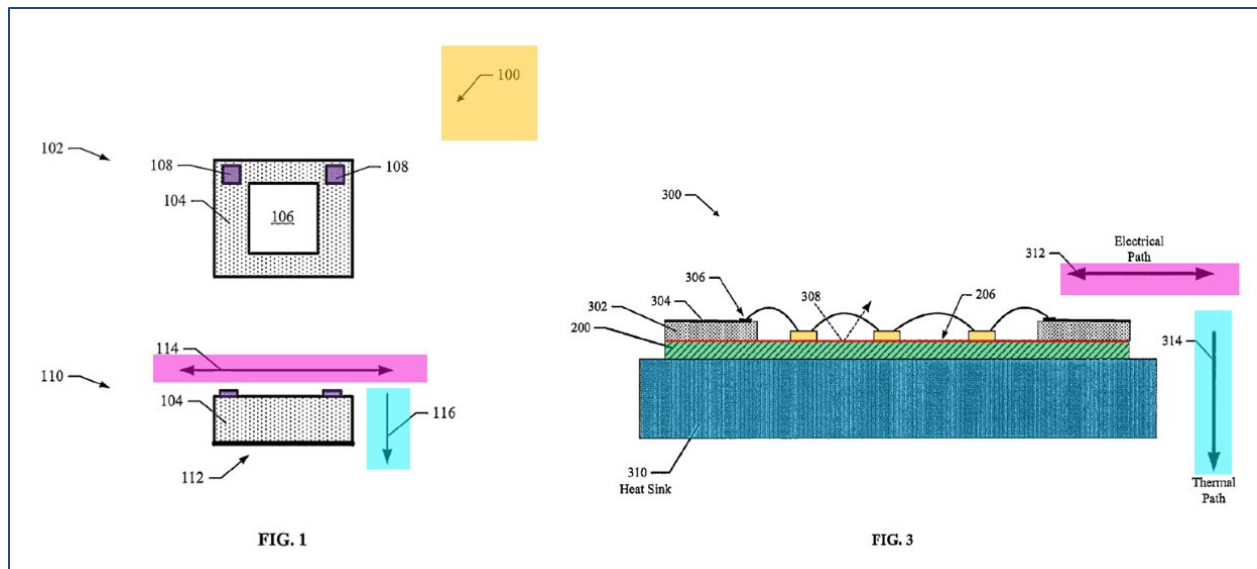
The patent explains that the LED array is “mounted directly to the **heat sink 310** without any dielectric insulation,” which heat sink “comprises any suitable material” and “provides for efficient transfer of heat from the metal substrate of the LED array 200 to the heat sink 310.” EX1001, 5:46-51.

According to the patent, because the LED chips are “mounted directly” to the substrate “without the need for an insulating dielectric,” which is in turn mounted directly to the heat sink, “an **efficient thermal path** is formed as illustrated at 314,” (vertical arrow in Figure 3), thereby allowing heat generated from the LED chips to be dissipated through the metal substrate into the heat sink “thereby reducing the degrading effects of heat on light output.” *Id.*, 5:51-62, 4:37-53. The patent further explains that the LED chips are connected with bonding wires “in a chip to chip fashion so that power may be applie[d] to all chips in the LED array,” resulting in an **electrical path** being formed as shown at 312 (horizontal arrow in Figure 3). *Id.*, 5:38-45.

The patent provides further implementation details. For example, it explains that “any suitable adhesive” may be used to mount the LED chips to the substrate

“without the need for an insulating dielectric.” *Id.*, 4:37-59. This is the only method disclosed to mount the LED to the substrate. *See generally id.* The patent also states that, in some aspects, the spacing between the LED chips is 0.5 millimeters or more, and that appropriate spacing exposes regions of the reflective surface between the chips and increases light output. *Id.*, 5:16-26.

The patent utilizes a typical wire-bonded **LED chip 100** known in the art, depicted in more detail in Figure 1 (below left), with “**electrical contacts 108** that are used to apply power” and “wires that carry an electrical signal to provide power are bonded to the contacts 108” (such wire-bonding is shown in Figure 3, above). *Id.*, 4:15-65, 1:9-32; *see also* §V.B.5 (discussing conventional wired-bonded LED chips). Per the patent, this LED chip design—with wire-bonded electrical contacts 108 and bottom mounting surface 112—can be “mounted directly to a metal substrate” and results in an “**efficient thermal path 116**” (downward arrow in Figure 1) and a separate **electrical path 114** (horizontal arrow in Figure 1). EX1001, 4:37-65. Similar **thermal path 314** and **electrical path 312** are depicted in LED array apparatus 300 in Figure 3 (below right). *Id.*, 5:30-62.



B. Person of Ordinary Skill in the Art

Several factors may be considered in determining the qualifications of a person of ordinary skill in the art (“POSA”). M.P.E.P. §2141.03. Here, the level of skill is apparent from the cited art. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner submits that a POSA would have had at least a bachelor’s degree in electrical engineering, materials science, or a related field, and three years’ experience in the field of LED package design, including optical design and thermal management. EX1003 ¶¶24-27. This description is approximate—a higher education or skill level might make up for less experience, and vice-versa. EX1003

¶26. Petitioner's expert, Dr. Jokerst, was at least a POSA as of the '988 patent's priority date, September 29, 2008. EX1003 ¶¶5-12, 27; EX1004.³

C. Claim Construction (37 C.F.R. §42.104(b)(3))

This Petition construes terms consistent with the understanding a POSA would have had at the time of the invention, in view of the evidence of record (including the intrinsic record and any extrinsic evidence). *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005). Only terms subject to a legitimate dispute relevant to the invalidity issues in this IPR need to be construed here. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

As shown herein, the prior art anticipates and renders obvious the challenged claims under any reasonable construction. Any implicit constructions derived from Petitioner's analysis are for the purposes of this IPR only, and may be based in-part on Patent Owner's infringement allegations and/or the positions Patent Owner and the prior assignee took during district court litigation.

³ Dr. Jokerst is an expert in optoelectronics, including LEDs and LED packaging. EX1003 ¶¶5-12; EX1004 (CV).

More particularly, Petitioner notes one previous claim-construction briefing involving Patent Owner. EX1008; EX1009. Patent Owner asserted:

Term (claims 1-9)	Patent Owner’s Proposed Construction
“efficient thermal path”	Plain and ordinary meaning – no need for construction. Alternatively, “the path for heat dissipation created by mounting an LED directly to a substrate with high thermal conductivity without intervening insulating materials”
“an electrical path formed by connecting the LED chips in a chip to chip fashion”	Plain and ordinary meaning

EX1008, 18-22; EX1009, 12-15; EX1010 ¶¶68-79.

The magistrate judge construed “efficient thermal path” to have its “Plain and Ordinary Meaning,” and the “electrical path...” term to have its “Plain and Ordinary Meaning, which does not include a connection of the chip through metal wires to the metal substrate.” EX1028, 4-5.

Petitioner also notes one previous claim-construction briefing involving the prior assignee (and original patent owner). EX1024; EX1025; EX1026. The then patent owner asserted:

Term	Prior Patent Owner's Proposed Construction
“mounted directly to the reflective surface” (claims 1-9)	“mounted/mounting directly to the reflective surface by adhesive or other means with no intervening elements present”

EX1024, 9-11; *see also* 3 n.2 (explaining patent family); EX1025, 6-9 (prior patent owner's reply brief); EX1026, 6-10 (accused infringer's response brief).

Petitioner does not necessarily agree with the prior proposed constructions or the district court's construction, but for purposes of this IPR, Petitioner relies—in certain instances—on alternative claim constructions and demonstrates how the prior art anticipates and/or renders obvious the challenged claims, regardless of the particular construction.

For example, Petitioner explains below how the prior art discloses the limitation, “the plurality of LED chips are *mounted directly to* the reflective surface...” regardless of whether “mounted directly to...” is found to (i) allow for the use of an adhesive (or a “suitable adhesive”) where no other intervening materials are present, *e.g.*, an insulating dielectric (which Petitioner understands to be Patent Owner's and the prior assignee's position and as the '988 patent specification seemingly indicates for wire-bonded LED chips) or (ii) not allow for any adhesive or intervening material (given other portions of the specification and file history).

On one hand, the patent discloses that “*any suitable adhesive* may be used *to* mount the LED chip 100 to the substrate” and mounting the LED chip “*directly to* a metal substrate without the need for an *insulating* dielectric.” EX1001, 4:37-53. Adhesives are the only way the patent discloses to mount the LED chip to the substrate. *See generally id.* Also, during prosecution, the applicant distinguished a machine translation of the prior-art “Yamada” reference based on “direct mounting” and that “Yamada” had “intervening *insulating* materials.” EX1002, 278-284.

On the other hand, the patent describes that elements are “directly on” one another where “there are no intervening elements present.” EX1001, 3:26-36. And, during prosecution, the applicant “noted that the term ‘directly’ is defined as excluding any intervening elements (between the plurality of LED chips and the surface of metal substrate), *cf.* ... application paragraph [0019].”⁴ EX1002, 280.

⁴ Application paragraph [0019] is 3:26-36 in the ’988 patent. EX1002, 7-8; EX1001, 3:26-36.

V. The Specific Grounds of Unpatentability

As evidenced by the prior art and Dr. Jokerst's declaration, there was nothing new or novel about the inventions claimed in the '988 patent.

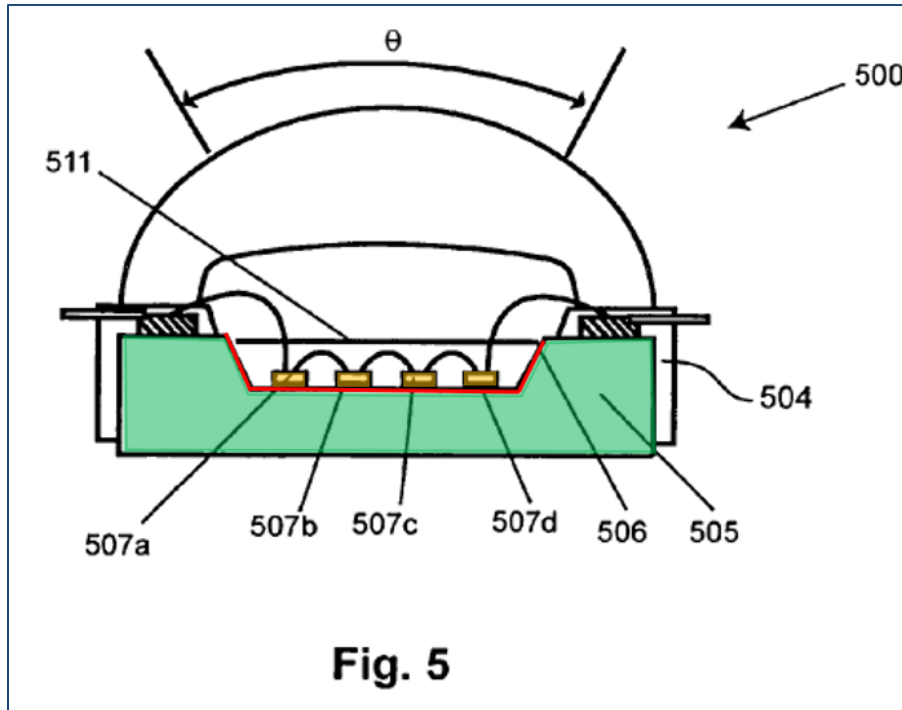
A. Exemplary Prior Art and State of the Art

The below provides an overview of certain exemplary prior art; additional such art is discussed in Sections V.B-E.

1. Cao753

Cao753 was filed February 6, 2004 and published August 11, 2005. EX1005, Cover Page. It is prior art under pre-AIA 35 U.S.C. §102(b).

Cao753 is directed toward a mining light with a semiconductor light source. EX1005, [Abstract]. Figure 5 depicts LED module 500 comprising **metal substrate (primary heat sink) 505** that may be a highly reflective metal such as silver or aluminum and includes a well 506 with a **surface** on which an array of **LED chips 507a-d** are directly mounted and "wired in series...." *Id.*, [0020], [0023], [0027]-[0028], [0034].



Cao753 discloses that LED chips 507a-d can be mounted to the primary heat sink 505 “by use of heat conductive or light reflective adhesive or other mounting means.” *Id.*, [0020], [0024] (same), [0028] (example adhesives). Cao753 further discloses various mounting means, including being “mounted directly on a heat sink,” *id.*, [0023], [0034], as well as mechanical fixation, brazing, welding, or other methods, *id.*, [0028].

Cao753 discloses that in embodiments with multiple LED chips (like Figure 5), “[t]he spacing between chips can be adjusted from zero to more than 1 mm, depending on the application requirements.” *Id.*, [0023]. Cao753 also explains that the heat sink can be “a single material,” and provides examples of heat sink materials including various reflective metals such as copper, aluminum, and silver, among

other materials “with adequate heat conductance and/or dissipation properties.” *Id.*, [0027].

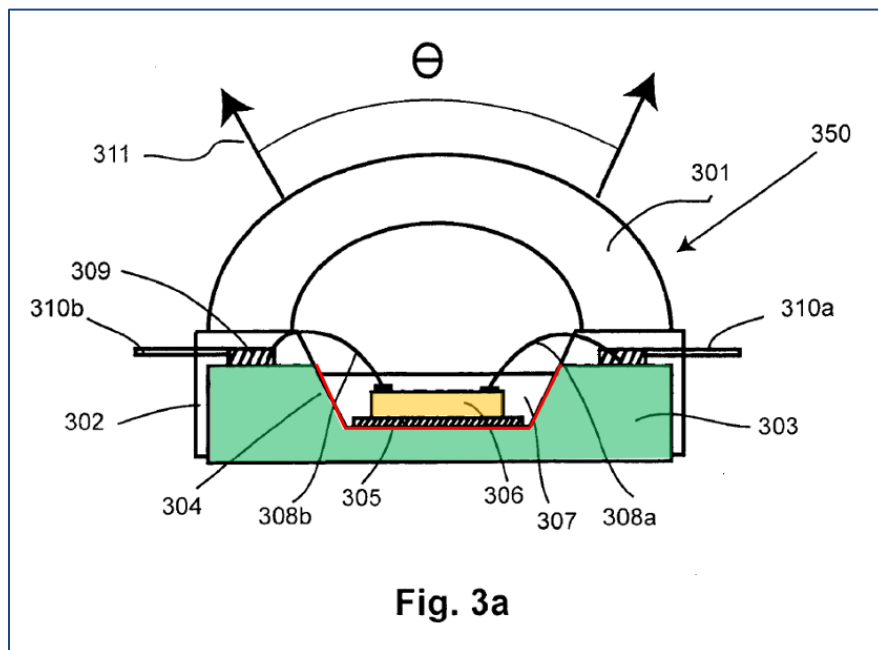
Cao753 further discloses the primary heat sink, in turn, “can be attached to a **secondary heat sink** if desired, such as[] by use of a heat conductive and/or electrically insulative adhesive, welding, brazing, soldering or mechanical fixation.” *Id.*, [0024] (secondary heat sink not depicted in the figures); cl. 1 (secondary heat sink “directly” attached to primary heat sink and “in heat conductance with each other”).

Lastly, Cao753 discloses that, in certain cases when a well is included, “all of the light emitted from the chip can be reflected back in the light exit direction for highest light output” and that “[t]he well may also include a reflective coating or polished surface.” *Id.*, [0019].

2. Cao630

Cao630 was filed February 5, 2004 and published December 23, 2004. EX1007, Cover Page. It is prior art under pre-AIA §102(b). The sole inventor of Cao630 is the lead inventor of Cao753. Cao630 and Cao753 are not formally related, but are both directed to LED light sources to illuminate spaces and have highly similar specifications and figures (*e.g.*, Cao630’s Figs. 3a and 3b are similar to Cao753’s Figs. 4 and 5). EX1003 ¶¶78-90.

Cao630 is directed toward an illuminating light with at least one semiconductor chip directly mounted to a primary heat sink, which is in turn mounted to a secondary heat sink to dissipate heat to the atmosphere. EX1007, Abstract. Cao630's Figure 3a depicts a high power LED package 350 using either a single wire-bonded LED chip 306 (as pictured) or a chip array mounted to metal substrate (primary heat sink) 303 including a well having a reflective surface that “may be polished to be light reflective, or may be covered, plated, painted or bonded with a light-reflective coating such as Al, Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastic and others to reflect light and thereby improve light source efficiency.” *Id.*, [0020], [0014].



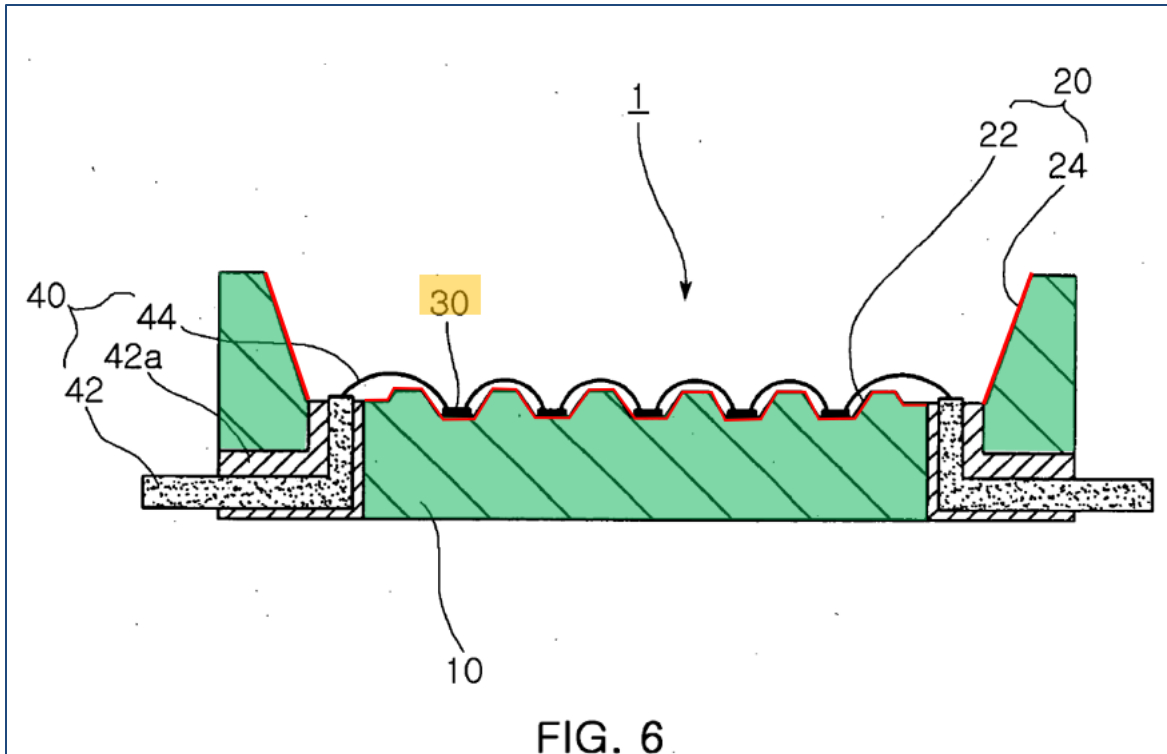
Cao630 shares other common disclosures with Cao753. For example, Cao630 discloses that mounting of the LED chips may be achieved by various methods,

including direct mount, mechanical fixation, brazing, welding, use of an adhesive or other methods, and notes that use of a heat conductive adhesive may be desired. *Id.*, [0015], [0020]. Cao630 also similarly discloses that the heat sink can be “a single material or a combination of two different kinds of materials,” and provides examples of heat sink materials including various reflective metals such as copper, aluminum, and silver, among other materials “with adequate heat conductance and/or dissipation properties.” *Id.*, [0014].

3. Baek

Baek was filed October 3, 2006 and published April 5, 2007. EX1006, Cover Page. It is prior art under pre-AIA 35 U.S.C. §102(b).

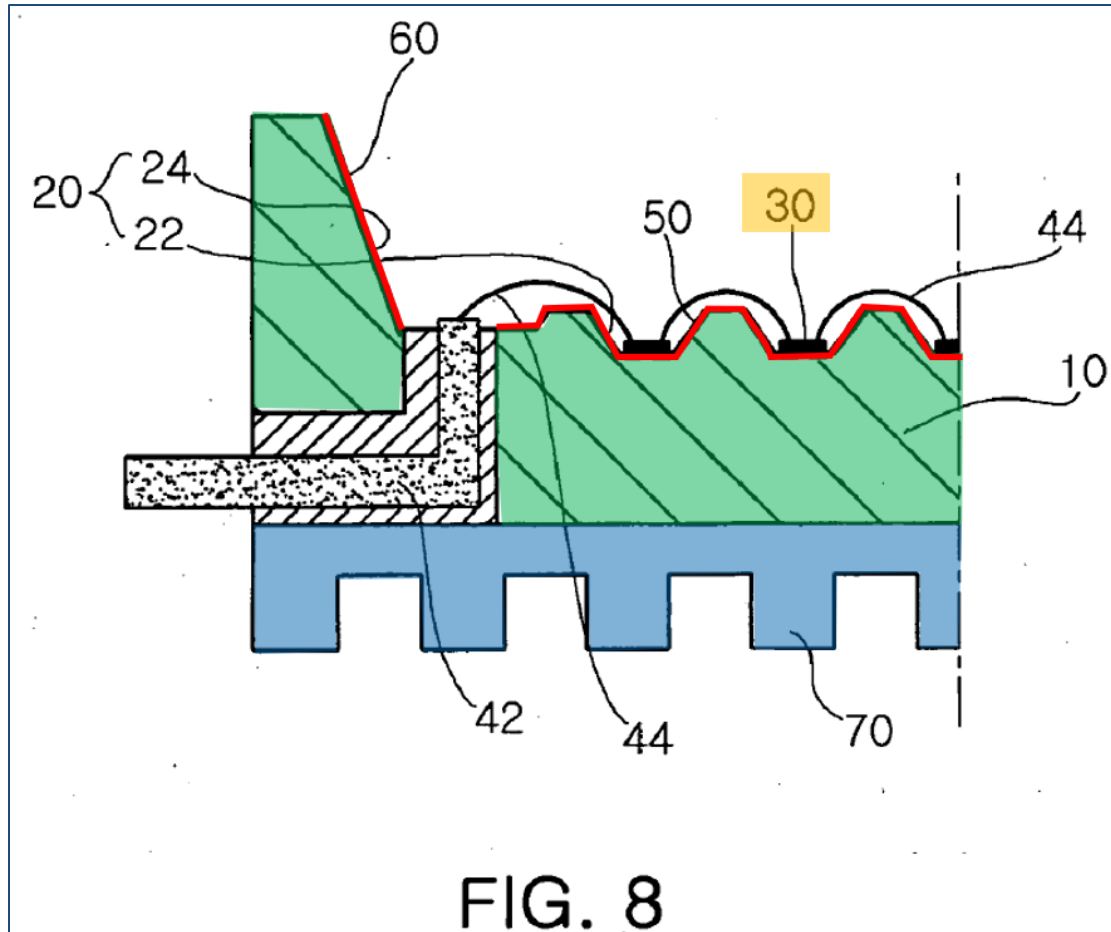
Baek discloses a high power LED package having excellent light efficiency and heat dissipating characteristics. EX1006, Abstract. Baek discloses an LED package with a base member, a set of first reflectors surrounding LED chips that are electrically connected to one another, and a set of second reflectors arranged to surround the first reflectors to prevent light interference and maximize efficiency. *Id.*, [0035], [0068], [0072], [0083]-[0084]. Figure 6 illustrates this general structure:



As described by Baek, Figure 6 includes **base member 10** formed together with **reflector unit 20** (made up of reflectors 22 and 24) with a **surface**, and **LED chips 30** mounted on base member 10 that are wired bonded to each other. *Id.*, [0060], [0072]-[0074]. Baek explains that, in this embodiment, the base member can be made from copper (*i.e.*, a reflective and heat-dissipating metal) and “can be fabricated with the first and second reflectors 22 and 24 through a single punching,” resulting in a single structure as depicted in Figure 6. *Id.*, [0073]. Baek explains that the base member has “excellent heat dissipating efficiency,” *id.*, [0083], and should dissipate or radiate heat outward, *id.*, [0036], [0065].

In another embodiment, Baek discloses adding a “reflect-activating layer” on reflectors 22 and 24, applied by silver plated on the surface to “further enhance light

efficiency.” *Id.*, [0078]-[0082]. This is illustrated in Figure 8, which depicts **reflect-activating layer 50** plated on **reflectors 22** and **layer 60** plated on **reflector 24**, formed together with **base member 10** and its **surface**. *Id.*, [0078]-[0082]. **Base member 10** may be mounted to **heat radiating plate 70** (also called “heat sink plate” in Baek). *Id.*, [0086], cl. 11. In Figure 8 below, layers 50 and 60, along with the base member surface, are shown in **red** (all of which are reflective in the visible spectrum when, *e.g.*, the base member is copper).



B. Cao753 Anticipates Claims 1 and 4-9

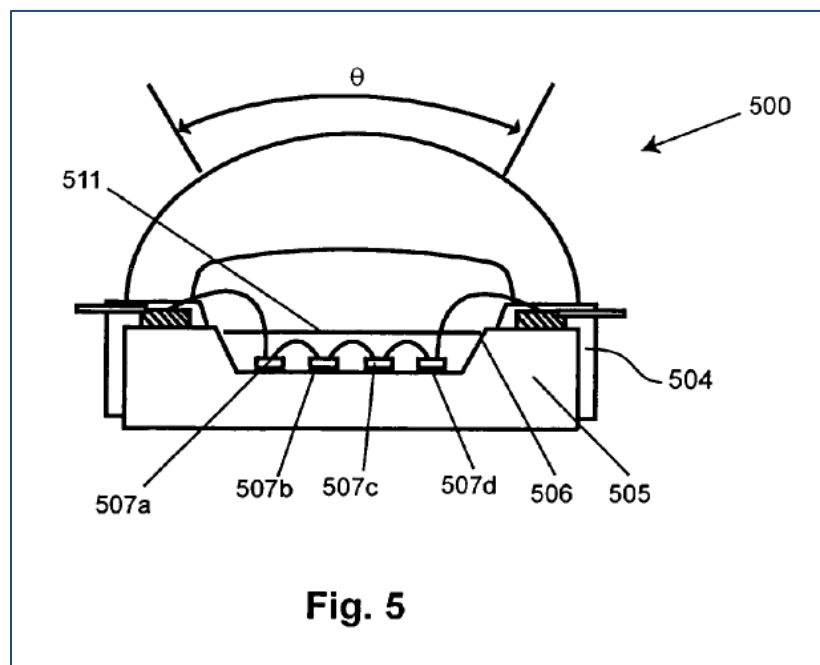
As explained below, Cao753 discloses claims 1 and 4-9 in its Figure 5 embodiment, arranged as in the claims.

1. Claim 1

1[pre] “A light emitting diode (LED) apparatus comprising:”

Cao753 discloses the preamble, regardless of whether it is limiting. EX1003 ¶¶97-99; *see also* limitations 1[a]-1[d].

Cao753 discloses an LED module with an array of LED chips mounted to a heat sink, such as LED module 500 in Figure 5. EX1005, [0020]; EX1003 ¶¶97-98.



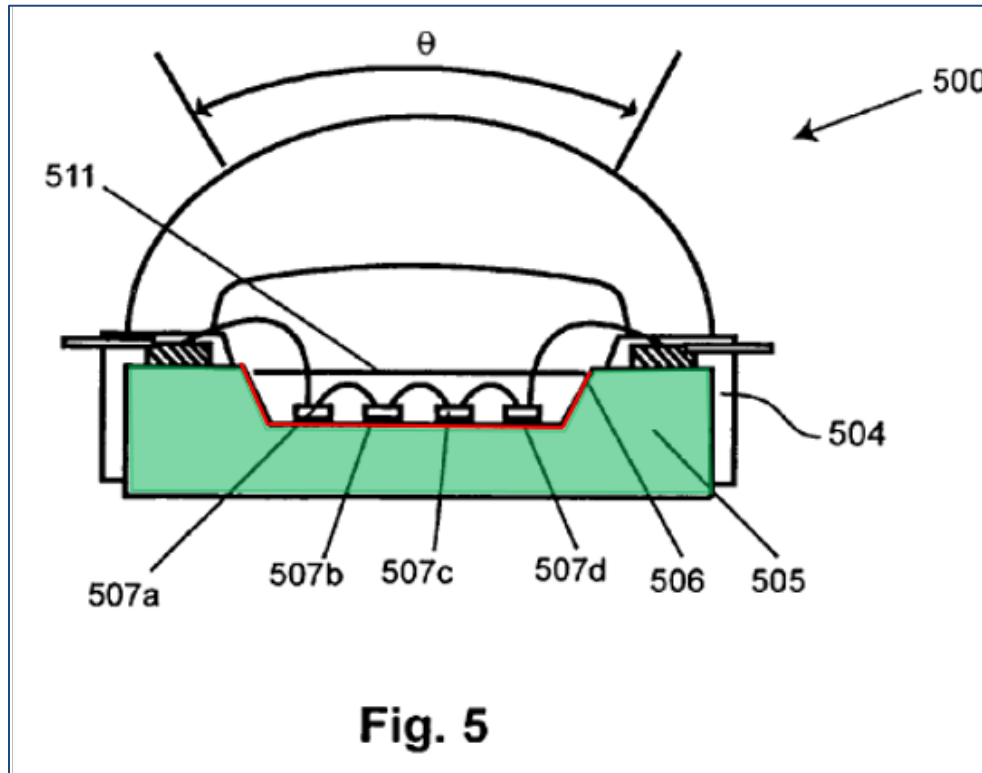
A POSA would have understood this LED module as an example of a LED apparatus, consistent with claim 1 and the '988 patent's description of its LED apparatus. EX1003 ¶99; EX1001, 1:65-66, 2:48-50, 5:30-37, FIG. 3.

1[a] “a metal substrate having a reflective surface; and”

Cao753 discloses limitation 1[a]. EX1003 ¶¶100-105.

Cao753 discloses that LED module 500 includes a well 506 within primary heat sink 505 and a plurality of LED chips 507*a-d* within the well. EX1005, [0020]; EX1003 ¶¶79, 100, 105. Cao753 further discloses that the heat sink “may be of a single material or a combination of two different kinds of materials,” and provides examples of heat sink materials including metals such as aluminum, silver, or copper (among others). EX1005, [0027], cls. 9, 19; EX1003 ¶101. A POSA would have understood that the metal primary heat sink described in Cao753 constitutes the claimed “metal substrate having a reflective surface” when the substrate is, for example, silver or aluminum, which are naturally highly reflective in the visible wavelength spectrum. EX1003 ¶¶102-103; EX1015, [0088], [0118]-[0119]; EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1016, 3, FIG. 1; EX1017, 162, FIG. 1; EX1012, 745; EX1023, 15 (App. A, 2). This is further confirmed by the ’988 patent’s disclosure that the metal substrate can be aluminum and the reflective surface may be “*bare* or polished aluminum” or “formed by silver plating.” EX1001, 4:63-67, 6:1-3; EX1003 ¶104. That is, when a substrate is made of a metal that is reflective, the substrate necessarily has a reflective surface. EX1001, 4:61-67, 6:1-3; EX1003 ¶104.

Figure 5 depicts **metal substrate 505** having a **reflective surface** (e.g., aluminum or silver). EX1005, [0027], [0020]; EX1003 ¶¶81, 105.



1[b] “a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path”

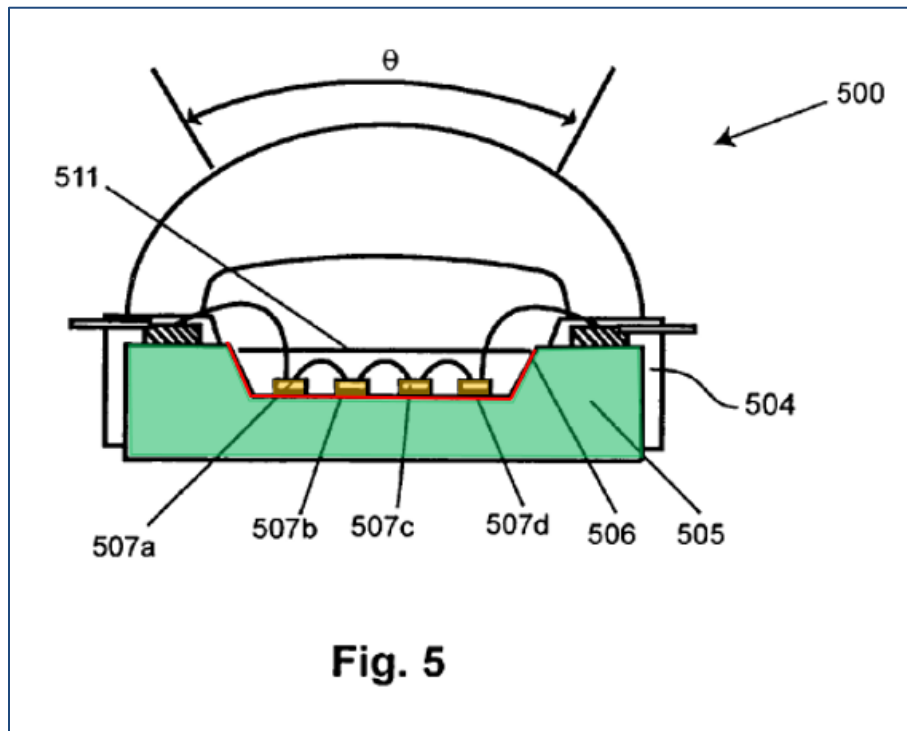
Cao753 discloses limitation 1[b]. EX1003 ¶¶106-127.

Petitioner addresses limitation 1[b] in two parts: (1) “a plurality of LED chips mounted directly to the reflective surface of the metal substrate” and (2) “creating an efficient thermal path.”

Part 1 (“a plurality of LED chips mounted directly to the reflective surface of the metal substrate...”): As shown in Figure 5, Cao753 discloses that

LED chips 507a-d are directly mounted to a **reflective surface** of **metal substrate**

505. EX1005, [0020], [0027]-[0028], [0034]; EX1003 ¶¶106-109; *see also* §V.B.1 (1[a]) (explaining Cao753’s reflective surface).



As explained above in Section V.A.1 and below in this section, Cao753 discloses that its LEDs chips are directly mounted to the reflective surface, regardless of whether direct mounting (i) allows for the use of an adhesive or “suitable adhesive” where no other intervening materials such as an insulating dielectric are present or (ii) does not allow for any adhesive or intervening material. *See* §IV.C above (discussing “mounted directly”).

Adhesive or “Suitable Adhesive” Allowed: To the extent that the claim allows for the use of an adhesive (or a “suitable adhesive”) where no other intervening materials are present (*e.g.*, a heat conductive adhesive with no intervening insulating

material), Cao753 discloses limitation 1[b]. EX1003 ¶¶111-115. Cao753 discloses that “[e]ach chip may be mounted to the heat sink by use of heat conductive or light reflective adhesive or other mounting means.” EX1005, [0020]; EX1003 ¶¶109, 112. Cao753 further discloses to use various “heat conductive and/or electrically insulative adhesives” such as “silver based epoxy, other epoxies, and other adhesives with a heat conductive quality and/or electrically insulative quality.” EX1005, [0028]; EX1003 ¶¶112-113. Cao753’s disclosure is consistent with the ’988 patent’s disclosure to mount LED chips using “any suitable adhesive.” EX1001, 4:37-53; EX1003 ¶114. A POSA would therefore have understood that using a heat conductive adhesive as disclosed in Cao753 to mount the LED chips to the reflective surface of the metal substrate means the chips are “mounted directly to the reflective surface” as used in the ’988 patent where the term encompasses “any suitable adhesive” without an intervening insulating material. EX1003 ¶115.

No Adhesive Allowed: To the extent the term “mounted directly” forecloses using any adhesive or bonding material to bond the chip and the substrate, Cao753 still discloses limitation 1[b]. EX1003 ¶¶116-121. Cao753 discloses that the LED chips in Figure 5 “may be mounted to the heat sink” by “other mounting means.” EX1005, [0020]; EX1003 ¶117. Cao753 discloses methods of mounting such chips that do not require additional materials, explaining that such mounting “may be achieved by various methods, including mechanical fixation (clips, press-fit, screws,

rivets, etc.), brazing, welding, ... or other methods.” EX1005, [0028]; EX1003 ¶118. Cao753 further explains that “[d]irect mount, surface mount, flip chip and any other desired chip mounting configuration may be employed,” EX1005, [0034]; EX1003 ¶119, and that the “chips may be mounted in a well of a heat sink or may be **mounted directly on a heat sink**,” EX1005, [0023]; EX1003 ¶119. Thus, a POSA would have understood that—even if the ’988 patent forecloses using any adhesive or bonding material to mount the LED chips to the substrate surface—Cao753 still discloses this limitation by describing these methods of mounting including non-adhesive direct mounting. EX1003 ¶120.

Notably, the ’988 patent provides no detail as to how to otherwise “directly mount” the LED to the substrate surface (disclosing only to use a “suitable adhesive”). See generally EX1001; EX1003 ¶¶58-59, 121. Accordingly, Patent Owner cannot credibly argue there is anything novel or unknown to a POSA about “directly mounting” an LED to a substrate surface without any adhesive (to the extent the term is so limited) or that Cao753’s disclosure does not disclose to a POSA such direct mounting. *See Streck, Inc. v. Research & Diagnostics Sys.*, 665 F.3d 1269, 1288 (Fed. Cir. 2012) (“It is well-established, however, that a specification need not disclose what is well-known in the art”); *Trustees of Columbia Univ. in the City of New York v. Illumina, Inc.*, 620 F. App’x 916, 933 (Fed. Cir. 2015) (“[I]f

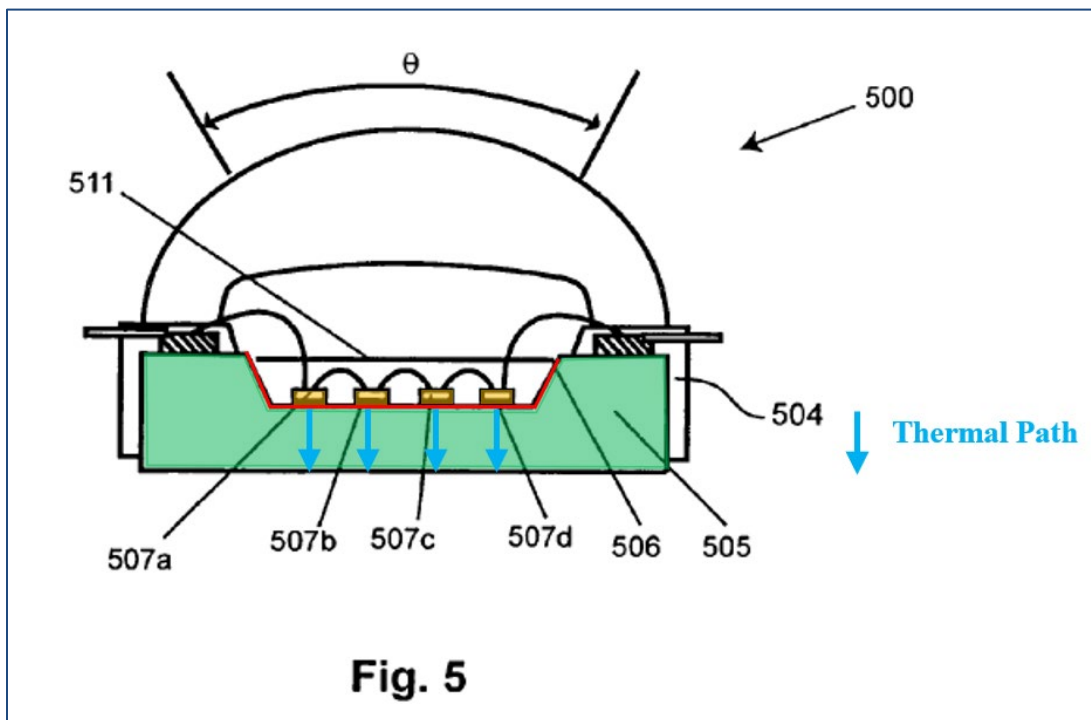
novel and nonobvious chemistry was needed to practice the claimed inventions, [patentee] would have been obligated to disclose this chemistry in the patent”).

Part 2 (“... creating an efficient thermal path”): The direct mounting disclosed in Cao753 and discussed above creates an efficient thermal path. EX1003 ¶¶122-127; EX1005, [0017], [0020], [0028], cls. 1, 12, 16.

Cao753 discloses that its direct-mount LED package design results in a “heat conductance path [that] originat[es] at said semiconductor chip [e.g., LED chip] where heat is produced by said chip when it is powered and emitting light, said heat conductance path thence to said primary heat sink, thence to said secondary heat sink....” EX1005, cls. 1, 12, 16; *see also* [0017] (disclosing “heat conductance path,” and describing how “[a]voidance of heat buildup is important to avoid overheating the semiconductor light source and decreasing its light intensity output or decreasing its life”); EX1003 ¶¶123-125.

Cao753’s **thermal path** is depicted in Figure 5, whereby **LED chips 507a-d** may be mounted to **primary heat sink 505** made of an efficient heat-dissipating metal by either (i) using heat conductive adhesive without any insulating material or (ii) “direct mounting” without an adhesive—both of which result in an efficient thermal path by allowing heat to pass through the bottom of the LED into and through the efficient heat-dissipating heat sink(s) in the shortest distance. EX1005, [0020], [0027]; EX1019, 4-157 (aluminum, silver, and copper—as disclosed in

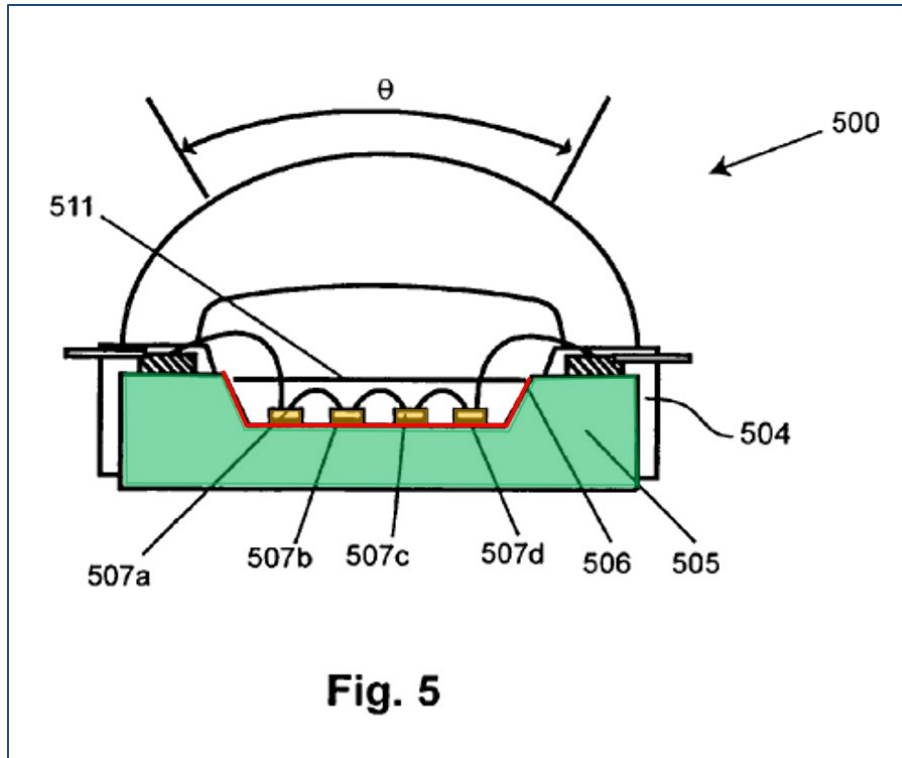
Cao753—are highly thermally conductive metals); EX1018, 10; EX1003 ¶127. This is consistent with the '988 patent, which similarly teaches that its direct mounting the LED chip to a metal substrate (*e.g.*, aluminum) without “an insulating dielectric” results in a similar “efficient thermal path 116.” EX1001, 4:37-59; EX1002, 280 (applicant asserting that “[b]ecause in general metals have high thermal conductivity, such direct mounting results in creation of an efficient thermal path....”); *see also* EX1010 ¶71 (Patent Owner district-court-claim-construction expert stating that “removing ‘insulating dielectric[s]’ creates an efficient thermal path” (citing EX1001, 4:54-59)); EX1008, 18-20; EX1009, 12-13; EX1028, 4-5; EX1003 ¶126.



1[c] “at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and”

Cao753 discloses limitation 1[c]. EX1003 ¶¶128-132.

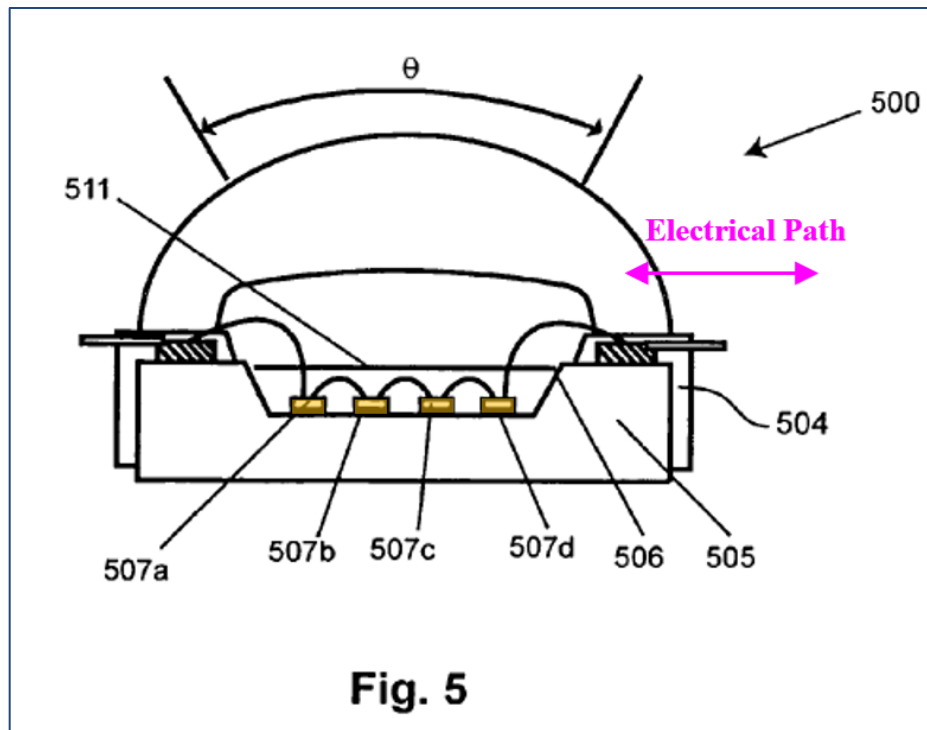
Figure 5 of Cao753 depicts LED chips 507a-d being spaced apart from each other, and Cao753 further explains that “[t]he spacing between chips can be adjusted from zero **to more than 1 mm**, depending on the application requirements.” EX1005, [0020], [0023]; *see also* [0019] (disclosing blue LED chip with shifting coating, *e.g.*, yellow phosphor to produce white light visible by human eye), [0020] (shifting coating), [0029] (disclosing to use various LED chips in the disclosed embodiments), [0032]; EX1003 ¶¶129-131. Such spacing—which can be seen in Figure 5 between LED chips 507a-d—results in exposing regions of the reflective surface between portions of the LED chips whereby the exposed regions reflect light emitted from the portions of the LED chips, just like in the ’988 patent. EX1003 ¶¶129-132; EX1001, 5:30-37, FIG. 3. Moreover, the ’988 patent places no significance or criticality on the effects of the particular spacing dimensions. *See generally* EX1001; EX1003 ¶132.



1[d] “an electrical path formed by connecting the LED chips in a chip to chip fashion.”

Cao753 discloses limitation 1[d]. EX1003 ¶¶133-135.

Figure 5 of Cao753 illustrates an arrangement where the LED chips are connected electrically via wires in a chip-to-chip fashion when the LED chips 507a-d are “wired in series.” EX1005, [0020]; EX1003 ¶134. This results in an electrical path from chip-to-chip as the LED module 500 is powered. EX1003 ¶134; EX1005, [0020].



A POSA would have understood this disclosure as showing LED chips connected in a chip-to-chip fashion in the same manner as described by the '988 patent without a connection of the chips through the wires to the substrate. EX1003 ¶135; EX1001, 5:38-45, 6:18-21, FIG. 3; §§IV.A, C.

2. Claim 4

“The apparatus of claim 1, wherein the reflective surface has a reflectivity of 70% or greater.”

Cao753 discloses claim 1. §V.B.1. Cao753 also discloses claim 4. EX1003 ¶¶136-143.

A POSA would have understood that both silver and aluminum—of which metal substrate 505 in Cao753 can be constructed as discussed in limitation 1[a]—have reflectivity of greater than 70% at the wavelengths of LED chips disclosed in

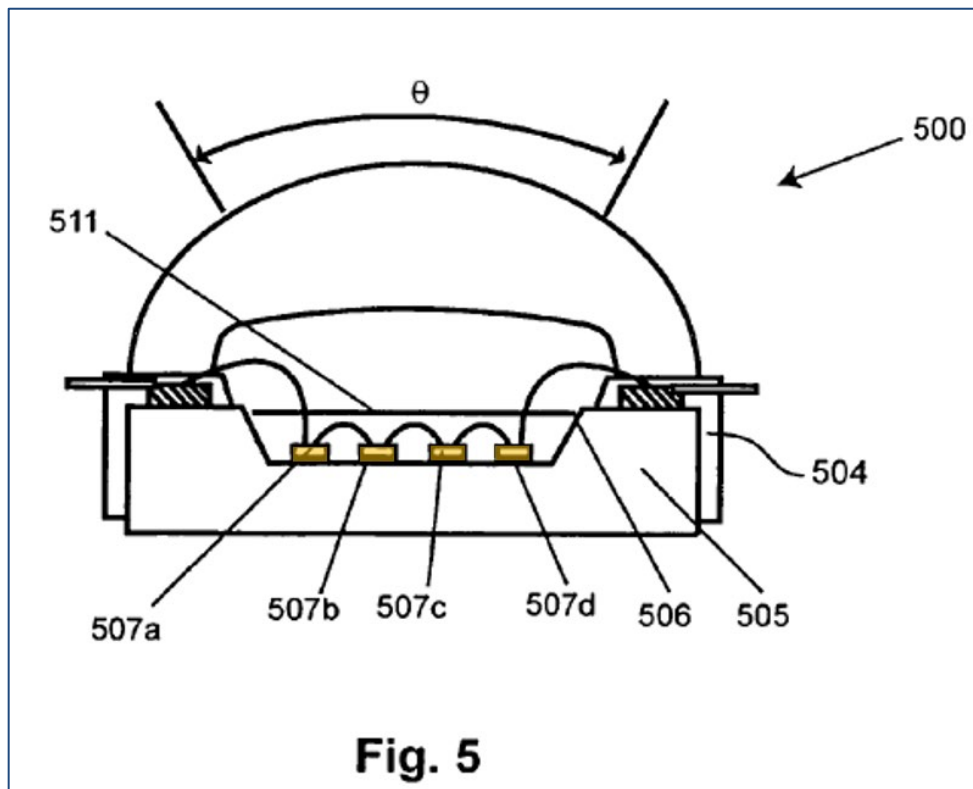
Cao753 and relevant to the '988 patent (including in the visible spectrum). EX1003 ¶¶137-143; EX1015, [0088], [0118]-[0119]; EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1016, 3, FIG. 1; EX1017, 162, FIG. 1; §V.B.1 (1[a]).

3. Claim 5

“The apparatus of claim 1, wherein the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater.”

Cao753 discloses claim 1. §V.B.1. Cao753 also discloses claim 5. EX1003 ¶¶144-148.

Figure 5 shows an “array of LED chips 507a, 507b, 507c within the well” being spaced apart from each other. EX1005, [0020]; EX1003 ¶145.



Cao753 further explains that, in embodiments like Figure 5 with multiple LED chips, “the spacing between chips can be adjusted from zero to more than 1 mm, depending on the application requirements.” EX1005, [0023]; EX1003 ¶146. A POSA would have understood that such disclosure encompasses the claimed “chip spacing that is approximately 0.5 millimeters or greater,” when the application so required, *e.g.*, to optimally reflect the light emitted from the LED chips out of the package and reduce the amount of light blocked by adjacent chips. EX1003 ¶147. And, again, the ’988 patent places no significance or criticality on the effects of the particular spacing dimensions; instead, the patent describes only to use a “pre-determined spacing” that may be “0.5 millimeters or greater” or other spacing resulting in exposed regions. EX1001, 5:16-29, 6:10-17; *see also generally id.* That is just like Cao753’s disclosed spacing. EX1003 ¶¶144-148; EX1005, [0020], [0023]; FIG. 5.

4. Claim 6

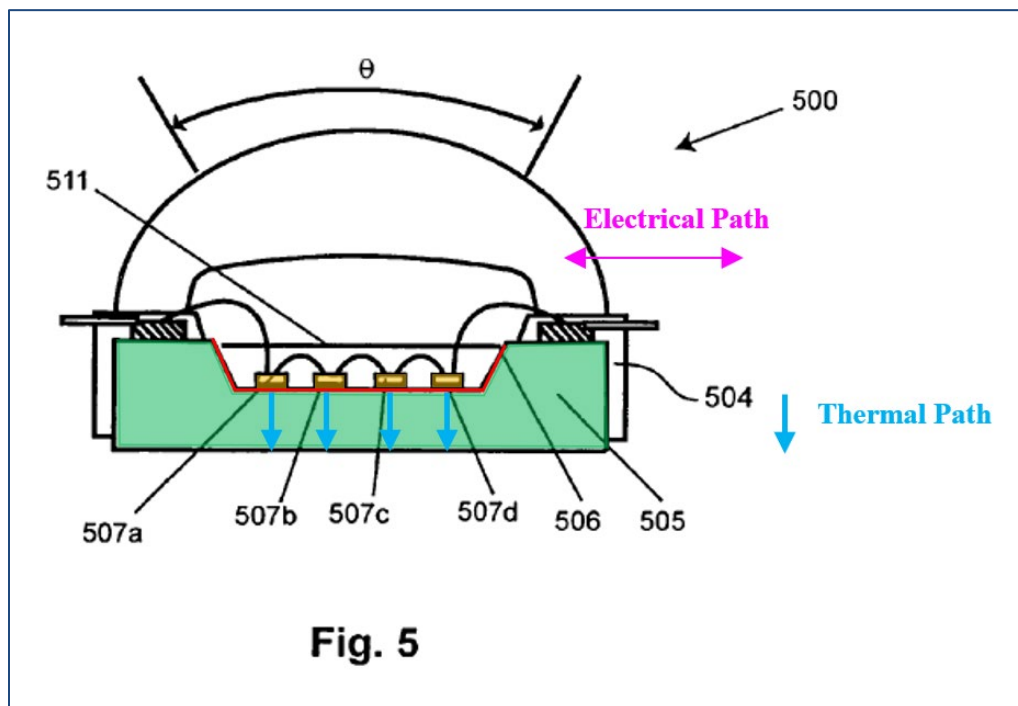
“The apparatus of claim 1, wherein the plurality of LED chips provide separate thermal and electrical paths.”

Cao753 discloses claim 1. §V.B.1. Cao753 discloses claim 6 for the same reasons discussed above regarding limitations 1[b] and 1[d]. EX1003 ¶¶149-151; *see also* §V.B.1 (1[b], 1[d]).

As explained in limitation 1[b], Cao753 discloses a thermal path down from the LED chips directly into the heat sink. *See also* EX1003 ¶150; §V.B.1 (1[b]). As

explained in limitation 1[d], Cao753 discloses a separate, horizontal electrical path between LED chips that are “wired in series” and are ultimately connected to external leads. *See also* EX1003 ¶150; §V.B.1 (1[d]). Thus, a POSA would have understood that Cao753 discloses its LED chips provide separate thermal and electrical paths—just like the ’988 patent. EX1003 ¶150; §§V.B.1 (1[b], 1[d]).

The **thermal path** and **electrical path** are depicted in Figure 5. EX1003 ¶151.

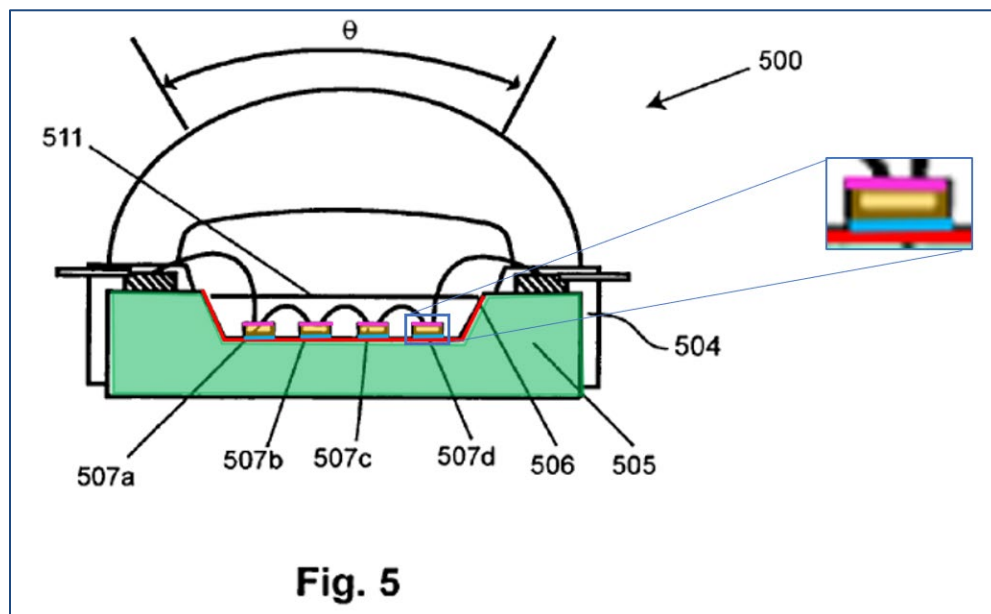


5. Claim 7

“The apparatus of claim 1 wherein the plurality of LED chips have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface.”

Cao753 discloses claim 1. §V.B.1. Cao753 also discloses claim 7. EX1003 ¶¶152-160.

This claim effectively amounts to a conventional wire-bonded LED chip whereby the LED chip's bottom surface is mounted to a substrate's surface and the electrical contacts are provided on the opposite (top) surface(s). EX1003 ¶¶153-154, 74-76; EX1005, [0028]-[0029], [0032]; EX1013, 95-96, FIG. 5.2.3(a); EX1011, 10:61-11:24, 12:61-13:30, FIGs. 17a, 18a, 24a, 25a; EX1001, 1:9-32. Wire-bonded LED chips 507a-d in Cao753 are consistent and have a bottom surface and electrical contacts (e.g., p and n electrode contacts to connect to the wires for powering the LED chips) that are on the opposite side of—and thus on different surface(s) than—the bottom surface. EX1005, [0020], [0029], [0032], FIG. 5; EX1003 ¶¶155-159. Cao753's Figure 5 shows—in a side view—an LED chip's **bottom surface** mounted to the heat sink's **reflective surface** and the chip's **top surface** that includes electrical contacts. EX1005, [0020], [0028]-[0029], [0032]; EX1003 ¶160.



Cao753 explains that the chips in this embodiment may be mounted to the heat sink using heat conductive adhesive or other means. EX1005, [0020], [0028], [0034] (describing other methods of mounting chips to the surface); EX1003 ¶156; *see also* §V.B.1 (1[b]); §V.A.1. Thus, Cao753 discloses the LED chips having a first surface mounted to the reflective surface and electrical contacts on a different one or more surfaces. EX1003 ¶¶153-160.

6. Claim 8

“The apparatus of claim 1, wherein the metal substrate is mounted directly to a heat sink.”

Cao753 discloses claim 1. §V.B.1. Cao753 also discloses claim 8. EX1003 ¶¶161-165.

Cao753 explains that its “heat sink(s) may be of a single material or a combination of two different kinds of materials, the first with a low thermal expansion rate and the second with high thermal conductivity.” EX1005, [0027]; EX1003 ¶162. Cao753 further discloses that the “primary heat sink” (*i.e.*, metal substrate, discussed in limitation 1[a]) “can be attached to **a secondary heat sink** if desired, such as[] by use of a heat conductive and/or electrically insulative adhesive, welding, brazing, soldering, or mechanical fixation.” EX1005, [0024], [0028]; EX1003 ¶163. Cao753 further discloses that this “secondary heat sink” may be “directly ... attached” to the “primary heat sink.” EX1005, cls. 1, 12, 22; EX1003 ¶163. Cao753’s direct attachment results in an efficient thermal path through the

secondary heat sink. EX1005, [0017], [0024], [0027]-[0028], cls. 1, 16; EX1003 ¶¶163, 125.

Thus, regardless of whether “mounted directly” permits use of an adhesive (such as a heat conductive adhesive without any insulating material) or requires no intervening materials whatsoever, *see* §§IV.C, V.B.1 (1[a]), Cao753 discloses that the metal substrate is mounted directly to a heat sink, *i.e.*, Cao753’s “primary heat sink” (the claimed “metal substrate”) is mounted directly to Cao753’s “secondary heat sink” (the claimed “heat sink”). EX1003 ¶164.

Moreover, Patent Owner cannot credibly argue there is anything novel or unknown to a POSA about direct mounting the heat sink given the ’988 patent’s lack of such disclosure explaining how to do so. EX1001, 5:46-62, 6:23-26; EX1003 ¶165. *See Trustees of Columbia Univ.*, 620 F. App’x at 933; *Streck*, 665 F.3d at 1288; §V.B.1.

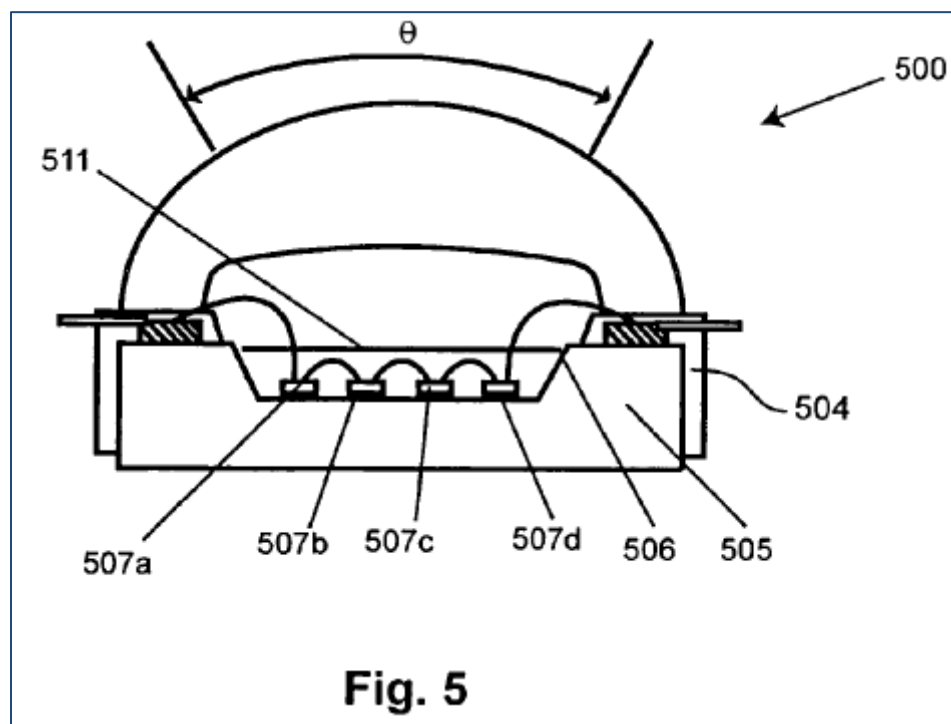
7. Claim 9

“The apparatus of claim 1, wherein the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface.”

Cao753 discloses claim 1. §V.B.1. Cao753 also discloses claim 9. EX1003 ¶¶166-168.

As discussed regarding limitation 1[b], Cao753 shows in Figure 5 an electrical connection formed by connecting the LED chips directly to one another, described

by Cao753 as “wired in series.” EX1005, [0020]; EX1003 ¶167; *see* §V.B.1 (1[b]). As shown, LED chips 507a-d are wired together and then to “intermediate islands” (unlabeled in Figure 5)—without an electrical connection between the LED chips and the reflective surface (if there were, it would result in a short circuit). EX1005, [0019]-[0020]; EX1003 ¶168; *see also* EX1007, [0020] (Cao630 referring to the islands as “connection blocks” for “electrical connection of the chip”).



Thus, Cao753 does not include an electrical connection between the LED chips and the reflective surface, but instead connects the chips in series. EX1003 ¶¶167-168.

C. Cao753 Renders Claims 1 and 4-9 Obvious

To the extent Cao753 does not anticipate claims 1 and 4-9 because Cao753 does not expressly or inherently disclose limitation 1[a] or 1[c] or claim 5 in the context of Figure 5, Cao753 alone renders these claims obvious. EX1003 ¶¶169-188. All of the other claim limitations of claims 1 and 4-9 are taught in Cao753. *See* §V.B.

Regarding limitation 1[a], Cao753 discloses that its metal substrate (such as substrate 505 in Figure 5) may be, *e.g.*, silver or aluminum. *See* §V.B.1 (1[a]). As discussed in Section V.B.1, a POSA would have understood—consistent with the ’988 patent’s disclosure that the substrate’s reflective surface may be a “bare” metal—when a reflective metal is used as the metal substrate, it necessarily has a reflective surface. *See also* EX1003 ¶170; §V.B.1 (1[a]).

To the extent the claim requires an additional “reflective surface” of the metal substrate, rather than the metal substrate being a single reflective metal which necessarily has a reflective surface—which it does not, *see* EX1001, 4:63-65 (disclosing “bare” reflective surface)—it would have nonetheless been obvious to a POSA to make the surface of metal substrate 505 in Figure 5 reflective. EX1003 ¶¶170-176. For example, Cao753 discloses an embodiment in Figure 4 which it describes as a “flip-chip design” with an LED chip mounted on a pad inside a well. EX1005, [0019]; EX1003 ¶172. Cao753 explains that in this embodiment, the pad’s “upper surface may be light reflective so that light is reflected from the pad in a

useful direction” and that the pad “may be coated with a light reflective film, such as Au, Al or Ag.” EX1005, [0019]; EX1003 ¶172. Cao753 further discloses that in this embodiment, “[t]he well may also include a reflective coating or polished surface.” EX1005, [0019]; EX1003 ¶172. While the Figure 4 embodiment differs from the Figure 5 embodiment because it refers to a flip chip design, it shows that Cao753 was concerned with ensuring that light is reflected from the LED chips in a useful direction and explains that using a reflective surface in the well of the metal substrate is an effective means of achieving this goal. EX1005, [0019]; EX1003 ¶¶173-174. This was also a commonly known and desirable method of increasing light reflectivity in LED packages at the time of the ’988 patent—including in various other Cao references with wire-bonded LED packages—which further demonstrates the known need, desire, and expectation of success of including a reflective surface (such as a polished or plated highly-reflective metal like silver or aluminum) in a metal substrate well to reflect light “in a useful direction,” and “thereby improve light source efficiency.” EX1003 ¶173; EX1007, [0019] (“The wells may include a light reflective surface for reflecting light emitted by the chips outward in a useful direction”), [0020] (“walls and bottom of the well” may be polished, plated, coated, etc. to reflect light and improve reflectivity in Cao630’s Figure 3a with wire-bonded LED, like in Cao753’s Figure 5); EX1011, 12:61-13:4; EX1014, [0012]-[0013] (“The well may also include a reflective coating or polished

surface” where the well is designed such that “all of the light emitted from the chip can be reflected back in the light exit direction for highest light output”); EX1015, [0011]-[0018], [0118], [0129]-[0130] (disclosing metal substrate with reflective surface such as plated silver to enhance light reflectivity). Moreover, the ’988 patent provides no detail about how to plate or polish metal, which is consistent with the knowledge of a POSA that such techniques were well known. EX1003 ¶176; EX1001, 4:63-65, 6:1-3. *See Trustees of Columbia Univ.*, 620 F. App’x at 933; *Streck*, 665 F.3d at 1288.

Further confirming the obviousness of including a separate reflective surface in Cao753’s Figure 5, in another similar reference where Cao is a named inventor (Cao975), Cao975 teaches that “the features of the LED 700 module [*i.e.*, with multiple LED chips wired in series in a well] are similar to those already discussed” (*i.e.*, that “[t]he well [in such embodiments] may also include a reflective coating or polished surface”). EX1014, [0012]-[0013]; EX1003 ¶175.

Regarding limitation 1[c], to the extent that Cao753 does not expressly or inherently disclose “the exposed regions reflecting light emitted from the portion of the LED chips,” (it does, *see* Section VI.B.1 (1[c]) above), it would nonetheless have been obvious to a POSA that such regions would do so. EX1003 ¶¶177-183; *see* §V.B.1 (1[c]).

First, a POSA would have understood that in LED chips such as those in Cao753 and known in the art, EX1005, [0029], light would be emitted and reflected against the various package surfaces including the surfaces of the bottom and side surfaces of the well (*i.e.*, including the exposed regions in Figure 5). EX1003 ¶¶179, 173-175; EX1013, 95-97.

Second, Cao753 teaches that when a well is used, “all of the light emitted from the chip can be reflected back in the light exit direction for highest light output” and that such a well can “include a reflective coating or polished surface,” for example, when a blue LED chip with yellow phosphor is used to produce white light visible by the human eye. EX1005, [0019]-[0020], [0029], [0032]; EX1003 ¶180. In other words, Cao753 confirms that the light is reflected in all directions of the well including the exposed regions. EX1003 ¶180.

Third, Cao753 explains that when multiple LED chips are used, “[t]he spacing between chips can be adjusted from zero to more than 1mm, depending on the application requirements.” EX1005, [0023]; EX1003 ¶181. Cao753 further explains that in mounting the LED chips to the surface, light reflective adhesives can be used. EX1005, [0028]; EX1003 ¶181. Thus, a POSA would have understood that spacing the chips apart in Cao753 would have the advantage of exposing light from the reflective surface and maximizing light reflectivity, which Cao753 already explains is important. EX1005, [0026]; EX1003 ¶181.

Fourth, the advantages of making the entire well reflective (bottom and side surfaces)—in a LED package just like Cao753’s Figure 5—to reflect light emitted from the LED chips off all surfaces were well known, further confirming the obviousness of the exposed regions reflecting such emitted light in Cao753. EX1007, [0020] (“walls *and* bottom of the well” may be polished, plated, coated, etc. “*to reflect light* and thereby improve light source efficiency”); EX1011, 12:67-13:4 (same); EX1003 ¶182.

Thus, a POSA would have understood, or at least found it obvious, that the light emitted from the LED chips in Cao753’s Figure 5 is reflected off the exposed regions. EX1003 ¶183.

Regarding claim 5, to the extent that Cao753 does not expressly or inherently disclose the claimed “approximately 0.5 millimeters or greater” spacing in the context of Figure 5 (it does, *see* limitation 1[c] and claim 5 above in Section V.B), it would nonetheless have been obvious to a POSA. EX1003 ¶¶184-188; *see* §V.B.1 (1[c]), §V.B.3.

As discussed regarding limitation 1[c] in this section and in Sections V.B.1 and V.B.3, Cao753 teaches to space the LED chips from 0 to 1 millimeter or more, which a POSA would have understood to apply to the Figure 5 disclosure. EX1003 ¶¶186-187. Moreover, it would have been logical and obvious to a POSA to so space the LED chips “depending on the application requirements” as taught by Cao753

(including approximately 0.5 millimeters or greater). EX1003 ¶¶186-187; EX1005, [0023]. For example, such spacing of the LED chips would enable light to be more efficiently and effectively reflected out of the package for highest light output, consistent with the stated goals of Cao753 and known in the art. EX1003 ¶187; EX1005, [0019]. It would have been nothing more than a routine optimization, depending on, *e.g.*, the chip size and make-up, number of chips, package size, and the well size and angle. EX1003 ¶187.

Again, the '988 patent places no significance or criticality on the effects of the particular spacing dimensions to expose regions between the chips. EX1001, 5:16-29, 6:10-17; EX1003 ¶188; *see also generally id.* The '988 patent does not otherwise explain what particular dimensions to use, the size of the chips, the size of the package, etc.—all of which confirms to a POSA there would be no technical difficulty or anything inventive in the routine experimentation in adjusting Cao753's "spacing between chips ... from zero to more than 1 mm, depending on the application requirements," as expressly disclosed in Cao753. EX1003 ¶¶186-188; EX1005, [0023]. *See K-Swiss Inc. v. Glide'n Lock GmbH*, 567 F. App'x 906, 913 (Fed. Cir. 2014) ("where the general conditions of a claim are disclosed in the prior art, ... it is not inventive to discover the optimum or workable ranges by routine experimentation"); *Gentiluomo v. Brunswick Bowling & Billiards Corp.*, 36 F. App'x 433, 439 (Fed. Cir. 2002) ("one of ordinary skill would have experimented

with various thicknesses to obtain an optimum range”); *Gardner v. TEC Sys., Inc.*, 725 F.2d 1338, 1345-49 (Fed. Cir. 1984); *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955).

D. Cao753 Alone or in View of Cao630 Renders Claims 2-4 Obvious

Claims 2-4 depend from claim 1. Cao753 alone discloses or renders obvious claim 1, for the reasons described in Ground 1 and 2. Claims 2-4 are further rendered obvious by Cao753 alone or in view of Cao630.

1. Motivation to Combine and Reasonable Expectation of Success

A POSA would have been motivated to apply, and had a reasonable expectation of success in applying, Cao630’s express polished aluminum and plated silver teachings to Cao753’s Figure 5. EX1003 ¶¶190-197.

First, Cao753 and Cao630 share a common inventor and are in the same field as each other and the ’988 patent (LED packaging for lighting devices). EX1003 ¶191; EX1005, [0001], [0007], [0019]-[0023]; EX1007, [0002]-[0003], [0020]-[0021]; EX1001, Abstract, 1:6-53. A POSA would have known of, and naturally looked to, their complementary teachings when constructing an LED package. EX1003 ¶¶193, 78-90; §§V.A.1-2.

Second, Cao753 and Cao630 are directed to the same problem: improved LED packaging for light emitting devices that, *e.g.*, address heat-dissipation and light-reflectivity issues, including for chip-to-chip wire bonded LED chips—just like the

'988 patent. EX1003 ¶192; EX1005, [0019]-[0024], [0035]; EX1007, [0014]-[0015], [0020]-[0021]; EX1001, 1:9-2:27; §§V.A.1-2.

Third, Cao753 and Cao630 share highly similar and complementary disclosures. *See* §§V.A.1-2; EX1003 ¶¶193, 78-90.

Fourth, a POSA would have been motivated to polish or plate the surface of substrate 505 in Figure 5 of Cao753. As discussed in Section V.A.1 (overview), and Sections V.B.1 and V.C (regarding limitation 1[a]), Cao753 already teaches polishing or coating the surface of the well substrate in order to improve light efficiency (in the context of Figure 4 with a single LED chip or chip array); and it would have been readily apparent to a POSA to apply such teaching to the Figure 5 embodiment for the same reasons. *See also* EX1003 ¶194; §§V.A.1, V.B.1, V.C.

Lastly, a POSA would further understand that: (i) there were known advantages to polishing or plating the substrate well's surface including to improve light reflectivity and package performance; and (ii) it would have been a simple addition using known polishing and plating techniques to polish or plate the surface of Cao753's substrate. EX1003 ¶195; EX1005, [0019]-[0020], [0027]; EX1006, [0066]; EX1007, [0020]; EX1011, 12:67-13:4; EX1015, [0018]; EX1020, [0043], [0066]. Indeed, the '988 patent provides no detail concerning how to polish or plate a substrate surface, EX1001, 4:63-65, 6:1-3, further confirming there would be no

technical difficulties in doing so. EX1003 ¶196. *See Trustees of Columbia Univ.*, 620 F. App'x at 933; *Streck*, 665 F.3d at 1288; §V.B.1.

The obviousness of combining Cao753 and Cao630 and of the claims is discussed further below.

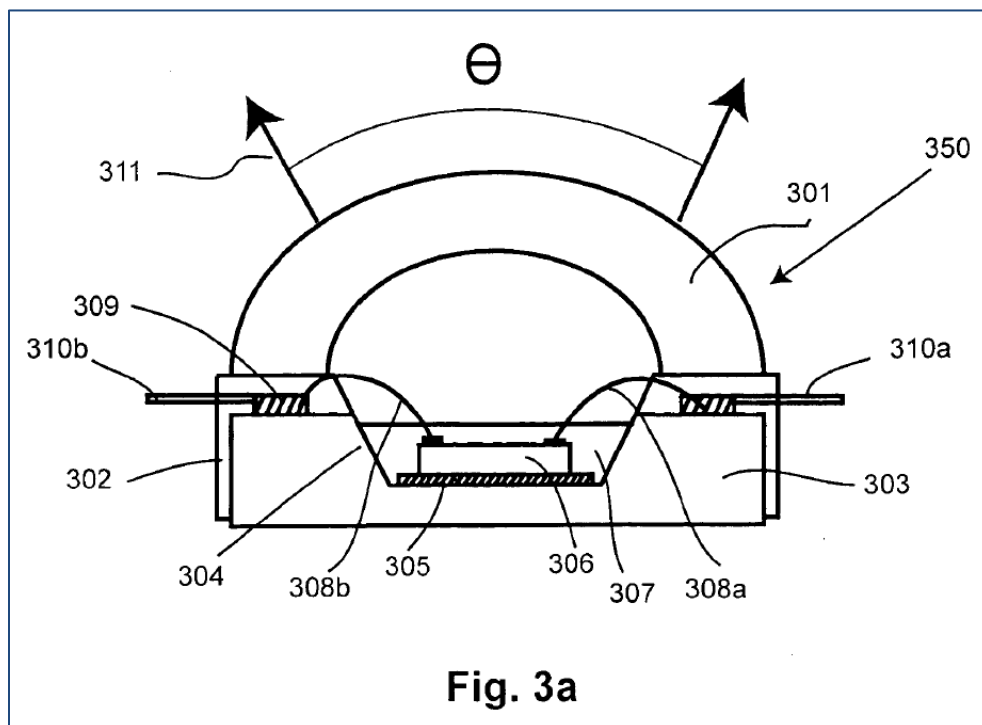
2. Claim 2

“The apparatus of claim 1, wherein the reflective surface comprises polished aluminum.”

Cao753 discloses or renders obvious claim 1. §§V.B.1, V.C. Cao753 alone or in view of Cao630 discloses or renders obvious claim 2. EX1003 ¶¶198-203.

Claim 2 simply specifies that “the reflective surface comprises polished aluminum.” Cao753 itself discloses that (i) its metal substrate can be made of aluminum and include a well (in various Figures) and (ii) a well can include a polished surface (in the context of Figure 4). EX1005, [0019]-[0020], [0027]; EX1003 ¶¶198-200. For the reasons discussed above in Sections V.C and V.D.1, a POSA would logically have understood to apply Cao753's polished-surface teachings to its Figure 5 embodiment, thereby resulting in an aluminum substrate with a polished surface. *See also* EX1003 ¶¶201, 194-196, 173; §§V.C, V.D.1. Indeed, as discussed above in Section V.D.1, the benefits and routine application of polishing a substrate surface were well known in order to improve the light-emitting properties of an LED package. *See also* EX1003 ¶201; §V.D.1.

Further confirming the obviousness of claim 2, Cao630—which has a common inventor with Cao753—discloses that in its embodiment in Figure 3a (below) where a wire-bonded chip array is mounted in a well, “[t]he walls and bottom of the well may be *polished to be light reflective*, or may be covered, plated, painted, or bonded with a light reflective coating such as *Al*, Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastic and others *to reflect light and thereby improve light source efficiency*.” EX1007, [0020], FIG. 3a (below); EX1011, 12:67-13:4; EX1003 ¶¶202-203. Especially taken together with Cao753’s disclosure to include a polished surface of the well substrate and that the substrate may be aluminum, it confirms the obviousness to a POSA to polish Cao753’s aluminum substrate to further enhance its reflectivity. EX1003 ¶¶202-203.



And, as discussed in this section and in Section V.D.1 above, a POSA would have been motivated to apply, and had a reasonable expectation of success in applying, Cao630's express polished aluminum teachings to Cao753's Figure 5. *See also* EX1003 ¶¶203, 194-196; §V.D.1.

3. Claim 3

“The apparatus of claim 1, wherein the reflective surface comprises silver plating.”

Cao753 discloses or renders obvious claim 1. §§V.B.1, V.C. Cao753 alone or in view of Cao630 discloses or renders obvious claim 3. EX1003 ¶¶204-208.

Claim 3 simply specifies that “the reflective surface comprises silver plating.” Like polishing, a POSA would have understood the known advantages of plating silver for the substrate's reflective surface to improve light reflectivity and package efficiency. EX1003 ¶¶206, 194-196, 173; *see also* §§V.C, V.D.1.

Further confirming the obviousness of claim 3, Cao630 discloses that in its embodiment in Figure 3a (below) where a wire-bonded chip array is mounted in a well, “[t]he walls and bottom of the well may be polished to be light reflective, or may be covered, ***plated***, painted, or bonded ***with a light reflective coating*** such as Al, Au, ***Ag***, Zn, Cu, Pt, chrome, other metals, plating, plastic and others to reflect light and thereby improve light source efficiency.” EX1007, [0020]; EX1011, 12:67-13:4; EX1003 ¶¶207-208.

And, as discussed in this section and Sections V.C and V.D.1 above, a POSA would have been motivated to apply, and had a reasonable expectation of success in applying, Cao630's express plating silver teachings to Cao753's Figure 5. *See also* EX1003 ¶¶208, 194-196; §§V.C, V.D.1.

4. Claim 4

“The apparatus of claim 1, wherein the reflective surface has a reflectivity of 70% or greater.”

Cao753 discloses or renders obvious claim 1. §§V.B.1, V.C. Cao753 alone or in view of Cao630 discloses and renders obvious claim 4 for the same reasons as claims 1-3 (*e.g.*, when aluminum or silver are used, the reflectivity is 70% of greater in the visible wavelength). EX1003 ¶¶209-210; EX1015, [0088], [0118]-[0119]; EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1016, 3, FIG. 1; EX1017, 162, FIG. 1; *see also* §V.B.1 (1[a]); §V.B.2.

E. Baek Alone or in View of Cao630 Renders Claims 1-9 Obvious

Baek alone or in view of Cao630 discloses and renders obvious claims 1-9.

1. Motivation to Combine and Reasonable Expectation of Success

A POSA would have been motivated to apply, and had a reasonable expectation of success in applying, Cao630's express teachings of a reflective substrate surface and direct mounting to Baek. EX1003 ¶¶212-221.

First, Baek and Cao630 are in the same field as each other and the '988 patent (LED packaging for lighting devices). EX1003 ¶213; EX1006, Abstract, [0003];

EX1007, [0002]-[0003], [0020]-[0021]; EX1001, Abstract, 1:6-53. A POSA would have known of, and naturally looked to, their complementary teachings when constructing an LED package. EX1003 ¶¶215, 86-89, 91-95.

Second, Baek and Cao630 are directed to the same problem: improved LED packaging for light emitting devices that, *e.g.*, address heat-dissipation and light-reflectivity issues, including for chip-to-chip wire bonded LED chips—just like the ’988 patent. EX1003 ¶214; EX1006, [0003], [0032]-[0044], [0085]; EX1007, [0014]-[0015], [0020]-[0021]; EX1001, 1:9-2:27.

Third, Baek and Cao630 share highly similar and complementary disclosures. *See* §§V.A.2-3; EX1003 ¶¶215, 86-89, 91-95.

Fourth, a POSA would have been motivated to polish or plate the entire surface of Baek’s metal substrate (*i.e.*, its base member and reflectors, as discussed in the following sections). As discussed in more detail in Sections V.E.2 and 4, Baek already teaches to plate the surface of the well substrate using, *e.g.*, silver, in order to improve light efficiency. *See also* EX1003 ¶¶216-219; §§V.E.2, 4. To the extent Baek does not teach to plate the entirety (it does), doing so would have been obvious and logical, as evidenced by Cao630 and the state of the art. EX1003 ¶¶217-218. For example, Cao630 explains why a POSA would plate, polish, coat, etc. with a reflective material the entire surface of a substrate well (*i.e.*, “[t]he walls **and** bottom

of the well”): “to reflect light and thereby improve light source efficiency.” EX1007, [0020]; EX1003 ¶217.

Fifth, a POSA would further have understood that: (i) there were known advantages to polishing or plating the entire substrate surface including to improve light reflectivity and package performance; and (ii) it would have been a simple addition using known polishing and plating techniques to polish or plate the surface of Baek’s substrate. EX1003 ¶218; EX1005, [0019]-[0020], [0027]; EX1006, [0066], [0078]-[0082]; EX1007, [0020]; EX1011, 12:67-13:4; EX1015, [0018]. Indeed, the ’988 patent provides no detail concerning how to polish or plate a substrate surface, EX1001, 4:63-65, 6:1-3, further confirming there would be no technical difficulties in doing so. EX1003 ¶219. *See Trustees of Columbia Univ.*, 620 F. App’x at 933; *Streck*, 665 F.3d at 1288.

Lastly, Baek does not expressly describe how to mount its LED chips to its substrate surface—it simply says to “mount” the LED chips and depicts direct mounting. *See* §V.E.2 below (1[b]); EX1003 ¶220. Thus, a POSA would have looked to other references in the field (such as Cao630) for express mounting teachings and understood there were many known, routine ways to mount such LED chips, EX1003 ¶220; EX1007, [0020], in order to maintain and improve heat dissipation efficiency (consistent with the stated goals in both Baek and Cao630),

EX1003 ¶220; EX1007, [0009], [0014]; EX1006, [0003], [0032]-[0036]; *see also* §V.E.2 below (1[b]).

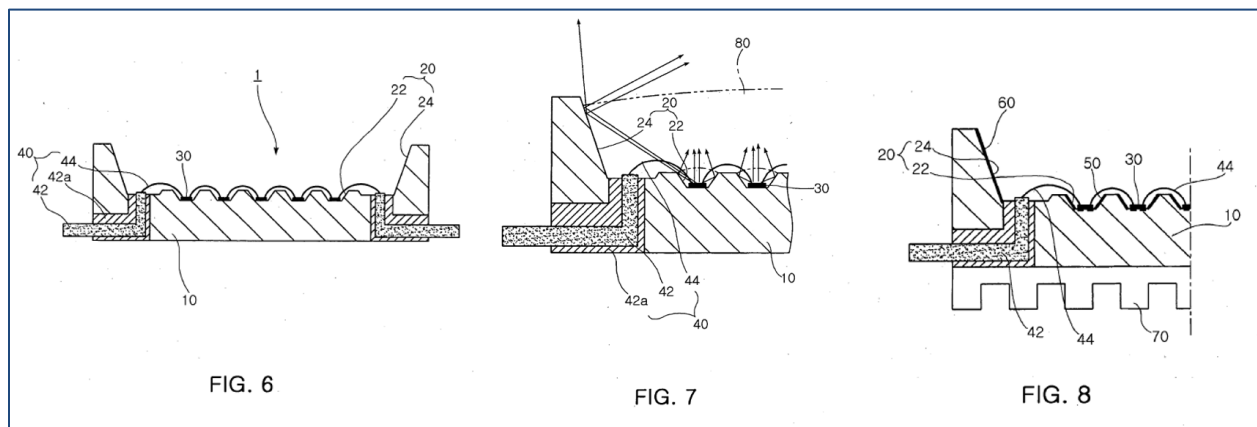
The obviousness of combining Baek and Cao630 and of the claims is further discussed below.

2. Claim 1

1[pre] “A light emitting diode (LED) apparatus comprising:”

Baek discloses the preamble, regardless of whether it is limiting. EX1003 ¶¶222-223; *see* limitations 1[a]-1[d].

Baek discloses a “high power LED package,” including LEDs 30 mounted to a substrate surface. EX1006, Abstract, [0060]-[0064], FIGs. 5-8; EX1003 ¶¶222-223.



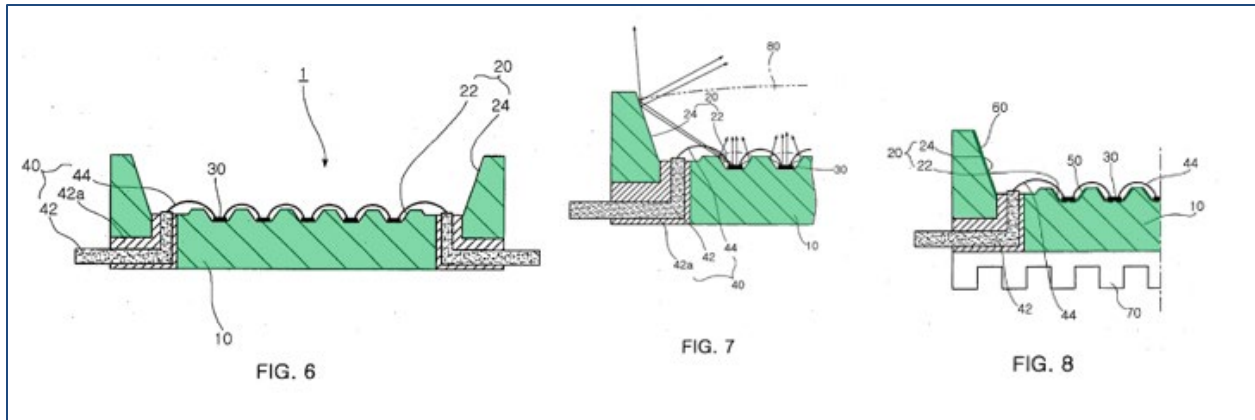
1[a] “a metal substrate having a reflective surface; and”

Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—limitation 1[a]. EX1003 ¶¶224-247.

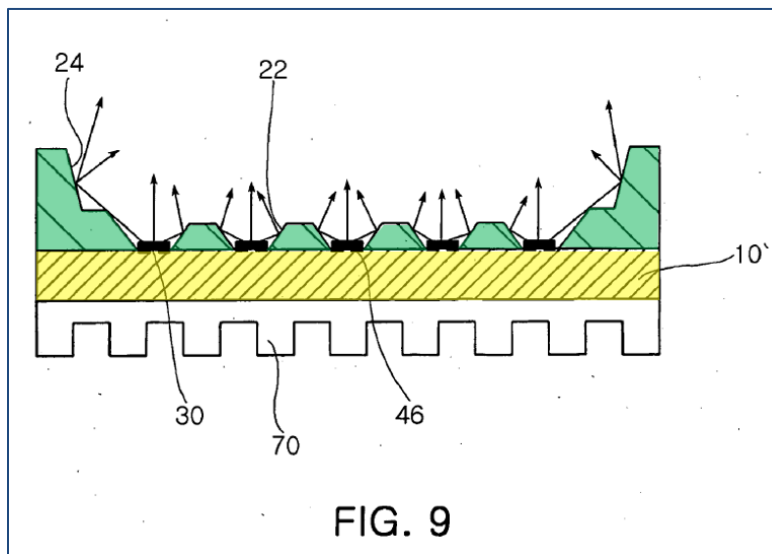
Baek discloses “base member 10,” which is “made of or plated (coated) with a metal of excellent heat conductivity.” EX1006, [0065]-[0066]; EX1003 ¶225. Baek discloses that the base member can be “made of a material capable of dissipating (radiating) heat such as Cu of excellent heat conductivity.” EX1006, [0072]; EX1003 ¶¶225-226. Baek also discloses reflectors 22 and 24. EX1006, [0060], [0068]-[0073], FIGs. 5-8; EX1003 ¶227.

A POSA would have understood that the base member and reflectors together constitute the claimed “metal substrate” and its surface (all of which are reflective) correspond to the claimed “reflective surface.” EX1003 ¶¶228-237; EX1012, 745; EX1023, 15 (“leadframe substrate”).

According to Baek, the reflectors and base member 10 can be “fabricated ... through single punching” and can be made of copper, EX1006, [0072]-[0073], which is a reflective metal in the visible spectrum, EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1003 ¶¶228-229. Thus, a POSA would have understood and logically treated base member 10 and reflectors collectively as a single unit that are fabricated together from the same material. EX1003 ¶¶228-229. This is further confirmed by the figures, in which Figures 5-8 depict the metal reflectors and base member as a single unit constructed from the same material. EX1006, FIGs. 5-8; EX1003 ¶¶230-232. For example, see Figures 6, 7, and 8 with **reflectors and base member**:



This is further confirmed by contrasting Figure 9, where “**first and second reflectors** are made *separately* from the **base member 10'** and mounted thereon.” EX1006, [0074]; EX1003 ¶232. Figure 9 likewise depicts **reflectors 22 and 24** as being separate from **base member 10'** (note the contrasting crosshatching in Figure 9, whereas Figures 6-8 above includes the *same* crosshatching and Figure 5 shows the outer view of the single structure, thereby further confirming to a POSA that they are a single structure in Figures 5-8). EX1006, FIGs. 5-9; EX1003 ¶232.



As yet additional confirmation of the single structure of its metal substrate comprising the base member 10 and dual reflectors 22 and 24 in Figures 5-8, Baek discloses that “the dual reflector structure can preferably prevent light interference and raise heat dissipating efficiency with a lead frame having a group of indented recesses,” (*i.e.*, the indented recesses (reflectors) are part of the lead frame substrate). EX1006, [0032], [0034], [0069], [0083]-[0084]; EX1003 ¶233.

A POSA would have understood, or at least found it obvious, that Baek’s metal substrate (base member and reflectors) includes a reflective surface where light emitted from the LED chips is reflected off the bottom and side walls of the substrate well. EX1003 ¶¶235-237.

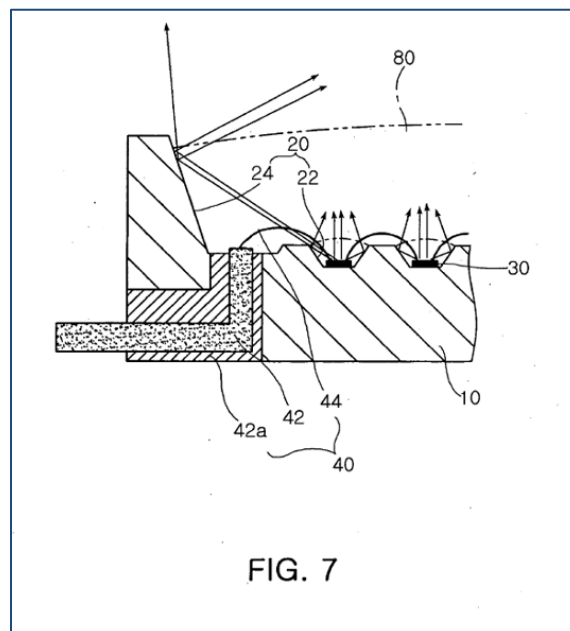
Consistent with the disclosure in the ’988 patent that a metal substrate having a reflective surface may simply be the “bare” metal substrate, EX1001, 4:63-67, Baek’s disclosure of its metal substrate—such as copper—that reflects light off its surface meets this requirement. EX1003 ¶234; EX1027, 511, FIG. 11-1 (discussing copper reflectivity in the visible spectrum); EX1022, 376, FIG. 13.8 (same).

To the extent that the “reflective surface” needs to be enhanced to meet the claim, it would still be disclosed by Baek (or obvious over Baek alone or in view of Cao630). EX1003 ¶¶238-247.

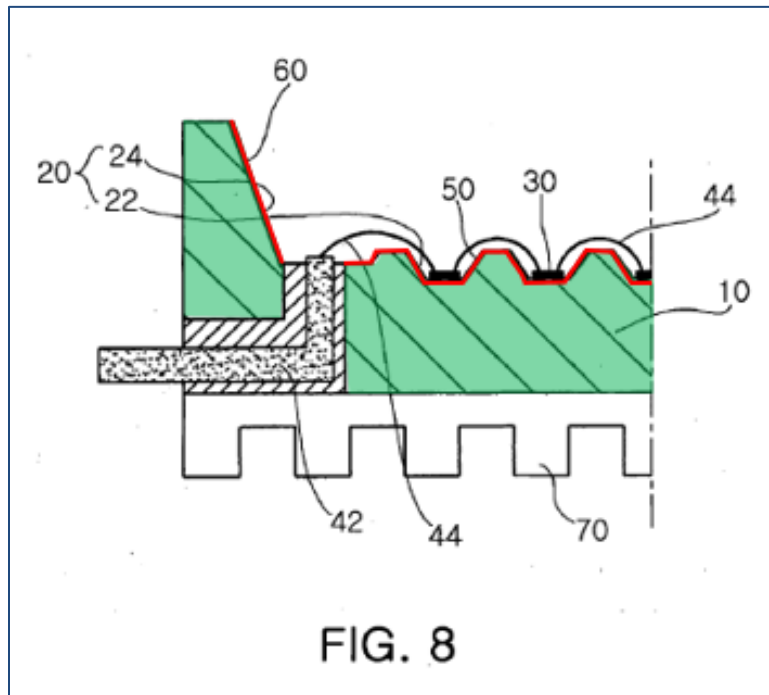
First, Baek discloses that “[p]referably, the first reflectors have a **reflect-activating layer formed on a surface** thereof to raise reflecting efficiency of light

generated from LED chips, and the second reflector has a **reflect-activating layer formed on a surface** thereof to raise reflecting efficiency of lights generated from the LED chips and reflecting from the first reflectors,” EX1006, [0043], [0066]-[0071], [0078]-[0081], which a POSA would have understood applies to the various embodiments (or at least would have found it obvious to so apply to achieve the stated goals in Baek regarding reflecting efficiency). EX1003 ¶¶239-242.

Second, Baek depicts and describes that the reflectors reflect light emitted from LED chips, as shown for example in Figure 7 with the arrows indicating emitted light reflecting off the surface. EX1006, [0068]-[0071]; EX1003 ¶243.



Third, Baek depicts and describes the **reflector-activating layer** of the **metal substrate**, such as in Figure 8, shown below in **red** with the base member **surface** (which is likewise reflective). EX1003 ¶244.



Per Baek, the reflect-activating layers may be silver “plated on the surface” of the substrate, EX1006, [0081]; EX1003 ¶245, just like the ’988 patent, EX1001, 4:63-65, 6:1-3; EX1003 ¶41.

Lastly, while Baek does not expressly state that the reflect-activating layer would be under the LED chips within the well, a POSA would have understood (or at least found it obvious) to do so consistent with the stated goals in Baek to enhance light reflectivity. EX1003 ¶¶246-247. Indeed, when a plating is applied to the surface, such plating would be applied to the entire surface after the base member and reflectors are fabricated together (which, here would be the surface of the base member and reflectors). EX1003 ¶246; EX1007, [0020]. This would not only be typical, but it would also be much simpler and more efficient during manufacturing

than individually plating the slopes of reflectors 22 and 24 to increase light reflection. EX1003 ¶246. And, it would at least have been obvious to do so for similar reasons discussed in Sections V.C, V.D.1 and V.E.1, including to enhance reflectivity for light reflecting off the base member portion and to improve LED package performance. EX1003 ¶¶247, 173-176, 194-196; EX1005, [0019]; EX1007, [0019]-[0020]; EX1011, 12:67-13:4; EX1014, [0012]-[0013]; EX1015, [0011]-[0018], [0055]-[0056], [0118], [0129]-[0130]; §§V.C, V.D.1, V.E.1.

The obviousness and advantages of doing so are further confirmed by Cao630, which teaches that “[t]he walls *and* bottom of the well may be *polished* to be light reflective, or may be covered, *plated*, painted, or bonded with a light reflective coating such as Al, Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastic and others *to reflect light and thereby improve light source efficiency.*” EX1007, [0020], FIG. 3a; EX1003 ¶247.

1[b] “a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path and”

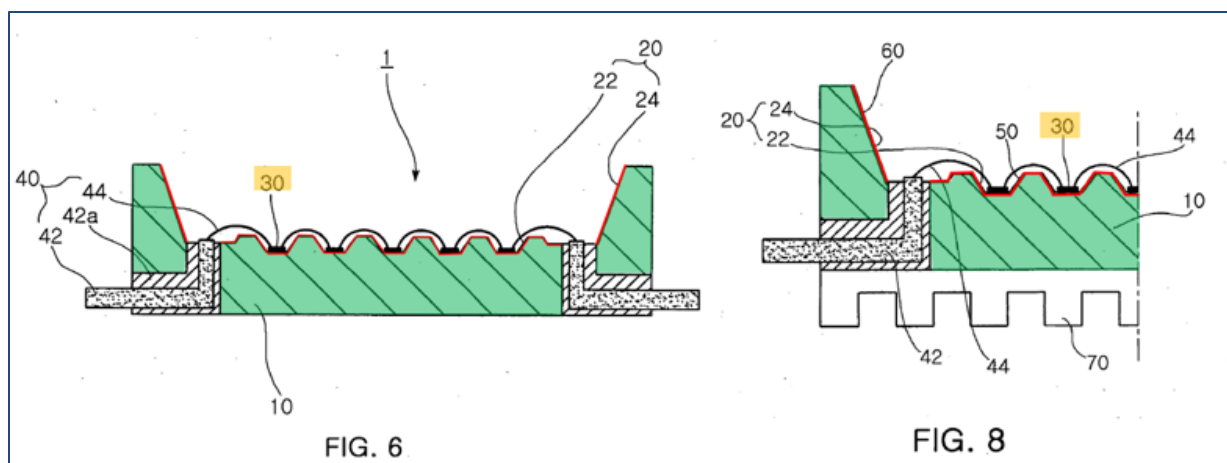
Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—limitation 1[b]. EX1003 ¶¶248-259.

Petitioner addresses this limitation in two parts: (1) “a plurality of LED chips mounted directly to the reflective surface of the metal substrate” and (2) “creating an efficient thermal path.”

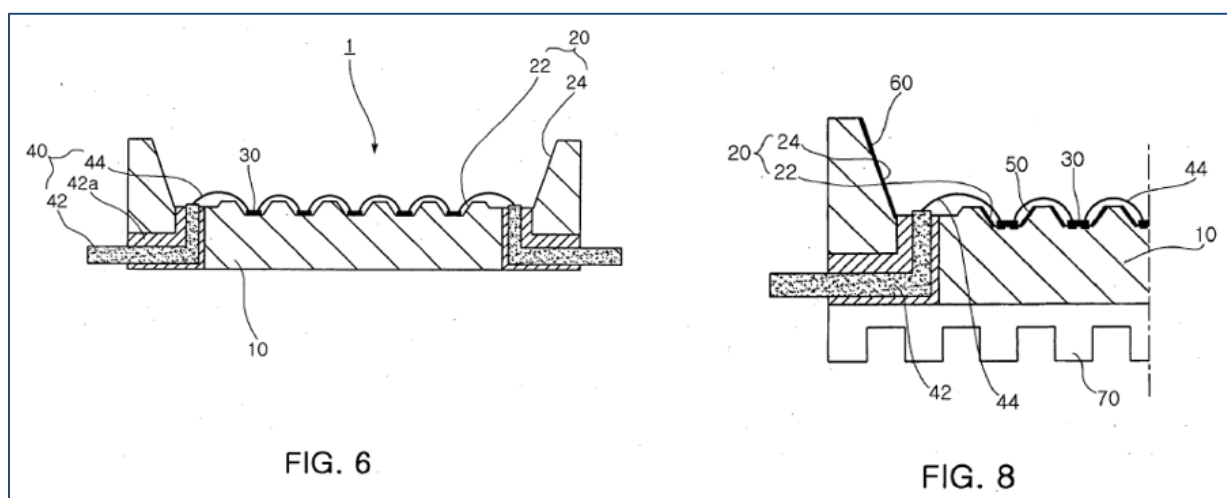
Part 1 (“a plurality of LED chips mounted directly to the reflective surface of the metal substrate...”): Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—that its LED chips are directly mounted to its metal substrate’s reflective surface. EX1003 ¶¶248-256. As explained below in this Section V.E.2 (1[b]), this is true regardless of whether direct mounting (i) allows for the use of an adhesive or “suitable adhesive” where no other intervening materials such as an insulating dielectric are present or (ii) does not allow for any adhesive or intervening material. *See* §IV.C.

Baek discloses that its LED chips are mounted on the surface of base member 10, explaining that the LED chips are “surface-mounted on the substrate.” EX1006, [0042], [0035] (“plurality of LED chips mounted on the base member”), [0060] (same), [0067]-[0068]; EX1003 ¶¶251-252. Moreover, Baek expressly notes that it was known in the art that “LEDs are produced in the form of Surface Mount Devices (SMDs) to be **directly mounted on the PCB**” (*e.g.*, substrate). EX1006, [0014]; *see also* [0042] (noting that in its invention, “[p]referably ... the LED chips ... are surface-mounted on the substrate”); EX1003 ¶252.

As depicted in its figures—such as Figures 6 and 8 below—there are no intervening materials disclosed between **LED chips 30** and the **reflective surface** of the **metal substrate**, demonstrating to a POSA that the chips are directly mounted to the reflective surface as Baek notes was known in the art. EX1003 ¶¶253-254.



The same can be seen in the unannotated versions:



A POSA further would have understood that the LED chips in Baek could be mounted to the surface in a number of ways, including using a heat conductive adhesive, and the advantages of doing so (*e.g.*, efficiently dissipate heat through the metal substrate)—consistent with the goals of Baek to have “excellent light efficiency and improved heat dissipating characteristics, which completely satisfy [the] most important two factors for LED packages, thereby improving package reliability.” EX1006, [0085]; EX1003 ¶¶255, 220; EX1007, [0020].

As one example, Cao630 discloses that mounting of the LED chips may be achieved by a variety of methods—with or without any adhesive or other material—including direct mount, mechanical fixation, brazing, welding, use of an adhesive or other methods, and notes that use of a heat conductive adhesive may be desired. EX1007, [0015]; EX1020, [0036]-[0037] (disclosing wire-bonded LED that is “directly mounted on the basic surface of the base” using an “adhesive member ... having heat conductivity” which results in the LED chip and base being “thermally coupled”); EX1021, [0049] (disclosing that the “LED chip is mounted directly on the bottom recess [of the metal plate]”), *c.f.* [0007] (prior lighting emitting device had “LED chip ... not mounted directly on the metal plate” and instead “mounted over the metal plate with [an] insulating layer....”); EX1003 ¶256. Moreover, further confirming the obviousness of such “direct mounting” is that there was a known advantage to “directly mounting” the LED chip to the metal substrate (as compared to having an “insulating layer” or insulating dielectric in between): “heat radiation of the light emitting device decreases [when direct mounting is not used], as compared to the case where the LED [chip] is directly mounted on the metal plate....” EX1021, [0007]; EX1003 ¶256. Notably, the result of such “direct mounting” is consistent with the goals of Baek. EX1003 ¶256. And, again, Patent Owner cannot credibly argue there is anything novel or nonobvious about direct

mounting without an adhesive given the '988 patent's lack of such disclosure. *See Trustees of Columbia Univ.*, 620 F. App'x at 933; *Streck*, 665 F.3d at 1288; §V.B.1.

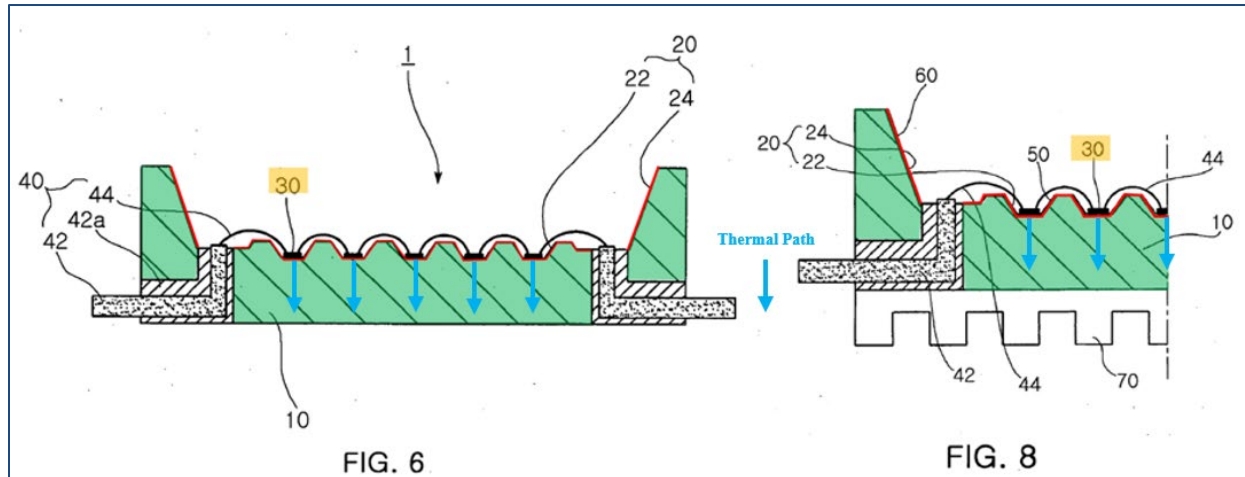
Part 2 (“... creating an efficient thermal path”): The direct mounting discussed above in Part 1 creates an efficient thermal path. EX1003 ¶¶257-259.

Baek explains that the base member is a “metal of excellent heat conductivity, and thus can maintain heat dissipating ability when embodied into a high power package where a plurality of LED chips are mounted.” EX1006, [0066]; EX1003 ¶258. Baek further explains that the base member “can at least dissipate or radiate heat outward” (relative to the side-view cut-out figures, in a downward vertical direction). EX1006, [0065]; EX1003 ¶258. Baek also explains that the base member and reflectors (the claimed “metal substrate”) can be “made of a material capable of dissipating (radiating) heat such as Cu of excellent heat conductivity.” EX1006, [0072]-[0073]; EX1003 ¶258.

Baek also discloses that an object of its invention is to mount LED chips in recesses between reflectors to “improve heat dissipating efficiency of a base member, thereby imparting excellent heat dissipating characteristics to the LED package.” EX1006, [0034], [0036] (“base member comprises a member capable of dissipating heat”), [0085]; EX1003 ¶258.

Thus, a POSA would have understood that Baek explains that mounting the LED chips directly to the surface of its efficient heat-dissipating metal substrate

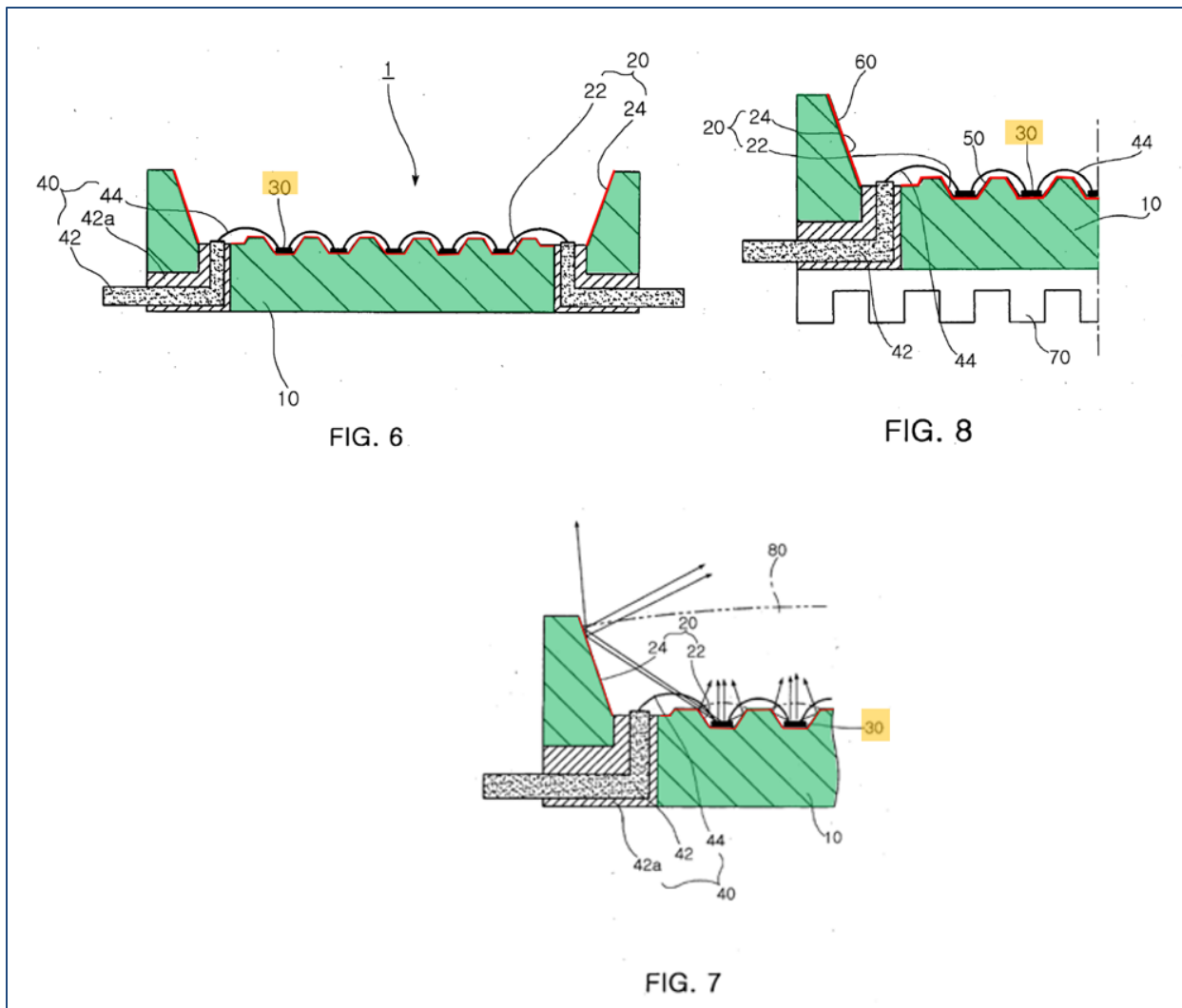
creates an **efficient thermal path** in the shortest distance (e.g., when an insulating dielectric is not used), as depicted in Figures 6 and 8. EX1006, [0083]-[0085]; EX1003 ¶259; *see also* EX1001, 4:37-59; EX1002, 280; EX1008, 18-20; EX1009, 12-13; EX1010 ¶71; EX1028, 4-5; §V.B.1 (1[b]). And, the obviousness and advantages of direct mounting are further confirmed by the state of the art (including Cao630) to further improve heat dissipation out of the package. EX1003 ¶¶256-257, 220; §V.B.1 (1[b]).



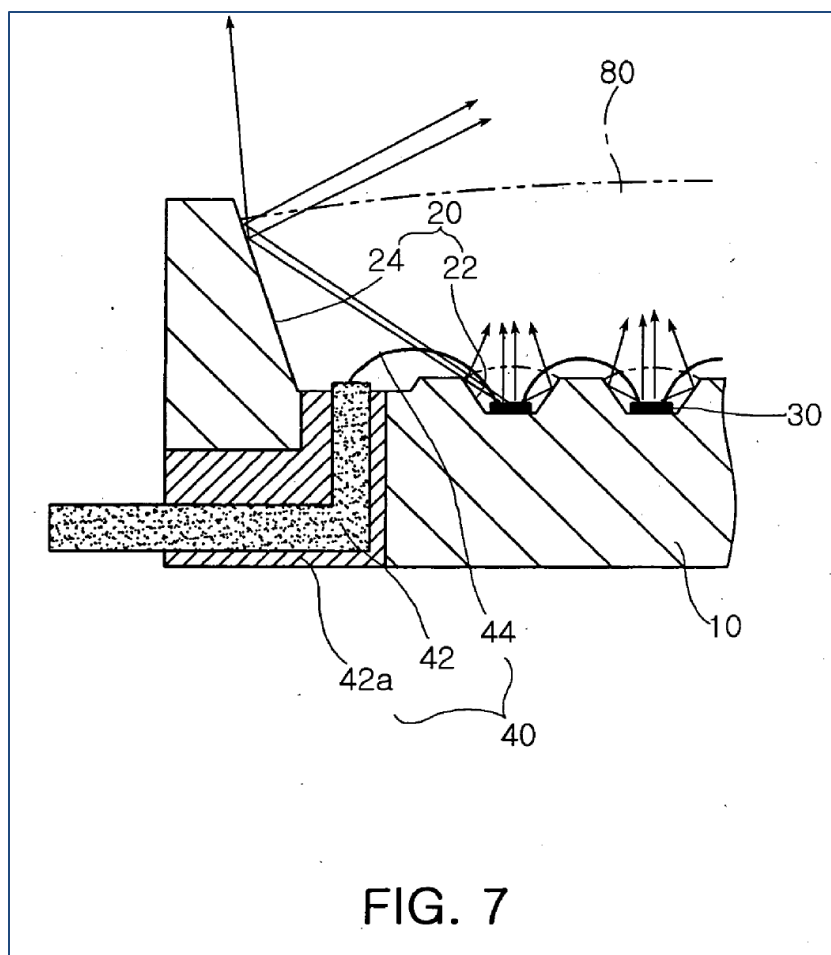
1[c] “at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and”

Baek discloses, or it would have been obvious to include as part of Baek, limitation 1[c]. EX1003 ¶¶260-263.

Baek discloses spacing the LED chips apart from each other with reflector units between the LED chips, as seen in Figures 6-8. EX1003 ¶261.



This can also be seen in unannotated Figure 7, where the spacing of the LED chips exposes regions of the reflective surface including the wells' bottoms and sides. EX1003 ¶262.



And, as discussed in limitation 1[a], the light emitted from the LED chips 30 is reflected off the various exposed regions—including the walls and bottom of the reflective surface—that are exposed between the LED chips. *See also* EX1003 ¶263; §V.E.2 (1[a]). Notably, the '988 patent does not ascribe any particular shape for its reflective surface or metal substrate, stating only that its metal substrate has such a surface. *See generally* EX1001; EX1003 ¶263. Moreover, further confirming that there is no patentable significance to the shape of the reflective surface, the '988 patent states that the particular shapes—*e.g.*, the metal substrate having a reflective

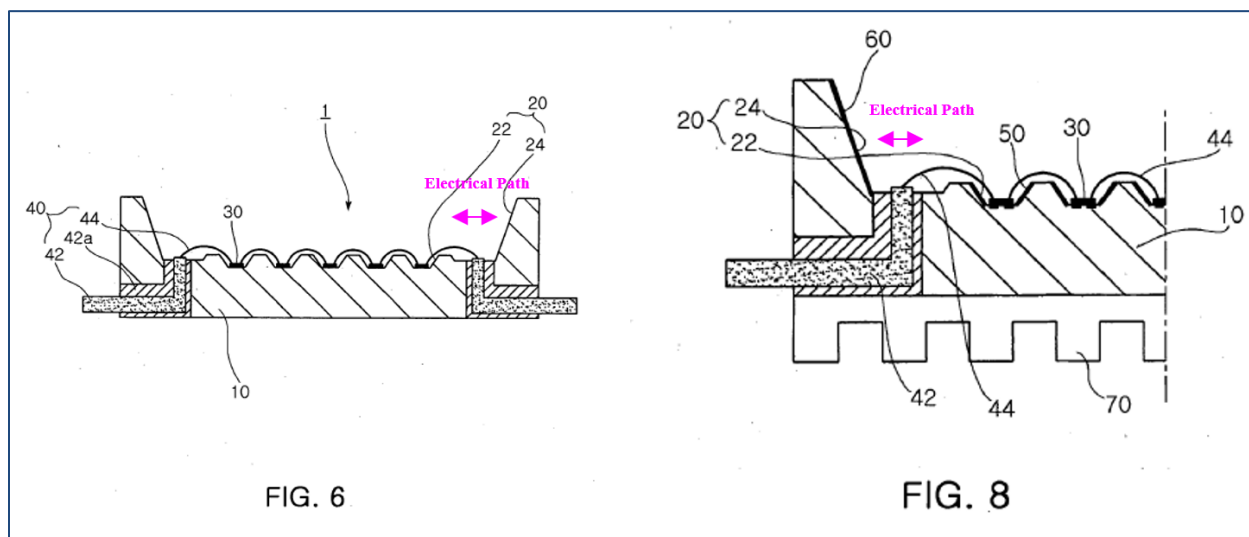
surface in Figure 3—“are not intended to limit the scope of [its] invention.” EX1001, 3:8-25; EX1003 ¶263.

1[d] “an electrical path formed by connecting the LED chips in a chip to chip fashion.”

Baek discloses limitation 1[d]. EX1003 ¶¶264-266.

Baek explains that “the lead frame is mounted on a main board of a device, and the connection unit 40 includes leads 42 attached to the base member 10 with insulating layers 42a interposed therebetween and bonding wires 44 for connecting the leads 42 with the LED chips 30. Then, the leads 42 are connected to an electric pattern on the main board.” EX1006, [0077]; EX1003 ¶265. In fact, Baek notes that that chip-to-chip configuration was already known in the art. EX1006, [0021]-[0030], FIGs. 1-4 (prior art packages); EX1003 ¶265.

Baek’s chip-to-chip connection forming an **electrical path** can be seen in Figure 6 and 8. EX1003 ¶266.



A POSA would have understood this disclosure as showing LED chips connected in a chip-to-chip fashion in the same manner as described by the '988 patent without a connection of the chips through the wires to the substrate. EX1003 ¶266; EX1001, 5:38-45, 6:18-21, FIG. 3; §§IV.A, C.

3. Claim 2

“...wherein the reflective surface comprises polished aluminum.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek in view of Cao630 renders claim 2 obvious. EX1003 ¶¶267-271.

Baek discloses using a base member and reflectors made of a “material capable of dissipating (radiating) heat such as Cu of excellent heat conductivity.” EX1006, [0072]-[0073]; EX1003 ¶268. Another known material capable of excellent heat conductivity is aluminum, which was commonly used as a substrate material in LED packages and could be readily substituted into Baek. EX1003 ¶269; EX1007, [0014] (Cao630 describing interchangeability of using various metals including copper and aluminum as the substrate so long as the “materials [have] adequate heat conductance”); EX1018, 10 (aluminum and copper are two of the most thermally conductive metals); EX1019, 4-157 (same). The interchangeability was further confirmed by the applicant during prosecution when it asserted that “[b]ecause in general metals have high thermal conductivity, such direct mounting results in creation of an efficient thermal path...” EX1002, 280; EX1003 ¶269.

Moreover, using aluminum instead of copper would advantageously provide for high reflectivity—stated goals in both Baek and Cao630—given that aluminum is highly reflective in the visible spectrum. EX1003 ¶270; EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1016, 3, FIG. 1; EX1017, 162, FIG. 1.

And, it would have been obvious to a POSA to polish the surface of the aluminum substrate to further enhance reflectivity in the LED package, for the same reasons discussed in Sections V.E.1-2. *See also* EX1003 ¶271; §§V.E.1-2.

4. Claim 3

“...wherein the reflective surface comprises silver plating.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—claim 3 for the same reasons as discussed above for limitation 1[a] (*i.e.*, when the reflective surface comprises silver plating as disclosed in Baek and commonly known to a POSA to enhance reflectivity and package performance). *See also* EX1003 ¶272; §§V.E.1, 3.

5. Claim 4

“...wherein the reflective surface has a reflectivity of 70% or greater.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—claim 4 for the same reasons as discussed above for limitation 1[a] and

claims 2 and 3 (*i.e.*, when the reflective surface is aluminum or silver, both of which have reflectivity of 70% or greater in the visible spectrum). *See also* EX1003 ¶¶273-274; EX1015, [0088], [0118]-[0119]; EX1027, 511, FIG. 11-1; EX1022, 376, FIG. 13.8; EX1016, 3, FIG. 1; EX1017, 162, FIG. 1; §§V.E.1-3.

6. Claim 5

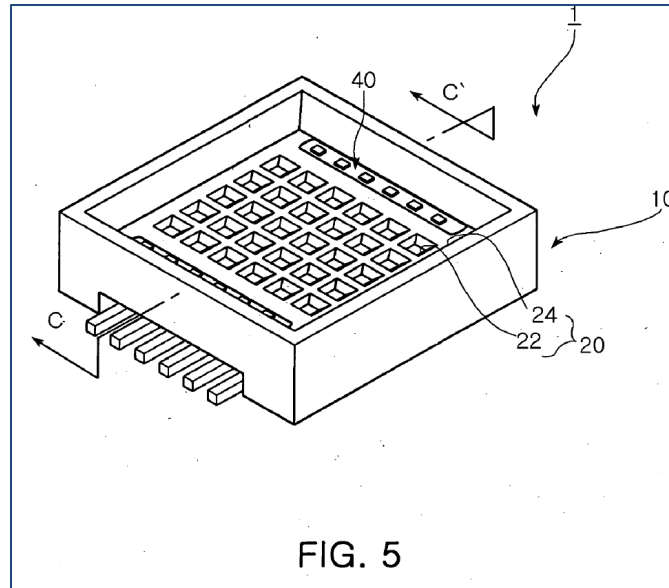
“...wherein the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—claim 5. EX1003 ¶¶275-280.

Baek discloses spacing apart the LED chips 30 surrounded by first reflectors 22 of the metal substrate, “thereby preventing light emitted from [] each LED chip from interfering with light emitted from adjacent one, which otherwise would degrade light efficiency.” EX1006, [0068]; *see also* [0063], [0082], [0089]; EX1003 ¶276.

Baek also discloses that a typical known LED is “fabricated in a very small size of about 0.25 mm, and mounted on a lead frame” and further that “[a] most typically used LED is provided in the form a 5 mm plastic package.” EX1006, [0012]-[0013]; EX1003 ¶277. Baek further notes that “LEDs are being further miniaturized” (*i.e.*, smaller than 0.25 mm). EX1006, [0014]; EX1003 ¶277.

Baek discloses in its Figures 5-7 embodiment an array of five by six LED chips, EX1006, FIGs. 5-7; EX1003 ¶278, which when used with a typical 5 mm package size as described by Baek (which would also apply to the lead frame substrates in Figures 5-7) would, as the application required, result in a spacing of greater than approximately 0.5 mm, consistent with Baek's design goal to prevent light interference from adjacent chips (thereby meeting claim 5's spacing requirement). EX1003 ¶279.



Further confirming the obviousness of the claimed spacing, it was well known in the art to a POSA to vary the spacing depending on the application requirements, and that a POSA would so space the LEDs to increase light efficiency within the package to avoid light interference from adjacent chips. EX1005, [0023]; EX1014, [0016]; EX1006, [0063], [0068], [0082], [0089]; EX1003 ¶280. This would confirm to a POSA that Baek's spacing met the claimed approximately 0.5 mm or greater,

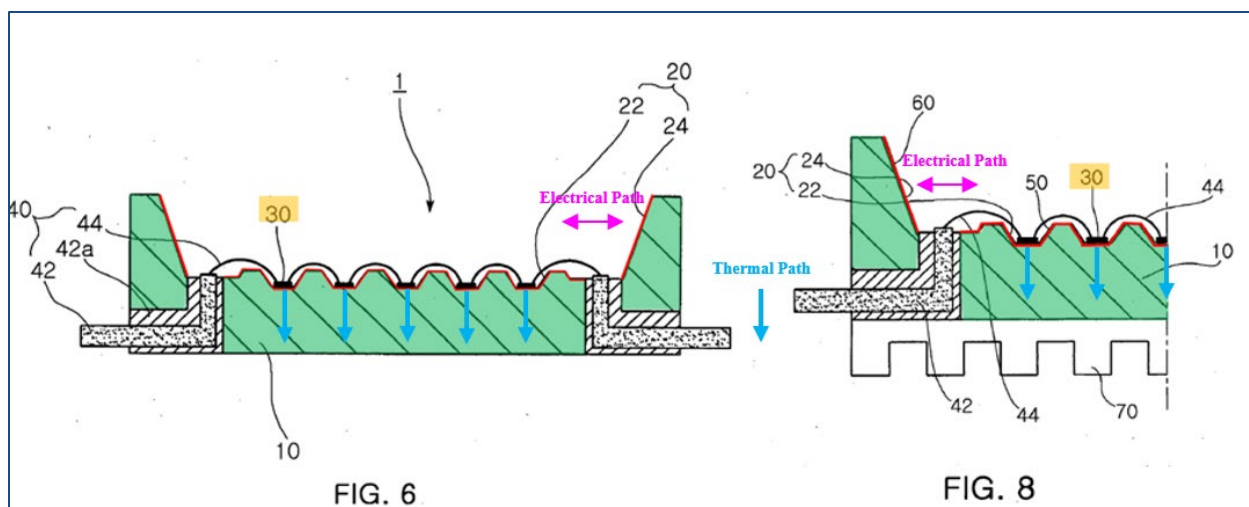
consistent with the '988 patent's disclosure that places no significance or criticality on effects of the particular 0.5 mm or greater spacing. *See generally* EX1001; EX1003 ¶280. Nor would there be any difficulty in routine experimentation and optimization to so space the LED chips, for the same reasons discussed in Section V.C (regarding claim 5). *See also K-Swiss*, 567 F. App'x at 91; *Gentiluomo*, 36 F. App'x at 439; *Gardner*, 725 F.2d at 1345-49; *Aller*, 220 F.2d at 456.

7. Claim 6

“...wherein the plurality of LED chips provide separate thermal and electrical paths.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek discloses claim 6 for the same reasons discussed above regarding limitations 1[b] and 1[d]. EX1003 ¶281-283.

As explained in limitation 1[b], Baek discloses a thermal path down from the LED chips directly into the substrate. *See also* EX1003 ¶282; §V.E.2 (1[b]). As explained in limitation 1[d], Baek discloses a separate, horizontal electrical path between LED chips that are wired together. *See also* EX1003 ¶282; §V.E.2 (1[d]). Thus, a POSA would have understood that Baek discloses its LED chips provide separate thermal and electrical paths—just as disclosed in the '988 patent. EX1003 ¶282. The separate **electrical path** and **thermal path** are depicted in Figures 6 and 8. EX1003 ¶283.



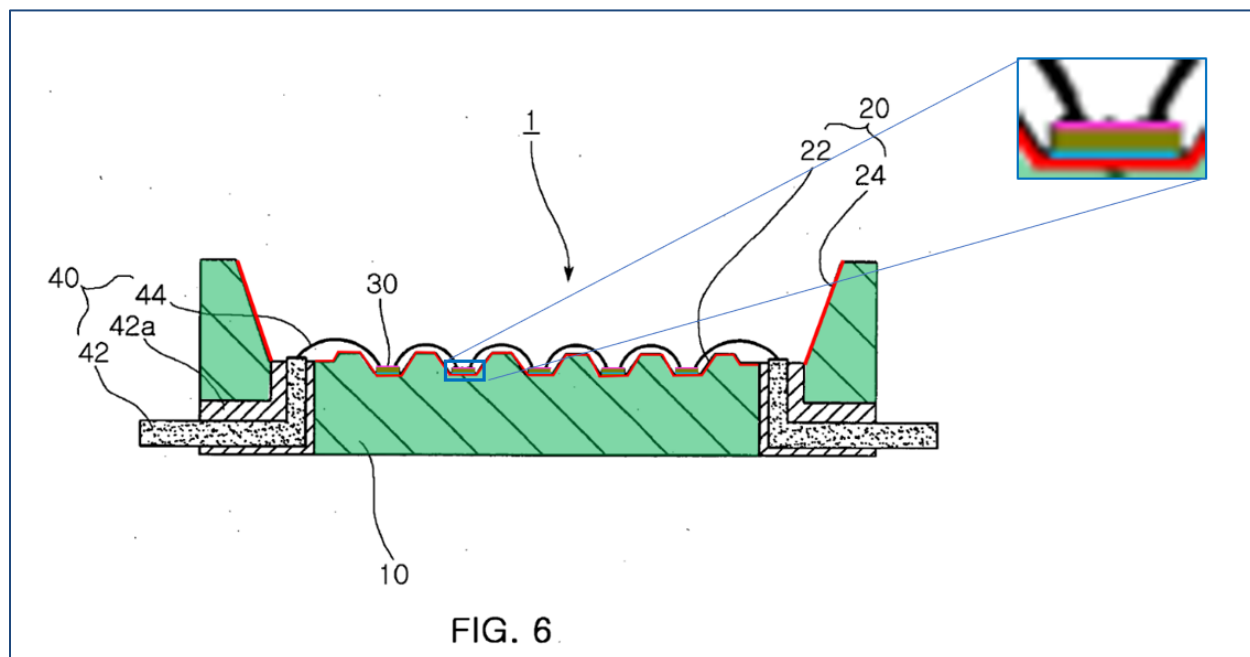
8. Claim 7

“...wherein the plurality of LED chips have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface.”

Baek alone or in view of Cao30 renders claim 1 obvious. §V.E.2. Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—claim 7. EX1003 ¶¶284-288.

Again, this claim effectively amounts to a conventional wire-bonded LED chip whereby the LED chip’s bottom surface is mounted to a substrate’s surface and the electrical contacts are provided on the opposite (top) surface(s). EX1003 ¶¶285-286, 74-76; EX1013, 95-96, FIG. 5.2.3(a); EX1011, 10:61-11:24, 12:61-13:30, FIGs. 17a, 18a, 24a, 25a. Wire-bonded LED chips in Baek are consistent and have a bottom and top surface. EX1006, [0005]-[0011], [0023], [0077] FIGs. 6-8; EX1003 ¶287. Figure 6 of Baek, for example, shows an LED chip’s **bottom surface**

mounted to the heat sink's **reflective surface** and the chip's **top surface(s)** that includes electrical contacts. EX1003 ¶288. The same would be true if Cao630's mounting techniques are implemented, as discussed in limitation 1[b]. *See also* EX1003 ¶256; §V.E.2 (1[b]).



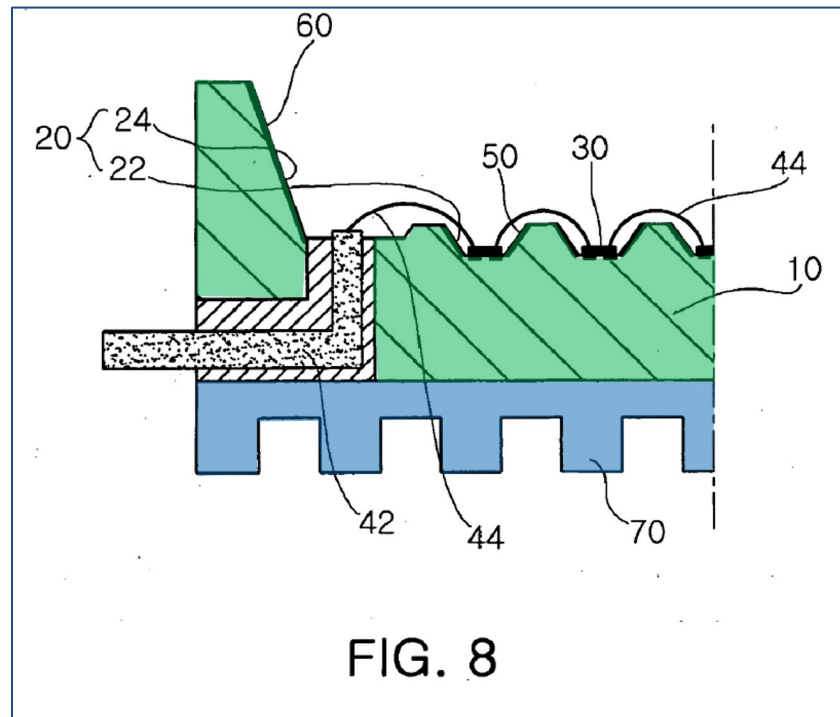
9. Claim 8

“...wherein the metal substrate is mounted directly to a heat sink.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—claim 8. EX1003 ¶¶289-294.

Baek discloses that the apparatus “may further comprise a heat sink plate underlying the base member.” EX1006, [0044], cl. 11; EX1003 ¶¶289-290. Baek also discloses in Figure 8 that “a **heat radiating plate 70** may be further applied to

the underside of the **base member 10.**” EX1006, [0086]; EX1003 ¶¶290-291. Baek explains that “[t]his may further enhance heat dissipating characteristics” of the apparatus. EX1006, [0087]; EX1003 ¶290.



Baek does not explicitly explain how the metal substrate is mounted to the heat sink, though it does not depict any intervening materials between the substrate and heat sink, indicating to a POSA there are none. EX1003 ¶292. Further, a POSA would have understood that there are many ways of mounting a metal substrate to a heat sink, including using a heat conductive adhesive or through other mounting means (as explained in Cao630) that would be consistent with the heat-dissipation goals of Baek and Cao630. EX1003 ¶¶292-293; EX1007, [0015], [0012], cls. 1, 12; EX1005, [0024], [0028], [0034], cls. 1, 12, 22. And, Patent Owner cannot credibly

argue there is anything novel or nonobvious about direct mounting the heat sink given the '988 patent's lack of such disclosure of how to do so. EX1001, 5:46-62, 6:23-26; EX1003 ¶294. *See Trustees of Columbia Univ.*, 620 F. App'x at 933; *Streck*, 665 F.3d at 1288.

10. Claim 9

“...wherein the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface.”

Baek alone or in view of Cao630 renders claim 1 obvious. §V.E.2. Baek discloses, or it would have been obvious to include as part of Baek—alone or in view of Cao630—claim 9. EX1003 ¶¶295-297.

As discussed regarding limitation 1[b], Baek discloses an electrical connection by connecting the LED chips directly to one another. *See also* EX1003 ¶296; §V.E.2 (1[b]). As shown in Figures 6-8 and also discussed regarding limitation 1[b], the LED chips 30 are wired together—without an electrical connection between the LED chips and the reflective surface (if there were, it would result in a short circuit). *See also* EX1003 ¶297; §V.E.2 (1[b]).

VI. The Board Should Not Deny Institution Under Sections 314(a) or 325(d)

A. The Board Should Not Deny Institution Under Section 314(a) Based on the Previous IPR Petition Filed By an Unrelated Party That Settled Prior to an Institution Decision

The Board should not exercise its discretion under 35 U.S.C. §314(a) to deny institution because: (i) this is Petitioner's *first and only* petition challenging the claims; (ii) Petitioner has *no* relationship with the prior petitioner (and is, in fact, a competitor); (iii) Petitioner had no knowledge of the '988 patent when the prior patent owner countersued the prior petitioner in 2017 or when the prior IPR petition was filed in 2018; (iv) the single, prior IPR petition settled and was terminated in 2018 *before* an institution decision (and so the Board did not consider the merits); (v) the '988 patent was not asserted in litigation again until June 2022 after being acquired by the current Patent Owner; and (vi) the prior IPR petition was filed years ago under a different claim construction standard (broadest-reasonable-interpretation) than in current use.

Accordingly, evaluation of the seven *General Plastic* factors⁵ weighs against using the Board's discretion to deny this petition without consideration on the merits,

⁵ *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, 9-10 (PTAB Sept. 6, 2017) (precedential).

especially where the present Petitioner is *different from and unrelated to* the petitioner in the earlier-filed IPR, which was terminated *pre-institution*, after which the '988 patent sat un-litigated for years until the current Patent Owner acquired it and filed its first suit in June 2022. *See Micron Tech., Inc. v. Sonrai Memory Ltd.*, IPR2023-00904, Paper 7, 8-9 (PTAB Nov. 29, 2023) (“Because this Petitioner has not previously filed a petition and Patent Owner does not assert extenuating circumstances ... factors 1-5 weigh against denial”; factors 6 and 7 “weigh against denying institution” because the “previous IPRs have all terminated due to settlement” leaving the petitioner’s IPR the only one pending); *Current Lighting Sols., LLC v. Jiazing Super Lighting Elec.*, IPR2023-00270, Paper 18, 45-47 (PTAB Aug. 16, 2023) (factors weighed against denial where instant petitioner (i) had “no significant relationship with” prior petitioner for which Board denied institution, and (ii) relied upon overlapping prior art but different arguments); *Alcatel-Lucent USA Inc. v. Oyster Optics, LLC*, IPR2017-02146, Paper 12, 12 (PTAB Feb. 28, 2018) (“Once resolution of factor 1 indicates that Petitioner had not previously filed a petition against the same patent, factors 2-5 bear little relevance unless there is evidence in the record of extenuating circumstances.”).

B. The Board Should Not Deny Institution Under Section 325(d) Because the Instant Petition Presents New Art and Arguments Not Previously Considered by the Patent Office

The Board should not exercise its discretion under 35 U.S.C. §325(d) to deny institution because no reference used as the basis for a Ground herein was cited by the Examiner or applied to the challenged claims. *See Apple Inc. v. Omni MedSci, Inc.*, IPR2020-00175, Paper 11, 11 (PTAB June 17, 2020); *Zip Top, LLC v. Stasher, Inc.*, IPR2018-01216, Paper 14, 35 (PTAB Jan. 17, 2019); *Amazon.com, Inc. v. M2M Sols. LLC*, IPR2019-01205, Paper 14, 16 (PTAB Jan. 27, 2020). In fact, of the references used as the basis for the Grounds in this Petition, *only* Baek was before the Examiner, and it was *not* relied upon by the Examiner in any rejection. EX1001, Cover Page; *see also generally* EX1002. Further, denial is unwarranted because: (i) all Grounds rely upon references not disclosed during prosecution; (ii) no rejection based on any reference or combination used herein was raised during prosecution; (iii) if the references in any Ground had actually been considered, the claims would have been found anticipated and/or obvious; and (iv) all Grounds rely upon the new testimony of Dr. Jokerst which explains how a POSA would have understood the prior art's teachings and state of the art, and why a POSA would have found the claims anticipated and/or obvious. *See Caterpillar Inc. v. Wirtgen Am., Inc.*, IPR2022-01278, Paper 12, 43 (PTAB Feb. 7, 2023); *Tesla, Inc. v. Arsus, LLC*,

IPR2022-01216, Paper 9, 7-8 (PTAB Dec. 23, 2022); *Amcol Int’l Corp. v. Oil-Dri Corp. of Am.*, IPR2022-01107, Paper 10, 12-14 (PTAB Dec. 5, 2022).

VII. Conclusion

The challenged claims are unpatentable. Petitioner requests cancellation.

Respectfully submitted,

REICHMAN, JORGENSEN, LEHMAN &
FELDBERG LLP

Dated: March 14, 2024

/Patrick Colsher/
Patrick Colsher (Reg. No. 74,955)
Lead Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

I hereby certify that this paper complies with the type-volume limitation of 37 C.F.R. §42.24 (as determined by the Microsoft Word word-processing system used to prepare this paper) because it contains 13,978 words, excluding the parts of the paper exempted by 37 C.F.R. §42.24(a).

REICHMAN, JORGENSEN, LEHMAN &
FELDBERG LLP

Dated: March 14, 2024

/Patrick Colsher/
Patrick Colsher (Reg. No. 74,955)
Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that the foregoing Petition for *Inter Partes* Review, the Exhibits listed on the List of Exhibits, and Power of Attorney were served on March 14, 2024, pursuant to 37 C.F.R. §§42.6 and 42.105 via Federal Express, upon the following at the correspondence address of record with the Patent Office for Patent Owner:

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6 McFaddin
San Antonio, TX 78261

Respectfully submitted,

REICHMAN, JORGENSEN, LEHMAN &
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Dated: March 14, 2024

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