

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Nichia Corp.,
Petitioner

v.

BX LED LLC,
Patent Owner

Case No. IPR2024-00542
Patent No. 8,567,988

DECLARATION OF NAN MARIE JOKERST, PHD

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I. ENGAGEMENT AND COMPENSATION

1. My name is Nan Marie Jokerst, PhD. I have been retained by Nichia Corp. (“Petitioner”) for the purpose of providing my opinion with respect to the patentability of claims 1-9 of U.S. Patent No. 8,567,988 (the “’988 Patent”).

2. I am being compensated for my time in preparing this declaration at my standard hourly rate, and my compensation is not dependent upon my opinions or the outcome of the proceedings. I have no stake in the outcome of this proceeding.

3. I am not an employee of Petitioner or any affiliate or subsidiary thereof.

4. This declaration summarizes the opinions I have formed to date. I reserve the right to modify my opinions, if necessary, based on further review and analysis of information that I receive subsequent to the filing of this declaration, including in response to positions that parties to the *inter partes* review proceeding, or their experts, may take that I have not yet seen.

II. QUALIFICATIONS

5. I have summarized in this section my educational background, career, publications, and other relevant qualifications. My full curriculum vitae is provided as Exhibit 1004, which I incorporate into this declaration by reference.

6. I am currently the J. A. Jones Distinguished Professor of Electrical and Computer Engineering at Duke University, and the Executive Director of the Duke University Shared Materials Instrumentation Facility, which includes the Duke University Cleanroom and Materials Characterization infrastructure. I completed a six-year appointment as the Associate Dean for Faculty Affairs and Community Engagement in the Pratt School of Engineering at Duke University in June, 2023. I received my B.S. in Physics from Creighton University in 1982, and my M.S. and Ph.D. degrees in Electrical Engineering from the University of Southern California in 1984 and 1989, respectively.

7. I am a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), a Fellow of the Optical Society of America (OSA), and I received an IEEE Third Millennium Medal in 2000.

8. I served on the U. S. National Academies Board on Global Science and Technology from 2010-2014, and I have served the IEEE Photonics Society as the Vice President for Technical Affairs, the Vice President for Conferences, and as an elected member of the Board of Directors. I also served the Atlanta IEEE Section as the Chair, Vice Chair, Treasurer, and Secretary over a four-year timespan. I was a member of the Editorial Board of IEEE Proceedings from 2016-2018. I served the OSA as the Chair of the Engineering Council, and I am currently an Associate Editor of *Optica*. I was awarded a National Science Foundation Presidential Young

Investigator Award in 1990, a DuPont Young Professor Award in 1989, a Newport Research Award in 1986, and a Hewlett Packard Fellowship in 1983. I received the University of Southern California Alumni in Academia award from the Viterbi School of Engineering in their 100th anniversary year, 2006. From 2015 through 2017, I served as the Chair of the Duke Academic Council, which is the Duke faculty senate.

9. I have served on the Duke University Electrical and Computing Engineering faculty as a full tenured Professor for 21 years (since 2003) after 14 years on the Electrical and Computer Engineering faculty at the Georgia Institute of Technology, where my ultimate rank was that of the Joseph Pettit Chaired Distinguished Professor of Electrical and Computer Engineering. A significant amount of my effort at Georgia Tech involved leadership and research in the National Science Foundation (NSF) funded Engineering Research Center at Georgia Tech: the Packaging Research Center. This Center was funded for 11 years by NSF for \$35M and involved over 30 faculty researchers and their research groups. I served as the co-Leader of the Optoelectronics and High Speed Electronics Thrust Area of the Packaging Research Center. In that role, I supervised multiple faculty researchers and led significant efforts in the integration and advanced packaging of optoelectronic devices, with support from companies that included Intel, Panasonic-Matsushita, Broadcom, National Semiconductor, Hitachi

Chemical, Kyocera, and Sony. For two years of the 9 years, I served as the Research Director of the entire Packaging Research Center. When I joined the Duke faculty in 2003, I supervised the design and upfit of Duke's new Shared Materials Instrumentation Facility (SMIF), a shared facility that has Duke, local, regional, and international users. SMIF is part of the Research Triangle Nanotechnology Network (RTNN), a partnership that I developed with North Carolina State University and the University of North Carolina at Chapel Hill, which is one of 16 sites funded by the National Science Foundation to serve as national resources for research, education, workforce development, and outreach in nanotechnology.

10. My research work has focused on the design, simulation, fabrication, integration, packaging, and application of semiconductor optoelectronic devices and waveguide devices for integrated fiber and planar optical interconnect systems, medical diagnostic systems, "smart pixel" systems, and chip scale integrated sensors and systems. I hold 7 patents and have authored over 295 peer reviewed journal and conference publications. Much of my research, many of my published papers, my IEEE Fellow and my OSA Fellow citations, and the majority of my patents are in the field of optical devices and integrated optoelectronic devices. I have consulted for the design and commercialization of optical and optoelectronic telecommunication and interconnection products with companies that include Cypress Semiconductor and Broadcom, as well as performed technology

evaluations for Windermere and the American Society for the Advancement of Science (AAAS). My research has been supported by companies that include BellSouth, Ford, Intel, Sony, Panasonic-Matsushita, Kyocera, National Semiconductor, Hitachi Chemical, Ford Visteon, and Delco, as well as government agencies that include the Defense Advanced Research Projects Agency (DARPA), the Army Research Office, the Office of Naval Research, the Naval Air Warfare Center, the Air Force Office of Scientific Research, the National Institutes of Health, and the National Science Foundation.

11. In addition to my research awards, I have also been recognized for my teaching accomplishments, which include the award for Best Teacher in Electrical Engineering at Georgia Tech in 1990, and the IEEE Education Society/Hewlett Packard Harriet B. Rigas Medal in 2002. I am a co-author of the three-volume book set “Microelectronics Packaging Handbook,” and I am an internationally recognized expert and speaker in optics, photonics, and integration/packaging. I have served on and Chaired review panels for organizations that include the Army Research Office in 2017 and the Scientific Foundation of Ireland in 2015 and 2017, as well as serving as a plenary speaker initiating the new Indian Institute of Technology Nanotechnology Center in Mandi, India in 2018. My undergraduate and graduate classes focus on optics and photonics, optoelectronic devices, and optical systems, as well as First Year Design and Senior Capstone Design courses.

These classes contain both theoretical groundwork as well as practical, hands-on design/build/operate content. I also created and originated the massively online Coursera course “Nanotechnology: A Maker’s Course,” which has had over 40,000 active learners since its release.

12. As a researcher, teacher, and consultant in the area of optoelectronic devices and integration/packaging, I am intimately familiar with the hardware technology associated with LEDs and LED packaging. I have personally led the design, fabrication, testing, and publication of original research in the area of optoelectronic devices that include LEDs, lasers, and photodetectors for applications such as transceivers, optical interconnections, and medical instruments. Through my research and leadership in the NSF-funded Packaging Research Center, I focused on many key challenges facing integrated electronic and optoelectronic systems, including thermal management. My activities in the Packaging Research Center focused on the packaging and integration of optoelectronic devices, however, as a co-Leader of the Center I followed all aspects of the Center research, and during my time as Research Director, I had oversight over the research activities of the entire Center, including the thermal management work, which was located in the Assembly, Reliability, and Thermal Management or “ART” research group. Thus, while I have not personally published in the field of thermal management, I am knowledgeable in that technology area.

III. SUMMARY OF OPINIONS

13. In my opinion, a person of ordinary skill in the art (“POSA” or “POSITA”) would have found the subject matter of claims 1-9 of the ’988 Patent (Ex. 1001), to be anticipated and/or obvious in view of the following prior art:

- **Ground 1:** U.S. Patent App. Pub. No. 2005/0174753 to Cao *et al.* (“Cao753”; Ex. 1005) anticipates claims 1 and 4-9;
- **Ground 2:** Cao753 (Ex. 1005) renders claims 1 and 4-9 obvious;
- **Ground 3:** Cao753 (Ex. 1005) alone or in view of U.S. Patent App. Pub. No. 2004/0256630 to Cao (“Cao630”; Ex. 1007) renders claims 2-4 obvious; and
- **Ground 4:** U.S. Patent App. Pub. No. 2007/0075325 to Baek *et al.* (“Baek”; Ex. 1006) alone or in view of Cao630 (Ex. 1007) renders claims 1-9 obvious.

IV. MATERIALS REVIEWED

14. In forming my opinions, I have relied on my knowledge of the field and my experience, and have specifically reviewed the following exhibits:

Ex. No.	Description	Abbreviation
1001	U.S. Patent No. 8,567,988	’988 Patent
1002	File History of U.S. Patent No. 8,567,988	
1005	U.S. Patent App. Pub. No. 2005/0174753 to Cao <i>et al.</i>	Cao753
1006	U.S. Patent App. Pub. No. 2007/0075325 to Baek <i>et al.</i>	Baek
1007	U.S. Patent App. Pub. No. 2004/0256630 to Cao	Cao630
1008	Patent Owner’s Responsive Claim Construction Brief, Dkt. 28, dated Feb. 17, 2023, in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.) (excerpt)	

Ex. No.	Description	Abbreviation
1009	Patent Owner's Sur-Reply Claim Construction Brief, Dkt. 32, dated Mar. 24, 2023, in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.) (excerpt)	
1010	Declaration of John K. Roberts in Support of Patent Owner's Responsive Claim Construction Brief, Dkt. 28-1, dated Feb. 17, 2023, in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.) (excerpt)	
1011	U.S. Patent No. 6,969,253 to Cao	Cao253
1012	Graf, Rudolf, <u>Modern Dictionary of Electronics</u> , 7 th Ed. (1999) (excerpt)	Graf
1013	Zukauskas, Arturas, <u>Introduction to Solid-State Lighting</u> , John Wiley & Sons, Inc. (2002) (excerpt)	Zukauskas
1014	U.S. Patent App. Pub. No. 2004/0119975 to Ostler <i>et al.</i>	Cao975 ¹
1015	U.S. Patent App. Pub. No. 2008/0055901 to Sanpei <i>et al.</i>	Sanpei
1016	Thomas, N., <u>High Reflectivity of Silver Extended Down to 200 NM</u> , <i>Optical Interference Coatings</i> , OSA Technical Digest Series, Optica Publishing Group (2001)	Thomas
1017	Bartek, M., <u>Silver-based reflective coatings for micromachined optical filters</u> , J. Micromech. Microeng. 9 (1999)	Bartek
1018	Pecht, Michael, <u>Electronic Packaging: Materials and Their Properties</u> , CRC Press (1999) (excerpt)	Pecht
1019	Fink, Donald, <u>Standard Handbook for Electrical Engineers</u> , 14th Ed., McGraw-Hill Book Co. (2000) (excerpt)	Fink
1020	U.S. Patent App. Pub. No. 2005/0023538 to Ishii <i>et al.</i>	Ishii
1021	U.S. Patent App. Pub. No. 2004/0065894 to Hashimoto <i>et al.</i>	Hashimoto
1022	Fischer, T., <u>Materials Science for Engineering Students</u> , Academic Press (2009) (excerpt)	Fischer

¹ I note that Calvin Ostler is listed as the first named inventor, and Densen Cao is listed second for this reference (Ex. 1014). Given the similarities with the other Cao references, I refer to this reference (Ex. 1014) as "Cao975" in my declaration.

Ex. No.	Description	Abbreviation
1023	Infringement Contentions in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (excerpt)	
1024	Bridgelux's Opening Claim Construction Brief in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (excerpt)	
1025	Bridgelux's Reply Claim Construction Brief in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (excerpt)	
1026	Everlight's Responsive Claim Construction Brief in <i>Everlight Electronics Co., Ltd. v. Bridgelux, Inc.</i> , No. 4:17-cv-03363-JSW (N.D. Cal.) (excerpt)	
1027	Ohring, Milton, <u>The Materials Science of Thin Films</u> , Academic Press (1992) (excerpt) ("Ohring")	Ohring
1028	Amended Claim Construction Order in <i>BX LED LLC v. Walmart Inc.</i> , No. 6:22-cv-00445 (W.D. Tex.)	

V. UNDERSTANDING OF THE RELEVANT LAW

A. Anticipation

15. I have been informed and understand that a patent claim is anticipated when a single piece of prior art describes every element of the claimed invention, arranged in the same way as in the claim, either expressly or inherently. I have been told to consider elements to be inherently described only if they are necessarily present in the piece of prior art.

B. Obviousness

16. I have been informed and understand that a patent claim is unpatentable and invalid if the subject matter of the claim as a whole would have been obvious to a person of ordinary skill in the art in the field of the patent as of

the time of the invention at issue.² I have been informed and understand that the following factors must be evaluated to determine whether the claimed subject matter is obvious: (i) the scope and content of the prior art; (ii) the difference or differences, if any, between each claim of the patent and the prior art; (iii) the level of ordinary skill in the art at the time the patent was filed; and (iv) any objective indicia of non-obviousness.

17. I have been informed and understand that the objective indicia of non-obviousness (or “secondary considerations”) that should be considered include, for example, the following: (i) commercial success; (ii) long-felt but unresolved needs; (iii) copying of the invention by others in the field; (iv) initial expressions of disbelief by experts in the field; (v) failure of others to solve the problem that the inventor solved; and (vi) unexpected results. I have been informed and understand that evidence of these objective indicia must be commensurate in scope with the claimed subject matter. I am not aware of any objective indicia of non-obviousness relevant to the claims of the ’988 Patent.

18. I have been informed and understand that independently made, simultaneous inventions, made within a comparatively short space of time, are

² As I discuss in Section VI, below, I use the shorthand “POSA” (or “POSITA”) to describe this person.

evidence that the claimed apparatus was the product only of ordinary mechanical or engineering skill.

19. In determining whether the subject matter as a whole would have been obvious at the time that the invention was made to a person having ordinary skill in the art, I have been informed of and understand certain principles regarding the combination of elements of the prior art. A combination of familiar elements according to known methods is likely to be obvious when it yields predictable results. Also, if a person of ordinary skill in the art can implement a predictable variation in a prior art device, and would see the benefit from doing so, such a variation would be obvious. In particular, when there is pressure to solve a problem and there are a finite number of identifiable, predictable solutions, it would be reasonable for a person of ordinary skill to pursue those options that fall within his or her technical grasp. If such a process leads to the claimed invention, then the latter is not a patentable invention, but the result of ordinary skill and common sense.

20. I have also been informed and understand that a teaching, suggestion, or motivation is a useful guide in establishing a rationale for combining elements of the prior art. The test poses the question as to whether there is an explicit teaching, suggestion, or motivation in the prior art to combine prior art elements in a way that realizes the claimed invention. Though useful to the obviousness inquiry,

I understand that this test should not be treated as a rigid rule. It is not necessary to seek out precise teachings; it is permissible to consider the inferences and creative steps that a person of ordinary skill in the art (who is considered to have an ordinary level of creativity and is not an automaton) would employ.

C. Claim Construction

21. I have been informed and understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I have been informed and understand that under this standard, the meaning of claim terms is considered from the viewpoint of one of ordinary skill in the art at the time of the invention.

22. I have been informed and understand that claim terms are generally given their plain and ordinary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I have been informed and understand, however, that claim terms are generally not limited by the embodiments described in the specification.

23. I have been informed and understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed and understand that this other evidence is

often less significant and less reliable than the claims, specification, and prosecution history.

VI. LEVEL OF ORDINARY SKILL IN THE ART

24. I have been informed and understand that the disclosure of patents and prior art references are to be viewed from the perspective of a person having ordinary skill in the art at the time of the alleged invention. I use the shorthand “POSA” (or “POSITA”) to describe this person. I have provided my opinions from this perspective. I understand that the relevant time period is around September 2008, the filing date of the application leading to the ’988 Patent.

25. I have been informed and understand that prior art references can provide evidence of the level of ordinary skill in the art, and that factors that may be considered in determining this level of skill can include the educational level of the inventors and active workers in the field, the types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, and the sophistication of the technology.

26. Based on my education and experience, as described above and in my CV, as well as consistent with the ’988 Patent and the prior art described below, it is my opinion that those of ordinary skill in the art during the relevant period would have had at least a bachelor’s degree in electrical engineering, materials science, or a related field, and three years’ experience in the field of LED package design,

including optical design and thermal management. However, I note that this description is approximate, and a higher level of education or skill might make up for less experience, and additional experience could make up for a lower education level.

27. Given my experience in the field, I am familiar with the knowledge that a person of ordinary skill in the art would have had at the time and how such a person would have viewed the available information at the time. My testimony is offered from this perspective, even if it does not specifically refer to the perspective of a person of ordinary skill in the art in every instance.

VII. OVERVIEW OF THE '988 PATENT

28. The '988 Patent "relates generally to light emitting diodes, and more particularly, to an efficient LED array." Ex. 1001 at 1:6-7.

29. The '988 Patent provides a "Background" section. Ex. 1001 at 1:8-53.

30. According to the "Background" of the '988 Patent:

A light emitting diode (LED) is a semiconductor material impregnated, or doped, with impurities. These impurities add "electrons" and "holes" to the semiconductor, which can move in the material relatively freely. Depending on the kind of impurity, a doped region of the semiconductor can have predominantly electrons or holes, and is referred to as an n-type or p-type semiconductor region, respectively. In LED applications, the semiconductor includes an n-type semiconductor region and a p-type semiconductor region. A reverse electric field is created at the junction between the two regions, which cause the electrons and holes to move away from

the junction to form an active region. When a forward voltage sufficient to overcome the reverse electric field is applied across the p-n junction, electrons and holes are forced into the active region and combine. When electrons combine with holes, they fall to lower energy levels and release energy in the form of light.

Ex. 1001 at 1:9-25.

31. The '988 Patent further states, in its "Background" section, that:

During operation, a forward voltage is applied across the p-n junction through a pair of electrodes. The electrodes are formed on the semiconductor material with a p-electrode formed on the p-type semiconductor region and an n-electrode formed on the n-type semiconductor region. Each electrode includes a wire bond pad that allows an external voltage to be applied to the LED.

Ex. 1001 at 1:26-32.

32. The '988 Patent further states, in its "Background," that "Generally, a device having multiple LED chips is created by mounting closely spaced LED chips on a ceramic substrate." Ex. 1001 at 1:33-35. However, the '988 Patent states that this leads to certain problems:

Unfortunately, the closely spaced LED chips may interfere with each other and result in reduced light output. Also, a ceramic substrate is used because the LED chips have thermal and electrical paths that come in contact with each other. For example, an LED chip may have electrical contacts on both top and bottom surfaces so that when the chip is mounted to a substrate, both heat and electricity may pass to the substrate. Thus, the ceramic substrate provides electrical insulating properties while allowing some heat to pass. Unfortunately, the ceramic substrate doesn't provide a very efficient thermal path so that heat generated by the closely spaced LED chips may

degrade light output. To facilitate heat dissipation, the ceramic substrate may be mounted to an aluminum heat spreader, which i[n] turn is mounted to an additional heat sink. This arrangement is costly and results in more complicated manufacture.

Ex. 1001 at 1:35-50.

33. Thus, according to the '988 Patent, “there is a need in the art for improvements in LED devices to increase light output, provide efficient heat dissipation, and simplify manufacture.” Ex. 1001 at 1:51-53.

34. The '988 Patent then teaches to address this “need” through “a light emitting diode apparatus ... that comprises a metal substrate having a reflective surface, and a plurality of LED chips mounted directly to the reflective surface of the metal substrate to allow for thermal dissipation, and wherein at least a portion of the LED chips are spaced apart from each other to allow light to reflect from a portion of the reflective surface that is located between the portion of the LED chips.” Ex. 1001 at 1:57-64.

35. I note that the '988 Patent describes certain relative terms, including “on” in comparison to “directly on”:

It will be understood that when an element such as a region, layer, section, substrate, or the like, is referred to as being “on” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present. It will be further understood that when an element is referred to as being “formed” on another element, it can be grown,

deposited, etched, attached, connected, coupled, or otherwise prepared or fabricated on the other element or an intervening element.

Ex. 1001 at 3:26-36 (emphasis added).

36. The '988 Patent includes five figures, Figures 1-5.

37. In my declaration, for ease of reference, coloring has been added to certain figures to highlight certain elements (*i.e.*, the figures in the patent are all black-and-white, and so any coloring in the figures in my declaration has been added to the figures from the patent).

38. Figure 1 “shows top and side views of an exemplary LED chip for use in aspects of an efficient LED array”. Ex. 1001 at 2:44-45. More particularly, the side view 110 of Figure 1, shown below, shows “**LED chip 100** [that] comprises a bottom mounting surface 112 that can be used to mount the LED chip 100 to a substrate.” Ex. 1001 at 4:37-39 (color added). The '988 Patent states that “any suitable adhesive may be used to mount the LED chip 100 to the substrate.” Ex. 1001 at 4:40-41. As I discuss below, including in Sections IX.A.1, IX.B.5, and IX.E.8, the '988 Patent discloses a conventional wire-bonded LED chip with p and n contacts opposite to the surface used to mount the chip to a substrate.

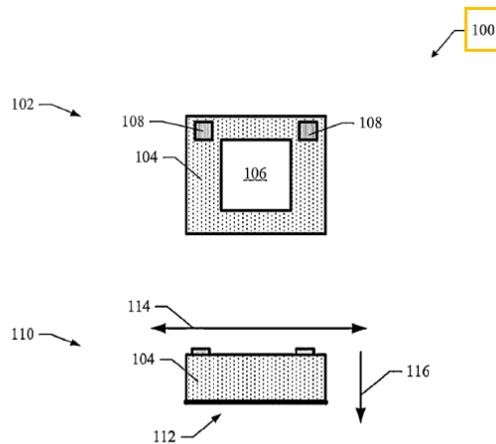


FIG. 1

Ex. 1001, FIG. 1 (coloring added).

39. According to the '988 Patent, “the electrical contacts 108 on the top surface of the LED chip 100 form a horizontal electrical path as illustrated by the arrow 114”, (the horizontal arrow 114 in the side-view portion of Figure 1 above), and “Since there are no electrical connections in contact with the mounting surface 112 of the LED chip 100, it can be mounted directly to a metal substrate without the need for an insulating dielectric.” Ex. 1001 at 4:41-47.

40. The '988 Patent also states that this mounting results in “an efficient thermal path” (the vertical downward arrow 116 in the side-view figure above): “By mounting the LED chip 100 directly on a metal substrate, an efficient thermal path is created (as indicated by the arrow 116) to allow heat to pass from the LED chip 100 to the metal substrate. By providing the efficient thermal path 116, the LED chip 100 is able to reduce or minimize any loss in optical power due to the effects of heating.” Ex. 1001 at 4:47-53.

41. Figure 2 “shows an exemplary LED array constructed in accordance with aspects of the present invention”. Ex. 1001 at 2:46-47. In Figure 2, shown below, “The LED array 200 comprises a **metal substrate 204** that has a **reflective surface 206**.” Ex. 1001 at 4:61-63 (color added). The ’988 Patent states that, “For example, the metal substrate may be constructed from aluminum and the reflective surface 206 may be bare or polished aluminum” or that “Alternatively, the reflective surface 206 may be formed by silver plating on the substrate 204.” Ex. 1001 at 4:63-66, 6:1-3. More generally, the ’988 Patent states that “the reflective surface 206 may be formed from any suitable material and formed upon the substrate 204 in any suitable way” and that “In various aspects, the reflective surface 206 has a reflectivity index of 70% or greater.” Ex. 1001 at 4:67-5:3.

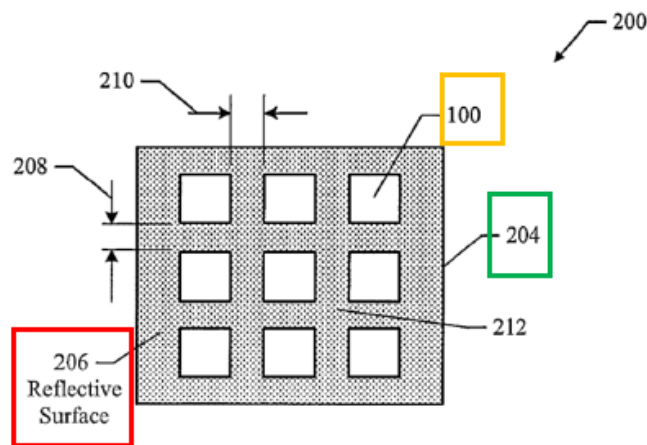


FIG. 2

Ex. 1001, FIG. 2 (coloring added).

42. I note that, as I discuss in my analysis below, including in Section IX.B.2, the disclosed reflectivity index of 70% or greater of the reflective surface is simply a property of certain metals, including the disclosed aluminum or silver, in the visible spectrum (*i.e.*, the spectrum relevant to the '988 Patent, which is concerned with making an LED apparatus that emits visible light for use in a lamp or light such as “an automobile headlamp, street light, overhead light, or in any other general illumination application”, Ex. 1001 at 6:34-47, FIG. 5). The metal reflectivity properties are explained in basic textbooks and in literature from before or around the time of the '988 Patent's filing date, such as Ohring (Ex. 1027 at 511 (Figure 11-1)), Fischer (Ex. 1022 at 376 (Figure 13.8)), Thomas (Ex. 1016 at 3 (Figure 1)) and Bartek (Ex. 1017 at 162 (Figure 1)).

43. The '988 Patent further states, in reference to Figure 2, that “the LED array 200 is mounted on the substrate 204 with a pre-determined spacing”, and that “For example, the LED chips are mounted having a vertical spacing as indicated at 208, and a horizontal spacing as indicated at 210. In various aspects, the horizontal and vertical spacing between the LED chips is 0.5 millimeters or greater.” Ex. 1001 at 5:16-21. The '988 Patent states that the result of the pre-determined spacing is that it “exposes regions 212 of the reflective surface 206 between the LED chips” and that “By exposing these regions 212, light emitted from the LED chips may reflect off the exposed portions of the reflective

surface 206 to increase the amount of light output from the LED array.” Ex. 1001 at 5:21-26.

44. Figure 3, shown below, “shows an exemplary efficient LED array apparatus 300 constructed in accordance with aspects of the present invention.” Ex. 1001 at 5:30-32. “The apparatus 300 comprises the LED array 200 with LED chips (i.e., LED 100) mounted directly to the **reflective surface 206** at a pre-determined spacing to expose regions of the reflective surface to allow light to reflect from the reflective surface located between the LED chips as illustrated at 308.” Ex. 1001 at 5:32-37 (color added). The **substrate 204** and **LED chips 100** are not labeled in Figure 3, but for reference, these have been colored to highlight them.

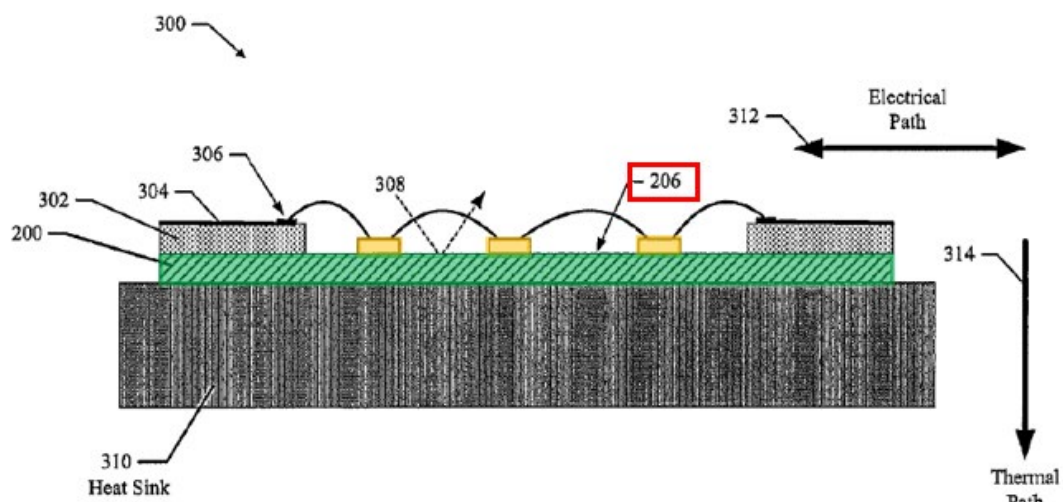


FIG. 3

Ex. 1001, FIG. 3 (coloring added).

45. “To enable electrical connections, a layer of dielectric insulator 302, which may be aluminum oxide, is mounted to the aluminum metal substrate of the LED array 200.” Ex. 1001 at 5:38-40. “On top of the dielectric 302 copper traces 304 are run to a bonding pad 306. Bonding wires are then routed from the bonding pad 306 in a chip to chip fashion so that power may be applied [sic: applied] to all chips in the LED array 200.” Ex. 1001 at 5:40-44. The ’988 Patent states that the result of this is that “an electrical path is formed as illustrated at 312” (horizontal arrow in Figure 3). Ex. 1001 at 5:44-45.

46. In Figure 3, “The LED array 200 is mounted directly to a heat sink 310,” which “comprises any suitable material”. Ex. 1001 at 5:46-47. The ’988 Patent further states that “the LED array 200 is mounted directly to the heat sink 310 without any dielectric insulation”, which “provides for efficient transfer of heat from the metal substrate of the LED array 200 to the heat sink 310.” Ex. 1001 at 5:47-58. According to the ’988 Patent, “Since the LED chips are mounted directly to the aluminum substrate and the aluminum substrate is mounted directly to the heat sink 310, an efficient thermal path is formed as illustrated at 314” (vertical arrow in Figure 3), and the “thermal path allows heat generated at the LED chips to be dissipated through the metal substrate and into the heat sink 310, thereby reducing the degrading effects of heat on light output.” Ex. 1001 at 5:55-62.

47. I have also reviewed the file history (Ex. 1002) for the application leading to the '988 Patent. I note that during prosecution of the application that led to the '988 Patent, the applicant distinguished a reference called "Yamada", which the applicant stated was a "a *machine* translation". Ex. 1002 at 279 (emphasis supplied by the applicant). The applicant made several statements related to the "directly mounting" limitation.

48. For example, the applicant stated:

To set the stage for the discussion, it is noted that the term "directly" is defined as excluding any intervening elements (between the plurality of LED chips and the surface of metal substrate), *cf.*, above-identified application paragraph [0019]. Because in general metals have high thermal conductivity, such direct mounting results in creation of an efficient thermal path allowing heat to pass from the plurality of LED chips to the metal substrate, *cf.* claim 1, application paragraph [0026]. As such, the claim language is not an intended use, but limitation, as explained below.

Ex. 1002 at 280. Application paragraph [0019] (Ex. 1002 at 7-8) refers to 3:26-36 of the '988 Patent, and application paragraph [0026] (Ex. 1002 at 9-10) refers to 4:37-53 of the '988 Patent.

49. The applicant also argued that Yamada did not teach direct mounting, emphasizing that Yamada had an "insulating layer":

Turning now an attention to the cited portion of Yamada et al., it is noted that the *recitation* does *not* indicate that the LEDs are bonded *directly to* the metallic base as per the meaning of the term as defined in the above-identified application. Referring to paragraph [0018] of Yamada et al., it is disclosed (emphasis supplied):

"In the figure, 1 is a metallic base which has a reflex function, *high reflection materials*, such as white, *are applied to the substrate* which uses as a base material metal with a good radiation characteristic which served as the *insulating layer*, or mirror finish is performed."

Ex. 1002 at 280-81.

50. The applicant continued to explain its view of why Yamada was different than the claim requirement of directly mounting the LED to the substrate surface, including because of the additional "intervening insulating materials":

The recitation appears to disclose that an *additional* electrical insulator - note the *indefinite* article introducing the term “electrical insulator” is applied to the metallic base, to which reflective material with *insulating* properties was already applied.

For statements with the *same* import, *cf.*, e.g., claims 1 and 2; paragraphs [0011], [0033]-[0034] of Yamada et al.

Based on the foregoing, it appears that a *high reflective material* with *insulation properties* is applied on the metallic base of the substrate and an additional electrical *insulator* is applied on the high reflective material.

This interpretation signifies the fact that the LED chips are *not mounted directly* to the reflective surface of the metal substrate as the term is defined, because of the presence of an *intervening insulating* materials applied to the metallic base substrate.

Ex. 1002 at 282.

51. After prosecution, the '988 Patent issued with nine claims, independent claim 1 and dependent claims 2-9.

VIII. CLAIM CONSTRUCTION

52. In comparing the claims of the '988 Patent to the prior art, I have carefully considered the '988 Patent and its file history based upon my experience and knowledge in the relevant field (discussed in Section II above and in my CV (Ex. 1004)). As relevant to determining the patentability of the claims of the '988 Patent in this proceeding, the proper interpretation of the claim terms of the '988 Patent is consistent with the terms' plain and ordinary meaning in view of the

evidence of record (including the intrinsic evidence of record, *i.e.*, the patent and file history, as well as any extrinsic evidence), as a POSA would understand them, as of the time of the invention of the '988 Patent.

53. In my analysis of the prior art in comparison to the claims, I have at times explained how the prior art would anticipate or render obvious the relevant claims, regardless of the particular construction adopted (for example, related to the claim limitation “*a plurality of LED chips mounted directly to the reflective surface of the metal substrate*” in independent claim 1, and by dependency, dependent claims 2-9).

54. Although it does not impact my opinions on patentability, because the prior art discloses the limitations regardless of the construction, I discuss three terms that have been involved in prior claim construction (Exs. 1008-1010, 1024-1026, 1028).

Term No. 1: “a plurality of LED chips mounted directly to the reflective surface of the metal substrate”

55. Regarding the limitation, “*a plurality of LED chips mounted directly to the reflective surface of the metal substrate*”, as I explain below in Section IX, the prior art discloses the claim limitation regardless of whether “*mounted directly*”: (i) allows for the use of an adhesive or a “suitable adhesive” where no additional

intervening materials are present (such as an insulating dielectric); or (ii) does not allow for any adhesive or intervening material.

56. I explain the bases for both interpretations in the following paragraphs (again, though, the particular interpretation does not impact my opinions, as the prior art discloses both).

57. Regarding the former (suitable adhesive), there are three items that would support this view.

58. **First**, as I explained in Section VII (Overview of the '988 Patent), the '988 Patent discloses to use “any suitable adhesive,” which results the LED chip being mounted “directly to a metal substrate without need for an insulating dielectric”:

Referring now to the side view 110, it can be seen that the LED chip 100 comprises a bottom mounting surface 112 that can be used to mount the LED chip 100 to a substrate. For example, **any suitable adhesive may be used to mount the LED chip 100 to the substrate.** As can be further seen in the side view 110, the electrical contacts 108 on the top surface of the LED chip 100 form a horizontal electrical path as illustrated by the arrow 114. **Since there are no electrical connections in contact with the mounting surface 112 of the LED chip 100, it can be mounted directly to a metal substrate without the need for an insulating dielectric.** By mounting the LED chip 100 directly on a metal substrate, an efficient thermal path is created (as indicated by the arrow 116) to allow heat to pass from the LED chip 100 to the metal substrate. By providing the efficient thermal path 116, the LED chip 100 is able to reduce or minimize any loss in optical power due to the effects of heating.

Ex. 1001 at 4:37-53 (emphases added). This supports the concept that direct mounting can be done using a suitable adhesive (*e.g.*, one that is heat conductive) and where there is no additional insulating material between the LED chip and substrate.

59. I note that the '988 Patent does not describe any other methods for mounting the LED (direct or otherwise, regardless of the meaning of direct mounting).

60. **Second**, as I explained in Section VII, during prosecution, the applicant argued that a machine translation of Yamada did not teach direct mounting, emphasizing that Yamada had an “insulating layer”:

Turning now an attention to the cited portion of Yamada et al., it is noted that the *recitation* does *not* indicate that the LEDs are bonded *directly* to the metallic base as per the meaning of the term as defined in the above-identified application. Referring to paragraph [0018] of Yamada et al., it is disclosed (emphasis supplied):

“In the figure, 1 is a metallic base which has a reflex function, *high reflection materials*, such as white, *are applied to the substrate* which uses as a base material metal with a good radiation characteristic which served as the *insulating layer*, or mirror finish is performed.”

Ex. 1002 at 280-81.

61. Also, as I discussed in Section VII, the applicant explained their view of why Yamada was different than the claim requirement of directly mounting the LED to the substrate surface including because of the additional “intervening insulating materials”:

The recitation appears to disclose that an *additional* electrical insulator - note the *indefinite* article introducing the term “electrical insulator” is applied to the metallic base, to which reflective material with *insulating* properties was already applied.

For statements with the *same* import, *cf.*, e.g., claims 1 and 2; paragraphs [0011], [0033]-[0034] of Yamada et al.

Based on the foregoing, it appears that a *high reflective material* with *insulation properties* is applied on the metallic base of the substrate and an additional electrical *insulator* is applied on the high reflective material.

This interpretation signifies the fact that the LED chips are *not mounted directly to* the reflective surface of the metal substrate as the term is defined, because of the presence of an *intervening insulating* materials applied to the metallic base substrate.

Ex. 1002 at 282.

62. **Third**, the prior patent owner, in a district court case, took a seemingly broader view than even this, asserting the following construction:

3. “mounted directly to the reflective surface” / “mounting . . . directly to the reflective surface”

Claim term (Patent No.)	Bridgelux, Inc.’s Proposed Claim Construction
“mounted directly to the reflective surface” / “mounting . . . directly to the reflective surface” (’929 and ’051 Patents/Claims 1, 3, and 5 of the ’929 Patent and Claims 1 and 5 of the ’051 Patent)	“mounted/mounting directly to the reflective surface by adhesive or other means with no intervening elements present”

Ex. 1024 at 9-11; Ex. 1025 at 6-9.

63. Although the prior patent owner does not mention the ’988 Patent in this table, I understand that to be a typographical omission, given that these patents are all related patents to the ’988 Patent and include the same term (as explained by the prior patent owner in its brief, Ex. 1024 at footnote 2 on page 3, and as the defendant explained in its responsive brief, Ex. 1026 at 6-10).

64. The parties in that litigation agreed that an adhesive could be used because it does not count as an “intervening element,” but disputed whether any adhesive could be used and if “other means” could be used (as the prior patent owner argued). Ex. 1024 at 9-11; Ex. 1025 at 6-9; Ex. 1026 at 6-10.

65. I understand that the district court did not reach a claim construction decision, because the case was dismissed or settled.

66. Regarding the latter possible interpretation (no adhesive or other material), as I explained in Section VII, the ’988 Patent describes the term “directly” in the context of being “on” versus “directly on”:

It will be understood that when an element such as a region, layer, section, substrate, or the like, is referred to as being “on” another element, it can be directly on the other element or intervening elements may also be present. **In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present.** It will be further understood that when an element is referred to as being “formed” on another element, it can be grown, deposited, etched, attached, connected, coupled, or otherwise prepared or fabricated on the other element or an intervening element.

Ex. 1001 at 3:26-36 (emphasis added).

67. While the '988 Patent is discussing “directly on” here (rather than “directly to” in the claims), as I explained in Section VII, during prosecution, the applicant relied, in part, on this portion of the specification (which is application paragraph [0019]) when distinguishing over the prior art Yamada “machine” translation:

To set the stage for the discussion, it is noted that the term “directly” is defined as excluding any intervening elements (between the plurality of LED chips and the surface of metal substrate), *cf.*, above-identified application paragraph [0019]. Because in general metals have high thermal conductivity, such direct mounting results in creation of an efficient thermal path allowing heat to pass from the plurality of LED chips to the metal substrate, *cf.* claim 1, application paragraph [0026]. As such, the claim language is not an intended use, but limitation, as explained below.

Ex. 1002 at 280.

68. Again, as I explain below in Section IX, the prior art discloses direct mounting, regardless of which interpretation is used.

Term No. 2: “efficient thermal path”; Term No. 3: “an electrical path formed by connecting the LED chips in a chip to chip fashion”

69. Regarding two other terms in the claims of the '988 Patent, I note that Patent Owner (BX LED), in a district court case, asserted that the plain and ordinary meaning applied to two terms that the parties disputed (and offered an alternative construction for one term):

Term	BX LED Construction	Walmart Construction
“efficient thermal path” (Claim 1)	Plain and ordinary meaning – no need for construction.	Indefinite
Proposed by Walmart	Alternatively, “the path for heat dissipation created by mounting an LED directly to a substrate with high thermal conductivity without intervening insulating materials”	

Term	BX LED Construction	Walmart Construction
“an electrical path formed by connecting the LED chips in a chip to chip fashion” (Claim 1)	Plain and ordinary meaning	“electrically connecting one LED chip directly to another LED chip”
Proposed by Walmart		

Ex. 1008 at 18-22; Ex. 1009 at 12-15.

70. The district court construed the terms as follows:

Patent	Term	BX LED Construction	Walmart Construction	Court's Final Construction
U.S. PATENT NO. 8,567,988	"efficient thermal path" (Claim 1) Proposed by Walmart	Plain and ordinary meaning Alternatively, "the path for heat dissipation created by mounting an LED directly to a substrate with high thermal conductivity without intervening insulating materials"	Indefinite	Plain and Ordinary Meaning. Not indefinite.
U.S. PATENT NO. 8,567,988	"an electrical path formed by connecting the LED chips in a chip to chip fashion" (Claim 1) Proposed by Walmart	Plain and ordinary meaning	"electrically connecting one LED chip directly to another LED chip"	Plain and Ordinary Meaning, which does not include a connection of the chip through metal wires to the metal substrate.

Ex. 1028 at 4-5.

71. As I explain below in Section IX, the prior art discloses both terms under the court's constructions and under Patent Owner's alternative construction for "efficient thermal path" (which effectively just means that no intervening insulating materials are used, consistent with the disclosures in the prior art that I discuss herein).

IX. ANALYSIS OF THE PATENTABILITY OF THE '988 PATENT CLAIMS

A. Overview of the State of the Art

1. Technical Overview: LED Fundamentals

72. Light emitting diodes ("LEDs") are typically made of semiconductor or organic materials (organic LEDs, or oLEDs). Herein, I focus on semiconductor

LEDs, for example, GaN-based LEDs. Ex. 1013 at 95-99. As I discuss throughout my declaration, prior-art literature often times used similar terms to refer to LEDs (such as LEDs, LED chips, or LED dies), as does the '988 Patent itself (*e.g.*, Ex. 1001 at 4:17-18, referring to “LED chip (or die) 100”; 5:33-37, referring to “LED chips (*i.e.*, LED 100)”; and 6:39-42, referring to “an array of LEDs with pre-determined spacing”).

73. At the time of the '988 Patent's priority date, September 29, 2008, semiconductor LED lighting was used (and still is used) for applications that include, for example, automotive lights, traffic lights, indoor and outdoor lighting, and decorative use. Ex. 1013 at xi (Preface); Ex. 1005 at Abstract; Ex. 1006 at [0006]; Ex. 1007 at [0002]-[0003].

74. Semiconductor LEDs are made of materials that are grown on a solid substrate in layers (often referred to as epitaxial layers). Ex. 1013 at 95-97; Ex. 1005 at [0020], [0029], [0032]; Ex. 1006 at [0009].

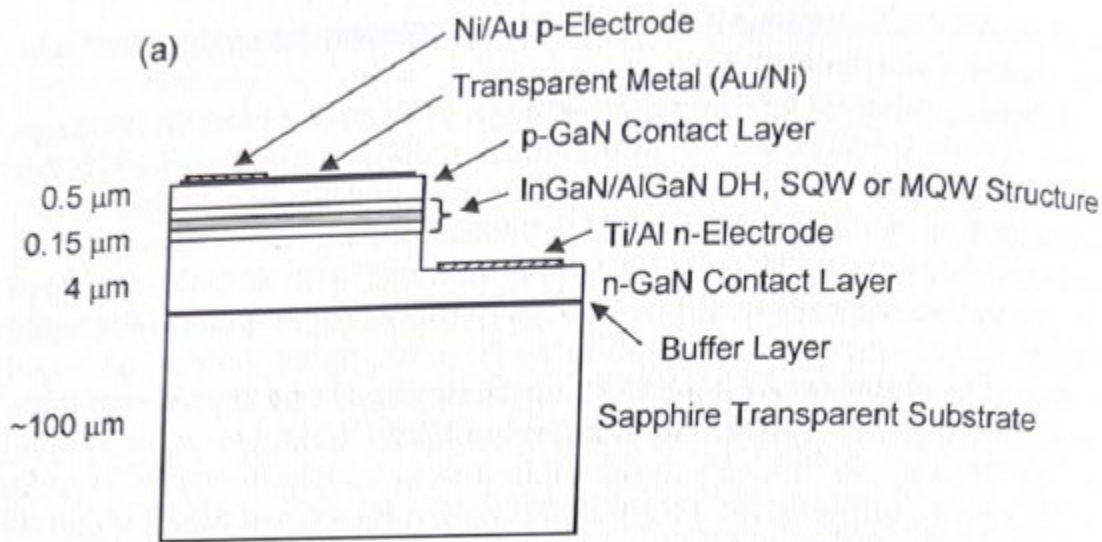
75. The following aspects of LEDs and LED packages are noteworthy and were known to a POSA prior to the '988 Patent:

- LEDs use two electrical contacts to emit light, often two top contacts that are wire bonded for powering the LED within a package. Ex. 1013 at 96 (Fig. 5.2.3(a)); Ex. 1011 at 10:61-11:24, 12:61-13:30, FIGs. 17a, 18a, 24a, 25a; Ex. 1005 at [0032]; Ex. 1001 at 1:9-32 (“Background”).
- GaN-based LEDs grown on sapphire substrates cannot be electrically contacted through the electrically insulating (non-conductive) sapphire

substrate, and thus, both the n-type and p-type contacts are typically electrically connected from the top of the GaN-based LED grown on sapphire. Ex. 1013 at 96 (Fig. 5.2.3(a)); Ex. 1011 at 11:4-11:24, FIG. 18a; Ex. 1005 at [0032].

- Extraction of light out of the LED package generally should be maximized - a known goal in LED packages. Ex. 1005 at [0019]; Ex. 1006 at [0033], [0068]; Ex. 1007 at [0019]-[0020]; Ex. 1011 at 12:51-54, 12:61-13:40; Ex. 1014 at [0012].
- Efficient collection of the LED emitted light from the LED package, which typically includes reflective and non-absorbing surfaces, should be maximized - a known goal in LED packages. Ex. 1005 at [0019]; Ex. 1006 at [0066]; Ex. 1007 at [0019]-[0020]; Ex. 1011 at 12:61-13:4; Ex. 1014 at [0012]; Ex. 1015 at [0014], [0118]-[0119].
- Efficient removal of heat from an LED can increase optical power output, package reliability and the lifetime of the LED - a known goal in LED packages. Ex. 1006 at Abstract, [0003], [0034], [0085]; Ex. 1014 at [0027]; Ex. 1005 at [0027]; Ex. 1007 at [0014], [0017]; Ex. 1015 at [0090]; Ex. 1021 at [0005], [0015].

76. Figure 5.2.3(a) of Zukauskas' Introduction to Solid State Lighting, shown below, shows a typical chip design for a GaN-based LED, with (i) top p and n contacts that can be wire bonded for powering the LED and (ii) an opposite bottom surface of the sapphire transparent substrate that is mounted into the LED package (such as onto a metal substrate external to the LED):



Ex. 1013 at 95-96 (FIG. 5.2.3.(a)).

2. Exemplary Prior Art

77. I have provided a brief overview in this Section of three prior art references: Cao753, Cao630, and Baek. I discuss these (and other) references in more detail in Sections IX.B-E.

a. Cao753

78. Cao753, in its Abstract, describes its focus: “A mining light having a semiconductor light source is disclosed. The light may include a semiconductor light source such as an LED or laser, a heat sink, a magnetic switch, a light reflective and focusing cone, and other features.” Ex. 1005 at Abstract.

79. Cao753 includes seven figures, of which Figure 5 is particularly noteworthy. In Figure 5, Cao753 depicts “an LED module 400 [sic: 500] that includes a well 506 within a primary heat sink 505 and having a plurality or array

of LED chips 507a, 507b, 507c within the well.” Ex. 1005 at [0020]. Regarding the LED chips, Cao753 explains that: (i) “Each individual LED chip may include semiconductor material or epitaxial layers on a substrate”; (ii) “Each chip may be mounted to the heat sink by use of heat conductive or light reflective adhesive or other mounting means”; and (iii) “The chips in this figure are wired in series, although wiring in parallel is also possible when the application requires it.” Ex. 1005 at [0020].

80. Cao753 discloses that the heat sinks (such as the primary heat sink) can be “a single material or a combination of two different kinds of materials,” and provides examples of heat sink materials including various reflective metals such as copper, aluminum, and silver, among other materials “with adequate heat conductance and/or dissipation properties”:

The heat sinks ... **may be any material capable of conducting heat away from the semiconductor light sources. The heat sink(s) may be of a single material** or a combination of two different kinds of materials, the first with a low thermal expansion rate and the second with high thermal conductivity. **Monolithic heat sinks may be used as well. Examples of some heat sink materials which may be used in lights depicted herein** include ceramic, powdered metal, **copper, aluminum, silver**, magnesium, steel, silicon carbide, boron nitride, tungsten, molybdenum, cobalt, chrome, Si, SiO₂, SiC, AlSi, AlSiC, natural diamond, monocrystalline diamond, polycrystalline diamond, polycrystalline diamond compacts, diamond deposited through chemical vapor deposition and diamond deposited through physical vapor deposition, and composite materials or

compounds. Any materials with adequate heat conductance and/or dissipation properties can be used.

Ex. 1005 at [0027] (emphases added).

81. Figure 5 of Cao753, shown below, depicts LED module 500 comprising **primary heat sink 505** that (i) may be a highly reflective metal such as silver or aluminum and (ii) includes a well 506 with a **surface** on which an array of **LED chips 507a-d** is mounted directly and “wired in series”. Ex. 1005 at [0020], [0023], [0027]-[0028], [0034]. I have added coloring to Figure 5 (below, left), and included the original version of Figure 5 (below, right). I note that the **surface** that I have colored **red** in this Figure 5 on the left is not an added layer, but rather indicates the bare surface of the primary heat sink 505 (which, per Cao753, may be a reflective metal such as aluminum, silver, or copper). Whether or not separately noted in my declaration, this is true of my coloring for Figure 5 of Cao753.

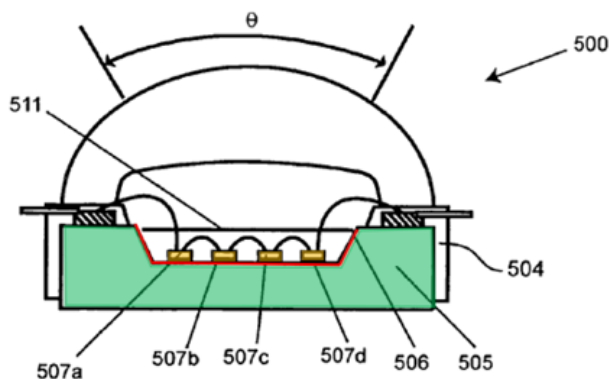


Fig. 5

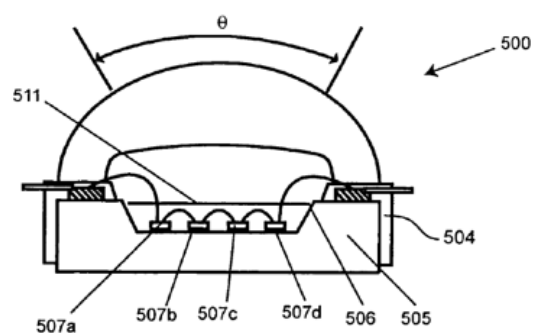


Fig. 5

Ex. 1005, FIG. 5 (coloring added to version of Figure 5 on left).

82. As I noted above, Cao753 discloses, in Figure 5, that LED chips 507a-d can be mounted to the primary heat sink 505 in various ways, including “by use of heat conductive or light reflective adhesive or other mounting means.” Ex. 1005 at [0020], [0024] (heat conductive adhesive), [0028] (example adhesives and other mounting means). Cao753 discloses, for example, that the LEDs can be “mounted directly on a heat sink”, as well as mechanical fixation, brazing, welding, or other methods. Ex. 1005 at [0023], [0028], [0034].

83. Cao753 discloses that, in multi-chip embodiments (such as Figure 5), “The spacing between chips can be adjusted from zero to more than 1 mm, depending on the application requirements.” Ex. 1005 at [0023].

84. Cao753 further discloses that the primary heat sink “can be attached to a **secondary heat sink** if desired, such as; [sic: such as,] by use of a heat conductive and/or electrically insulative adhesive, welding, brazing, soldering or mechanical fixation.” Ex. 1005 at [0024] (color added).

85. Cao753 also discloses that, in certain cases when a well is included as part of the LED package in which the LED is mounted, “all of the light emitted from the chip can be reflected back in the light exit direction for highest light output” and that “The well may also include a reflective coating or polished

surface.” Ex. 1005 at [0019] (discussing Figure 4 which is highly similar to Figure 5 except for the number of chips and that Figure 4 is a flip-chip design).

b. Cao630

86. Cao630 states in its Abstract: “An illuminating light for illuminating a physical space for use by humans has been invented. In one example the illuminating light includes at least one semiconductor chip that can emit light mounted to a primary heat sink. The primary heat sink is mounted to a secondary heat sink and a heat sink grid is provided to dissipate heat to the atmosphere. Other examples are also disclosed.” Ex. 1007 at Abstract.

87. The sole inventor (Densen Cao) of Cao630 is also the first named inventor of Cao753. The Cao630 and Cao753 patent application publications (Exhibits 1007 and 1005, respectively) are not formally related, but are both directed to LED light sources to illuminate spaces and have highly similar specifications and figures (*e.g.*, Figs. 3a and 3b in Cao630 are similar to Figs. 4 and 5 in Cao753, as I discuss further in Section IX.D.1).

88. Cao630 includes five figures, of which Figures 3a and 3b are particularly noteworthy.

89. Figure 3a of Cao630, shown below, discloses a high-power LED package 350 with a single wire-bonded **LED chip or chip array 306** mounted to **primary heat sink 303** including a well having a **reflective surface** where “The

walls and bottom of the well may be polished to be light reflective, or may be covered, plated, painted or bonded with a light-reflective coating such as Al, Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastic and others to reflect light and thereby improve light source efficiency.” Ex. 1007 at [0020]. I have included below side-by-side versions of Figure 3a, the original version on the right and my colored version on the left.

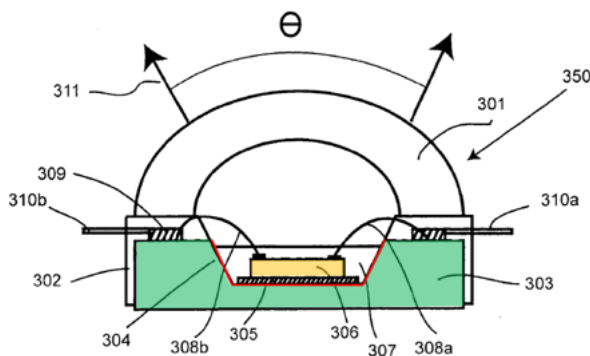


Fig. 3a

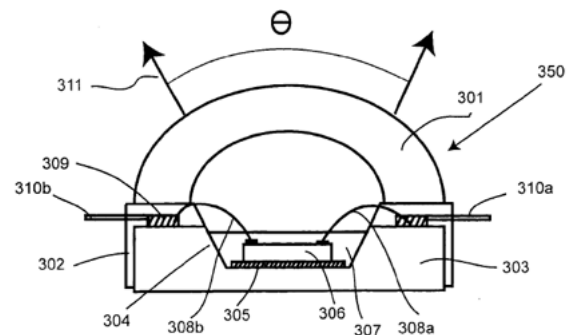


Fig. 3a

Ex. 1007, FIG. 3a (coloring added to version of Figure 3a on left).

90. Cao630 shares other common disclosures with Cao753. For example, first, just like in Cao753, Cao630 discloses LED packages designed for efficient heat dissipation and light reflectivity for visible light. Ex. 1007 at [0003], [0020]. Second, just like in Cao753, Cao630 discloses that mounting of the LED chips may be achieved by a variety of methods, including direct mount, mechanical fixation, brazing, welding, use of an adhesive or other methods, and notes that use of a heat

conductive adhesive may be desired. Ex. 1007 at [0015], [0020]. Third, also just like in Cao753, Cao630 discloses that the heat sink can be “a single material or a combination of two different kinds of materials,” and provides examples of heat sink materials including various reflective metals such as copper, aluminum, and silver, among other materials “with adequate heat conductance and/or dissipation properties”. Ex. 1007 at [0014]. And fourth, Cao630 discloses a multi-chip wire-bonded LED package with chips within a substrate well (in Figure 3b), which uses the same materials and has the same structure as Figure 5 of Cao753, except for the addition of sub-wells within the larger well. Ex. 1007 at [0021], FIG. 3b.

b. Baek

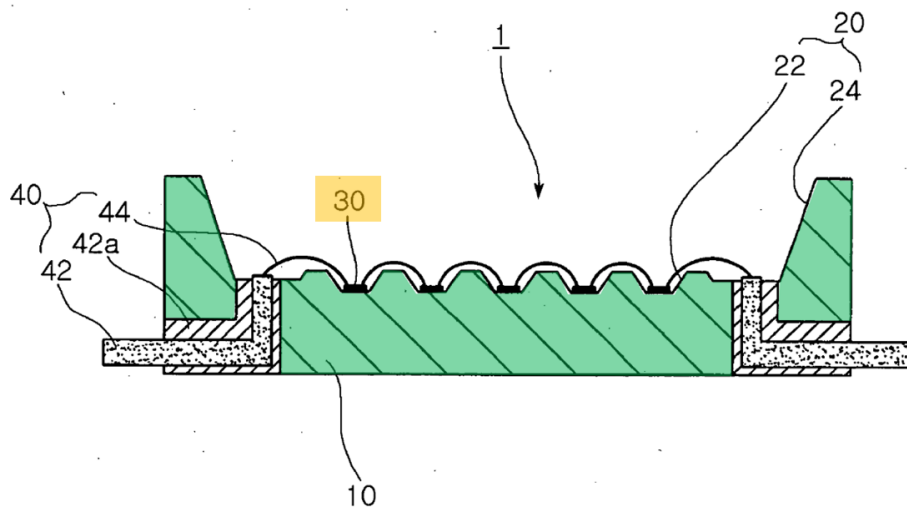
91. Baek states in its Abstract:

The invention relates to a high power LED package having excellent light efficiency and heat dissipating characteristics. The LED package includes a base member, a reflector unit arranged on the base member and having a plurality of first reflectors, a plurality of LED chips mounted on the base member and surrounded by the first reflectors, and a connection unit arranged on the base member, for electrically connecting the LED chips to an outside. The reflector unit also includes a second reflector surrounding the first reflectors. The second reflector is arranged to surround the first reflectors in order to completely prevent any interference of emission lights and collect the emission lights together, thereby enabling excellent light efficiency. Furthermore, with the first reflectors surrounding the individual LED chips, it is possible to maximize heat dissipating efficiency of the lead frame, thereby stabilizing operating characteristics of the package.

Ex. 1006 at Abstract.

92. Baek includes nine figures, of which Figures 5-8 are particularly relevant. As I explain further in Section IX.E, Figures 5-7 are different views of the same embodiment, and Figure 8 is the same as Figures 5-7, except for an additional reflective layer(s) added. Ex. 1006 at [0059], [0078]. I focus on Figures 6 and 8 in my overview in this section.

93. In Figure 6, shown below, Baek discloses **base member 10** with a **reflector unit 20** (made up of reflectors 22 and 24). **LED chips 30** are mounted on the base member 10, and wire bonded in a chip to chip manner. Ex. 1006 at [0060], [0072]-[0074], [0077].



Ex. 1006, FIG. 6 (coloring added to figure).

94. Baek discloses that, in this embodiment (*i.e.*, Figures 5-7), base member 10 can be “made of a material capable of dissipating (radiating) heat such

as Cu [copper] of excellent heat conductivity” and “can be fabricated with the first and second reflectors 22 and 24 through a single punching”, resulting in a single structure as depicted in Figure 6 above. Ex. 1006 at [0072]-[0073]. Baek also discloses that the base member has “excellent heat dissipating efficiency,” and should dissipate or radiate heat outward. Ex. 1006 at [0083], [0036], [0065].

95. Regarding Figure 8, Baek discloses adding a “reflect-activating layer” on reflectors 22 and 24, that can be applied by plating silver on the surface to “further enhance light efficiency.” Ex. 1006 at [0078]-[0082]. In Figure 8, shown below, Baek depicts reflect-activating layer 50 plated on **reflectors 22** and reflect-activating layer 60 plated on **reflector 24**, the surface of **base member 10**. Ex. 1006 at [0078]-[0082]. **Base member 10** may be mounted to **heat radiating plate 70**. Ex. 1006 at [0086].³ In Figure 8, the reflective surfaces are shown in **red**, which include layer 50, layer 60, and the copper base member surface (all of which are reflective in the visible spectrum when, *e.g.*, the base member is copper). I have included below side-by-side versions of Figure 8, the original version on the right and my colored version on the left.

³ I note that paragraph [0086] refers to Figure 9, but a POSA would have understood that this disclosure applies to the same numbered element in Figure 8, which is generally true of Baek’s element numbering across figures and embodiments.

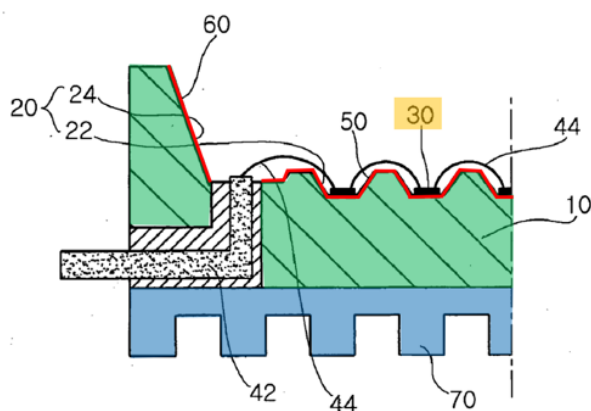


FIG. 8

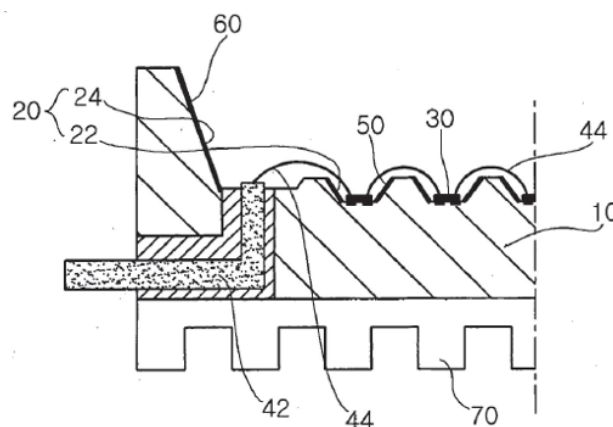


FIG. 8

Ex. 1006, FIG. 8 (coloring added to version of Figure 8 on left).

B. Ground 1: Cao753 Anticipates Claims 1 and 4-9

96. In my opinion, Cao753 discloses all of the limitations of claims 1 and 4-9, arranged as in the claims, in its Figure 5 embodiment. Thus, it is my opinion that Cao753 anticipates these claims.

1. Claim 1

1[pre] “A light emitting diode (LED) apparatus comprising:”

97. Regardless of whether the preamble of claim 1 is found to be a limitation, Cao753 discloses the claimed “*light emitting diode (LED) apparatus*”, as shown in Figure 5, below.

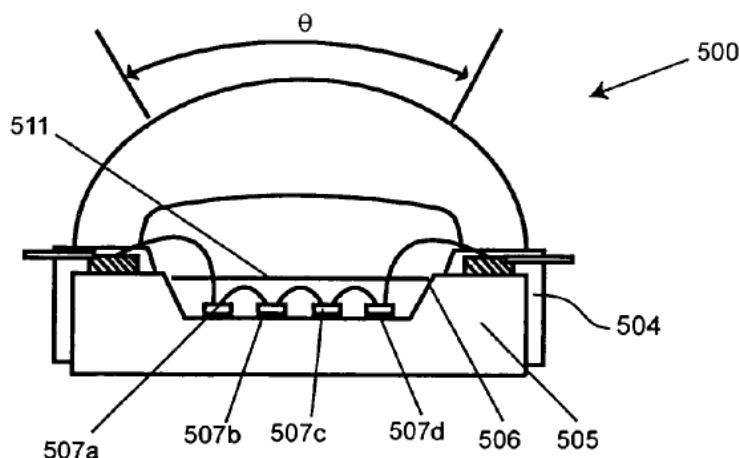


Fig. 5

Ex. 1005, FIG. 5.

98. According to Cao753, “FIG. 5 depicts an **[light emitting diode] LED module 400** [sic: 500] that includes a well 506 within a primary heat sink 505 and having a plurality or array of LED chips 507a, 507b, 507c within the well.” Ex. 1005 at [0020].

99. I note that this LED module with LED chips mounted on a primary heat sink in Cao753 (the claimed “*metal substrate*” of limitation 1[a]) being a “*light emitting diode apparatus*” of the preamble in claim 1 is consistent with the usage in the claims, as well as the '988 Patent and its description of an LED apparatus (such as “LED array apparatus 300” with a metal substrate on which LEDs are mounted in Figure 3, which I discussed in Section VII (Overview of the '988 Patent)). Ex. 1001 at 1:65-66, 2:48-50, 5:30-37. In other words, a POSA would have

understood that the LED module in Figure 5 of Cao753 corresponds to the claimed “*light emitting diode apparatus*” of the preamble in claim 1.

1[a] “a metal substrate having a reflective surface; and”

100. Cao753 discloses the claimed “*a metal substrate having a reflective surface*”, in particular, “primary heat sink 505” of Figure 5, which may be made of various metals including aluminum, silver, and copper. Ex. 1005 at [0020], [0027], claims 9 and 19 of Cao753.

101. Cao753 discloses that its “heat sinks ... may be **any material capable of conducting heat away** from the semiconductor light sources.” Ex. 1005 at [0027] (emphasis added). Cao753 also discloses examples of the heat sink material:

The heat sink(s) **may be of a single material** or a combination of two different kinds of materials, the first with a low thermal expansion rate and the second with high thermal conductivity. Monolithic heat sinks may be used as well. **Examples of some heat sink materials** which may be used in lights depicted herein include ceramic, powdered metal, **copper, aluminum, silver**, magnesium, steel, silicon carbide, boron nitride, tungsten, molybdenum, cobalt, chrome, Si, SiO₂, SiC, AlSi, AlSiC, natural diamond, monocrystalline diamond, polycrystalline diamond, polycrystalline diamond compacts, diamond deposited through chemical vapor deposition and diamond deposited through physical vapor deposition, and composite materials or compounds. **Any materials with adequate heat conductance and/or dissipation properties can be used.**

Ex. 1005 at [0027] (emphases added).

102. As explained in paragraph [0027] of Cao753 (quoted above), the heat sinks disclosed in Cao753 - which a POSA would have understood to include primary heat sink 505 that is earlier disclosed in Cao753 at paragraph [0020] and to which Cao753 is referring to in paragraph [0027] (among others) - can be various metals such as aluminum, silver and copper. In such a situation, the primary heat sink corresponds to the claimed “*metal substrate*” because it is “metal” and because it is a “substrate,” consistent with the understanding of a POSA and the ’988 Patent. I note, for example, that Graf (the Modern Dictionary of Electronics, 7th Ed.) states that a “substrate” is “Also called base material” and provides various definitions:

substrate— Also called base material. 1. The supporting material on or in which the parts of an integrated circuit are attached or made. The substrate may be passive (thin film, hybrid) or active (monolithic compatible). 2. A material on the surface of which an adhesive substance is spread for bonding or coating; any material that provides a supporting surface for other materials, especially materials used to support printed-circuit patterns. 3. The physical material upon which an electronic circuit is fabricated. Used primarily for mechanical support but may serve a useful thermal or electrical function. Also, a material on whose surface an adhesive substance is spread for bonding or coating, or any material that provides a supporting surface for other materials. 4. The base or support layer of a transistor or monolithic chip, which usually constitutes a major proportion of the total volume. When composed of ceramic, glass, or sapphire, the substrate functions mainly as a support during the operations of fabrication and encapsulation. However, when composed of heavily doped semiconductor material it normally performs the additional function of a distributed low-resistance connection to the physically lowest region of the device. 5. That part of an integrated circuit that acts as a support. 6. A slab of insulating material used for structural support of thick-film depositions and assembly components, usually high-purity (96 to 99 percent) alumina. *See* alumina. 7. The material on which the chips and other components are mounted, comparable to a printed circuit board. Substrate materials in common use include glass, sapphire, silicon, alumina, beryllia, and porcelainized steel. 8. The underlying material on which a microelectronic device is built.

Ex. 1012 at 745; Ex. 1023 at 15 (App. A at 2). Moreover, consistent with the knowledge of a POSA, I note that the '988 Patent does not explain what its “substrate” is, other than stating exemplary material that it may be made of (metal, such as aluminum), stating that heat is dissipated through it, and depicting it as a base material for, *e.g.*, the LED chips. Ex. 1001 at 1:57-64, 4:60-61, 5:46-62, FIG. 3. That is just like Cao753's primary heat sink 505.

103. Moreover, when primary heat sink 505 is made of, for example, silver, aluminum, or copper as described in Cao753 at paragraph [0027] (quoted above), it also has a reflective surface because each of these metals reflects light in the visible spectrum. Ex. 1027 at 511 (Figure 11-1); Ex. 1022 at 376 (Figure 13.8); Ex. 1016 at 3 (Figure 1); Ex. 1017 at 162 (Figure 1); Ex. 1015 at [0088],⁴ [0118]-[0119]. In fact, as explained in these references, aluminum and silver are two of the most highly reflective metals (including in the visible spectrum) and copper is reflective as well. Ex. 1027 at 511 (Figure 11-1); Ex. 1022 at 376 (Figure 13.8); Ex. 1016 at 3 (Figure 1); Ex. 1017 at 162 (Figure 1); Ex. 1015 at [0088], [0118]-[0119].

⁴ Even though the legend in Figure 5 of Sanpei (Ex. 1015) is incorrect, I note that, in Figure 5, the curve for the white resin is shown as a solid line, and the silver curve is a dashed line, as identified in paragraph [0088] of Ex. 1015.

104. I note that the '988 Patent also discloses that the reflective surface of its substrate can be aluminum (bare or polished) or silver (plated). For example, the '988 Patent states that, "For example, the metal substrate may be constructed from aluminum and the reflective surface 206 may be bare or polished aluminum" or that "Alternatively, the reflective surface 206 may be formed by silver plating on the substrate 204." Ex. 1001 at 4:63-66, 6:1-3. In other words, the '988 Patent itself confirms that a metal substrate has a reflective surface if it is made of a reflective metal (including, as the '988 Patent explains, a reflective metal with a "bare" surface).

105. Thus, Figure 5 from Cao753, below, which shows **primary heat sink 505** (the claimed "*metal substrate*"), has a **reflective surface** (such as aluminum, silver, or copper), which I have annotated in **red** for clarity. I note that the **reflective surface** that I have colored **red** in this Figure 5 is not an added layer, but rather indicates the bare surface of the primary heat sink 505 that is itself a reflective metal. I have included below side-by-side versions of Figure 5, the original version on the right and my colored version on the left.

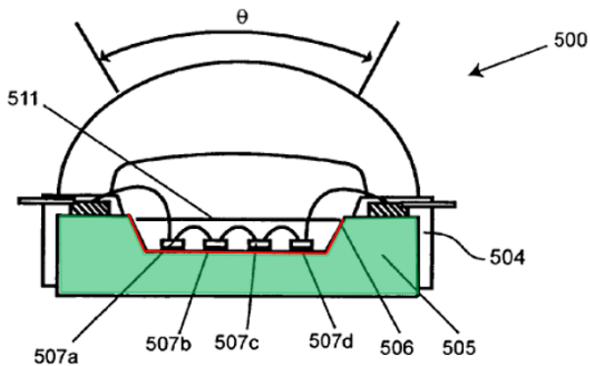


Fig. 5

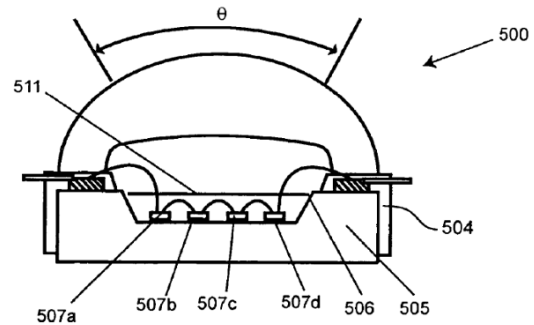


Fig. 5

Ex. 1005, FIG. 5 (coloring added to version of Figure 5 on left).

1[b] “a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path”

106. Cao753 discloses the claimed “*a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path,*” in particular, LED chips 507a-d in Figure 5 that are directly mounted (via various means, as I explain below) to primary heat sink surface 505 resulting in an efficient thermal path. Ex. 1005 at [0020], [0027]-[0028], [0034].

107. I first address Cao753’s disclosure in Figure 5 of the claimed “*a plurality of LED chips mounted directly to the reflective surface of the metal substrate*”. I then address the claimed “*creating an efficient thermal path*” portion of limitation 1[b].

108. **First**, Cao753 discloses the claimed “a plurality of LED chips mounted directly to the reflective surface of the metal substrate”.

109. Cao753 explains that “Each chip” (507a-d as shown in Figure 5, below) “may be mounted to the heat sink” (*i.e.*, primary heat sink 505) “by use of **heat conductive** or light reflective adhesive or **other mounting means.**” Ex. 1005 at [0020] (emphases added). This can be seen in Figure 5, below, where the **LED chips 507a-d** are mounted to the **top surface** (*i.e.*, the claimed “reflective surface”) of **primary heat sink 505** (*i.e.*, the claimed “metal substrate”). I have included below side-by-side versions of Figure 5, the original version on the right and my colored version on the left.

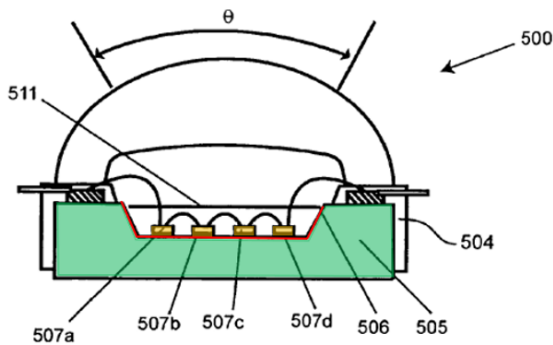


Fig. 5

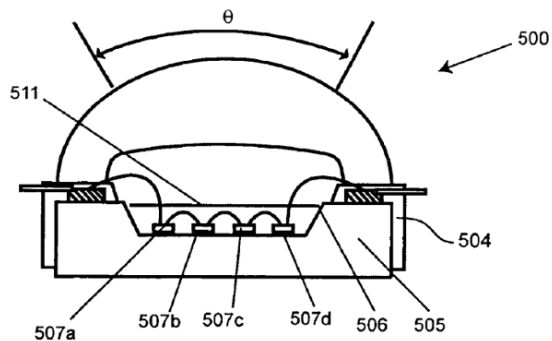


Fig. 5

Ex. 1005, FIG. 5 (coloring added to version of Figure 5 on left).

110. I explain in this section that Cao753 discloses the claimed direct mounting, regardless of (i) whether any adhesive or “suitable adhesive” without an

intervening insulating material is allowed, or (ii) no adhesive or other bonding material is allowed. I do this because there are competing possible interpretations of this limitation based on the '988 Patent, the file history, and the positions that the Patent Owner and the prior patent owner took in district court litigation, as I explained in Section VIII (Claim Construction). Regardless of what construction is adopted, Cao753 still discloses this limitation 1[b].

Cao753 Discloses Using Suitable Adhesive Without Intervening Material

111. If the claimed “*mounted directly*” allows an adhesive or a “suitable adhesive” with no other intervening materials (*e.g.*, a heat conductive adhesive that has no additional intervening insulating material), Cao753 discloses this limitation in the context of its Figure 5.

112. For example, Cao753 discloses “Each chip” (*i.e.*, LED chips 507*a-d* shown in Figure 5⁵) “may be mounted to the heat sink by use of **heat conductive or light reflective adhesive** or other mounting means.” Ex. 1005 at [0020] (emphasis added). Cao753 also discloses that the LED chips disclosed in Cao753 (including LED chips 507*a-d*) may be mounted using “**heat conductive** and/or electrically insulative adhesives” such as “silver based epoxy, other epoxies, and

⁵ I note that chip 507*d* is labeled in Figure 5, but not referenced in paragraph [0020] of Cao753.

other adhesives with a **heat conductive quality** and/or electrically insulative quality”. Ex. 1005 at [0028] (emphasis added).

113. Paragraph [0028] of Cao753 states, in full:

Mounting of *any* semiconductor chip or light module or semiconductor light source may be achieved by a variety of methods, including mechanical fixation (clips, press-fit, screws, rivets, etc.), brazing, welding, **use of an adhesive** or other methods. **Use of a heat conductive and/or electrically insulative adhesive may be desired.** Examples of heat conductive and/or electrically insulative adhesives which may be used are silver based epoxy, other epoxies, and other adhesives with a heat conductive quality and/or electrically insulative quality. In order to perform a heat conductive function, it is important that the adhesive possess the following characteristics: (i) strong bonding between the materials being bonded, (ii) adequate heat conductance, (iii) electrically insulative or electrically conductive if desired (or both), and (iv) light reflectivity if desired, or any combination of the above. Examples of light reflective adhesives which may be used include silver and aluminum based epoxy. One example heat conductive and electrically insulative adhesive includes a mixture of a primer and an activator. In this example, the primer may contain one or more heat conductive agents such as aluminum oxide (about 20-60%) and/or aluminum hydroxide (about 15-50%). The primer may also contain one or more bonding agents such as polyurethane methacrylate (about 8-15%), and/or hydroxyalkyl methacrylate (about 8-15%). An activator may be mixed with the primer to form an adhesive. The activator may include any desired catalyst, for example n-heptane (about 5-50%), aldehyde-aniline condensate (about 30-35%), isopropyl alcohol (about 15-20%), and an organocopper compound (about 0.01 to 0.1%). **Adhesives such as described herein can be used to mount a chip to a primary heat sink, or to mount a primary heat sink to a secondary heat sink, or both.**

Ex. 1005 at [0028] (emphases added).

114. This disclosure of Cao753 is consistent with the '988 Patent that mounting LED chips should use “any suitable adhesive” without insulating material. Ex. 1001 at 4:37-53. Notably, the '988 Patent does not specify the type of “suitable adhesive” to use, consistent with the common knowledge of a POSA to select the appropriate adhesive.

115. Based on the above, a POSA would have understood that using a heat conductive adhesive (as in Cao753) to mount LED chips 507*a-d* to the reflective surface of primary heat sink 505 corresponds to the chips being “*mounted directly to the reflective surface*”, where the claim term allows for “any suitable adhesive” without any additional intervening insulating material. That is, a POSA would have understood that LED chips 507*a-d* are directly mounted to the reflective surface under this claim interpretation.

Cao753 Also Discloses Using No Adhesive or Bonding Material

116. If the claimed “*mounted directly*” does not allow an adhesive or other material, Cao753 also discloses this limitation in the context of its Figure 5.

117. For example, Cao753 discloses “Each chip [507*a-d* shown in Figure 5, above] may be mounted to the heat sink by use of heat conductive or light reflective adhesive or **other mounting means.**” Ex. 1005 at [0020] (emphasis added).

118. Cao753 discloses a variety of other means that do not require additional material in paragraph [0028]:

Mounting of *any* semiconductor chip or light module or semiconductor light source **may be achieved by a variety of methods, including mechanical fixation (clips, press-fit, screws, rivets, etc.), brazing, welding,** use of an adhesive or **other methods.**

Ex. 1005 at [0028] (emphases added).

119. Cao753 also expressly discloses direct mounting:

- the LED chips can be “**Direct mount[ed]**, surface mount[ed], flip chip and any other desired chip mounting configuration may be employed”, Ex. 1005 at [0034] (emphasis added); and
- the “chips may be mounted in a well of a heat sink or may be **mounted directly on a heat sink**”, Ex. 1005 at [0023] (emphasis added).

120. Based on the above - by describing these methods of mounting including non-adhesive direct mounting - a POSA would have understood that Cao753 discloses direct mounting without any adhesive or intervening material.

121. I also note, as I did in Sections VII and VIII, that the only method disclosed in the '988 Patent to mount the LED to the substrate (directly or otherwise, regardless of the meaning of direct mounting) is using an undefined “suitable adhesive”. No other methods are disclosed. This is consistent with Cao753 and the other prior art I discuss in my declaration that it was well known and common knowledge to a POSA how to mount an LED to a substrate, directly or otherwise.

For example: (i) Baek discloses that “LEDs are produced in the form of Surface Mount Devices to be directly mounted on the PCB”, Ex. 1006 at [0014]; (ii) Cao630 includes similar disclosure to Cao753 regarding the mounting methods, Ex. 1007 at [0015]; (iii) Ishii discloses a wire-bonded LED that is “directly mounted on the basic surface of the base” using an “adhesive member ... having heat conductivity” which results in the LED chip and base being “thermally coupled”, Ex. 1020 at [0036]-[0037]; and (iv) Hashimoto discloses that the “LED chip 1 is mounted directly on the bottom recess [of the metal plate]”, Ex. 1021 at [0049], in comparison to prior lighting emitting devices where the “LED chip 1 [was] ... not mounted directly on the metal plate” and instead was “mounted over the metal plate with [an] insulating layer”, Ex. 1021 at [0007].

122. **Second**, Cao753 discloses the claimed “*creating an efficient thermal path*”.

123. For example, the direct mounting discussed above (with or without a heat conductive adhesive and without any additional intervening insulating material) creates an efficient thermal path from the LED chips 507*a-d* through the primary heat sink 505. Ex. 1005 at [0020], [0028], claim 1 of Cao753.

124. Cao753 discloses that its direct-mount LED package design results in a “heat conductance path originating at said semiconductor chip [*e.g.*, LED chip 507] where heat is produced by said chip when it is powered and emitting light, said

heat conductance path thence to said primary heat sink, thence to said secondary heat sink”. Ex. 1005 at claim 1 of Cao753. Claims 12 and 16 also disclose the same concept. Ex. 1005 at claims 12, 16 of Cao753.

125. Cao753 also discloses a “heat conductance path,” and how “Avoidance of heat buildup is important to avoid overheating the semiconductor light source and decreasing its light intensity output or decreasing its life.” Ex. 1005 at [0017].

126. I also note that, consistent with the ’988 Patent, the file history, and the arguments in district court (discussed in my Section VIII above), mounting using a heat conductive adhesive without an additional intervening insulating material itself results in the claimed “efficient thermal path”. That is, the ’988 Patent similarly teaches that its direct mounting of the LED chip to a metal substrate (*e.g.*, aluminum) without “an insulating dielectric” results in a similar “efficient thermal path 116”. Ex. 1001 at 4:37-59. Moreover, the applicant asserted, during prosecution, that “Because in general metals have high thermal conductivity, such direct mounting results in creation of an efficient thermal path”. Ex. 1002 at 280. And during the district court proceedings, Patent Owner and its expert argued that “removing ‘insulating dielectric[s]’ creates an efficient thermal path.” Ex. 1010 ¶71 (citing Ex. 1001, 4:54-59); Ex. 1008 at 18-20; Ex. 1009 at 12-13. I also note that the district court, as I discussed in Section VIII, agreed with the Patent Owner that “efficient thermal path” has its plain and ordinary meaning. Ex. 1028 at 4-5.

127. In Figure 5, below, the **thermal path** is shown with the downward vertical arrows, and **LED chips 507a-d** are directly mounted to **primary heat sink 505** made of an efficient heat-dissipating metal (such as copper, silver or aluminum disclosed in Cao753 for the heat sink 505), resulting in an efficient thermal path by allowing heat to pass through the bottom of the LED into and through the efficient heat-dissipating heat sink(s) in the shortest distance. Ex. 1005 at [0020], [0027]; Ex. 1019 at 4-157 (aluminum, silver, and copper are highly thermally conductive metals); Ex. 1018 at 10 (explaining high thermal conductivity of aluminum and copper).

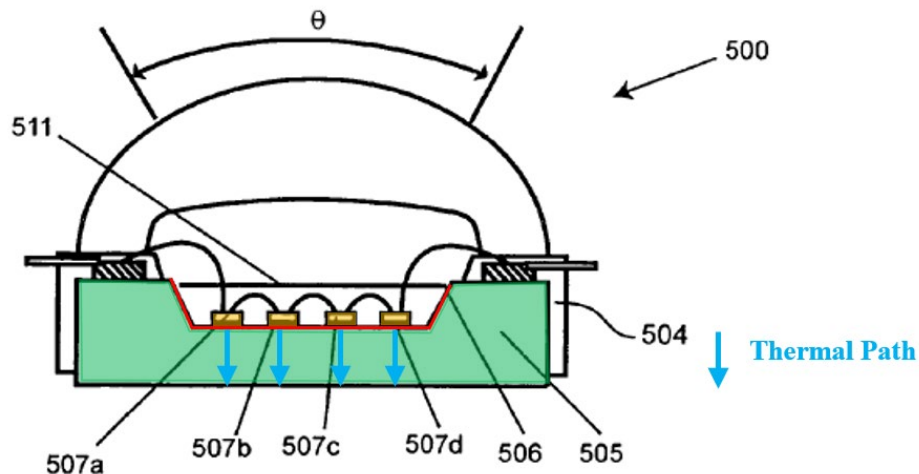


Fig. 5

Ex. 1005, FIG. 5 (coloring and blue arrows indicating thermal path added to figure; words "Thermal Path" also added to figure).

1[c] “at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and”

128. Cao753 discloses the claimed “*at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips,*” as evident, for example, in Cao753 Figure 5. Ex. 1005 at [0020], [0023].

129. I note that Figure 5 depicts LED chips 507*a-d* being spaced apart from one another, which results in exposed regions of the reflective surface between the LED chips, as shown below. I again note that the reflective surface that I have colored **red** in this Figure 5 is not an added layer, but rather indicates the bare surface of the primary heat sink 505. I have included below side-by-side versions of Figure 5, the original version on the right and my colored version on the left.

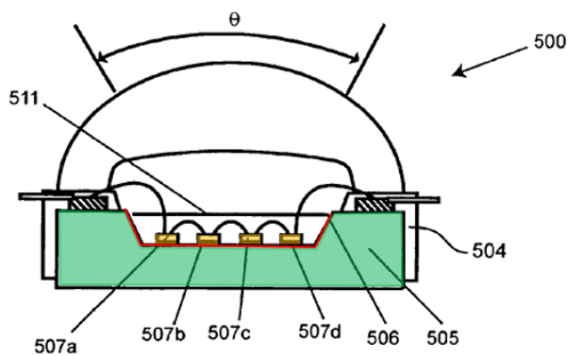


Fig. 5

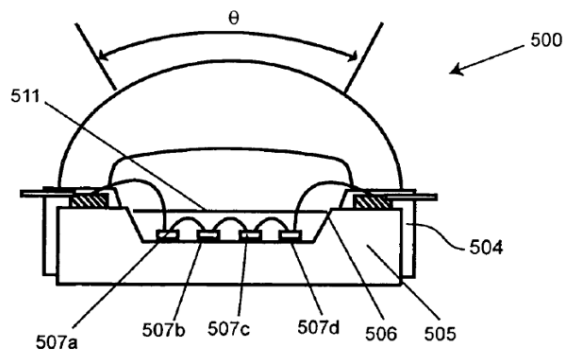


Fig. 5

Ex. 1005, FIG. 5 (coloring added to version of Figure 5 on left)

130. In addition to being evident from Figure 5, Cao753 also discloses to vary the spacing between chips in multi-chip packages (in Figure 5 and others): “The spacing between chips can be adjusted from zero **to more than 1 mm**, depending on the application requirements.” Ex. 1005 at [0023] (emphasis added). Paragraph [0023] of Cao753 is referring back to the disclosed embodiments including Figure 5, such as discussed in paragraph [0020] of Cao753.

131. Cao753 also explains that “The semiconductor light sources can include semiconductor chips that emit light when provided with electrical power” and “may include any of a variety of materials known for constructing chips that emit light.” Ex. 1005 at [0029], [0032]. That is, Cao753 discloses to apply any of a variety of known chip types for emitting light, including, for example, a blue LED chip with a wavelength shifting coating such as yellow phosphor that produces

multiple wavelengths that are perceived as white light visible by the human eye. Ex. 1005 at [0019]. Given the explanation at paragraph [0029] in Cao753 (Ex. 1005) and that paragraph [0020] in Cao753 (discussing Figure 5) likewise teaches to use a wavelength shifting coating to make visible white light, a POSA would have understood that the explanation at paragraph [0019] in Cao753 applies to all embodiments including Figure 5 of Cao753.

132. Accordingly, a POSA would have understood that the spacing (shown in Figure 5 above between LED chips 507a-d) results in exposing regions of the reflective surface between portions of the LED chips whereby the exposed regions reflect light emitted from the portions of the LED chips. This is like the '988 Patent, in which spacing between chips necessarily results in exposed regions that reflect light emitted from the portions of the LED chips. Ex. 1001 at 5:30-37, FIG. 3. There is no explanation in the '988 Patent about how that otherwise occurs, or, in fact, any particular significance of the effects of the particular spacing dimensions.

1[d] “an electrical path formed by connecting the LED chips in a chip to chip fashion.”

133. Cao753 discloses the claimed “*an electrical path formed by connecting the LED chips in a chip to chip fashion*”, as can be seen in Figure 5 with wire-bonded LED chips 507a-d that are connected in a chip to chip fashion. Ex. 1005 at [0020].

134. Cao753 discloses that, in Figure 5, “The chips ... are wired in series”. Ex. 1005 at [0020]. This results in a chip to chip connection, with an electrical path between the chips when powered. Ex. 1005 at [0020]. In Figure 5 of Cao753, below, the wire-bonded **LED chips 507a-d** result in an **electrical path** from chip to chip as the LED module 500 is powered.

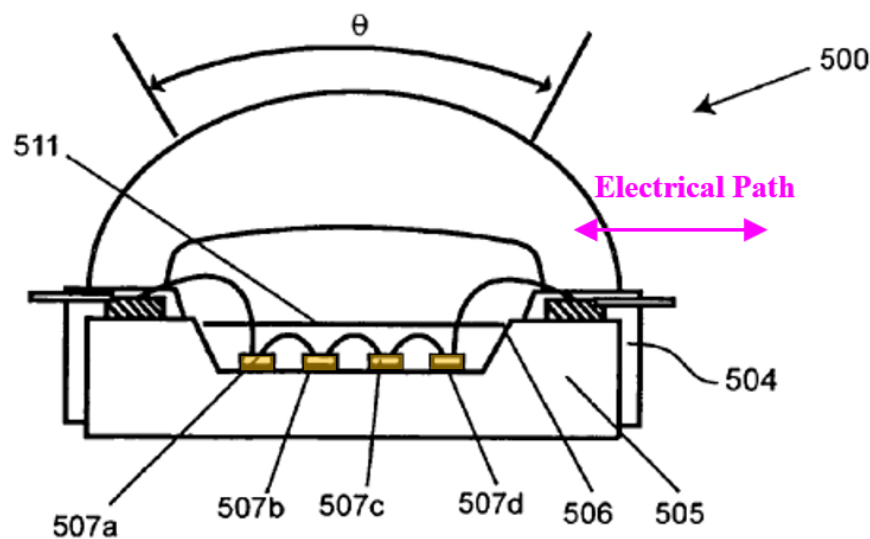


Fig. 5

Ex. 1005, FIG. 5 (coloring and magenta arrow indicating electrical path added to figure; words “Electrical Path” also added to figure).

135. A POSA would have understood the above chip to chip connection in Figure 5 is the same as described by the '988 Patent without a connection of the chips through the wires to the substrate (Figure 3 in the '988 Patent has chips wire

bonded from chip to chip, which results in the horizontal electrical path shown at arrow 312). Ex. 1001 at 5:38-45, 6:18-21, FIG. 3.

2. Claim 4

“The apparatus of claim 1, wherein the reflective surface has a reflectivity of 70% or greater.”

136. Cao753 discloses the claimed “*the reflective surface has a reflectivity of 70% or greater,*” for example, through its disclosure to use aluminum and silver as the primary heat sink 505 having a reflective surface made of the same corresponding metal in Figure 5. Ex. 1005 at [0020], [0027]. Cao753 also discloses claim 1, from which claim 4 depends, as I explained above.

137. As I explained in Section VII, a POSA would have understood that aluminum and silver both have a reflectivity of greater than 70% including in the visible spectrum (*i.e.*, the spectrum relevant to the '988 Patent, which again is concerned with making an LED apparatus that emits visible light for use in a lamp or light such as “an automobile headlamp, street light, overhead light, or in any other general illumination application”, Ex. 1001 at 6:34-58, FIG. 5).

138. These metal reflectivity properties in the visible spectrum are explained in basic textbooks, literature and patents from before or around the time of the '988 Patent's filing date, such as Ohring (Ex. 1027 at 511 (Figure 11-1)),

Fischer (Ex. 1022 at 376 (Figure 13.8)), Thomas (Ex. 1016 at 3 (Figure 1)), Bartek (Ex. 1017 at 162 (Figure 1)), and Sanpei (Ex. 1015 at [0088],⁶ [0118]-[0119]).

139. Ohring explains, for example, that “Silver and aluminum reflect all portions of the visible spectrum and therefore appear to have white color.” Ex. 1027 at 511. Ohring also depicts the reflectance percentages of these metals:

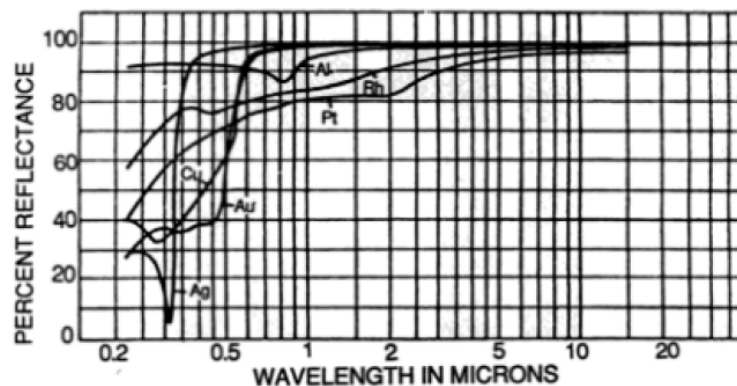
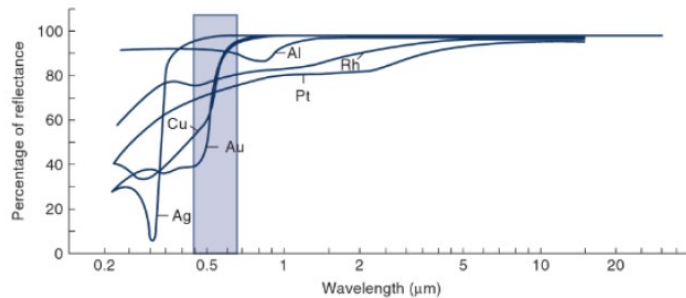


Figure 11-1. Reflectance of Al, Ag, Au, Cu, Rh, and Pt mirror coatings from the UV to the IR. (From Ref. 8).

Ex. 1027 at 511 (Figure 11-1).

140. As do other references, including Fischer:

⁶ As I discussed above, even though the legend in Figure 5 of Sanpei (Ex. 1015) is incorrect, I note that, in Figure 5, the curve for the white resin is shown as a solid line, and the silver curve is a dashed line, as identified in paragraph [0088] of Ex. 1015.



■ FIGURE 13.8 Reflection coefficient of some metals. (Visible range is shaded.)

Ex. 1022 at 376 (Figure 13.8) (color in original).

141. And Thomas:

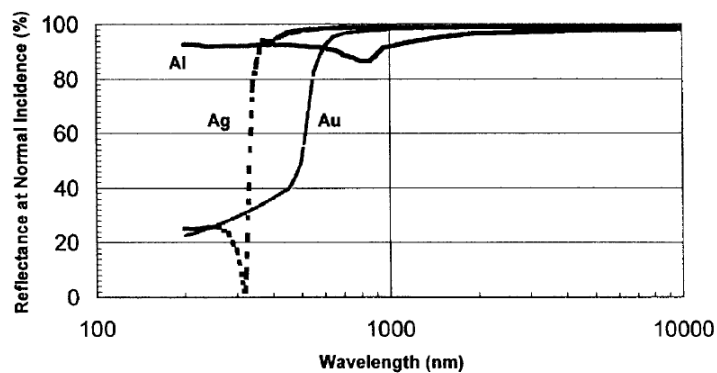


Fig. 1 Reflectance of evaporated metals in the visible and infrared

Ex. 1016 at 3 (Figure 1).

142. And Bartek:

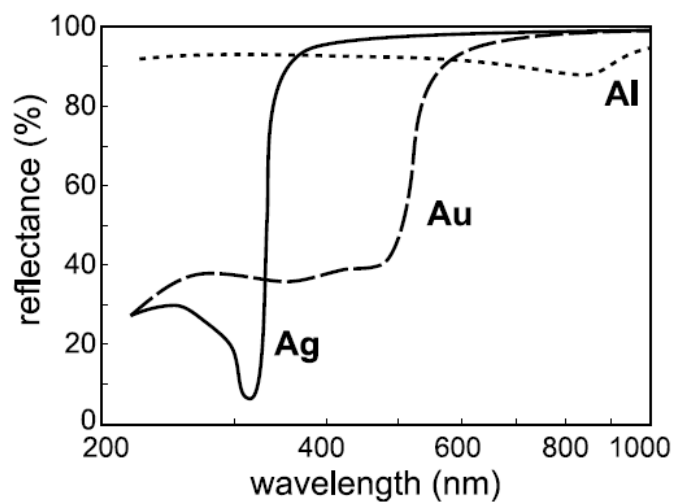


Figure 1. Reflectance of silver, gold and aluminum as a function of the radiation wavelength, after [5].

Ex. 1017 at 162 (Figure 1).

143. And, Sanpei explains that when silver is used, there is “total light reflectance of 85% or more in the whole region of a wavelength from 400 to 740 nm.” Ex. 1015 at [0088], FIG. 5.⁷

3. Claim 5

“The apparatus of claim 1, wherein the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater.”

144. Cao753 discloses the claimed “*the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater*”, for example, through its disclosure to have up to 1 mm spacing as applicable to Figure 5. Ex. 1005 at [0020], [0023]. Cao753 also discloses claim 1, from which claim 5 depends, as I explained above.

145. First, I note that Cao753 discloses in Figure 5, below, an “**array of LED chips 507a, 507b, 507c** within the well” being spaced apart from each other

⁷ As I discussed above, even though the legend in Figure 5 of Sanpei (Ex. 1015) is incorrect, I note that, in Figure 5, the curve for the white resin is shown as a solid line, and the silver curve is a dashed line, as identified in paragraph [0088] of Ex. 1015.

(i.e., the claimed “at least a portion of the LED chips form an array having a chip spacing”). Ex. 1005 at [0020] (emphasis and color added).

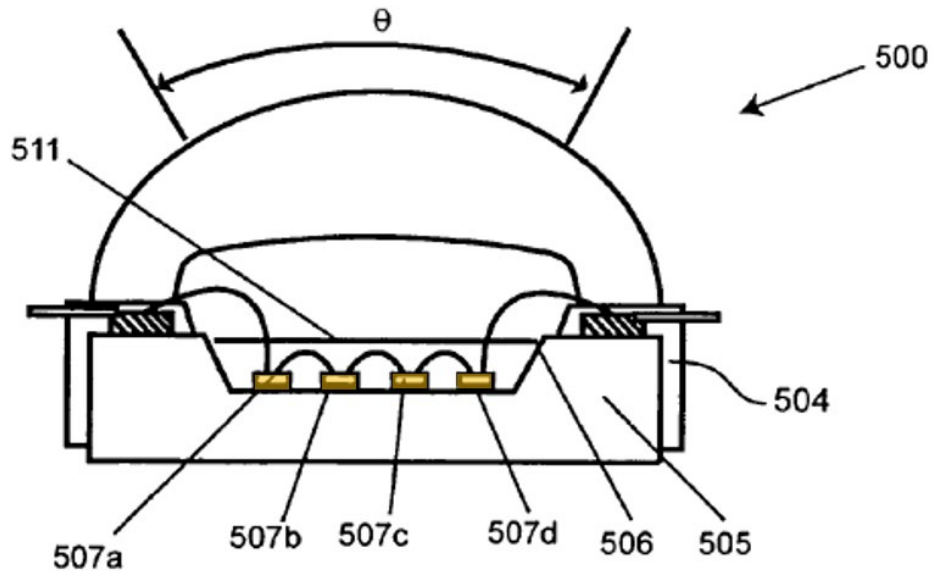


Fig. 5

Ex. 1005, FIG. 5 (coloring added to figure).

146. Second, Cao753 discloses the spacing to use in its LED module embodiments with multiple LED chips, such as in Figure 5. Ex. 1005 at [0023]. In those multi-chip embodiments, Cao753 teaches that “the spacing between chips can be adjusted from zero to **more than 1 mm**, depending on the application requirements.” Ex. 1005 at [0023].

147. Cao753’s disclosure meets the claimed “*chip spacing is approximately 0.5 millimeters or greater*”, and I note that the half-way point between the range in

Cao753 is 0.5 mm, meaning that Cao753 discloses claim 5. For example, a POSA would have understood that Cao753's disclosure encompasses the claimed "*chip spacing is approximately 0.5 millimeters or greater*", when the application so required (to optimally reflect the light emitted from the LED chips out of the package, to reduce the amount of light blocked by adjacent chips, etc.).

148. I note, as I did above, that the '988 Patent places no significance on the effects of the particular spacing dimensions. It only states to use a "pre-determined spacing" that may be "0.5 millimeters or greater" or other spacing resulting in exposed regions. Ex. 1001 at 5:16-29, 6:10-17. That too, is simply an application requirement, as in Cao753 (*e.g.*, based on the chip size, the chip materials, the number of chips in the package, the package size, and the well size and angle).

4. Claim 6

"The apparatus of claim 1, wherein the plurality of LED chips provide separate thermal and electrical paths."

149. Cao753 discloses the claimed "*the plurality of LED chips provide separate thermal and electrical paths*", for the reasons I explained above regarding limitation 1[b] (regarding the downward thermal path in Figure 5 of Cao753) and limitation 1[d] (regarding the separate horizontal electrical path in Figure 5 of Cao753 from chip to chip). I summarize this further in the following paragraphs. Cao753 also discloses claim 1, from which claim 6 depends, as I explained above.

150. As I explained in limitation 1[b], Cao753 discloses a thermal path downward from the LED chips 507a-d through the primary heat sink 505. As I explained in limitation 1[d], Cao753 discloses a separate electrical path from chip to chip wired in series and to the end connector leads. The design in Figure 5 results in Figure 5 having separate thermal and electrical paths, which I note are consistent with the '988 Patent's disclosure (such as regarding Figure 3, as I explained in Section VII).

151. Figure 5 of Cao753, below, shows the **thermal path** and separate **electrical path**.

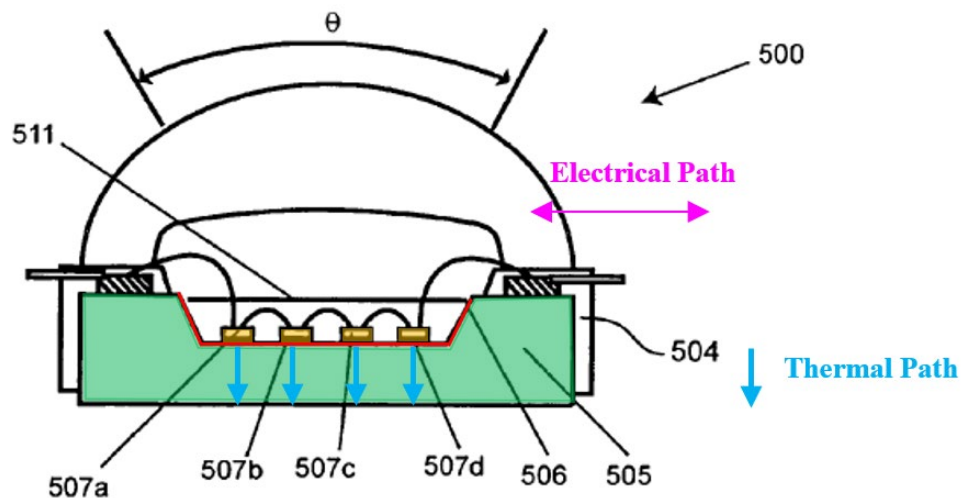


Fig. 5

Ex. 1005, FIG. 5 (coloring and magenta arrow added to indicate the electrical path and blue arrows to indicate the thermal path added to figure; words “Electrical Path” and “Thermal Path” also added to figure).

5. Claim 7

“The apparatus of claim 1 wherein the plurality of LED chips have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface.”

152. Cao753 discloses that its LED chips 507a-d “*have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface*”, as required by claim 7. Cao753 also discloses claim 1, from which claim 7 depends, as I explained above.

153. I note that claim 7 claims conventional wire bonded LED chips (with two wire bonds) which have top contacts for connecting to the wires (resulting in powering the LED when power is supplied) and an opposite bottom surface that is mounted into a package (such as onto a substrate). Ex. 1005 at [0028]-[0029], [0032]; Ex. 1013 at 95-96, FIG. 5.2.3(a); Ex. 1011 at 10:61-10:67, 11:4-11:24, 12:61-13:30, FIGs. 17a, 18a, 24a, 25a. I have explained this in Section IX.A.1.

154. I also note that the '988 Patent admits in its “Background” section that LEDs have p and n contacts for applying power to the LED through wire bonds:

A light emitting diode (LED) is a semiconductor material impregnated, or doped, with impurities. These impurities add “electrons” and “holes” to the semiconductor, which can move in the material relatively freely. Depending on the kind of impurity, a doped region of the semiconductor can have predominantly electrons or holes, and is referred to as an n-type or p-type semiconductor region, respectively. In LED applications, the semiconductor includes an n-type

semiconductor region and a p-type semiconductor region. A reverse electric field is created at the junction between the two regions, which cause the electrons and holes to move away from the junction to form an active region. When a forward voltage sufficient to overcome the reverse electric field is applied across the p-n junction, electrons and holes are forced into the active region and combine. When electrons combine with holes, they fall to lower energy levels and release energy in the form of light.

During operation, a forward voltage is applied across the p-n junction through a pair of electrodes. The electrodes are formed on the semiconductor material with a p-electrode formed on the p-type semiconductor region and an n-electrode formed on the n-type semiconductor region. **Each electrode includes a wire bond pad that allows an external voltage to be applied to the LED.**

Ex. 1001 at 1:9-32 (emphases added).

155. Cao753's LED chips 507*a-d* are consistent with conventional wire-bonded LED chips, as Cao753 itself discloses. Ex. 1005 at [0020], [0028]-[0029], [0032].

156. Cao753 discloses, in Figure 5, that the "chips in this figure are wired in series", which a POSA would have understood to mean that the chips have two top contacts to connect to the wires. Ex. 1005 at [0020]. Cao753 further discloses that the chips are mounted to the substrate surface as I discussed regarding limitation 1[b], namely, that there is an opposite bottom surface of the chips for such mounting. Ex. 1005 at [0020], [0028], [0034].

157. Cao753 also discloses that “The semiconductor light sources can include semiconductor chips that emit light when provided with electrical power”, that “The chips may include any of a variety of materials known for constructing chips that emit light”, that “The chips may include a variety of epitaxial layers grown on a substrate”, and that “Examples of substrates on which the semiconductors used in the lights depicted herein may be grown include Si, GaAs, GaN, ZnS, ZnSe, InP, Al₂O₃, SiC, GaSb, InAs and others.” Ex. 1005 at [0029].

158. Cao753 also discloses:

Epitaxial layers and structures of semiconductor light emitting chips useful in lights disclosed herein may include a substrate (such as sapphire) that serves as a carrier pad or platform on which to grow the chip's epitaxial layers. The first layer placed on the substrate may be a buffer layer (such as a GaN buffer layer). Use of a buffer layer reduces defects in the chip that would otherwise arise due to differences in material properties between the epitaxial layers and the substrate. **Then a contact layer, such as n-GaN, may be provided.** A cladding layer such as n-AlGaN Sub may be present to confine injected electrons. An active layer may be provided to emit the light when excited by electrons. An example active layer is such as AGaN with multiple quantum wells. The active layer is where electrons jump from a conduction band to valance and emit energy which converts to light. On the active layer, another cladding layer may be provided, such as p-AlGaN, to serve to confine electrons. **A contact layer such as p+ GaN may be provided that is doped for Ohmic contact. The contact layer may have an electrode mounted on it.**

Ex. 1005 at [0032] (emphases added).

159. In other words, Cao753 discloses a variety of known LED chips, which, relative to Figure 5, include p and n contacts on the top for connecting to the wires as explained by Cao753 itself and which are on the opposite side of the bottom surface (the claimed “*first surface*”), and thus the contacts are on different surface(s) than the bottom surface. This is consistent with Cao753’s disclosure and my explanation above in this section and in Section IX.A.1, that the electrical contacts are on the opposite side of - and thus on different surface(s) than - the bottom surface. Ex. 1005 at [0020], [0029], [0032].

160. Figure 5, below, depicts in a side view an LED chip’s **bottom surface** mounted to the heat sink’s **reflective surface** and the chip’s **top surface** that includes electrical contacts. Ex. 1005 at [0020], [0028]-[0029], [0032]. As the chips are small and somewhat difficult to see in Figure 5, I have also added a magnified view of chip 507*d* to the Figure 5, below. This magnified view is the same as for the other chips, 507*a*, 507*b*, and 507*c*.

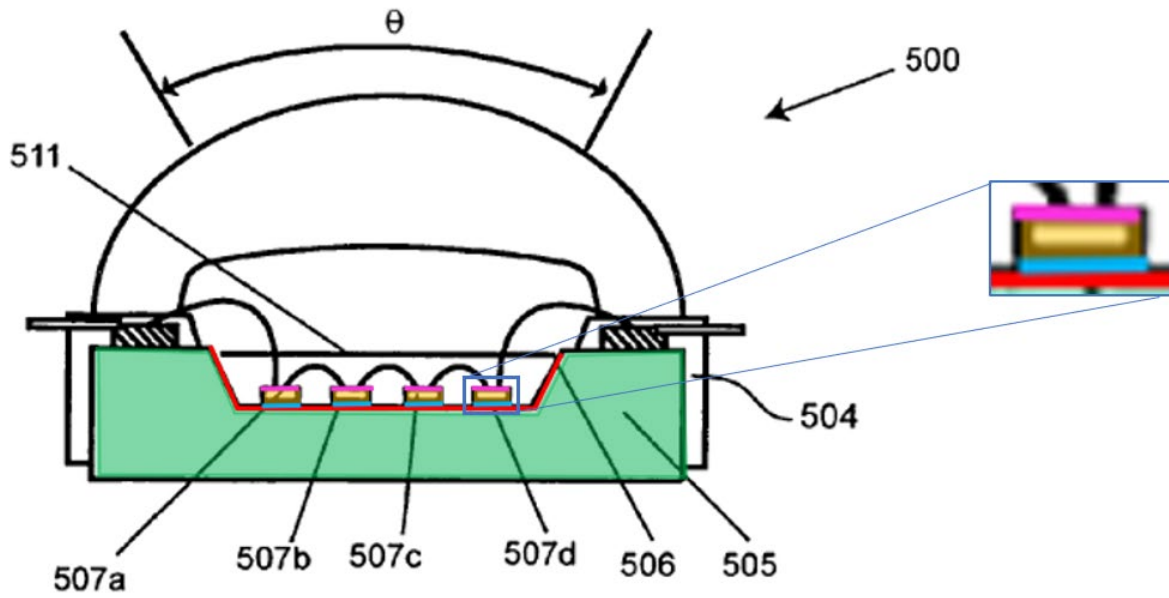


Fig. 5

Ex. 1005, FIG. 5 (coloring added to figure).

6. Claim 8

“The apparatus of claim 1, wherein the metal substrate is mounted directly to a heat sink.”

161. Cao753 discloses that the claimed *“the metal substrate is mounted directly to a heat sink”*, which in Figure 5 corresponds to the primary heat sink 505 being mounted directly to a secondary heat sink. Ex. 1005 at [0024], [0027]-[0028], claims 1, 12, 22 of Cao753. Cao753 also discloses claim 1, from which claim 8 depends, as I explained above.

162. Cao753 discloses that the heat sinks, including in Figure 5, “may be of a single material or a combination of two different kinds of materials, the first with

a low thermal expansion rate and the second with high thermal conductivity.” Ex. 1005 at [0027]. As explained in limitation 1[a], Cao753 discloses, in Figure 5, a primary heat sink 505 (the claimed “*metal substrate*”). Ex. 1005 at [0020].

163. Cao753 further discloses a variety of means to mount the primary heat sink to the secondary heat sink, both with and without adhesives: “The primary heat sink can be attached to a **secondary heat sink** if desired, such as; [sic: such as,] **by use of a heat conductive and/or electrically insulative adhesive, welding, brazing, soldering or mechanical fixation.**” Ex. 1005 at [0024] (emphases added). “Adhesives such as described [in Cao753] can be used to mount a chip to a primary heat sink, or to mount a primary heat sink to a secondary heat sink, or both.” Ex. 1005 at [0028]. Cao753 also discloses that this “secondary heat sink” may be “directly ... attached” to the “primary heat sink,” Ex. 1005 claims 1, 12, 22, and that this direct attachment results in an efficient thermal path through the secondary heat sink (*e.g.*, with no intervening insulating material, just like in limitation 1[b]). Ex. 1005 at [0017], [0024], [0027], [0028], claim 1, 16 of Cao753.

164. Accordingly, a POSA would have understood that Cao753 discloses to directly mount primary heat sink 505 to a secondary heat sink, regardless of whether the claimed “*mounted directly*” (i) allows for an adhesive (such as heat conductive adhesive without additional intervening insulating material) or (ii) does not allow for any adhesive or intervening material.

165. I also note, consistent with the knowledge of a POSA (as evidenced by the prior art I discuss herein), that the '988 Patent does not explain how to mount its metal substrate directly to its heat sink (only that it is “mounted directly”). Ex. 1001 at 5:46-62, 6:23-26.

7. Claim 9

“The apparatus of claim 1, wherein the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface.”

166. Cao753 discloses, in Figure 5, the claimed “*the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface.*” Cao753 also discloses claim 1, from which claim 9 depends, as I explained above.

167. As I explained for limitation 1[b], Cao753 depicts and describes relative to Figure 5 that an electrical connection is formed by wiring the LED chips 507a-d in series. Ex. 1005 at [0020].

168. Figure 5, below, shows such wire-bonded LED chips 507a-d that are connected chip to chip. A POSA would have understood that there is no electrical connection between LED chips 507a-d and the reflective surface of the primary heat sink 505 because, if there were such a connection, the package would not function, as it would short circuit. Ex. 1005 at [0019]-[0020].

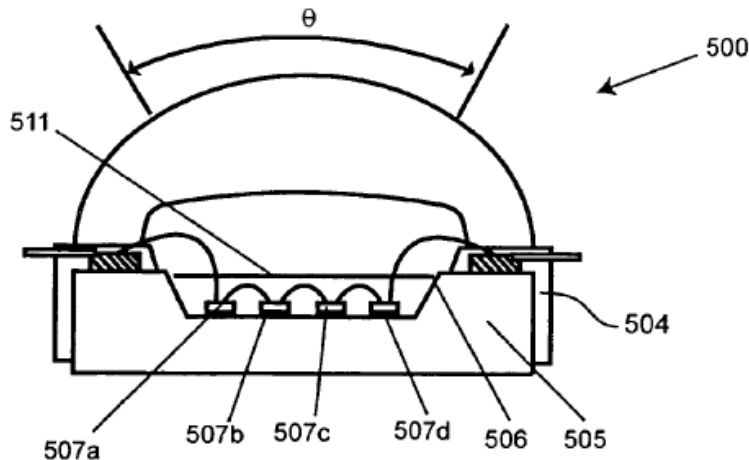


Fig. 5

Ex. 1005, FIG. 5.

C. Ground 2: Cao753 Renders Claims 1 and 4-9 Obvious

169. In my opinion, Cao753 anticipates claims 1 and 4-9, as I explained in Section IX.B. However, to the extent it is determined that Cao753 does not disclose every limitation, arranged as in the claims, in my opinion, Cao753 also renders these claims obvious, as I explain below. More particularly, I explain below why Cao753 renders claims 1 and 4-9 obvious if it is determined that Cao753 does not expressly or inherently disclose limitation 1[a], limitation 1[c], or claim 5 in its Figure 5 embodiment.

Limitation 1[a] “a metal substrate having a reflective surface; and”

170. As I explained regarding limitation 1[a] in Section IX.B.1, Cao753 discloses that the primary heat sink, such as primary heat sink 505 in Figure 5 (*i.e.*,

the claimed “*metal substrate*”) may be various metals, including aluminum, silver, or copper. As I also explained regarding limitation 1[a], a POSA would have understood that, when the substrate is made of a reflective metal (such as aluminum, silver, or copper) it necessarily has a reflective surface, which is consistent with the ’988 Patent’s teaching that a reflective surface can be “bare” metal such as “bare ... aluminum.” Ex. 1001 at 4:63-65.

171. To the extent, however, that the claim requires the “*metal substrate*” to have an additional reflective surface, the claims would still have been obvious in view of Cao753. That is, as I explain below, it would have been obvious to a POSA to make the surface of primary heat sink 505 reflective, for example by plating or polishing the surface.

172. First, Cao753 teaches to plate or polish the surface of a well to enhance reflectivity. Cao753 discloses, in Figure 4, a “flip-chip design” with an LED chip mounted on a pad inside a well. Ex. 1005 at [0019]. Cao753 discloses, in Figure 4, that the pad’s “upper surface may be light reflective so that light is reflected from the pad in a useful direction” and that the pad “may be coated with a light reflective film, such as Au, Al or Ag.” Ex. 1005 at [0019]. Cao753 also discloses, in Figure 4, that “The well may also include a reflective coating or polished surface.” Ex. 1005 at [0019].

173. Second, the Cao753 Figure 4 design is similar to Cao753's Figure 5 (differing primarily in the number of chips and that Figure 4 relies on a flip chip). Cao753's teaching regarding Figure 4 and the similarities with Figure 5: (i) demonstrate to a POSA that Cao753 was concerned with ensuring that light is reflected from the LED chips in a useful direction; and (ii) explain that using a reflective surface in the well of the metal substrate is an effective means of achieving this goal. Ex. 1005 at [0019]. I note that, more generally, polishing or plating was a commonly known and desirable method of increasing light reflectivity in LED packages at the time of the '988 Patent - including in various references to Cao and others - with wire-bonded LED packages. For example:

- Cao630 teaches that "The wells [of an LED package] may include a light reflective surface for reflecting light emitted by the chips outward in a useful direction" and that "walls and bottom of the well" may be polished, plated, coated, etc. to reflect light and improve reflectivity in Cao630's Figure 3a with a wire-bonded LED, like in Cao753's Figure 5. Ex. 1007 at [0019]-[0020].
- Cao253 similarly teaches that "The walls and bottom of the well may be polished to be light reflective, or may be covered, plated, painted or bonded with a light-reflective coating such as Al, Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastics and others to reflect light and thereby improve light source efficiency." Ex. 1011 at 12:67-13:4.
- Cao975 teaches that "The well may also include a reflective coating or polished surface" where the well is designed such that "all of the light emitted from the chip can be reflected back in the light exit direction for highest light output." Ex. 1014 at [0012]-[0013].

- Sanpei discloses to plate a metal substrate with, for example, silver, to enhance light reflectivity. Ex. 1015 at [0011]-[0018], [0118], [0129]-[0130].

174. The above confirms and further shows that there was a known need and desire - and that there would be no technical difficulty (*e.g.*, a POSA would expect it to work) - in including a reflective surface (such as a polished or plated highly-reflective metal like silver or aluminum) in a metal substrate well to reflect light in a useful direction and thereby improve light source efficiency, as explained by various Cao and other references.

175. Third, as additional confirmation that a POSA would have understood the advantages of, and would have been easily able to, enhance a metal substrate's surface by plating or polishing primary heat sink 505 in Figure 5 of Cao753, in another similar reference where Cao is a named inventor (Cao975), Cao975 teaches that "the features of the LED 700 module [*i.e.*, with multiple LED chips wired in series in a well] are similar to those already discussed" (*e.g.*, that "The well may also include a reflective coating or polished surface"). Ex. 1014 at [0012]-[0013].

176. Fourth, I note that, consistent with the knowledge of a POSA as I have discussed, the '988 Patent does not explain how to plate or polish metal (only to do so). Ex. 1001 at 4:63-66, 6:1-3.

Limitation 1[c] “at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and”

177. As I explained regarding limitation 1[c] in Section IX.B.1, Cao753 discloses that the LED chips 507a-d are spaced apart to expose regions of the reflective surface of primary heat sink 505, where the exposed regions reflect light from the portion of the LED chips.

178. To the extent, however, that Cao753 does not expressly or inherently disclose the claimed “*the exposed regions reflecting light emitted from the portion of the LED chips,*” it would have been obvious to a POSA that the regions would reflect light emitted from the LED chips.

179. Consistent with my discussion above in this section regarding limitation 1[a], a POSA would have understood that in LED chips such as those in Cao753 and known in the art, light would be emitted and reflected against the various package surfaces including the surfaces of the bottom and sides of the well (including the exposed regions in Figure 5 of Cao753). Ex. 1005 at [0029]; Ex. 1013 at 95-97.

180. Cao753 also teaches that when a well is used, “**all** of the light emitted from the chip can be reflected back in the light exit direction for highest light output” and that such a well can “include a reflective coating or polished surface”,

for example, when a blue LED chip with yellow phosphor is used to produce white light visible by the human eye. Ex. 1005 at [0019]-[0020], [0029], [0032] (emphasis added). Thus, a POSA would have understood that the light is reflected by the surfaces of the well, including the exposed regions.

181. Further, as I discussed in limitation 1[c] and claim 5 in Sections IX.B.1 and IX.B.3, Cao753 explains that when multiple LED chips are used, “The spacing between chips can be adjusted from zero to more than 1 mm, depending on the application requirements.” Ex. 1005 at [0023]. Cao753 also discloses that in mounting the LED chips to the surface, light reflective adhesives can be used. Ex. 1005 at [0028]. A POSA would have understood that spacing the chips apart in Cao753 would have the advantage of reflecting light from the reflective surface and thus maximizing light capture and use, which Cao753 explains is important. Ex. 1005 at [0026].

182. A POSA also would have understood the known advantages of making the entire well reflective (including bottom and side surfaces) in a package like Figure 5 of Cao753, in order to reflect light emitted from the LED chips. For example, Cao630 explains just that: to polish, plate, coat, or otherwise enhance both the “walls **and** bottom of the well” in order to “**to reflect light and thereby improve light source efficiency.**” Ex. 1007 at [0020] (emphases added). Cao253 discloses the same thing: “The walls **and** bottom of the well may be polished to be

light reflective, or may be covered, plated, painted or bonded with a light-reflective coating such as Al, Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastics and others **to reflect light and thereby improve light source efficiency.**” Ex. 1011 at 12:67-13:4 (emphases added).

183. In view of the above, a POSA would have understood, or at least found it obvious given the known advantages and ease of implementation, that the light emitted from the LED chips in Figure 5 of Cao753 is reflected by the exposed regions.

Claim 5 “The apparatus of claim 1, wherein the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater.”

184. As I explained regarding claim 5 in Section IX.B.3, Cao753 discloses an array of LED chips 507a-d where “*the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater*”, as required by claim 5. Cao753 also discloses or renders obvious claim 1, from which claim 5 depends, as I explained above.

185. However, to the extent that Cao753 does not expressly or inherently disclose the claimed “*approximately 0.5 millimeters or greater*” spacing in the context of Figure 5, claim 5 would still have been obvious to a POSA.

186. Cao753 discloses that “For light sources with multiple semiconductor light producing chips, the number of chips used may vary depending on application,

and can range from 1 to several hundred”, and that “The spacing between chips can be adjusted from zero **to more than 1 mm**, depending on the application requirements.” Ex. 1005 at [0023] (emphasis added). In this paragraph [0023] of Cao753 (Ex. 1005), Cao753 is explaining that the disclosed spacing applies to its disclosed light sources that have multiple LED chips, which a POSA would have understood to include the multi-LED chip embodiment in Figure 5 that Cao753 earlier discloses in paragraph [0020]. In other words, paragraph [0023] of Cao753 refers back to the earlier disclosed embodiments, including Figure 5. And, a POSA would have understood that such application requirement adjustments would be made consistent with the stated goals in Cao753 to more efficiently reflect light out of the package for highest light output.

187. A POSA would have understood to adjust the particular spacing “depending on the application requirements”, for example, based on the chip size, the chip make up, the number of chips in the package, the package size, and the well size and angle. This would simply require size adjustments and basic geometric measurements to factor in the various components and sizes, and to space the LED chips so that they are most efficiently and effectively located within the package.

188. I note that a POSA’s understanding as explained in Cao753 is consistent with the ’988 Patent, which states only that there should be some pre-determined spacing which can be 0.5 mm or greater, but does not explain the effects

of the particular spacing dimensions. Ex. 1001 at 5:16-29, 6:10-17. Nor does the '988 Patent explain particular dimensions (besides the 0.5 mm or greater horizontal and vertical spacing) including the size of the chips, the size of the package, etc., and instead stays silent and leaves such considerations to a POSA.

D. Ground 3: Cao753 Alone or in View of Cao630 Renders Claims 2-4 Obvious

189. In my opinion, Cao753 by itself or in view of Cao630 renders claims 2-4 obvious. I explain in this section how Cao753 by itself, or when viewed with Cao630, renders claims 2-4 obvious. I first provide an overview of a POSA's motivation to combine the references, and why a POSA would have had no technical difficulty and expected it to work. I then explain how Cao753 by itself or with Cao630 renders the claims obvious.

1. Motivation and Reasonable Expectation of Success

190. A POSA would have been motivated and had a reasonable expectation of success in combining the references - and in fact, a high expectation - for example, to apply the teachings in Cao630 to plate or polish the substrate surface to the LED package in Figure 5 of Cao753.

191. As an initial matter, Cao753 and Cao630 share a common inventor and are in the same field as each other and the '988 Patent (LED packaging for lighting

devices). Ex. 1005 at [0001], [0007], [0019]-[0023]; Ex. 1007 at [0002]-[0003], [0020]-[0021]; Ex. 1001 at Abstract, 1:6-53.

192. Cao753 and Cao630 are directed to the same problem: improved LED packaging for light emitting devices that, for example, address heat-dissipation and light-reflectivity issues, including for chip-to-chip wire-bonded LED chips. Ex. 1005 at [0019]-[0024], [0035]; Ex. 1007 at [0014]-[0015], [0020]-[0021]. So too is the '988 Patent. Ex. 1001 at 1:9-2:27. And, they all solve the problem in the same way: an LED apparatus including a metal substrate having a reflective surface, where LED chips are directly mounted to the surface and connected together through wire bonds, which results in an efficient thermal path through the substrate and a separate electrical path from chip to chip. Ex. 1005 at [0019]-[0024], [0028], [0035]; Ex. 1007 at [0014]-[0015], [0020]-[0021]; Ex. 1001 at 4:37-5:62.

193. As is evident by my explanation in Section IX.A.2, Cao753 and Cao630 also have highly similar and complementary disclosures. This is evident, for example, by comparing figures and disclosure in the references, such as comparing Cao753's Figure 4 to Cao630's Figure 3a and Cao753's Figure 5 to Cao630's Figure 3b. Note, for example, the multiple LED chips, in Cao753's Figure 5 and Cao630's Figure 3b, directly mounted in a well of a metal substrate, where the LED chips are wire bonded from chip to chip in series.

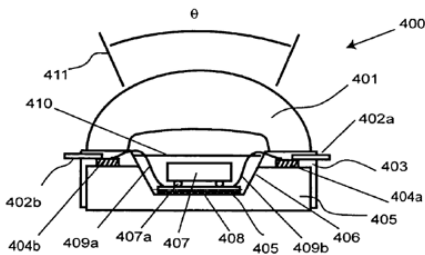
Cao753

Fig. 4

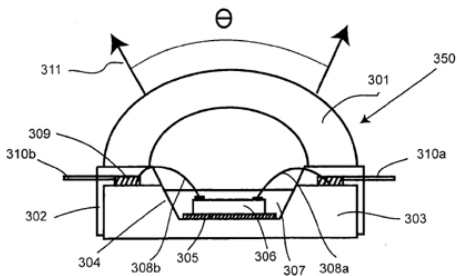
Cao630

Fig. 3a

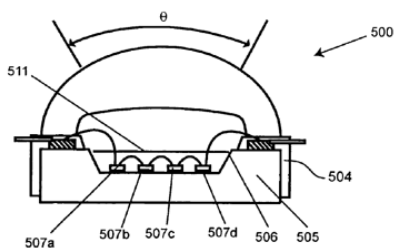


Fig. 5

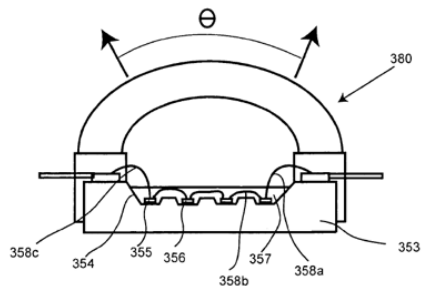


Fig. 3b

Ex. 1005, FIGs. 4, 5; Ex. 1007, FIGs. 3a, 3b.

194. A POSA would also have had a motivation to enhance the upper surface of primary heat sink 505 in Figure 5 of Cao753 using various known techniques (such as plating or polishing disclosed in both Cao753 and Cao630) in order to enhance the reflectivity of the surface to achieve the goals in both Cao753 and Cao630 to improve light output efficiency. Indeed, it would have been readily apparent from Cao753 itself - which teaches a package design that is intended for maximizing light output: “all of the light emitted from the chip can be reflected back in the light exit direction for highest light output”, and that “The well [of the primary heat sink] may also include a reflective coating or polished surface.” Ex.

1005 at [0019]. Cao753 is describing its Figure 4 (shown above) in this paragraph [0019], but a POSA would have understood that this teaching logically applies, more generally, to LED packages where the goal is to efficiently reflect all of the LED chip light in the light exit direction for highest output (such as in Figure 5 where the light is to be reflected out through the angle of departure (Θ)), Ex. 1005 at [0019]-[0020], FIG. 5, for example, as explained in the Cao references and as I explained in Section IX.A.1.

195. A POSA would also have understood that there were known advantages to polishing or plating the surface of the substrate well, including to improve light reflectivity and package performance, and that it would have been a simple addition using known polishing and plating techniques to polish or plate the surface of Cao753's substrate. Ex. 1005 at [0019]-[0020]; Ex. 1006 at [0066], [0078]-0082]; Ex. 1007 at [0020]; Ex. 1011 at 12:67-13:4; Ex. 1015 at [0018]; Ex. 1020 at [0043], [0066]. Numerous Cao and other references explain this common knowledge achievable through basic package design and known techniques. Ex. 1005 at [0019]-[0020], [0027]; Ex. 1006 at [0066]; Ex. 1007 at [0020]; Ex. 1011 at 12:67-13:4; Ex. 1015 at [0018].

196. I again note that the '988 Patent does not explain how to polish or plate, but rather states only to do so (consistent with the knowledge of a POSA that such polishing or plating were readily known). Ex. 1001 at 4:63-66, 6:1-3.

197. I provide further explanation below of why a POSA would have applied the teachings of Cao630 and the state of the art to Cao753.

2. Claim 2

“The apparatus of claim 1, wherein the reflective surface comprises polished aluminum.”

198. Claim 2 requires that the reflective surface of the metal substrate “*comprises polished aluminum.*” Cao753 alone or with Cao630 discloses such polished aluminum, and renders the claim obvious. Cao753 also discloses or renders obvious claim 1, from which claim 2 depends, as I explained above.

199. Cao753 discloses that the primary heat sink (*i.e.*, the claimed “*metal substrate*”) can be made of aluminum and include a well (in various Figures, including Figures 4 and 5, shown below). Ex. 1005 at [0019]-[0020], [0027].

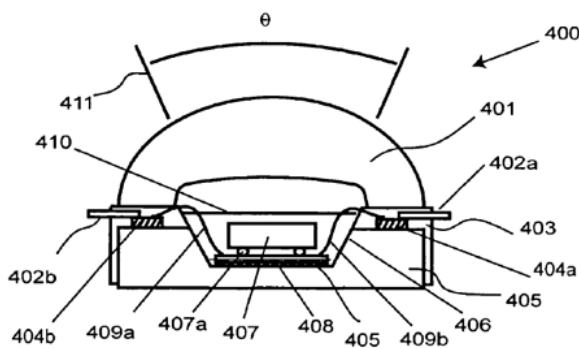


Fig. 4

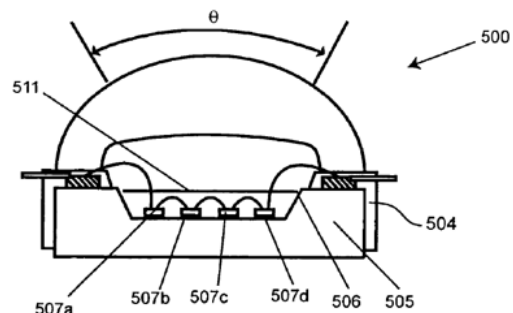


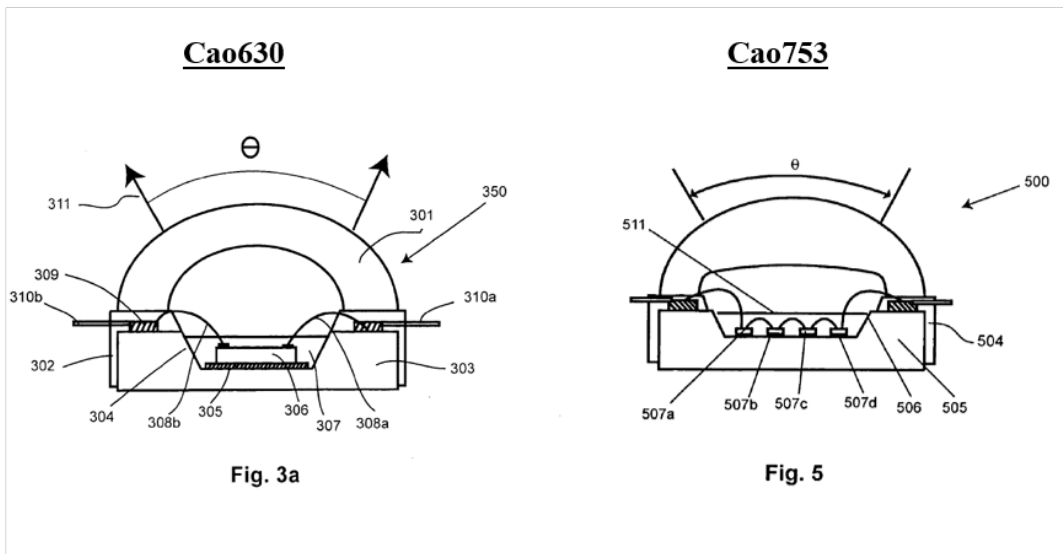
Fig. 5

Ex. 1005, FIGs. 4, 5.

200. Cao753 also discloses, relative to Figure 4, above left, that “The well may also include a reflective coating or **polished surface.**” Ex. 1005 at [0019] (emphasis added).

201. As I explained in Section IX.D.1, a POSA would have thought to polish substrate surfaces (such as the surface of the primary heat sink in Figure 5 in Cao753) to enhance the package light-emitting properties - which when primary heat sink 505 is aluminum (per Cao753), results in an aluminum substrate with a polished surface.

202. Additionally, Cao630 discloses, in its Figure 3a, below left, with a wire-bonded chip or chip array mounted in a well that “The walls and bottom of the well may be **polished to be light reflective**, or may be covered, plated, painted or bonded with a light-reflective coating such as **Al** [aluminum], Au, Ag, Zn, Cu, Pt, chrome, other metals, plating, plastic and others **to reflect light and thereby improve light source efficiency.**” Ex. 1007 at [0020] (emphases added), FIG. 3a (below); *see also* [0014] (explaining that the heat sink may be aluminum). The same discussion applies to Cao253, Figure 24a. Ex. 1011 at 12:67-13:4.



Ex. 1007, FIG. 3a; Ex. 1005, FIG. 5.

203. As can be seen above in the prior paragraph, the main difference between the figures is the single chip or array in Figure 3a of Cao630, whereas Figure 5 of Cao753 has multiple chips. Also, note that for Figure 3a, Cao630 indicates that “LED package 350 is depicted using a single chip or **chip array** 306.” Ex. 1007 at [0020] (emphasis added). These similarities provide further evidence to a POSA that there would have been no difficulty polishing the surface of aluminum primary heat sink 505 in Figure 5 of Cao753, and that it would result in an improved reflectivity.

3. Claim 3

“The apparatus of claim 1, wherein the reflective surface comprises silver plating.”

204. Claim 3 requires that the reflective surface of the metal substrate “*comprises silver plating.*” Cao753 alone or with Cao630 discloses such silver plating, and renders the claim obvious. Cao753 also discloses or renders obvious claim 1, from which claim 3 depends, as I explained above.

205. Cao753 discloses that the various primary heat sinks (*i.e.*, the claimed “*metal substrate*”) can be made of silver, aluminum, copper, etc. and include a well (in various Figures, including Figures 4 and 5, below). Ex. 1005 at [0019]-[0020], [0027].

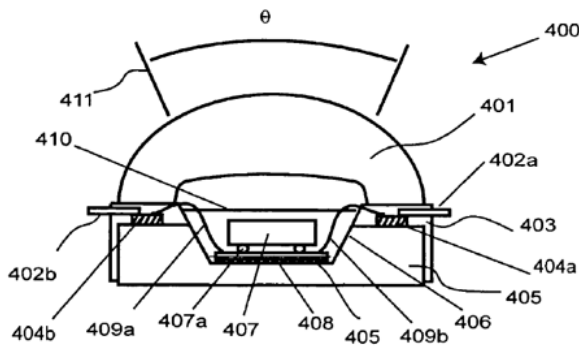


Fig. 4

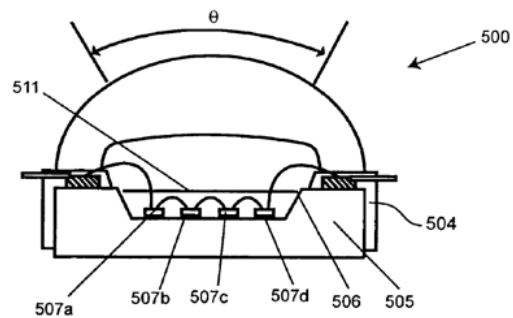


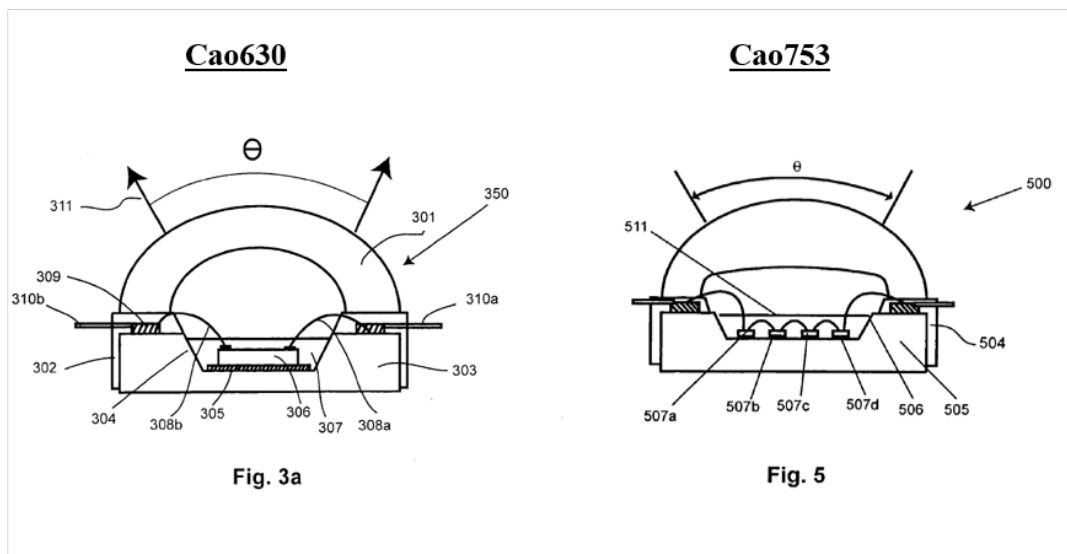
Fig. 5

Ex. 1005, FIGs. 4, 5.

206. Cao753 also discloses, relative to Figure 4, above left, that “The well may also include a **reflective coating** or polished surface.” Ex. 1005 at [0019] (emphasis added). Cao753 does not specify, however, plating, but as I explained in

Section IX.D.1, a POSA would have understood the known advantages of plating silver for the substrate's reflective surface to improve light reflectivity and package output light efficiency. And, when primary heat sink 505 in Figure 5 is plated with silver - as it would have been obvious to a POSA to do, as I explained - it would result in primary heat sink 505 in Figure 5 being silver plated.

207. Additionally, Cao630 discloses, in its Figure 3a, below left, with a wire-bonded chip array mounted in a well that “The walls and bottom of the well may be polished to be light reflective, or may be covered, **plated**, painted or bonded with a light reflective coating such as **Al** [aluminum], Au, **Ag** [silver], Zn, **Cu** [copper], Pt, chrome, other metals, plating, plastic and others **to reflect light and thereby improve light source efficiency.**” Ex. 1007 at [0020] (emphases added), FIG. 3a (below). The same discussion applies to Cao253, Figure 24a. Ex. 1011 at 12:67-13:4.



Ex. 1007, FIG. 3a; Ex. 1005, FIG. 5.

208. As can be seen above in the prior paragraph, the main difference between these two figures is the single chip or array in Figure 3a of Cao630, whereas Figure 5 of Cao753 has multiple chips. Also, note that for Figure 3a, Cao630 indicates that “LED package 350 is depicted using a single chip or **chip array 306.**” Ex. 1007 at [0020] (emphasis added). These similarities provide further evidence to a POSA that there would have been no difficulty plating silver on the surface of aluminum primary heat sink 505 in Figure 5 of Cao753, and that it would result in an improved reflectivity.

4. Claim 4

“The apparatus of claim 1, wherein the reflective surface has a reflectivity of 70% or greater.”

209. Claim 4 specifies the reflectivity of the reflective surface. This is simply a property of the surface of the material and obvious over Cao753 or in view of Cao630 for the reasons I discussed above in Sections IX.B.1, IX.B.2, and IX.D.1-3. Cao753 also discloses or renders obvious claim 1, from which claim 4 depends, as I explained above.

210. When aluminum or silver are used, the surface will have a reflectivity of 70% or greater in the visible wavelengths, as I explained in Section IX.B.2 (anticipation of claim 4 by Cao753). Ex. 1027 at 511 (Figure 11-1); Ex. 1022 at 376 (Figure 13.8); Ex. 1016 at 3 (Figure 1); Ex. 1017 at 162 (Figure 1); Ex. 1015 at [0088],⁸ [0118]-[0119].

⁸ As I discussed above, even though the legend in Figure 5 of Sanpei (Ex. 1015) is incorrect, I note that, in Figure 5, the curve for the white resin is shown as a solid line, and the silver curve is a dashed line, as identified in paragraph [0088] of Ex. 1015.

E. Ground 4: Baek Alone or in View of Cao630 Renders Claims 1-9 Obvious

211. In my opinion, Baek by itself or in view of Cao630 renders claims 1-9 obvious. I explain in this section how Baek by itself, or when viewed with Cao630, renders claims 1-9 obvious. I first provide an overview of a POSA's motivation to combine the references, and why a POSA would have had no technical difficulty and expect it to work. I then explain how Baek by itself or with Cao630 renders the claims obvious.

1. Motivation and Reasonable Expectation of Success

212. A POSA would have been motivated and had a reasonable expectation of success in combining the references - and in fact, a high expectation - for example, to apply Cao630's express teachings of a reflective substrate surface and direct mounting to Baek.

213. As an initial matter, Baek and Cao630 are in the same field as each other and the '988 Patent (LED packaging for lighting devices). Ex. 1006 at Abstract, [0003]; Ex. 1007 at [0002]-[0003], [0020]-[0021]; Ex. 1001 at Abstract, 1:6-53.

214. Baek and Cao630 are directed to the same problem: improved LED packaging for light emitting devices that, for example, address heat-dissipation and light-reflectivity issues, including for chip-to-chip wire-bonded LED chips. Ex.

1006 at [0003], [0032]-[0044], [0085]; Ex. 1007 at [0014]-[0015], [0020]-[0021]. So too is the '988 Patent. Ex. 1001 at 1:9-2:27. And they all solve the problem in the same way: an LED apparatus including a metal substrate having a reflective surface, where LED chips are directly mounted to the surface and connected together through wire bonds, which results in an efficient thermal path through the substrate and a separate electrical path from chip to chip. Ex. 1006 at [0066], [0072]-[0074], [0078]-[0084]; Ex. 1007 at [0014]-[0015], [0020]-[0021]; Ex. 1001 at 4:37-5:62.

215. As is evident by my explanation in Section IX.A.2, Baek and Cao630 share highly similar and complementary disclosures. This is evident, for example, by comparing the figures and disclosure in the references, such as comparing Baek's Figure 6 to Cao630's Figure 3b, below. Note, for example, the multiple LED chips each mounted in a subwell of a metal substrate, where the LED chips are wire bonded from chip to chip in series.

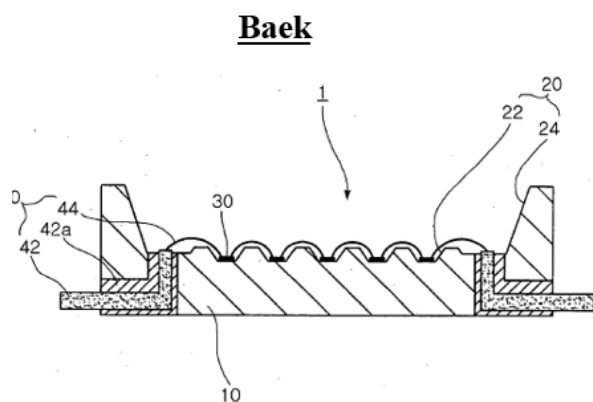


FIG. 6

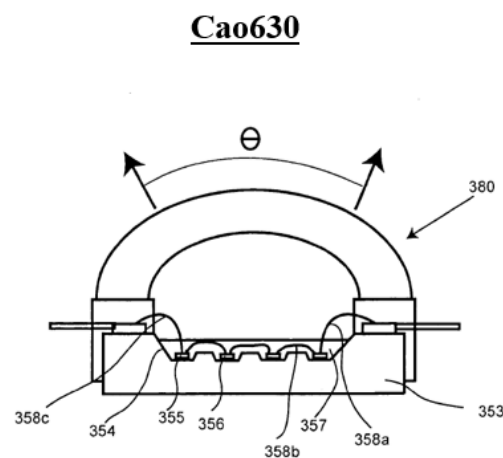


Fig. 3b

Ex. 1006, FIG. 6; Ex. 1007, FIG. 3b.

216. A POSA would have had a motivation to polish or plate the entire surface of the claimed “*metal substrate*” in Baek (*i.e.*, its base member and reflectors, as discussed in the following sections). As I discuss in more detail in the following sections (analyzing Baek’s disclosure relative to the claims), Baek already teaches to plate the surface of the well substrate using, *e.g.*, silver, in order to improve light efficiency. Ex. 1006 at [0081].

217. Moreover, to the extent Baek does not teach to plate or polish the entire surface of its base member and reflector unit (*i.e.*, the claimed “*metal substrate*”) (as I explain, Baek does teach to do so), it would have been logical, practical, and advantageous, as evidenced by Cao630 and the state of the art. I note, for example, that Cao630 explains why a POSA would plate, polish, coat, etc. with a reflective

material the **entire** surface of a substrate well (*i.e.*, “The walls **and** bottom of the well”): “to reflect light and thereby improve light source efficiency.” Ex. 1007 at [0020] (emphasis added). More particularly, Cao630 teaches “The walls **and** bottom of the well may be **polished to be light reflective**, or may be covered, **plated**, painted or bonded with a light reflective coating such **as Al** [aluminum], Au, **Ag** [silver], Zn, **Cu** [copper], Pt, chrome, other metals, plating, plastic and others **to reflect light and thereby improve light source efficiency.**” Ex. 1007 at [0020] (emphases added); *see also* [0014] (explaining heat sink materials such as aluminum, silver, or copper). This teaching would apply to Baek, where the polishing or plating occurs on base 10 and reflector unit 20 in Figures 5-8 of Baek.

218. A POSA would also have understood that there were known advantages to polishing or plating the substrate well’s surface, including to improve light reflectivity and package performance, and that it would have been a simple addition using known polishing and plating techniques to polish or plate the surface of the Baek substrate. Ex. 1005 at [0019]-[0020], [0027]; Ex. 1006 at [0066], [0078]-[0082]; Ex. 1007 at [0020]; Ex. 1011 at 12:67-13:4; Ex. 1015 at [0018]. Numerous Cao and other references explain this common knowledge achievable through basic package design and known techniques. Ex. 1005 at [0019]-[0020], [0027]; Ex. 1006 at [0066]; Ex. 1007 at [0020]; Ex. 1011 at 12:67-13:4; Ex. 1015 at [0018].

219. I again note that the '988 Patent does not explain how to polish or plate, but rather states only to do so (consistent with the knowledge of a POSA that such polishing or plating were readily known). Ex. 1001 at 4:63-66, 6:1-3.

220. And, while Baek does not expressly state how to mount its LED chips to its substrate surface, it does say to “mount” the LED chips and depicts direct mounting, as I discuss below regarding limitation 1[b]. Confronted with a reference that explains to mount the LED chips to the substrate, but not a specific means, a POSA logically would have looked to other references in the field (such as Cao630) for express mounting teachings and understood there were many known, routine ways to mount such LED chips. Ex. 1007 at [0015], [0020]; Ex. 1005 at [0028]. A POSA also would have understood the advantages of direct mounting as in Cao630: maintain and improve heat dissipation efficiency (consistent with the stated goals in both Baek and Cao630). Ex. 1007 at [0009], [0014]; Ex. 1006 at [0003], [0032]-[0036].

221. I provide further explanation below of why a POSA would have applied the teachings of Cao630 and the state of the art to Baek.

2. Claim 1

1[pre] “A light emitting diode (LED) apparatus comprising:”

222. Regardless of whether the preamble of claim 1 is found to be a limitation, Baek discloses the claimed “*light emitting diode (LED) apparatus*”, as

shown in Figures 5-8, below. Baek discloses a “high power LED [light emitting diode] package”, including LED chips 30 mounted to a metal substrate surface. Ex. 1006 at Abstract, [0060]-[0064], [0067].

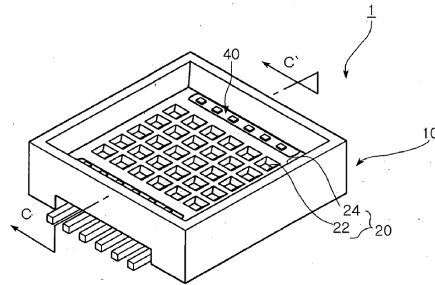


FIG. 5

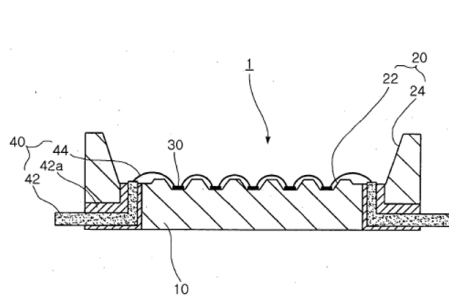


FIG. 6

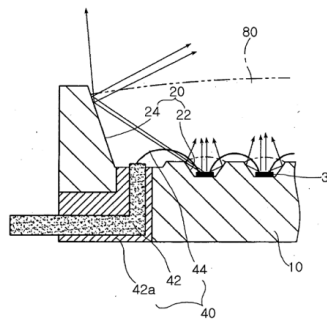


FIG. 7

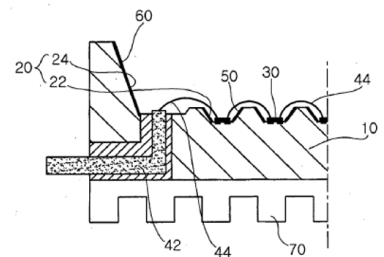


FIG. 8

Ex. 1006, FIGs. 5-8.

223. I note that these LED packages with LED chips mounted on a metal substrate being a light emitting diode apparatus of claim 1 is consistent with the '988 Patent and its description of an LED apparatus (such as “LED array apparatus 300” with a metal substrate on which LEDs are mounted in Figure 3 of the '988

Patent, which I discussed in Section VII (Overview of the '988 Patent)). Ex. 1001 at 2:48-50, 5:30-37. In other words, a POSA would have understood that the LED packages of Baek correspond to the claimed light emitting diode apparatus of the preamble in claim 1.

1[a] “a metal substrate having a reflective surface; and”

224. Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - the claimed “*a metal substrate having a reflective surface*”.

225. Baek discloses that “the base member 10 of the LED package 1 ... is selected from a metal lead frame, a metal substrate and a metal-plated resin substrate, which can at least dissipate or radiate heat outward.” Ex. 1006 at [0065]. Baek further explains regarding base member 10: “That is, the base member 10 of the invention is **made of or plated (coated) with a metal of excellent heat conductivity**, and thus can maintain heat dissipating ability when embodied into a high power packet where a plurality of LED chips are mounted.” Ex. 1006 at [0066] (emphasis added), [0081].

226. As an example of “a metal with excellent heat conductivity,” Baek further discloses that base member 10 can be “made of a material capable of dissipating (radiating) heat such as **Cu** [copper] of excellent heat conductivity.” Ex. 1006 at [0066], [0072] (emphasis added).

227. Baek further discloses a “reflector unit 20” with “first reflectors 22” and “second reflector 24”, where “the second reflector 24 of the reflector unit 20 is arranged around the first reflectors 22, forming an enclosed package reflector in order to collect lights emitted from the LED chips 30 and reflecting from the first reflectors 22 around the LED chips 30”, such as shown in Figures 6 and 7 (as well as Figures 5 and 8). Ex. 1006 at [0070], [0060], [0068]-[0073].

228. Baek explains that base member 10 and the reflectors can be fabricated as an integral unit “through single punching”:

Then, as shown in FIGS. 5 and 7, the base member 10 is configured as a lead frame as shown in FIG. 2, and made of a material capable of dissipating (radiating) heat such as Cu of excellent heat conductivity. Accordingly, **the base member 10 of the lead frame made of Cu can be fabricated with the first and second reflectors 22 and 24 through single punching.**

Ex. 1006 at [0072]-[0073] (emphasis added).

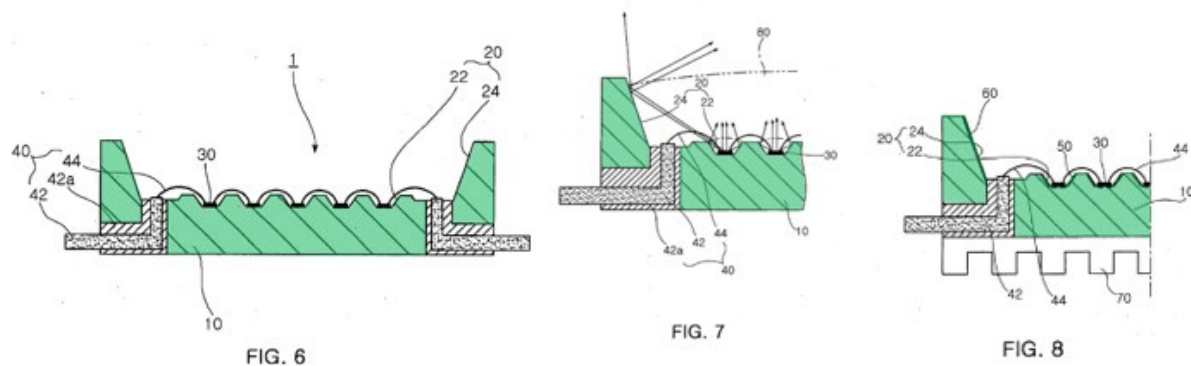
229. Given that Baek explains that its base member 10 and reflectors 22 and 24 are “fabricated” together “through single punching”, a POSA would have understood and treated together the base member and reflector unit as a single unit that can be copper, which together make up the claimed “*metal substrate having a reflective surface*”. I note again that copper is a reflective metal in the visible spectrum, and thus - consistent with the '988 Patent's disclosure that a reflective surface can simply be the “bare” surface of the substrate - a metal substrate made

of copper meets the claimed “*metal substrate having a reflective surface*” limitation. Ex. 1027 at 511, FIG. 11-1 (copper reflectivity); Ex. 1022 at 376, FIG. 13.8.

230. I further note that a POSA’s understanding that Baek discloses the claimed “*metal substrate*” in Figures 5-8 is additionally confirmed by the figures. For example, Figures 6-8 depict the metal reflectors and base member as a single unit constructed from the same material. Baek explains the relationship among the figures: (i) Figure 5 “is a perspective view illustrating high power LED package having excellent light efficiency according to the invention;” (ii) Figure 6 “is a cross-sectional view taken along the line C-C’ of FIG. 5;” (iii) Figure 7 “is a fragmentary cross-sectional view of important parts illustrating light emission from the LED package of the invention;” and (iv) Figure 8 “is a fragmentary cross-sectional view of important parts illustrating a high power LED package according to another embodiment of the invention”. Ex. 1006 at [0053]-[0056]. Baek also discloses that Figures 5-7 show the same LED package from different views: “FIGS. 5 to 7 show a high power LED package 1 of the invention, in which FIG. 5 illustrates a lead frame or base member when LED chips are not mounted, FIG. 6 is a cross sectional view illustrating a high power LED package of the invention, and FIG. 7 illustrates important parts.” Ex. 1006 at [0059]. Baek further explains that Figures 5-7 have base member 10 and reflectors. Ex. 1006 at [0070]-[0073]. It

also explains that Figure 8 is like Figures 5-7, but with “a reflect-activating layer”. Ex. 1006 at [0078]-[0082], [0043]. That these are the same LED package is further confirmed by analyzing the figures.

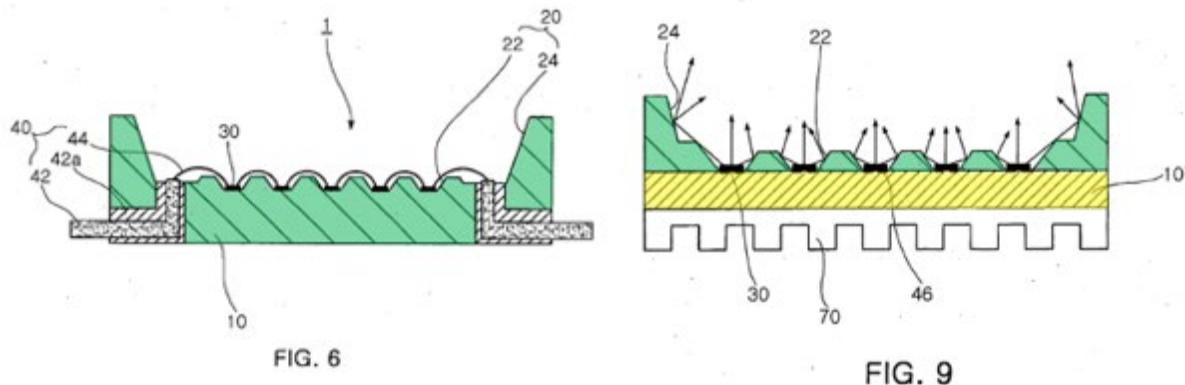
231. Relevant to the claimed “*metal substrate*” limitation, I note that Baek Figures 6, 7, and 8, below, include the same cross-hatching for the **reflectors and base member** (which indicates to the POSA they can be (and are, using single punching) a single structure and material).



Ex. 1006, FIGs. 6-8 (coloring added to figures).

232. As even further confirmation about Baek teaching the claimed “*metal substrate*” in Figures 5-8, I note that Baek’s depiction and description of Figures 6-8 contrast Baek’s Figure 9. In Figure 9, Baek explains that “**first and second reflectors** are made **separately** from the **base member 10’** and mounted thereon.” Ex. 1006 at [0074] (emphasis and color added). Figure 9 likewise depicts **reflectors 22 and 24** as being separate from **base member 10’** (indicated by the **contrast in**

different cross-hatching in Figure 9, shown below), which is different than Figures 6-8 above, that have the **same** cross-hatching. To illustrate this point, I have included side-by-side Figure 6 and 9 below.



Ex. 1006, FIGs. 6, 9 (coloring added to figures).

233. For additional confirmation of the single structure in Baek comprising the base member 10 and dual reflectors 22 and 24 in Figures 5-8 (*i.e.*, the claimed “*metal substrate*”), Baek discloses that “the dual reflector structure can preferably prevent light interference and raise heat dissipating efficiency with a lead frame having a group of indented recesses,” (*i.e.*, the indented recesses (reflectors) are part of the metal lead frame substrate). Ex. 1006 at [0032], [0034], [0069], [0083]-[0084].

234. Consistent with the disclosure in the '988 Patent that a metal substrate having a reflective surface may simply be the “bare” metal substrate, Ex. 1001, 4:63-65, Baek’s disclosure that its base member can be copper (a reflective metal),

and are thus reflectors (the claimed “*metal substrate*”), meets the claimed “*metal substrate having a reflective surface*”. Ex. 1027 at 511, FIG. 11-1 (discussing copper reflectivity in the visible spectrum); Ex. 1022 at 376, FIG. 13.8.

235. Based on the above, a POSA would have understood, or at least found it obvious, that Baek’s base member and reflectors (the claimed “*metal substrate*”) includes a reflective surface where light emitted from the LED chips is reflected off the bottom and side walls of the substrate well.

236. A POSA would also have understood that the base member 10 and reflector unit 20 (*e.g.*, in Baek Figures 5-8) correspond to the claimed “*metal substrate*”, consistent with the understanding of a POSA and the ’988 Patent. I again note, for example, that Graf (the Modern Dictionary of Electronics, 7th Ed.) states that a “substrate” is “Also called base material” and provides various definitions:

substrate—Also called base material. 1. The supporting material on or in which the parts of an integrated circuit are attached or made. The substrate may be passive (thin film, hybrid) or active (monolithic compatible). 2. A material on the surface of which an adhesive substance is spread for bonding or coating; any material that provides a supporting surface for other materials, especially materials used to support printed-circuit patterns. 3. The physical material upon which an electronic circuit is fabricated. Used primarily for mechanical support but may serve a useful thermal or electrical function. Also, a material on whose surface an adhesive substance is spread for bonding or coating, or any material that provides a supporting surface for other materials. 4. The base or support layer of a transistor or monolithic chip, which usually constitutes a major proportion of the total volume. When composed of ceramic, glass, or sapphire, the substrate functions mainly as a support during the operations of fabrication and encapsulation. However, when composed of heavily doped semiconductor material it normally performs the additional function of a distributed low-resistance connection to the physically lowest region of the device. 5. That part of an integrated circuit that acts as a support. 6. A slab of insulating material used for structural support of thick-film depositions and assembly components, usually high-purity (96 to 99 percent) alumina. *See* alumina. 7. The material on which the chips and other components are mounted, comparable to a printed circuit board. Substrate materials in common use include glass, sapphire, silicon, alumina, beryllia, and porcelainized steel. 8. The underlying material on which a microelectronic device is built.

Ex. 1012 at 745.

237. Consistent with the knowledge of a POSA, I also again note that the '988 Patent does not explain what its "substrate" is, other than stating exemplary material that it may be made of (aluminum), stating that heat is dissipated through it, and depicting it as a base material for, *e.g.*, the LED chips. Ex. 1001 at 1:57-64, 4:60-63, 5:46-62, FIG. 3. That is likewise true for Baek's "*metal substrate*" (*i.e.*, Baek's base member and reflector unit as I described above). I also note that the prior patent owner has asserted that a lead frame is a substrate in the context of these claims. Ex. 1023 at 15 (identifying "leadframe substrate").

238. To the extent that the claimed “*reflective surface*” needs to be enhanced to meet the claim, it would still be disclosed by Baek, or obvious over Baek alone or in view of Cao630.

239. As an initial matter, Baek discloses to add to both base member 10 and reflectors a reflective surface. Ex. 1006 at [0043], [0066]-[0071], [0078]-[0081].

240. Baek discloses that “the base member 10 of the invention is made of or **plated (coated)** with a metal of excellent heat conductivity, and thus can maintain heat dissipating ability when embodied into a high power packet where a plurality of LED chips are mounted.” Ex. 1006 at [0066] (emphasis added).

241. Baek discloses that “Preferably, the first reflectors have a **reflect-activating layer formed on a surface** thereof to raise reflecting efficiency of light generated from LED chips, and the second reflector has a **reflect-activating layer formed on a surface** thereof to raise reflecting efficiency of lights generated from the LED chips and reflecting from the first reflectors.” Ex. 1006 at [0043] (emphases added).

242. A POSA would have understood that these disclosures apply to the various embodiments in Baek, including in Figures 5-8. Alternatively, a POSA would have found it obvious to polish or plate the surface of the base member and reflectors (the claimed “*metal substrate*”) in these embodiments, as I explained in Section IX.E.1.

243. In addition, Baek depicts and describes that the reflectors reflect light emitted from LED chips, as shown, for example, in Figure 7, below, with the arrows indicating emitted light reflecting off the surface. Ex. 1006 at [0068]-[0071].

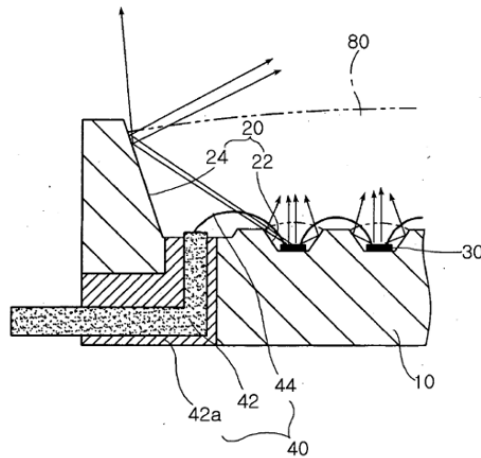


FIG. 7

Ex. 1006, FIG. 7.

244. Baek also depicts and describes the reflect-activating layers of the **metal substrate**, such as in Figure 8, below. In Figure 8, below, the reflective surfaces are shown in **red**, which include reflect-activating layer 50, reflect-activating layer 60, and the copper base member surface (all of which, again, are reflective in the visible spectrum when, *e.g.*, the base member is copper). I have included below side-by-side versions of Figure 8, the original version on the right and my colored version on the left.

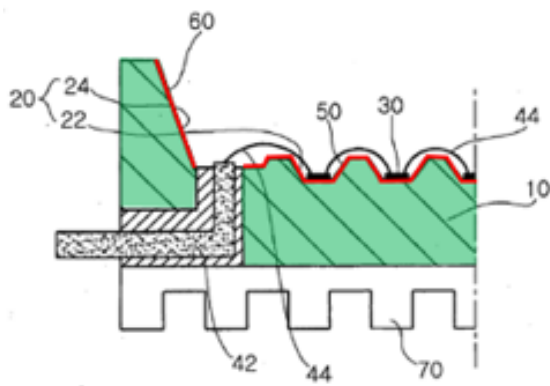


FIG. 8

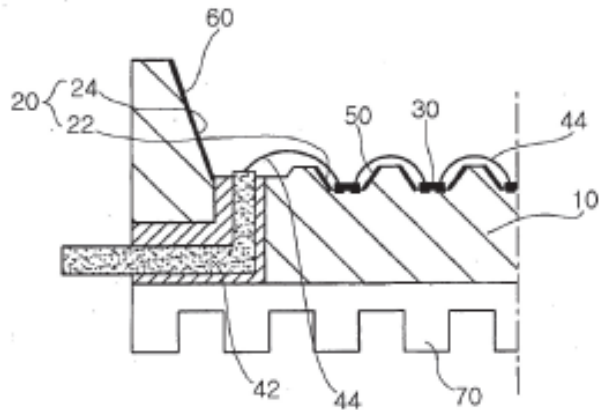


FIG. 8

Ex. 1006, FIG. 8 (coloring added to version of Figure 8 on left).

245. Baek discloses that the reflect-activating layers may be silver “plated on the surface” of the substrate. Ex. 1006 at [0081].

246. Although Baek does not expressly state that the reflect-activating layer would be under the LED chips within the well, a POSA would have understood (or at least found it obvious) to do so consistent with the stated goals in Baek to enhance light reflectivity. Baek already teaches to plate with metal the base member 10 (as I explained above), and when the plating was, for example, silver, it would result in the claimed “*metal substrate having a reflective surface*” that was enhanced through plating. And, logically, when minimizing the number of steps in a manufacturing process to create such a reflective layer on the base member and reflectors in Baek (the claimed “*metal substrate*”), the plating is applied to the surface, and such plating would be applied to the entire surface after the base member and reflectors

are fabricated together (*i.e.*, the surface of the base member and reflectors). This is further evidenced by Cao753, which describes to plate the entire well surface (bottom and walls) to enhance reflectivity. Ex. 1007 at [0020]. This would not only be typical, but it would also be simpler, more efficient, and more effective during manufacturing than individually plating the slopes of reflectors 22 and 24 to increase light reflection.

247. The known advantages and routine implementation of reflective metal substrates and walls are described in my Section IX.E.1. It is also confirmed by Cao630, which discloses - for similar LED packages with metal substrate wells - that “The walls and bottom of the well may be **polished to be light reflective**, or may be covered, **plated**, painted or bonded with a light reflective coating such as **Al, Au, Ag, Zn, Cu, Pt, chrome**, other metals, plating, plastic and others **to reflect light and thereby improve light source efficiency**.” Ex. 1007 at [0020].

1[b] “a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path and”

248. Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - the claimed “*a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path*”.

249. I first address the portion of the limitation 1[b], “*a plurality of LED chips mounted directly to the reflective surface of the metal substrate*”. I then address the “*creating an efficient thermal path*” portion of limitation 1[b].

250. **First**, Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - that its LED chips are directly mounted to the reflective surface of the base member, regardless of whether direct mounting (i) allows for the use of an adhesive or a “suitable adhesive” where no other intervening materials (such as an insulating dielectric) are present or (ii) does not allow for any adhesive or intervening material.

251. As an initial matter, Baek discloses that its LED chips are mounted on the surface of base member 10, for example, as in Figures 6-8: (i) “a plurality of LED chips mounted on the base member”, Ex. 1006 at [0035]; (ii) “That is, as shown in FIGS. 6 and 7, the high power LED package 1 of the invention generally includes a base member 10, a reflector unit 20 provided on the base member 10, a plurality of LED chips 30 mounted on the base member 10 and surrounded at least by first reflectors 22 of the reflector unit 20 and a connection unit 40 arranged in the base member 10 to electrically connect the LED chips 30 to the outside”, Ex. 1006 at [0060]; (iii) “Also, in the LED package 1 of the invention, each of the LED chips 30 is mounted inside each of the first reflectors 22 of the reflector unit 20 so that light emitted from the each LED chip 30 does not interfere with light emitted

from adjacent one”, Ex. 1006 at [0067]; and (iv) “Now, referring to FIGS. 6 and 7, in a case where at least a plurality of the LED chips 30 are mounted on the high LED package 1, each of the first reflectors 22 surrounds each of the LED chips 30, thereby preventing light emitted from the each LED chip from interfering with light emitted from adjacent one, which otherwise would degrade light efficiency”, Ex. 1006 at [0068].

252. Baek discloses that “**Preferably**, the base member comprises a substrate, wherein the connection unit comprises a connection pattern connected with the **LED chips which are surface-mounted on the substrate.**” Ex. 1006 at [0042] (emphasis added). Baek also discloses that it was known in the art that “LEDs are produced in the form of **Surface Mount Devices (SMDs) to be *directly mounted on* the PCB**” (*e.g.*, substrate). Ex. 1006 at [0014] (emphasis added). Taken together, a POSA would have understood that the LED chips in Baek are preferably directly mounted to the base member (that is, surface mounting indicates direct mounting known in the art, per Baek).

253. Direct mounting is illustrated in Baek’s Figures. For example, Figures 6 and 8, below, show that there are no intervening materials disclosed between **LED chips 30** and the **reflective surface** of the **base member and reflector unit**, demonstrating to a POSA that the chips are directly mounted to the reflective surface, as Baek notes was known and preferable in the art.

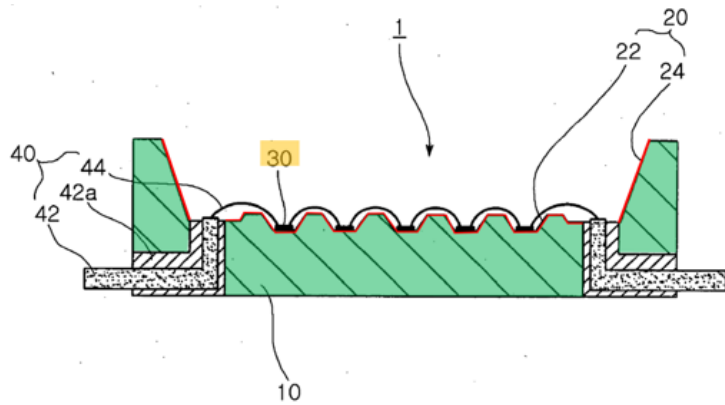


FIG. 6

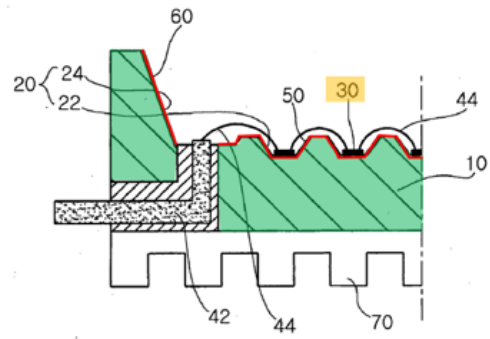


FIG. 8

Ex. 1006, FIGs. 6, 8 (coloring added to figures).

254. The direct mounting is also seen in the original figures without coloring, below:

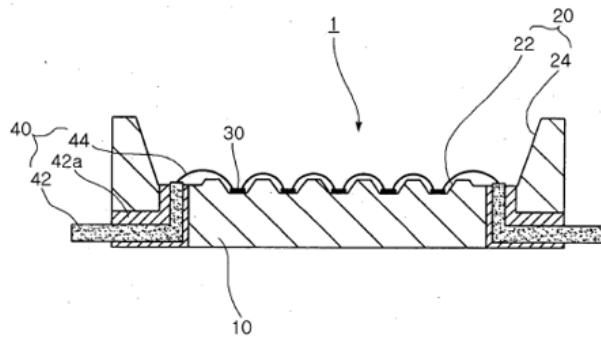


FIG. 6

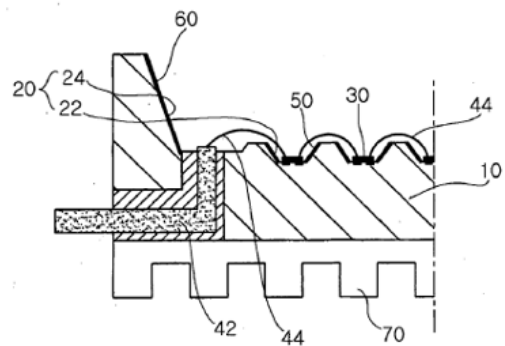


FIG. 8

Ex. 1006, FIGs. 6, 8.

255. A POSA further would have understood: (i) that the LED chips in Baek could be mounted to the surface in a number of ways, including using a heat

conductive adhesive or without any adhesive or other material; and (ii) the advantages of doing so (*e.g.*, efficiently dissipate heat through the metal substrate), which understanding is consistent with the goals of Baek to have “excellent light efficiency and improved heat dissipating characteristics, which completely satisfy [the] most important two factors for LED packages, thereby improving package reliability.” Ex. 1006 at [0085].

256. Among the examples known to a POSA, Cao630 discloses that mounting of the LED chips may be achieved by a variety of methods (with or without any adhesive or other material) including direct mount, mechanical fixation, brazing, welding, use of an adhesive or other methods, and notes that use of a heat conductive adhesive may be desired. Ex. 1007 at [0015] (Cao630 explaining to use various known methods including those summarized herein). Numerous other examples exist in the art that also demonstrate that direct mounting was both routine and desirable for mounting LED chips to substrate surfaces in LED packages (which are also consistent with the teachings and goals in Baek, including to improve heat dissipation):

- Hashimoto describes that prior-art lighting emitting devices had an “LED chip [that was]... **not mounted directly** on the metal plate” and was instead “mounted over the metal plate with the insulating layer”, whereas the Hashimoto disclosure had the “LED chip ... **mounted directly** on the bottom of the recess [of the metal plate].” Ex. 1021 at [0007], [0049] (emphases added).

- Hashimoto further explains the problems resulting when an LED chip is not directly mounted: “heat radiation of the light emitting device **decreases** [when direct mounting is not used], **as compared to the case where the LED is directly mounted on the metal plate**”. Ex. 1021 at [0007] (emphases added).
- Ishii discloses a wire-bonded LED that is “**directly mounted** on the basic surface of the base”, preferably using an “adhesive member ... having heat conductivity” which results in the LED chip and base being “thermally coupled”. Ex. 1020 at [0036]-[0037] (emphasis added).

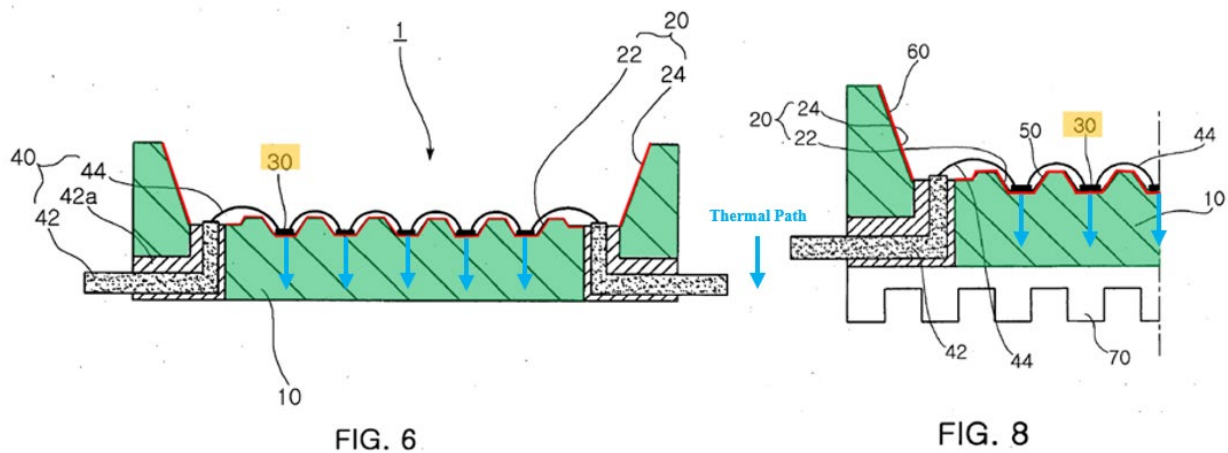
257. **Second**, the above results in the claimed “*creating an efficient thermal path.*”

258. As I discussed above, Baek explains that:

- The base member is a “metal of excellent heat conductivity, and thus can maintain heat dissipating ability when embodied into a high power packet [sic: package] where a plurality of LED chips are mounted.” Ex. 1006 at [0066].
- The base member “can at least dissipate or radiate heat outward” (relative to the side-view cut-out figures of Figures 6-8, in a downward vertical direction). Ex. 1006 at [0065].
- The base member and reflectors (the claimed “*metal substrate*”) can be “made of a material capable of dissipating (radiating) heat such as Cu of excellent heat conductivity.” Ex. 1006 at [0072]; where “the base member 10 of the lead frame made of Cu can be fabricated with the first and second reflectors 22 and 24 through single punching.” Ex. 1006 at [0073].
- An object of the Baek invention is to mount LED chips in recesses between reflectors to “improve heat dissipating efficiency of a base member, thereby imparting excellent heat dissipating characteristics to the LED package”, Ex. 1006 at [0034], and where the “base member comprises a member capable of dissipating heat”, Ex. 1006 at [0036].

Thus, the LED package of the Baek invention “has excellent light efficiency and improved heat dissipating characteristics”. Ex. 1006 at [0085].

259. Given the above teachings, a POSA would have understood that mounting the LED chips directly to the surface of its efficient heat-dissipating base member portion creates an **efficient thermal path** in the shortest distance (*e.g.*, when an insulating dielectric is not used). I have added arrows in **blue** to these figures to illustrate this path, as depicted in Baek Figures 6 and 8, below. Ex. 1006 at [0083]-[0085]. I note the result is consistent with the '988 Patent, the file history, and Patent Owner's positions in district court. Ex. 1001 at 4:37-59; Ex. 1002 at 280; Ex. 1008 at 18-20; Ex. 1009 at 12-13; Ex. 1010 ¶71; Ex. 1028 at 4-5.



Ex. 1006, FIGs. 6, 8 (coloring and blue arrows added to figures; words “Thermal Path” added to figure).

1[c] “at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and”

260. Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - the claimed “*at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips*”.

261. As can be seen in its figures, such as Figures 6-8, below, Baek discloses spacing the **LED chips** apart from each other with **reflector units** between the LED chips that have exposed regions of the **reflective surface** on the **base member**.

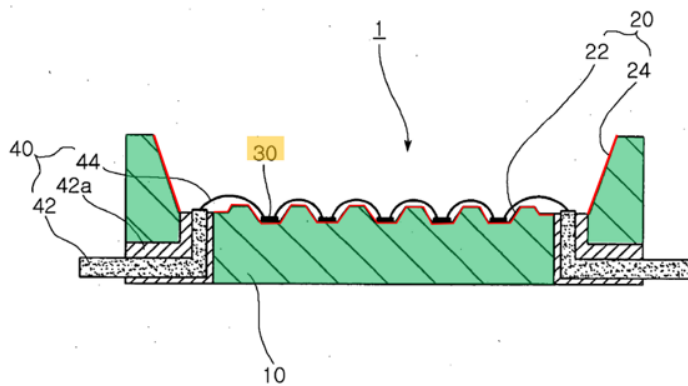


FIG. 6

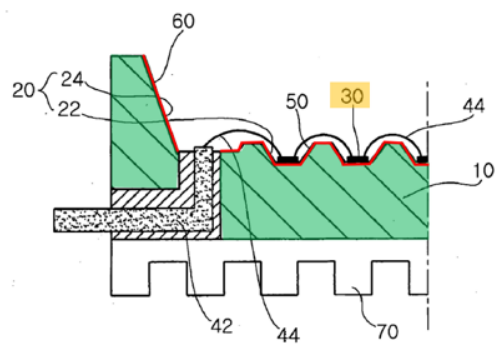


FIG. 8

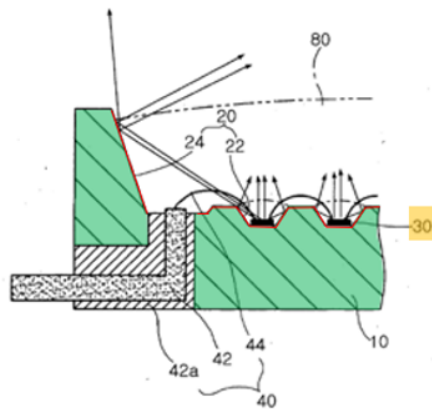


FIG. 7

Ex. 1006, FIGs. 6-8 (coloring added to figures).

262. This can also be seen in the original figures in Baek, such as Figure 7, below, where the spacing of the LED chips exposes regions of the reflective surface including the wells' bottoms and sides.

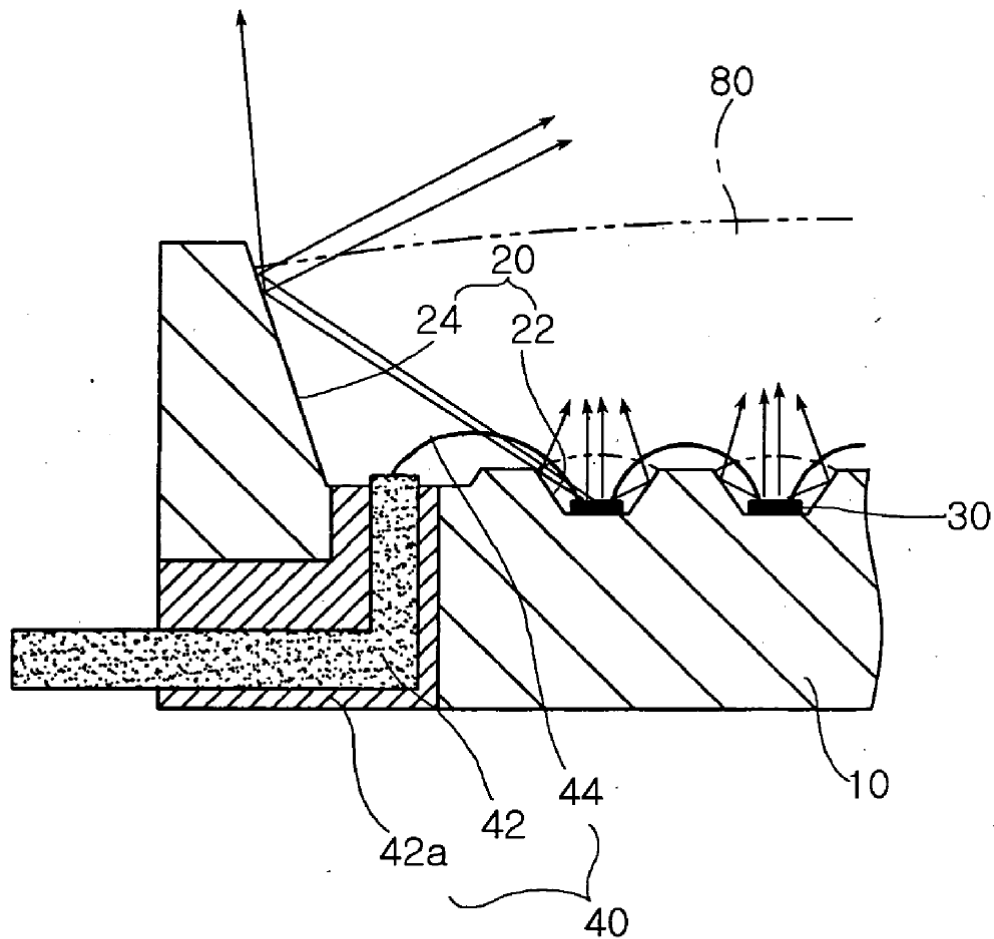


FIG. 7

Ex. 1006, FIG. 7.

263. As I explained in limitation 1[a] above for Baek, the light emitted from the LED chips 30 is reflected off the various exposed regions - including the walls and bottom of the reflective surface - that are exposed between the LED chips. As I explained above, including in Sections IX.B.1 and IX.C, such reflection is typical

of LED chips in packages. I note further that the '988 Patent does not explain any particular shape for its reflective surface or metal substrate, stating only that its metal substrate has such a surface (which is consistent with the knowledge of a POSA designing a particular LED package to appropriately size and shape the package and components to efficiently and effectively reflect the light out the package, as I have already explained above). Consistent with this knowledge and the fact that the claims do not claim any particular shape, I also note that the '988 Patent states that the particular shapes of its components "are not intended to limit the scope of [its] invention." Ex. 1001 at 3:8-25.

1[d] "an electrical path formed by connecting the LED chips in a chip to chip fashion."

264. Baek discloses in Figures 5-8 the claimed "*an electrical path formed by connecting the LED chips in a chip to chip fashion.*"

265. Baek discloses that "the lead frame is mounted on a main board of a device, and the connection unit 40 includes leads 42 attached to the base member 10 with insulating layers 42a interposed therebetween and bonding wires 44 for connecting the leads 42 with the LED chips 30" and "Then, the leads 42 are connected to an electric pattern on the main board." Ex. 1006 at [0077]. Baek also discloses that the chip-to-chip configuration was already known in the art. Ex. 1006 at [0021]-[0030], FIGs. 1-4 (prior art packages depicting chip-to-chip connections).

266. The chip to chip connection in Baek that forms an **electrical path** without a connection through the substrate is depicted in Figures 6 and 8, below (I have added **magenta** arrows to this figure to illustrate the electrical path). Such a connection resulting in the electrical path is consistent with the '988 Patent, as I discussed in Section VII, without a connection of the chips through the wires to the substrate. Ex. 1001 at 5:38-45, 6:18-21, FIG. 3.

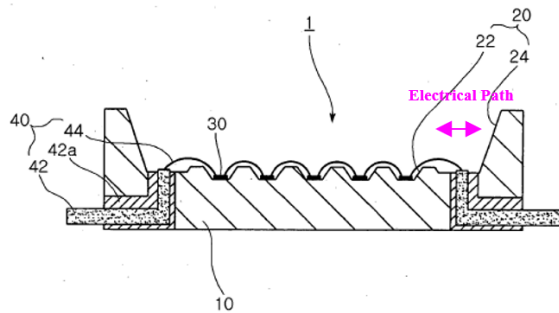


FIG. 6

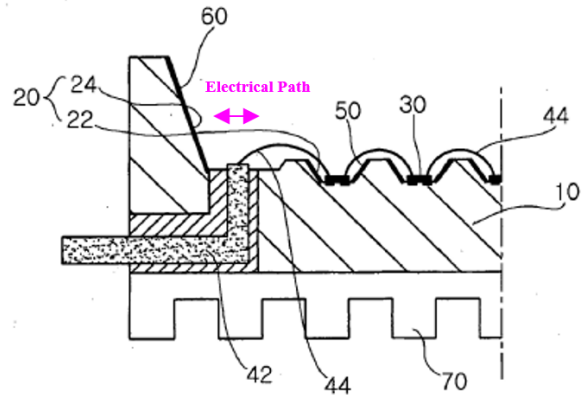


FIG. 8

Ex. 1006, FIGs. 6, 8 (coloring and arrows added to figures; words “Electrical Path” also added to figures).

3. Claim 2

“The apparatus of claim 1, wherein the reflective surface comprises polished aluminum.”

267. Claim 2 requires that the reflective surface of the metal substrate “*comprises polished aluminum.*” Baek in view of Cao630 discloses such polished

aluminum, and renders the claim obvious. Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 2 depends, as I explained above.

268. As I explained in the previous section (Section IX.E.2), Baek discloses using a base member and reflectors made of a “material capable of dissipating (radiating) heat such as Cu of excellent heat conductivity.” Ex. 1006 at [0072]-[0073].

269. Another known material capable of excellent heat conductivity is aluminum, which was known as a substrate material in LED packages and could be readily substituted into Baek. For example, Cao630 describes the interchangeability of using various metals including copper and aluminum as the substrate so long as the “materials [have] adequate heat conductance”. Ex. 1007 at [0014]. It is well known that aluminum and copper are two of the most thermally conductive metals Ex. 1018 at 10 and Ex. 1019, 4-157. The interchangeability was further confirmed by the applicant during prosecution when it asserted that “Because in general metals, have high thermal conductivity, such direct mounting results in creation of an efficient thermal path”. Ex. 1002 at 280.

270. A POSA would have understood that using aluminum instead of copper would provide high reflectivity - stated goals in both Baek and Cao630 - given that aluminum is highly reflective in the visible spectrum. Ex. 1027 at 511

(Figure 11-1); Ex. 1022 at 376 (Figure 13.8); Ex. 1016 at 3 (Figure 1); Ex. 1017 at 162 (Figure 1).

271. It would have been a simple substitution of materials to provide high package reflectivity. In other words, it would have been obvious to a POSA to use a polished aluminum substrate to enhance reflectivity in the LED package, for the same reasons discussed in Section IX.D.2, for example.

4. Claim 3

“The apparatus of claim 1, wherein the reflective surface comprises silver plating.”

272. Claim 3 requires that the reflective surface of the metal substrate “*comprises silver plating*.” Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - claim 3 for the same reasons as discussed above for limitation 1[a] (*i.e.*, when the reflective surface comprises silver plating as disclosed in Baek and commonly known to a POSA to enhance reflectivity and package performance). Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 3 depends, as I explained above.

5. Claim 4

“The apparatus of claim 1, wherein the reflective surface has a reflectivity of 70% or greater.”

273. Claim 4 specifies the reflectivity of the reflective surface. This is simply a property of the material surface and is disclosed by or obvious over Baek

or in view of Cao630, for the reasons I discussed above. Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 4 depends, as I explained above.

274. When aluminum or silver are used, the surface will have a reflectivity of 70% or greater in the visible wavelength, as I explained in Section IX.B.2 (anticipation of claim 4 by Cao753). Ex. 1027 at 511 (Figure 11-1); Ex. 1022 at 376 (Figure 13.8); Ex. 1016 at 3 (Figure 1); Ex. 1017 at 162 (Figure 1); Ex. 1015 at [0088] and Fig 5,⁹ [0118]-[0119].

6. Claim 5

“The apparatus of claim 1, wherein the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or greater.”

275. Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - that *“the at least a portion of the LED chips form an array having a chip spacing that is approximately 0.5 millimeters or*

⁹ As I discussed above, although the legend in Figure 5 of Sanpei (Ex. 1015) is incorrect, I note that, in Figure 5, the curve for the white resin is shown as a solid line, and the silver curve is a dashed line, as identified in paragraph [0088] of Ex. 1015.

greater” as required by claim 5. Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 5 depends, as I explained above.

276. First, Baek discloses that the LED chips 30 are spaced apart, as they are surrounded by the first reflectors 22 to prevent the light emitted from the LED chips from interfering with each other: “Now, referring to FIGS. 6 and 7, in a case where at least a plurality of the LED chips 30 are mounted on the high LED package 1, each of the first reflectors 22 surrounds each of the LED chips 30, thereby preventing light emitted from the each LED chip from interfering with light emitted from adjacent one, which otherwise would degrade light efficiency.” Ex. 1006 at [0068]. Baek additionally discloses this light-interference-prevention concept elsewhere, which is at the core of its LED package design, including:

- “As will be described in detail hereunder, in the first reflector unit 20 of the LED package 1 of the invention, the first reflectors 22 serve to surround the LED chips 30, respectively, to prevent any interference of lights emitted from adjacent ones of the LED chips 30, and the second reflector 24 serves to focus and collect the entire lights reflecting from the first reflectors 22 and directly emitted from the LED chips 30.” Ex. 1006 at [0063].
- “Accordingly, the LED package 1 of the invention with the dual reflecting structure of the first and second reflecting layers 22 and 24 can prevent light interference and achieve more excellent light emitting efficiency through individual reflectors. Moreover, the reflect-activating layer can further enhance light efficiency.” Ex. 1006 at [0082].
- “According to the high power LED package of the invention as set forth above, the first reflectors are provided corresponding to a

plurality of LED chips mounted on a single lead frame and the second reflector is arranged to surround the first reflectors. This as a result can produce light emitting characteristics, which completely prevent light interference and focus emission light, thereby enabling excellent light efficiency.” Ex. 1006 at [0089].

277. Baek discloses typical sizing as well:

“In addition, the LEDs are fabricated in a very small size of about 0.25 mm, and mounted on a lead frame via epoxy molding and then on a Printed Circuit Board (PCB).

A most typically used LED is provided in the form of a 5 mm plastic package. However, new types of packages are under development according to specific applications. The composition of a semiconductor chip determines the color of light emitted from an LED according to a specific wavelength.

In particular, LEDs are being further miniaturized as information communication devices are more reduced in size and slimmed, in which elements of the devices such as a resistor, a capacitor and a noise filter are further reduced in size. Recently, the LEDs are produced in the form of Surface Mount Devices (SMDs) to be directly mounted on the PCB.”

Ex. 1006 at [0012]-[0014].

278. In the embodiment depicted in Figures 5-7, Baek discloses an array of five LED chips by six LED chips (each subwell includes an LED chip, as explained in Baek):

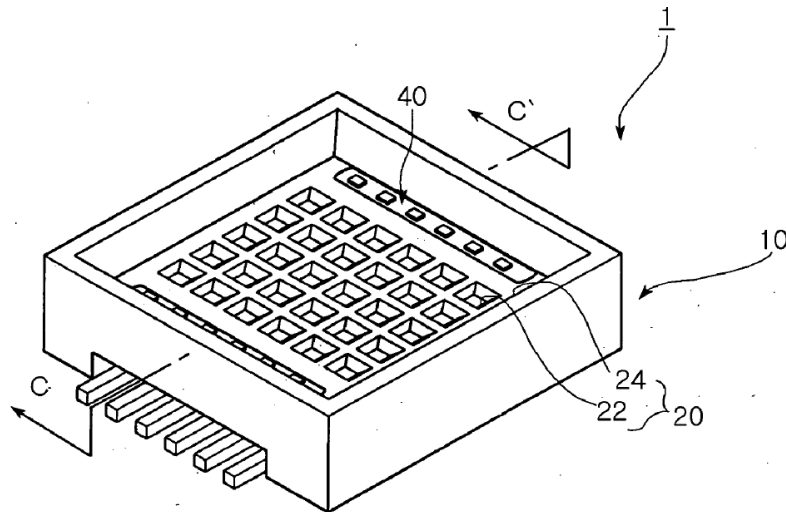


FIG. 5

Ex. 1006, FIG. 5.

279. When a “typical[]” 5 mm package is used as described in Baek (which a POSA would also have thought to apply to the lead frame substrates in Figures 5-7 when constructing an LED package using that embodiment), it would, depending on application requirements well known in the art, result in a spacing of greater than 0.5 mm for the LED chips as illustrated in Figure 5. This would also be consistent with the concept disclosed in Baek that the subwells are designed and spaced so that they prevent light interference from adjacent LEDs.

280. A POSA would have understood that it was well known to vary the LED chip spacing, depending on application requirements and package design, and which spacing would result in the LEDs having increased light efficiency within

the package and for avoiding light interference from adjacent chips. For example: (i) Cao753 teaches to adjust LED spacing from “zero to more than 1 mm, depending on the application requirements” Ex. 1005 at [0023]; (ii) Cao975 also teaches to adjust LED spacing from “zero to more than 1 mm, depending on the application requirements” Ex. 1014 at [0016]; and (iii) Baek also describes the LED placement in the wells. Ex. 1006 at [0063], [0068], [0082], [0089]. This knowledge would confirm to a POSA that Baek’s spacing met the claimed approximately 0.5 mm or greater (or at least it would have been a routine optimization when designing packages to meet application requirements). This is also consistent with the ’988 Patent’s disclosure that does not explain or place any significance on the effects of the particular 0.5 mm spacing. And, it would have been a simple adjustment in size to space the LED chips as appropriate within the package such that the light output would be optimized and as well as thermal and electrical conditions met.

7. Claim 6

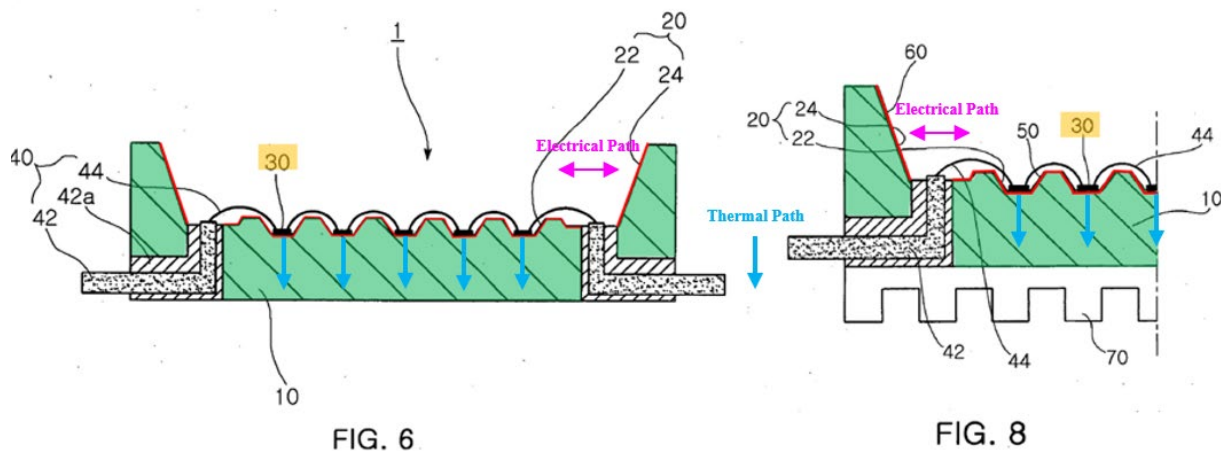
“The apparatus of claim 1, wherein the plurality of LED chips provide separate thermal and electrical paths.”

281. Baek discloses the claimed “*the plurality of LED chips provide separate thermal and electrical paths*”, for the reasons I explained above regarding limitation 1[b] (regarding the downward thermal path in Figures 6-8) and limitation 1[d] (regarding the separate electrical path in Figures 6-8 from chip to chip). I summarize this further in the following paragraphs. Baek alone or with Cao630 also

discloses or renders obvious claim 1, from which claim 6 depends, as I explained above.

282. As I explained in limitation 1[b], Baek discloses a thermal path from the LED chips 30 vertically down through the base member 10 of the metal substrate. As I explained in limitation 1[d], Baek discloses a separate horizontal electrical path from the chip to chip wiring in series. The design in Figures 6-8 results in the LED packages having separate thermal and electrical paths, which I note is consistent with the '988 Patent's disclosure (such as regarding Figure 3, as I explained in Section VII).

283. Figures 6 and 8 of Baek, below, show the **thermal path** and the separate **electrical path**.



Ex. 1006, FIGs. 6, 8 (coloring and arrows and words “Electrical Path” and “Thermal Path” added to figures).

8. Claim 7

“The apparatus of claim 1 wherein the plurality of LED chips have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface.”

284. Baek discloses or it would have been obvious to include as part of Baek- alone or in view of Cao630 - that its LED chips 30 *“have a first surface that is mounted to the reflective surface, and electrical contacts that are provided on one or more surfaces that are not the first surface”*, as required by claim 7. Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 7 depends, as I explained above.

285. I again note that claim 7 claims conventional wire bonded LED chips (with two wire bonds) which have top contacts for connecting to wires (resulting in supplying power to the LEDs when power is applied) and an opposite bottom surface that is mounted into a package (such as onto a substrate). Ex. 1005 at [0028]-[0029], [0032]; Ex. 1013 at 95-96, FIG. 5.2.3(a); Ex. 1011 at 10:61-11:24, 12:61-13:30, FIGs. 17a, 18a, 24a, 25a. I have explained this in Section IX.A.1.

286. I also again note that the '988 Patent admits in its “Background” section that LEDs have p and n contacts for applying power to the LED through wire bonds:

A light emitting diode (LED) is a semiconductor material impregnated, or doped, with impurities. These impurities add

Nichia Exhibit 1003

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“electrons” and “holes” to the semiconductor, which can move in the material relatively freely. Depending on the kind of impurity, a doped region of the semiconductor can have predominantly electrons or holes, and is referred to as an n-type or p-type semiconductor region, respectively. In LED applications, the semiconductor includes an n-type semiconductor region and a p-type semiconductor region. A reverse electric field is created at the junction between the two regions, which cause the electrons and holes to move away from the junction to form an active region. When a forward voltage sufficient to overcome the reverse electric field is applied across the p-n junction, electrons and holes are forced into the active region and combine. When electrons combine with holes, they fall to lower energy levels and release energy in the form of light.

During operation, a forward voltage is applied across the p-n junction through a pair of electrodes. The electrodes are formed on the semiconductor material with a p-electrode formed on the p-type semiconductor region and an n-electrode formed on the n-type semiconductor region. **Each electrode includes a wire bond pad that allows an external voltage to be applied to the LED.**

Ex. 1001 at 1:9-32 (emphases added).

287. Baek’s wire-bonded LED chips 30 are consistent with conventional wire-bonded chips. Ex. 1006 at [0005]-[0011], [0023], [0077], FIGs. 6-8.

288. For example, Figure 6 of Baek shows an LED chip’s **bottom surface** mounted to the heat sink’s **reflective surface** and the chip’s **top surface(s)** that includes electrical contacts (coloring added to indicate the LED chip’s top and bottom surfaces). I note that the same result occurs, if Cao630’s mounting techniques are implemented, as I discussed in limitation 1[b]. As the chips are small

and somewhat difficult to see in Figure 6, I have also added a magnified view of an LED chip 30 to the Figure 6, below. This magnified view is the same for the other LED chips 30.

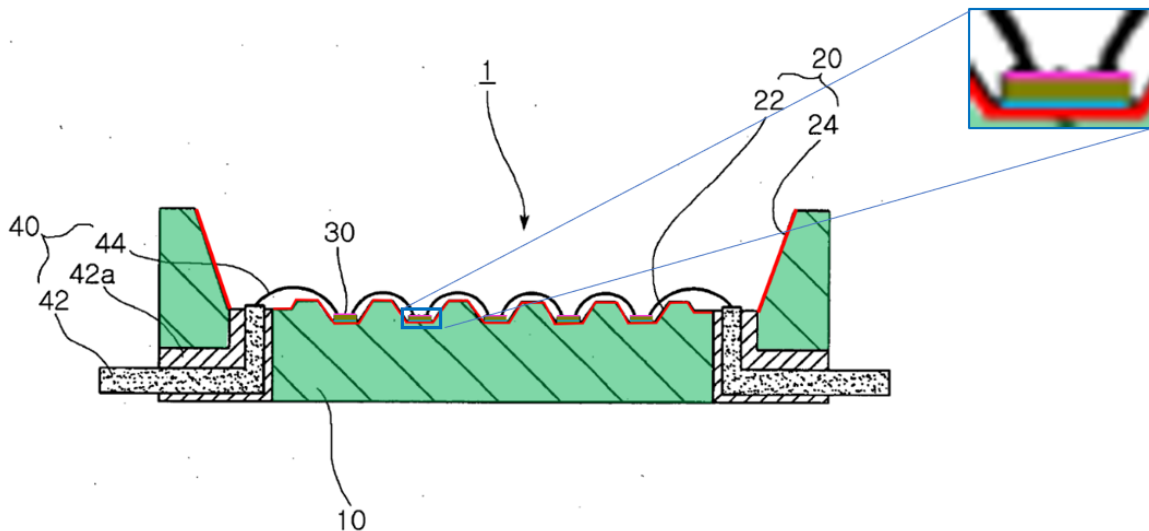


FIG. 6

Ex. 1006, FIG. 6 (coloring and magnified view added to figure).

9. Claim 8

“The apparatus of claim 1, wherein the metal substrate is mounted directly to a heat sink.”

289. Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - that “*the metal substrate is mounted directly to a heat sink*”, as required by claim 8, such as the “heat sink plate” mounted to the base member that may further enhance heat dissipation of the package. Ex. 1006 at

[0044], [0086]-[0087], claim 11 of Baek. Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 8 depends, as I explained above.

290. Regarding the heat sink plate, Baek explains:

- “the high power LED package may further comprise a **heat sink plate** underlying the base member.” Ex. 1006 at [0044] (emphasis added).
- “a **heat radiating plate 70** may be further applied to the underside of the base member 10. This may further enhance heat dissipating characteristics of the high power LED package 1 of the invention.” Ex. 1006 at [0086]-[0087] (emphases added).¹⁰
- “11. The high power light emitting diode package according to claim 1, further comprising a **heat sink plate** underlying the base member.” Ex. 1006 at claim 11 of Baek (emphasis added).

291. The **heat radiating plate 70** is depicted in Figure 8, below, mounted to **base member 10** (of the claimed “*metal substrate*”).

¹⁰ I again note that paragraph [0086] refers to Figure 9, but a POSA would have understood that this disclosure applies to the same numbered element in Figure 8, which is generally true of Baek’s element numbering across figures and embodiments.

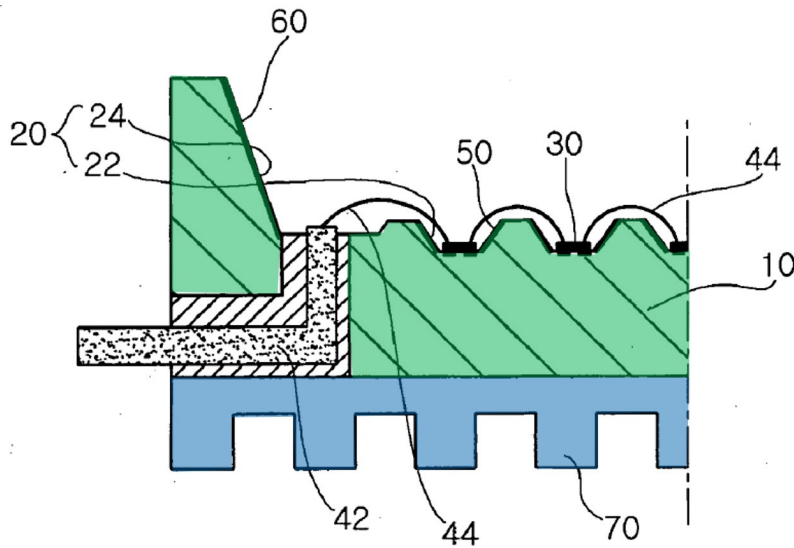


FIG. 8

Ex. 1006, FIG. 8 (coloring added to figure).

292. Baek does not explicitly state how the metal substrate is mounted to the heat sink. However, I note that Baek does not depict any intervening materials between the substrate and heat sink, which indicates to a POSA there are no such materials. A POSA would also have understood that there are many ways of mounting a metal substrate to a heat sink, including using a heat conductive adhesive or through other mounting means (as explained in Cao630) that would be consistent with the heat-dissipation goals of Baek and Cao630 (without any insulating material and even without any adhesive at all) that enable the heat to efficiently be dissipated out of the package. Ex. 1007 at [0015], [0012], claims 1, 12 of Cao630; Ex. 1005 at [0024], [0028], [0034], claims 1, 12, 22 of Cao753.

293. Accordingly, a POSA would have understood that Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 - directly mounting the base member to a heat sink, regardless of whether direct mounting (i) allows for an adhesive (such as heat conductive adhesive without additional intervening insulating material) or (ii) does not allow for any adhesive or intervening material.

294. I once again also note, consistent with the knowledge of a POSA (as evidenced by the prior art I discuss herein), that the '988 Patent does not explain how to mount its metal substrate directly to its heat sink (only that it is “mounted directly”). Ex. 1001 at 5:46-62, 6:23-26.

10. Claim 9

“The apparatus of claim 1, wherein the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface.”

295. Baek discloses, or it would have been obvious to include as part of Baek - alone or in view of Cao630 “*the electrical path formed by connecting the LED chips in a chip to chip fashion does not include an electrical connection between the LED chips and the reflective surface*”, as required by claim 9. Baek alone or with Cao630 also discloses or renders obvious claim 1, from which claim 9 depends, as I explained above.

296. As I explained for limitation 1[b], Baek depicts and describes relative to Figures 6-8 that an electrical connection is formed by connecting the LED chips 30 directly to one another by wiring them in series.

297. As shown in Figures 6-8 and also discussed regarding limitation 1[b], the LED chips 30 are wired together - without an electrical connection between the LED chips and the reflective surface (if there were, it would result in a short circuit).

X. CONCLUDING STATEMENTS

298. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

299. I declare that all statements made herein of my knowledge are true and correct. I also declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 35 U.S.C. § 1001.

300. I declare under the penalty of perjury that the foregoing is true and correct.

Executed on March 14, 2024

A handwritten signature in black ink, reading "Nan Marie Jokerst". The signature is written in a cursive style with a large, stylized initial "N".

Nan Marie Jokerst, PhD