



**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

BX LED LLC,

Plaintiff,

v.

WALMART INC.,

Defendant.

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Case No. 6:22-cv-00445-ADA-DTG

JURY DEMANDED

EXPERT DECLARATION OF

John K. Roberts

REGARDING CLAIM CONSTRUCTION

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This declaration is submitted pursuant to Rule 26(a)(2) of the Federal Rules of Civil Procedure.

I. INTRODUCTION

1. My name is John K. Roberts, and I have been retained as an independent technical expert to provide opinions concerning certain claim construction disputes in this litigation.

2. The opinions set forth in this declaration are based on scientific, mathematical, and logical principles, my education, 4.5 decades of experience inventing, patenting and commercializing new products for high-rate production including 3 decades in the LED, LED Lighting and related industries, and finally my analysis of the materials and information referenced below in this declaration.

3. I am being compensated at a rate of \$300.00 per hour for time spent plus reimbursement of reasonable expenses incurred during work on this matter. My compensation is not contingent on the outcome of this litigation, nor do I have any personal interest in the outcome of this case.

II. BACKGROUND AND QUALIFICATIONS

4. In this section I have summarized my educational background, career history, and other relevant qualifications. A detailed description of my professional qualifications is outlined in my resume, a copy of which is attached to this declaration.

5. I have nearly fifty (50) years of post-undergraduate professional work experience, starting with the United States Marine Corps (USMC) in 1983 and then including nearly 45 years in industry inventing, patenting and commercializing new products for high-rate production with companies I helped start or grow to success. This includes 3 decades of commercial experience advancing the state of the art in LED chips, LED components, LED lighting systems and LED

based display systems primarily within the semiconductor, automotive, lighting, and flat panel display industries.

6. In May of 1983, I earned a Bachelor of Science degree in Earth and Planetary Sciences from the Massachusetts Institute of Technology (MIT) in Cambridge, Massachusetts. I was simultaneously commissioned as a 2nd Lt with a regular commission in the USMC and commenced active-duty service.

7. In December of 1983, I completed USMC training for commissioned officers at The Basic School (TBS) in Quantico, Virginia. In early 1985 I completed training to become a Naval Aviator at NAS Pensacola and NAS Whiting Field in Florida, was issued my wings and transitioned to fly the UH-1N Iroquois ("Huey") aircraft with the Fleet Marine Force in the 1st Marine Air Wing, MAG 39, at Camp Pendleton, CA. While on active duty with the USMC, I specialized in advanced tactical flying techniques, deployed extensively across the Western USA and Western Pacific, and accumulated approximately 1800 flight hours, mostly in high performance conditions (low altitude, night, shipboard, at sea or all the above). I left active duty with the USMC in 1989 to form a startup company in the automotive industry based on a then patent-pending display technology I had invented and begun commercializing.

8. Since 1989 I have held technical positions in several companies ranging from individual contributor to leadership positions such as Director of Technology, VP of Technology, VP of Engineering, Chief Engineer, Engineering Fellow, and Chief Technology Officer. I remain actively employed full time, presently as Principal Engineering Fellow with a large contractor in the Defense industry working to develop and deploy next generation sensor systems for defense of the United States and allies.

9. I have been inventor or co-inventor on 154 US patents issued over 4.5 decades

assigned to several technically and commercially disruptive companies and resulting in billions of dollars in revenue. These companies became leaders in industries such as the LED and LED Lighting industries by commercializing, producing in high volume and selling products based on these inventions. Innovations protected by these patents include:

- a. Some of the earliest high-intensity LED based automotive turn and brake signal systems used in the OEM automotive industry in the early 1990's;
- b. Some of the earliest white light emitting LED components, high power LED components and LED based illumination systems used in the automotive industry in the late 1990's and early 2000's;
- c. The 1st comprehensive line of AlInGaN based power LED chips and components available in many colors, including lighting class white light emitting power LEDs for the lighting industry starting in the late 2000's; and
- d. Numerous additional patented developments widely used within the LED backlighting and LED lighting industries since the early 2010's.

III. MATERIALS CONSIDERED

10. In forming the opinions set forth in this declaration, I have considered and analyzed the following material:

- a. U.S. Patent No. 6,869,812 ("the '812 Patent");
- b. The prosecution history of the '812 Patent;
- c. References cited in the '812 Patent;
- d. U.S. Patent No. 7,901,109 ("the '109 Patent");
- e. The prosecution history of the '109 Patent;
- f. References cited in the '109 Patent;
- g. U.S. Patent No. 7,973,465 ("the '465 Patent");
- h. The prosecution history of the '465 Patent;
- i. References cited in the '465 Patent;
- j. U.S. Patent No. 8,203,260 ("the '260 Patent");
- k. The prosecution history of the '260 Patent;
- l. References cited in the '260 Patent;
- m. U.S. Patent No. 8,567,988 ("the '988 Patent");
- n. The prosecution history of the '988 Patent;
- o. References cited in the '988 Patent;
- p. U.S. Patent No. 8,998,433 ("the '433 Patent");
- q. The prosecution history of the '433 Patent;

- r. References cited in the '433 Patent;
- s. U.S. Patent No. 10,966,300 ("the '300 Patent");
- t. The prosecution history of the '300 Patent;
- u. References cited in the '300 Patent;
- v. Plaintiff's Complaint for Patent Infringement;
- w. Defendant's Opening Claim Construction Brief and Exhibits, including the Declaration of Dr. Gary Eden; and
- x. Extrinsic Evidence cited in this declaration¹.

IV. APPLICABLE LEGAL STANDARDS

11. I am not an attorney, but I have been informed of the following legal standards and principles, which I have used and applied in forming the opinions set forth herein.

A. Claim Construction

12. I understand that deciding if a claim has been infringed directly is a two-step process. Claim construction is the first step in any infringement or validity analysis. Claims are construed in light of their explicit language as informed by their preambles, as well as the patent's specification, figures, and prosecution history.

13. I understand that the specification is the best source for understanding a technical term, to be supplemented, as needed, by the prosecution history. The prosecution history represents key evidence of how the examiner and the inventor construed the patent. I understand that claims should generally be interpreted in a manner consistent with other claims, as well as with the prosecution history. Claim terms in patents sharing a common specification and application should usually be given the same interpretation. I understand that it is not proper to confine a claim to a particular embodiment; the claim language itself is paramount.

14. I understand that extrinsic evidence may also be relevant to claim construction. Such evidence consists of all evidence extrinsic to the patent and its prosecution history, including

¹ Although listed here, the materials footnoted in this declaration were not used to form the basis for my opinions. Rather, they are intended to further demonstrate certain principles I discuss throughout this declaration.

expert and inventor testimony, dictionaries, and learned treatises. I understand that while extrinsic evidence can shed useful light on the relevant art, it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

15. I understand that the prosecution history of a patent can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention during prosecution, making the claim scope narrower than it would be otherwise. I understand that when the patentee unequivocally and unambiguously disavows a certain meaning to obtain a patent, the doctrine of prosecution history disclaimer narrows the meaning of the claim consistent with the scope of the claim surrendered.

16. I understand that a claim is invalid for indefiniteness only when its language, read in light of the specification and the prosecution history fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention. The definiteness requirement mandates clarity while recognizing that absolute precision is unattainable. I understand that reasonable certainty does not require absolute or mathematical precision. I further understand that general principles of claim construction apply to determining whether a claim is indefinite.

V. LEVEL OF ORDINARY SKILL IN THE ART

17. I have been informed, and I understand, that the disclosure of a patent is to be viewed from the perspective of a person having ordinary skill in the art at the time of the alleged invention i.e., a “POSITA”.

18. I have been informed, and I understand, that the prior art references can provide evidence of the level of ordinary skill in the art, and the factors that may be considered in determining this level of skill can include the educational level of the inventors, the types of problems encountered in the art, prior art solutions to those problems, the rapidity with which

innovations are made, the sophistication of the technology, and the educational level of others active in the field.

19. I understand that a POSITA is also expected to be a person of ordinary creativity, not an automaton, and further would have the capability of understanding the scientific and engineering principles applicable to the pertinent art.

20. I understand that the relevant time for the Asserted Patents ranges from May 13, 2003 to October 13, 2011.

21. It is my opinion that a POSITA during the relevant period would have possessed at least:

- a. A bachelor's degree or equivalent in a relevant scientific, engineering or mathematical field (e.g. applied physics, physical chemistry, materials science, engineering, applied mathematics, manufacturing engineering or other interdisciplinary science or engineering degree);
- b. Three or more years of technical experience in the semiconductor field;
- c. At least one year of technical experience designing, commercializing, and manufacturing Light Emitting Diode (LED) chips or alternately LED discrete components, modules or assemblies directly incorporating LED chips;
- d. A working knowledge of basic electronic, optical, and thermal principals; and
- e. A working knowledge of measurement, process control and dimensional tolerancing principles fundamental to LED production and application.

Under this standard, I am at least a POSITA and was one on the earliest date to which the Asserted Patents claim priority.

22. My education and experience qualify me as at least a POSITA and give me expertise in the fields of LED chips, LED components, LED modules and LED lighting systems including the technologies described and claimed in the Asserted Patents. My close association

unconventional, confusing, and ambiguous.

X. THE '988 PATENT

A. Background of the '988 Patent

66. I have been asked to consider the construction of certain terms in Claim 1 of the '988 Patent, entitled "Efficient LED Array," which generally relates "to light emitting diodes, and more particularly, to an efficient LED array."

67. Asserted Claim 1 is reproduced here:

Claim 1: A light emitting diode (LED) apparatus comprising: a metal substrate having a reflective surface; and a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path and at least a portion of the LED chips being spaced apart from each other to expose regions of the reflective surface between the portion of the LED chips, the exposed regions reflecting light emitted from the portion of the LED chips, and an electrical path formed by connecting the LED chips in a chip to chip fashion.

B. Construction of "efficient thermal path"

68. The phrase "efficient thermal path" is found in an independent Claim 1 and for the reasons discussed below, it is my opinion that in the context of the patent and the art, this is a clear and unambiguous term to POSITA.

69. A POSITA will know that most heat dissipation in high power LED or other electronic components occurs by the physical process of thermal conduction whereby heat flow out of the device keeps the device cool and is aided by low thermal resistance or conversely impeded by high thermal resistance. A POSITA would further understand that an efficient thermal path across an interface between elements in an assembly is a heat path exhibiting low thermal resistance via which heat may be dissipated with high heat flow and minimal temperature gradient. A POSITA will further know that the thermal resistance across an interface between elements in an assembly is determined by the thermal conductivity of any intervening material layer and the

length, width and thickness of the separating material. The first order approximation of this relationship well known to a POSITA is available from the equation:

$$\text{Thermal Resistance } R = T / (L \times W \times K) = T / (A \times K)$$

Where R is the thermal resistance, L and W are the cross-sectional length and width of the interface between the elements, A is the cross sectional area of the interface between the elements, and T and K are the thickness and thermal conductivity of the intervening medium if any.³ These simple thermal relationships derive directly from Newton's Law of Cooling and have been known and used in power electronics such as transistor chip, component, module, and system design for decades (long before high power LEDs were invented). As will be apparent to a POSITA or virtually anyone with basic math skills observing the simple equation for thermal resistance, keeping the Thermal Resistance low requires making A high, and/or K high and/or T low. For the best high-power LED devices, all 3 would be substantially true and none would be substantially false.

70. To a POSITA, an "efficient thermal path" is thus understood to be one with low thermal resistance that does not incorporate thermally-insulating, low thermal conductivity materials (low K), or thick (high T) intervening layers between elements producing heat by electric power consumption (e.g. the LED chip) and the structures supporting them that must draw the heat away. A POSITA knows that, as is evident from the equation above, mounting a high-power LED chip to a substrate using a thick (high T) layer of general-purpose (low K) silicone, epoxy or other formulation would be inefficient, whereas mounting it with a thin (low T) layer of a formulation of filled silicone or epoxy having high thermal conductivity (high K), or employing solder or another metallic bond (high K) would be efficient. A POSITA will also know that mounting a

³ Ex. U, <https://www.thermal-engineering.org/what-is-thermal-resistance-thermal-resistivity-definition/>

high-power LED chip to a general-purpose ceramic or polymeric substrate having poor thermal conductivity (low K) will lead to an inefficient thermal path yet mounting it to a high thermal conductivity (high K) metal substrate with a thick cross section (high A) will lead to an efficient thermal path.

71. This understanding is supported by the six references in the specification to an “efficient thermal path”. *See* ‘988 Patent at 1:44-46; 4:47-53; 4:54-59; 5:10-12; and 5:55-56. Each instance refers to substrate materials with low thermal conductivity (such as ceramic) as creating an “inefficient” thermal path, while describing that substances with high thermal conductivity (such as metal) create “efficient” thermal paths. *See id.* at 1:44-46; 4:47-53. The references further reinforce the natural understanding of the term by describing that removing “insulating dielectric[s]” creates an efficient thermal path. *See id.* at 4:54-59.

72. This is further reinforced because the inventor of the ‘988 Patent has included limitations within Claim 1 that unambiguously create an efficient thermal path on the basis of well-known principles reviewed above, e.g., “metal substrate”, “a plurality of LED chips mounted directly to the reflective surface of the metal substrate creating an efficient thermal path”. If a thick or poorly conductive material was inserted between the LED chips and the substrate then the LED chips would not be “mounted directly to the reflective surface of the metal substrate creating an efficient thermal path”. This would also be clear to a POSITA and measurable because the LED chip itself would heat up unacceptably in such a configuration (a problem the invention solves and the specification and claims teach away from).

73. For these reasons the meaning of the claim as written is plain, unambiguous and definite to a POSITA.

C. Construction of “an electrical path formed by connecting the LED chips in a chip-to-chip fashion”

74. The phrase “an electrical path formed by connecting the LED chips in a chip to chip fashion” appears in independent claim 1. It is my opinion that this language is clear, unambiguous and definite to a POSITA in the context of the ‘988 Patent and field of art. An electrical path would be universally understood to a POSITA as one that conducts electricity. A POSITA would further be familiar with a means for forming such a path such as via a connection using a metallic material having low electrical resistivity. Similarly, there is no ambiguity or lack of clarity in a literal reading of the phrase “chip to chip fashion” in the context of this claim, the ‘988 patent and field of art. Since the claim is about an electrical path, “chip to chip” would simply indicate electrical directness, in other words an absence of intervening elements having a significant impact on electrical conduction. Most simply, “an electrical path formed by connecting the LED chips in a chip to chip fashion” means a low resistance electrical path between the LED chips.

75. One embodiment disclosed by the ‘988 Patent, for example, employs wirebonds stretched directly between topside contacts of adjacent LED chips. Dr. Eden concludes that the prosecution history restricts the scope of independent claim 1 to cover *only* this embodiment by altering the interpretation to mean “electrically connecting one LED chip directly to another LED chip” and by arguing this is the only interpretation that overcomes prior art by Yamada that was cited by the patent examiner in the prosecution history.

76. The Patentee responds to the patent examiner by identifying that the disclosure discussed in reference to Figure 2 and 3 of the ‘988 Patent describes an embodiment of the claimed invention that uses wirebonds formed between the top sides of LED chips in addition to electrically conductive traces on an insulating substrate the LEDs rest upon where both wirebonds and intervening conductive traces on the substrate are needed to connect LED chip to LED chip. Dr.

Eden asserts that the '988 inventor disavowed a disclosed embodiment to overcome examiner rejections over Yamada. I disagree.

77. The patentee first distinguished Yamada in two ways. First, in that “Yamada discloses that each LED chip is connected to the metal substrate [] through wires”. Ex. J, Response to Office Action (May 28, 2013) at 4. And second, in that Yamada “[taught] that the LED chips 2 are die-bonded to the metal substrate [] and mounted by wire bonding the metal wires [.]” Ex. J, Response to Office Action (May 28, 2013) at 4. Either or both of these distinctions were sufficient to distinguish Yamada as not teaching or anticipating connection in a chip to chip fashion. For example, a chip to chip connection that did not use wire bonds to the substrate would still conform with the distinctions cited by the patentee. And in either case, the patentee specifies that Fig. 3 was only an “example” of a chip to chip fashion configuration. Ex. J, Response to Office Action (May 28, 2013) at 5.

78. I further disagree with Dr. Eden’s proposed construction of “electrically connecting one LED directly to another LED” as arbitrarily and unnecessarily narrow, precluding embodiments outside the scope of Yamada yet supported by the present specification and within the scope of the current plain language of independent claim 1.

79. For example, as one possible configuration encompassed by “chip to chip fashion”, a POSITA will recognize that one or more passive interconnect chips may be mounted on the same metallic substrate as the LED chips and interspersed among them to serve as jumpers to support flexibility in wiring the LED chips in various series and parallel combinations. These passive interconnect chips may be constructed in a fashion familiar to a POSITA using materials such as silicon, sapphire, silicon carbide, ceramic or other electrically insulating substrate materials and configured with low resistance conductive traces and wire-bondable metallic pads on top.

Adjacent LEDs may then be wirebonded to one or more pads on top of one of more of these passive chips, and then further connected in a series or parallel fashion to another topside LED contact. This is just one example of a chip to chip configuration that would provide additional flexibility when connecting LEDs that have only 2 top side contacts. Such passive chips serving as low resistance jumper stations allow configuring a given device with multiple LED chips for various series/parallel chip configurations suited for different power supplies and applications. As would be understood by a POSITA, such an arrangement is not taught or anticipated by Yamada, would be considered a chip-to-chip connection, and offer the advantages supported by the '988 specification and within the scope of '988 independent claim 1 as written.

XI. THE '433 PATENT

A. Background of the '433 Patent

80. I have been asked to consider the construction of certain terms in the '433 Patent entitled "Light Emitting Device Utilizing Remote Wavelength Conversion With Improved Color Characteristics" and which describes a light emitting device that utilizes remote wavelength conversion with improved color characteristics.

81. Asserted Claims 1 and 2 are shown here:

Claim 1: A light emitting device configured to emit light of a selected color having a selected peak wavelength, comprising: a radiation source operable to generate and radiate excitation energy, the source being configured to irradiate a wavelength conversion component with excitation energy; the wavelength conversion component comprising: a layer comprising a photoluminescent material which, when irradiated by the radiation source, emits light of a first wavelength range having a single peak wavelength corresponding to the selected peak wavelength; and a color enhancement filter layer to filter wavelengths of light outside of a second wavelength range, wherein the second wavelength range is narrower than the first wavelength range and centered on the selected peak wavelength.

*"Power rail can be defined as the voltage source within the device from which its various functions can draw power."*⁷

*"A power rail is all or part of a plane layer that is used for some voltage. In virtually all printed circuit boards, some signals, often half of them, have to be routed over the power layers."*⁸

*"A computer's power supply converts AC power into several DC voltages (typically plus and minus 3.3v, 5v and 12v), each of which is known as a rail. The term comes from the power lines on motherboards. Power must be available throughout a motherboard; hence, voltage lines tend to run in long strips like railroad tracks."*⁹

*"At the top of the standard cell, there is VDD rail and bottom there is a VSS rail. Both the Power rails are drawn in the Metal-1 layer. In between the VDD rail and VSS rail there are three main regions, a nwell region, a gap of nwell and pwell and pwell region. nwell region is near to the VDD rail and pwell region is near the VSS rail. pMOS transistors are build inside the nwell, so all the pMOS transistors are in the top half of the cell and similarly, all nMOS are in the bottom half of the standard cell."*¹⁰

99. Given that "power rails" is a term so well recognized in electronics and the present art and, given that the Inventors' use of the term within the specification, figures and subject claims is consistent and compatible with the common meaning to POSITAs, it requires no further interpretation in my opinion.

100. I reserve the right to modify and supplement my opinions in the future to respond to new arguments raised and to take into account new information as it becomes available to me.

101. I hereby declare all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

Dated: February 17, 2023

John K. Roberts

2/17/2023



⁷ Ex. T, <https://www.sciencedirect.com/topics/engineering/power-rail>

⁸ Ex. P, <https://resources.altium.com/p/why-power-rails-need-be-low-impedance>

⁹ Ex. Q, <https://www.pcmag.com/encyclopedia/term/rail#:~:text=A%20computer%27s%20power%20supply%20converts%20AC%20power%20into.to%20run%20in%20long%20strips%20like%20railroad%20tracks>

¹⁰ Ex. R, <https://teamvlsi.com/2020/05/standard-cells-in-asic-design-standard-cells-in-vlsi.html>