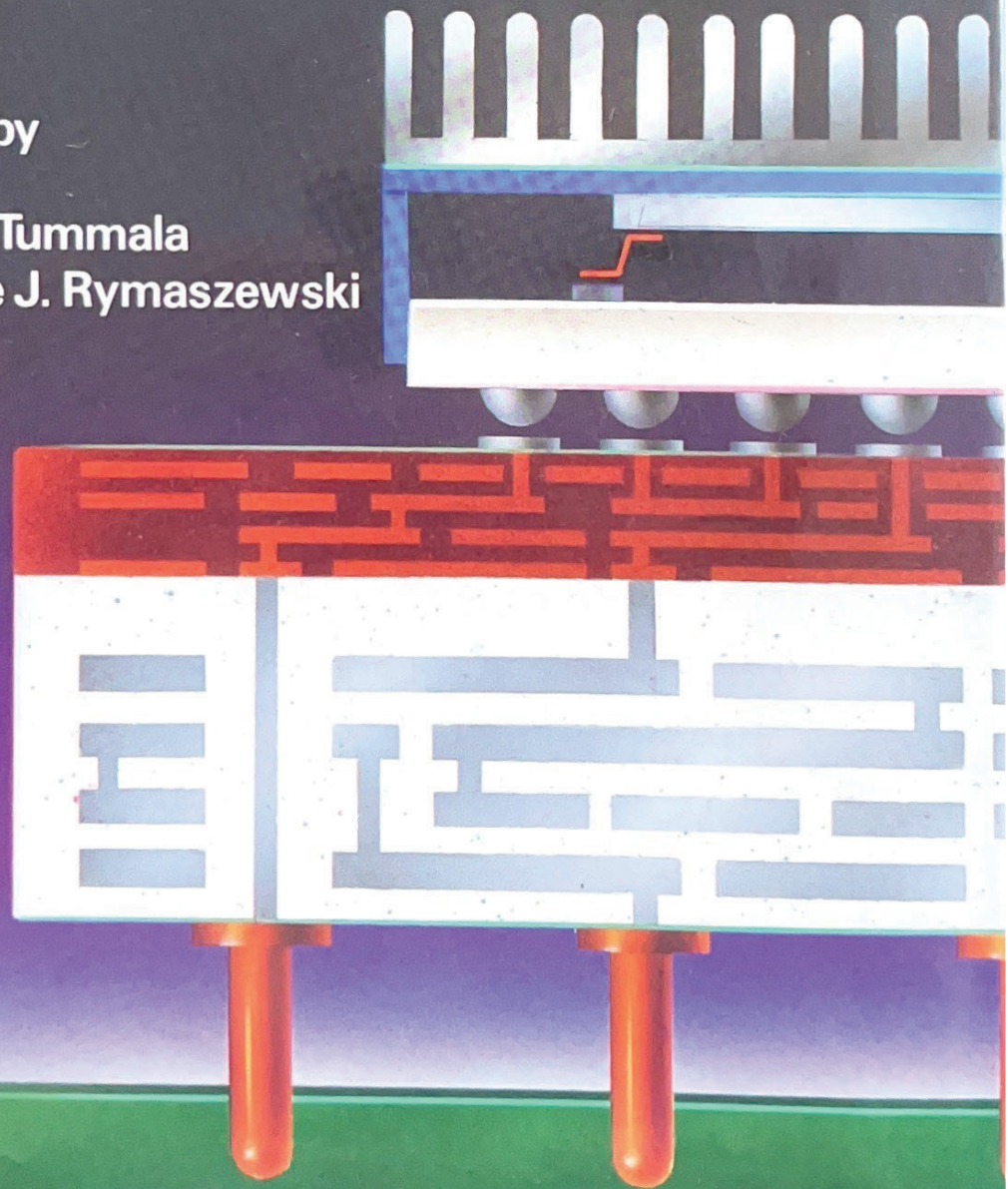


Microelectronics Packaging Handbook

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CERAMIC PACKAGING

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7.1 INTRODUCTION

Ceramics and glasses, defined as inorganic and nonmetallic materials, have been an integral part of the information-processing industry. Glasses and ceramics are used for data processing by the use of semiconductor devices interconnected onto packages. They are also used for storing information by the use of such magnetic materials as iron and chromium oxides and ferrites; for displaying information by the use of low-temperature solder glasses sealed to transparent faceplate glasses; for printing information by the use of ceramic-metal print heads and corrosion-resistant glasses; and for transferring information by the use of very low-loss glass fibers. The materials currently used for these applications are shown in Table 7-1.

Integrated circuit packaging is one of the most important applications of ceramics in microelectronics. Ceramic materials in the form of dual-in-line

Table 7-1. Application of Ceramics in Microelectronics.

<u>Information Processing Function</u>	<u>Application</u>	<u>Ceramic Materials</u>
Information Processing		
• Package	Substrate	Al_2O_3, BeO, SiC, AlN
• Device	Dielectric	Si_3N_4, SiO_2
	Mask	Borosilicate Glasses
Information Storage		
	Disk	Iron Oxide, Ferrite
	Tape	Chrome Oxide
	Head	Ferrites, Glass
		$Al_2O_3 + TiC$ Substrate
Information Display		
	Dielectric	Lead Borosilicates
	Seals	Lead Zinc Borosilicates
	Face Plate	Soda-lime Glass
Information Printing		
	Ink Jet	ZrO_2 -Containing Glass
	Electro-erosion	Ceramic-metal Composites
Information Transfer		
	Optical Fiber	$SiO_2, B_2O_3-SiO_2$

packages, chip carriers, and pin-grid arrays are used throughout the industry, from consumer electronics to mainframe computers. While plastic packages outnumber ceramic packages, ceramic packages constitute roughly two thirds of the total packaging market, which is currently considered a multibillion dollar industry worldwide. The Japanese market illustrated in Figure 7-1 is considered roughly a third of the total market, since it does not include the ceramic substrates manufactured by United States and European computer and ceramic manufacturers. The ceramic package market in the U.S. along with a list of ceramic package suppliers to this market and their market share are shown in Table 7-2 and Table 7-3 respectively [1]. It should be noted, again, that these numbers do not include those markets for internal consumption of individual companies, such as IBM, which manufactures ceramics for its own high-performance applications. Ceramics for these applications possess a combination of electrical, thermal, mechanical, and dimensional properties unmatched by any other group of materials. For example, ceramics have dielectric constants from 4 to 10,000, thermal-expansion coefficients matching silicon ($30 \times 10^{-7}/^{\circ}C$) or copper ($170 \times 10^{-7}/^{\circ}C$), and

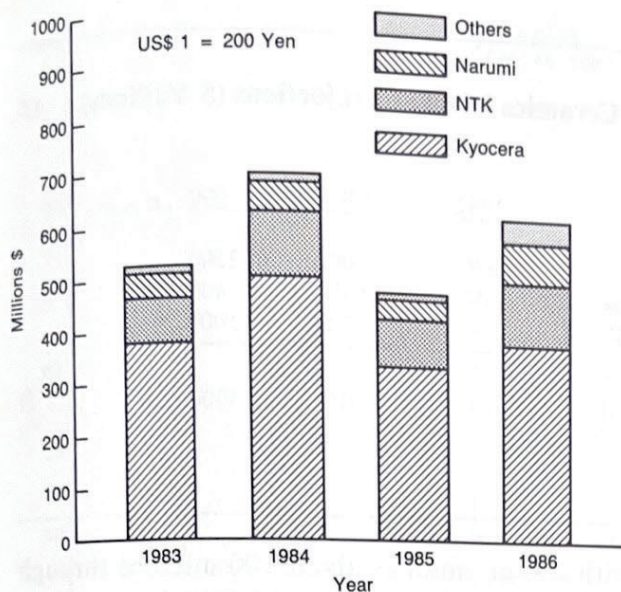


Figure 7-1. Japanese Ceramic Companies Shipments.

thermal conductivities from one of the best insulators to better than aluminum metal ($220 \text{ W/m}\cdot\text{K}$), which is one of the best thermal conductors known. Dimensional stability as measured by shrinkage control has been achieved at better than $\pm 0.1\%$ of nominal shrinkage, allowing as many as 30 to 50 layers

Table 7-2. Package Suppliers to U.S. Market. Market shares based on sales volume. After Black, Ref. [1], 1986.

	Percent
Kyocera	55-70
NTK	15-25
Narumi	5-10
GE	4
American Hoescht (Metceram)	2
Cabot	2
Raychem/Interamics	1
General Ceramics	1
Brush Wellman (EPI)	0.5
LDC	0.5
Diacon	0.5
Bourns	0.5
Shinko	0.5
	100

Table 7-3. U.S. Multilayer Ceramics Market Projections (\$ Millions). After Black, Ref. [1], 1986.

	<u>1982</u>	<u>1984</u>	<u>1990</u>
Ceramic packages	430	600	2500
Multilayer capacitors	350	610	1400
All other electronics	—	700	1000
Total	780+	1910	4900

of ceramic to be metallized with vias as small as about 100 microns through all these layers. Recent technology breakthroughs have led to the use of ceramics as superconductors, offering no electrical resistance to the flow of current. Figure 7-2 illustrates the developments in this area over the last eight decades. It should be noted, however, that ceramics have started to play a role in this area only within the last couple of years, starting with the *La-Sr-Cu-O* system. These developments could lead to improved power distribution of future high-performance computer systems. Another desirable property of ceramic substrates is their high-temperature stability. Where hermeticity is required, ceramic packages are often the only choice. On the other hand, ceramic packages suffer from three main drawbacks. They require higher-temperature processing than plastics, making them more expensive. Ceramics are brittle, making them prone to catastrophic failure and sensitive to stress corrosion unless designed carefully for each application for which they are used. In very-high-performance applications requiring very low dielectric constants and very high packaging densities, ceramics cannot compete with thin-film organic packages. However, ceramics are expected to be used as stable building blocks on which high-performance thin-film wiring can be developed with the use of polymeric materials for high-performance applications.

Ceramic packages offered in a variety of forms, such as DIPs, chip carriers, flat packs, and pin-grid arrays are capable of supporting from 1 chip to as many as 100 or more chips per package, as discussed later in this chapter.

In this chapter the **history and evolution** of ceramic packaging are discussed, from simple dual-in-line and solid logic packages to the **state-of-the-art** ceramic processing (as in fabricating multilayer packages capable of interconnecting in excess of 30 ceramic layers with 30 layers of metal to support devices in excess of 100 chips on a single substrate with all the required power distribution and thermal dissipation to and from each of the devices). **Recent**

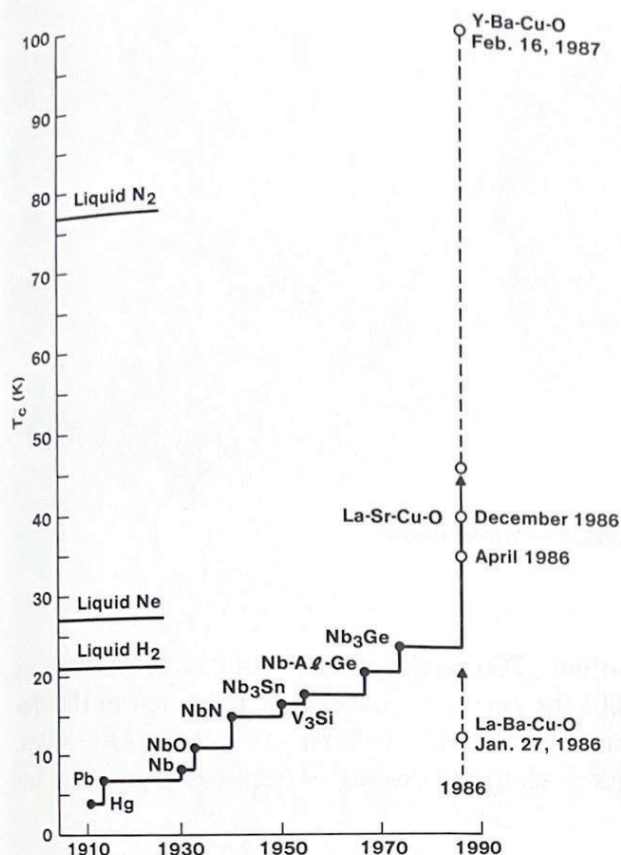


Figure 7-2. Progress and Role of Ceramics in Superconductors. T_c refers to the critical temperature at which superconductivity is observed for the material.

developments in the use of ceramics with thermal-expansion coefficients near that of silicon, such as AlN , SiC , glass $\pm$ ceramics²¹, are also included. Future technology trends and the scientific areas required to develop the understanding necessary to support the new product developments are pointed out.

7.2 EARLY CERAMIC PACKAGING

Early transistors were either solder-bonded to glass-epoxy cards or packaged in simple plastic packages (as shown in Fig. 7-3). The need for hermetic sealing led to the development of the transistor outline (TO) metal packages, which were sealed by welding nickel lids to gold-plated metal bases.

²¹ See section 7.5.4, "Glasses, Glass + Ceramics, and Glass-Ceramics," on page 500 for an explanation of the "glass $\pm$ ceramic" nomenclature.

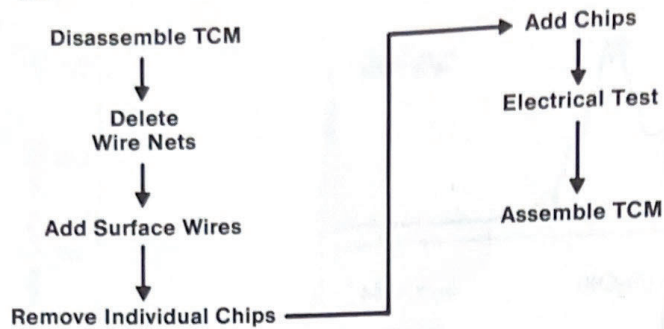


Figure 7-28. Engineering-Change Process Flow.

Rework: Processes have been developed for the replacement of individual chips. Replacement is accomplished by mechanical removal of the chip, thermal rework of the substrate pads, and reflow of the replaced chip either in a furnace or by a localized heat source.

A key feature of the multilayer ceramic design and process is the ability to rework the assembly to make engineering changes (EC). This feature is essential during the design and debug phases of the systems development.

The process flow (Fig. 7-28) utilizes the individual chip-replacement techniques just described. Wire nets internal to the multilayer ceramic substrates are disconnected at the surface. Surface wires are added in the desired pattern, using ultrasonic bonding. The module is tested, reassembled using a C-ring, and filled with helium.

The multilayer ceramic module has been designed to maintain the chip junction temperature below 85°C with a maximum thermal load of 5 W/chip and a total of 500 W/module. The heat sink is a water jacket which mounts to the module cover assembly. The cover assembly contains 5.5-mm-diameter spring-loaded pistons that contact the back side of each chip and form the main thermal path to the water jacket (Fig. 16-9, on page 1093). The TCM assembly is charged with helium to a pressure of 0.16 MPa (1.6 atm) to minimize the thermal resistance at the chip-to-piston and piston-to-housing interfaces. The total thermal resistance from the chip surface to the module housing/water jacket interface is a maximum of 10°C/W . More recent designs accommodate 10-15 W/per chip.

7.5 RECENT DEVELOPMENTS IN CERAMIC PACKAGING

Ceramic packaging is one of the most active areas in all of packaging. Surface-mount technology of both ceramic and plastic packages, which is currently at about the 20% level (of all packages), is expected to increase to 55% in 1990 and 80% by 1995. The trend in the low end is almost entirely to plastic packages except for those applications that require very high reliabil-

Table 7-16. Recent Ceramic-Package Materials Developments.

<u>Package Material</u>	<u>Package Property</u>
Glass $\pm$ Ceramics	• Diel. constant as low as 5 • Thermal expansion coefficients near that of silicon • Co-fired metallization of high-conductive metal such as gold, copper • Low thermal conductivity
Silicon Carbide	• Thermal conductivity better than Aluminum metal • Thermal-expansion coefficient near silicon • Electrical insulation • Potential cofired W metallurgy • Dielectric constant >10
Aluminum Nitride	• Thermal conductivity approaching aluminum • Thermal expansion near silicon • Cofired multilayer metallurgy (W) • Dielectric constant about 9

ity. Flat packs, leadless chip-carriers, and pin-grid arrays are continuing to be developed, and the pin-grid spacing is moving from 2.54-mm to finer than 1.27-mm centers. In high-end packaging, a number of ceramic materials shown in Table 7-16 are being developed very actively so that packages will have improved:

- signal propagation.
- thermal expansion matching to silicon, allowing larger chips with more circuits directly solder-bonded.
- electrical conductors for added power distribution.
- thermal conductors for improved power dissipation.
- and input/output connection to support more circuits.

The recent progress in ceramic substrate materials is discussed in the following sections.

7.5.1 Aluminum Nitride

The worldwide development of aluminum nitride to produce ceramic packages with thermal conductivity far superior to alumina, a dielectric constant no more than alumina, and a thermal-expansion coefficient matching that of silicon has been reported [30, 31, 32]. Package metallization using thick-film

tungsten is being developed to form multilayer substrates similar to alumina multilayer ceramic. Such an AlN substrate is also expected to have superior mechanical strength, surface roughness, and camber over conventional alumina multilayer ceramic.

The high thermal conductivity of carbides and nitrides was demonstrated on single crystals a few decades ago. The development of commercial ceramic substrates, starting with fine-grained powders, to produce fine-grained and nonporous microstructures, has been relatively recent.

It is expected that ceramic materials with the following properties will have high thermal conductivity:

- Low molecular weight.
- Strong interatomic bonding.
- Simple crystal structure.
- Low anharmonicity.

By these criteria, diamond is expected to be the best thermal conductor when compared to carbides and nitrides (see Fig. 7-29). Aluminum nitride compositions have been reported with a number of additives that either improve sinterability or modify microstructure. The best AlN substrate material with the highest thermal conductivity [30] to date (1986) is processed according to the process flow in Figure 7-30, and is compared with other recent ceramic-package developments in Table 7-17 (with alumina multilayer ceramic as reference). Two points worth noting with aluminum nitride: (1) Its thermal conductivity seem to be very much dependant on the amount of oxygen (Fig. 7-31) [33]. Thus high thermal conductivity can only be accomplished with very low oxygen, often achieved with "scavengers" added during the sintering process. (2) Long-term exposure to humidity at elevated temperatures may result in hydroxide formation, possibly resulting in reliability concerns. It should be noted that while thermal conductivity of AlN , SiC , and BeO will provide power dissipations around 15 watts per chip in air-cooling mode, the expected requirements of the 1990s to go beyond this level of power dissipation will require enhanced water-cooling technologies, as discussed in Chapter 6, "Chip-to-Package Interconnections," unless chips are spaced apart.

Metallizations: A number of metallization processes, such as thin-film deposition by evaporation or sputtering, electroless plating, as well as thick-film by postfired and cofired thick-film metallization, as shown in Table 7-18, are being developed for AlN . The cofired AlN with tungsten to form a multilayer ceramic is considered a recent technology achievement [31].

Conductor patterns of silver-palladium, copper, or gold are deposited by conventional screen-printing and bonding techniques, with adhesion