

Monolithic Power Systems, Inc.
v.
Greenthread, LLC

IPR2024-00468-00470 and 00550-00553

Petitioner's Demonstratives
September 10, 2025

*The word-for-word identical paper is filed in each proceeding identified in the heading.

- Overview of the pending IPR petitions
- Overview of the challenged patents
- The instituted grounds
- The petitions are not time-barred
- The prior art discloses all claim limitations
- The prior art discloses “a graded concentration of dopants . . . to aid the movement of minority carriers”
- Greenthread’s all-force-calculation premise is faulty

- Greenthread fails to demonstrate secondary considerations
- Petitioner’s expert Dr. Campbell is more reliable than Greenthread’s expert Dr. Glew

IPRs and Claims

	Patents (IPR Proceedings)	Grounds
1	195 patent (cl. 1-3, 5-6) (IPR2024-00468) 502 patent (cl. 7-8) (IPR2024-00469) 222 patent (cl. 44) (IPR2024-00470)	I. Onoda (obviousness) II. Onoda + Nishizawa III. Kawagoe (obviousness)
2	842 patent (cl. 1-2, 4-9, 12-18) (IPR2024-00550) 481 patent (cl. 1-9, 13, 15, 17, 20, 22-27, 31-32, 34) (IPR2024-00551) 222 patent (cl. 1, 3-9, 13, 15-17, 20- 21, 24-28, 32-34, 39-42) (IPR2024-00552) 014 patent (cl. 1, 3-9, 13, 15-17, 20- 21, 23-28) (IPR2024-00553)	I. Kawagoe (obviousness) II. Onoda (obviousness) III. Onoda + Nishizawa

Final Written Decisions In Other Proceedings Have Already Invalidated Multiple Patent Claims Based on a Very Similar Kawagoe Ground

- Most claims from Set 2 were already invalidated under a very similar ground based on Kawagoe alone:
 - **842 patent:**
 - IPR2023-01243, Final Written Decision, Paper 83 at 20-49 (invalidating claims 1, 2, 4–10, 12–18)
 - IPR2024-00016, Final Written Decision, Paper 74 at 15-49 (invalidating claims 1–18)
 - **481 patent**
 - IPR2024-00001, Final Written Decision, Paper 78 at 18-63 (invalidating claims 1–9, 12–14, 16–27, 30–36)
 - **222 patent**
 - IPR2023-01242, Final Written Decision, Paper 85 at 11-52 (invalidating claims 1–9, 13, 14, 16–21, 23–28, 32–42)
- A Set 1 claim was also invalidated under a ground including Kawagoe (in combination with another reference):
 - **Claim 44 of the 222 Patent:** IPR2023-01244, Final Written Decision, Paper 84 at 33-52

Set 1

'195 Patent, Claim 1	'222 Patent, Claim 44	'502 Patent, Claim 7
A CMOS Semiconductor device comprising:	A CMOS Semiconductor device comprising:	A semiconductor device comprising:
a surface layer;	a surface layer;	a surface layer;
a substrate;	a substrate;	a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;	an active region including a source and a drain, disposed on one surface of the surface layer;	an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate,	a single drift layer disposed between the other surface of the surface layer and the substrate,	a single drift layer disposed between the other surface of said surface layer and said substrate,
said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

(IPR2024-00468-470, EX1003 at ¶ 23.)

Set 2

'842 Patent, Claim 1	'481 Patent, Claim 1	'222 Patent, Claim 1	'014 Patent, Claim 1
[1.Pre] A semiconductor device comprising:	[1.Pre] A semiconductor device comprising:	[1.Pre] A VLSI semiconductor device comprising:	[1.Pre] An electronic system, the system comprising: at least one semiconductor device, the at least one semiconductor device including:
[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;	[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;	[1.1] a substrate of a first doping type at a first doping level having a surface;	[1.1] a substrate of a first doping type at a first doping level having a surface;
[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	[1.2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	[1.2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[1.4] transistors formed in at least one of the first active region or second active region; and	[1.4] transistors formed in at least one of the first active region or second active region;	[1.4] transistors formed in at least one of the first active region or second active region;	[1.4] transistors formed in at least one of the first active region or second active region;
[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
	[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,	[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,
		[1.7] wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	[1.7] wherein at least some of the transistors form digital logic of the semiconductor device.

(IPR2024-00550-553, EX1003 at Appendix B.)

Claims of Sets 1 and 2

Set 1: '195 Patent, Claim 1

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a **graded concentration of dopants** extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field **to aid the movement of minority carriers** from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 2: '842 Patent, Claim 1

1. A semiconductor device, comprising:
a substrate of a first doping type at a first doping level having first and second surfaces;
a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region; and
at least a portion of at least one of the first and second active regions having at least **one graded dopant concentration to aid carrier movement** from the first surface to the second surface of the substrate.

The petitions are not time-barred

The Board *Sua Sponte* Requested Discovery after Patent Owner Declined

1. Scope and Timing of Supplemental Discovery

Petitioner is instructed to provide the following discovery to Patent Owner by July 11, 2025:

(a) The following documents:

a. Sales agreements between Petitioner and Intel for the Intel Accused Products;⁵ and

b. Indemnification agreements between Petitioner and Intel for the Intel Accused Products. *See* IPR1242, Dir. Dec. 3.

(b) Documents sufficient to show the asserted privity relationship between Petitioner and Intel, including any new declaration(s) that establish that no documents responsive to Subsection (a) above exist, as well as any documents and new declaration(s) that establish (1) the time by which Petitioner became aware of the Intel litigation referenced in the Director's Decision; (2) whether Petitioner was the supplier of any product, or component of a product, accused of infringement in the Intel litigation; and (3) whether Petitioner was in a position to control, or actually controlled, Intel's defense of that litigation.

(IPR2024-00468, Paper 69 (Discovery Order) at 6–7)

“[T]he Board asked Patent Owner whether it wanted to take similar discovery in these IPRs, but Patent Owner declined to do so. Disc. Order at 4 (citing “IPR017,” Paper 63 at 2). Presumably perplexed by that decision, the Board *sua sponte* ordered additional discovery into Patent Owner's privity question.”

(IPR2024-00468, Paper 77 (Responsive Supplemental Brief) at 4)

“[T]he Director, upon review of the final written decisions holding all challenged claims unpatentable (*see, e.g., Semiconductor Components Indus., LLC v. Greenthread, LLC*, IPR2023-01242, Paper 84), ordered additional, narrowly tailored discovery to the same privity question that Patent Owner has raised here, so that Patent Owner could use such discovery to attempt to meet its initial burden—to offer more than a “mere assertion” under *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1242–44 (Fed. Cir. 2018).

(IPR2024-00468, Responsive Supplemental Brief at 3–4)

Petitioner Provided All Requested Discovery, Establishing No Privity

6. I have searched for sales agreements between Petitioner and Intel. There are **no sales agreements** at all between Petitioner and Intel, much less any sales agreements between Petitioner and Intel that would cover any of the Intel Accused Products.

7. I have searched for indemnification agreements between Petitioner and Intel. There are **no indemnification agreements** at all between Petitioner and Intel, much less any indemnification agreements between Petitioner and Intel that would cover any of the Intel Accused Products.

8. Petitioner did not sell to Intel, or supply Intel with, any of the Intel Accused Products. Consequently, Petitioner was **not the supplier to Intel of any product, or component of a product, accused of infringement** in the Intel litigation. (By way of background, Petitioner's principal customers are contract manufacturers located in Asia, rather than downstream branded companies such as Intel.)

(IPR2024-00468, EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12)

10. None of the searches described above turned up any reference to Patent Owner or Patent Owner's prior litigation against Intel prior to May 26, 2023, the date that Patent Owner filed its lawsuit against Petitioner in the United States District Court for the District of Delaware. Thus, I found no evidence that Petitioner had any knowledge of Patent Owner at all prior to May 26, 2023, much less Patent Owner's prior litigation against Intel. Instead, Petitioner learned of the Intel litigation as it began to investigate the allegations in, and merits of, Patent Owner's May 26, 2023 complaint against Petitioner. Based on my investigation, it appears Petitioner **first learned** of Patent Owner's litigation against Intel on or about **May 26, 2023**.

12. Petitioner had **no knowledge of, or involvement in, Intel's defense in its litigation against Patent Owner**. Petitioner **did not actually control, nor was it in a position to control**, Intel's defense in that litigation.

Petitioner is Not in Privity with Intel – No Ability to Participate in Litigation

“[I]n analyzing privity, the Federal Circuit and P.T.A.B. have generally focused on evidence of control, indemnity agreements, sales agreements, and fairness to the petitioner. *See, e.g., WesternGeco*, 889 F.3d at 1319–22.”

(IPR2024-00468, Paper 77 (Responsive Supplemental Brief) at 9)

Control Factor Weighs Against Privity

Petitioner did not control or direct lawsuit between PO and Intel.

- Petitioner did not learn of Intel lawsuit until a month after it settled.
- Petitioner was in no position to control it. Petitioner could not have controlled lawsuit.
- No contractual agreements existed giving Petitioner that authority.

(IPR2024-00468, Responsive Supplemental Brief at 9–10)

Legal Relationship Factors Weigh Against Privity

No special legal relationship between Petitioner and Intel.

- Petitioner does not have any indemnity or sales agreements with Intel.

Federal Circuit found no privity even with an indemnity agreement (*WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1321 (Fed. Cir. 2018)).

(IPR2024-00468, Responsive Supplemental Brief at 10–11)

Fairness Weigh Against Privity

It would be unfair to hold Petitioner in privity with Intel for a lawsuit it did not know about and could not control, and where it had no sales agreements or indemnity agreements with Intel.

(IPR2024-00468, Responsive Supplemental Brief at 11–12)

Patent Owner Cannot Show Any Factors Support a Finding of Privity

Petitioner's Products Hypothetically Showing up in Intel Accused Products Would Not Show Privity

- “Patent Owner does not cite a case showing that a party’s product which was not implicated as an accused product in another lawsuit was a dispositive factor for finding privity.”
- PO has not produced evidence of Petitioner’s products being in an IAP despite investigating those Intel products.

(IPR2024-00468, Responsive Supplemental Brief at 13)

If There Had Been Any Evidence of Petitioner's Products in the IAPs, It Would Not Show Privity

- Petitioner’s products were not implicated in the Intel lawsuit (directed to Intel microprocessors, not low-level tiny power converters and regulators).
- Even if Petitioner products were in IAPs, it would not show privity given the other undisputed facts

(IPR2024-00468, Responsive Supplemental Brief at 15)

Indirect Business Relationships Do Not Show Privity

Privity has not been found in cases even where there was a direct sales relationship because such a sales relationship alone does not show that the parties are “sufficiently close that both should be bound by the trial outcome and related estoppels.” *WesternGeco*, 889 F.3d at 1321.

(IPR2024-00468, Responsive Supplemental Brief at 14)

Preceding/Succeeding Owners of Property Are Not Privies

“If the sale of an electrical component (i.e., a transfer of property) meant that the buyer and seller were always in privity, then Petitioner would be in privity with every single downstream product manufacturer that ever incorporated one of Petitioner’s products That cannot possibly be true”

(IPR2024-00468, Responsive Supplemental Brief at 14)

The prior art discloses all claim limitations

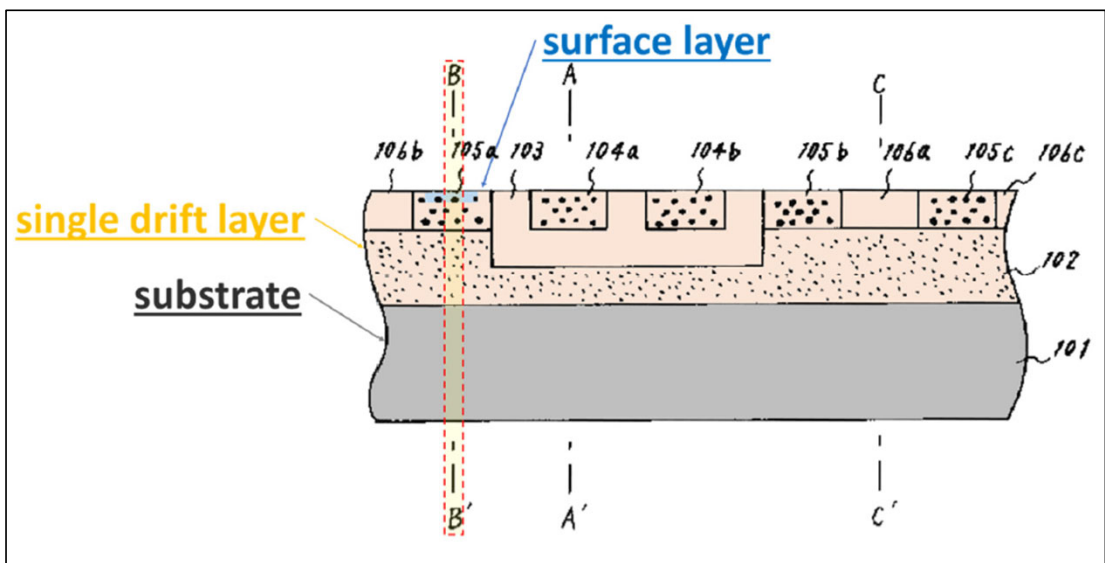
Set 1, G1 (Set 2, G2): Obviousness Over Onoda (Ex. 1042)

[OBJECT]

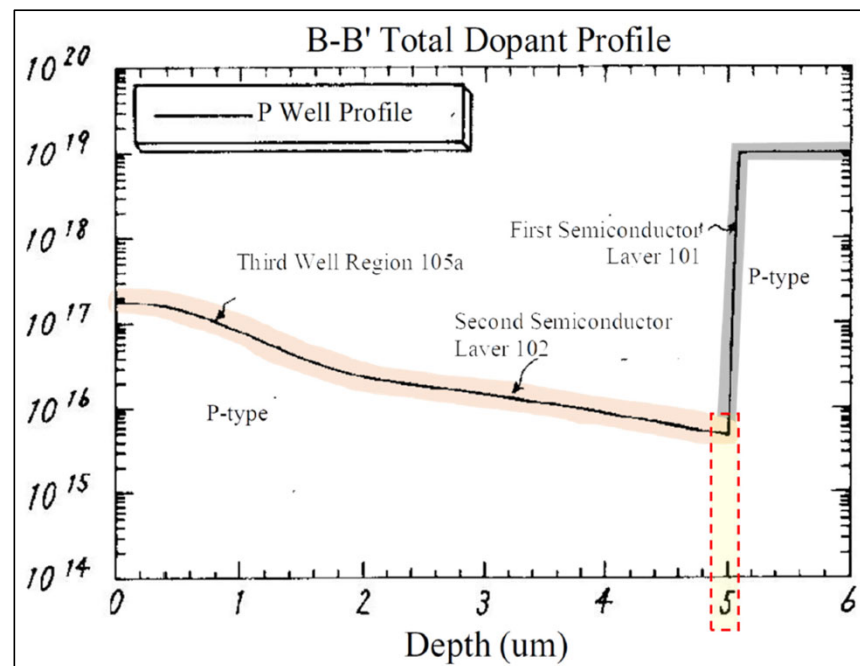
To provide a nonvolatile semiconductor storage device with improved latch-up resistance and punch-through breakdown voltage and improved junction breakdown voltage between the well regions and the semiconductor substrate.

(IPR2024-00468, Ex. 1042 (Onoda) at Object)

Set 1, G1: Onoda (Ex. 1042)

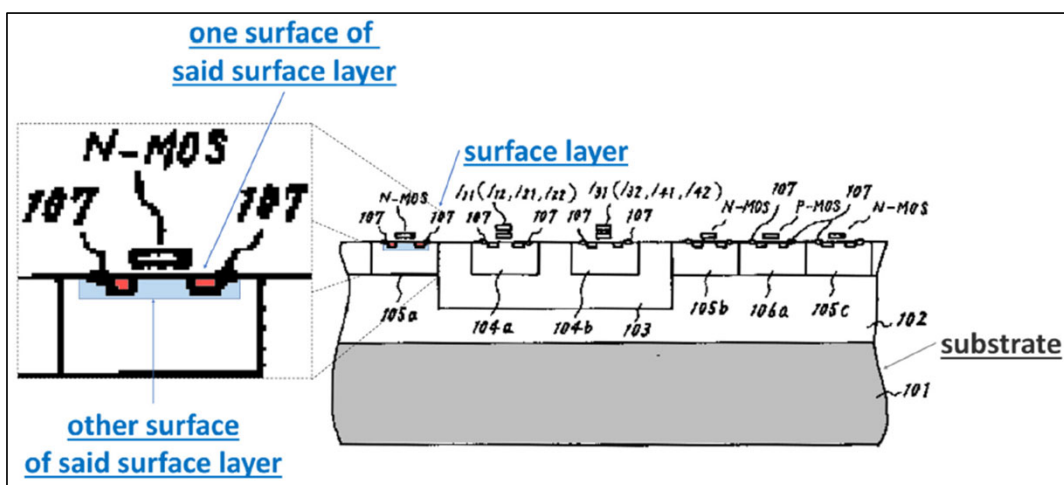


(IPR2024-00468, Petition at 30 (citing Onoda at FIG. 8))



(IPR2024-00468, Petition at 31 (citing Onoda at FIG. 11))

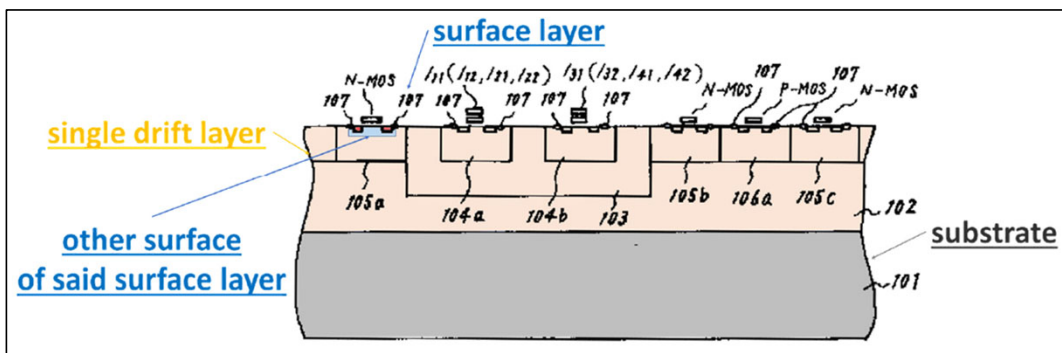
Set 1, G1: '195 Patent, Claim 1: surface layer, substrate, active region



(IPR2024-00468, Petition at 25 (citing Onoda at FIG. 3))

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

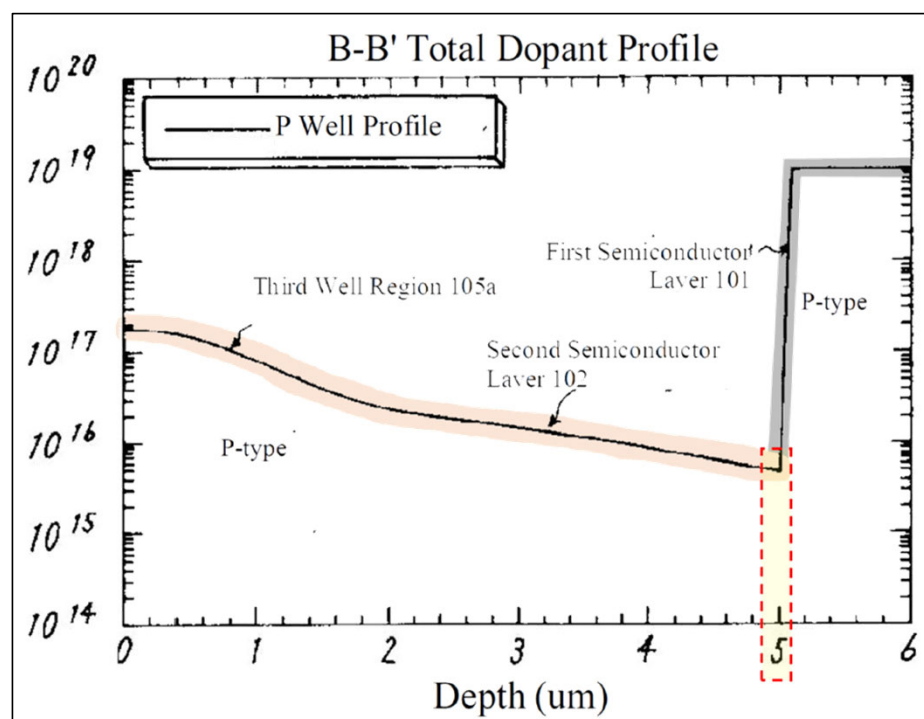
Set 1, G1: '195 Patent, Claim 1: single drift layer between other surface and substrate



(IPR2024-00468, Petition at 29 (citing Onoda at FIG. 3))

1. A CMOS Semiconductor device comprising:
 - a surface layer;
 - a substrate;
 - an active region including a source and a drain, disposed on one surface of said surface layer;
 - a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
 - at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

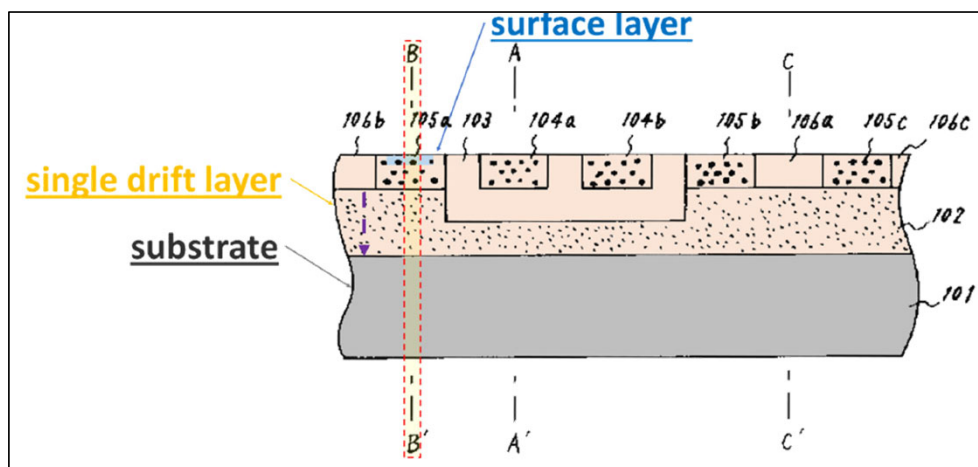
Set 1, G1: '195 Patent, Claim 1: graded concentration of dopants



(IPR2024-00468, Petition at 31 (citing Onoda at FIG. 11))

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 1, G1: '195 Patent, Claim 1: graded concentration of dopants



(IPR2024-00468, Petition at 33 (citing Onoda at FIG. 8))

1. A CMOS Semiconductor device comprising:
 - a surface layer;
 - a substrate;
 - an active region including a source and a drain, disposed on one surface of said surface layer;
 - a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
 - at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 1, G1: '195 Patent, Claim 1: aid the movement prosecution history

3. Claim 10-16 and 18-24 rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for “a unidirectional drift field” (see line 8 of base claims 10 and 18, each, which is shown in Figure 2 of the specification) , does not reasonably provide enablement for “drawing all minority carriers from said substrate to said surface layer” (emphasis added, see last two lines each of base claims 10 and 18).

(IPR2024-00468 (EX1002 at 269); Reply at 5-6))

knowing other parameters of the device) that it will draw ‘all’ minority carriers...” Yet, this argument appears to not consider that the graded dopant concentration itself creates a “built-in” electrical field that forces the movement of carriers into a particular direction, whereby the “direction” of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant. With regard to the existence of a

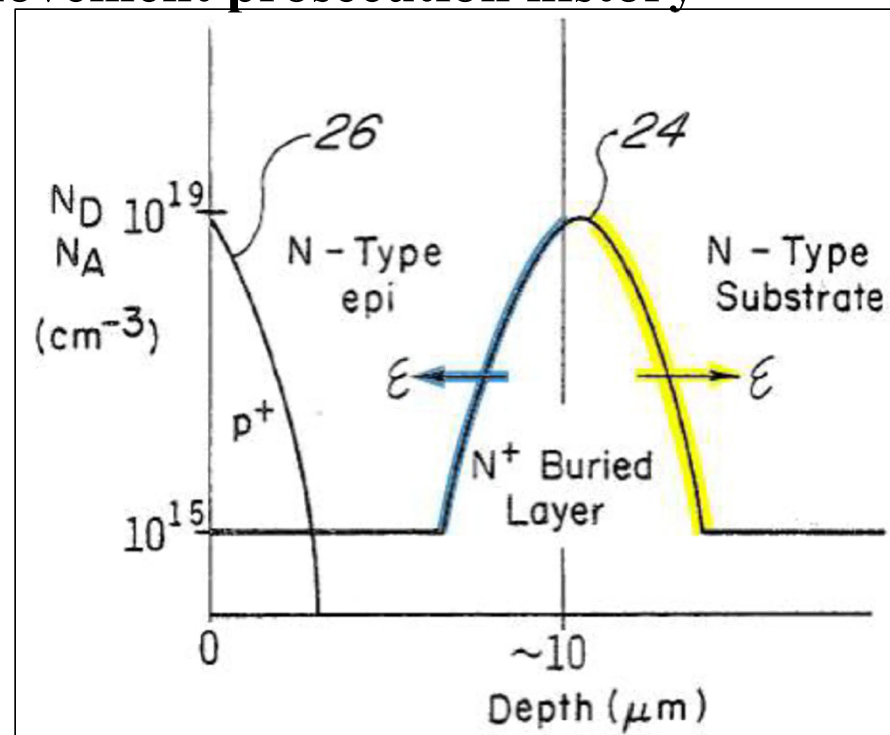
(IPR2024-00468 (EX1002 at 270); Reply at 5-6))

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 1, G1: '195 Patent, Claim 1: aid the movement prosecution history

"maintain" and "single." With regard to the remaining term "static," Applicant respectfully notes that prior art reference Kamins (US 4,160,985), just like Applicant, discloses the presence of a "static" drift field, "because the drift field is created by graded concentration of dopants which does not change over time." See Office Action ¶4 p.4 lines 1-3, further citing to Kamins, Col. 2, lines 15-16; Col. 2, line 64 – Col. 3, line 2; Col. 1, lines 38-46; and Col. 3, lines 8-11.

(IPR2024-00468, EX1002 at 333, Reply at 7)



(IPR2024-00468 (EX1009 at FIG. 3); Petition at 11))

face. More specifically, carriers created below the maximum dopant concentration are accelerated into the substrate where they recombine without contributing to

(IPR2024-00468 (EX1009 at 3:8-10); Reply at 7; Petition at 12))

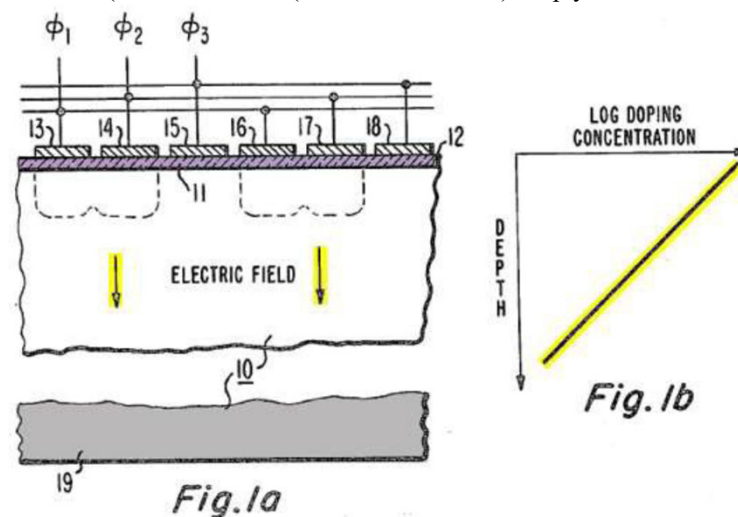
Set 1, G1: '195 Patent, Claim 1: aid the movement prosecution history

solely on the slope of the graded concentration of dopant. With regard to the existence of a “built-in” electric field created by a graded dopant density, *see*, e.g., Jastrzebski (US 4,481,522) col. 5, lines 11-13 (cited in Office Action). Applicant respectfully submits that this inherent “built-in” unidirectional electric field is the additional parameter for ensuring that all minority carriers are being moved in one direction and which parameter the Office Action deemed to be missing from the disclosure.

(IPR2024-00468, EX1002 at 290, Reply at 7)

regions induced adjacent to surface 11. This electric field can be a drift field created by a graded concentration of doping in the substrate. In the FIG. 1a structural segment the gradient of doping concentration would be normal, or perpendicular, to the surface 11 of substrate 10, with the doping concentration decreasing with depth from surface 11. The drift field is accordingly directed to force most of the charge carriers generated outside a depletion region deep into the substrate 10 bulk. In these portions of the bulk remote from surface

(IPR2024-00468 (EX1010 at 5:11-20); Reply at 7; Petition at 11))



(IPR2024-00468 (EX1010 at FIG. 1a, FIG. 1b); Petition at 11))

MPS

Set 1, G1: '195 Patent, Claim 1: Patent Owner's district court construction

other charge carriers passing by. When the dopant concentration is graded in a particular direction, other charge carriers will move in the gradient direction (or opposite direction) depending on the charge carrier's polarity. This phenomenon is called "carrier drift."

(IPR2024-00468, EX1030 at 2, Reply at 4, 14)

Set 1, G1: '195 Patent, Claim 1: Patent Owner's claim construction arguments

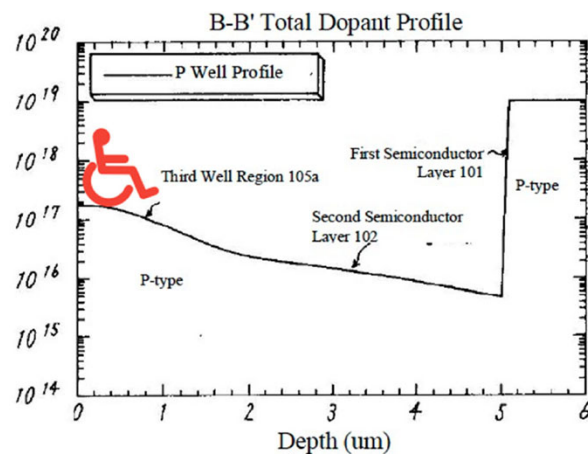
language. Electric drift fields are a well-known phenomenon that cause carriers to move, and a POSITA would have readily recognized that when a “static unidirectional electric drift field” is present that it aids the movement of the minority carriers. If it isn't present, then it doesn't. The claim turns on the presence of the “unidirectional electric drift field,” and the phrase “to aid the movement of minority carriers” merely states what the “unidirectional electric drift field” does. The drift field points to one direction and charge carriers, when free to move, respond to the drift field by moving in one direction or the other depending on their charge polarity. Ex. 1, ¶88.

(IPR2024-00468 (EX1030 at 26-27); Reply at 4)

Set 1, G1: '195 Patent, Claim 1 : Patent Owner's district court construction

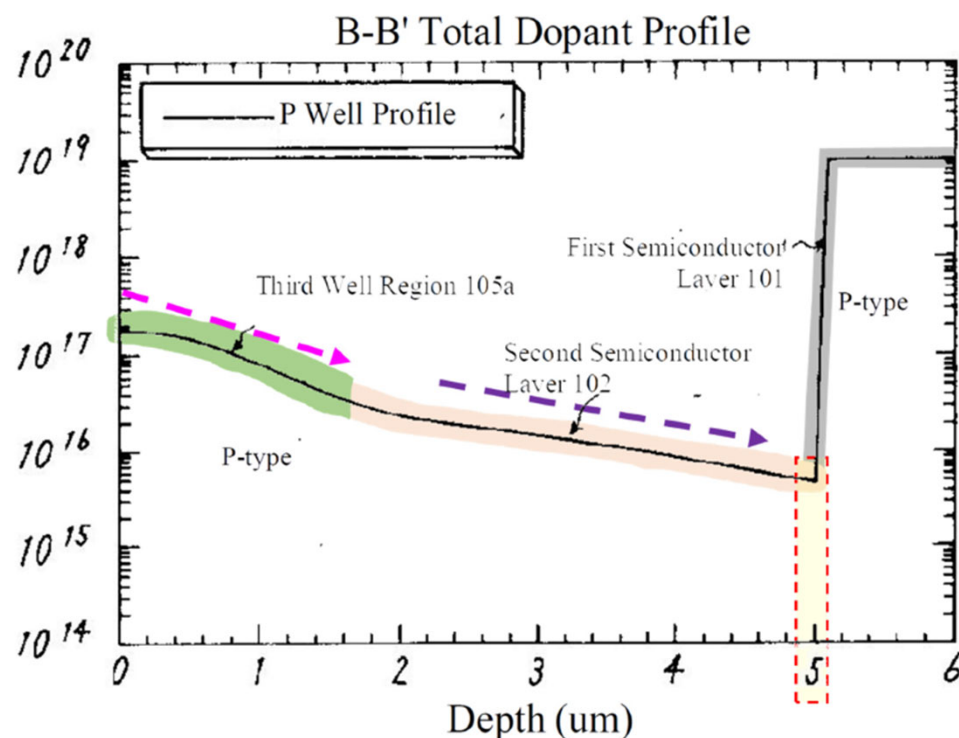
to determine the bounds of the invention. To use another example, if a claim recites: a wheelchair ramp to aid movement of a wheel chair from a first level to a ground level. There is no requirement that the claim specify the length or slope of the ramp as long as it allows the wheelchair user to get to ground level. Again the same is true here. When the claims specify what is providing the movement, and the direction of the movement, nothing more is required.

(IPR2024-00468 (EX1030 at 27); Reply at 11-12)



(IPR2024-00468 (Onoda at FIG. 11); Reply at 12)

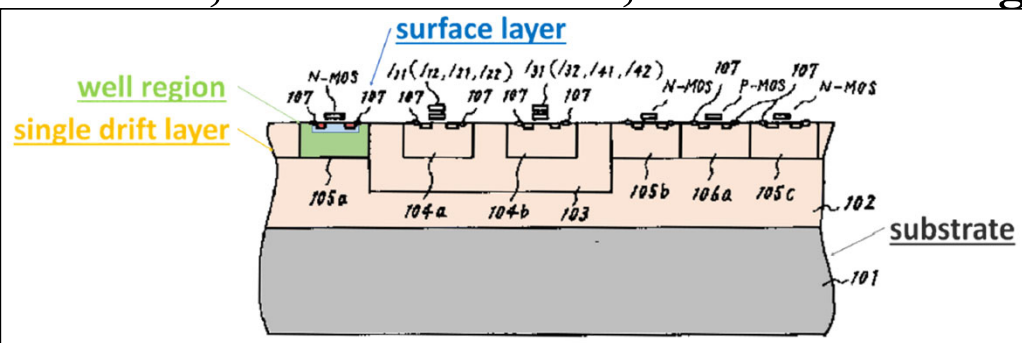
Set 1, G1: '195 Patent, Claim 1: well region's graded concentration of dopants



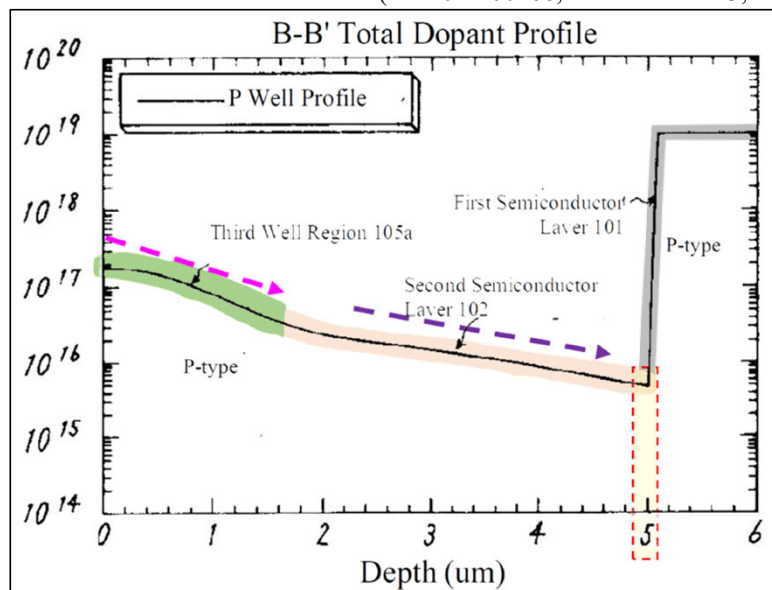
(IPR2024-00468, Onoda at FIG. 11, Petition at 37)

1. A CMOS Semiconductor device comprising:
 a surface layer;
 a substrate;
 an active region including a source and a drain, disposed on one surface of said surface layer;
 a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
 at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 1, G1: '195 Patent, Claim 1: all together



(IPR2024-00468, Onoda at FIG. 3, Petition at 35)



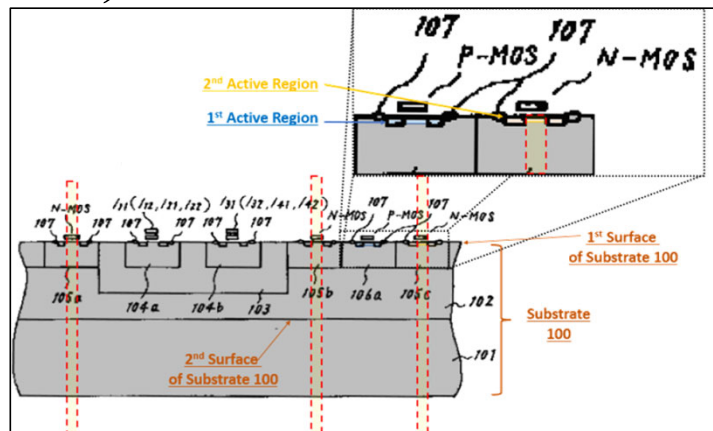
(IPR2024-00468, Onoda at FIG. 11, Petition at 37)

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

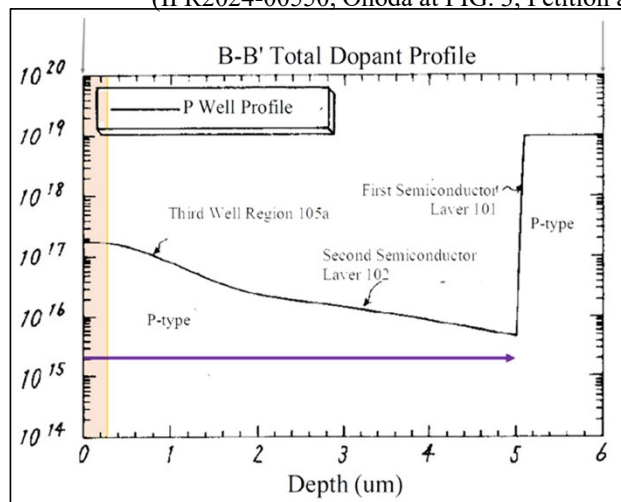
Slide: 28

Petitioner's Demonstratives – IPR2024-00468-00470 and 00550-00553

Set 2, G2: '842 Patent: Claim 1 all together



(IPR2024-00550, Onoda at FIG. 3, Petition at 51)



(IPR2024-00550, Onoda at FIG. 1, Petition at 55))

1. A semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level having first and second surfaces;
 - a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region; and
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate

Set 1, G1 : Obviousness Over Onoda in view of Nishizawa (EX1046)

gradient (*e.g.*, Onoda at FIG. 11). (Ex. 1003 at ¶¶ 91-92.) Again, Nishizawa makes explicit the concept of an “electric field” that migrates minority carriers to a substrate based on a dopant gradient (Nishizawa at 18:10-18), whereas Onoda describes the structure (*e.g.*, the downward dopant gradient, Onoda at FIG. 11), which a POSITA would have understood necessarily creates the specified physical conditions. A

(IPR2024-00468, Petition at 48))

b. Elements [1.1]-[1.4]

For the same reasons as in Ground I, Elements 1.1-1.4 are disclosed and/or rendered obvious by the Onoda-Nishizawa combination.

(IPR2024-00468, Petition at 50))

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 2, G2 : Obviousness Over Onoda in view of Nishizawa (EX1046)

Onoda discloses multiple active regions whose dopant concentrations have a downward gradient, which a POSITA would have recognized as providing an electric drift field in the active region to aid the movement of minority carriers from the first surface to the second surface of the substrate (substrate 100). (III.B.1.a.vi; Ex. 1003 at ¶¶66-69, ¶101 (and Footnote 7) and ¶¶113-116; Ex. 1003 at ¶143.) Nishizawa similarly discloses employing graded dopant concentrations to create drift electric fields to aid carrier movement. (Nishizawa at 18:10-18.) Nishizawa makes explicit that the downward gradient aids in the movement of carriers to the substrate. (*Id.* at 18:47-50, 19:1-19, 18:10-18.)

(IPR2024-00550, Petition at 73)

b. Elements [1.1]-[1.4]

Consistent with Ground II, Onoda discloses and/or renders obvious Elements

[1.1] through [1.4]. (Ex. 1003 at ¶142.)

Slide: 31

(IPR2024-00550, Petition at 73)

Petitioner's Demonstratives – IPR2024-00468-00470 and 00550-00553

1. A semiconductor device, comprising:
a substrate of a first doping type at a first doping level having first and second surfaces;
a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
transistors formed in at least one of the first active region or second active region; and
at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.



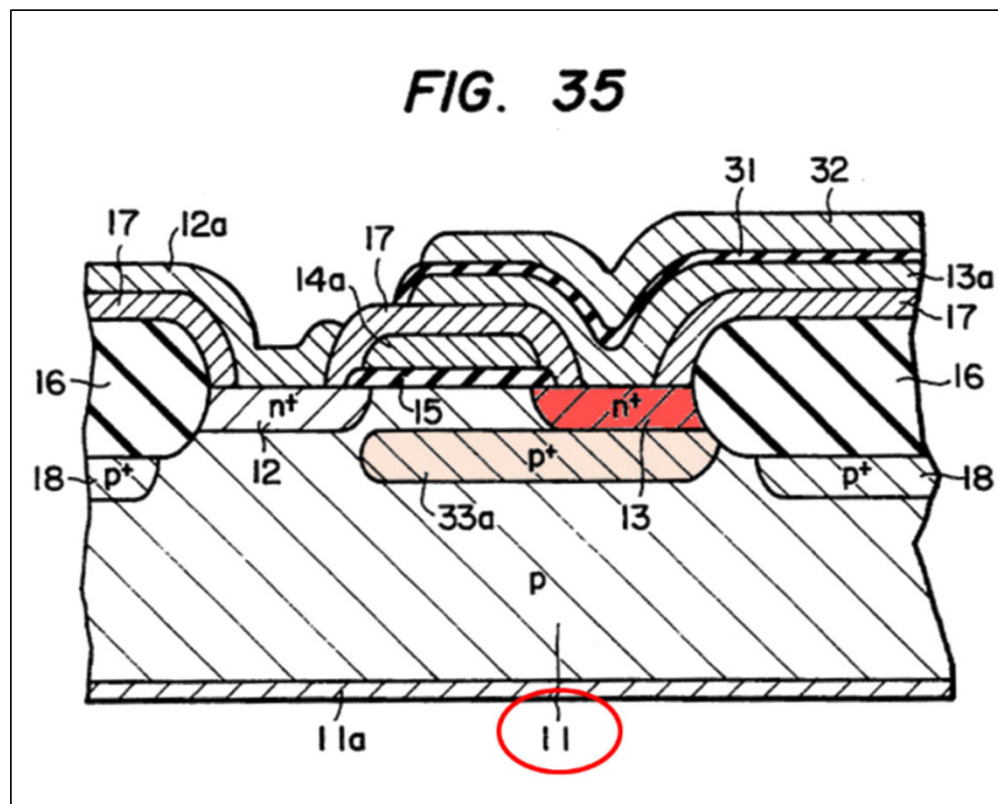
Nishizawa – downward gradient drifts electrons downward

However, with the device structure as described just above and shown in FIG. 35, those electrons, among the electrons which have been created by alpha-particle in the p⁺ type buried region 33a, which are located in the upper half portion of the p⁺ type buried region 33a located closer to the n⁺ type region 13, will diffuse toward that side which is contiguous with the n⁺ type region 13. This diffusion of electrons will be accelerated by a reverse bias electric field applied between the two regions 33a and 13, so that the electrons will flow into the n⁺ type region 13 and will constitute a cause of extinction of memory. In order to prevent such flow of electrons, it is only necessary to form an impurity concentration gradient in the p⁺ type buried region 33a in the direction toward the p type substrate 11. For example, the impurity concentration of that portion of the p⁺ type buried region 33a located adjacent the channel region and the n⁺ type region 13 is set at about $1 \times 10^{17} \text{ cm}^{-3}$, with progressively lowered concentration as the portions of the buried region 33a go progressively toward the p type substrate 11, in such manner that the impurity concentration of lowermost portion of the buried region is less than at least one third of that of the highest impurity concentration. Usually, the impurity concentration of the p type substrate 11 is about 10^{15} cm^{-3} . However, it is also effective to arrange this impurity concentration of the semiconductor substrate 11 at a low level such as about $1 \times 10^{15} \text{ cm}^{-3}$ or about $1 \times 10^{14} \text{ cm}^{-3}$, and also to arrange the impurity concentration of the channel region at a desired higher level by channel doping using ion-implantation technique. The p⁺ buried region, usually, is fabricated by ion-implantation.

(Nishizawa at 18:35-68; IPR2024-00468, Petition at 50-51, Reply at 18)

Slide: 32

Petitioner's Demonstratives – IPR2024-00468-00470 and 00550-00553



(Nishizawa at FIG. 35; IPR2024-00468, Reply at 19)

Nishizawa – uniform gradient does not solve problems of electrons generated via alpha ray

may be higher than that. Even where the impurity concentration of the p⁺ type region 33a is substantially uniform as portions of this region go progressively toward the p type substrate 11, there is being produced.

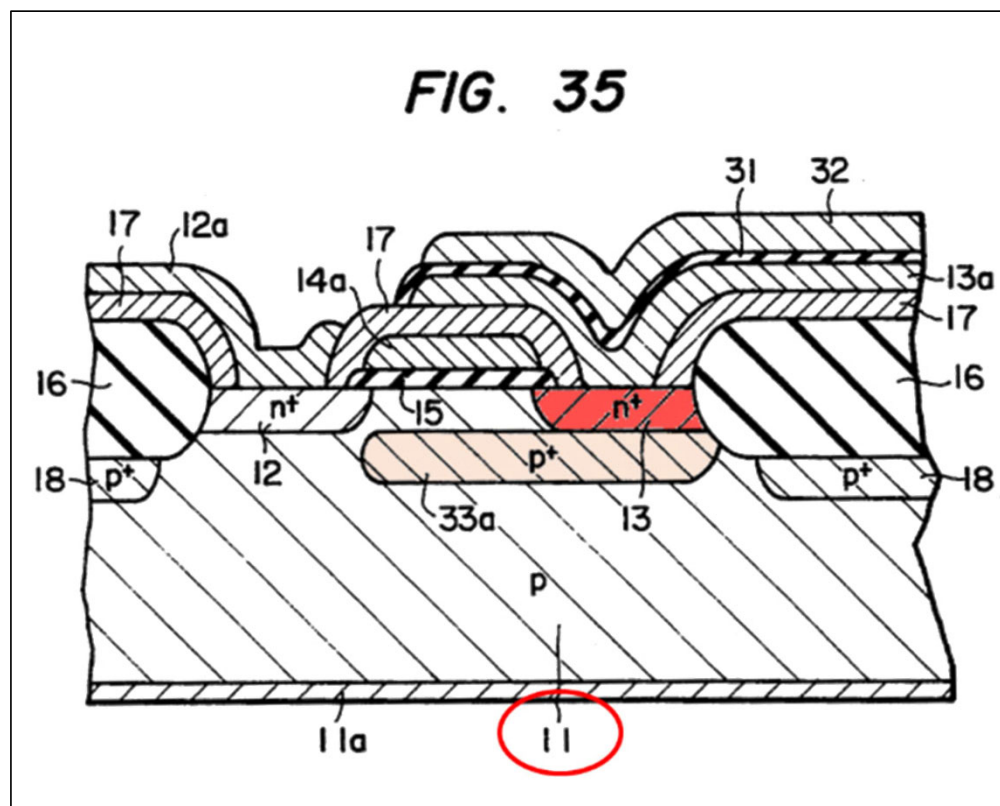
(Nishizawa at 18:5-7; IPR2024-00468, Reply at 18)

toward the p⁺ type buried region 33a. Those electrons which are created by alpha-particle in the p type substrate 11 are transferred back to the p type substrate 11 side by this electric field, and thus they cannot enter into the p⁺ type buried region 33a. Therefore, these

(Nishizawa at 18:18-22; IPR2024-00468, Reply at 18)

However, with the device structure as described just above and shown in FIG. 35, those electrons, among the electrons which have been created by alpha-particle in the p⁺ type buried region 33a, which are located in the upper half portion of the p⁺ type buried region 33a located closer to the n⁺ type region 13, will diffuse toward that side which is contiguous with the n⁺ type region 13. This diffusion of electrons will be accelerated

(Nishizawa at 18:35-42; IPR2024-00468, Reply at 18)

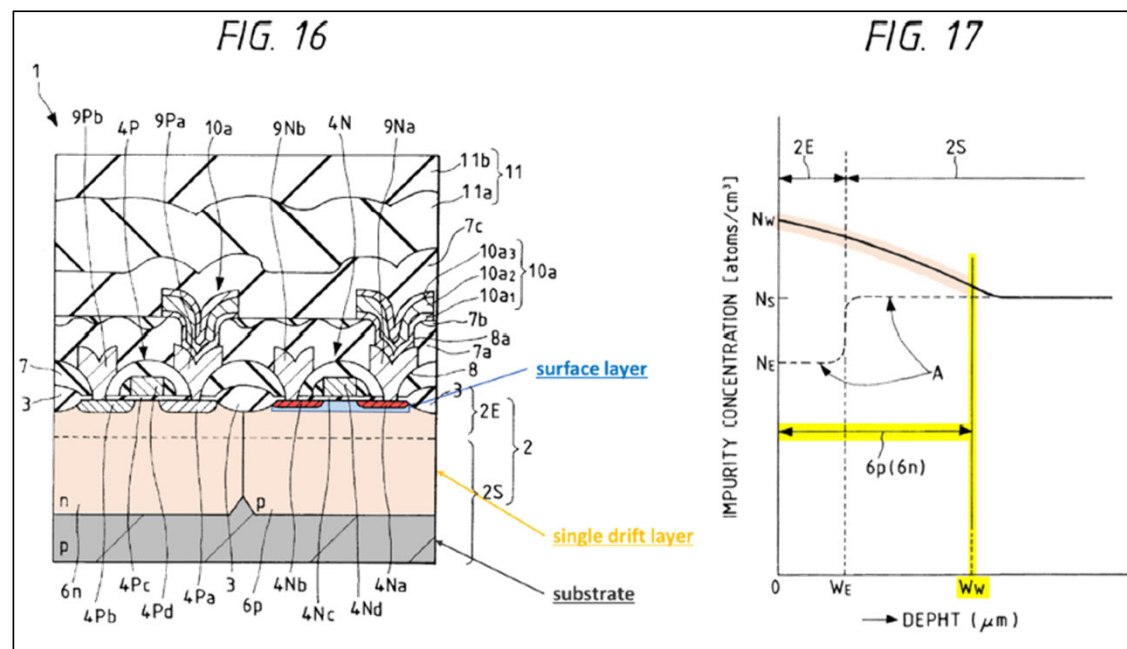


(Nishizawa at FIG. 35; IPR2024-00468, Reply at 19)

Set 1, G3 (Set 2, G1): Obviousness over Kawagoe (EX1007)

from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E. Thus, the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p. The impurity

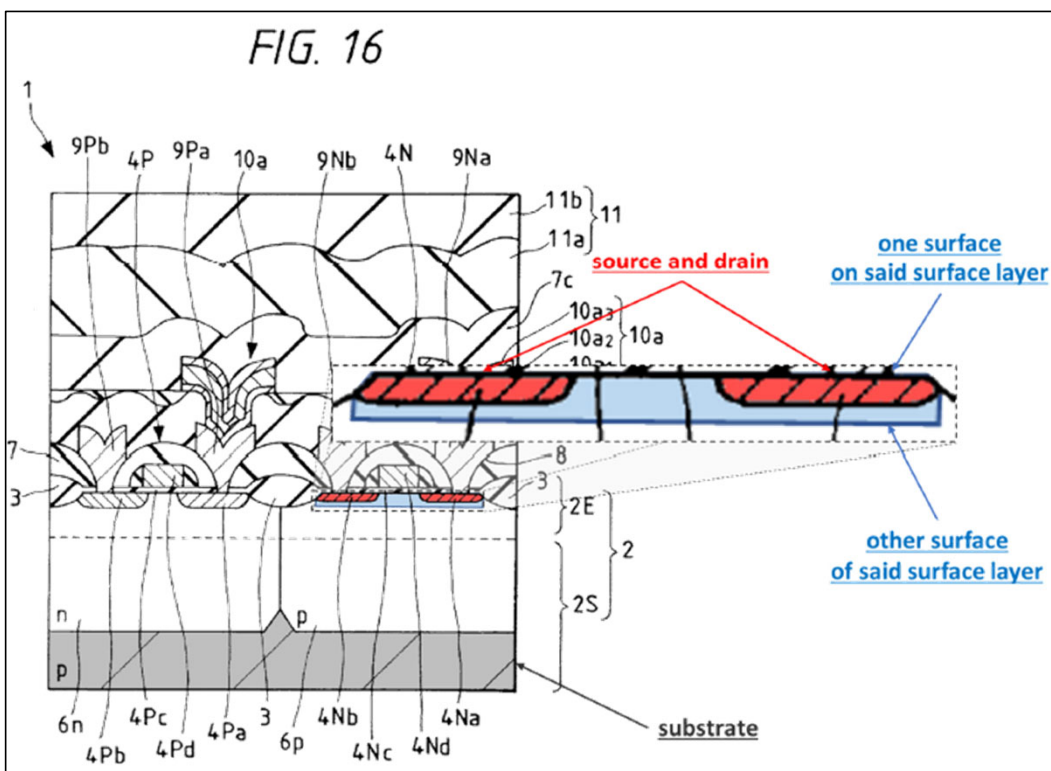
(Kawagoe at 16:2-11; IPR2024-00468, Petition at 64)



(Kawagoe at FIGS. 16 and 17; IPR2024-00468, Petition at 66)

Set 1, G3: '195 Patent, Claim 1: surface layer, substrate, active region

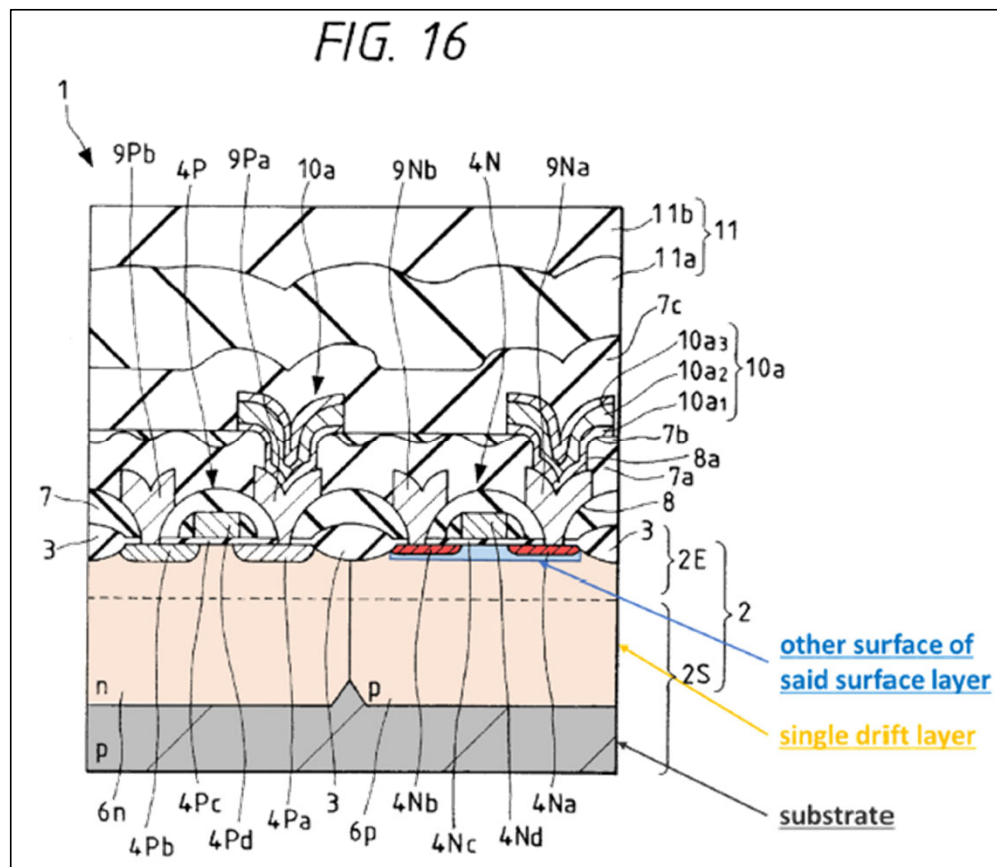
FIG. 16



(Kawagoe at FIG. 16; IPR2024-00468, Petition at 60)

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

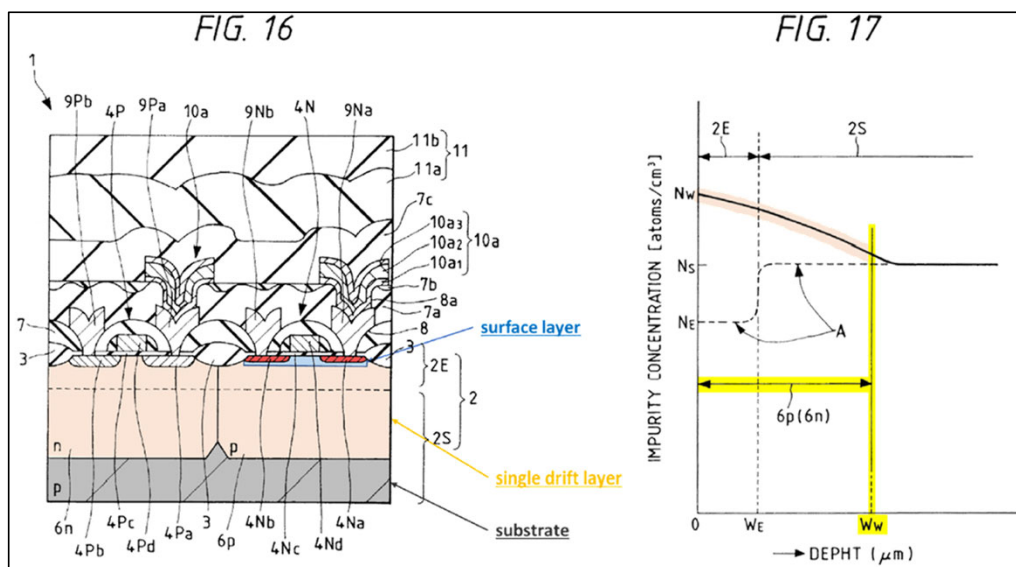
Set 1, G3: '195 Patent, Claim 1: single drift layer between other surface and substrate



(Kawagoe at FIG. 16; IPR2024-00468, Petition at 64)

1. A CMOS Semiconductor device comprising:
 - a surface layer;
 - a substrate;
 - an active region including a source and a drain, disposed on one surface of said surface layer;
 - a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
 - at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 1, G3: '195 Patent, Claim 1: graded concentration of dopants



(Kawagoe at FIGS. 16 and 17; IPR2024-00468, Petition at 66)

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

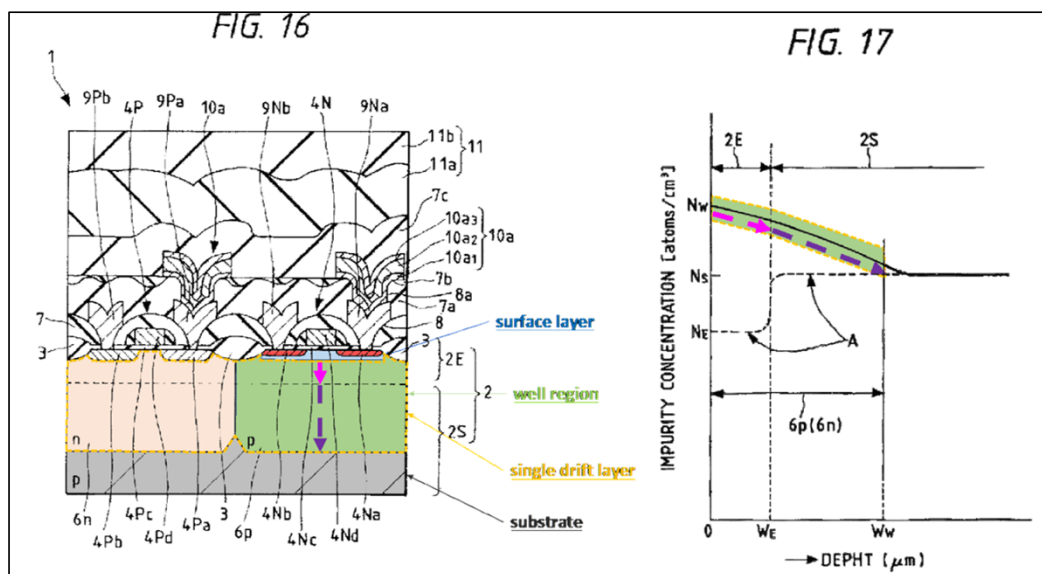
Set 1, G3: '195 Patent, Claim 1: graded concentration of dopants

from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E. Thus, the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p. The impurity

(Kawagoe at 16:1-11; IPR2024-00468, Petition at 64)

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

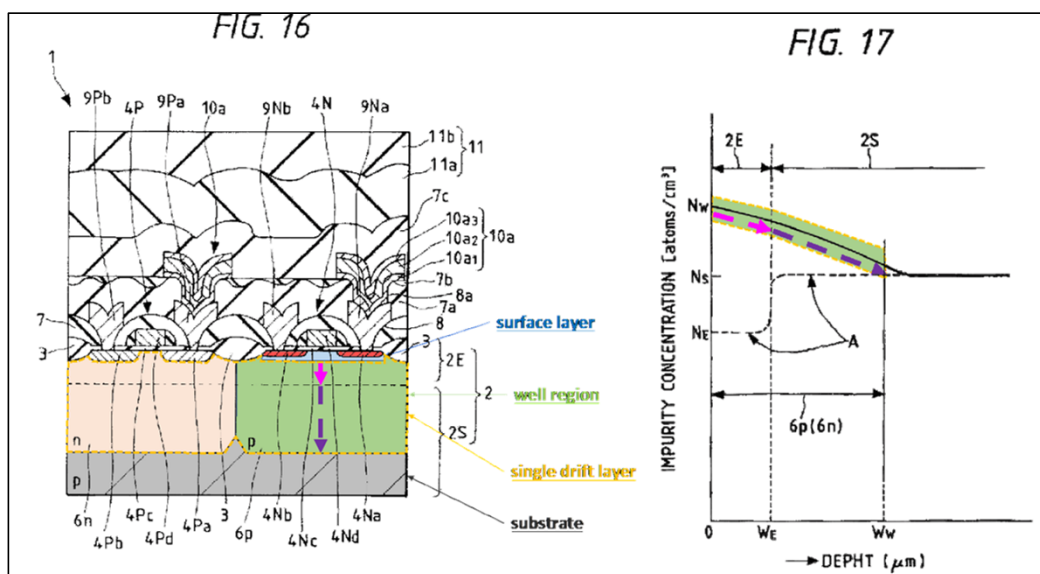
Set 1, G3: '195 Patent, Claim 1: well region's graded concentration of dopants



(Kawagoe at FIGS. 16 and 17; IPR2024-00468, EX1003, ¶ 124, Petition at 75, 77)

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Set 1, G3: '195 Patent, Claim 1: all together



(Kawagoe at FIGS. 16 and 17; IPR2024-00468, EX1003 at ¶ 124, Petition at 75, 77)

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Level of ordinary skill in the art

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) “would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience.” Pet. 5 (citing Ex. 1003 ¶ 17). According to Petitioner, “[a]dditional education might compensate for a deficiency in experience, and vice-versa.” *Id.* On the present record, Patent Owner does not contest Petitioner’s definition of a person of ordinary skill in the art. Prelim. Resp. 1–31.

(IPR2024-00468, Institution Decision at 6.)

The challenged claims are directed to a device

Claims directed to device

Apparatus claims “cover what a device is, not what a device does.”
ParkerVision, Inc. v. Qualcomm Inc.,
903 F.3d 1354, 1361 (Fed. Cir. 2018).

(IPR2024-00468, Reply at 2-3)

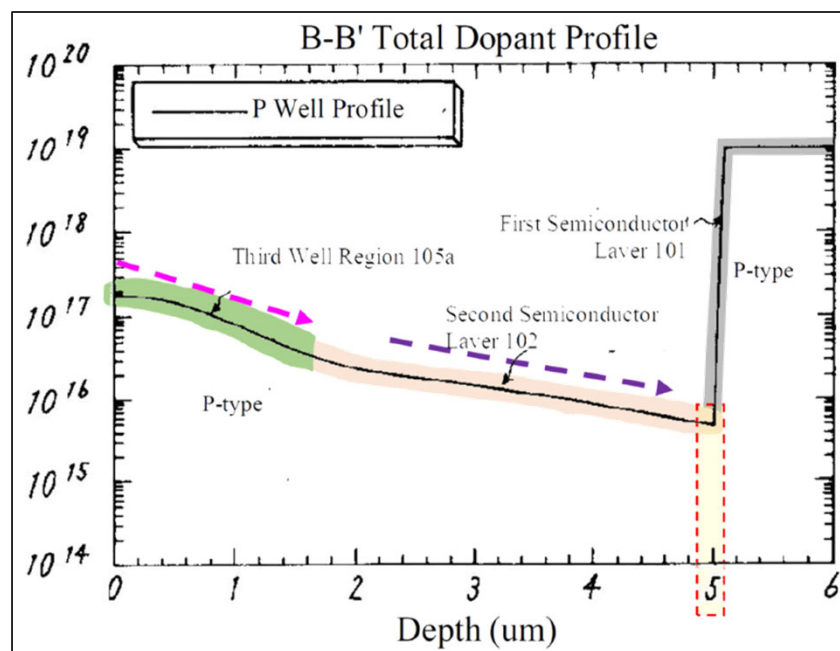
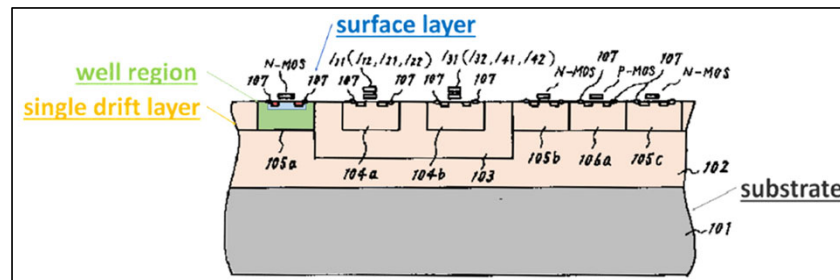
1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Patent Owner's Sur-Reply

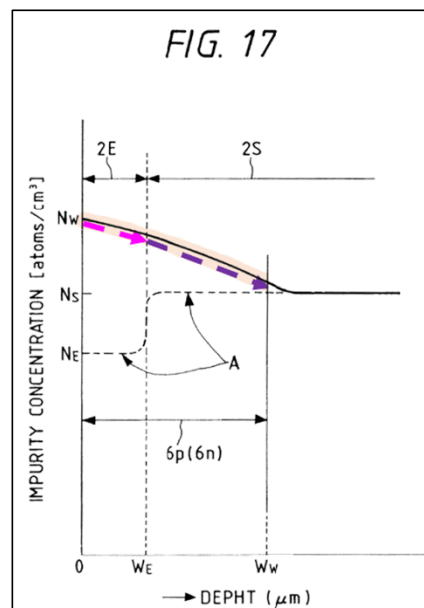
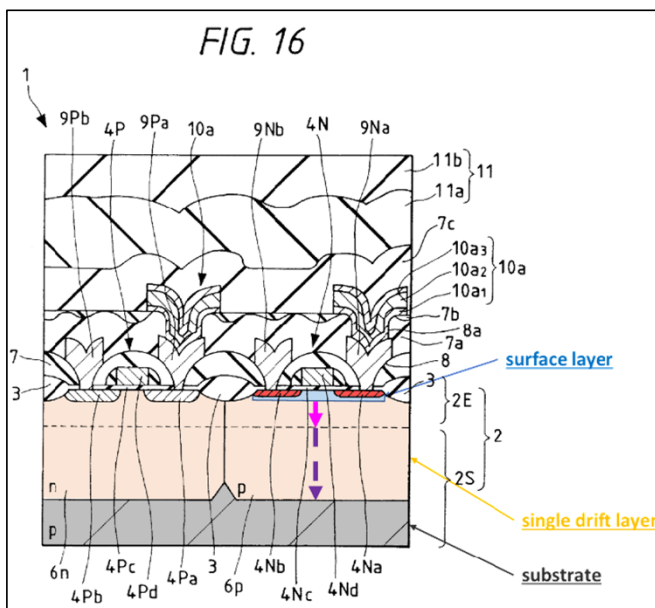
The Federal circuit has recognized that for “mechanical apparatus claims” (as opposed to computer or software claims), the claims are “configuration-type claims.” *Id.* at 1371-72 (citing *Ball Aerosol* and *Cross Medical*). Here, the claims are clearly “mechanical apparatus claims.” The claims require a “graded

(IPR2024-00468, Paper 47 (Sur-Reply) at 3 (citing *INVT SPE LLC v. Int’l Trade Comm’n*, 46 F.4th 1361, 1372-72 (Fed. Cir. 2022))

Onoda and Kawagoe



(Onoda at FIGS. 3 and 11; IPR2024-00468, Petition at 35 and 37)



(Kawagoe at FIGS. 16 and 17; IPR2024-00468, Petition at 72)

Claims do not require a magnitude or slope

The claims do not require any specific magnitude for the slope gradient or electric field

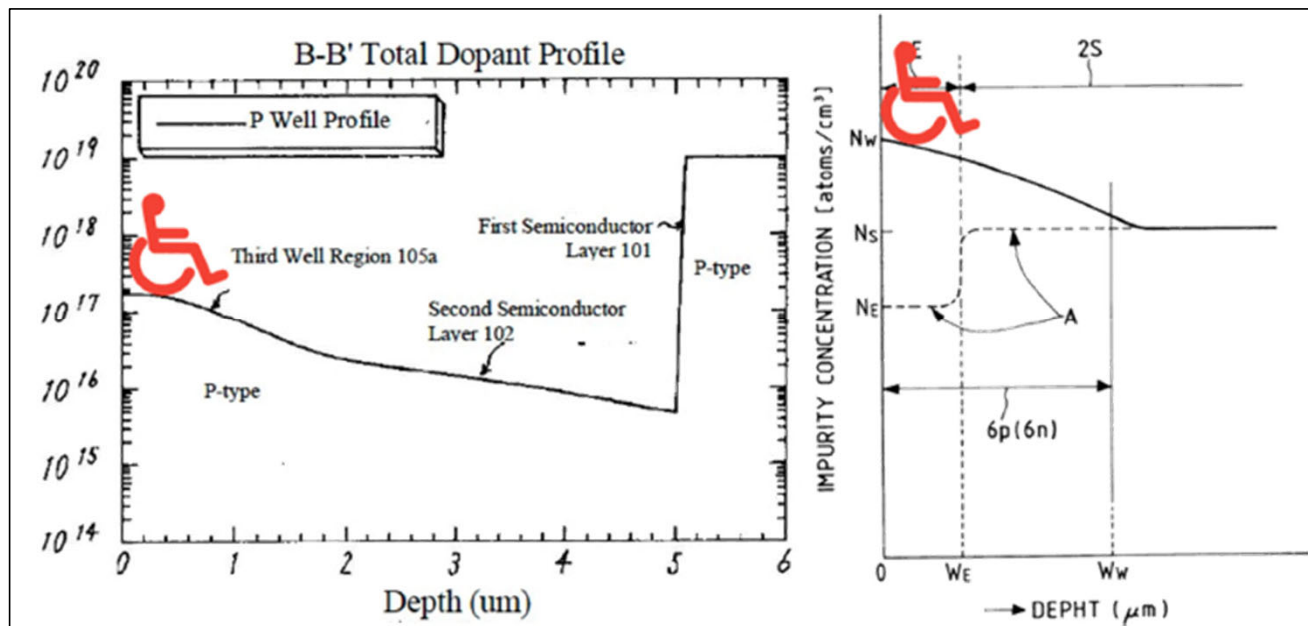
to determine the bounds of the invention. To use another example, if a claim recites: a wheelchair ramp to aid movement of a wheel chair from a first level to a ground level. There is no requirement that the claim specify the length or slope of the ramp as long as it allows the wheelchair user to get to ground level. Again the same is true here. When the claims specify what is providing the movement, and the direction of the movement, nothing more is required.

(IPR2024-00468 (EX1030 at 25, 27-28); Reply at 11))

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Patent Owner's Arguments Fail

Onoda and Kawagoe have a graded concentration of dopants . . . to aid the movement of minority carriers

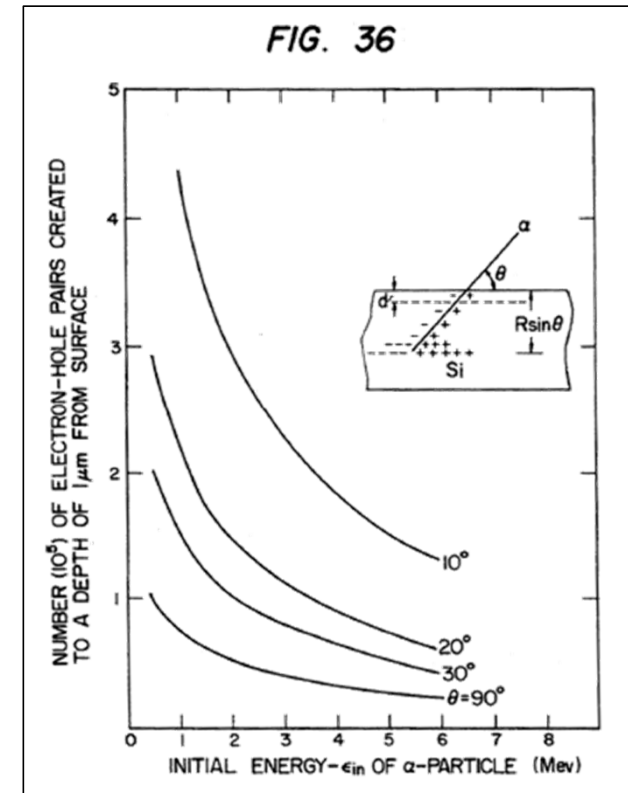


(Onoda at FIG. 11 and Kawagoe at FIG. 16; IPR2024-00468, Reply at 12))

Nishizawa's surface electrons

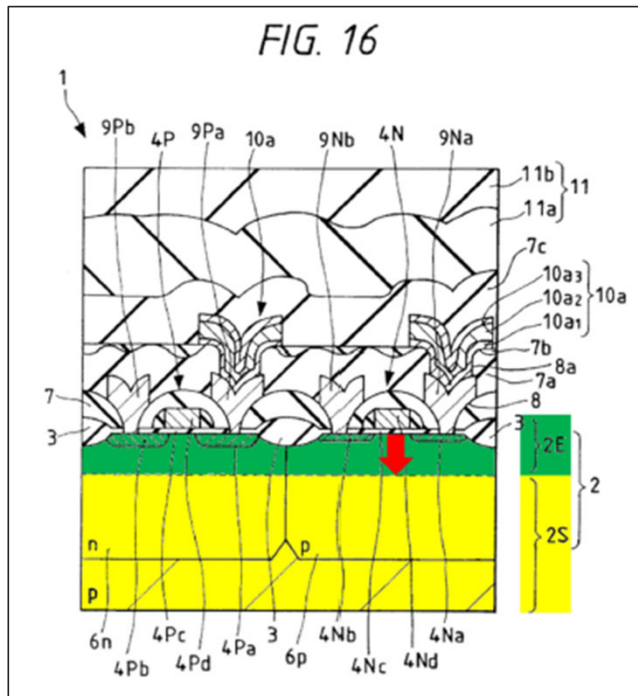
the depth of entry of alpha-particle will be $25\text{ }\mu\text{m}$. Accordingly, alpha-particle which is irradiated with an energy of about 5 MeV will not make many electron-hole pairs at the surface of silicon semiconductor substrate, and will create a greater number of electron-hole pairs when alpha-particle has lost 90% or more of its energy. An alpha-particle is considered, in ordinary

(Nishizawa at 17:12-18; IPR2024-00468, Reply at 19-20)



(Nishizawa at FIG. 36; IPR2024-00468, Reply at 19-20))

Patent Owner's “Prevents” Argument



(Kawagoe at FIG. 16; IPR2024-00468, Reply at 21)

from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E. Thus, the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p. The impurity concentration N_w in the principal surface of the epitaxial layer 2E of the p-well 6p and the n-well 6n is at about 6×10^{16} atoms/cm³, so that the impurity concentration of the p-well 6p and the n-well 6n is at 5×10^{15} to 6×10^{16} atoms/cm³.

(Kawagoe at 16:1-15; IPR2024-00468, Reply at 20-21)

Patent Owner's prevent argument – defies logic

Finally, PO's arguments defy common sense. PO argues that the prior art prevents upward movement. Logically, if electron movement is prevented upwards, there are two positional options: (1) not allowed to move; or (2) pushed downwards. Locking the electron in place requires that all net-forces be finely tuned to "0." This—which PO appears to argue—is an impractical scenario. The Nishizawa and Kawagoe electrons' movements would be aided downward.
(EX1054, ¶¶6-7.)

(IPR2024-00468, Reply at 13, 22)

Patent Owner's prevent argument – defies logic

6. I further note that, if a graded dopant concentration exists, it will cause carrier drift. Dr. Glew states that Nishizawa and Kawagoe teach preventing upward movement of electrons, as opposed to aiding their movement downwards. This is wrong and defies logic.

7. Once an electron is generated via alpha rays in Nishizawa and Kawagoe, it will be affected by the drift field created by their respective graded dopant concentrations. This is a downward force to cause electrons to drift downwards. To state that the references teach only preventing upward movement and they do not drift electrons downwards (as Dr. Glew does) effectively means that electrons must be locked in place. This is highly impractical because to accomplish this, a specific upward force would need to be introduced into the device to precisely counteract the one introduced by the dopant gradient. This is not described in Nishizawa and Kawagoe and, moreover, defies logic as it would be impossible (and pointless) to design a force to exactly counteract that introduced by the graded dopant concentration. When a graded concentration prevents upward movement, a POSITA would understand that it causes a downward drift of electrons.

(IPR2024-00468, Reply at 22; EX1054 at ¶ 6-7)

Greenthread's all-force-calculation premise is faulty

Greenthread's all-force argument is wrong

Patent Owner's "force"	Reply
Resistance	Increases/decreases speed of movement equally in all directions (EX1055, 77:11-23, 79:15-81:5)
Temperature	Increases/decreases speed of movement equally in all directions (EX1055, 77:11-23, 79:15-81:5)
Imperfections	Would typically be uniform and non-impactful (EX1055, 77:11-23, 79:15-81:5)
PN Junction	P-N junction capacitance exists in every P-N junction, including those junctions disclosed in the '195 Patent. Moreover, the field effect from the P-N junctions requires an applied voltage for electrons to flow. (EX2058, 35:10-17; EX1059, 18-20)

Intrinsic resistance, silicon stress, and temperature do not preclude movement of carriers

Dr. Glew

Q. In your opinion, does resistance impart a force into a semiconductor device?

A. I'm sorry. Does what impart force?

Q. A device's resistance.

A. One can think of resistance as an opposing or impeding force against current flow. So the more resistance, the less current flows given the same voltage potential. At an infinite resistance, a voltage causes no current flow. At a very low resistance that same voltage could cause high current flow. It's not a force in the Newtonian sense, but we're using the term force as sort of a resisting force against current flow.

(IPR2024-00468, Reply at 15; EX1055 at 77:11-23)

Dr. Glew

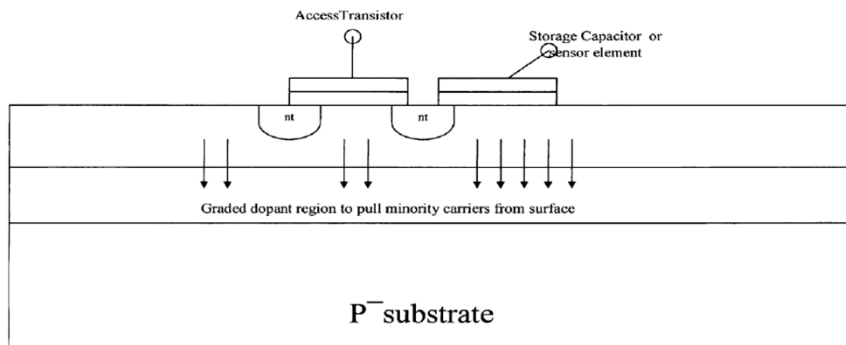
Q. Would a certain temperature value -- actually, I'll take that back. In the Newtonian sense, does temperature impart a force that would move an electron backwards or forwards in space?

A. Well, the temperature does two things. One, it impedes the motion by the expansion or contraction of the silicon crystal. So it makes it harder for it to move, or easier. Also, it creates stress fields around any of the impurities. So phosphorous, for example, and Boron have different sizes than the silicon crystal lattice. They also are affected by temperature.

Imperfections also have affected by expansion, thermal expansion. These are drag, essentially, on current.

(IPR2024-00468, Reply at 15; EX1055 at 81:6-20)

P-N Junction Capacitance—No Consideration



(EX1001 at FIG. 5(b))

The Office Action also states that “such a unidirectional drift field may attempt to apply a force on all minority carriers in a specific direction, it does not appear to ensure (without knowing other parameters of the device) that it will draw ‘all’ minority carriers...” Yet, this argument appears to not consider that the graded dopant concentration itself creates a “built-in” electrical field that forces the movement of carriers into a particular direction, whereby the “direction” of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant. With regard to the existence of a “built-in” electric field created by a graded dopant density, *see*, e.g., Jastrzebski (US 4,481,522) col. 5, lines 11-13 (cited in Office Action). Applicant respectfully submits that this inherent “built-in” unidirectional electric field is the additional parameter for ensuring that all minority carriers are being moved in one direction and which parameter the Office Action deemed to be missing from the disclosure.

(IPR2024-00468 (EX1002 at 289-290); Reply at 5-6)

P-N Junction Capacitance—Applied Voltage

Dr. Campbell

Q. Do capacitants affect impact carrier movement?

A. Could you explain what you mean by capacitance effects?

Q. What -- what's is your understanding of the term capacitance effects?

A. It is s too broad for me to say.

I would say you're talking about a capacitor, and where I have two plates and an insulator of some kind between, and we create an electric field and put the voltage across those two points.

(IPR2024-00468 (EX2058 at 35:10-17); Reply at 16)

Patent Owner's Evidence

U.S. Pat. No. 8,704,292

and linearly graded in between. Such a graded doping profile, in combination with the capacitive depletion effect of the gate and insulator regions, may provide a substantially uniform electric field within the drift region. The solid line in FIG. 5

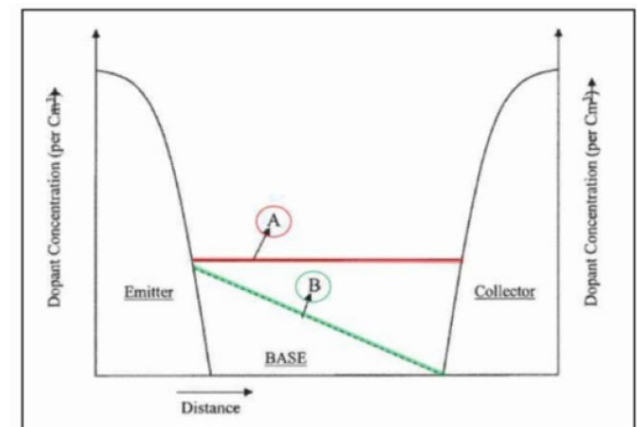
(IPR2024-00468 (EX2030 at 35:10-17); Reply at 16))

Inconsistent with intrinsic evidence

Specification: aiding carrier movement does not hinge on a specific magnitude of the gradient

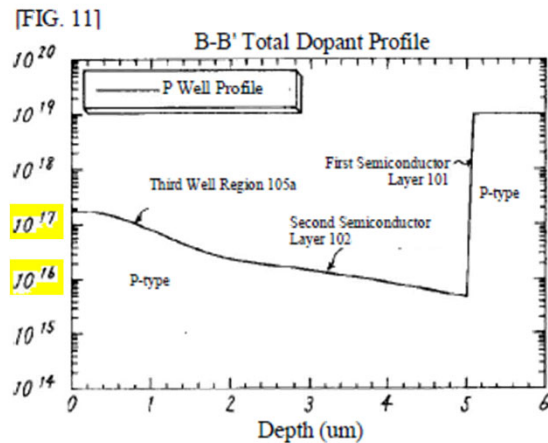
The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complementary error function. The relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

(IPR2024-00468, EX1001 at 2:35-50)



(IPR2024-00468, EX1001 at 2-3)

Prior art teaches slopes



50 the direction toward the p type substrate 11. For example, the impurity concentration of that portion of the p⁺ type buried region 33a located adjacent the channel region and the n⁺ type region 13 is set at about 1×10^{17} cm⁻³, with progressively lowered concentration as the

cm⁻³. However, it is also effective to arrange this impurity concentration of the semiconductor substrate 11 at a low level such as about 1×10^{15} cm⁻³ or about 1×10^{14} cm⁻³, and also to arrange the impurity concen-

layer 2E of the p-well 6p and the n-well 6n is at about 6×10^{16}

500 to 800 μm, for example. The semiconductor substrate body 2S is doped with a p-type impurity such as boron (B) in a concentration of about 1.3×10^{15} atoms/cm³.

(Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; IPR2024-00468, Reply at 13)

Inconsistent with prosecution history

Prosecution history: applicant urged that no other “forces and fields” need to be analyzed to satisfy the claims

The Office Action maintains a rejection pursuant to 35 U.S.C. §112, first paragraph, and in particular states that, because “movement of minority carriers is affected by multiple forces and fields ... it does not appear that simply the presence of ‘a unidirectional drift field’ in itself can achieve ‘drawing all minority carriers from said surface layer to said substrate.’” Office Action at ¶3.

(EX1002 at 289-290; IPR2024-00468, Reply at 6)

Prosecution history: applicant urged that no other “forces and fields” need to be analyzed to satisfy the claims

Applicant respectfully disagrees with this position because (as previously argued by Applicant) a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way – moving all minority carriers in the same direction because of the unidirectional drift due to the existence of the electric field. *See* “Physics and Technology of Semiconductor Devices,” A.S. Grove, pp. 224-225, John Wiley and Sons, Inc., New York, 1st Edition 1967 (“This same electric field will then be of such direction as to aid the motion of injected holes. Thus the injected minority carriers will now move not only by diffusion but also by drift due to the existence of this electric field.”). Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept “down” (from the surface layer to the substrate) or “up” (from the substrate to the surface layer). *See* Applicant’s Figs. 5(b) and 5(c).

(EX1002 at 289; IPR2024-00468, Reply at 9)

Inconsistent with litigation stance

Greenthread's present arguments on “aid carrier movement” are inconsistent with its litigation positions

layer to said substrate” or similar language in other claims. “To aid the movement” is a simple term that is readily understood by POSITAs and lay persons alike. Ex. 1, ¶85. Any one that has put a little WD40 on a rusty hinge, or stretched before exercising, knows what it means “to aid the movement” of something. Likewise, nobody would dispute that a wheelchair ramp “aids the movement” of someone in a wheelchair.

(EX1030 at 25; IPR2024-00468, Reply at 4)

drift layer with graded dopants that create a particular type of electric field. By the time the claim gets to the phrase “to aid movement,” it is merely clarifying what the electric field does. Any question about what is meant by “to aid the movement” is answered by the preceding claim language. Electric drift fields are a well-known phenomenon that cause carriers to move, and a POSITA would have readily recognized that when a “static unidirectional electric drift field” is present that it aids the movement of the minority carriers. If it isn't present, then it doesn't. The

(EX1030 at 26; IPR2024-00468, Reply at 4)

a particular doping profile, or a particular result. But this is not the test for indefiniteness. While the claims require that the graded dopants create an electric field that aids movement of the carriers, they do not require a specific range of doping, a particular doping field, or a particular result, and this information is not necessary to understand the scope of Dr. Rao's invention.

(EX1030 at 28; IPR2024-00468, Reply at 4-5)

Greenthread's present arguments on "aid carrier movement" are inconsistent with its litigation positions

W.D. Tex – Dealt with Indefiniteness

D. Term #4: "graded dopant concentration" / "graded dopant region" / "graded dopant acceptor concentration" / "graded donor dopant concentration" / "graded concentration of dopants" / "graded dopant" / "graded concentration"		
Term	Greenthread's Proposed Construction	Cirrus's Proposed Construction
#4: "graded dopant concentration" / "graded dopant region" / "graded dopant acceptor concentration" / "graded donor dopant concentration" / "graded concentration of dopants" / "graded dopant" / "graded concentration"	Not indefinite. Plain and ordinary meaning, where the plain and ordinary meaning is a graded (or varying) concentration of dopants.	Indefinite
U.S. Patent No. 8,421,195, Claims 1, 5, 6; U.S. Patent No. 9,190,502, Claim 7; U.S. Patent No. 10,510,842, Claims 1, 6, 8–9, 14, 16; U.S. Patent No. 10,734,481, Claims 1, 5, 7, 9, 20, 25, 27, 31; U.S. Patent No. 11,121,222, Claims 1, 5, 7, 9, 21, 26, 28, 32, 39–42, 44 Proposed by Cirrus		

(EX2074 at 32; IPR2024-00468, Reply at 3)

Patent Owner Argued Definite

In its sur-reply, Greenthread contends that the intrinsic evidence provides sufficient guidance about the scope of the claim. Sur-Reply (ECF No. 39) at 6. More specifically, Greenthread contends that the claims specify that the graded dopants generate an electric field that aids in the movement of minority carriers. *Id.* at 7. Greenthread contends that Figure 1 in the '195 Patent depicts the difference between uniform and graded concentration, namely, that the concentration in the former is the same across a region while in the latter, the concentration has a slope. *Id.*

(EX2074 at 38; IPR2024-00468, Reply at 4)

Slide: 68

Petitioner's Demonstratives – IPR2024-00468-00470 and 00550-00553



Greenthread's present arguments on “aid carrier movement” are inconsistent with its litigation positions

W.D. Tex – Court Found it Definite

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Greenthread that the term is not indefinite for the reasons that follow. First, the specification provides some guidance as to the meaning of this claim term. For example, Figure 1 depicts a graded doping concentration of the base in a bipolar junction transistor. This figure shows that, in contrast, to a “uniform” doping concentration, the graded doping concentration has a linearly decreasing doping concentration from the emitter-side to the collector-side of the base.¹ The specification also provides a numerical example of what constitutes a graded dopant concentration. *See, e.g.*, '195 Patent at 2:38–4 (“n graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (IX).”).

(EX2074 at 39; IPR2024-00468, Reply at 4)

Greenthread mischaracterizes EDTX claim construction order

A. “single drift layer . . . having a graded concentration of dopants [. . . said drift layer further having / generating] a first static unidirectional electric drift field”		
Disputed Term	Plaintiff’s Proposed Construction	Defendants’ Proposed Construction
“single drift layer . . . having a graded concentration of dopants . . . said drift layer further having a first static unidirectional electric drift field” • ’195 Patent Claim 1	no construction necessary	single layer whose concentration of dopants either increases across the layer or decreases across the layer
“single drift layer . . . having a graded concentration of dopants generating a first static unidirectional electric drift field” • ’502 Patent Claim 7		

(EX2075 at 10; IPR2024-00468, Reply at 4)

“electric drift field,” not to the “graded concentration of dopants.” The slope of the graded concentration need not be solely decreasing or solely increasing to yield the recited “unidirectional electric drift field.” Further, the claims allow for more than one “unidirectional electric drift field”

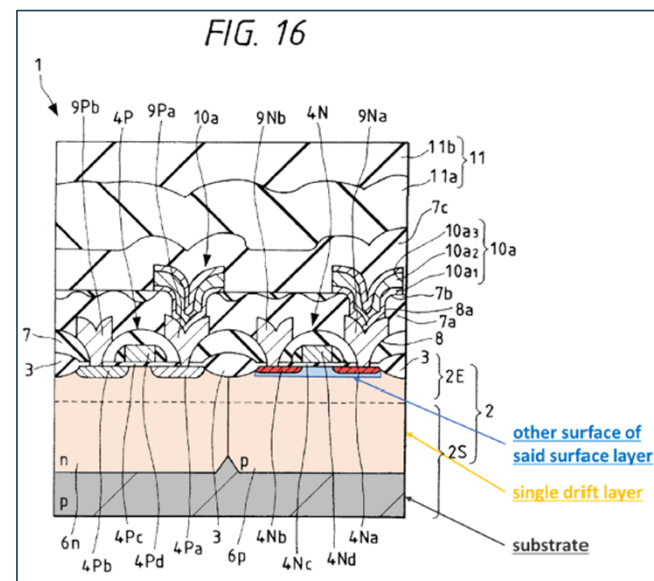
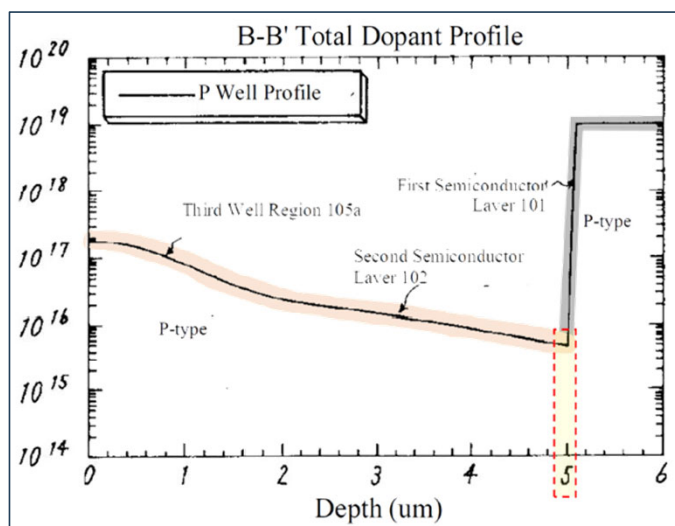
(EX2075 at 11; IPR2024-00468, Reply at 4)

Greenthread's Sur-Reply

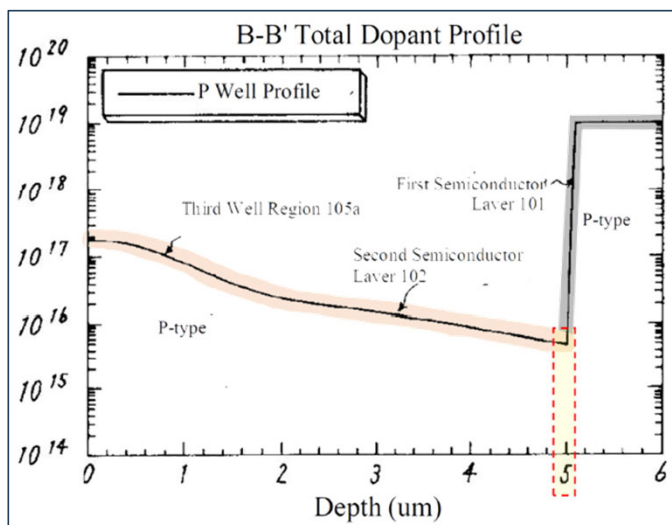
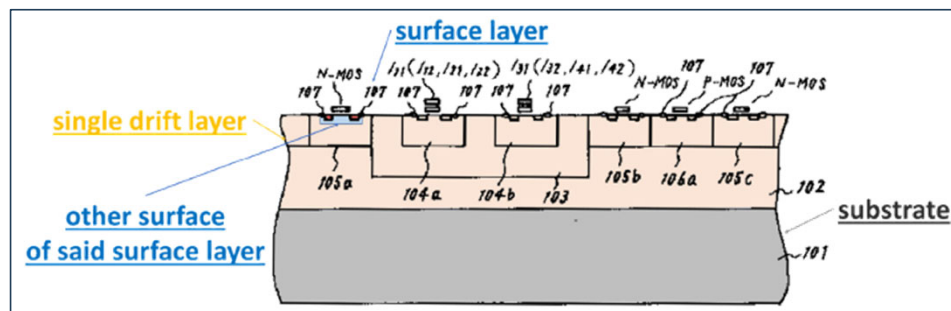
Greenthread's “minority carrier” argument

Minority carrier: “a hole in an n-type or an electron in a p-type semiconductor.” (EX1056; *see also* EX1057, EX1058.)

(Reply at 24)



Greenthread's "surface layer" not size limited



(Onoda at Figs. 3, 11)

8 Q. The '195 patent, Exhibit 1001, if you could
9 look at column 4, line 14 that says, "a surface
10 layer."
11 A. I see that.
12 Q. Is the surface layer limited in size?
13 A. I'm a little unclear on your question.
14 These are very small devices. They don't have sizes.
15 Q. Is a specific sizing requirement included
16 in the limitation of a surface layer?
17 MR. WHITEHURST: Object to form.
18 THE WITNESS: The limitations describe some
19 of what's in the surface layer. It doesn't limit it
20 to a certain size beyond being inclusive of those
21 elements.

(EX1055 at 186:8-12; IPR2024-00468, Reply at 19)

Greenthread fails to demonstrate secondary considerations

Evidence of nexus is required for license agreements as secondary considerations

“[T]he fact that a patent has been licensed, taken alone, generally is insufficient for purposes of showing commercial success.”

*(Intron Networked Sols., Inc. v. Acoustic Tech., Inc., No. IPR20170-01031, 2018 WL 10440326, at *10 (P.T.A.B. Aug. 21, 2018))*

We “specifically require affirmative evidence of nexus . . . because it is ‘often cheaper to take licenses than to defend infringement suits.’”

(Iron Grip Barbell Co. v. USA Sports, Inc., 392 F.3d 1317, 1324 (Fed. Cir. 2004) (cit. omitted))

Litigation settlements are not objective evidence of non obviousness

Greenthread's Response:

Finally, licenses that are part of litigation settlements can also be probative of non-obviousness. ***Fox Factory Inc. v. SRAM LLC*, IPR2017-00472, Paper 64 at 44 (PTAB April 18, 2018).**

('195 POR at 29; '502 POR at 29; '222 POR at 29)

The Federal Circuit vacated this *Fox Factory* decision because “the Board **erroneously presumed nexus** between the evidence of secondary considerations and the independent claims.”

(*Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1378 (Fed. Cir. 2019))

On remand, the Board ultimately found **all challenged claims unpatentable**, concluding that “at best, Patent Owner shows a *weak nexus*” for licenses mentioning the challenged patent and “*no nexus* with respect to the remaining licenses” that did not.

(*Fox Factory, Inc. v. SRAM, LLC*, IPR2017-00472, Paper 74, 11, 14-15 (P.T.A.B. Feb. 25, 2021))

RPX's involvement shows licenses were motivated by litigation costs



FAQs

We are a unique solution to all forms of patent risk

Only RPX has the scale and independence to efficiently acquire patent portfolios pre-litigation and out of active litigation. Only RPX can spread the cost of reducing patent litigation across a large network of participating companies. Only RPX has accurate litigation cost data and a proven actuarial model to provide affordable, comprehensive patent litigation insurance. And only RPX can deliver – to companies of any size and with a patent litigation problem of any severity – significant, quantifiable, and cost-effective reduction of risk.

We provide compelling cost savings

RPX's interests are 100% aligned with those of our clients. We work to ensure that each RPX client avoids more in legal costs and settlements each year than they pay RPX in subscription fees. We quantify the cost savings we have delivered collaboratively with the client. Together, we review the RPX acquisitions relevant to the client and determine a specific "avoided cost". The cumulative avoided cost is applied against the client's annual fee to calculate the dollar savings we have delivered for the year. We have been very successful delivering cost savings to all of the members in our network, a key factor in our consistently strong annual renewal rate.

(Ex. 1060 (RPX FAQs))

Petitioner's expert Dr. Campbell is more reliable than Greenthread's
expert Dr. Glew

Petitioner's expert has only provided expert opinion in one other litigation

8. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than

(Ex. 1003 (Campbell Dec.) at 7)

Consulting

2019-2021

2008:

2005-2007

2004-2005:

2003-2004:

1997-2000:

1997

1994-96

1991-93

1992, 94

1989-92

Wilmer-Hale, Advanced CMOS Litigation

3M, Optoelectronic Devices

CIMA Nanotech: Nanoparticle materials

Precision Press: Thin film devices

Ennovato, Inc. A startup working on novel transistors for thin film displays

Offered IC fabrication short courses through UC Berkeley and independently

Fusion Semiconductor Developed a design for radiative heating of 300 mm wafers.

FSI Corporation Studied effects of wafer cleaning steps on gate oxide quality

AG Associates, Modeling and design of rapid thermal processing equipment.

National Science Board, Naval Studies Board (JAST)

Institute for Defense Analysis Participant, Defense Sciences Study Group

(Ex. 1004 (Campbell CV) at 2)

Greenthread's expert has worked on countless litigations and Inter Partes Reviews for Greenthread

- Greenthread's expert repeatedly took positions that contradict the prior art's plain wording.

(See, e.g., Ex. 1055 (Glew Depo.) at 116:19-120:19)

- He filibustered, was evasive, and refused to answer simple questions.

(See, e.g., Ex. 1055 (Glew Depo.) at 106:8-109:21, 127:6-128:12, 129:19-130:7, 130:25-131:22, 133:19-138:11)

Citations

Slide Number	468	469	470	550	551	552	553
5			IPR2023-01244, Final Written Decision, paper 84 at 59	IPR2023-01243, Final Written Decision, Paper 83 at 55; IPR2024-00016, Final Written Decision, Paper 74 at 66	IPR2024-00001, Final Written Decision, Paper 78 at 80	IPR2023-01242, Final Written Decision, Paper 85 at 72	
6	Ex. 1003 at ¶ 23	Ex. 1003 at ¶ 23	Ex. 1003 at ¶ 23				
7				Ex. 1003 at App. B	Ex. 1003 at App. B	Ex. 1003 at App. B	Ex. 1003 at App. B
10	Paper 69 (Discovery Order) at 6–7; Paper 77 (Responsive Supplemental Brief) at 3–4	Paper 69 (Discovery Order) at 6–7; Paper 78 (Responsive Supplemental Brief) at 3–4	Paper 69 (Discovery Order) at 6–7; Paper 77 (Responsive Supplemental Brief) at 3–4	Paper 69 (Discovery Order) at 6–7; Paper 66 (Responsive Supplemental Brief) at 3–4	Paper 69 (Discovery Order) at 6–7; Paper 68 (Responsive Supplemental Brief) at 3–4	Paper 69 (Discovery Order) at 6–7; Paper 67 (Responsive Supplemental Brief) at 3–4	Paper 69 (Discovery Order) at 6–7; Paper 67 (Responsive Supplemental Brief) at 3–4
11	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12	EX2086 (Summers Decl.) at ¶¶ 6–8, 10, 12
12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12	Responsive Supplemental Brief at 9, 9–10, 10–11, 11–12

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13	Responsive Supplemental Brief at 13, 15, 14	Responsive Supplemental Brief at 13, 15, 14	Responsive Supplemental Brief at 13, 15, 14	Responsive Supplemental Brief at 13, 15, 14	Responsive Supplemental Brief at 13, 15, 14	Responsive Supplemental Brief at 13, 15, 14	Responsive Supplemental Brief at 13, 15, 14
15	Onada (EX1042) at Object	Onada (EX1042) at Object	Onada (EX1042) at Object	Onada (EX1042) at Object	Onada (EX1042) at Object	Onada (EX1042) at Object	Onada (EX1042) at Object
16	Paper 1 (Pet.) at 30 (citing Onoda at FIG. 8); Pet. at 31 (citing Onoda at FIG. 11)	Paper 1 (Pet.) at 31 (citing Onoda at FIG. 8); Pet. at 31 (citing Onoda at FIG. 11)	Paper 1 (Pet.) at 32 (citing Onoda at FIG. 8); Pet. at 33 (citing Onoda at FIG. 11)	Paper 1 (Pet.) at 49-50 (citing Onoda at FIG. 8); Pet. at 49-50 (citing Onoda at FIG. 11)	Paper 1 (Pet.) at 54-55 (citing Onoda at FIG. 8); Pet. at 54-55 (citing Onoda at FIG. 11)	Paper 1 (Pet.) at 55-56 (citing Onoda at FIG. 8); Pet. at 55-56 (citing Onoda at FIG. 11)	Paper 1 (Pet.) at 53-54 (citing Onoda at FIG. 8); Pet. at 54-54 (citing Onoda at FIG. 11)
17	Pet. at 25 (citing Onoda at FIG. 3)	Pet. at 24 (citing Onoda at FIG. 3)	Pet. at 27 (citing Onoda at FIG. 3)	Pet. at 41-46 (citing Onoda at FIG. 3)	Pet. at 46-50 (citing Onoda at FIG. 3)	Pet. at 48-51 (citing Onoda at FIG. 3)	Pet. at 46-49 (citing Onoda at FIG. 3)
18	Pet. at 29 (citing Onoda at FIG. 3)	Pet. at 29 (citing Onoda at FIG. 8)	Pet. at 31 (citing Onoda at FIG. 8)	Pet. at 42 (citing Onoda at FIG. 3)	Pet. at 47 (citing Onoda at FIG. 3)	Pet. at 48 (citing Onoda at FIG. 3)	Pet. at 46 (citing Onoda at FIG. 3)
19	Pet. at 31 (citing Onoda at FIG. 11)	Pet. at 31 (citing Onoda at FIG. 11)	Pet. at 33 (citing Onoda at FIG. 11)	Pet. at 52 (citing Onoda at FIG. 11)	Pet. at 56 (citing Onoda at FIG. 11)	Pet. at 57 (citing Onoda at FIG. 11)	Pet. at 55 (citing Onoda at FIG. 11)
20	Pet. at 33 (citing Onoda at FIG. 8)	Pet. at 33 (citing Onoda at FIG. 8)	Pet. at 33 (citing Onoda at FIG. 8)	Pet. at 50 (citing Onoda at FIG. 8)	Pet. at 55 (citing Onoda at FIG. 8)	Pet. at 56 (citing Onoda at FIG. 8)	Pet. at 54 (citing Onoda at FIG. 8)

Citations

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21	EX1002 at 269; EX1002 at 270; Reply at 5-6	EX1002 at 269; EX1002 at 270; Reply at 5-6	EX1002 at 269; EX1002 at 270; Reply at 5-6	EX1002 at 269; EX1002 at 270; Reply at 5	EX1002 at 269; EX1002 at 270; Reply at 5	EX1002 at 269; EX1002 at 270; Reply at 5	EX1002 at 269; EX1002 at 270; Reply at 5
22	EX1002 at 333; Paper 42 (Reply) at 7; EX1009 at FIG. 3; Petition at 12; EX1009 at 3:8-10; Reply at 7; Petition at 12	EX1002 at 333; Paper 42 (Reply) at 7; EX1009 at FIG. 3; Petition at 12; EX1009 at 3:8-10; Reply at 7; Petition at 12	EX1002 at 333; Paper 42 (Reply) at 7; EX1009 at FIG. 3; Petition at 12; EX1009 at 3:8-10; Reply at 7; Petition at 12	EX1002 at 333; Paper 36 (Reply) at 6; EX1009 at FIG. 3; Petition at 10; EX1009 at 3:8-10; Reply at 6; Petition at 11	EX1002 at 333; Paper 38 (Reply) at 6; EX1009 at FIG. 3; Petition at 10; EX1009 at 3:8-10; Reply at 6; Petition at 13	EX1002 at 333; Paper 38 (Reply) at 6; EX1009 at FIG. 3; Petition at 10; EX1009 at 3:8-10; Reply at 6; Petition at 16	EX1002 at 333; Paper 37 (Reply) at 6; EX1009 at FIG. 3; Petition at 10; EX1009 at 3:8-10; Reply at 6; Petition at 14
23	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 11	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 11	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 11	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 10	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 13	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 16	EX1002 at 290; Reply at 7; EX1010 at FIG. 1a, 1b; Petition at 13
24	EX1030 at 2; Reply at 4, 14	EX1030 at 2; Reply at 4, 14	EX1030 at 2; Reply at 4, 14	EX1030 at 2; Reply at 7, 14	EX1030 at 2; Reply at 7, 14	EX1030 at 2; Reply at 7, 14	EX1030 at 2; Reply at 7, 14
25	EX1030 at 26-27; Reply at 4	EX1030 at 26-27; Reply at 4	EX1030 at 26-27; Reply at 4	EX1030 at 26-27; Reply at 7	EX1030 at 26-27; Reply at 7	EX1030 at 26-27; Reply at 7	EX1030 at 26-27; Reply at 7
26	EX1030 at 27; Reply at 11-12; Onoda at Fig. 11; Reply at 12	EX1030 at 27; Reply at 11-12; Onoda at Fig. 11; Reply at 12	EX1030 at 27; Reply at 11-12; Onoda at Fig. 11; Reply at 12	EX1030 at 27; Reply at 11; Onoda at Fig. 11; Reply at 11	EX1030 at 27; Reply at 11; Onoda at Fig. 11; Reply at 11	EX1030 at 27; Reply at 11; Onoda at Fig. 11; Reply at 11	EX1030 at 27; Reply at 11; Onoda at Fig. 11; Reply at 11
27	Onoda at Fig. 11; Pet. at 37	Onoda at Fig. 11; Pet. 37	Onoda at Fig. 11; Pet. 37	Onoda at Fig. 11; Pet. at 51-56	Onoda at Fig. 11; Pet. at 55-60	Onoda at Fig. 11; Pet. at 55-61	Onoda at Fig. 11; Pet. at 54-59

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28	Onoda at Fig. 3; Pet. 35; Onoda at Fig. 11; Pet. 37	Onoda at Fig. 3; Pet. 35; Onoda at Fig. 11; Pet. 37	Onoda at Fig. 3; Pet. 35; Onoda at Fig. 11; Pet. 37				
29				Onoda at Fig. 3; Pet. at 51; Onoda at Fig. 11; Pet. at 55	Onoda at Fig. 3; Pet. at 56; Onoda at Fig. 11; Pet. at 59	Onoda at Fig. 3; Pet. at 57; Onoda at Fig. 11; Pet. at 60	Onoda at Fig. 3; Pet. at 55; Onoda at Fig. 11; Pet. at 58
30	Pet. at 48; Pet. at 50	Pet. at 48; Pet. at 50	Pet. at 45; Pet. at 47				
31				Pet. at 73	Pet. at 80-81	Pet. at 84	Pet. at 79-80
32	EX1046 (Nishizawa) at 18:35-68; Pet. at 50-51, Reply at 18; Nishizawa at FIG. 35; Reply at 19	EX1046 (Nishizawa) at 18:35-68; Petition at 47-48, Reply at 18	EX1046 (Nishizawa) at 18:35-68; Petition at 46-47, Reply at 18	EX1046 (Nishizawa) at 18:35-68; Pet. at 73-75, Reply at 19; Nishizawa at FIG. 35; Reply at 20	EX1046 (Nishizawa) at 18:35-68; Pet. at 84-85, Reply at 19; Nishizawa at FIG. 35; Reply at 20	EX1046 (Nishizawa) at 18:35-68; Pet. at 80-81, Reply at 19; Nishizawa at FIG. 35; Reply at 20	EX1046 (Nishizawa) at 18:35-68; Pet. at 73-75, Reply at 19; Nishizawa at FIG. 35; Reply at 20
33	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 18, 19	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 18	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 18	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 19-20	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 19-20	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 19-20	Nishizawa at 18:5-7; Nishizawa at 18:18-22; Nishizawa at 18:35-42; Nishizawa at FIG. 35; Reply at 19-20
34	EX1007 (Kawagoe) at 16:2-11; Pet. 64; Kawagoe at FIGS. 16 and 17; Pet. 66	EX1007 (Kawagoe) at 16:2-11; Pet. 49-50; Kawagoe at FIGS. 16 and 17; Pet. 74	EX1007 (Kawagoe) at 16:2-11; Pet. 49; Kawagoe at FIGS. 16 and 17; Pet. 61	EX1007 (Kawagoe) at 16:2-11; Pet. at 22; Kawagoe at FIGS. 16 and 17; Pet. at 24-25	EX1007 (Kawagoe) at 16:2-11; Pet. at 25; Kawagoe at FIGS. 16 and 17; Pet. at 27	EX1007 (Kawagoe) at 16:2-11; Pet. at 26; Kawagoe at FIGS. 16 and 17; Pet. at 27-28	EX1007 (Kawagoe) at 16:2-11; Pet. at 24; Kawagoe at FIGS. 16 and 17; Pet. at 26

Citations

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35	Kawagoe at FIG. 16; Pet. 60	Kawagoe at FIG. 16; Pet. 60	Kawagoe at FIG. 16; Pet. 55	Kawagoe at FIG. 16; Pet. at 16	Kawagoe at FIG. 16; Pet. at 19	Kawagoe at FIG. 16; Pet. at 19	Kawagoe at FIG. 16; Pet. at 18
36	Kawagoe at FIG. 16; Pet. 64	Kawagoe at FIG. 16; Pet. 64	Kawagoe at FIG. 16; Pet. 59	Kawagoe at FIG. 16; Pet. at 25	Kawagoe at FIG. 16; Pet. at 27	Kawagoe at FIG. 16; Pet. at 28	Kawagoe at FIG. 16; Pet. at 26
37	Kawagoe at FIGS. 16 and 17; Pet. 66	Kawagoe at FIGS. 16 and 17; Pet. 66	Kawagoe at FIGS. 16 and 17; Pet. 61	Kawagoe at FIGS. 16 and 17; Pet. at 24-25	Kawagoe at FIGS. 16 and 17; Pet. at 27	Kawagoe at FIGS. 16 and 17; Pet. at 27-28	Kawagoe at FIGS. 16 and 17; Pet. at 26
38	Kawagoe at 16:18-11; Pet. at 64	Kawagoe at 16:18-11; Pet. at 64	Kawagoe at 16:18-11; Pet. at 64	Kawagoe at FIG. 16; Pet. at 23	Kawagoe at FIG. 16; Pet. at 25	Kawagoe at FIG. 16; Pet. at 26	Kawagoe at FIG. 16; Pet. at 24
39	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 124; Pet. at 75, 77	Kawagoe at FIGS. 16 and 17; Ex. 1003 at 124; Pet. 75, 77	Kawagoe at FIGS. 16 and 17; Ex. 1003 at 124; Pet. 73	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 24-26	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 27-28	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 27-28	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 26-27
40	Kawagoe at FIGS. 16 and 17; Ex. 1003 at 124; Pet. 75, 77	Kawagoe at FIGS. 16 and 17; Ex. 1003 at 124; Pet. 75, 77	Kawagoe at FIGS. 16 and 17; Ex. 1003 at 124; Pet. 73	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 24-26	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 27-28	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 27-28	Kawagoe at FIGS. 16 and 17; Ex. 1003 at ¶ 174; Pet. at 26-27
41	Paper 23 (Decision) at 6	Paper 24 (Decision) at 9	Paper 22 (Decision) at 7	Paper 20 (Decision) at 21	Paper 22 (Decision) at 19	Paper 26 (Decision) at 20	Paper 25 (Decision) at 8
43	Reply 2-3 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))	Reply 2-3 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))	Reply 2-3 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))	Reply 3-4 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))	Reply 3-4 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))	Reply 3-4 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))	Reply 3-4 (citing ParkerVision, Inc. v. Qualcomm Inc., 903 F.3d 1354, 1361 (Fed. Cir. 2018))

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45	Kawagoe at FIGS. 16 and 17; Pet. 72	Kawagoe at FIGS. 16 and 17; Pet. 68	Kawagoe at FIGS. 16 and 17; Pet. 67	Kawagoe at FIGS. 16 and 17; Pet. at 23-25	Kawagoe at FIGS. 16 and 17; Pet. 26-28	Kawagoe at FIGS. 16 and 17; Pet. 26-28	Kawagoe at FIGS. 16 and 17; Pet. 25-27
45	Onoda at FIGS. 3 and 11; Petition at 35 and 37	Onoda at FIGS. 3 and 11; Petition at 35 and 37	Onoda at FIGS. 3 and 11; Petition at 37 and 39	Onoda at FIGS. 3 and 11; Pet. at 51-52	Onoda at FIGS. 3 and 11; Pet. at 55-56	Onoda at FIGS. 3 and 11; Pet. at 55-57	Onoda at FIGS. 3 and 11; Pet. at 54-55
47	Ex. 1030 at 25, 27-28; Reply 11	Ex. 1030 at 25, 27-28; Reply 11	Ex. 1030 at 25, 27-28; Reply 11	Ex. 1030 at 25, 27-28; Reply 11	Ex. 1030 at 25, 27-28; Reply 11	Ex. 1030 at 25, 27-28; Reply 11	Ex. 1030 at 25, 27-28; Reply 11
49	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 12	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 12	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 12	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 11	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 11	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 11	Onoda at FIG. 11 and Kawagoe at FIG. 16; Reply at 11
50	Nishizawa at 17:12-18; Reply at 19-20; Nishizawa at FIG. 36; Reply at 19-20	Nishizawa at 17:12-18; Reply at 19-20; Nishizawa at FIG. 36; Reply at 19-20	Nishizawa at 17:12-18; Reply at 19-20; Nishizawa at FIG. 36; Reply at 19-20	Nishizawa at 17:12-18; Reply at 20-21; Nishizawa at FIG. 36; Reply at 20-21	Nishizawa at 17:12-18; Reply at 20-21; Nishizawa at FIG. 36; Reply at 20-21	Nishizawa at 17:12-18; Reply at 20-21; Nishizawa at FIG. 36; Reply at 20-21	Nishizawa at 17:12-18; Reply at 20-21; Nishizawa at FIG. 36; Reply at 20-21

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52	Reply at 13, 22	Reply at 13, 22	Reply at 13, 22	Reply at 12, 17	Reply at 12, 17	Reply at 12, 17	Reply at 12, 17
53	Reply at 22; EX1054 at ¶ 6-7	Reply at 22; EX1054 at ¶ 6-7	Reply at 22; EX1054 at ¶ 6-7	Reply at 17; EX1054 at ¶ 6-7	Reply at 17; EX1054 at ¶ 6-7	Reply at 17; EX1054 at ¶ 6-7	Reply at 17; EX1054 at ¶ 6-7
56	Reply at 15; EX1055 at 77:11-23; EX1055 at 81:6-20	Reply at 15; EX1055 at 77:11-23; EX1055 at 81:6-20	Reply at 15; EX1055 at 77:11-23; EX1055 at 81:6-20	Reply at 14; EX1055 at 77:11-23; EX1055 at 81:6-20	Reply at 14; EX1055 at 77:11-23; EX1055 at 81:6-20	Reply at 14; EX1055 at 77:11-23; EX1055 at 81:6-20	Reply at 14; EX1055 at 77:11-23; EX1055 at 81:6-20
57	EX1001 at Fig. 5b	EX1001 at Fig. 5b	EX1001 at Fig. 5b	EX1001 at Fig. 5b	EX1001 at Fig. 5b	EX1001 at Fig. 5b	EX1001 at Fig. 5b
57	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6
58	EX2058 at 35:10-17; Reply at 16	EX2058 at 35:10-17; Reply at 16	EX2058 at 35:10-17; Reply at 16	EX2058 at 35:10-17; Reply at 15	EX2058 at 35:10-17; Reply at 15	EX2058 at 35:10-17; Reply at 15	EX2058 at 35:10-17; Reply at 15
59	EX2058 at 35:10-17; Reply at 16	EX2058 at 35:10-17; Reply at 16	EX2058 at 35:10-17; Reply at 16	EX2058 at 35:10-17; Reply at 15	EX2058 at 35:10-17; Reply at 15	EX2058 at 35:10-17; Reply at 15	EX2058 at 35:10-17; Reply at 15
61	EX1001 at 2:35-50	EX1001 at 2:39-54	EX1001 at 2:54-3:3	EX1001 at 2:62-3:11	EX1001 at 2:66-3:15	EX1001 at 2:54-3:3	EX1001 at 2:66-3:15

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61	EX1001 at 2-3	EX1001 at 2-3	EX1001 at 2-3	EX1001 at 2-3	EX1001 at 2-3	EX1001 at 2-3	EX1001 at 2-3
62	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 13	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 13	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 13	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 12-13	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 12-13	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 12-13	Onoda at Fig. 11; Nishizawa at 18:50-54, 18:64; Kawagoe at 16:13, 6:62-64; Reply at 12-13
64	EX1002 at 289-290; Reply at 6	EX1002 at 289-290; Reply at 6	EX1002 at 289-290; Reply at 6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6	EX1002 at 289-290; Reply at 5-6
65	EX1002 at 289; Reply at 9	EX1002 at 289; Reply at 9	EX1002 at 289; Reply at 9	EX1002 at 289; Reply at 9	EX1002 at 289; Reply at 9	EX1002 at 289; Reply at 9	EX1002 at 289; Reply at 9
67	EX1030 at 25; Reply at 4	EX1030 at 25; Reply at 4	EX1030 at 25; Reply at 4	EX1030 at 25; Reply at 7	EX1030 at 25; Reply at 7	EX1030 at 25; Reply at 7	EX1030 at 25; Reply at 7
67	EX1030 at 26; Reply at 4	EX1030 at 26; Reply at 4	EX1030 at 26; Reply at 4	EX1030 at 26; Reply at 7	EX1030 at 26; Reply at 7	EX1030 at 26; Reply at 7	EX1030 at 26; Reply at 7
67	EX1030 at 28; Reply at 4-5	EX1030 at 28; Reply at 4-5	EX1030 at 28; Reply at 4-5	EX1030 at 28; Reply at 7	EX1030 at 28; Reply at 7	EX1030 at 28; Reply at 7	EX1030 at 28; Reply at 7
68	EX2074 at 32; Reply at 3	EX2074 at 32; Reply at 3	EX2074 at 32; Reply at 3	EX2074 at 32; Reply at 4	EX2074 at 32; Reply at 4	EX2074 at 32; Reply at 4	EX2074 at 32; Reply at 4
68	EX2074 at 38; Reply at 4	EX2074 at 38; Reply at 4	EX2074 at 38; Reply at 4	EX2074 at 38; Reply at 4-5	EX2074 at 38; Reply at 4-5	EX2074 at 38; Reply at 4-5	EX2074 at 38; Reply at 4-5
69	EX2074 at 39; Reply at 4	EX2074 at 39; Reply at 4	EX2074 at 39; Reply at 4	EX2074 at 39; Reply at 4	EX2074 at 38; Reply at 4-5	EX2074 at 38; Reply at 4-5	EX2074 at 38; Reply at 4-5

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70	EX2075 at 10; Reply at 4	EX2075 at 10; Reply at 4	EX2075 at 10; Reply at 4	EX2075 at 11; Reply at 5	EX2075 at 11; Reply at 5	EX2075 at 11; Reply at 5	EX2075 at 11; Reply at 5
72	Reply at 23-24	Reply at 23-24	Reply at 23-24	Reply at 23	Reply at 23	Reply at 23	Reply at 23
73	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 19	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 19	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 19	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 20	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 20	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 20	Onoda at Figs. 3, 11; EX1055 at 186:8-12; Reply at 20
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