

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MONOLITHIC POWER SYSTEMS, INC.,

Petitioner,

v.

GREENTHREAD, LLC,

Patent Owner.

IPR2024-00468 (Patent 8,421,195 B2)
IPR2024-00469 (Patent 9,190,502 B2)
IPR2024-00470 (Patent 11,121,222 B2)
IPR2024-00550 (Patent 10,510,842 B2)
IPR2024-00551 (Patent 10,734,481 B2)
IPR2024-00552 (Patent 11,121,222 B2)
IPR2024-00553 (Patent 11,316,014 B2)¹

**PETITIONER'S OBJECTIONS TO
PATENT OWNER'S DEMONSTRATIVES**

¹ The word-for-word identical paper is filed in each proceeding identified in the heading.

Pursuant to the Board's Order regarding Oral Hearing (Paper 70² at 6) addressing objections to demonstratives, Petitioner provides below its objections to certain slides of Patent Owner's Demonstrative Exhibits served on September 4, 2025. The slides referenced below are attached to the end of this filing.

Slide Number(s)	OBJECTIONS
12	This slide purports to argue that Petitioner is in privity with [REDACTED] but neither the Director Review order, nor the following Board's Order regarding Supplemental Discovery (Paper 69) ordered any discovery related to [REDACTED] and Patent Owner expressly declined to pursue any discovery on [REDACTED] (<i>id.</i> at 4-5), such that Patent Owner should be deemed to have waived any further argument on [REDACTED] beyond what was already rejected by the Board's Institution Decision. Paper 23 at 27-36.
57-84	The entirety of the argument in these slides—that the minority carrier can only be a “hole” as opposed to an electron—is an argument that was newly raised in Patent

² For convenience, this filing cites papers and exhibits filed in IPR2024-00468 unless otherwise indicated. Substantially identical papers were filed in the other instant cases. *See also* Paper 69 at 3 nn.1, 4.

	Owner's sur-reply and as such is subject to Petitioner's motion to strike (Paper 52), making these slides objectionable for the same reason.
100-111	The entirety of the argument in these slides—that the dopant concentration remains flat in Onoda's surface region—is an argument that was newly raised in Patent Owner's sur-reply and as such is subject to Petitioner's motion to strike (Paper 52), making these slides objectionable for the same reason.

Dated: September 9, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the foregoing
**PETITIONER'S OBJECTIONS TO PATENT OWNER'S
DEMONSTRATIVES** were served in their entirety this 9th day of September, 2025
by electronic mail on the Patent Owner via its attorneys of record:

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Dated: September 9, 2025

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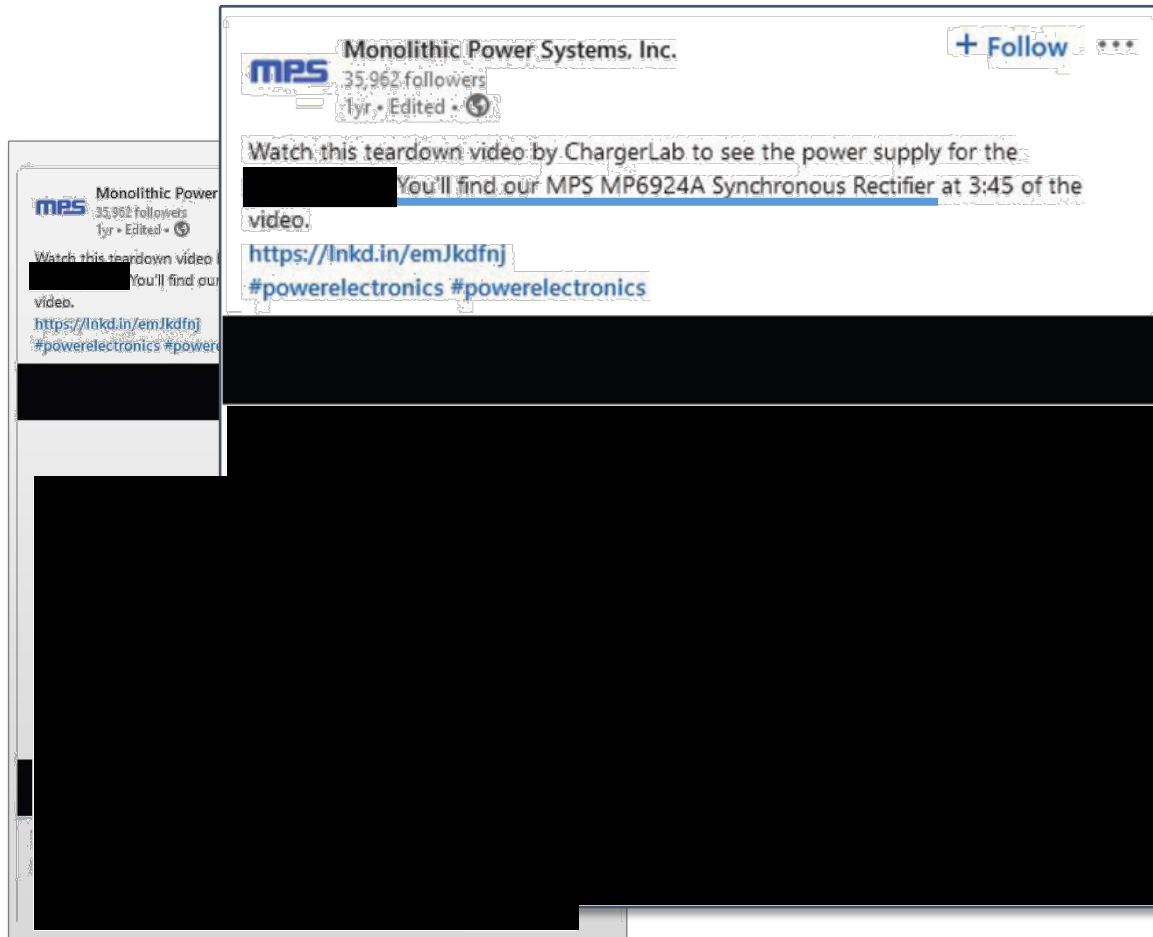
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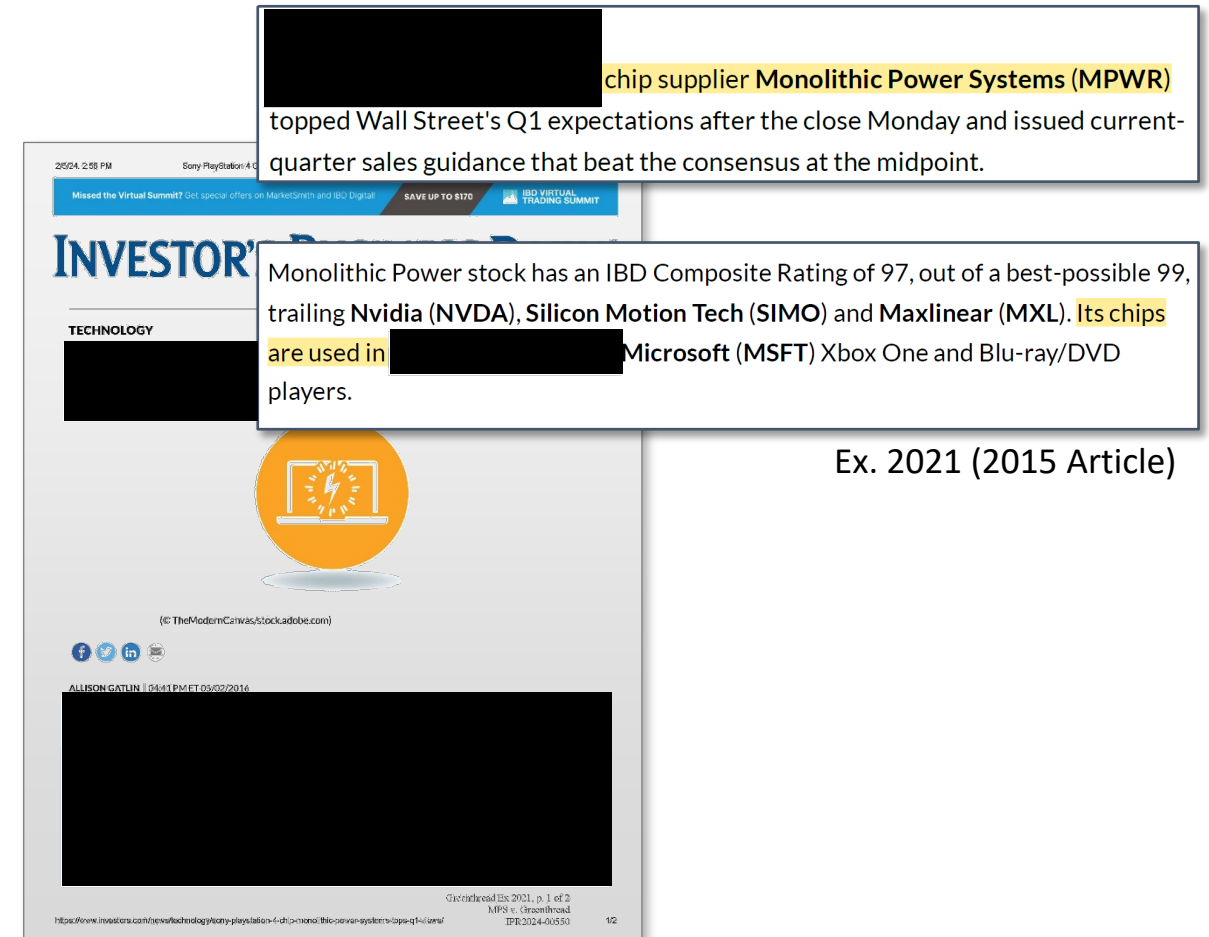
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Paralegal

1. The Petitions Are Time-Barred

- PO has “presented more than enough evidence to sufficiently put this issue into dispute.”



Ex. 2020 (MPS LinkedIn Post)



Ex. 2021 (2015 Article)

Overview of Issues

1. **Petitioner has presented zero “actual evidence” that the Petitions are timely.**
2. **The Claims require “movement of carriers” from the “surface layer” or “active region.”**
3. **The '195 and '502 Claims require “movement of minority carriers” from the “surface layer.”**
4. Kawagoe does not disclose “movement of [minority] carriers” from the “surface layer.”
5. Onoda/Nishizawa does not disclose “movement of [minority] carriers” from the “surface layer.”
6. Petitioner has the burden to identify electric fields that would “aid carrier movement.”
7. Petitioner’s expert confirmed that carriers in the “surface layer” are affected by numerous other fields and forces.
8. Petitioner’s expert confirmed “movement of carriers” depends on the sum of all fields in the “surface layer.”
9. Petitioner’s expert did not analyze any of the fields or force magnitudes in the “surface layer.”
10. Petitioner's prosecution-related arguments are incorrect.
11. Greenthread’s licensing agreements provide substantial evidence of objective indicia of non-obviousness.

3. Movement of Minority Carriers from the Surface Layer

- The '195 and '502 claims require “movement of minority carriers.”

US 8,421,195

1. A CMOS Semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

-00468: Ex. 1001 ('195 pat.) at 4:13-29

US 9,190,502

7. A semiconductor device comprising:
a surface layer;
a substrate;
an active region including a source and a drain, disposed on one surface of said surface layer;
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

-00469: Ex. 1001 ('502 pat.) at 4:52-67

3. Movement of Minority Carriers from the Surface Layer

- The Challenged Claims **must** be considered in light of the specification.



¶¶ 1,2. The claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose. Thus the claims are construed to state the legal scope of each patented invention, on examination of the language of the claims, the description in the specification, and the prosecution history. See *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250, 48 USPQ2d 1117, 1122 (Fed. Cir.1998) (“[T]he interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim.”). Although

Netword LLC v. Centraal Corp.,
242 F.3d 1347, 1352 (Fed. Cir. 2001)

[1–3] “If the intrinsic record fully governs the proper construction of a term, we review the [b]oard’s claim construction *de novo*.” *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1278 (Fed. Cir. 2017). During reexamination, “the PTO must give claims their broadest reasonable construction consistent with the specification.” *In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1379 (Fed. Cir. 2007). Even under the broadest reasonable construction rubric, however, the board must always “consider the claims in light of the specification and teachings in the underlying patent.” *In re CSB-Sys. Int’l, Inc.*, 832 F.3d 1335, 1341 (Fed. Cir. 2016) (citations and internal quotation marks omitted). And there is no reason why this construction could not coincide with that of a court in litigation.

In re Power Integrations,
884 F.3d 1370, 1375 (Fed. Cir. 2018)

Courts must exercise caution lest dictionary definitions, usually the least controversial source of extrinsic evidence, be converted into technical terms of art having legal, not linguistic, significance. The best source for understanding a technical term is the specification from which it arose, informed, as needed, by the prosecution history. The evolution of restrictions in the claims, in the course of examination in the PTO, reveals how those closest to the patenting process—the inventor and the patent examiner—viewed the subject matter. See *Hoechst Celanese Corp. v. BP Chemicals Ltd.*, 78 F.3d 1575, 1578, 38 USPQ2d 1126, 1129 (Fed.Cir. 1996) (“A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning.”) When the specification explains and defines a term used in the claims, without ambiguity or incompleteness, there is no need to search further for the meaning of the term.

Multiform Desiccants, Inc. v. Medzam, Ltd., 133 F.3d 1473, 1478 (Fed. Cir. 1998)

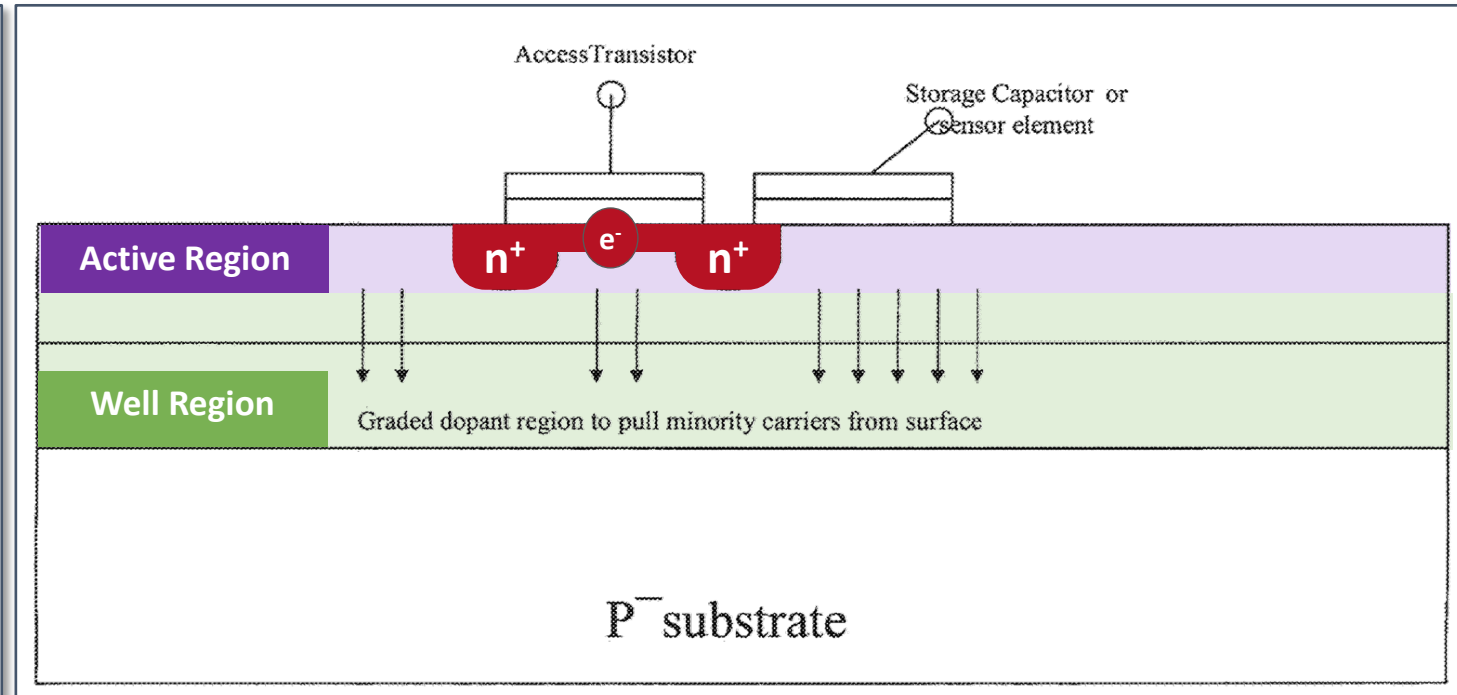
Greenthread Ex. 2088, p. 59 of 149
MPS v. Greenthread

3. Movement of Minority Carriers from the Surface Layer

- The specification explains the “majority carriers” are the majority carrier in the MOSFET channel.

Bipolar Junction transistors (BJT) are minority carrier devices as the principle device conduction mechanism. However, majority carriers also a small yet finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. Carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an ‘aiding drift field’, to enhance the diffusing minority carrier’s speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT’s (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region⁴ in a IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other

-00468: Ex. 1001 (’195 pat.)
at 1:23-46



-00468: Ex. 1001 at Fig. 5B

⁴ Because the channel is formed by electrons with a negative charge, the MOSFET is referred to as an n-channel MOSFET, and the “minority carriers” are holes.

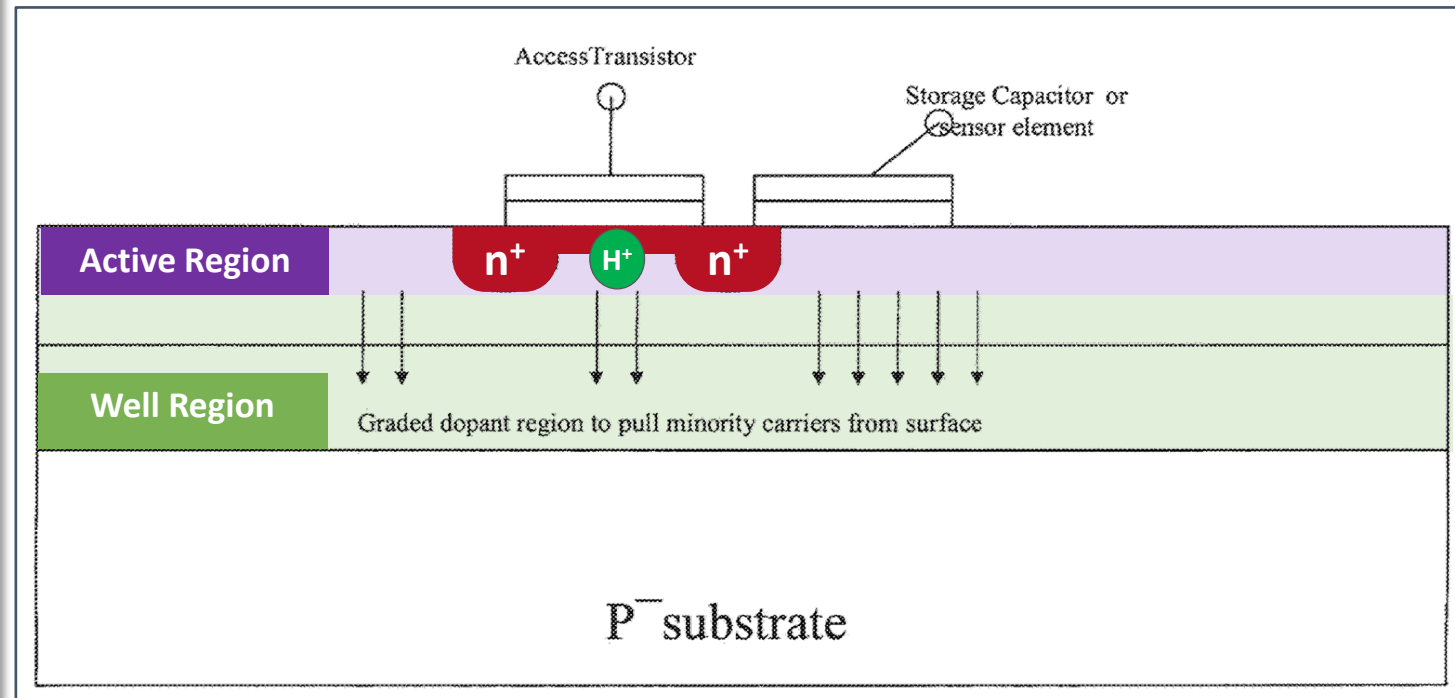
-00468: Ex. 2057 (Glew Decl.) at ¶36, p. 3

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3. Movement of Minority Carriers from the Surface Layer

- The “spurious minority carriers” interfere with the “active circuitry at the surface.”

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)– VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC'S. These unwanted carriers can discharge dynamically-held ‘actively held high’ nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM's is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC's is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC's with the embodiments described here. Creating ‘Sub Terrain’ recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well.



-00468: Ex. 1001 at Fig. 5B

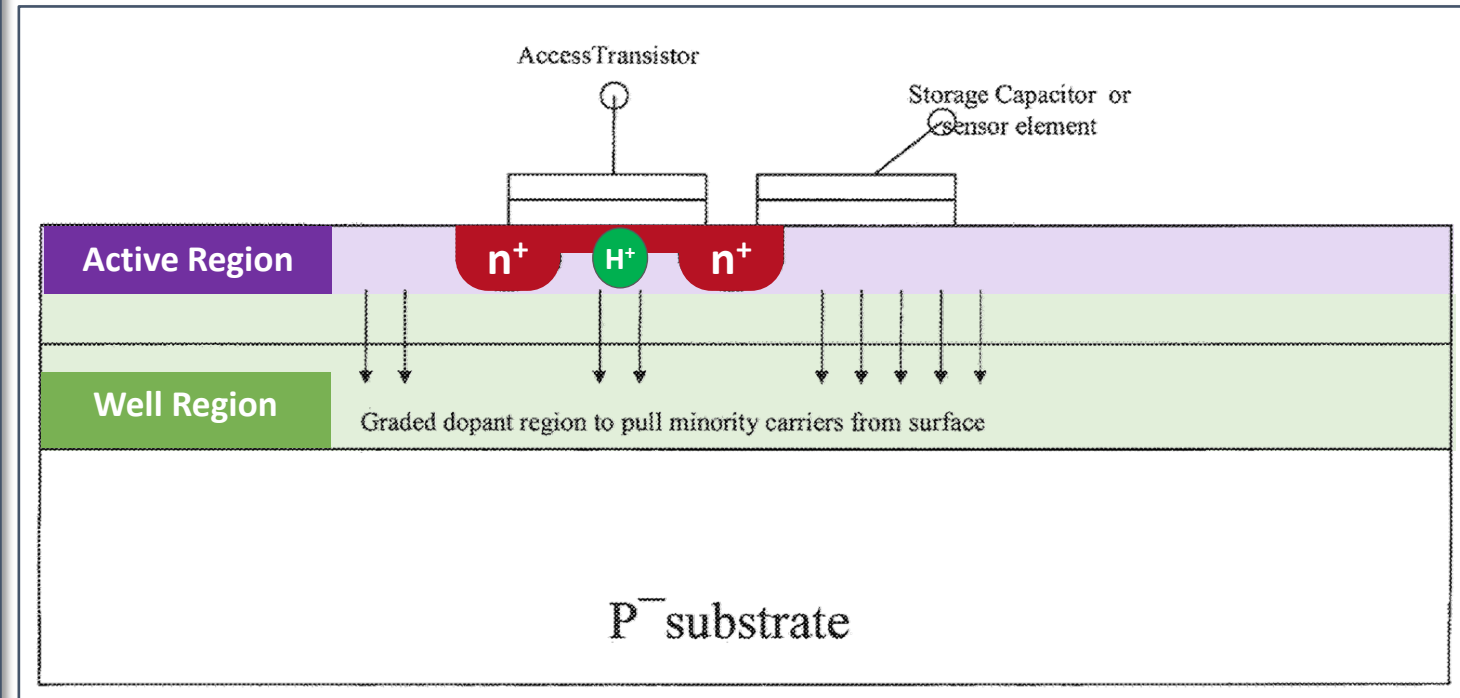
-00468: Ex. 1001 ('195 pat.) at 3:14-40

Greenthread Ex. 2088, p. 61 of 149
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3. Movement of Minority Carriers from the Surface Layer

- The “minority carriers” interfere with the MOSFET’s channel.

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)– VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC’S. These unwanted carriers can discharge dynamically-held ‘actively held high’ nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM’s is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC’s is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC’s with the embodiments described here. Creating ‘Sub Terrain’ recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well.



-00468: Ex. 1001 at Fig. 5B

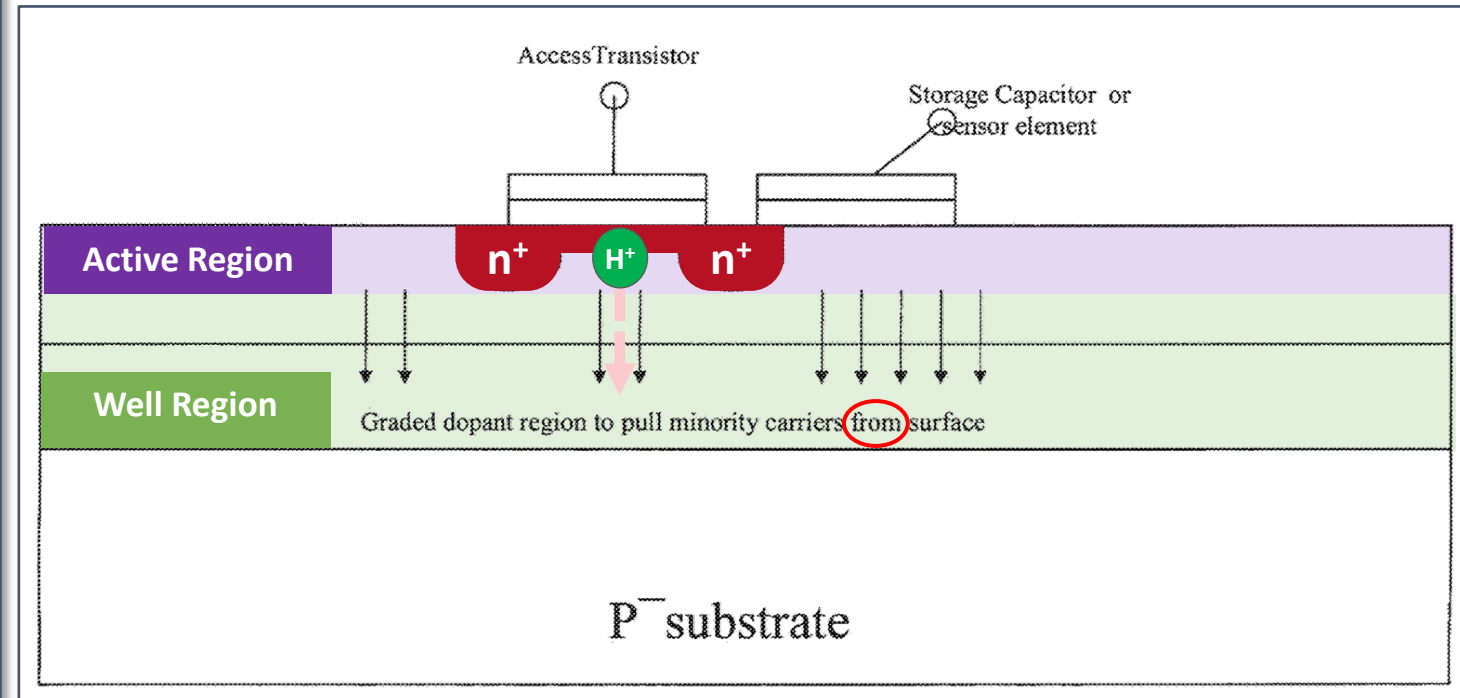
-00468: Ex. 1001 ('195 pat.) at 3:14-40

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3. Movement of Minority Carriers from the Surface Layer

- A “drift field” with a “graded dopant region” sweeps the minority carriers from the surface.

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)– VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC'S. These unwanted carriers can discharge dynamically-held ‘actively held high’ nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM's is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC's is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC's with the embodiments described here. Creating ‘Sub Terrain’ recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well.



-00468: Ex. 1001 at Fig. 5B

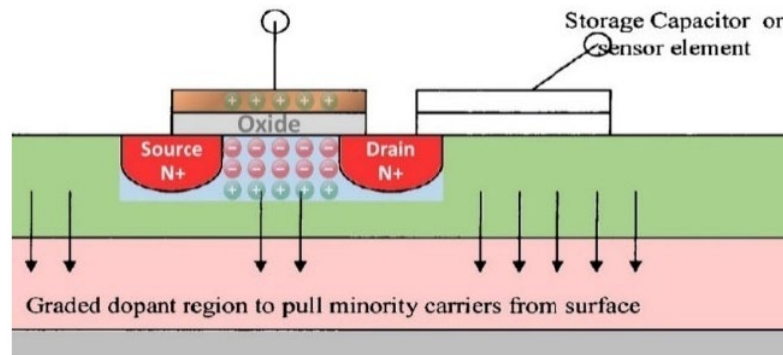
-00468: Ex. 1001 ('195 pat.) at 3:14-40

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3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew explained that in Fig. 5B, the “minority carriers” are holes.

36. When a positive voltage is applied to the gate, an electric field forms in the oxide. This positive electric field repels the “positive” holes downwards, while the negative electrons (red circles) are attracted to move into the blue surface layer. When enough electrons have accumulated in the surface layer below the oxide, they form a conductive channel (as annotated in Figure 5B below) of electrons between the source and the drain, and current can begin to flow through the transistor.



Greenthread Ex. 2027, p. 1 of 45
MPS v. Greenthread

Ex. 1001, FIG. 5B (annotated).³ In order to turn the transistor “off,” the positive voltage is removed from the gate and the channel disappears as the holes return to the surface layer.

³ Because the channel is formed by electrons with a negative charge, the MOSFET is referred to as an n-channel MOSFET, and the “minority carriers” are holes.

-00468: Ex. 2057 (Glew Decl.) at ¶36, n. 3

3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew confirmed the same when cross-examined by Petitioner's counsel.

Transcript

Case: Monolithic P

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WORLDWIDE C

10 Q. I guess while we're on it, what's a
11 minority carrier?
12 A. Well, you know, it depends on the context
13 of what we're looking at. But there's a minority
14 carrier as opposed to majority carrier. As I cited
15 to at the '195 patent in column 3, it describes at
16 341, quote, "The graded dopant can also be
17 implemented in surface channel of MOS devices to
18 accelerate majority carriers towards the drain." End
19 quote.
20 So in a MOS device, the majority carrier is
21 the electron if it's an NMOS device. Column 1 also,
22 for example, describes that at column 1, line 43, "In
23 contrast to BJTs MOS device is a majority carrier
24 device for conduction. The conduction is channel
25 dominated." End quote.

1 So basically in a MOS device, the majority
2 carrier in an NMOS device would be electrons.
3 Electrons flow from an N-type source to an N-type
4 drain.
5 Minority carriers would be the holes. So
6 when one applies voltage to the gate which sits on
7 top of the channel, one inverts the layers so that
8 holes are -- a positive voltage pushes holes away
9 from the surface and attracts electrons to the
10 surface. That way, there is a connection between the
11 source and drain which have electrons, and now the
12 channel has electrons, and the channels are that
13 majority carrier -- excuse me, the electrons in that
14 channel are the majority carrier, and the P -- the
15 holes represented by the symbol P are pushed away,
16 and those are the minority carriers.

Ex. 1055 (Glew Dep. Tr.) at 38:10-39:16

GreenThread Ex. 2088, p. 65 of 149
MPS v. GreenThread

3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew confirmed the same when cross-examined by Petitioner's counsel.

12 Q. In the well 6P, is a minority carrier an
13 electron or a hole?
14 MR. WHITEHURST: Object to form.
15 THE WITNESS: In the minority carrier 6P,
16 there's an NMOS device, and so in the NMOS device the
17 majority carriers are the electrons, the minority
18 carriers are holes. As I wrote in my declaration on
19 page 18, column 35, I believe we reviewed this
20 earlier, I cite to Exhibit 1001, the '195 patent, at
21 column 3, line 10.

Ex. 1055 (Glew Dep. Tr.) at
126:12-21

15 Q. Is that an electron or a hole which is the
16 minority carrier?
17 A. For NMOS, the minority carrier is P. For
18 PMOS, a minority carrier would be N.

Ex. 1055 at 133:15-18

6 Q. I'll ask again because that doesn't
7 actually answer. Are the minority carriers of P-type
8 electron or hole?
9 MR. WHITEHURST: Object to form.
10 THE WITNESS: A hole or P-type minority
11 carrier is a minority carrier in an NMOS device, an
12 NMOS transistor. On the other hand, an electron or
13 N-type carrier would be the minority in a PMOS
14 device.

Ex. 1055 at 136:6-14

Transcript

Case: Monolithic P

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MPS EX. 1055

3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew confirmed the same when cross-examined by Petitioner's counsel.

22 Q. Okay. In a device that has an N doped
23 drain and an N doped source in a P doped well, are
24 the minority carriers electrons or holes?
25 A. In an NMOS device with an N-type source and
1 drain in a P-well, the majority carriers in an NMOS
2 device are electrons. The minority carriers are
3 holes.

Ex. 1055 at 138:22-139:3

Transcript

Case: Monolithic P

23 Q. Do you have an opinion what the spurious
24 minority carriers would be in Figure 5B?
25 A. Figure 5B is an NMOS device. So it would
1 store and pass electrons to spurious minority
2 carriers -- would be holes, or P.

Ex. 1055 (Glew Dep. Tr.) at 152:23-153:2

25 Q. Do you have an opinion whether the majority
1 carriers -- before I ask that question, can you go
2 back and look at Figure 5B where you identified an
3 NMOS transistor in a P-well?
4 A. Yes.
5 Q. Can you explain what the majority carrier
6 would be?
7 A. Yes. This is an NMOS transistor shown
8 because the source and drain are labelled N and T.
9 So an NMOS transistor requires electrons to connect
10 the N-type source and drain. So electrons are the
11 majority carrier N-type and the minority carriers are
12 holes or P-type.

Ex. 1055 at 154:25-155:12

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MPS EX. 1055

3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew confirmed the same when cross-examined by Petitioner's counsel.

7 Q. And I believe you testified previously that
8 these unwanted minority carriers would be holes in
9 Figure 5B?
10 A. Yes. Figure 5B is NMOS, so electrons are
11 majority and holes are minority carriers.

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Ex. 1055 at 157:7-11

8 Q. If I understand your testimony correctly,
9 the minority carrier as claimed in claim 1 can be
10 either an electron or a hole?
11 A. Not precisely. It can be a hole for an
12 NMOS device or an electron for a PMOS device, as I
13 understand it. It must be the minority carrier for
14 that specific transistor in the CMOS structure.

Ex. 1055 (Glew Dep. Tr.) at 188:8-14

13 Q. So just like we saw in Figure 5B of the
14 patent, Figure 11 of ONODA is showing a dopant
15 profile for an NMOS transistor in a P-well?
16 A. That is my understanding, yes.
17 Q. And for an NMOS transistor, the majority
18 carrier would be an electron?
19 A. Yes, that is correct. NMOS has a majority
20 of electrons as the carriers.
21 Q. And what is the minority carrier?
22 A. The minority carrier for an NMOS is a hole.

Ex. 1055 at 176:13-22

Transcript

Case: Monolithic P

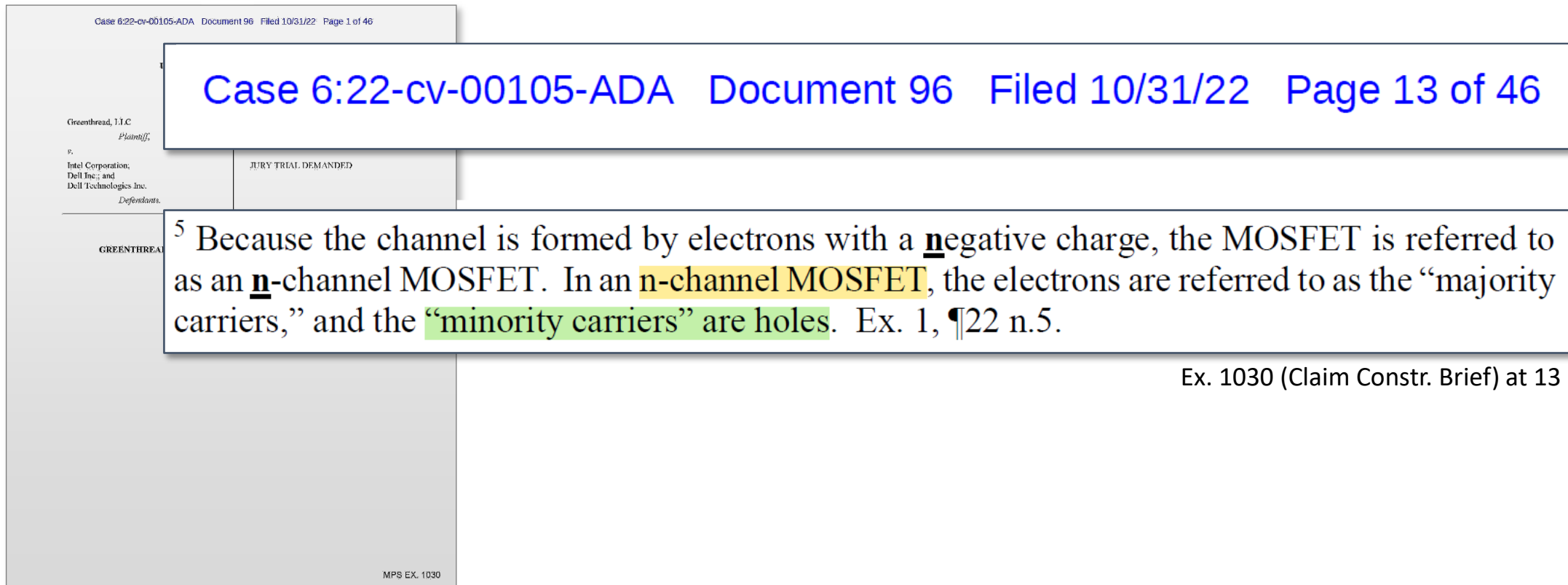
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MPS EX. 1055

3. Movement of Minority Carriers from the Surface Layer

- Petitioner was aware of Greenthread's position when it filed its Petitions in February and March 2024 and cited Greenthread's prior claim construction briefing.



Ex. 1030 (Claim Constr. Brief) at 13

3. Movement of Minority Carriers from the Surface Layer

- Dr. Campbell (Petitioner's expert) relies on the doping type within a region to define the "minority carrier."

C. Overview of the Technical Concepts

32. My analysis will primarily rely on prior art patents Onoda, Nishizawa, and Kawagoe to show that the '195, '502, and '222 patents are invalid. All three prior art patents deal with the same technical challenge as the patents being challenged: how to protect electronic circuits from impacts of high energy photons such as x-rays or high energy particles such as alpha particles. When a high-energy collision takes place in a semiconductor, it creates a very large number of negatively charged electrons and positively charged holes. Of particular interest are the minority carriers such as electrons in a p-type region. If enough of these electrons

are collected by the circuitry on the surface of the semiconductor, they can introduce faults in the circuit. As will be discussed, these charged species move in response to an electric field, and so an electric field that is properly constructed will push the minority carriers away from the surface, making their collection much less probable. I will also point out that an electric field caused by a doping profile can improve the performance of photosensing devices (Patents from Jastrzebski and from Kamins) by drifting minority carriers into the substrate.

-00468: Ex. 1003 (Campbell Decl.) at ¶132

charged electrons and positively charged holes. Of particular interest are the minority carriers such as electrons in a p-type region. If enough of these electrons

3. Movement of Minority Carriers from the Surface Layer

- Ground I: Dr. Campbell views electrons as “minority carriers.”

72. In my opinion, Onoda discloses this limitation. Onoda's drift layer has a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (gray, starting at the 5 μm depth level). Such a dopant concentration profile can be considered a decaying exponential as Onoda's FIG. 11 depicts the carrier concentration as nearly a straight line on a semi-log (log/linear) graph. The below annotation of Onoda's FIGS. 8 and 11 depicts the movement of the minority carriers (purple arrow) due to the first static unidirectional electric drift field, at a depth corresponding to Onoda's second semiconductor layer 102 (tan) as the single drift layer. The arrow indicates the movement of minority carriers from the surface layer to the substrate. A POSITA would understand that the field would be in the opposite direction

79. The well region 105a, like the “single drift layer” 102, has a dopant profile that has a downward sloping gradient. (Onoda at [0052].) The well region 105a has the claimed second static unidirectional electric drift field. The pink arrow depicts the direction of minority carrier movement (where the field would be depicted in the opposite direction) to aid the movement of minority carriers from the surface layer to said substrate.

-00468: Ex. 1003 (Campbell Decl.) at ¶¶72, 79

3. Movement of Minority Carriers from the Surface Layer

- Ground II: Dr. Campbell views electrons as “minority carriers.”

89. Onoda and Nishizawa both disclose CMOS devices and are concerned with minority carriers (electrons) moving into the functioning circuitry. Specifically,

layer to move the minority carriers to the substrate. Nishizawa at 18:10-19:53. Such an impurity gradient will keep the **electrons** from being captured by the circuitry at the surface and impairing the circuit. (*Id.* at 18:42-50.) FIG. 16 in Nishizawa depicts

-00468: Ex. 1003 (Campbell Decl.) at ¶¶89, 96

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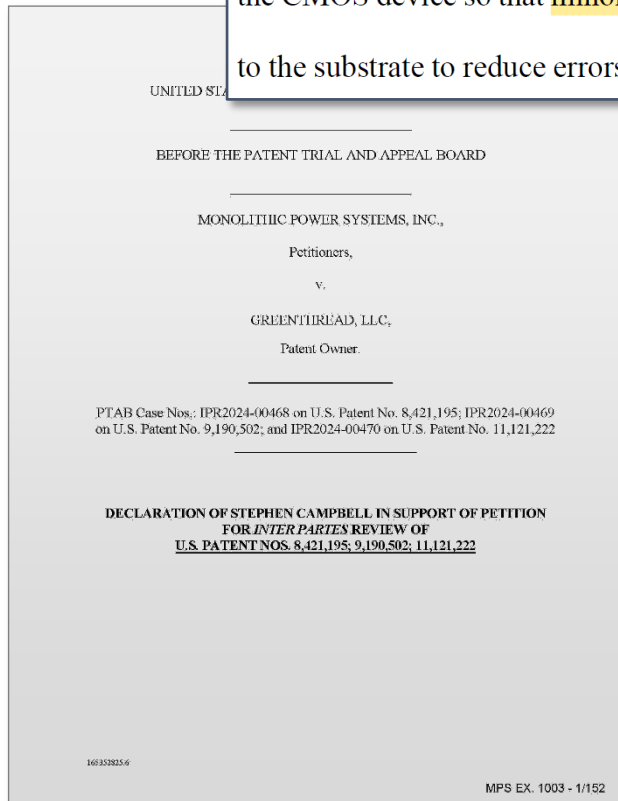
3. Movement of Minority Carriers from the Surface Layer

- Ground III: Dr. Campbell views electrons as “minority carriers.”

transistors for the CMOS device. This single drift layer in Kawagoe is at the surface of the semiconductor device (*see, e.g.*, Kawagoe at 15:62-16:15) and is formed into the CMOS device so that minority carriers (*e.g.*, electrons in the p-well) are attracted to the substrate to reduce errors. (*Id.* at 16:7-11.) The single drift layer in Kawagoe

-00468: Ex. 1003 (Campbell Decl.)
at ¶¶111, 117

117. Kawagoe teaches a single drift layer with a graded dopant profile. This graded dopant profile results in “electrons ... [being] attracted to the substrate body 2S by that concentration gradient.” (Kawagoe at 16:7-11.) A POSITA would understand that electrons are minority carriers in the p-well, and that the electrons are attracted to the substrate due to a static unidirectional electric drift field. A POSITA would understand the field to be static because it is created by doping impurities that are fixed during device fabrication, as depicted in Kawagoe (*see, e.g.*, Kawagoe at 15:26-36, FIGS. 20-21). There are electric fields in separate regions due to the graded doping concentrations, *e.g.*, those depicted by pink and purple arrows in annotated FIG. 17 below, where the pink field would have been understood to be the first static unidirectional electric drift field. The arrow orientation and direction are depicting the drift of minority carriers (electrons) in the p-well and a POSITA would understand that the electric field would exist in the opposite direction.



3. Movement of Minority Carriers from the Surface Layer

- Dr. Campbell's understanding of "minority carrier" is inconsistent with how the term is used in the patents.

Transcript

Case: Monolithic P

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MPS EX. 1055

25 Q. I'm asking about Kawagoe, though, and I'm
1 asking a simple question. It's A or B in those
2 specific wells. Figure 16 is a minority carrier in
3 N-well 6N, an electron or a hole?
4 A. The term majority or minority character as
5 used in the patents in suit relates to an electronic
6 structure such as a transistor, not to a chunk of raw
7 material such as a well.

Ex. 1055 (Glew Dep. Tr.)
at 129:25-130:7 (left); 139:4-22 (right)

4 Q. Okay. And taking your answer to Figure 16
5 of Kawagoe, the minority carriers of the well 6N,
6 according to your testimony, are electrons; correct?
7 A. A well doesn't have a minority/majority. A
8 transistor has a minority/majority carrier. It
9 carries from the source to the drain. So you're
10 asking me about a PMOS device, P source drain in an
11 N-well; is that correct?
12 Q. I'm asking specifically about the N
13 material 6N of Kawagoe's Figure 16 which the P doped
14 source and P doped drain are implanted thereon. What
15 would the minority carrier be there?
16 MR. WHITEHURST: Object to form.
17 THE WITNESS: As I've stated previously,
18 the term, concept of carrier has meaning in a context
19 of a transistor or device. The current is carried
20 from the source to the drain. The PMOS device with a
21 P source in a P drain has holes as the majority
22 carrier and electrons as the minority.

Greenthread Ex. 2088, p. 74 of 149
MPS v. Greenthread

3. Movement of Minority Carriers from the Surface Layer

- Dr. Campbell recognized that what constitutes a “minority carrier” changes when one looks at the channel itself.

19 Q. So, in an NMOS device, when you have
20 these electrons carrying the charge, what is the
21 majority carrier?
22 A. You have to qualify that by saying
1 where. In most of the device -- sorry. In the
2 substrate below the channel, the majority carrier
3 is holes. In the channel, the majority carrier
4 is electrons.

Ex. 2085 (Campbell Dep. Tr.) at 80:19-81:4

16 Q. And when you form an N-channel, what
17 is the majority carrier in the channel?
18 A. For an NMOS device, it would be
19 electrons.
20 Q. Okay. So, if we are talking about
21 turning this transistor on and it forms an
22 N-channel, the majority carrier in the N-channel
1 is an electron, correct?
2 A. Correct.
3 Q. What is the minority carrier in the
4 N-channel?
5 A. Holes.

Ex. 2085 at 98:16-99:5

Greenthread Ex. 2088, p. 75 of 149
MPS v. Greenthread

3. Movement of Minority Carriers from the Surface Layer

- In an NMOS device, electrons are the majority carriers and holes are the minority carriers.

10 So in the NMOS device shown in the P-well,
11 NMOS devices are formed in P-wells, the majority
12 carrier from NMOS device is an electron.
13 Q. So you're stating that the minority carrier
14 in the P-well 6P of Figure 16 is a hole; correct?
15 A. What I'm saying is the minority carrier in
16 the NMOS device would be considered P. The majority
17 carrier in the NMOS device in the P-well is an
18 electron.

Case: 1 Date: February 5, 2025
Ex. 1055 (Glew Dep. Tr.) at 129:10-18

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

MPS EX. 1055

24 Q. And let me ask that more simply. In the
25 P-type material, P-well 6P in Figure 16, is the
1 minority carrier an electron or a hole?
2 MR. WHITEHURST: Object to form.
3 THE WITNESS: The question makes no sense
4 because there is no carrier unless there's device.
5 Where would this electron be carrying something? You
6 know, to carry it has to go from A to B. There's
7 nowhere for an electron to carry in this. The term
8 carrier as it's used in the '195 patent is very
9 clearly associated with a specific device type, and
10 with the NMOS device type shown in that figure, the
11 majority carrier in the language used in the '195
12 patent is an electron.

Ex. 1055 at 127:24-128:12

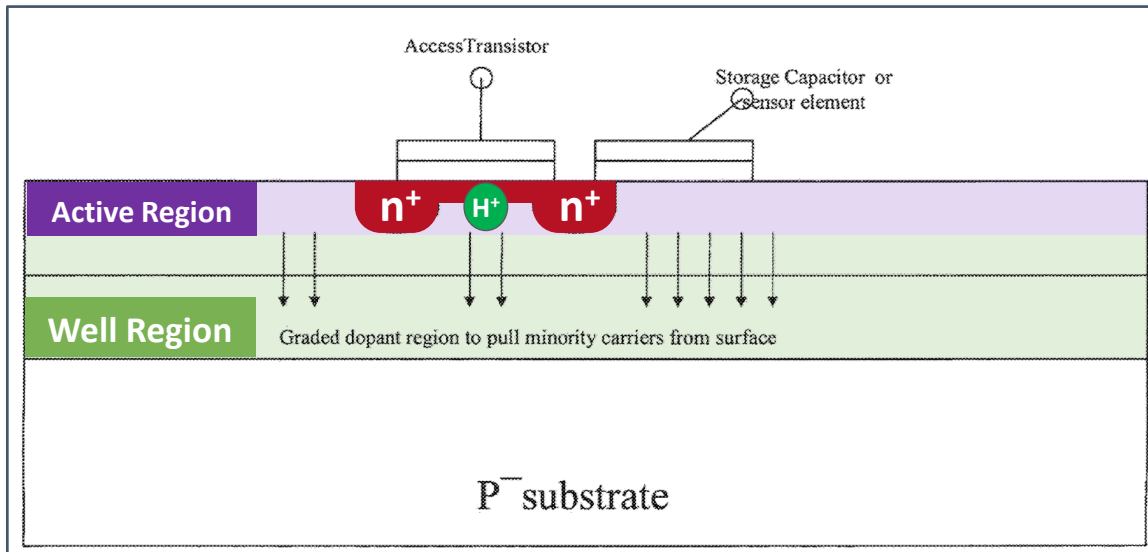
2 Q. Does it matter whether the transistor is on
3 or off?
4 A. No. The majority carrier for an NMOS
5 transistor is always an electron. Transistors are
6 meant to turn on and off. That's a normal part of
7 their operation.
8 Q. So a majority carrier -- strike that. So
9 for the NMOS transistor shown in Figure 5B, the
10 majority carrier is an electron regardless of whether
11 the transistor is on or off?
12 A. Yes. The majority carrier is always an
13 electron for NMOS transistor, regardless of its
14 state. It is channel dominated. And the only way to
15 get an electrical signal from the source to the drain
16 is to use electrons. The source is filled with
17 electrons, the drain is filled with electrons, and
18 the only way to connect the two is with electrons.
19 It never changes.

Ex. 1055 at 160:2-19

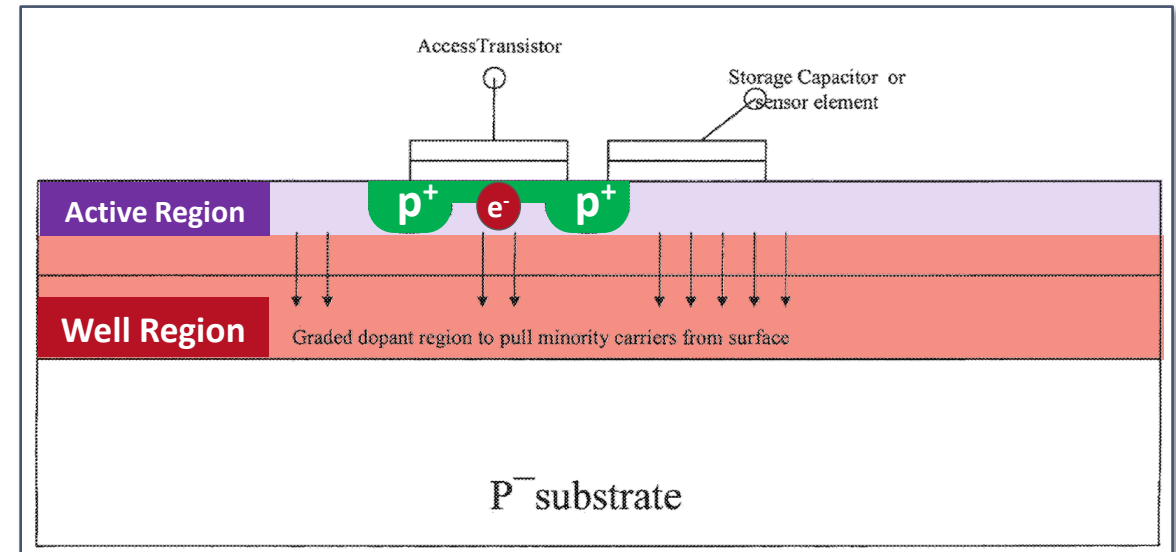
Greenthread Ex. 2088, p. 76 of 149
MPS v. Greenthread

3. Movement of Minority Carriers from the Surface Layer

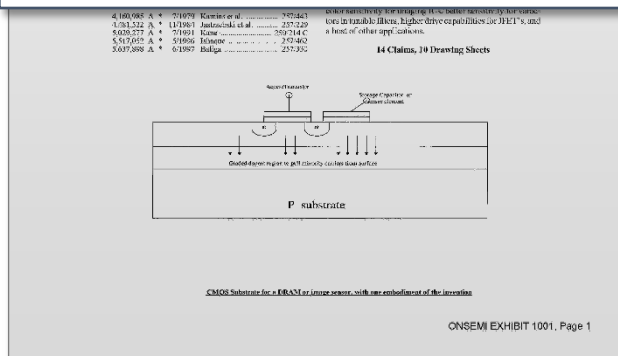
- In an NMOS transistor, the “majority carrier” is an electron, and the “minority carrier” is a hole.
- In an PMOS transistor, the “majority carrier” is a hole, and the “minority carrier” is an electron.



-00468: Ex. 1001 ('195 pat.)
at Fig. 5B

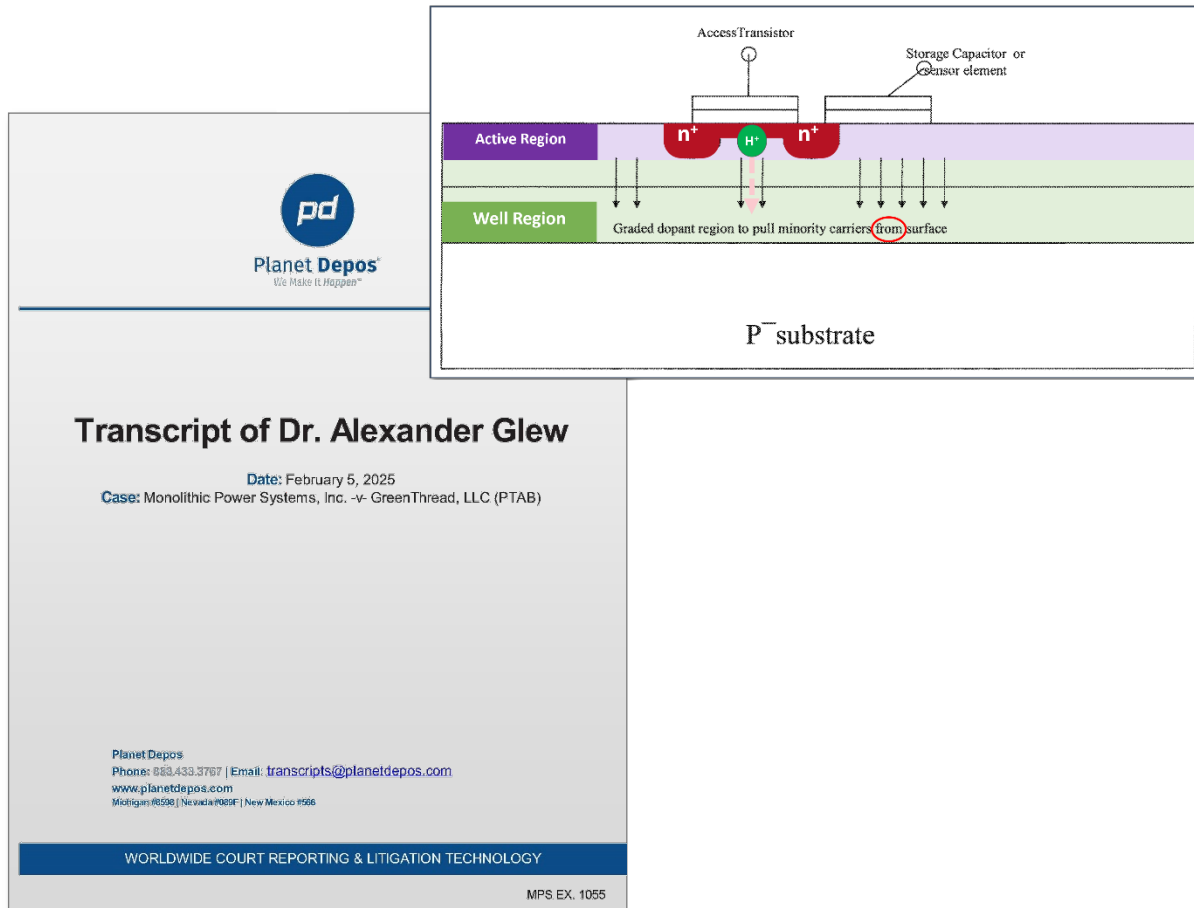


-00468: Ex. 1001 at Fig. 5B



3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew explained how the only “carrier” that Fig. 5B’s electric field can move from the “surface layer” is a positively-charged hole.



6 Q. Now what effect, if any, would the electric
7 field shown in Figure 5B have on an electron?
8 A. Figure 5B shows an electric field pointed
9 downward. So it would pull holes downward and push
10 electrons upward in the opposite direction. The
11 electric field acts in opposite direction on carriers
12 of opposite polarity. Thanks to Ben Franklin,
13 electrons go in the opposite direction of the
14 electric field.
15 Q. Looking at Figure 5B, would the electric
16 field in Figure 5B be capable of pulling electrons
17 from the surface?
18 A. No. The electric field at 5B is pointed
19 downwards. It only would pull holes downward. It
20 would push electrons upwards. It could not pull
21 electrons downward.

Ex. 1055 (Glew Dep. Tr.) at 159:6-21

GreenThread Ex. 2088, p. 78 of 149
MPS v. GreenThread

3. Movement of Minority Carriers from the Surface Layer

- Dr. Glew explained how the only “carrier” that Fig. 5B’s electric field can move from the “surface layer” is a positively-charged hole.

7 Q. Just to -- well, strike that. To slow down
8 a little, assuming electrons will flow in the
9 opposite direction of the electric field current
10 created; right?

11 A. Yes. Holes flow in the direction of the
12 field, electrons flow in the opposite direction. We
13 can thank Benjamin Franklin for creating this
14 confusing scenario.

Ex. 1055 (Glew Dep. Tr.) at 70:7-14

25 and technology and semiconductor devices. An
1 electric field acts on everything in its area. Where
2 the field exists, it acts on charged particles, and
3 it acts on all charged particles of a certain
4 polarity in the same way. It will act on particles
5 of opposite polarity in the opposite direction.

Ex. 1055 at 74:25-75:5

Transcript

Case: Monolithic P

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MPS EX. 1055

3. Movement of Minority Carriers from the Surface Layer

- Dr. Campbell agrees that the downward-facing electric field can only move holes.

1 Q. What did you mean by
2 "properly constructed"?

3 A. You would have to construct an
4 electric field that moves the carriers away, and
5 that means the electric field has to be, the
6 direction has to be correct.

```
7         If you're moving poles, then you
8         have to have the electric field that points
9         downward.
```

10 If you're moving electrons, the
11 electric field has to be pointing upward and you
12 have to have a sufficient electric field
13 intensity to prevent most of the carriers from
14 being collected by the drain.

Ex. 2058 (Campbell Dep. Tr.) at 34:1-14

10/17/2024 Monks

IN THE UNITED
STATE OF CALIFORNIA
COUNTY OF ALameda

MONOLITHIC POWER
INC.,
Petitioner
V.
GREENTHREAD, LLC,
Patent Owner.

REMOVAL DECISION OF
STEPHEN A. CAMPELLO, PH.D.

October 17, 2024
9:00 a.m. Central Daylight Time

Reported by: Leri J. Goodin, RFR, CRR, RSA,
California CSR #13959

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Greenthread Ex. 2058, p. 1 of 65
MPS v. Greenthread

3. Movement of Minority Carriers from the Surface Layer

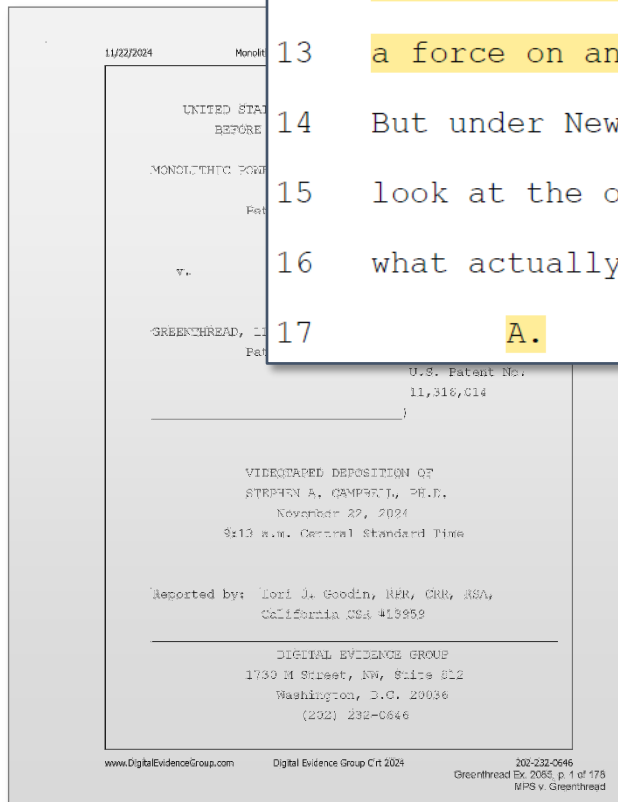
- Dr. Campbell agrees that the downward-facing electric field can only move holes.

11 So, when an electron field is
12 pointing in a downward direction, it will create
13 a force on an electron in an upward direction.
14 But under Newton's first law, you would have to
15 look at the other forces in order to determine
16 what actually happens?
17 A. Yes, that is always true.

Ex. 2085 (Campbell Dep. Tr.) at 95:11-17

12 Q. Okay. Just so the record is clear,
13 the electric field shown in Figure 5B would cause
14 holes to move in a downward direction and
15 electrons move in an upward direction, right?
16 A. Yes.
17 Q. And why is that?
18 A. Because holes are positively charged
19 and electrons are negatively charged.

Ex. 2085 at 109:12-19



3. Movement of Minority Carriers from the Surface Layer

- If the “minority carrier” in an NMOS transistor were an electron, it would exclude the specification’s preferred embodiment.



[17] Moreover, Defendants’ expert admitted that construing the claims such that “employ[ing] the common technique of grounding the system” would cause the converter to be considered non-isolated would prevent the claims from encompassing the preferred embodiment. J.A. at 45070–71. A claim construction that “excludes the preferred embodiment is rarely, if ever, correct and would require highly persuasive evidentiary support.” *Adams Respiratory Therapeutics, Inc. v. Perrigo Co.*, 616 F.3d 1283, 1290 (Fed.Cir.2010). In this case, the specification, including the claims, supports a reading that encompasses the preferred embodiment.

SynQor, Inc. v. Artesyn Techs., Inc.,
709 F.3d 1365, 1378-79 (Fed. Cir. 2013)

3. Movement of Minority Carriers from the Surface Layer

- Kawagoe's graded concentration is only concerned with **electrons**.
- But the Petition says nothing about Kawagoe's effect on "minority carriers" (*i.e.*, holes).

C. Ground III: Kawagoe Renders Obvious Claims 1, 2, 3, 5, and 6.

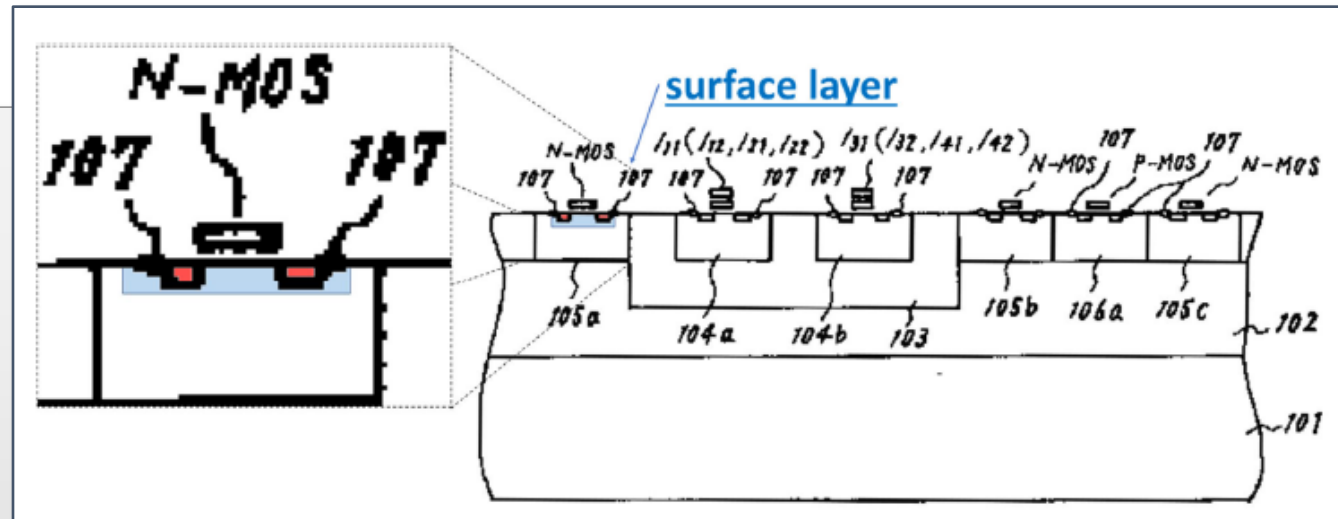
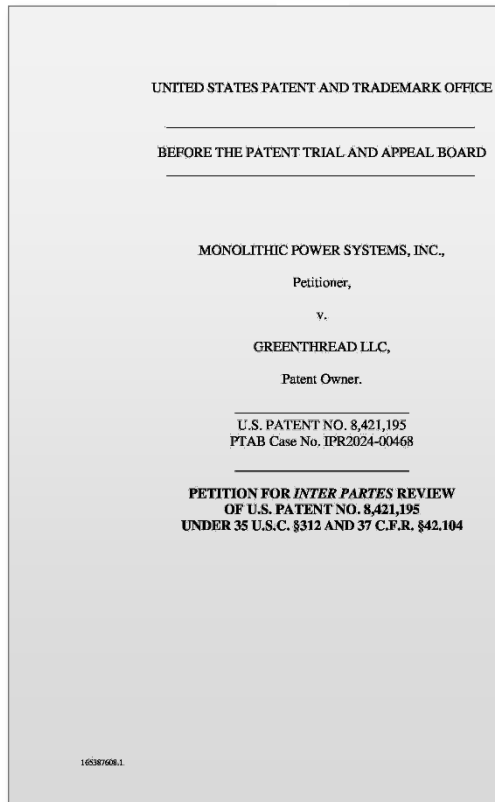
Kawagoe teaches a CMOS device whose surface region (its epitaxial layer) has its "impurity concentration gradually lowered depth wise of said epitaxial layer." (Kawagoe at Abstract.) The "gradient ... is gradually lowered in the depth wise direction from the surface of the epitaxial layer ... so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient." (*Id.* at 16:3-8.)

-00468: Petition [1] at 53

Greenthread Ex. 2088, p. 83 of 149
MPS v. Greenthread

3. Movement of Minority Carriers from the Surface Layer

- Petitioner relies on Onoda's NMOS transistor whose “minority carrier” is holes.
- The Petition says nothing about Onoda's effect on holes but instead discusses *electrons*.



⁵ The arrow indicates the movement of minority carriers from the surface layer to the substrate. (Ex. 1003 at ¶¶ 72-74). A POSITA would understand that the field would be in the opposite direction. (*Id.*)

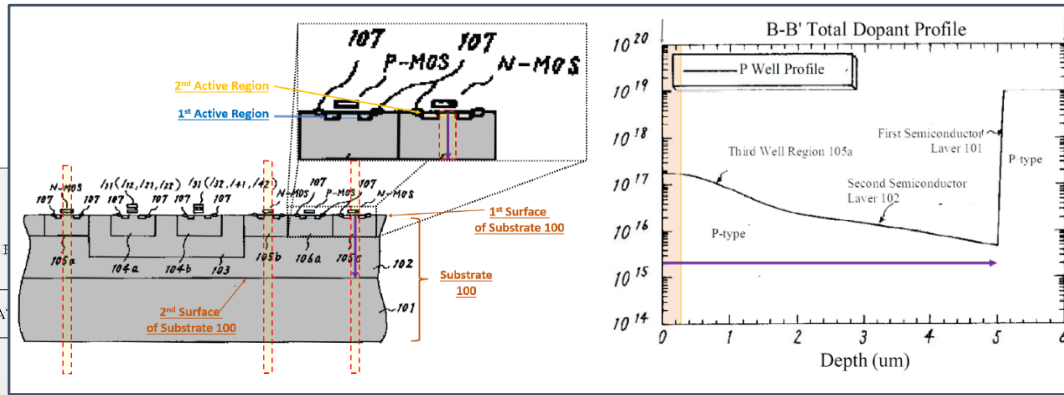
-00468: Petition [1] at 21, 32 n.5

Overview of Issues

1. **Petitioner has presented zero “actual evidence” that the Petitions are timely.**
2. **The Claims require “movement of carriers” from the “surface layer” or “active region.”**
3. **The '195 and '502 Claims require “movement of minority carriers” from the “surface layer.”**
4. **Kawagoe does not disclose “movement of [minority] carriers” from the “surface layer.”**
5. **Onoda/Nishizawa does not disclose “movement of [minority] carriers” from the “surface layer.”**
6. Petitioner has the burden to identify electric fields that would “aid carrier movement.”
7. Petitioner’s expert confirmed that carriers in the “surface layer” are affected by numerous other fields and forces.
8. Petitioner’s expert confirmed “movement of carriers” depends on the sum of all fields in the “surface layer.”
9. Petitioner’s expert did not analyze any of the fields or force magnitudes in the “surface layer.”
10. Petitioner's prosecution-related arguments are incorrect.
11. Greenthread’s licensing agreements provide substantial evidence of objective indicia of non-obviousness.

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Onoda does not mention moving carriers from the “surface layer.”



-00550: Petition [1] at 54-55

The fact that a graded concentration aids the movement of carriers was a well-known property of semiconductor devices long before September 2004. (Ex. 1003, ¶¶103, 46-58.) Indeed, Patent Owner admitted that to be the case in prosecution, where Patent Owner, citing prior art, stated that “the graded dopant concentration itself creates a ‘built-in’ electrical field” and this “built-in” electric field “forces the movement of carriers into a particular direction, whereby the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.” (Ex. 1003, ¶¶47, 103.). The net effect of the graded dopant concentration is to cause carriers (e.g., electrons) to move from the top surface of the substrate 100 to the bottom surface of the layer 102, which is towards the second surface of the substrate 100. (Ex. 1003, ¶104.)

-00550: Petition [1] at 52-53

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Onoda’s dopant profile is not graded in the “surface layer” to aid carrier movement.

UNITED STATES
BEFORE THE PATENT AND TRADEMARK OFFICE

MONOLITHIC SEMICONDUCTOR DEVICE

FIG. 100.

PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 10,510,842
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

140450727.5

Shown below is the graded concentration profile of FIGS. 8 and 11 (which depict intermediate processing steps) annotated on top of FIG. 3 (which is the final constructed device) to demonstrate that the “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration.” As can be seen from the below, the dopant profile is downward graded going through the channel of the active region, the third well regions 105a/b/c, and the second semiconductor layer 102. Immediately following annotated FIG. 3, is annotated FIG. 11, depicting that the downward gradient exists in the active region’s (tan) channel. (Ex. 1003 at ¶100.)

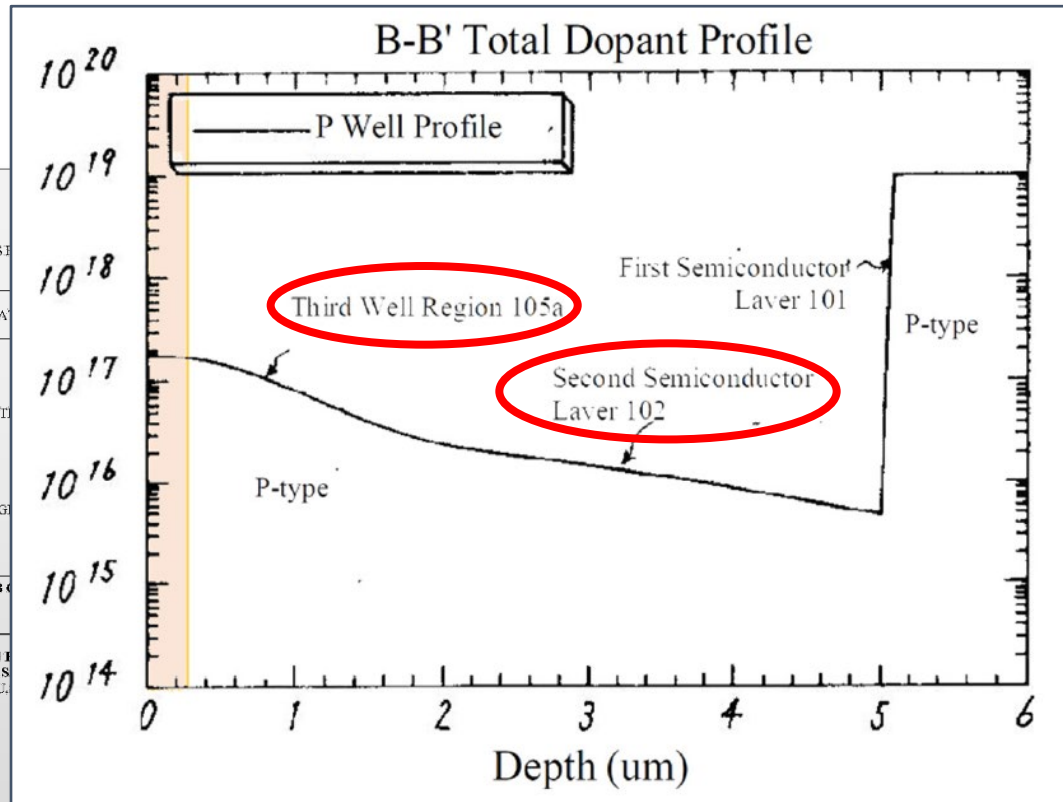
-00550: Petition [1] at 51

Onoda’s FIG. 11 depicts the graded dopant profile across the p-type well regions 105a, 105b, 105c, which constitutes the “at least one graded dopant concentration” of the “at least a portion of at least one of the first and second active regions.” FIG. 11 is a cross sectional slice (B-B) through the device depicted in FIG. 8, which is the same embodiment as FIG. 3. (See, e.g., Onoda at [0041]-[0045]). As can be seen from the below, the dopant concentration decreases as a function of depth through the third well region 105a (p-type) and the second semiconductor layer 102 (p-type). Then, at the point where the slice reaches the semiconductor layer 101, the dopant concentration increases. (Id. at [0052].). Moreover, a POSITA would have understood that third well regions 105b and 105c would have the same dopant profile as region 105a, because the composition of all three regions are identical. (Ex. 1003 at ¶¶98-100.) FIGS. 8 and 11 are shown annotated below.

-00550: Petition [1] at 49-50

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Onoda’s dopant profile is graded below the “surface layer.”



-00550: Petition [1] at 52

Onoda’s FIG. 11 depicts the graded dopant profile across the p-type well regions 105a, 105b, 105c, which constitutes the “at least one graded dopant concentration” of the “at least a portion of at least one of the first and second active regions.” FIG. 11 is a cross sectional slice (B-B) through the device depicted in FIG. 8, which is the same embodiment as FIG. 3. (See, e.g., Onoda at [0041]-[0045]). As can be seen from the below, the dopant concentration decreases as a function of depth through the third well region 105a (p-type) and the second semiconductor layer 102 (p-type). Then, at the point where the slice reaches the semiconductor layer 101, the dopant concentration increases. (*Id.* at [0052]). Moreover, a POSITA would have understood that third well regions 105b and 105c would have the same dopant profile as region 105a, because the composition of all three regions are identical. (Ex. 1003 at ¶¶98-100.) FIGS. 8 and 11 are shown annotated below.

-00550: Petition [1] at 49

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Onoda is silent as to where the “active region” or “surface layer” begins and ends.

10/17/2024 Monolithic Power Systems Inc v. Greent
IN THE UNITED STATES PATENT AND
REPORT TIP PATENT TRIAL AND
MONOLITHIC POWER SYSTEMS)
INC.,)
Petitioner,)
v.)
GREENTHREAD, LLC,)
Patent Owner.)
RECORD DEPOSITION
STEPHEN A. CAMPBELL,
October 17, 202
9:00 a.m. Central Dayli
Reported by: Lori J. Coodin, RT
California CSR #13
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Washington, D.C.
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Greenthread Ex. 2088, p. 1 of 65
MPS v. Greenthread

2 Q. Dr. Campbell, can you tell me where
3 the active region would be on this graph?
4 A. The active region, as I mentioned
5 before, is coincident with the depth of the
6 source of drain.
7 This profile is showing the channel
8 doping and below. So, we don't see the source or
9 drain here.
10 So, I can't say exactly where the
11 active area would end.
12 But consistent with my previous
13 remarks, I believe the source drain depth was
14 about a half a micron.
15 So, with that, assertion, the active
16 area would go from 0 to 0.5 on this spot.

17 Q. Okay. But you can't be sure because
18 you are not sure of the depth of source and
19 drain?
20 A. That is correct.

Ex. 2058 (Campbell Dep. Tr.) at 52:2-20

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Onoda’s dopant profile does not begin to angle downward until below the “active region.”

10/17/2024 Mon
IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF COLUMBIA
MONOLITHIC POWER SYSTEMS, INC.,
Petitioner,
v.
GREENTHREAD, LLC,
Respondent.
Patent Case No. 2:24-cv-01055-MJD
REMOVAL DEPOSITION OF
STEPHEN A. CAMPBELL, PH.D.
October 17, 2024
9:30 a.m. Central Daylight Time
Reported by: Lori J. Coodin, RCR, CRR, RSA,
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Greenthread Ex. 2028, p. 1 of 65
MPS v. Greenthread

2 Q. Dr. Campbell, can you tell me where
3 the active region would be on this graph?
* * *
12 But consistent with my previous
13 remarks, I believe the source drain depth was
14 about a half a micron.
15 So, with that, assertion, the active
16 area would go from 0 to 0.5 on this spot.

Ex. 2058 (Campbell Dep. Tr.) at 52:2-16

22 Q. How would you describe this gradient?
23 A. The dopant file is shown on an X scale of
24 zero to six micrometers, UN or UM. The initial
25 portion on the left side approximately half a micron
1 appears to be flat. I don't see a downward slope.
2 Subsequent to the first half micron, it does slope
3 downward. Then, beyond five microns, the dopant
4 profile.

Case: Monolithic Power Systems, Inc. -v- Greenthread, LLC (PTAB)

Ex. 1055 (Glew Dep. Tr.)
at 91:22-92:4

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MPS EX. 1055

Greenthread Ex. 2088, p. 105 of 149
MPS v. Greenthread

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Onoda’s dopant profile does not exert a downward force in the “active region.”

Transcript of
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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

MPS EX. 1055

1 Q. I misspoke. Let me just re-ask. In the
2 vertical direction, looking at Figure 11, how would
3 you presume a force to be applied onto an electron in
4 the device of ONODA? Would it be upwards force,
5 downwards force, or net canceled? So zero force.
6 MR. WHITEHURST: Object to form.
7 THE WITNESS: To begin with, in the region
8 of zero to about half-a-micron in Figure 11, the
9 concentration appears to be flat or constant,
10 roughly, in terms of concentration. So there would
11 be no force in the first half-micron exerted by this
12 -- by a field generated by this dopant profile.
13 Beyond half-a-micron, the concentration decreases.

Ex. 1055 (Glew Dep. Tr.) at 94:1-13

9 Q. Looking at Figure 11, is it possible to
10 tell whether Figure 11 is capable of aiding the
11 movement of holes from the surface layer to the
12 substrate?
13 MR. BOMBACH: Objection. Leading.
14 THE WITNESS: Because the dopant profile is
15 flat, it does not generate an electric field near the
16 surface. It is flat near the surface. Thus, it
17 cannot move holes or electrons or any charged
18 carrier.

Ex. 1055 at 178:9-18

5. Onoda Does Not Move Carriers from the “Surface Layer”

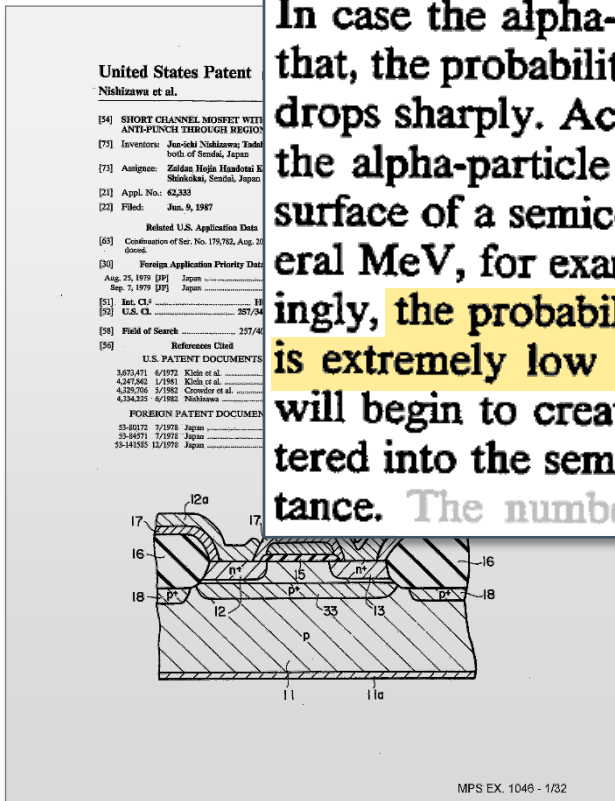
- Nishizawa does not address carriers at the surface; these can be “disregarded.”

into, for example, silicon. As shown in FIG. 33, when the alpha-particle gains an energy ϵ_3 of about 360 keV, it creates electron-hole pairs with highest probability. In case the alpha-particle gains an energy higher than that, the probability of generation of electron-hole pairs drops sharply. Accordingly, it will be understood that the alpha-particle immediately after irradiation to the surface of a semiconductor body has an energy of several MeV, for example about 5 MeV, and that, accordingly, the probability of creation of electron-hole pairs is extremely low near the surface. The alpha-particle will begin to create electron-hole pairs after it has entered into the semiconductor substrate to a certain distance. The number of electron-hole pairs which are

electrons is 1.9×10^6 . That is, the amount of electrons created which adversely affect the memory action is no greater than only 10% of the stored electric charge, and thus it can be disregarded.

Ex. 1046 at 20:19-11

Ex. 1046 (Nishizawa) at 19:21-34



5. Onoda Does Not Move Carriers from the “Surface Layer”

- Dr. Campbell explained that Nishizawa does not teach moving carriers downward from the “surface layer.”

13 Q. So, the electrons are coming,
14 Nishizawa is concerned with electrons coming up
15 from the substrate?
16 A. That is correct.

Ex. 2058 (Campbell Dep. Tr.) at 31:13-16

8 Q. And the focus of Kawagoe and
9 Nishizawa and Onoda, was to solve that problem
10 and block the carriers from coming up into the
11 substrate, or into the transistor?

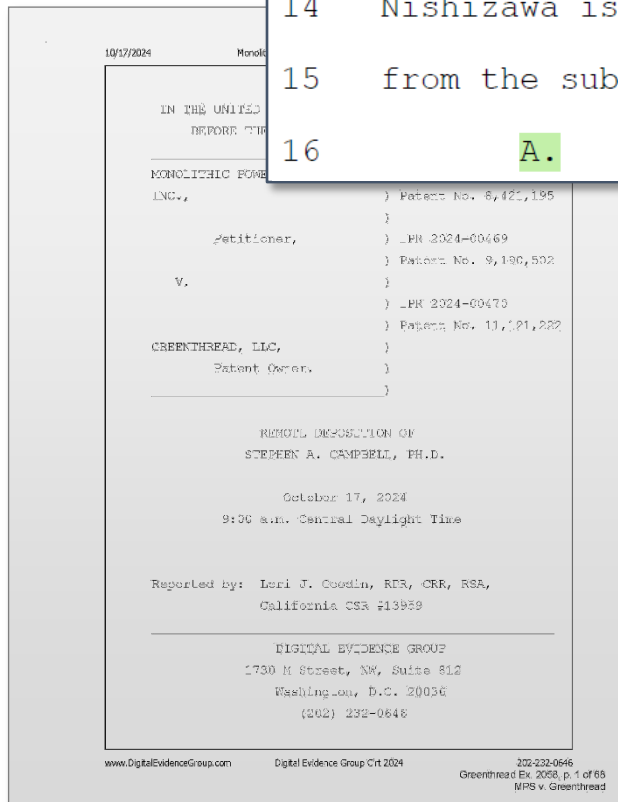
12 A. I would put it just slightly
13 differently. They are not saying that they are
14 totally blocking all of the carriers. They are
15 reducing the carrier flow to an acceptable level.

16 Q. Okay. But they are reducing the
17 carrier flow in an upwards direction?

18 A. Yes, that's correct.

19 Q. Upwards from the substrate?

20 A. Yes, that's correct.



5. Onoda Does Not Move Carriers from the “Surface Layer”

- Dr. Glew confirmed that Nishizawa does not teach moving carriers downward from the “surface layer.”

13 Q. What PN junction of Nishizawa are you
14 specifically referring to in paragraph 60?
15 A. In that I'm rebutting Dr. Campbell, I might
16 need to look at Dr. Campbell's declaration to put
17 better light on this. In general -- I'll give this
18 one more minute. Nishizawa is generally concerned
19 with, among other things, spurious electrons
20 generated by events, external events, and has created
21 a shield of sorts underneath the transistor.

Ex. 1055 (Glew Dep. Tr.) at 96:13-21

Case: Monolithic Power Systems, Inc. -v- GreenThread, LLC (P IAB)

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MPS EX. 1055

2 A. And to the extent that the whole purpose of
3 that feature 33A in Figure 35 is to keep electrons
4 from entering the transistor region and interfering
5 with the operation of NMOS device shown in 35, it is
6 a barrier to electrons entering from the substrate
7 upward. If it were to pull electrons down from the
8 operating transistor that would be, as I described
9 previously, deleterious to the functioning of an NMOS
10 device, robbing it of the majority of its electron
11 carriers, which are required for operation. So
12 either it would render it non-functional if it pulled
13 them down, or degrade the speed or performance of the
14 NMOS device.

Ex. 1055 at 98:2-14

8 Q. I'll ask this more simply. Looking at
9 Nishizawa column 18, lines 35 through 54, are you
10 able to tell me whether an electron generated by an
11 alpha particle hitting region 33A goes up, down, or
12 is fixed in place?
13 MR. WHITEHURST: Object to form.
14 THE WITNESS: Column 18 at the paragraph
15 beginning at line 35 describes that the electron that
16 enters region 33A is stopped from entering source
17 drain region 13. So to some extent, it is hindered
18 from vertical entry into the region 13.

Ex. 1055 at 106:8-18

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Because Onoda (and Nishizawa) do not expressly teach moving carriers from the “surface layer,” Petitioner had the burden to identify an electric field that would move carriers from the “surface layer.”

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In the absence of any teaching of the claim limitation in the prior art, Petitioner has two options: 1) it can read “aid carrier movement from the first surface” (or active region) out of the claim or 2) it can argue that any “graded dopant concentration” in the active region will “aid carrier movement.” Both options fail.

-00550: PO Response [32] at 2

5. Onoda Does Not Move Carriers from the “Surface Layer”

- Petitioner did not identify an electric field, much less an electric field starting at the surface layer.
- Petitioner’s only mention of “field” related to its erroneous prosecution history arguments.

f. Element [1.5]: “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.”

-00550: Petition [1] at 23, 49

The fact that a graded concentration aids the movement of carriers was a well-known property of semiconductor devices long before September 2004. (Ex. 1003, ¶¶103, 46-58.) Indeed, Patent Owner admitted that to be the case in prosecution, where Patent Owner, citing prior art, stated that “the graded dopant concentration itself creates a ‘built-in’ electrical field” and this “built-in” electric field “forces the movement of carriers into a particular direction, whereby the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.” (Ex. 1003, ¶¶47, 103.). The net effect of the graded dopant concentration is to cause carriers (e.g., electrons) to move from the top surface of the substrate 100 to the bottom surface of the layer 102, which is towards the second surface of the substrate 100. (Ex. 1003, ¶104.)

-00550: Petition [1] at 52-53

