Single Event Upset: An Embedded Tutorial

Fan Wang and Vishwani D. Agrawal
Dept. of Electrical and Computer Engineering, Auburn University, Auburn, AL, 36849, USA
Email: *wangfan@auburn.edu, vagrawal@eng.auburn.edu*

***Abstract*— With the continuous downscaling of CMOS technologies, the reliability has become a major bottleneck in the evolution of the next generation systems. Technology trends such as transistor down-sizing, use of new materials, and system on chip architectures continue to increase the sensitivity of systems to soft errors. These errors are random and not related to permanent hardware faults. Their causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation). To meet the system reliability requirements it is necessary for both the circuit designers and test engineers to get the basic knowledge of the soft errors. We present a tutorial study of the radiation-induced single event upset phenomenon caused by external radiation, which is a major source of soft errors. We summarize basic radiation mechanisms and the resulting soft errors in silicon. Soft error mitigation techniques with time and space redundancy are illustrated. An industrial design example, the IBM z990 system, shows how the industry is dealing with soft errors these days.**

I. Introduction

From the beginning of the recorded history, man has believed in the influence of heavenly bodies on the life on Earth. Machines, electronics included, are considered scientific objects whose fate is controlled by man. So, in spite of the knowledge of the exact date and time of its manufacture, we do not draft a horoscope for a machine. Lately, however, we have started noticing certain behaviors in the state of the art electronic circuits whose causes are traced to be external and to the celestial bodies outside our Earth. The *Single Even Upset* (SEU) phenomenon, as this non-permanent (i.e., random or soft) error behavior is termed, in digital systems affects the modern nanotechnology electronic devices. We believe SEU will assume greater importance in the future [12]. Sifting through the literature of the last half a century, we have collected the necessary material for a starter. Our aim is not to cram up these six pages with most information, but to provide the essentials that can be assimilated conveniently to help a reader to become an effective contributor. We begin with the definition.

> "**Single Event Upset (SEU):** Radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs". $\cdots$ *NASA Thesaurus*

The objective of this tutorial is to familiarize the reader with the SEU in digital electronics – definitions and terms, causes (mostly experimental), measurement and estimation, reliability standards, and the related design methods. You should expect to get almost complete, but not comprehensive, information. Looking over the Appendix on the last page will improve the comprehension as you read through this article.

We will present an up-to-date understanding of the SEU phenomena. Following the historical note of the following section, we summarize the concept of basic radiation mechanisms and explain how a soft error occurs in silicon in Section III. Examples of soft error mitigation techniques are presented in Section IV. In Section V, a case study of soft error detection and tolerance in IBM z990 system is given.

II. Historical Notes

Soft errors have been studied by electrical, aerospace, nuclear and radiation engineers for almost half a century. In the period 1954 through 1957 failures in digital electronics were reported during the above-ground nuclear bomb tests. These were treated as electronic anomalies in the monitoring equipment because they were random and their cause could not be traced to any hardware fault [27]. Perhaps the first paper concerning the role of cosmic rays on electronics is by Wallmark and Marcus [24]. As quoted in the recent literature [16], these authors predicted that cosmic rays would start upsetting microcircuits due to heavy ionized particle strikes and cosmic ray reactions when feature sizes become small enough. Through 1970s and early 1980s, the effects of radiation received attention and more researchers examined the physics of these phenomena. Also from 1950s, theories of fault tolerance and self-repairing computing were being developed due to the increased reliability requirement of critical applications like the space-mission [23].

May and Woods of Intel Corporation [13] determined that these errors were caused by the alpha particles emitted in the radioactive decay of uranium and thorium present just in few parts-per-million levels in package materials. Their paper represented the first public account of radiation-induced upsets in electronic devices at sea level and these errors were referred to as "soft errors". The term soft error was used to differentiate from the repeatable errors traceable to permanent hardware faults. Guenzer and Wolicki [10] reported that the error causing particles came not only from uranium and thorium but that nuclear reactions generated high energy neutrons and protons, which could also cause upsets in circuits. Because the title of their paper was "Single Event Upset of Dynamic RAMs by Neutrons and Protons", the term "SEU" has been in use ever since [10] (refer to [16]). In 1979, Ziegler and Lanford from IBM [28] predicted that cosmic rays could

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MPS EX. 1013 - 1/6

TABLE I

PROJECTED FAILURE RATE ON SRAM-BASED FPGAS APPLICATIONS DUE TO NEUTRON EFFECTS (ACTEL)

Application Examples	Altitude (feet)	Neutron Flux (relative)	FPGAs/ System	#upsets/1M-gate FPGA/day(.13μ)	MTBF[1] (hours)		FIT[1] (in million)	
					0.13μ	0.09μ	0.13μ	0.09μ
(1) Ground-based Communication Network	5000	1	512	4.19E-4	112	58	8.92	17.24
(2) Civilian Avionics System	30,000	$\sim$40	4	1.85E-2	324	162	3.09	6.17
(3) Military Avionics System	60,000	$>$160	16	8.33E-2	18	9	55.56	111.11

result in the same upset phenomenon in electronics (not only memories) even at sea level.

Recent *Soft Error Rate* (SER) testing result of SRAM-based FPGAs from Actel [1] shows a significant and growing risk of functional failures due to the corruption of configuration data, especially when the system has higher densities. Table I shows the failure rate projection for different applications without using any protection. The number of upsets per 1 million gates per day increases for cases (1) through (3) because of the altitude dependent increase in neutron flux density. The table includes projected failure rates for the 90nm process. It is expected that neutron-induced soft errors get worse by a factor of two as we move from 0.13μ to 0.09μ technology. Note that this table ignores alpha particle effects, which are also expected to be significant for nanometer technologies and will further increase the system failure rate.

The radiation induced soft errors have become one of the most important and challenging failure mechanisms in modern electronic devices. SER of commercial chips is controlled to within 100~1000 FITs[1]. Compared to most hard failure mechanisms that produce failure rates on the order of 1~100 FIT, the SER of a low-voltage embedded SRAM can easily be 1000 FIT/Mbit. Therefore, a four-phase approach to deal with them is in progress [21]:

1) Methods to protect chips from soft errors (prevention).
2) Methods to detect soft errors (testing).
3) Methods estimate the impact of soft errors (assessment).
4) Methods to recover from soft errors (recovery).

III. WHAT IS SOFT ERROR?

A. Soft Error Categories

An electronic circuit, that bears no permanent hardware fault, may witness unexplained events resulting in single bit changes spontaneously in the system, and there is no way to repeat such failures. Within the computer industry such phenomenon is known as a "soft fail", to differentiate from the "hard or permanent fail", which may be repairable [28]. After observing a soft error, there is no implication that the system hardware is any less reliable than before because the soft fail is completely random. These soft fails may be caused by the well-known electronic noise sources such as a noisy power supply, lighting, and electrostatic discharge (ESD), or the thermal radiation from the galaxy, such as from radiation-emitting stars and atmospheric gases. A soft or non-permanent fault is a non-destructive fault and falls into two categories [22]:

1) Transient faults, caused by environmental conditions like temperature, humidity, pressure, voltage, power supply, vibrations, fluctuations, electromagnetic interference, ground loops, cosmic rays and alpha particles.
2) Intermittent faults caused by non-environmental conditions like loose connections, aging components, critical timing, power supply noise, resistive or capacitive variations or couplings, and noise in the system.

With advances in the design and manufacturing technology, non-environmental conditions may not affect the sub-micron semiconductor reliability. However, the errors caused by cosmic rays and alpha particles remain the dominant factors causing errors in electronic systems.

B. Radiation Mechanisms in Semiconductors

Three principal radiation sources cause soft errors in advanced semiconductor devices [5]:

1) Alpha particles are emitted when the nucleus of an unstable isotope decays to a lower energy state. They contain kinetic energy in the range of 4 to 9 MeV. There are many radioactive isotopes, however, uranium and thorium have the highest activity among naturally occurring materials. In the terrestrial environment, major sources of alpha particles are radioactive impurities such as lead-based isotopes in solder bumps of the flip-chip technology, gold used for bonding wires and lid plating, aluminum in ceramic packages, lead-frame alloys and interconnect metalization [8].
2) High-energy (>1 MeV) neutrons from cosmic radiation can induce soft errors in semiconductor devices via secondary ions produced by the neutron reaction with silicon nuclei. Cosmic rays that are of galactic origin react with the Earth's atmosphere to produce complex cascades of secondary particles. Less than 1% of the primary flux reaches ground level and the predominant particles include muons, neutrons, protons, and pions. Because pions and muons are short-lived and proton and electrons are attenuated by Coulombic interaction with the atmosphere, neutrons are the most likely cosmic radiation sources to cause SEU in deep-submicron semiconductors at terrestrial altitude. The neutron flux is dependent on the altitude above the sea level, the density of the neutron flux increases with altitude.
3) The third significant source of ionizing particles in electronic devices is the secondary radiation induced from the interaction of cosmic ray neutrons and boron. It is the radiation induced by low-energy cosmic neutron interactions with the isotope *boron-10* (^{10}B is commonly used as *p*-type dopant for junction formation

[1]See Appendix

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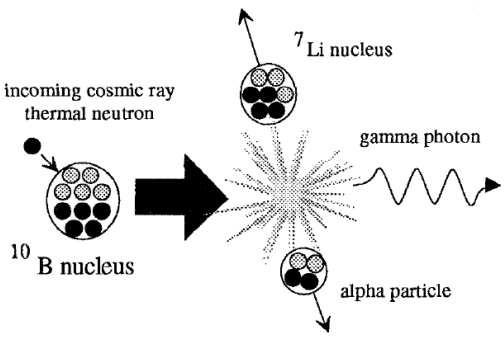

Fig. 1. Fission of ^{10}B induced by the capture of a neutron (commonly happened in SRAMs) [3].

in IC package). Specifically, BPSG (*Borophosphosilicate glass*) dielectric layer is commonly used to form insulator layers in IC manufacturing. Boron has two isotopes: ^{10}B and ^{11}B of which ^{10}B is unstable. The reaction scheme is shown in Figure 1. In the $^{10}B(n,\alpha)$ Li reaction the lithium nucleus is emitted with a kinetic energy of 0.84 MeV 94% of the time and 1.014 MeV 6% of the time. The gamma photon has energy of 478 KeV, while the alpha particle is emitted with an energy of 1.47 MeV [3]. This mechanism has recently been found to be the dominant source of soft errors in 0.25 and 0.18μ SRAM fabricated with BPSG. Modern microprocessors use highly purified package materials and this radiation mechanism is greatly reduced, making the high-energy cosmic rays the major reason for soft errors.

C. Sensitive Regions in Silicon

A *single event transient* (SET) is caused by the generation of charge due to a single particle (proton or heavy ion) passing through a sensitive node in the circuit. SETs in linear devices differ significantly from other types of *single event effects* (SEE) like SEU in a memory. Each SET has its unique characteristics like polarity, waveform, amplitude, duration, etc. These characteristics depend on particle impact location, particle energy, device technology, device supply voltage and output load. In CMOS circuits, the "off" transistors struck by a heavy ion in the junction area are most sensitive to SEU by particles with high enough LET (*linear energy transfer*; see Appendix) of around 20 MeV-cm^2/mg. When these particles hit the silicon bulk, the minority carriers are created and if collected by the source/drain diffusion regions, the change of the voltage value of those nodes occurs [20]. A particle can induce SEU when it strikes at the channel region of an off NMOS transistor or the drain region of an off PMOS transistor. The ionization can induce a current pulse in a p-n junction. Conceptually, when the charge injected by the current pulse at a sensitive node exceeds the critical charge (Q_{crit}), a SET is generated at the affected junction.

D. Single Event Transient

In Figure 2, an SET is produced after an energetic ionizing particle has been brought to the silicon near sensitive device

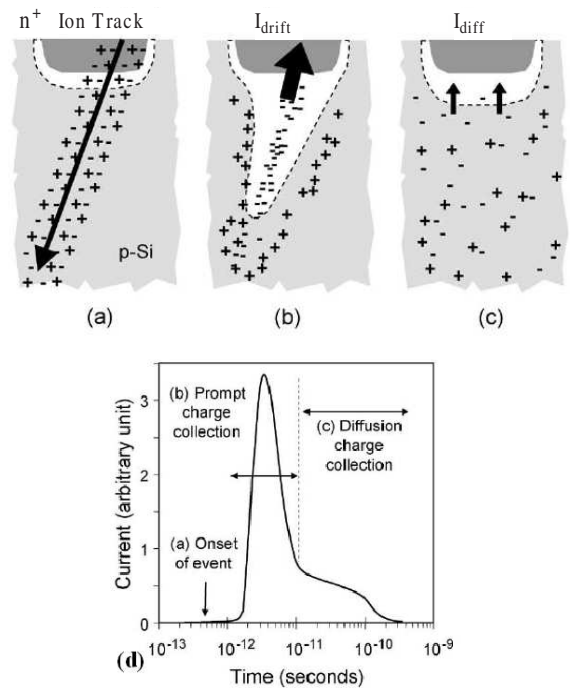

Fig. 2. Schematic representation of charge collection in a silicon junction immediately after (a) an ion strike, (b) prompt (drift) collection , (c) diffusion collection, (d) the junction current induced as a function of time [4].

nodes [4]. Along the traversed path, the particle produces a dense radial distribution of electron-hole pairs as illustrated in Figure 2(a). If the resultant ionization track traverses the depletion region, carriers are rapidly collected by the electric field, thus compensating the charge stored in the junction. Outside the depletion region the non-equilibrium charge distribution induces a temporary funnel-shaped potential distortion along the trajectory of the event, thus further enhancing charge collection by drift (Figure 2(b)). A "prompt" collection phase typically follows for tens of picoseconds and as the funnel collapses, diffusion then dominates the collection process (Figure 2(c)) until all excess carriers have been collected, recombined, or diffused away from the junction area (about nanoseconds). The transient charge collected from the radiation event produces a current pulse at the junction as illustrated in Figure 2(d) [4]. The current transient typically lasts 200 picoseconds with the bulk of the charge collection occurring within 2~3 microns of the junction region for modern submicron CMOS technologies. The time constants depend strongly on the type of ion, its initial energy and the properties of the specific technology [4]. If enough charge is collected by a node the data state may change. The collected charge (Q_{coll}) is a function of the ionizing particle's energy and trajectory, silicon substrate structure and doping, and the local electric field [4].

A commonly used approximate analytical model for the induced transient current waveform for ion track charge collection has a double-exponential form [15] with a rapid rise

MPS EX. 1013 - 3/6

time and a gradual fall time:

$$\begin{cases} I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) & \text{(a)} \\ Q_{coll} = 10.8 \times L \times LET & \text{(b)} \end{cases} \quad (1)$$

where Q_{coll} is the collected charge (in femto coulomb) in the sensitive region, τ_α is a process-dependent collection time constant of the junction, and τ_β is the ion-track establishment time constant, which is relatively independent of the technology. Typical values are approximately $1.64 \times 10^{-10} sec$ for τ_α and $5 \times 10^{-11} sec$ for τ_β [7]. In bulk silicon, a typical *charge collection depth* (L in micron) is 2 for every linear energy tranfer (LET) of 1 MeV-cm^2/mg, and an ionizing particle deposits about $10.8 fC$ charge along each micron of its track.

The induced transient voltage pulse may propagate through several levels of logic gates. Because a particle can induce an SEU when it strikes either the channel region of an off NMOS transistor or the drain region of an off PMOS transistor, we will consider the strike at an off PMOS drain area as an illustrative example. The critical charge depends on the total charge collected at the sensitive node as well as on the temporal shape of the current pulse and the device supply voltage. So, a parameter called "switching time (t_{th})" or "feedback time" is defined as the interval after the particle strikes at which the affected node voltage exceeds the threshold voltage. The charge on the output capacitor equals Q_{crit} at that time. Q_{crit} can be calculated by integrating the current that flows at the sensitive node after the strike [9]. The condition for the SEE to propagate is that output node voltage follows Equation 2.

$$V \geq \frac{Q_{crit}}{C} = \frac{1}{C}\int_0^{t_{th}} I_{drain}(t)dt \quad (2)$$

The pulse width of the voltage pulse depends on the value of the capacitance and the RC time constant of the discharging path. For example, in ami12 technology, when the output load capacitance is 100fF and the cumulative collected charge is 0.65pC, the amplitude of the voltage pulse is $0.65pC/100fF = 0.65 \times 10^{-12}C/100 \times 10^{-15}F = 0.65V$. We observe that for the same charge collected in the sensitive area a smaller load capacitance will have a larger amplitude of the SEE-induced voltage pulse. The discharge process can be modeled by a simple RC-circuit. So, the voltage as a function of time is $v(t) = v(0)^{\frac{-t}{RC}}$. Thus, smaller the RC value, faster is the discharge process. A schematic view of how the SEE-induced current pulse translates into an SEE-induced voltage pulse is given in Figure 3.

IV. Soft Error Mitigation Techniques

Soft error tolerant techniques can be classified into two types: prevention and recovery. The methods to protect microchips from soft-errors are the prevention methods. They are used during the chip design and development. The recovery methods include on-line recovery mechanisms from soft-errors in order to achieve the chip robustness requirement. These include fault tolerant computing, ECC/parity, online-testing and redundancy. One should note that soft error is not the only reason why computer systems need to resort to a

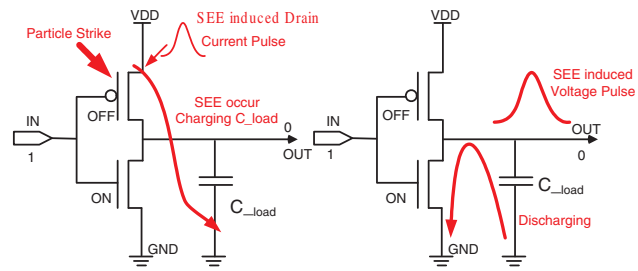

Fig. 3. An schematic view of how SEE-induced current pulse translates into a voltage pulse in a CMOS inverter.

recovery procedure. Random errors due to noise, unreliable components, and coupling effects may also require recovery mechanisms [21]. The need for a recovery mechanism stems from the fact that prevention techniques may not be enough for contemporary microchips, because the supply voltage keeps reducing, feature size keeps shrinking, and the clock frequency keeps increasing. Also, the cost of prevention techniques for a fault tolerant design may be too high. Because the error-tolerant computing is a broad area, here we only give a few examples of techniques used for soft error mitigation. In addition, a built-in soft error resilience (BISER) technique for correcting radiation-induced soft errors in latches and flip-flops may be found [25]. In that work, the error-correcting latch and flip-flop designs are power efficient and can correct both flip-flop errors and combinational logic errors, and employ reuse of on-chip scan design-for-testability in cell-level SER.

A. Prevention Techniques

1) Purify the Fabrication Material: A significant improvement in the SER performance of microelectronics can be achieved by eliminating or reducing the sources of radiation. To reduce the alpha particle emission in the final packaged IC, high purity materials and processes are employed. Uranium and thorium impurities have been reduced below one hundred parts per trillion for high reliability. Going from the conventional IC packaging to an ultra-low alpha packaging materials the alpha emission is reduced from 5~10 alphas/cm^2-hr to less than 0.001 alphas/cm^2-hr. To reduce the SER induced by the ^{10}B activation by low energy neutrons, BPSG is replaced by other insulators that do not contain boron. In addition, any processes using boron precursors is carefully checked for ^{10}B content before introducing them to manufacturing process [4]. When these measures are employed the SER of the IC is reduced dramatically, but the SER caused by the cosmic high energy neutron interactions cannot be easily shielded.

2) Radiation Hardened Process Technologies: SER performance can be greatly improved by adapting the process technology either to reduce the collected charge (Q_{coll}) or increase the critical charge (Q_{crit}) [26]. One approach is to use additional well isolation (triple-well or guard-ring structure) to reduce the amount of charge collected by creating potential barriers, which can limit the efficiency of the funneling effect and reduce the likelihood of parasitic bipolar collection paths [6].

MPS EX. 1013 - 4/6

Another approach replaces bulk silicon well-isolation with silicon-on-insulator (SOI) substrate material. The direct charge collection is significantly reduced in SOI devices because the active device volume is greatly reduced (due to thin silicon device layer on the oxide layer) [18]. Recent work shows a 10X reduction in SER achieved over conventional bulk devices when a fully depleted SOI substrate is used. Unfortunately, SOI substrates are more expensive than conventional bulk substrates and phenomena like parasitic bipolar action limit further reduction of SER [4]. Circuit-level solutions such as the addition of cross-coupled resistors and capacitors to decrease bit-line float time are also employed.

B. Recovery Techniques

Fault-tolerant computing methods have existed in the literature for quite some time [23] but have seen renewed interest due to the SEU phenomenon. On-line testing techniques are frequently used as recovery solutions for soft error mitigation. Specific techniques includes self-checking design [19], concurrent error detection for finite state machines (FSM) by signature monitoring, error detection and correction (EDAC) codes, and redundancy.

1) Redundancy: The basic idea of redundancy in design is to gain higher system reliability by sacrificing the minimality of time or space, or both. The classic triple modular redundancy (TMR) with a majority voter [2] continues to be widely used.

Mitra *et al.* [17] combine a self-checking design with time redundancy based on the C-element gate to compare two samples of the outputs signal from a combinational circuit at times t_0 and $t_0 + d$. The C-element has the ability to eliminate glitches at combinational outputs. Their error correction structure is illustrated in Figure 4. The space redundancy and time redundancy are often combined together to meet high fault-tolerance requirement with reduced hardware overhead, such as duplication and comparison instead of TMR.

2) ECC and Parity: Memories have a significant role in modern systems. Because of very high density of storage cells, a large memory is more sensitive to ionized particles than the logic. A simple solution for protecting a memory is to add parity bits to each memory word. During each write operation, a parity generator computes the parity bits of the data to be written with the data in the memory. If a particle strike alters the state of a single bit of a memory word, the error can be discovered by checking the parity code during the read operation. Depending on the number of parity bits used, this scheme may only detect an error, or correct it as well. Such schemes are often combined with system-level approachs for error recovery [19]. In most situations, however, the error recovery in a memory is more complex so protection of the memory by means of codes, like error correcting code (ECC), is preferable. Table II summarizes sample EDAC methods for memory, data and systems [11].

TABLE II
SAMPLE EDAC METHODS FOR MEMORY OR DATA DEVICES [11]

EDAC Method	EDAC Capability
Parity	Single Bit Error Detect
Hamming Code	Single Bit Error Correct, double bit detect
RS Code	Correct consecutive and multiple bytes in error
Conventional Encoding	Corrects isolated burst noise in a communication stream
Overlying Protocol	Specific to each system implementation

V. A CASE STUDY

The IBM eServer z990 system is designed to detect and recover from both soft and permanent errors [14]. The z990 contains up to four pluggable nodes connected through a planar board in a daisy chain interconnect structure. Each node contains up to 64 GB physical memory and 32 MB L2 cache for a system capacity of 256 GB memory and 126 MB L2 cache. In IBM z990 system, microarchitecture-level SEU mitigation features include: extensive use of ECC and parity with retry on data and controls; full SRAM ECC and parity protection; operational retries; microprocessor mirroring, checkpointing and rollback, and some hardware derating techniques. These approaches may be useful for future mainframe, general purpose, and application-specific computing systems.

VI. CONCLUSION

Soft error rate in logic and and memory chips will continue to increase as devices become more sensitive to soft errors even at sea level. The logic FIT rate is expected to increase faster due to internal phenomena such as cross coupling, ground bounce and delay faults, becoming comparable to the prevailing FIT rate of memory. The IBM z990 system provides an illustration of how the soft error issue might be handled in the industry. Open soft error issues are in the areas of EDA tools, radiation tests and measurement, analysis of newer radiation mechanisms, device hardening, soft error rate analysis, and error mitigation methods, on which research is being conducted. We hope we have given a running start to our reader.

APPENDIX

Definitions and Terminology[2]

Collected Charge (Q_{coll}): The charge collected by a particular device node during the passage of a particle. The collected charge is dependent on the geometry and doping of the node, the particle property like mass, energy and trajectory, and the density and type of material in the volume being penetrated by the incident radiation.

Cross Section (σ): The device SEE response to ionizing radiation.Normally, the units for cross section are $cm^2/device$ or cm^2/bit.

Critical Charge (Q_{crit}): The minimum amount of charge that when collected at any sensitive node will cause the node to change state. The critical charge is usually generated by incident radiation and, it is dependent on the linear energy transfer effective which is usually a function of the angle of incident particle radiation.

LET: Linear Energy Transfer. LET is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material. The common unit is MeV-cm^2/mg of material (Si for MOS devices).

LET$_{th}$: LET threshold (LET_{th}) is the minimum LET to cause an effect at a given particle fluence.

SEE: Single Event Effect. Any measurable or observable change in state or performance of a microelectronic device, component, subsystem or system resulting from a single energetic particle strike. SEE includes **SEU** (Single

[2]These miscellaneous definitions and terms are collected from JEDEC standard and relevant papers.

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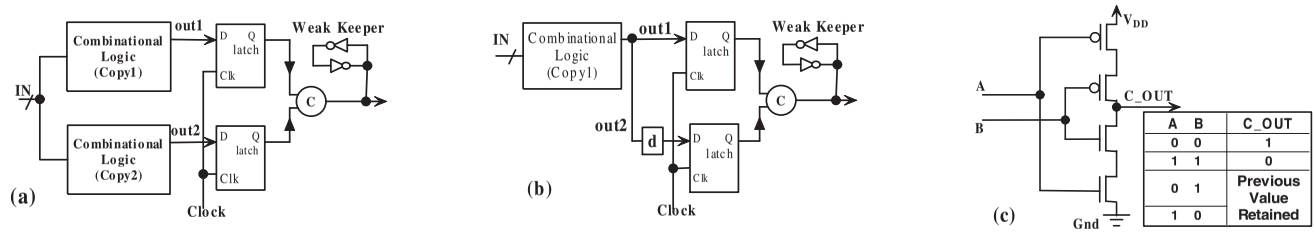

A	B	C_OUT
0	0	1
1	1	0
0	1	Previous Value Retained
1	0	

Fig. 4. Error correction using duplication, (a) space redundancy structure, (b) time redundancy structure, and (c) C-element [17].

Event Upset), **SEL** (Single Event Latchup), **SEB** (Single Event Burnout), **SEFI** (Single Event Functional Interrupt), and **SET** (Single Event Transient).

Sensitive Volume: A region, or multiple regions affected by SEE-induced radiation. The sensitive volume is determined by the angle of the incident radiation, the mass and energy of the incident particles and the density, type of the material in the volume being penetrated by the incident radiation. Is is not easy to know the geometry of the sensitive volume of the device but some information can be gained from the test cross section data.

Units and Conversion Factors

Energy Unit: Electron Volt (eV) One eV is the energy gained by one electron in accelerating through a potential difference of 1 volt. Energy in radiation is usually in unit of MeV (10^6eV) or KeV (10^3eV). 1eV = 1.6×10^{-19} J, 1MeV = 1.6×10^{-13} J.

FIT: Failure in Time; the number of failures per 10^9 device hours. 1 year MTTF (Mean Time To Failure) = $10^9/(24\times365)$ FIT = 114,155 FIT.

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MPS EX. 1013 - 6/6