

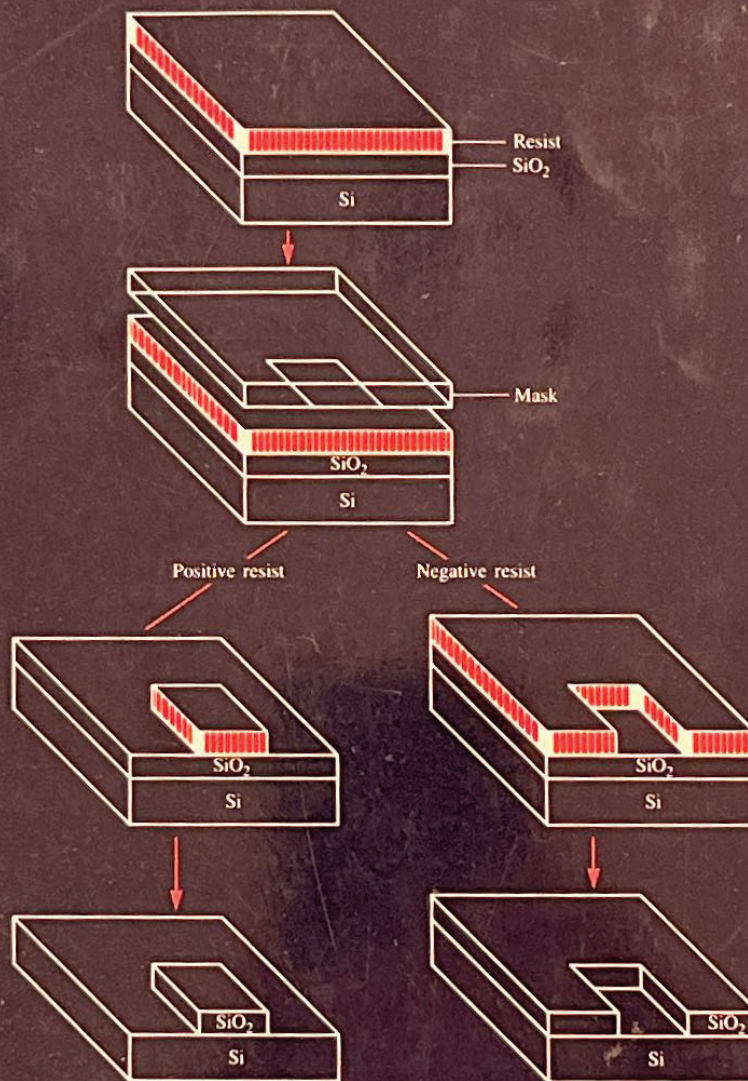
VOLUME V

INTRODUCTION TO MICROELECTRONIC FABRICATION

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6.4 EPITAXY

Chemical vapor deposition processes can be used to deposit silicon onto the surface of a silicon wafer. Under appropriate conditions, the silicon wafer acts as a seed crystal, and a single-crystal silicon layer is grown on the surface of the wafer. The growth of a crystalline silicon layer from the vapor phase is called *vapor-phase epitaxy* (VPE), and it is the most common form of epitaxy used in silicon processing. In addition, *liquid-phase epitaxy* (LPE) and *molecular-beam epitaxy* (MBE) are being used widely in GaAs technology.

Epitaxial growth was first used in integrated-circuit processing to grow single-crystal n -type layers on p -type substrates for use in standard buried-collector bipolar processing. More recently, it has been introduced into CMOS VLSI processes where lightly doped layers are grown on heavily doped substrates of the same type (n on n^+ or p on p^+) to help suppress a circuit-failure mode called *latchup*.

6.4.1 Vapor-Phase Epitaxy

Silicon epitaxial layers are commonly grown with silicon deposited from the gas phase. A basic model for the process is given in Fig. 6.9. At the silicon surface, the flux J_s of gas molecules is determined by

$$J_s = k_s N_s \quad (6.22)$$

in which k_s is the surface-reaction rate constant and N_s is the surface concentration of the molecule involved in the reaction. In the steady state, this flux must equal the flux J_g of molecules diffusing in from the gas stream. The flux J_g may be approximated by

$$J_g = (\bar{D}_g/\delta)(N_g - N_s) = h_g(N_g - N_s) \quad (6.23)$$

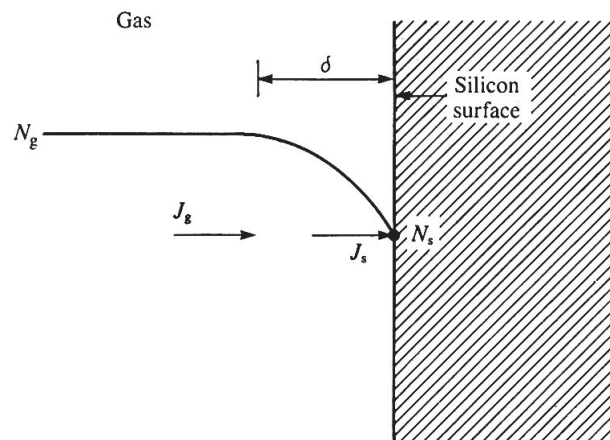


Fig. 6.9 Schematic model for the epitaxial growth process.

in which $\bar{D}_g$ is an effective diffusion constant for the gas molecule and δ is the distance over which the diffusion is taking place. The ratio $\bar{D}_g/\delta$ is called the *vapor-phase mass-transfer coefficient*, h_g . Equating J_s and J_g yields the flux impinging on the surface of the wafer. The growth rate is equal to the flux divided by the number N of molecules incorporated per unit volume of film.

$$v = \frac{J_s}{N} = \frac{k_s h_g}{k_s + h_g} \frac{N_g}{N} \quad (6.24)$$

If $k_s \gg h_g$, then growth is said to be mass-transfer-limited, and

$$v = h_g \frac{N_g}{N} \quad (6.25)$$

If $h_g \gg k_s$, then growth is said to be surface-reaction-limited, and

$$v = k_s \frac{N_g}{N} \quad (6.26)$$

Figure 6.10 shows epitaxial growth rate as a function of temperature. Chemical reactions at the surface tend to follow an Arrhenius relationship characterized by an activation

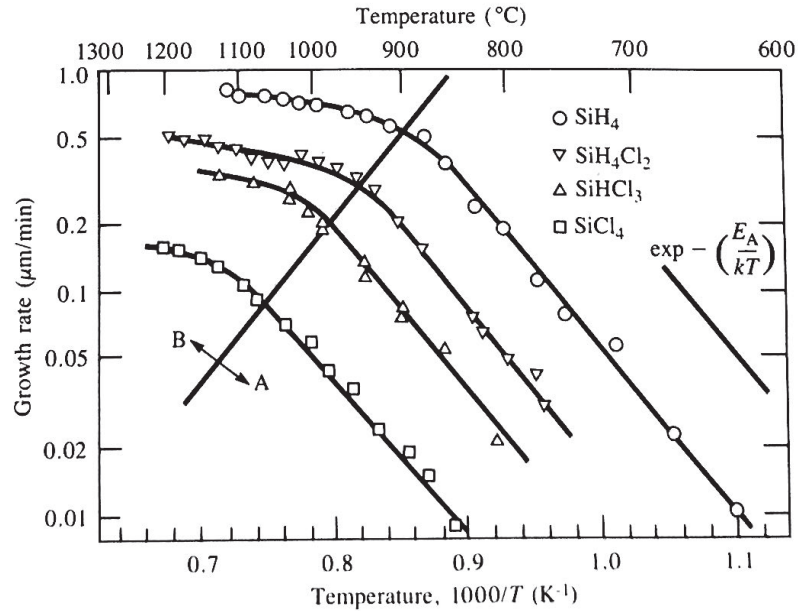


Fig. 6.10 Temperature dependence of the silicon epitaxial growth process for four different sources. The growth rate is surface-reaction-limited in region A and is mass-transfer-limited in region B. Reprinted with permission from Philips Journal of Research from ref. [3].

energy E_A , whereas the mass-transfer process tends to be independent of temperature. These two regions show up clearly in this figure. At low temperatures, the growth rate follows an Arrhenius relationship with an activation energy of approximately 1.5 eV. At higher temperatures, the growth rate becomes independent of temperature. In order to have good growth-rate control and to minimize sensitivity to variations in temperature, epitaxial growth conditions are usually chosen to yield a mass-transfer-limited growth rate.

Three common types of VPE reactors, the horizontal, vertical, and barrel systems, are shown in Fig. 6.11. The susceptor that supports the wafers is made of graphite and is heated by RF induction in the horizontal and vertical reactors and by radiant heating in the barrel reactor.

Silicon tetrachloride (SiCl_4), silane (SiH_4), dichlorosilane (SiH_2Cl_2), and trichlorosilane (SiHCl_3) have all been used for silicon VPE. Silicon tetrachloride has been widely used in industrial processing:



This reaction takes place at approximately 1200 °C and is reversible. If the carrier gas coming into the reactor contains hydrochloric acid, etching of the surface of the silicon wafer can occur. This in situ etching process can be used to clean the wafer prior to the start of epitaxial deposition.

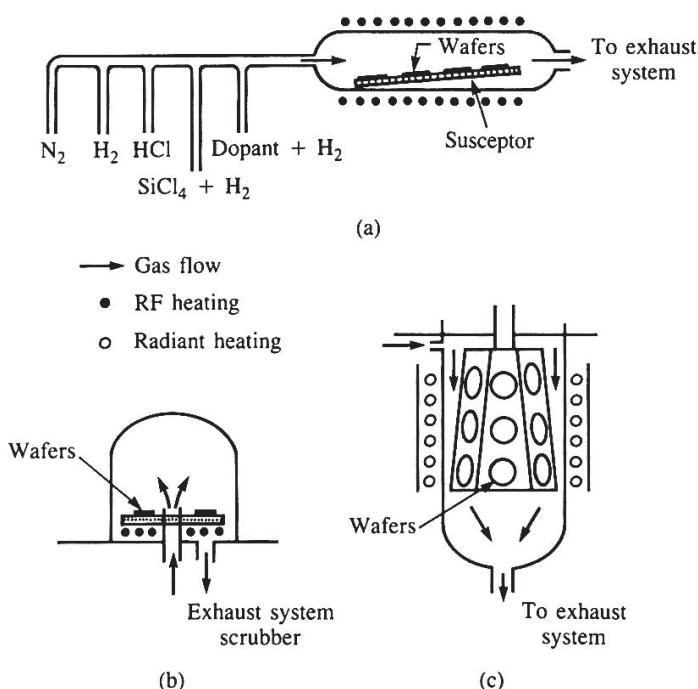


Fig. 6.11 (a) Horizontal, (b) pancake, and (c) barrel susceptors commonly used for vapor-phase epitaxy. Copyright, 1985, John Wiley & Sons, Inc., with permission from ref. [1].

A second reaction competes with the epitaxial deposition process:



This second reaction also etches the silicon from the wafer surface. If the concentration of SiCl_4 is too high, etching of the wafer surface will take place rather than epitaxial deposition. Figure 6.12 shows the effect of SiCl_4 concentration on the growth of epitaxial silicon. The growth rate initially increases with increasing SiCl_4 concentration, peaks, then decreases. Eventually, growth stops and the etching process becomes dominant. If the growth rate is too high, a polysilicon layer is deposited rather than a layer of single-crystal silicon.

Epitaxial growth can also be achieved by the pyrolytic decomposition of silane:



The reaction is not reversible and takes place at low temperatures. In addition, it avoids the formation of HCl gas as a reaction by-product. However, careful control of the reactor is needed to prevent formation of polysilicon rather than single-crystal silicon layers. The presence of any oxidizing species in the reactor can also lead to contamination of the epitaxial layer by silica dust.

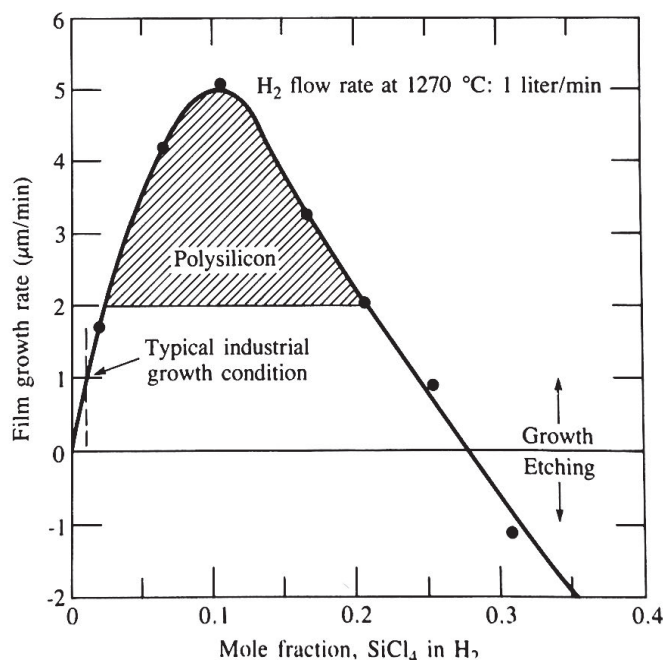


Fig. 6.12 Silicon epitaxial growth rate as a function of SiCl_4 concentration. Polysilicon deposition occurs for growth rates exceeding $2 \mu\text{m/min}$. Etching of the surface will occur for mole fraction concentrations exceeding 28%. Copyright, 1985, John Wiley & Sons, Inc., with permission from ref. [1].

6.4.2 Doping of Epitaxial Layers

Epitaxial layers may be doped during the growth process by adding impurities to the gas used for deposition. Arsine, diborane, and phosphine are the most convenient sources of the common impurities. The resistivity of the epitaxial layer is controlled by varying the partial pressure of the dopant species in the gas supplied to the reactor. The addition of arsine or phosphine tends to slow down the rate of epitaxial growth, while the addition of diborane tends to enhance the epitaxial growth rate.

Lightly doped epitaxial layers are often grown on more heavily doped substrates, and "autodoping" of the epitaxial layer can occur during growth. Impurities can evaporate from the wafer or may be liberated by chlorine etching of the surface during deposition. The impurities are incorporated into the gas stream, resulting in doping of the growing layer. As the epitaxial layer grows, less dopant is released from the wafer into the gas stream, and the impurity profile eventually reaches a constant level determined by the doping in the gas stream.

During deposition, the substrate also acts as a source of impurities which diffuse into the epitaxial layer. This "out-diffusion" will be discussed more fully in the next section. Both autodoping and out-diffusion cause the transition from the doping level of the substrate to that of the epitaxial layer to be less abrupt than desired. The effects of autodoping and out-diffusion are illustrated in Fig. 6.13.

6.4.3 Buried Layers

Out-diffusion is a common problem that occurs with the buried layer in bipolar transistors. In order to reduce the resistance in series with the collector of the bipolar transistor, heavily doped n -type regions are diffused into the substrate prior to the growth of an n -type epitaxial layer. During epitaxy, impurities diffuse upward from the heavily doped buried-layer regions.

Diffusion of impurities from the substrate during epitaxial growth is modeled by the diffusion equation with a moving boundary,^[4] as in Fig. 6.14:

$$D \frac{\partial^2 N}{\partial x^2} = \frac{\partial N}{\partial t} + v_x \frac{\partial N}{\partial x} \quad (6.30)$$

in which v_x is the rate of growth of the epitaxial layer.

Two specific solutions of eq. (6.30) are applicable to epitaxial layer growth. The first case is the growth of an undoped epitaxial layer on a uniformly doped substrate. The boundary conditions are $N(x, 0) = N_s = N(\infty, t)$, and the flux $J_x = (h + v_x)N(0, t)$ where h is the mass-transfer coefficient which characterizes the escape rate of dopant atoms from the silicon into the gas. Normally, $h \ll v_x$. A change of variables from x to $x' = x - v_x t$ simplifies eq. (6.30) and gives an approximate solution for $N(x, t)$:

$$N_1(x, t) = \frac{N_s}{2} \left[1 + \operatorname{erfc} \frac{x - x_{\text{epi}}}{2\sqrt{D_{st}}} \right] \quad (6.31)$$

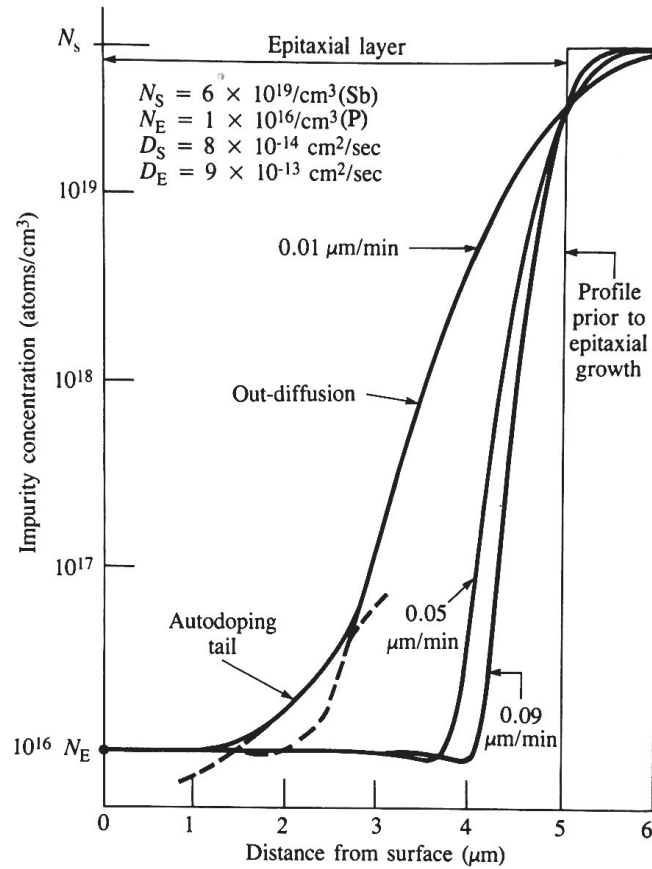


Fig. 6.13 Redistribution of impurity atoms due to gas-phase autodoping and impurity out-diffusion during epitaxial layer growth. Out-diffusion is calculated using eq. (6.33) for epitaxial growth of a phosphorus-doped layer at 1150 °C over an antimony-doped buried layer with a surface concentration of $6 \times 10^{19}/\text{cm}^3$. The three curves are for growth rates of 0.01, 0.05, and 0.09 $\mu\text{m}/\text{min}$. For clarity, the effects of autodoping are shown on only one curve.

Eq. (6.31) assumes that the epitaxial layer growth rate greatly exceeds the rate of movement of the diffusion front. Eq. (6.31) is the exact solution for diffusion from one semi-infinite layer into a second semi-infinite layer.

The second case is the growth of a doped epitaxial layer on an undoped substrate. The boundary conditions for this case are $N(0, t) = N_E$, and $N(\infty, t) = 0 = N(x, 0)$. The solution of eq. (6.30) for these boundary conditions is:

$$N_2(x, t) = \frac{N_E}{2} \left[\operatorname{erfc} \frac{x - x_{\text{epi}}}{2\sqrt{D_E t}} + \exp \frac{v_x x}{D_E} \operatorname{erfc} \frac{x + x_{\text{epi}}}{2\sqrt{D_E t}} \right] \quad (6.32)$$

in which $x_{\text{epi}} = v_x t$ is the epitaxial layer thickness. Superposition of the solutions for

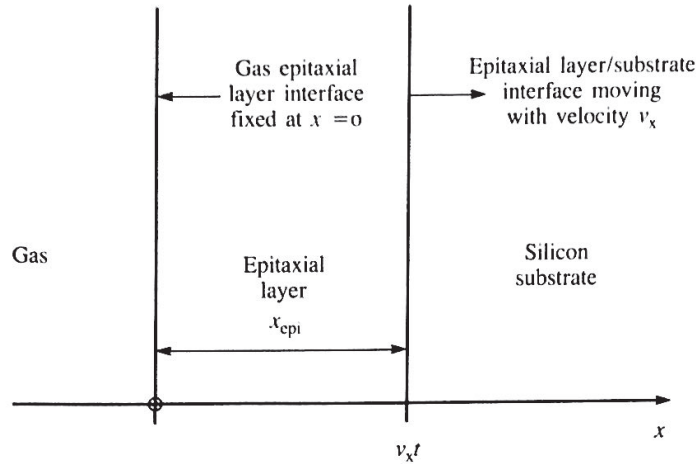


Fig. 6.14 Geometrical structure of moving boundary value problem which models the epitaxial growth process.

these two cases gives a good approximation to diffusion which occurs during epitaxial growth:

$$N(x, t) = N_1(x, t) + N_2(x, t) \quad (6.33)$$

N_s represents the doping in the substrate, and N_E is the doping intentionally introduced into the epitaxial layer. D_s and D_E represent the diffusion coefficients of the impurity species in the substrate and epitaxial layer, respectively. Figure 6.13 shows diffusion profiles for a phosphorus-doped epitaxial layer grown at various rates on an antimony-doped substrate. The curves were produced using eq. (6.33).

An additional problem occurs during epitaxial growth. The oxidation and lithographic processing steps used during formation of a buried layer result in a step of as much as $0.2 \mu\text{m}$ around the perimeter of the buried layer. Epitaxial growth on this nonplanar surface causes the pattern to shift during growth, as illustrated in Fig. 6.15. Pattern shift is difficult to predict, may be as large as the epitaxial layer thickness, and must be accounted for during the design of subsequent mask levels.

6.4.4 Liquid-Phase and Molecular-Beam Epitaxy

In liquid-phase epitaxy, the substrate is brought into contact with a solution containing the material to be deposited in liquid form. The substrate acts as a seed for material crystallizing directly from the solute. Growth rates typically range between 0.1 and $1 \mu\text{m}/\text{min}$.

In the molecular-beam epitaxy process, the crystalline layer is formed by deposition from a thermal beam of atoms or molecules. Deposition is performed in ultrahigh-

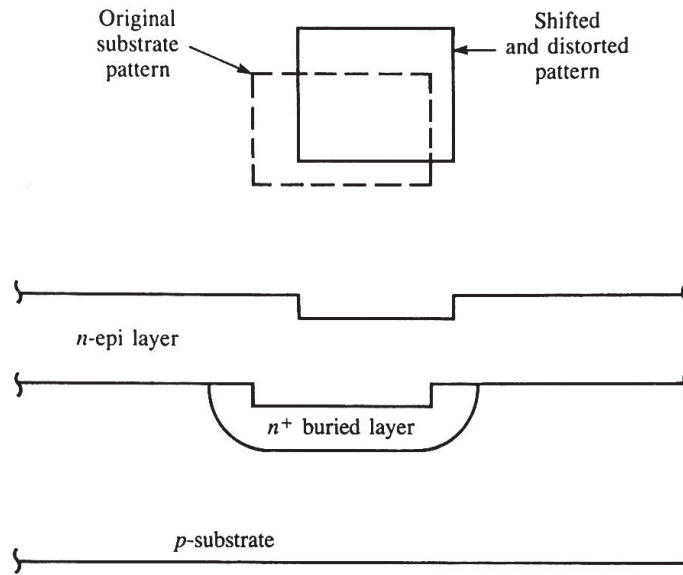


Fig. 6.15 Pattern shift during epitaxial growth over an n^+ buried layer. The original pattern is shifted and distorted in shape.

vacuum conditions (10^{-8} Pa). Substrate temperatures during MBE range from 400 to 900 °C, and the growth rate is relatively low (0.001 to 0.3 $\mu\text{m}/\text{min}$). The epitaxial layer is grown atomic layer by atomic layer, and many unique device structures can be fabricated by changing the material which is deposited between one layer and the next.

The throughput of MBE is relatively low at the present time. Plasma-assisted CVD processes, which promise to give many of the benefits of MBE with much higher throughput, are presently being investigated in research laboratories.

6.5 SUMMARY

Thin films of a very broad range of materials are used in integrated-circuit fabrication. This chapter has presented an overview of film-deposition techniques including physical evaporation, chemical vapor deposition (CVD), epitaxial growth, and sputtering. Most of these processes are performed at low pressure, and this chapter has presented an introduction to vacuum systems and a review of some important aspects of ideal gas theory.

Physical evaporation using filament or electron-beam evaporators can be used to deposit metals and other materials which can easily be melted. E-beam systems can operate at high power levels and melt high-temperature metals. However, E-beam evaporation may result in radiation damage to thin oxide layers at the surface of the wafer. In addition, it is difficult to deposit material compounds and alloys using evaporation. Finally, gas molecules at low pressures have large mean free paths, and evaporation has problems with shadowing and poor step coverage during film deposition.

Sputtering uses energetic ions such as argon to bombard a target material and dislodge atoms from the surface of the target. The dislodged atoms are deposited on the surface of the wafer. Direct-current sputtering systems can be used to deposit conductive materials, and RF sputtering can be used to deposit insulators. Sputtering can be used to deposit composite materials in which the deposited film maintains the same composition as the source material. Sputtering also uses higher pressures than evaporation. The much shorter mean free paths which result yield a deposition with freedom from shadowing and much better step coverage.

Low-pressure and atmospheric chemical vapor deposition (CVD) systems deposit films from chemical reactions taking place in a gas stream passing over the wafer. Polysilicon, silicon dioxide, silicon nitride, and metals can all be deposited using CVD techniques. A special type of CVD deposition called epitaxy results in the growth of single-crystal silicon films on the surface of silicon wafers. Out-diffusion and autodoping cause problems with impurity profile control during epitaxial layer growth.

In a modern bipolar or MOS fabrication process, one can expect to find evaporation, sputtering, and chemical vapor deposition techniques all used somewhere in the process flow.

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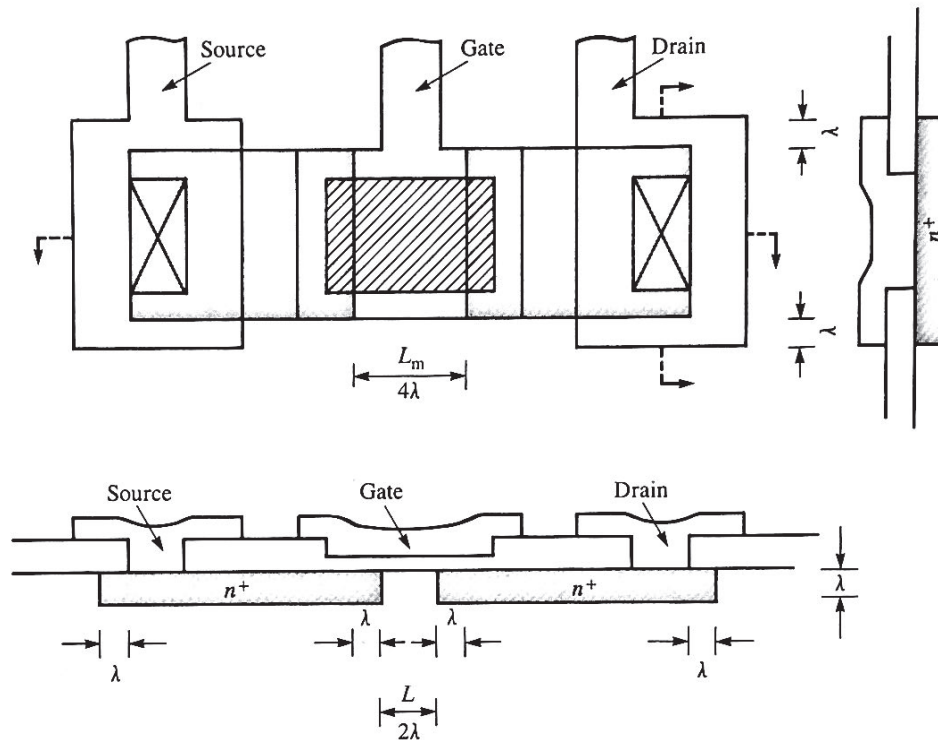


Fig. 9.13 Channel-length bias in a metal-gate NMOS device caused by lateral diffusion under the edge of the diffusion window. The transistor has $Z/L = 1/1$ at the mask level but ends up with an actual $Z/L = 2/1$ after the device is fabricated. Layout of the contact position is based on knowledge of the lateral diffusion which occurs during processing.

In sets of very tight design rules developed for high-volume-production ICs, all critical dimensions are adjusted to account for the processing and alignment sequences. This often results in a layout which must conform to a set of 50 to 100 design rules.^[7] Such a set of design rules is highly technology-specific and cannot be transferred from one generation of lithography to the next. The Mead-and-Conway-style rules^[7] reach a compromise between a set of rules which is overly pessimistic and wastes a lot of silicon area, and one that is extremely complex but squeezes out all excess area. The Mead-and-Conway-style design rules are being used for low-volume ICs in which design time, and not silicon area, is of dominant importance.

9.3 COMPLEMENTARY MOS (CMOS) TECHNOLOGY

The basic CMOS process of Fig. 1.5 requires a *p*-well diffusion and formation of both NMOS and PMOS transistors. Substrate resistivity is chosen to give the desired PMOS characteristics, and an additional implant step may be introduced to adjust the PMOS

threshold separately. The p -well-to-substrate junction may range from a few microns to as much as twenty microns in depth. The net surface concentration of the p -well must be high enough above the substrate concentration to provide adequate process control without severely degrading the mobility and threshold voltage of the NMOS transistors. The surface concentration of the p -well typically ranges between three and ten times the substrate impurity concentration. An additional implant step is often introduced to adjust the NMOS threshold voltage.

Parasitic bipolar devices are formed in the CMOS process in which merged pnp and nnp transistors form a four-layer ($pnpn$) lateral SCR, as shown in Fig. 9.14. If this SCR is turned on, the device may destroy itself via a condition called *latchup*.^[8,9] The p -well depth and the spacings between the source/drain regions and the edge of the p -well must be carefully chosen to minimize the current gain of the bipolar transistors and the size of the shunting resistors R_s and R_w . A CMOS process will have a number of additional ground rules which are not present in an NMOS or PMOS process. A more detailed discussion of the design of bipolar transistors will be given in Chapter 10.

In order to reduce the resistance of the two shunting resistors, "guard ring" diffusions are sometimes added to the process, as in Fig. 9.14. Guard rings can be formed using the source/drain diffusions of the PMOS and NMOS transistors or can be added as

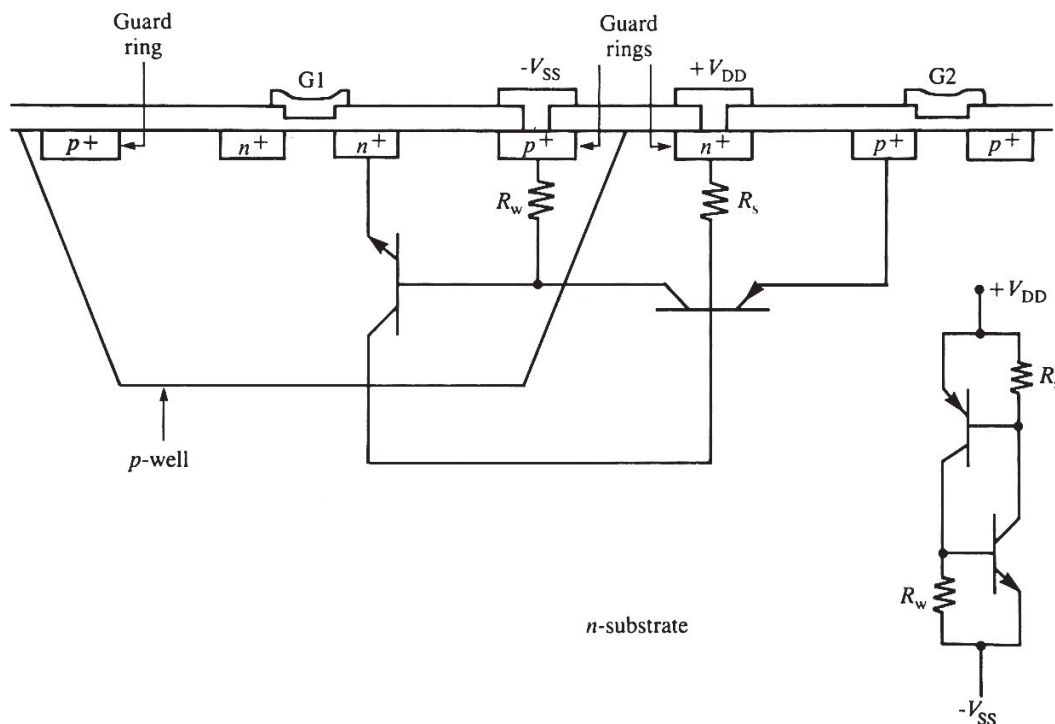


Fig. 9.14 Cross-section of a CMOS structure, showing the existence of a parasitic lateral $pnpn$ SCR and the use of guard rings to reduce the value of R_s and R_w .

separate diffusion steps. Recent CMOS processes have used an n -well version of this technology, which permits optimization of the NMOS devices fabricated in the original substrate.

Twin-well processes, such as in Fig. 9.15, permit separate optimization of both NMOS and PMOS devices.^[10] A lightly doped n - or p -type epitaxial layer is grown on a heavily doped n - or p -type substrate. (Lightly doped n - and p -type regions are often referred to as ν and π regions, respectively.) Separate implantations and diffusions are used to form wells for both the NMOS and PMOS transistors. The low-resistivity substrate substantially reduces the substrate resistance R_s and improves latchup resistance.

Example 9.2: A CMOS process uses an n -type substrate with a doping of $10^{15}/\text{cm}^3$. An implant/drive-in schedule will be used to form a p -well with a net surface concentration of $4 \times 10^{15}/\text{cm}^3$ and a junction depth of $7.5 \mu\text{m}$. (a) What is the drive-in time at 1150°C ? (b) Solve for the implanted dose in silicon. (c) What are the threshold voltages of the n - and p -channel transistors if the oxide thickness is 50 nm ?

Solution: The $7.5\text{-}\mu\text{m}$ junction depth and low surface concentration suggest that the well has a Gaussian profile resulting from a two-step diffusion or implant/diffusion process. A final surface concentration of $5 \times 10^{15}/\text{cm}^3$ is required to produce a net concentration of $4 \times 10^{15}/\text{cm}^3$ at the surface. Solving for the Dt product yields

$$Dt = x_j^2/2 \ln(N_0/N_B) = 8.74 \times 10^{-8} \text{ cm}^2$$

At 1150°C , $D = 8.87 \times 10^{-13} \text{ cm}^2/\text{sec}$, which gives $t = 27.5 \text{ h}$. The dose in silicon is given by $Q = N_0\sqrt{\pi Dt} = 2.62 \times 10^{12}/\text{cm}^2$. The p -channel devices reside in the n -type substrate with a doping concentration of $10^{15}/\text{cm}^3$. From Fig. 9.2, the threshold voltage will be -0.95 V . The deep well diffusion will be almost constant near the surface with a value of $4 \times 10^{15}/\text{cm}^3$. Figure 9.2 yields an n -channel threshold of 0.2 V . A threshold adjustment implant would be needed in this process to increase the n -channel threshold voltage.

9.4 OTHER MOS STRUCTURES

Chemical etching techniques may be used to crystallographically etch silicon. A solution of KOH, water, and alcohol^[11] etches the $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ crystal planes at relative rates of 40:30:1. This etch may be masked by silicon dioxide or silicon nitride and can be used to etch cavities and V-shaped grooves in $\langle 100 \rangle$ silicon (Fig. 9.16).

VMOS technology^[12] makes use of the grooves to reduce the channel length and increase the Z/L ratio of the MOS transistor. A basic VMOS process is shown in Fig. 9.17. The channel is formed along the four sides of the groove, and the channel length is determined by the thickness of the epitaxial layer and the diffusions. At the time VMOS was invented, channel lengths achievable with this technology were much shorter than those that could be achieved with normal planar technology, because the epitaxial

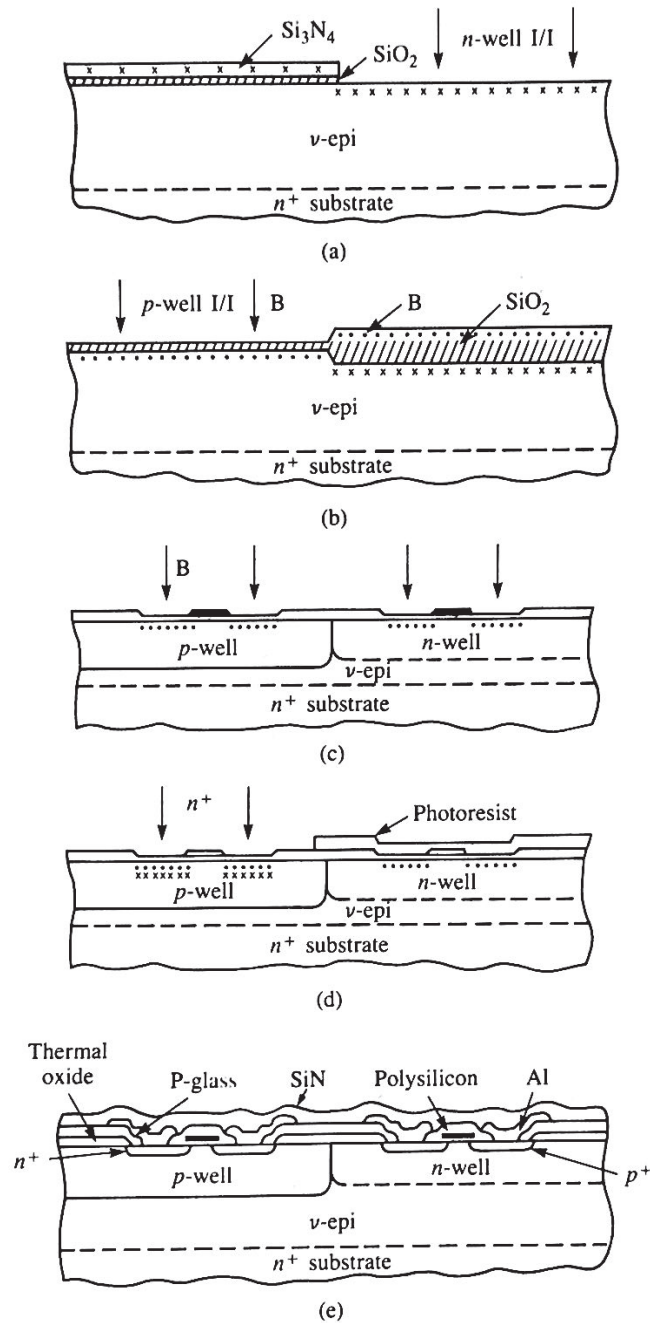


Fig. 9.15 Twin-well CMOS structure at several stages of the process. (a) n -well ion implant; (b) p -well implant; (c) nonselective p^+ source/drain implant; (d) selective n^+ source/drain implant using photoresist mask; (e) final structure. Copyright 1980 IEEE. Reprinted with permission from ref. [10].

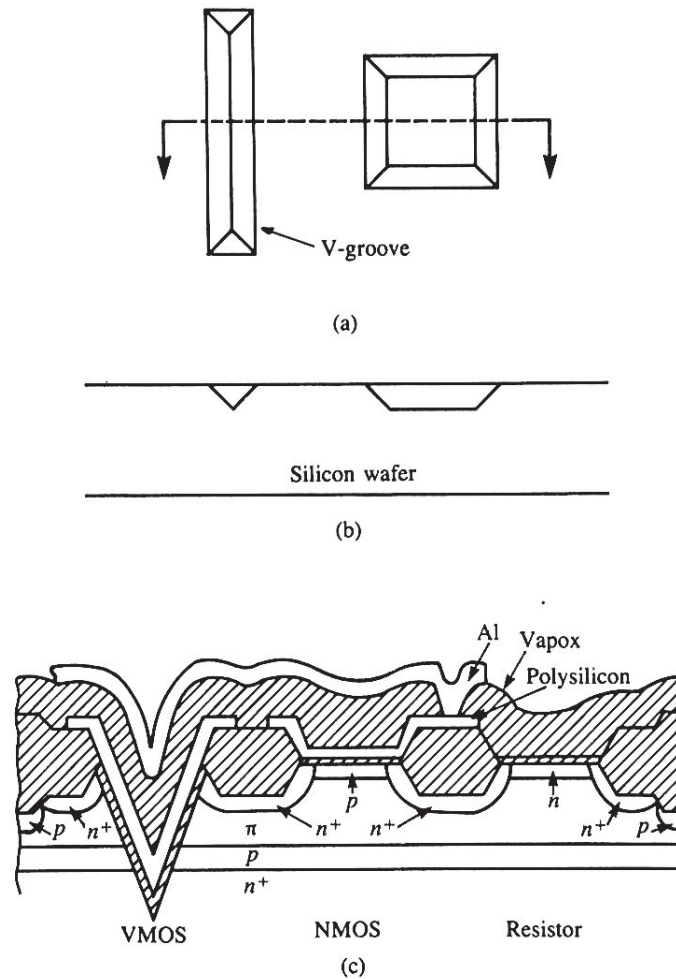


Fig. 9.16 Groove formation in the surface of (100) silicon using anisotropic etching of silicon. (a) Top view; (b) cross section; (c) use of a groove in the formation of a VMOS transistor. Copyright 1977 IEEE. Reprinted from ref. [12] with permission.

layer thickness was not limited by lithographic dimensions. Present-day MOS power transistors have improved and expanded the use of the ideas of the original VMOS structure.^[13]

9.5 SUMMARY

In this chapter we have explored the interaction of process design with MOS device characteristics and transistor layout, including the relationships between processing parameters and breakdown voltage, punch-through voltage, threshold voltage, and junction capacitance. A low value of substrate doping is desired to minimize junction

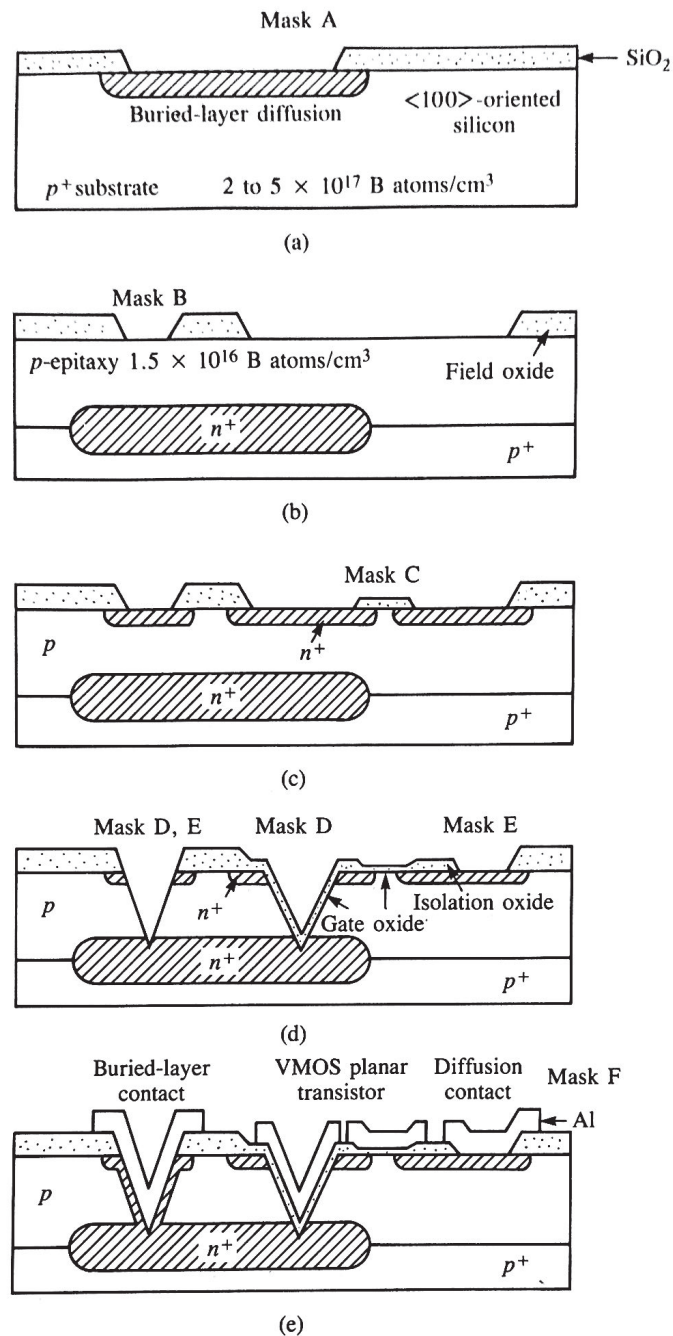


Fig. 9.17 Fabrication sequence for the formation of VMOS transistors for use in memory circuits. (a) Buried-layer diffusion; (b) epitaxial growth; (c) source/drain diffusion; (d) anisotropic etch and oxide growth; (e) metallization and pattern definition. Copyright 1978 IEEE. Reprinted with permission from ref. [17].

capacitance, substrate sensitivity, and junction breakdown voltage, whereas a high substrate doping is needed to maximize punch-through voltage. The use of ion implantation permits the designer to separately tailor the threshold voltage of the transistor.

We have developed basic ideas relating minimum feature size and alignment tolerances and have discussed simple sets of layout design rules. The strong relation between layout design rules and the size of transistors has been demonstrated. Polysilicon-gate technology has been shown to result in a much smaller device area than metal-gate technology for a given transistor Z/L ratio as well as to minimize the parasitic gate capacitance of the device. In addition, the polysilicon-gate process substantially reduces channel-length bias caused by lateral diffusion.

A combination of ion implantation and diffusion is commonly used to form the p - or n -well required for CMOS technology. VLSI CMOS often uses twin-well processes which permit separate optimization of both the n - and p -channel devices.

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