

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MONOLITHIC POWER SYSTEMS, INC.,

Petitioner,

v.

GREENTHREAD LLC,

Patent Owner.

PTAB CASE NO. IPR2024-00552

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,121,222
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104**

TABLE OF CONTENTS

I.	MANDATORY NOTICES.....	1
A.	Real Party-In-Interest	1
B.	Related Matters.....	1
C.	Counsel Service Information	3
D.	37 C.F.R. §42.8(b)(4): Service Information	4
II.	CLAIM LISTING.....	5
III.	PAYMENT OF FEES UNDER 37 C.F.R. §42.103	12
IV.	CERTIFICATION OF GROUNDS FOR STANDING.....	12
V.	OVERVIEW OF CHALLENGE AND RELIEF REQUESTED	12
A.	Printed Publications as Prior Art	13
B.	Relief Requested.....	13
VI.	PERSON OF ORDINARY SKILL IN THE ART	14
VII.	CLAIM CONSTRUCTION.....	14
VIII.	THE '222 PATENT AND BACKGROUND	14
A.	The '222 Patent	14
B.	General Background	15
IX.	SPECIFIC GROUNDS OF INVALIDITY	16
A.	Ground I: Kawagoe Renders Obvious Claims 1, 3-9, 13, 15-17, 20, 21, 24-28, 32-34, and 39-42 of the '222 Patent.	16
1.	Independent Claim 1	17
a.	Preamble [1.Pre].....	17
b.	Element [1.1]	17

c.	Element [1.2]	19
d.	Element [1.3]	22
e.	Element [1.4]	25
f.	Element [1.5]	26
g.	Element [1.6]	29
h.	Element [1.7]	32
2.	Claim 3	32
3.	Claim 4	33
4.	Claim 5	33
5.	Claim 6	35
6.	Claim 7	36
7.	Claim 8	37
8.	Claim 9	38
9.	Claim 13	38
10.	Claim 15	39
11.	Claim 16	39
12.	Claim 17	39
13.	Claim 20	39
14.	Independent Claim 21	40
15.	Claim 24	42
16.	Claim 25	42
17.	Claim 26	42
18.	Claim 27	42
19.	Claim 28	42
20.	Claim 32	42

Claim 32/7 are similar and taught for the same reasons.....	42
21. Claim 33	42
22. Claim 34	43
23. Claim 39	43
24. Claim 40	43
25. Independent Claim 41	44
26. Independent Claim 42	44
B. Ground II: Onoda Renders Obvious Claims 1, 3-9, 13, 15-17, 20, 21, 24-28, 32-34, and 39-42 of the '222 Patent.	45
1. Independent Claim 1	45
a. Preamble.....	45
b. Element [1.1]	46
c. Element [1.2]	47
d. Element [1.3]	51
e. Element [1.4]	53
f. Element [1.5]	54
g. Element [1.6]	62
h. Element [1.7]	65
2. Claim 3	65
3. Claim 4	66
4. Claim 5	67
5. Claim 6	68
6. Claim 7	70
7. Claim 8	70
8. Claim 9	72

9.	Claim 13	73
10.	Claim 15	75
11.	Claim 16	76
12.	Claim 17	76
13.	Claim 20	76
14.	Claim 21	76
a.	Element [21.7]	77
A.	Claim 24	78
B.	Claim 25	78
C.	Claim 26	78
D.	Claim 27	78
E.	Claim 28	78
F.	Claim 32	78
G.	Claim 33	78
H.	Claim 34	78
I.	Claim 39	78
J.	Claim 40	79
K.	Claim 41	79
L.	Claim 42	80
C.	Ground III: Onoda in view of Nishizawa Renders Obvious Claims 1, 3-9, 13, 15-17, 20, 21, 24-28, 32-34, and 39-42 of the '222 Patent.	80
1.	Claim 1	84
a.	Preamble	84
b.	Elements [1.1]-[1.4]	84
c.	Elements [1.5] and [1.6]	84

2.	Claims 21, 39, 40, 42.....	86
3.	Claims 13, 15, 33.....	86
4.	Claims 3-9, 15-17, 20, 24-28, 32, 34, and 40.....	86
X.	THE BOARD SHOULD INSTITUTE IPR.....	86
1.	35 U.S.C. § 314(a).....	86
2.	35 U.S.C. § 325(d).....	87
3.	Prior Petitions Do Not Warrant Denying Institution	89

TABLE OF AUTHORITIES

FEDERAL CASES

<i>Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH,</i> IPR2019- 01469.....	76
<i>Apple Inc. v. Uniloc 2017 LLC,</i> IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020).....	79
<i>Becton, Dickinson, & Co. v. B. Braun Melsungen AG,</i> IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017).....	76
<i>Bowtech Inc. v. MCP IP, LLC,</i> IPR2019-00383, Paper 14 (P.T.A.B. Aug. 6, 2019)	77
<i>Dell Technologies, Inc. et al. v. Greenthread, LLC,</i> IPR2023-00509.....	2
<i>Fasteners for Retail, Inc. v. RTC Indus., Inc.,</i> IPR2019-00994, Paper 9 (P.T.A.B. Nov. 5, 2019)	77
<i>Intel Corp. v. Greenthread, LLC,</i> IPR2023-00420.....	2
<i>Intel Corp. v. Greenthread, LLC,</i> IPR2023-00552.....	2
<i>Phillips v. AWH Corp.,</i> 415 F.3d 1303 (Fed. Cir. 2005) (<i>en banc</i>). 37 C.....	5
<i>PopSockets LLC v. Flygrip, Inc.,</i> IPR2022- 00938.....	76
<i>Samsung Electronics, Co., Ltd., v. Greenthread, LLC,</i> IPR2020-00289.....	2
<i>Sony Group Corp. (Japan) v. Greenthread, LLC,</i> IPR2023-00324.....	2
<i>Xilinx, Inc. v. Arbor Global Strategies, LLC,</i> IPR2020-01568, Paper No. 12 (P.T.A.B. Mar. 5, 2021).....	79

OTHER CASES

<i>Greenthread, LLC v. Cirrus Logic, Inc.</i> , Civil Action No. 1:23-cv-00369.....	1
<i>Greenthread, LLC v. Intel Corp. et al.</i> , Case No. 6:22-cv-00105, Dkt. 96.....	7
<i>Greenthread, LLC v. Intel Corp. et al.</i> , Case No. 6:22-cv-105-ADA.....	14, 15
<i>Greenthread, LLC v. Intel Corporation</i> , Civil Action No. 6:22-cv-01293.....	2
<i>Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.</i> , Civil Action No. 6:22-cv-00105.....	2
<i>Greenthread, LLC v. Micron Technology, Inc. et al.</i> , Civil Action No. 1:23-cv-00333.....	2
<i>Greenthread, LLC v. Monolithic Power Systems, Inc.</i> , Civil Action No. 1:23-cv-00579.....	1
<i>Greenthread, LLC v. OmniVision Technologies, Inc.</i> , Civil Action No. 2:23-cv-00212.....	1
<i>Greenthread, LLC v. ON Semiconductor Corp., et al.</i> Civil Action No. 1-23-cv-00443.....	2
<i>Greenthread, LLC v. OSRAM GmbH et al.</i> , Civil Action No. 2:23-cv-00179.....	1
<i>Greenthread, LLC v Texas Instruments Incorporated</i> , Civil Action No. 2:23-cv-00157.....	1
<i>Greenthread, LLC v. Western Digital Corporation et al.</i> , Civil Action No. 1:23-cv-00326.....	2

FEDERAL STATUTES

35 U.S.C. § 103.....	4, 5
35 U.S.C. § 314(a)	75, 76

35 U.S.C. § 325(d).....	76, 77
pre-America Invents Act.....	4

RULES

Rule 42.104(a)	4
----------------------	---

REGULATIONS

37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4) and 42.10(a).....	3
37 C.F.R. § 42.8(b)(4)	3
37 C.F.R. § 42.10(b)	3
37 C.F.R. § 42.15(a)(1).....	3
37 C.F.R. § 42.103	3

TABLE OF EXHIBITS

Ex. 1001	U.S. Patent No. 11,121,222 (the “’222 Patent”)
Ex. 1002	Prosecution History of the ’195 Patent
Ex. 1003	Declaration of Dr. Stephen Campbell
Ex. 1004	Curriculum Vitae of Dr. Stephen Campbell
Ex. 1005	U.S. Patent No. 4,684,971 (“Payne”)
Ex. 1006	U.S. Patent No. 4,907,058 to Sakai (“Sakai”)
Ex. 1007	U.S. Patent No. 6,043,114 to Kawagoe, et al., (“Kawagoe”)
Ex. 1008	Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000)
Ex. 1009	U.S. Patent No. 4,160,985 (“Kamins”)
Ex. 1010	U.S. Patent No. 4,481,522 (“Jastrzebski”)
Ex. 1011	U.S. Patent Application Publication No. 2003/0042511 (“Rhodes”)
Ex. 1012	U.S. Patent Application Publication No. 2002/0102783 (“Fujimoto”)
Ex. 1013	Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21st Intl Conf on VLSI Design, IEEE 2008 (“Wang”)
Ex. 1014	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 (“Resnick Decl.”)
Ex. 1015	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 (“Watters Decl.”)
Ex. 1016	IPR2020-00289, Patent Owner Preliminary Response
Ex. 1017	U.S. Pat. No. 11,121,222 (the “’222 Patent”)
Ex. 1018	U.S. Pat. No. 11,316,014 (the “’014 Patent”)

Ex. 1019	Civil Action No. 2:19-cv-00147-JRG, Dkt. 67 (E.D. Tex. Apr. 20, 2019)
Ex. 1020	Prosecution History of U.S. Pat. No. 11,121,222
Ex. 1021	Prosecution History of U.S. Pat. No. 11,316,014
Ex. 1022	U.S. Patent Application Publication No. 2004/0063288 (“Kenney”)
Ex. 1023	Jaeger, <i>Introduction to Microelectronic Fabrication</i> , Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) (“Jaeger”)
Ex. 1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics , dated June 30, 2023
Ex. 1025	U.S. Patent No. 4,435,896 (“Parrillo”)
Ex. 1026	L.C. Parrillo, R.S. Payne et al., <i>Twin-Tub CMOS - A Technology for VLSI Circuits</i> , IEEE 1980 (“Parrillo2”)
Ex. 1027	U.S. Patent Application Publication No. 2007/0045682 to Hong <i>et al.</i> (“Hong”)
Ex. 1028	The Oxford American Dictionary and Language Guide, Oxford University Press (1996)
Ex. 1029	U.S. Patent No. 9,190,502 File History
Ex. 1030	Patent Owner’s Responsive Claim Construction Brief
Ex. 1031	RESERVED
Ex. 1032	Patent Owner’s Sur-Reply Claim Construction Brief
Ex. 1033	Proposed Claim Constructions in the District Court Case
Ex. 1034	Redacted District Court Case Transfer Order
Ex. 1035	Civil Action No. 2:19-cv-00147-JRG, Dkt. 105 (E.D. Tex. Jul. 9, 2020)
Ex. 1036	Publication Declaration of Sylvia Hall-Ellis for Wolf
Ex. 1037	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105

Ex. 1038	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek (“Wieczorek”)
Ex. 1039	Parrillo IEEE Citation List
Ex. 1040	Dictionary of Engineering, McGraw Hill (2003)
Ex. 1041	Rubin et al., <i>Ranges and Moments of Depth Distributions of Boron and Phosphorus Implanted into Silicon in the Energy Range 1.7 - 5.0 MeV with an Eaton NV-GSD/VHE Implanter</i> , IEEE 1997 (“Rubin”)
Ex. 1042	Certified translation of Japanese Unexamined Patent Application Publication No. H8-279598 (“Onoda”)
Ex. 1043	Japanese Unexamined Patent Application Publication No. H8-279598, published on October 22, 1996
Ex. 1044	IPR2020-289, Termination Order
Ex. 1045	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
Ex. 1046	U.S. Pat. No. 5,384,476 (the “576 Patent”) (“Nishizawa”)
Ex. 1047	U.S. Pat. No. 6,900,091 (the “091 Patent”) (“Williams”)
Ex. 1049	Patent Owner’s claim construction brief in <i>Greenthread, LLC v. Cirrus Logic, Inc.</i> , 1-23-cv-00369-DC-DTG
Ex. 1050	Patent Owner’s reply claim construction brief in <i>Greenthread, LLC v. Cirrus Logic, Inc.</i> , 1-23-cv-00369-DC-DTG
Ex.1051	CMOS Layout, Plate 4, from Principles of CMOS VLSI Design: A Systems Perspective, by Neil H. E. Weste and Kamran Eshraghian, Addison-Wesley Publishing, Reading PA (1985)
Ex. 1052	Cover Pages of Modern VLSI Design: System-on-Chip Design, Third Edition, by Wayne Wolf, Prentice Hall (January 2002)

Monolithic Power Systems, Inc. (“Petitioner”) requests *inter partes* review (“IPR”) of claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39-42 (the “Challenged Claims”) of U.S. Patent No. 11,121,222 (Ex. 1001, the “’222 Patent”).

I. MANDATORY NOTICES

A. Real Party-In-Interest

All real parties in interest for this IPR petition are as follows: Monolithic Power Systems, Inc.

B. Related Matters

The ’222 Patent is the subject of the following active court proceedings:

- *Greenthread, LLC v. Monolithic Power Systems, Inc.*, Civil Action No. 1:23-cv-00579 in the District of Delaware, filed May 26, 2023 (“MPS Litigation”);
- *Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-00369 in the Western District of Texas, filed March 31, 2023;
- *Greenthread, LLC v Texas Instruments Incorporated*, Civil Action No. 2:23-cv-00157 in the Eastern District of Texas, filed April 6, 2023;
- *Greenthread, LLC v. OSRAM GmbH et al*, Civil Action No. 2:23-cv-00179 in the Eastern District of Texas, filed April 19, 2023;
- *Greenthread, LLC v. OmniVision Technologies, Inc.*, Civil Action No. 2:23-cv-00212 in the Eastern District of Texas, filed May 10, 2023; and

- *Greenthread, LLC v. ON Semiconductor Corp., Inc. et al*, Civil Action No. 1-23-cv-00443 in Delaware, filed on April 21, 2023.

The '222 Patent was previously subject to the following court proceedings, which are no longer pending:

- *Greenthread, LLC v. Western Digital Corporation et al*, Civil Action No. 1-23-cv-00326 in Delaware, filed on March 24, 2023;
- *Greenthread, LLC v. Micron Technology, Inc. et al*, Civil Action No. 1-23-cv-00333 in Delaware, filed on March 24, 2023;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 3-22-cv-02001 in Oregon, filed on December 29, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6-22-cv-01293 in the Western District of Texas, filed on December 21, 2022; and
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6-22-cv-00105 in the Western District of Texas, filed on January 27, 2022.

The '222 Patent is involved in the following pending PTAB proceedings:

- *Cirrus Logic, Inc. et al v. Greenthread, LLC*, IPR2024-00020 (PTAB) (Oct. 27, 2023);
- *Cirrus Logic, Inc. et al v. Greenthread, LLC*, IPR2024-00021 (PTAB) (Oct. 27, 2023);
- *Semiconductor Components Industries, LLC d/b/a ON Semiconductor v. Greenthread, LLC* IPR2023-01242 (PTAB) (Jul. 27, 2023);

- *Semiconductor Components Industries, LLC d/b/a ON Semiconductor v. Greenthread, LLC* IPR2023-01244 (PTAB) (Jul. 27, 2023); and
- *Texas Instruments Inc. v. Greenthread, LLC*, IPR2024-00673 (PTAB) (Mar. 12, 2024);
- *Texas Instruments Inc. v. Greenthread, LLC*, IPR2024-00674 (PTAB) (Mar. 12, 2024); and
- *Monolithic Power Systems, Inc. v. Greenthread, LLC*, IPR2024-00470 (PTAB) Feb. 03, 2024.

The '222 Patent was involved in the following PTAB proceedings that were terminated:

- *Dell Technologies Inc. et al v. Greenthread, LLC* IPR2023-00509 (PTAB) (Jan. 27, 2023);
- *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00420 (PTAB) (Dec. 28, 2022);
- *Intel Corporation v. Greenthread, LLC*, IPR2023-00552 (PTAB) (Feb. 01, 2023); and
- *Intel Corporation v. Greenthread, LLC*, IPR2023-00552 (PTAB) (Feb. 01, 2023).

C. Counsel Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints Miguel Bombach (Reg. No. 68,636) as its lead counsel, and Bing Ai (Reg. No. 43,312),

John D. Esterhay (Reg. No. 73,512), John P. Schnurer (Reg. No. 52,196), Brianna Kado (Reg. No. 74,307), and Runkun (Justin) Jiang (Reg. No. 78,118) as its back-up counsel.

D. 37 C.F.R. §42.8(b)(4): Service Information

Petitioner concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address:

PerkinsServiceMPS-GreenthreadIPR@perkinscoie.com.

II. CLAIM LISTING

A. Claim 1

1.Pre	A VLSI semiconductor device comprising:
1.1	a substrate of a first doping type at a first doping level having a surface;
1.2	a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
1.3	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
1.4	transistors formed in at least one of the first active region or second active region;
1.5	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
1.6	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,
1.7	wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

B. Claim 3

3	The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
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C. Claim 4

4	The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.
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D. Claim 5

5	The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
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E. Claim 6

6	The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.
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F. Claim 7

7	The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.
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G. Claim 8

8	The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.
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H. Claim 9

9	The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
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I. Claim 13

13	The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.
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J. Claim 15

15	The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
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K. Claim 16

16	The VLSI semiconductor device of claim 1, wherein the device is a flash memory.
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L. Claim 17

17	The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.
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M. Claim 20

20	The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.
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N. Claim 21

21. Pre	A VLSI semiconductor device comprising:
21.1	a substrate of a first doping type at a first doping level having a surface;
21.2	a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;
21.3	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;
21.4	transistors formed in at least one of the first active region or second active region;
21.5	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and
21.6	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions,
21.7	and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

O. Claim 24

24	The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
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P. Claim 25

25	The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.
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Q. Claim 26

26	The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
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R. Claim 27

27	The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.
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S. Claim 28

28	The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
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T. Claim 32

32	The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.
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U. Claim 33

33	The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.
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V. Claim 34

34	The VLSI semiconductor device of claim 1, wherein the device is a flash memory
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W. Claim 39

39.Pre	A semiconductor device comprising:
39.1	a substrate of a first doping type at a first doping level;
39.2	a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
39.3	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
39.4	transistors formed in at least one of the first active region or second active region;
39.5	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

X. Claim 40

40	The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.
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Y. Claim 41

41.Pre	A semiconductor device comprising:
41.1	a substrate of a first doping type at a first doping level;
41.2	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
41.3	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
41.4	transistors formed in at least one of the first active region or second active region;
41.5	at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

Z. Claim 42

42.Pre	A semiconductor device comprising:
42.1	a substrate of a first doping type at a first doping level;
42.2	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
42.3	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
42.4	transistors formed in at least one of the first active region or second active region;
42.5	at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 50-0665. Review of the Challenged Claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '222 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

The '222 Patent claims priority to Sept. 4, 2004. For the purposes of the Petition,

this date has been applied, and the review is governed by pre-AIA 35 U.S.C. §§ 102 and 103 and AIA 35 U.S.C. §§ 311 to 319 and 325(d):

A. Printed Publications as Prior Art

Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '222 Patent:

- **Kawagoe:** U.S. Patent No. 6,043,114 to Kawagoe et al. (Ex. 1007) issued on March 28, 2000 and is prior art under §102(b).
- **Nishizawa:** U.S. Patent No. 5,384,476 to Nishizawa et al. (Ex. 1046) issued on January 24, 1995 and is prior art under §102(b).
- **Onoda** – Japanese Application H8-279598 to Onoda (Ex. 1043, certified translation 1042) published on October 22, 1996 and is prior art under §102(b).

B. Relief Requested

Petitioner requests cancellation of the Challenged Claims as unpatentable under Pre-AIA 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Campbell (Ex. 1003).

Ground	Basis	Challenged Claims	Reference(s)
I	§ 103	1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39-42	Kawagoe
II	§ 103	1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39-42	Onoda
III	§ 103	1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39-42	Onoda and Nishizawa

VI. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) of the subject matter of the ’222 Patent would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. (Ex. 1003, ¶18.) Additional education might compensate for a deficiency in experience, and vice-versa. *Id.*

VII. CLAIM CONSTRUCTION

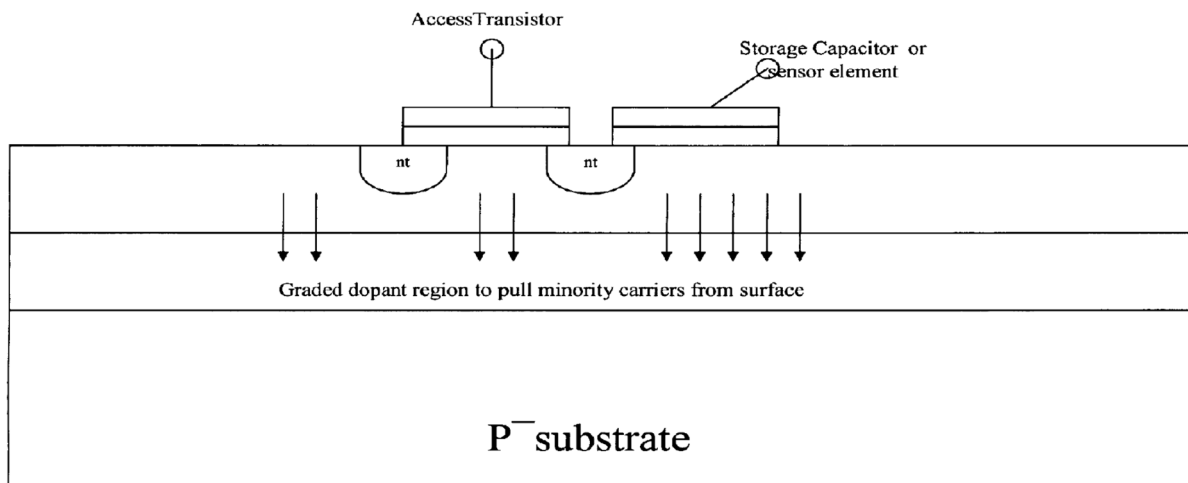
Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). In a currently pending litigation (*Greenthread, LLC v. Cirrus Logic, Inc.*, 1-23-cv-00369-DC-DTG), the Western District of Texas adopted constructions provided in Ex. 1048 at 3-10. For the purpose of this IPR proceeding, Petitioner does not propose any claim terms to be construed but reserves the right to respond to any claim constructions that may arise subsequent to the filing of this Petition.

VIII. THE ’222 PATENT AND BACKGROUND

A. The ’222 Patent

The ’222 Patent is directed to a semiconductor device whose semiconductor layers have a graded dopant concentration to create a drift electric field that sweeps minority carriers from the semiconductor’s active region at the surface to its substrate. (’222 Patent at Abstract and 3:52-56.) Some devices had an “‘aiding drift field’ to enhance the diffusing minority carrier’s speed from emitter to collector” (*id.* at 1:46-

47) but most had a uniformly doped base. (*Id.* at 1:48-53.) The purported improvement is to provide a graded dopant region between the surface and the substrate. (*Id.* at 3:52-56.) This purported improvement is illustrated below from FIG. 5(b). The '222 Patent did not use a new dopant concentration profile and used known techniques. (Ex. 1003, ¶¶31-32.)

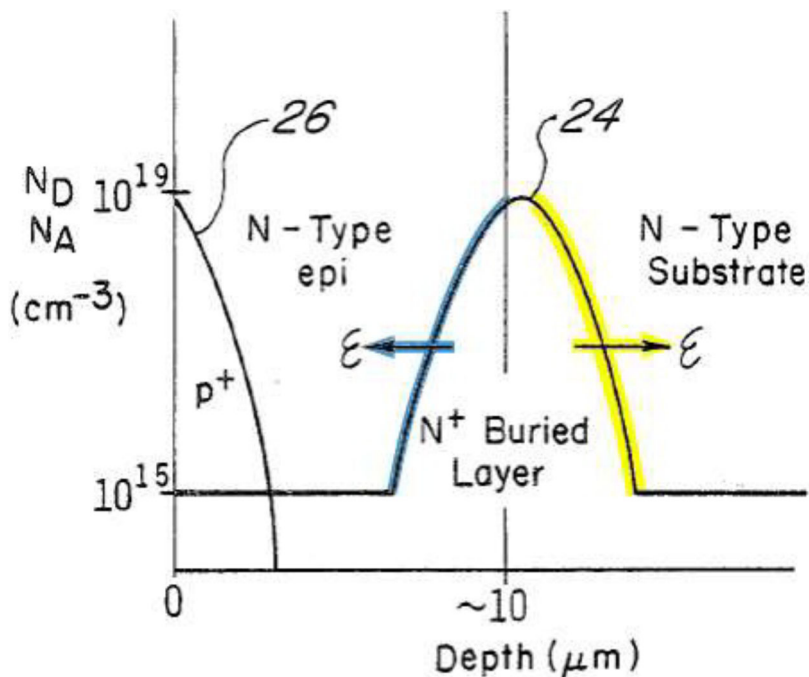


('222 Patent at FIG. 5(b).)

B. General Background

Patent Owner represented that it was well-known that a graded dopant concentration creates a static unidirectional electric drift field. (Ex. 1003, ¶¶46-58 (explaining in more detail).) During prosecution of the '222 Patent's parent, U.S. Pat. No. 8,421,195, Patent Owner admitted that both upward and downward-sloping graded dopant concentrations were known and created an "inherent 'built-in' unidirectional electric field'." (Ex. 1002 at 289-290.) Patent Owner further represented that "a unidirectional drift (electric) field necessarily affects all the present minority carriers

in the same way... Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept ‘down’ ... or ‘up...’” (*Id.* at 289.) Patent Owner made the same representation to the Patent Office regarding the Kamins prior art. (*Id.* at 237-238, 253-254.) According to Patent Owner, Kamins’ Figure 3 shows “two electrical fields with opposing directions” (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. (*Id.* at 237, 253 (citing Ex. 1009 at 3:6-13, FIGS. 2-3).) Patent Owner explained that Kamins “show[s] minority carrie[r]s accelerated into the substrate.” (*Id.* (citing Ex. 1009, FIG. 2 and quoting Ex. 1009 at 3:6-13 (“carriers... accelerated... away from the surface... into the substrate”))).)



(Ex. 1009 at FIG. 3.)

IX. SPECIFIC GROUNDS OF INVALIDITY

A. Ground I: Kawagoe Renders Obvious Claims 1, 3-9, 13, 15-17, 20,

21, 24-28, 32-34, and 39-42 of the '222 Patent.

1. Independent Claim 1

a. Preamble [1.Pre]

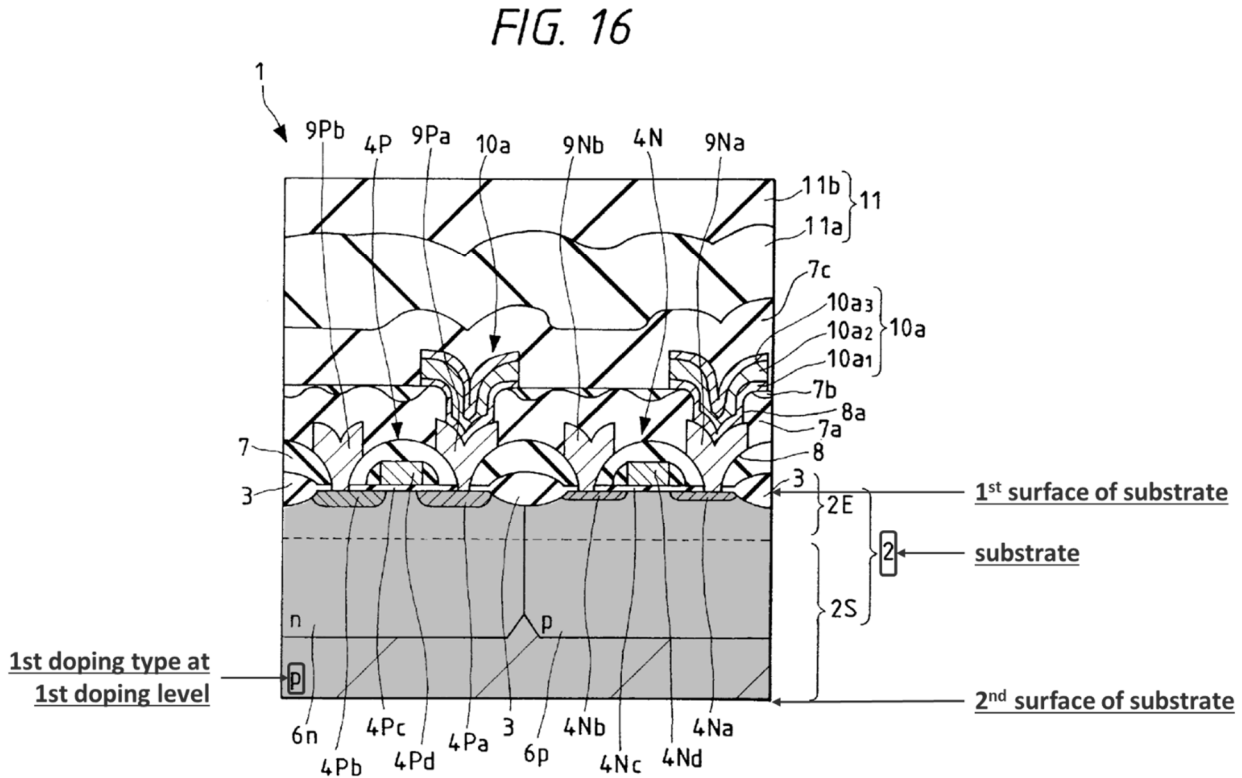
Kawagoe discloses this element. (Kawagoe at 1:13-17.) Semiconductor integrated circuit devices (including MOSFET circuits and various VLSI circuits) can be used in various applications, including memory devices such as DRAM, SRAM, ROM, and semiconductor devices with logic circuits such as the so-called “microcomputer” (*id.* at 24:21-31). Kawagoe is directed to large scale integration (Kawagoe at 2:26-28) which a POSITA would have understood to encompass very large scale integration or at least render it obvious. (Ex. 1003, ¶¶151, 350.)

b. Element [1.1]

Kawagoe discloses this element. (Ex. 1003 at ¶¶152-157, 351.) Kawagoe discloses a p-type substrate 2, *i.e.*, the claimed “a substrate of a first doping type at a first doping level.” Annotated FIG. 16, below, depicts on the p-type substrate 2 including a p-type Si single crystal substrate body 2S and a p-type Si single crystal epitaxial layer 2E. (Kawagoe at 14:61-15:12, 15:11 and 15:26.) The substrate 2 has various surfaces between different layers or components, where two are annotated below as the top surface of epitaxial layer 2E of the substrate 2 and the bottom surface of the N well 6n and the P well 6p.¹ Kawagoe’s substrate 2 thusly satisfies the claimed

¹ FIG. 16 shows the final device, with several insulating layers and connectors on top. (Kawagoe at 10:34-39, 18:1-8.). A POSITA would understand that those layers

“a substrate of a first doping type at a first doping level having a surface.” (Ex. 1003, ¶¶153, 351.) The claimed surface is marked as “1st surface of substrate” below.²



Therefore, Kawagoe discloses Element [1.1].

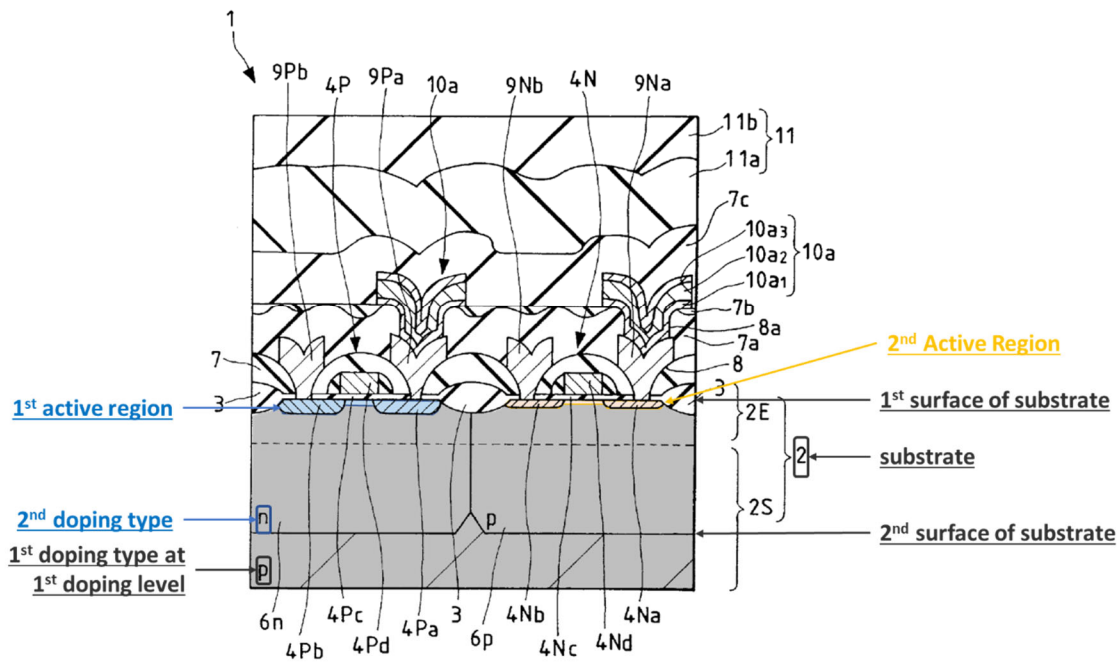
would not be part of the substrate. (Ex. 1003, ¶154.)

² Other surfaces, e.g., interface surfaces have been marked-throughout due to similarity of patent claims in other challenged patents, however, the 1st surface of the substrate satisfies the claimed “having a surface”

c. Element [1.2]

Kawagoe discloses this element. (Ex. 1003, ¶¶165, 352.) Kawagoe teaches “a first active region disposed adjacent the surface.” Kawagoe provides an n-well 6n that includes an active region (annotated blue, below), forming the source, drain, and channel of PMOS transistor 4P. (Kawagoe at 15:26-36; 9:41-54.)

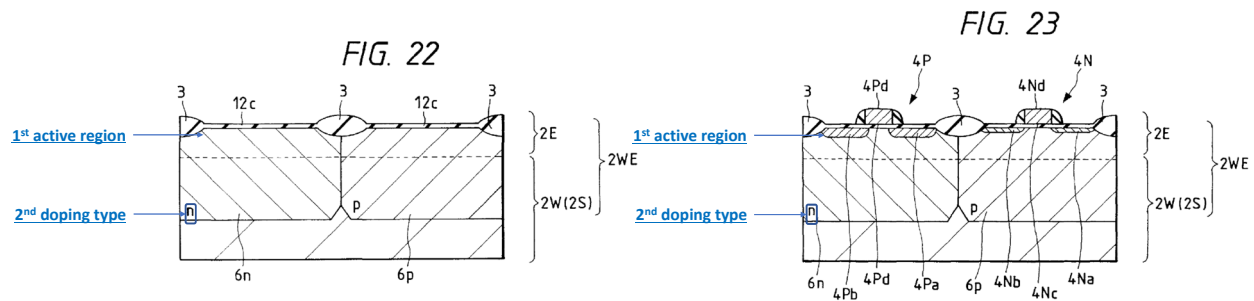
FIG. 16



(Kawagoe at FIG. 16 (Annotated).)

The claimed “first active region” is in the n-type region-well 6n that is opposite in conductivity to the first doping type of the substrate 2 (*i.e.*, p-type). (Kawagoe at 14:61-15:12, 15:7-12, 15:26-28, and 15:30-43.) A POSITA would have understood that the active region’s channel region would remain n-type after forming the source and drain, and the claimed “a first active region ... with a second doping type opposite

in conductivity to the first doping type” is satisfied by the PMOS formed in the n-well.³ (Ex. 1003, ¶¶352, 161.) This is depicted in FIG. 22 and then in FIG. 23 (which are steps in the fabrication of the device of FIG. 16), where the paired semiconductor regions 4Pa and 4Pb are implanted into the n-well 6n. (Kawagoe at 18:18-23.)

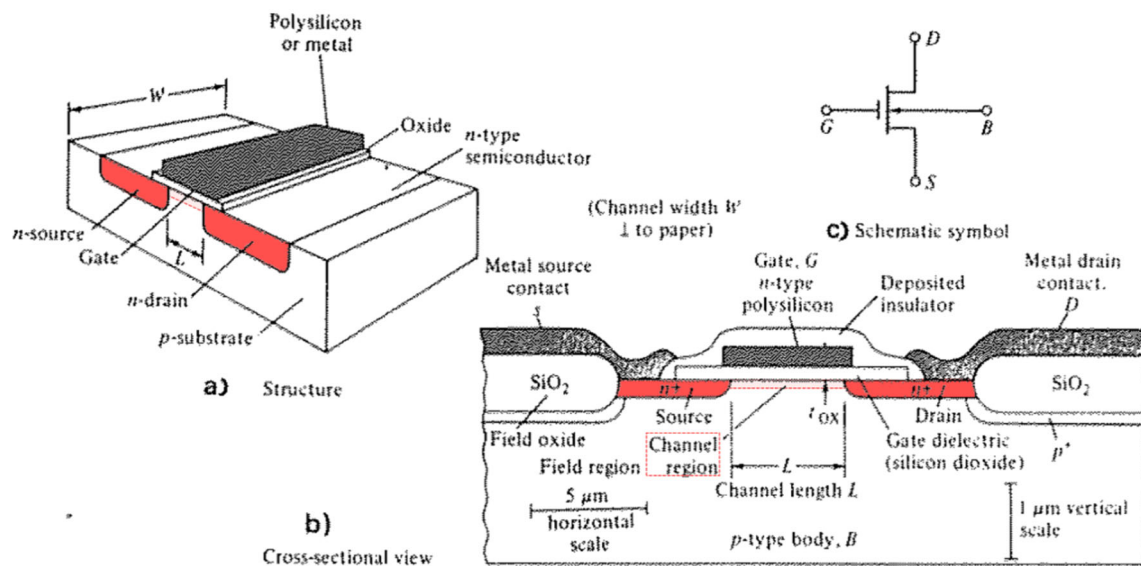


(Kawagoe at FIGS. 22-23 (Annotated).)

Finally, a POSITA would understand that the above-annotated “active region” comprises a source, channel region, and drain, that provides for conductivity and thusly is an active region. The active region of a MOS transistor is known to be “[its] channel

³ A POSITA would understand that the active region’s channel region would remain n-type for the PMOS even if the source and drain are doped to be p-type. (Ex. 1003, ¶¶352, 161.). Nonetheless, even if it were argued that the claimed “a first active region ... with a second doping type opposite in conductivity to the first doping type” refers to the doping types of the source/drain only, this element would be met by Kawagoe’s NMOS transistor. Kawagoe’s NMOS transistor has n-type source/drain regions (and a p-type well).

and [its] heavily doped source and drain regions.” (Ex. 1003, ¶162; Ex. 1008 at 299.) This is also confirmed by Patent Owner’s arguments, where when discussing the term “active region ... within which transistors can be formed” it argued that “this term means exactly what it says: an active region (*i.e.*, a doped region at the surface of a semiconductor device) where a transistor can be formed.” (Ex. 1030 at 31.) Kawagoe thusly discloses the claimed “active region.”



(Ex. 1008 at 299 (Annotated).)

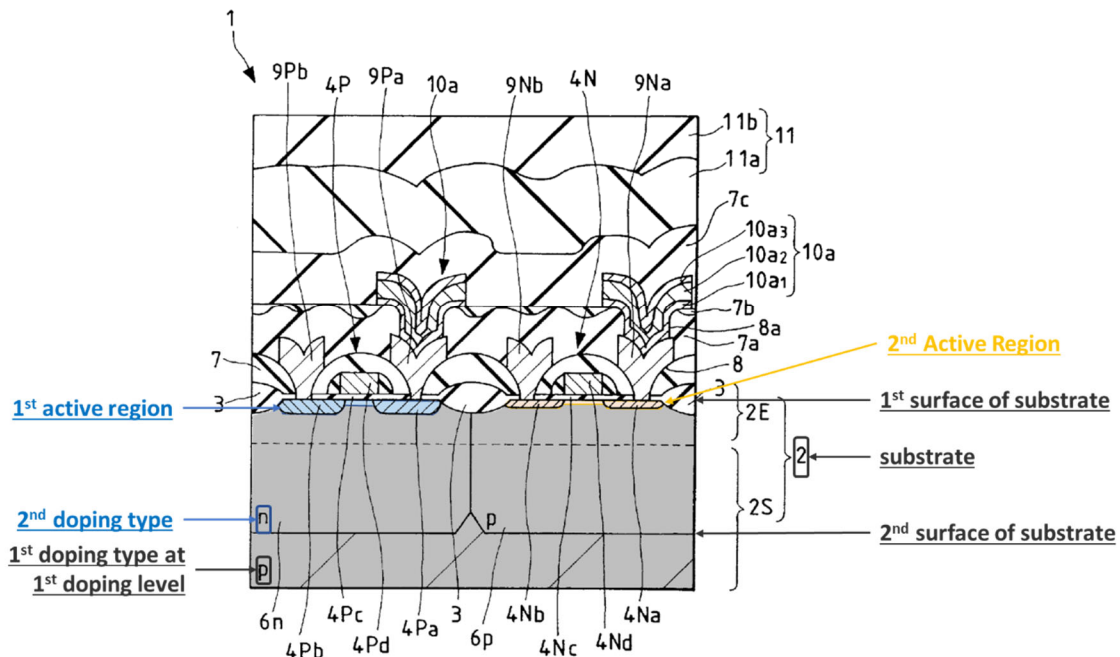
Further, a POSITA would have understood that “a first active region disposed adjacent the surface of the surface” means the first active region is disposed vertically adjacent the first surface of the substrate because the first active region in which transistors can be formed is below the top surface of the substrate to include the source, the drain and the channel region of a transistor. (Ex. 1003, ¶¶163-164, 352.)

Kawagoe thusly discloses Element [1.2].

d. Element [1.3]

Kawagoe discloses, and at least renders obvious, this element. (Ex. 1003, ¶166, 353.) Kawagoe’s FIG. 16 discloses a second active region (tan, below) separate from, and adjacent to, the first active region (blue). (Kawagoe at 15:26-28.) “The p-well 6p is doped with a p-type impurity such as boron” and “formed with the nMOS 4N.” (*Id.* at 15:28-30.) Kawagoe discloses that the semiconductor regions 4Na and 4Nb are regions for forming the source-drain regions of the nMOS 4N. (*Id.* at 8:55-9:6 and 18:9-38.)

FIG. 16



(Kawagoe at FIG. 16 (Annotated).)

As discussed above in Element [1.2], a POSITA would understand that the claimed second active region encompasses a source, drain, and channel region. This

is depicted in Kawagoe's FIG. 16 where the NMOS transistor, having the claimed "second active region," is formed.

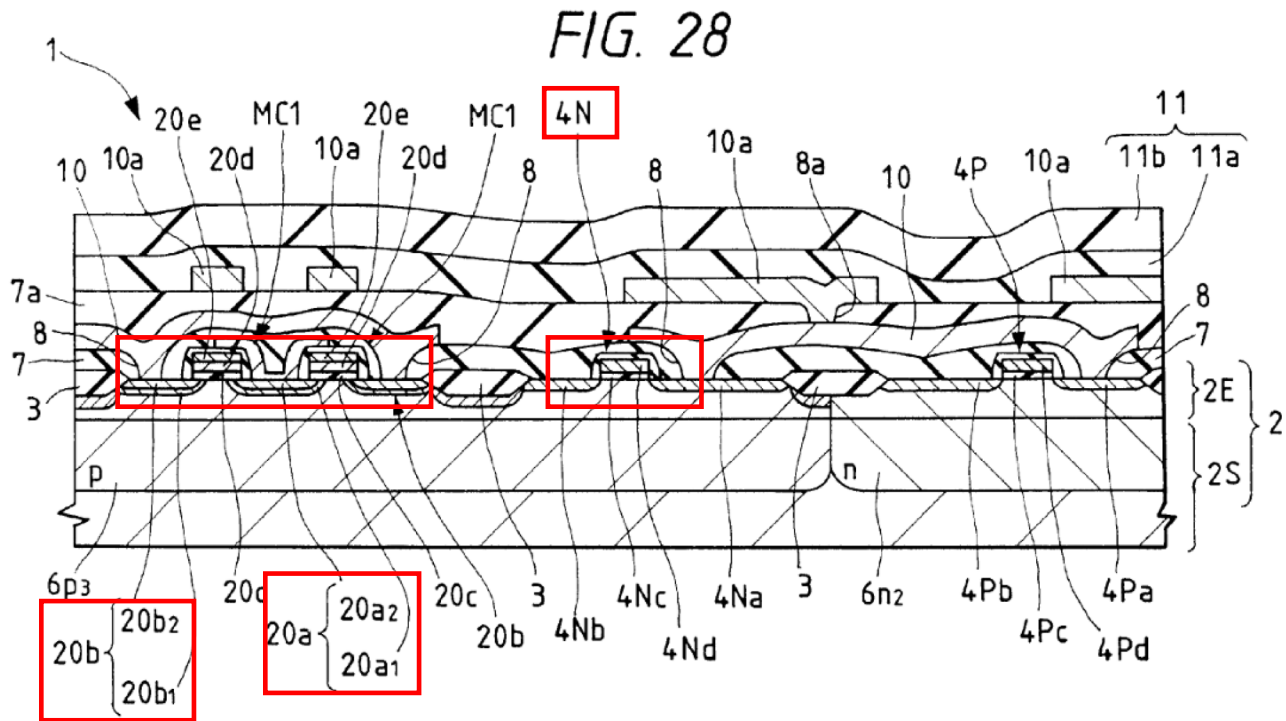
In the context of Element [1.3], a POSITA would have understood "a second active region separate from the first active region disposed adjacent to the first active region" to mean a lateral adjacency between the first and second active regions because the first and second active regions are regions "in which transistors can be formed." Similarly, in Kawagoe, the first active region in the n-well 6n associated with the PMOS transistor 4P and the second active region in the p-well 6p associated with the NMOS transistor 4N are adjacent to each other based on a lateral adjacency. (Ex. 1003, ¶168, 353.)

Finally, to the extent that it is argued that "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed," requires that the "second active region" exist in the same well as the "first active region," such an implementation would have been obvious in view of a POSITA's knowledge and in view of other embodiments of Kawagoe.⁴ A POSITA would have understood that it was standard practice to include multiple transistors active regions in a single well, as described in further detail by Dr. Campbell. (Ex. 1003, ¶¶35-45, 168, 353; Ex. 1051 and Ex. 1052). A POSITA would have found

⁴ This would be inconsistent with the claim language, because it injects the concept that the active regions be directly adjacent with no intervening structures.

it obvious to employ known methods (multiple active regions per single well) and would have achieved known and predictable results, because doing so was common in the industry. (*Id.*) Therefore, a POSITA would have found it obvious to include the “second active region” within the same well as the “first active region.”

Kawagoe discloses multiple active regions in a singular well, demonstrating that this concept was well-known and would have been obvious. FIG. 28 illustrates a memory cell MC1 constructed of a single MOSFET, with its active region (red) formed within the same p-well 6p3 (yellow) as the NMOS transistor 4N. (Kawagoe at 22:39-44, 22:51-59.) As can be seen below, there are multiple semiconductor regions (e.g., 20b, 20a, 4n) within the p-well 6p. A POSITA would have been motivated via Kawagoe’s own embodiments (and via their general knowledge in the art) and would have found it obvious to provide multiple active regions within a single well. (Ex. 1003, ¶¶353, 168, 38-45 (describing the well-known and obvious nature), 168.) A POSITA would have thusly found it obvious to include multiple active regions in its embodiment of FIG. 16 to arrive at multiple active regions within n-well 6n.



(Kawagoe at FIG. 28 (Annotated).)

Kawagoe thusly discloses, and at least renders obvious, Element [1.3].

e. Element [1.4]

Kawagoe discloses, and at least renders obvious, this element. As described in Element [1.2] and [1.3], transistors are formed in the first and second active regions to form a PMOS transistor 4P and an NMOS transistor 4N, respectively.

To the extent this element requires multiple transistors in the first active region or the second active region, it would have been obvious to add multiple transistors into the same active region for the same reasons as described in [1.3]. (Ex. 1003, ¶¶354, 38-45 (describing the well-known and obvious nature), 168, 170.)

Kawagoe thusly discloses, and at least renders obvious, Element [1.4].

f. Element [1.5]

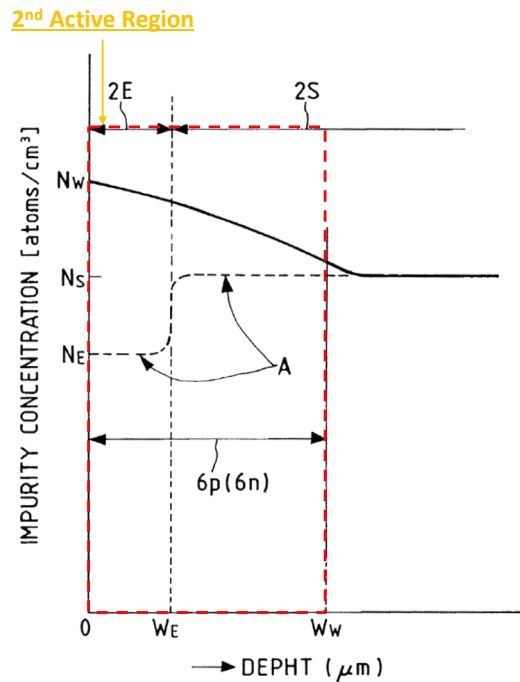
Kawagoe discloses this element. FIGS. 16 and 17 illustrate the claimed “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration.” FIG. 17 illustrates dopant concentration as a function of depth of the physical device depicted in FIG. 16. (Kawagoe at 14:46-67, 15:62-16:15.) The first and second active regions (annotated in blue and tan) are at the first surface of the semiconductor device (*id.* at 15:62-16:15) and have a graded dopant gradient so that carriers (*e.g.*, minority carriers, *i.e.*, electrons in the p-well 6p and holes in the n-well 6n, whose movement is annotated with the purple arrow) are attracted to the substrate’s other surface to reduce errors. (*Id.*)

As can be seen from FIGS. 16 and 17, the “second active region” at the top surface of the p-well 6p in the substrate is where the downward dopant gradient begins, and it levels off shortly after the well 6p (red-dashed annotation).⁵ Similarly, the “first active region” at the top surface of the n-well 6n in the substrate also has a downward dopant gradient which levels off when the depth goes beyond the n-well 6n into the

⁵ The graded dopant profile applies to both the n and p wells, and both the claimed first and second active region would have a downward graded dopant profile (Kawagoe at 15:26-36) which would drive electrons in the p-well 6p (minority carriers in the p-well) downward and drive holes in the n-well 6n (minority carriers in the n-well) downward. (*Id.* at 16:1-16.) (Ex. 1003, ¶¶66-69, ¶101, ¶¶113-116.)

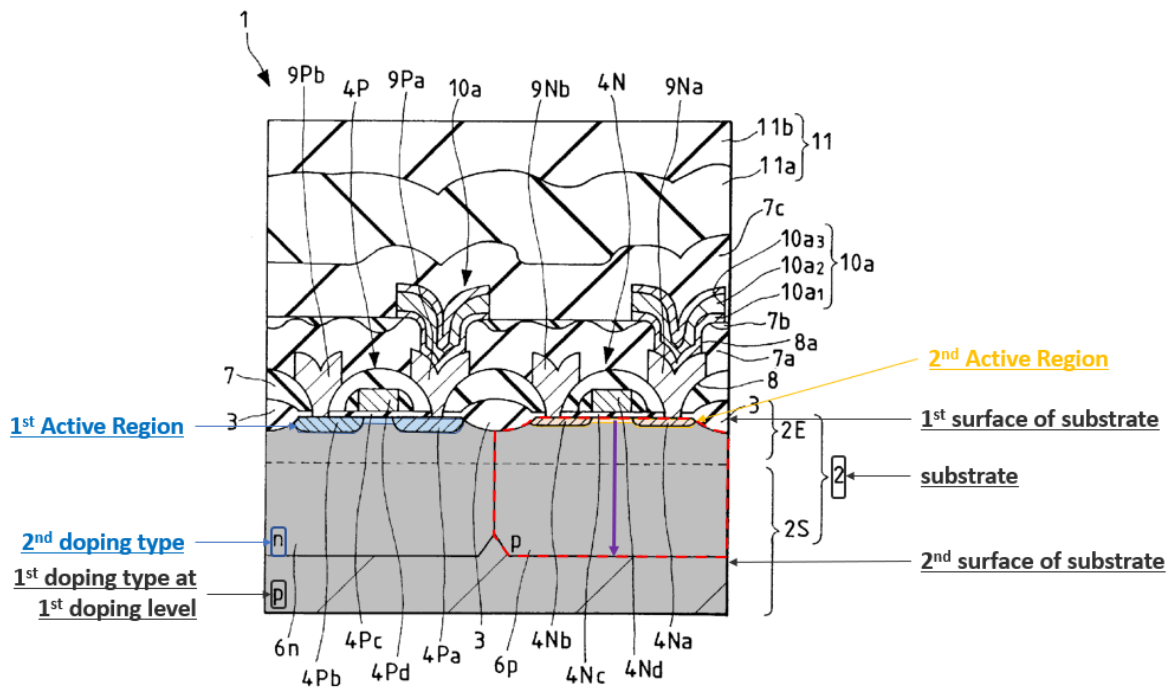
lower part of the substrate. Kawagoe thusly discloses the claimed “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration.” (Ex. 1003, ¶¶355, 171-172.)

FIG. 17



(Kawagoe at FIG. 17 (Annotated).)

FIG. 16



(Kawagoe at FIG. 16 (Annotated).)

Kawagoe's downward graded dopant concentration for each of the p-well 6p and n-well 6n is present from the top surface to the bottom surface of each well to generate a drift electric field to move their respective minority carriers downward to the bottom surface of each well. (Ex. 1003, ¶¶355, 173-178.) Therefore, Kawagoe's downward graded dopant concentration meets the claimed "aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions." Furthermore, as can be seen from Kawagoe's FIG. 16, the bottom portion of the substrate body 2s is "an area of the substrate where there are no active regions." (Ex. 1003 at ¶356.)

Kawagoe's dopant gradient in the p-well 6p is designed to aid carrier movement from the top substrate 2 surface to the substrate body 2S. (Kawagoe at 15:62-16:40.)

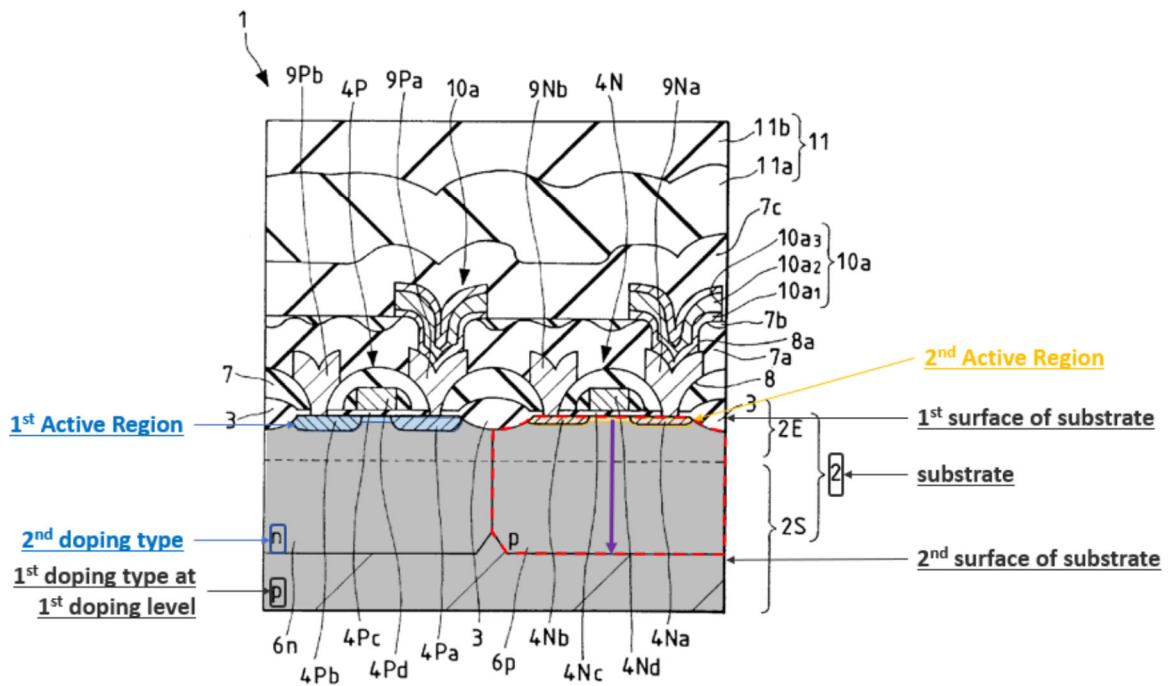
Kawagoe states that “the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.” (Kawagoe at 16:2-11.) Kawagoe’s graded concentration at the active regions (and into the wells) thusly meets the claimed “aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions.”

Kawagoe thusly discloses or renders obvious Element [1.5] and claim 1 as a whole.

g. Element [1.6]

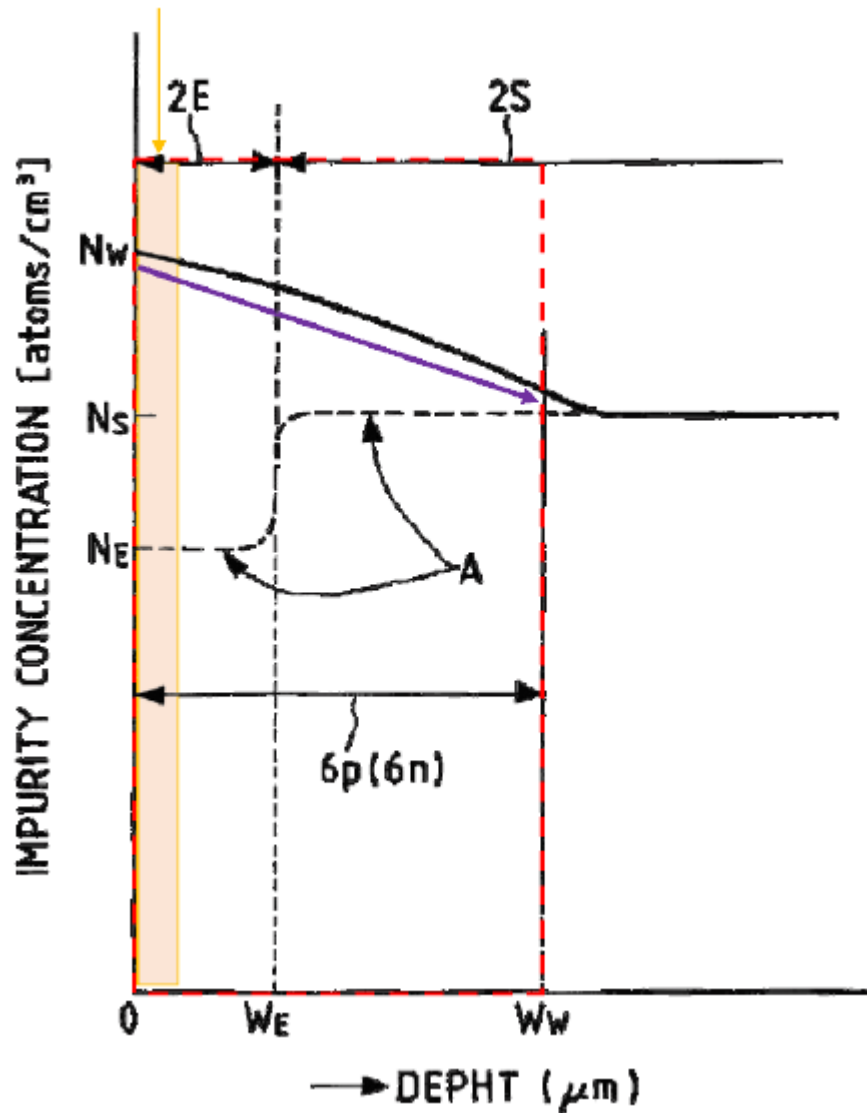
Kawagoe discloses Element [1.6]. As depicted below, Kawagoe provides a p-well 6p (the claimed at least one well region) (annotated in red) that is adjacent to the first active region. The p-well has a graded dopant region from its surface (through the second active region) that aids in the movement of carriers from the claimed surface (annotated first surface). A POSITA would further understand that the n-well 6n (another well region) is similarly adjacent to the second active region. (Ex. 1003 at ¶¶246, 357.)

FIG. 16



Kawagoe in FIG. 17 discloses an example of the graded dopant (impurity) concentration profile at different depths from the top surface of the substrate 2 of FIG. 16. It discloses that the impurity concentration of the p-well 6p (the graded dopant concentration curve with a maximum concentration of N_w at the top surface in FIG. 17) is designed to aid carrier movement of electrons from the top surface of the layer 2E of the substrate 2 by using the graded dope concentration to attract the electrons to the substrate body 2S. (Kawagoe at 15:62-16:40.) (Ex. 1003 at ¶¶248, 357.)

2nd Active Region



The first and second active regions (annotated in blue and tan) are within well regions so that carriers (*e.g.*, minority carriers, *i.e.*, electrons in the p-well) are attracted to the bottom part of substrate where there are no active regions. The depthwise gradient extends from the first surface of the semiconductor device toward the substrate body 2S (Kawagoe at 16:2-15, 15:26-36). As depicted in annotated FIGS. 16 and 17 above, Kawagoe's second active region is disposed on the top portion of the p-well 6p. This portion of the second active region (and at least the channel region) has a graded

dopant concentration. (*Id.* at 15:62-16:40, 15:26-36, 17:11-21, 1:59-2:5, 2:20-23, 15:62-16:15.) The gradient of this graded dopant concentration is represented by a portion of the purple arrow which is also the direction of the electron carrier movement caused by a drift electric field associated with the graded dopant concentration in the second active region which is at the top of the p-well 6p. This portion of the graded dopant profile in the second active region in Kawagoe discloses Element [1.6]. (Ex. 1003 at ¶¶249-250, 357.)

Kawagoe thusly teaches Element [1.6].

h. Element [1.7]

Kawagoe discloses this element. Kawagoe teaches a logic device. Kawagoe states “the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called ‘microcomputer.’” (Kawagoe at 24:28-31.) A POSITA would have understood that formed digital logic of a VLSI semiconductor device. (Ex. 1003 at ¶358.)

2. Claim 3

Kawagoe discloses this element. Kawagoe’s substrate 2 has an epitaxial silicon layer 2E on top of a nonepitaxial silicon substrate body 2S. (*See* Element [1.1] and FIG. 16.) “The epitaxial layer 2E made of a p⁻-type Si single crystal or the like is formed over a principal surface of the semiconductor substrate body 2S.” (*Id.* at 15:1-3.) A POSITA would understand that the substrate body 2S is a nonepitaxial substrate. (Ex. 1003, ¶¶183, 360.) Kawagoe thusly teaches this claim.

3. Claim 4

Kawagoe discloses this element. As previously discussed in Elements [1.2] and [1.3], Kawagoe's first active region contains pMOS transistor 4P and Kawagoe's second active region contains nMOS transistor 4N. (It was well known, and Kawagoe explicitly teaches, that describing the device as either a p-channel or n-channel device is merely a matter of naming convention (and would be in reference to their channel dopant types). (Ex. 1003, ¶¶184, 361.) The full name of the transistors is "n-channel MOS.FET (as will be shortly referred to as 'nMOS') 4N and [] p-channel MOS.FET (as will be shortly referred to as 'pMOS') 4P." (Kawagoe at 8:46-50.)

Further, Kawagoe discloses a logic device. Kawagoe states "the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31.) (Ex. 1003, ¶361.)

Kawagoe thusly teaches this claim.

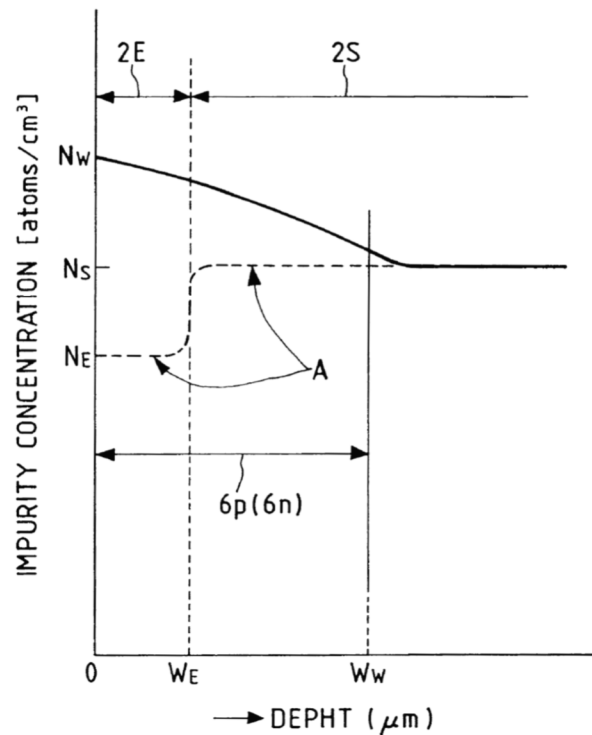
4. Claim 5

Kawagoe discloses this element. (Ex. 1003, ¶¶185, 362.) First, Kawagoe discloses a first active region and a second active region containing either p-channel and n-channel devices in n-wells or p-wells, respectively. As previously discussed with respect to Elements [1.2] and [1.3], Kawagoe's first active region contains pMOS transistor 4P that is located at the top of n-well 6n and Kawagoe's second active region contains nMOS transistor 4N which is located at the top of p-well 6p, with each having

a respective p-channel and n-channel. This structure is the foundation of semiconductor devices which take advantage of the electrical characteristics of the opposing doping types to operate.

Second, as discussed in Element [1.5], the n-well 6n and p-well 6p in Kawagoe each contain a graded dopant concentration. (Ex. 1003, ¶¶362, 186.) The p-wells and n-wells comprise the active regions, where the “impurity concentrations [of those wells are] gradually lowered in the depthwise direction from the principal surface ... of the epitaxial layer 2E.” (Kawagoe at 15:66-16:2.) Kawagoe’s graded concentration of dopants is depicted in FIG. 17 (reproduced below) where the dopant concentrations of both p-well 6p and n-well 6n are represented by the graded dopant concentration profile. Kawagoe thusly teaches this claim.

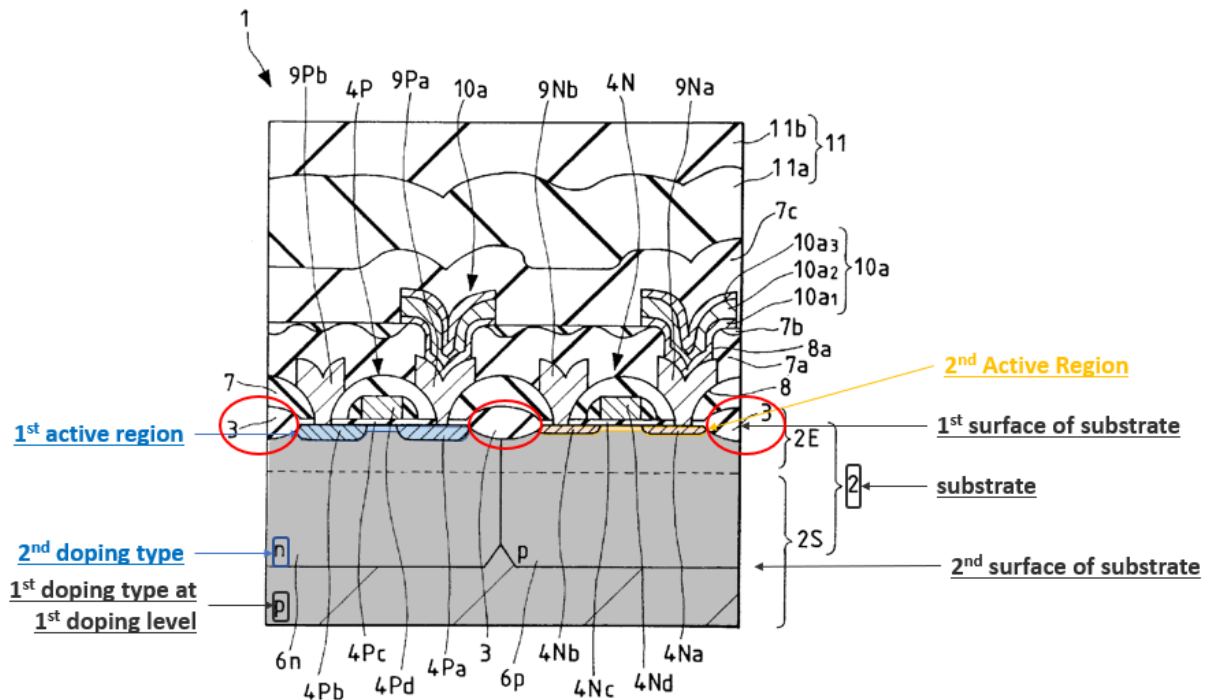
FIG. 17



5. Claim 6

Kawagoe discloses this element. In particular, Kawagoe discloses the claimed active regions are each separated by an isolation region in the form of a field insulating film region 3 that is located between each active region. (Kawagoe at 8:46-54.) FIG. 16 in Kawagoe is annotated to show field insulating film regions 3 in red near the top surface of the substrate 2. Notably, the field insulating film region 3 located between the first and second active regions in FIG. 16 is an isolation region that separates the first active region and second active region.

FIG. 16



(Kawagoe at FIG. 16 (Annotated).)

A POSITA would have understood that the insulating film provides the functionality of creating an isolation region that electrically isolates the active regions so they do not interfere with one another. (Ex. 1003, ¶¶187-188, 363.) Kawagoe thusly teaches this claim.

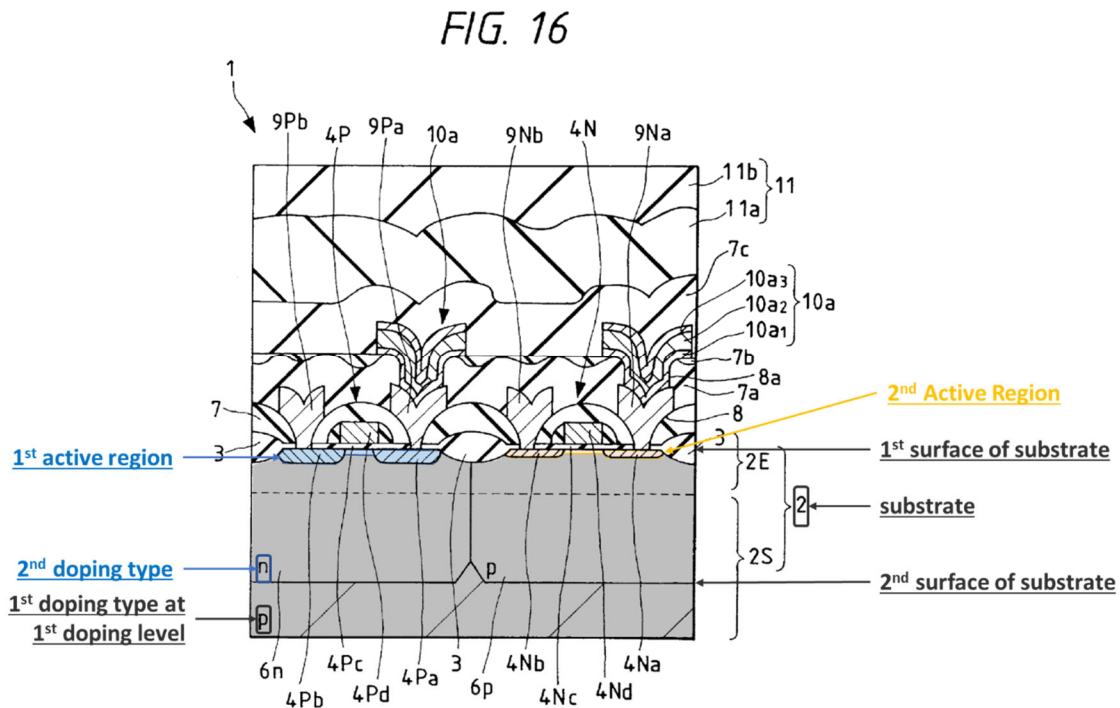
6. Claim 7

Kawagoe discloses this element. (Ex. 1003, ¶¶189, 364.) Kawagoe teaches a diffusion layer that creates the n and p wells and extends into the substrate. As depicted in FIGS. 16 and 17, the diffusion layer is “formed to extend from the surface of the epitaxial layer 2E to the upper portion of the substrate body ... [where its] impurity concentration[] [is] gradually lowered in the depthwise direction.” (Kawagoe at 15:62-16:4.) The layers of the wafer are originally formed via “ion implantation” (id. at

17:32-49) and are then annealed to extend the diffusion. (Id. at 17:50-54.) Kawagoe thusly teaches this claim.

7. Claim 8

Kawagoe discloses this element. (Ex. 1003, ¶¶190. 365.) As previously discussed with respect to Elements [1.2] and [1.3], Kawagoe's active regions are located near the first surface of the substrate. As shown in Figure 16, Kawagoe's first and second active regions are both adjacent to the first surface of the substrate 2 as they are located at the top (but inside) of epitaxial layer 2E of the substrate 2. Kawagoe thusly teaches this claim.



(Kawagoe at FIG. 16 (Annotated).)

8. Claim 9

Kawagoe teaches this. Kawagoe discloses a first active region and a second active region containing either p-channel and n-channel devices in n-wells or p-wells, respectively. As previously discussed with respect to Elements [1.2] and [1.3], Kawagoe's first active region contains PMOS transistor 4P that is located at the top of n-type n-well 6n and Kawagoe's second active region contains NMOS transistor 4N which is located at the top of p-type p-well 6p. (Ex. 1003, ¶¶366, 185.) (*See also* Kawagoe at 15:66-16:2.)

9. Claim 13

Kawagoe discloses this element. (Kawagoe at 8:46-54 (“The element forming region, as enclosed by the field insulating film 3, is formed for example with an n-channel MOS.FET (as will be shortly referred to as ‘nMOS’) 4N and [] p-channel MOS.FET (as will be shortly referred to as ‘pMOS’) 4P, and these nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit.”).) 4N and 4P are CMOS transistors and they have the claimed source and drain (*id.* at 8:66-67, 9:47-48, the claimed gate (*id.* at 9:19 (gate electrode 4Nd); 10:1 (gate electrode 4Pd)), and a channel region which a POSITA would understand is in the well region between the source-drain regions. Kawagoe thusly teaches this claim. (Ex. 1003 at ¶¶367, 191.)

10. Claim 15

Kawagoe discloses a CMOS device (*id.* at 8:46-54) with a nonepitaxial substrate (2S) (*id.* at 15:1-3.) (Ex. 1003 at ¶368.)

11. Claim 16

Kawagoe discloses its structures and teachings can be applied to fabricate improved flash memory devices. (Kawagoe at 23:12-13 (“[I]t is possible to improve the performance, reliability and production yield of flash memory(i.e., EEPROM).”); 24:21-27.) (Ex. 1003 at ¶369.)

12. Claim 17

Kawagoe discloses memory cells with digital logic and capacitor (FIGs. 26(B), 27(B)). Kawagoe also states “the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called ‘microcomputer.’” (Kawagoe at 24:28-31.) (Ex. 1003 at ¶370.)

13. Claim 20

The '222 Patent does not explain which direction is lateral or vertical. Nonetheless, Kawagoe discloses this element. The active regions in 6p and 6n well regions in Kawagoe are spread across the top surface of the substrate layer 2E of the substrate 2, which gives them each a position relative to one another in the lateral direction. The active regions in 6p and 6n well regions in Kawagoe are also spread down into a portion of their respective well regions, which gives the active regions

each a position in the vertical direction with respect to the top surface of the substrate layer 2E of the substrate 2. (*See* FIG. 16.) (Ex. 1003 at ¶371.)

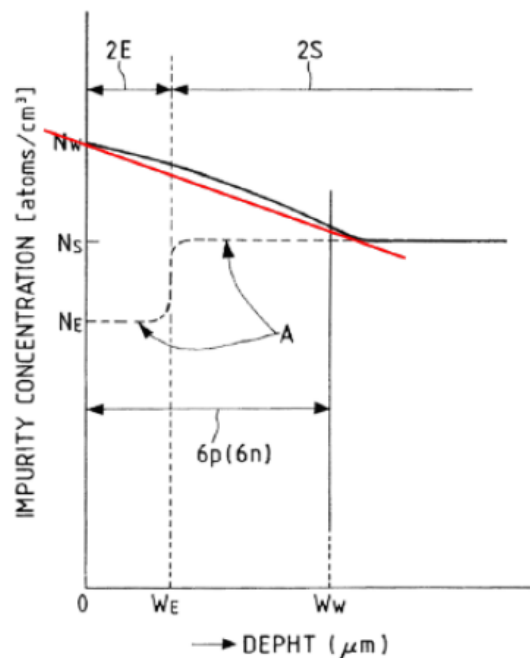
14. Independent Claim 21

Kawagoe discloses Claim 21. Independent claim 21 is substantially similar to independent claim 1 with minor modifications (*e.g.*, “transistors can be formed in the surface thereof” as opposed to merely “transistors can be formed,” “aid carrier movement from the surface to the substrate” as opposed to “aid carrier movement from the first surface to the second surface of the substrate”). (Ex. 1003 at ¶¶372-381.) Elements [21.Pre]-[21.6] are taught for same reasons as [1.Pre]-[1.6]. (Ex. 1003 at ¶¶372-378.)

Element [21.7]⁶ requires “wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof,” which is also taught by Kawagoe. (Ex. 1003 at ¶¶379-381.) Kawagoe discloses the above part of Element [21.7]. Further, FIG. 17 of Kawagoe depicts a graded concentration. (Kawagoe at 16:16-40.) However, the vertical axis is not defined. As a result, a POSITA would not be able to discern if FIG. 17 depicts a quasi-linear or exponential gradient. If it is intended to be a linear scale, a linear gradient is depicted in red). As discussed earlier, either type of profile would improve the transport of minority carriers to the substrate.

⁶ [21.7] is referred to as [21.6] (continued) in the Campbell Decl.

FIG. 17



Moreover, a POSITA would have also found it obvious to use a quasi-linear gradient because it was a simple usage of one known method. The '222 Patent only mentions quasi-linear gradient once ('222 Patent at 2:60-61 and does not illustrate or otherwise describe it, or describe any process steps for obtaining it, thus confirming that such a gradient was a well-known alternative to a POSITA. It would have been obvious to modify Kawagoe's dopant profile based on the POSITA's general knowledge in the art to achieve a known quasi-linear gradient. (Ex. 1003 at ¶380.) This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while

retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success.

Kawagoe thusly teaches this claim.

15. Claim 24

Claim 24/3 are similar and taught for the same reasons.

16. Claim 25

Claim 25/4 are similar and taught for the same reasons.

17. Claim 26

Claim 26/5 are similar and taught for the same reasons.

18. Claim 27

Claim 27/6 are similar and taught for the same reasons.

19. Claim 28

Claim 28/9 are similar and taught for the same reasons.

20. Claim 32

Claim 32/7 are similar and taught for the same reasons.

21. Claim 33

Claim 33 is similar to claim 15, but states that the substrate is CMOS. Kawagoe discloses a CMOS device (*id.* at 8:46-54) with a nonepitaxial substrate (2S) (Kawagoe at 15:1-3.) (Ex. 1003 at ¶368, 388.)

22. Claim 34

Kawagoe discloses its technique is applicable for flash memory. (Kawagoe at 23:12-13 (“[I]t is possible to improve the performance, reliability and production yield of flash memory (*i.e.*, EEPROM).”); 24:21-27.) (Ex. 1003 at ¶ 389.)

23. Claim 39

Kawagoe discloses Claim 39 which is similar to claim 1 with minor modifications (*e.g.*, “transistors can be formed in the surface thereof” v. “transistors can be formed,” “aid carrier movement from the surface to the substrate” v. “aid carrier movement from the first surface to the second surface of the substrate”). (Ex. 1003 at ¶¶391-396.) Elements [39.pre]-[39.5] are taught for same reasons as [1.pre]-[1.5]. In addition, Element [39.5] recites that carriers are added to move to where there are no active regions. Further, Kawagoe FIG. 16 shows there are no active regions in the bottom portion of the substrate body 2S. As further discussed above, the graded dopant concentration in Kawagoe aids the movement of carriers from the active regions on the surface to that bottom portion of substrate body 2S. (Ex. 1003 at ¶¶395-396, 151-181.)

24. Claim 40

Claim 40 is substantively identical to Element [1.6] but recites “the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.” As shown above in Kawagoe FIG. 16, there is no well in the bottom portion of substrate area 2S. The wells are located to a different area of the substrate. (Ex. 1003 at ¶ 397.)

25. Independent Claim 41

Kawagoe discloses Claim 41. Independent claim 41 is substantially similar to independent claim 1 with minor modifications (*e.g.*, “transistors can be formed in the surface thereof” as opposed to merely “transistors can be formed,” “aid carrier movement from the surface to the substrate” as opposed to “aid carrier movement from the first surface to the second surface of the substrate”). (Ex. 1003 at ¶¶398-404, 151-181.) Elements [41.pre]-[41.5] are taught for same reasons as [1.pre]-[1.5]. In addition, Element [41.5] recites “acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region” while Element [1.5] recites “graded dopant concentration.” A POSITA would have understood that “acceptor concentration” and “dopant concentration” to be synonymous. (Ex. 1003 at ¶403.) Kawagoe discloses substrate body 2S in Figure 16 that has a bottom portion with no active regions and where the carrier movement flows from the first or second active regions.

26. Independent Claim 42

Kawagoe discloses Claim 42. Claim 42 is substantively identical to claim 1 but [42.5] requires “at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration” while [1.5] requires “at least one well region adjacent to the first or second active region containing at least one graded dopant region” and “VLSI.” (Ex. 1003, ¶¶405-411, 151-181.) Elements [42.pre]-[42.5] are taught for same reasons as [1.pre]-[1.5]. In addition, Element [42.5]

further recites “donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.” As described above, Kawagoe discloses the bottom portion of substrate 2S in Figure 16 that has no active regions and where the carrier movement flows from the first or second active regions. The donor dopant concentration refers to well region (e.g., n-type) which is disclosed in Kawagoe. Kawagoe thusly discloses this element. (Ex. 1003 at ¶ 410.)

B. Ground II: Onoda Renders Obvious Claims 1, 3-9, 13, 15-17, 20, 21, 24-28, 32-34, and 39-42 of the '222 Patent.

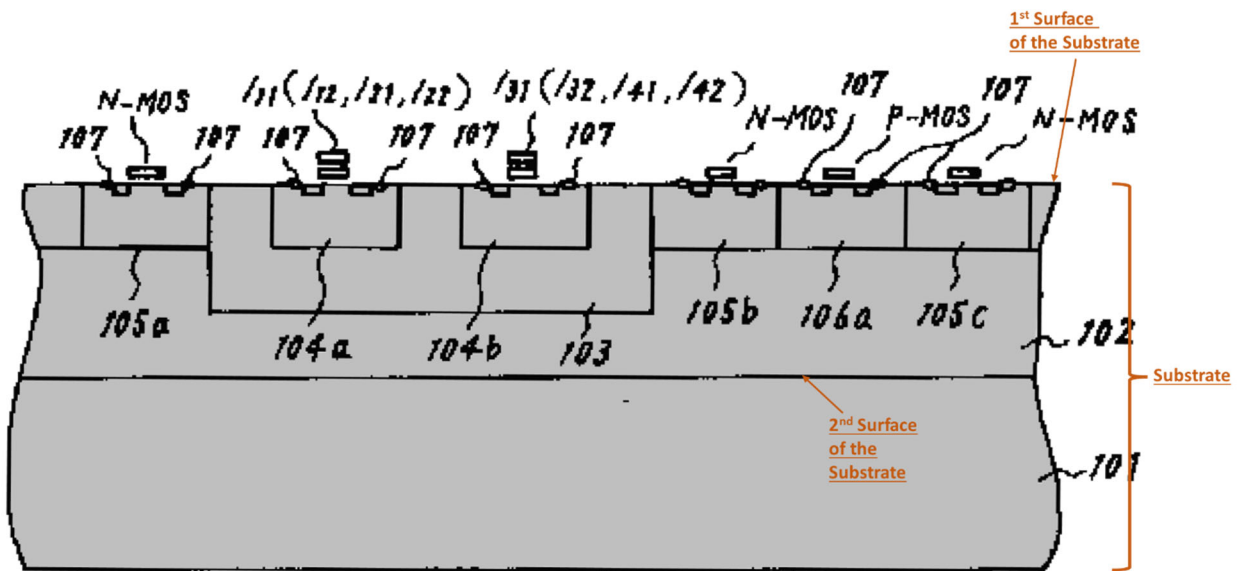
1. Independent Claim 1

a. Preamble

Onoda renders obvious a VLSI semiconductor device. (Ex. 1003, ¶281, 70.) Onoda discloses “a nonvolatile semiconductor storage device with improved latch-up resistance and punch-through breakdown voltage.” (Onoda at [Abstract], Claims 2-6, [0006], [0008]-[0011].) Onoda’s semiconductor device discloses PMOS and NMOS transistors and fabrication methods. (Onoda at Claims 1, 7 and 8-12; [0006], [0007], [0012]-[0017].) VLSI stands for “very large scale integrated circuits.” This naming modifier merely refers to the number of components and does not indicate any relevant changes to the process of developing a semiconductor device with a graded dopant concentration. To the extent that the preamble is limiting, VLSI would have been obvious. (Ex. 1003 at ¶281.)

b. Element [1.1]

Onoda discloses this element. (Ex. 1003, ¶282, ¶71.) Onoda teaches a substrate that has the claimed “surface,” annotated as the “1st surface of the substrate” below.⁷ Onoda’s “semiconductor substrate 100” includes a first and second semiconductor layers 101/102. (Onoda at [0043] (“semiconductor substrate 100 ... is depicted in FIG. 3”); FIG. 2 (describing “substrate 100” as encompassing layers 101 and 102).)

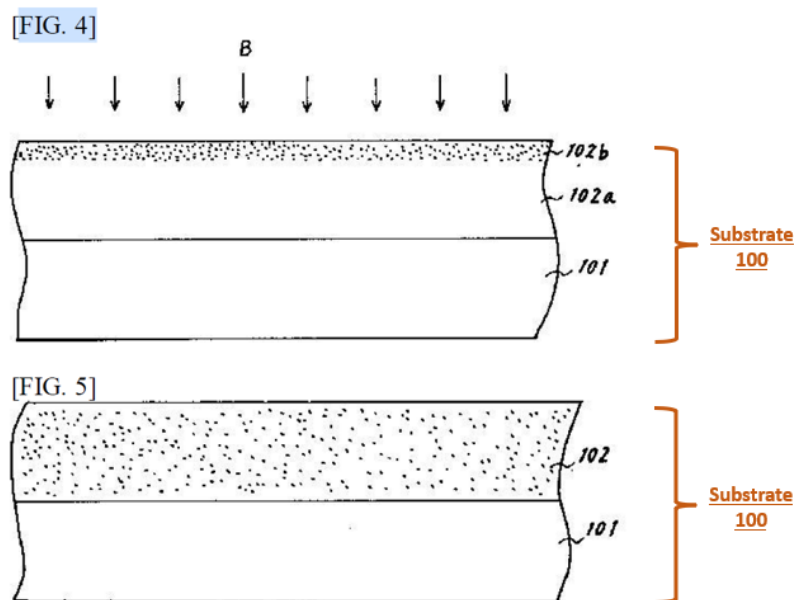


(Onoda at FIG. 3 (Annotated).)

Onoda’s “semiconductor substrate 100” (Onoda at [0043]) is doped to be p-type, and this satisfies the claimed “a substrate of a first doping type at a first doping level.”

⁷ Annotations due to the “2nd surface” have been retained due to similarity of patents to other challenges using same graphics. For the sake of clarity, the identified claimed surface of the ’222 patent is the “1st surface”

Onoda's "semiconductor substrate 100" is made of "a first semiconductor layer made from a heavily-doped [] P-type silicon substrate" labeled as 101 and a p-type doped second semiconductor layer 102 on the top of the first semiconductor layer 101. (Onoda at [0041], "Brief Description of the Drawings" describing FIGS. 1-14 as "first embodiment.") Both of these layers of the semiconductor substrate 100—prior to well and transistor formation shown in FIG. 3—are depicted below in FIGS. 4-5. (Ex. 1003, ¶¶282, 72-78.)



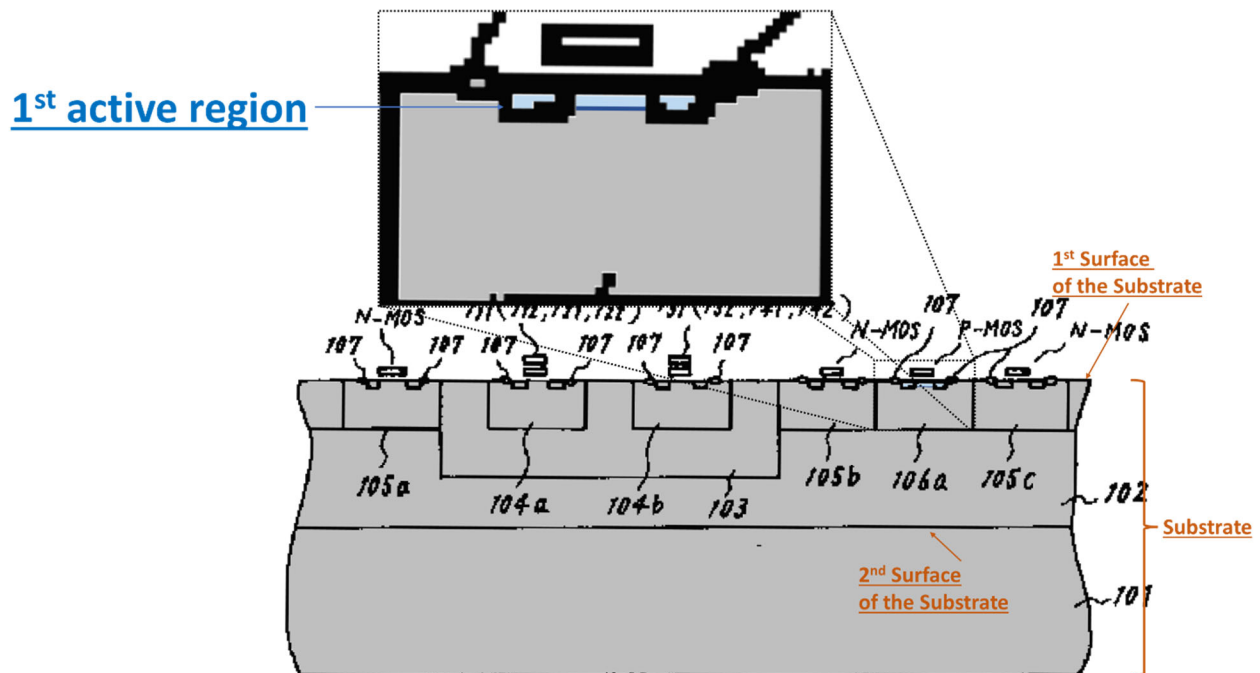
Formation of Substrate 100
FIGS. 4 and 5 of Onoda (Annotated)

Onoda thusly discloses Element [1.1].

c. Element [1.2]

Onoda discloses this element. (Ex. 1003, ¶¶283, 80-87.) Onoda discloses the claimed "a first active region that is disposed adjacent the surface." The top portion of each n-well region 106a, 106b, 106c have PMOS transistors, and each of those

transistors have an active region.⁸ (Onoda at [0043] (“106a, 106b, and 106c are N-type [] well regions”); [0044] (“plurality of P-channel MOS transistors is formed in the fourth well regions 106a, 106b, and 106c”).) The active region of a single PMOS transistor formed in N-type well 106a is annotated blue below.

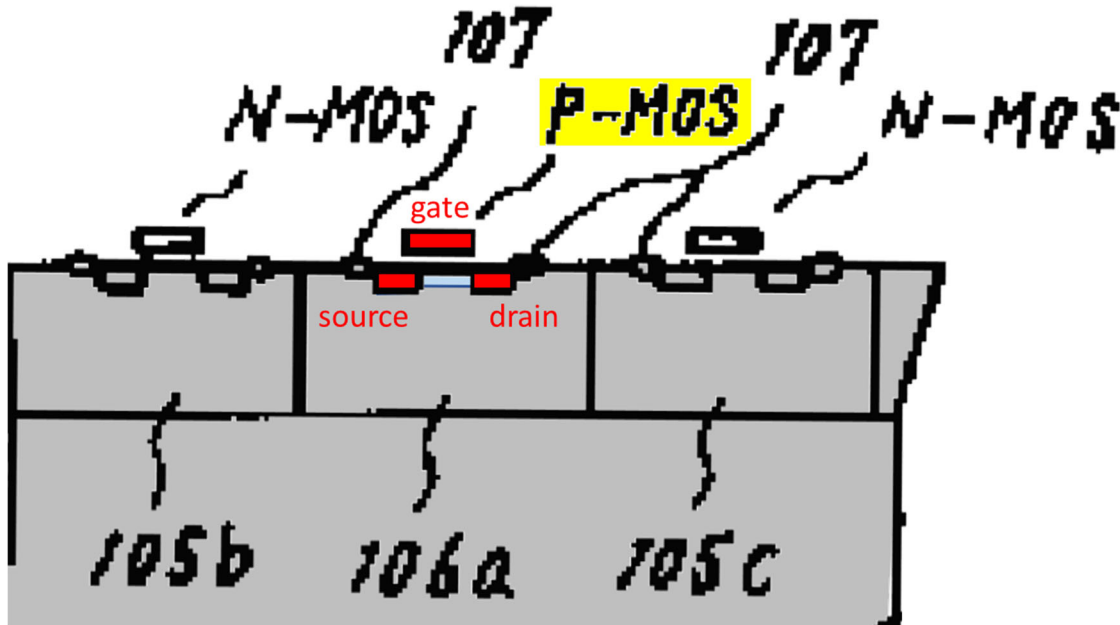


(Onoda at FIG. 3 (Annotated).)

Onoda’s first active region is also where “within which transistors can be formed.” The top portion of each n-well (*i.e.*, 106a, 106b, or 106c), which has the claimed “first active region,” also contains a transistor. (Onoda at [0041]-[0045].) As

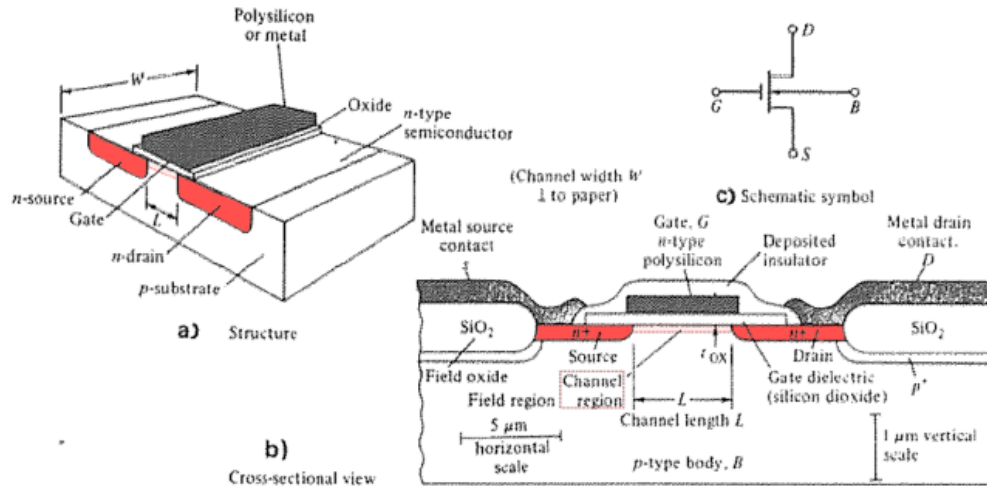
⁸ The claimed “active region” is adjacent to the first surface because it is vertically adjacent to it, and this orientation is consistent with the ’222 Patent specification. The ’222 Patent describes adjacent to mean layers that are next to each other. (’222 Patent at FIG. 5(b).)

can be seen from the excerpted FIG. 3, below, a PMOS transistor (with its gate/source/drain annotated in red and a channel region remains annotated in blue) is formed in the first active region. (*Id.* at [0029] and [0041]-[0045]).)



(Onoda at FIG. 3 (Excerpted and Annotated).)

The above understanding of a transistor is consistent with how a POSITA would have understood it. (Ex. 1003, ¶¶283, 85-87.) A POSITA would have understood that an active region is formed within a well, and the transistor would comprise a source, drain, and gate. A voltage applied to the gate would create a channel in the active region which would allow electrons to flow between the source and the drain. This is demonstrated below from the below textbook excerpt that shows the channel region maintains the same doping of the well.



(Ex. 1008 at 299 (Annotated).)

Onoda’s “first active region” contains “a second doping type opposite in conductivity to the first doping type.” The claimed “first active region” is formed within fourth well region 106a (Onoda at [0044]) which is doped to be n-type. (*Id.* at [0042] (“106a, 106b, and 106c are N-type fourth well regions”).). As described in [1.1], the claimed “first doping level” is p-type, which is opposite in conductivity to n-type of the “first active region” contained within well region 106a.⁹ Onoda thusly discloses the claimed “second doping type opposite in conductivity to the first doping type.”

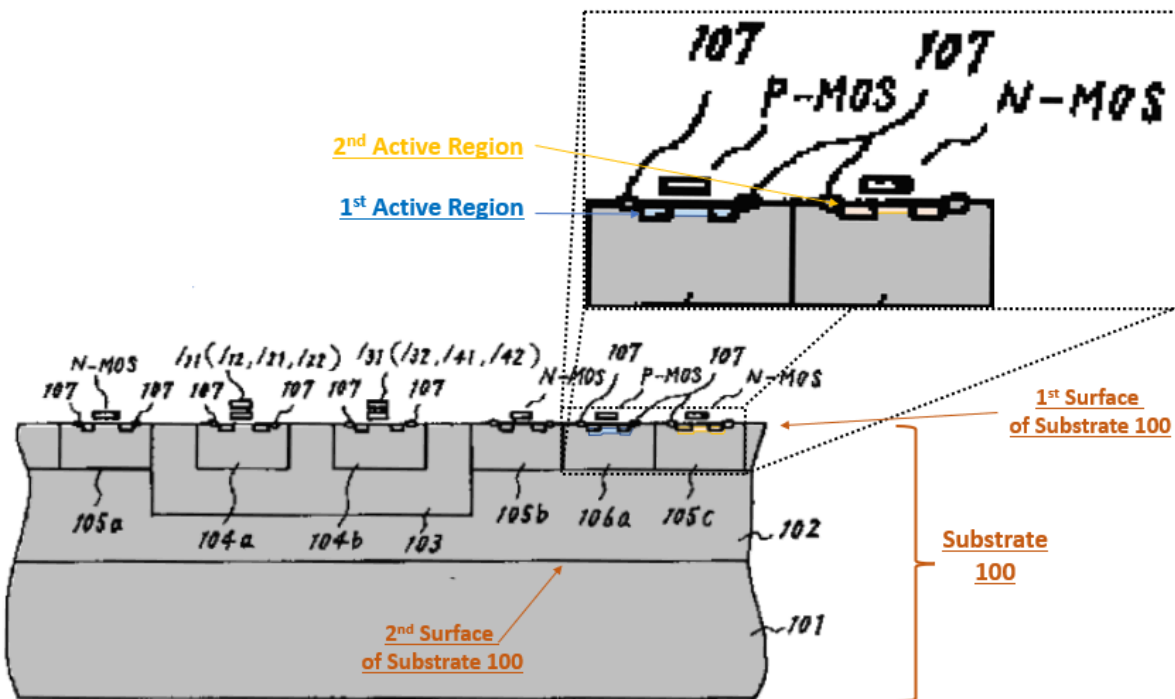
Onoda thusly discloses Element [1.2].¹⁰

⁹ As noted above, the channel region of the active region is n-type.

¹⁰ The above understanding is consistent with the Patent Owner’s claim construction arguments: “active region ... within which transistors can be formed” “means exactly

d. Element [1.3]

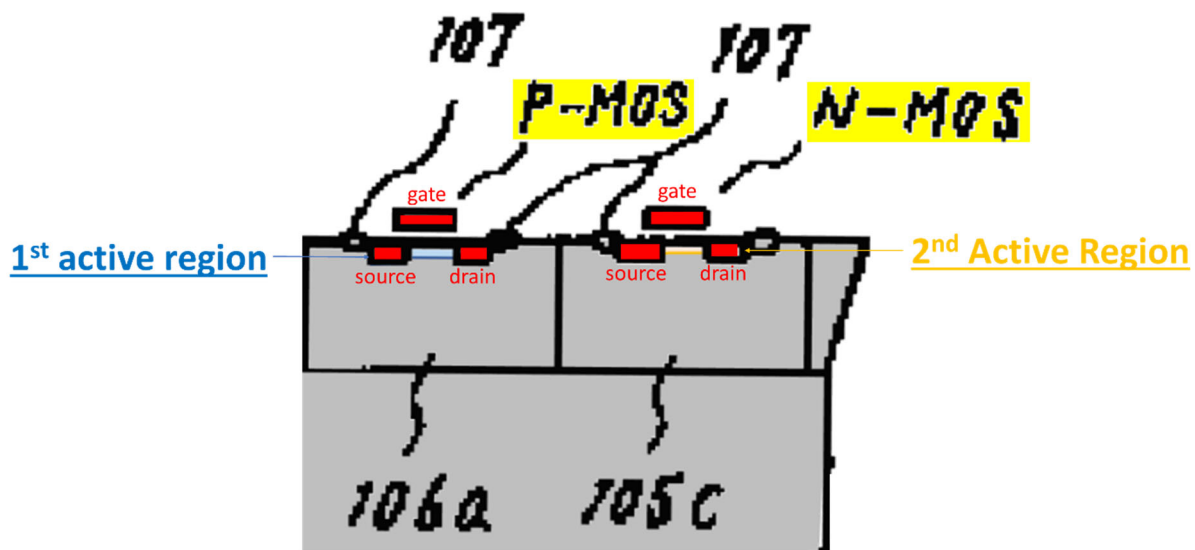
Onoda discloses, and at least renders obvious, this element. (Ex. 1003 at ¶¶284, 88-91.) Onoda discloses a “second active region” “within which transistors can be formed.” Onoda discloses a second active region formed in p-type wells 105a, 105b, and 105c, one of which is annotated tan below. (Onoda at [0043] (“105a, 105b, and 105c are P-type [] well regions”), [0044], Claim 2.)



(Onoda at FIG. 3 (annotated).)

what it says: an active region (*i.e.*, a doped region at the surface of a semiconductor device) where a transistor can be formed.” (Ex. 1030 at 31.)

As can be seen from the above, the second active region (tan) is “separate from the first active region” (blue) and is “disposed adjacent to the first active region.” As shown in the enlarged view of the transistors in FIG. 3 (below), the 2nd active region is a part of p-type well 105c and forms an NMOS transistor, while the 1st active region is a part of n-type well 106a and forms a PMOS transistor. (Onoda at [0029]; [0044] (“the plurality of N-channel MOS transistors is formed in the third well regions 105a, 105b, and 105c, and the plurality of P-channel MOS transistors is formed in the fourth well regions 106a, 106b, and 106c”).)



(Onoda at FIG. 3 (Excerpted and Annotated).)

Finally, to the extent that it is argued that “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed” requires that the “second active region” exist in the same

well as the “first active region,” such an implementation would have been obvious.¹¹ A POSITA would have understood that it was standard practice to include multiple active regions in a single well, as described in further detail by Dr. Campbell. (Ex. 1003 at ¶¶35-45, 91, 284.) Moreover, Onoda itself suggests that multiple transistors can exist in a well region. (Onoda at Claim 3 (“at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region” and “at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region”).) A POSITA would have found it obvious to employ known methods (multiple active regions per single well) and would have achieved known and predictable results, because doing so was common in the industry. (Ex. 1003 at ¶¶35-45, 284.)

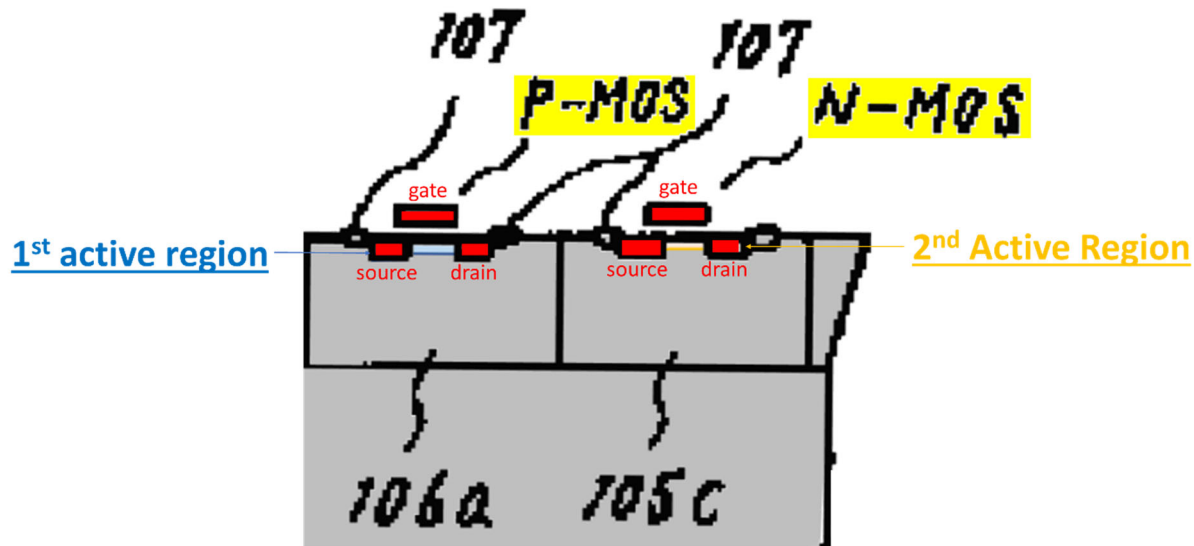
Onoda thusly discloses, and at least renders obvious, Element [1.3].

e. Element [1.4]

Onoda discloses, and at least renders obvious, this element. As demonstrated in Element [1.2] and [1.3], Onoda discloses transistors that are formed in the first active

¹¹ This interpretation would be inconsistent with the claim language, because it injects the concept that the active regions be directly adjacent, with no intervening structures.

region and the second active region, where the “first active region” contains a P-MOS and the “second active region” contains an N-MOS. This is depicted below.



(Onoda at FIG. 3 (Excerpted and Annotated).)

To the extent this element is construed to require multiple transistors in the first active region or the second active region, it would have been obvious to include multiple transistors into the same active region for the same reasons as discussed immediately above in [1.3]. (Ex. 1003 at ¶¶35-45, 93, 285.)

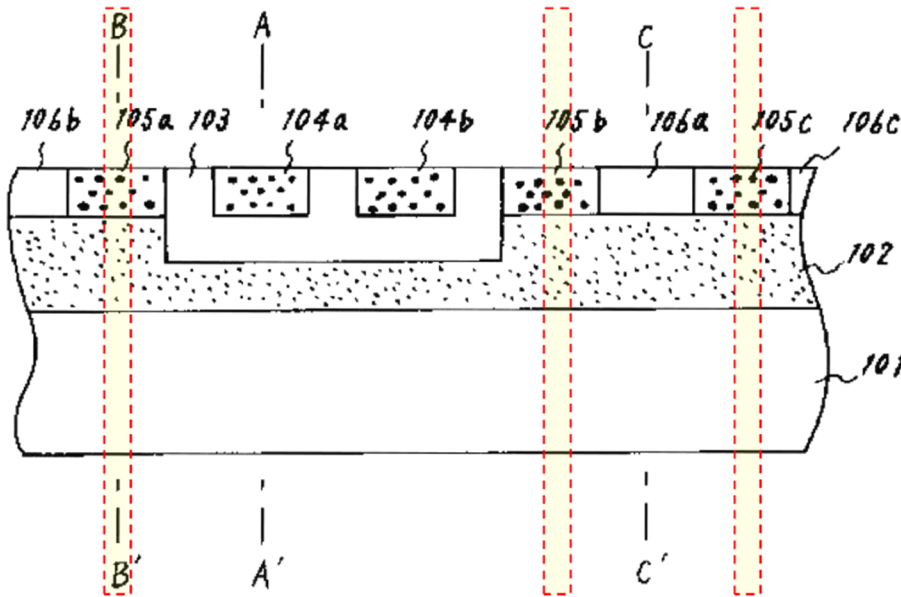
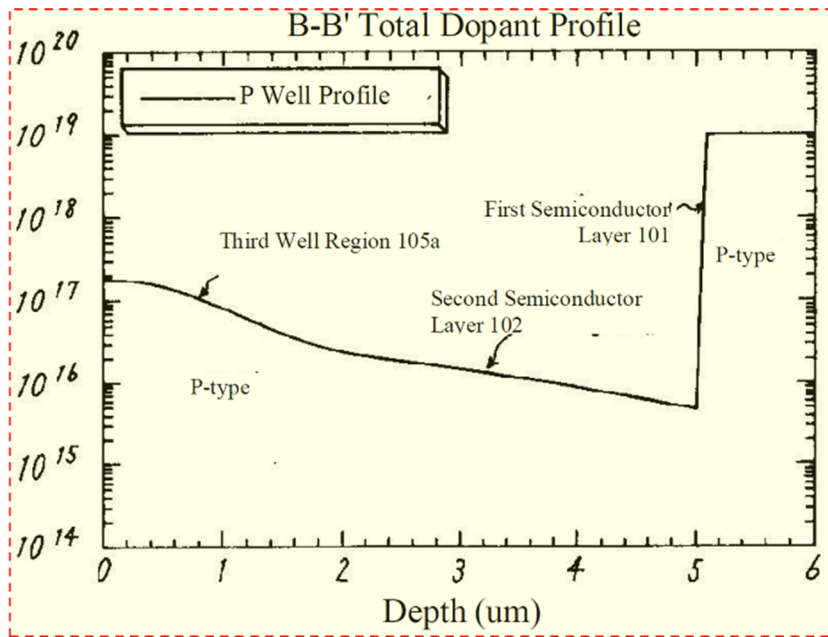
Onoda thusly discloses, and at least renders obvious, Element [1.4].

f. Element [1.5]

Onoda discloses this element. (Ex. 1003 at ¶¶286, 94-117.) Onoda discloses that “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration.” As described in Element [1.3], a second active region is formed within p-well region 105c. Onoda further discloses (described in more detail below) that the well region has a doping profile that is downward graded and,

consequently, the active region would have the same doping profile because it is formed within the well region.

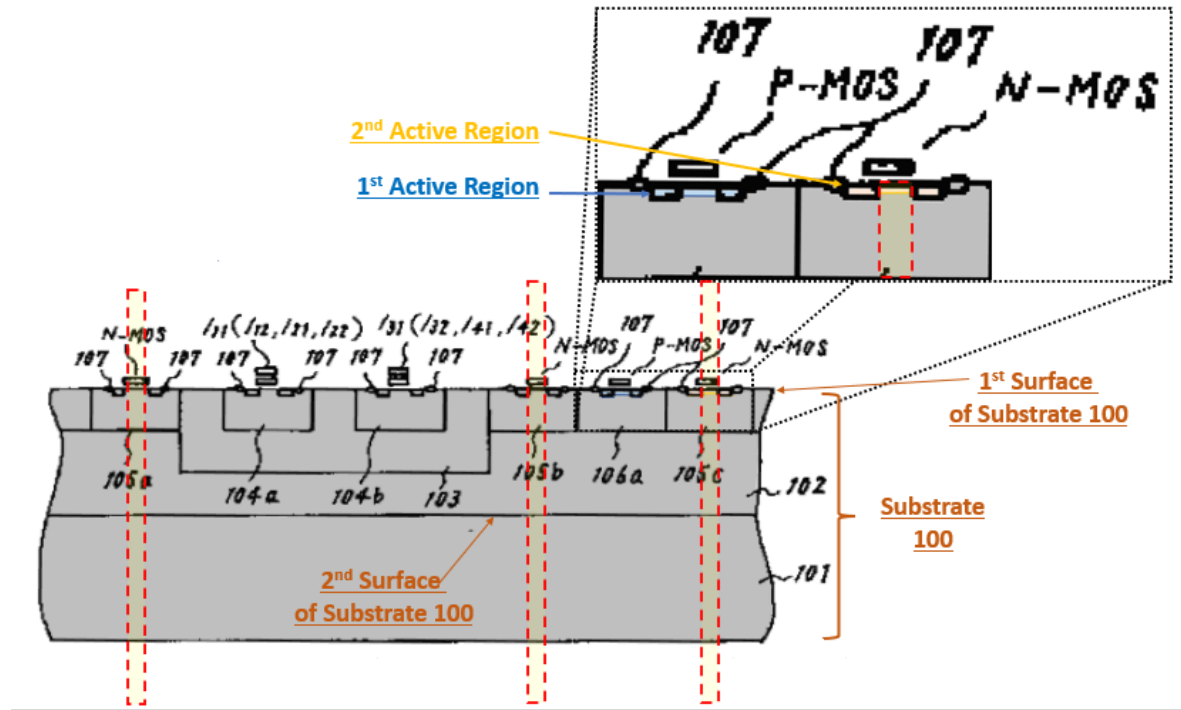
Onoda's FIG. 11 depicts the graded dopant profile across the p-type well regions 105a, 105b, 105c, which constitutes the "at least one graded dopant concentration" of the "at least a portion of at least one of the first and second active regions." FIG. 11 is a cross sectional slice (B-B) through the device depicted in FIG. 8, which is the same embodiment as FIG. 3. (Onoda at [0041]-[0045]). As can be seen from the below, the dopant concentration decreases as a function of depth through the third well region 105a (p-type) and the second semiconductor layer 102 (p-type). Then, at the point where the slice reaches the semiconductor layer 101, the dopant concentration increases. (*Id.* at [0052].). Moreover, a POSITA would have understood that third well regions 105b and 105c would have the same dopant profile as region 105a, because the composition of all three regions are identical. (Ex. 1003 at ¶¶200, 98-100.) FIGS. 8 and 11 are shown annotated below.



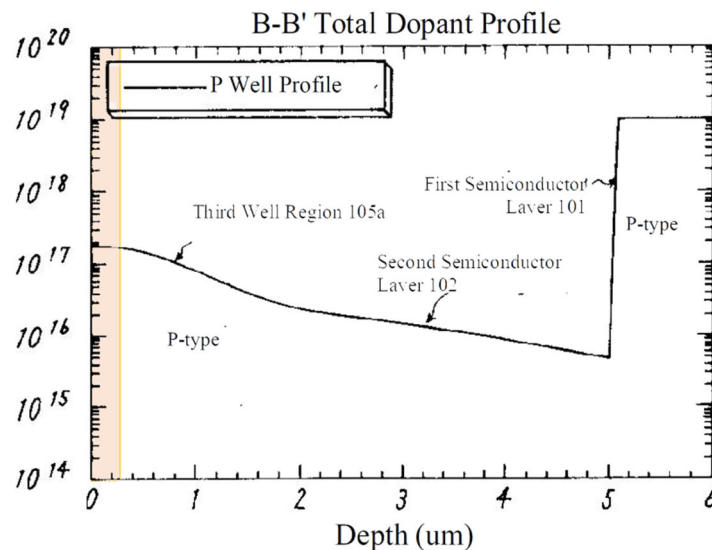
(Onoda at FIGS. 8 and 11 (Annotated).)

Shown below is the graded concentration profile of FIGS. 8 and 11 (which depict intermediate processing steps) annotated on top of FIG. 3 (which is the final constructed device) to demonstrate that the “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration.” As can be seen from the below, the dopant profile is downward graded going through the channel

of the active region, the third well regions 105a/b/c, and the second semiconductor layer 102. Immediately following annotated FIG. 3, is annotated FIG. 11, depicting that the downward gradient exists in the active region's (tan) channel. (Ex. 1003 at ¶¶286, 100.)



(Onoda at FIG. 3 (Annotated).)



(Onoda at FIG. 11 (Annotated).)

There is a decrease in the dopant gradient as a function of depth across the claimed “at least a portion of ... the second active region.” It was known that a decrease in the dopant concentration as a function of depth produces an electric field to drive electrons downward, *i.e.*, from the top surface of the active region (through its channel) towards the bottom of the p-type well region 105a and this provides the claimed “to aid carrier movement from the first surface to the second surface of the substrate.” (Ex. 1003 at ¶¶286, 101.)

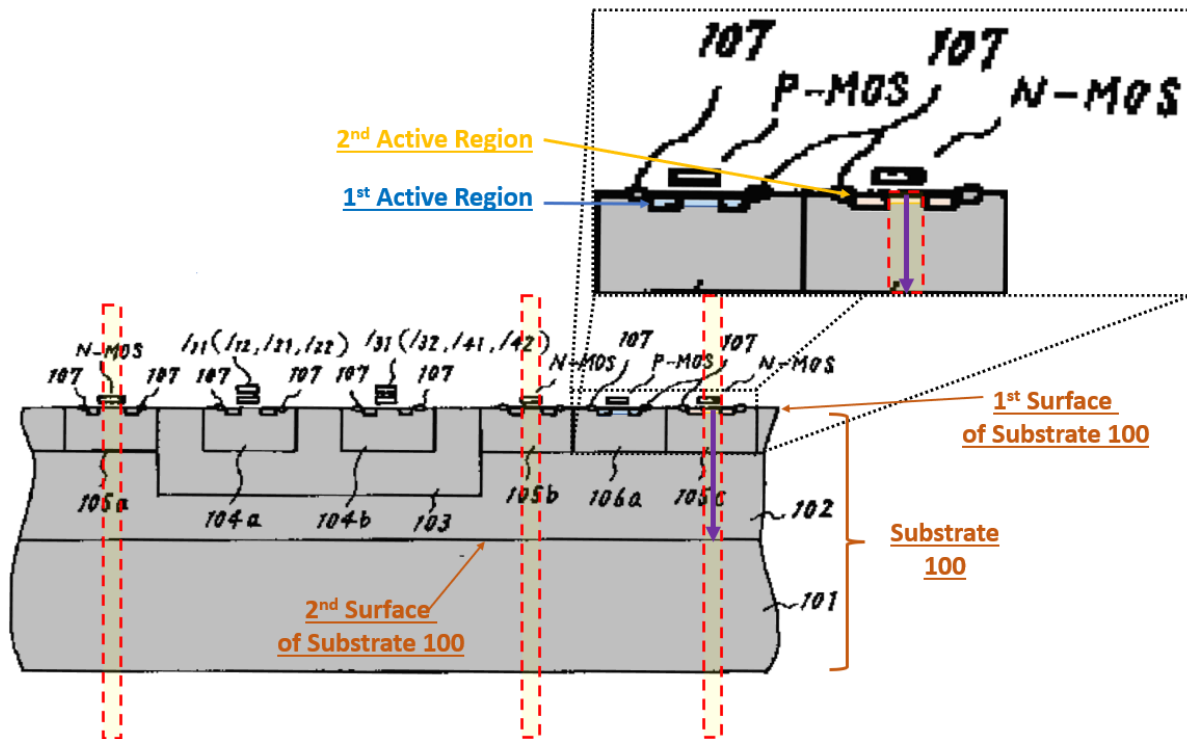
The fact that a graded concentration aids the movement of carriers was a well-known property of semiconductor devices long before September 2004. (Ex. 1003, ¶¶286, 103, 46-58.) Patent Owner admitted that to be the case in prosecution, where Patent Owner, citing prior art, stated that “the graded dopant concentration itself creates a ‘built-in’ electrical field” and this “built-in” electric field “forces the movement of carriers into a particular direction, whereby the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.” (Ex. 1003, ¶¶286, 47, 103.). The net effect of the graded dopant concentration is to cause carriers (e.g., electrons) to move from the top surface of the substrate 100 to the bottom surface of the layer 102, which is towards the second surface of the substrate 100. (Ex. 1003, ¶¶286, 104.)

Onoda discloses the use of graded dopant concentrations in P and N wells to aid the movement of minority carriers away from corresponding transistor active regions

towards the lower part of the substrate. (Ex. 1003 at ¶¶286, 66-69, ¶101, ¶¶113-116.)

This movement of the minority carriers (electrons) by Onoda's graded dopant concentration in an example of P well is depicted by the purple arrow in annotated FIG.

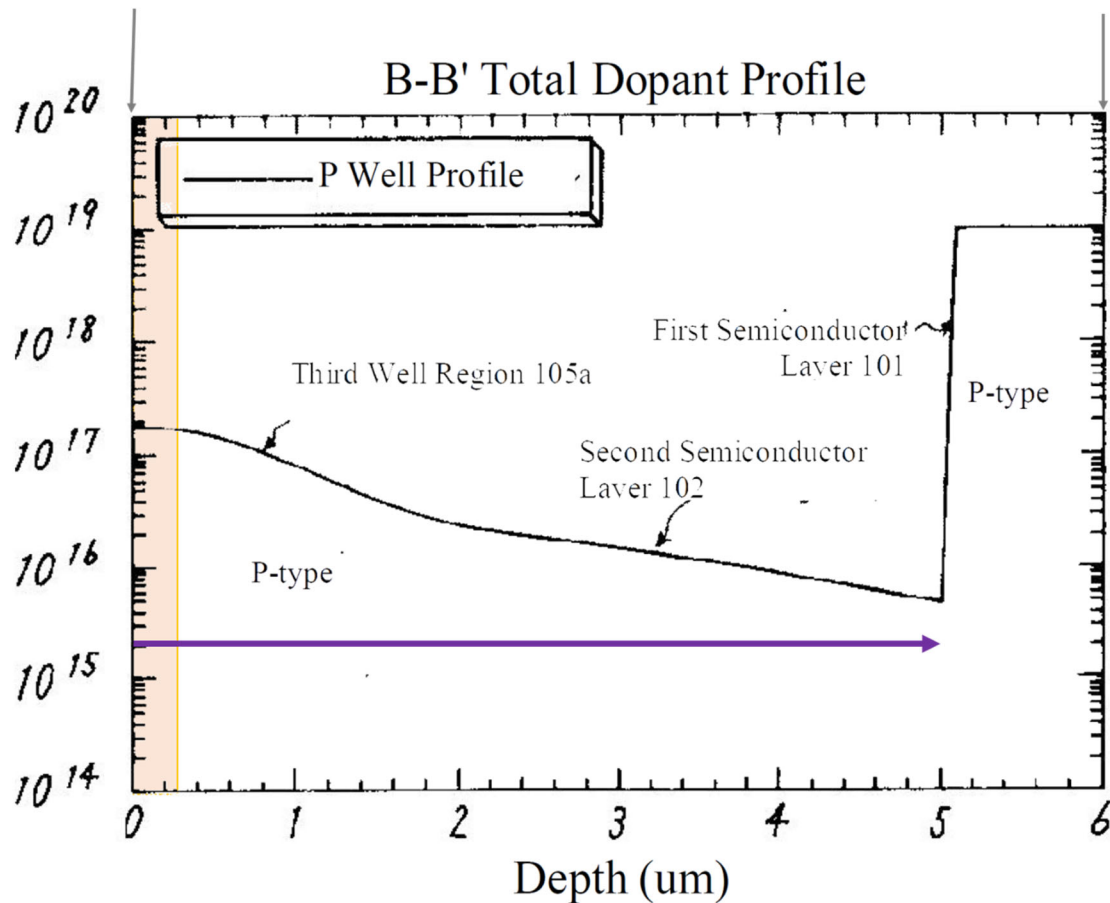
3 and FIG. 11.¹²



(Onoda at FIG. 3 (Annotated).)

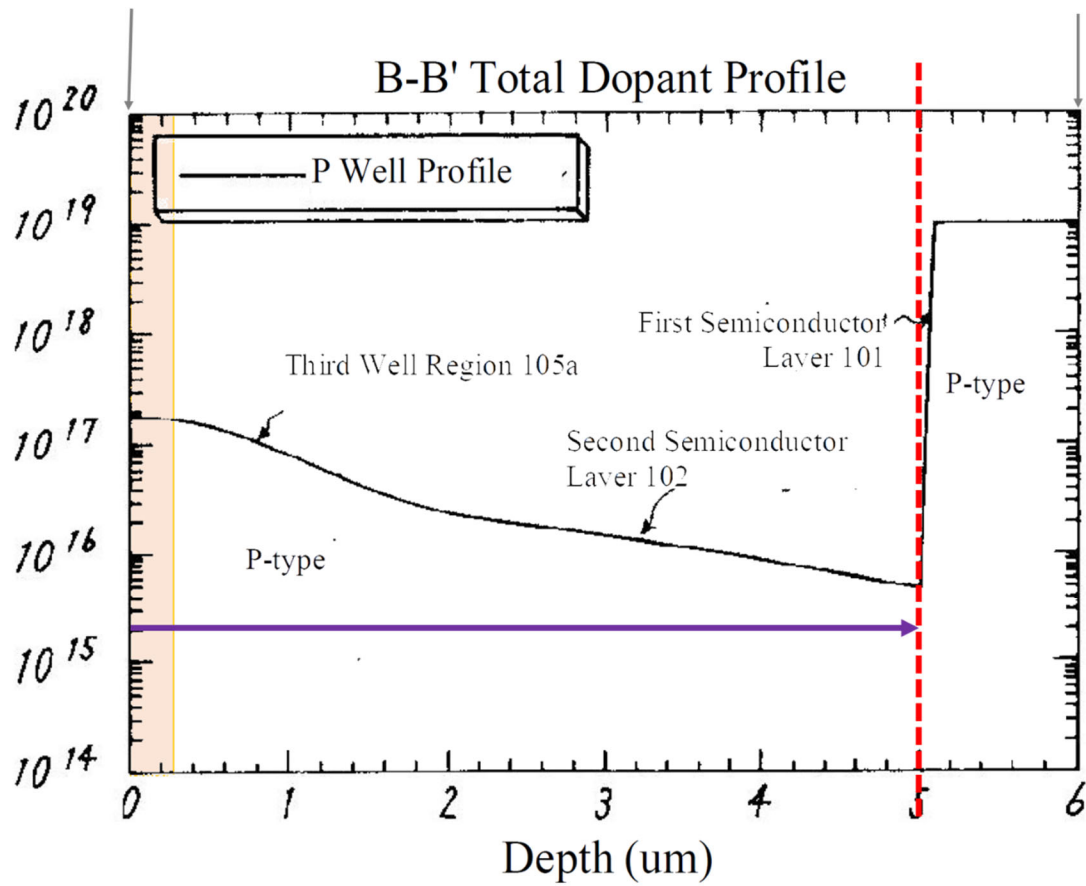
¹² Moreover, as Dr. Campbell explains, there same case exists across other transistors.

(Ex. 1003, ¶¶112-115.)



(Onoda at FIG. 11 (Annotated).)

Finally, it should be noted that the movement of electrons is aided downward but their progression is halted at the junction of the second semiconductor layer 102 and first semiconductor layer 101. (Ex. 1003, ¶¶286, 106.) The electrons will be halted at the red annotated point. This does not affect the claim analysis.



(Onoda at FIG. 11 (Annotated).)

Element [1.5] only requires that “at least a portion of at least one of the first and second active regions” have the “at least one graded dopant concentration” to “aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions.” The element does not require that carriers migrate all the way to the bottom, *i.e.*, through the entire substrate to the physical bottom of the device. (Ex. 1003, ¶¶286, 107) (Dr. Campbell explaining that requiring carriers to traverse the entire device is inconsistent with the ’842 Patent specification (which the ’222 patent shares a specification with)).) This understanding is consistent with Patent Owner’s claim construction arguments (which were adopted by the District

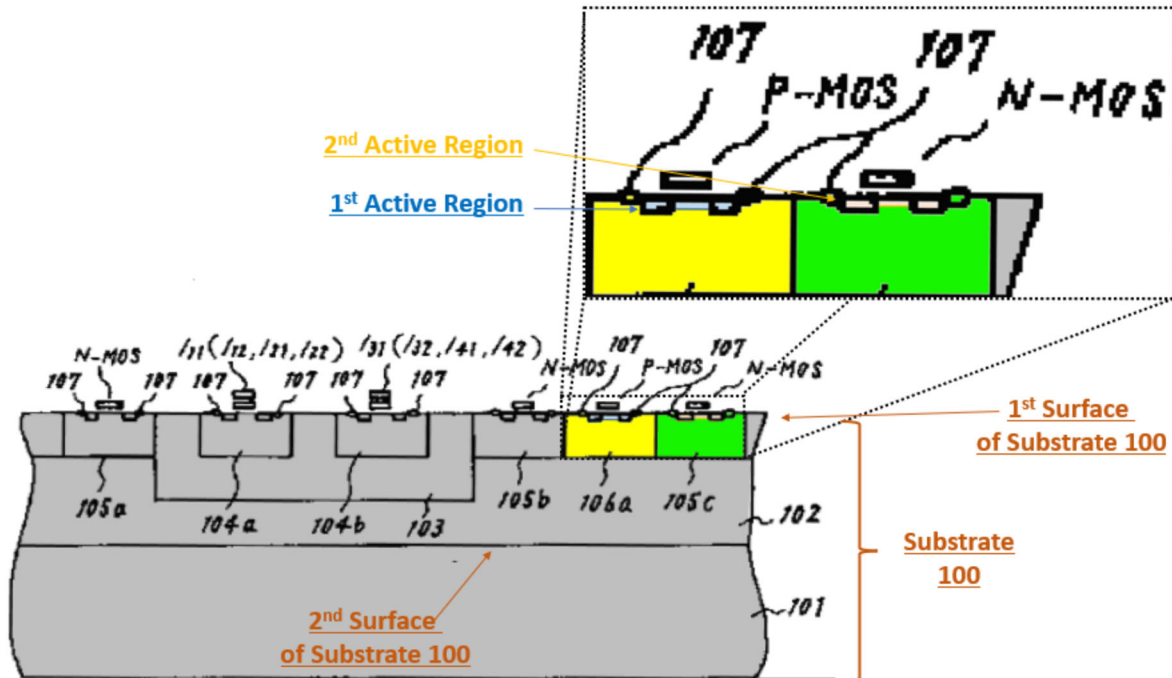
Court) that this limitation does not require that carriers actually reach the second surface and that the limitation only requires that the carriers be aided downward. (Ex. 1003, ¶¶286, 109.)

Onoda thusly discloses Element [1.5].

g. Element [1.6]

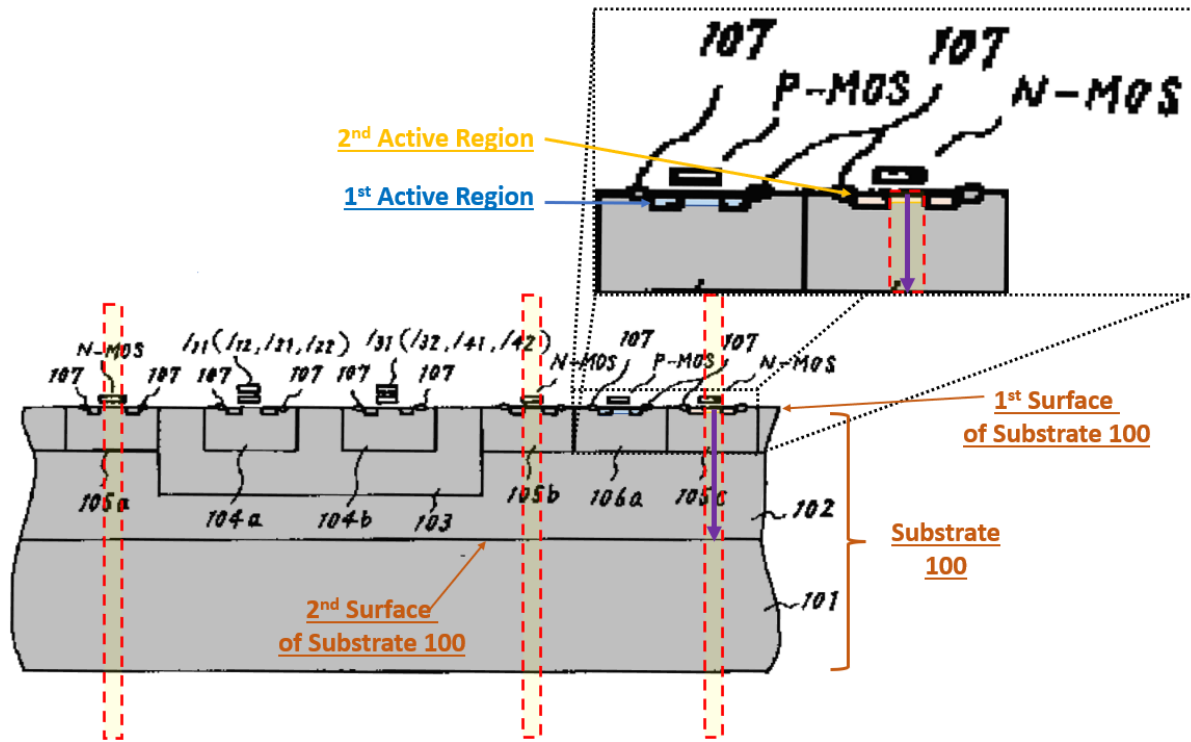
Onoda discloses [1.6]. (Ex. 1003 at ¶¶ 287, 201-206.)

Onoda discloses multiple well regions including at least one well region having a graded dopant region that aids carrier movement from the surface to an area where there are no active regions. Onoda discloses semiconductor well regions in the second semiconductor layer 102 within the substrate 100 that are p doped to form p-well regions, e.g., 105a, 105b and 105c (one colored in green) and n doped to form n-well regions, e.g., 106a, 106b and 106c (one colored in yellow). (Onoda at [0041]-[0045].) As can be seen from FIG. 3 of Onoda below, the p-well region 105c is adjacent to the first active region located near the top of the p-well region 105c, and the n-well region 106a is adjacent to the second active region located near the top of the n-well region 106a.

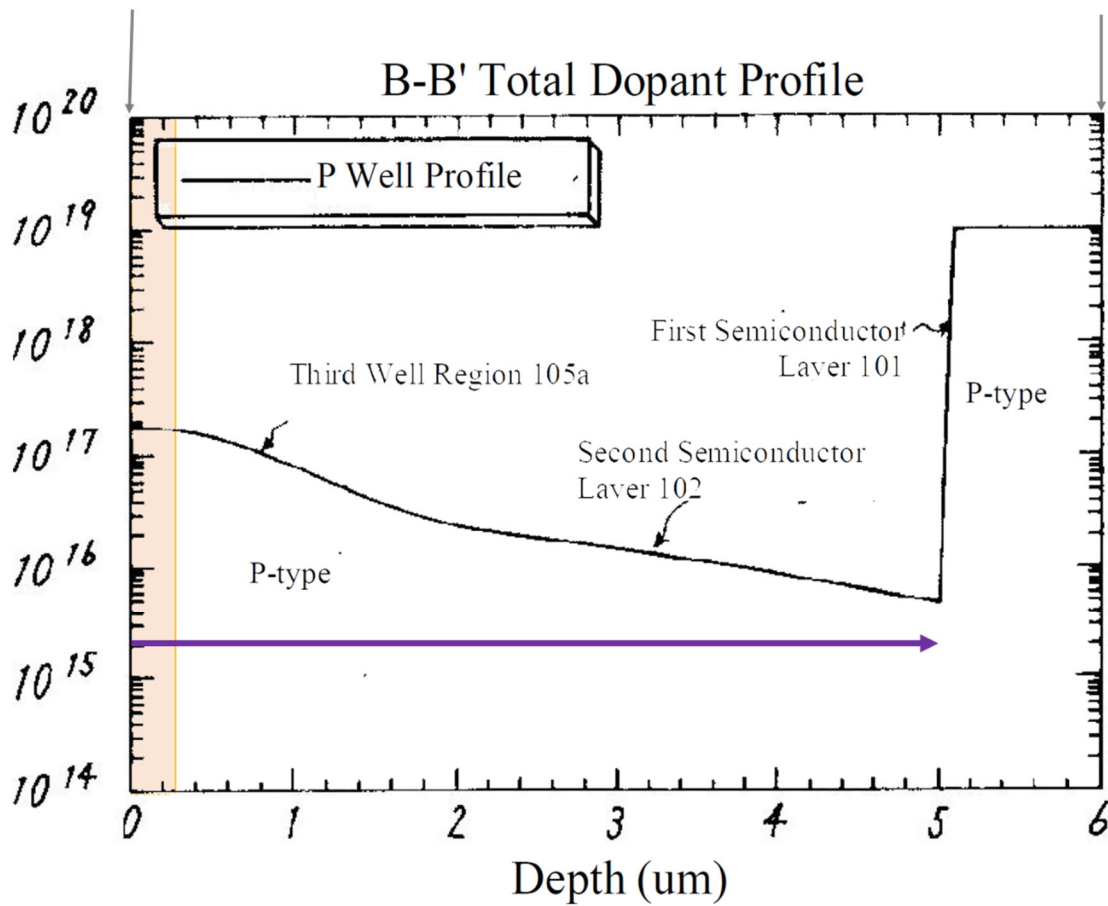


These active regions within the wells further have a graded dopant region to aid carrier movement downward. FIG. 11 in Onoda discloses that the p-well region 105a in Onoda at least has a p dopant concentration decreases from the top surface of the p-well region 105a (the first surface of the substrate 100) into the well region 105a. (Onoda at [0052].) The p-well regions 105b and 105c have the same graded dopant concentration profile. As discussed above regarding Element [1.5], this graded dopant region in the p-well region 105a, 105b or 105c drives electrons to the bottom of the respective well region towards the bottom of the substrate and, accordingly, has the effect “to aid carrier movement from the surface towards the area of the substrate where there are no active regions.”

The dopant profile of FIG. 11 annotated on top of FIG. 3 is provided again below.



(Onoda at FIG. 3 (Annotated).)



(Onoda at FIG. 11 (Annotated).)

As can be seen from the above, the “well region” adjacent to the “first or second active region” has a graded dopant profile that drives carriers downward, and Element [1.6] is met.

h. Element [1.7]

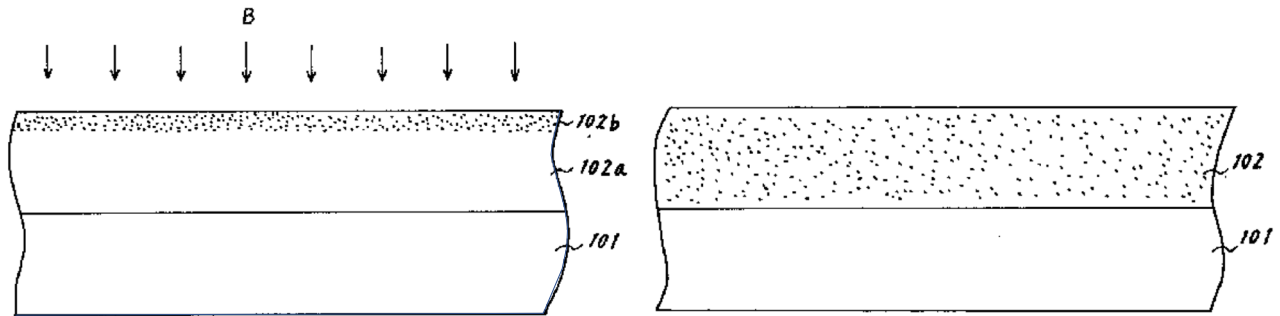
Onoda renders obvious [1.7].

Onoda renders obvious this element. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) In addition, a POSITA would have understood that the doping gradient aspect of the flash memory semiconductor devices would be useful in logic devices as both memory and logic devices suffer from issues related to minority carrier movement, and would have found it obvious to apply teachings from flash to VLSI. (Ex. 1003 at ¶ 288.)

Onoda thusly teaches, or at least renders obvious, claim 1.

2. Claim 3

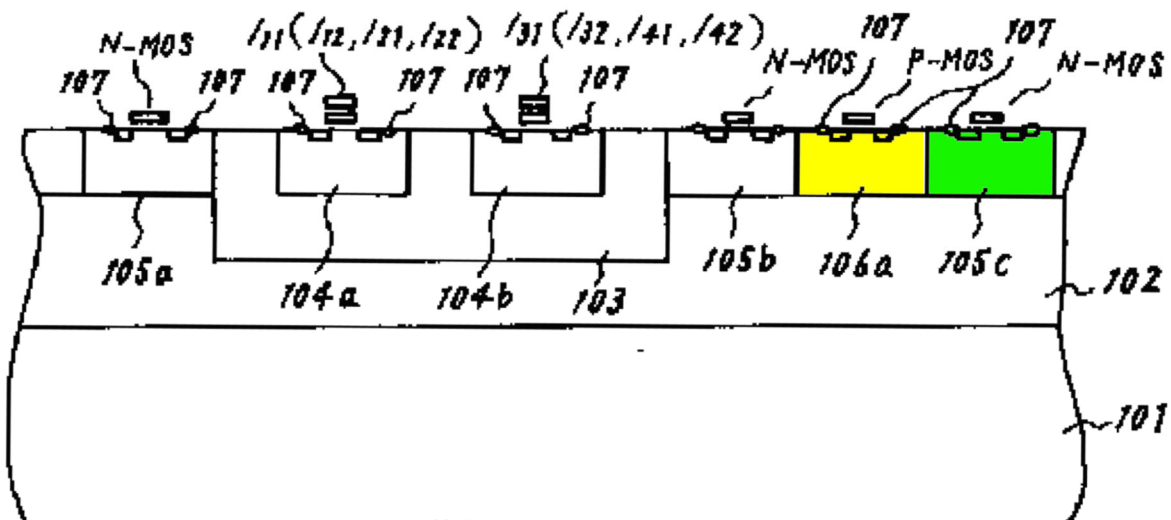
Onoda discloses this element. (Ex. 1003, ¶¶119, 290.) In particular, Onoda teaches that the substrate 100 includes the epitaxial semiconductor substrate 102 on top of a nonepitaxial substrate 101 which is a heavily-doped p-type silicon substrate. (Onoda at [0041] and [0046]-[0047].) As shown in Figure 5, Onoda’s lightly-doped P-type semiconductor layer 102 is an epitaxial layer on top of the first semiconductor layer 101 which is a nonepitaxial substrate. Onoda thusly teaches this claim.



(Onoda at FIGS. 4-5.)

3. Claim 4

Onoda discloses this element. (Ex. 1003, ¶120, 291.) In particular, as shown in annotated FIG. 3 of Onoda, each of Onoda’s active regions contains one of either p-channel and n-channel devices. Onoda discloses that a “plurality of N-channel MOS transistors” are contained in the second active regions formed in P-type wells 105a, 105b, and 105c, one of which is colored in green. (Onoda at [0044] (“105a, 105b, and 105c are P-type [] well regions”).) Similarly, a “plurality of P-channel MOS transistors” are contained in the first active regions formed in N-type wells 106a, 106b, and 106c, one of which is colored in yellow. (*Id.*) Onoda thusly teaches this claim.

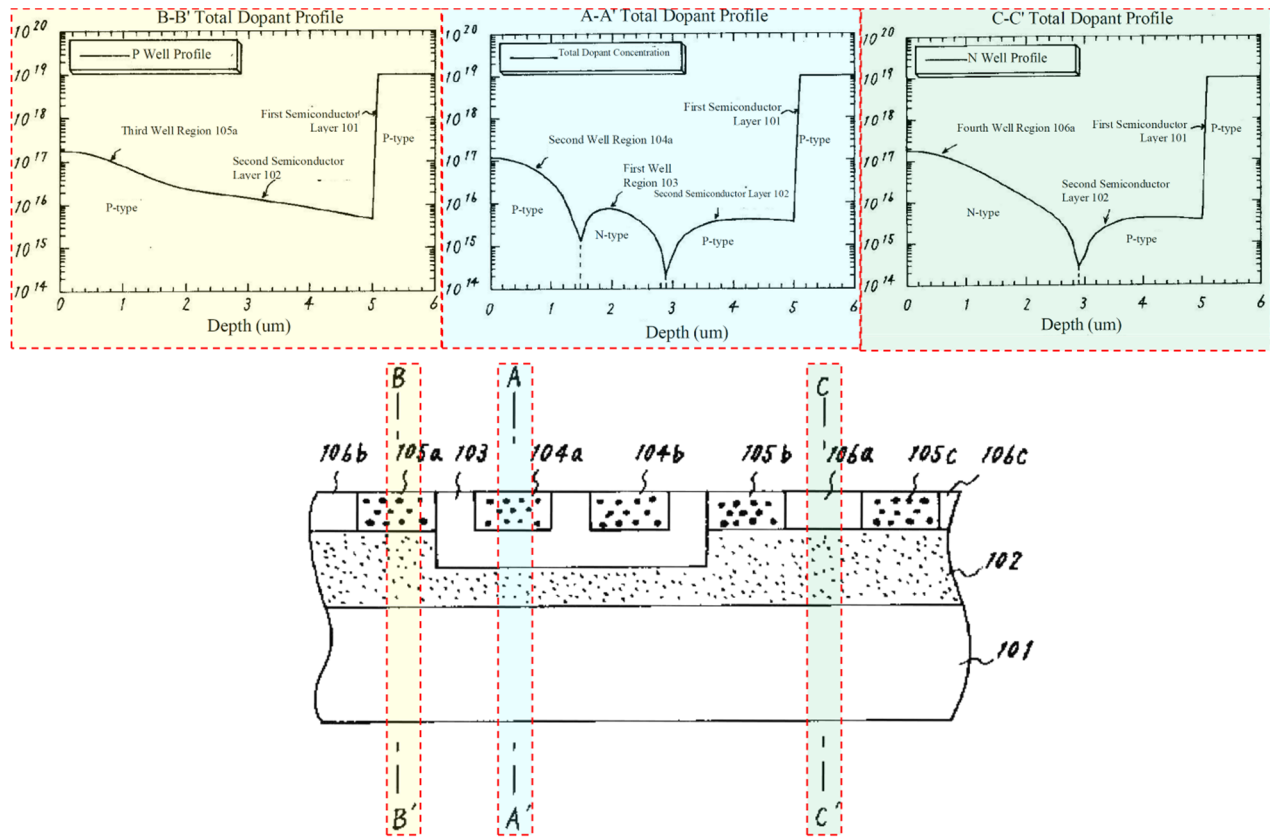


(Onoda at FIG. 3 (Annotated).)

4. Claim 5

Onoda discloses this element. As previously discussed, the second active regions in Onoda contain a plurality of N-channel MOS transistors formed in the p-wells (105a, 105b, 105c) and the first active regions in Onoda contain a plurality of P-channel MOS transistors formed in the n-wells (106a, 106b, 106c). (See Onoda at [0042]-[0044].) Furthermore, each active region has a graded doping profile, as shown in Onoda FIGS. 11 and 12, which depict graded dopant concentration profiles of the p-well 105a in a second active region along the line B-B' (yellow) in FIG. 8 and n-well 106a in a first active region along the line C-C' (green) in FIG. 8, respectively.

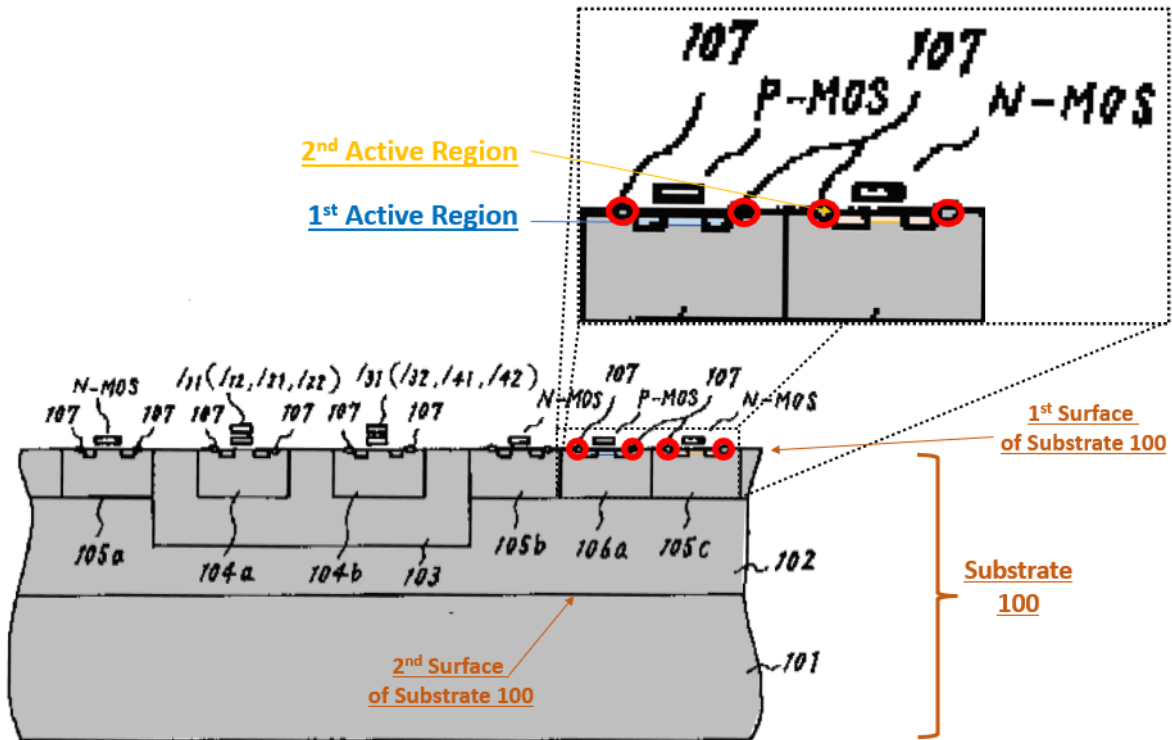
FIG. 8 is further annotated (below) to show the area of the N well region 106a along the line C-C' for which the graded dopant concentration profile along the line C-C' is shown in FIG. 12. A POSITA would understand the figures show the respective dopant profiles decrease in concentration while going further in depth toward the substrate to make a graded dopant in the well-region. (See Onoda FIG. 11 (“Third Well Region 105a”); FIG. 12 (labeled “Fourth Well Region 106a”).) (Ex. 1003, ¶121, 292.) Onoda thusly teaches this claim.



(Onoda at FIGS. 8, 10-12 (Annotated).)

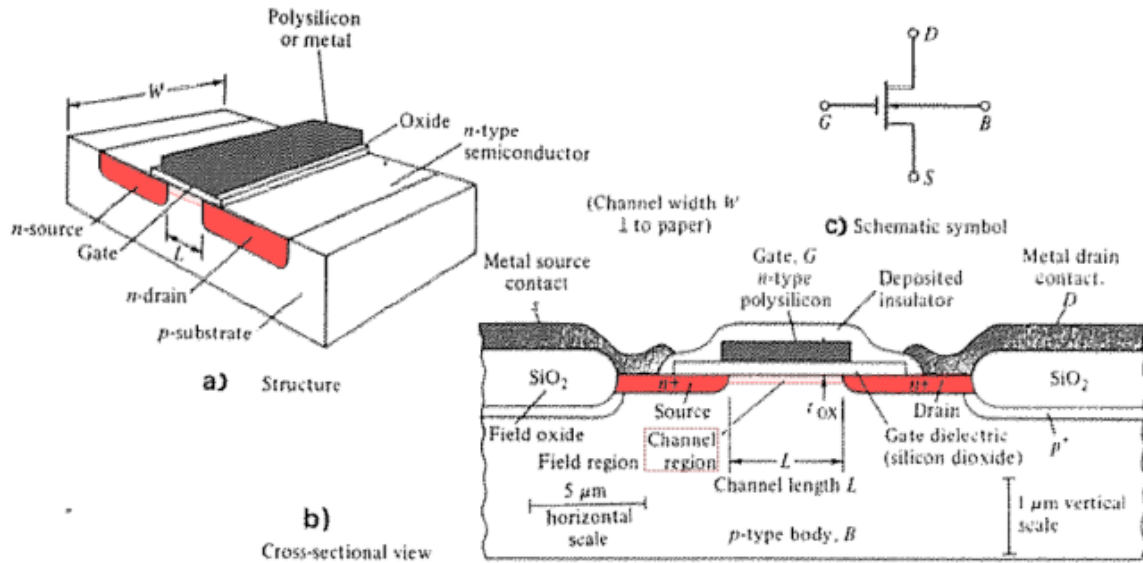
5. Claim 6

Onoda discloses this element. In particular, Onoda discloses an “isolating oxide film (LOCOS) 107, that is formed surrounding the individual MOS transistors, as depicted in FIG. 3.” (Onoda at [0045].) A POSITA would understand that having an isolating oxide film around each individual MOS transistor located in each active region, provides a barrier or “isolation region” to separate the first and second active regions from electrically influencing each other. (Ex. 1003, ¶122, 293.)



(Onoda at FIG. 3 (Annotated).)

In addition, it would have been obvious to employ the teachings of using an isolating oxide film to form an isolation region around each MOS transistor to the entire active region. Long before September 2004 it was standard practice in CMOS integrated circuit design and manufacturing to create an electrical isolation barrier between electrically different areas to safeguard these areas from electrically influencing the other. (Onoda at [0045].) As shown in the figure below from Wolf and Tauber, “[a] thick oxide layer (0.5-1.0 μ m) is normally grown over the field regions” to prevent “[c]onduction between separate active regions.” (Ex. 1030 at 299.) Applying Onoda’s teachings to the entire active region would not only have been obvious to do, it would have been expected. Onoda thusly teaches this claim.



6. Claim 7

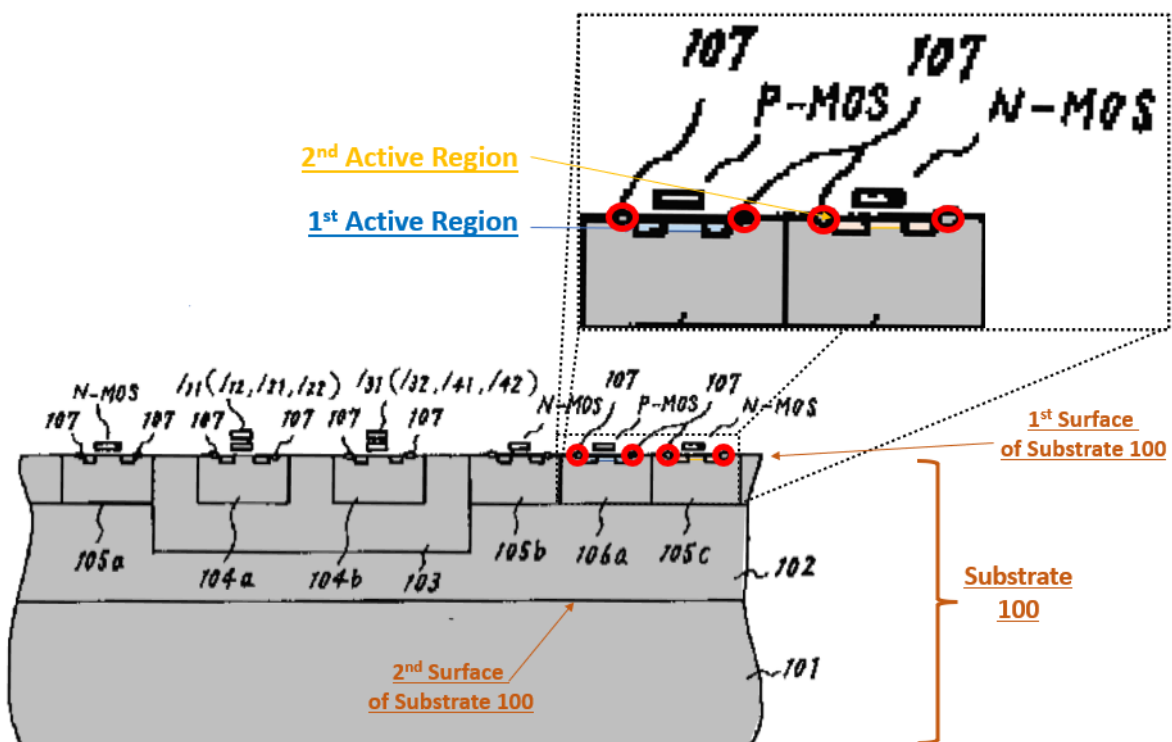
Onoda discloses this element. (Ex. 1003, ¶¶124, 294.) In particular, Onoda teaches that the doped epitaxial semiconductor layer 102 is fabricated using ion implantation and includes an epitaxial layer 102a with a depth of “about 5 μm.” (Onoda at [0046]-[0047].) Further, Onoda teaches forming its well structures with deep wells are formed by ion implantation and thermal diffusion, extending 3-5 μm deep. (*Id.* at [0049]-[0050], [0052].) (See also FIG. 11.) Onoda thusly teaches this claim.

7. Claim 8

Onoda discloses this element. (Ex. 1003, ¶¶125, 295.) In particular, Onoda discloses multiple active regions and each active region is formed adjacent to the first surface of the substrate. Referring to FIG. 3 in Onoda below, the top surface of Onoda’s semiconductor substrate 100 contains the second active regions of the N-MOS

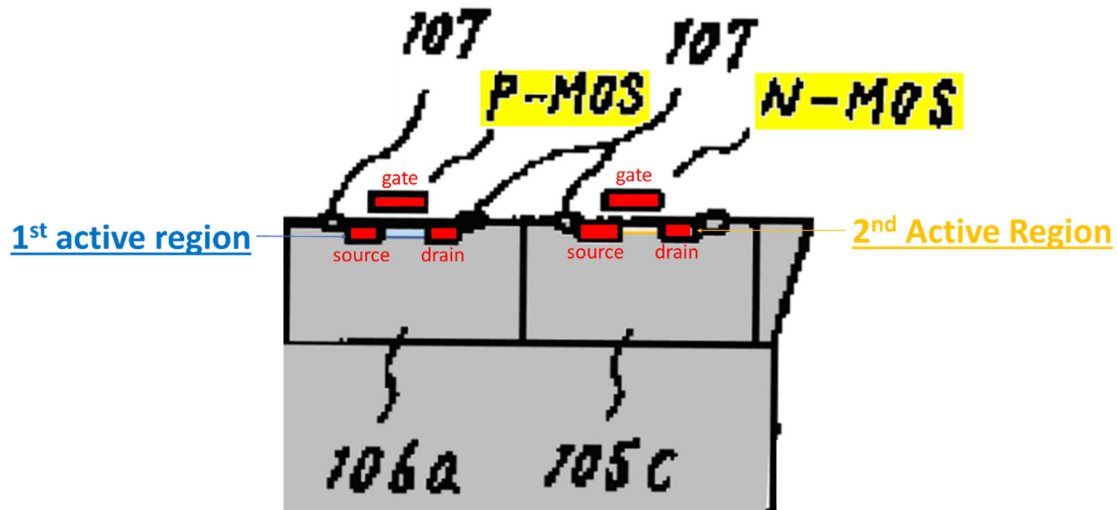
transistor's p-well regions 105a, 105b and 105c. Each of p-well regions 105a, 105b and 105c itself has source and drain regions (marked in red). (Onoda at [0043] (“105a, 105b, and 105c are P-type [] well regions”); *see also id.* at [0044], Claim 2 (“floating gate electrode formed over the second well region, positioned between the source region and the drain region”).)

As can be seen from the annotated FIG. 3 of Onoda below, Onoda's first surface is at the top surface of semiconductor substrate 100, and the source and drain regions (red) of Onoda's transistors are in that first surface. Similarly, the first active region in n-type well region 106a is also located at (or adjacent to) the first surface of the substrate 100 in Onoda.



(Onoda at FIG. 3 (annotated).)

FIG. 3 is further excerpted showing the active regions with a source, drain, and channel.



(Onoda at FIG. 3 (excerpted and annotated).)

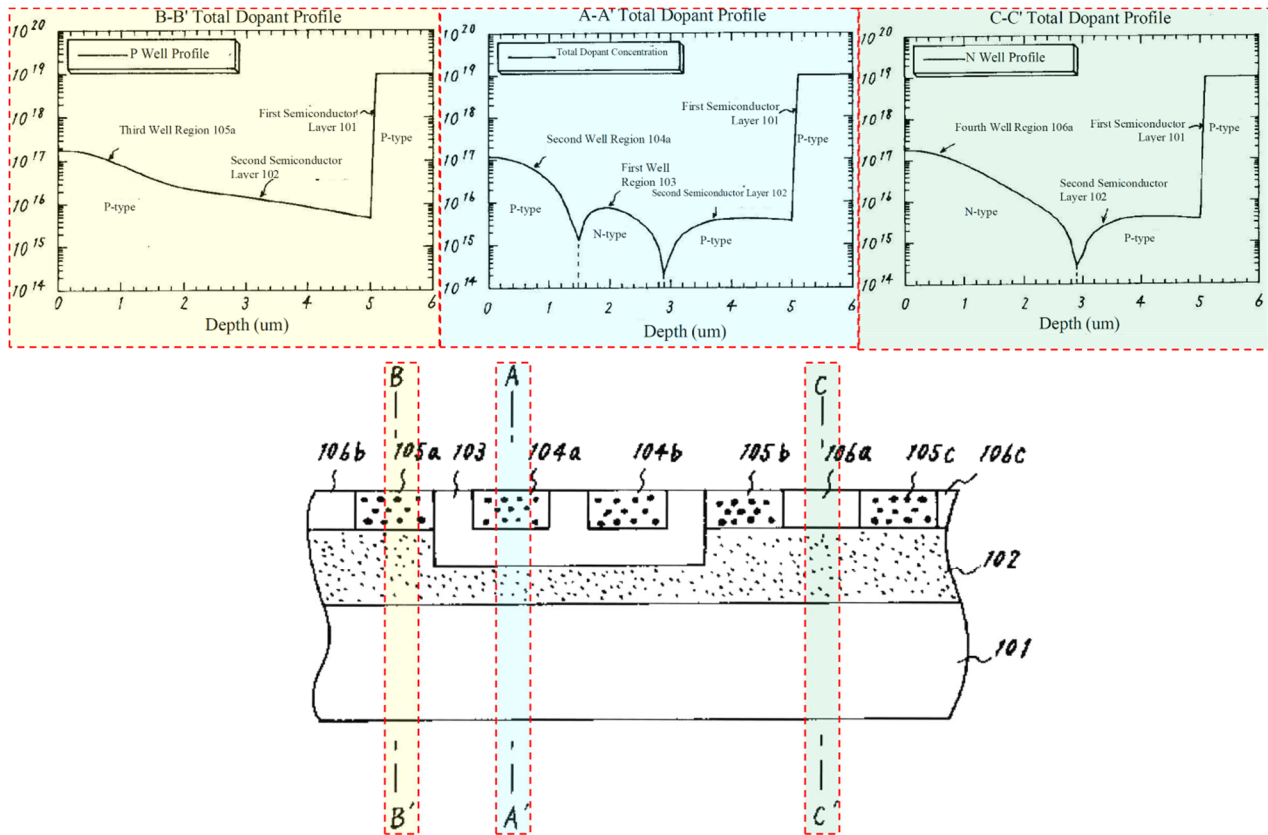
Onoda thusly teaches this claim.

8. Claim 9

Onoda discloses this element. Claim 9 is substantively similar to claim 5.

As previously discussed, the second active regions in Onoda contain a plurality of N-channel MOS transistors formed in the p-wells which are p-type (105a, 105b, 105c) and the first active regions in Onoda contain a plurality of P-channel MOS transistors formed in the n-wells which are n-type (106a, 106b, 106c). (See Onoda at [0042]-[0044].) Furthermore, each active region has a graded doping profile, as shown in Onoda FIGS. 11 and 12, which depict graded dopant concentration profiles of the p-well 105a in a second active region along the line B-B' (yellow) in FIG. 8 and n-well

106a in a first active region along the line C-C' (green) in FIG. 8, respectively. (Ex. 1003 at ¶ 296, 121.) Claim 9 is thusly taught.

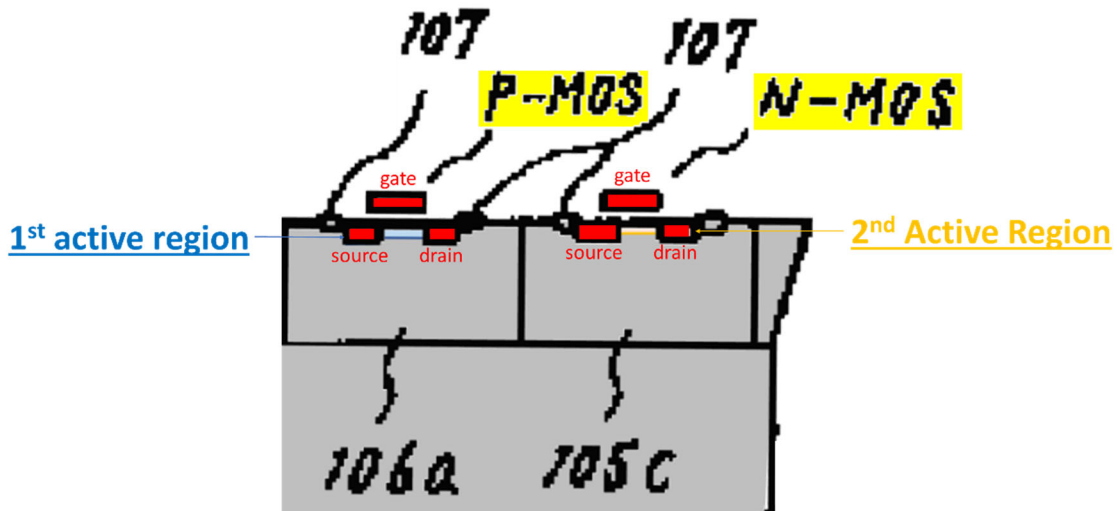


(Onoda at FIGS. 8, 10-12 (Annotated).)

9. Claim 13

Onoda discloses this element. Onoda discloses PMOS and NMOS devices, which a POSITA would understand to be CMOS (which stands for complimentary MOS, having one PMOS and one NMOS). (Ex. 1003 at ¶¶297, 126-129.) As previously discussed, Onoda discloses both N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the first and second active regions. (Onoda at FIGS. 2, 3 and 8, [Abstract], [0041]-[0047], [0052], Claim 2.) The transistors have a source, drain, gate, and channel regions. (Onoda at [0043] (“105a, 105b, and 105c are

P-type [] well regions”); *see also id.* at [0044], Claim 2 (“floating gate electrode formed over the second well region, positioned between the source region and the drain region”).) This is graphically depicted in excerpted FIG. 3, below.



(Onoda at FIG. 3 (excerpted and annotated).) A POSITA would have understood Onoda’s teachings of NMOS and PMOS to be directed to CMOS due to the pervasiveness of CMOS in the art. As of September 2004, the earliest potential priority date of the ‘222 Patent, CMOS was (and it still is) the dominant integrated circuit fabrication technology. (Ex. 1008 at 315 (explaining that MOS technology evolved to have CMOS as the dominant technology).) For example, flash devices have been predominantly manufactured with CMOS since the 1980s. (*Id.* at 369 (explaining that CMOS rose to dominance because of the increased functional density and speed capabilities for both memory and microprocessor (*i.e.*, digital logic) chips).) Moreover, Onoda notes that one of the objectives of the invention “is to provide a semiconductor

integrated device ... with improved resistance to latch-up” (Onoda at [0006]), which a POSITA would have understood to be a problem of CMOS transistors having both NMOS and PMOS transistors as shown in the illustrated circuits in Onoda. (*See* Wolf at 400 (“A major problem in CMOS circuits is the inherent, self-destructive phenomenon known as *latchup*.”) (emphasis in original).). A POSITA would have understood Onoda was directed to CMOS due to its discussion of NMOS and PMOS.

Moreover, even if it were argued that Onoda did not disclose CMOS, it would have been obvious. CMOS was the predominant integrated circuit fabrication technology beginning in the 1980s, and Onoda explicitly describes both NMOS and PMOS transistors on a single device (FIG. 3), which are the ingredients for a CMOS device. Applying Onoda’s teachings to CMOS would not only have been obvious to do, it would have been expected by a POSITA. (Ex. 1003 at ¶¶297, 127-129.). Due to CMOS being NMOS/PMOS pairs, a POSITA would have found that applying Onoda’s teachings to CMOS would yield predictable results. Onoda thusly renders obvious this claim.

10. Claim 15

As described immediately above in claim 13, Onoda renders obvious CMOS. Moreover, Onoda teaches that the substrate 100 includes the epitaxial semiconductor substrate 102 on top of a nonepitaxial substrate 101 which is a heavily-doped p-type silicon substrate. (Onoda at [0041] and [0046]-[0047].) Onoda renders claim 15 obvious. (Ex. 1003 at ¶298.)

11. Claim 16

Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) (Ex. 1003 at ¶299.)

12. Claim 17

Onoda renders obvious this claim. Onoda discloses flash memory semiconductor devices, which are logic device. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) Onoda describes having capacitive devices. (Onoda at [0089]; FIG. 17.) (Ex. 1003 at ¶ 300.)

13. Claim 20

The '222 Patent does not explain which direction is lateral or vertical; nonetheless, Onoda discloses this element. The active regions in Onoda are spread across the top surface of the second semiconductor layer 102 of the substrate 100 which gives them each a position relative to one another in the lateral direction and also spreads down into a portion of each p or n-well relative to the top surface of the well, which places each active region in a position along the vertical direction with respect to the top surface of the well. (*See* Onoda, FIGS. 2 and 3.) (Ex. 1003 at ¶301.)

14. Claim 21

Onoda discloses Claim 21. Independent claim 21 is substantially similar to independent claim 1 with minor modifications (*e.g.*, “transistors can be formed in the surface thereof” as opposed to merely “transistors can be formed,” “aid carrier movement from the surface to the substrate” as opposed to “aid carrier movement from

the first surface to the second surface of the substrate”). (Ex. 1003 at ¶¶302-309.) Elements [21.Pre]-[21.6] are taught for same reasons as [1.Pre]-[1.6].

a. Element [21.7]

Element [21.7] is taught or rendered obvious by Onoda. (Ex. 1003 at ¶¶310-311, 70-117, 201.) Onoda teaches several dopant gradient profiles, in addition to providing graphical depictions of profiles that to a POSITA render a quasi-linear (or linear) gradient obvious. For instance, Onoda’s FIG. 11 depicts a gradient that is quasi-linear (or at least linear). Moreover, Onoda teaches a gaussian distribution of dopants. (Onoda at [0053] (“the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate Gaussian distributions with the concentrations at maxima near the surface”).) Furthermore, providing a quasi-linear gradient was well-known, and this is confirmed by the ’222 Patent describing them amongst a list of known profiles while providing no teachings as to how to construct a device with such profiles. (’222 Patent at 2:60-61 (“The gradient can be linear, quasi linear, exponential or complimentary error function.)) It would have been obvious to apply a quasi-linear gradient in view of a POSITA’s general knowledge that such a gradient facilitates the movement of minority carriers. It would have further been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile, and would have been readily available as a known option.

Onoda thusly teaches this claim.

A. Claim 24

Claim 24/3 are similar and taught for the same reasons.

B. Claim 25

Claim 25/4 are similar and taught for the same reasons.

C. Claim 26

Claim 26/5 are similar and taught for the same reasons.

D. Claim 27

Claim 27/6 are similar and taught for the same reasons.

E. Claim 28

Claim 28/9 are similar and taught for the same reasons.

F. Claim 32

Claim 32/7 are similar and taught for the same reasons.

G. Claim 33

Claim 33/15 are similar and taught for the same reasons.

H. Claim 34

Claim 34/16 are similar and taught for the same reasons.

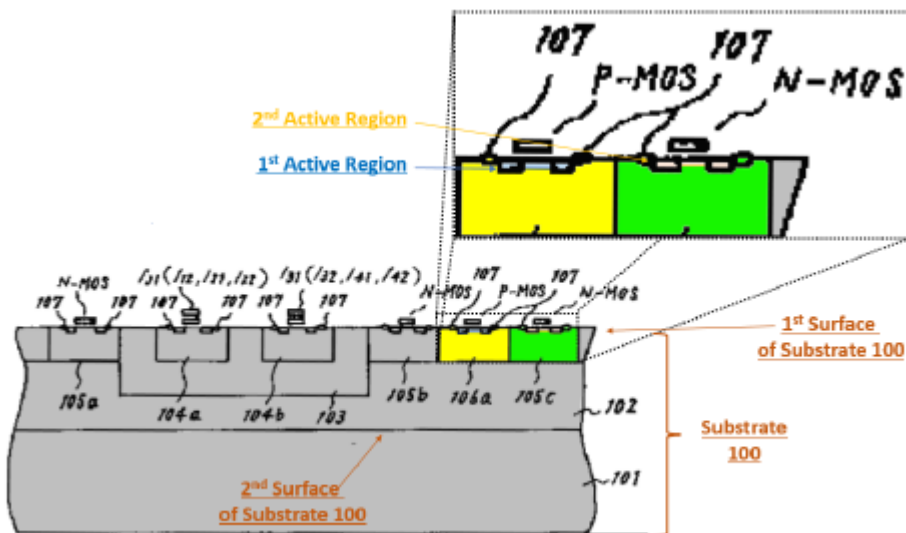
I. Claim 39

Onoda discloses Claim 39 and is substantially similar to claim 1 with minor modifications (*e.g.*, “transistors can be formed in the surface thereof” as opposed to merely “transistors can be formed,” “aid carrier movement from the surface to the substrate” as opposed to “aid carrier movement from the first surface to the second

surface of the substrate”). (Ex. 1003 at ¶¶321-327, 70-117, 201.) Elements [39.pre]-[39.5] are taught for same reasons as [1.pre]-[1.5].

J. Claim 40

Claim 40 is substantively identical to Element [1.6] but recites “the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.” As shown above in the figure below, there is no well in substrate area 101. The wells (in yellow and green) are located in a different area of the substrate. (Ex. 1003 at ¶328.)



K. Claim 41

Onoda discloses Claim 41 and is substantially similar to independent claim 1 with minor modifications (e.g., “transistors can be formed in the surface thereof” as opposed to merely “transistors can be formed,” “aid carrier movement from the surface to the substrate” as opposed to “aid carrier movement from the first surface to the second surface of the substrate”). (Ex. 1003 at ¶¶329-335, 70-117, 201.) Elements

[41.pre]-[41.5] are taught for same reasons as [1.pre]-[1.5]. In addition, Element [41.5] recites “acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region” while Element [1.5] recites “graded dopant concentration.”

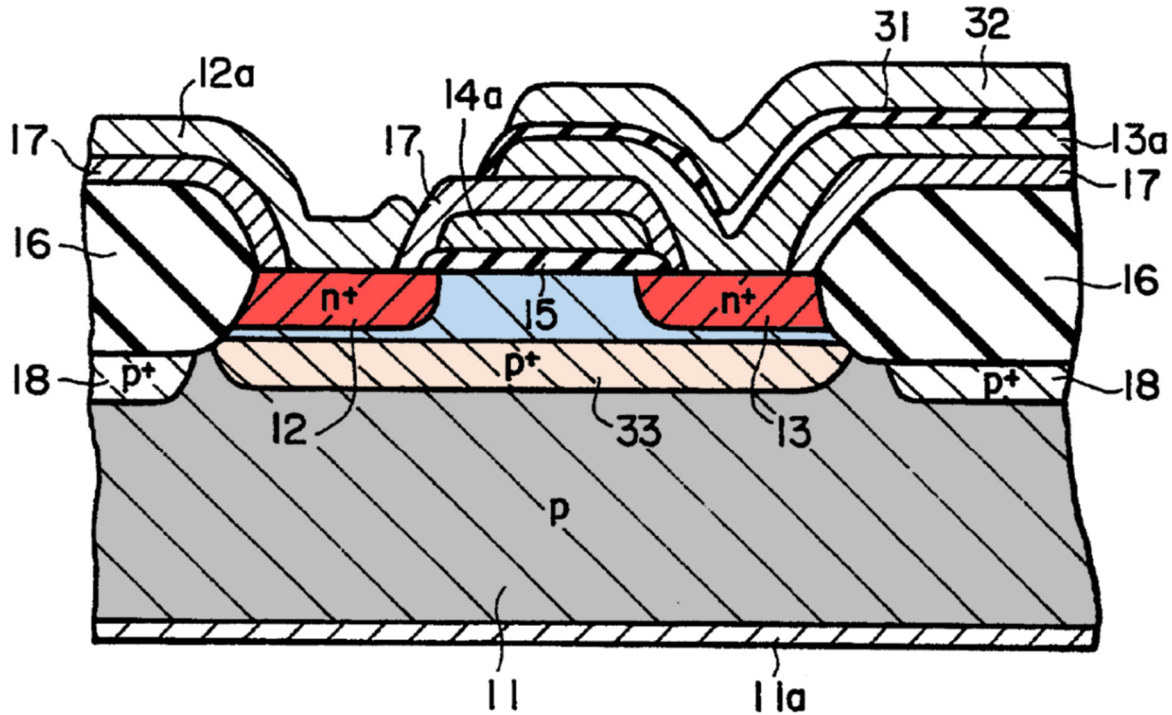
L. Claim 42

Onoda discloses Claim 42. Independent claim 42 is substantially similar to independent claim 1 with minor modifications (*e.g.*, “transistors can be formed in the surface thereof” as opposed to merely “transistors can be formed,” “aid carrier movement from the surface to the substrate” as opposed to “aid carrier movement from the first surface to the second surface of the substrate”). (Ex. 1003 at ¶¶336-342, 70-117, 201.) Elements [42.pre]-[42.5] are taught for same reasons as [1.pre]-[1.5]. In addition, Element [42.5] further recites “donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.”

C. Ground III: Onoda in view of Nishizawa Renders Obvious Claims 1, 3-9, 13, 15-17, 20, 21, 24-28, 32-34, and 39-42 of the '222 Patent.

Onoda and Nishizawa both disclose semiconductor devices and are concerned with minority carriers (electrons) moving into the functioning circuitry. Nishizawa teaches a semiconductor device (Nishizawa at Abstract) that provides a buried region that has a graded dopant profile (annotated tan, below). (*Id.* at FIG. 16, 18:46-67, 20:25-27.) Nishizawa’s source and drain are annotated in red, with the well (which has part of the channel) in blue.

FIG. 16



(Nishizawa at FIG. 16 (Annotated).)

Nishizawa discloses a “CMOS arrangement [that] may be termed an ideal circuit arrangement” (Nishizawa at 15:29-30). Figure 16 is a DRAM which has a p+ type buried region with a high impurity concentration at the “top” that progressively decreases as the buried region gets closer to the substrate. (*Id.* at 18:47-56, 18:64-66.) Decreasing the concentration in this manner provides an electric drift field (*id.* at 18:10-18) that allows minority carriers (electrons) to move from the surface region (blue) having the source and drain (red) to the substrate (gray). (*Id.* at 19:1-9; *see also id.* at 16:19-24.¹³ Nishizawa discloses that if the electrons were allowed to “flow” to the

¹³ While the cited text from Nishizawa principally discusses the technology by

circuit rather than down to the substrate, the circuit would not function correctly. (*Id.* at 19:1-9).)

Likewise, Onoda discloses a semiconductor device having a graded dopant profile. Onoda teaches that “there is a tendency [for the devices] to become a structure wherein latch-up is inherently likely to occur due to transistors of a parasitic thyristor structure.” (Onoda at [004]). Onoda is similarly concerned with unwanted movement of carriers (electrons) into the circuit and causing issues, as a POSITA would understand that issues with “latch-up” are related to such carrier movement. (Ex. 1003 at ¶¶345, 134-140.). Both Nishizawa and Onoda use a graded doping profile to control movement of minority carriers.

A POSITA would have been motivated to combine the teachings of Onoda with the teachings of Nishizawa as both are semiconductors that have a downward doping gradient to drift minority carriers to the substrate. (Ex. 1003 at ¶¶345, 138.). A POSITA would have been motivated to apply Nishizawa’s teachings of minority carrier diffusion based on a downward sloping dopant gradient (*e.g.*, Nishizawa at 18:46-67) to Onoda’s teachings of a downward sloping dopant gradient (*e.g.*, Onoda at

referencing FIG. 35, both FIGS. 35 and 16 depict DRAM cells (Nishizawa at 8:25-27, 63-65) with a buried layer. The buried layer in FIG. 16 extends under both the source and drain regions, which a POSITA would understand provides for a more effective movement of the electrons to the substrate.

FIG. 11). (Ex. 1003 at ¶¶345, 138.). Both Nishizawa and Onoda disclose similar structures with a graded dopant, and while Onoda generally references known issues related to minority carrier movement (*e.g.*, soft errors and latch-up), Nishizawa makes explicit the concept of using an electric field, deliberately created through a dopant gradient, to move minority carriers to a substrate (Nishizawa at 18:10-18). A POSITA would have been motivated to combine teachings of Nishizawa's explicit discussion of concepts to the structures described in Onoda as confirmation of Onoda's teachings.

Making this combination of teachings would have combined known elements to achieve predictable results (*e.g.*, applying Onoda's downward dopant gradient to Nishizawa's teaching of the electric fields and minority carrier drifts that a downward dopant gradient inherently creates). A POSITA would have understood that such combinations of known prior art elements would yield expected results and, moreover, would have found it obvious to try such combinations. (Ex. 1003 at ¶¶345, 139.).

Moreover, both Nishizawa and Onoda are directed to similar devices, which face similar problems, and seek similar solutions. Both are directed to memory devices (Nishizawa at Abstract; Onoda at [0004]), and to reducing punch through. (Nishizawa at Title; Onoda at Object.) (Ex. 1003 at ¶¶345, 140.).

1. Claim 1

a. Preamble

Nishizawa teaches a CMOS semiconductor device. (Nishizawa at Abstract, 7:61-62.) Nishizawa discloses both memory and CMOS semiconductor devices. (Nishizawa at 7:40-63, FIG. 32 and 15:27-52.) (Ex. 1003 at ¶¶345, 138.).

b. Elements [1.1]-[1.4]

Consistent with Ground II, Onoda discloses and/or renders obvious Elements [1.1] through [1.4]. (Ex. 1003 at ¶¶345, 142.).

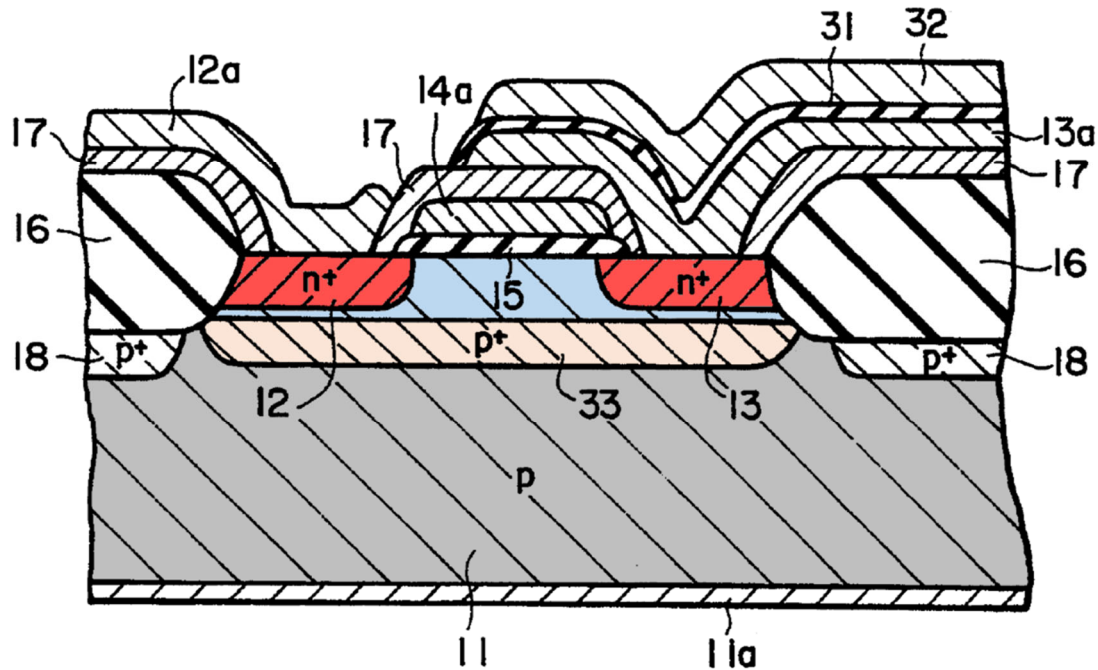
c. Elements [1.5] and [1.6]

Onoda discloses multiple active regions whose dopant concentrations have a downward gradient, which a POSITA would have recognized as providing an electric drift field in the active region to aid the movement of minority carriers from the first surface to the second surface of the substrate (substrate 100). (Ex. 1003 at ¶¶345, 143.). Nishizawa similarly discloses employing graded dopant concentrations to create drift electric fields to aid carrier movement. (Nishizawa at 18:10-18.). Nishizawa makes explicit that the downward gradient aids in the movement of carriers to the substrate. (*Id.* at 18:47-50, 19:1-19; *see also* 18:10-18.)

FIG. 16 in Nishizawa depicts a source and drain (red, below) at the surface region (blue), where buried region 33 (tan) provides an “impurity concentration gradient ... [that is] progressively decreasing toward the p type substrate” (gray). (Nishizawa at 19:4-5; *see also id.* at 18:50-59.) The cited-to text refers to the

embodiment of FIG. 35, and Nishizawa states that the discussion is likewise applicable to the structure of FIG. 16 which is illustrated. (Nishizawa at 20:23-27.)

FIG. 16



(Nishizawa at FIG. 16 (Annotated).)

Nishizawa teaches “a drift electric field” that is created when there is a “difference in the degree of impurity concentration,” which is used to drift minority carriers to the substrate. (Nishizawa at 18:9-18.) To drift electrons from the p+ buried layer to the substrate, “an impurity concentration gradient in the p+ type buried region 33a in the direction toward the p type substrate” is formed. (*Id.* at 18:35-50; *see also id.* at 18:51-67; *see also id.* at 19:1-9.) Onoda-Nishizawa thusly discloses Elements [1.5] and [1/6].

2. Claims 21, 39, 40, 42

Independent claims 21, 39, 40, 42 are substantively similar to claim 1, and are rendered obvious by the same reasons as described with respect to claim 1.

3. Claims 13, 15, 33

Nishizawa teaches CMOS. FIG. 32 depicts using NMOS and PMOS as CMOS (Nishizawa at FIG. 32 and 15:27-52) and further states one of its objects is to provide an improved CMOS device (*id.* at 7:61-63). Onoda-Nishizawa thusly discloses and renders obvious claims 13, 15, and 33.

4. Claims 3-9, 15-17, 20, 24-28, 32, 34, and 40

Claims 3-9, 15-17, 20, 24-28, 32, 34, and 40 are disclosed and/or rendered obvious by the Onoda-Nishizawa combination for the same reasons as discussed in Ground II and claim 1 of Ground III.

X. THE BOARD SHOULD INSTITUTE IPR

1. 35 U.S.C. § 314(a)

“[T]he PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling evidence of unpatentability.” (Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 9 (June 21, 2022).) Kawagoe is subject to a ground in the already-instituted Petition in IPR2024-01242 and the Board has already determined that there is a reasonable likelihood of invalidity. As another example, Onoda (Ground II) is a single-reference obviousness ground explaining how Onoda renders obvious all of the Challenged Claims. Ground III presents Onoda in combination with Nishizawa.

None of Onoda or Nishizawa are subject to the pending *Inter Partes* Reviews, nor were they before the USPTO. And, this evidence, “if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable” (Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” at 4) and the Board must decline to exercise its discretion under §314(a) to deny institution. *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022- 00938, Paper 8 at 9 (P.T.A.B. Nov. 1, 2022).

Finally, Petitioner is a separate party than those of other proceedings, and it has faced unique infringement contentions that had been served on December 13, 2023 (which further crystalized Patent Owner’s asserted claims). The Petition presents unique challenges using Onoda, not present in any other filed Petition, which demonstrate unpatentability considering Patent Owner’s infringement theories and understanding of claim scope. Tellingly of the strength of the prior art, Patent Owner provided no argument of patentability over the prior art cited in IPR2023-01242. *See* IPR2023-01242, Paper 35.

2. 35 U.S.C. § 325(d)

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020).

The Board has consistently “held that a reference that ‘was neither applied against the claims nor discussed by the Examiner does not weigh in favor of exercising [] discretion under §325(d).” *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7–11 (P.T.A.B. Nov. 5, 2019); *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5-6 (P.T.A.B. Aug. 6, 2019). That is the case here because none of the references presented in grounds (Onoda, Kawagoe, Nishizawa) is cited art by the ’222 Patent, and the arguments presented herein were not considered during its prosecution.

Patent Owner had previously incorrectly argued that other art not at issue in this Petition was cumulative to already-examined art (U.S. Pat. Pub. No. 2003/0042511, Rhodes) in the ’222 Patent’s parent (’195 Patent). (Ex. 1011 at 21-24.) Patent Owner’s arguments there lacked merit, and are similarly inapplicable to Onoda, Nishizawa, and Kawagoe because Onoda and Kawagoe are not cumulative with Rhodes. The Examiner relied on Rhodes’ paragraphs [0046], [0047], [0049], and [0049], and FIGS. 5-14 in rejection, stating that well-regions 160/170/180 aid carrier movement from the surface regions to the substrate. (Ex. 1002 at 55-56.) In response, Patent Owner amended the claims to recite “VLSI digital” and that “the active channel regions” aid in carrier movement (Ex. 1002 at 72, 94), and further argued that Rhodes is inapplicable to CMOS image sensors because it only provides a graded dopant concentration in the image sensor. (Ex. 1002 at 74; *see also id.* at 97.) The Examiner thereafter dropped rejections based on Rhodes. (*Id.* at 111-115.)

Here, in contrast, both Onoda and Kawagoe describe CMOS and, moreover, provide graded dopants in p wells having active regions that form conductive channels in memory devices. (Ex. 1003 at ¶¶ 32-34.) Moreover, Figure 2 of Onoda discloses forming P-type well regions (105a through 105c) and N-type well regions (103, 106a through 106c) in a lightly-doped semiconductor layer 102 that is formed through epitaxial deposition. (Onoda at FIG. 2.) Kawagoe similarly provides well regions doped into an epitaxial layer. (Kawagoe at FIG. 16.) Onoda and Kawagoe describe non-cumulative systems that are relevant to the claims in a manner that Rhodes was not.

Onoda and Kawagoe are not cumulative and, even assuming *arguendo* that they were, the Examiner overlooked Rhodes’ relevance to CMOS devices, generally, and downward graded dopant well regions as claimed due to Patent Owner’s arguments regarding Rhodes. In either case, review of the challenged claims is warranted.

3. Prior Petitions Do Not Warrant Denying Institution

MPS pursues this IPR Petition for the reasons Congress intended—as a “quick and cost-effective alternative[] to litigation” (H.R. Rep. No. 112-98, pt.1, 40 (2011), 2011 U.S.C.C.A.N. 67, 69). *General Plastic* factors do not provide a basis for denial. *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, 18 (Sept. 6, 2017) (precedential).

Factor 1 examines “whether the same petitioner previously filed a petition directed to the same claims....” *Qualcomm v. Monterey Research*, IPR2020-01493,

Paper 11, 15 (Mar. 8, 2021). *General Plastic* addressed multiple petitions by the same petitioner, but this is MPS’s only petition against the Challenged Claims. Further, *Valve* extended the *General Plastic* doctrine to include cases with a “significant relationship” between different petitioners such as that between HTC and Valve—HTC had incorporated Valve’s technology into its device, under license and with technical assistance from Valve. *Valve Corp. v. Electronic Scripting Prods., Inc.*, IPR2019-00062, Paper 11 at 9-10 (Apr. 2, 2019) (precedential). MPS and other Petitioners are not the same entity, and there is no relevant relationship between them. Greenthread sued other petitioners before it sued MPS, accusing completely different products. Greenthread cannot be heard to complain that its subsequent suit triggered subsequent IPRs. And unlike HTC and Valve, MPS did not incorporate those other defendants’ technologies under license or receive defendants’ technical assistance with respect to the accused products, or vice versa. Greenthread is accusing MPS of patent infringement separately from and independently of others. Further, MPS had no involvement with any other defendants’ IPR petitions, and vice versa. Accordingly, Factor 1 weighs “strongly” against denial.

Factor 2 examines “whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it.” *Qualcomm*, 17. “Unlike Valve, [MPS] does not have a significant relationship with other petitioner[] challenging the same patent.” *Sony Mobile Comm. AB, et al*, IPR2021-00663, Paper 17, 12 (citing *Netflix, Inc. v. Broadcom Corp.*, IPR2020-01423,

Paper 7 at 5-6 (Mar. 11, 2021)). Therefore, Factor 2 has “limited, neutral value” because the parties are “neither the same ... nor related.” *Qualcomm* at 17.

Factor 3 examines whether MPS received a Preliminary Response or an institution decision for another’s petition. *Qualcomm*, 18. This factor should be in favor of MPS. As the Director explained in *Code200*, “road-mapping concerns are minimized” when, as here, the petitioner did not and could not “refine[]” its petition in view of any “lessons learned from later developments” because prior POPRs in other petitions on the ’222 Patent (*e.g.*, IPR2024-001242 and IPR2023-01244) were filed at the PTAB confidentially for the Board and parties only and thus were not available to MPS and the public. In addition, the technical merits of the previous POPRs have not been addressed by the Board to provide any road-mapping for MPS because the Patent Owner in those IPRs did not challenge claim limitations. *Code200, UAB v. Bright Data Ltd.*, IPR2022-00861, Paper 18 at 5 (Aug. 23, 2022) (precedential) (“Code200”); Paper 14 (POPR) at 25-70 (June 20, 2022) (extensively addressing the merits). Indeed, the Board recently refused to deny institution under *General Plastic* despite two previous IPRs by other parties against the same patent, one of which was instituted and terminated due to settlement. *Siemens Gamesa Renewable Energy, Inc. v. General Elec. Co.*, IPR2022-01479, Paper 11 at 10-14 (Mar. 7, 2023).

In another example, the Board faced similar circumstances as here: Google and Facebook were sued by Express Mobile on the same day, but Facebook filed its IPR roughly five months after Google—and thus after Express Mobile filed its POPR, but

before the Board issued its institution decision. *Facebook, Inc. v. Express Mobile*, IPR2021-01455, Paper 11 at 12-13. As the Board explained, because Facebook “filed [its] Petition before the Board issued its decision in the [Google IPR],” Facebook “received limited benefit from having been able to review [the POPR] in that matter.” *Id.* Here, each other defendant in other prior IPRs was sued before MPS, and MPS filed its IPR after. This factor does not favor denial.

Factor 4 is “based on the elapsed time between... petitioner learn[ing] of the prior art asserted in the second petition and the filing of the second petition,” and Factor 5 relates to Petitioner’s explanation for time elapsed between petitions. *Sony*, 13-15. As in *Sony*, this “is [MPS’s] first petition challenging the [’222 Patent] there is no filing of a second petition challenging the same patent by [MPS]. And, unlike Valve, [MPS] does not have a significant relationship with the other petitioner[,]” and therefore Factor 4 “weighs strongly in favor of institution.” *Sony*, 14. Factor 5 also “weighs strongly in favor of institution” where, as here, MPS “did not file a prior petition.” *Id.*

Further, as in *Qualcomm*, MPS’s Petition was filed before the statutory deadline, and MPS ““had zero influence over [others’] Petitions.”” *Qualcomm*, 18. MPS did not discuss IPR strategy with defendants and is not a RPI in their petitions, and the timing of MPS’s filing here had nothing to do with others’ (who were sued months before MPS). Like *Qualcomm*, MPS’s counsel “developed invalidity positions from the time the suit was filed until filing the Petition.” *Qualcomm*, 18. Indeed, MPS filed its Petition just 3 months after Greenthread served its preliminary infringement

contentions. Factors 4 and 5 weigh strongly in favor of institution.

Factors 6 and 7 consider the Board's finite resources and requirement to issue a final determination within a year of institution. *Qualcomm*, 18. There is only one ground from 3 grounds that cites Kawagoe that is also used as prior art in other IPRs, e.g., IPR2023-01242 and IPR2024-01244. Onoda and Nishizawa are in 2 grounds that were not presented in any others' IPRs. Further, there is no risk the Board could not issue a final determination within a year. This factor thus does not weigh against institution of this Petition. *Microsoft Corp. v. Iron Oak Techs., LLC*, IPR2019-00107, Paper NO. 8, 53-54, 58 (May 15, 2019) (finding "factors six and seven do not weigh in favor of exercising our discretion to deny institution" even though two other petitions on same patent were pending).

Other factors considered by the Board extending the *General Plastics* factors further weigh towards institution. Here, if not instituted, MPS would be prejudiced if other parties settled their IPR (or did not prevail on its distinct arguments), and multiple petitions being filed is a direct result of Greenthread's litigation activities suing numerous other defendants besides MPS. *Microsoft Corp., LLC*, IPR2019-00107, Paper No. 8, 53-54.

Finally, MPS filed a separate petition against the '222 Patent addressing claim 44, alone, in IPR2024-00470 which was filed on Feb. 3, 2024. Claim 44 is substantively different than the Challenged Claims here, and a second Petition was necessary given the word-count. Notably, Petition IPR2024-00470's lone challenged

claim 44 claims a “surface layer,” a “single drift layer,” and “at least one well region disposed in the single drift layer,” which are not claimed in the Challenged Claims of the instant Petition. Indeed, the Board faced similar claim groupings and felt two Petitions was appropriate by a single petitioner. (IPR2023-01242, Paper 32; IPR2023-01244, Paper 35.) Petitioner thusly requests that the Board review and institute both Petitions.

Dated: March 18, 2024

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CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(d)

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this *Petition for Inter Partes Review* totals 13,453, excluding the parts exempted by 37 C.F.R. §42.24(a).

The word count was made using the built-in word count function in the Microsoft 365 software used to prepare this document.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of this PETITION FOR INTER PARTES REVIEW and supporting materials (Exhibits 1001-1030, 1032-1052 and Power of Attorney) have been electronically served in their entireties on counsel for patent owner as follows:

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In addition, the undersigned certifies that a true copy of the petition and supporting materials have been served on Patent Owner via email to its legal counsel:

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