UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MONOLITHIC POWER SYSTEMS, INC.,

Petitioner,

v.

GREENTHREAD, LLC,

Patent Owner.

PTAB Proceeding Nos.:
IPR2024-00550 on U.S. Patent No. 10,510,842
IPR2024-00551 on U.S. Patent No. 10,734,481
IPR2024-00552 on U.S. Patent No. 11,121,222
IPR2024-00553 on U.S. Patent No. 11,316,014

DECLARATION OF STEPHEN CAMPBELL IN SUPPORT OF PETITIONS FOR *INTER PARTES* REVIEW OF U.S. PATENT NOS. 10,510,842; 10,734,481; 11,121,222; AND 11,316,014

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I. INTRODUCTION

1. I, Stephen Campbell, have been retained by Petitioner Monolithic Power Systems, Inc. ("Petitioner") to investigate and opine on certain issues relating to certain patent claims in United States Patent Nos. 10,510,842; 10,734,481; 11,121,222; and 11,316,014 (the "'842 Patent," "'481 Patent," "'222 Patent," and "'014 Patent" respectively) in Petitions for *Inter Partes* Reviews. The Petitions request that the Patent Trial and Appeal Board ("PTAB" or "Board") review and cancel the following claims in Petitions identified by their respective PTAB proceeding case numbers:

- PTAB Case No. IPR2024-00550: Claims 1, 2, 4-9, and 12-18 of the '842 Patent;
- PTAB Case No. IPR2024-00551: Claims 1-9, 13, 15, 17, 20, 22-27, 31, 32, and 34 of the '481 Patent;
- PTAB Case No. IPR2024-00552: Claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, and 39-42 of the '222 Patent; and
- PTAB Case No. IPR2024-00553: Claims 1, 3-9, 13, 15-17, 20-21, and 23-28 of the '014 Patent.

2. I provide my analysis of these four patents in a single declaration due to the significant overlap in subject matter of the above identified claims in the four

patents. I have limited my analysis to the above-identified claims and my lack of analysis with respect to other claims of the ’842, ’481, ’222 and ’014 Patents should in no way be interpreted as a concession of their validity.

3. I reserve the right to provide further opinion in other proceedings regarding those claims. I have also provided my analyses and opinions on certain patent claims in the following listed patents in 3 pending PTAB proceedings:

- PTAB Case No. IPR2024-00468 on Claims 1-3, 5 and 6 of United States Patent No. 8,421,195 (the “‘195 Patent);
- PTAB Case No. IPR2024-00469 on Claims 7 and 8 of United States Patent No 9,190,502 (the “‘502 Patent”); and
- PTAB Case No. IPR2024-00470 on Claim 44 of the ‘222 Patent.

4. The opinions set forth in this declaration on the ’842, ’481, ’222 and ’014 Patents are based on my personal knowledge, my professional judgment, and my analysis of the materials and information referenced in this declaration and its exhibits.

5. I am being compensated for consulting services. I am also reimbursed for reasonable and customary expenses associated with my work in this case. I receive no other forms of compensation related to this case. My compensation does not depend on the outcome of this post-grant review or the co-pending district court

litigation, and I have no other financial interest in the post-grant review or the co-pending district court or Petitioner.

6. I understand that the '842, '481, '222 and '014 Patents have been assigned to Greenthread, LLC. I make no opinion on whether this assignment or ownership is correct.

7. This declaration is based on the information currently available to me. To the extent that additional information becomes available, I reserve the right to continue my investigation and study, which may include a review of documents and information that may be produced, as well as testimony from depositions that have not yet been taken.

A. Qualifications

1. Education and Work Experience

8. I received my Bachelor's degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the

company. This involved a wide variety of process technologies for submicron CMOS.

9. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than $100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200 mm wafers, particle control in CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I

developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

10. A brief summary of my work at the University would include:

A. Approximately 200 publications

B. The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.

C. Honors from outside the University such as being named a Presidential Young Investigator by the National Science Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

D. Honors within the University including outstanding service and outstanding teaching.

E. As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new $80M building with an expansive cleanroom facility.

11. Since retiring from the University, I have consulted with semiconductor companies including patent litigation.

2. Curriculum Vitae

12. A copy of my curriculum vitae is attached as Appendix A to this declaration.

B. Materials Reviewed

13. My opinions expressed in this declaration are based on documents and materials identified in this declaration, including the '842, '481, '222 and '014 Patents, the prior art references and background materials discussed in this declaration, and the other references specifically identified in this declaration. I have considered these materials in their entirety, even if only portions are discussed here.

14. I have also relied on my own experience and expertise in semiconductor fabrication.

C. Level of Ordinary Skill in the Art

15. I am not an attorney and offer no legal opinions. I have been informed about certain aspects of the law for purposes of my analyses and opinions.

16. I understand that in analyzing questions of invalidity and infringement, the perspective of a person having ordinary skill in the art ("POSITA") is often implicated, and the Board may need assistance in determining that level of skill.

17. I understand that the claims and written description of a patent must be understood from the perspective of a POSITA. I have been informed that various factors may affect the level of skill of the hypothetical POSITA, including, for example, (1) the type of problems encountered in the art; (2) the prior-art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the educational level of active workers in the field. A person of ordinary skill in the art is also a person of ordinary creativity in the art.

18. In my opinion, a POSITA of the subject matter of the '842, '481, '222 and '014 Patents at the time of the alleged inventions (in this case, September 2004) would have had a Bachelor's degree in electrical engineering, chemical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for a deficiency in experience, and vice-versa.

D. Summary of Opinions

19. I have reviewed and analyzed the '842, '481, '222 and '014 Patents.

20. Based on my review and analysis, it is my opinion that claims 1-2, 4-9, and 12-18 of the '842 Patent, claims 1-9, 13, 15, 17, 20, 22-27, 31-32, and 34 of the '481 Patent, claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, and 39-42 of the '222

Patent and claims 1, 3-9, 13, 15-17, 20-21, and 23-28 of the ’014 Patent are invalid as obvious by three prior art patents by Kawagoe, Onoda and Nishizawa three different grounds listed in the table below.

Ground	Legal Basis	Prior Art Reference(s)
I	Pre-AIA 35 U.S.C. § 103	Kawagoe
II	Pre-AIA 35 U.S.C. § 103	Onoda
III	Pre-AIA 35 U.S.C. § 103	Onoda and Nishizawa

II. OVERVIEW OF THE TECHNOLOGY

A. Priority Date of the Claims

21. I have been informed that a U.S. patent application may claim the benefit of the filing date of an earlier patent application if the earlier patent application disclosed each limitation of the invention claimed in the later-filed U.S. patent application. I have also been informed that priority is determined on a claim-by-claim basis so that certain claims of a patent may be entitled to the priority date of an earlier-filed patent application even if other claims of the same patent are not entitled to that priority date.

22. I have also been informed that a patented claim is invalid if the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention, or the claimed invention was described in an issued patent or a published patent application that was effectively filed before the effective filing date of the claimed invention.

23. All of the ’842, ’481, ’222 and ’014 Patents, along with the ‘502 Patent claim priority to U.S. Patent No. 8,421,195 (the “’195 Patent”), which further claims priority to September 3, 2004 the filing date of U.S. Patent Application No. 10/934,915 which was abandoned for failure to respond to an office action issued by the U.S. Patent and Trademark Office.

B. Overview of the ’842, ’481, ’222 and ’014 Patents

24. As an initial matter, the independent claims of the ’842, ’481, ’222 and ’014 Patents recite combinations that contain various identical or similar claim limitations. A table showing the claim language for each challenged claim of the ’842, ’481, ’222 and ’014 Patents, with highlighted substantive differences, is provided in **Appendix B**.

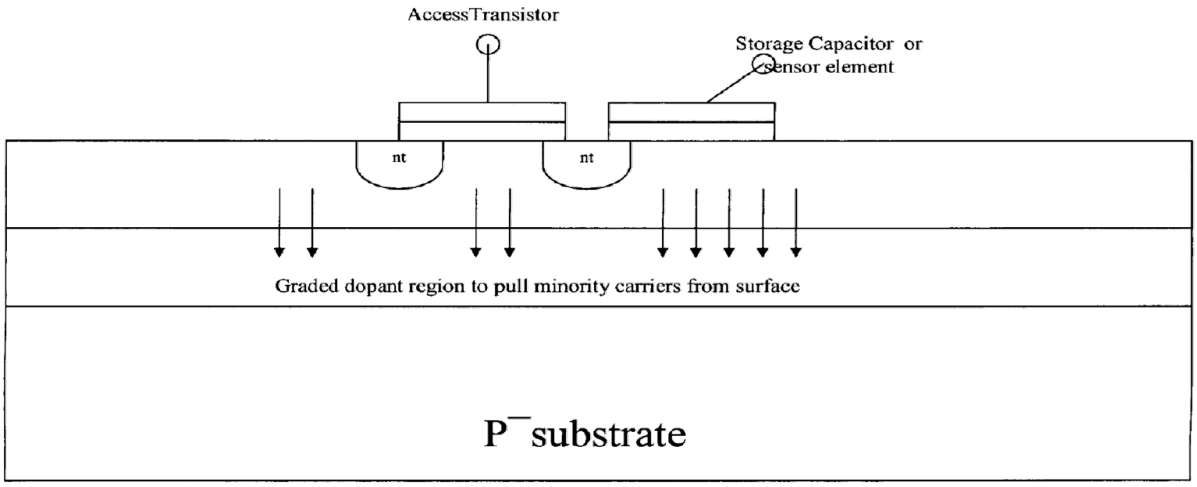
25. The ’842, ’481, ’222 and ’014 Patents contain similar patent specifications with identical drawings and substantially identical technical disclosures.

26. The ’842, ’481, ’222 and ’014 Patents describe and claim semiconductor devices that include first and second active regions with at least a portion of at least one active region having at least one graded dopant concentration to aid carrier movement from the surface of the substrate adjacent to the active region into the device substrate. (’842 Patent at Abstract, 3:60-4:13 and 4:44-6:28; ’481 Patent at Abstract, 3:64-4:18 and 4:49-6:59; ’222 Patent at Abstract, 3:53-4:5, and 5:38-8:39; ’014 Patent at Abstract, 3:64-4:17 and 4:48-6:62.) The ’842, ’481, ’222 and ’014 Patents state that the doping profile is graded, to enable an electric drift field “to sweep unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible.” (‘842 Patent at 3:60-64; ‘481 Patent at 3:64-4:1; ‘222 Patent at 3:53-59; and ‘014 Patent at 3:64-4:1.)

27. The ’842, ’481, ’222 and ’014 Patents acknowledge that graded doping profiles or graded dopant concentrations were used in the past. They state that some prior art bipolar junction transistors employed a graded dopant base to create an “‘aiding drift field’ to enhance the diffusing minority carrier’s speed from emitter to collector.” (’842 Patent at 1:55-57; ’481 Patent at 1:59-61; ’222 Patent at 1:46-

48; ’014 Patent at 1:62-64.) The ’842, ’481, ’222 and ’014 Patents state that this had deficiencies because “most semiconductor devices … still use a uniformly doped drift epitaxial region in the base.” (’842 Patent at 1:55-62; ’481 Patent at 1:59-66; ’222 Patent at 1:46-53; ’014 Patent at 1:62-2:2.)

28. The ’842, ’481, ’222 and ’014 Patents state that these purported problems of the prior art could be improved by having active regions (and/or well regions) with graded dopant concentration. (’842 Patent at 3:12-30; *see also id.* at 3:60-4:13; ’481 Patent at 3:16-33 and 3:64-4:18; ’222 Patent at 3:4-35 and 3:53-4:5; ’014 Patent at 3:16-34 and 3:64-4:17.) This would carry minority carriers from the surface into the substrate (indicated by arrows in FIG. 5(b). (*Id.*)



(’842, ’481, ’222 and ’014 Patents at FIG. 5(b).)

29. In my opinion, doping profiles with a gradient (*i.e.*, non-uniform) were well known and documented in publications at the time of the purported inventions.

It was common in the industry, and widely employed via common techniques. For example, the process for using thermally diffusing dopants was a common technique in semiconductor formation, and it provided for a graded dopant profile in the semiconductor layers by the nature of the process. A dopant would be introduced to the surface, and thereafter thermally diffused. There would be a greater concentration at the surface and then a downward gradient where the concentration disperses away from the surface.

30. Based on my analyses of prior art references in this Declaration, the "novel technique" of using a graded dopant concentration profile to create an electric drift field to sweep unwanted minority carriers from the active circuitry at the substrate surface into the substrate as proclaimed in the '842, '481, '222 and '014 Patents was a well-known concept and was already documented in the literature before those patents' earliest priority date of September 3, 2004. Doping in the art was widely known to be done in order to create various layers where various regions are doped to be n or p type, along with associated drain and source regions, to create p-channel metal–oxide–semiconductor ("PMOS") transistors or n-channel metal–oxide–semiconductor ("NMOS") transistors. This is fundamental to forming transistors.

31. It was also well known to use doping gradients or graded dopant concentrations to control electric fields and to move minority carriers before September 3, 2004. Indeed, the '842, '481, '222 and '014 Patents state doping gradients at the emitter (decreasing as a function of distance) and collector (increasing upward) as part of prior art. ('842 Patent at 1:55-57 and FIG. 1; '481 Patent at 1:59-61 and FIG. 1; '222 Patent at 1:46-48 and FIG. 1; '014 Patent at 1:62-64 and FIG. 1.) In my opinion, the '842, '481, '222 and '014 Patents contain statements acknowledging the well-known nature of various doping profiles by merely listing them by name (*e.g.*, "linear, quasi linear, exponential") rather than fully describing them or disclosing how to obtain them. ('842 Patent at 3:1-2; '481 Patent at 3:5-6; '222 Patent at 2:60-62; '014 Patent at 3:5-6.) I consider the first two profiles (*i.e.*, "linear" and "quasi linear") to have a change in concentration no more than a factor of ten; they are usually displayed on a linear-linear plot. An exponential profile has a change in concentration more than a factor of ten and is usually displayed on a log-linear plot. Gaussian and error function curves are examples of exponential profiles.

32. The '842, '481, '222 and '014 Patents also do not disclose any new or novel layer to which those known doping techniques were to be applied. The layers described are routine and known layers in routine and well-known semiconductor

devices, and this is confirmed by the ’842, ’481, ’222 and ’014 Patents in describing various known semiconductor layers and devices when describing the prior art. (’842 Patent at 1:55-57 and FIG. 1; ’481 Patent at 1:59-61 and FIG. 1; ’222 Patent at 1:46-48 and FIG. 1; ’014 Patent at 1:62-64 and FIG. 1.)

C. Overview of the Technical Concepts

33. My analysis will primarily rely on prior art patents Onoda, Nishizawa, and Kawagoe to show that the claims of the ’842, ’481, ’222 and ’014 Patents recite technical subject matter that was disclosed in Onoda, Nishizawa, and Kawagoe and thus are invalid. All three prior art patents deal with the same technical challenge as the patents being challenged: how to protect electronic circuits from impacts of high energy photons such as x-rays or high energy particles such as alpha rays. When a high-energy collision takes place in a semiconductor, it creates a very large number of negatively charged electrons and positively charged holes. The dopants with additional electrons are donors of negatively charged electrons and are used for n-type doping; and the dopants with additional positively charged holes are acceptors of electrons and are used for p-type doping. Of particular interest are the minority carriers such as electrons in a p-type doped region or as holes in an n-type doped region. In an NMOS transistor or memory cell formed in a p-type doped region, if enough of the minority charge carrier electrons are collected by the circuitry on the

surface of the semiconductor, they can introduce faults in the circuit. As will be discussed, these charged species move in response to an electric field, and so an electric field that is properly constructed will push the minority carriers away from the surface, making their collection much less probable. I will also point out that it was well known that an electric field caused by a doping profile can improve the performance of photosensing devices (patents from Jastrzebski and from Kamins) by drifting minority carriers into the substrate.

34. Onoda, Nishizawa, and Kawagoe disclose reducing undesired latch-up, punch-through, and/or soft errors to motivate the need for the innovations described in those prior art patents. To explain the latch-up, consider a CMOS inverter which is a widely used circuit that includes one NMOS transistor formed in a p-doped region and one PMOS transistor formed in an adjacent n-doped region of the same substrate. Parasitic bipolar transistors are automatically formed in the active region of the CMOS inverter. These bipolar transistors are inevitably connected so as to create a latch. Once triggered, the latch remains in the state it enters until the circuit forces a change or until the circuit is powered down. The minority carriers, which are electrons in the p-doped region that supports one or more NMOS transistors, and are holes in the n-doped region that supports one or more PMOS transistors, are respectively collected by the active regions of the NMOS and PMOS transistors of

the circuitry and such minority carriers can provide the trigger to start the latch-up process. The punch-through effect is caused by the merger or overlap of the depletion regions of the source and drain of a transistor, which leads to an undesirable conductive path between the source and the drain. The collection of minority carriers in the active region of the transistor enhances this undesirable conductive path between the source and the drain. Soft errors in a memory cell occur when the circuitry collects enough of the minority carriers to change the voltage of that part of the circuit to the point where it produces an incorrect datum. Thus, a logical "1" becomes a logical "0", or vice versa. It is a "soft" error in the sense that the memory cell circuitry is not damaged, only the stored information is corrupted.

35. While the exact faults identified in the cited prior art patents vary from patent to patent, the source of the faults (the collection of excess minority carriers) and the proposed solution in the prior art patents are nearly identical: using a graded dopant concentration to produce a static electric field that will drift excess minority carriers away from the active regions at or near the surface of the semiconductor device and to the substrate.

36. Further, when discussing the applications disclosed in the prior art, whether an application merely discloses memory or logic circuitry is of no consequence to my analysis of the alleged invention. Very large scale and ultra

large-scale integrated circuits (VLSI and ULSI) are often categorized by their end use. A common categorization for digital chips is: logic for a chip that primarily contains logical operations and memory for a chip that primarily allows the user to store and read information. While this distinction is often used by general public, a POSITA understands that the distinction is somewhat arbitrary.

37. Indeed, textbooks analogize integrated circuit manufacturing to a "versatile" manufacturing line that "can make any circuit of that type simply by changing a few basic tools called masks." Modern VLSI Design, Wayne Wolfe, Prentice Hall, 2002.[1] For example, processor chips are something of a hybrid as performance goals invariably require a large amount of memory on the same chip as extensive logical processing. Furthermore, memory chips usually require logic circuitry to address the memory bits to read and write information, to decode the information, and to send the information off-chip. Thus, memory chips are generally built using logic technology. Additional processes may be required for specific memory types such as Flash memory, static random-access memory ("SRAM"), and dynamic random access memory ("DRAM"). In practical chip applications, logic

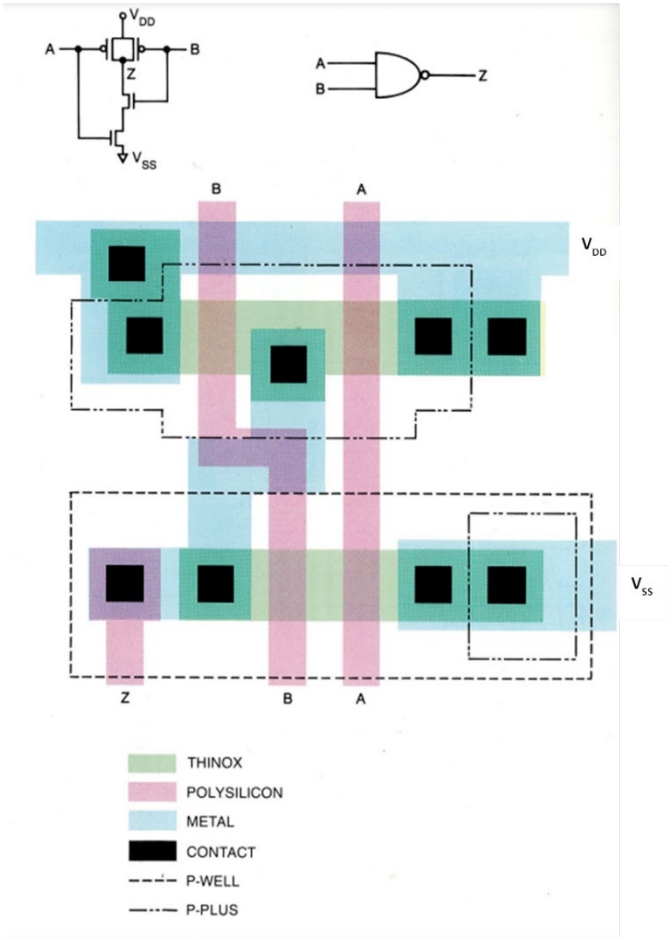
[1] Exhibit 1088 ("Wayne Wolfe").

elements of the chips are simply masked off from those added process steps. Thus, it makes sense that both Kawagoe and Nishizawa explicitly state their techniques are applicable for both memory and logic circuitry. (Nishizawa at 1:26-29 ("Also the invention concerns such semiconductor devices serving as a semiconductor memory and a logic circuitry."); Kawagoe at 24:21-31 (disclosing the techniques are applicable to memory and logic circuitry).)

38. The use of multiple transistors in a single well was obvious to a POSITA with any exposure to CMOS circuit design before September 2004, the potentially earliest priority of the challenged patent claims of the '842, '481, '222 and '014 Patents. One of the primary goals for the circuit designer is to minimize the area required to implement the desired function, be it memory or logic. The formation of a well requires space that cannot be used for circuitry. This includes the lateral diffusion of the well dopant and the need to have ohmic contacts made to the well so that the proper well voltage can be applied. As a result, it is standard practice to put multiple transistors in a single well, thereby spreading the overhead space needed for the well among the transistors. This was standard practice when I started working in the CMOS industry in 1981 and has been so ever since.

39. The excerpted figure below shows a very simple CMOS layout from a textbook published almost two decades prior to the '842, '481, '222 and '014 Patents

by Greenthread. Note that designers typically do not look at the cross sections of transistors such as those used in other parts of this Declaration. Instead, they look at the surface of the device. In addition to the visually obvious structures like metal lines and gate electrodes, they also map out where the dopants are implanted. The upper left region of the figure shows the circuit design to be implemented. The transistors that have a small circle adjacent to the gate are PMOS devices and the transistors without such a circle are NMOS transistors. The upper right figure shows the corresponding logic element, a NAND gate. A and B are the two inputs and Z is the output in both figures.



Example of CMOS layout, Plate 4 from Weste and Eshraghian[2]

40. The large figure at the bottom shows the actual layout. The key for the various layers is shown below the design figure. The shapes labeled as "thin ox" are more commonly known as "active areas". These define the shape of the region containing the source, drain, and gate. This layout assumes an n-type substrate with

[2] Principles of CMOS VLSI Design: A Systems Perspective, Neil H. E. Weste and Kamran Eshraghian, Addison-Wesley Publishing, Reading PA 1985

a p-well. Two PMOS transistors are formed in the substrate and two NMOS transistors are formed in a single well. V_{DD} is the most positive power line and V_{SS} is the least positive power line. V_{SS} is typically ground in a CMOS circuit. Note that the two NMOS devices are connected in series. As shown here, this is often done by using the source of one transistor as the drain of the other. No contacts are needed at this node. While this type of gate is routinely used to implement logic, NAND-like designs are also commonly used in flash memories as well. From this figure, published years before September 2004, it is clear that placing multiple transistors in a single well has been the most common way to design CMOS circuits long prior to the '842, '481, '222 and '014 Patents.

41. Further, figure 6-31 in Wayne Wolfe, annotated and reproduced below, shows an example of a six-transistor SRAM cell, from 2002.[3] Once again I note that designers typically do not look at the cross sections that I have used in other parts of this Declaration. Instead, they look at the top of the cell or chip.

[3] Wayne Wolfe at 346.

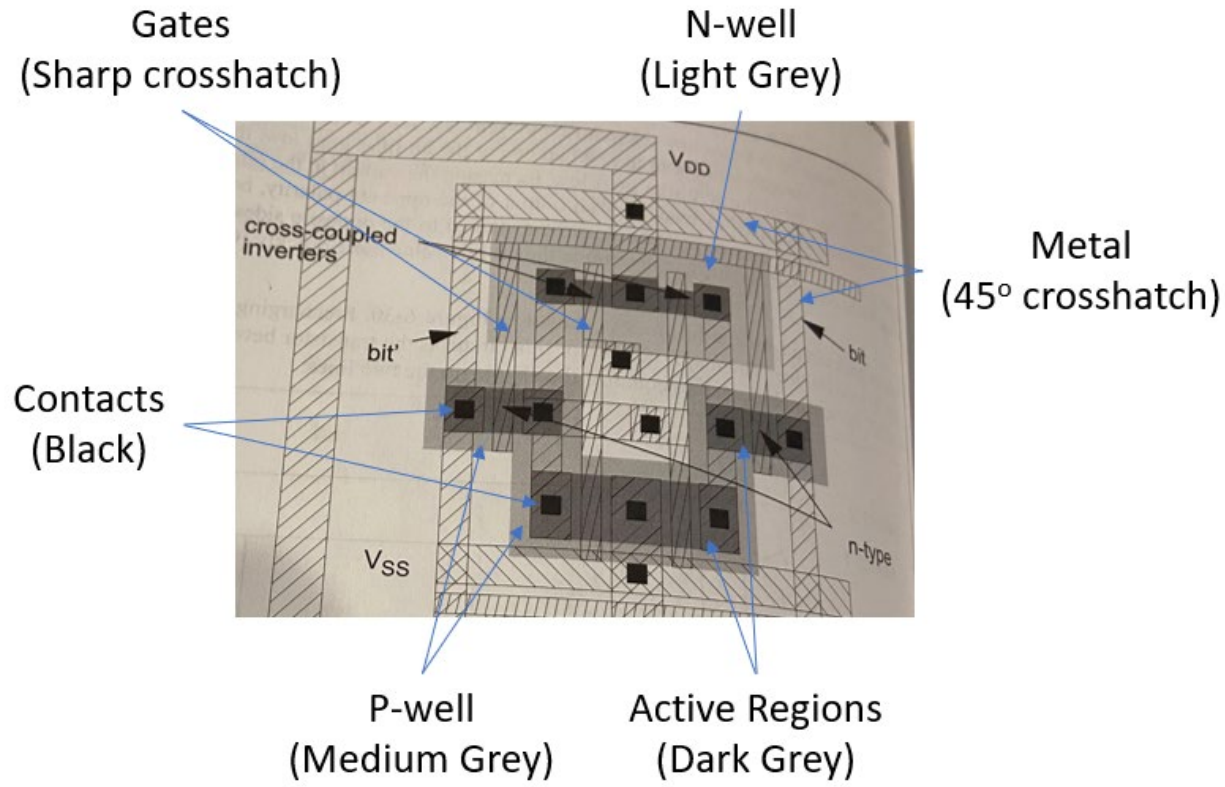


Figure 6-31 in Wayne Wolfe (Annotated)

42. In addition to the visually obvious structures like metal lines and gate electrodes, designers also map out where the dopants have been implanted. I have annotated the figure to indicate the various regions. Transistors can be easily recognized as having a gate electrode, flanked by contacts to make connections to the source and drain.

43. I have included below my annotated Figure 6-31 in Wayne Wolfe to show a closeup version of the illustrated semiconductor device indicating the

transistor components for the two PMOS transistors 1 and 2 in the same N-well at the top of the cell. The sources and the common drain are both in the same N-well.

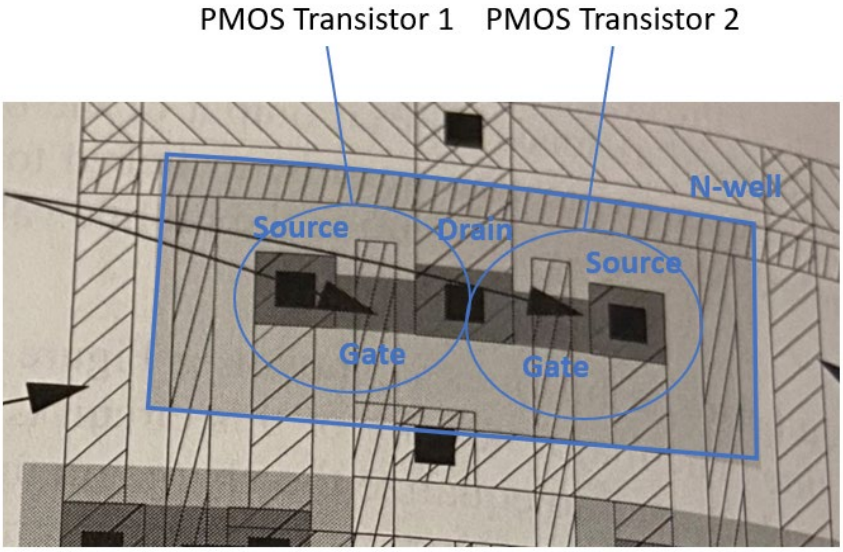


Figure 6-31 in Wayne Wolfe (Closeup & Annotated)

44. Figure Y1 in Wayne Wolfe[4] is reproduced below to show the layout of a logic function using the same layer designations.[5] The layout has two parts – the large block at the bottom and the smaller block in the upper left. Note that both of

[4] Wayne Wolfe at 287.

[5] Although the design is considerably more complex than that shown above, the point of this discussion is only to show that it was well known prior to September 2004 to fabricate integrated circuits having multiple transistors in a single well.

these blocks are separated into the top and bottom halves by the shading of the wells. The top set of blocks are NMOS transistors formed within a P-well and the bottom set of blocks are PMOS transistors formed within an N-well. These are the wells with multiple transistors in each well.

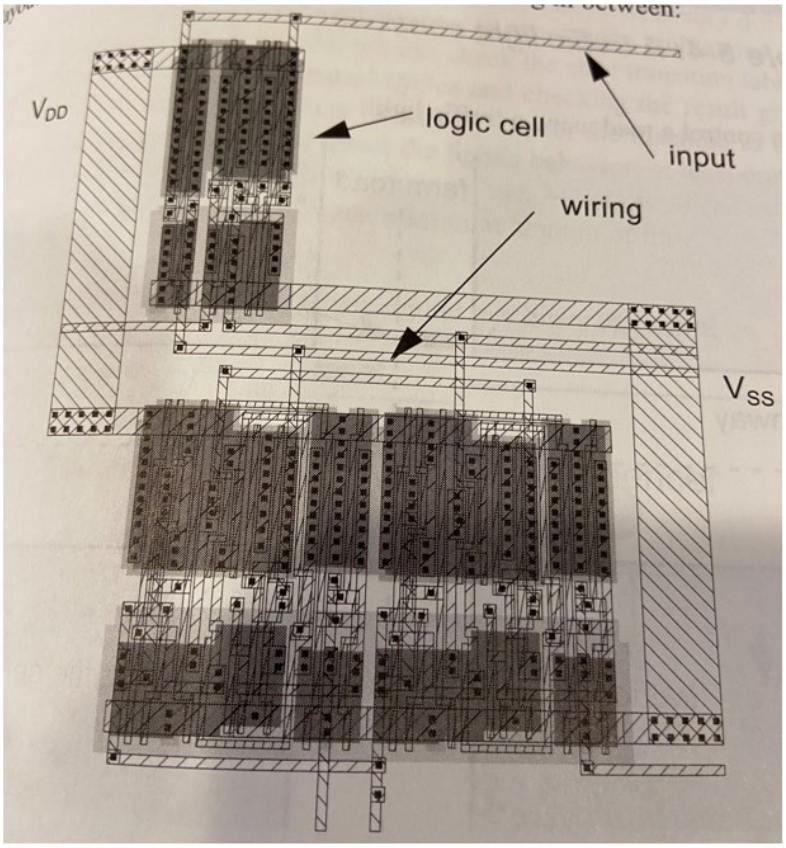


Figure Y1 Showing Two Rows of CMOS Gates

45. To make this more discernable, the next figure shows a closeup version of just the upper left corner of the circuitry. This figure illustrates formation of four PMOS transistors in a single N-well. Thus, placing multiple transistors in a single well has been a common – indeed, the most common – way to design CMOS circuits

since well before the September 2004 priority date of the ’842, ’481, ’222, and ’014 Patents.

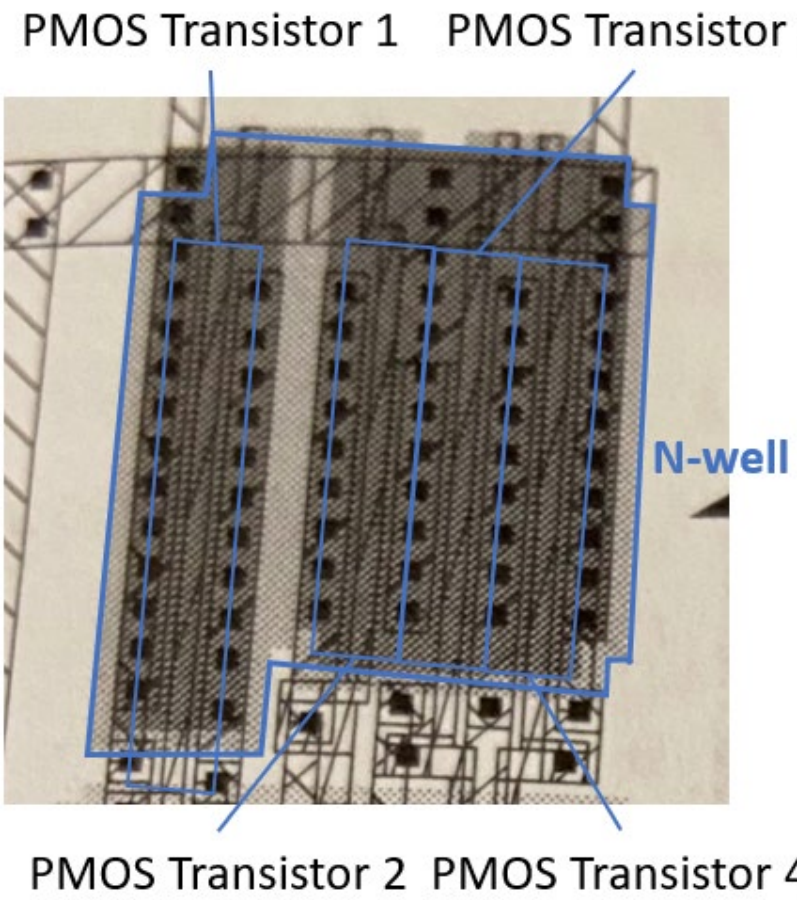


Figure Y2 N-Wells containing multiple PMOS Devices (Closeup & Annotated)

D. Static Unidirectional Electric Drift Fields

46. The ’842, ’481, ’222 and ’014 Patents state that a graded doping concentration sweeps minority carriers into the substrate. (’842 Patent at 3:60-66; ’481 Patent 3:64-4:3; ’222 Patent at 3:53-58; ’014 Patent 3:64-4:3 (“Hence, a novel technique has been described here by creating a drift field to sweep these

unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate.”))

47. In my opinion, Patent Owner represented to the U.S. Patent and Trademark Office that a graded dopant concentration creates, as an inherent physical property, a static unidirectional electric drift field. Patent Owner argued this in the ’195 Patent prosecution, and the ’842, ’481, ’222, and ’014 Patents claim priority to that application. In arguing that the specification of the ’195 Patent provided written description support for the claimed “static unidirectional electric drift field,” the Patent Owner represented that:

> “[T]he graded dopant concentration itself creates a ‘built-in’ electrical field that forces the movement of carriers into a particular direction, whereby the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.”

(’195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 7.)

48. Patent Owner further represented that:

> “a unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way… Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept ‘down’ … or ‘up…’”

('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 6-7.)

49. Patent Owner referenced U.S. Pat. No. 4,481,522 ("Jastrzebski") in support. ('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 7.) Patent Owner stated that:

> "With regard to the existence of a "built-in" electric field created by a graded dopant density, see, e.g., Jastrzebski (US 4,481,522) col. 5, lines 11-13 (cited in Office Action). Applicant respectfully submits that this inherent "built-in" unidirectional electric field is the additional parameter for ensuring that all minority carriers are being moved in one direction and which parameter the Office Action deemed to be missing from the disclosure."

(Jastrzebski at FIGS. 1a, 1b.)

50. Jastrzebski confirms that this inherent physical property does result from a graded dopant. It states that a downward-sloping graded-dopant concentration creates an electric drift field that "force[s] most of the charge carriers … deep into the substrate[.]" (Jastrzebski at 5:14-22; *id.* at 2:27-32 ("This is done by creating a field, such as a drift field, in the semiconductor substrate to sweep minority charge carriers…into the bulk [substrate], away from the electrode-bearing surface of the substrate.").).

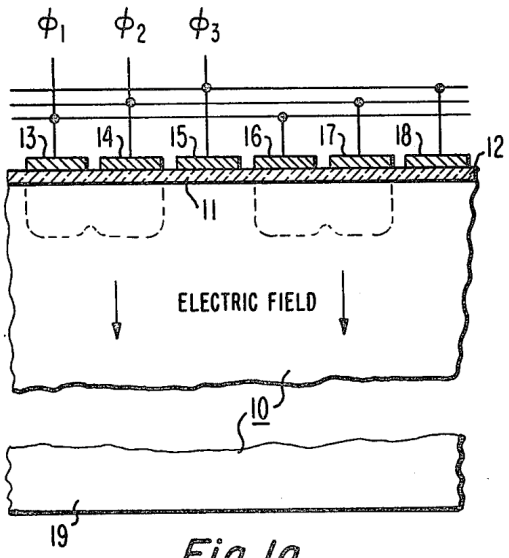


Fig. 1a

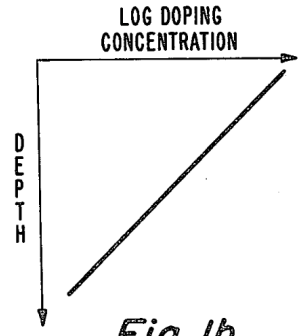


Fig. 1b

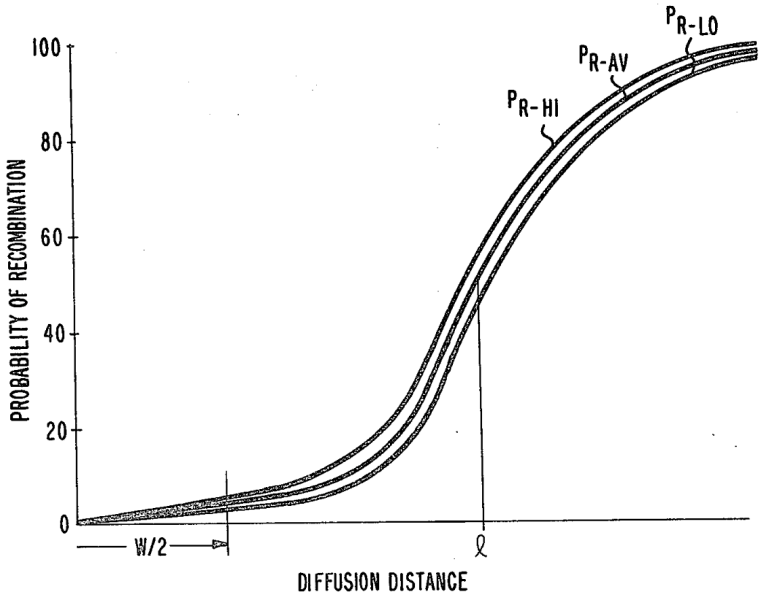


Fig. 2

51. Jastrzebski at 5:5-24 discloses:

> These background striation and cross-talk problems are surmounted by constructing CCD shift registers, as exemplified by the FIG. 1a structural segment, in accordance with the present

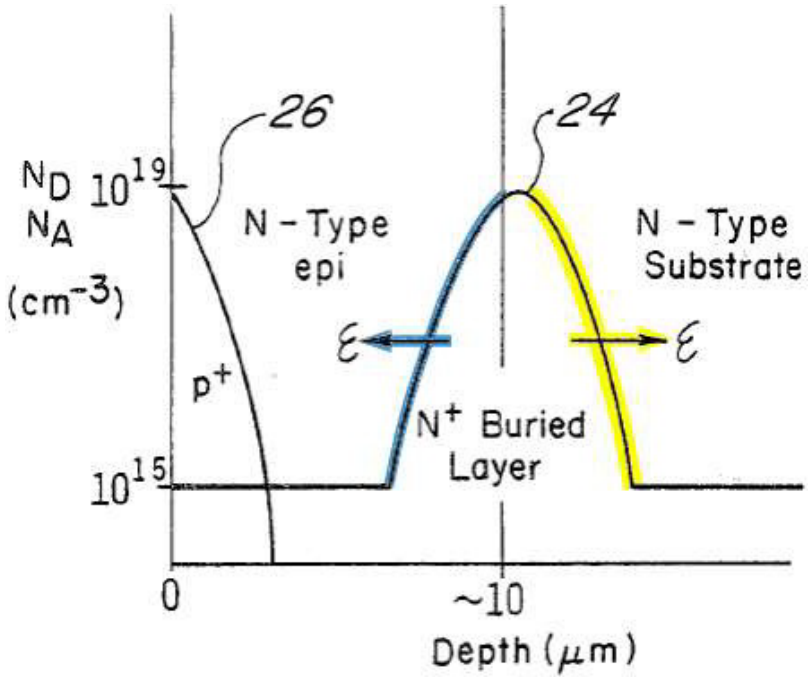
> invention, so that there is an electric field normal to the surface 11 that tends to force carriers deeper into the bulk away from the depletion regions induced adjacent to surface 11. This electric field can be a drift field created by a graded concentration of doping in the substrate. In the FIG. 1a structural segment the gradient of doping concentration would be normal, or perpendicular, to the surface 11 of substrate 10, with the doping concentration decreasing with depth from surface 11. The drift field is accordingly directed to force most of the charge carriers generated outside a depletion region deep into the substrate 10 bulk. In these portions of the bulk remote from surface 11 of substrate 10 the charge carriers recombine. Arrangements can also be made to place deep drain structures to dispose of the charge carriers driven into these remote portions of the bulk.

52. Patent Owner made the same representation to the Patent Office regarding U.S. Pat. No. 4,160,985 ("Kamins"). ('195 Patent App., App. No. 11/622,496, Apr. 17, 2012 Amendment at 7.). Patent Owner stated:

> Kamins discloses a photosensing device in which selective doping of a semiconductor substrate of the device produces electric fields in the substrate which accelerate photo generated charge carriers toward or away from the surface of the device. Abstract, Fig. 3.

53. According to Patent Owner, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to

increasing and decreasing graded-dopant concentrations, respectively. (*Id.* at 237, 253 (citing Kamins at 3:6-13, FIGS. 2-3).)



(Kamins at FIG. 3.)

54. Patent Owner argued that:

> In particular, Kamins' disclosure further states that "[t]he carriers therefore tend to be accelerated either toward the nearest photosensor or away from the surface. More specifically, carriers created below the maximum dopant concentration are accelerated into the substrate [...], while carriers created above the maximum dopant concentration are accelerated toward the surface [...]." Col. 3, Lines 6-13, Fig. 2 (showing minority carries accelerated into the substrate and the surface layer, depending on the location of the carriers relative to the maximum dopant concentration

within the “buried layer” 21) and Fig. 3 (showing two electrical fields with opposing directions, away from the area of maximum dopant concentration towards both the surface layer and the substrate, respectively).

55. Kamins at 2:64-3:18 teaches that a graded dopant concentration creates electric fields:

> FIG. 3 schematically illustrates profiles of doping concentration vs. depth into substrate 19. Curve 24 represents the N-type dopants, while curve 26 indicates the P+ -type doping for photosensors 11, 13 etc. The non-uniform dopant concentration in the substrate creates electric fields in the substrate, indicated by arrows labeled "ε" in FIGS. 2 and 3. In devices fabricated as described above, the electric field in the substrate is about 460 V/cm near the surface, decreasing to 60 V/cm at 1 μm above the maximum dopant concentration. The carriers therefore tend to be accelerated either toward the nearest photosensor or away from the surface. More specifically, carriers created below the maximum dopant concentration are accelerated into the substrate where they recombine without contributing to the collected current of any sensor, while carriers created above the maximum dopant concentration are accelerated toward the surface where they increase the collected current of the adjacent photosensor. In either case, the probability of a carrier reaching a distant sensor is reduced. The field also leads to more rapid collection of

photogenerated carriers, thus improving the frequency response of the device.

56. FIG. 3 of Kamins depicts these two electric fields that are inherently created by a graded dopant concentration.

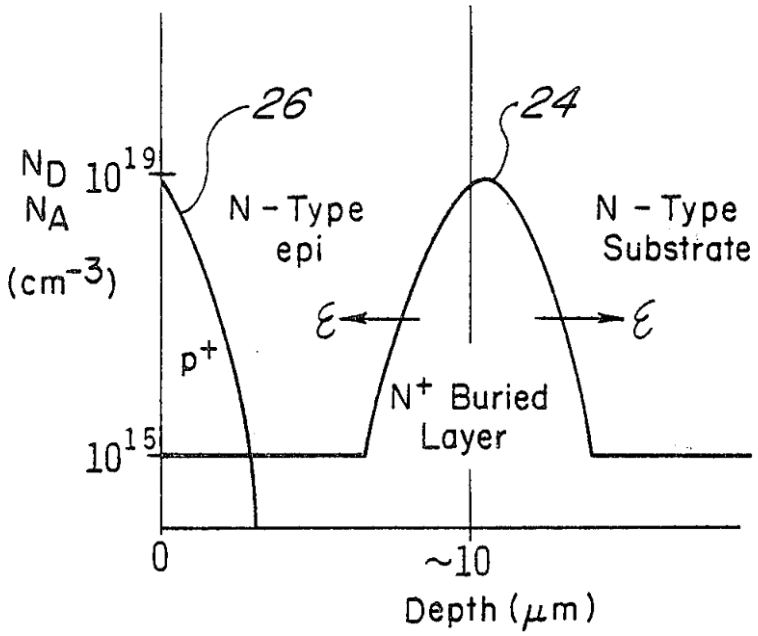


Figure 3

57. Kamins depicts the minority carriers in FIG. 2, stating that it provides "built-in electric fields into the structure so that a directional drift motion is superposed on the random thermal diffusion of the charge carriers." (Kamins at 2:32-36.)

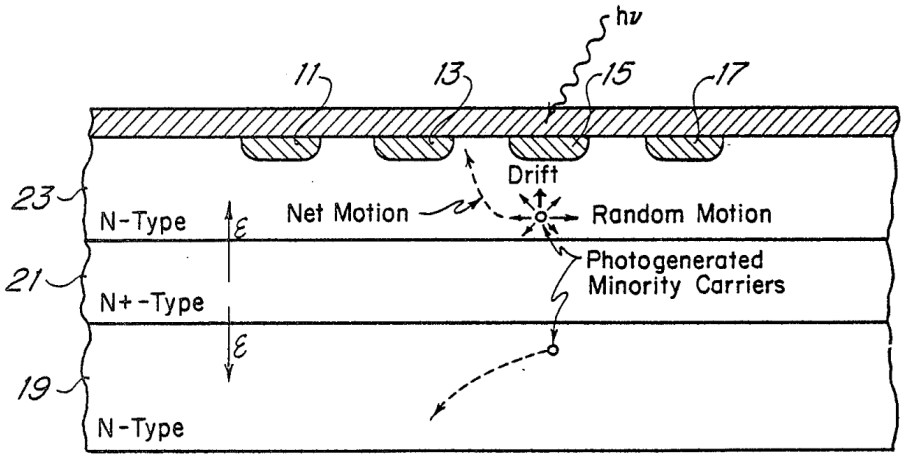


Figure 2

58. Patent Owner also described "static" with respect to Kamins and represented that it "discloses the presence of a 'static' drift field, 'because the drift field is created by graded concentration of dopants which does not change over time.'" ('195 Patent App., App. No. 11/622,496, Oct. 15, 2015 Amendment at 6 (citing Office Action ¶ 4 p.4 lines 1-3, further citing to Kamins, Col. 2, lines 15-16; Col. 2, line 64- Col. 3, line 2; Col. 1, lines 38-46; and Col. 3, lines 8-11.).

E. Claim Construction

59. I understand that claim terms generally are construed in accordance with the ordinary and customary meaning they would have to a POSITA at the time of the invention in light of the claim language, the specification, and the prosecution

history. I understand that dictionaries and other extrinsic evidence may be considered as well, though such evidence is typically regarded as less significant than the intrinsic record in determining the meaning of the claim language.

60. For all terms of the challenged claims of the '842, '481, '222 and '014 Patents, I have interpreted them as they would have been understood by a POSITA at the time of the asserted priority date, *i.e.*, Sept. 3, 2004.

III. UNPATENTABILITY OF THE '842, '481, '222, AND '014 PATENT CLAIMS

A. Standards for Invalidity

1. Obviousness

61. I am informed and understand that a patent cannot be properly granted for subject matter that would have been obvious to a POSITA at the time of the alleged invention, and that a patent claim directed to such obvious subject matter is invalid under 35 U.S.C. § 103. It is also my understanding that in assessing the obviousness of claimed subject matter, one should evaluate obviousness in light of the prior art from the perspective of a person having *ordinary* skill in the art at the time the alleged invention was made (and not from the perspective of either a layman or a genius in that art). It is my further understanding that the question of obviousness is to be determined based on:

- The scope and content of the prior art;

- The difference or differences between the subject matter of the claim and the prior art (whereby in assessing the possibility of obviousness one should consider the manner in which a patentee and/or a Court has construed the scope of a claim);

- The level of ordinary skill in the art at the time of the alleged invention of the subject matter of the claim; and

- Any relevant objective factors (the "secondary indicia") indicating nonobviousness, including evidence of any of the following: commercial success of the products or methods covered by the patent claims; a long-felt need for the alleged invention; failed attempts by others to make the alleged invention; copying of the alleged invention by others in the field; unexpected results achieved by the alleged invention; praise of the alleged invention by the alleged infringer or others in the field; the taking of licenses under the patent by others and the nature of those licenses; expressions of surprise by experts and those skilled in the art at the subject matter of the claim; and whether the patentee proceeded contrary to accepted wisdom of the prior art.

- Any relevant objective factors (the "secondary indicia") indicating obviousness: independent invention of the claimed invention by others before or at about the same time as the named inventor thought of it; and other evidence tending to show obviousness.

62. Further, I understand that when combining references or modifying a reference, rationales that may support a conclusion of obviousness include: (a)

combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve similar devices (methods, or products) in the same way; (d) applying a known technique to a known device (method, or products) in the same way; (e) "obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; (f) known work in the field that may prompt variations of it for use in either the same field or different one based on design incentives, or other market forces; (g) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. When considering these rationales, one should be careful not to engage in hindsight analysis such that the reconstruction of the alleged invention is based on the knowledge gleaned from the patent disclosure itself. I have not engaged in hindsight analysis as the prior art references disclose the same problems, the same solutions, the same structures, the same inherent characteristics, and the same benefits that are disclosed and claimed in the '842, '481, '222 and '014 Patents. My detailed analyses of the '842, '481, '222 and '014 Patents below are organized in the following order : (1) Onoda under

Ground II; (2) the combination of Onoda and Nishizawa under Ground III; and (3) Kawagoe under Ground I.

B. ’842 Patent

1. Ground II: Onoda Renders Obvious Claims 1, 2, 4-9, 12-18 of the ’842 Patent

a. Independent Claim 1 of the ’842 Patent

63. Onoda discloses a semiconductor device with a graded dopant concentration in one of adjacent first and second active regions to aid carrier movement from the first surface to the second surface of the substrate. FIG. 8 depicts a cross-sectional view of a semiconductor substrate 100 where the dopant concentration gradually decreases from the top of the doped epitaxial second semiconductor layer 102 (aqua), through the well region 105a (green) and into the doped first semiconductor layer 101 (pink) along the direction indicated by the B-B’ line (yellow and dashed-red). (Onoda at [0046]-[0047], [0052].) Only a singular well region (105a) has been annotated, but Onoda discloses other well regions, *e.g.*, first well regions 103, second well regions (104a, 104b), third well regions (105a, 105b, 106c), and fourth well regions 106a, 106b, 106c. (Onoda at [0042]). These well regions are n and p types, and form NMOS and PMOS transistors.

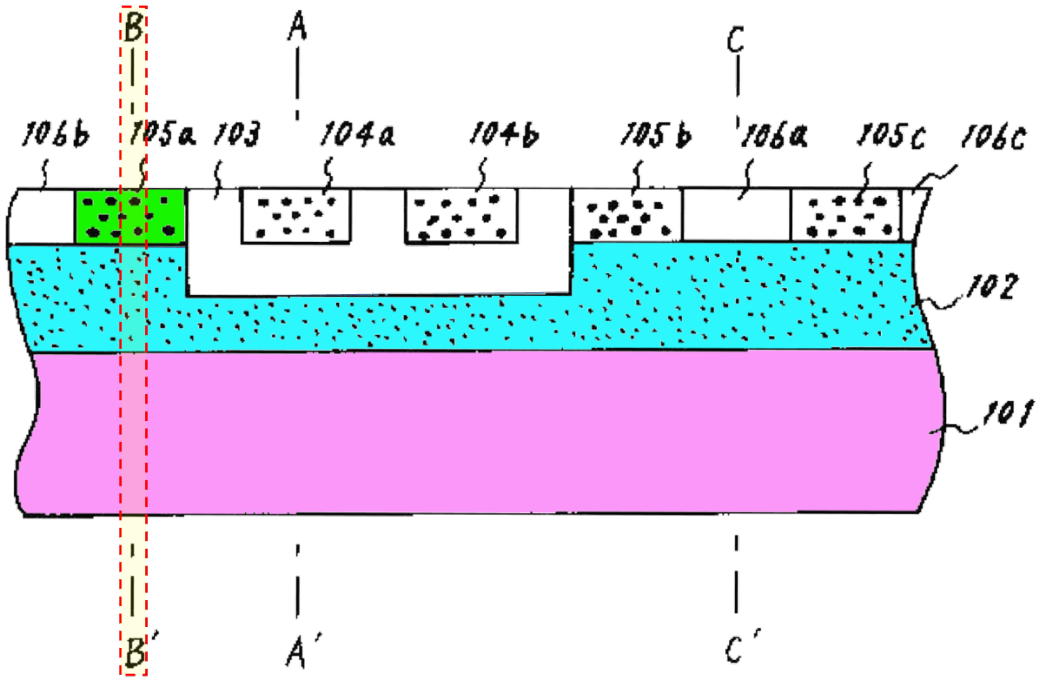


FIG. 8 of Onoda (Annotated)

64. The dopant concentration profile for p type dopants at different locations in different layers at different depths along the B-B' line (yellow) in FIG. 8 is shown in FIG. 11 below with corresponding colors, the well region 105a (green), the second semiconductor layer 102 (aqua) and the doped first semiconductor layer 101 (pink). The X-axis of FIG. 11 depicts the depth while the Y-axis depicts the dopant or impurity concentration. As can be seen in FIG. 11, Onoda discloses that the graded dopant or impurity concentration of p type dopants decreases from the top surface into the substrate 100 and this decrease continues through the second semiconductor layer 102 of the substrate 100.

65.

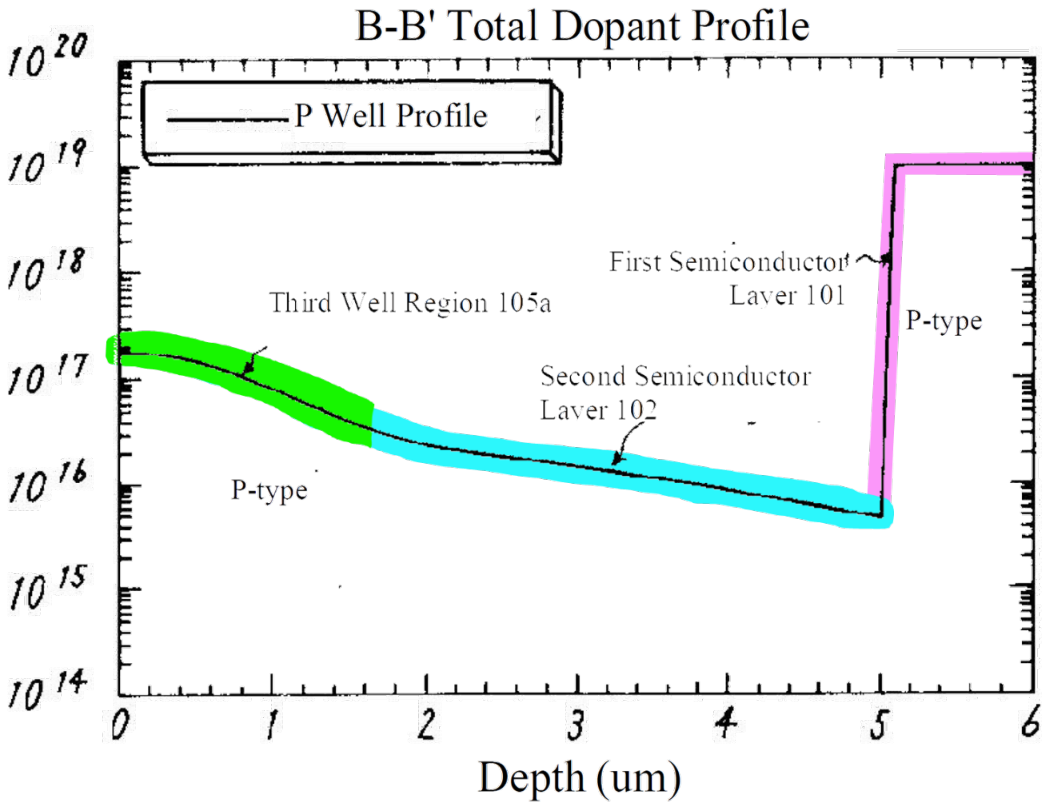


FIG. 11 of Onoda (Annotated)

66. For silicon substate 100 with first and second semiconductor layers 101 and 102 formed of silicon, boron may be used as P-type dopants to form p doped regions. Onoda at [0046]-[0053] and FIG. 7 (reproduced below). FIG. 7 in Onoda shows the structures of its memory device during the doping of boron and phosphorus for forming the p and n-wells. Examples in FIG. 7 Onoda include substrate 100 with first and second semiconductor layers 101 and 102 and boron doped P-type wells 105a, 105b, and 105c. Since the boron atom has 3 valence

electrons, one fewer than the 4 valence electrons in the silicon atom, a doped boron atom at a fixed location is bonded with 4 adjacent silicon atoms in the silicon crystal structure and behaves like a positively charged hole due to a missing electron at the boron site. This missing electron at the boron site bonded with 4 neighboring silicon atoms can attract (and thus be "filled" by) another free moving electron in the boron doped silicon. As a result, the additional electron attracted to, or filled in at, the site of the doped boron atom in the doped silicon turns the doped boron atom into a fixed negatively charged ion and the movement of a free moving electron to a doped boron atom is equivalent to the movement of a positively charged hole in the opposite direction of the additional electron. The doped boron atoms in the doped silicon contribute to P-type holes as the majority charge carriers and accordingly, the minority carriers in the boron doped silicon are free electrons. Therefore, doping of boron atoms in silicon creates a spatial distribution of fixed negatively charged boron ions in the P-type boron doped silicon.

[FIG. 7]

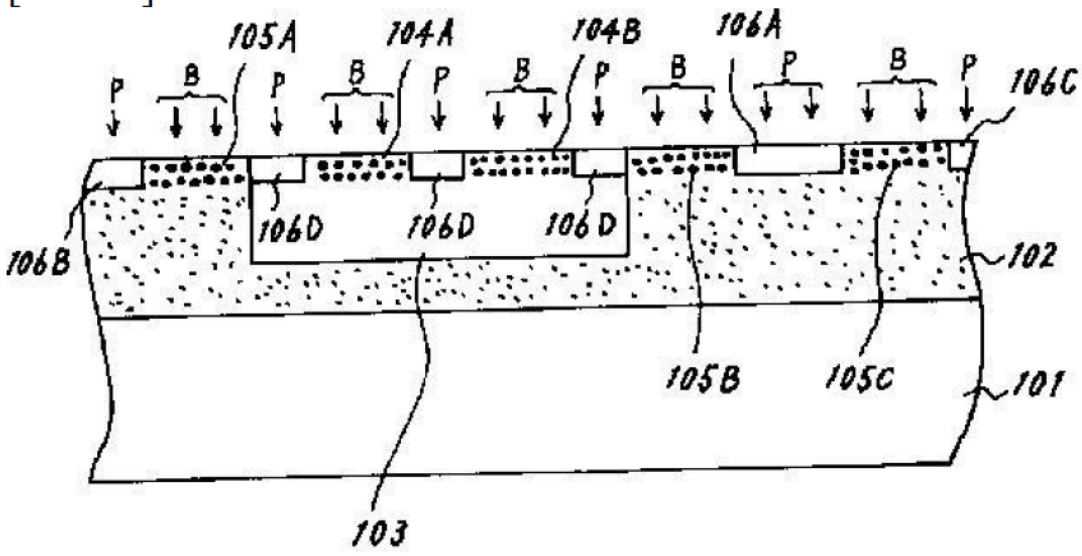


FIG. 7 of Onoda showing boron (B) is used to form p doped regions and phosphorus (P) is used to form n doped regions

67. Onoda also discloses using phosphorus as an N-type dopant to dope silicon based substate 100 with silicon first and second semiconductor layers 101 and 102, to form n doped regions. Onoda at [0046]-[0053]. Examples in Onoda include N-type wells 103, 106a, 106b, and 106c. Since the phosphorus atom has 5 valence electrons, one more than the 4 valence electrons in the silicon atom, a doped phosphorus atom at a fixed location is bonded with 4 adjacent silicon atoms in the silicon crystal structure such that there is an extra electron from the phosphorus atom

that is not bonded with the with 4 adjacent silicon atoms. This extra, unbonded electron becomes a free moving electron in the phosphorus doped silicon, and the loss of the extra electron by a doped phosphorus atom fixed in the doped silicon turns the doped phosphorus atom into a fixed positively charged ion. The dopant phosphorus atoms in the phosphorus doped silicon contribute their respective extra, unbonded electrons as the majority charge carriers and accordingly, the minority carriers in the phosphorus doped silicon are holes. Therefore, the doping of phosphorus atoms in silicon creates a spatial distribution of fixed positively charged phosphorus ions in the N-type phosphorus doped silicon.

68. As disclosed in Onoda, Nishizawa, and Kawagoe, it was well known that the electrical field associated with the gradient of N-type doping such as phosphorus in the silicon or P-type doping such as boron in silicon can be controlled by the dopant profile to impact the movement of the minority carriers.

69. In my opinion, Onoda discloses and/or renders obvious each of the elements of claims 1-2, 4-9, and 12-18 of the ’842 Patent. This is described below.

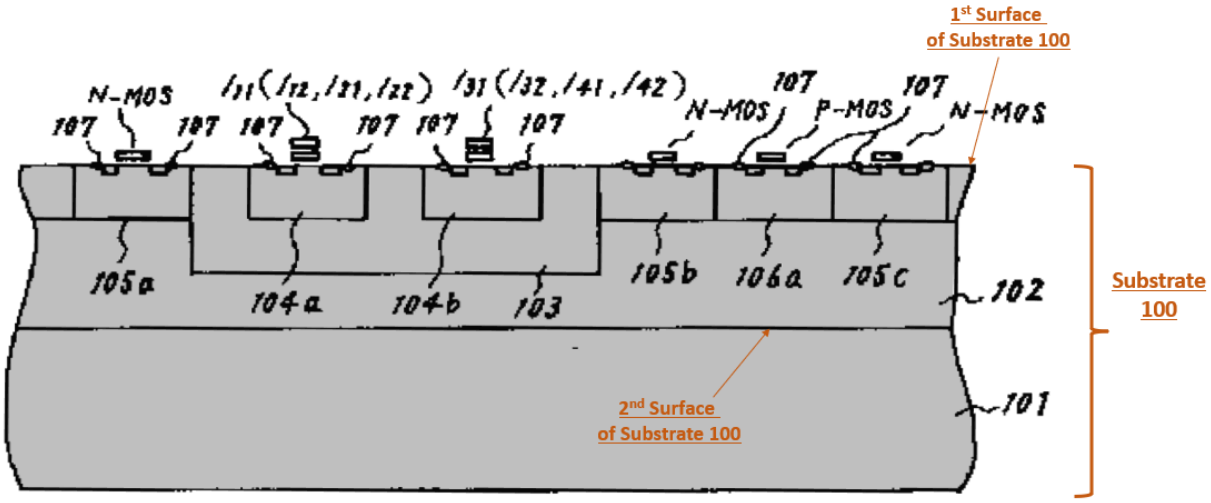
(i) Preamble: “A semiconductor device comprising:”

70. Onoda discloses semiconductor devices and semiconductor integrated circuit devices with various circuits and components, including PMOS and NMOS transistors and fabrication methods. (Onoda at Claims 1, 7 and 8-12; [0006], [0007],

[0012]-[0017].) Onoda discloses implementations of semiconductor integrated circuit devices in the form of semiconductor storage devices including "a nonvolatile semiconductor storage device with improved latch-up resistance and punch-through breakdown voltage." (Onoda at [Abstract], Claims 2-6, [0006], [0008]-[0011].) Thus, Onoda discloses a semiconductor device.

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

71. Onoda discloses a substrate of a first doping type at a first doping level having first and second surfaces in the form of the p-type semiconductor substrate 100 that includes a first semiconductor layer 101 and a second semiconductor layer 102 that is epitaxially grown and integrated to the first semiconductor layer 101. The substrate 100 is annotated in grey, along with the first and second surface identified, below.



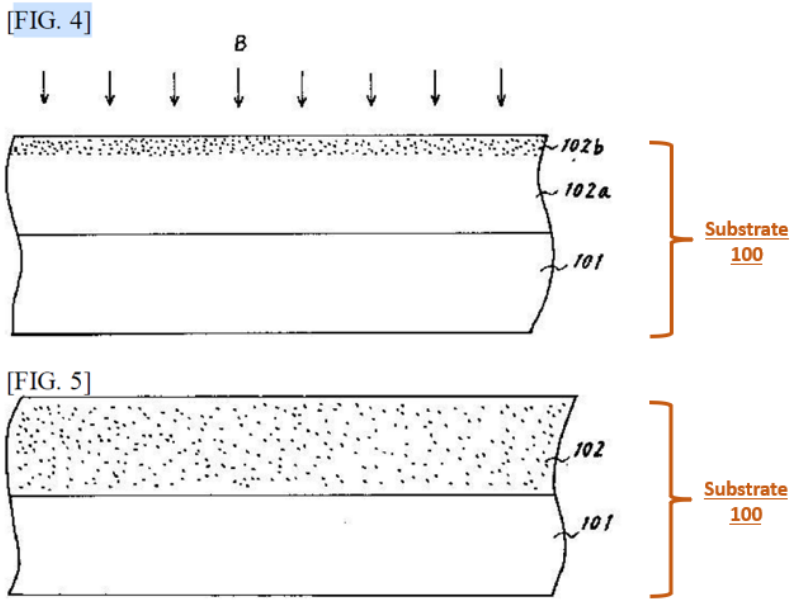
Substrate 100 in FIG. 3 of Onoda (Annotated)

(Onoda Annotated FIG. 3.)

72. Onoda's flash memory has "a semiconductor substrate 100." FIG. 3 depicts portions of the semiconductor substrate in the first embodiment disclosed by Onoda. (Onoda at [0040]-[0043]; *see also* at FIGS. 1, 2 and 3 (denoting "substrate 100" as encompassing first and second semiconductor layers 101 and 102).) As described by Onoda, the "flash memory … is formed on the semiconductor substrate that is … depicted in FIG. 3." (Onoda at [0043]; FIG. 3.)

73. FIG. 3 depicts the final device after well and active region formation, and Onoda discloses the formation of the substrate 100 (shown above) in FIGS. 4 and 5, which depict its doping levels as being p-type by using boron as the P-type

dopant. (Onoda at [0046]-[0047.) Semiconductor substrate 100 in Onoda is formed by "a first semiconductor layer made from a heavily-doped [] P-type silicon substrate" labeled as 101 and a P-type doped second semiconductor layer 102 on the top of the first semiconductor layer 101. (Onoda at [0041]; *see also id.* at "Brief Description of the Drawings" describing FIGS. 1 through 14 as describing features of the "first embodiment.") Both first and second semiconductor layers 101 and 102 of the substrate 100—prior to well and transistor formation—are depicted in FIGS. 4 and 5, reproduced below.



Formation of Substrate 100
FIGS. 4 and 5 of Onoda (Annotated)

74. The second semiconductor layer 102 is epitaxially grown silicon on the silicon first semiconductor 101 so that the epitaxial layer 102 and the silicon first

semiconductor layer 101 constitute an epitaxially integrated single substrate structure 100 with the same single crystal silicon structure and the same P-type doping by using boron. (Onoda at [0041] ("101 is a first semiconductor layer made from a heavily-doped (for example, about 1 x $10^{19}/cm^3$) P-type silicon substrate, and 102 is a P-type second semiconductor layer having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer 101 (for example 1 x $10^{15}/cm^3$, and may be between 1 x$10^{15}/cm^3$ and 1 x 10^{18}), deposited through epitaxial deposition to a thickness of between 1 and 10 μm onto the surface of the first semiconductor layer.") and [0046]-[0047].) This epitaxially integrated silicon substrate 100 with the silicon first semiconductor layer 101 and epitaxial silicon second semiconductor layer 102 discloses the claimed "substrate" because both first and second semiconductor layers 101 and 102 of the substrate 100 in Onoda are P-type doped.

75. The specific doping levels in the above referenced sections in Onoda disclose the claimed "first doping type at a first doping level." As further explained below, Onoda discloses a graded dopant concentration with a spatially varying dopant concentration at different depths of a semiconductor device such as different depths of an active region or a well region formed in the semicodncutor device.

76. Onoda's teaching of the "substrate" matches Patent Owner's proposed claim construction in district court, where Patent Owner stated the term "substrate" should be construed to mean "an underlying layer." (*Greenthread, LLC v. Intel Corp.*, 6:22-cv-105-ADA, PO Res. Br. at 15-16 (citing the '195 Patent at 2:18-23, 27-28 ("a MOS silicon substrate with two wells, and an underlying layer").) Patent Owner also stated that "'substrate' is a relative term, and Dr. Rao (the named inventor on the '842, '481, '222 and '014 Patents), sometimes used it to refer to the bottom layer, and at other times he used it to refer to the wells that are underneath the surface layer and active region." (*Id.* at 6, fn. 6.) Furthermore, according to Patent Owner, "the claim never says the well region and drift layer cannot be part of the substrate" and "[i]n fact, the specification says the opposite when it specifically mentions a 'MOS silicon substrate with two wells, and the underlying layer.'" (*Id.* at 17 ("In this scenario, the two wells and underlying layer can all be part of the substrate.").) Thus, Onoda's substrate 100, which has the well regions (e.g., phosphorus doped N-type wells 103, 106a, 106b, and 106c and boron doped P-type wells 105a, 105b, and 105c) as part of the substrate 100, satisfies Patent Owner's expressly stated understanding of the term "substrate."

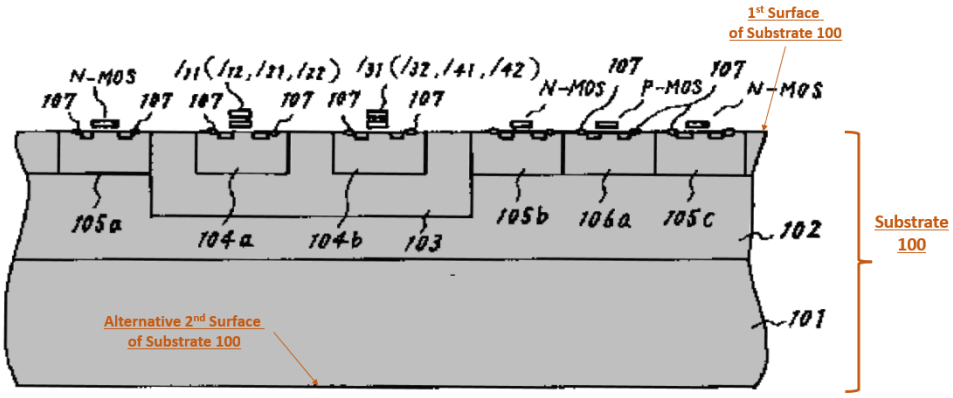
77. Onoda's teaching of the term "a substrate of a first doping type" also matches Patent Owner's agreed upon construction in district court where the term

was construed as "a substrate with either p-type doping or n-type doping." (PO Res. Br. at viii.) Substrate layers 101 and 102 have a p-type doping and satisfy this limitation.

78. The well regions in Onoda are formed in the second semiconductor layer 102 of the substrate 100, such as phosphorus doped N-type wells 103, 106a, 106b, and 106c and boron doped P-type wells 105a, 105b, and 105c. As disclosed in Onoda, the top parts of the well regions are used to support transistor active regions and memory cells. Accordingly, P-type doped substrate 100 discloses the claimed "first and second surfaces" as depicted in the above annotated FIG. 3: the claimed first surface as the top surface of the second semiconductor layer 102 of the substrate 100 and the claimed second surface as the bottom surface of the second semiconductor layer 102 of the substrate 100. Under this mapping of the claimed first and second surfaces of the substrate to Onoda's device in FIG. 3, the substrate region within the first semiconductor layer 101 does not contain well regions for supporting transistors and memory cells.

79. Alternatively, the claimed second surface of the substrate may be mapped to the bottom surface of the first semiconductor layer 101 of the substrate 100 in Onoda. This alternative mapping is illustrated in the below annotated FIG. 3 of Onoda. See my more detailed analyses and explanations below with respect to

Claim Element [1.5] of Claim 1 of the '842 Patent. My analysis of all claims in the four patents in this declaration remains the same for the above two mappings of the disclosure of surfaces of the substrate 100 in Onoda to the claimed "second surface" of the substrate.



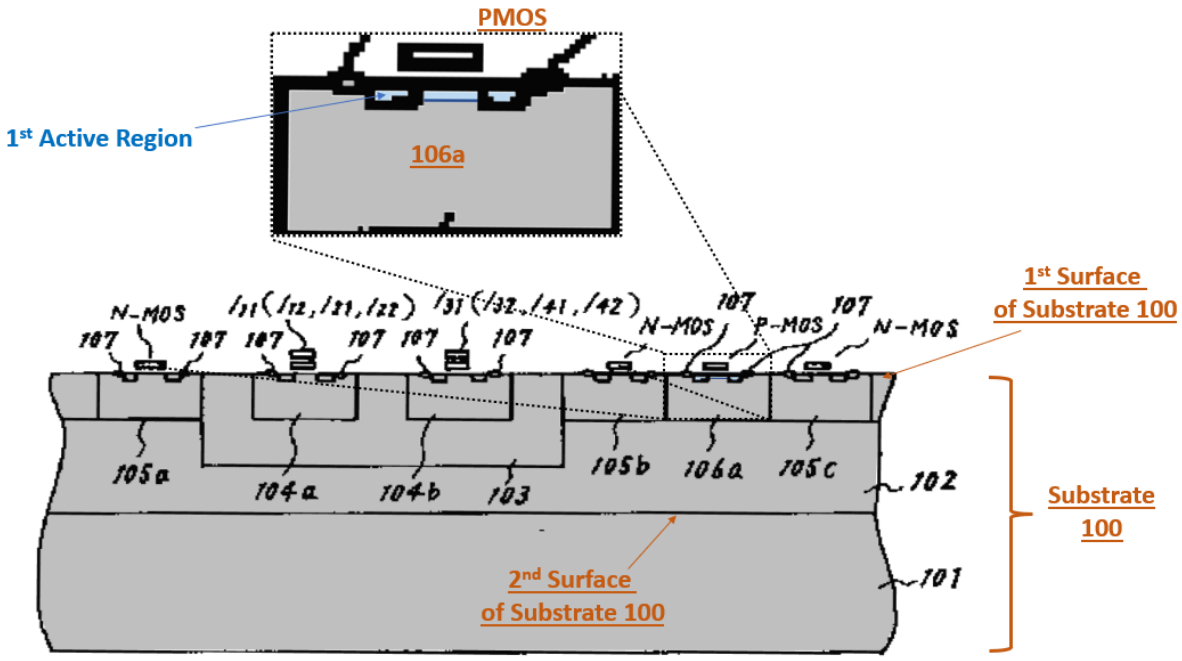
Alternative "Second Surface" of Substrate 100 in FIG. 3 of Onoda (Annotated)

(iii) Element [1.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

80. Onoda discloses this element.

81. First, Onoda discloses "a first active region that is disposed adjacent to the first surface of the substrate." Referring to annotated FIG. 3 of Onoda, reproduced below, Onoda discloses a first active region that is at or near top surface of the second semiconductor layer 102 of the substrate 100 with a PMOS transistor

and includes the top portion of N-well region 106athat is annotated in blue. (Onoda at [0043] ("106a, 106b, and 106c are N-type [] well regions") and [0044] ("the plurality of P-channel MOS transistors is formed in the fourth well regions 106a, 106b, and 106c."); see also *id*. at [0029] ("channel region that is positioned between the source region and the drain region" and [0062].)



First Active Region in n-Doped Well 106a in FIG. 3 of Onoda (Annotated)

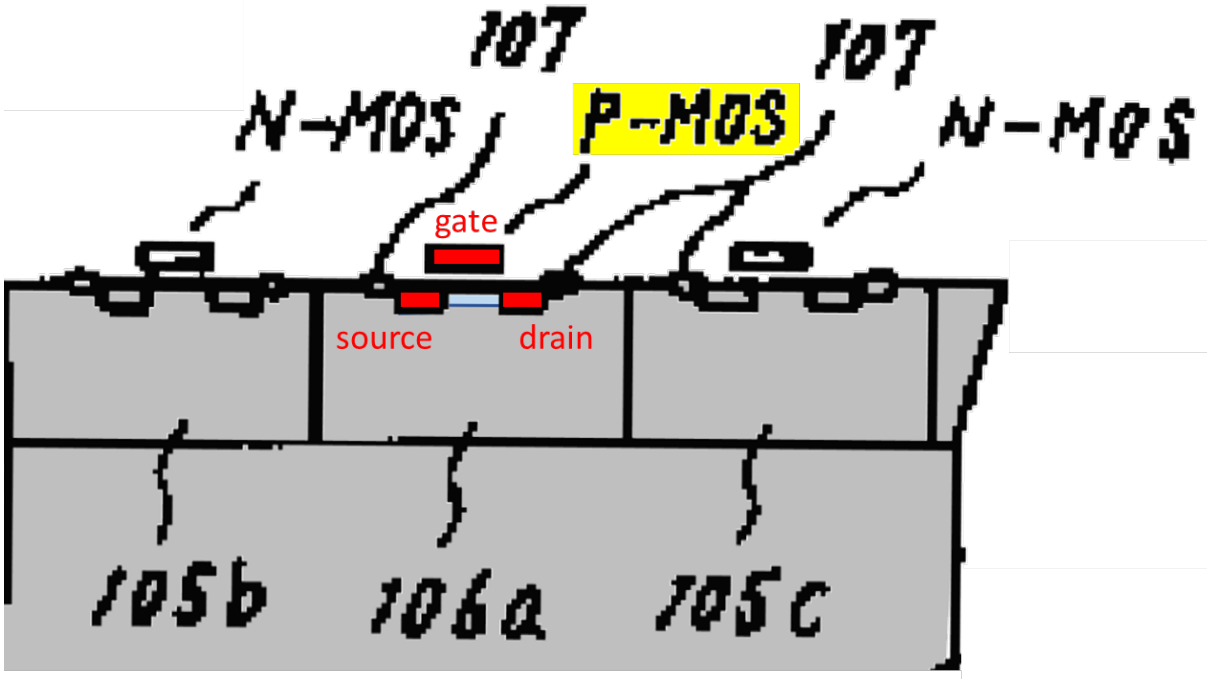
Onoda identifies multiple N-type well regions 106a, 106b, and 106c in FIG. 8 and a POSITA would have understood that the top portion of each N-type well could be

the first active region due to formation of PMOS transistors at the first surface of the substrate 100. Onoda at [0044]. For purposes of focusing my analysis, I will only discuss the top portion of N-type well region 106a as the claimed first active region that has the drain, the source and the channel of the PMOS transistor formed in the top portion of N-type well region 106a. *Id*.

82. Second, Onoda's first active region formed in the top portion of N-type well region 106a contains "a second doping type opposite in conductivity to the first doping type" of the substrate as claimed. Referring back to the above annotated FIG. 3, the first active region associated with N-well 106a contains the top portion of N-well 106a, which contains an N-type doping in its channel region between the drain and source regions by using phosphorus (P) as the N-type dopant, and that N-type doping is opposite in conductivity to the "first doping type," which was previously identified as the P-type doping in the substrate 100 by using boron (B) as the P-type dopant in Onoda. Within semiconductor devices, there are only 2 types of doping: N-type doping and P-type doping, which are opposites of each other.

83. In addition, Onoda's first active region is where "within which transistors can be formed." Onoda discloses that the top portion of n-well 106a is the "first active region" where PMOS transistors can be formed as shown in FIG. 3. Onoda at [0041]-[0045].

84. Onoda discloses that the n-well 106a supports a PMOS transistor formed in the first active region associated with the n-well 106a, and the adjacent p-well 105b/105c supports an NMOS transistor formed in the second active region associated with the p-well 105b/105c. (Onoda at [0044] ("the plurality of P-channel MOS transistors is formed in the fourth well regions 106a, 106b, and 106c"), FIG. 3).) As can be seen from the enlarged view of the transistors below taken from FIG. 3, the PMOS transistor formed in the first active region associated with the n-well 106a contains source and drain regions colored in red in the upper portion of the n-well 106a, and a gate colored in red located over the upper portion of the N well 106a. (*See also* Onoda at [0040].) The gate for the PMOS transistor is formed by an electrode as the transistor gate located over a channel region between the source and drain regions. (*See, e.g.*, Onoda at [0029] and [0041]-[0045].)



Enlarged view of a PMOS transistor in n-well 106a as an example of the PMOS and NMOS transistors in FIG. 3 of Onoda.

85. The above understanding of Onoda is consistent with the Patent Owner's own representation to the district court: "active region … within which transistors can be formed" "means exactly what it says: an active region (*i.e.*, a doped region at the surface of a semiconductor device) where a transistor can be formed." PO Res. Br. at 31. As an example, Patent Owner stated, "that an active region includes a source and drain (two doped regions at the surface of a semiconductor device where a transistor can be formed)" and that "[w]hile the active region may be

'located within' or 'surrounded by' the well region, Dr. Rao made it clear that the active region is where the transistors are built or may be built." PO. Br. at 31.

86. In the context of Element [1.2], a POSITA would have understood that "a first active region disposed adjacent the first surface of the substrate" means the first active region is disposed vertically adjacent the first surface of the substrate because the first active region in which transistors can be formed is below the top surface of the substrate to include the source, the drain and the channel region between the source and drain of a transistor.

87. In my opinion, the above understanding of the structure and operation of a transistor is consistent with and is confirmed by Wolf and Tauber, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986),[6] which teaches and depicts the active region of a MOS transistor that includes a channel under a gate G (e.g., doped polysilicon or metal electrode) and heavily doped source and drain regions in a doped semiconductor body with an opposite doping type to the doping of the drain and source regions. (Wolf at 299 ("The top surface of the body consists

[6] Exhibit 1008.

of *active* or *transistor* regions …. The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions.”))

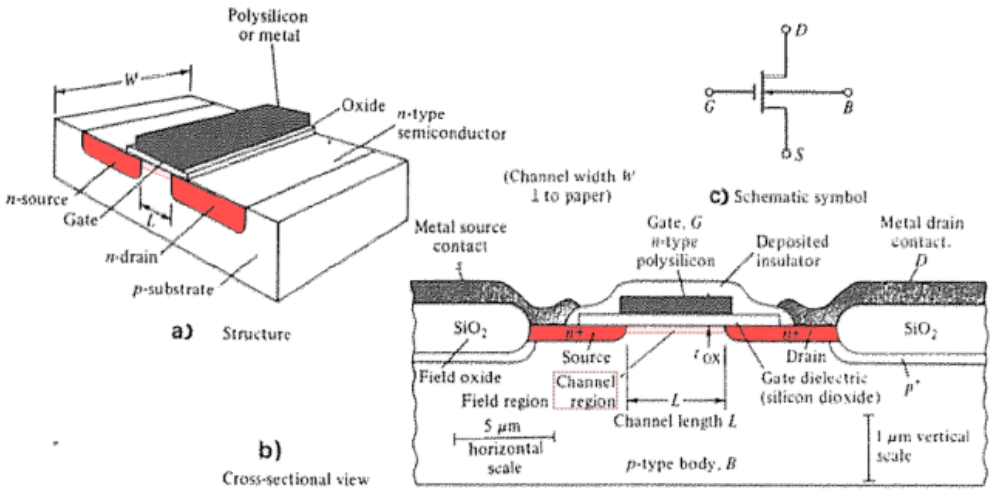


FIG. 5-1 of Wolf and Tauber, at Page 299

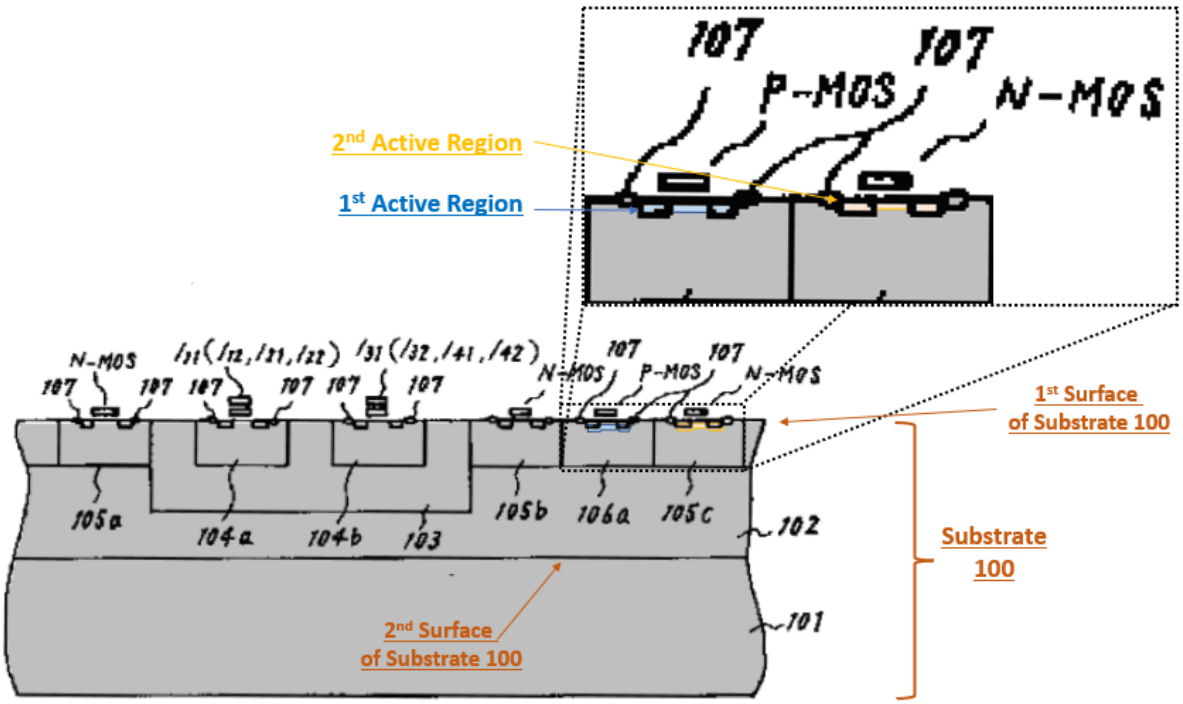
(iv) Element [1.3]: “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;”

88. In the context of Element [1.3], a POSITA would have understood “a second active region separate from the first active region disposed adjacent to the first active region” to mean a lateral or horizontal adjacency between the first and second active regions because Element [1.3] recites that the first and second active regions are regions “in which transistors can be formed.”

89. Onoda discloses this element. In annotated FIGS. 2 and 3, Onoda discloses second active regions formed in P-type wells 105a, 105b, and 105c, with

one of them annotated in tan to include a drain, a source and a channel region between the drain and source in the top portion of each P-type well, where an electrode is located over the channel region as the transistor gate for an NMOS transistor. (Onoda at [0043] ("105a, 105b, and 105c are P-type [] well regions"); *see also id.* at [0044] ("the plurality of P-channel MOS transistors is formed in the fourth well regions 106a, 106b, and 106c"), Claim 2 and [0029] ("a channel region that is positioned between the source region and the drain region" and [0062].) The second active region associated with the p-well 105c[7] is laterally or horizontally separate from and adjacent to the first active region associated with the adjacent n-well 106a.

[7] As with my discussion of the n-type wells, I will only discuss one p-type well to focus my analysis, but any p-type well would satisfy this limitation.

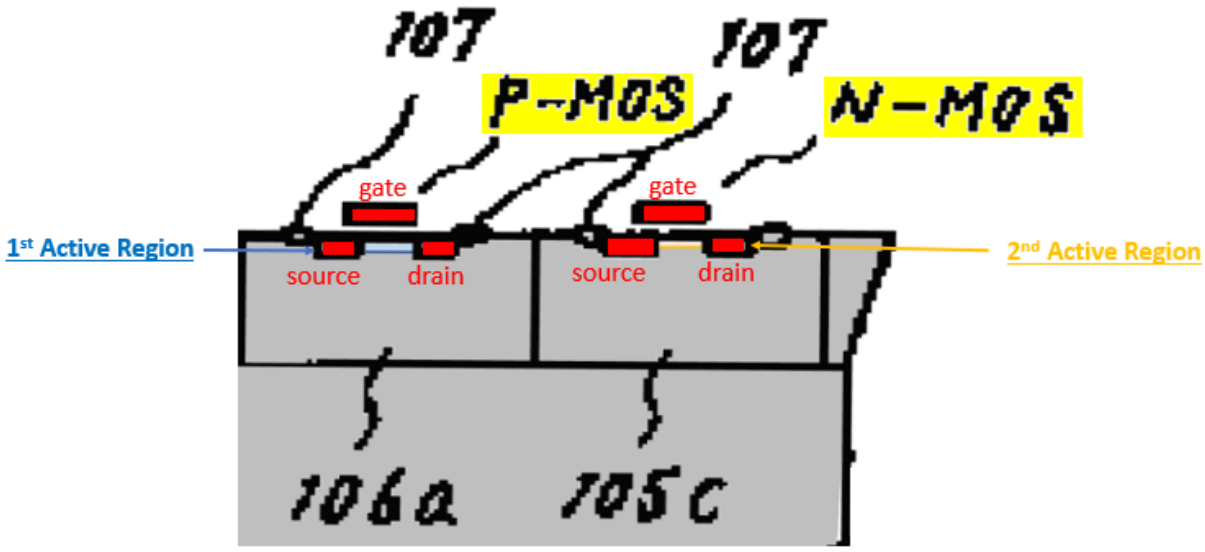


(Onoda at FIG. 3 (annotated).)

90. As I discussed above in the Overview of Technical Concepts, a POSITA would have understood that the first active region associated with the N-type well 106a in Onoda is a region in which multiple PMOS transistors "can be formed" and that the second active region associated with the P-type well 105c in Onoda is a region in which multiple NMOS transistors "can be formed." In addition, a POSITA would have understood FIG. 3 to be only a small section of the entire device, and other transistors would exist. For instance, an NMOS is depicted in p-

well 105a (left) and a POSITA would understand that a PMOS, in an n-well 106b, would be to the left of that. See FIG. 2 of Onoda.

91. Furthermore, as shown in the above annotated FIG. 3 of Onoda and the enlarged view of the transistors in FIG. 3 (below), Onoda discloses an NMOS transistor formed in the second active region with the source and drain regions provided in the upper portion of the P-well 105c as indicated by red color. As can be seen from the enlarged view of the transistor, a gate marked in red is provided for the NMOS transistor above a channel between the source and drain regions. (See, e.g., Onoda at [0029] ("a channel region that is positioned between the source region and the drain region") and [0062].) Furthermore, as I have discussed in preceding portions of my declaration at ¶¶ 35-45, a POSITA would have found it obvious to include multiple active regions in a single well (if that we argued to be a requirement of the claim, which it is not).



Enlarged Portion of FIG. 3 of Onoda (Annotated)

(v) Element [1.4]: "transistors formed in at least one of the first active region or second active region; and,"

92. Onoda discloses this element. As discussed with regards to Elements [1.2] and [1.3], Onoda discloses transistors that are formed in the first active region and the second active region, where the "first active region" contains a PMOS and the "second active region" contains an NMOS. This is depicted in the above enlarged portion of FIG. 3 in Onoda.

93. To the extent this element is construed to require multiple transistors in the first active region or the second active region, it would have been obvious to

include multiple transistors into the same active region. As discussed in the Overview of Technical Concepts, forming multiple transistors in a single n-well or p-well was well known in September 2004 (the time of the purported inventions) and a POSITA would have understood that Figure 3 is a 2-D cross section of the wells and active regions and that both extend into and out of the page. (II.C; *see also* Onoda at [Brief Descriptions of the Drawings] ("FIG. 3 is a cross-sectional drawing")) When the plane is adjusted to view the wells from the top, a POSITA would observe multiple transistors in the same well region and thus active region.

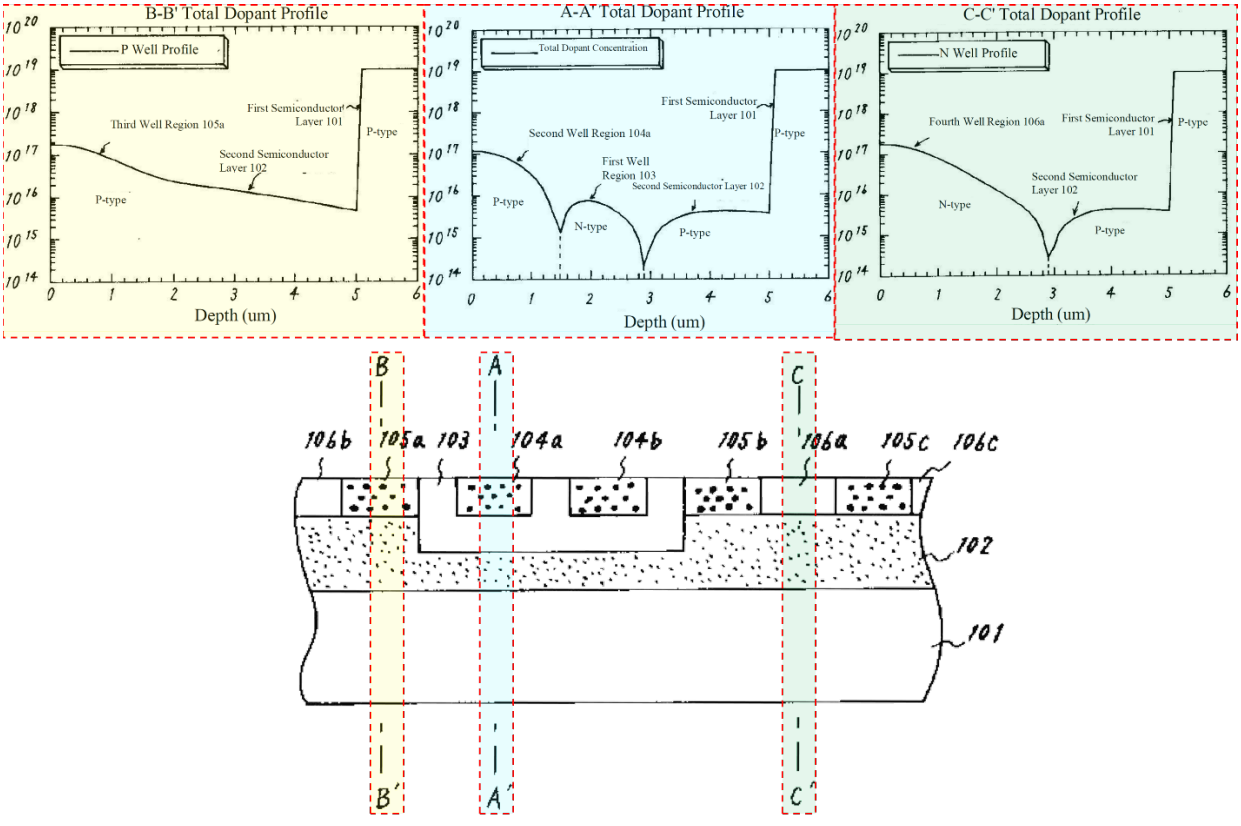
(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

94. Onoda discloses this element.

95. At least a portion of at least one of Onoda's first and second active regions has a downward-sloping dopant concentration extending from the first surface (the top surface of the second semiconductor layer 102 of the substrate 100) to the second surface (the bottom surface of the second semiconductor layer 102 of the substrate 100).

96. Onoda discloses several cross-sectionals demonstrating dopant concentration as a function of depth in FIGS. 10-12. FIG. 10 depicts a cross

sectional of A-A' in FIG. 8 across p-type second well region 104a and n-type first well region 103; FIG. 11 depicts a cross sectional of B-B' in FIG. 8 across third well region 105a, which is p-type; and FIG. 12 depicts a cross sectional of C-C' in FIG. 8 across fourth well region 106a (which is n-type). FIGS. 10-12 show different dopant concentrations and their spatial variations along the lines A-A', B-B' and C-C' through the second semiconductor layer 102 and first semiconductor layer 101 of the substrate 100 in the Onoda device.



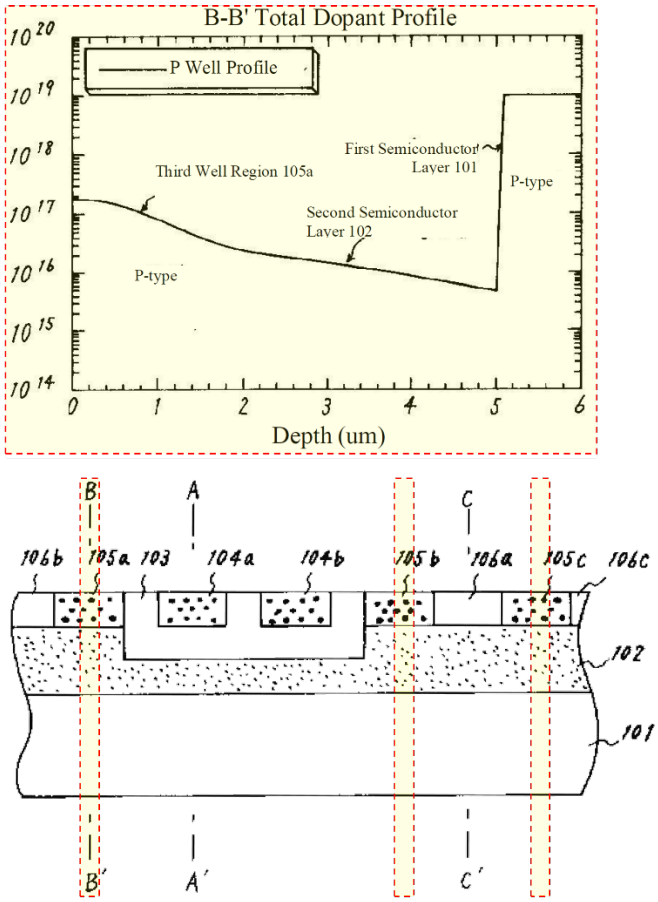
(Onoda, Annotated FIGS. 8, 10-12.)

97. The Claim Element [1.5] recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate." I analyze FIGS. 8 and 11 with respect to Claim Element [1.5] below.

98. FIG. 8 from Onoda, again excerpted below, shows a slice B-B' through the fabricated device via P-type well region 105a in FIG. 3 (*see, e.g.*, Onoda at [0041]-[0045]). Annotated FIG. 11 from Onoda, also shown below, depicts the graded dopant concentration profile from the top to the bottom of the fabricated device along the line B-B', which cuts through one of the "second active regions," namely the "second active region" formed in P-type well region 105a. FIG. 11 shows the graded dopant concentration of p dopants in that P-type well region 105a decreases from the top surface into the interior of the P-type well region 105a and, in addition, the graded dopant concentration continues below the P-type well region 105a in the P-type second semiconductor layer 102. The B-B' cross sectional demonstrates the dopant profile as a function of depth from the surface through third well region 105a, second semiconductor layer 102, and first semiconductor layer 101, and a POSITA would understand that the same or similar dopant profile would exist for locations where other third well regions are located, *e.g.*, 105b and 105c because they undergo similar doping. (*See, e.g.,* Onoda at [0042] ("105a, 105b, and

106c are P-type third well regions formed in the surface of the second semiconductor layer 102"), [0049] ("the region wherein the N-channel MOS transistors that structure the peripheral circuitry are formed) are masked (not shown), and boron [B], which is a P-type dopant, is implanted through the mask into the desired region at 100 keV and between 1×10^{12} and 1 x $10^{13}/cm^2$, to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Thereafter, the mask is removed, the boron implantation layers 104A, 104B, 105A, 105B, and 105C, are masked, and phosphorus [P], which is an N-type dopant, is implanted through the mask into the regions other than the boron implantation layers 104A, 104B, 105A, 105B, and 105C at 150 keV and between 1 x 10^{12} and 1 x 10^{13}/cm2, to form phosphorus implantation layers 106A through 106D.").)

99. The paths showing dopant profiles going through the third well region 105a (and, as a POSITA would understand, p-well regions 105b, 105c) are annotated below in yellow.



FIGS. 8 and 11 of Onoda

100. Shown above is the graded concentration profile of FIG. 11 annotated in yellow on top of FIG. 3, going through the third well regions 105a, 105b and 105c, second semiconductor layer 102, and first semiconductor layer 101. The below illustrates the claimed "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

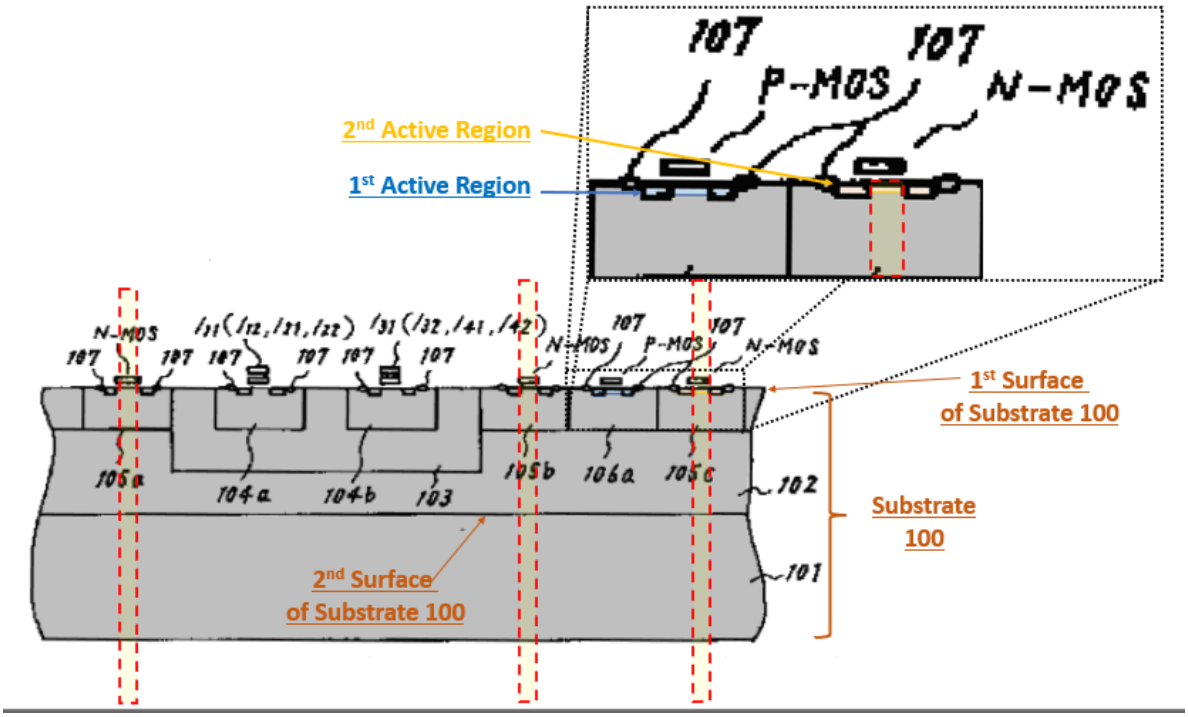


FIG. 3 of Onoda (Annotated)

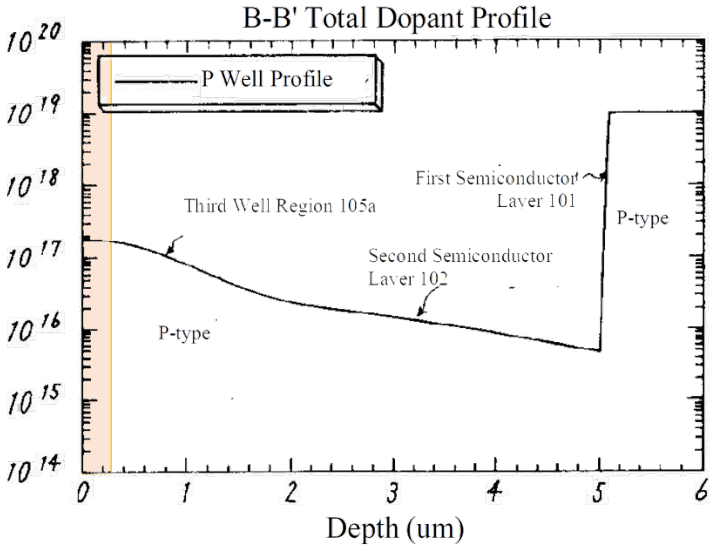


FIG. 11 of Onoda (Annotated)

101. FIG. 11 of Onoda above is annotated to show the second active region in tan and the associated graded P-type boron dopant concertation in the second active region: a decrease in the P-type boron dopant graded concentration as a function of depth across the second active region. It was known that a decrease in the dopant concentration of P-type dopants from the top of the P-type well region 105a towards the bottom of the P-type well region 105a as shown in Onoda produces an electric field to drive electrons as the minority carriers in the P-type well region 105a to move from the top surface of the second active region towards the bottom of the P-type well region 105a. It is basic semiconductor physics that the electric drift field created by the decreasing P-type graded dopant concentration is directed against the decreasing direction of the graded dopant concentration because the boron dopant concentration is greater near the top surface and decreases with depth into the substrate away from the top surface.[8] The presence of this electric field with

[8] The generation of the above electric field pointing against the decreasing direction of the P-type graded dopant concentration in p-well region 105a is due to the fact that boron atoms fixed in position within the silicon and bonded to 4 adjacent silicon atoms are negatively charged boron ions due to the missing 4th electron in each

its direction pointed to the top surface pushes the electrons in the opposite direction of the electric filed toward the P-type doped substrate layer 102. Thus, the continuous decrease in the graded dopant concentration of p dopants in the P-type doped second semiconductor layer 102 below the second active region near the top of the P-type well 105a, 105b or 105c keeps driving electrons towards the bottom surface of the P-type doped second semiconductor layer 102. Therefore, an electron is subject to this electric field pointing from the bottom surface of the second

boron atom and the concentration of such negatively charged boron ions in the boron doped silicon is higher at and near the top surface and decreases with depth below the top surface. The electric field created by such a spatial gradient of negatively charged boron ion concentration is directed from a lower negatively charged boron ion concentration location to a higher negatively charged boron ion concentration location. This can also be understood by the fact that, in the presence of the graded boron dopant concentration, a negative charge electron is subject to more electric repulson by negatively charged boron ions at a location with a higher negatively charged boron ion concentration than a location with a lower negatively charged boron ion concentration.

semiconductor layer 102 to its top surface throughout the second semiconductor layer 102. As a result, an electron will be driven by this electric field to move from the top surface to/towards the bottom surface of the second semiconductor layer 102. This movement of the electrons in the second semiconductor layer 102 is towards the first semiconductor layer 101 in the substrate 100. The net effect of the above operations in both p-well region 105c (also in 105a and 105b) and the P-type doped second semiconductor layer 102 is to aid carrier movement of minority carrier electrons from the top surface of the p-well region 105a (the first surface of the substrate 100) to the bottom surface of the layer 102 and into or toward the first semiconductor layer 101. This movement of minority carrier electrons is directed to the bottom surface of the second semiconductor layer 102 of the substrate 100. This movement of the minority carrier electrons is along a direction that points towards the bottom surface of the first semiconductor layer 101.

102. Moreover, claim limitation [1.5] requires that "at least a portion of at least one of the first and second active regions" be the active regions that have the recited graded dopant concentration. This is taught by Onoda because the above annotated "second active region" itself (within the P-type well 105c that supports one or more NMOS transistors) has a graded dopant concentration. As can be seen in annotated FIG. 11, above, the small area which comprises the "second active

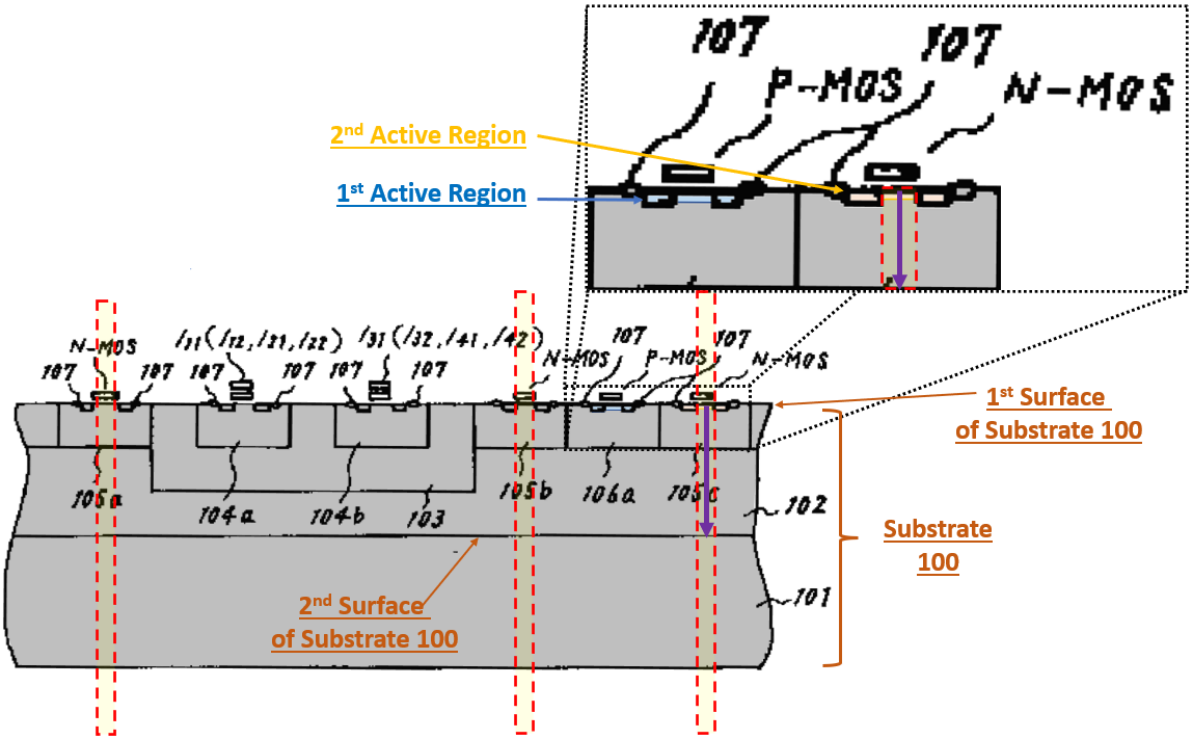
region" (tan) has a downward gradient dopant concentration. A POSITA would have understood that, because the claim requires a "region," the claimed "region" can encompass a larger or smaller portion of a well, such as the p-well 105a, or 105b or 105c.

103. As discussed previously above, Patent Owner acknowledged during prosecution of the '842 Patent's parent (the '195 Patent) that graded dopant concentrations were known to create a static electric drift field that would result in carrier movement (e.g., the movement of minority carriers). (*Supra* II.D) Indeed, Patent Owner declared, "[T]he graded dopant concentration itself creates a 'built-in' electrical field." *Id.* This "built-in" electric field "forces the movement of carriers into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant." This movement of the minority carriers (electrons) in Onoda is depicted by the purple arrow in annotated FIGS. 8 and 11. This teaching by Onoda teaches and renders obvious the claimed "having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

104. This downward dopant gradient—in the claimed "second active region"—provides the claimed "aid carrier movement from the first surface to the

second surface of the substrate." A POSITA would understand, in the p-well, that minority carriers are electrons and that those electrons would flow in accordance with a downward P-Type dopant gradient profile (as depicted in FIG. 11). As can be seen from the purple arrowed lines in both the P-type well 105c and the second semiconductor layer 102 of the substrate in an annotated FIG. 3 below, in the active region carrier movement of minority carrier electrons is aided from the first surface as the top surface of the second semiconductor layer 102 to the second surface as the bottom surface of the second semiconductor layer 102.

105. This is depicted below, where the portion of the tan-annotated second active region "aid[s] carrier movement from the first surface to the second surface of the substrate."



(Onoda at FIG. 3 (annotated).)

106. Finally, it should be noted that the downward movement of minority carrier electrons is halted at the junction of the second semiconductor layer 102 and first semiconductor layer 101 of the substrate 100 in Onoda. FIG. 11 of Onoda further shows that the P-type boron dopant concentration in the first semiconductor layer 101 of the substrate 100 exhibits a sharp step like increase from a low dopant concentration of 1 x $10^{15}/cm^3$ to a very high dopant concentration around 1 x $10^{19}/cm^3$, which is much higher (by nearly two orders of magnitude) than the highest P-type dopant concentration (around dopant concentration of 1 x $10^{17}/cm^3$. The

minority carrier electrons, once reaching this heavy P-type doping in the second semiconductor layer 101, will be annihilated by the heavy P-type doping and will no longer exist.

107. It would be incorrect to interpret the claims to require the second surface of the substrate in the claim to be the physical bottom surface of the first semiconductor layer 101 of the substrate 100 in Onoda. *First*, such an interpretation is inconsistent with the claim language, which requires only that " ***at least a portion of*** at least one of the first and second active regions" to have the "at least one graded dopant concentration" to aid carrier movement from the first surface to the second surface of the substrate. A POSITA would understand that the first or second active region is necessarily a shallow region near the top of a doped well where "transistors can be formed" and would not extend beyond the first and second active regions or all the way to an area of the substrate where there are no active regions or wells. *Second*, the '842 Patent specification discloses the movement of minority carriers only in the regions where the dopant concentration has a decreasing graded concentration. The '842 Patent provides that a graded dopant region that exists above a P^- substrate region to pull minority carriers downward as shown by the allows in FIG. 5B, below, toward the top surface of the P^- substrate region. The specification of the '842 Patent confirms this by stating that minority carriers are

swept ***into*** the substrate and not out of the substrate. ('842 Patent at 3:61-64 ("creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible").)

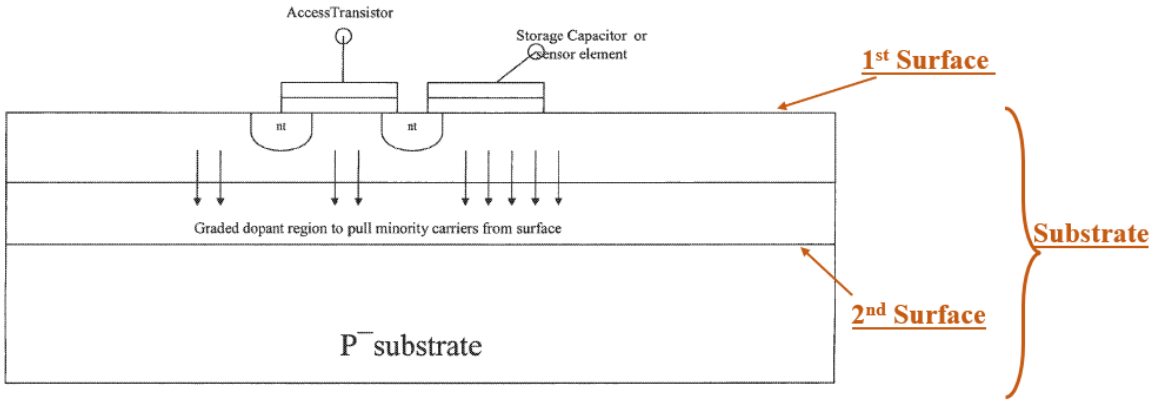
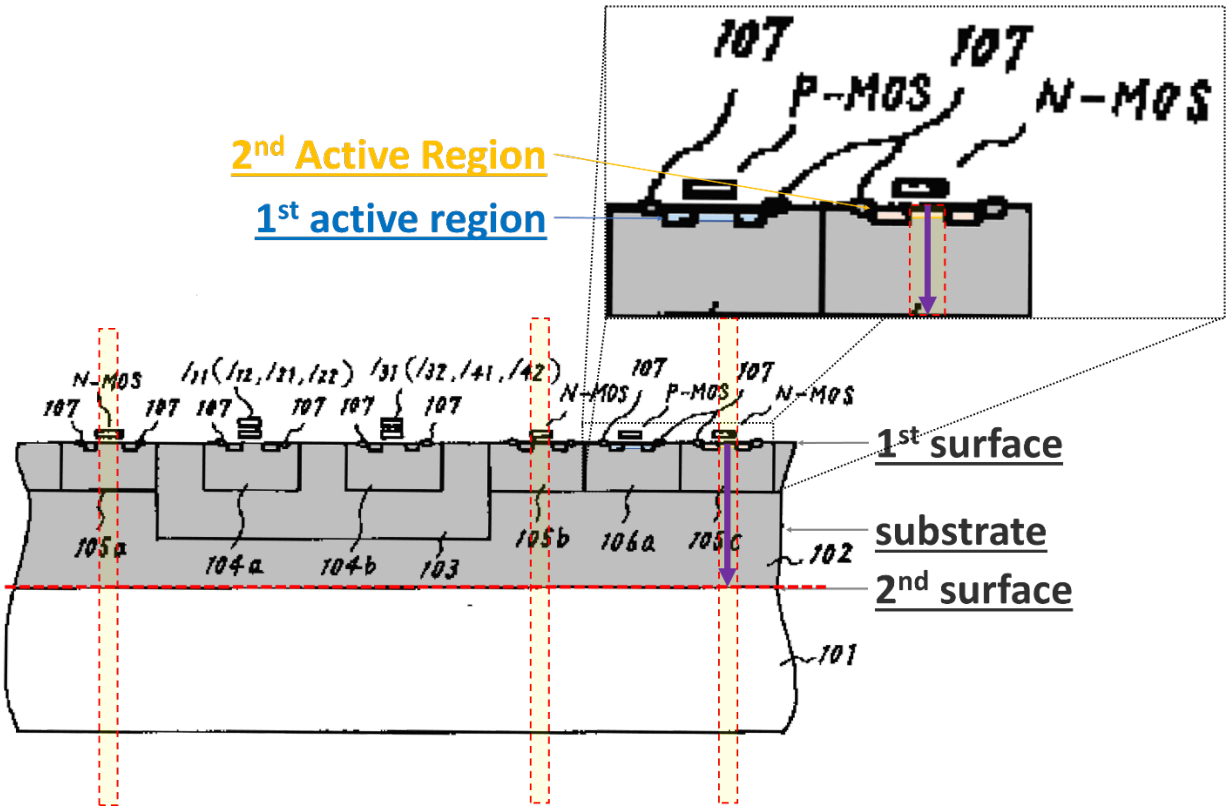


FIG. 5B of '842 Patent (Annotated)

108. Furthermore, the substrate itself has several interfaces between different substrate layers in the substrate, and a POSITA would understand that those interfaces could be understood as a surface. For instance, as I explained above, I map Onoda's interface between the first and second semiconductor layers 101 and 102 to the claimed second surface of the substrate. With that mapping, the carriers (*e.g.*, minority carrier electrons) would drift from the first surface to the second surface of the second semiconductor layer 102 of the substrate 100 in Onoda.



109. Finally, to the extent that the claimed "second surface of the substrate" in "at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate" is construed to be the physical outer or bottom surface of the substrate, the term "aid" in "to aid carrier movement from the first surface to the second surface of the substrate" in Claim Element [1.5] only states "to aid" the movement and does not require to physically place the carriers at the bottom surface of the substrate. In addition, the term "to" in "from the first surface ***to*** the second surface of the substrate" has an ordinary and plain meaning as a function word to indicate movement or an action or condition suggestive of

movement toward a place or to indicate a direction of the movement.[9] This interpretation of the term "to" is consistent with and supported by the specification of the '842 Patent. Therefore, a POSITA would understand, the disclosure by Onoda of its downward P-type graded dopant concentration in the second active region, in the p-well 105a, and in the second semiconductor layer 102 (as depicted in FIG. 11) will cause the minority carrier electrons to move from the first surface as the top surface of the second semiconductor layer 102 to the second surface as the bottom surface of the second semiconductor layer 102 and this effect is to aid the movement of minority carrier electrons towards the bottom surface of the first semiconductor layer 101 because the direction of the movement is pointed downward.

110. Therefore, my analyses of Onoda and my conclusion with respect to Claim Element [1.5] above are unchanged and remain the same when mapping either the bottom surface of the second semiconductor layer 102 of the substrate 100 in Onoda or the bottom surface of the first semiconductor layer 101 of the substrate 100 to the claimed "second surface of the substrate" in Claim Element [1.5] and Claim 1.

[9] For example, see dictionary definition of "to" in the Merriam-Webster online dictionary at https://www.merriam-webster.com/dictionary/to.

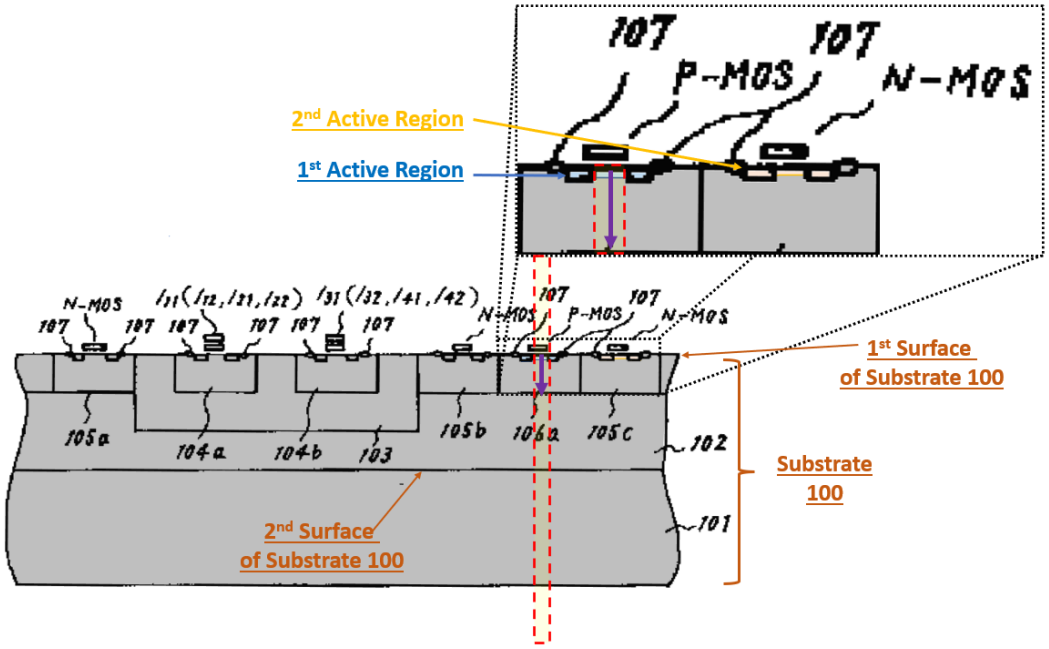
111. Accordingly, the above analyses of teachings in Onoda in FIGS. 8 and 11 demonstrate Onoda discloses or renders obvious Claim Element [1.5].

112. Next, I analyze Onoda's disclosure of its N-type well 106a that has a first active region in the top part of the well 106a in which PMOS transistors can be formed as shown in FIGS. 8 and 12 to demonstrate those additional teachings in Onoda disclose or render obvious Claim Element [1.5].

113. FIGS. 3 and 12 of Onoda are produced and annotated below to show relevant features of Onoda's N-type well 106a. Since well 106a is N-type doped with phosphorus, electrons donated by phosphorus are the majority charge carriers and electrons are the minority charge carriers in well 106a. As shown in FIG. 12, the N-type graded phosphorus dopant concentration in the well 106a has a downward gradient from the top surface of the well 106a which is the top surface of the second semiconductor layer 102 to the bottom of the well 106a. Along the C-C' line below the well 106a within the second semiconductor layer 102, the doping type is P-type by using boron. The PN junction at this interface forms a depleted region containing a strong electric field pointing downward. This field will continue to move holes downward. At the interface between the P-doped second semiconductor layer 102 and the P-doped first semiconductor layer 101 of the substrate 100, the P-type dopant

concentration jumps up stepwise by more than two orders of magnitude in the first semiconductor layer 101.

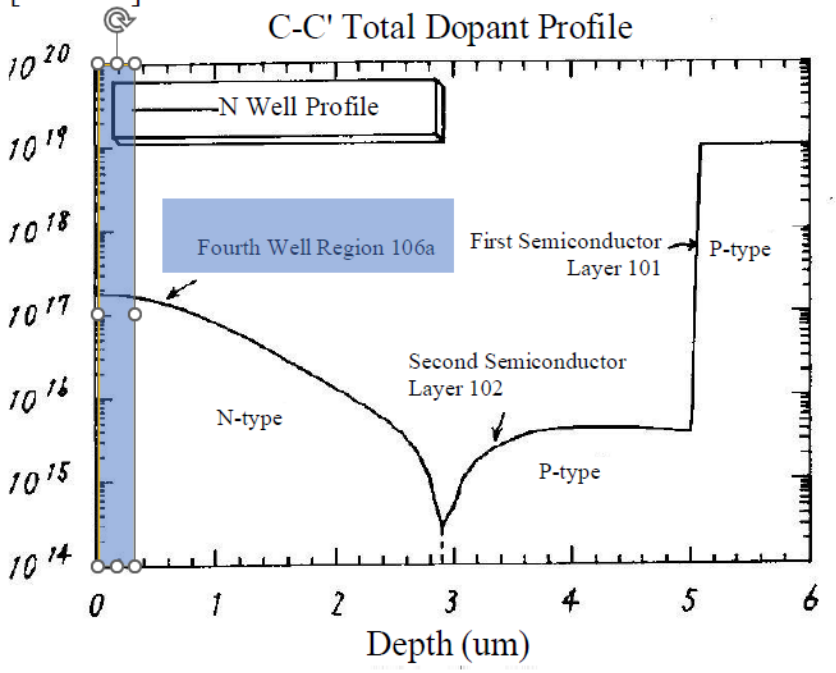
114. Although the N-type doping in the well 106a along the C-C' line is different from the above P-type doping along the B-B' line through the well 105a (the well105b or 105c should have a similar doping profile), the design is based on the same basic semiconductor physics of using the electric drift field created by the N-type graded phosphorus dopant concentration to move holes as the minority carriers away from the top surface of the n-well 106a and the first active region therein towards lower part of the second semiconductor layer 102 of the substrate 100. The difference here in the n type doping in the well 106a along the C-C' line is to aid downward movement of holes as minority carriers in the N well 106a instead of the electrons as the minority carriers in the p-well 105a along the B-B's line.



PMOS Transistor and Associated N-Type Well 106a in FIG. 3 of Onoda

(Annotated)

[FIG. 12]



Graded N-Type Dopant Concentration in First Active Region in N-Type Well 106a of FIG. 12 of Onoda (Annotated)

115. In Onoda's the n-well 106a, n type phosphorus atoms fixed in silicon are bonded to 4 adjacent silicon atoms as positively charged phosphorus ions due to the presence of its 5th valance electron as a free moving electron in each phosphorus atom and the concentration of such positively charged phosphorus ions in the phosphorus doped silicon is higher at and near the top surface and decreases with depth below the top surface towards the bottom of the n-well 106a. The electric field created by such a spatial gradient of positively charged ion concentration is directed downward. For positively charged holes as minority carriers in the n-well

106a, the electric field created by the downward graded N-type phosphorus dopant concentration points from a region at or near the top surface of the well 106a towards the bottom of the n-well 106a. In addition, the electric field created by the graded increasing P-type boron dopant concentration in the lower part of the second semiconductor layer 102 of the substrate 100 below the well 106a is also pointed towards the bottom surface of the second semiconductor layer 102 along the line C-C' due to the spatially increasing concentration of negatively charged boron ions in silicon. Therefore, the electric fields in both the n-well 106a and below the n-well 106a in the second semiconductor layer 102 of the substrate 100 along the line C-C' are pointed downward towards the first semiconductor layer 101 and are opposite to the direction of the electric field created by the downward P-type graded dopant concentration in the p-well 105a, 105b or 105c along the line B-B' in FIG. 8. As a result, the minority hole carriers after being moved away from the top surface and the first active region in the upper portion of the n-well 106a to enter the region within the second semiconductor layer 102 below the n-well 106a will be continued moved by the downward electric field created by the increasing concentration of negatively charged boron ions with depth and so are swept into the first semiconductor layer 101 of the substrate 100.

116. Therefore, Onoda discloses "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration" by its stepwise decreasing n type graded phosphorus dopant concentration in the N well 106a. Because this n type graded phosphorus dopant concentration in the N well 106a moves holes along the line C-C's towards the bottom of the n-well 106a and into semiconductor layer 101, Onoda teaches that this graded phosphorus dopant concentration in the n-well 106a is "to aid carrier movement from the first surface to the second surface of the substrate."

117. In light of the above, Onoda discloses and renders obvious all limitations and their combination of Claim 1.

b. Dependent Claim 2 of the '842 Patent: "The semiconductor device of claim 1, wherein the substrate is a p-type substrate."

118. Onoda discloses this claim, as it discloses a p-type substrate 100. Onoda's flash memory has "a semiconductor substrate 100" that includes a first semiconductor layer 101 that is p doped and a second semiconductor layer 102 that is also p type doped. (Onoda at [0041] ("FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention").) "101 is a first semiconductor layer made from a heavily-doped … P-type silicon substrate, and 102 is a P-type doped second semiconductor layer." (*Id*.;

see also id. at [0041] and [0046]-[0047]; *see also id.* at "Brief Description of the Drawings" describing FIGS. 1 through 14 as describing features of the "first embodiment.")

c. Dependent Claim 4 of the '842 Patent: "The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

119. Onoda discloses this claim. In particular, Onoda teaches that the substrate 100 includes the epitaxial semiconductor substrate 102 on top of a nonepitaxial substrate 101 which is a heavily-doped P-type silicon substrate. (Onoda at [0041] and [0046]-[0047].) Onoda discloses that a lightly-doped P-type epitaxial layer 102a with a dopant concentration of 1 x $10^{15}/cm^3$ is formed with a thickness of about 5 μm through epitaxial deposition onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x $10^{19}/cm^3$. (Onoda at [0046].) Subsequent implantation of dopant (*e.g.*, boron B) creates an ion implantation layer 102b, which is then subjected to heat treatment to produce a lightly-doped P-type second semiconductor layer 102. As shown in Figure 5, Onoda's lightly-doped P-type semiconductor layer 102 is an epitaxial layer on top of the first semiconductor layer 101 which is a nonepitaxial substrate.

d. Dependent Claim 5 of the '842 Patent: "The semiconductor device of claim 1 wherein the first active region and second active region contain one of either p-channel and n-channel devices."

120. Onoda discloses this claim. In particular, as shown in annotated FIG. 3 of Onoda, each of Onoda's active regions contains one of either p-channel devices like the PMOS transistor in the first active region in the n-well 106a and n-channel devices like the NMOS transistor in the second active region in the p-well 105a, 105b or 105c. Onoda discloses that a "plurality of N-channel MOS transistors" are contained in the second active regions formed in P-type wells 105a, 105b, and 105c, one of which is colored in green. (Onoda at [0044] ("105a, 105b, and 105c are P-type [] well regions").) Similarly, a "plurality of P-channel MOS transistors" are contained in the first active regions formed in N-type wells 106a, 106b, and 106c,. (*Id.*)

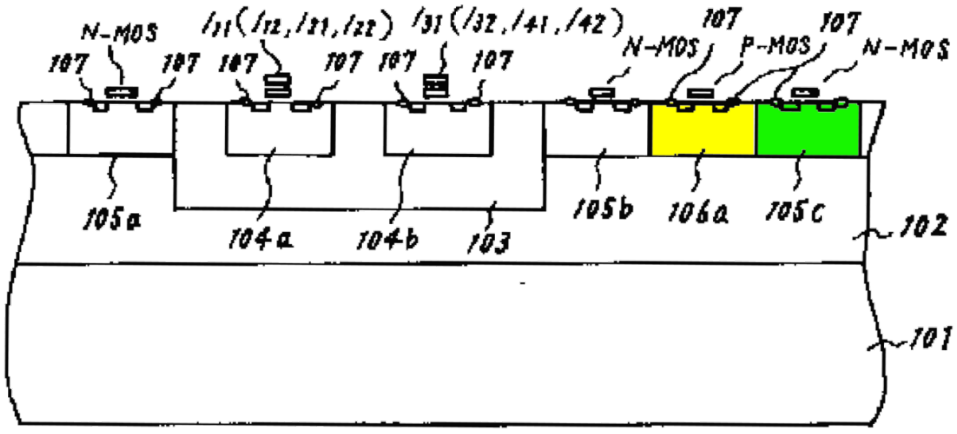
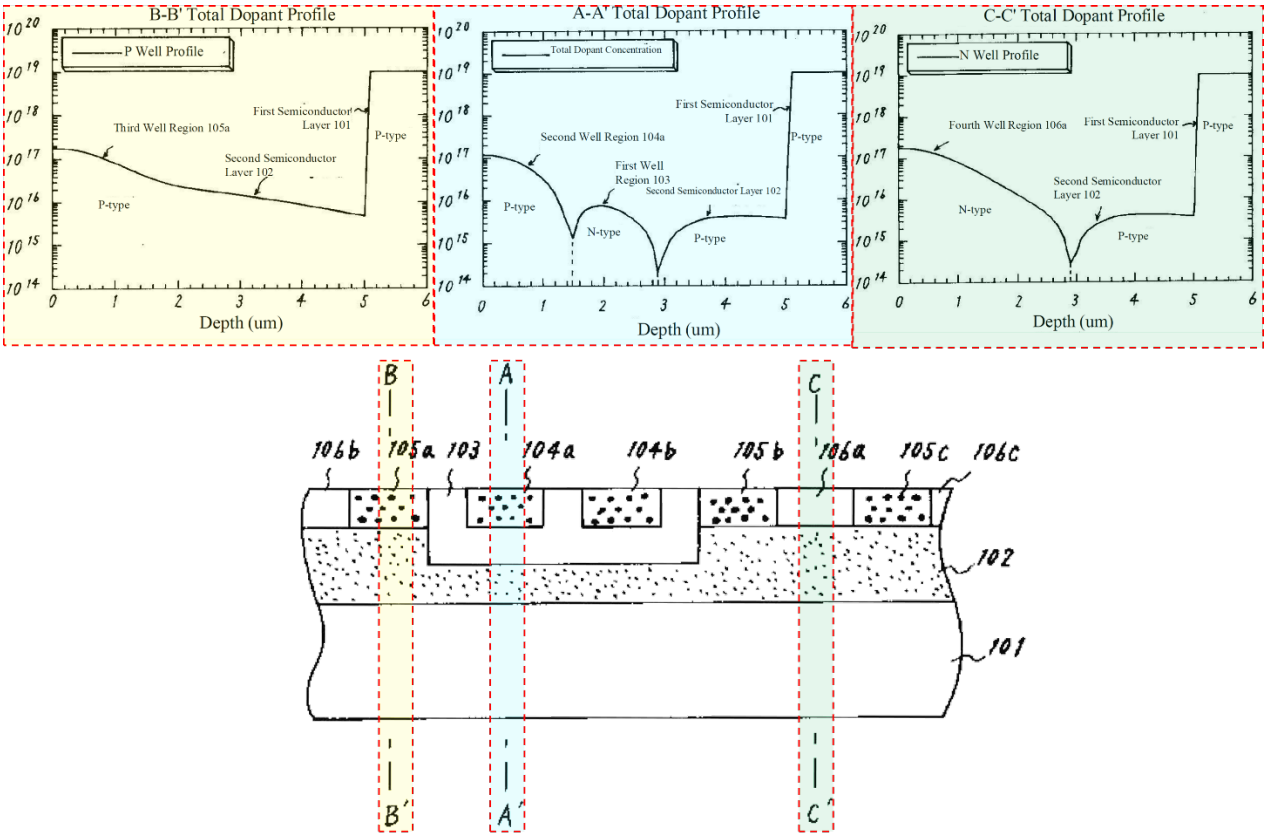


FIG. 3 of Onoda (Annotated)

e. Dependent Claim 6 of the '842 Patent: "The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each has a graded dopant."

121. Onoda discloses this claim. As previously discussed, the second active regions in Onoda contain a plurality of N-channel MOS transistors formed in the p-wells (105a, 105b, 105c) and the first active regions in Onoda contain a plurality of P-channel MOS transistors formed in the n-wells (106a, 106b, 106c). (*See* Onoda at [0042]-[0044].) Further, each active region has a graded doping profile, as shown in Onoda FIGS. 11 and 12, which provide graded dopant concentration profiles of the p-well 105a in a second active region along the line B-B' in FIG. 8 and n-well 106a in a first active region along the line C-C' in FIG. 8, respectively. FIG. 8 is further annotated (below) to show the area of the n-well region 106a along the line C-C' for which the graded dopant concentration profile along the line C-C' is shown in FIG. 12. A POSITA would understand the figures show the respective dopant profiles decrease in concentration while going further in depth toward the substrate to make a graded dopant in the well-region. (*See* Onoda FIG. 11 (the green portion labeled Third Well Region 105a"); FIG. 12 (labeled "Fourth Well Region 106a").)

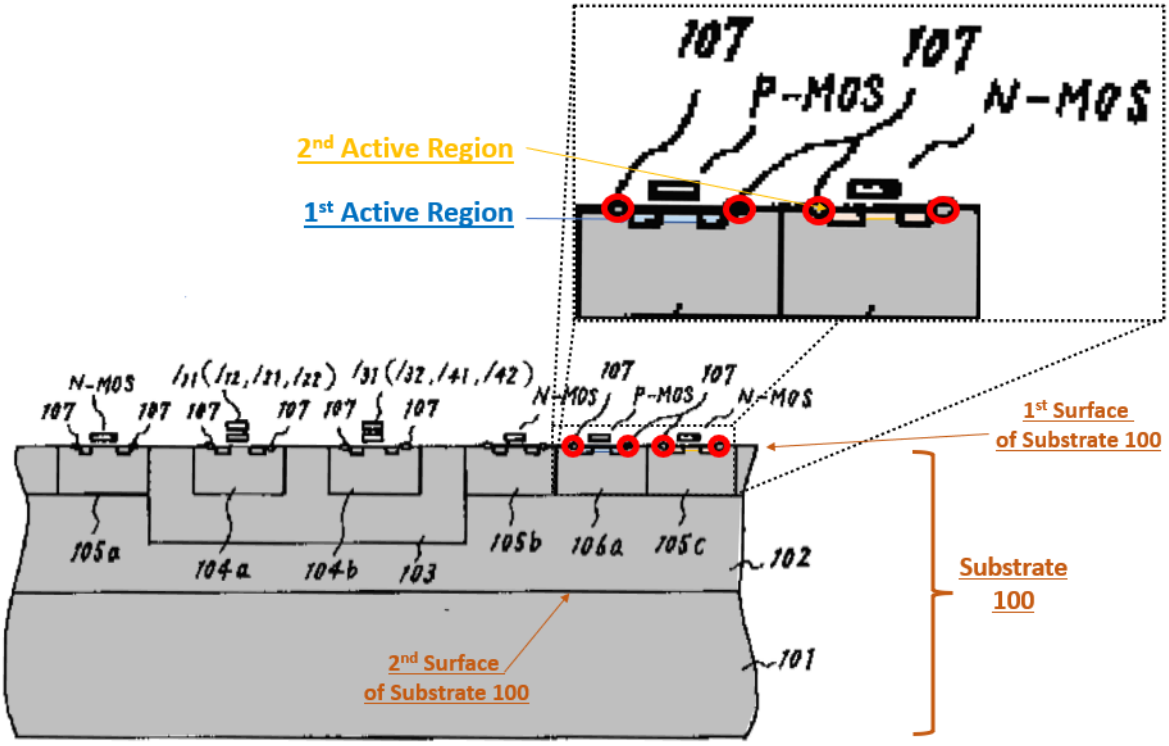


(Onoda at FIGS. 8, 10-12.)

f. Dependent Claim 7 of the '842 Patent: "The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

122. Onoda discloses this claim. In particular, Onoda discloses an "isolating oxide film (LOCOS) 107, that is formed surrounding the individual MOS transistors, as depicted in FIG. 3." (Onoda at [0045].) See annotated FIG. 3 of Onoda where the isolating oxide file 107 is marked in red. A POSITA would understand that having an isolating oxide film around each individual MOS transistor located in each

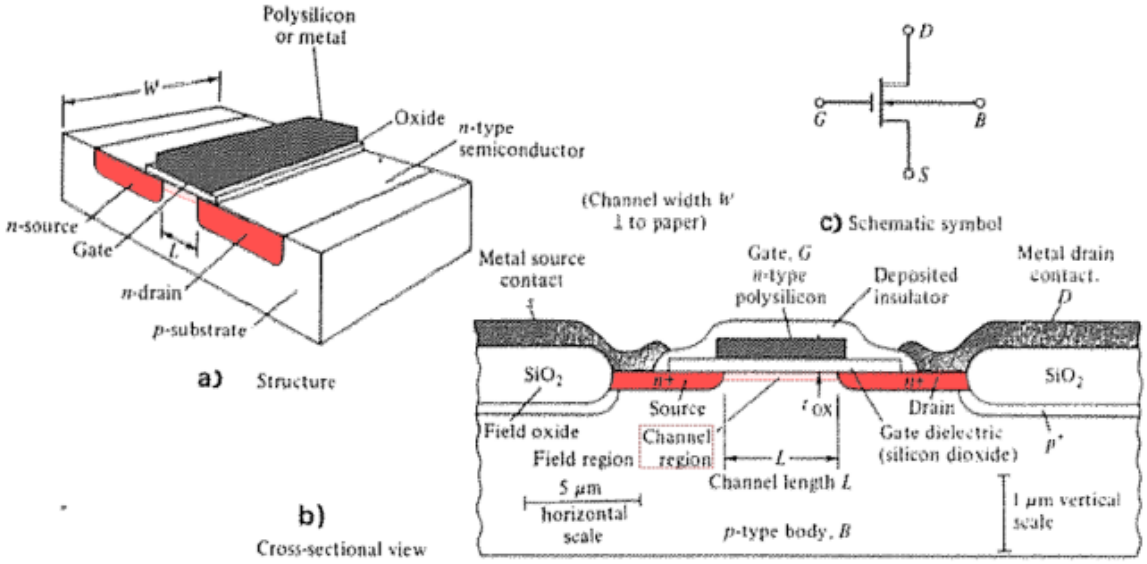
active region, provides a barrier or "isolation region" to separate the first and second active regions from electrically influencing each other.



Isolation Region in FIG. 3 of Onoda (Annotated)

123. In addition, it would have been obvious for a POSITA to employ the teachings of using an isolating oxide film to form an isolation region around each MOS transistor to the entire active region. It was well known that an electrical isolation barrier can be implemented between electrically different areas to

safeguard these areas from electrically influencing each other. (Onoda at [0045].) As shown in the figure below from Wolf and Tauber, "[a] thick oxide layer (0.5-1.0μm) is normally grown over the field regions" to prevent "[c]onduction between separate active regions." (Wolf at 299.) Applying Onoda's teachings to the entire active region would not only have been obvious to do, it would have been expected as a standard practice.



g. Dependent Claim 8 of the '842 Patent: "The semiconductor device of claim 1 wherein the graded dopant is fabricated with an ion implantation process."

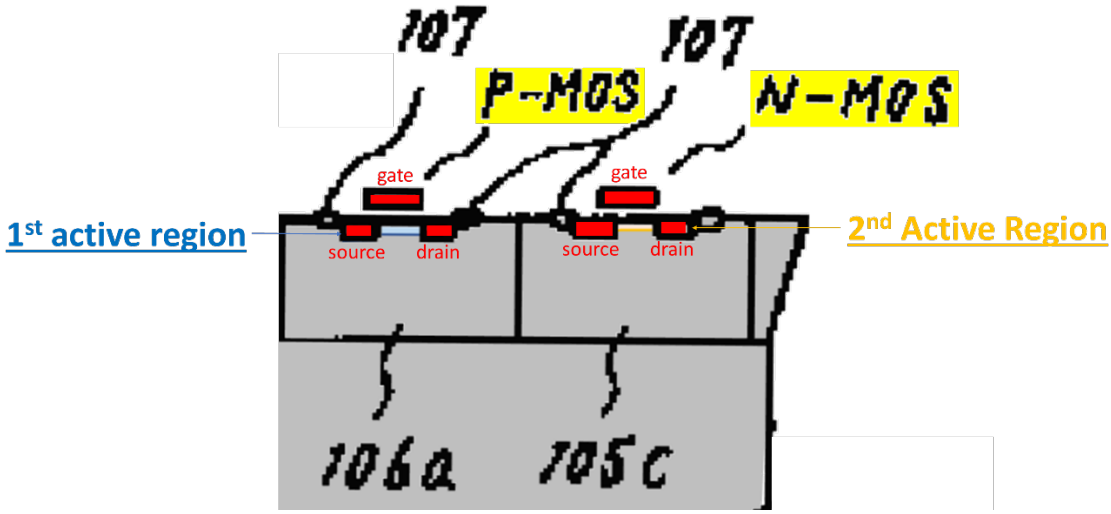
124. Onoda discloses this claim. In particular, Onoda teaches that the doped epitaxial semiconductor layer 102 is fabricated using ion implantation and includes an epitaxial layer 102a with a depth of "about 5 μm." (Onoda at [0046]-[0047].)

Further, Onoda teaches forming its well structures with deep wells are formed by ion implantation and thermal diffusion, extending 1.5 μm deep. (*Id*. at [0049]-[0050], [0052].) (*See also* FIGS. 11.)

h. Dependent Claim 17 of the '842 Patent: "The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

125. Onoda discloses this claim. In particular, Onoda discloses multiple first active regions associated with n-wells and PMOS transistors, and multiple second active regions associated with p-wells and NMOS transistors. Each active region is formed adjacent to the first surface of the substrate which is the top surface of the second semiconductor layer 102 of the substrate 100. Referring to the above and other produced versions of FIG. 3 in Onoda, the top surface of Onoda's semiconductor substrate 100 contains the second active regions of the NMOS transistors in p-well regions 105a, 105b and 105c. Each of p-well regions 105a, 105b and 105c itself has source and drain regions (marked in red). (Onoda at [0043] ("105a, 105b, and 105c are P-type [] well regions"); see also id. at [0044], Claim 2 ("floating gate electrode formed over the second well region, positioned between the source region and the drain region").) As can be seen from the annotated FIG. 3 of

Onoda below, Onoda's first surface is at the top surface of semiconductor substrate 100, and the source and drain regions (red) of Onoda's transistors are in that first surface. Similarly, the first active region (e.g. in N-type well region 106a) is also located at (or adjacent to) the first surface of the substrate 100 in Onoda.



(Onoda at FIG. 3 (excerpted and annotated).)

i. Dependent Claim 18 of the '842 Patent: "The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region."

126. Onoda discloses this claim. In particular, Onoda discloses a CMOS semiconductor device. CMOS devices have a complimentary pair of NMOS and

PMOS transistors. (Wolf at 368.) As such, each of the NMOS and PMOS transistors in CMOS devices contains a source, drain, gate, and channel region. (Wolf Fig. 6-8.)

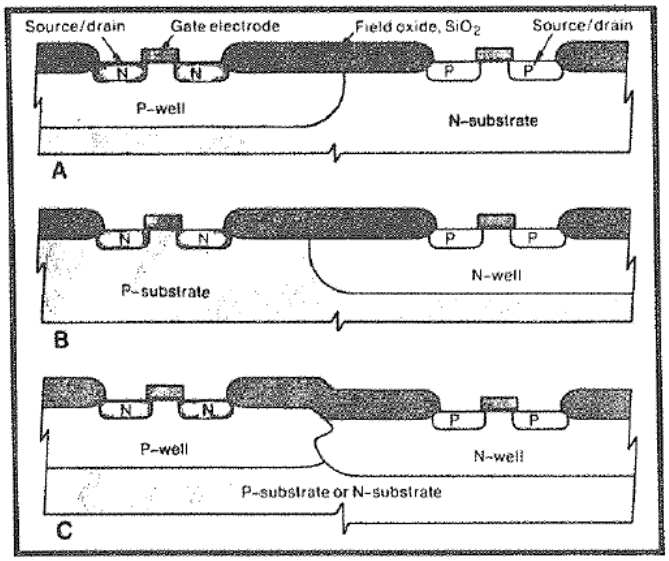


FIG. 6-8 of Wolfe

127. As of September 3, 2004, the earliest potential priority date of the '842, the CMOS technology for making CMOS devices was and still is the dominant fabrication technology in commercial semiconductor devices. (Wolf at 315 (explaining that MOS technology evolved to have CMOS as the dominant technology).) For example, flash devices have been predominantly manufactured with CMOS since the 1980s. (*Id.* at 369 (explaining that CMOS rose to dominance because of the increased functional density and speed capabilities and the reduction in power consumption for both memory and microprocessor (*i.e.*, digital logic)

chips).) A POSITA would have understood that a publication describing NMOS and PMOS transistors was directed to CMOS transistors, which employ a source, a drain, a gate, and a channel region.

128. Onoda discloses both N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the first and second active regions. (Onoda at FIGS. 2, 3 and 8, [Abstract], [0041]-[0047], [0052], Claim 2.) The transistors have a source, drain, gate, and channel regions. (Onoda at [0043] ("105a, 105b, and 105c are P-type [] well regions"); *see also id*. at [0044], Claim 2 ("floating gate electrode formed over the second well region, positioned between the source region and the drain region").) In my opinion, a POSITA would have understood these teachings to be directed to CMOS circuits with a source, a drain, a gate, and a channel region between the source and drain under the gate. Onoda further mentions that one of the objectives of the Onoda's invention "is to provide a semiconductor integrated device … with improved resistance to latch-up" (*id.* at [0006]), which a POSITA would have understood to be a problem of CMOS transistors having both NMOS and PMOS transistors in the circuits in Onoda. (*See* Wolf at 400 ("A major problem in CMOS circuits is the inherent, self-destructive phenomenon known as *latchup*.") (emphasis in original).)

129. In addition, it would have been obvious to employ the teachings of implementing both NMOS and PMOS transistors in the circuits taught by Onoda to CMOS devices. As I have noted above, CMOS was the predominant technology as of the 1980s, and Onoda explicitly describes both NMOS and PMOS transistors on a single device (FIG. 3) which are the ingredients for a CMOS device. Applying Onoda's teachings to CMOS would not only have been obvious to do, it would have been expected.

j. Independent Claim 9 of the '842 Patent

130. Onoda discloses Claim 9. Independent claim 9 is substantially similar to independent claim 1 and thus I incorporate my analysis from claim 1 here. The only difference in the claim language of claim 9 is that for both the first and second active regions, claim 9 requires that "transistors can be formed in the surface thereof" as opposed to merely "transistors can be formed" as in claim 1, and claim 9 requires the graded dopant concentration to "aid carrier movement from the surface to the substrate" as opposed to "aid carrier movement from the first surface to the second surface of the substrate" as in claim 1. The addition of "the surface" limitation is of no consequence because, the recited "the surface thereof" refers to the recited "first surface" of the substrate in light of the language and context of

Claim 9 with respect to "the surface thereof."[10] Accordingly, in "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate" in Claim 9,

[10] In my reading of "a first active region disposed ***adjacent the first surface of the substrate*** with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in ***the surface thereof***" in Claim 9, the recited "the first surface thereof" at the end should refer to the "first surface of the substrate." First, the language only recites two surfaces: the first surface and the second surface of the substrate. Second, because the language specifies the recited transistors can be formed within the first active region and because the first active region is recited to be adjacent to the first surface of the substrate, the recited first active region has no specified spatial relationship with respect to the recited second surface in Claim 9. Therefore, the recited "the surface thereof" cannot be the second surface of the substrate and should be the first surface. Similarly, in "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof," the recited "the surface thereof" refers to the recited "first surface" of the substrate.

the recited "the surface to the substrate" refers to the "first surface" to the substrate. As previously discussed for Elements [1.2] and [1.3], the transistors disclosed in Onoda are formed on the first surface of the substrate which contains the first and second active regions. Furthermore, when the graded dopant concentration of the active region aids carrier movement from the first surface to the second surface of the substrate, it is without doubt that the graded dopant concentration also aids carrier movement from the surface to the substrate. Thus, Onoda discloses and/or renders obvious Claim 9.

131. I have provided a claim listing in Appendix B showing similarities and differences between the claims.

k. Dependent Claims 12-16 of the '842 Patent

132. Dependent claims 12 through 16 recite the same claim language as dependent claims 4 through 8, except that they depend from independent claim 9 rather than from independent claim 1. For the same reasons as discussed above with regard to the dependent claims associated with claim 1, dependent claims 12-16 are disclosed and/or rendered obvious by the teachings of Onoda. (*See supra* claim 4 for claim 12, claim 5 for claim 13, claim 6 for claim 14, claim 7 for claim 15, and claim 8 for claim 16.)

133. I have provided a claim listing in Appendix B showing similarities and differences between the claims.

2. Ground II: Onoda in view of Nishizawa Renders Obvious Claims 1-2, 4-9, 12-18 of the '842 Patent

134. Onoda and Nishizawa both disclose semiconductor devices including CMOS devices and are concerned with the same technical issues caused by the minority carriers (e.g., electrons in a P-doped region) moving into the functioning circuitry.

135. Specifically, Nishizawa teaches a semiconductor device (*e.g.*, Nishizawa at Abstract ("A semiconductor device having a source region, a drain region, and a channel region which are formed in a surface portion of a semiconductor substrate.") that provides a buried region that has a graded dopant profile (annotated tan, below). (*Id.* at FIG. 16, 18:46-67, 20:25-27.)

136. Nishizawa discloses its device in Figure 32 as a "CMOS arrangement [that] may be termed an ideal circuit arrangement" (15:29-30) and that "the CMOS arrangement [of Figure 32] using the MOS transistor of the present invention is extremely excellent in its high-speed operation and low power dissipation," and can "easily" be used to form RAM (15:49-52). Thus, the structures and arrangements disclosed in Nishizawa can be used in complementary metal-oxide-semiconductor ("CMOS") technology for both logic and memory. Figures 16 and 35 illustrate

examples of a dynamic random-access memory ("DRAM") device that uses the disclosed features of Nishizawa. Figure 16 is annotated and is reproduced below. The graded dopant profile is a p+ type buried region 33 (33a in FIG. 35) that contains a relatively high impurity concentration at the "top" that progressively decreases as the buried region 33 gets closer to the p type substrate 11. *Id.* Decreasing the concentration in this manner provides an electric drift field (*id.* at 18:10-25) that allows minority carriers (electrons) in the active region to move from the surface region (blue) having the source and drain (red) to the substrate (gray). (*Id.* at 19:1-9; *see also id.* at 16:19-24 (describing the migration of carriers flowing to the surface as causing errors).)[11] Nishizawa discloses that if the electrons were allowed to "flow" to the circuit rather than down to the substrate, the circuit would not function correctly. (*Id.* at 19:1-9 (discussing how the electrons contribute to "the extinction of memory.").

[11] While the discussion cited focuses on FIG. 35, both FIGS. 35 and 16 depict DRAM cells (8:25-27, 63-65) with a buried layer. The buried layer in FIG. 16 extends under both the source and drain regions, which a POSITA would understand provides for a more effective movement of the electrons to the substrate.

FIG. 16

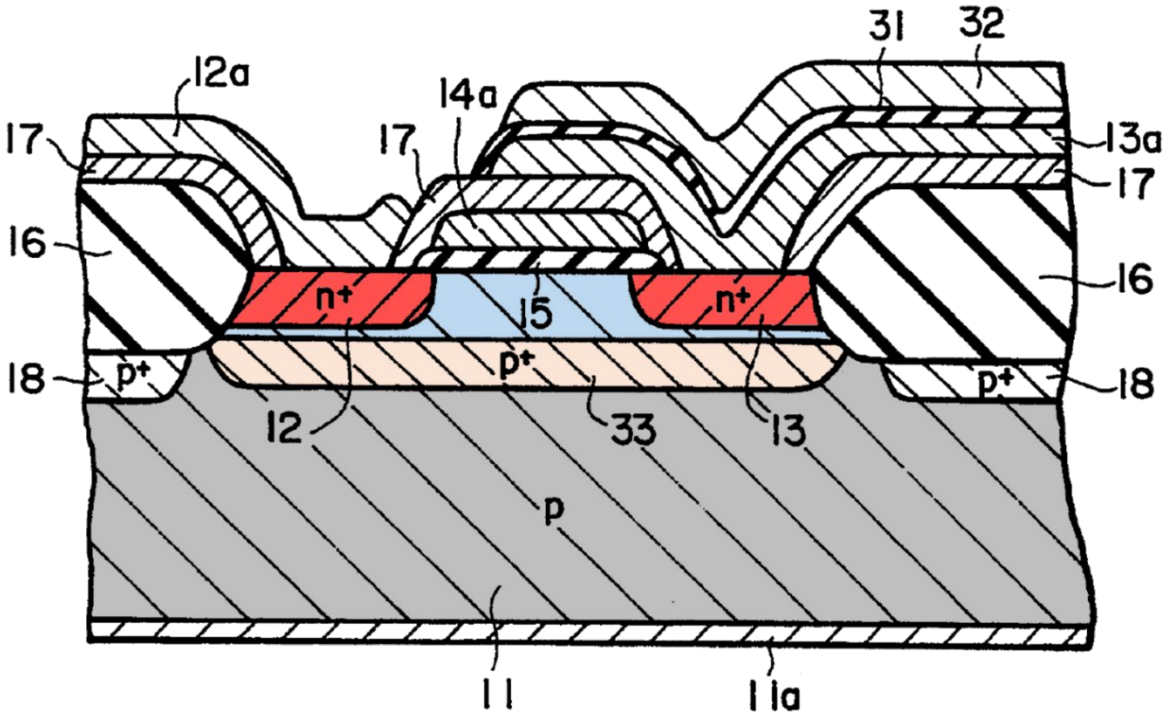


FIG. 16 of Nishizawa

137. Similarly, and as previously discussed, Onoda, discloses a semiconductor device in the form of memory devices including PMOS and NMOS transistors on one substrate with a graded dopant profile in active regions. Onoda teaches that "there is a tendency [for the devices] to become a structure wherein latch-up is inherently likely to occur due to transistors of a parasitic thyristor structure." (Onoda at [004]). Essentially, Onoda is also concerned with unwanted movement of minority carriers (e.g., electrons in a P-doped region) into the circuit and causing issues, as a POSITA would understand that issues with "latch-up" are

related to such minority carrier movement. Thus, both Nishizawa and Onoda disclose the use of a graded dopant profile to control the movement of minority carriers.

138. A POSITA would have been motivated to combine the teachings of Onoda with the teachings of Nishizawa as both prior art references focus on semiconductor devices with gradient doping such that the impurity concentration is intentionally reduced toward the substrate and effectively controls the movement of minority carriers. Nishizawa's teachings of semiconductor devices and minority carrier diffusion are well known elements which, when combined with Onoda, would yield predictable results. A POSITA would have found it obvious to apply the well-known teachings and descriptions of semiconductor devices in Nishizawa to Onoda's teachings of semiconductor devices. Nishizawa repeatedly states an "object of the present invention is to provide a semiconductor device." *See generally* Nishizawa at 7:40-63. A POSITA would have been motivated to apply Nishizawa's teachings of minority carrier diffusion based on a downward sloping dopant gradient (*e.g.*, Nishizawa at 18:46-67) to Onoda's teachings of a downward sloping dopant gradient (*e.g.*, Onoda at FIG. 11). Both Nishizawa and Onoda disclose similar structures with a graded dopant, and while Onoda generally references known issues related to minority carrier movement (*e.g.*, soft errors and latch-up), Nishizawa

makes explicit the concept of an electric field that migrates minority carriers to a substrate based on a dopant gradient (Nishizawa at 18:10-18). A POSITA would have been motivated to combine teachings of Nishizawa's explicit discussion of concepts to the structures described in Onoda as confirmation of Onoda's teachings.

139. Making this combination of teachings would have combined known elements to achieve predictable results (*e.g.*, applying Onoda's downward dopant gradient to Nishizawa's teaching of the electric fields and minority carrier drifts that a downward dopant gradient inherently creates). A POSITA would have understood that such combinations of known prior art elements would yield expected results and, moreover, would have found it obvious to try such combinations.

140. Moreover, both Nishizawa and Onoda are directed to similar devices, which face similar problems, and seek similar solutions. Both are directed to memory devices (Nishizawa at Abstract; Onoda at [0004]), and to reducing punch through. (Nishizawa at Title; Onoda at Object.)

a. Independent Claim 1 of the '842 Patent

(i) Preamble: "A semiconductor device comprising:"

141. Nishizawa teaches a semiconductor device. (Nishizawa at Abstract ("A semiconductor device having a source region, a drain region, and a channel region which are formed in a surface portion of a semiconductor substrate.") More

specifically, Nishizawa discloses both memory and CMOS semiconductor devices. (Nishizawa at 7:40-63, FIG. 32 and 15:27-52.)

(ii) Elements [1.1]-[1.4]

142. Consistent with Ground II, Onoda discloses and/or renders obvious the elements [1.1] through [1.4].

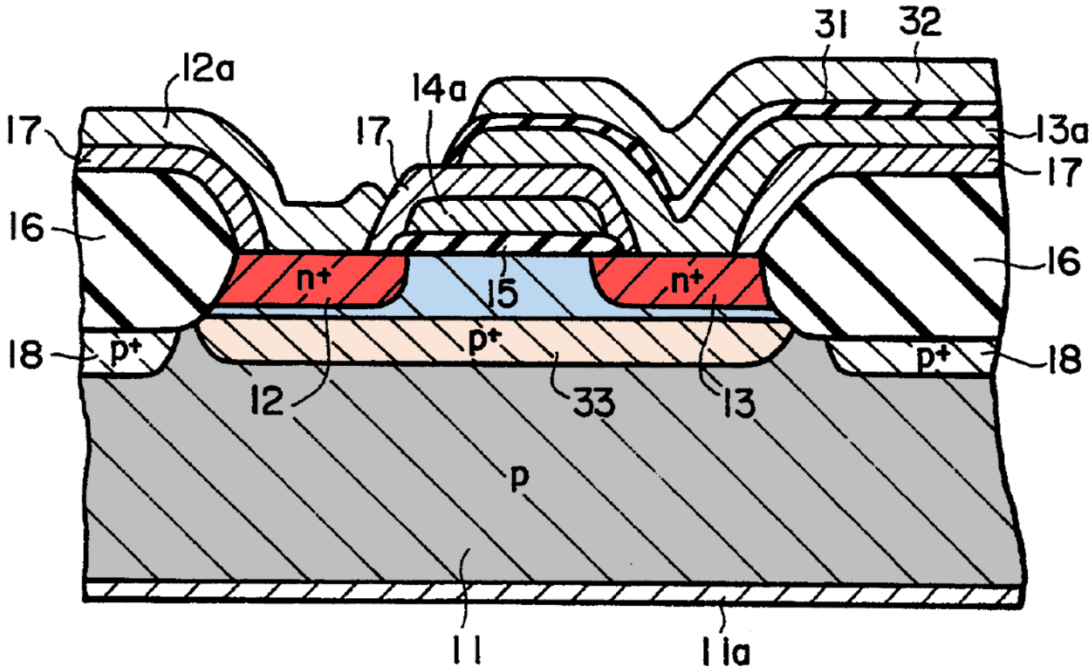
(iii) Element [1.5]: " at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

143. Onoda discloses multiple active regions whose dopant concentrations have a downward gradient which a POSITA would have recognized as providing an electric drift field to aid the movement of minority carriers from the first surface (the top of layer 102) to the second surface (the bottom of layer 101) of the substrate (substrate 100). (III.B.1.a.vi.) Nishizawa similarly discloses active regions having such graded dopant concentrations with downward gradients and provides explicit explanations on how the gradient dopant concentrations create drift electric fields to aid carrier movement. (Nishizawa at 18:10-18.)

144. FIG. 16 in Nishizawa depicts a source and drain (red, below) at the surface region (blue), where buried region 33 (tan) provides an "impurity concentration gradient … [that is] progressively decreasing toward the p type

substrate" (gray). (Nishizawa at 19:4-5; *see also id.* at 18:50-59 ("the impurity concentration of that portion of the p+ type buried region 33a located adjacent the channel region and the n+ type region 13 is set at about $1x10^{17}$ cm^{-3}, with progressively lowered concentration as the portions of the buried region 33a go progressively toward the p type substrate 11, in such manner that the impurity concentration of lowermost portion of the buried region is less than at least one third of that of the highest impurity concentration.").) The cited-to text refers to the embodiment of FIG. 35, and Nishizawa states that the discussion is likewise applicable to the structure of FIG. 16 which is illustrated. (Nishizawa at 20:23-27.)

FIG. 16



145. Nishizawa teaches "a drift electric field" that is created when there is a "difference in the degree of impurity concentration," which is used to drift minority carriers to the second surface of the substrate. (Nishizawa at 18:9-18.) To drift electrons within the p+ buried layer to the second surface of the substrate, "an impurity concentration gradient in the p+ type buried region 33a in the direction toward the p type substrate" is formed. (*Id.* at 18:35-50; *see also id.* at 18:51-67 (stating that the impurity concentration has a downward gradient to the substrate); *see also id.* at 19:1-9.)

146. Therefore, the combination of Onoda and Nishizawa discloses or renders obvious all claim elements and their combination in Claim 1.

b. Claims 2, 4-9, 12-18 of the '842 Patent

147. Claims 2, 4-9, and 12-18 are disclosed and/or rendered obvious by the Onoda-Nishizawa combination for the same reasons as discussed in Ground II and Claim 1 of Ground III. Moreover, with respect to claim 18 which requires that "The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region," Nishizawa teaches CMOS in FIG. 32 using NMOS and PMOS. (Nishizawa at FIG. 32, 7:61-63, 15:27-52)

3. Ground I: Kawagoe Renders Obvious Claims 1, 2, 4-9, and 12-18 of the '842 Patent

148. Kawagoe is issued from U.S. Patent Application No. 08/934,774 which is a divisional application of U.S. Patent Application No. 08/508,483, filed Jul. 28, 1995 that further claims priorities from two Japanese priority documents 6-176872 dated Jul. 28, 1994 and 6-265529 dated Oct. 28, 1994. (Kawagoe at Cover Page.)

149. Kawagoe teaches a semiconductor device whose surface region (its epitaxial layer) has its "impurity concentration gradually lowered depthwise of said epitaxial layer." (Kawagoe at Abstract.) The "gradient … is gradually lowered in the depthwise direction from the surface of the epitaxial layer … so that the influence

to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient." (*Id.* at 16:3-8.) In particular, Kawagoe discloses that a graded dopant concentration of a p doped well can be designed to aid carrier movement of electrons from the top surface of the substrate to the substrate by attracting the electrons to the substrate. Kawagoe at 15:62-16:40; FIGS. 16 and 17.

150. As explained below, Kawagoe discloses the features and combinations of Claims 1, 2, 4-9, and 12-18 of the '842 Patent and represents the public knowledge of the claimed features around 1994, approximately one decade prior the patent owner's purported invention in 2004.

a. Independent Claim 1 of the '842 Patent

(i) Preamble: "A semiconductor device comprising:"

151. Kawagoe discloses a semiconductor device. (*See, e.g.,* Kawagoe at 1:13-17 ("The present invention relates to … a process for manufacturing a semiconductor integrated circuit device, and a semiconductor integrated circuit device.") and 2:30-4:57 ("The Summary of Present Invention"). Kawagoe teaches that the disclosed semiconductor integrated circuit devices (including MOSFET circuits and various VLSI circuits) can be used in various applications, including

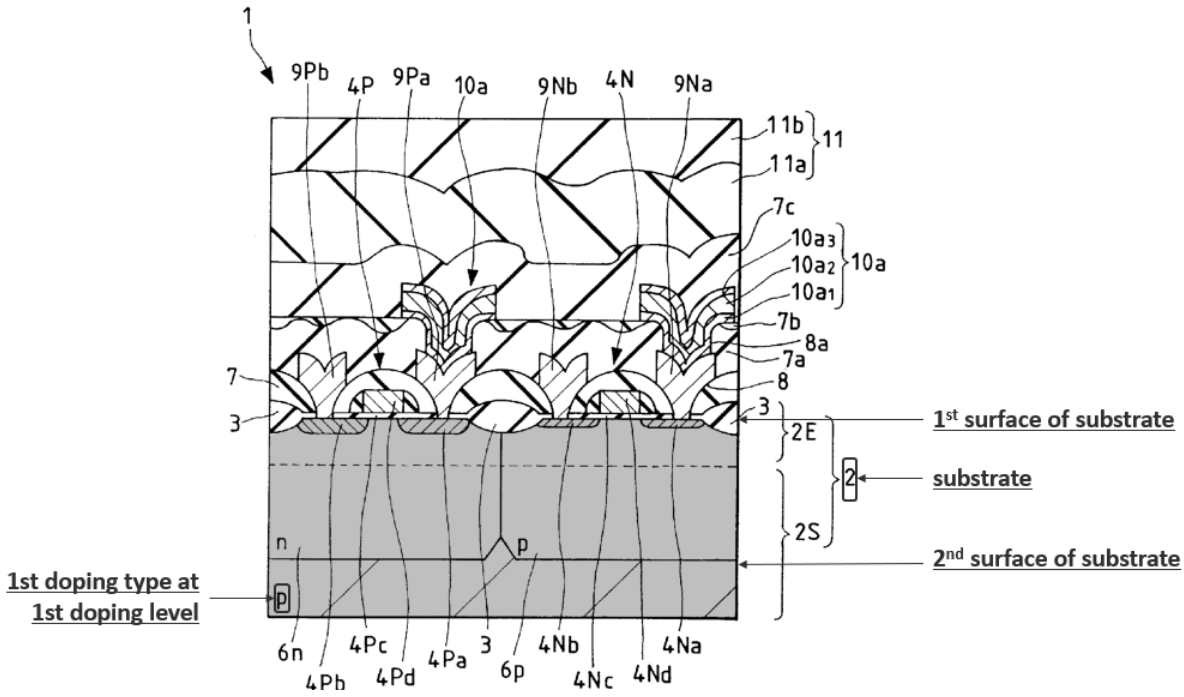
memory devices such as DRAM, SRAM, ROM, and semiconductor devices with logic circuits such as the so-called "microcomputer" (*id.* at 24:21-31).

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

152. Kawagoe discloses this element. First, Kawagoe discloses a substrate 2 that with doping of the p type as a first doping type at a first doping level.

153. As annotated FIG. 16 in Kawagoe is reproduced below to highlight the substrate 2 that includes a p-type Si single crystal substrate body 2S and a p-type Si single crystal epitaxial layer 2E. (Kawagoe at 14:61-15:12 ("The semiconductor substrate body 2S is doped with a p-type impurity such as boron in a concentration of about $1.5xl0^{15}$ atoms/cm^3.").) As disclosed by Kawagoe, the "semiconductor substrate 2" of the embodiment of FIG. 16 is a substrate (*Id.* at 15:11, 15:26.) The first and second surface of the substrate are also annotated below where the first surface is the top surface of the p-type Si single crystal epitaxial layer 2E of the substrate 2 and the second surface is the bottom surface of the n-well 6n and the p-well 6p. Alternatively, the bottom surface of the body substrate 2S of the substrate 2 in Kawagoe also discloses or render obvious the claimed second surface in Element [1.1] as further explained below in my analysis of Element [1.5].

FIG. 16



Substrate in FIG. 16 of Kawagoe (Annotated)

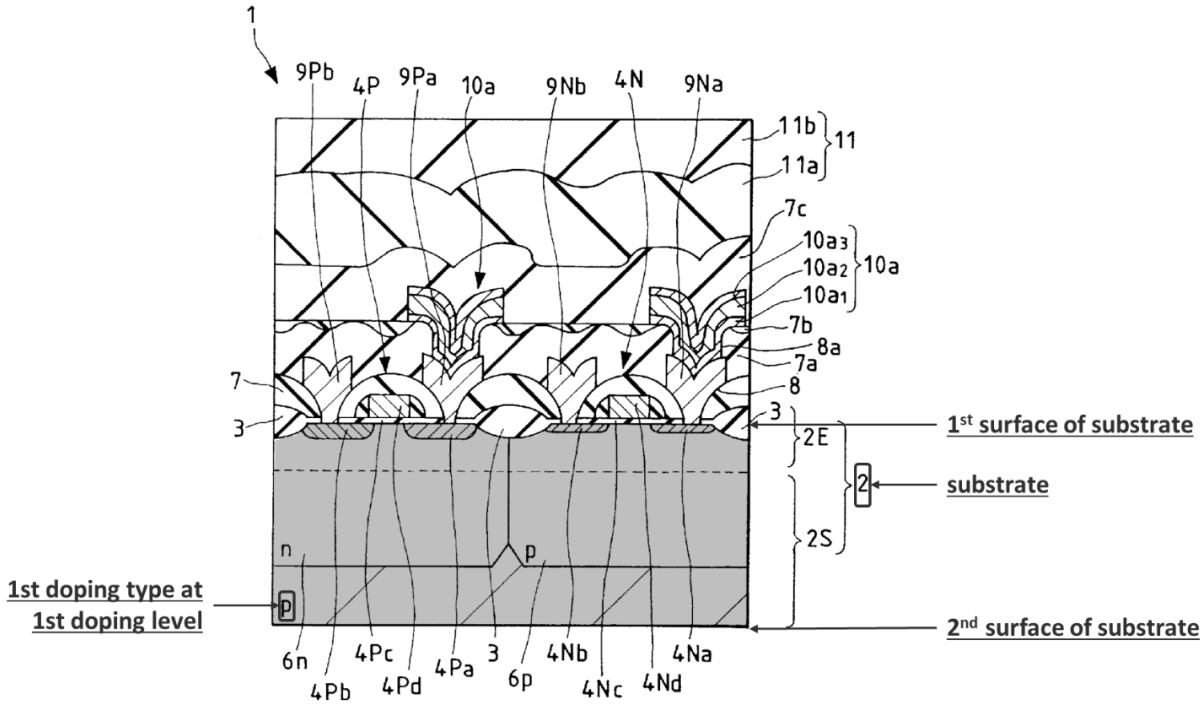
154. The embodiment of FIG. 16 shows an example of the final device of Kawagoe, with several insulating layers and connectors on top, *e.g.*, insulating films 3, 7, 11 and electrodes 10. (Kawagoe at 10:34-39, 18:1-8.). A POSITA would understand that those layers would not be part of the substrate.

155. Kawagoe's substrate 2 has a first doping type at a first doping level, for instance p-type doping in the p-type Si single crystal substrate body 2S. Kawagoe at 14:61-15:12 ("The semiconductor substrate body 2S is doped with a p-type impurity such as boron in a concentration of about 1.5×10^{15} atoms/cm^3.") Kawagoe discloses a "relatively lightly doped semiconductor substrate body 2S of the semiconductor

integrated circuit device 1 [] is made of a p-type Si single crystal" and "doped with a p-type impurity such as boron." (*Id.* at 14:61-67.) Kawagoe's substrate also includes epitaxial layer 2E that is made up of a "p-type Si" over the substrate body 2S and "doped with a p-type impurity." (*Id.* at 15:1-6) Combined, substrate body 2S and epitaxial layer 2E form an epitaxially integrated substrate as the claimed substrate.

156. Kawagoe's first surface and second surfaces of the substrate 2 exist at the top of the epitaxial layer 2E and the bottom of the n-well 6n and p-well 6p, respectively. The epitaxial layer 2Eis used to form multiple active regions with source and drain regions and channel regions formed within it to form transistors (discussed in more detail with respect to Element [1.3]). (Kawagoe at 8:66-9:6; *see also id*. at 15:26-32.) Kawagoes' active regions with source and drain regions and channel regions are located at or near the top surface of the epitaxial layer 2E of the substrate 2 which is mapped to the claimed first surface of the substrate. Moreover, the identification of the interfaces is merely exemplary. As I have noted, a POSITA would further understand that there exists more surface, for instance the bottom of the substrate would likely provide a second surface with the top surface providing a "second surface." This is depicted below.

FIG. 16



(Kawagoe at FIG. 16 (Annotated).)

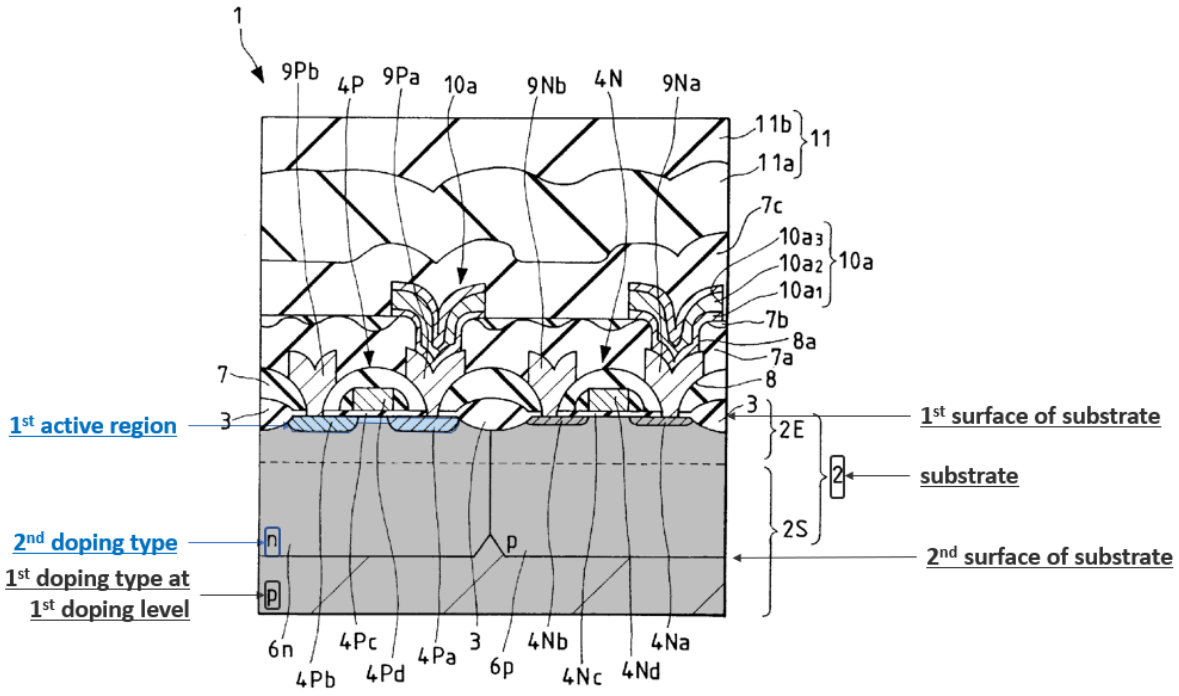
157. Kawagoe's substrate is consistent with Patent Owner's proposed claim construction in district court, where Patent Owner stated that a substrate is "an underlying layer." Consistent with the plain and ordinary meaning, the epitaxial layer 2E is epitaxially grown on the upper surface of the substrate body 2S so that the epitaxial layer 2E and the substrate body 2S constitute an epitaxially integrated single structure with the same single crystal silicon structure and the same p doping. (Kawagoe at FIG. 1 and 6:60-7:3.)

(iii) Element [1.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

158. Kawagoe discloses this element. In particular, Kawagoe teaches a first active region adjacent to the first surface of the substrate.

159. In Kawagoe, the first active region for PMOS transistor 4P exists at the top of n-well 6n and includes the source and the drain of PMOS transistor 4P and the p-channel formed between the source and drain. (Kawagoe at 8:46-9:6, 9:41-58, 15:26-36, 21:43-47, 26:31-36, 27:27-32, 29:9-14 and 31-37, 30:16-21, 39-44 and 62-67, 31:17-22 and 31:13-18.) The first active region is annotated below, marked by a blue box within an n type doping region 6n for its channel region (on the left-hand side) that is opposite in conductivity to the first doping type (*i.e.*, p-type) of the substrate 2 with layers 2E and 2S. (Kawagoe at 14:61-15:12, 15:7-12, and 15:30-43.)

FIG. 16



First Active Regions in FIG. 16 of Kawagoe (Annotated)

160. The first active region in FIG. 16 of Kawagoe marked by the blue box is disposed adjacent to the first surface of the substrate 2 (the top surface of the layer 2E and in which transistors can be formed, e.g., the pMOS 4P which has drain and source regions and a channel therebetween). Kawagoe at 8:46-9:6, 9:41-58, 15:26-36, 21:43-47, 26:31-36, 27:27-32, 29:9-14 and 31-37, 30:16-21, 39-44 and 62-67, 31:17-22 and 31:13-18. See also Kawagoe at 9:41-54 ("the pMOS 4P is composed of: a pair of semiconductor regions 4Pa and 4Pb formed over the epitaxial layer 2E and apart from each other; a gate insulating film 4Pc formed over the epitaxial layer

2E; and a gate electrode 4Pd formed over the gate insulating film 4Pc.").) and "The semiconductor regions 4Pa and 4Pb are regions for forming the source-drain regions of the pMOS 4P.") and 18:9-38.

161. As depicted above, the first active region is formed within the n-well 6n. (Id. at 15:26-28.). A POSITA would understand that prior to the formation of the source and drain (which would be p-type), that the active region would be n-type. And, after doping of the source and drain to be p-type, other portions of the region would remain as n-type. This is depicted in FIG. 22 and then in FIG. 23, where the paired semiconductor regions 4Pa and 4Pb are implanted onto the n-well. (Kawagoe at 18:18-23.) A POSITA would have understood that the active region's channel region would remain n-type for the PMOS even if the source and drain are doped to be p-type (and the inverse is true for NMOS, *i.e.*, the channel would remain p-type even if the source and drain are doped to be n-type).

FIG. 22

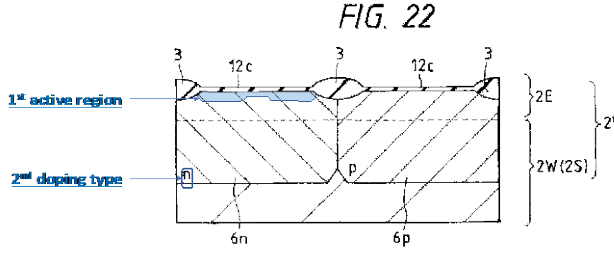
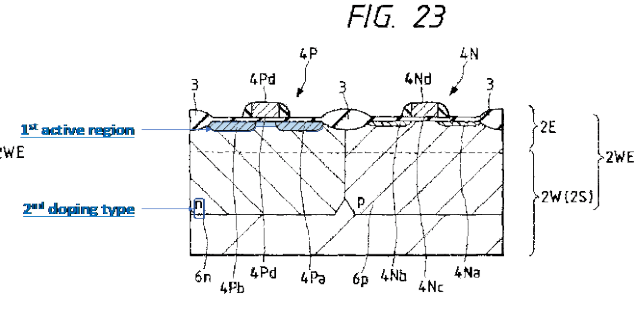
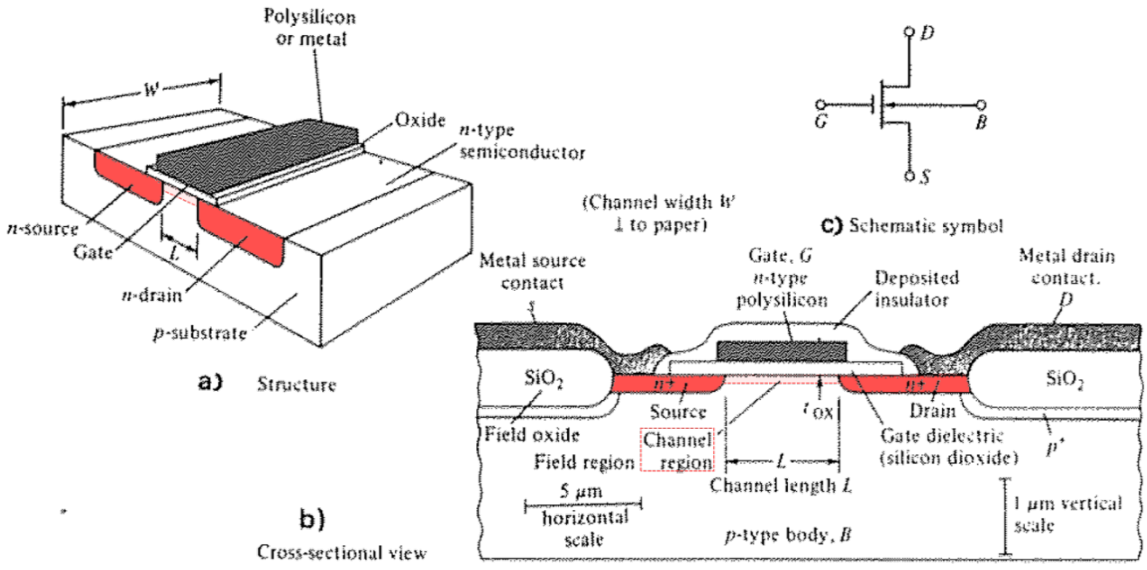


FIG. 23



162. A POSITA would have understood that the above-annotated "active region" comprises a source, a drain and a channel between the source and drain,

which together would provide for conductivity and thusly be an active region. Kawagoe at 8:46-9:6, 9:41-58, 15:26-36, 21:43-47, 26:31-36, 27:27-32, 29:9-14 and 31-37, 30:16-21, 39-44 and 62-67, 31:17-22 and 31:13-18. This understanding of source, gate, drain, and transistor operation is confirmed via Wolf and Tauber, Silicon Processing For The VLSI Era, Vol 1, Lattice Press (1986), which depicts the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions." A POSITA would have understood that the active region's channel region would remain n-type for the PMOS even if the source and drain are doped to be p-type (and the inverse is true for NMOS, *i.e.*, the channel would remain p-type even if the source and drain are doped to be n-type).



163. The '842 Patent describes adjacent to mean regions that are next to each other, and makes no distinction between a lateral or vertical adjacency. ('842 Patent

at 3:36-39; *see also id.* at FIG. 5(b).). A POSITA would moreover understand "adjacent" to encompasses a vertical adjacency because the claims describe "adjacent [to] the first surface of the substrate," which would be understood to be below the surface.

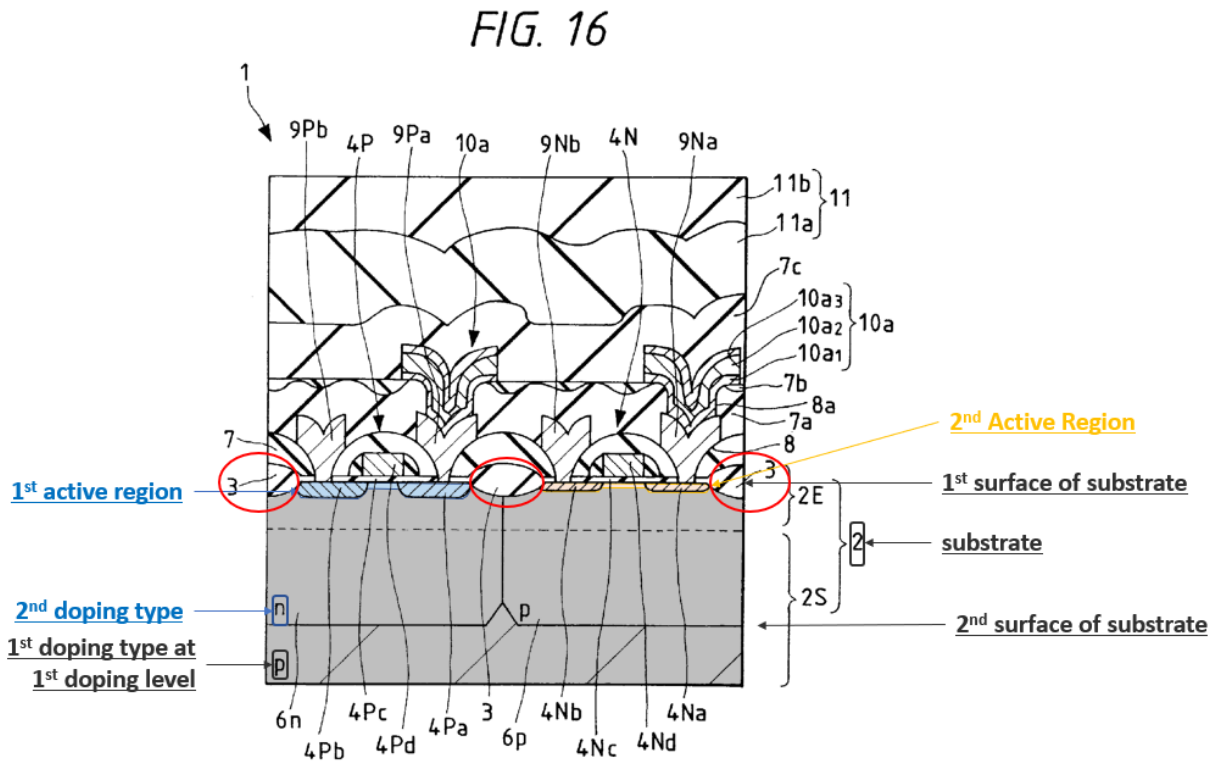
164. Furthermore, when discussing the term "active region … within which transistors can be formed," Patent Owner argued, "this term means exactly what it says: an active region (*i.e.*, a doped region at the surface of a semiconductor device) where a transistor can be formed." PO Res. Br. at 31. As an example, Patent Owner stated "that an active region includes a source and drain (two doped regions at the surface of a semiconductor device where a transistor can be formed)" and that "[w]hile the active region may be 'located within' or 'surrounded by' the well region, Dr. Rao made it clear that the active region is where the transistors are built or may be built." PO. Br. at 31.

165. A POSITA would understand that Patent Owner's claimed first active region encompasses the source, drain, and channel region as these are doped regions where the transistors are built. (PO. Br. at 32 ("a doped region at the surface of a semiconductor device where a transistor can be built").) Kawagoe's teachings associated with Figure 16 provide such a first active region with a transistor pMOS 4P at the first surface (top surface) of the substrate 2 over an n-doped well that is

opposite of the first doping (p-type) of the substrate 2 and within which transistors (e.g. the transistor PMOS 4P) can be, and indeed are, built.

(iv) Element [1.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed,"

166. Kawagoe discloses this element. Kawagoe's Figure 16, reproduced below, discloses a p-well 6p that contains a second active region (tan) separate from, and adjacent to, the first active region (blue) in the area of the n-well 6n. (Kawagoe at 15:26-28.) "The p-well 6p is doped with a p-type impurity such as boron" and "formed with the nMOS 4N" transistor. (*Id.* at 15:28-30.) Kawagoe discloses that the semiconductor regions 4Na and 4Nb are regions for forming the source-drain regions of the NMOS 4N transistor and a channel between the source and drain regions (*Id.* at 8:55-9:6 and 18:9-38; see also *id.* at 8:46-9:6, 9:41-58, 15:26-36, 21:43-47, 26:31-36, 27:27-32, 29:9-14 and 31-37, 30:16-21, 39-44 and 62-67, 31:17-22 and 31:13-18.)



Second Active Region in FIG. 16 of Kawagoe (Annotated)

167. As discussed above for the first active region, a POSITA would understand that the Patent Owner's claimed second active region encompasses the source, channel region, and drain as these are doped regions where the transistors are built. (PO Res. Br. at 32 ("a doped region at the surface of a semiconductor device where a transistor can be built").) Kawagoe's Figure 16 provides such a second active region with NMOS 4N transistor at the first surface (top surface) of the substrate 2 over a p-doped well that is adjacent to the first active region and within which transistors can be, and indeed are, built (e.g., the transistor NMOS 4N transistor).

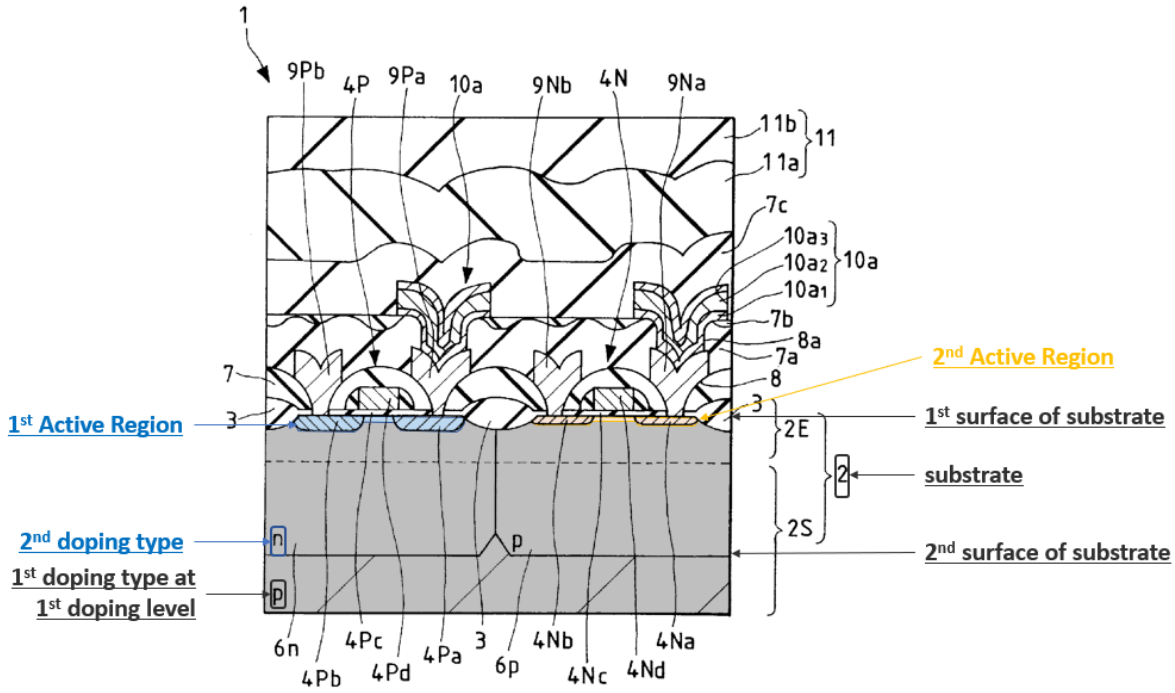
168. Further, the ’842 Patent describes adjacent to mean regions that are next to each other, and makes no distinction between a lateral or vertical adjacency. (’842 Patent at 3:36-39; *see also id.* at FIG. 5(b).). A POSITA would moreover understand “adjacent” to encompasses a lateral adjacency because the claims describe two active regions that are adjacent to each other. Furthermore, as I have discussed in preceding portions of my declaration at ¶¶ 35-45, a POSITA would have found it obvious to include multiple active regions in a single well (if that we argued to be a requirement of the claim, which it is not). Moreover, a POSITA would have been motivated to do so in light of Kawagoe’s own teachings, which provide multiple semiconductor regions (e.g., 20b, 20a, 4n) within the p-well 6p of FIG. 28 that illustrates a memory cell MC1 constructed of a single MOSFET, with its active region formed within the same p-well 6p3 as the NMOS transistor 4N. (Kawagoe at FIG. 28, 22:39-44, 22:51-59.)

(v) Element [1.4]: “transistors formed in at least one of the first active region or second active region; and”

169. Kawagoe discloses this element. In Kawagoe, transistors are formed in the first active region or second active region as discussed above in Elements [1.2] and [1.3], where the first active region contains pMOS 4P transistor as an example

of such transistors and the second active region contains NMOS 4N transistor as an example of such transistors.

FIG. 16



PMOS and NMOS Transistors in FIG. 16 of Kawagoe (Annotated)

170. To the extent this limitation requires multiple transistors in the first active region or the second active region, it would have been obvious to add multiple transistors into the same active region. As discussed in the Overview of Technical Concepts, forming multiple transistors was well known and a POSITA would have understood that Figure 16 is a 2-D cross section of the wells and active regions and that both extend into and out of the page in real world applications. (II.C) When the

plane is adjusted to view the wells from the top of the cell or device, a POSITA would understand that multiple transistors can be built (and typically were built before September 2004 and are built today) in the same well region and thus active region.

(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

171. Kawagoe discloses this element. In particular, Kawagoe's disclosure in FIGS. 16 and 17 teaches that Kawagoe's first and second active regions have at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

172. FIG. 16 is reproduced below with further annotations to identify the n-well 6n and adjacent p-well 6p in a dashed red and an arrowed line in purple to represent the graded dopant concentration which is within the second active region (and goes throughout the p-well). A POSITA would further understand that the n-well likewise has a graded dopant concentration.

FIG. 16

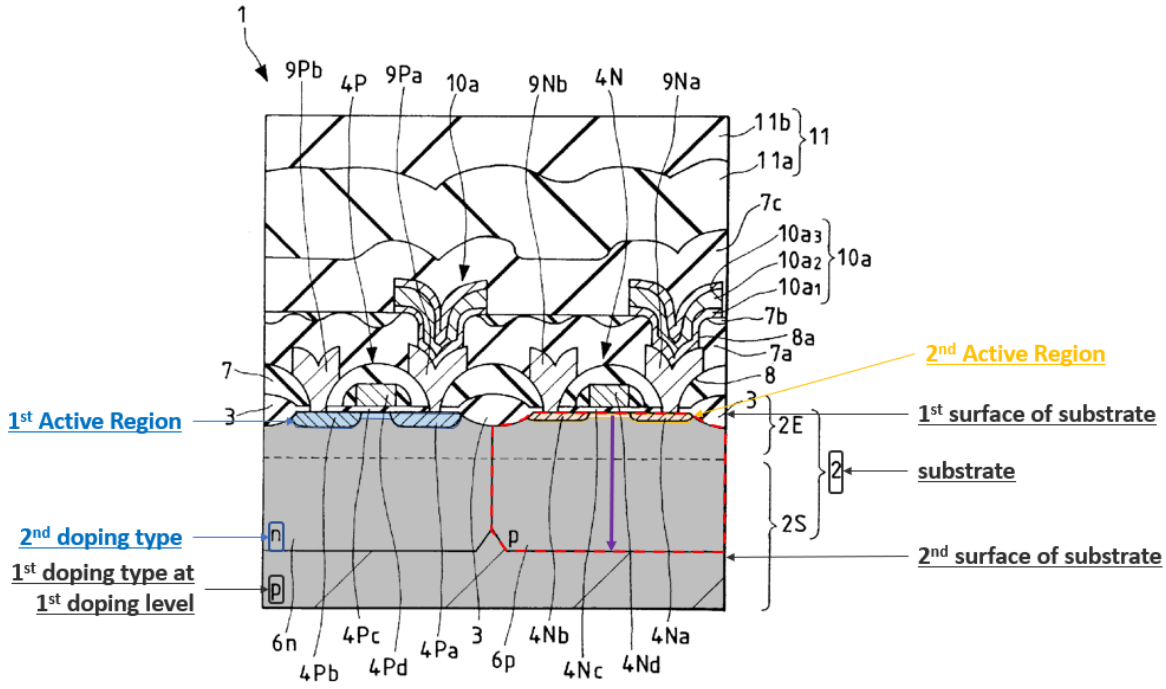
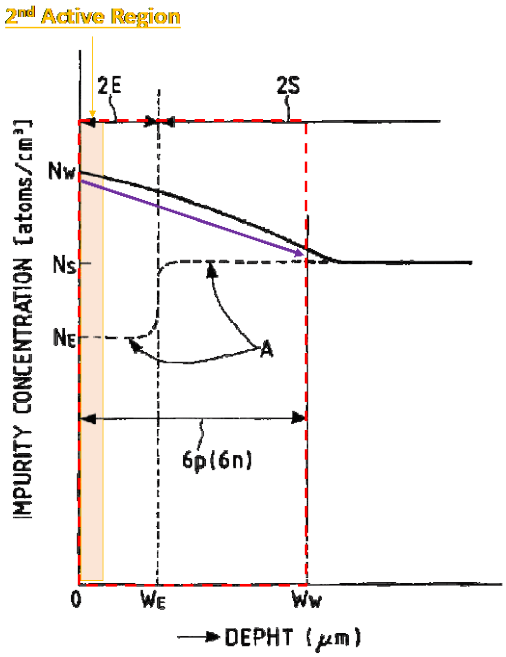


FIG. 16 of Kawagoe (Annotated)

Annotated First and Second Active Regions in FIG. 16 of Kawagoe to Indicate Correspondence to Graded Dopant Concentration in FIG. 17

FIG. 17



Annotated Graded Dopant Concentration in Pink in Second Active Region in FIG. 17 of Kawagoe

173. As can be seen in FIGs. 16 and 17, the epitaxial layer 2E has a thickness W_E from the surface of the epitaxial layer 2E part of the substrate 2 and that the n-well 6n and the p-well 6p have a depth W_w from the top surface of the epitaxial layer 2E of the substrate 2. (Kawagoe at 15:18-36.)

174. Kawagoe in FIG. 17 discloses an example of the graded dopant (impurity) concentration profile with a decreasing dopant concentration at different depths from the top surface of the substrate 2 of the Kawagoe device in FIG. 16. In particular, Kawagoe discloses that the impurity concentration of the p-well 6p (the

graded dopant concentration curve with a maximum concentration of N_w at the top surface in FIG. 17) is designed to aid carrier movement of electrons from the top surface of the layer 2E of the substrate 2 by using the P-type graded dope concentration to attract the minority charge carrier electrons away from the top surface to the bottom of the p-well 6p towards the substrate body 2S. Kawagoe at 15:62-16:40.

175. In FIG. 16, the n-well 6n employs N-type doping so the majority charge carriers are electrons and the minority charge carriers are holes. As I analyzed for n-wells associated with PMOS transistors and p-wells associated with NMOS transistors with respect to Onoda above, a decreasing dopant concentration for the n dopant is needed in the n-well 6n to move minority carrier holes away from the top surface to the bottom of the n-well 6n towards the substrate body 2S. FIG. 17 illustrates a nearly identical decreasing dopant concentration for the N dopant.

176. The following text is reproduced from Kawagoe at 15:62-16:15:

> "Incidentally, in the present embodiment 4, the aforementioned p-well 6p and n-well 6n are formed to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S, as shown in FIGS. 16 and 17, and the p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the

principal surface (having an impurity concentration N_W) of the epitaxial layer 2E. Thus, the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p. The impurity concentration N_W in the principal surface of the epitaxial layer 2E of the p-well 6p and the n-well 6n is at about 6×10^{16} atoms/cm^3, so that the impurity concentration of the p-well 6p and the n-well 6n is at 5×10^{15} to 6×10^{16} atoms/cm^3."

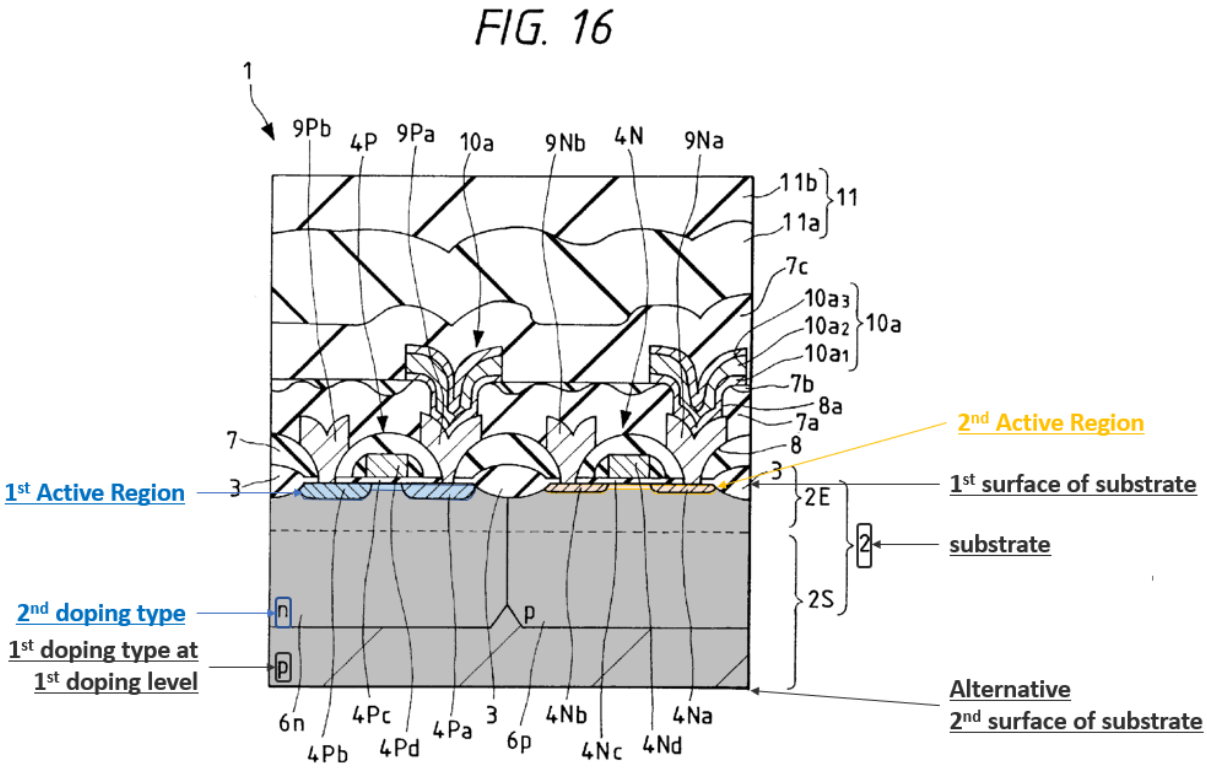
177. The first and second active regions (annotated in blue and tan) are at the first surface of the semiconductor device (*see, e.g.,* Kawagoe at 15:62-16:15) and are formed into the semiconductor device so that carriers (*e.g.*, minority carriers, *i.e.*, electrons in the p-well 6p and holes in the n-well 6n) are attracted to the substrate to reduce errors. (*Id.*) The depthwise gradient extends from the first surface of the semiconductor device toward the substrate body 2S (*id.* at 16:2-15 and 15:26-36). As depicted in annotated FIGS. 16 and 17 above, Kawagoe's second active region

is disposed on the top portion of the p-well 6p. This portion of the second active region has a graded dopant concentration. (Kawagoe 15:62-16:40; *see also id.* at 15:26-36, 17:11-21; *see also id.* at 1:59-2:5, 2:20-23, 15:62-16:15.) The gradient of this graded dopant concentration is represented by a portion of the purple arrow which is also the direction of the electron carrier movement caused by a drift electric field associated with the graded dopant concentration in the second active region which is at the top of the p-well 6p. Notably, Kawagoe specifically teaches that "the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p" (*Id*. at 6:7-11). Therefore, Kawagoe teaches moving electrons through the bottom surface (the "second surface of the substrate") of the p-well 6p into the substrate body 2S. Similarly, Kawagoe's graded N dopant concentration in the n-well 6n is designed to move its minority charge carrier holes through the bottom surface (the "second surface of the substrate") of the n-well 6n into the substrate body 2S.

178. In light of the above teachings in Kawagoe, this portion of the graded dopant profile in the second active region in Kawagoe discloses the claimed "least one of the first and second active regions having at least one graded dopant

concentration to aid carrier movement from the first surface to the second surface of the substrate."

179. In the above analyses of Kawagoe, the bottom surface of the p-well 6p and n-well 6n is mapped to the claimed "second surface of the substrate." Alternatively, the claimed second surface may be mapped to the bottom surface of the body substrate 2S of the substrate 2 in Kawagoe. This alternative mapping is illustrated below, another annotated FIG. 16 of Kawagoe.



Alternative Mapping of FIG. 16 of Kawagoe to Claimed Second Surface of Substrate (Annotated)

180. For reasons similar to my analyses of Onoda with respect to mapping different surfaces within a substrate in Onoda to the claimed second surface of the substrate and the claimed feature of "to aid carrier movement from the first surface to the second surface of the substrate" for Element [1.5] in Ground II, my analysis of all claims in the four patents in this declaration remains the same for this alternative mapping of the disclosure in Kawagoe to the claimed "second surface" of the substrate.

181. In light of teachings in Onoda and above explanations, Onoda discloses or renders obvious all claim elements and their combination of Claim 1 of the '842 Patent.

b. Dependent Claim 2 of the '842 Patent: "The semiconductor device of claim 1, wherein the substrate is a p-type substrate."

182. Kawagoe discloses this element. Kawagoe's layers 2E and 2S are part of the semiconductor wafer prior to forming the diffusion layer. (See Kawagoe at FIGS. 20 and 21.) The substrate body 2S is made of a p-type Si single crystal that is initially formed with a p type impurity such as boron and the epitaxial layer 2E is made up of a p-type Si single crystal. (*Id.* at 14:61-15:16.) The layers contain the same p-type doping, thus disclosing this element.

c. Dependent Claim 4 of the '842 Patent: " The semiconductor device of claim 1 wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

183. Kawagoe discloses this element. Kawagoe's substrate 2 has an epitaxial silicon layer 2E on top of a nonepitaxial silicon substrate body 2S. See above analysis of Element [1.1] and the above annotated FIG. 16. "The epitaxial layer 2E made of a p^--type Si single crystal or the like is formed over a principal surface of the semiconductor substrate body 2S." (*Id.* at 15:1-3.) A POSITA would understand that 2S is a nonepitaxial substrate.

d. Dependent Claim 5 of the '842 Patent: "The semiconductor device of claim 1 wherein the first active region and second active region contain one of either p-channel and n-channel devices."

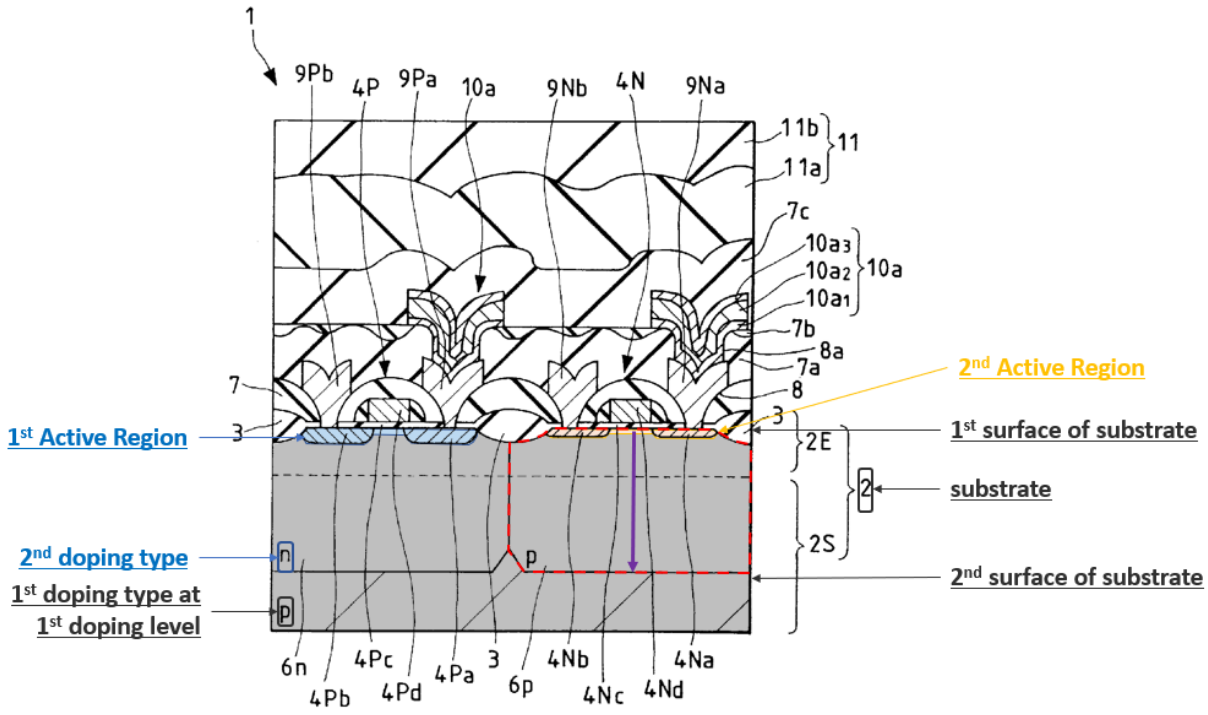
184. Kawagoe discloses this element. As previously discussed (Elements [1.2] and [1.3]), Kawagoe's first active region contains a PMOS transistor 4P and Kawagoe's second active region contains an NMOS transistor 4N. Kawagoe at 8:46-9:6, 9:41-58, 15:26-36, 21:43-47, 26:31-36, 27:27-32, 29:9-14 and 31-37, 30:16-21, 39-44 and 62-67, 31:17-22 and 31:13-18. It was well known, and Kawagoe explicitly teaches, that describing the device as either a p-channel or n-channel device is merely a matter of naming convention. The full name of the transistors is "n-channel MOSFET (as will be shortly referred to as 'nMOS') 4N and

[] p-channel MOSFET (as will be shortly referred to as 'pMOS') 4P." (Kawagoe at 8:46-50.)

e. Dependent Claim 6 of the '842 Patent: "The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each has a graded dopant."

185. Kawagoe discloses this element. First, Kawagoe discloses a first active region and a second active region containing either p-channel and n-channel devices in n-wells or p-wells, respectively. As previously discussed with respect to Elements [1.2] and [1.3], Kawagoe's first active region contains PMOS transistor 4P that is located at the top of n-well 6n and Kawagoe's second active region contains NMOS transistor 4N which is located at the top of p-well 6p. See annotated FIG. 16 below. This structure is the foundation of semiconductor devices which take advantage of the electrical characteristics of the opposing doping types to operate.

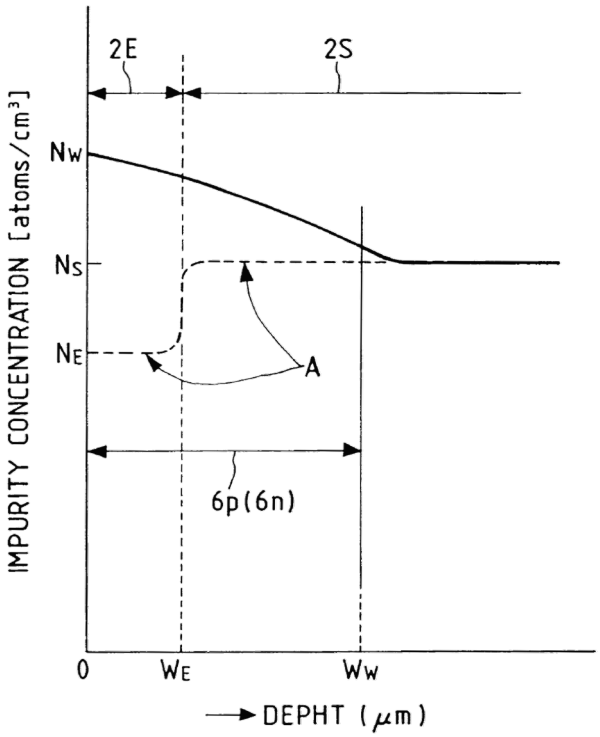
FIG. 16



186. Second, as discussed in Element [1.5], the n-well 6n and p-well 6p in Kawagoe each contain a graded dopant concentration. The p-wells and n-wells comprise the active regions, where the "impurity concentrations [of those wells are] gradually lowered in the depthwise direction from the principal surface … of the epitaxial layer 2E." (Kawagoe at 15:66-16:2.) The depthwise gradient extends from the first surface of the semiconductor device toward the bottom of the substrate (the second surface) (*id.* at 16:2-15) and is formed by diffusing impurities in the upper portion of the semiconductor substrate. (*Id.* at 15:26-36). Kawagoe's graded concentration of dopants is depicted in FIG. 17 (annotated and reproduced below)

where the dopant concentrations of both p-well 6p and n-well 6n are represented by the graded dopant concentration profile (that extends from the surface of 2E (the first surface) through the p and n-wells (6p and 6n)), and into an upper portion of the substrate body 2S below the p and n-wells 6p and 6n (i.e., below depth W_w in FIG. 17).

FIG. 17



f. Dependent Claim 7 of the '842 Patent: "The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

187. Kawagoe discloses this element. In particular, Kawagoe discloses the claimed active regions are each separated by at an isolation region in the form of a field insulating film region 3 that is located between each active region. (*Id.* at 8:46-54 ("The element forming region, as enclosed by the field insulating film 3, is formed for example with an n-channel MOSFET (as will be shortly referred to as 'nMOS') 4N and [] p-channel MOSFET (as will be shortly referred to as 'pMOS') 4P.").) FIG. 16 in Kawagoe is annotated to show field insulating film regions 3 in red near the top surface of the substrate 2. Notably, the field insulating film region 3 located between the first and second active regions in FIG. 16 is an isolation region that separates the first active region and second active region.

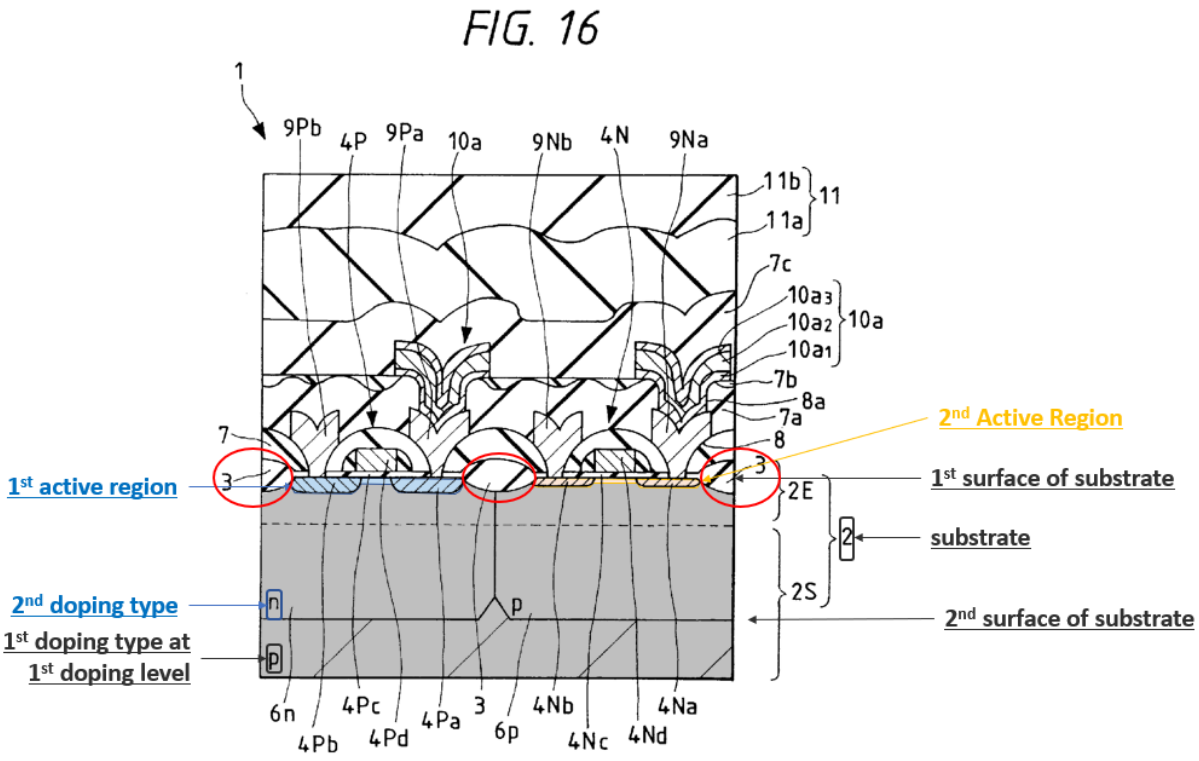


FIG. 16 of Kawagoe Annotated to Show Field Insulating Film Regions 3

188. A POSITA would have understood that the insulating film provides the functionality of creating an isolation region that electrically isolates the active regions so they do not interfere with one another. Thus, this element is disclosed.

g. Dependent Claim 8 of the '842 Patent: "The semiconductor device of claim 1 wherein the graded dopant is fabricated with an ion implantation process.

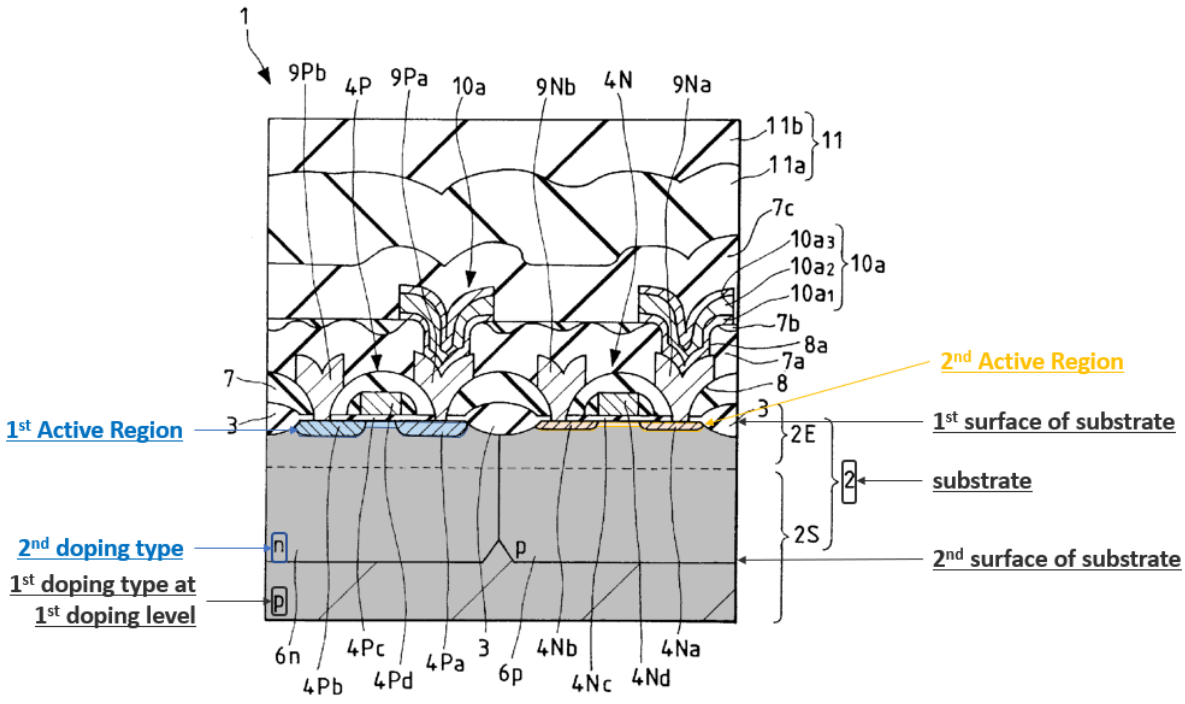
189. Kawagoe discloses this element. Kawagoe teaches a diffusion layer that creates the n and p-wells and extends into the substrate. As depicted in FIGS. 16 and 17, the diffusion layer is "formed to extend from the surface of the epitaxial layer 2E to the upper portion of the substrate body … [where its] impurity

concentration[] [is] gradually lowered in the depthwise direction." (Kawagoe at 15:62-16:4.) The layers of the wafer are originally formed via "ion implantation" (id. at 17:32-49) and are annealed to extend the diffusion. (*Id*. at 17:50-54.)

h. Dependent Claim 17 of the '842 Patent: "The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

190. Kawagoe discloses this element. As previously discussed with respect to Elements [1.2] and [1.3], Kawagoe's active regions are located on the first surface of the substrate. As shown in Figure 16 below, Kawagoe's first and second active regions are both adjacent to the first surface of the substrate 2as they are located at the top (but inside) of epitaxial layer 2E of the substrate 2.

FIG. 16



i. Dependent Claim 18 of the '842 Patent: "The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region."

191. Kawagoe discloses this element. (*Id.* at 8:46-54 ("The element forming region, as enclosed by the field insulating film 3, is formed for example with an n-channel MOSFET (as will be shortly referred to as 'nMOS') 4N and [] p-channel MOSFET (as will be shortly referred to as 'pMOS') 4P, and these nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit.").) 4N and 4P are CMOS transistors and they have the claimed source and drain (*id.* at 8:66-67 ("semiconductor regions 4Na and 4Nb are regions for forming

the source-drain regions of the nMOS 4N"); 9:47-48 ("semiconductor regions 4Pa and 4Pb are regions for forming the source-drain regions of the pMOS 4P")), the claimed gate (*id.* at 9:19 (gate electrode 4Nd); 10:1 (gate electrode 4Pd)), and a channel region which a POSITA would understand is in the well region between the source-drain regions.

j. Independent Claim 9 of the '842 Patent

192. Independent claim 9 is substantially similar to independent claim 1 and thus I incorporate my analysis from claim 1 here. The only difference in the claim language of claim 9 is that for both the first and second active regions, claim 9 requires that "transistors can be formed in the surface thereof" as opposed to merely "transistors can be formed" as in claim 1, and Claim 9 requires the graded dopant concentration to "aid carrier movement from the surface to the substrate" as opposed to "aid carrier movement from the first surface to the second surface of the substrate" as in Claim 1. The addition of "the surface" limitation is of no consequence as previously discussed for Claim 9 under Ground II with respect to Onoda. Similarly, in light of my above analyses of the teachings in Kawagoe with respect to Elements [1.2] and [1.3], Kawagoe teaches that the transistors are formed on the first surface of the substrate which contains the first and second active regions. Furthermore, when the graded dopant concentration of the active region in Kawagoe aids carrier

movement from the first surface to the second surface of the substrate, it is without doubt that the graded dopant concentration also aids carrier movement from the surface to the substrate. Thus, Kawagoe discloses and/or renders obvious claim 9.

k. Dependent Claims 12-16 of the ’842 Patent

193. Dependent claims 12 through 16 recite the same claim language as dependent claims 4 through 8, other than that they depend from claim 9 rather than from claim 1. For the same reasons as discussed above with regard to the dependent claims associated with claim 1, dependent claims 12-16 are disclosed and/or rendered obvious by the teachings of Kawagoe. (See supra claim 4 for claim 12, claim 5 for claim 13, claim 6 for claim 14, claim 7 for claim 15, and claim 8 for claim 16.)

C. ’481 Patent

194. In this section, I analyze Claims 1-9, 13, 15, 17, 20, 22-27, 31-32, 34 of the ’481 Patent based on the same prior art applied to Claims 1, 2, 4-9, 12-18 of the ’842 Patent.

1. Ground II: Onoda Renders Obvious Claims 1-9, 13, 15, 17, 20, 22-27, 31, 32, and 34 of the '481 Patent.

a. Independent Claim 1 of the '481 Patent

(i) Preamble: "A semiconductor device comprising:"

195. Claim 1, preamble, is substantively identical to claim 1, preamble, of the '842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

196. Claim 1, Element [1.1] is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [1.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

197. Claim 1, Element [1.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [1.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

198. Claim 1, Element [1.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [1.4]: "transistors formed in at least one of the first active region or second active region;"

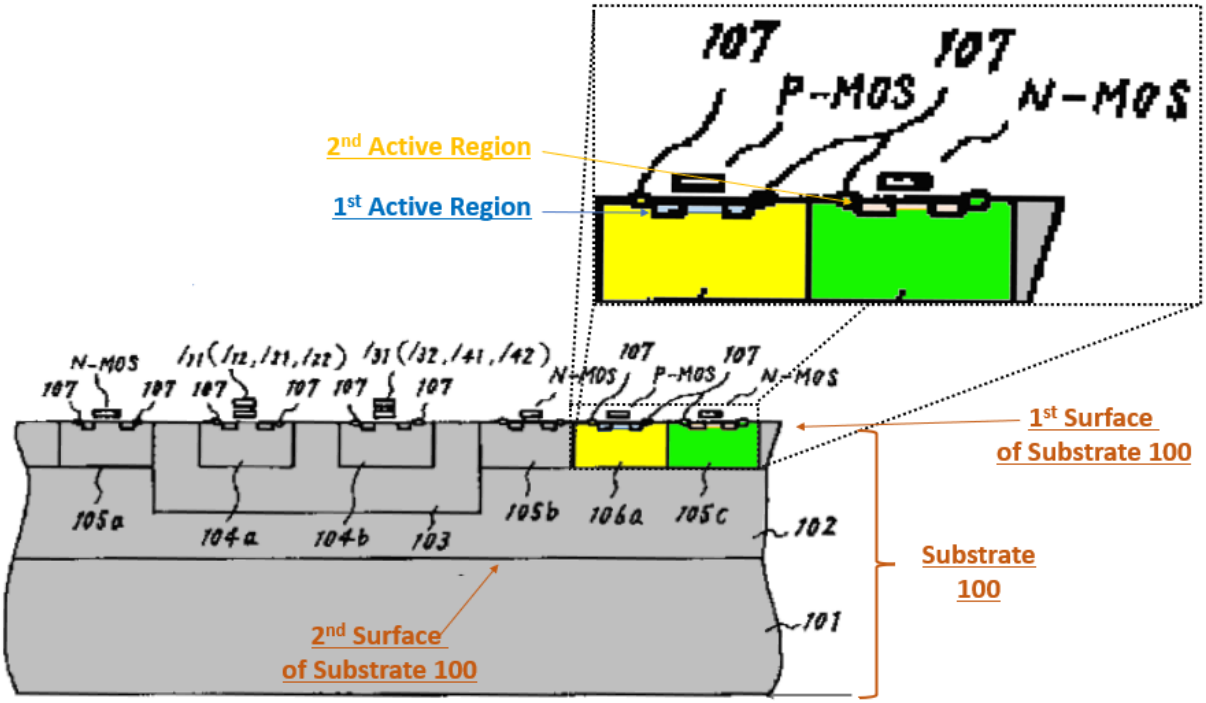
199. Claim 1, Element [1.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and"

200. Claim 1, Element [1.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate."

201. Onoda discloses Element [1.6] of Claim 1 of the '481 Patent. Onoda discloses multiple well regions including at least one well region having a grade dopant region that aids carrier movement form the first surface to the second surface of the substrate. FIG. 3 in Onoda as presented and discussed above in connection with Claim 1 of the '842 Patent are reproduced below for convenience. Onoda discloses semiconductor well regions in the second semiconductor layer 102 within the substrate 100 that are p doped to form p-well regions, e.g., 105a, 105b and 105c (one colored in green) and n doped to form n-well regions, e.g., 106a, 106b and 106c (one colored in yellow). As can be seen from FIG. 3 of Onoda below, the p-well region 105c is adjacent to the first active region located near the top of the p-well region 105c , and the n-well region 106a is adjacent to the second active region located near the top of the n-well region 106a.



202. FIG. 3 further shows first active regions are formed in the substrate 100 adjacent to the first surface of the substrate 100 and are located in the top portion of n-well regions (e.g., 106a) to enable formation of PMOS transistors; and second active regions are also formed in the substrate 100 adjacent to the first surface of the substrate 100 and are located in the top portion of p-well regions (e.g., 105b or 105c) to enable formation of NMOS transistors. Onoda at [0041]-[0045].

203. FIG. 11 in Onoda discloses that the p-well region 105a in Onoda at least has a p dopant concentration decreases from the top surface of the p-well region

105a (the first surface of the substrate 100) into the well region 105a. The p-well regions 105b and 105c should have the same graded dopant concentration profile. Therefore, each of the p-well regions 105a, 105b and 105c constitutes a graded dopant region. As discussed above regarding Element [1.5] in the '842 Patent, this graded dopant region in the p-well region 105a, 105b or 105c drives electrons to the bottom of the respective well region and, accordingly, has the effect "to aid carrier movement from the first surface to the second surface of the substrate."

204. Referring to each second active region marked in FIG. 3 in Onoda, the second active region includes a top portion of the respective p-well region 105a, 105b or 105c. Each active region is adjacent to the corresponding well region. Onoda discloses "at least one well region adjacent to the first or second active region." In Onoda, each second active region marked in FIG. 3 includes a top portion of the respective p-well region 105a, 105b or 105c. Each active region has a graded dopant concentration of the p type that decreases with depths from the top surface of the p-well region 105a (the first surface of the substrate 100) and to the extent that Element [1.5] is construed to tie the recited "containing at least one graded dopant region" to "the first or second active region," it is also disclosed by Onoda.

205. In light of the above, Onoda discloses Element [1.5].

206. Therefore, Onoda discloses or renders obvious all claim elements and their combination of Claim 1 of ‘481 Patent.

b. Dependent Claim 2 of the ’481 Patent: “The semiconductor device of claim 1, wherein the substrate is a p-type substrate.”

207. Claim 2 is substantively identical to claim 2 of the ’842 Patent and is disclosed for the same reasons I described for claim 2 of the ’842 Patent.

c. Dependent Claim 3 of the ’481 Patent: “The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

208. Claim 3 is substantively identical to claim 4 of the ’842 Patent and is disclosed for the same reasons I described for claim 4 of the ’842 Patent.

d. Dependent Claim 4 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.”

209. Claim 4 is substantively identical to claim 5 of the ’842 Patent and is disclosed for the same reasons I described for claim 5 of the ’842 Patent.

e. Dependent Claim 5 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

210. Claim 5 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent.

f. Dependent Claim 6 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.”

211. Claim 6 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

g. Dependent Claim 7 of the ’481 Patent: “The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

212. Claim 7 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 8 of the ’842 Patent.

h. Dependent Claim 8 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.”

213. Claim 8 is substantively identical to claim 17 of the ’842 Patent and is disclosed for the same reasons I described for claim 17 of the ’842 Patent.

i. Dependent Claim 9 of the ’481 Patent: “The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

214. Claim 9 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. In Onoda, the second active region is located in the upper portion of a p-well region 105a, 105b or 105c on the semiconductor device which has a graded dopant concentration as shown in FIG. 11 where the doping is p-type.

j. Dependent Claim 13 of the ’481 Patent: “The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.”

215. Claim 13 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent.

k. Dependent Claim 15 of the ’481 Patent: “ The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.”

216. Claim 15 recites a combination of different claim limitations in claim 4 and claim 18 of the ’842 Patent in a slightly different way: “wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.” The claim does not foreclose the device having an epitaxial substrate and as

previously discussed, Onoda discloses both an epitaxial substrate part (second semiconductor layer 102) and nonepitaxial substrate part (first semiconductor layer 101) of its substrate 100. Onoda discloses Claim 15for the same reasons I described for claim 4 and claim 18 of the ’842 Patent.

l. Dependent Claim 17 of the ’481 Patent: “ The semiconductor device of claim 1, wherein the device is a logic device.”

217. Onoda renders obvious claim 17. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) In addition, a POSITA would have understood that the doping gradient aspect of the flash memory semiconductor devices would be useful in logic devices, because both memory and logic devices suffer from the same issues related to minority carrier movement. (II.C.)

m. Independent Claim 20 of the ’481 Patent

(i) Preamble: “A semiconductor device comprising:

218. Claim 20, preamble, is substantively identical to claim 1, preamble of ‘481 Patent and claims 1 and 9, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [20.1]: "a substrate of a first doping type at a first doping level having first and second surfaces"

219. Claim 20, Element [20.1] is substantively identical to claim 1, Element [1.1] of the '481 Patent and claim 1, Element [1.1] and the substrate limitation in claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [20.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

220. Claim 20, Element [20.2] is substantively identical to claim 1, Element [1.2] of the '481 Patent and claim 1, Element [1.2] of the '842 Patent but recites "in the surface thereof" in a way substantially similar way to Claim 9 of the '842 Patent. Thus, this element is disclosed for the same reasons I described above for that element in Claim 9 of the '842 Patent.

(iv) Element [20.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

221. Claim 20, Element [20.3] is substantively identical to claim 1, Element [1.3] of '481 Patent and claim 1, Element [1.3] of the '842 Patent but recites "in the

surface thereof" in a way substantially similar to Claim 9 of the '842 Patent. Thus, this element is disclosed for the same reasons I described above for that element in Claim 9 of the '842 Patent.

(v) Element [20.4]: "transistors formed in at least one of the first active region or second active region;"

222. Claim 20, Element [20.4] is substantively identical to claim 1, Element [1.4] of the '481 Patent and claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [20.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and"

223. Claim 20, Element [20.5] is substantively identical to claim 1, Element [1.5] of the '481 Patent and claim 1, Element [1.5] of the '842 Patent but recites "from the surface" in a way substantially similar to Claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element in Claim 9 of the '842 Patent.

(vii) Element [20.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate."

224. Claim 20, Element [20.6] is substantively identical to claim 1, Element [1.6] of the '481 Patent and is disclosed for the same reasons I described for that element.

225. Therefore, Onoda discloses or renders obvious all claim elements and their combination in Claim 20.

n. Dependent Claim 22 of the '481 Patent: "The semiconductor device of claim 20, wherein the substrate is a p-type substrate."

226. Claim 22 is substantively identical to claim 2 of the '481 Patent and claim 2 of the '842 Patent and is disclosed for the same reasons I described for claim 2 of the '481 Patent and claim 2 of the '842 Patent.

o. Dependent Claim 23 of the '481 Patent: "The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

227. Claim 23 is substantively identical to claim 3 of the '481 Patent and claim 4 of the '842 Patent and is disclosed for the same reasons I described for claim 3 of the '481 Patent and claim 4 of the '842 Patent.

p. Dependent Claim 24 of the ’481 Patent: “The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.”

228. Claim 24 is substantively identical to claim 4 of the ’481 Patent and claim 5 of the ’842 Patent and is disclosed for the same reasons I described for claim 4 of the ’481 Patent and claim 5 of the ’842 Patent.

q. Dependent Claim 25 of the ’481 Patent: “The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

229. Claim 25 is substantively identical to claim 5 of the ’481 Patent and claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 5 of the ’481 Patent and claim 6 of the ’842 Patent.

r. Dependent Claim 26 of the ’481 Patent: “The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.”

230. Claim 26 is substantively identical to claim 6 of the ’481 Patent and claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’481 Patent and claim 7 of the ’842 Patent.

s. Dependent Claim 27 of the ’481 Patent: “The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

231. Claim 27 is substantively identical to claim 9 of the ’481 Patent and claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 9 of the ’481 Patent and claim 6 of the ’842 Patent. In Onoda, the second active region is located in a p-well region 105a, 105b or 105c on the semiconductor device which has a graded dopant concentration as shown in FIG. 11 where the doping is p-type.

t. Dependent Claim 31 of the ’481 Patent: “The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.”

232. Claim 31 is substantively identical to claim 7 of the ’481 Patent and claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’481 Patent and claim 8 of the ’842 Patent.

u. Dependent Claim 32 of the ’481 Patent: “The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

233. Claim 32 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent.

v. Dependent Claim 34 of the ’481 Patent: “ The semiconductor device of claim 20, wherein the device is a logic device.”

234. Onoda renders obvious this claim. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) A POSITA would have understood that the doping gradient aspect of the flash memory semiconductor devices would be useful in logic devices as both memory and logic devices suffer from issues related to minority carrier movement. (II.C.)

2. Ground III: Onoda in view of Nishizawa Renders Obvious Claims 1-9, 13, 15, 17, 20, 22-27, 31, 32, and 34 of the ’481 Patent

235. I incorporate my analysis regarding the motivation to combine Onoda and Nishizawa as provided for the ’842 Patent, Ground III in section III.B.2.

a. Independent Claim 1 of the ’481 Patent

(i) Element [1.5]: “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and”

236. Claim 1, Element [1.5] is substantively identical to claim 1, Element [1.5] of the ’842 Patent and is disclosed for the same reasons I described above for that element. Nishizawa explicitly provides that the graded dopant regions aid

carrier movement from the first surface to the second surface of the substrate. (III.B.2)

(ii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate."

237. Claim 1, Element [1.6] is substantively identical to claim 1, Element [1.4] and [1.5] and is disclosed for the same reasons I described for that element. Onoda discloses multiple well regions, each having an active region and having a grade dopant region that aids carrier movement form the first surface to the second surface of the substrate. Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the first surface to the second surface of the substrate. (III.B.2.)

b. Independent Claim 20 of the '481 Patent

238. Claim 20 of '842 Patent is substantively identical to claim 1, which is substantively similar to claim 1 of the '842 Patent and is disclosed for the same reasons I described above for that element. (III.B.2 and III.C.2.)

a. Claims 3-9, 13, 15-17, 22-27, 31, 32, and 34 of the '481 Patent

239. Claims 3-9, 13, 15-17, 22-27, 31, 32, and 34 of '842 Patent are disclosed and/or rendered obvious by the Onoda-Nishizawa combination for the same reasons as discussed in Ground II and Claim 1 of Ground III.

3. Ground I: Kawagoe Renders Obvious Claims 1-9, 13, 15, 17, 20, 22-27, 31, 32, and 34 of the '481 Patent

a. Independent Claim 1 of the '481 Patent

(i) Preamble: "A semiconductor device comprising:"

240. Claim 1, preamble, is substantively identical to claim 1, preamble, of the '842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

241. Claim 1, Element [1.1] is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [1.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

242. Claim 1, Element [1.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [1.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

243. Claim 1, Element [1.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [1.4]: "transistors formed in at least one of the first or second active region;"

244. Claim 1, Element [1.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

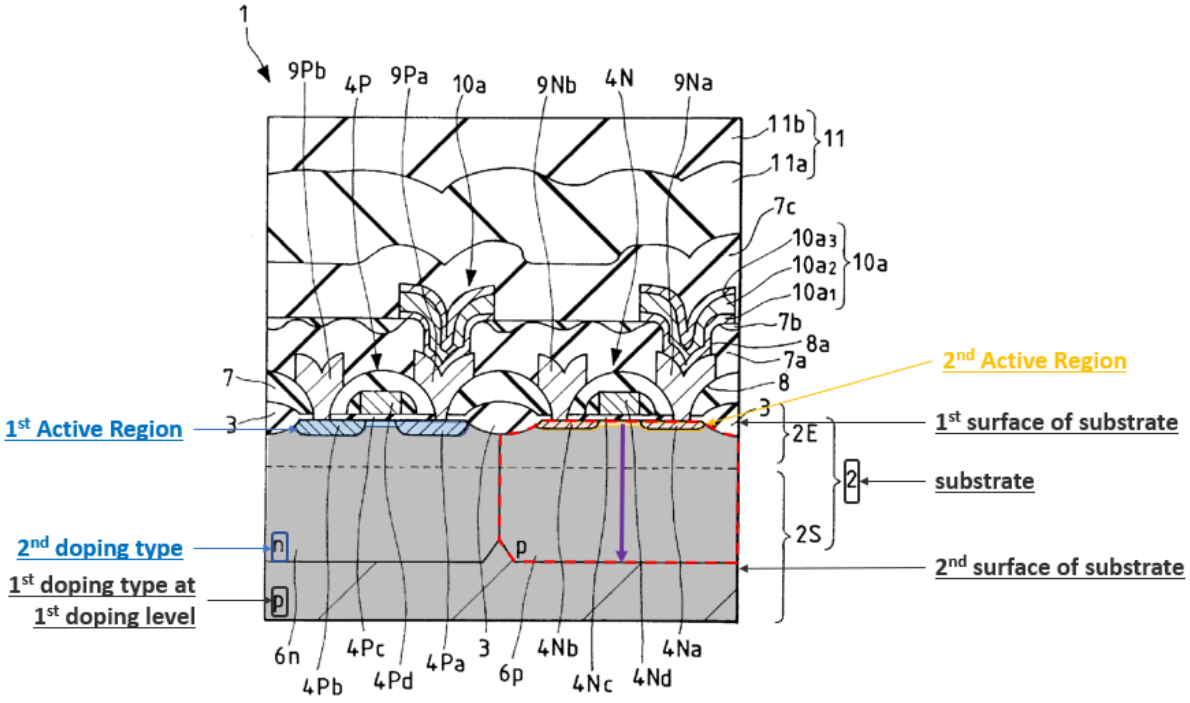
(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and"

245. Claim 1, Element [1.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate."

246. Kawagoe discloses Element [1.6] of the '481 Patent. As depicted below, Kawagoe provides a p-well 6p (the claimed at least one well region) (annotated in red) that is adjacent to the first active region. The p-well has a graded dopant region from its surface (through the second active region) that aids in the movement of carriers from the first surface to the second surface.

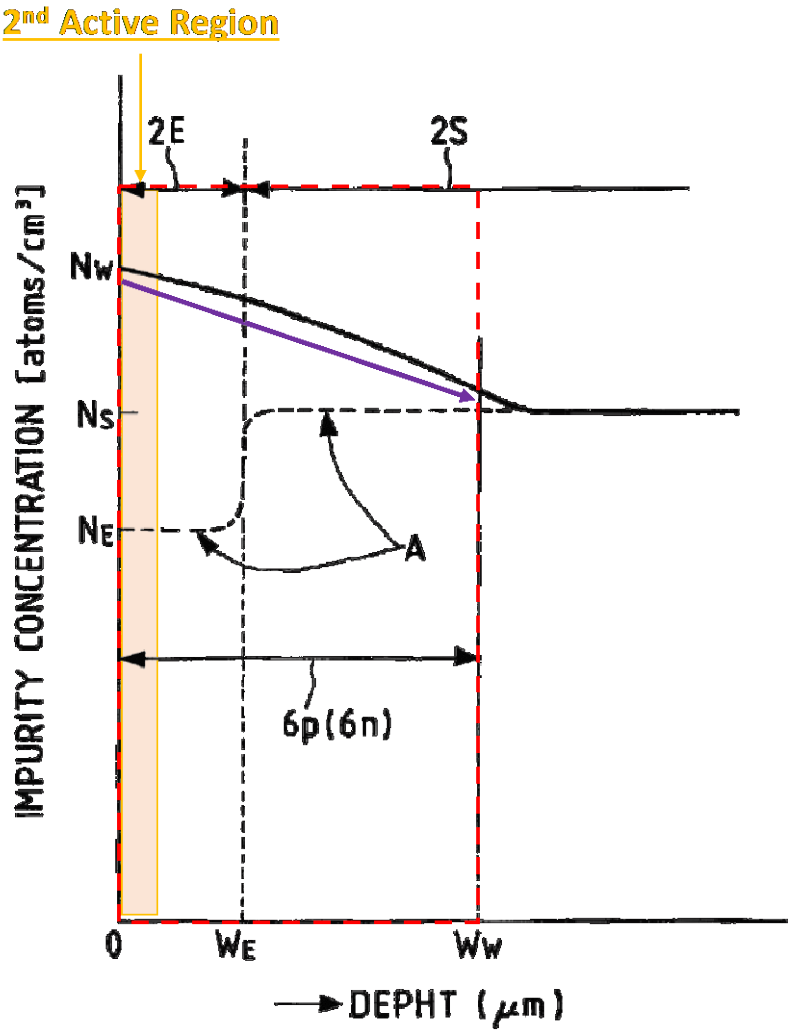
FIG. 16



247. A POSITA would further understand that the n-well 6n (another well region) is similarly adjacent to the second active region.

248. As can be seen in FIGs. 16 and 17, the epitaxial layer 2E has a thickness W_E from the surface of the epitaxial layer 2E part of the substrate 2 and that the n-well 6n and the p-well 6p have a depth W_w from the top surface of the epitaxial layer 2E of the substrate 2. (Kawagoe at 15:18-36.)

FIG. 17



249. Kawagoe in FIG. 17 discloses an example of the graded dopant (impurity) concentration profile at different depths from the top surface of the substrate 2 of the Kawagoe device in FIG. 16. In particular, Kawagoe discloses that the impurity concentration of the p-well 6p (the graded dopant concentration curve with a maximum concentration of N_w at the top surface in FIG. 17) is designed to

aid carrier movement of electrons from the top surface of the layer 2E of the substrate 2 by using the graded dope concentration to attract the electrons to the substrate body 2S. Kawagoe at 15:62-16:40. The following text is reproduced from Kawagoe at 15:62-16:15:

> "Incidentally, in the present embodiment 4, the aforementioned p-well 6p and n-well 6n are formed to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S, as shown in FIGS. 16 and 17, and the p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E. Thus, the impurity concentration of the p-well 6p is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p. The impurity concentration N_W in the principal surface of the epitaxial layer 2E of the p-well 6p and the n-well 6n is at

about 6×10^{16} atoms/cm^3, so that the impurity concentration of the p-well 6p and the n-well 6n is at 5×10^{15} to 6×10^{16} atoms/cm^3."

250. The first and second active regions (annotated in blue and tan) are at the first surface of the semiconductor device (*see, e.g.,* Kawagoe at 15:62-16:15) and are formed into the semiconductor device so that carriers (*e.g.*, minority carriers, *i.e.*, electrons in the p-well) are attracted to the substrate to reduce errors. (*Id.*) The depthwise gradient extends from the first surface of the semiconductor device toward the substrate body 2S (*id.* at 16:2-15). (*Id.* at 15:26-36). As depicted in annotated FIGS. 16 and 17 above, Kawagoe's second active region is disposed on the top portion of the p-well 6p. This portion of the second active region has a graded dopant concentration. (Kawagoe 15:62-16:40; *see also id.* at 15:26-36, 17:11-21; *see also id.* at 1:59-2:5, 2:20-23, 15:62-16:15.) The gradient of this graded dopant concentration is represented by a portion of the purple arrow which is also the direction of the electron carrier movement caused by a drift electric field associated with the graded dopant concentration in the second active region which is at the top of the p-well 6p. This portion of the graded dopant profile in the second active region in Kawagoe discloses the claimed "least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

251. Therefore, in light of teachings in Kawagoe and above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 1.

b. Dependent Claim 2 of the ’481 Patent: “The semiconductor device of claim 1, wherein the substrate is a p-type substrate.”

252. Claim 2 is substantively identical to claim 2 of the ’842 Patent and is disclosed for the same reasons I described for that element.

c. Dependent Claim 3 of the ’481 Patent: “The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

253. Claim 3 is substantively identical to claim 4 of the ’842 Patent and is disclosed for the same reasons I described for that element.

d. Dependent Claim 4 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.”

254. Claim 4 is substantively identical to claim 5 of the ’842 Patent and is disclosed for the same reasons I described for that element.

e. Dependent Claim 5 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

255. Claim 5 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element.

f. Dependent Claim 6 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.”

256. Claim 6 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for that element.

g. Dependent Claim 7 of the ’481 Patent: “The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

257. Claim 7 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for that element.

h. Dependent Claim 8 of the ’481 Patent: “The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.”

258. Claim 8 is substantively identical to claim 17 of the ’842 Patent and is disclosed for the same reasons I described for that element.

i. Dependent Claim 9 of the ’481 Patent: “The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

259. Claim 9 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element. The second active region is located in a p-well 6p (FIG. 16) and has a graded dopant concentration as shown in FIG. 17 where the doping is p-type.

j. Dependent Claim 13 of the ’481 Patent: “The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.”

260. Claim 13 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for that element.

k. Dependent Claim 15 of the ’481 Patent: “ The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.”

261. Claim 15 is substantively identical to claim 4 and claim 18 of the ’842 Patent yet recites “wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.” The claim does not foreclose the device having an epitaxial substrate and as previously discussed, Kawagoe discloses both an epitaxial substrate layer 2E and a nonepitaxial body substrate 2S

for its substrate 2. This limitation is disclosed for the same reasons I described for those elements.

l. Dependent Claim 17 of the '481 Patent: " The semiconductor device of claim 1, wherein the device is a logic device."

262. Kawagoe discloses this element. In particular, Kawagoe states "the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31.)

m. Independent Claim 20 of the '481 Patent

(i) Preamble: "A semiconductor device comprising:

263. Claim 20, preamble, is substantively identical to claim 1, preamble of the '842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [20.1]: "a substrate of a first doping type at a first doping level having first and second surfaces"

264. Claim 20, Element [20.1] is substantively identical to claim 1, Element [1.1] and the substrate limitation of claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [20.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

265. Claim 20, Element [20.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 Patent which does not change my analysis as the surface discussed is the first surface which was already shown to contain transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(iv) Element [20.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

266. Claim 20, Element [20.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 Patent which does not change my analysis as the surface discussed is the first surface which was already shown to contain transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(v) Element [20.4]: "transistors formed in at least one of the first active region or second active region;"

267. Claim 20, Element [20.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [20.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and"

268. Claim 20, Element [20.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "from the surface" in a way substantially similar to Claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vii) Element [20.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate"

269. Claim 20, Element [20.6] is substantively identical to claim 1, Element [1.6] and is disclosed for the same reasons I described for that element. Kawagoe discloses multiple well regions, each having an active region and having a grade

dopant region that aids carrier movement form the first surface to the second surface of the substrate.

270. Therefore, in light of teachings in Kawagoe and the above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 20.

n. Dependent Claim 22 of the ’481 Patent: “The semiconductor device of claim 20, wherein the substrate is a p-type substrate”

271. Claim 22 is substantively identical to claim 2 of the ’842 Patent and is disclosed for the same reasons I described for claim 2 of the ’842 Patent.

o. Dependent Claim 23 of the ’481 Patent: “The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

272. Claim 23 is substantively identical to claim 4 of the ’842 Patent and is disclosed for the same reasons I described for claim 4 of the ’842 Patent.

p. Dependent Claim 24 of the ’481 Patent: “The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.”

273. Claim 24 is substantively identical to claim 5 of the ’842 Patent and is disclosed for the same reasons I described for claim 5 of the ’842 Patent.

q. Dependent Claim 25 of the ’481 Patent: “The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

274. Claim 25 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent.

r. Dependent Claim 26 of the ’481 Patent: “The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.”

275. Claim 26 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

s. Dependent Claim 27 of the ’481 Patent: “The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

276. Claim 27 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. In Kawagoe, the active regions are located in n-wells and p-wells which have a graded dopant concentration as shown in their respective doping profiles (FIGS. 16 and 17) where the doping is either p-type or n-type.

t. Dependent Claim 31 of the ’481 Patent: “The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.”

277. Claim 31 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent.

u. Dependent Claim 32 of the ’481 Patent: “The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

278. Claim 32 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent.

v. Dependent Claim 34 of the ’481 Patent: “ The semiconductor device of claim 20, wherein the device is a logic device.”

279. Kawagoe discloses this claim. In particular, Kawagoe states “the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called ‘microcomputer.’” (Kawagoe at 24:28-31.)

D. ’222 Patent

280. In this section, I analyze Claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39, 40-42 of the ‘222 Patent based on the same prior art applied to claims of the ‘842 Patent and ‘481 Patent.

1. Ground II: Onoda Renders Obvious Claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39, 40-42 of the '222 Patent

a. Independent Claim 1 of the '222 Patent

(i) Preamble: "A VLSI Semiconductor device comprising:"

281. Claim 1, preamble, is substantively identical to claim 1, preamble, of the '842 Patent and is disclosed for the same reasons I described above for that element. Further, the addition of the term "VLSI" is of no consequence to my analysis. As mentioned above (II.C.), VLSI stands for "very large scale integrated circuits." This naming modifier merely refers to the number of components and does not indicate any relevant changes to the process of developing a semiconductor device with a graded dopant concentration.

(ii) Element [1.1]: " a substrate of a first doping type at a first doping level having a surface;"

282. Claim 1, Element [1.1], is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [1.2]: " a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

283. Claim 1, Element [1.2], is substantively identical to claim 1, Element [1.2] of the ' 842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [1.3]: " a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

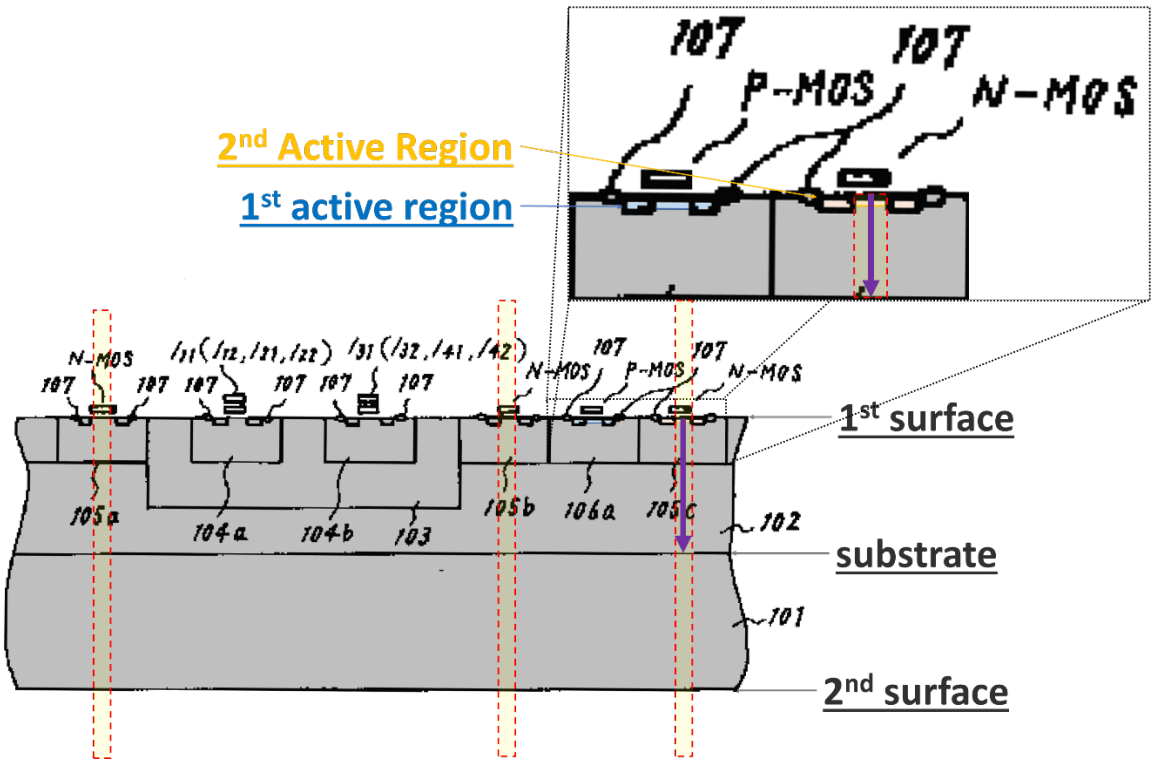
284. Claim 1, Element [1.3], is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [1.4]: " transistors formed in at least one of the first active region or second active region;"

285. Claim 1, Element [1.4], is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

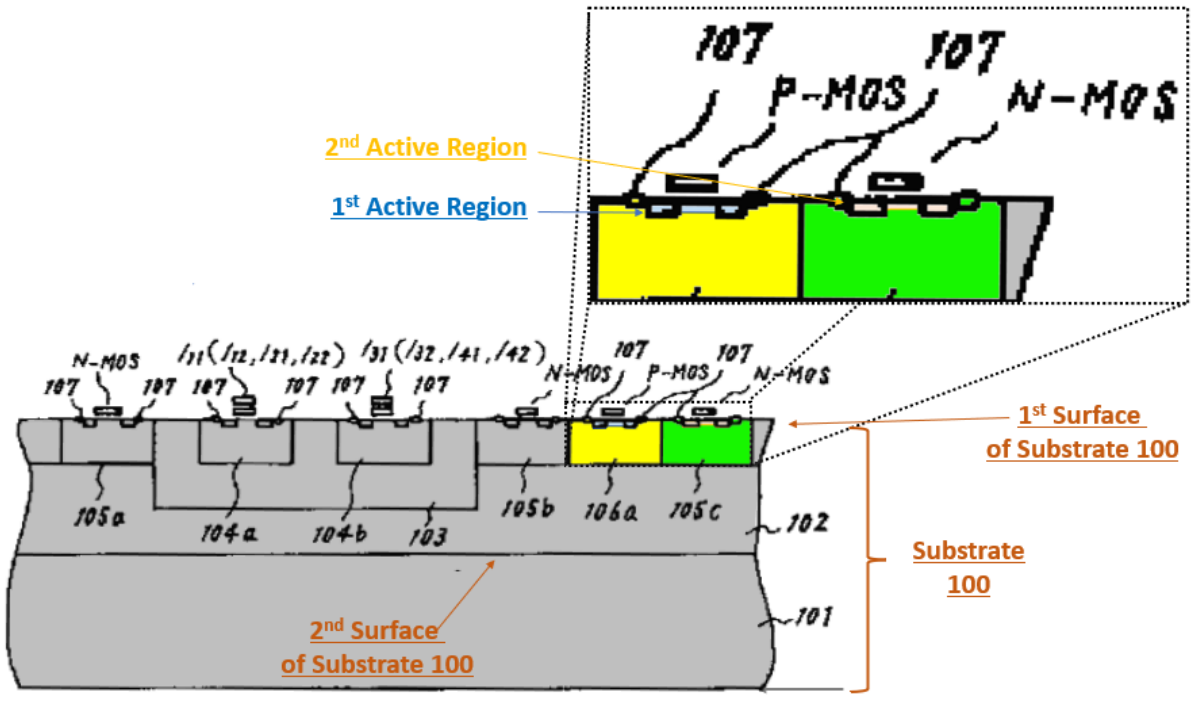
(vi) Element [1.5]: " at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

286. Claim 1, Element [1.5], is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "from the first and second active regions towards an area of the substrate where there is no active regions." As can be seen from the below, there are no active regions in the area 101 of the substrate which is the direction of the carrier movement.



(vii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,"

287. Claim 1, Element [1.6], is substantively identical to claim 1, Element [1.6] of the '481 Patent but recites "the surface towards the area of the substrate where there are no active regions" As can be seen from the below FIG. 3 of Onoda, there are no active regions in the area 101 of the substrate which is the direction of the carrier movement.



(viii) Element [1.7]: "wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

288. Onoda renders obvious this element. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) In addition, a POSITA would have understood that the doping gradient aspect of the flash memory semiconductor devices would be useful in logic devices as both memory and logic devices suffer from issues related to minority carrier movement. (II.C.)

289. Therefore, in light of teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 1.

b. Dependent Claim 3 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

290. Claim 3 is substantively identical to claim 4 of the '842 Patent and is disclosed for the same reasons I described for claim 4 of the '842 Patent.

c. Dependent Claim 4 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices."

291. Claim 4 is substantively identical to claim 5 of the '842 Patent and is disclosed for the same reasons I described for claim 5 of the '842 Patent. Further, a

POSITA would have understood that the teachings of Onoda were not limited to the disclosed flash memory and would be applicable to digital logic applications. (II.C.)

d. Dependent Claim 5 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

292. Claim 5 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent.

e. Dependent Claim 6 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.”

293. Claim 6 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

f. Dependent Claim 7 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

294. Claim 7 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 8 of the ’842 Patent.

g. Dependent Claim 8 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.”

295. Claim 8 is substantively identical to claim 17 of the ’842 Patent and is disclosed for the same reasons I described for claim 17 of the ’842 Patent.

h. Dependent Claim 9 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

296. Claim 9 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. In Onoda, the second active region is located in a p-well region 105a, 105b or 105c on the semiconductor device which has a graded dopant concentration as shown in FIG. 11 where the doping is p-type.

i. Dependent Claim 13 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.”

297. Claim 13 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent. Further, a POSITA would have understood that the teachings of Onoda were not limited to

the disclosed flash memory and would be applicable to digital logic applications. (II.C.)

j. Dependent Claim 15 of the ’222 Patent: “ The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.”

298. Claim 15 recites a combination of different claim limitations in claim 4 and claim 18 of the ’842 Patent in a slightly different way: “wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.” The claim does not foreclose the device having an epitaxial substrate and as previously discussed. Onoda discloses both an epitaxial substrate part (second semiconductor layer 102) and nonepitaxial substrate part (first semiconductor layer 101) of its substrate 100. Onoda discloses Claim 15 for the same reasons I described for claim 4 and claim 18 of the ’842 Patent.

a. Dependent Claim 16 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the at least one semiconductor device is a flash memory.

299. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.)

b. Dependent Claim 17 of the ’222 Patent: “ The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.”

300. Onoda renders obvious this claim. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) In addition, a POSITA would have understood that the doping gradient aspect of the flash memory semiconductor devices would be useful in logic devices as both memory and logic devices suffer from issues related to minority carrier movement. (II.C.) Onoda describes having capacitive devices. (Onoda at [0089]; FIG. 17.)

c. Dependent Claim 20 of the ’222 Patent: “ The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.”

301. The ’222 Patent does not explain which direction is lateral or vertical; nonetheless, Onoda discloses this element. The active regions in Onoda are spread across the top surface of the second semiconductor layer 102 of the substrate 100 which gives them each a position relative to one another in the lateral direction and also spreads down into a portion of each p or n-well relative to the top surface of the well, which places each active region in a position along the vertical direction with respect to the top surface of the well. (*See* Onoda, FIGS. 2 and 3.)

d. Independent Claim 21 of the ’222 Patent

(i) Preamble: “A VLSI semiconductor device comprising:

302. Claim 21, preamble, is substantively identical to claim 1 and 9, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element. Further, the addition of the term “VLSI” is of no consequence to my analysis. As mentioned above (II.C.), VLSI stands for “very large scale integrated circuits.” This naming modifier merely refers to the number of components and does not indicate any relevant changes to the process of developing a semiconductor device with a graded dopant concentration.

(ii) Element [21.1]: “a substrate of a first doping type at a first doping level having a surface;”

303. Claim 21, Element [21.1] is substantively identical to claim 1, Element [1.1] and the substrate limitation of Claim 9 of the ’842 Patent but recites “having a surface.” My analysis does not change as the claimed surface is the first surface in Element [1.1] of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [21.2]: "a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

304. Claim 21, Element [21.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 Patent which does not change my analysis as the surface discussed is the first surface which was already shown to contain transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(iv) Element [21.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

305. Claim 21, Element [21.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 Patent which does not change my analysis as the surface discussed is the first surface which was already shown to contain transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(v) Element [21.4]: "transistors formed in at least one of the first active region or second active region;"

306. Claim 21, Element [21.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

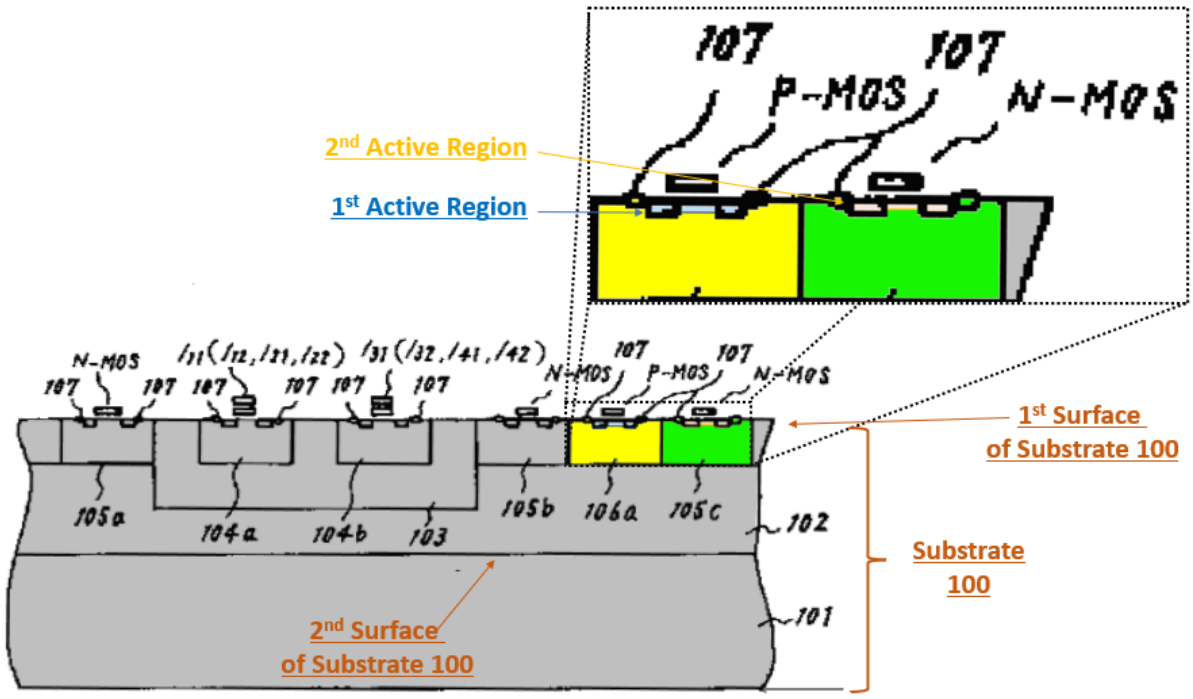
(vi) Element [21.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and"

307. Claim 21, Element [21.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "to an area of the substrate where there are no active regions." Onoda discloses the first semiconductor layer 101 on the lower part of its substrate 100 in FIGS. 3 and 8 that has no active regions. Onoda further discloses that the direction of the downward carrier movement is pointed to the area without active regions in the first semiconductor layer 101. For these reasons and the reasons described in claim 1, Element [1.5], Onoda discloses or renders obvious this element.

(vii) Element [21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions,"

308. Claim 21, Element [21.6] is substantively identical to claim 1, Element [1.6] of the '481 Patent but recites "from the surface to the area of the substrate where there are no active regions."

309. As shown in the figure below, there is no active region in substrate 101. The active regions are located at the top of the well regions and do not extend into the substrate.

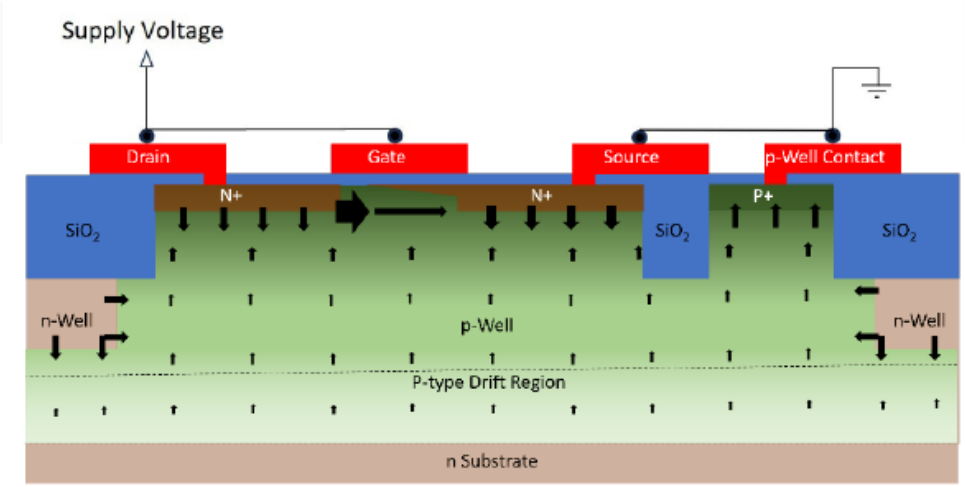


(viii) Element [21.7]: and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

310. Onoda discloses this element. Onoda teaches several dopant gradient profiles, in addition to providing graphical depictions of profiles that to a POSITA render a quasi-linear (or linear) gradient obvious. For instance, Onoda's FIG. 11 depicts a gradient that is quasi-linear (or at least linear).

311. Moreover, Onoda teaches a gaussian distribution of dopants. (Onoda at [0053] ("the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate Gaussian distributions with the concentrations at maxima near the surface").) Furthermore, providing a quasi-linear gradient was well-known, and this is confirmed by the '222 Patent describing them amongst a list of known profiles while providing no teachings as to how to construct a device with such profiles. ('222 Patent at 2:60-61 ("The gradient can be linear, quasi linear, exponential or complimentary error function.)) It would have been obvious to apply a quasi-linear gradient in view of a POSITA's general knowledge that such a gradient facilitates the movement of minority carriers. It would have further been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile, and would

have been readily available as a known option. As shown in the figure below, the unidirectional doping gradient produces a unidirectional electric field.



Linearly graded profile with the graded drift region matching the bottom of the well

312. Therefore, in light of teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 21.

e. Dependent Claim 24 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

313. Claim 24 is substantively identical to claim 4 of the ’842 Patent and is disclosed for the same reasons I described for that element.

f. Dependent Claim 25 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.”

314. Claim 25 is substantively identical to claim 5 of the ’842 Patent and is disclosed for the same reasons I described for that element.

g. Dependent Claim 26 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

315. Claim 26 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element.

h. Dependent Claim 27 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.”

316. Claim 27 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for that element.

i. Dependent Claim 28 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

317. Claim 28 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element. In Onoda, the active regions are located in n-wells and p-wells which have a graded dopant concentration

as shown in their respective doping profiles (FIG. 11 and 12) where the doping is either p-type or n-type.

j. Dependent Claim 32 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.”

318. Claim 32 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for that element.

k. Dependent Claim 33 of the ’222 Patent: “The VLSI semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

319. Claim 33 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for that element.

l. Dependent Claim 34 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the device is a flash memory.”

320. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3)

m. Independent Claim 39 of the ’222 Patent

(i) Preamble: “A semiconductor device comprising:

321. Claim 39, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [39.1]: "a substrate of a first doping type at a first doping level"

322. Claim 39, Element [39.1] is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [39.2]: "a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

323. Claim 39, Element [39.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "a surface of the substrate" which does not change my analysis as the surface discussed is the first surface which was already shown to contain active regions with transistors. Thus, Onoda discloses this element for the same reasons I described above for that element.

(iv) Element [39.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

324. Claim 39, Element [39.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and this limitation is disclosed for the same reasons I described above for that element.

(v) Element [39.4]: "transistors formed in at least one of the first active region or second active region;"

325. Claim 39, Element [39.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

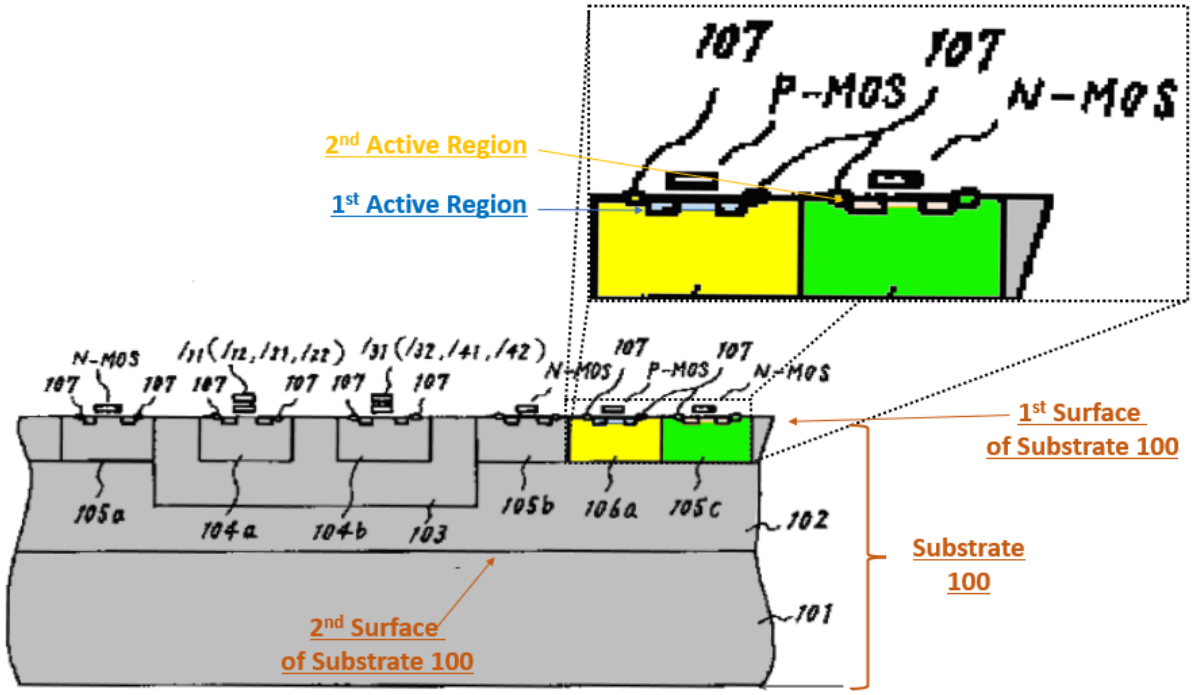
(vi) Element [39.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."

326. Claim 39, Element [39.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "from the first or second active region to at least one substrate area where there is no active region." Onoda discloses substrate area 101 in Figure 3 that has no active regions and where the carrier movement flows from the first or second active regions. For these reasons and the reasons described in claim 1, Element [1.5], Onoda discloses this element.

327. Therefore, in light of teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 39.

n. Dependent Claim 40 of the ’222 Patent: “The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.”

328. Claim 40, Element [40.6] is substantively identical to claim 1, Element [1.6] of the ’481 Patent but recites “the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.” As shown in the figure below, there is no well in substrate area 101. The wells (in yellow and green) are located in a different area of the substrate.



o. Independent Claim 41 of the ’222 Patent

(i) Preamble: “A semiconductor device comprising:

329. Claim 41, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [41.1]: “a substrate of a first doping type at a first doping level”

330. Claim 41, Element [41.1] is substantively identical to claim 1, Element [1.1] of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [41.2]: “a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”

331. Claim 41, Element [41.2] is substantively identical to claim 1, Element [1.2] of the ’842 Patent but recites “a surface of the substrate” which does not change my analysis as the surface discussed is the first surface which was already shown to contain active regions with transistors. Thus, Onoda discloses this element for the same reasons I described above for that element.

(iv) Element [41.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

332. Claim 41, Element [41.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and this limitation is disclosed for the same reasons I described above for that element.

(v) Element [41.4]: "transistors formed in at least one of the first active region or second active region; and"

333. Claim 41, Element [41.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [41.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."

334. Claim 41, Element [41.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region." Onoda discloses substrate 101 in Figure 3 that has no active regions and where the carrier movement flows from the first or second active regions. As previously discussed (II.C), the acceptor dopant concentration refers to p-type region

which is disclosed in Onoda. For these reasons and the reasons described in claim 1, Element [1.5], Onoda discloses this element.

335. Therefore, in light of teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 41.

p. Independent Claim 42 of the ’222 Patent

(i) Preamble: “A semiconductor device comprising:

336. Claim 42, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [42.1]: “a substrate of a first doping type at a first doping level”

337. Claim 42, Element [42.1] is substantively identical to claim 1, Element [1.1] of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [42.2]: “a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”

338. Claim 42, Element [42.2] is substantively identical to claim 1, Element [1.2] of the ’842 Patent but recites “a surface of the substrate” which does not change

my analysis as the surface discussed is the first surface which was already shown to contain active regions with transistors. Thus, Onoda discloses this element for the same reasons I described above for that element.

(iv) Element [42.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

339. Claim 42, Element [42.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and this limitation is disclosed for the same reasons I described above for that element.

(v) Element [42.4]: "transistors formed in at least one of the first active region or second active region; and"

340. Claim 42, Element [42.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [42.5]: "at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."

341. Claim 42, Element [42.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region." Onoda discloses substrate 101 in Figure 3 that has no

active regions and where the carrier movement flows from the first or second active regions. As previously discussed (II.C), the donor dopant concentration refers to n-type region which is disclosed in Onoda. For these reasons and the reasons described in claim 1, Element [1.5], Onoda discloses this element.

342. Therefore, in light of teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 42.

2. Ground III: Onoda in view of Nishizawa Renders Obvious Claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39, 40-42 of the '222 Patent

343. For claims not specifically discussed below based on Onoda in view of Nishizawa, I apply my analyses of those claims based on Onoda alone in Ground II.

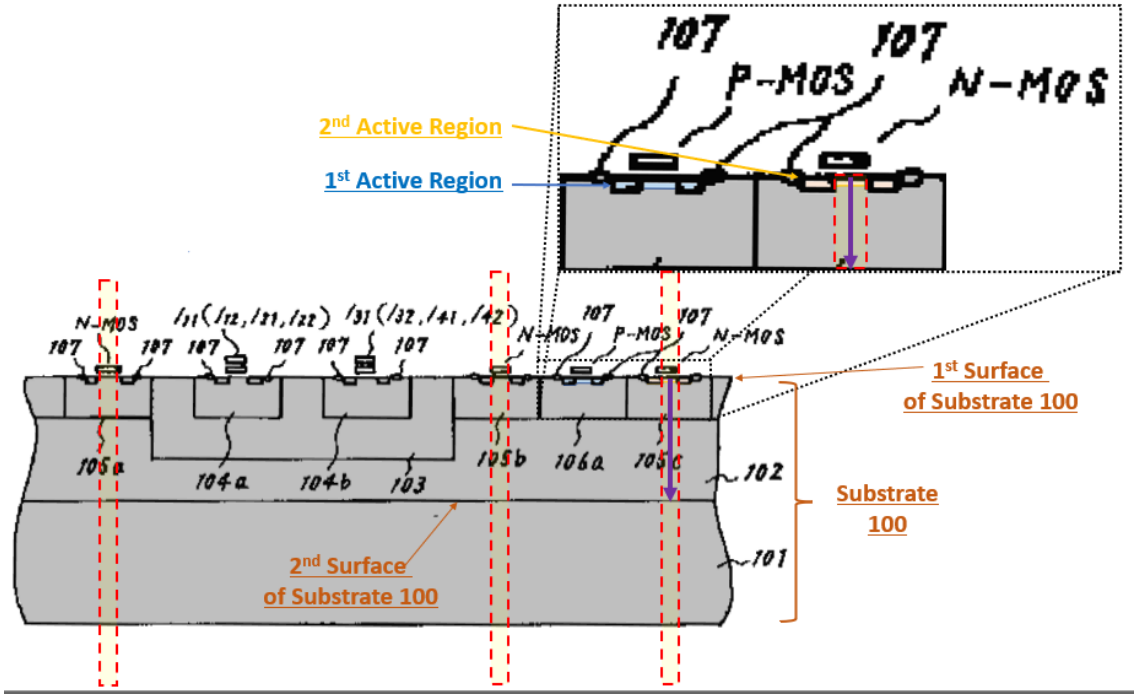
a. Independent Claim 1 of the '222 Patent

344. I incorporate my analysis regarding the motivation to combine Onoda and Nishizawa as provided for the '842 Patent, Ground III in section III.C.2.

345. In addition, for Claim Elements of Claim 1 not specifically discussed below based on Onoda in view of Nishizawa, I apply my analyses of those Claim Elements of Claim 1 based on Onoda alone in Ground II.

(i) Element [1.5]: " at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

346. Claim 1, Element [1.5], is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "from the first and second active regions towards an area of the substrate where there is no active regions." As can be seen from FIG. 3 of Onoda below, along the direction of the carrier movement in lines B-B' and C-C' shown in FIGS. 3 and 8, there are no active regions below p and n-wells in the second semiconductor layer 102 and in the area within the first semiconductor 101 of the substrate 100. Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the first surface to the second surface of the substrate. (III.B.2) Therefore, the combination of Onoda and Nishizawa discloses or renders obvious Claim Element [1.5].



(ii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions"

347. Claim 1, Element [1.6], is substantively identical to claim 1, Element [1.6] of the '842 Patent but recites "the surface towards the area of the substrate where there are no active regions." As can be seen from FIG. 3 of Onoda above, along the direction of the carrier movement in lines B-B' and C-C' shown in FIGS. 3 and 8, there are no active regions below p and n-wells in the second semiconductor layer 102 and in the area within the first semiconductor 101 of the substrate 100. Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the first surface to the second surface of the substrate. (III.B.2) Therefore, the

combination of Onoda and Nishizawa discloses or renders obvious Claim Element [1.6].

348. Therefore, in light of the combined teachings in Onoda and Nishizawa and the above explanations, the combination of Onoda and Nishizawa discloses or renders obvious all claim elements and their combination in Claim 1.

b. Independent Claims 21, 39, 41, and 42 of the '222 Patent

349. Independent claims 21, 39, 41, and 42 are rendered obvious based on the Onoda-Nishizawa combination for the reasons stated in Ground II as to the structure disclosed in Onoda and for the explicit teaching in Nishizawa that a graded dopant region aids carrier movement from the first surface to the second surface of the substrate. (III.B.2)

3. Ground I: Kawagoe Renders Obvious Claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, 39, 40-42 of the '222 Patent

a. Independent Claim 1 of the '222 Patent

(i) Preamble: "A VLSI Semiconductor device comprising:"

350. Claim 1, preamble, is substantively identical to claim 1, preamble, of the '842 Patent and is disclosed for the same reasons I described above for that element. In addition, Kawagoe relies on books entitled "VLSI Technology" for its

disclosure. (Kawagoe at 6:57-59.) Further, the addition of the term "VLSI" is of no consequence to my analysis. As mentioned above (II.C.), VLSI stands for "very large scale integrated circuits." This naming modifier merely refers to the number of components and does not indicate any relevant changes to the process of developing a semiconductor device with a graded dopant concentration. Kawagoe itself is directed to large scale integration (Kawagoe at 2:26-28) which a POSITA would have understood to encompass very large scale integration (VLSI) or at least render it obvious.

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having a surface;"

351. Claim 1, Element [1.1], is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [1.2]: "a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

352. Claim 1, Element [1.2], is substantively identical to claim 1, Element [1.2] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [1.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

353. Claim 1, Element [1.3], is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [1.4]: "transistors formed in at least one of the first active region or second active region;"

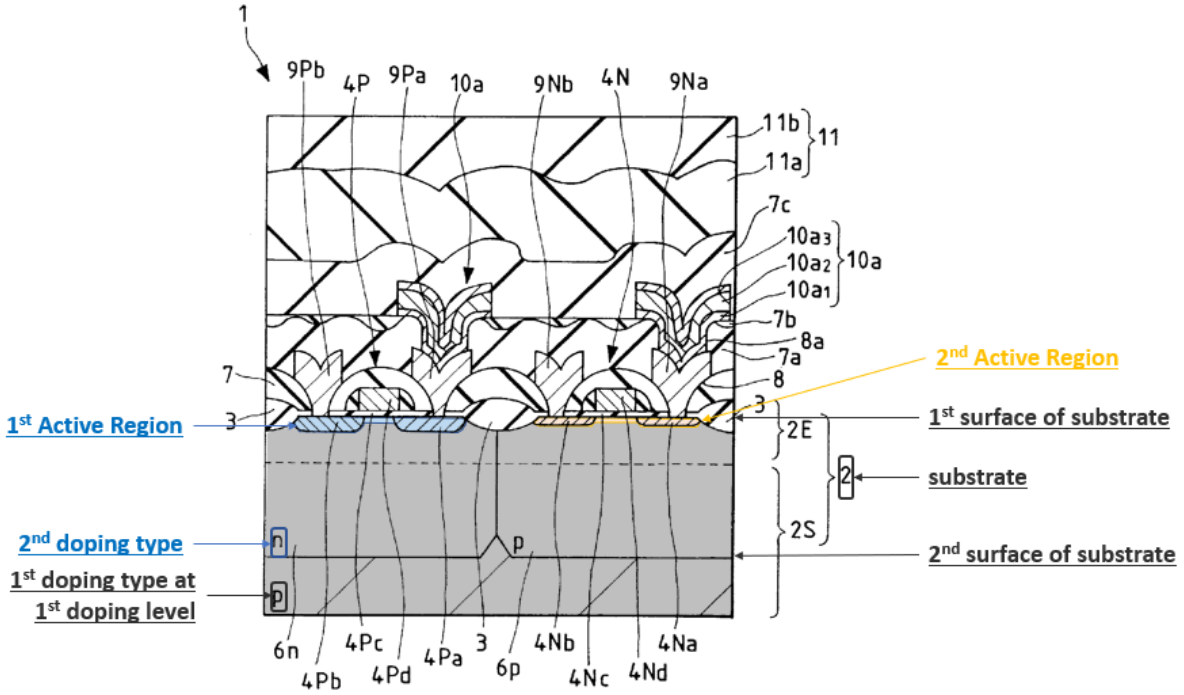
354. Claim 1, Element [1.4], is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

355. Claim 1, Element [1.5], is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "from the first and second active regions towards an area of the substrate where there is no active regions."

356. As can be seen from Kawagoe FIG. 16 below, the bottom portion of the substrate body 2S is "an area of the substrate where there are no active regions.".

FIG. 16



(vii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions"

357. Claim 1, Element [1.6], is substantively identical to claim 1, Element [1.6] of the '481 Patent (paragraph 246) but recites "the surface towards the area of the substrate where there are no active regions." As discussed above, Kawagoe FIG. 16 shows there are no active regions in the bottom portion of the substrate body 2S. As further discussed above, the graded dopant concentration in Kawagoe aids the movement of carriers from the surface to that bottom portion.

(viii) Element [1.7]: "wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

358. Kawagoe discloses this element. Kawagoe teaches a logic device. Kawagoe states "the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31.) A POSITA would have understood that formed digital logic of a VLSI semiconductor device.

359. Therefore, in light of the teachings in Kawagoe and the above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 1.

b. Dependent Claim 3 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

360. Claim 3 is substantively identical to claim 4 of the '842 Patent and is disclosed for the same reasons I described for that element.

c. Dependent Claim 4 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices."

361. Claim 4 is substantively identical to claim 5 of the '842 Patent and is disclosed for the same reasons I described for that element. Further, Kawagoe discloses a logic device. Kawagoe states "the techniques of the foregoing

embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31.)

d. Dependent Claim 5 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

362. Claim 5 is substantively identical to claim 6 of the '842 Patent and is disclosed for the same reasons I described for that element.

e. Dependent Claim 6 of the 'Patent: "The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

363. Claim 6 is substantively identical to claim 7 of the '842 Patent and is disclosed for the same reasons I described for that element.

f. Dependent Claim 7 of the 'Patent: "The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process."

364. Claim 7 is substantively identical to claim 8 of the '842 Patent and is disclosed for the same reasons I described for that element.

g. Dependent Claim 8 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

365. Claim 8 is substantively identical to claim 17 of the '842 Patent and is disclosed for the same reasons I described for that element.

h. Dependent Claim 9 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

366. Claim 9 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element. In Kawagoe, the second active region is located in a p-well 6p (FIG. 16) and has a graded dopant concentration as shown in FIG. 17 where the doping is p-type.

i. Dependent Claim 13 of the ’222 Patent: “The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.”

367. Claim 13 is substantively identical to claim 18 of the ’842 Patent and is disclosed by Kawagoe for the same reasons I described for that element. (Kawagoe at 8:46-54 (“The element forming region, as enclosed by the field insulating film 3, is formed for example with an n-channel MOS.FET (as will be shortly referred to as ‘nMOS’) 4N and [] p-channel MOS.FET (as will be shortly referred to as ‘pMOS’) 4P, and these nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit.”).) 4N and 4P are CMOS transistors and they have the claimed source and drain (*id.* at 8:66-67 (“semiconductor regions 4Na and 4Nb are regions for forming the source-drain regions of the nMOS 4N”); 9:47-48

("semiconductor regions 4Pa and 4Pb are regions for forming the source-drain regions of the pMOS 4P")), the claimed gate (*id.* at 9:19 (gate electrode 4Nd); 10:1 (gate electrode 4Pd)), and a channel region which a POSITA would understand is in the well region between the source-drain regions.

j. Dependent Claim 15 of the '222 Patent: " The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate."

368. Claim 15 is substantively identical to claim 4 ("a nonepitaxial substrate") and claim 18 ("the device is a [CMOS]") of the '842 Patent and is disclosed for the same reasons I described for that element. Kawagoe discloses a CMOS device (*id*. at 8:46-54) with a nonepitaxial substrate (2S) (*id*. at 15:1-3.)

k. Dependent Claim 16 of the '222 Patent: "The VLSI semiconductor device of claim 1, wherein the at least one semiconductor device is a flash memory.

369. Kawagoe discloses its structures and teachings can be applied to fabricate improved flash memory devices. (Kawagoe at 23:12-13 ("[I]t is possible to improve the performance, reliability and production yield of flash memory(i.e., EEPROM)."); 24:21-27.)

l. Dependent Claim 17 of the ’222 Patent: “ The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.”

370. Kawagoe discloses memory cells with digital logic and capacitor (FIGs. 26(B), 27(B)). Kawagoe also states “the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called ‘microcomputer.’” (Kawagoe at 24:28-31.)

m. Dependent Claim 20 of the ’222 Patent: “ The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.”

371. The ’222 Patent does not explain which direction is lateral or vertical. Nonetheless, Kawagoe discloses this element. The active regions in 6p and 6n well regions in Kawagoe are spread across the top surface of the substrate layer 2E of the substrate 2, which gives them each a position relative to one another in the lateral direction. The active regions in 6p and 6n well regions in Kawagoe are also spread down into a portion of their respective well regions, which gives the active regions each a position in the vertical direction with respect to the top surface of the substrate layer 2E of the substrate 2. (*See* FIG. 16.)

n. Independent Claim 21 of the ’222 Patent

(i) Preamble: “A VLSI semiconductor device comprising:

372. Claim 21, preamble, is substantively identical to claims 1 and 9, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element. In addition, Kawagoe relies on books entitled “VLSI Technology” for its disclosure. (Kawagoe at 6:57-59.) Further, the addition of the term “VLSI” is of no consequence to my analysis. As mentioned above (II.C.), VLSI stands for “very large scale integrated circuits.” This naming modifier merely refers to the number of components and does not indicate any relevant changes to the process of developing a semiconductor device with a graded dopant concentration.

(ii) Element [21.1]: “a substrate of a first doping type at a first doping level having a surface”

373. Claim 21, Element [21.1] is substantively identical to claim 1, Element [1.1] and the substrate limitation of Claim 9 of the ’842 Patent but recites “having a surface.” My analysis does not change as the claimed surface is the first surface in Element [1.1] and Claim 9 of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [21.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

374. Claim 21, Element [21.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 Patent which does not change my analysis as the surface discussed is the first surface which was already shown to contain transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(iv) Element [21.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

375. Claim 21, Element [21.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 patent which does not change my analysis as the surface discussed is the first surface which was already shown to contain transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(v) Element [21.4]: "transistors formed in at least one of the first active region or second active region;"

376. Claim 21, Element [21.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [21.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and"

377. Claim 21, Element [21.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "to an area of the substrate where there are no active regions." Kawagoe discloses the bottom portion of 2S in Figure 16 that has no active regions and where the carrier movement flows. For these reasons and the reasons described in claim 1, Element [1.5], Kawagoe discloses this element.

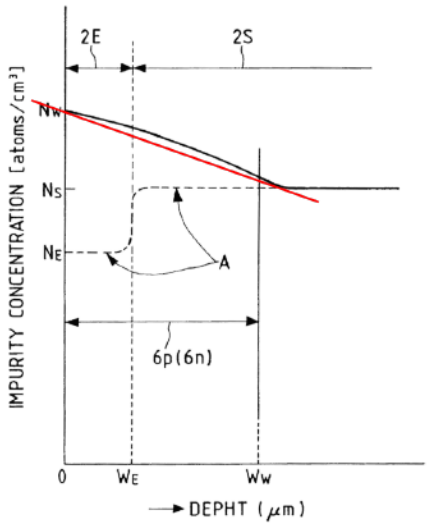
(vii) Element [21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions,"

378. Claim 21, the above part of Element [21.6] is substantively identical to claim 1, Element [1.6] of the '481 Patent but recites "from the surface to the area of the substrate where there are no active regions." As shown in Kawagoe FIG. 16 and discussed above, there is no active region in the bottom portion of 2S.

(viii) Element [21.6] (Continued): "and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

379. Kawagoe discloses the above part of Element [21.6]. Further, FIG. 17 of Kawagoe depicts a graded concentration. (Kawagoe at 16:16-40.) However, the vertical axis is not defined. As a result, a POSITA would not be able to discern if FIG. 17 depicts a quasi-linear or exponential gradient. If it is intended to be a linear scale, a linear gradient is depicted in red). As discussed earlier, either type of profile would improve the transport of minority carriers to the substrate.

FIG. 17



380. Moreover, a POSITA would have also found it obvious to use a quasi-linear gradient because it was a simple usage of one known method. The '222 Patent

only mentions quasi-linear gradient once (’222 Patent at 2:60-61 and does not illustrate or otherwise describe it, or describe any process steps for obtaining it, thus confirming that such a gradient was a well-known alternative to a POSITA. It would have been obvious to modify Kawagoe’s dopant profile based on the POSITA’s general knowledge in the art to achieve a known quasi-linear gradient. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success.

381. Therefore, in light of the teachings in Kawagoe and the above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 21.

o. Dependent Claim 24 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

382. Claim 24 is substantively identical to claim 4 of the ’842 Patent and is disclosed for the same reasons I described for claim 4 of the ’842 Patent.

p. Dependent Claim 25 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.”

383. Claim 25 is substantively identical to claim 5 of the ’842 Patent and is disclosed for the same reasons I described for claim 5 of the ’842 Patent.

q. Dependent Claim 26 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

384. Claim 26 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent.

r. Dependent Claim 27 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.”

385. Claim 27 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

s. Dependent Claim 28 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

386. Claim 28 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. In Kawagoe, the second active region is located in a p-well 6p (FIG. 16) and has a graded dopant concentration as shown in FIG. 17 where the doping is p-type.

t. Dependent Claim 32 of the ’222 Patent: “The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.”

387. Claim 32 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 8 of the ’842 Patent.

u. Dependent Claim 33 of the ’222 Patent: “The VLSI semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

388. Claim 33 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent.

v. Dependent Claim 34 of the ’222 Patent: “ The VLSI semiconductor device of claim 21, wherein the device is a flash memory.”

389. Kawagoe discloses its technique is applicable for flash memory. (Kawagoe at 23:12-13 (“[I]t is possible to improve the performance, reliability and production yield of flash memory(i.e., EEPROM).”); 24:21-27.)

w. Independent Claim 39 of the ’222 Patent

(i) Preamble: “A semiconductor device comprising:

390. Claim 39, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [39.1]: "a substrate of a first doping type at a first doping level"

391. Claim 39, Element [39.1] is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [39.2]: "a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

392. Claim 39, Element [39.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "a surface of the substrate" which does not change my analysis as the surface discussed is the first surface which was already shown to contain active regions with transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(iv) Element [39.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

393. Claim 39, Element [39.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [39.4]: "transistors formed in at least one of the first active region or second active region;"

394. Claim 39, Element [39.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [39.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."

395. Claim 39, Element [39.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "from the first or second active region to at least one substrate area where there is no active region." As described above, Kawagoe FIG. 16 shows there are no active regions in the bottom portion of the substrate body 2S. As further discussed above, the graded dopant concentration in Kawagoe aids the movement of carriers from the active regions on the surface to that bottom portion of substrate body 2S. For these reasons and the reasons described in claim 1, Element [1.5], Kawagoe discloses this element.

396. Therefore, in light of the teachings in Kawagoe and the above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 39.

x. Dependent Claim 40 of the ’222 Patent: “The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.”

397. Claim 40, is substantively identical to claim 1, Element [1.6] of the ’842 Patent but recites “the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.” As shown above in Kawagoe FIG. 16, there is no well in the bottom portion of substrate area 2S. The wells (in yellow and green) are located to a different area of the substrate.

y. Independent Claim 41 of the ’222 Patent

(i) Preamble: “A semiconductor device comprising:

398. Claim 41, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(ii) Element [41.1]: “a substrate of a first doping type at a first doping level”

399. Claim 41, Element [41.1] is substantively identical to claim 1, Element [1.1] of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [41.2]: "a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

400. Claim 41, Element [41.2] is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "a surface of the substrate" which does not change my analysis as the surface discussed is the first surface which was already shown to contain active regions with transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(iv) Element [41.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

401. Claim 41, Element [41.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [41.4]: "transistors formed in at least one of the first active region or second active region;"

402. Claim 41, Element [41.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [41.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."

403. Claim 41, Element [41.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region" while Element [1.5] recites "graded dopant concentration." A POSITA would have understood that "acceptor concentration" and "dopant concentration" to be synonymous. Kawagoe discloses substrate body 2S in Figure 16 that has a bottom portion with no active regions and where the carrier movement flows from the first or second active regions. As previously discussed (II.C), the acceptor dopant concentration refers to p-type region which is disclosed in Kawagoe. For these reasons and the reasons described in claim 1, Element [1.5] of the '842 Patent, Kawagoe discloses this element.

404. Therefore, in light of the teachings in Kawagoe and the above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 41.

z. Independent Claim 42 of the ’222 Patent

(i) Preamble: “A semiconductor device comprising:

405. Claim 42, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element. The preamble of the ’842 Patent describes a semiconductor device..

(ii) Element [42.1]: “a substrate of a first doping type at a first doping level”

406. Claim 42, Element [42.1] is substantively identical to claim 1, Element [1.1] of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [42.2]: “a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”

407. Claim 42, Element [42.2] is substantively identical to claim 1, Element [1.2] of the ’842 Patent but recites “a surface of the substrate” which does not change my analysis as the surface discussed is the first surface which was already shown to contain active regions with transistors. Thus, this element is disclosed for the same reasons I described above for that element.

(iv) Element [42.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

408. Claim 42, Element [42.3] is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [42.4]: "transistors formed in at least one of the first active region or second active region; and"

409. Claim 42, Element [42.4] is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [42.5]: "at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region."

410. Claim 42, Element [42.5] is substantively identical to claim 1, Element [1.5] of the '842 Patent but recites "donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region." As described above, Kawagoe discloses the bottom portion of substrate 2S in Figure 16 that has no active regions and where the carrier movement flows from the first or second active regions. As previously discussed (II.C), the donor dopant concentration refers to n-type region which is disclosed in

Kawagoe. For these reasons and the reasons described in claim 1, Element [1.5], Kawagoe discloses this element.

411. Therefore, in light of the teachings in Kawagoe and the above explanations, Kawagoe discloses or renders obvious all claim elements and their combination in Claim 42.

E. '014 Patent

412. In this section, I analyze Claims 1, 3- 9, 13, 15-17, 20-21, 23-28 of the '014 Patent based on the same prior art applied to claims of the '842 Patent, '481 Patent and '222 Patent.

1. Ground II: Onoda Renders Obvious Claims 1, 3-9, 13, 15-17, 20-21, 23-28 of the '014 Patent

a. Independent Claim 1 of the '014 Patent

(i) Preamble: "An electronic system, the system comprising: at least one semiconductor device, the at least one semiconductor device including:"

413. Claim 1, preamble, is substantively identical to claim 1, preamble of the '842 Patent and is disclosed for the same reasons I described above for that element. The preamble of the '842 Patent describes a CMOS device, which is a semiconductor device. A POSITA would also consider a semiconductor device to be an electronic system because it is a circuit and conducts electricity.

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having a surface;"

414. Claim 1, Element [1.1], is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [1.2]: "a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

415. Claim 1, Element [1.2], is substantively identical to claim 1, Element [1.2] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [1.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed,"

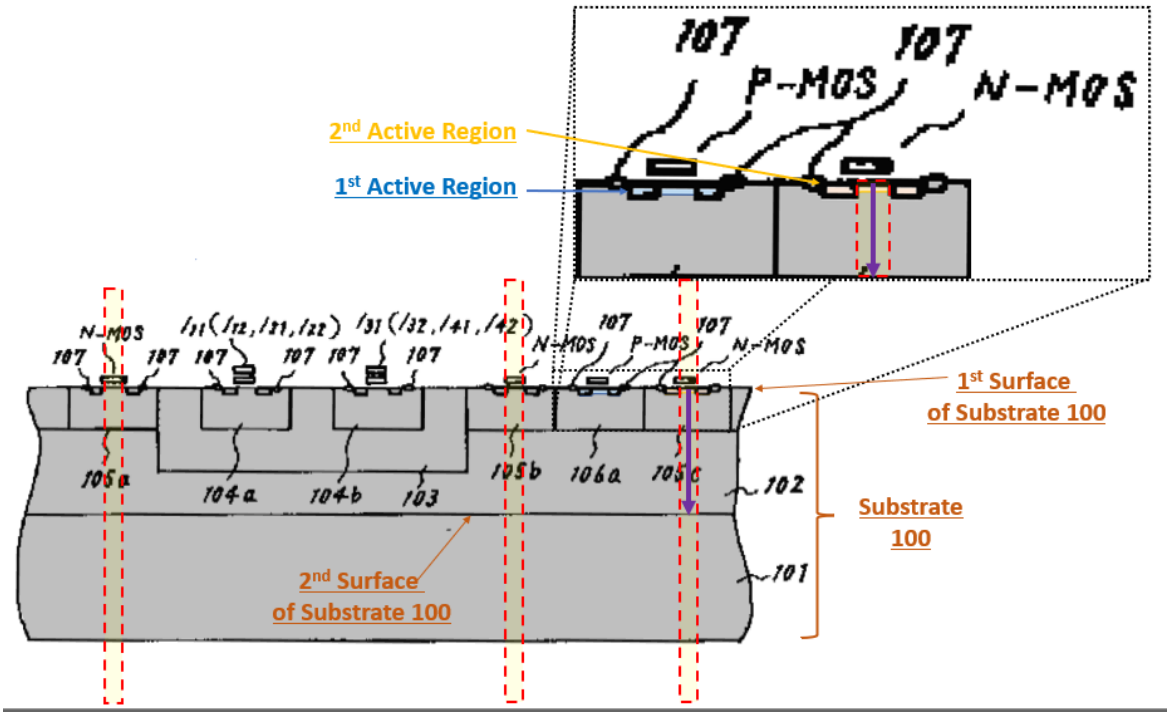
416. Claim 1, Element [1.3], is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [1.4]: "transistors formed in at least one of the first active region or second active region"

417. Claim 1, Element [1.4], is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

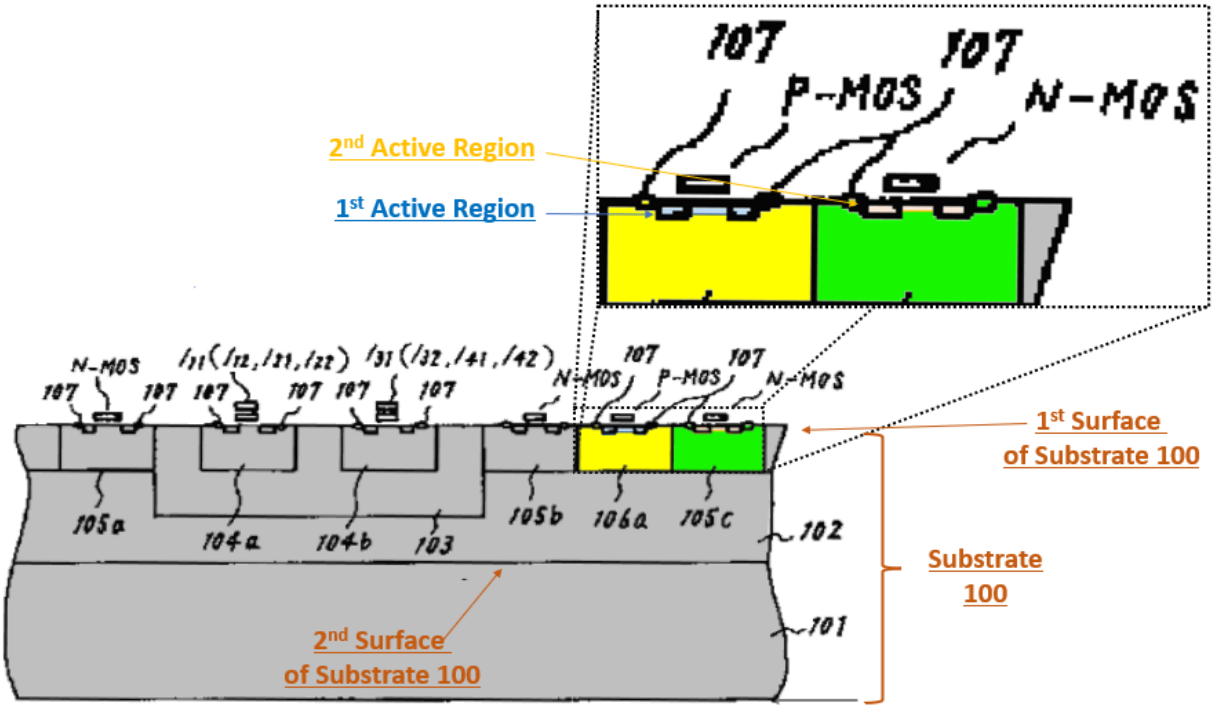
(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

418. Claim 1, Element [1.5], is substantively identical to claim 1, Element [1.5] of the '842 Patent and is disclosed for the same reasons I described above for that element, but recites "from the first and second active regions towards an area of the substrate where there is no active regions." As can be seen from FIG. 3 of Onoda below, along the direction of the carrier movement in lines B-B' or C-C' in FIGS. 3 and 8, there are no active regions in the area of the first semiconductor layer 101 of the substrate 100.



(vii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions"

419. Claim 1, Element [1.6] is a combination of claim 1, Element [1.2]-[1.5] but recites "the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions." As shown in figures 2 and 3, p-well 105c (green) is adjacent to the first active region (blue) and n-well 106a (yellow) is adjacent to the second active region (tan).



420. The p-well region 105c contains at least one graded dopant region as shown in FIG. 11 where the dopant concentration is shown to reduce as the depth of the device increases. And as previously discussed, this graded dopant concentration aids carrier movement from the surface to the area of the substrate where there are no active regions as the concentration decreases closer to the first semiconductor layer 101.

(viii) Element [1.7]: "wherein at least some of the transistors form digital logic of the semiconductor device."

421. Further, a POSITA would have understood that the teachings of Onoda were not limited to the disclosed flash memory and would be applicable to digital logic applications on semiconductor devices. (II.C.)

422. Therefore, in light of the teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 1.

b. Dependent Claim 3 of the '014 Patent: "The system of claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

423. Claim 3 is substantively identical to claim 4 of the '842 Patent and is disclosed for the same reasons I described for claim 4 of the '842 Patent.

c. Dependent Claim 4 of the '014 Patent: "The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices."

424. Claim 4 is substantively identical to claim 5 of the '842 Patent and is disclosed for the same reasons I described for claim 5 of the '842 Patent. Further, a POSITA would have understood that the teachings of Onoda were not limited to the disclosed flash memory and would be applicable to digital logic applications on semiconductor devices. (II.C.)

d. Dependent Claim 5 of the ’014 Patent: “The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

425. Claim 5 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent.

e. Dependent Claim 6 of the ’014 Patent: “The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.”

426. Claim 6 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

f. Dependent Claim 7 of the ’014 Patent: “The system of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

427. Claim 7 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 8 of the ’842 Patent.

g. Dependent Claim 8 of the ’014 Patent: “The system of claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.”

428. Claim 8 is substantively identical to claim 17 of the ’842 Patent and is disclosed for the same reasons I described for claim 17 of the ’842 Patent.

h. Dependent Claim 9 of the ’014 Patent: “The system of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.”

429. Claim 9 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. In Onoda, the second active region is located in a p-well region 105a, 105b or 105c on the semiconductor device which has a graded dopant concentration as shown in FIG. 11 where the doping is p-type.

i. Dependent Claim 13 of the ’014 Patent: “The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.”

430. Claim 13 is substantively identical to claim 18 of the ’842 Patent and is disclosed for the same reasons I described for claim 18 of the ’842 Patent. Further, a POSITA would have understood that the teachings of Onoda were not limited to the disclosed flash memory and would be applicable to digital logic applications. (II.C.)

j. Dependent Claim 15 of the ’014 Patent: “ The system of claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.”

431. Claim 15 recites a combination of different claim limitations in claim 4 and claim 18 of the ’842 Patent in a slightly different way: “wherein the device is a

complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate." The claim does not foreclose the device having an epitaxial substrate and as previously discussed. Onoda discloses both an epitaxial substrate part (second semiconductor layer 102) and nonepitaxial substrate part (first semiconductor layer 101) of its substrate 100. Onoda discloses Claim 15 for the same reasons I described for claim 4 and claim 18 of the '842 Patent.

k. Dependent Claim 16 of the '014 Patent: "The system of claim 1, wherein the at least one semiconductor device is a flash memory.

432. Onoda discloses flash memory semiconductor devices. ((Onoda at [0040]-[0043] and FIGS. 1, 2 and 3)

l. Dependent Claim 17 of the '014 Patent: " The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors."

433. Onoda renders obvious this claim. Onoda discloses flash memory semiconductor devices. (Onoda at [0040]-[0043] and FIGS. 1, 2 and 3.) In addition, a POSITA would have understood that the doping gradient aspect of the flash memory semiconductor devices would be useful in logic devices as both memory and logic devices suffer from issues related to minority carrier movement. (II.C.) Onoda discloses using capacitors. (Onoda at [0089]; FIG. 17.)

m. Dependent Claim 20 of the ’014 Patent: “ The system of claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.”

434. The ’014 Patent does not explain which direction is lateral or vertical. Nonetheless, this element is disclosed in Onoda. The different active regions are spread across the surface of the substrate including adjacent p and n-wells and this configuration gives the different active regions relative to one another in a “lateral direction.” The different active regions are spread down into a portion of the well with respect to the top surface of the substrate layer 102, which gives them each a relative position in the “vertical direction” with respect to the top surface of the substrate layer 102. (*See* FIG. 2 and 3.)

n. Independent Claim 21 of the ’014 Patent

(i) Preamble: “An electronic system, comprising: at least one semiconductor device, the at least one semiconductor device including:”

435. Claim 21, preamble, is substantively identical to claim 1, preamble, of the ’842 Patent and is disclosed for the same reasons I described above for that element. The preamble of the ’842 Patent describes a semiconductor device. A POSITA would also consider a semiconductor device to be an electronic system because it is a circuit and conducts electricity.

(ii) Element [21.1]: "a substrate of a first doping type at a first doping level having a surface;"

436. Claim 21, Element [21.1], is substantively identical to claim 1, Element [1.1] and the substrate limitation of Claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element. The first surface identified in claim 1 and 9 of the '842 Patent is the claimed surface for claim 21, Element [21.1], but does not change my analysis.

(iii) Element [21.2]: " a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

437. Claim 21, Element [21.2], is substantively identical to claim 1, Element [1.2] of the '842 Patent but recites "in the surface thereof" in a way substantively similar to Claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [21.3]: " a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof,"

438. Claim 21, Element [21.3], is substantively identical to claim 1, Element [1.3] of the '842 Patent but recites "in the surface thereof" in a way substantially similar to Claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [21.4]: " transistors formed in at least one of the first active region or second active region"

439. Claim 21, Element [21.4], is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [21.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and"

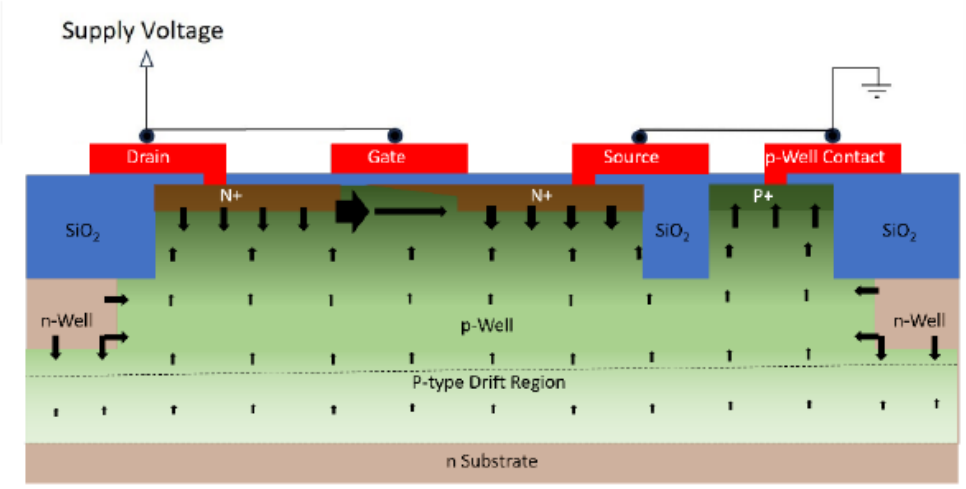
440. Claim 21, Element [21.5], is substantively identical to claim 1, Element [1.5] of the '842 Patent and is disclosed for the same reasons I described above for that element, but recites "from the surface to an area of the substrate where there are no active regions" As can be seen from Figures 2 and 3 of Onoda, there are no active regions in the area 101 of the substrate which is the direction the carrier movement is being aided toward.

(vii) Element [21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

441. Claim 21, Element [21.6] is substantively identical to claim 1, Element [1.6] of the '014 Patent but recites "wherein the graded dopant concentration is

linear, quasilinear, error function, complementary error function, or any combination thereof."

442. Onoda teaches several dopant gradient profiles, in addition to providing graphical depictions of profiles that to a POSITA render a quasi-linear gradient obvious. For instance, Onoda teaches a gaussian distribution of dopants. (Onoda at [0053] ("the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate Gaussian distributions with the concentrations at maxima near the surface").) Moreover, providing a quasi-linear gradient was well-known, and this is confirmed by the '842, '481, '222, and '014 Patents describing them amongst a list of known profiles. ('014 Patent at 3:5-6 ("The gradient can be linear, quasi linear, exponential or complimentary error function.)) It would have been obvious to apply a quasi-linear gradient in view of a POSITA's general knowledge that such a gradient facilitates the movement of minority carriers. It would have further been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile, and would have been readily available as a known option. As shown in the figure below, the unidirectional doping gradient produces a unidirectional electric field.



Linearly graded profile with the graded drift region matching the bottom of the well

443. Therefore, in light of the teachings in Onoda and the above explanations, Onoda discloses or renders obvious all claim elements and their combination in Claim 21.

o. Dependent Claim 23 of the '014 Patent: "The system of claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate."

444. Onoda discloses a p-type substrate. Onoda's flash memory has "a semiconductor substrate 100." (Onoda at [0041] ("FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention").) Element 101 "is a first semiconductor layer made from a heavily-doped … P-type silicon substrate." (*Id*.; see also id. at [0041]; *see also id*. at "Brief

Description of the Drawings" describing FIGS. 1 through 14 as describing features of the "first embodiment.")

p. Dependent Claim 24 of the '014 Patent: "The system of claim 21, wherein the substrate of the at least one semiconductor device, has epitaxial silicon on top of a nonepitaxial substrate.

445. Claim 24 is substantively identical to claim 4 of the '842 Patent and is disclosed for the same reasons I described for claim 4 of the '842 Patent.

q. Dependent Claim 25 of the '014 Patent: "The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices."

446. Claim 25 is substantively identical to claim 5 of the '842 Patent and is disclosed for the same reasons I described for claim 5 of the '842 Patent.

r. Dependent Claim 26 of the '014 Patent: "The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

447. Claim 26 is substantively identical to claim 6 of the '842 Patent and is disclosed for the same reasons I described for claim 6 of the '842 Patent.

s. Dependent Claim 27 of the ’014 Patent: “The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.”

448. Claim 27 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

t. Dependent Claim 28 of the ’014 Patent: “The system of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.”

449. Claim 28 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. The active regions are located in n-wells and p-wells on the semiconductor device which have a graded dopant concentration as shown in their respective doping profiles (FIGS. 11 and 12) where the doping is either p-type or n-type.

2. Ground III: Onoda in view of Nishizawa Renders Obvious Claims 1, 3-9, 13, 15-17, 20-21, 23-28 of the ’014 Patent

450. I incorporate my analysis regarding the motivation to combine Onoda and Nishizawa as provided for the ’842 Patent, Ground III in section III.B.2.

a. Independent Claim 1 of the '014 Patent

(i) Preamble – Element [21.4] and Element [21.7]

451. Consistent with Ground II, Onoda discloses and/or renders obvious the Preamble through Element [1.4] and [1.7] under the combination of Onoda and Nishizawa.

(ii) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

452. For the same reasons I described above in Ground II for Element [1.5] this element is rendered obvious. Further, Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions (i.e., substrate 101). (III.B.2)

(iii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,"

453. For the same reasons I described above in Ground II for Element [1.6] this element is rendered obvious. Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the surface towards the area of the substrate where there are no active regions (i.e., substrate 101). (III.B.2)

454. Therefore, in light of the combined teachings in Onoda and Nishizawa and the above explanations, the combination of Onoda and Nishizawa discloses or renders obvious all claim elements and their combination in Claim 1.

b. Independent Claim 21 of the '014 Patent

(i) Preamble – Element [21.4] and Element [21.7]

455. Consistent with Ground II, Onoda discloses and/or renders obvious the Preamble through Element [21.4] and [21.7] under the combination of Onoda and Nishizawa.

(ii) Element [21.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and"

456. For the same reasons I described above in Ground II for Element [21.5] this element is rendered obvious. Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the surface to an area of the substrate where there are no active regions (i.e., substrate 101). (III.B.2)

(iii) Element [21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

456. For the same reasons I described above in Ground II for Element [21.6] this element is rendered obvious. Nishizawa explicitly provides that the graded dopant regions aid carrier movement from the surface to the area of the substrate where there are no regions (i.e., substrate 101). (III.B.2)

3. Ground I: Kawagoe Renders Obvious Claims 1, 3-9, 13, 15-17, 20-21, 23-28 of the '014 Patent

a. Independent Claim 1 of the '014 Patent

(i) Preamble: "An electronic system, the system comprising: at least one semiconductor device, the at least one semiconductor device including:"

457. Claim 1, preamble, is substantively identical to claim 1, preamble, of the '842 Patent and is disclosed for the same reasons I described above for that element. The preamble of the '842 Patent describes a semiconductor device. A POSITA would also consider a semiconductor device to be an electronic system because it is a circuit and conducts electricity.

(ii) Element [1.1]: "a substrate of a first doping type at a first doping level having a surface;"

458. Claim 1, Element [1.1], is substantively identical to claim 1, Element [1.1] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iii) Element [1.2]: " a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

459. Claim 1, Element [1.2], is substantively identical to claim 1, Element [1.2] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [1.3]: " a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed,"

460. Claim 1, Element [1.3], is substantively identical to claim 1, Element [1.3] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [1.4]: " transistors formed in at least one of the first active region or second active region"

461. Claim 1, Element [1.4], is substantively identical to claim 1, Element [1.4] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and"

462. Claim 1, Element [1.5], is substantively identical to claim 1, Element [1.5] of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vii) Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions"

463. Claim 1, Element [1.6] is substantively identical to claim 1, Element [1.6] of the '481 Patent but recites "the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions." As shown in Kawagoe Figure 16, there are no active regions in the bottom portion of substrate body 2S. The active regions are located in a different area of the substrate. Kawagoe also discloses a logic device. Kawagoe states "the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31.)

(viii) Element [1.7] "wherein at least some of the transistors form digital logic of the semiconductor device."

464. Claim 1, Element [1.7] is substantively identical to claim 1, Element [1.7] of the '481 Patent and is disclosed for the same reasons I described for claim 1 of the '481 Patent.

b. Dependent Claim 3 of the '014 Patent: "The system of claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

465. Claim 3 is substantively identical to claim 4 of the '842 Patent and is disclosed for the same reasons I described for claim 4 of the '842 Patent.

c. Dependent Claim 4 of the '014 Patent: "The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices."

466. Claim 4 is substantively identical to claim 5 of the '842 Patent and is disclosed for the same reasons I described for claim 5 of the '842 Patent. Further, Kawagoe discloses a logic device. Kawagoe states "the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31.)

d. Dependent Claim 5 of the ’014 Patent: “The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

467. Claim 5 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent.

e. Dependent Claim 6 of the ’014 Patent: “The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.”

468. Claim 6 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for claim 7 of the ’842 Patent.

f. Dependent Claim 7 of the ’014 Patent: “The system of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

469. Claim 7 is substantively identical to claim 8 of the ’842 Patent and is disclosed for the same reasons I described for claim 8 of the ’842 Patent.

g. Dependent Claim 8 of the ’014 Patent: “The system of claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.”

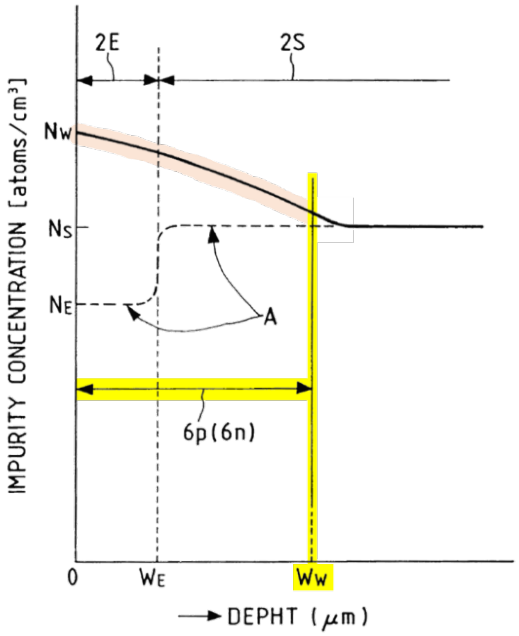
470. Claim 8 is substantively identical to claim 17 of the ’842 Patent and is disclosed for the same reasons I described for claim 17 of the ’842 Patent.

h. Dependent Claim 9 of the ’014 Patent: “The system of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.”

471. Claim 9 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for claim 6 of the ’842 Patent. In Kawagoe, the second active region is located in -a p-well 6p on the semiconductor device and has a graded dopant concentration as shown in the doping profile (FIG. 17 (tan line)) where the doping is p-type. Kawagoe also discloses a first active region located in an n-well 6n on the semiconductor device and has a graded dopant concentration as shown in the doping profile in FIG. 17 where the doping is n-type.

472.

FIG. 17



i. Dependent Claim 13 of the '014 Patent: "The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel."

473. Claim 13 is substantively identical to claim 18 of the '842 Patent and is disclosed for the same reasons I described for claim 18 of the '842 Patent. Further, Kawagoe discloses a CMOS logic device. Kawagoe states "the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called 'microcomputer.'" (Kawagoe at 24:28-31, *id*. at 8:46-54 ("The element forming region, as enclosed by the field insulating film 3, is formed for example with an n-channel MOS.FET (as

will be shortly referred to as 'nMOS') 4N and [] p-channel MOS.FET (as will be shortly referred to as 'pMOS') 4P, and these nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit.").)

j. Dependent Claim 15 of the '014 Patent: " The system of claim 1, wherein at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate."

474. Claim 15 is substantively identical to claim 4 and claim 18 of the '842 Patent yet recites "wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate." The claim does not foreclose the device having an epitaxial substrate and as previously discussed, Kawagoe discloses both an epitaxial substrate layer 2E and nonepitaxial body substrate 2S for its substrate 2. This limitation is disclosed for the same reasons I described for those elements.

k. Dependent Claim 16 of the '014 Patent: "The system of claim 1, wherein the at least one semiconductor device is a flash memory.

475. Kawagoe discloses its technique is applicable for flash memory. (Kawagoe at 23:12-13 ("[I]t is possible to improve the performance, reliability and production yield of flash memory (i.e., EEPROM)."), 24:21-27.)

l. Dependent Claim 17 of the ’014 Patent: “ The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.”

476. Claim 17 is substantively identical to claim 17 of the ’222 Patent and is disclosed for the same reasons I described for that element.

m. Dependent Claim 20 of the ’014 Patent: “ The system of claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.”

477. The ’014 Patent does not explain which direction is lateral or vertical. Nonetheless, Kawagoe discloses this element. The active regions in 6p and 6n well regions in Kawagoe are spread across the top surface of the substrate layer 2E of the substrate 2, which gives them each a position relative to one another in the lateral direction. The active regions in 6p and 6n well regions in Kawagoe are also spread down into a portion of their respective well regions, which gives the active regions each a position in the vertical direction with respect to the top surface of the substrate layer 2E of the substrate 2. (*See* FIG. 16.)

n. Independent Claim 21 of the ’014 Patent

(i) Preamble: “An electronic system, the system comprising: at least one semiconductor device, the at least one semiconductor device including:”

478. Claim 21, preamble, is substantively identical to claim 1 and 9 of the ’842 Patent and is disclosed for the same reasons I described above for that

element. The preamble of the ’842 Patent describes a semiconductor device. A POSITA would also consider a semiconductor device to be an electronic system because it is a circuit and conducts electricity.

(ii) Element [21.1]: “a substrate of a first doping type at a first doping level having a surface;”

479. Claim 21, Element [21.1], is substantively identical to claim 1, Element [1.1] and the substrate limitation of claim 9 of the ’842 Patent and is disclosed for the same reasons I described above for that element. The first surface identified in claim 1 of the ’842 Patent is the claimed surface for claim 21, Element [21.1], but does not change my analysis.

(iii) Element [21.2]: “ a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;”

480. Claim 21, Element [21.2], is substantively identical to claim 1, Element [1.2] but recites “in the surface thereof” in a way substantially similar to claim 9 of the ’842 Patent and is disclosed for the same reasons I described above for that element.

(iv) Element [21.3]: " a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof,"

481. Claim 21, Element [21.3], is substantively identical to claim 1, Element [1.3] but recites "in the surface thereof" in a way substantially similar to claim 9 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(v) Element [21.4]: " transistors formed in at least one of the first active region or second active region"

482. Claim 21, Element [21.4], is substantively identical to claim 1, Element [1.4] and claim 9, Element 9.4 of the '842 Patent and is disclosed for the same reasons I described above for that element.

(vi) Element [21.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and"

483. Claim 21, Element [21.5], is substantively identical to claim 1, Element [1.5] and claim 9, Element [9.5] of the '842 Patent and is disclosed for the same reasons I described above for that element, but recites "from the surface to an area of the substrate where there are no active regions." As shown in Kawagoe Figure 16, there are no active regions in the bottom portion of substrate body 2S of the substrate 2. The active regions are located in a different area of the substrate.

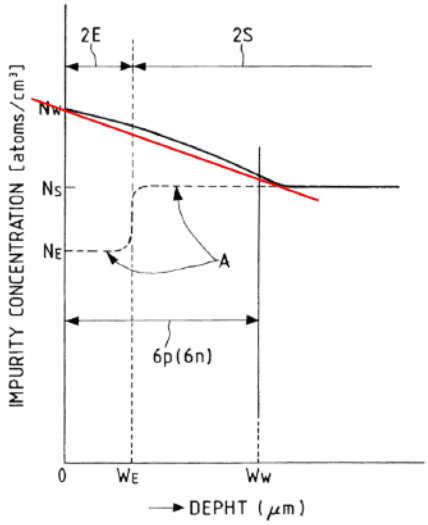
(vii) Element [21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions,"

484. The above portion of Claim 21, Element [21.6] is substantively identical to claim 1, Element [1.6] of the '014 Patent but recites "from the surface to the area of the substrate where there are no active regions," As shown in Kawagoe Figure 16, there is no active region in the bottom portion of the body substrate 2S of the substrate 2.

(viii) Element [21.6] (Continued) "and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

485. Further, FIG. 17 depicts a graded concentration. (Kawagoe at 16:16-40.) However, the vertical axis is not defined. As a result, a POSITA would not be able to discern if FIG. 17 depicts a quasi-linear or exponential gradient. If it is intended to be a linear scale, a linear gradient is depicted in red). As discussed earlier, either type of profile would improve the transport of minority carriers to the substrate.

FIG. 17



486. Moreover, a POSITA would have also found it obvious to use a quasi-linear gradient because it was a simple usage of one known method. The '195 Patent only mentions quasi-linear gradient once ('014 Patent at 3:5-6) and does not illustrate or otherwise describe it, or describe any process steps for obtaining it confirming that such a gradient was a well-known alternative to a POSITA. It would have been obvious to modify Kawagoe's dopant profile based on the POSITA's general knowledge in the art to achieve a known quasi-linear gradient. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another

while retaining the same known benefit of aiding minority carrier movement with a reasonable expectation of success

o. Dependent Claim 23 of the ’014 Patent: “The system of claim 1, wherein the substrate of the at least on semiconductor device is a p-type substrate.”

487. Kawagoe discloses this element. Kawagoe layers 2E and 2S are part of the semiconductor wafer prior to forming the diffusion layer. (See Kawagoe at FIGS. 20 and 21.) The substrate body 2S is made of a p-type Si single crystal that is initially formed with a p type impurity such as boron and the epitaxial layer 2E is made up of a p-type Si single crystal. (Id. at 14:61-15:16.) The layers contain the same p-type doping to satisfy this limitation.

p. Dependent Claim 24 of the ’014 Patent: “The system of claim 21, wherein the substrate of the at least one semiconductor device, has epitaxial silicon on top of a nonepitaxial substrate.

488. Claim 24 is substantively identical to claim 4 of the ’842 Patent and is disclosed for the same reasons I described for that element.

q. Dependent Claim 25 of the ’014 Patent: “The system of claim 21, wherein the first active region and second active region of the at least one of either p-channel and n-channel devices.”

489. Claim 25 is substantively identical to claim 5 of the ’842 Patent and is disclosed for the same reasons I described for that element.

r. Dependent Claim 26 of ’014 Patent: “The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

490. Claim 26 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element.

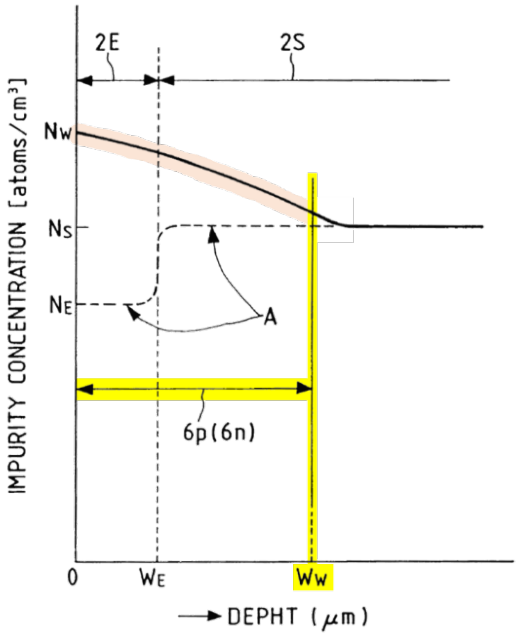
s. Dependent Claim 27 of the ’014 Patent: “The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.”

491. Claim 27 is substantively identical to claim 7 of the ’842 Patent and is disclosed for the same reasons I described for that element.

t. Dependent Claim 28 of the ’014 Patent: “The system of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.”

492. Claim 28 is substantively identical to claim 6 of the ’842 Patent and is disclosed for the same reasons I described for that element. In Kawagoe, the second active region is located in p-well on the semiconductor device and has a graded dopant concentration as shown in the graded doping profile (FIG. 17) where the doping is p-type.

FIG. 17



IV. CONCLUSION

493. Based on my review and analysis, it is my opinion that claims 1,2, 4-9, and 12-18 of the '842 Patent, claims 1-9, 13, 15, 17, 20, 22-27, 31, 32, and 34 of the '481 Patent, claims 1, 3-9, 13, 15-17, 20-21, 24-28, 32-34, and 39-42 of the '222 Patent, and claims 1, 3-9, 13, 15-17, 20, 21, and 23-28 of the '014 Patent are invalid as obvious by: (1) Onoda; (2) Onoda and Nishizawa; and (3) Kawagoe.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001; and further that such willful false statements may jeopardize the validity of the application or any patent issued thereon. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on __March 18, 2024_____ in __Arden Hills, Minnesota_____.

Stephen Campbell

Stephen Campbell

Curriculum Vitae
Stephen A. Campbell



Educational History

PhD	Physics	Northwestern University	1981
MS	Physics	Northwestern University	1978
BA	Physics	College of St. Thomas	1975

Employment History

1986 – 2023 University of Minnesota
- Emeritus Professor
- Director, Minnesota Nano Center (1999 – 2021)
- Penrose Professorship in Science and Engineering (2015 – 2021)
- Bordeau Chair in Electrical and Computer Engineering (2007 - 2015)
- Professor of Electrical and Computer Engineering (1998 - Present)
- Associate Professor of Electrical Engineering (1992 - 1998)
- Assistant Professor of Electrical Engineering (1986 - 1992)
- Presidential Young Investigator

Professor Campbell is very active in education, research, and service to the university. In the first, he leads the University's participation in Nano-Link, an NSF sponsored regional center for nanotechnology education at the AAS level. He has designed and implemented a one-semester capstone experience that is considered to be one of the best in the country. Professor Campbell is the author of *Fabrication Engineering at the Micro and Nanoscale*, one of the most widely used textbook on microfabrication. This text has been used in more than 60 US schools as well as many schools in Europe and Asia. After more than a dozen printings, it is now entering its fourth edition. Professor Campbell's teaching experience includes Microfabrication, Semiconductor Devices, Electromagnetic Fields, Analog Electronics, Linear Circuits, Circuits Lab, Senior Design, and Materials and Devices. In research, Professor Campbell is most well-known for pioneering efforts in high permittivity (aka high-k) materials for the gate insulator in deeply scaled MOSFETs. This revolution in transistor design has now been adopted by most of the leading-edge integrated circuit manufacturers. His other current interests include ultra-high-speed MEMS and efficient thin film photovoltaics. Professor Campbell serves as the Minnesota lead for the National Nanotechnology Coordinated Infrastructure (NNCI) network, established by NSF to support nanotechnology research. He directs the University's Nano Center (www.mnc.umn.edu) where has developed funding for many new pieces of equipment including a 2.5 M$ direct write e-beam lithography. Most recently he has been instrumental in developing support for construction of a new Physics and Nanotechnology Building.

1981-86 Sperry (Unisys), Semiconductor Operations
- Device Physicist, 1981-83
- Manager, MOS Process Development, 1983-84
- Manager, Silicon Research, 1984-86

Dr. Campbell held a variety of positions within Sperry relating to the research and development of high-speed silicon devices. He was the principal architect of Sperry's 1.25 micron CMOS technology. Dr. Campbell managed Sperry's silicon research group where he initiated and directed work in 0.5 micron CMOS, laser photochemical deposition, silicon SOI, super self aligned bipolar devices for high speed ECL, polyimide dielectrics, and novel BiMOS design approaches. He also represented Sperry on the Technical Advisory Board of the Semiconductor Research Corporation.

Consulting

2019-2021	Wilmer-Hale, Advanced CMOS Litigation
2008:	3M, Optoelectronic Devices
2005-2007	CIMA Nanotech: Nanoparticle materials
2004-2005:	Precision Press: Thin film devices
2003-2004:	Ennovato, Inc. A startup working on novel transistors for thin film displays
1997-2000:	Offered IC fabrication short courses through UC Berkeley and independently
1997	Fusion Semiconductor Developed a design for radiative heating of 300 mm wafers.
1994-96	FSI Corporation Studied effects of wafer cleaning steps on gate oxide quality
1991-93	AG Associates, Modeling and design of rapid thermal processing equipment.
1992, 94	National Science Board, Naval Studies Board (JAST)
1989-92	Institute for Defense Analysis Participant, Defense Sciences Study Group

Professional Activities and Affiliations

Life Fellow, IEEE
Conference Committee, Semiconductor Interface Specialists Conference (2002-2004)
Associate Editor, Journal of Semiconductor Technology and Science (2002- present)
Symposium Organizer, Gate Stacks, Materials Research Society Spring Meeting (MRS), 2000, 2001
Executive Committee and Technical Committee member, Bipolar Circuits and Technology Meeting (IEEE), 1995, 1996, 1997
Symposium Organizer, GeSi and Related Materials, Materials Research Society Spring Meeting (MRS), 1996
Member, Technical Advisory Board, Semiconductor Research Corp, 1983-86
Reviewer
IEEE Transactions of Electron Devices
IEEE Electron Device Letters
Journal of Applied Physics
Journal of the Electrochemical Society
Journal of Vacuum Science and Technology

Awards and Honors

Russell J. Penrose Professorship in Science and Engineering (2015)
George W. Taylor Award for Distinguished Service, 2011
Sanford P. and Lenore Edgerton Bordeau Chair in Electrical and Computer Engineering (2007)
Institute of Electrical and Electronic Engineers (IEEE) Fellow 2007
Institute of Technology Distinguished Professor, 2006
George W. Taylor Award for Distinguished Teaching, 2005
IBM University Partnership Award, 1998
Outstanding EE Instructor Award, Inst of Technology Student Board, 1991
Presidential Young Investigator (National Science Foundation) 1989
Engineering Initiation Award (National Science Foundation) 1987
Sperry Outstanding Technical Achievement Award, 1986
President's Fellow, Northwestern University 1976 - 1977
Argonne National Laboratory Research Participant 1978 -1981

Graduate Students Advised - Degrees Completed

PhD

1. Abhimanyu Ravinadrath – "High Density Chronic Neural Probes PhDEE 2023.
2. Nezhueyotl Izquierdo – "Thin Film Growth of Black Phosphorus and Black Arsenic Phosphorus" (MatSci), September 2020.
3. Tim Bontrager – "Optimizing the Interactions Between the Buffer and Barrier Layers for CIGS Based Tandem Photovoltaics", PhDEE February 2019
4. Sehyun Wang – Growth and Characterization of Wide Bandgap CIAGS Solar Cell Material and Devices, PhDEE December 2018
5. Brian Benton – Electronic Transport in Semiconductor Nanocrystal Thin Films – PhDEE May 2018
6. Mandip Sibokati – Electrical Characterization and Device Modeling to Study Degradation Mechanisms in CIAGS Solar Cells– PhDEE June 2017
7. Liyuan Zhang – Earth Abundant CZTS Solar Cells – PhDEE 2016
8. Jun Young Lim – CNT Films and Processing, PhDEE 2015
9. Forrest Johnson – Broken Gap Junctions for Tandem Solar Cells – PhDEE 2015
10. Brijesh Kumar – Modeling of Embedded Quantum Dot Structures PhDEE 2013
11. Sang Ho Song – Characterization and Modeling of PV Devices – PhDEE 2013
12. Dan Yu – Si Nanoparticle Composites – PhDEE 2012
13. Maryam Jalali – An IR Scene Projector – PhDEE 2011
14. Min Woo Jang – Low Mass NEMS Switch – PhDEE 2011
15. Richard Liptak – Passivation of Si Nanoparticles – PhDEE 2009
16. Rebeccah Ligman - Si Nanoparticles in Organic LEDs– PhDEE May, 2007
17. Min Li – "Development and Characterization of Ultrathin Hafnium Titinates and High Permittivity Gate Insulators", Oct, 2005
18. Zhihong Zhang – "Hafnium Oxide gate Dielectrics for Deeply Scaled MOSFETs", Oct 2005
19. Ying Dong – Devices Made on Single Crystal Silicon Nanoparticles" – Sept. 2005
20. Zhe Shen – Nano-sized Silicon Particle Formation in Silane HDP", Sept 2004
21. Noel Hoilien – "Zirconium Based High k Materials", PhDEE, May 2004
22. Fang Chen – "Hafnium Based High k Materials", PhDEE Jan 2004
23. Taesung Kim - "Particle Measurement and Transport in SiO_2 CVD and Si HDPCVD", PhDME, March, 2002 (co-advised with Peter McMurry)
24. Tiezong Ma – High Permittivity Materials, PhDEE, August 2001 (co-advised with Wayne Gladfelter)
25. Boyong He – "High Permittivity FETs", March, 2000
26. Sandeep Nijawan - "Particle Measurement and Control in Silane CVD", PhDME, December, 1998 (co-advised with Peter McMurry)
27. David Gilbert - "The Deposition and Characterization of TiO_2 from Titanium Tetrakis Isopropoxide and from Tetrakis Nitrato Titanium", PhD Chem, May, 1998 (co-advised with Wayne Gladfelter)
28. Hyeong Saug Kim - "Electrical Characteristics and Reliability of High Permittivity FETs", PhDEE, March, 1998
29. Richard Tran - "GeSi Based Microwave ICs", July, 1995
30. Jinhua Yan - "High ε Dielectrics for MOS Transistors", March, 1995
31. John Leighton - "Rapid Thermal Vapor Phase Epitaxy - A Technique for Growing Thin Films of Silicon and Germanium-Silicon on Silicon", April, 1994
32. Karson Knutson - "Modeling of the Thermal Uniformity and Gas Phase Reactions in a Rapid Thermal Epitaxy System", August, 1993
33. Weihua Liu - "Performance of Deep Submicron GeSi Devices", June, 1993
34. Kyungho Lee - "Radiation Damage in Ultra Thin Dielectric Layers", May, 1993

MSEE

1. Maryam Jalali – A Restricted Channel Gas Sensor - January 2009
2. Gagan Aggrawal – Optical Transistor – August 2008
3. Richard Liptak – Passivation of Silicon Nanoparticles – August 2006
4. Bek Ligman – Nanoparticle LEDs June 2006
5. Dan Yu – CVD of SrHfO3 – MSEE, May, 2006
6. Niles Graf– Fine Alignment of an E-Beam Lithography System – MSEE, April, 2005
7. Paul Chen – CVD of Ternary High-k Materials MSEE May, 2005
8. Sharon Hilchie – "Si Nanoparticle Processing" MSEE, September 2004
9. Bek Ligman – "A Fine Comb Structure for Integrated Gas Sensors", MSEE, May 2004
10. Ying Dong – "Formation of Single Crystal Si Nanoparticles", MSEE, September 2003
11. Xiaorong Shi – "UHV Nitrides", MSEE, March 2003
12. Fang Chen – "Deposition of Titanium Nitride", MSEE June 2002
13. Henry Utomo – "A Control System for an ALD Reactor", MSEE June, 2001
14. Robert Rassel – "Particle Formation During Low-Pressure Chemical Vapor Deposition Of Silicon Dioxide From Silane And Oxygen: Measurement And Film Properties", MSEE June, 2001
15. Richard Rassel – "A Solenoid Type Microtransformer and Its Fabrication", MSEE June 2001
16. Mark Shriver – "UHV Nitridization", MSEE April, 2001
17. Hans Christianson "High Resistance Silicon Devices", MSEE March, 1999
18. Zhang Wu - Ultrafine Particle Control in Tungsten CVD, MSEE, May, 1998
19. Rongshan Wang - Semi-insulating Silicon, MSEE, April, 1998
20. Ray Tan – "High Resistance Silicon", MSEE, April, 1997
21. Bret Schwab - Effects of Surface Preparation on MOS Reliability, MSEE, July, 1996
22. Jay Meyer - Production and Performance of Semi-Insulating Silicon, MSEE, June, 1996
23. Hyeong Saug Kim - "Reliability of Ultrathin SiO_2", MSEE, May, 1994
24. Kai Ping Liu - Charge Pumping Measurements of Silicon MOSFETs, MSEE, February, 1992
25. Martin Kale - "Spreading Resistance Depth Profiling", MSEE, October 1991
26. Gregory Case - "Detection of Defects in Integrated Circuit Interconnects", MSEE, July, 1991
27. Karson Knutson - "Numerical Analysis of Rapid Thermal Processing", MSEE, April, 1991
28. Kyungho Lee - "Wafer Level Reliability Tests of IC's", MSEE, March, 1991
29. Kaseem Hamze - "Temperature Dependence of GeSi Mobility", January, 1991
30. Ling Shang - Particles in LPCVD Silicon Nitride", October, 1990
31. John Leighton - "Rapid Thermal Vapor Phase Epitaxy", November, 1989
32. Steve Guccione - "DC MOSFET Parameter Extraction", May, 1989

Synopsis of Research Accomplishments
Director, Minnesota Nano Center

Over the period 9/99 to the present, Professor Campbell has served as the Director of the MicroTechnology Lab, which changed its name in 2003 to the NanoFabrication Center. With a staff of 14 permanent employees and an annual budget of approximately 1.9 M$, the NFC has as its charter to act as a central resource at the University for all work involving the fabrication of micro and nano structures. The Lab is heavily used by many Departments at the University including EE, CEMS, ME, Physics, Chemistry, Plant Biology, Cellular Biology, and Biomedical Engineering. In addition, the Lab hosts outside users including many companies and researchers from other institutions.

During the period of Professor Campbell's appointment, the Lab upgraded its facilities considerably. One of the major accomplishments was the addition of a nanotechnology capability. Professor Campbell led the acquisition of a direct write electron beam lithography system and ultimately to a state of the art, 6 nm Vistec system. This machine has been widely adopted by academic users and has been augmented by a nano imprint tool. Lithography capabilities have also expanded with an i-line exposure tool. At the same time the Lab upgraded its sputtering capability, replacing a system built in the 1970's with two state of the art tools which are much better suited to the current faculty needs. Professor Campbell has started new Lab initiatives. As a result of this and other innovative incentive programs, usage of the Lab by University faculty has increased by a factor of five over his tenure. The lab conservatively estimates that these facilities enable approximately 10 M$ of research annually. This growth has led to the development of support for a new building, include a 10,000 square foot (5000 under filter) clean room which will be the primary facility for nano research for current and future University researchers. This building was occupied in late 2013.

Professor Campbell has successfully allied the Laboratory with Stanford, Cornell, and 11 other schools in a successful bid to become the National Nanotechnology Infrastructure Network (NNIN). This activity began in April, 2004, and has been renewed to March 2014. In 2015, Professor Campbell successfully led a team to ensure Minnesota participation in the follow-on NSF program, the National Nanotechnology Coordinated Infrastructure (NNCI) program. NNCI will provide support to critical nano facilities until at least 2020 and, if renewed, until 2025. Professor Campbell has also worked with local community colleges to spearhead a successful bid to develop a new nano education initiative at the 2-year level in a 3+1 format, becoming a regional center in nano education at the AAS level.

Synopsis of Research Accomplishments
Thin Film Photovoltaics

Our group is active in the area of thin film PV, particularly CIGS and related materials. We have built a molecular beam epitaxy system for depositing these films in an oxygen-free ambient. We are currently working on the development of tandem CIGS devices using the wide bandgap absorber material CIAGS and on improving the efficiency of the earth-abundant absorber CZTS. Supporting this work is 2D device modeling using DESIS, and a wide variety of characterization equipment including DLTS, photocapacitance spectroscopy, and a novel technique that we have developed to distinguish interface from bulk traps in these devices.

Papers (Journal and Conference)

1. Sreejith Karthikeyan, Sehyun Hwang, Mandip Sibakoti, Timothy Bontrager, Richard W. Liptak, Stephen A. Campbell, "Effect of rapid thermal annealing of Copper Indium Aluminium Gallium diSelenide device and its deposition challenges", Applied Surface Science **493**, pp. 105-111 (2019) https://doi.org/10.1016/j.apsusc.2019.06.279.

2. A High Stability Near-Broken Gap Junction for Multijunction Photovoltaics, Forrest Johnson, Joel Pankow, Glenn Teeter, Brian Benton, and Stephen A. Campbell, JVST A **37**(1) 011201 (2019).

3. Sreejith Karthikeyan, Liyuan Zhang, Sehyun Hwang, and Stephen A. Campbell, Experimental scheme for a stable molybdenum bilayer back contacts for photovoltaic applications" Applied Surface Science **449**, Pages 647-653 (2018).

4. Mandip Jung Sibakoti, Sreejith Karthikeyan1, Sehyun Hwang, Timothy Bontrager, Stephen Campbell, "Defects in Copper Indium Gallium Aluminum Diselenide (CIAGS) Films and their Impact on Photovoltaic Device Performance" Proceedings of the Spring 2017 Materials Research Conference.

5. "Interface Characterization and Modeling of CIAGS Devices", Mandip J. Sibakoti, Sreejith Karthikeyan, Sehyun Hwang, Timothy Bontrager and Stephen A. Campbell, Proceedings of the 42nd IEEE Photovoltaic Specialist Conference, Portland (2016).

6. "Cu_2ZnSnS_4 thin film growth optimization and post rapid thermal annealing of solar cells and its influence on device performance", Liyuan Zhang, Sreejith Karthikeyan, Mandip J. Sibakoti, Stephen A. Campbell, Proceedings of the 41st IEEE Photovoltaic Specialist Conference (2015).

7. "Metal Oxide Broken Gap Tunnel Junction for Copper Indium Gallium Diselenide Tandem Solar Cells", Sang Ho Song, Eray Aydil, and Stephen A. Campbell, Solar Energy Materials and Solar Cells Vol. 133C (2015) pp. 133-142 DOI 10.1016/j.solmat.2014.10.046.

8. "Sputtered Metal Oxide Broken Gap Junctions for Tandem Solar Cells", Forrest Johnson, Sang Ho Song, Joel Abrahamson, Richard Liptak, Boris Chernomordik, Eray Aydil, and Stephen A. Campbell, Solar Energy Materials and Solar Cells Vol. 132C (2015) pp. 515 522 DOI 10.1016/j.solmat.2014.09.042.

9. "Atomic Layer Deposition of Tin Oxide and Zinc Tin Oxide Using Tetraethyltin and Ozone", Ellis J Warner, Forrest Johnson , Stephen A. Campbell, and Wayne L.

Gladfelter, J. Vac. Sci. Technol. A 33, pp. 021517-1 to 021517-7 (2015). DOI: 10.1116/1.4907562.

10. "Challenges in deposition of wide band gap copper indium aluminum gallium selenide (CIAGS) thin films for tandem solar cells", Sreejith Karthikeyan, Mandip Sibakoti, Richard Liptak, Sang Ho Song, Joel Abrahamson, Eray S. Aydil and Stephen A. Campbell, 40th IEEE Photovoltaic Specialist Conference (2014).

11. "In-situ stress and thermal stability studies of molybdenum bilayer back contacts for photovoltaic applications", Sreejith Karthikeyan, Liyuan Zhang and Stephen A. Campbell, 40th IEEE Photovoltaic Specialist Conference (2014).

12. "Sputtered Metal Oxide Broken Gap Junctions", Stephen Campbell, Forrest Johnson, Sreejith Karthikeyan, Sang-Ho Song, Richard Liptak, Brian Benton, Proc of the Spring Meeting of the Electrochemical Society Orlando (2014).

13. "In-situ stress and thermal stability studies of molybdenum bilayer back contacts for photovoltaic applications", Sreejith Karthikeyan, Liyuan Zhang and Stephen A. Campbell, accepted for publication, IEEE J. Photovoltaics (2014).

14. "Heteroepitaxy and the performance of CIGS solar cells", Sang Ho Song and Stephen A. Campbell, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

15. "Synthesis and Structural Characterization of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Sreejith Karthikeyan,and Stephen A. Campbell, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

16. "Sputtering of Metal Oxide Tunnel Junctions for Tandem Solar Cells", Forrest Johnson, Sang Ho Song, Richard Liptak, and Stephen A. Campbell, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

17. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher Cheng, Stephen A. Campbell, Eray S. Aydil, Proceedings of the 39th IEEE Photovoltaic Specialist Conference (2013).

18. "A low temperature, single step, pulsed d.c magnetron sputtering technique for copper indium gallium diselenide photovoltaic absorber layers", Sreejith Karthikeyan, Kushagra Nagaich, Arthur E Hill, Richard D Pilkington, and Stephen A Campbell, Proceedings of the Spring Meeting of the MRS **1538** (2013) doi.org/10.1557/opl.2013.1008

19. "Tin dioxide as an alternative window layer for improving the Damp-Heat Stability of Copper Indium Gallium Diselenide Solar Cells", Selin Tosun, Rebekah K. Feist, Stephen A. Campbell and Eray S. Aydil, J. Vac. Sci. Techn. A **30**, 04D101 (2012).

20. "Improving the damp-heat stability of copper indium gallium diselenide solar cells with a semicrystalline tin dioxide overlayer", Tosun, B.S.; Feist, R.K.; Gunawan, A.; Mkhoyan, K.A.; Campbell, S.A.; Aydil, E.S. Solar Energy Mat and Solar Cells 101, p 270-6, (2012).

21. "Sputter deposition of semicrystalline tin dioxide films", Tosun, B. Selin; Feist, Rebekah

K.; Gunawan, Aloysius; Mkhoyan, K. Andre; Campbell, Stephen A.; Aydil, Eray S. Thin Solid Films, v 520, n 7, p 2554-2561, January 31, 2012

22. "Structure and composition of ZnxCd1-xS films synthesized through chemical bath deposition", Tosun, B. Selin; Pettit, Chelsea; Campbell, Stephen A.; Aydil, Eray S. ACS Applied Materials and Interfaces, v 4, n 7, p 3676-3684, July25, 2012

23. Ozone Assisted ALD of Doped ZnO as a Transparent Metal Oxide", Hai Yuan, Bing Luo, Wayne L. Gladfelter, Stephen A. Campbell, ECS Transactions - Seattle, Washington" Volume 45, "Dielectrics for Nanosystems 5: Materials Science, Processing, Reliability, and Manufacturing, Seattle (2012).

24. "Atomic Layer Deposition of Al-doped ZnO films Using Ozone as the Oxygen Source: A Comparison of Two Methods to Deliver Aluminum", Hai Yuan, Bing Luo, Dan Yu, An-jen Chen, Stephen A. Campbell, and Wayne L.Gladfelter, J. Vac. Sci. Technol. A 30, 01A138 (2012); doi:10.1116/1.3666030.

25. B. S. Tosun, C. Pettit, S. A. Campbell and E. S. Aydil, "Structure and Composition of $Zn_xCd_{1-x}S$ Films Synthesized through Chemical Bath Deposition," *ACS Appl. Mater. Interfaces* **4**, 3676-3684 (2012).

26. "Atomic layer deposition of p-type phosphorus-doped zinc oxide films using diethylzinc, ozone and trimethylphosphite", H. Yuan, B. Luo, S. A. Campbell and W. L. Gladfelter, Electrochem. Solid-State Lett., Volume 14, Issue 5, pp. H181-H183 (2011).

27. "Imaging and phase identification of Cu2ZnSnS4 thin films using confocal Raman spectroscopy", A.-J. Cheng, M. Manno, A. Khare, C. Leighton, S. A. Campbell, and E. S. Aydil, J. Vac. Sci. Tech. v 29, n 5, (2011).

28. "Tin dioxide as an alternative window layer for improving the Damp-Heat Stability of Copper Indium Gallium Diselenide Solar Cells", Selin Tosun, Rebekah K. Feist, Stephen A. Campbell and Eray S. Aydil, J. Vac. Sci. Techn. A **30**, 04D101 http://dx.doi.org/10.1116/1.3692225 (*5 pages*) (2012).

29. "Sputter Deposition of Amorphous and Nanocrystalline Tin Dioxide Films," B. S. Tosun, R. K. L. Feist, S. A. Campbell and E. S. Aydil, Thin Solid Films **520**, pp. 2554-2561 (2011).

30. "Simultaneous Interface And Bulk Trap Characterization in CIGS Solar Cells", S. H. Song, S. Jeong, E. Aydil, B. Todd R. Feist, R. Haley, and S. A. Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference (2011).

31. "Improving the Damp-Heat Stability of Copper Indium Gallium Diselenide Solar Cells with a Semicrystalline Tin Dioxide Overlayer" Selin Tosun, Rebekah Feist, Stephen A. Campbell, and Eray Aydil, accepted for publication, Solar Energy Materials and Solar Cells (2011).

32. "Wide Band-gap CuIn1-xGaxSe2 based chalcopyrite absorbers for Tandem cell applications", Kushagra Nagaich, Eray Aydil, and Stephen Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference (2011).

33. "An analysis of temperature dependent current-voltage characteristics of Cu2O-ZnO heterojunction solar cells", Seong Ho Song, Sang Ho Song, Kushagra Nagaich, Stephen A. Campbell and Eray S. Aydil, Thin Solid Films v 519, n 19, p 6613-6619, July 29 (2011).

34. "Sulfurization Studies of the Potential Thin Film Solar Absorber Cu_2ZnSnS_4" An-Jen Cheng, Mike Manno, Rachel Frakie, Rachel Hoffman, Chris Leighton, Eray Aydil and Stephen A. Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference, Honolulu (2010).

35. "Structure Optimization for a High Efficiency CIGS Solar Cell", S. H. Song, K. Nagaich, E. Aydil, R. Feist, R. Haley, and S. A. Campbell, Proceedings of the IEEE Photovoltaics Specialists Conference, Honolulu (2010).

Patent

1. "Optoelectronic Devices With Thin Barrier Films With Crystalline Characteristics That Are Conformally Coated Onto Complex Surfaces To Provide Protection Against Moisture", U.S. Provisional Patent Application, Attorney Docket No. 71385, Selin Tosun, Stephen Campbell, Eray Aydil, and Rebekah Feist , Dow Chemical (2012).

Talks

1. **Invited Talk** – "PV Technologies and Outlook: Mostly Sunny with Scattered Clouds", Reforming Electric Energy Systems Curriculum with Emphasis on Sustainability Workshop, National Academy of Engineering and NSF, Washington DC (2015).

2. **Invited Talk** – "Solar Outlook for Minnesota", Minnesota Power Systems Conference, Minneapolis (2014).

3. **Invited Talk** – "Transparent Metal Oxides for Tunnel Junctions", Spring Meeting of the Electrochemical Society Orlando (2014).

4. **Invited Talk** – "The Future of Solar Energy", Upper Midwest Power Conference, Pine City Minnesota (2014).

5. "Heteroepitaxy and the performance of CIGS solar cells", Sang Ho Song and Stephen A. Campbell, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

6. "Synthesis and Structural Characterizations of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Sreejith Karthikeyan,and Stephen A. Campbell, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

7. "Sputtering of Metal Oxide Tunnel Junctions for Tandem Solar Cells", Forrest Johnson, Sang Ho Song, Richard Liptak, and Stephen A. Campbell, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

8. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher

Cheng, Stephen A. Campbell, Eray S. Aydil, 39th IEEE Photovoltaic Specialist Conference, Tampa (June, 2013).

9. "A low temperature, single step, pulsed d.c magnetron sputtering technique for copper indium gallium diselenide photovoltaic absorber layers", Sreejith Karthikeyan, Kushagra Nagaich, Arthur E Hill, Richard D Pilkington, and Stephen A Campbell, Proceedings of the Spring Meeting of the MRS (April, 2013)

10. "Continuous-Flow Chemical Bath Deposition of ZnxCd1-xS Thin Films For Chalcopyrite Solar Cells", Selin Tosun, Joel Abrahamson, Aloysius Gunawan, K. Andre Mkhoyan, Stephen A. Campbell and Eray S. Aydil, AVS Fall Meeting 2013.

11. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher Cheng, Stephen A. Campbell, Eray S. Aydil, 39th IEEE Photovoltaic Specialist Conference (2013).

12. "Copper Indium Aluminum Gallium diSelenide as a Potential Wide band-gap Absorber for CIGS based Tandem Photovoltaic Cells", Kushagra Nagaich*, Sreejith Karthikeyan* and Stephen A. Campbell, Spring meeting of the MRS (2013)

13. "Efficient Continuous-Flow Chemical Bath Deposition of CdS Films as Buffer Layers for Chalcogenide-Based Solar Cells", B. Selin Tosun, Joel T. Abrahamson, Christopher Cheng, Stephen A. Campbell and Eray S. Aydil. Photo Voltaics Spec Conf (2013).

14. "Synthesis and Structural Characterizations of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Xin Zhang, Sreejith Karthikeyan, Stephen A. Campbell, Photo Voltaics Spec Conf (2013).

15. "Sputtering of Metal Oxide Tunnel Junctions for Tandem Solar Cell Applications", Forrest Johnson, Sang Ho Song, Ricard Liptak, Boris XXX, Eray Aydil, Stephen A. Campbell, Photo Voltaics Spec Conf (2013).

16. "Deposition and Structural Characterizations of Cu2ZnSnS4 Thin Films", Liyuan Zhang, Xin Zhang, Michael Manno, Melissa Johnson, Eray Aydil, Chris Leighton, Stephen Campbell, Minneapolis AVS Sectional Meeting Fall 2012.

17. "Electrical scanning probe microscopy of thin films for CIGS-based solar cells", Joel T. Abrahamson, B. Selin Tosun, Forrest Johnson, Greg Haugstad, Stephen A. Campbell, and Eray S. Aydil, Spring ACS (2013).

18. "Copper Indium Aluminum Gallium diSelenide as a Potential Wide band-gap Absorber for CIGS based Tandem Photovoltaic Cells", Kushagra Nagaich, Sreejith Karthikeyan and Stephen A. Campbell, Spring MRS (2013).

19. "A low temperature, single step, pulsed d.c magnetron sputtering technique for copper indium gallium diselinide photovoltaic absorber layers", Sreejith Karthikeyan, Kushagra Nagaich, Arthur Hill, Richard D Pilkington, and Stephen A. Campbell, Spring MRS (2013).

20. **Invited Talk** "Ozone Assisted ALD of Doped ZnO as a Transparent Metal Oxide", ", Hai Yuan, Bing Luo, Wayne L. Gladfelter, Stephen A. Campbell, Spring ECS meeting Seattle (2012).

21. 60th International AVS Symposium, Long Beach, California, "Continuous-Flow Chemical Bath Deposition of $Zn_xCd_{1-x}S$ Thin Films for Chalcopyrite Solar Cells," B. S. Tosun, J. T. Abrahamson, A. A. Gunawan, K. A. Mkhoyan, S. A. Campbell and E. S. Aydil (speaker), October 2013.

22. 245th American Chemical Society National Meeting, New Orleans, Lousiana, "Synthesis of Compositionally Graded $Zn_xCd_{1-x}S$ Films using Chemical Bath Deposition," B. S. Tosun (speaker), J. T. Abrahamson, A. A. Gunawan, C. Pettit, C. Cheng, K. A. Mkhoyan, S. A. Campbell and E. S. Aydil, April 2013.

23. 245th American Chemical Society National Meeting, New Orleans, Lousiana, "Electrical Scanning Probe Microscopy of Thin Films for CIGS-based Solar Cells," J. T. Abrahamson (speaker), B. S. Tosun, F. Johnson, G. Haugstad, S. A. Campbell and E. S. Aydil, April 2013.

24. 59th International AVS Symposium, Tampa Bay, Florida, "$Zn_xCd_{1-x}S$ Thin Films For Chalcopyrite Solar Cells Deposited Through Batch and Continuous-Flow Chemical Bath Deposition," B. S. Tosun, C. Pettit, S. A. Campbell and E. S. Aydil, October 2012.

25. "Imaging and Phase Identification of Cu2ZnSnS4 Thin Films using Confocal Raman Spectroscopy", A.-J. Cheng,; M. Manno, A.; Ankur Khare, C.; Chris Leighton, S. A. Campbell, and E. S. Aydil, Fall AVS Meeting, Minneapolis (2011).

26. "Sputter Deposition of Amorphous and Nanocrystalline Tin Dioxide Films" Selin Tosun, Rebekah Feist, Steve Campbell and Eray S. Aydil, American Institute of Chemical Engineering Conference, Minneapolis (2011).

27. "p-Type phosphorus-doped zinc oxide films deposited by atomic layer deposition: Microstructural effects", Wayne L. Gladfelter, Hai Yuan, Bing Luo, and; Stephen A. Campbell, ALD Conference, Cambridge MA (2011).

28. "Simultaneous Interface And Bulk Trap Characterization in CIGS Solar Cells", S. H. Song, S. Jeong, E. Aydil, B. Todd R. Feist, R. Haley, and S. A. Campbell, IEEE Photovoltaics Specialists Conference, Seattle (2011).

29. "Wide Band-gap CuIn1-xGaxSe2 based chalcopyrite absorbers for Tandem cell applications", Kushagra Nagaich,; Eray Aydil, and Stephen Campbell, IEEE Photovoltaics Specialists Conference, SeattleAVS 58th Annual International Symposium and Exhibition (2011).

30. "Sulfurization Studies of the Potential Thin Film Solar Absorber Cu_2ZnSnS_4" An-Jen Cheng, Mike Manno, Rachel Frakie, Rachel Hoffman, Chris Leighton, Eray Aydil and Stephen A. Campbell, IEEE Photovoltaics Specialists Conference, Honolulu (2010).

31. "Structure Optimization for a High Efficiency CIGS Solar Cell", S. H. Song, K. Nagaich, E. Aydil, R. Feist, R. Haley, and S. A. Campbell, EEE Photovoltaics Specialists Conference Honolulu (2010).

32. "Solar Cells from Abundant Nontoxic Materials: Copper Zinc Tin Sulfide Photovoltaics", Eray S. Aydil, Ankur Khare, An-Jen Cheng, Michael Manno, Melissa Johnson, David Norris, Chris Leighton and Stephen Campbell", E3 Conference (an IREE sponsored event), 2010.

33. "An Overview of Lab-Scale Fabrication of High Performance PVs", S. A. Campbell, Colorado Workshop on Photovoltaics, Boulder (2010).

Semiconductor Nanoparticles

Collaborators in Mechanical Engineering developed particle beam mass spectroscopy (PBMS) as a tool to measure nanoscale particle size distributions in low pressure processing chambers in real-time. We have observed and sized particles as small as 5 nm in diameter with a sensitivity of ~1 cm^{-3}. More working with Professor Kortshagen, have developed techniques for making cubic, single crystal Si nanoparticles. These could have tremendous applications in building three dimensional, multi-material integrated systems on a chip and in low substrate temperature electronic applications. We have built both n- and p- channel devices and are working on optimizing the device structure. We have also developed processes for making light emitting silicon quantum dots, single crystal silicon nanoparticles that emit all colors (depending on size) and have made the first hybrid silicon OLED.

Papers (Journal and Conference)

1. Brian T. Benton, Benjamin L. Greenberg, K. V. Reich, B. I. Shklovskii, Uwe R. Kortshagen, S. A. Campbell, Variable Range Hopping Conduction in ZnO Nanocrystal Thin Films, Nanotechnology **29**(41) 415202 (2018).

2. UV and Air Stability of High-Efficiency Photoluminescent Silicon Nanocrystals, Jihua Yang, Richard Liptak, Stephen Campbell, Uwe Kortshagen, James Casey and Jon Hannington, Applied Surface Science Vol. 323 pp. 54-58 (2014).

3. Modeling Charge Transport in Quantum Dot Light Emitting Devices with NiO and ZnO transport layers and Si Quantum Dots", Brijesh Kumar, Stephen A. Campbell, Paul Ruden, Journal of Applied Physics **114**(4) p. 044507 (2013). http://dx.doi.org/10.1063/1.4816680

4. "Tunneling Conduction in Dense Silicon Quantum Dot/PMMA Composites, "D. Yu, R. W. Liptak, G. Aggarwal, A. –J. Cheng, and S. A. Campbell, Thin Solid Films 527, pp 261-266 (2013). http://dx.doi.org/10.1016/j.tsf.2012.11.056

5. "Environmental Photostability of SF6-Etched Silicon Nanocrystals", Richard W. Liptak, Jihua Yang, Uwe R. Kortshagen, and Stephen A. Campbell, Nanotechnology 23(39), 395205 (7 pp.) (2012).

6. "Comparing Direct Charge Injection and Forster Energy Transfer into Quantum Dots to Maximize Light Output in Hybrid Organic/Inorganic QD-LEDs" Brijesh Kumar, Ryan Hue, Wayne L. Gladfelter, Stephen A. Campbell, J. Applied Physics 112(3), August 2012 (2012).

7. "Electron energy band alignment at the NiO/SiO2 interface", V. V. Afanas'ev, M. Badylevich, M. Houssa and A. Stesmans, G. Aggrawal, and S. A. Campbell, Appl. Phys. Lett. L09-11903 (2010).

8. "Surface Chemistry Dependence of Native Oxidation Formation on Silicon Nanocrystal", R. W. Liptak, U. Kortshagen, and S. A. Campbell, JAP **106**, p. 064313 (2009).

9. Sang Ho Song and S. A. Campbell, "The Effect of Composition on Surface Morphology

and Electrical Characteristics of Cosputtered Ytterbium Silicide", accepted for publication, Thin Solid Films v. 517(24), 30 October 2009, Pages 6841-6846 (2009).

10. "SF_6 Dry Etching of Silicon Nanocrystals", R. W. Liptak, J. H. Thomas III, U. Kortshagen, and S. A. Campbell, Nanotechnology v 20, n 3, p 035603, Jan 21 (2009).

11. "Nanoparticles: A Route to Post-Shrink Information Systems", S. A. Campbell, R. Liptak, S. H. Song, R. Ligman, Yongping Ding, Ying Dong, A. Bapat, F. Gali, X. D. Pi, U. Kortshagen, Proceedings of the UGIM (2008).

12. "Air-stable full-visible-spectrum emission from silicon nanocrystals synthesized by an all-gas-phase plasma approach", X. D. Pi, R. W. Liptak, J Deneen Nowak, N. P. Wells, C B Carter, S A Campbell and U Kortshagen, Nanotechnology **19** 245603 (2008).

13. "Doping Efficiency, Dopant Location, and Oxidation of Si nanocrystals", X. D. Pi, R. Gresback , R. W. Liptak , S. A. Campbell , and U. Kortshagen, APL 92, 123102 (2008).

14. "Full Spectrum Emission and Hybrid OLEDs from Silicon Nanoparticles", X. Pi, R. Liptak, R. Ligman, U. Kortshagen, and S. A. Campbell, Proceedings of the 4th International Conference on Group Four Photonics Workshop, IEEE/LEOS, Tokyo (2007).

15. "Nonthermal plasma Synthesis of Faceted Germanium Nanocrystals", Patrizio Cernetti, Ryan Gresback,, Stephen A. Campbell, and Uwe Kortshagen, Chemical Vapor Deposition **13**, Issue 6-7, July, 2007, Pages: 345-350 (2007).

16. "TEM Study of Ytterbium Silicide Thin Films", J Deneen Nowak, S H Song1, S A Campbell1 and C B Carter, Proceedings of the Microscopy of Semiconducting Materials Conference (2007).

17. "Electroluminescence from Surface Oxidized Silicon Nanoparticles Randomly Dispersed within a Polymer Matrix", Rebekah K Ligman, Lorenzo Mangolini, Uwe Kortshagen, Stephen A Campbell, proceedings of Nano Science and Technology International, Santa Clara (2007).

18. "400-900 nm Light Emitting Silicon Nanoparticles Produced By An All-Gas Phase Approach", R. W. Liptak, X.D. Pi, U. Kortshagen and S. A. Campbell, proceedings of Nano Science and Technology International, Santa Clara (2007).

19. "N-channel Single Crystal Si Nanoparticle Schottky Barrier Transistor", Sang Ho Song, Yongping Ding, Ameya Bapat, Uwe Kortshagen, Stephen A. Campbell, proceedings of Nano Science and Technology International, Santa Clara (2007).

20. X. D. Pi, R. W. Liptak, S. A. Campbell and U. Kortshagen, "In-Flight dry etching of Si nanocrystals synthesized by nonthermal plasma", Appl. Phys. Lett. **91**, 083112 (2007).

21. Rebekah K. Ligman, Stephen A. Campbell, Lorenzo Mangolini and Uwe Kortshagen "Electroluminescence from Surface Oxidized Silicon Nanoparticles Dispersed Within a Polymer Matrix", Applied Physics Letters **90**, 061116 (2007), also appears in February 19, 2007 issue of Virtual Journal of Nanoscale Science & Technology (APS).

22. Patrizio Cernetti, Ryan Gresback, Stephen A. Campbell and Uwe Kortshagen, ”Nonthermal plasma synthesis of highly oriented Germanium nanocrystals”, Cherm Vap Dep. **13**, pp. 345–350 (2007).

23. Ameya Bapat, Marco Gatti, Yong-Ping Ding, Stephen Campbell and Uwe Kortshagen, “A plasma process for the synthesis of cubic-shaped silicon nanocrystals for nanoelectronic devices”, J. Applied Phys. D **40** No 8 (21 April 2007) 2247-2257 (2007).

24. X. D. Pi, L. Mangolini, J. Schidmit, and U. Kortshagen, and S. A. Campbell, “Room-temperature atmospheric oxidation of Si nanocrystals after etching in HF acid vapor” Physical Review B **75**, March 15 p. 085423-1 to 085423-5 (2007).

25. Yongping Ding and S. A. Campbell, “Quantum Size Effect in the Nanostructure PtSi/Si Contacts”, Applied Physics Letters **89**, 093508 (2006).

26. Yongping Ding, Ying Dong, Ameya Bapat, Julia Deneen, C. Barry Carter, Uwe R. Kortshagen, and Stephen A. Campbell, “A Single Nanoparticle Silicon Transistor”, IEEE Trans. Elect. Dev. **53**(10), pp. 2525-2531 (2006).

27. Barry, Chad R. (University of Minnesota); Campbell, Steven; Jacobs, Heiko O. “Nanoxerography: Electrostatic force directed printing of nanomaterials” Digital Fabrication 2005 - Final Program and Proceedings, Digital Fabrication 2005 - Final Program and Proceedings, 2005, p 25

28. S. A. Campbell, Y. Dong, Y. Ding, A. Bapat, J. Deneen, Uwe R. Kortshagen, and C. Barry Carter, “Single Nanoparticle Semiconductor Devices”, Nanofabrication: Technologies, Devices, and Applications II, W. Y. Lai, L. E. Ocola, and S. Pau, Eds., SPIE Boston (2005).

29. J. Deneen, C R Perrey, Y Ding, A Bapat, S A Campbell, U Kortshagen and C B Carter, “Microscopy of nanoparticles for semiconductor devices”, Proceedings of the Microscopy of Semiconductors Conference MSMXIV (2005).

30. T. J. Belich, Z. Shen, C. Blackwell, S. Campbell and J. Kakalios, “Conductance Fluctuations in Free-Standing Hydrogenated Amorphous Silicon Nanoparticles”, in the Proceedings of the Third SPIE International Symposium on Fluctuations and Noise - Session on Fluctuations and Noise in Materials II 23-26 May, 2005, Austin, Texas

31. T. J. Belich, Z. Shen, C. Blackwell, S. Campbell and J. Kakalios, “Conductance Fluctuations in Amorphous Silicon Nanoparticles”, Proceedings of Symposium A-Amorphous and Nanocrystalline Science and Technology Spring 2005 MRS meeting

32. S. A. Campbell, U. Kortshagen, A. Bapat, Y. Dong, S. Hilchie, Z. Shen, **Invited Paper**, “The Production and Electrical Characterization of Free Standing Cubic Single Crystal Silicon Nano Particles”, JOM 56(10), pp. 26-28 (2004).

33. Y. P. Ding, Y. Dong, S. A. Campbell, H. O. Jacobs, A. Bapat, U. Kortshagen, C. Perrey, and C. B. Carter, “Field-Effect Transistor Built with a Single Crystal Si Nanoparticle”, Proceedings of the Design, Service, and Manufacturing Research Conference, Scottsdale, Arizona (2005)

34. A. Bapat, C. Anderson, C. R Perrey, C B. Carter, S. A Campbell, and U. Kortshagen, "Plasma Synthesis of Single-Crystal Silicon Nanoparticles For Novel Electronic Device Applications", Plasma Phys. Control. Fusion **46,** pp. 1–13 (2004).

35. Silicon nanoparticle synthesis using constricted mode capacitive silane plasma, Bapat, A.; Ying Dong; Perrey, C.R.; Carter, C.B.; Campbell, S.A.; Kortshagen, U. Source: Nanoparticles and Nanowire Building Blocks-Synthesis, Processing, Characterization and Theory, p 405-10, (2004).

36. Z. Shen, U. Kortshagen, P. L. McMurry, and S. A. Campbell, "Electrical Characterization of Amorphous Silicon Nanoparticles", J. Appl. Phys. **96**(4) pp. 2204-2209 (2004).

37. Y. Dong, A. Bapat, S. Hilchie, U. Kortshagen, and S. A. Campbell, "The Generation of Free-Standing Single Crystal Silicon Nanoparticles", JVST B **22**(4), pp. 1923-1930 (2004).

38. Y. Dong, A. Bapat, Z. Shen, C. R. Perrey, C. B. Carter, U. Kortshagen, and S. A. Campbell, Single Crystal Nanoparticles for 3D Integrated Systems, Proceedings of the Future of Ultra Large Scale Integration of Silicon Workshop, Leuven Belgium (2004).

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20. **Invited talk** - "Coulomb-Force Directed Assembly and Transfer of Nanomaterials", C. R. Barry, A. M. Welle, T. Hatch, U. Kortshagen, S. A. Campbell, and H. O. Jacobs, MRS Symposium on Flexible Electronics, Fall (2005).

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Synopsis of Research Accomplishments
High Permittivity Insulators and Ultrathin SiO_2 for Deeply Scaled CMOS

Our group has played a pioneering role in the developments of high permittivity layers for deeply scaled MOSFETs. We were the first in the rapidly growing area of research. Papers in 1996 and 97 proved seminal and sparked research efforts at many schools and companies into the use of high permittivity materials as gate insulators. Together with Professor Gladfelter, we have developed new precursors for depositing TiO_2, ZrO_2, HfO_2, and other materials, and have demonstrated the formation of, and electrical effects of, a thin interfacial layer. We have measured the effects of charge injection in these composite gate insulator systems, developed techniques for controlling the interfacial layer thickness, and investigated binary oxides. More recently we have also explored the use of high k materials on SiC, producing the highest quality SiC MOSCAPs ever published.

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Papers (Journal and Conference)

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2. “Synthesis and Structures of Bis(2-dimethylaminoethyl)amine Adducts of Strontium Bis(2,2,6,6-tetramethylheptane-3,5-dionate) and Their Use in the Chemical Vapor Deposition of Cubic Strontium-doped Hafnium Dioxides”, D. Yu, S. A. Campbell, W. L. Gladfelter, Division of Inorganic Chemistry for the 233rd ACS National Meeting, Chicago (2007).

3. “Materials and Processes for High k Gate Stacks: Results from the FEP Transition Center”, C.M. Osburn, S.A. Campbell, A. Demkov, E. Eisenbraun, E. Garfunkel, T. Gustafson, A. Kingon, J. Lee, D. Lichtenwalner, G. Lucovsky, T.P. Ma, J.P. Maria, V.

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5. Zhihong Zhang and Stephen A. Campbell ,"Effect of Deposition Chemistry on Charge Removal in Cr gated HfO2 Stacks", submitted to SISC Washington DC (2005).

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31. **Invited Talk –** Semiconductor Interface Specialists Conference IEEE, San Diego, December, 2000.

32. Invited Talk - "Interface Layer Inhibition in the CVD of Column IVB Metal Oxides", S. A. Campbell, High-k Gate Dielectrics Workshop, MRS, New Orleans, June, 2000.

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37. **Invited Talk –** "Performance of Group IVB Oxides as High Permittivity Gate Insulators", S. A. Campbell, B. He, R. Smith, T. Ma, N. Hoilien, C. Taylor, W. L. Gladfelter, Materials Research Society, Fall Meeting, Boston (1999).

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49. "The Deposition of TiO_2 from TTIP and H_2O", S. A. Campbell, J. Yan, D. C. Gilmer, and W. L. Gladfelter, Fall Meeting of the Electrochemical Society, Chicago (1995).

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51. "Low Temperature Nitridation of Silicon by Direct Amonnia Nitridation in a Molecular Beam Epitaxy Reactor", T. K. Higman, R. T. Fayfield, M. S. Hagedorn, K. H. Lee, S. A. Campbell, J. N. Baillargeon, and K. Y. Cheng, 1992 North American Conference on Molecular Beam Epitaxy.

Synopsis of Research Accomplishments
Rapid Thermal Processing and GeSi Technology

Rapid thermal processing, and its application to the growth of epitaxial layers, comprised a significant fraction of my research efforts from 1991-94. Our group was the first to apply computational fluid dynamics, along with conventional radiative transfer, to model the rapid thermal processing chamber. We developed code for 2 and 3 dimensional steady state calculations and 2 dimensional transient analysis of two chambers. The first was an experimental, single side heated system in which we did GeSi epitaxial growth. The other was an industry standard, Heat Pulse, manufactured by AG Associates. We demonstrated with our model the need for multizone heating and the tendency of wafer edges to overheat during thermal transients. In the area of RTCVD, we demonstrated the effect of dopant addition to the growth chemistry. Specifically we demonstrated that arsine poisoned the surface, raising the activation energy for the growth to that of conventional silicon. This provided significant support to the growth rate enhancement model of Sturm, et. al.

Papers (Journal and Conference)

1. "A Critical Review - The Epitaxial Growth of Semiconductors By Rapid Thermal Chemical Vapor Deposition" S. A. Campbell, Materials Science & Engineering R - Reports **20**, pp 1-36 (1997).

2. "Rapid Thermal Processing", in *Computational Modeling in Semiconductor Processing*, M. Meyyappan, Ed., Artech Publishing (1994)

3. "A Kinetics and Transport Model of Dichlorosilane Chemical Vapor Deposition", K. L. Knutson, S. A. Campbell, and R. Carr, J. Crystal Growth **140**, p. 191 (1994).

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Synopsis of Accomplishments
Semiconductor Processing Education and Technology

The Science and Technology of Microelectronic Fabrication, was released in March, 1996 by Oxford University Press. The first edition went through seven printings before the second edition was released in 2001. The third edition is now in preparation. Approximately 50 US institutions have adopted it as a course textbook, including Stanford, Berkeley, Cornell, and UT Austin. Numerous schools in Europe, the Middle East, and the Pacific Rim have also adopted the book, and the book has been translated into Chinese. A major new initiative has been the development of new AAS capstone experience at the University. This was developed in collaboration with Dakota County Technical. Minnesota State College - Southeast Technical recently joined and will be submitting students to the program in 2009. Four other schools have joined with the University and DCTC to create an upper Midwest consortia in nano education. Finally, this section covers several small research projects including MEMS-related work and one project funded by ONR on the formation of semi-insulating silicon wafers by the addition of Au as a Fermi level pinning impurity.

Books

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1. Nezhueyotl Izquierdo, Jason C. Myers, Prafful Golani, Nicholas C. A. Seaton, Steven J. Koester, and Stephen A. Campbell, "Growth of Black Arsenic Phosphorus Thin Films and its Application for Field-Effect Transistors", Nanotechnology 32 325601 (2021).

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1. "Anisotropy of the Fermi Surface, Fermi Velocity, Many-Body Enhancement and Super Conducting Energy Gap in Nb", G. W. Crabtree, D. H. Dye, D. P. Karim, S.A. Campbell, J. B. Ketterson, Phys. Rev. B, 35, pp. 1728-1741 (1987).

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Challenged Claims:

- **U.S. Pat. No. 10,510,842:** Claims 1, 2, 4-9, 12-18.
- **U.S. Pat. No. 10,734,481:** Claims 1-9, 13, 15, 17, 20, 22-27, 31-32, 34.
- **U.S. Pat. No. 11,121,222:** Claims 1, 3-9, 13, 15-17, 20, 21, 24-28, 32-34, 39-42.
- **U.S. Pat. No. 11,316,014:** Claims 1, 3- 9, 13, 15-17, 20-21, 23-28.

The below organizes like-claims via row, with differing limitations across patents annotated in highlighted yellow. There is further identification regarding which claims within a patent match other claims (*e.g.*, claim 4 of the '842 Patent is substantively identical to claim 12 of the '842 Patent). Differences between claim-sets in a single identified patent are described in ***green text***.

'842 Patent	**'481 Patent**	**'222 Patent**	**'014 Patent**
Claim 1	**Claim 1**	**Claim 1**	**Claim 1**
[1.Pre] A semiconductor device comprising:	[1.Pre] A semiconductor device comprising:	[1.Pre] A VLSI semiconductor device comprising:	[1.Pre] An electronic system, the system comprising: at least one semiconductor device, the at least one semiconductor device including:

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[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;	[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;	[1.1] a substrate of a first doping type at a first doping level having a surface;	[1.1] a substrate of a first doping type at a first doping level having a surface;
[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	[1.2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	[1.2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[1.4] transistors formed in at least one of the first active region or second active region; and	[1.4] transistors formed in at least one of the first active region or second active region;	[1.4] transistors formed in at least one of the first active region or second active region;	[1.4] transistors formed in at least one of the first active region or second active region;
[1.5] at least a portion of at least one of the first and second active regions having	[1.5] at least a portion of at least one of the first and second active regions having	[1.5] at least a portion of at least one of the first and second active regions having at least one graded	[1.5] at least a portion of at least one of the first and second active regions

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at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
	[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,	[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,
		[1.7] wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	[1.7] wherein at least some of the transistors form digital logic of the semiconductor device.
Claim 2	**Claim 2**		
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.		

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Claim 4	**Claim 3**	**Claim 3**	**Claim 3**
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	3. The system of claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.
Claim 5	**Claim 4**	**Claim 4**	**Claim 4**
5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	4. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.
Claim 6	**Claim 5**	**Claim 5**	**Claim 5**
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	5. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells,

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			respectively, and each well has at least one graded dopant.
Claim 7	**Claim 6**	**Claim 6**	**Claim 6**
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	6. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.
Claim 8	**Claim 7**	**Claim 7**	**Claim 7**
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	7. The system of claim 1, wherein the graded dopant is fabricated with an ion implantation process.
Claim 17	**Claim 8**	**Claim 8**	**Claim 8**
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	8. The system of claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of

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			the at least one semiconductor device.
Claim 18	**Claim 9**	**Claim 9**	**Claim 9**
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	9. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.
	Claim 13	**Claim 13**	**Claim 13**
	13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.
	Claim 15	**Claim 15**	**Claim 15**
	15. The semiconductor device of claim 1, wherein the device is a complementary metal	15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal	15. The system of claim 1, wherein the at least one semiconductor device is a

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	oxide semiconductor (CMOS) with a nonepitaxial substrate.	oxide semiconductor (CMOS) with a nonepitaxial substrate.	complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
		Claim 16	**Claim 16**
		16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	16. The system of claim 1, wherein the at least one semiconductor device is a flash memory.
	Claim 17	**Claim 17**	**Claim 17**
	17. The semiconductor device of claim 1, wherein the device is a logic device.	17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	17. The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.
		Claim 20	**Claim 20**
		20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction	20. The system of claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.
Claim 9	**Claim 20**	**Claim 21**	**Claim 21**
Claim 9 is substantively identical to claim 1, but	*Claim 20 is substantively identical to claim 1, but*	*Claim 21 is substantively identical to claim 1, but recites "within*	*Claim 21 is substantively identical to claim 1, but*

*recites "within which transistors can be formed **in the surface thereof**" in [9.2] and [9.3] and "from the surface to the substrate" in [9.5].*	*recites "within which transistors can be formed **in the surface thereof**" in [20.2] and [20.3].*	*which transistors can be formed **in the surface thereof**" in [21.2] and [21.3] and "from the surface" in [21.5], and "and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof" in [21.6].*	*recites "within which transistors can be formed **in the surface thereof**" in [21.2] and [21.3] and "from the surface" in [21.5], and "and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof" in [21.6].*
[9.PRE] A semiconductor device, comprising:	[20.PRE] A semiconductor device, comprising:	[21.PRE] A VLSI semiconductor device, comprising:	[21.PRE] An electronic system, comprising: at least one semiconductor device, the at least one semiconductor device including:
[9.1] a substrate of a first doping type at a first doping level having first and second surfaces;	[20.1] a substrate of a first doping type at a first doping level having first and second surfaces;	[21.1] a substrate of a first doping type at a first doping level having a surface;	[21.1] a substrate of a first doping type at a first doping level having a surface;
[9.2] a first active region disposed adjacent the first surface of the substrate with	[20.2] a first active region disposed adjacent the first surface of the substrate with a	[21.2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite	[21.2] a first active region disposed adjacent the surface of the substrate

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a second doping type opposite in conductivity to the first doping type and within which transistors can be formed ***in the surface thereof***;	second doping type opposite in conductivity to the first doping type and within which transistors can be formed ***in the surface thereof***;	in conductivity to the first doping type and within which transistors can be formed ***in the surface thereof***;	with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed ***in the surface thereof***;
[9.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed ***in the surface thereof***;	[20.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed ***in the surface thereof***;	[21.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed ***in the surface thereof***;	[21.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed ***in the surface thereof***;
[9.4] transistors formed in at least one of the first active region or second active region; and	[20.4] transistors formed in at least one of the first active region or second active region;	[21.4] transistors formed in at least one of the first active region or second active region;	[21.4] transistors formed in at least one of the first active region or second active region;
[9.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement ***from the surface to the substrate***.	[20.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement ***from the surface to the substrate***; and	[21.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement ***from the surface*** to an area of the substrate where there are no active regions; and	[21.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement ***from the surface*** to an area of the substrate where

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			there are no active regions; and
	[20.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	[21.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, ~~***and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof***~~.	[21.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, ***and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof***.
		[21.7] ***and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof***.	
	Claim 22		**Claim 23**
	Claim 22 is substantively identical to claim 2.		*Claim 23 is substantively identical to claim 2.*

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	22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.		23. The system of claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.
Claim 12	**Claim 23**	**Claim 24**	**Claim 24**
Claim 12 is substantively identical to claim 4.	*Claim 23 is substantively identical to claim 3.*	*Claim 24 is substantively identical to claim 3.*	*Claim 24 is substantively identical to claim 3.*
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	24. The system of claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.
Claim 13	**Claim 24**	**Claim 25**	**Claim 25**
Claim 13 is substantively identical to claim 5.	*Claim 24 is substantively identical to claim 4.*	*Claim 25 is substantively identical to claim 4.*	*Claim 25 is substantively identical to claim 5.*
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	25. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.
Claim 14	**Claim 25**	**Claim 26**	**Claim 26**

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Claim 14 is substantively identical to claim 6.	*Claim 25 is substantively identical to claim 5.*	*Claim 26 is substantively identical to claim 5.*	*Claim 26 is substantively identical to claim 5.*
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	26. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
Claim 15	**Claim 26**	**Claim 27**	**Claim 27**
Claim 15 is substantively identical to claim 7.	*Claim 26 is substantively identical to claim 6.*	*Claim 27 is substantively identical to claim 6.*	*Claim 27 is substantively identical to claim 6.*
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	27. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.
	Claim 27	**Claim 28**	**Claim 28**
	Claim 27 is substantively identical to claim 9.	*Claim 28 is substantively identical to claim 9.*	*Claim 28 is substantively identical to claim 9.*

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	27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	28. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.
Claim 16	**Claim 31**		
Claim 16 is substantively identical to claim 8.	*Claim 31 is substantively identical to claim 7.*		
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.		
		Claim 32	
		Claim 32 is substantively identical to claim 7.	
		32. The VLSI semiconductor device of claim 21, wherein the	

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		graded dopant is fabricated with an ion implantation process.	
	Claim 32	**Claim 33**	
	Claim 32 is substantively similar to claim 15, but claim 15 requires that the "device" is CMOS whereas claim 32 requires that the "substrate" is CMOS	*Claim 33 is substantively similar to claim 15, but claim 15 requires that the "device" is CMOS whereas claim 32 requires that the "substrate" is CMOS*	
	32. The semiconductor device of claim 20, wherein ***the substrate*** is a complementary metal oxide semiconductor (CMOS) device.	33. The VLSI semiconductor device of claim 21, wherein ***the substrate*** is a complementary metal oxide semiconductor (CMOS) device.	
	Claim 34		
	Claim 34 is substantively similar to claim 17		
	34. The semiconductor device of claim 20, wherein the device is a flash memory .		
		Claim 34	
		Claim 34 is substantively identical to claim 16.	
		34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	

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		Claim 39	
		Claim 39 is substantively identical to claim 1 but [39.5] requires "portion of at least one of the first and second active regions" while [1.5] requires "at least one well region" and "VLSI."	
		[39.PRE] A semiconductor device, comprising:	
		[39.1] a substrate of a first doping type at a first doping level;	
		[39.2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	
		[39.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	
		[39.4] transistors formed in at least one of the first active region or second active region; and	

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		[39.5] at least a ***portion of at least one of the first and second active regions*** having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	
		Claim 40	
		40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	
		Claim 41	
		Claim 41 is substantively identical to claim 1 but [41.5] requires "portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration" while [1.5] requires	

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		"at least one well region adjacent to the first or second active region containing at least one graded dopant region" and "VLSI."	
		[41.PRE] A semiconductor device, comprising:	
		[41.1] a substrate of a first doping type at a first doping level;	
		[41.2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	
		[41.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	
		[41.4] transistors formed in at least one of the first active region or second active region; and	
		[41.5] at least ***a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration*** to	

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		aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	
		Claim 42	
		Claim 42 is substantively identical to claim 1 but [42.5] requires "at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration" while [1.5] requires "at least one well region adjacent to the first or second active region containing at least one graded dopant region" and "VLSI."	
		[42.PRE] A semiconductor device, comprising:	
		[42.1] a substrate of a first doping type at a first doping level;	
		[42.2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	

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		[42.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	
		[42.4] transistors formed in at least one of the first active region or second active region; and	
		[42.5] ***at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration*** to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	

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