UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION

Petitioner

v.

GREENTHREAD, LLC

(record) Patent Owner

IPR2023-00376
Patent No. 10,510,842

PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.200 ET. SEQ

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 10,510,842 ("**the '842 patent**").
1002	Declaration of R. Michael Guidash.
1003	C.V. of R. Michael Guidash.
1004	U.S. Pat. No. 6,614,560 ("**Silverbrook**").
1005	U.S. Pat. No. 6,420,763 ("**Yamashita**").
1006	File History of U.S. App. Ser. No. 11/622,496 (issued as U.S. Pat. No. 8,421,195).
1007	File History of U.S. App. Ser. No. 15/590,282 (issued as the '842 patent).
1008	U.S. Pat. No. 4,481,522 ("**Jastrzebski**").
1009	Redline comparison of claim 1 and claim 9
1010	U.S. Pat. Pub. 2004/0063288 A1 ("**Kenney**").
1011	U.S. Pat. Pub. 2001/0032983 A1 ("**Miyagawa**").
1012	Excerpt from Nishi, et al. (eds.) *Handbook of Semiconductor Manufacturing*, Marcel Dekker, Inc., New York (2000) ("**Nishi**").
1013	Defendants' Opening Claim Construction Brief in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. Oct. 10, 2022).
1014	Plaintiffs' Claim Construction Brief in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. Oct. 31, 2022).
1015	Complaint in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. January 27, 2022).

1016	Amended Complaint in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. April 29, 2022).
1017	Exhibit 12 from Amended Complaint in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. April 29, 2022).
1018	U.S. Pat. App. Pub. 2003/0136982A1 ("**Rhodes**").
1019	Scheduling Order in *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-105-ADA (W.D. Tex. May 23, 2022).
1020	United States District Courts — National Judicial Caseload Profile, March 31, 2022, available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1
1021	Scheduling Order in *Topia Tech., Inc. v. Box, Inc., et al.*, Case No. 6:21-cv-01372-ADA (W.D. Tex. May 20, 2022).
1022	Scheduling Order in *Parus Holdings, Inc., v. Apple Inc., et al.*, Case No. 6:21-cv-00570-ADA (W.D. Tex. August 22, 2022).
1023	Scheduling Order in *Lone Start SCM Systems, Ltd. V. Zebra Tech. Corp.*, Case No. 6:21-cv-00570-ADA (W.D. Tex. August 3, 2022).
1024	U.S. Pat. No. 6,483,176 ("**Noguchi**").
1025	U.S. Pat. App. Pub. 2003/0063272A1 ("**Zaidi**").
1026	U.S. Pat. App. Pub. 2003/0081463A1 ("**Bocian**").
1027	U.S. Pat. App. Pub. 2003/0098419A1 ("**Ji**").
1028	Screen capture of https://www.bestbuy.com/site/sony-alpha-a7-iii-mirrorless-4k-video-camera-body-only-black/6213101.p?skuId=6213101
1029	Excerpt from Pierret, *Semiconductor Fundamentals, Vol. I*, Addison-Wesley Publishing Company, Reading, MA, 1983.

1030	Excerpt from Grove, *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, 1967.
1031	Excerpt from Sze, *VLSI Technology*, McGraw-Hill Book Company, 1983.
1032	Excerpt from Wolf and Tauber*, Silicon Processing for the VLSI ERA,* Lattice Press, Sunset Beach, CA, (2000).

Petitioner respectfully requests *inter partes* review under 35 U.S.C. §311 of claims 1-18 of U.S. Pat. No. 10,510,842 ("the '842 patent").

NOTICE OF LEAD AND BACKUP COUNSEL

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NOTICE OF RELATED MATTERS

The '842 patent has been asserted in *Greenthread, LLC v. Intel Corporation et al,* Case No. 6-22-cv-00105 (W.D. Tex.), filed January 27, 2022, and is the subject of *Intel Corporation v. Greenthread, LLC,* IPR2023-00308. A submission addressing multiple proceedings is filed herewith.

NOTICE OF THE REAL-PARTIES-IN-INTEREST

The real-parties-in-interest ("RPIs") are Sony Group Corporation, Sony Corporation, Sony Semiconductor Solutions Corporation, Sony Semiconductor Manufacturing Corporation, Sony Taiwan Ltd., Sony Corporation of America, Sony Electronics Inc., Dell Inc., and Dell Technologies Inc.

NOTICE OF SERVICE INFORMATION

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GROUNDS FOR STANDING

Petitioner hereby certifies that the patent for which review is sought is available for *inter partes* review, and that the Petitioner is not barred or estopped from requesting *inter partes* review on the grounds identified in the petition.

STATEMENT OF PRECISE RELIEF REQUESTED

Petitioner respectfully requests that claims 1-18 of the '842 patent be canceled based on the following grounds:

Ground 1: Claims 1-5, 7-13, and 15-18 were obvious over Miyagawa

Ground 2: Claims 1-18 were obvious over Yamashita.

Ground 3: Claims 1-18 were obvious over Yamashita and Nishi.

THRESHOLD REQUIREMENT FOR *INTER PARTES* REVIEW

As shown in the Grounds set forth below, the information presented in the instant petition, if unrebutted, demonstrates that "it is more likely than not that at least 1 of the claims challenged in the petition is unpatentable." 35 U.S.C. § 314(a).

I. INTRODUCTION

A. Technical Background

The '842 patent relates to semiconductor devices having graded dopant concentrations. Petitioner's expert, Mr. Guidash, provides an introduction to the technology concepts relevant to the '842 patent. (Ex. 1002, ¶¶24-68).

II. CLAIM CONSTRUCTION

"In an inter partes review proceeding, a claim of a patent…shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. §42.100(b).

Petitioner does not believe that claim construction is required for the Board to evaluate obviousness in this Petition.

Greenthread LLC and defendants related to Dell and Intel have taken claim construction positions in the co-pending litigation, as reflected in Exhibits 1013 and 1014.

III. DETAILED EXPLANATION OF THE REASONS FOR UNPATENTABILITY

Ground 1. Claims 1-5, 7-13, and 15-18 were obvious over Miyagawa

Claims 1-5, 7-13, and 15-18 were obvious under pre-AIA 35 U.S.C. §103(a) over U.S. Pat. Pub. 2001/0032983 A1 ("**Miyagawa**")(Ex. 1011).

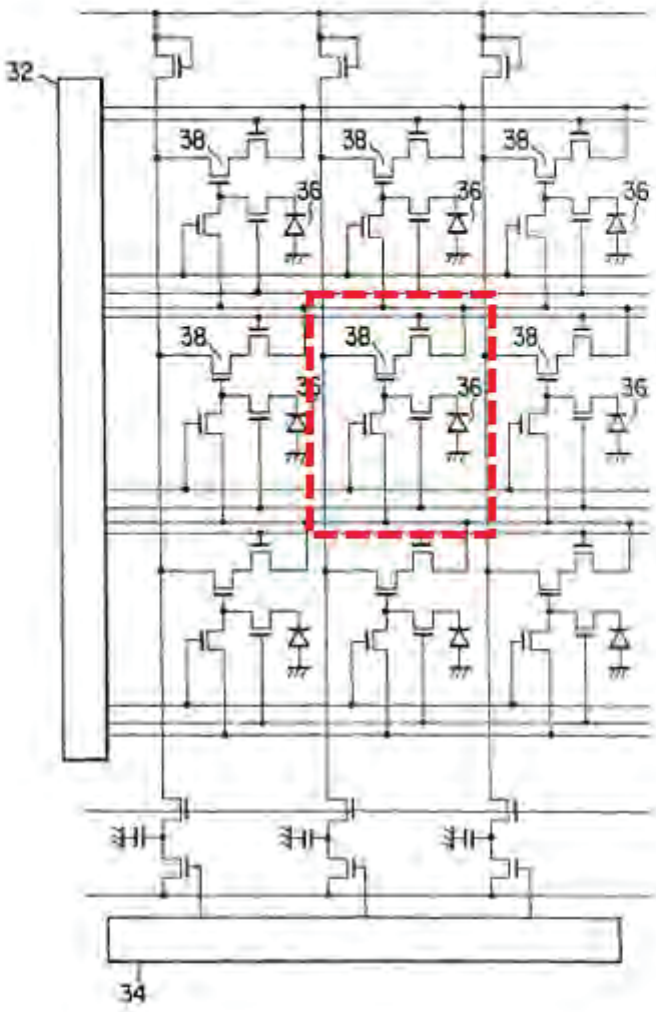
A. Effective Prior Art Date of Miyagawa

Miyagawa is a U.S. patent application publication that published on October 25, 2001, and is thus prior art under pre-AIA 35 U.S.C. §102(b).

B. Overview of Miyagawa

Miyagawa teaches semiconductor devices useful for MOS (Metal Oxide Semiconductor) image sensors. (Ex. 1011, Title, Abstract)(Ex. 1002, ¶72). Such image sensors are usually fabricated using CMOS techniques in a silicon substrate. (Ex. 1002, ¶72). Within that domain, Miyagawa teaches the techniques for arranging the semiconductor structure of pixels within image sensor arrays. A "pixel" or "picture element" is a single dot in an image. (Ex. 1002, ¶72). A pixel is also a portion of an image sensor that senses the intensity of incoming light at a particular position in space that corresponds to a position in an image. (Ex. 1002, ¶72). Miyagawa uses a particular type of pixel circuit called an "amplifier-type" pixel. (Ex. 1011, ¶0001)(Ex. 1002, ¶72). An "amplifier-type" pixel is a pixel that uses a photodiode to convert incoming light to an electric charge, but also has transistors within the area of the pixel circuit to move and amplify the charge of the photodiode. (Ex. 1002, ¶72).

A circuit diagram of a portion of an image sensor, showing multiple pixels (one of which is highlighted by an added, red-dashed box), is provided in Miyagawa's Fig. 3, reproduced here:



F I G. 3

(Ex. 1011, Fig. 3, ¶¶0030, 0057-0058)(Ex. 1002, ¶73). In Fig. 3, the pixel elements are laid out in a grid (nine elements of which are shown in Fig. 3, although typically there would be millions). (Ex. 1002, ¶73). Within the grid, each pixel element has a photodiode 36 (symbol:) and several transistors (symbol:). (Ex. 1002, ¶73). Incoming light enters the area of the photodiode 36 in each pixel, is converted to charge, processed by transistors in the pixel, and ultimately converted to form the

numerical values of a digital image. (Ex. 1002, ¶73).

Miyagawa provides semiconductor arrangements for portions of individual pixels. An example is shown in Fig. 9E, reproduced below, which is a cross-section of a semiconductor image sensor device in a portion of a pixel:

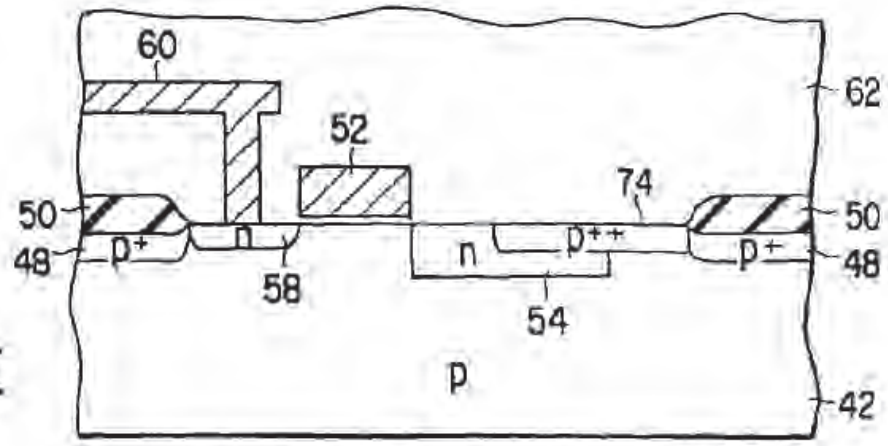


FIG. 9E

(Ex. 1011, Fig. 9E, ¶¶0036, 0110-0116)(Ex. 1002, ¶74). In Fig. 9E, there is a photodiode formed by the contact between the n-type region 54 and the p-type region 42. (Ex. 1011, Abstract, ¶¶0110, 0113, 0067)(Ex. 1002, ¶74). This photodiode will convert incoming light to electric charge (specifically: electrons and holes, with the electrons collected in the photodiode). (Ex. 1002, ¶74). The electrons can be read out through a read-out transistor formed from n-type region 54 (the source), electrode 52 (the gate electrode), and n-type region 58 (the drain). (Ex. 1011, ¶0113)(Ex. 1002, ¶74).

Miyagawa teaches active regions that have graded dopant regions. (Ex. 1011, Figs. 12-17, ¶¶0043, 0121-0132)(Ex. 1002, ¶75). Miyagawa, for example, teaches

a Seventh Embodiment having a dopant profile with depth as shown in Fig. 16, reproduced here (where the top surface of the substrate is on the left):

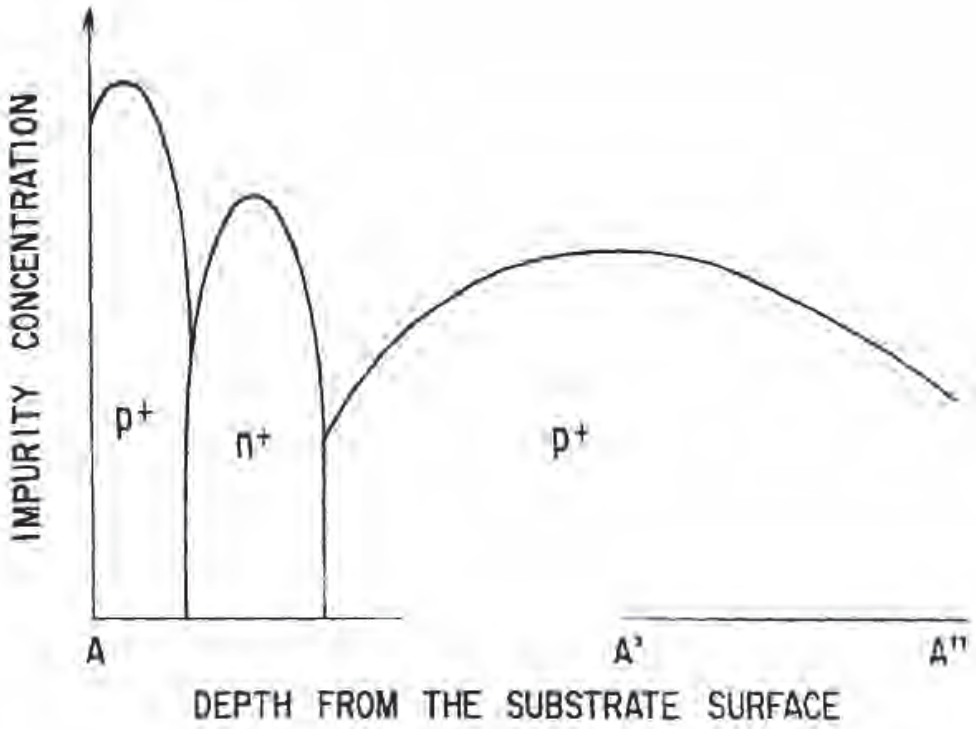
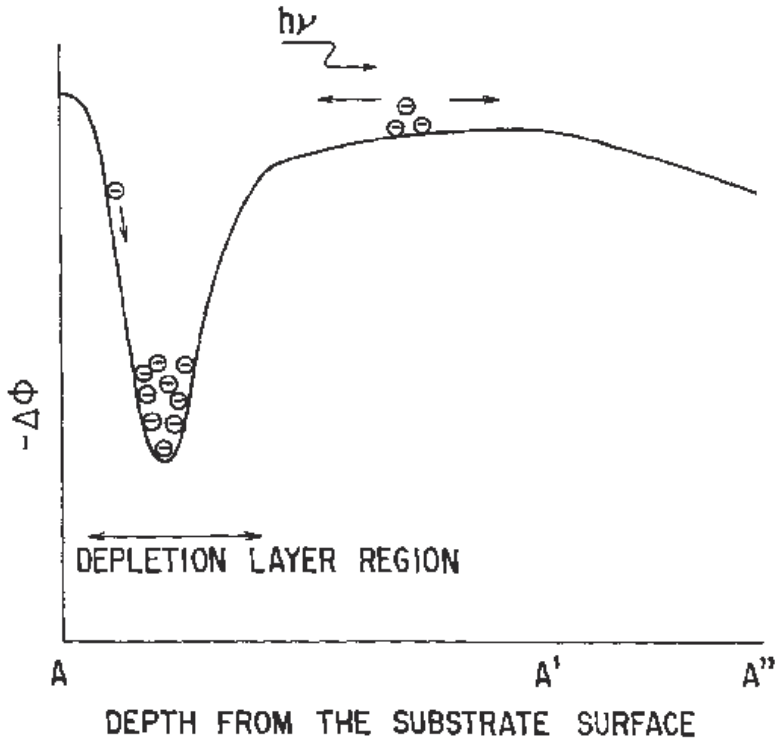


FIG. 16

(Ex. 1011, Fig. 16, ¶¶0043, 0125-0132)(Ex. 1002, ¶75). The dopant profile in Fig. 16 results in the relationship between the depth from the substrate surface and the electric potential as shown in Fig. 17, reproduced here:



F I G. 17

(Ex. 1011, Fig. 17, ¶0044)(Ex. 1002, ¶75). As shown in Fig. 17, charge carriers (shown as small circles with negative signs within them) that are near the surface (left side) are aided in their movement toward the lower portion of the substrate by the electric field that results from graded dopant profiles. (Ex. 1002, ¶75). Similarly, negative charge carriers that occur deeper are aided in their movement toward the lower portion of the substrate by the graded dopant profile. (Ex. 1011, ¶0131-0132)(Ex. 1002, ¶75). Miyagawa teaches that this arrangement is advantageous:

> "Thus, in a photodiode having an impurity concentration distribution profile as shown in FIG. 16, signal charges are apt to defect to the storage section when they are few in number, whereas they show a downward gradient toward the substrate when the substrate is

> irradiated with highly bright light so that the storage section is less liable to be saturated with signals as excessive signal charges are diffused toward the substrate to increase the dynamic range where the number of stored signals is increased in response to the intensity of incident light."

(Ex. 1011, ¶0132)(Ex. 1002, ¶75). This arrangement is "designed to realize a high dynamic range." (Ex. 1011, ¶0124)(Ex. 1002, ¶75).

C. Overview of the Ground

Miyagawa nearly anticipates the independent claims. This ground is presented as one of obviousness because Miyagawa does not *expressly* state that the dopant profile of Fig. 16 is used with the semiconductor structure shown in Fig. 9E. This ground thus posits that the dopant profile of Fig. 16 of Miyagawa would have been obvious to use with the structure shown in Fig. 9E of Miyagawa. (Ex. 1002, ¶76). This ground further posits that it would have been obvious to arrange adjacent pixel cells, each having an active region such as the one shown in Fig. 9E, to form an image sensor. Finally, this ground posits that Miyagawa renders certain dependent claims obvious.

D. Rationale (Motivation) Supporting Obviousness

It would have been obvious to use the dopant profile of Fig. 16 and the attendant electrical potential profile of Fig. 17 in the semiconductor cross-section shown in Fig. 9E. (Ex. 1002, ¶77).

First, the disclosure of the two embodiments in Miyagawa already suggests their combination. (Ex. 1002, ¶78). Miyagawa presents a number of related, structural embodiments (Figs. 4-9) directed at specific semiconductor arrangements for addressing a problem of leakage current. (*e.g.*, Ex. 1011, ¶0066-0067, 0112, 0116)(Ex. 1002, ¶78). Miyagawa then presents a number of embodiments that address a problem of saturation in bright light to provide a high dynamic range. (Ex. 1011, ¶¶0131-0132)(Ex. 1002, ¶78). It would have been obvious to combine these two techniques. *See Boston Sci. Scimed, Inc., et al. v. Cordis Corp., et al.*, 554 F.3d 982, 991 (Fed. Cir. 2009)("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.").

Furthermore, a POSITA would have been motivated to use the techniques of the Seventh Embodiment (including Figs. 16 and 17) in the device of Fig. 9E in order to achieve the advantage of high dynamic range, as expressly taught by Miyagawa. (Ex. 1011, ¶¶0001, 0025, 0124-0125, 0132)(Ex. 1002, ¶79). The embodiments were compatible and could have been combined with no unpredictable results. (Ex. 1002, ¶79).

Finally, the structure of Fig. 9E represents a known device that was ready for improvement using the known techniques of the Seventh Embodiment of Miyagawa, which would have been predictable and within ordinary skill to implement. (Ex. 1002, ¶80). *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416-21 (2007).

To the extent additional rationales to support obviousness are necessary, they will be explained in the Claim Mapping section below as appropriate.

E. *Graham* Factors

The **level of ordinary skill** encompassed a person having a Bachelor's Degree in electrical engineering, microelectronics engineering or a related field and three years of experience relating to semiconductor device manufacturing, where a higher level of education may substitute for experience and vice versa. (Ex. 1002, ¶82).

The **scope and content of the prior art** are discussed throughout the Ground.

The **differences between the prior art and the claims** are discussed in the sections entitled "Overview of the Ground" and "Rationale (Motivation) Supporting Obviousness", above, and in the claim mapping, below.

Petitioner is not aware of any **secondary considerations** that would make an inference of non-obviousness more likely.

F. Reasonable Expectation of Success

A person of ordinary skill in the art ("POSITA") in the relevant timeframe would have had a reasonable expectation of success in using the prior art in the manner discussed in this petition. (Ex. 1002, ¶86). As Mr. Guidash explains, the art was relatively predictable in the relevant timeframe (September 2004), with commercially available sophisticated circuit design, process modeling, and physic-based transistor modeling software tools. (Ex. 1002, ¶86). A POSITA would have

been able to make any necessary modifications to implement the Ground, and in particular would have been able to apply the techniques of Miyagawa's Seventh Embodiment in an image sensor having the structure of Fig. 9E in its pixel regions. (Ex. 1002, ¶86).

G. Analogous Art

Miyagawa is analogous art because it is in the same field as the '842 patent (semiconductor devices). (Ex. 1001, Abstract)(Ex. 1011, Abstract, ¶0001). Furthermore, the methods of Miyagawa would have been reasonably pertinent to the problems facing the named inventors, for example, the problem of controlling carriers in CMOS image sensors. (Ex. 1001, 3:44-64)(Ex. 1011, ¶¶0123-0133)(Ex. 1002, ¶87). *See Wyers v. Master Lock Co.*, 616 F.3d 1231, 1238 (Fed. Cir. 2010)("The Supreme Court's decision in *KSR* [cite omitted], directs us to construe the scope of analogous art broadly….").

H. Claim Mapping

This section maps the challenged claims to the relevant disclosures of Miyagawa, where the claim text appears in bold-italics, and the relevant mapping follows the claim text. The Petitioner has added numbering and lettering in brackets (*e.g.*, 1[a], [1b]) to certain claim elements, to facilitate the discussion.

<u>CLAIM 1</u>

"1[a]. A semiconductor device, comprising:"

Miyagawa teaches a **semiconductor device**, one example of which is shown in cross-section in Fig. 9E, reproduced here:

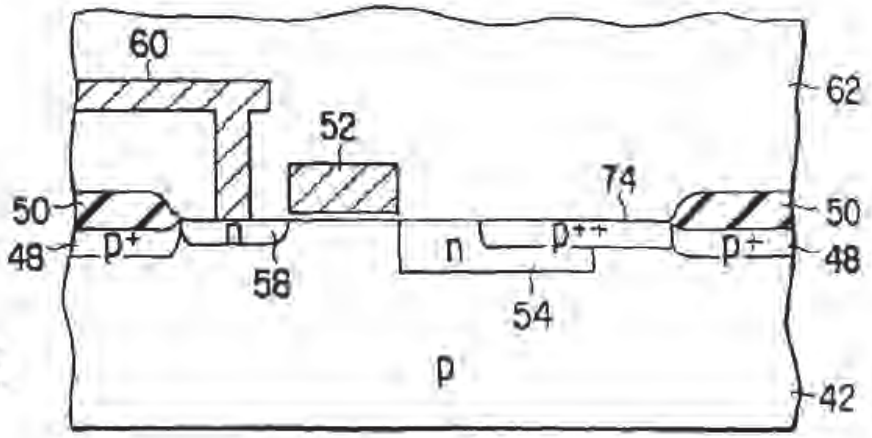


FIG. 9E

(Ex. 1011, Fig. 9, ¶¶0110-0111)(Ex. 1002, ¶89). The device shown in Fig. 9E is a cross section of the "solid-state imaging apparatus" of Miyagawa, which is also a semiconductor device. (Ex. 1011, ¶0001)(Ex. 1002, ¶89).

"[1b] a substrate of a first doping type at a first doping level having first and second surfaces;"

The device of Fig. 9E of Miyagawa has **a substrate of a first doping type at a first doping level having first and second surfaces,** in the form of a "p-type" semiconductor substrate 42. (Ex. 1011, ¶¶0110-0113, 0060)(Ex. 1002, ¶90). The substrate is **of a first doping type** because it is "p-type", which refers to a type of doping, and must obviously have a **first doping level**. (*Id.*). The substrate has **first and second surfaces**, which are the top surface and bottom surface of the device,

respectively. (Ex. 1002, ¶90). The surfaces are shown by the added, red-dashed lines in Fig. 9E, reproduced again here:

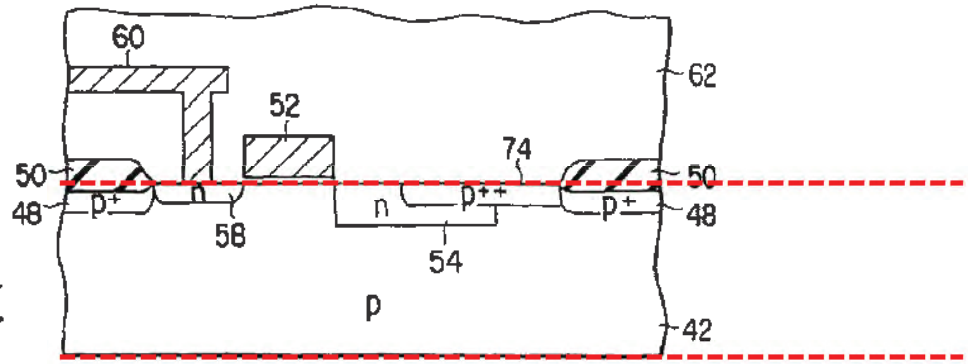


FIG. 9E

(Ex. 1011, Fig. 9E)(Ex. 1002, ¶90). As Mr. Guidash explains, the substrate comprises almost the entire thickness of a semiconductor device, whereas active devices, such as transistors and photodiodes, are built with relatively shallow depths at the top of the substrate. (Ex. 1002, ¶90).

> ***"[1c] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"***

Miyagawa teaches **a first active region disposed adjacent the surface** in the form of a region indicated by the added red arrow in Fig. 9E, reproduced below:

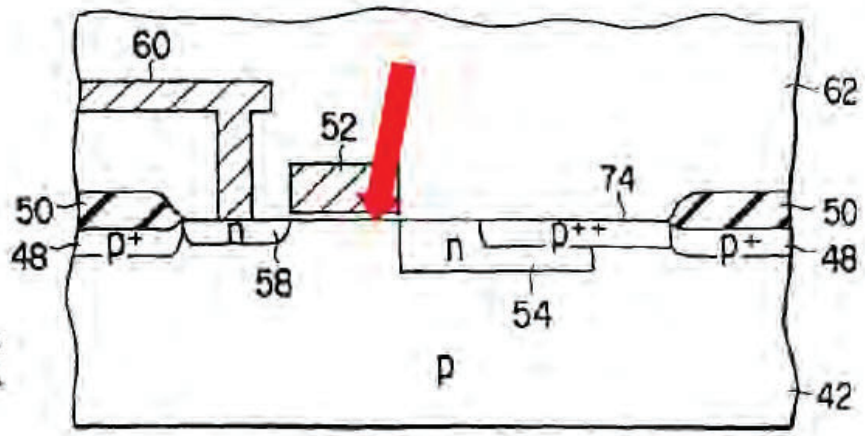


FIG. 9E

(Ex. 1011, Fig. 9E)(Ex. 1002, ¶91). Laterally, the active region extends between the isolating oxide portions 50 on the right and left sides of the figure. (Ex. 1002, ¶91). The active region is **adjacent the surface** because it is formed in the surface of the substrate. (Ex. 1002, ¶91).

The active region furthermore has **a second doping type opposite in conductivity to the first doping type.** (Ex. 1011, ¶0113)(Ex. 1002, ¶92). Specifically, there are n-type doping regions 58 and 54 in the active region. (Ex. 1011, ¶0113)(Ex. 1002, ¶92). N-type doping is **opposite in conductivity to the first doping type.** (Ex. 1011, ¶¶0060, 0110-0113)(Ex. 1002, ¶92). The first doping type was p-type, as explained above under limitation [1b]. (Ex. 1002, ¶92).

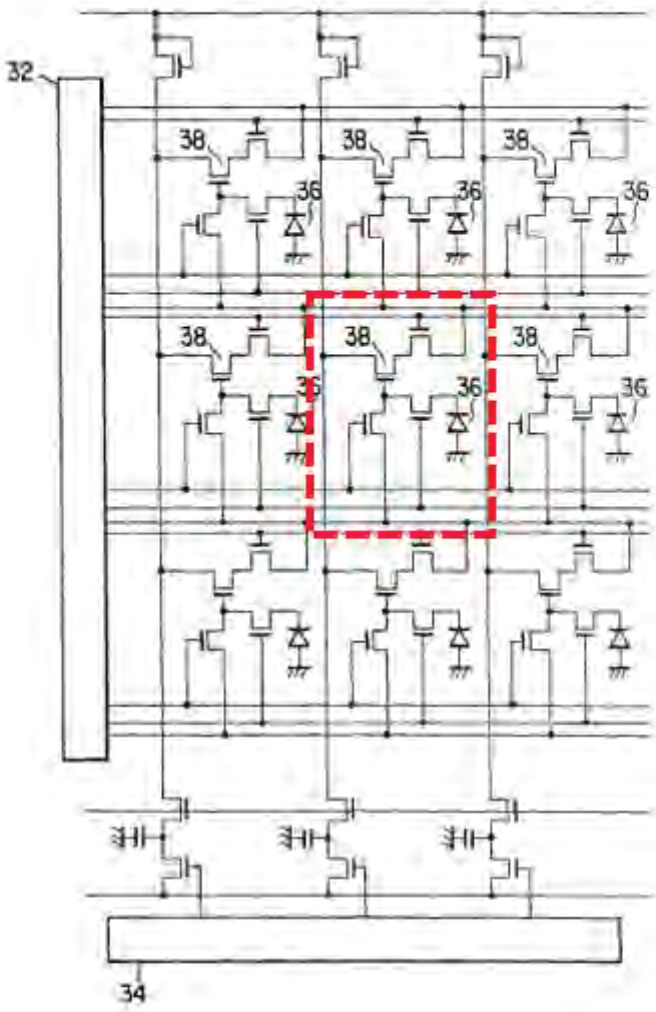
Transistors can be formed within the active region. (Ex. 1002, ¶93). Specifically, the active region has a "read-out transistor" with a "gate electrode 52" (Ex. 1011, ¶0113), which is formed from n-type source and drain regions 58 and 54, as well as p-type channel region under the gate electrode 52. (Ex. 1002, ¶93). This

meets the claim language under the Patent Owner's interpretation of the claim. (Ex. 1014, p. 33). Furthermore, an amplifier and other transistors are found in each pixel region (Ex. 1011, ¶¶0113, 0057-0058, 0001, Fig. 3), making it obvious to form these in the same "active region" to maximize photodiode area by avoiding additional separation regions. (Ex. 1002, ¶93).

"[1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

Miyagawa renders obvious a **second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed**. (Ex. 1002, ¶94). The **second active region** is similar to the first, but in an adjacent pixel cell in the image sensor array. (Ex. 1002, ¶94).

Specifically, Miyagawa teaches an image sensor, including "an imaging means comprising an **array of pixels**, each having at least a photodiode for a photoelectric conversion region…." (Ex. 1011, claim 17, *see also* claims 22, 24, ¶¶0001-0003, 0015, 0019-0021, 0058, 0110, 0157, Figs. 2-3)(Ex. 1002, ¶95). An array of pixel cells is shown in Fig. 3 of Miyagawa, reproduced below, which "is a schematic circuit diagram of a typical solid state imaging apparatus comprising an amplifier type MOS sensor." (Ex. 1011, ¶0030)(Ex. 1002, ¶95). In Fig. 3 below, a red-dashed box has been added around a single unit cell:



F I G. 3

(Ex. 1011, Fig. 3, ¶¶0030, 0057-0058)(Ex. 1002, ¶95). Each unit cell has a photodiode 36 with an associated set of transistors, including the read-out transistor connected directly to the photodiode. (Ex. 1011, ¶¶0057-0058)(Ex. 1002, ¶95).

As is obvious from Fig. 3 and associated teachings in Miyagawa, each unit cell containing a photodiode and transistors is adjacent to multiple other unit cells. (Ex. 1011, Fig. 3, ¶¶0057-0058)(Ex. 1002, ¶96). This was obvious both from the

direct teachings of Miyagawa (Ex. 1011, claims 17, 22, 24, ¶¶0001-0003, 0019-0021, 0058, 0110, 0157, Figs. 2-3)(Ex. 1002, ¶96), and because this was standard operation for an image sensor in the relevant timeframe. (Ex. 1002, ¶96).

An additional active region, containing a photodiode with n-type regions 58 and 54 as well as a read-out transistor (having the same characteristics explained above for the first active region under element [1c]) is obviously found within each unit cell. (Ex. 1011, ¶¶0058-0059, 0110-0111)(Ex. 1002, ¶¶97). The active region in a unit pixel cell is obviously **separated** from adjacent unit pixels by oxide portions 50 and inter-pixel separation regions. (Ex. 1011, ¶¶0061, 0111, 0130)(Ex. 1002, ¶¶97).

Miyagawa thus renders obvious a **second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed, in the form of the active region of an adjacent pixel cell**. (Ex. 1002, ¶98).

"[1e] transistors formed in at least one of the first active region or second active region; and"

As discussed above under limitations [1c] and [1d], at least a read-out transistor with source and drain regions 58 and 54 is formed in each of the first and second active regions. This meets the claim language under the Patent Owner's interpretation of the claim. (Ex. 1011, ¶¶0113, 0057-0058, 0001, Fig. 3)(Ex. 1002,

¶99)(Ex. 1014, p. 8)(Patent Owner arguing "According to claim 842:1, there may be multiple active regions (*i.e.*, the first and second active regions), where **a transistor** is formed in at least one of them (*i.e.*, transistors formed in at least one of the active regions).")(Emphasis added).

Furthermore, an amplifier and other transistors are found in each pixel region (Ex. 1011, ¶¶0113, 0057-0058, 0001, Fig. 3), making it obvious to form these in the same "active region" to maximize photodiode area by avoiding additional separation regions. (Ex. 1002, ¶99).

"[1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

Miyagawa renders obvious **a portion of the first active region having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate**. Specifically, Miyagawa teaches a dopant profile as shown in connection with the Seventh Embodiment, in order to achieve a high dynamic range. (Ex. 1011, ¶¶0124-0125)(Ex. 1002, ¶100). The graded dopant profile is shown in Fig. 16, reproduced below, where the left side of the figure represents the surface of the device ("A", *see* Fig. 14), with increasing depth to the right-hand side of the device.

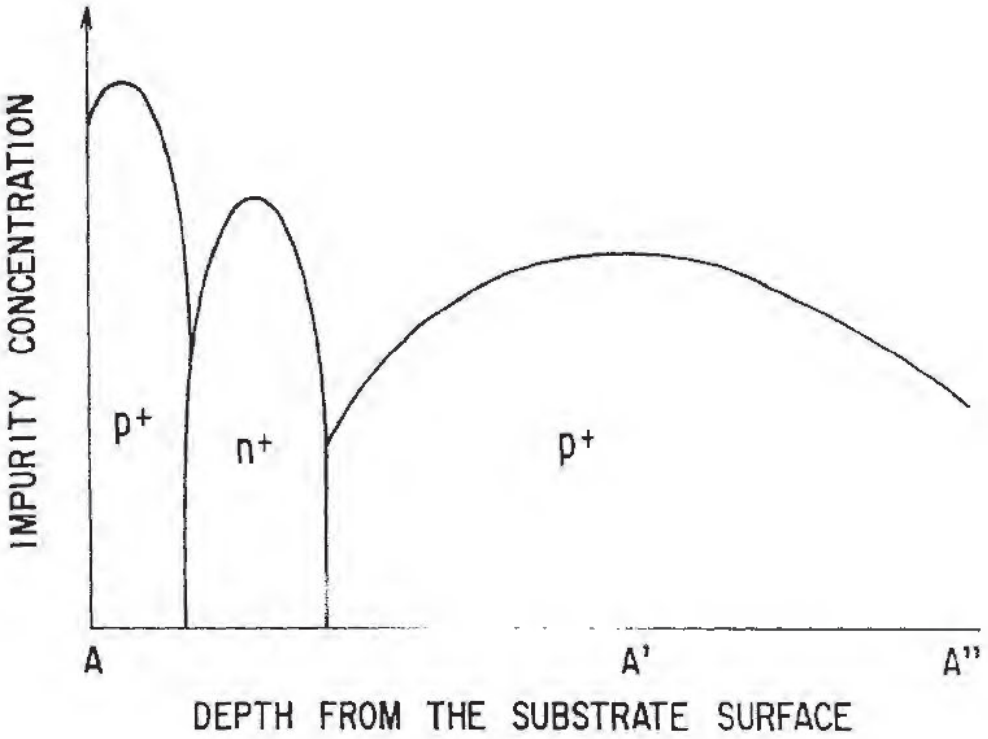


FIG. 16

(Ex. 1011, Fig. 16, ¶¶0043, 0127, 0131-0132)(Ex. 1002, ¶100). As can be seen from the Figure, there is no portion of the dopant profile that is not graded, as would be expected from Miyagawa's description of the processes involved. (Ex. 1011, ¶¶0124-0133)(Ex. 1002, ¶100).

Under the Patent Owner's claim construction apparent from both its claim construction briefing and its infringement contentions,[1] Miyagawa teaches that the

[1] (Ex. 1014, pp. 26)(patent owner's claim construction briefing, interpreting all claim terms in all asserted patents containing "to aid the movement" of carriers,

graded dopant concentrations **aid carrier movement from the first surface to the second surface of the substrate**, because graded dopant profiles of Miyagawa move carriers downward in the device. Specifically, Miyagawa teaches that the dopant profile shown in Fig. 16 results in a potential function as shown in Fig. 17, reproduced here:

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stating "[t]he claim even says where the movement occurs: it is in the drift layer, and the carriers move **downward**")(Emphasis added); (Ex. 1017, pp. 12-13 (numbers at top))(Patent Owner's infringement contentions directed to a Sony image sensor, describing alleged dopant profiles that aid carrier movement from the surface to the bottom of the substrate, by arguing that "**at least one downward sloped portion** is shown in each of the boron-11 and arsenic plots above, viewed from right (more depth) to left (less depth).")(Emphasis added)(Ex. 1017, pp. 31-32)(applying the same reasoning to the '014 patent).

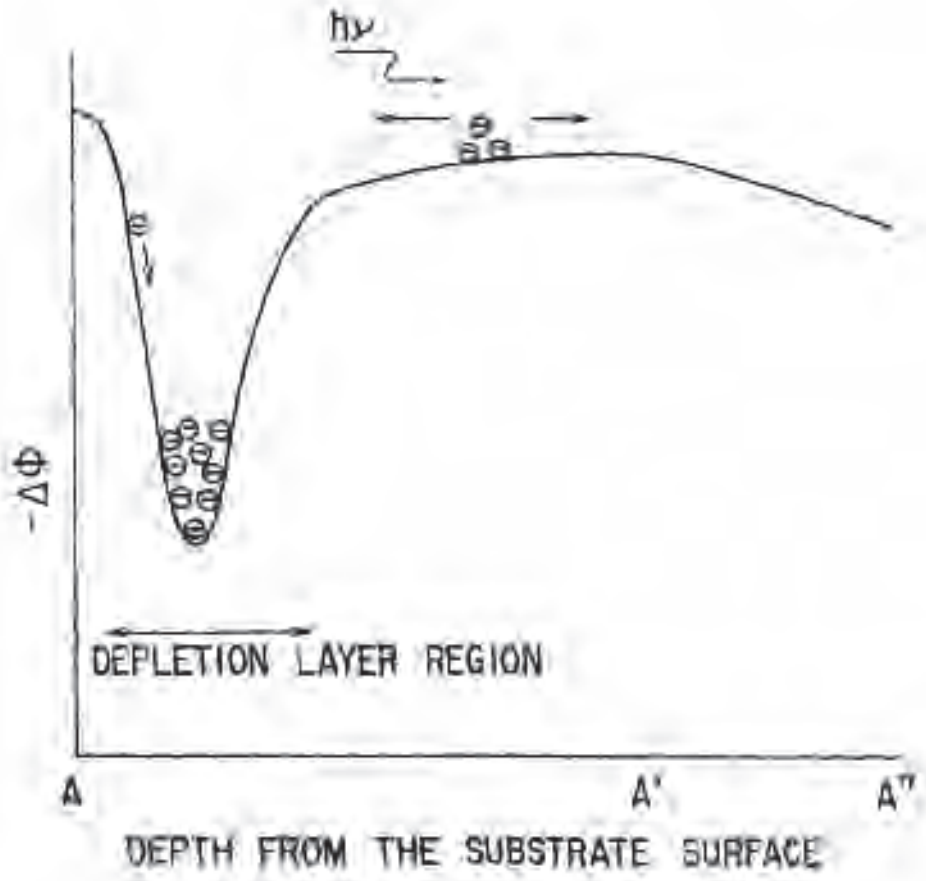


FIG. 17

(Ex. 1011, Fig. 17, ¶¶0044, 0131-0132)(Ex. 1002, ¶101). As Fig. 17 shows, electrons will be aided in their movement down the slope of the function of Fig. 17 by the electric fields involved. (Ex. 1002, ¶101). In the regions near the first (top) surface and in the regions deeper than (to the right of) A', the electrons will be aided in their movement toward the second surface (bottom) of the substrate. (Ex. 1011, ¶¶0131-0132)(Ex. 1002, ¶101). Miyagawa explains, for example, that:

> "In a photodiode having an impurity concentration distribution profile as described above by referring to FIG. 16, some of the signal

> charges that are photoelectrically converted by incident light hv in regions under the depletion layer are distributed from depth A' as viewed from the surface A of the substrate further down to the inside A" of the substrate, while the others are distributed to the signal storage section."

(Ex. 1011, ¶0131, *see also* ¶0132)(Ex. 1002, ¶101). As Mr. Guidash explains, this effect is caused in each pixel cell by the graded dopant profiles in the active regions. (Ex. 1002, ¶101).

It would have been obvious to use the graded dopant profile of Fig. 16, or a similar graded dopant profile, in the active region of Fig. 9E of Miyagawa, for the reasons discussed above in the section entitled "Rationale (Motivation) for the Combination". (Ex. 1002, ¶102).

Miyagawa thus renders obvious having **at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.** (Ex. 1002, ¶103).

Furthermore, during prosecution of related U.S. Patent No. 8,421,195, the Applicant stated that "a graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carrier into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concertation of dopant." (Ex.

1006, pp. 100-101)(*citing* Ex. 1008, 5:11-13). Accordingly, under Applicant's interpretation, the dopant profiles of Miyagawa are sufficient to meet the claim language.

CLAIM 2

"2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate."

Miyagawa's Fig. 9E teaches a p-type substrate, as discussed above under claim 1, element [1b]. (Ex. 1002, ¶104).

CLAIM 3

"3. The semiconductor device of claim 1, wherein the substrate is an n-type substrate."

Miyagawa renders claim 3 obvious. Although Miyagawa's embodiment in Fig. 9E has a p-type substrate, Miyagawa also teaches that it is possible to use an n-type substrate. (Ex. 1011, ¶¶0142, 0146, Fig. 10, Fig. 20A)(Ex. 1002, ¶105). For example, a POSITA could use the same structure that Miyagawa has shown in Fig. 9E, where the p-type substrate is replaced by a p well in an n-type substrate. (Ex. 1002, ¶105). It would have been obvious to a POSITA in the relevant timeframe that there were only two doping types for silicon, that these dopant types were known alternatives, and that either doping type could have been used in the embodiment of Fig. 9E, with no substantial difference in function. (Ex. 1002, ¶105). *See KSR*, 550 U.S. at 416-21.

CLAIM 4

"4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

Miyagawa renders obvious a substrate with epitaxial silicon on top of a nonepitaxial substrate. While Miyagawa does not expressly state whether its layers are epitaxial or nonepitaxial, claim 4 represented a common practice in the relevant timeframe, as explained by Mr. Guidash. (Ex. 1002, ¶106). In general, epitaxial silicon layers are higher quality for device manufacturing, but slower to grow. Therefore, providing a thicker nonepitaxial substrate for handling and stability, topped by a higher-quality epitaxial substrate, made economic sense in the relevant timeframe. (Ex. 1002, ¶106). Thus, it would have been obvious for Miyagawa to provide for a **substrate having epitaxial silicon on top of a nonepitaxial substrate**. (Ex. 1002, ¶106).

CLAIM 5

"5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices."

The first and second active regions of Miyagawa contain a n-channel device, which is the read-out transistor 52. (Ex. 1011, ¶0113)(Ex. 1002, ¶107). The n-channel nature of the device is apparent because of the n-type source and drain 58/54 regions. (Ex. 1002, ¶107).

CLAIM 7

"7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

Miyagawa renders obvious having **the first and second active regions separated by at least one isolation region**. For example, Fig. 14 (reproduced below) shows isolation between adjacent pixel units having respective active regions:

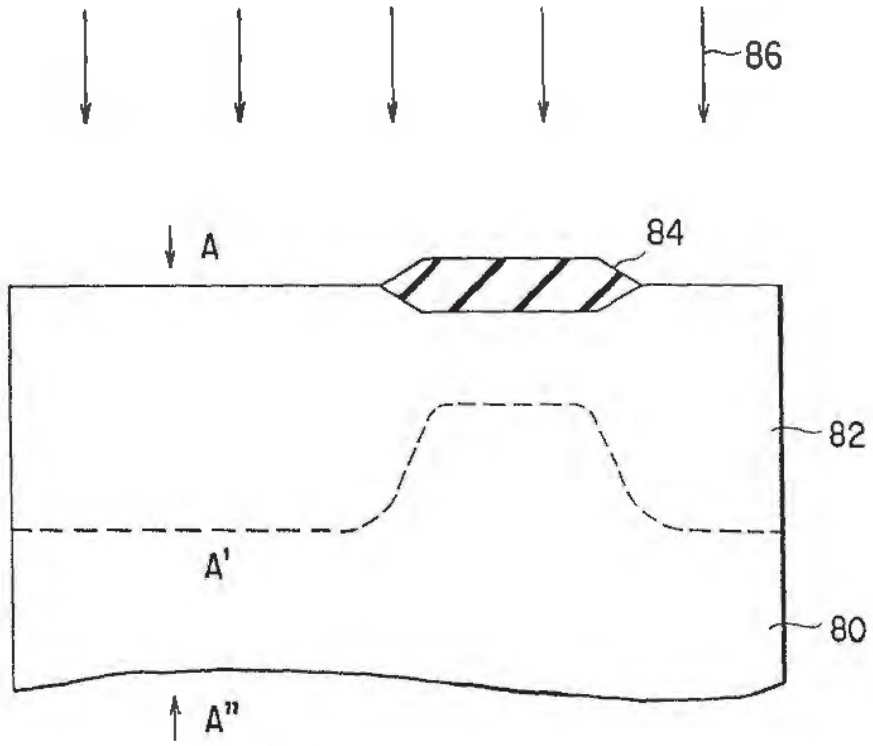


FIG. 14

(Ex. 1011, Fig. 14, ¶¶0041, 0128-0130)(Ex. 1002, ¶108). Miyagawa states:

"Referring to FIG. 14, a LOCOS layer 84 is formed as device

> **separating layer** on the surface A of the substrate 80 prior to forming a signal charge barrier layer 82 in the substrate 80."

(Ex. 1011, ¶0128)(Ex. 1002, ¶108). The "LOCOS" (which stands for **LOC**al **O**xidation of **S**ilicon) layer is an insulating oxide layer that electrically isolates devices, and is thus an **isolation region**. (Ex. 1002, ¶108). It corresponds to the isolation regions 50 as shown in Fig. 9E. (Ex. 1002, ¶108).

Miyagawa further teaches forming an interdevice barrier layer 82 "below the LOCOS layer 84 so that signal charges are apt to be stored in the storage section and signals can be prevented from being mixed with those of adjacent pixels." (Ex. 1011, ¶0132)(Ex. 1002, ¶109). Thus, Miyagawa teaches that each of the LOCOS region 84 and the interdevice barrier layer 82 form isolation regions that separate "pixels", and (as discussed above under claim 1, elements [1c] and [1d]), the pixels contain the first and second active regions. (Ex. 1002, ¶109).

CLAIM 8

> ***"8. The semiconductor device of claim 1 , wherein the graded dopant is fabricated with an ion implantation process."***

Miyagawa teaches **the graded dopant is fabricated with an ion implantation process**. (Ex. 1011, ¶¶0126-0129, 0060, 0062, 0065, and 0110-0111)(Ex. 1002, ¶110).

CLAIM 9

Claim 9 is similar to claim 1. A comparison (redline) of differences between

claims 1 and 9 is provided in Ex. 1009 (p. 1).

"9[a]. A semiconductor device, comprising:"

See above, claim 1, element 1[a]. (Ex. 1002, ¶111).

"[9b] a substrate of a first doping type at a first doping level having first and second surfaces;"

See above, claim 1, element [1b]. (Ex. 1002, ¶112).

"[9c] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

See above, claim 1, element [1c]. (Ex. 1002, ¶113). The present claim element [9c] adds that transistors can be formed "in the surface thereof". As discussed above under claim 1, element [1c], and as shown in Fig. 9E of Miyagawa, the transistors can be formed in the surface of the substrate and active region. (Ex. 1011, Fig. 9E, ¶0113)(Ex. 1002, ¶113).

"[9d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

See above, claim 1, element [1d]. (Ex. 1002, ¶114). The present claim element [9d] adds that transistors can be formed "in the surface thereof". As discussed above under claim 1, element [1d], and as shown in Fig. 9E of Miyagawa,

the transistors are formed in the surface of the substrate and active region. (Ex. 1011, Fig. 9E, ¶0113)(Ex. 1002, ¶114).

"[9e] transistors formed in at least one of the first active region or second active region; and"

See above, claim 1, element [1e]. (Ex. 1002, ¶115).

"[9f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate."

See above, claim 1, element [1f]. (Ex. 1002, ¶116). The present claim element [9f] states that the dopant concentration is "to aid carrier movement from the surface to the substrate", as opposed to being "to aid carrier movement from the first surface to the second surface of the substrate", as in claim 1. This difference in claim language, however, does not make a material difference to the claim interpretation. (Ex. 1002, ¶116)(Ex. 1006, p. 100)(Ex. 1017, pp. 12-13 (numbers at top)).

CLAIM 10

"10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate."

See above, claim 2. (Ex. 1002, ¶117).

CLAIM 11

"11. The semiconductor device of claim 9, wherein the substrate is an n-type substrate."

See above, claim 3. (Ex. 1002, ¶118).

CLAIM 12

"12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

See above, claim 4. (Ex. 1002, ¶119).

CLAIM 13

'13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices."

See above, claim 5. (Ex. 1002, ¶120).

CLAIM 15

"15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region."

See above, claim 7. (Ex. 1002, ¶121).

CLAIM 16

"16. The semiconductor device of claim 9 , wherein the graded dopant is fabricated with an ion implantation process."

See above, claim 8. (Ex. 1002, ¶122).

CLAIM 17

"17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

Miyagawa teaches that the first and second active regions are formed adjacent

the first surface (*i.e.*, the top) of the substrate. (Ex. 1002, ¶123). *See* above, claim 1, elements [1c] and [1d], as well as Fig. 9E of Miyagawa. (Ex. 1002, ¶123).

CLAIM 18

> ***"18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region."***

As detailed above under claim 1, element [1e], Miyagawa teaches a read-out transistor with source and drain regions 58 and 54, and renders obvious an amplifier transistor. (Ex. 1011, ¶0057, ¶0112-0116)(Ex. 1002, ¶124). These transistor MOS transistors, having a source, a drain, a gate and a channel region. (Ex. 1002, ¶124). (Ex. 1002, ¶124). Under the Patent Owner's construction, *see* Ex. 1017, pp. 14-15, this meets the claim language.

Ground 2. Claims 1-18 were obvious over Yamashita

Claims 1-18 were obvious under 35 U.S.C. §103(a) over U.S. Pat. No. 6,420,763 ("**Yamashita**")(Ex. 1005).

Yamashita was not of record during the prosecution of the application leading to the '842 patent.

A. Effective Prior Art Date of Yamashita

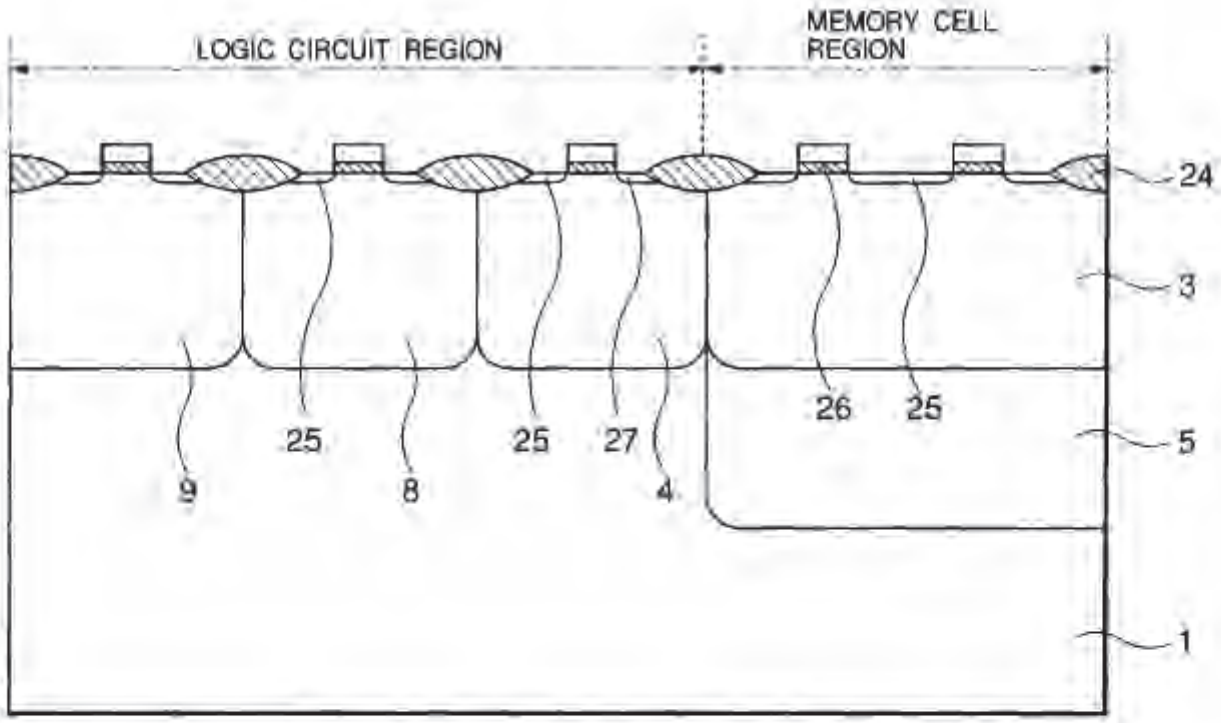
Yamashita is a U.S. patent that issued on July 16, 2002, and is thus prior art

under pre-AIA 35 U.S.C. §102(b).

B. Overview of the Combination

Yamashita teaches semiconductor devices for, *e.g.*, DRAM in integrated circuits. (Ex. 1005, 1:7-15)(Ex. 1002, ¶126). In Yamashita's Eighth Embodiment, on which this Ground primarily relies, Yamashita teaches semiconductor structures useful for memory having both a logic circuit region and a memory cell region, as shown in Fig. 53, reproduced here:

FIG.53



(Ex. 1005, Fig. 53, 6:1-2, 21:19-34)(Ex. 1002, ¶125). Yamashita states:

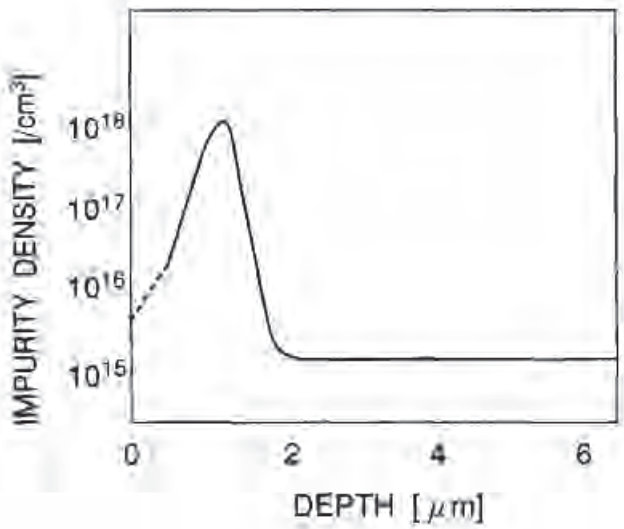
> "The semiconductor device is divided roughly into an element region (a memory cell region) for storing information of large-capacity

> mainly and an element region (a logic circuit region) for executing logical calculations while exchanging information of large-capacity with the memory cell region."

(Ex. 1005, 21:27-32)(Ex. 1002, ¶126).

Yamashita further teaches "retrograde" n-wells and p-wells, meaning wells that have a doping concentration peak below the surface. (Ex. 1005, 21:19-41, Figs. 10, 55)(Ex. 1002, ¶127). These wells have graded dopant concentration profiles that aid carrier movement. (Ex. 1002, ¶127). For example, Fig. 55 shows the dopant concentration with depth of a retrograde p-well:

FIG.55



(Ex. 1005, Fig. 55, 6:5-6, 21:35-41, 23:18-26)(Ex. 1002, ¶127).

Yamashita, on its own, expressly teaches almost all elements of the claims.

(Ex. 1002, ¶128). This Ground is presented as one of obviousness for a few reasons. First, Yamashita describes retrograde n-wells and retrograde p-wells. "Retrograde" wells are wells that have a dopant level peak below the surface. (Ex. 1005, Fig. 55, 21:35-41)(Ex. 1002, ¶128). While Yamashita expressly shows a dopant profile concentration having a graded dopant profile in a retrograde p-well, it does not illustrate the corresponding graded dopant concentration profile in a retrograde n-well, which would have been obvious. (Ex. 1005, Figs 77 and 82, 1:50-53, 2:38-42)(Ex. 1002, ¶128). Second, Yamashita teaches that graded dopant profiles create potential gradients that aid carrier movement, and the ability to aid carrier movement in the specific Eighth Embodiment on which the Ground relies would have been obvious. (Ex. 1002, ¶128). Finally, this Ground also posits obviousness for certain dependent claims, as explained in detail in the claim mapping section where appropriate. The Rationale underpinning other obviousness grounds will be presented in the Claim Mapping section, under each claim element as appropriate.

C. Rationale (Motivation) Supporting Obviousness

The Rationale supporting obviousness will be explained below in the Claim Mapping section, below, under the claim limitation to which the obviousness argument pertains.

D. *Graham* Factors

The **level of ordinary skill** encompassed a person having a Bachelor's Degree

in electrical engineering, microelectronics engineering or a related field and three years of experience relating to semiconductor device manufacturing, where a higher level of education may substitute for experience and vice versa. (Ex. 1002, ¶130).

The **scope and content of the prior art** are discussed throughout the Ground.

The **differences between the prior art and the claims** are discussed in the section entitled "Overview of the Ground", above, and in the claim mapping, below.

Petitioner is not aware of any **secondary considerations** that would make an inference of non-obviousness more likely.

E. Reasonable Expectation of Success

A person of ordinary skill in the art ("POSITA") in the relevant timeframe would have had a reasonable expectation of success in using the prior art in the manner discussed in this petition. (Ex. 1002, ¶134). As Mr. Guidash explains, the art was relatively predictable in the relevant timeframe (September 2004), with commercially available and sophisticated circuit design, process modeling, and physic-based transistor modeling software tools. (Ex. 1002, ¶134). A POSITA would have been able to make any necessary modifications to implement the Ground, and in particular would have been able to adjust doping gradients, electric fields created by dopant gradients, and carrier movement to effect the purposes of Yamashita. (Ex. 1002, ¶134).

F. Analogous Art

Yamashita is analogous art because it is directed to the same field as the '842 patent (semiconductor devices). (Ex. 1001, claim 1, Abstract, 1:32-39)(Ex. 1005, Title, Abstract). Furthermore, the teachings of Yamashita would have been reasonably pertinent to the problems facing the named inventors, specifically, the improvement of memory function. (Ex. 1001, 3:44-64)(Ex. 1005, 1:12-3:22)(Ex. 1002, ¶135). *See Wyers*, 616 F.3d at 1238.

G. Claim Mapping

This section maps the challenged claims to the relevant disclosures of Yamashita, where the claim text appears in bold-italics, and the relevant mapping follows the claim text. The Petitioner has added numbering and lettering in brackets (*e.g.*, 1[a], [1b]) to certain claim elements, to facilitate the discussion.

CLAIM 1

"1[a]. A semiconductor device, comprising:"

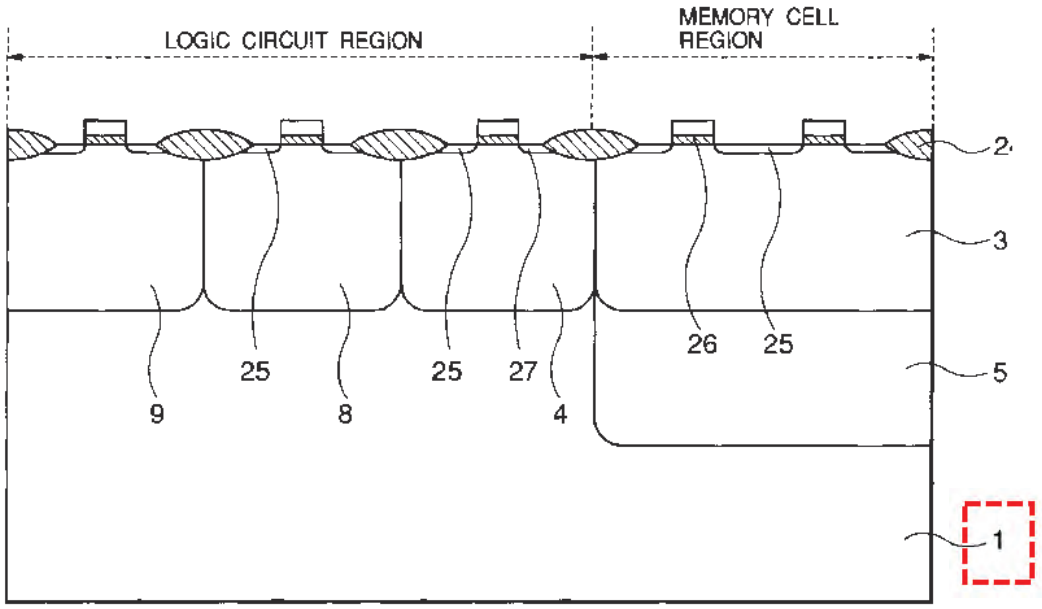
Yamashita teaches a semiconductor device. (Ex. 1005, Title, 1:7-9)(Ex. 1002, ¶137).

"[1b] a substrate of a first doping type at a first doping level having first and second surfaces;"

Yamashita teaches **a substrate of a first doping type at a first doping level having first and second surfaces**. Yamashita teaches a semiconductor device

having a **substrate 1**, as shown below in the reproduction of Fig. 53 of Yamashita, with an added, red-dashed box to show the reference numeral 1 of the substrate:

FIG.53



(Ex. 1005, Fig. 53, 6:1-2, 7:19-21, 21:20-24, 22:19-24)(Ex. 1002, ¶138).

The substrate 1 is "p type semiconductor substrate 1 containing boron of a concentration on the order of $1 \times 10^{16} / cm^3$". (Ex. 1004, 6:1-2, 21:20-24, 22:19-24, 7:19-21)(Ex. 1002, ¶139). Thus, the substrate is **of a first doping type** (p-type) **at a first doping level** ($1 \times 10^{16} / cm^3$). (Ex. 1005, 8:13-14)(Ex. 1002, ¶139). The substrate has a **first surface** (the top surface of the device shown in Fig. 53) and a **second surface** (the bottom surface as indicated in Fig. 53), and thus has **first** and **second surfaces**. (Ex. 1002, ¶139).

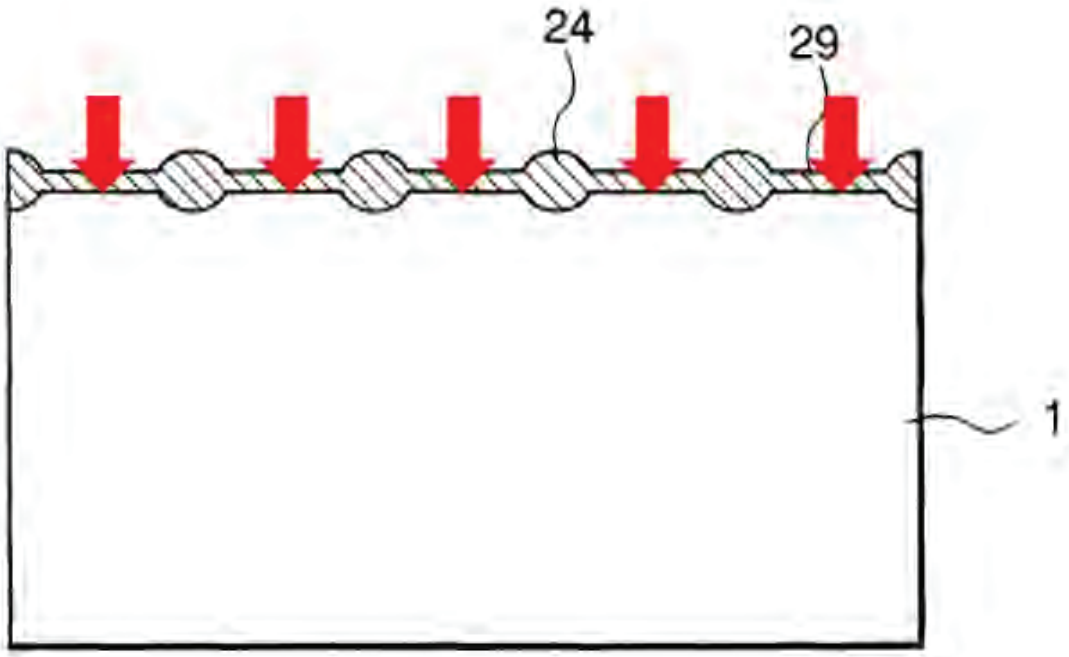
"[1c] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

Yamashita teaches **a first active region disposed adjacent the first surface with a second doping type opposite in conductivity to the first doping type within which transistors can be formed**. Yamashita teaches a series of active regions separated by separation regions:

> "As shown in FIG. 57, **the field oxide film 24 is formed on the separation region** on the main surface of the p type semiconductor substrate 1 containing boron of concentration on the order of 1×10^{16} / cm^3, and **the oxide film 29 for the gate oxide film 26 is formed on the active region**."

(Ex. 1005, 22:33-37)(Emphasis added)(Ex. 1002, ¶140). Figure 57 of Yamashita (referenced in the quote above) is reproduced below, with the locations of the eventual active regions indicated with added red arrows:

FIG.57



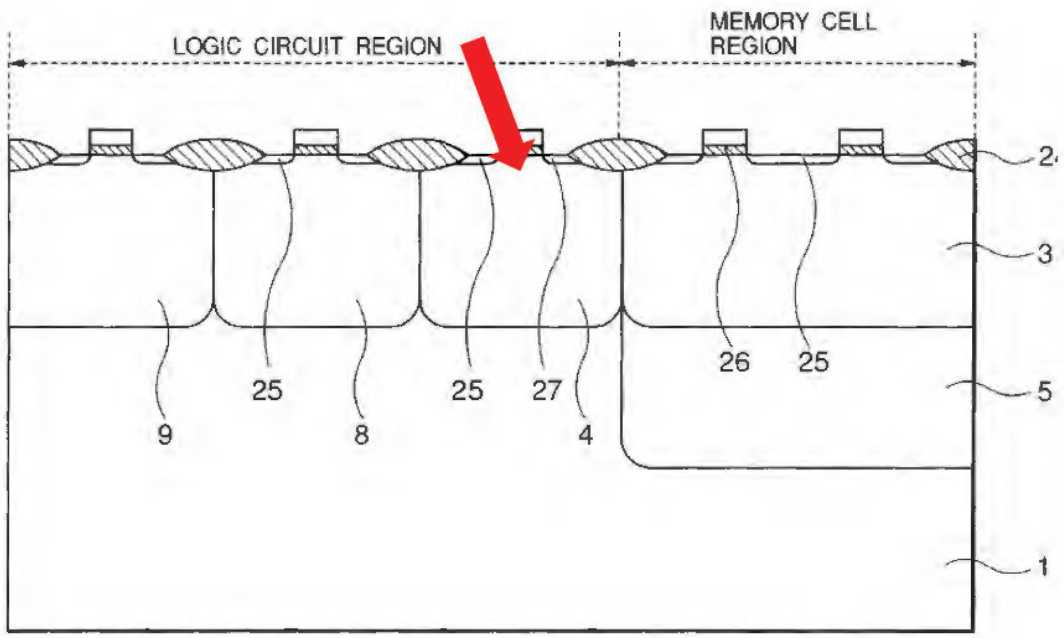
(Ex. 1005, Fig. 57, 6:9-10, 22:29-39)(Ex. 1002, ¶140). The active regions at this stage in manufacturing are covered by a thin gate oxide, and separated by thick portions of field oxide 24. (Ex. 1005, 22:33-37)(Ex. 1002, ¶140). The field oxide has the function of isolating active regions from one another. (Ex. 1005, 22:33-37)(Ex. 1002, ¶140). The "gate oxide", after later steps, will become the oxide that separates gate electrodes from transistor channels in MOSFET transistors. (Ex. 1002, ¶140).

The active regions are disposed **adjacent to** the **first surface of the substrate** 1. (Ex. 1005, Fig. 57, 22:33-37)(Ex. 1002, ¶141).

Yamashita teaches that certain active regions will have n-type doping, which

is **a second doping type opposite in conductivity to the first doping type** (which is p-type, as discussed above under claim limitation [1b]). (Ex. 1005, 23:4-16, 21:55-58, 21:66-22:1, 21:20-24, 22:7-9)(Ex. 1002, ¶142). The **first active region** with an n-type doping is indicated by the added red arrow in the reproduction of Fig. 53, reproduced below:

FIG.53



(Ex. 1005, 6:1-2, 21:20-24)(Ex. 1002, ¶142).

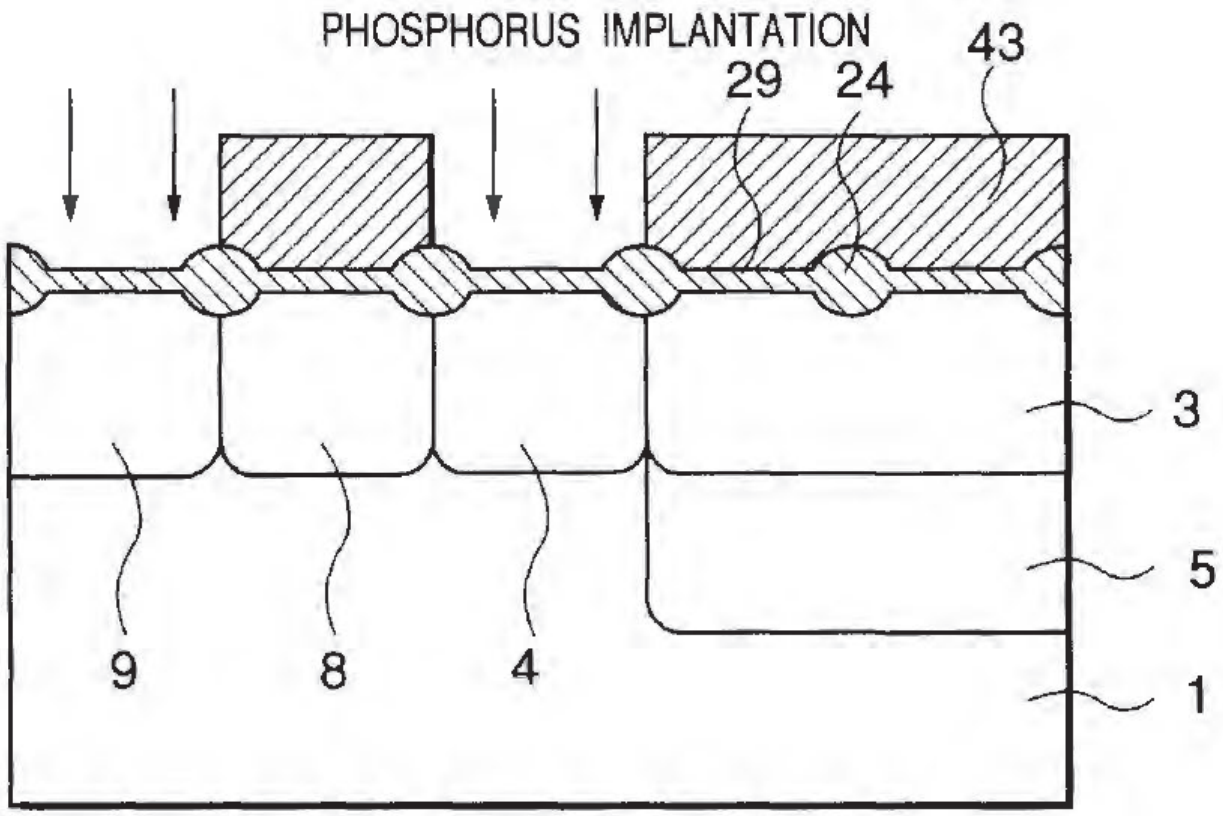
The **first active region** is formed by ion implantation of Phosphorous, producing a "retrograde n well 4" extending from the surface of the semiconductor to some depth. Yamashita explains:

> "As shown in FIG. 63, a resist 43 is formed. The resist 43 has an opening portion on a formation region for the PMOSFET in the logic

> circuit region. **Phosphorus, which is a source of n type impurity** ions, **is implanted** through the opening portion in the formation region by conditions of 300 keV - 2.5 MeV, $1 \times 10^{12} - 1 \times 10^{14} / cm^2$, and the **retrograde n wells 4**, **9 are formed**."

(Ex. 1005, 23:4-10)(Emphasis added)(Ex. 1002, ¶143). Figure 63, discussed in the quote above, is reproduced here:

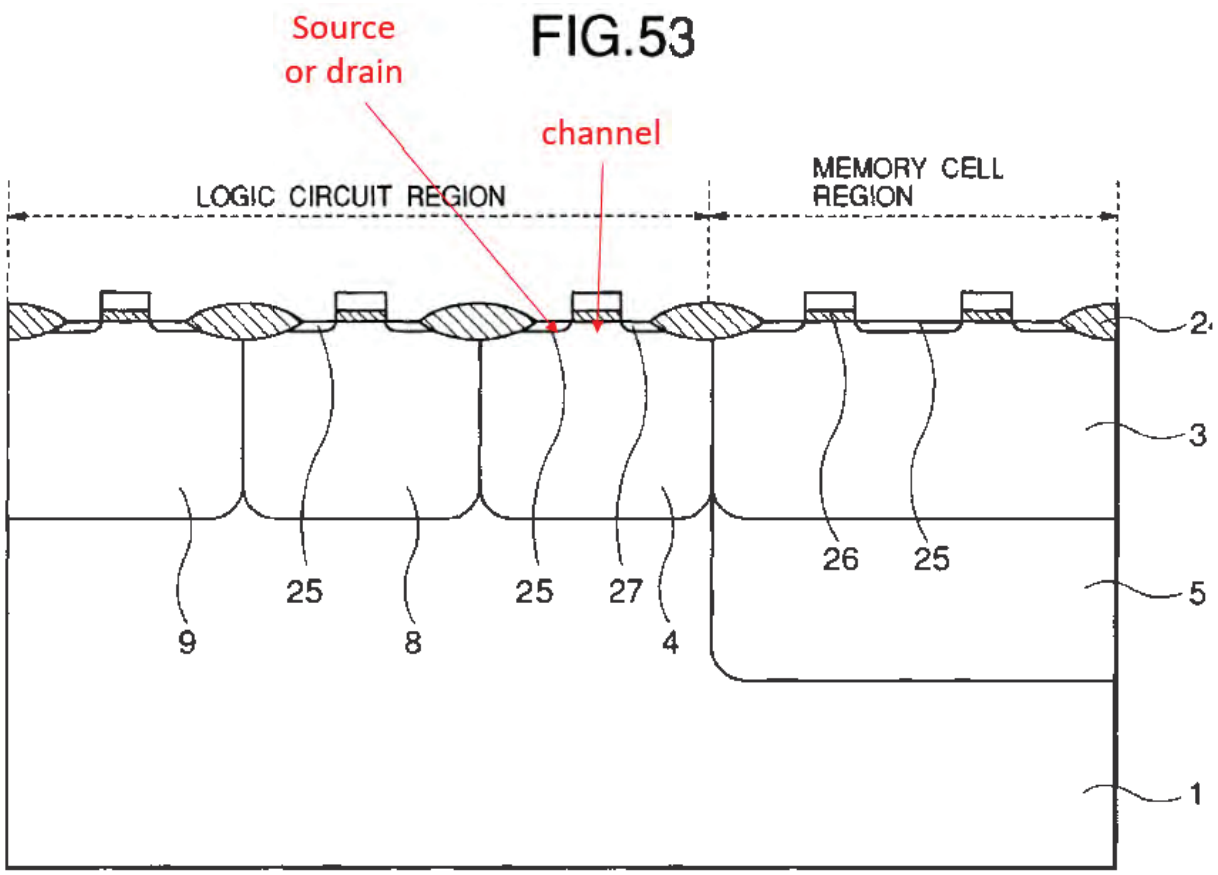
FIG.63



(Ex. 1005, FIG. 63)(Ex. 1002, ¶143).

The first active region is a region **within which transistors can be formed.**

Fig. 53, reproduced below with added labels and arrows, depicts the source, drain and channel of a transistor, which meets the claim language under the Patent Owner's interpretation (Ex. 1014, p. 33):



(Ex. 1005, Fig. 53, 6:1-2, 21:55-58)(Ex. 1002, ¶144). Furthermore, Yamashita teaches that additional transistors can be formed in this same region:

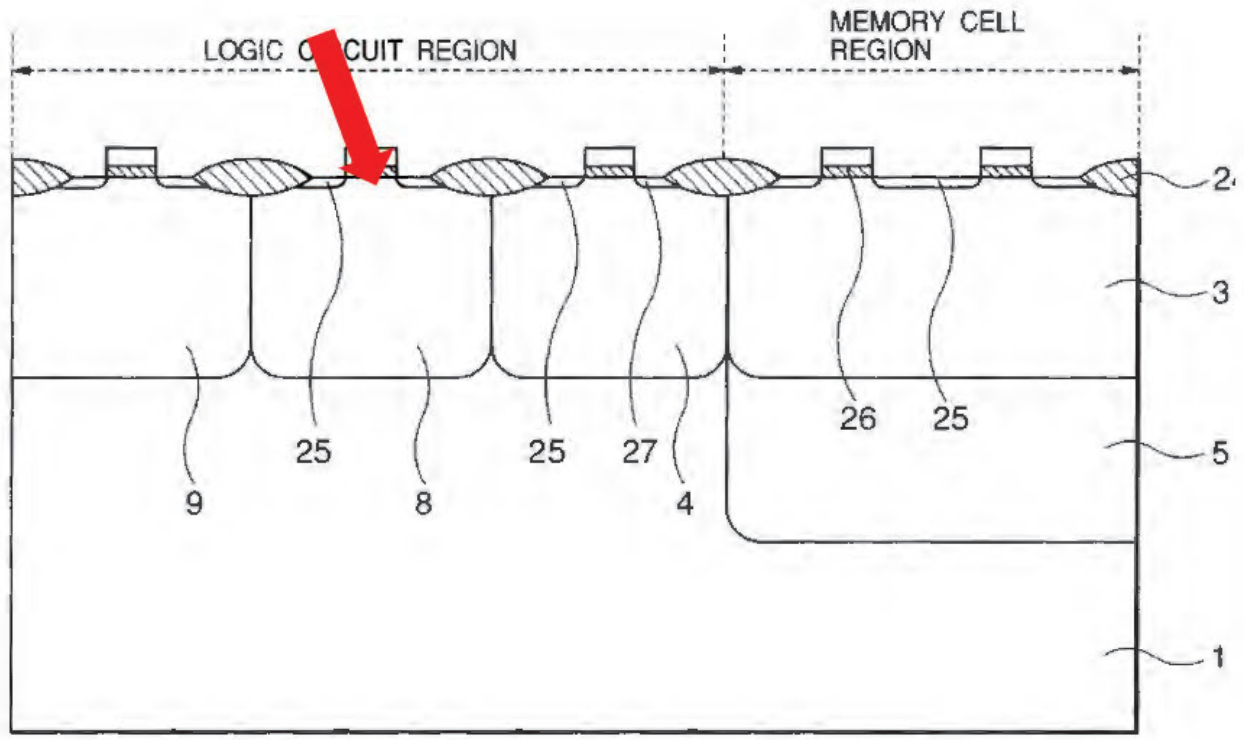
> "**A plurality of transistors** or a single transistor **is formed on the** retrograde p well 8, **the retrograde n well 4** and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region."

(Ex. 1005, 21:55-58)(Emphasis added)(Ex. 1002, ¶144).

> ***"[1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"***

Yamashita teaches **a second active region separate from the first active region disposed adjacent to the first active region** within which transistors can be formed**.** (Ex. 1002, ¶145). The second active region is shown in Fig. 53, reproduced below, with an added red arrow showing the **second active region**:

FIG.53



(Ex. 1005, Fig. 53)(Ex. 1002, ¶145). The second active region has a retrograde p well 8. (Ex. 1005, 21:20-23, 21:55-58, 22:64-33:3, 23:13-14)(Ex. 1002, ¶145). Petitioner notes that in the semiconductor arts, a substrate typically contains active

regions, which can in turn contain or be contained in wells. (Ex. 1002, ¶145).

The second active region is **separate from the first active region** by a "separation region", which is comprised of an isolating field oxide layer 24, as explained above under element [1c]. (Ex. 1005, 22:33-37)(Ex. 1002, ¶146). Petitioner notes that the '842 patent also separates active regions by isolation regions. (*e.g.*, Ex. 1001, claims 7, 15)(Ex. 1002, ¶146).

The second active region is also **adjacent to the first active region**, as shown in Fig. 53, above. (Ex. 1002, ¶147). This adjacent nature of the active regions was also obvious from the disclosure of CMOS logic, as Mr. Guidash explains. (Ex. 1002, ¶147).

Finally, Fig. 53 depicts a transistor formed in the second active region, and Yamashita teaches that additional **transistors can be formed in the second active region**:

> "**A plurality of transistors** or a single transistor **is formed on the retrograde p well 8**, **the retrograde n well 4** and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region."

(Ex. 1005, 21:55-58)(Emphasis added)(Ex. 1002, ¶148).

"[1e] transistors formed in at least one of the first active region or second active region; and"

As explained above under elements [1c] and [1d], Yamashita teaches that

transistors are formed in both the first and second active regions. (Ex. 1005, 21:55-58)(Ex. 1002, ¶149).

"[1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

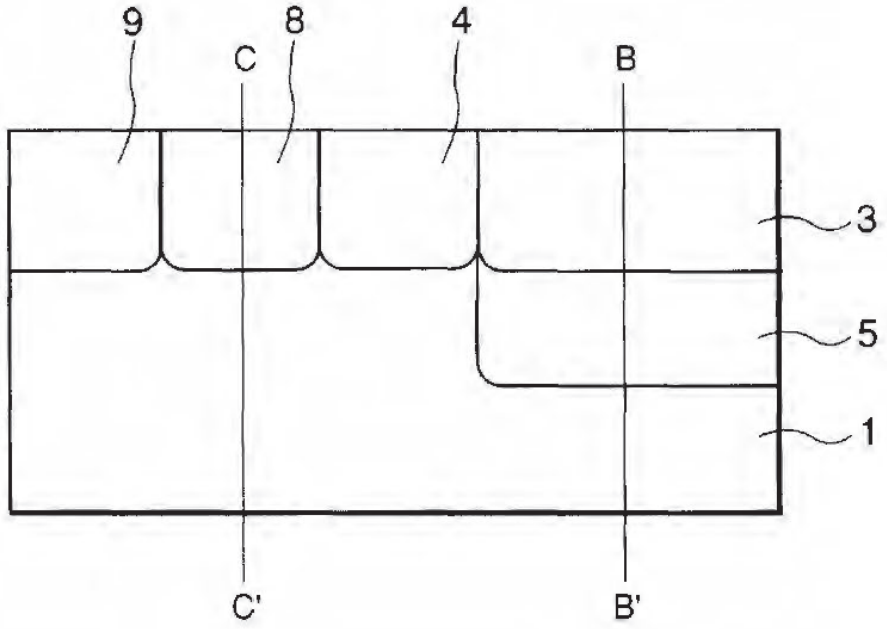
Yamashita teaches that both **the first and second active regions** have **at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.** Specifically, the first active region contains a retrograde n well 4, and the second active region contains a retrograde p well 8. (Ex. 1005, 21:19-25, 22:7-9)(Ex. 1002, ¶150). As Mr. Guidash explains, a "retrograde well" is an area of a semiconductor device that has a dopant concentration peak below the surface of the device, and thus a graded dopant profile that creates the claimed carrier movement. (Ex. 1002, ¶150)(Ex. 1018, ¶0045). The '842 patent admits that:

> "As desired, the n-well and p-wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well."

(Ex. 1001, 4:3-5).

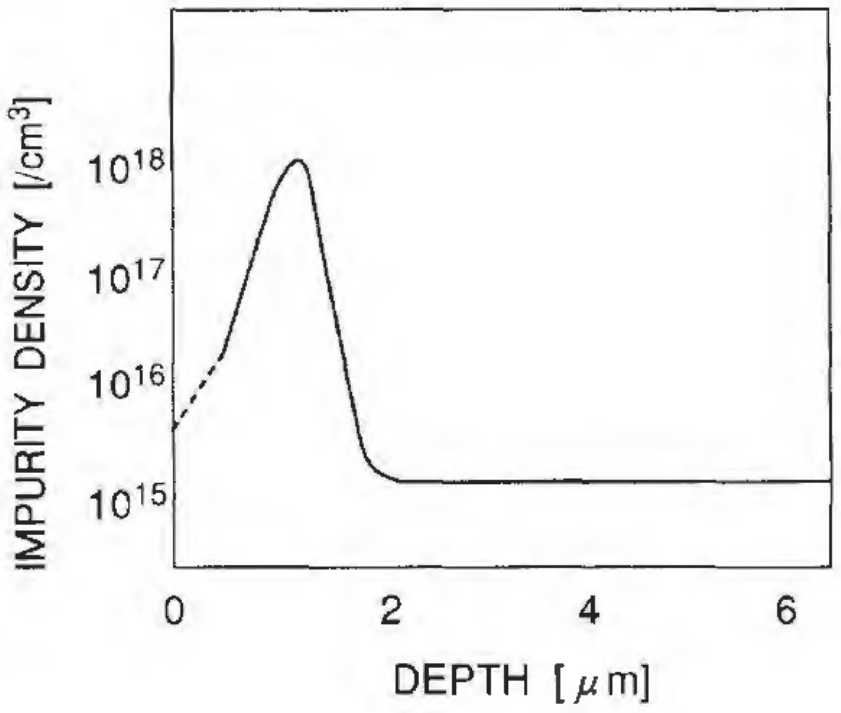
With respect to the **second active region** (which has a retrograde p well 8), Yamashita discloses a cross-section in Fig. 54. The cross-section in Fig. 54 is reproduced here:

FIG.54



(Ex. 1005, Fig. 54, 6:3-4, 21:19-26)(Ex. 1002, ¶151). In Fig. 54, Yamashita shows, running through the second active region, a vertical axis C-C' toward the left-hand side. Along that axis, there is the dopant ("impurity") concentration profile shown in Fig. 55, reproduced here:

FIG.55



(Ex. 1005, Fig. 55, 6:5-6, 21:35-36)(Ex. 1002, ¶151). The horizontal axis of Fig. 55 represents the depth from the top surface of the device, where the top surface is at depth zero on the left-hand side. (Ex. 1002, ¶150). The vertical axis represents the dopant concentration (called the "impurity density" here). (Ex. 1002, ¶151). As is visible from the figure, the **dopant concentration is graded**, because it increases from the surface, reaches a peak, and because it then decreases from the peak to a flatter portion at around a depth of two microns. (Ex. 1002, ¶151).

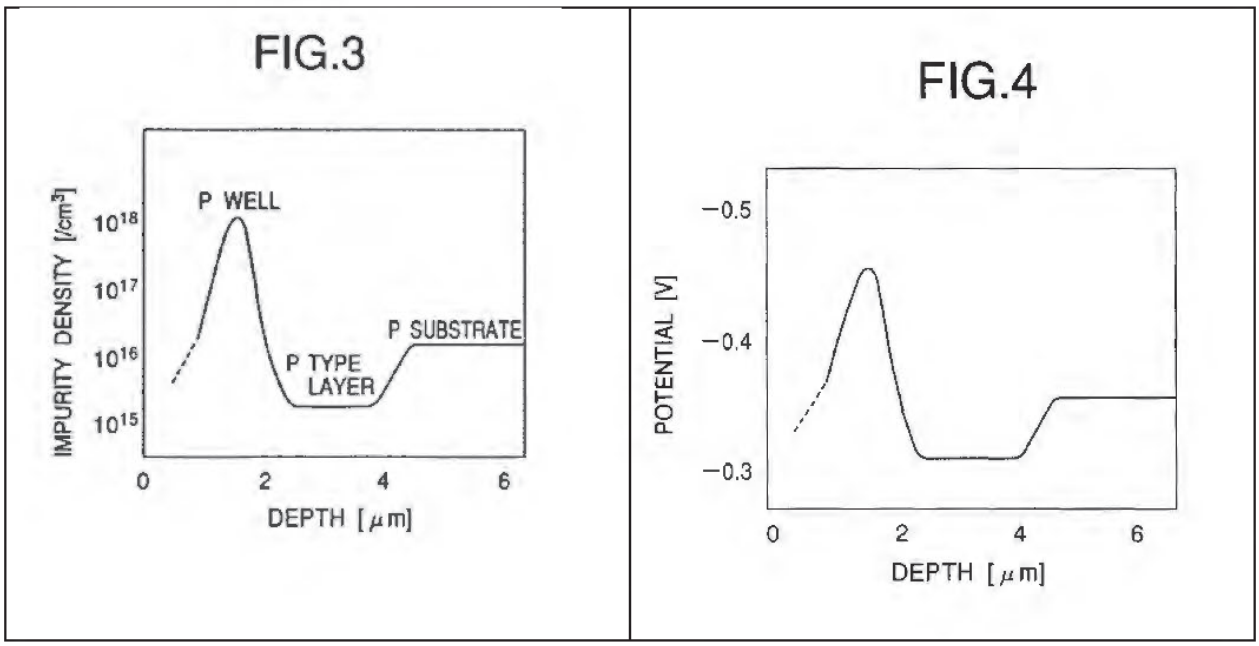
With respect to the **first active region**, although Yamashita does not provide

a graph similar to the one shown in Fig. 55, Yamashita does disclose that the well 4 is a "retrograde n well". (Ex. 1005, 21:19-23, 21:55-22:1, 22:7-9, 23:4-17)(Ex. 1002, ¶152). This indicates that the n well 4 has a dopant concentration profile with a peak below the surface, similar to the one shown in Fig. 55. (Ex. 1002, ¶152). Furthermore, the ion implantation step describe by Yamashita (Ex. 1005, 23:4-12, Fig. 63) would have produced a phosphorus (dopant) profile in the retrograde n well 4 similar to the dopant profile shown in Fig. 55 for boron. (Ex. 1002, ¶152). Thus, it would have been obvious based on the description of well 4 as a "retrograde n well", the corresponding description of the dopant profile of the similarly-labeled retrograde p well 8, and the conditions under which the retrograde n well was created, that the first active region also had a dopant profile with a peak below the surface of the device, and thus a **graded dopant concentration**. (Ex. 1002, ¶152).

Under the Patent Owner's claim construction (as explained above under Ground 1, element [1f]) the graded dopant profiles would obviously have the effect of **aiding carrier movement from the first surface to the second surface of the substrate**, because graded dopant profiles of Yamashita move carriers downward in the device. As explained by Mr. Guidash, a dopant concentration that is graded from the top to the bottom of the device will produce an electric field that carriers with one type of charge toward the bottom of the device, and carriers with the opposite charge toward the top of the device. (Ex. 1002, ¶153). The carriers that move toward

the bottom of the device (**to the second surface of the substrate**) are carriers that are **aided from the first surface to the second surface of the substrate.** (Ex. 1002, ¶153).

The obvious effect of Yamashita's graded dopant profiles is exemplified by Figs. 3 and 4 of Yamashita, shown side-by-side below. (Ex. 1002, ¶154). Fig. 3 shows a dopant profile concentration that has a peak between 1 and 2 microns' depth, similar to the peak shown in the dopant concentration profile of Fig. 55. (Ex. 1002, ¶154). That peak produces an electric potential function (the derivative of which is an electric field) as shown in Fig. 4 (right side):



(Ex. 1005, Figs. 3 and 4, 3:61-64, 7:32-8:5)(Ex. 1002, ¶154). Because of the electric field produced by the retrograde P well, negative carriers (electrons) will move down the slope to the right of the large negative potential peak, while positive carriers

(holes) will move up the slope to the left of the positive potential peak, and thus both types of carriers are aided in their movement from the first surface to the second surface of the substrate. (Ex. 1005, 7:32-8:5)(Ex. 1002, ¶154). It would have been obvious to implement, in the Eighth embodiment of Yamashita, a potential gradient similar to the one in Fig. 4 from the surface to about 2.5 microns in depth using a graded dopant concentration. (Ex. 1002, ¶154). This was obvious because of the similarity of the dopant concentration profiles between 0 and 2.5 microns depth in Figs. 3 and 55, and because the potential gradient of Fig. 4 would fulfill the function of the Eighth Embodiment of Yamashita, namely that "soft error based on electrons can be controlled" by aiding minority carriers toward the bottom of the device. (Ex. 1005, 23:17-26, 7:56-63)(Ex. 1002, ¶154).

Furthermore, during prosecution of related U.S. Patent No. 8,421,195, the Applicant stated that "a graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carrier into a particular direction, whereby the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concertation of dopant." (Ex. 1006, pp. 100-101)(*citing* Ex. 1008, 5:11-13). Accordingly, under Applicant's interpretation, the retrograde wells of Yamashita are sufficient to meet the claim language.

CLAIM 2

"2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate."

Yamashita teaches **the substrate is a p-type substrate**. (Ex. 1005, 22:10-14, 22:33-35)(Ex. 1002, ¶155).

CLAIM 3

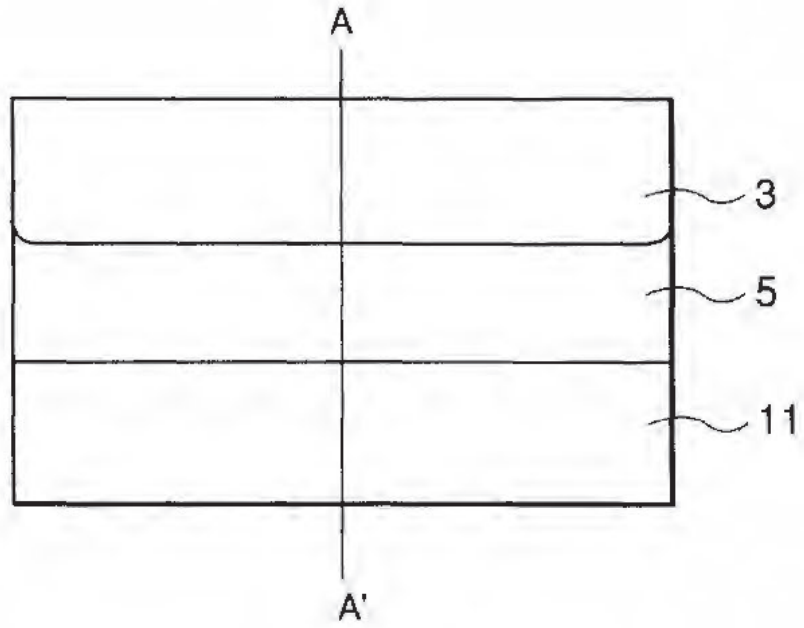
"3. The semiconductor device of claim 1, wherein the substrate is an n-type substrate."

The combination renders claim 3 obvious. Yamashita discloses, in the context of its Seventh Embodiment, an "n type semiconductor substrate 11". (Ex. 1005, Fig. 48, Fig. 51, 19:57-20:9, 20:31-39)(Ex. 1002, ¶156). The n-type semiconductor 11 then has a p-type impurity layer 2 and a retrograde p well 3. Yamashita states:

> "A substrate of the semiconductor device, as shown in FIG. 48, comprises the n type semiconductor substrate 11 containing phosphorus of concentration on the order of $1x10^{16}$ /cm^3, the n type impurity layer 5 containing phosphorus of concentration on the order of $1x10^{15}$ /cm^3 and the retrograde p well 3 containing boron of concentration on the order of $1x10^{18}$ /cm^3."

(Ex. 1005, 20:1-7)(Ex. 1002, ¶156). The layers are shown in Fig. 48, reproduced here:

FIG.48



(Ex. 1005, Fig. 48)(Ex. 1002, ¶156).

It would have been obvious to use an n-type substrate, as suggested by the Seventh Embodiment of Yamashita, in the Eighth Embodiment of Yamashita. (Ex. 1002, ¶157). A POSITA would have recognized that the Eighth Embodiment could have been used with a p-type or an n-type substrate without unpredictable results and with a reasonable expectation of success, as long as the appropriately doped well is implanted for each type of device. (Ex. 1002, ¶157). In the Seventh Embodiment, for example, the retrograde p well 3 is implanted near the surface, which is similar to the retrograde wells implanted for the active regions. (Ex. 1005, 20:1-7, 20:35-39, *compare* Figs. 50 and 54)(Ex. 1002, ¶157). In addition, Yamashita teaches that the structure of the Seventh Embodiment is advantageous, specifically because:

> "As in the sixth embodiment, the semiconductor structure can improve pressure resistance, because the field between the retrograde p well 3 and the n type semiconductor substrate 11 is alleviated. Further, since the n type semiconductor substrate 11 has a high concentration and the retrograde p well 3 has a low impurity concentration surface for forming the transistor, degradation of transistor threshold voltage or the like can be reduced. In case of the n type semiconductor substrate 11 containing phosphorous of concentration of on the order of $1x10^{18}/cm^3$, the semiconductor device can obtain a low substrate resistance and, and in addition improvement in latch up resistance based on the retrograde p well 3 when CMOS transistor is formed on the substrate structure is realized."

(Ex. 1005, 20:31-45)(Ex. 1002, ¶157). A POSITA would thus have expected advantages in using the n-type semiconductor substrate and structure of the Seventh Embodiment together with the Eighth Embodiment of Yamashita. (Ex. 1002, ¶157).

CLAIM 4

"4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

Yamashita teaches that its **substrates** can have **epitaxial silicon**. Specifically, Yamashita teaches that the p-type layer 2, as well as the n-type layer 5, are "formed…by epitaxial growth". (Ex. 1005, 8:11-16, 8:50-54, 11:62-64, 12:27-28. 15:56-61, 16:53-57, 18:39-42, 21:20-24, 26:31-36)(Ex. 1002, ¶158). Silicon

formed by epitaxial growth is **epitaxial silicon**. Furthermore, these layers are "formed on the p type semiconductor substrate 1". (Ex. 1005, 8:11-15, 10:50-54, 11:62-67, 21:20-24, Figs. 60, 53)(Ex. 1002, ¶158).

While Yamashita does not expressly state that the substrate of the Eighth Embodiment is epitaxial silicon is **on top of a nonepitaxial substrate**, this was a common practice in the relevant timeframe, as explained by Mr. Guidash. (Ex. 1002, ¶159)(*citing* Ex. 1012, pp. 051, 058-059). In general, epitaxial silicon layers are higher quality for device manufacturing, but slower to grow. (Ex. 1002, ¶159). Therefore, providing a thicker nonepitaxial substrate for handling and stability, topped by a higher-quality epitaxial substrate, made economic sense in the relevant timeframe. (Ex. 1002, ¶159). Thus, it would have been obvious for Yamashita to provide for a **substrate having epitaxial silicon on top of a nonepitaxial substrate**. (Ex. 1002, ¶159).

CLAIM 5

"5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices."

See above, claim 1, limitations [1c]-[1e] (discussing the formation of transistors in the first and second active regions, as well as their dopant types), limitation [1h] (discussing the transistors forming digital logic). The transistors in the first and second active region comprise both **p-channel and n-channel** devices.

Specifically, transistors in the first active region comprise p-channel devices, because their channels are formed between p-type sources and drains in the n well 4, while the transistors in the second active region comprise n-channel devices, because their channels are formed between n-type sources and drains in the p well 8. (Ex. 1005, 21:42-65)(Ex. 1002, ¶160).

CLAIM 6

"6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant."

See above, claim 5 (discussing p-channel and n-channel devices), claim 1, elements [1c] and [1d] (discussing the n-wells (*e.g.*, n well 4) and p-wells (*e.g.*, p well 8) respectively), and claim limitation [1f] (discussing the graded dopant regions in the retrograde n well 4 and the retrograde p well 8). (Ex. 1002, ¶161).

CLAIM 7

"7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

Yamashita teaches that the **first active region and second active region are each separated by at least one isolation region**, specifically field oxide region 24. (Ex. 1002, ¶162). As discussed above under claim 1, element [1c], the active regions

under gate oxide 29 in Fig. 57 are separated by "separation regions" in the form of field oxide 24. (Ex. 1005, 22:32-39)(Ex. 1002, ¶162). These separation regions are visible between active regions, including after transistor construction, in Figs. 53 and 57-63. (Ex. 1002, ¶162). Field oxide regions are isolation regions. (Ex. 1002, ¶162).

CLAIM 8

"8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process."

Yamashita teaches that the **graded dopant is fabricated with an ion implantation process** in each of retrograde p wells 3 and 8, as well as retrograde n well 4. (Ex. 1005, 22:57-23:17)(Ex. 1002, ¶163).

CLAIM 9

"9[a]. A semiconductor device, comprising:"

See above, claim 1, element 1[a]. (Ex. 1002, ¶164).

"[9b] a substrate of a first doping type at a first doping level having first and second surfaces;"

See above, claim 1, element [1b]. (Ex. 1002, ¶165).

"[9c] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

See above, claim 1, element [1c]. (Ex. 1002, ¶166). The present claim element [9c] adds that transistors can be formed "in the surface thereof". As discussed above under claim 1, element [1c], and as shown in Fig. 53 of Yamashita, the transistors are **formed in the surface** of the substrate and active region. (Ex. 1005, Fig. 53, 21:55-58)(Ex. 1002, ¶166).

"[9d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

See above, claim 1, element [1d]. (Ex. 1002, ¶167). The present claim element [9d] adds that transistors can be formed "in the surface thereof". As discussed above under claim 1, element [1d], and as shown in Fig. 53 of Yamashita, the transistors are **formed in the surface** of the substrate and active region. (Ex. 1005, 21:55-58)(Ex. 1002, ¶167).

"[9e] transistors formed in at least one of the first active region or second active region; and"

See above, claim 1, element [1e]. (Ex. 1002, ¶168).

"[9f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate."

See above, claim 1, element [1f]. (Ex. 1002, ¶169). The present claim element [9f] states that the dopant concentration is "to aid carrier movement from the surface

to the substrate", as opposed to being "to aid carrier movement from the first surface to the second surface of the substrate", as in claim 1. This difference in claim language, however, does not make a material difference to the claim interpretation. (Ex. 1002, ¶169).

CLAIM 10

"10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate."

See above, claim 2. (Ex. 1002, ¶170).

CLAIM 11

"11. The semiconductor device of claim 9, wherein the substrate is an n-type substrate."

See above, claim 3. (Ex. 1002, ¶171).

CLAIM 12

"12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

See above, claim 4. (Ex. 1002, ¶172).

CLAIM 13

'13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices."

See above, claim 5. (Ex. 1002, ¶173).

CLAIM 14

"14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant."

See above, claim 6. (Ex. 1002, ¶174).

CLAIM 15

"15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region."

See above, claim 7. (Ex. 1002, ¶175).

CLAIM 16

"16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process."

See above, claim 8. (Ex. 1002, ¶176).

CLAIM 17

"17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

Yamashita teaches this claim. (Ex. 1002, ¶177). *See* above, claim 1, element [1c], which already requires that the *first* active region be "disposed adjacent to the surface". (Ex. 1002, ¶177). The *second* active region, in turn, is disposed horizontally adjacent to the first active region (*see* above, claim 1, element [1d]), and is also **adjacent the first** (top) **surface of the substrate**. *See* above, claim 1,

element [1d]. (Ex. 1002, ¶177). To the extent that the word "formed" (as opposed to the word "disposed" in claim 1) requires a physical process, the first and second active regions are also "formed" where they are ultimately "disposed". (Ex. 1005, 21:55-22:6, Fig. 53)(Ex. 1002, ¶177).

CLAIM 18

> ***"18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region."***

Yamashita teaches that **the transistors which can be formed in the first and second active regions are CMOS digital logic transistors.** The first and second active regions, and their transistors, are discussed above under claim 1, elements [1c]-[1e]. Yamashita states that the transistors can form CMOS digital logic. Yamashita states:

> "**A plurality of transistors** or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a **CMOS** is formed on the logic circuit region."

(Ex. 1005, 21:55-58)(Emphasis added)(Ex. 1002, ¶178). As Mr. Guidash explains, a POSITA would have understood from this description that pMOS transistors are formed in the n well 4, and nMOS transistors are formed in the p well 8, and that these transistors together form CMOS digital logic, and are thus **CMOS digital logic transistors**. (Ex. 1002, ¶178). The MOSFET transistors in Yamashita have sources,

drains, channels and gates. (Ex. 1005, 21:55-65, 22:10-18, 22:32-39)(Ex. 1002, ¶178).

Ground 3. Claims 1-18 are obvious over Yamashita and Nishi.

Claims 1-18 were obvious over Yamashita (Ground 2) in view of Nishi, *et al.* (eds.) *Handbook of Semiconductor Manufacturing Technology*, Marcel Dekker, Inc., New York (2000)(Ex. 1012).

A. Effective Prior Art Dates

Yamashita is prior art as discussed under Ground 2.

Nishi is a textbook published in the year 2000. (Ex. 1002, ¶180)(*citing* Exs. 1024-1027). It thus qualifies as prior art under pre-AIA 35 U.S.C. §102(b).

B. Overview of the Ground

This ground posits that it would have been obvious to provide for additional graded dopant profile portions to the retrograde wells 4 and 8 of Yamashita, as taught by Nishi. The ground is directed to the possibility that the Patent Owner might argue both that the term "active region" has a particular depth at which it stops, and that Yamashita does not teach a graded dopant profile within that depth.

The combination with Nishi begins with the observation that Nishi teaches a "modulated retrograde well" dopant profile—applicable to CMOS transistors—in its Fig. 11 and surrounding text. (Ex. 1012, p. 086)(Ex. 1002, ¶182). Figure 11 of

Nishi is reproduced below, and shows a dopant concentration profile with depth, where the surface of the substrate is on the left side of the figure:

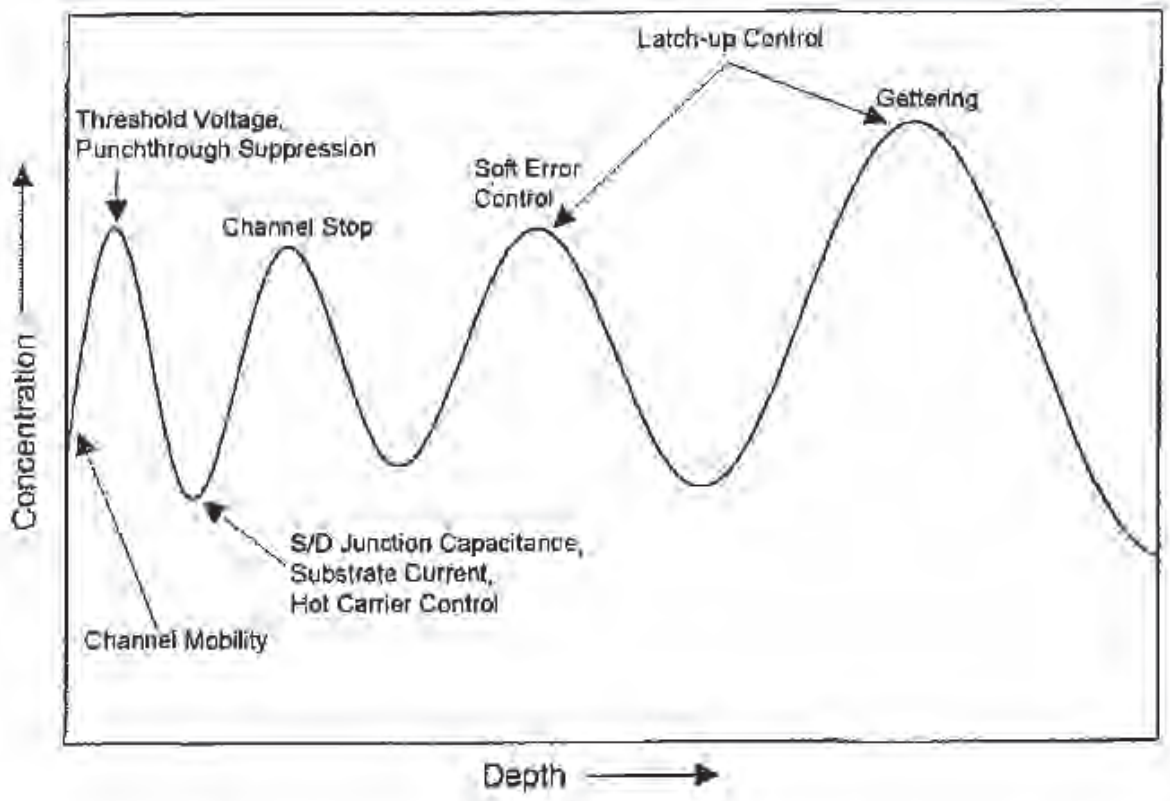
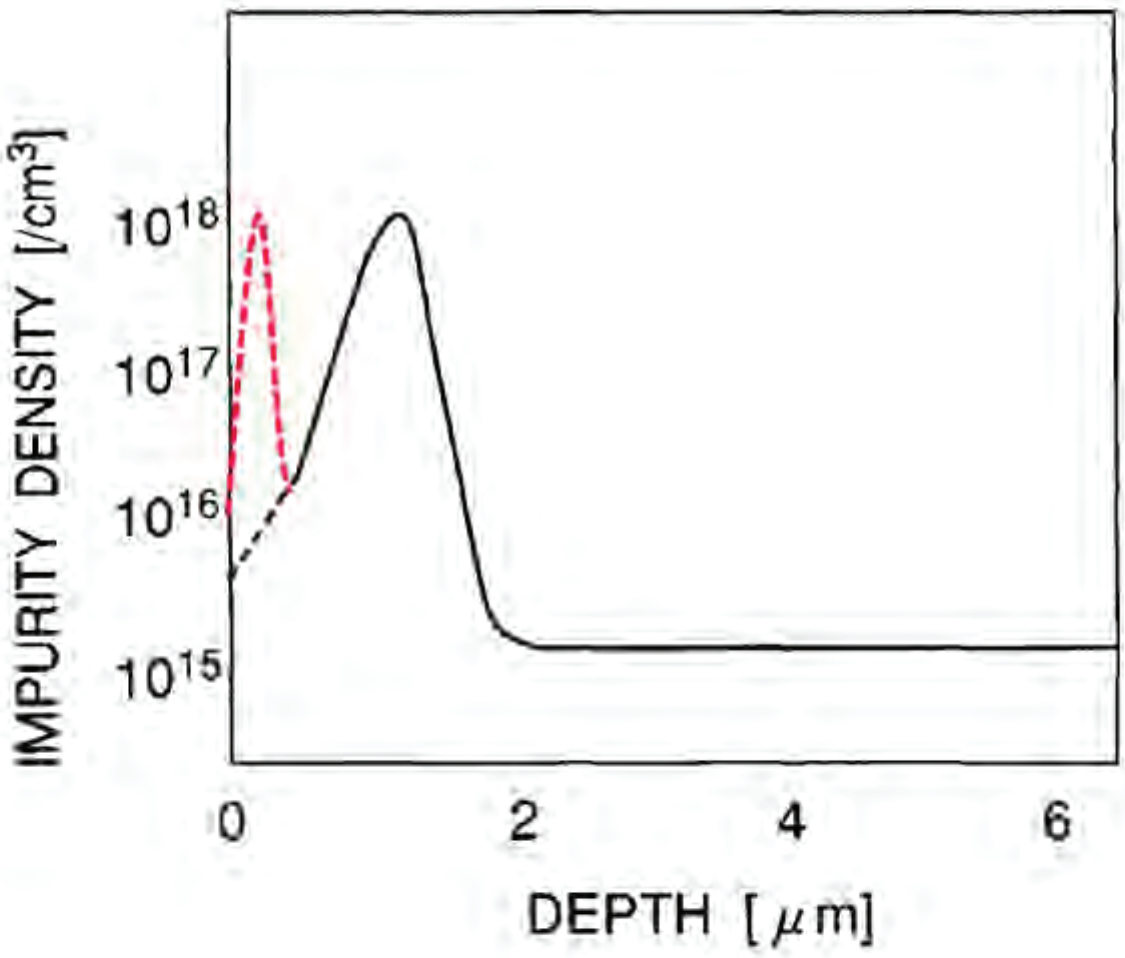


Figure 11 Doping profile of a modulated retrograde well structure, showing the device parameters affected by the doping level at each depth. Adapted from references [40,41].

(Ex. 1012, Fig. 11, p. 086)(Ex. 1002, ¶182).

This ground posits that it would have been obvious to provide for at least the left-most peak in the Nishi Fig. 11 profile (labeled with "Threshold voltage, Punchthrough Suppression" at the peak and "Channel Mobility" at the left shoulder") in Yamashita's retrograde wells 4 and 8. (Ex. 1012, p. 086)(Ex. 1002,

¶183). This would have provided for a graded dopant profile that is very close to the surface of the device in Yamashita, and within the transistor channel. (Ex. 1002, ¶183). A modified version of Fig. 55 of Yamashita, showing the additional peak from Nishi, is provided below, with an added, red-dashed line indicating the peak from Nishi provided for punch-through suppression and threshold voltage, with adjacent valleys for channel mobility and hot carrier control:



(Ex. 1005, Fig. 55)(Ex. 1002, ¶183). A similar modification would be made to the dopant profiles in both wells 4 and 8, using n-type and p-type dopants, respectively.

(Ex. 1002, ¶184).

C. Rationale (Motivation) Supporting Obviousness

The modification would have been obvious. (Ex. 1002, ¶185). Yamashita already suggests such a modification, stating:

> "A plurality of transistors or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region. **In this case, in the retrograde wells, the channel implantation layer for punch-through prevention and threshold control is formed at the depth of 0-0.2 μm from the substrate as needed**."

(Ex. 1005, 21:55-61)(Emphasis added)(Ex. 1002, ¶185). This expressly suggests forming an implantation in the transistor channel region, which would result in a peak of dopant concentration at a depth between 0 and 0.2 μm. (Ex. 1002, ¶185). Furthermore, the purpose of this implantation is for "punch-through prevention and threshold control", which are exactly the purposes shown in Fig. 11 of Nishi for the left-most (shallowest) dopant concentration peak. (Ex. 1002, ¶185). This implantation would make sense in Yamashita's device, as Mr. Guidash explains. (Ex. 1002, ¶185).

Furthermore, Yamashita teaches that the transistors in the Logic Circuit Region (*see* Fig. 53) are MOSFET transistors in a CMOS process. (Ex. 1005, 21:33-34)(Ex. 1002, ¶186). Nishi teaches that the modulated retrograde well is particularly

effective for such transistors, and had, by 2000, replaced other standard well processes. (Ex. 1012, p. 086)(Ex. 1002, ¶186). Nishi explains:

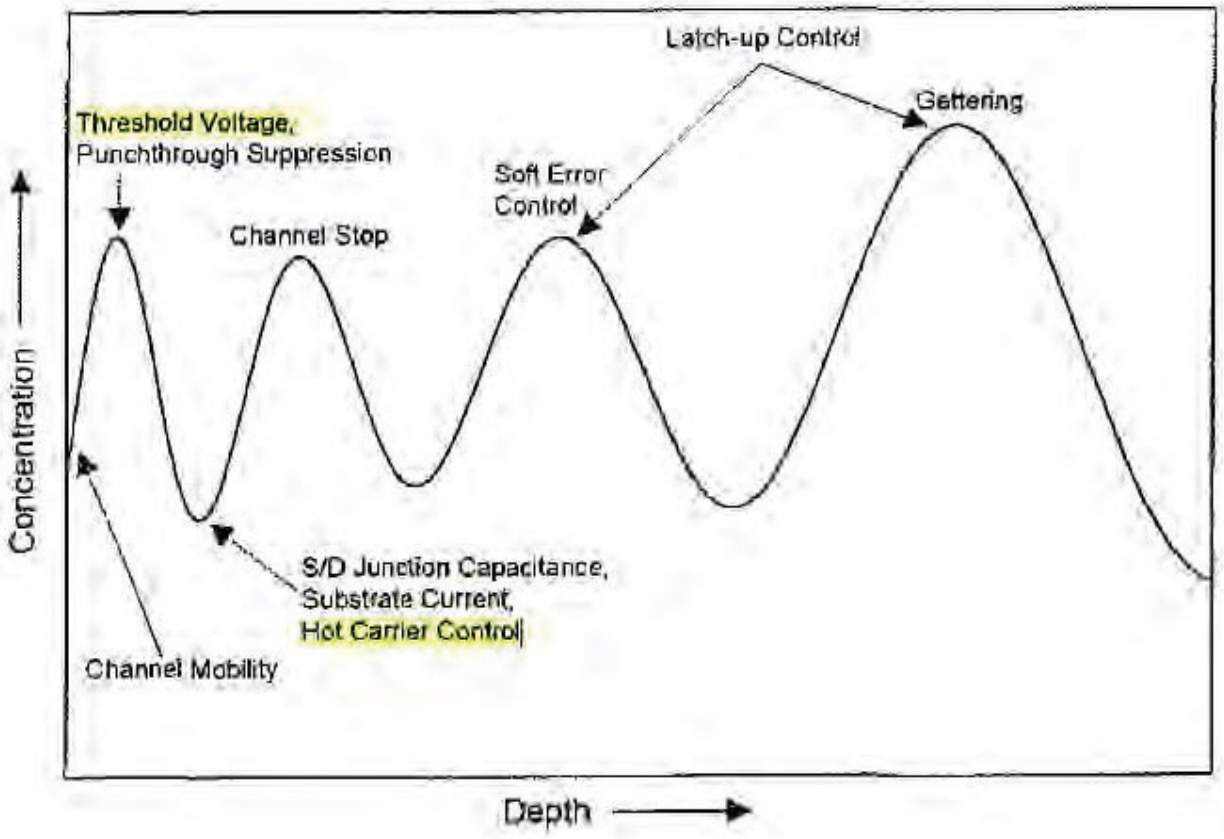
> "Ion implantation is essential for fabricating the twin tub (both p-well and n-well implants) CMOS process. **The modulated well structure (Fig. 11) has replaced the older diffused well process**, **due to its higher processing flexibility and lower cost**. Since the well forms the MOSFET's 'back gate', the well doping will fundamentally affect the transistor's electrical performance. **Engineering the well with multiple implants and minimal thermal diffusion** allows independent control of dopant levels throughout the depth of the well, and thus **independent optimization of key MOSFET performance characteristics** (Fig. 11). Device speed (carrier mobility, S/D capacitance), inter-device leakage currents, **V_T control**, **punchthrough suppression**, parasitic transistor effects, and soft error and latch-up resistance can be optimized almost independently by carefully positioned dopant peaks and valleys [41,42]. **Low surface doping levels increase mobility and decrease capacitance.** Heavier doping below the surface (retrograde doping) reduces minority carrier collection by reducing depletion widths, thus reducing soft errors and latch-up susceptibility [43-46]. This degree of design flexibility is not possible with diffused wells."

(Ex. 1012, p. 086)(Emphasis added)(Ex. 1002, ¶186). Nishi thus teaches to engineer wells "with multiple implants and minimal thermal diffusion", which results in multiple peaks in the dopant profile concentration, as shown in Fig. 11. (Ex. 1012,

p. 086)(Ex. 1002, ¶186). Among other things, this allows better control of the threshold voltage of the transistor ("V_T" in the quote above), allows for punch-through suppression, and allows for hot carrier control, as shown in Nishi Fig. 11 and (as to V_T and punch-through suppression) taught expressly by Yamashita. (Ex. 1005, 21:55-61)(Ex. 1012, pp. 085-086)(Ex. 1002, ¶186). Nishi further teaches that having a lower dopant concentration at shallower depths in the transistor channel "increase[s] mobility and decrease[s] capacitance", while "[h]eavier doping below the surface (retrograde doping) reduces minority carrier collection…." (Ex. 1012, p. 086)(Ex. 1002, ¶186). To the extent desired, a POSITA could have used all four peaks shown in Nishi Fig. 11 in an obvious manner. (Ex. 1002, ¶186). These advantages (the ability to better control the transistor threshold voltage, punch-trough suppression, hot carrier control and increased transistor channel mobility, decreased minority carrier collection and decreased capacitance) would have been seen as valuable by a POSITA in the relevant timeframe, and would have rendered the combination obvious. (Ex. 1002, ¶186).

Furthermore, it would have been obvious to arrange the doping peak of Nishi in Yamashita specifically to **aid the movement of carriers from the first surface to the second surface of the substrate** (applying the Patent Owner's construction, as explained above under Ground 1, element [1f]). (Ex. 1002, ¶187). This would have been obvious to a POSITA in order to achieve the threshold voltage control

and hot carrier control, as shown in Fig. 11 of Nishi, reproduced again here with highlighting added:



(Ex. 1012, Fig. 11, p. 086)(Ex. 1002, ¶187). As Mr. Guidash explains, threshold voltage control can be provided by the gradient in the doping profile. (Ex. 1002, ¶186). This allows the designer a way to influence threshold voltage that is less coupled to punchthrough voltage. (Ex. 1012, p. 086)(Ex. 1002, ¶187). Such independent control over design parameters is an express goal of Nishi's modulated well. (Ex. 1012, p. 086)(Ex. 1002, ¶187). Furthermore, hot carriers (which can damage the transistor) are controlled by the right-hand slope of the first peak in Fig. 11, because they are aided away from the surface toward the substrate, where they

cannot damage the transistor. (Ex. 1002, ¶187). Thus it would have been obvious to arrange the graded dopant profile in order **to aid carrier movement from the first surface to the second surface of the substrate**. (Ex. 1002, ¶187).

Finally, the technique suggested by Nishi was, in the relevant timeframe, a well-known (indeed, textbook) technique for improving exactly the type of transistors taught by Yamashita, and could have been used in Yamashita with no unpredictable results, and was thus obvious under *KSR*, 550 U.S. 398, 416-21 (2007). (Ex. 1002, ¶188).

D. *Graham* Factors

The *Graham* factors are the same as discussed under Grounds 1 and 2, with the exception that the relationship of the prior art to the claims is altered in this Ground.

E. Reasonable Expectation of Success

A POSITA in the relevant timeframe would have had a reasonable expectation of success in implementing the transistor channel peak (and any other of Nishi's peaks in Fig. 11, as desired). As Mr. Guidash explained, the dopant profiles shown in Nishi were accomplished by ion implantation, which was a standard, predictable technique in the relevant timeframe. (Ex. 1002, ¶190).

F. Analogous Art

Nishi is analogous art because it is in the same field as the '842 patent (electronic and semiconductor devices) and as a handbook on manufacturing such

devices, would have been highly relevant to the problems purportedly facing the named inventors. (Ex. 1002, ¶191).

G. Claim Mapping

The claim mapping is the same as described in Ground 2, except that the first and second active regions would have one (or more, if desired) additional **at least one graded dopant concentration to aid carrier movement.** (Ex. 1002, ¶192). These graded regions would be the additional peak as discussed above, present in the channels of transistors formed in both the retrograde p-well 8 and retrograde n-well 4. (Ex. 1002, ¶192). This peak is a **graded dopant profile** in each active region, which would have obviously and necessarily been **to aid carrier movement from the first surface to the second surface of the substrate** (claim limitations [1f] and [21f]), as explained above in the section entitled Rationale (Motivation) Supporting Obviousness. (Ex. 1002, ¶192). The mapping for other elements of the independent or dependent claims does not change. (Ex. 1002, ¶192).

IV. DISCRETIONARY INSTITUTION

A. The Board should not deny the petition under 35 U.S.C. §325(d)

The Board should not exercise its discretion to deny the petition. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte G.m.b.H.*, IPR2019-01469, Paper 6, *8-9 (PTAB Feb. 13, 2020) (precedential).

The principal prior art references, Miyagawa, Yamashita, and Nishi, were not

before the Office during the Examination the application leading to the '842 patent. (Ex. 1007).

Furthermore, the breadth of the claims in light of the prior art, combined with the strength of the prior art and the additional evidence presented in the petition would "warrant reconsideration of the prior art or arguments". *Becton, Dickinson,* at 17-18.

B. The Board should not deny the petition under 35 U.S.C. §314(a)

Nor should the Board deny the petition under 35 U.S.C. §314(a) in view of the co-pending litigation between Greenthread, Dell and Intel (hereinafter the "West-Texas Litigation"). *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential)("*Fintiv*").

The *Fintiv* factors weigh in favor of institution, as follows:

***Fintiv* Factor 1** ("*whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*"). None of the parties in the West-Texas Litigation have moved for a stay pending *inter partes* review, and it is unclear whether any party would. This factor is thus neutral.

***Fintiv* Factor 2** ("*proximity of the court's trial date to the Board's projected statutory deadline for a final written decision*"): The trial date in the West-Texas Litigation is only tentatively set for 12/11/23, but the Court expects to revisit that date at the conclusion of the claim construction hearing. (Ex. 1019, p. 3)("[t]he

Court expects to set this date [December 11, 2023] at the conclusion of the Markman Hearing"). At least three other *patent* cases have also been assigned the same trial date in the same courtroom before the same judge (Exs. 1021-1023), meaning that the provisional date is unlikely to hold. The district has a median 28.3 months to jury trial in civil cases, which would result in a jury trial in approximately June 2024, approximately concurrent with the Board's likely Final Written Decision in this matter. (Ex. 1020, p. 037). *See Interim Procedure for Discretionary Denials in AIA Postgrant Proceedings with Parallel District Court Litigation*, USPTO, June 21, 2022, p. 8.[2]

This factor thus weighs in favor of institution.

***Fintiv* Factor 3** ("*investment in the parallel proceeding by the court and the parties*"): In the parallel proceeding, discovery began only recently (Ex. 1009, p. 2), the parties have begun, but not completed, Markman proceedings, and the parties have not yet filed motions for summary judgment. (Ex. 1019). This factor thus favors institution.

***Fintiv* Factor 4** ("*overlap between issues raised in the petition and in the parallel proceeding*"): Defendants in the West-Texas litigation have asserted a wide

[2] https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

variety of prior art in preliminary invalidity contentions, including Yamashita, Nishi, and Kenney. However, it is likely that these references would need to be narrowed before trial, and it is thus too early to determine the extent of overlap of any trial. This factor is thus neutral.

***Fintiv* Factor 5** ("*whether the petitioner and the defendant in the parallel proceeding are the same party*"):

While the Dell RPIs are parties to the litigation, the Sony RPIs are not. Moreover, Greenthread made no allegations against Sony Products until April 29, 2022, several months after filing its action. (Ex. 1015)(Ex. 1016, ¶¶18, 60, 76-81, 102, 110, 118, 126). The Sony RPIs sell accused products to entities other than entities accused in the West-Texas Litigation (*e.g.*, Ex. 1028), and thus have an independent interest in the proceeding. This factor thus weighs in favor of institution.

***Fintiv* Factor 6** ("*other circumstances that impact the Board's exercise of discretion, including the merits*."): The merits of the petition are compelling, and the Board should institute on this basis alone. *See Interim Procedure for Discretionary Denials,* p. 8.

V. CONCLUSION

Petitioner thus respectfully requests that claims 1-18 of the '842 patent be canceled.

Date: December 17, 2022	/Matthew A. Smith/ (RN 49,003) Matthew A. Smith SMITH BALUCH LLP 700 Pennsylvania Ave. SE, 2nd Floor Washington, DC 20003 (202) 669-6207 smith@smithbaluch.com *Counsel for Petitioner*

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing petition for *inter partes* review, together with all exhibits and other documents filed therewith, was served by Express Mail on December 17, 2022, on the Patent Owner's counsel of record at the United States Patent & Trademark Office having the following address:

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UNITED STATES

Date: December 17, 2022 /Matthew A. Smith/ (RN 49,003)

CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the foregoing petition for *inter partes* review contains 12,154 words according to the word processing program used to prepare it.

Date: December 17, 2022 /Matthew A. Smith/ (RN 49,003)