

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

GREENTHREAD, LLC

Plaintiff,

vs.

MONOLITHIC POWER SYSTEMS, INC.

Defendant.

Civil Action No.

JURY TRIAL DEMANDED

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Greenthread, LLC (“Greenthread” or “Plaintiff”) files this Original Complaint against Monolithic Power Systems, Inc. (“MPS” or “Defendant”) and hereby alleges as follows:

THE NATURE OF THE ACTION

1. Greenthread owns a family of patents related to transistors and other components of integrated semiconductor devices. Greenthread’s patented inventions describe semiconductor devices that employ graded dopants and well regions for creating electric fields for aiding and/or limiting the movement of carriers to (or from) the semiconductor surface to (or from) the semiconductor substrate. These inventions improve semiconductor devices by (1) creating faster, more efficient, and more reliable mixed-signal circuits and sensor devices, power management integrated circuits, junction field effect transistors, processors, logic devices, DRAM and NAND flash, and image sensors and (2) allowing manufacturers to scale down the feature size of their semiconductor products.

2. Defendant has infringed and continues to infringe six Greenthread patents: U.S. Patent Nos. 8,421,195 (“the ’195 Patent”), 9,190,502 (“the ’502 Patent”), 10,510,842 (“the ’842 Patent”), 10,734,481 (“the ’481 Patent”), 11,121,222 (“the ’222 Patent”), and 11,316,014 (“the

'014 Patent”), (collectively “the Greenthread Patents”), copies of which are attached hereto as Exhibits 1-6, respectively. Defendant has infringed and continues to infringe the Greenthread Patents by: making, using, selling, offering for sale, and/or importing into the United States, semiconductor devices with infringing graded dopant regions and/or electronic products containing the same; and inducing others to do the same.

THE PARTIES

3. Greenthread is a limited liability company organized and existing under the laws of Texas, having its principal place of business at 7424 Mason Dells Drive, Dallas, Texas 75230-3244.

4. MPS is a corporation organized and existing under the laws of Delaware with its headquarters at 5808 Lake Washington Blvd., Kirkland, Washington 98033.

5. “MPS Accused Products” are products accused of meeting the claim limitations of a Greenthread Patent in this suit. MPS designs and manufactures semiconductor devices containing transistors and other structures that infringe the Greenthread Patents in the United States. The infringing structures within semiconductor devices have application in many types of devices designed and manufactured by MPS, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOFSET drivers, isolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, current sensors, and other products containing transistors.

6. Exhibit 8, demonstrating how exemplary MPS Accused Products meet the claim

limitations of Greenthread Patents, is incorporated herein by reference.

7. MPS sells MPS Accused Products directly and indirectly.¹

Customers, Sales and Marketing

We sell our products through third-party distributors, value-added resellers and directly to original equipment manufacturers (“OEMs”), original design manufacturers (“ODMs”), electronic manufacturing service (“EMS”) providers and other end customers. Our third-party distributors are subject to distribution agreements with us, which allow the distributors to sell our products to end customers and other resellers, including OEMs, ODMs or EMS providers. Our value-added resellers may second source our products and provide other services to customers. ODMs typically design and manufacture electronic products on behalf of OEMs, and EMS providers typically provide manufacturing services for OEMs and other electronic product suppliers.

8. For example, MPS allows customers to purchase MPS Accused Products directly through its website.²

¹ MPS, Form 10-K (Dec. 31, 2022), https://media.monolithicpower.com/mps/cms/document/2/0/2022_mps_annual_report.pdf?_gl=1*leopt24*_ga*MTU4NTU1NTQ3Ny4xNjgzNjM4MjIx*_ga_XNRPF6L9DD*MTY4NDE4NTgzOS4zLjEuMTY4NDE4NjA4OS4yMi4wLjA.&_ga=2.178535588.183754632.1684185838-1585555477.1683638221

² Product Overview of MPQ4425M-AEC1, <https://www.monolithicpower.com/en/mpq4425m-aec1.html>

MPQ4425M-AEC1 Automotive-Grade High Efficiency 1.5A, 36V, 2.2MHz Synchronous Step-Down LED Driver Active [Datasheet](#)

[Overview](#) [Evaluation Tools](#) [Resources](#) [Design Resources](#) [Technical Forum](#) [Quality](#) [Buy Order](#)

Buy direct from MPS

Quantity	Price
1+	\$4.05 /unit
10+	\$3.49 /unit 13 % Discount
100+	\$4.37 /unit 28 % Discount
250+	\$3.97 /unit 34 % Discount
500+	\$3.16 /unit 40 % Discount

IN STOCK
ARRIVES 3-4 BUSINESS DAYS.
SHIPPING ONLY \$5 PER ORDER.

Quantity: 1

2500 Max per Company
Limited Inventory to support product development

[Add to Cart](#)

Why Choose MPS

[Learn Why](#)

9. Some of MPS's direct sales, offers for sale, and importation into the United States of MPS Accused Products are to "support product development" by MPS customers who may make integrate MPS Accused Products into their designs, sometimes called "design wins," and make large additional purchases of MPS Accused Products.³

10. For example, MPS directly sells "Evaluation Kits" which are used to market MPS Accused Products and win larger contracts/design wins, including indirect sales.⁴

³ *Id.*

⁴ Product Overview of EVKT-MP2651, <https://www.monolithicpower.com/en/products/evkt-mp2651.html>

Overview Related Tools Design Resources Technical Forum Quality [Order](#)

Products > EV Kits and EV Board > EVKT-MP2651

EVKT-MP2651

MP2651 Evaluation Kit Active [Datasheet](#)




Description

The EVKT-MP2651 is an evaluation kit designed for the MP2651. It demonstrates the capabilities of the MP2651, a buck-boost charger IC designed for battery packs with 1 cell to 4 cells in series.

The device can accept a wide 4V to 22V input voltage (V_{IN}) range to charge the battery. It also supplies a wide 3V to 21V voltage range at the V_{OUT} pin in source mode. This function is compliant with USB power delivery (PD) specifications.

Product Evaluated

MP2651GVT Active

¹²C-Controlled, USB PD 6A Buck-Boost Charger with OTG/Source Mode for 1-Cell to 4-Cell Series Battery Applications

11. MPS maintains sales offices in the United States to sell MPS Accused Products and MPS assists its customers with the design of customer products to integrate MPS Accused Products into MPS customer products, including in the United States.⁵

We have sales offices in China, India, Japan, South Korea, Singapore, Taiwan, the United States and throughout Europe. Our products typically require a highly technical sales and applications engineering effort where we assist our customers in the design and use of our products in their application. We maintain a staff of applications engineers who work directly with our customers' engineers in the development of their systems' electronics containing our products.

12. For example, MPS makes sales of MPS Accused Products through offices in Michigan, Washington, and California.⁶ On information and belief, MPS sales and marketing

⁵ MPS, Form 10-K (Dec. 31, 2022), https://media.monolithicpower.com/mps/cms/document/2/0/2022_mps_annual_report.pdf?_gl=1*1eopt24*_ga*MTU4NTU1NTQ3Ny4xNjgzNjM4MjIx*_ga_XNRPF6L9DD*MTY4NDE4NTgzOS4zLjEuMTY4NDE4NjA4OS4yMi4wLjA.&_ga=2.178535588.183754632.1684185838-1585555477.1683638221

⁶ MPS, Job Listings, <https://www.monolithicpower.com/en/about-mps/careers/job-listings.html>

personnel use MPS Accused Products in the United States, for example in demonstrations. This use is important to achieving design wins.

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[Sustainability & ESG](#)
[Careers](#)
[News & Press Releases](#)

[Apply](#)

View By Region: U.S.

Job Type	Title	Location
Finance (3)	Field Sales Engineer	Michigan
Design Engineering (62)	Field Sales Engineer (MPSnow)	
Marketing (4)	Position Overview	
Legal (5)	Job Functions:	
Applications Engineering (32)	Responsible for driving all design-in activity and wins within assigned customer accounts and geographies. Responsible for consistently exceeding assigned revenue targets. Indirect management of Manufacturers Representatives and channel partners (distribution branches)	
Other (31)	Field Sales Engineer	Washington
Human Resources (2)	Field Sales Engineer (MPSnow)	
Product Engineering (1)	Position Overview	
Test Engineering (4)	Job Functions:	
Field Applications Engineering (11)	Responsible for driving all design-in activity and wins within assigned customer accounts and geographies. Responsible for consistently exceeding assigned revenue targets. Indirect management of Manufacturers Representatives and channel partners (distribution branches)	

[North America Channel Manager](#)

San Jose, CA

North America Channel Manager

Overall knowledge of distribution and Rep sales processesAt least 5 years' experience working with semiconductor distributorsMust have general technical understanding of power semiconductors, customers, applications.General understanding of DTAM regions, and organizations Past history of success in driving a closed loop distribution process including:Training...

[Field Sales Engineer](#)

Michigan

Field Sales Engineer (FSE)

Primary functions:

Responsible for driving all design-in activity and wins within assigned customer accounts and geographies. Responsible for consistently meeting or exceeding assigned revenue targets.Work closely with MPS product division marketing and engineering personnel to identify target applications/circuits t...

13. MPS performs quality assurance in the United States, which on information and belief, involves use of MPS Accused Products in the United States.⁷ Quality control use in the United States is important to MPS design wins.

The screenshot shows a job listing for a 'Sr. Customer Quality Engineer' position. The header is in a dark blue bar with the title in white. Below the header, the title is repeated in bold, followed by 'Job Code: 1686' and 'Location: San Jose, CA'. A blue 'Apply' button is on the right. The job description states: 'This is an important customer-facing, hands-on role in an emerging Automotive Quality organization in a rapidly growing semiconductor IC company. The key responsibilities are to work seamlessly with related Engineering, Production, Business groups and other QA functions to ensure timely responses and efficient closure of customer Quality requests, such as handling field returns/8D/FA cases, and audit support. He/she will interface to many internal functions, as well as directly with customers, in responding to requests and managing customer quality situations. As such, candidate should have a solid quality / engineering background, along with good team competence and communication skills.' Below this, 'Major Responsibilities' are listed in a bulleted format.

Sr. Customer Quality Engineer

Sr. Customer Quality Engineer
Job Code: 1686
Location: San Jose, CA

Apply

This is an important customer-facing, hands-on role in an emerging Automotive Quality organization in a rapidly growing semiconductor IC company. The key responsibilities are to work seamlessly with related Engineering, Production, Business groups and other QA functions to ensure timely responses and efficient closure of customer Quality requests, such as handling field returns/8D/FA cases, and audit support. He/she will interface to many internal functions, as well as directly with customers, in responding to requests and managing customer quality situations. As such, candidate should have a solid quality / engineering background, along with good team competence and communication skills.

Major Responsibilities

- Manage customer quality requirements, inquiries/questions or issues, as the front-line interface.
- Manage Quality issue diagnoses, root-cause analysis with FA and other groups as hand-on contributor for the assigned customer accounts.
- Project-manage Automotive customer-audits in both HQ and our location in Chengdu as the customer-facing contact for MPS and our sub-cons.
- Write FA and co-develop 8D reports as well as manage customer-facing communications.

SUBJECT MATTER JURISDICTION

14. This court has subject matter jurisdiction over the patent infringement claims asserted in this case under 28 U.S.C. §§ 1331 and 1338(a).

PERSONAL JURISDICTION, VENUE, AND JOINDER

15. This Court has personal jurisdiction over Defendant MPS as a citizen/resident of Delaware. On information and belief, the Court further has personal jurisdiction over MPS, because MPS has regularly conducted and continue to conduct business in the United States, in the State of Delaware, and in this judicial district. On information and belief, MPS has committed infringing activities in Delaware and in this judicial district by making, using, offering for sale, and/or selling in the United States and/or importing into the United States, products and systems that infringe upon the Greenthread Patents, or by placing such infringing products and systems

⁷ MPS, Job Listings, <https://www.monolithicpower.com/en/about-mps/careers/job-listings.html>

into the stream of commerce with the awareness, knowledge, and intent that they would be used, offered for sale, or sold by others in this judicial district and/or purchased by consumers in this district.

16. Venue is proper as to MPS pursuant to 28 U.S.C. §§ 1391(b) and 1400(b) because it is a citizen/resident of Delaware and has committed, and continues to commit, acts of infringement in this District.

THE GREENTHREAD PATENTS

17. On April 16, 2013, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 8,421,195 (“the ’195 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed January 12, 2007. The ’195 Patent claims priority from U.S. Patent Application No. 10/934,915,⁸ filed on September 3, 2004. A true and correct copy of the ’195 Patent is attached hereto as Exhibit 1 and incorporated herein by reference.

18. On November 17, 2015, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 9,190,502 (“the ’502 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed October 16, 2014. The ’502 Patent claims priority from U.S. Patent Application No. 10/934,915,⁹ filed on September 3, 2004. A true and correct copy of the ’502 Patent is attached hereto as Exhibit 2 and incorporated herein by reference.

19. On December 17, 2019, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 10,510,842 (“the ’842 Patent”), entitled “Semiconductor Devices with

⁸ Pub. No. US 2006/0049464.

⁹ Pub. No. US 2006/0049464.

Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on May 9, 2017. The ’842 Patent claims priority from U.S. Patent Application No. 10/934,915,¹⁰ filed on September 3, 2004. A true and correct copy of the ’842 Patent is attached hereto as Exhibit 3 and incorporated herein by reference.

20. On August 4, 2020, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 10,734,481 (“the ’481 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on December 17, 2019. The ’481 Patent claims priority from U.S. Patent Application No. 10/934,915,¹¹ filed on September 3, 2004. A true and correct copy of the ’481 Patent is attached hereto as Exhibit 4 and incorporated herein by reference.

21. On September 14, 2021, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 11,121,222 (“the ’222 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on July 27, 2020. The ’222 Patent claims priority from U.S. Patent Application No. 10/934,915,¹² filed on September 3, 2004. A true and correct copy of the ’222 Patent is attached hereto as Exhibit 5 and incorporated herein by reference.

22. On April 26, 2022, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 11,316,014 (“the ’014 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on July 9, 2021. The ’014 Patent claims priority from U.S. Patent Application No. 10/934,915,¹³ filed on

¹⁰ Pub. No. US 2006/0049464.

¹¹ Pub. No. US 2006/0049464.

¹² Pub. No. US 2006/0049464.

¹³ Pub. No. US 2006/0049464.

September 3, 2004. A true and correct copy of the '014 Patent is attached hereto as Exhibit 6 and incorporated herein by reference.

23. The '195, '502, '842, '481, '222, and '014 Patents are collectively referred to as the "Greenthread Patents."

24. Greenthread exclusively owns all rights, title, and interest in the Greenthread Patents necessary to bring this action, including the right to recover past and future damages. Certain of the Greenthread Patents were previously owned by Dr. G.R. Mohan Rao ("Dr. Rao"). On April 27, 2015, Dr. Rao assigned to Greenthread the then-issued Greenthread Patents and all related "continuations, continuations-in-part and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents." Dr. Rao's assignment was recorded with the U.S. Patent and Trademark Office on May 13, 2015, and again on July 22, 2021, and is attached hereto as Exhibit 7. Greenthread has therefore owned all rights to the Greenthread Patents necessary to bring this action throughout the period of MPS's infringement and still owns those rights to the Greenthread Patents.

25. MPS is not currently licensed to practice the Greenthread Patents.

26. The Greenthread Patents are valid and enforceable.

FACTUAL BACKGROUND

27. Dr. G.R. Mohan Rao ("Dr. Rao"), the sole inventor of the Greenthread Patents, has been an innovator in the semiconductor industry since the 1960s. He is a named inventor on more than 100 Patents worldwide and authored numerous technical publications over the last 50 years.

28. In September 1968, Dr. Rao received a Ph.D. in physics with a specialization in electronics from Andhra University in Waltair, India. He then traveled to the United States to attend a graduate program in physics at the University of Cincinnati.

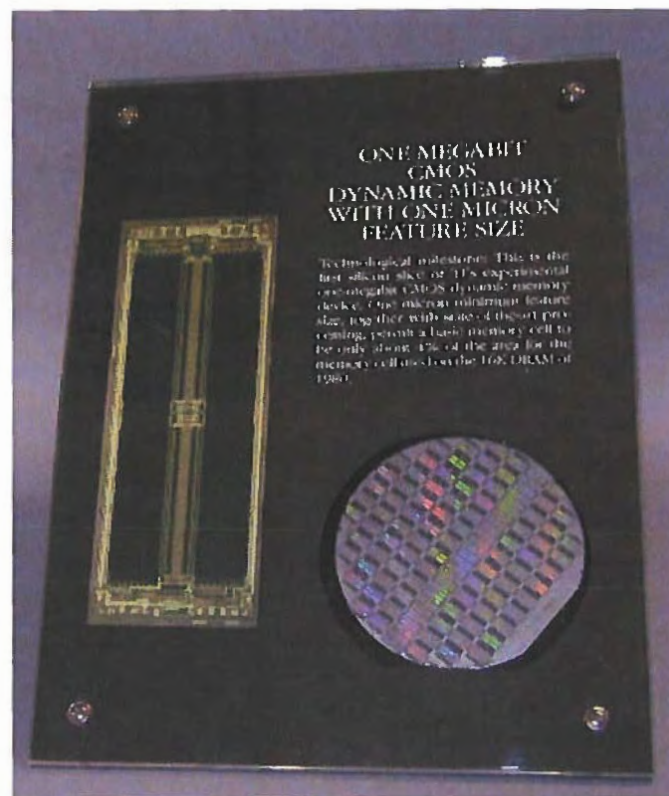
29. After learning of an opportunity to work with Professor William Carr of Southern Methodist University (“SMU”), Dr. Rao transferred to SMU where he earned a Ph.D in Electrical Engineering. While there, he worked in the SMU laboratory with Jack Kilby of Texas Instruments (a pioneering electrical engineer who would later receive a Nobel Prize for his work), on metal-oxide-silicon transistors (“MOS devices”), which are used for switching and amplifying electronic signals in electronic devices. MOS devices form the basis of modern electronics and are the most widely used semiconductor devices in the world. The U.S. Patent and Trademark Office has called this device a “groundbreaking invention that transformed life and culture around the world.”¹⁴ Dr. Rao built these devices from scratch while a graduate student at SMU.

30. Through his mentor, Jack Kilby, Dr. Rao interviewed with—and was ultimately hired by—Texas Instruments to continue his work on MOS devices in 1972. Dr. Rao worked at Texas Instruments for the next twenty-two years, rising from an engineer to a Senior Fellow. At that time, Texas Instruments had only 12 Senior Fellows out of approximately 20,000 engineers. Eventually, Dr. Rao moved into a management position at Texas Instruments, ultimately becoming a Senior Vice President in 1985.

31. At Texas Instruments, Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments’ 4-kilobit RAM product. That patent was merely the beginning of Dr. Rao’s long inventive career. Indeed, from the late 1970s through the mid-1980s, Dr. Rao worked on or managed projects relating to Texas Instruments’ 64kb RAM, 256Kb RAM, 1Mb RAM, 4 Mb RAM, EEPROM, SRAM, and microcontrollers. For that work, Dr. Rao received numerous additional U.S. Patents.

¹⁴ *Remarks by Director Iancu at the 2019 International Intellectual Property Conference* (June 10, 2019), <https://www.uspto.gov/about-us/news-updates/remarks-director-iancu-2019-international-intellectual-property-conference>

32. The USPTO was not the only organization to recognize Dr. Rao's achievements. Some of Dr. Rao's work at Texas Instruments was so remarkable that it has been credited in multiple exhibits in the National Museum of American History at the Smithsonian Institution.¹⁵ For example, the Smithsonian has displayed Texas Instruments' experimental 1-megabit CMOS DRAM, produced in April 1985 under Dr. Rao's leadership, and credited Dr. Rao for the achievement.¹⁶



33. In 1994, Dr. Rao left Texas Instruments for Cirrus Logic. During his two-year tenure at Cirrus Logic, he received more U.S. Patents relating to his work on integrated graphics

¹⁵ *Texas Instruments Collection Summary Comments Provided by Texas Instruments Staff*, <http://smithsonianchips.si.edu/texas/wafer.htm>

¹⁶ *Texas Instruments Collection Wafer Display*, TI number: G00200 (1985), http://smithsonianchips.si.edu/texas/t_360.htm

controllers and memory.

34. In 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different consulting companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years.

35. In 2003, Dr. Rao and Philip John founded Greenthread to continue Dr. Rao's pioneering work. A focal point of Dr. Rao's research was poor refresh time and the related problem of how to deal with and control the movement of both wanted and unwanted carriers in semiconductor devices, including memory and logic devices. Dr. Rao realized that graded dopants could be used to create a "drift layer" and other structures to facilitate the movement—in an upward or downward direction, as appropriate—of carriers from the semiconductor surfaces down into the substrate and vice versa. It was Dr. Rao's work on this problem that culminated in the Greenthread Patents.

MPS'S INFRINGEMENT

36. MPS has directly and indirectly infringed, and continues to infringe, one or more claims of each of the Greenthread Patents through making, using, offering to sell, selling within the United States, and/or importing into the United States semiconductor products that practice the claimed inventions (*i.e.*, the MPS Accused Products).

37. Further, in concert with its authorized distributors and customers, MPS causes or induces infringing accused products to be made, used, offered to be sold, sold within the United States, and/or imported into the United States.

38. Specifically, MPS has designed and/or incorporated into other products semiconductor devices for use in analog, digital, and mixed-signal integrated circuits. The MPS Accused Products include switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOSFET drivers, isolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, current sensors, and other products containing transistors, and are further identified in Exhibit 8.

39. MPS had knowledge of Greenthread Patents at least through the USPTO's citation of U.S. Patent Pub. 2007/0158790 (U.S. Patent Application No. 11/622,496 issued as U.S. Patent No. 8,421,195) during prosecution of MPS's U.S. Patent No. 8,598,637, titled "High voltage junction field effect transistor with spiral field plate." Accordingly MPS has had knowledge of the Greenthread Patents since before 2013, the date of the MPS patent.

40. MPS has knowledge of the Greenthread Patents at least as of the filing of this complaint.

41. MPS's infringement is willful.

42. As shown in Exhibit 8, the exemplary MPS MP86905 monolithic half-bridge meets each and every element of at least one claim of the Greenthread Patents.

43. The infringing structures within semiconductor devices identified in Exhibit 8 have application, not only in the product identified in Exhibit 8, but in many types of devices designed and manufactured by MPS, for example to improve switching speed of MPS Accused Products.

44. Upon information and belief, MPS designs and contracts fabrication for

semiconductor devices using similar designs according to a limited number of processes, many or all of which utilize substantially similar process steps, including process steps for creating regions with graded dopant concentrations.

45. Upon information and belief, the MPS semiconductor devices are in relevant part substantially similar to the exemplary MPS MP86905 monolithic half-bridge shown in Exhibit 8, particularly with regard to the manner in which the exemplary MPS MP86905 monolithic half-bridge includes and utilizes regions with graded dopant concentrations. Exhibit 8 is thus illustrative of the manner in which the MPS Accused Products meet the claim limitations of the Greenthread Patents.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,421,195

46. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

47. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the MPS Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the MPS Accused Products that it obtains during discovery.

48. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

49. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '195 Patent.

50. As alleged above, the products analyzed in Exhibit 8 are exemplary of the MPS Accused Products.

51. As alleged above, MPS has and continues to infringe at least one claim of the '195

Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States MPS Accused Products. Defendant's infringement is and continues to be willful.

52. As alleged above, Defendant induces infringement of at least one claim of the '195 Patent by designing and marketing infringing products for sale, use, and importation into the United States.

53. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,190,502

54. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

55. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the MPS Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the MPS Accused Products that it obtains during discovery.

56. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

57. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '502 Patent.

58. As alleged above, the products analyzed in Exhibit 8 are exemplary of the MPS Accused Products.

59. As alleged above, MPS has and continues to infringe at least one claim of the '502 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States MPS Accused Products. Defendant's infringement is and continues to be willful.

60. As alleged above, Defendant induces infringement of at least one claim of the '502 Patent by designing and marketing infringing products for sale, use, and importation into the United States.

61. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 10,510,842

62. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

63. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the MPS Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the MPS Accused Products that it obtains during discovery.

64. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

65. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '842 Patent.

66. As alleged above, the products analyzed in Exhibit 8 are exemplary of the MPS Accused Products.

67. As alleged above, MPS has and continues to infringe at least one claim of the '842 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States MPS Accused Products. Defendant's infringement is and continues to be willful.

68. As alleged above, Defendant induces infringement of at least one claim of the '842 Patent by designing and marketing infringing products for sale, use, and importation into the United States.

69. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,734,481

70. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

71. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the MPS Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the MPS Accused Products that it obtains during discovery.

72. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

73. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '481 Patent.

74. As alleged above, the products analyzed in Exhibit 8 are exemplary of the MPS Accused Products.

75. As alleged above, MPS has and continues to infringe at least one claim of the '481 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States MPS Accused Products. Defendant's infringement is and continues to be willful.

76. As alleged above, Defendant induces infringement of at least one claim of the '481 Patent by designing and marketing infringing products for sale, use, and importation into the

United States.

77. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 11,121,222

78. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

79. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the MPS Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the MPS Accused Products that it obtains during discovery.

80. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

81. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '222 Patent.

82. As alleged above, the products analyzed in Exhibit 8 are exemplary of the MPS Accused Products.

83. As alleged above, MPS has and continues to infringe at least one claim of the '222 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States MPS Accused Products. Defendant's infringement is and continues to be willful.

84. As alleged above, Defendant induces infringement of at least one claim of the '222 Patent by designing and marketing infringing products for sale, use, and importation into the United States.

85. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 11,316,014

86. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

87. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the MPS Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the MPS Accused Products that it obtains during discovery.

88. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

89. As alleged above and in Exhibits 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '014 Patent.

90. As alleged above, the products analyzed in Exhibit 8 are exemplary of the MPS Accused Products.

91. As alleged above, MPS has and continues to infringe at least one claim of the '014 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States MPS Accused Products. Defendant's infringement is and continues to be willful.

92. As alleged above, Defendant induces infringement of at least one claim of the '014 Patent by designing and marketing infringing products for sale, use, and importation into the United States.

93. MPS's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

DAMAGES

94. As a result of MPS's acts of infringement, Greenthread has suffered and continues to suffer actual and consequential damages. However, Greenthread does not yet know the full extent of the infringement and the amount of damages cannot be ascertained except through discovery and special accounting. To the fullest extent permitted by law, Greenthread seeks recovery of damages at least for reasonable royalties, unjust enrichment, and benefits received by MPS as a result of using the patented technology. Greenthread further seeks any other damages to which Greenthread is entitled under law or in equity, including enhanced damages for MPS's willful infringement.

DEMAND FOR JURY TRIAL

95. Greenthread hereby demands a jury trial for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Greenthread respectfully requests that this Court enter judgment in its favor as follows:

A. That Judgment be entered that Defendant has infringed one or more claims of the Greenthread Patents, literally and under the doctrine of equivalents;

B. That, in accordance with 35 U.S.C. § 283, Defendant and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Greenthread Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the MPS Accused Products;

C. An award of damages sufficient to compensate Greenthread for Defendant's infringement and enhanced damages under 35 U.S.C. § 284;

D. That the case be found exceptional under 35 U.S.C. § 285 and that Greenthread be awarded its reasonable attorneys' fees;

E. Costs and expenses in this action;

F. Damages for pre-issuance infringement under 35 U.S.C. § 154(d);

G. An award of prejudgment and post-judgment interest; and

H. Such other and further relief as the Court may deem just and proper.

Dated: May 26, 2023

Respectfully submitted,

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GREENTHREAD, LLC***

EXHIBIT 1

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 8,421,195 B2**
(45) **Date of Patent:** **Apr. 16, 2013**

(54) **SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS**

(76) Inventor: **G. R. Mohan Rao**, McKinney, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/622,496**

(22) Filed: **Jan. 12, 2007**

(65) **Prior Publication Data**

US 2007/0158790 A1 Jul. 12, 2007

Related U.S. Application Data

(62) Division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) **Int. Cl.**
H01L 21/02 (2006.01)

(52) **U.S. Cl.**
USPC 257/655; 257/611; 257/E33.048;
438/510

(58) **Field of Classification Search** 257/655,
257/269
See application file for complete search history.

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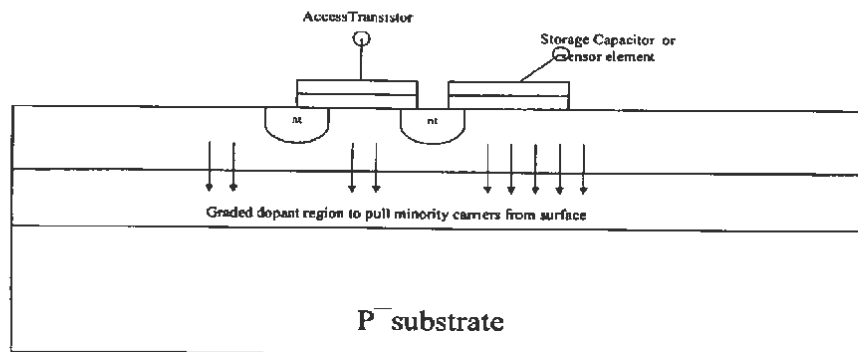
Primary Examiner Ajay K Arora

(74) *Attorney, Agent, or Firm* Eugene M. Cummings, P.C.

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICS, improvement in refresh time for DRAM's, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFET's, and a host of other applications.

14 Claims, 10 Drawing Sheets



CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

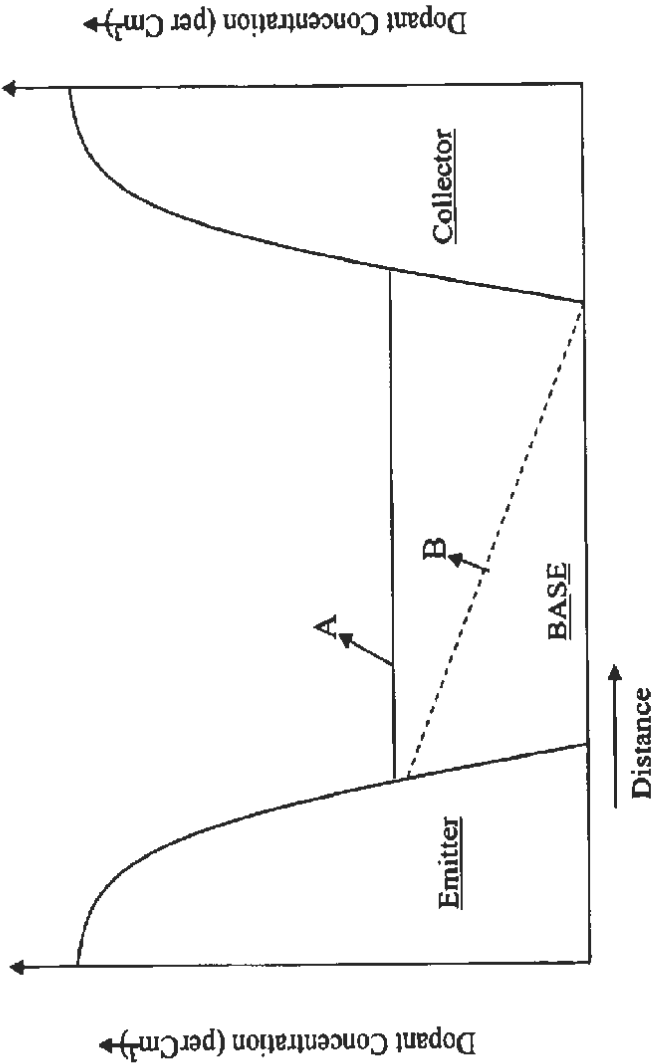


Figure 1 Prior Art

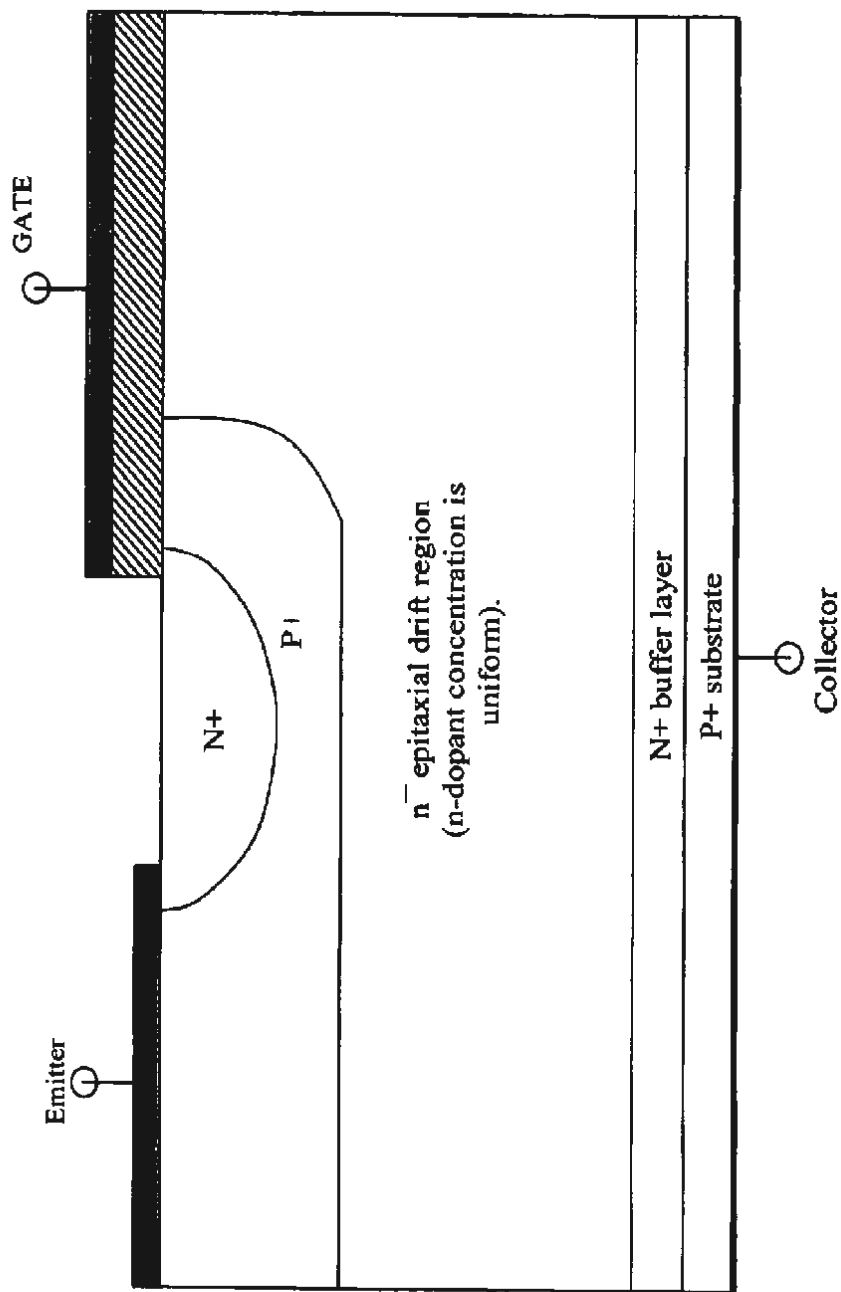


FIGURE 2 Prior art

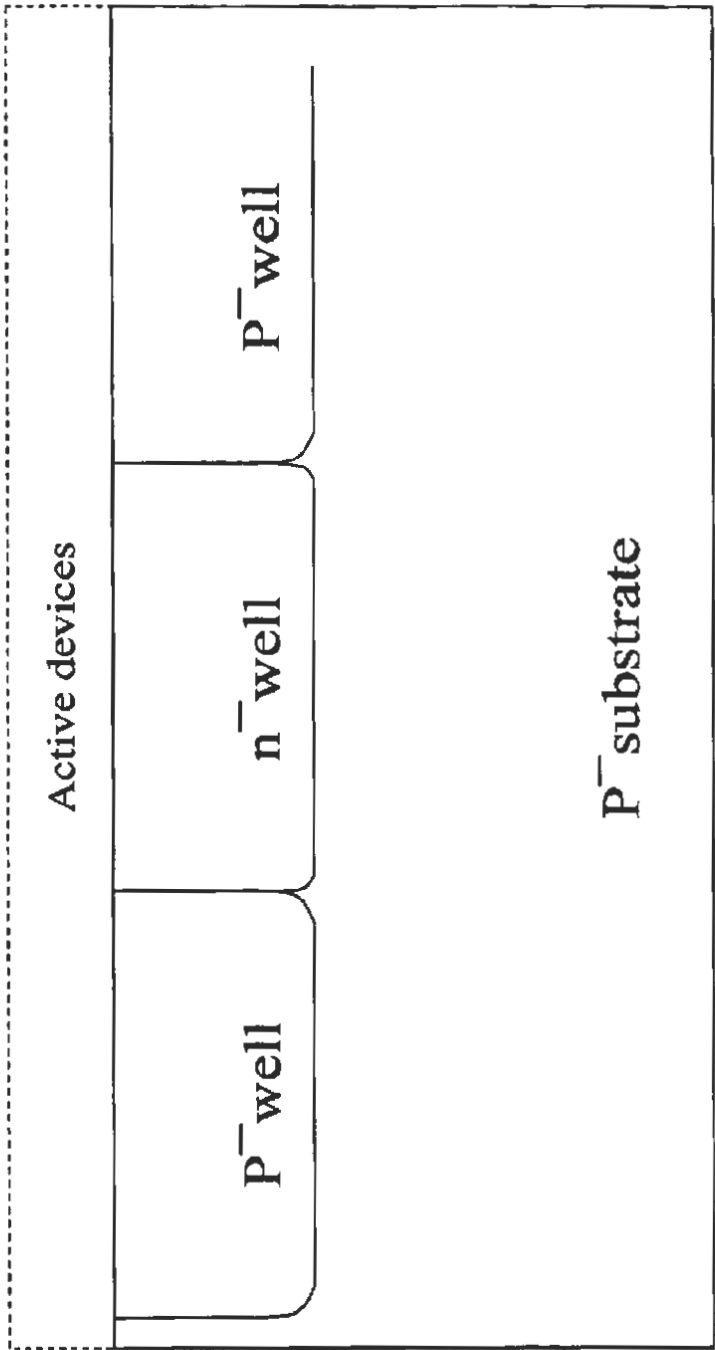


FIGURE 3(a) Prior art (Twin well CMOS) for a CMOS integrated circuit

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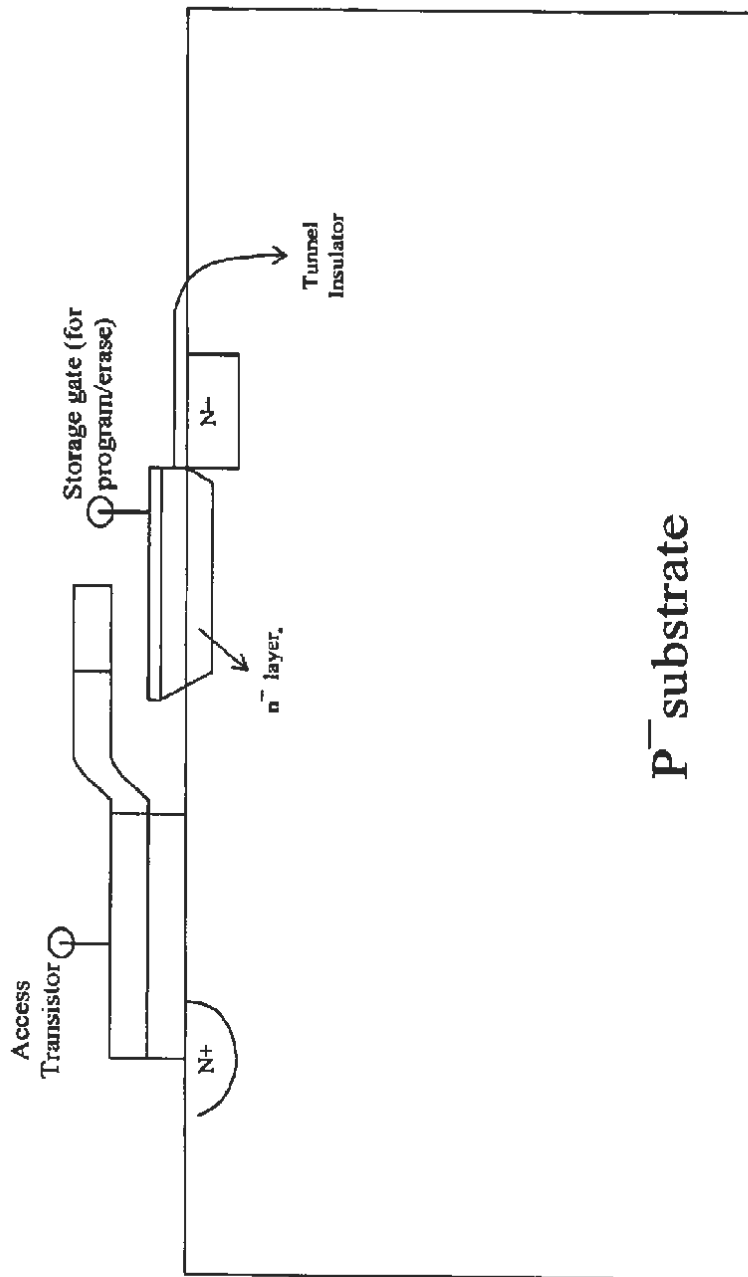


FIGURE 3(b) Prior art for a two-device EEPROM memory cell

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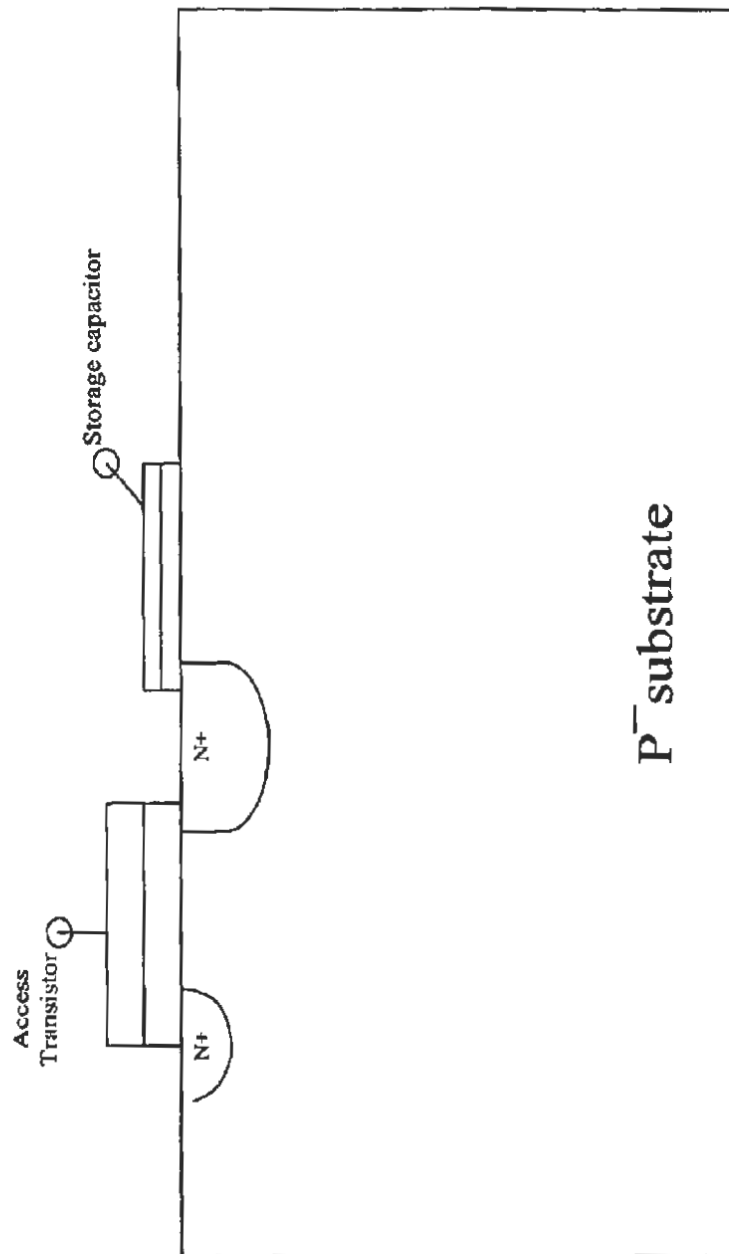


FIGURE 3(c) Prior art for a 1T-1C DRAM memory cell

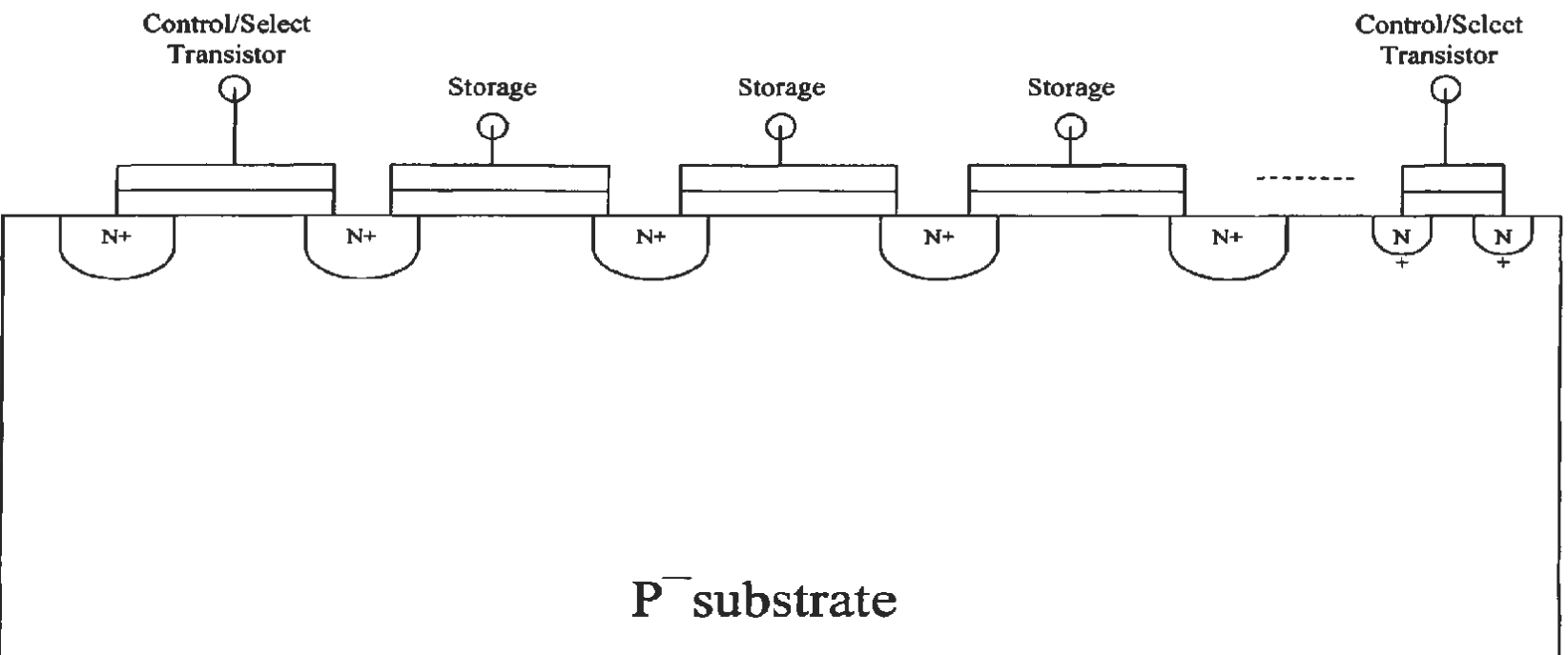


FIGURE 3(d) Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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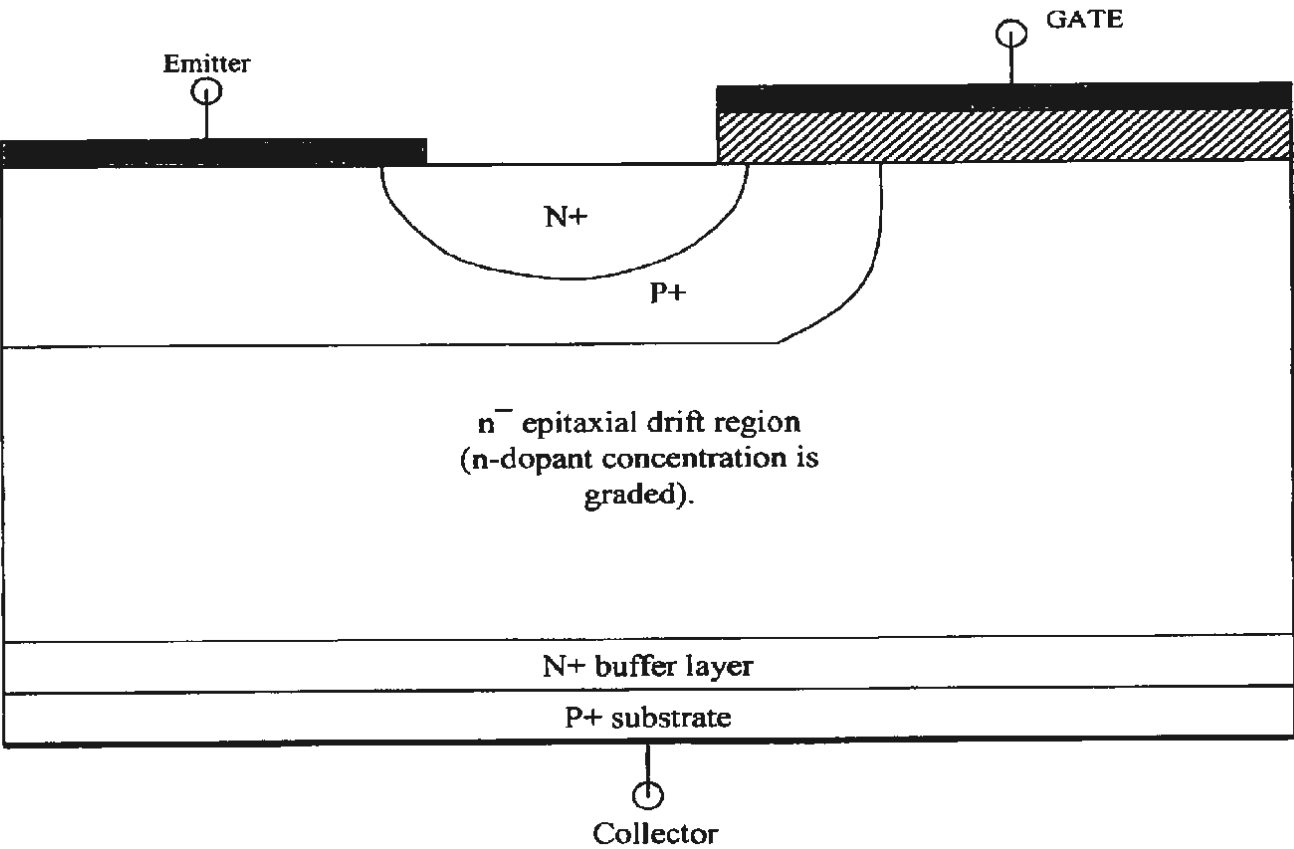


FIGURE 4 A dopant - concentration grinded drift region in a IGBT

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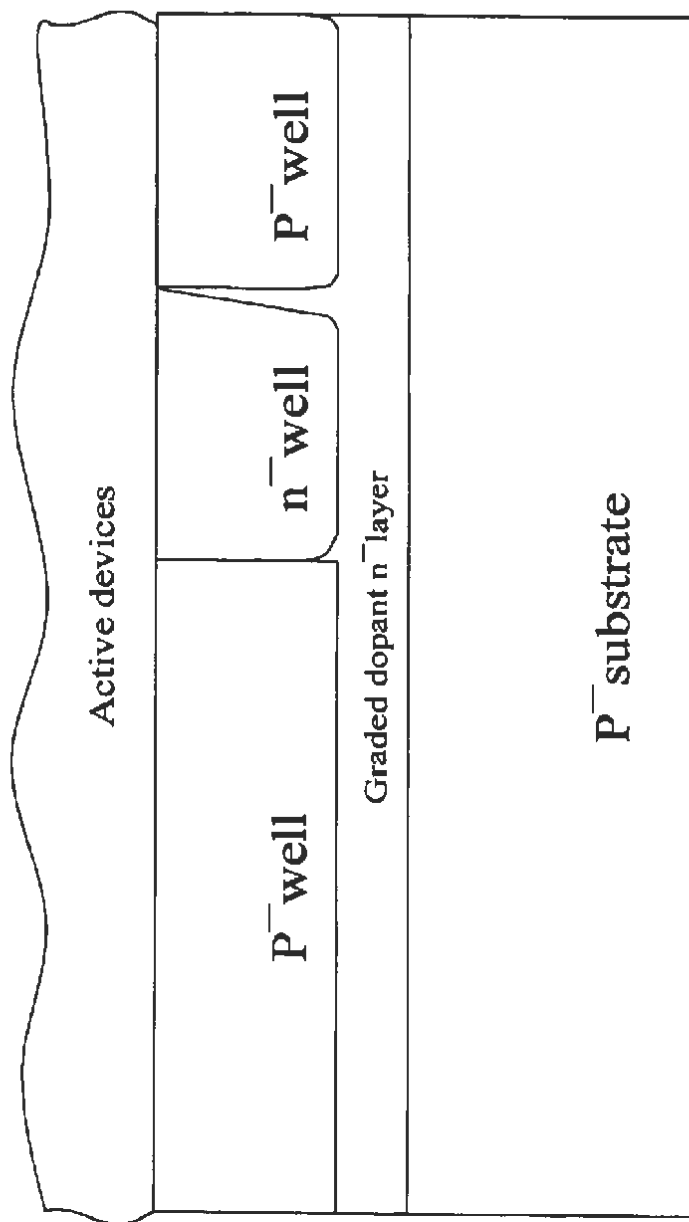


FIGURE 5(a) A CMOS Substrate for digital, mixed, signal, and sensors IC's

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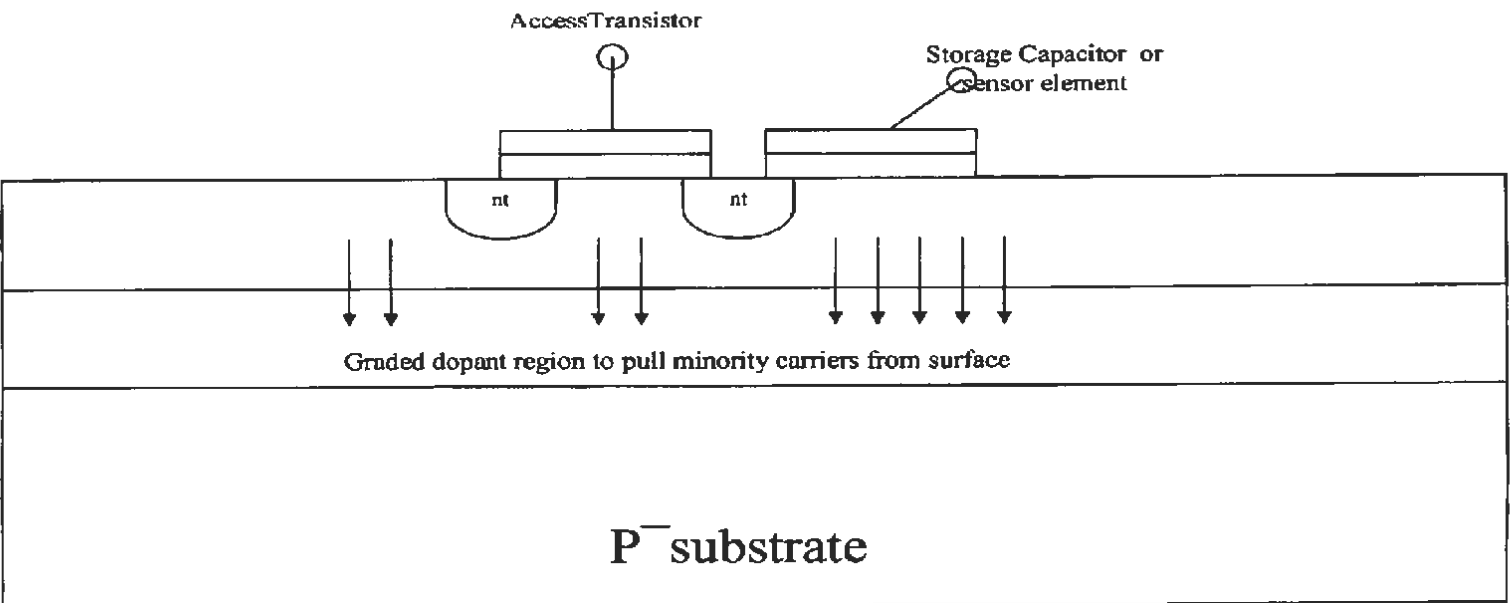


FIGURE 5(b) CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

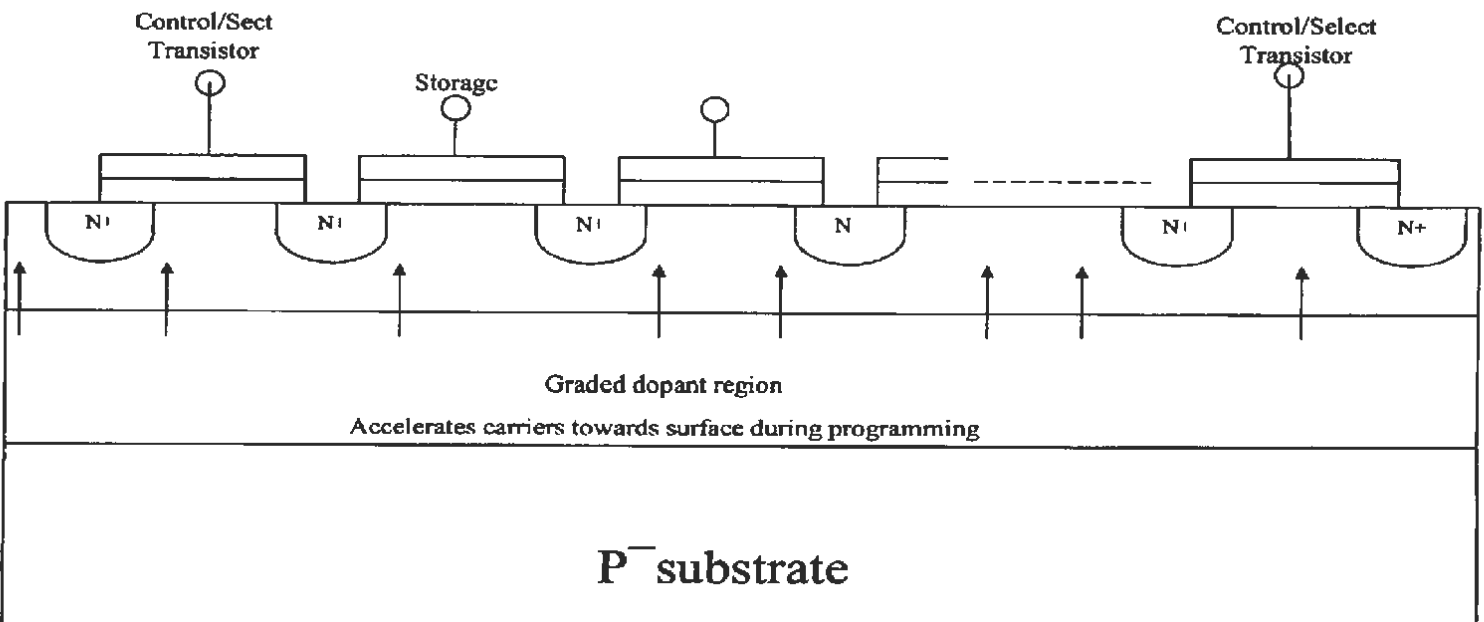


FIGURE 5(c) CMOS Substrate for a NAND flash device to improve programming times

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**SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS****CROSS-REFERENCE TO RELATED
APPLICATION**

This application is a Divisional of U.S. application Ser. No. 10/934,915, filed on Sep. 3, 2004, now abandoned which application is incorporated herein by reference.

FIELD OF INVENTION

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBT's (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND OF INVENTION

Bipolar Junction transistors (BJT) are minority carrier devices as the principle device conduction mechanism. However, majority carriers also a small yet finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. Carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an 'aiding drift field', to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFET's (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region' in a IGBT. In contrast to BJT's, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in the case of an n-channel IGBT) require different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

'Retrograde' wells have been attempted, with little success, to help improve soft error immunity in SRAM's and visual quality in imaging circuits. FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3(b), 3(c), and 3(d) illustrate device cross sections, as practiced today. 'Retrograde' and 'halo' wells have also been attempted to improve refresh time in DRAM's (dynamic random access memories), as well as, reducing dark current (background noise)

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and enhance RGB (Red, Green, Blue) color resolution in digital camera Ics. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base, and collector, for the two most popular bipolar junction transistors: namely, A uniform base, and B graded base;

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base):

FIGS. 3(a), 3(b), 3(c), 3(d) illustrate cross sections commonly used CMOS silicon substrate with two wells (one n-well in which p-channel transistors are subsequently fabricated, and, one p-well in which n-channel transistors are subsequently fabricated)—typical IC, EEPROM using tunnel insulator, DRAM and NAND flash;

FIG. 4 illustrates the cross section of a IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5(a), 5(b), 5(c) illustrate the cross sections of a MOS silicon substrate with two wells, and, an underlying layer using embodiments of the invention to improve performance in each application VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION OF THE INVENTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, where as the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region - n' buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The 'average' base resistance is optimized, so that conductivity modulation and lifetime (for minority carriers) in base region are not compromised. By sweeping the carriers towards the n' buffer region two advantages are obtained the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. More importantly, during t_{off} , holes can be recombined much quicker at the n' buffer layer, compared to a uniformly doped n' epitaxial drift region by establishing a different dopant gradient near the n+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Epitaxy enhances lifetime, but, epitaxy is

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not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC's. These unwanted carriers can discharge dynamically-held 'actively held high' nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM's is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC's is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC's with the embodiments described here. Creating 'Sub Terrain' recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. In nonvolatile memory devices, to decrease programming time, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction field-effect transistors where the "channel pinchoff" is controlled by a graded channel instead of a uniformly doped channel (as practiced in prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface, to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single well, as well triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments, individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It

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should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.

3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.

4. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a linear gradient.

5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.

6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.

7. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a complimentary error function gradient.

8. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer.

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said substrate to said surface layer; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said substrate TO SAID SURFACE LAYER.

9. The CMOS Semiconductor device of claim 8, wherein said drift layer is deeply-implanted layer.

10. The CMOS Semiconductor device of claim 8, wherein said drift layer is an epitaxial layer.

11. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a linear gradient.

12. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a quasi-linear gradient.

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13. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a exponential gradient.

14. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a complimentary error function gradient.

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* * * * *

EXHIBIT 2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 9,190,502 B2**
(45) **Date of Patent:** ***Nov. 17, 2015**

(54) **SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS**

(71) Applicant: **G. R. Mohan Rao**, Allen, TX (US)

(72) Inventor: **G. R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **Greenthread, LLC**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/515,584**

(22) Filed: **Oct. 16, 2014**

(65) **Prior Publication Data**

US 2015/0035004 A1 Feb. 5, 2015

Related U.S. Application Data

(60) Continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) **Int. Cl.**

H01L 21/02 (2006.01)
H01L 29/739 (2006.01)
H01L 27/115 (2006.01)
H01L 29/36 (2006.01)
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 29/7395** (2013.01); **H01L 27/11521** (2013.01); **H01L 27/11524** (2013.01); **H01L 29/36** (2013.01); **H01L 27/0214** (2013.01); **H01L 27/10844** (2013.01)

(58) **Field of Classification Search**

CPC **H01L 29/7395**
USPC **438/37**
See application file for complete search history.

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Primary Examiner Ajay K Arora

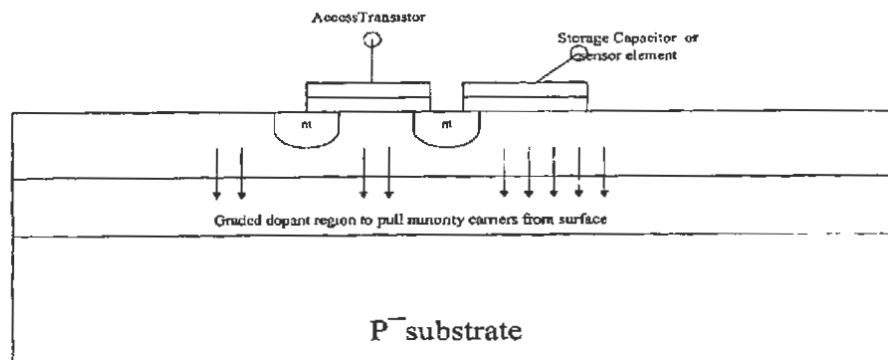
(74) *Attorney, Agent, or Firm* Howison & Arnott, LLP

(57)

ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT IC's, improvement in refresh time for DRAM's, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging IC's, better sensitivity for varactors in tunable filters, higher drive capabilities for JFET's, and a host of other applications.

12 Claims, 10 Drawing Sheets



CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

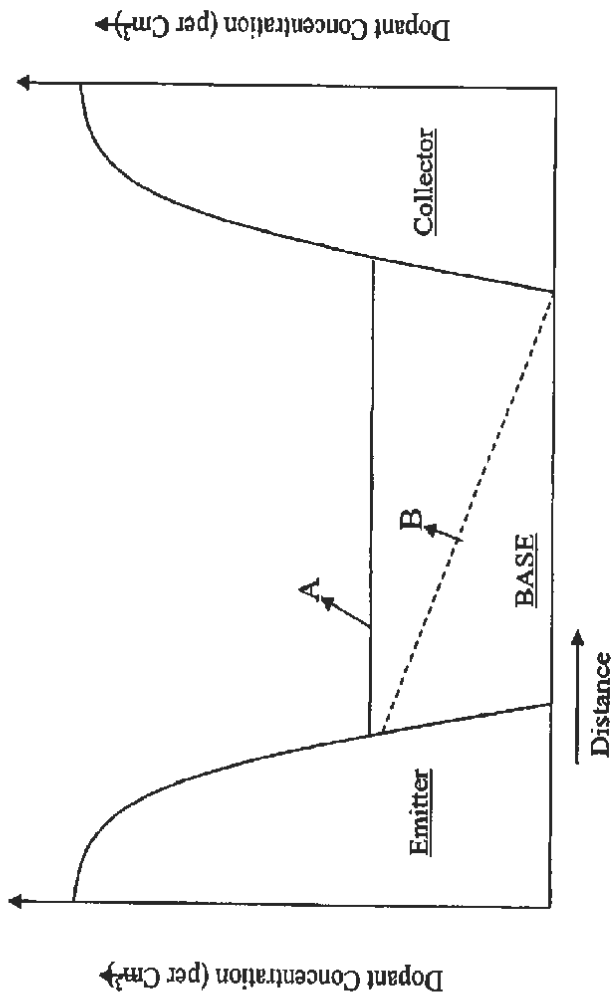


Figure 1 Prior Art

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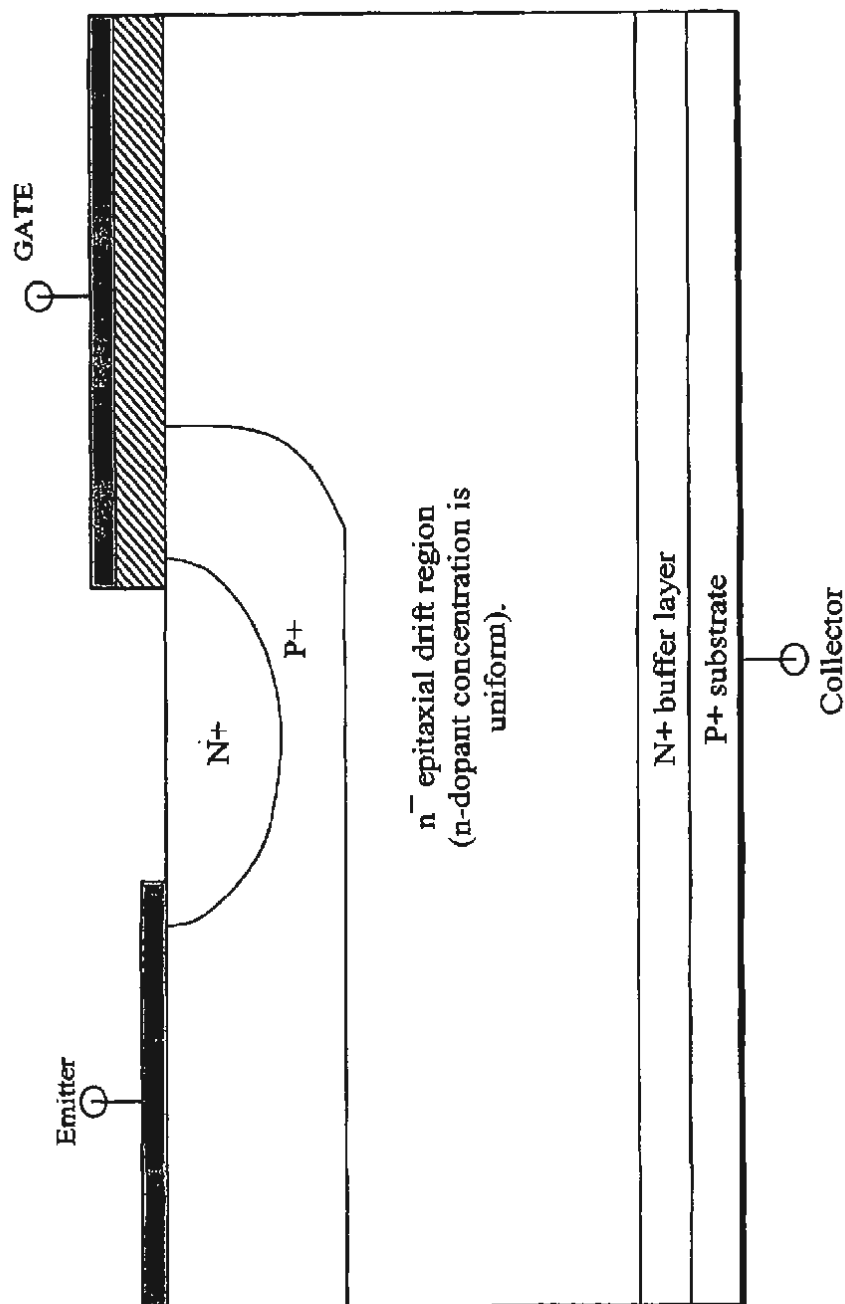


FIGURE 2 Prior art

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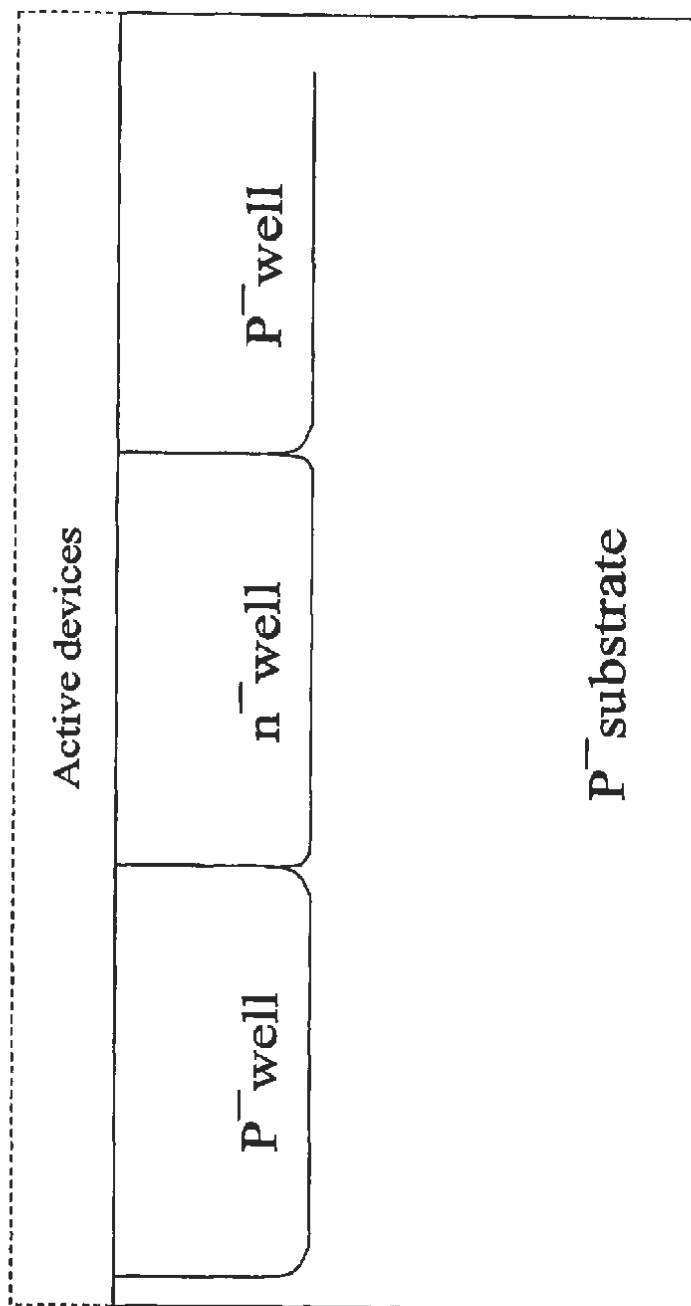


FIGURE 3(a) Prior art (Twin well CMOS) for a CMOS integrated circuit

U.S. Patent

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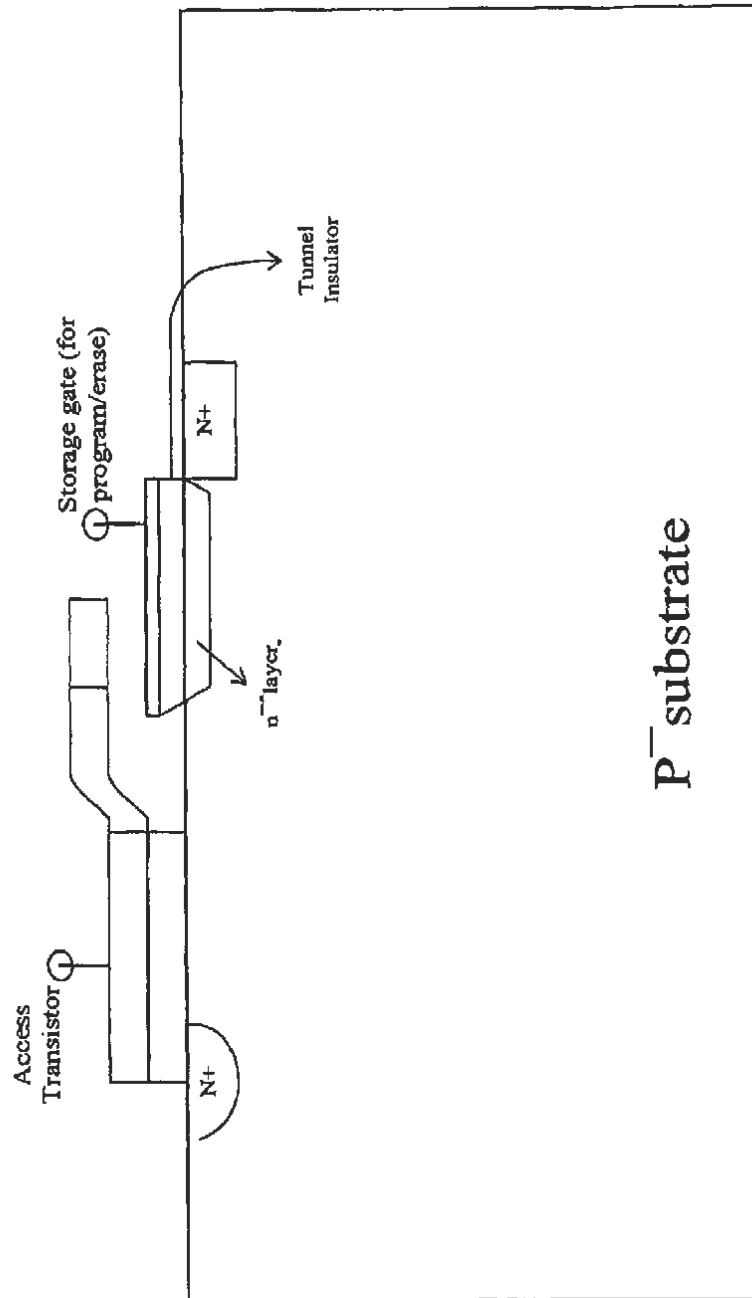


FIGURE 3(b) Prior art for a two-device EEPROM memory cell

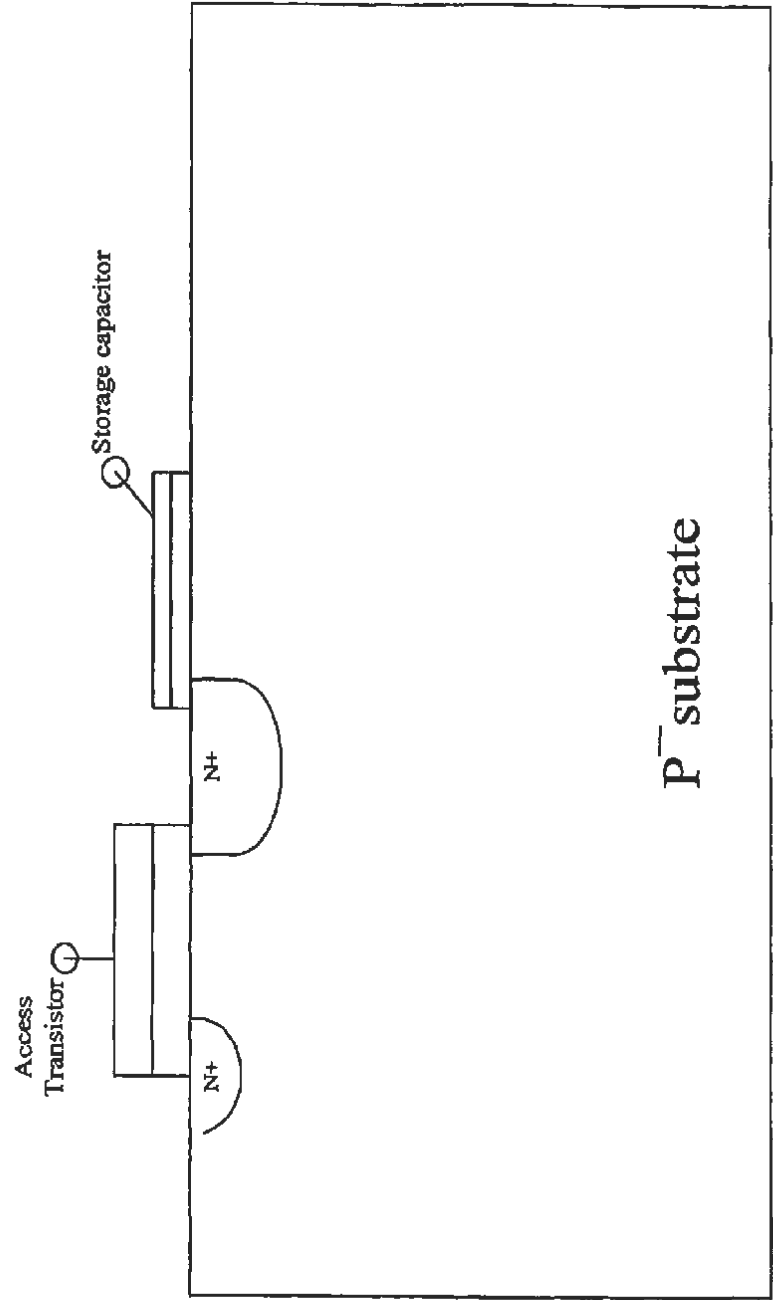


FIGURE 3(c) Prior art for a 1T-1C DRAM memory cell

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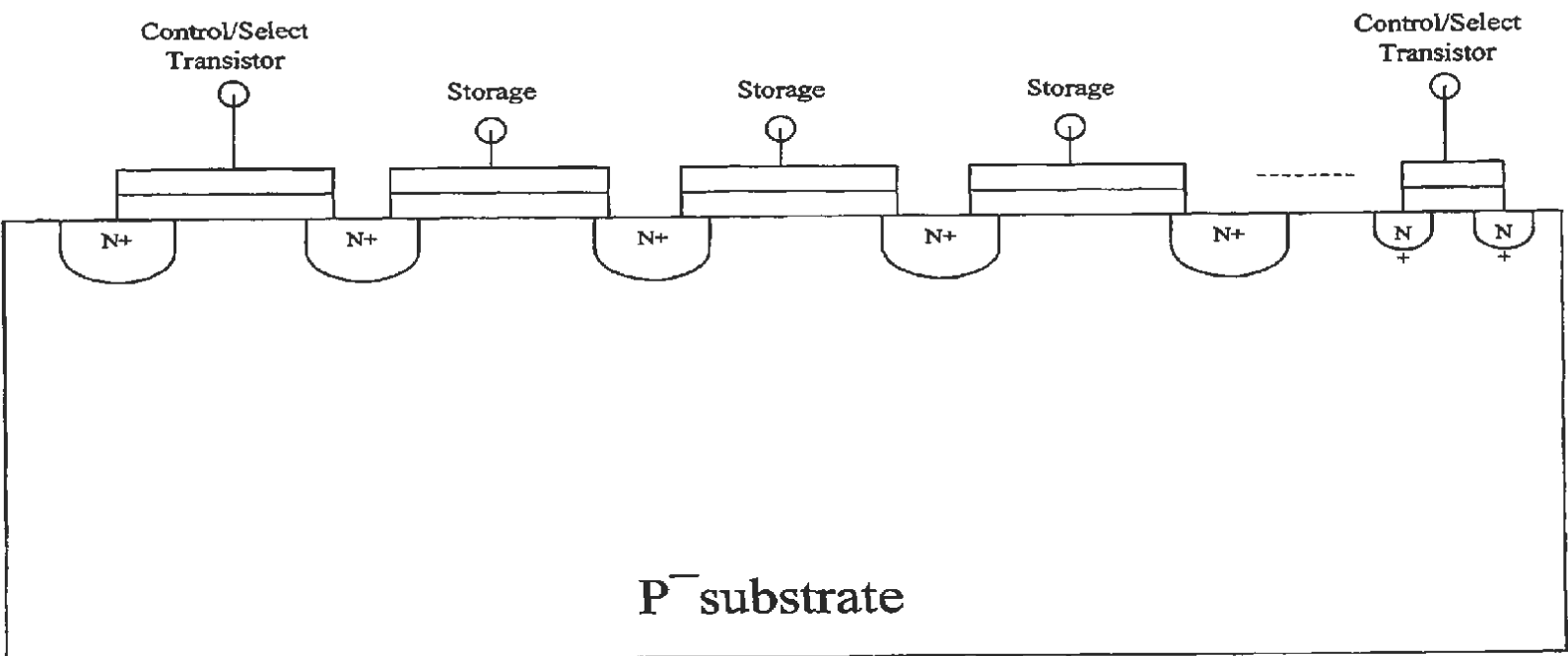


FIGURE 3(d) Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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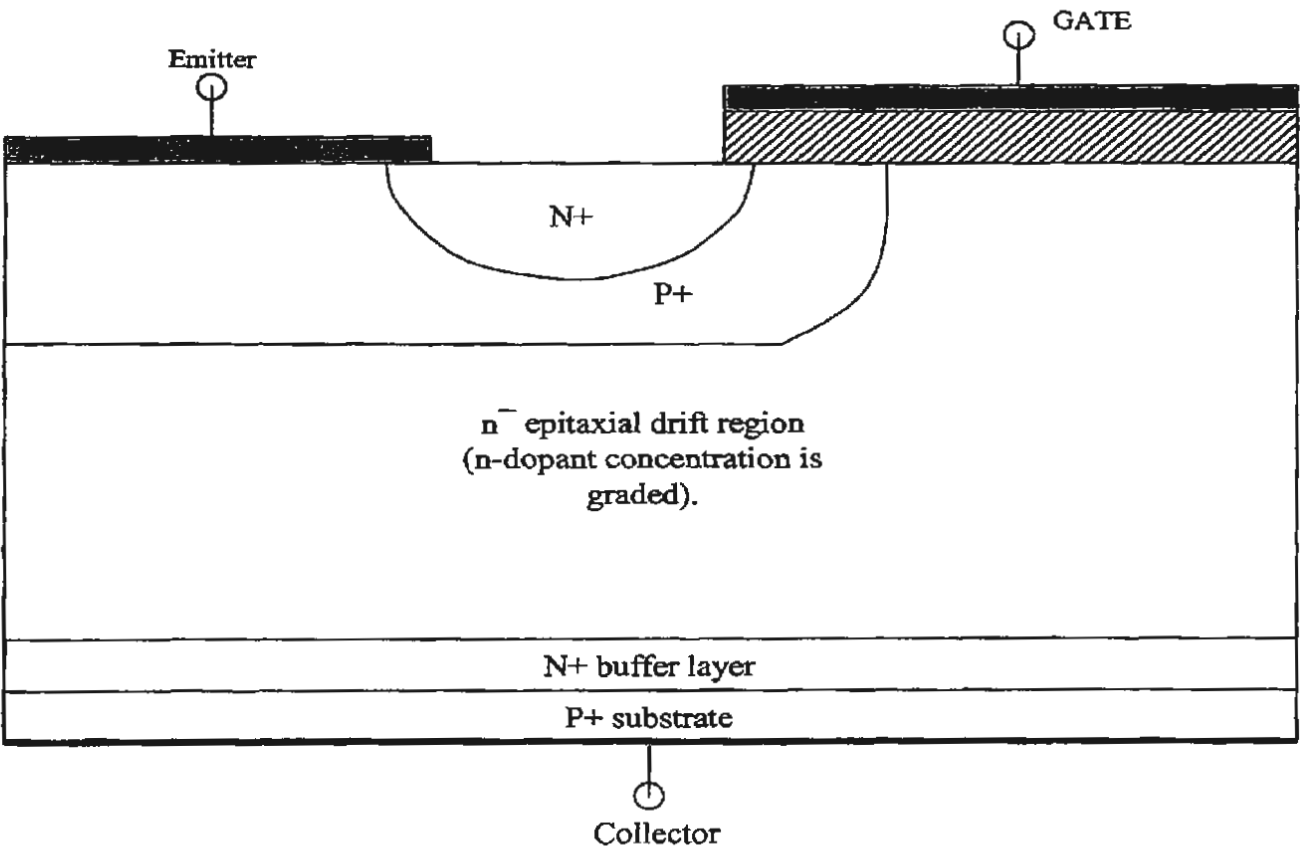


FIGURE 4 A dopant - concentration graded drift region in a IGBT

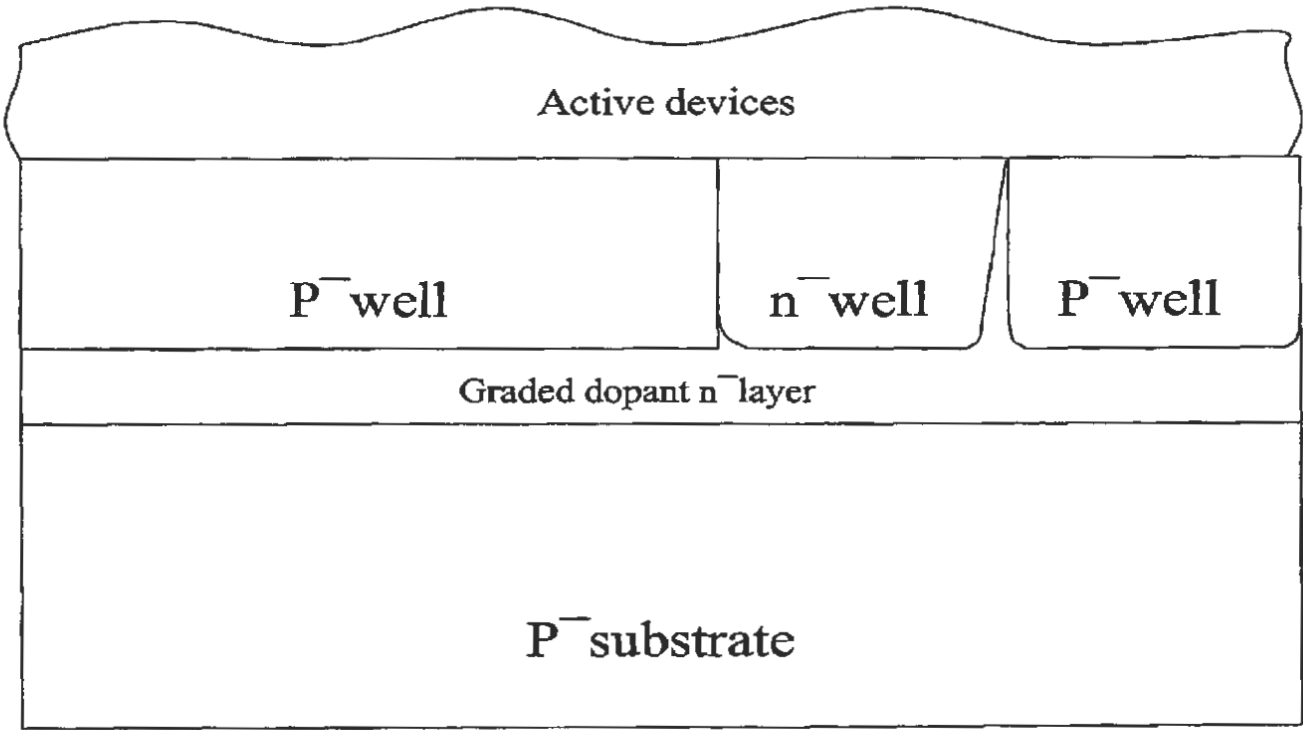


FIGURE 5(a) A CMOS Substrate for digital, mixed, signal, and sensors IC's

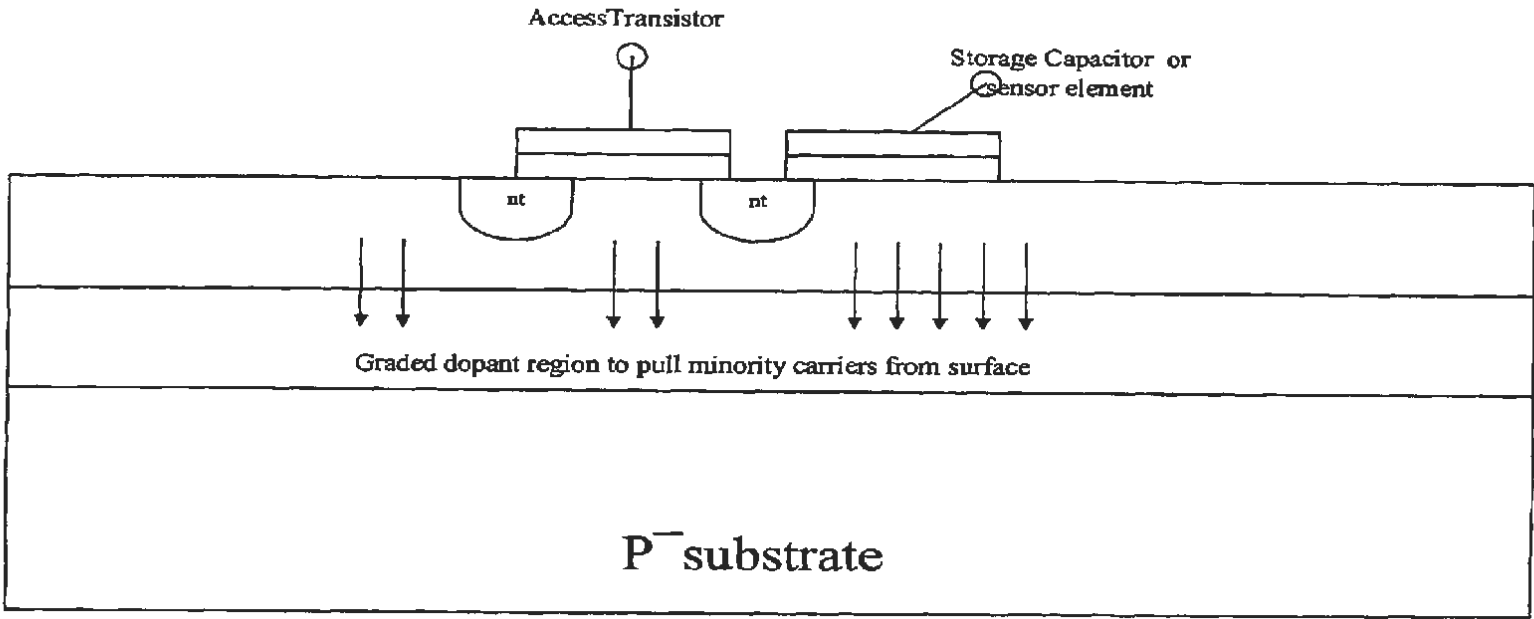


FIGURE 5(b) CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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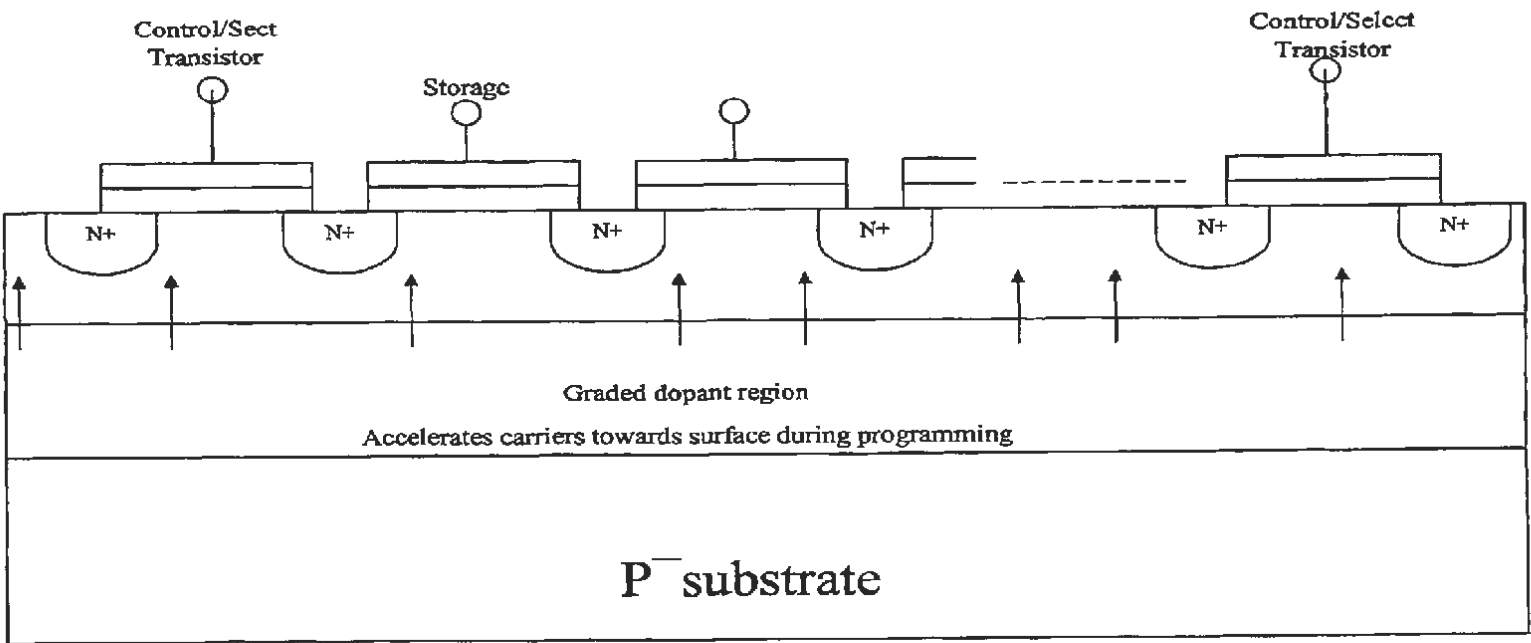


FIGURE 5(c) CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATION

This continuation application claims priority to and the benefit of U.S. application Ser. No. 13/854,319, filed on Apr. 1, 2013, which is a continuation of U.S. application Ser. No. 11/622,496, filed Jan. 12, 2007, now U.S. Pat. No. 8,421,195, which is a divisional of U.S. application Ser. No. 10/934,915, filed on Sep. 3, 2004, now abandoned, all of which are incorporated by reference.

FIELD OF INVENTION

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND OF INVENTION

Bipolar Junction transistors (BJT) are minority carrier devices as the principle device conduction mechanism. However, majority carriers also a small yet finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. Carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an 'aiding drift field', to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the 'uniformly doped epi region' in a IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in the case of an n-channel IGBT) require different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

'Retrograde' wells have been attempted, with little success, to help improve soft error immunity in SRAM's and visual quality in imaging circuits. FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3(b), 3(c), and

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3(d) illustrate device cross sections, as practiced today. 'Retrograde' and 'halo' wells have also been attempted to improve refresh time in DRAM's (dynamic random access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base, and collector, for the two most popular bipolar junction transistors: namely, A uniform base, and B graded base;

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3(a), 3(b), 3(c), 3(d) illustrate cross sections commonly used CMOS silicon substrate with two wells (one n-well in which p-channel transistors are subsequently fabricated, and, one p-well in which n-channel transistors are subsequently fabricated)—typical IC, EEPROM using tunnel insulator, DRAM and NAND flash;

FIG. 4 illustrates the cross section of a IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5(a), 5(b), 5(c) illustrate the cross sections of a MOS silicon substrate with two wells, and, an underlying layer using embodiments of the invention to improve performance in each application VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION OF THE INVENTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, where as the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complementary error function. The relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region - n' buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The 'average' base resistance is optimized, so that conductivity modulation and lifetime (for minority carriers) in base region are not compromised. By sweeping the carriers towards the n' buffer region two advantages are obtained—the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. More importantly, during t_{off} , holes can be recombined much quicker at the n' buffer layer, compared

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to a uniformly doped n⁺ epitaxial drift region by establishing a different dopant gradient near the n⁺ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Epitaxy enhances lifetime, but, epitaxy is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n⁺ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n⁺ buffer layer. This can improve t(on) and t(off) in the same device.

The following paragraph, beginning on page 5, line 6, and ending on page 11, line 28, is amended as indicated in the marked up version below:

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC's. These unwanted carriers can discharge dynamically-held 'actively held high' nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM's is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC's is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC's with the embodiments described here. Creating 'Sub Terrain' recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. In nonvolatile memory devices, to decrease programming time, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction field-effect transistors where the "channel pinchoff" is controlled by a graded channel instead of a uniformly doped channel (as practiced in prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface, to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single well, as well triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments, individually and collectively. Any modifications of such embodiments

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(described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said substrate to said surface layer; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said substrate to said surface layer.

2. The semiconductor device of claim 1 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.

3. The semiconductor device of claim 1 wherein the semiconductor device is a central processing unit (CPU).

4. The semiconductor device of claim 1 wherein the semiconductor device is a DRAM device.

5. The semiconductor device of claim 1 wherein the semiconductor device is a flash memory device.

6. The semiconductor device of claim 1 wherein the semiconductor device is an image sensor device.

7. A semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

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8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.

9. The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU). 5

10. The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device.

11. The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device. 10

12. The semiconductor device of claim 7 wherein the semiconductor device is an image sensor device.

* * * * *

EXHIBIT 3

US010510842B2

(12) **United States Patent**
Rao(10) **Patent No.: US 10,510,842 B2**(45) **Date of Patent: Dec. 17, 2019**(54) **SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS***H01L 29/7395* (2013.01); *H01L 27/0214*
(2013.01); *H01L 27/10844* (2013.01)(71) Applicant: **GREENTHREAD, LLC**, Dallas, TX
(US)(58) **Field of Classification Search**CPC *H01L 29/1095*USPC *257/655*

See application file for complete search history.

(72) Inventor: **G.R. Mohan Rao**, Allen, TX (US)(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX
(US)(56) **References Cited****U.S. PATENT DOCUMENTS**4,001,864 A 1 1977 Gibbons
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(Continued)(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.(21) Appl. No.: **15/590,282**(22) Filed: **May 9, 2017**(65) **Prior Publication Data**

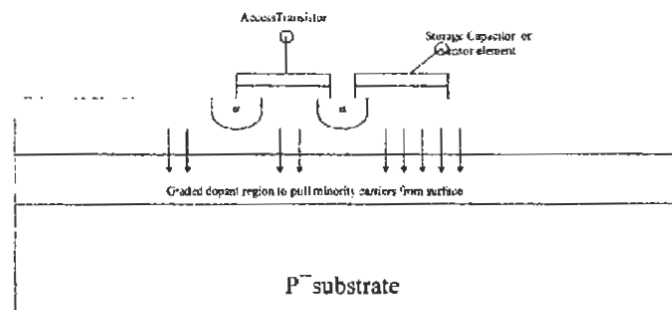
US 2017/0243876 A1 Aug. 24, 2017

Related U.S. Application Data(60) Continuation of application No. 14/931,636, filed on
Nov. 3, 2015, now Pat. No. 9,647,070, which is a
continuation of application No. 14/515,584, filed on
Oct. 16, 2014, now Pat. No. 9,190,502, which is a
continuation of application No. 13/854,319, filed on
(Continued)(51) **Int. Cl.***H01L 21/02* (2006.01)
H01L 29/10 (2006.01)
H01L 27/11524 (2017.01)
H01L 27/146 (2006.01)
H01L 27/11521 (2017.01)
H01L 29/739 (2006.01)
H01L 29/36 (2006.01)

(Continued)

(52) **U.S. Cl.**CPC *H01L 29/1095* (2013.01); *H01L 27/11521*
(2013.01); *H01L 27/11524* (2013.01); *H01L*
27/14643 (2013.01); *H01L 29/36* (2013.01);**OTHER PUBLICATIONS**P.D. Moor, Advanced CMOS-based pixel sensors, <https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEEimecPdM.pdf>, 2011, 41 pages.

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Primary Examiner Ajay Arora(74) *Attorney, Agent, or Firm* Bill R. Naifeh; Timothy
F. Bliss(57) **ABSTRACT**Most semiconductor devices manufactured today, have uni-
form dopant concentration, either in the lateral or vertical
device active (and isolation) regions. By grading the dopant
concentration, the performance in various semiconductor
devices can be significantly improved. Performance
improvements can be obtained in application specific areas
like increase in frequency of operation for digital logic,
various power MOSFET and IGBT ICs, improvement in
refresh time for DRAMs, decrease in programming time for
nonvolatile memory, better visual quality including pixel
resolution and color sensitivity for imaging ICs, better
sensitivity for varactors in tunable filters, higher drive capa-
bilities for JFETs, and a host of other applications.**18 Claims, 10 Drawing Sheets**CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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Related U.S. Application Data

Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

- (51) **Int. Cl.**
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

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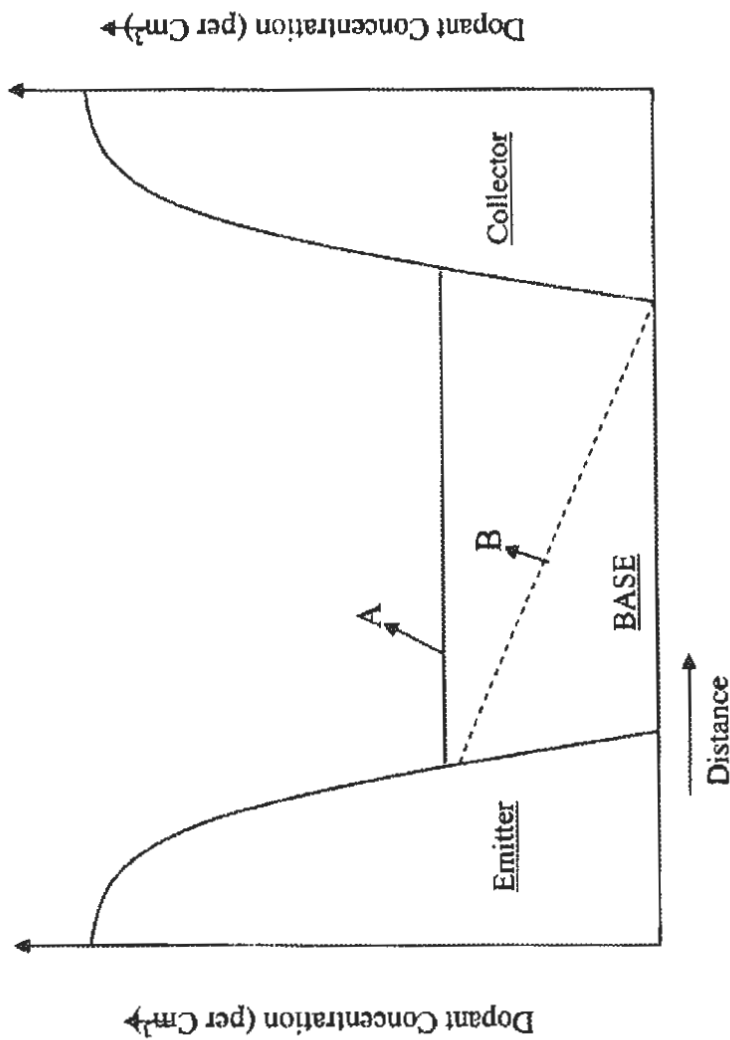


Figure 1 Prior Art

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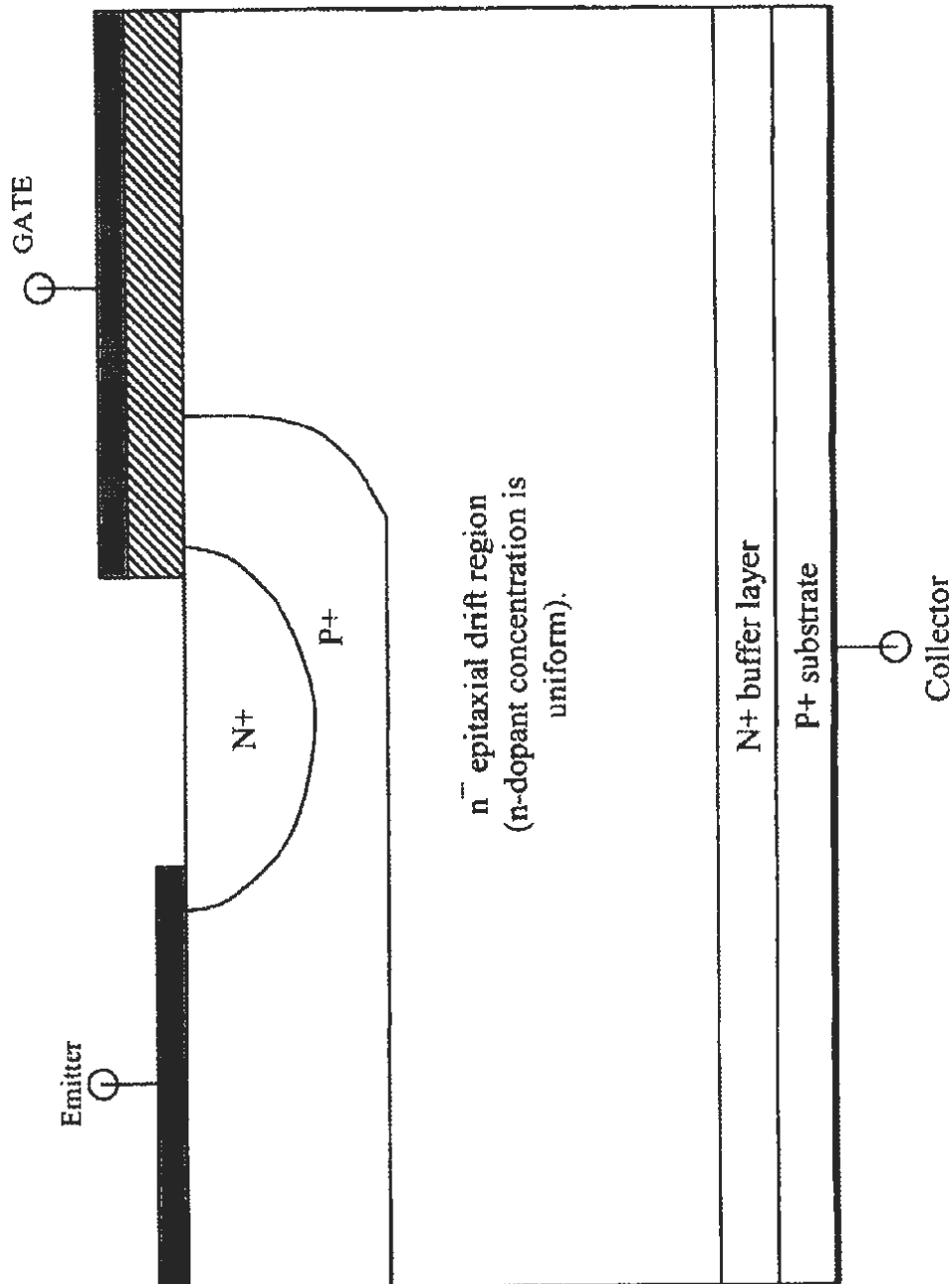


FIGURE 2 Prior art

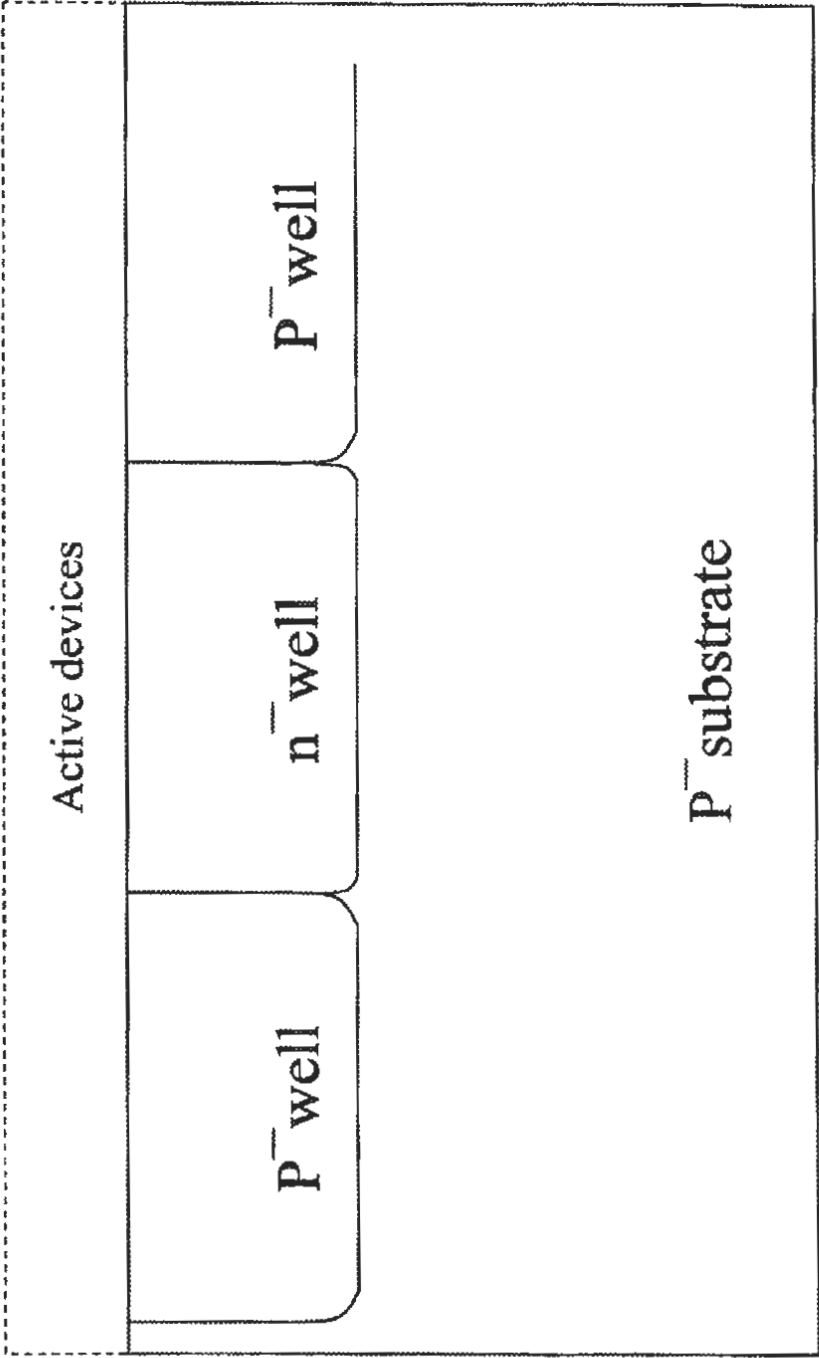


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

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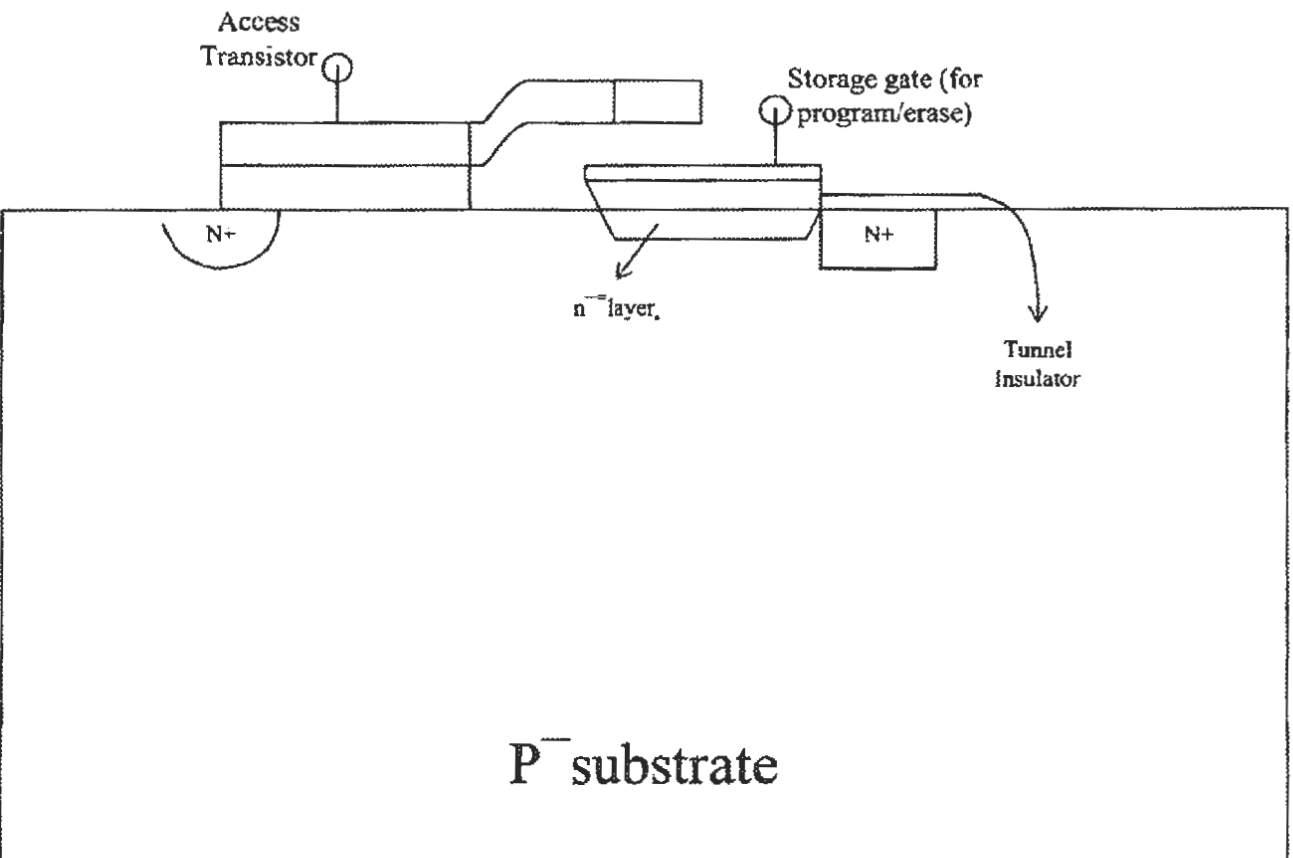


FIGURE 3B Prior art for a two-device EEPROM memory cell

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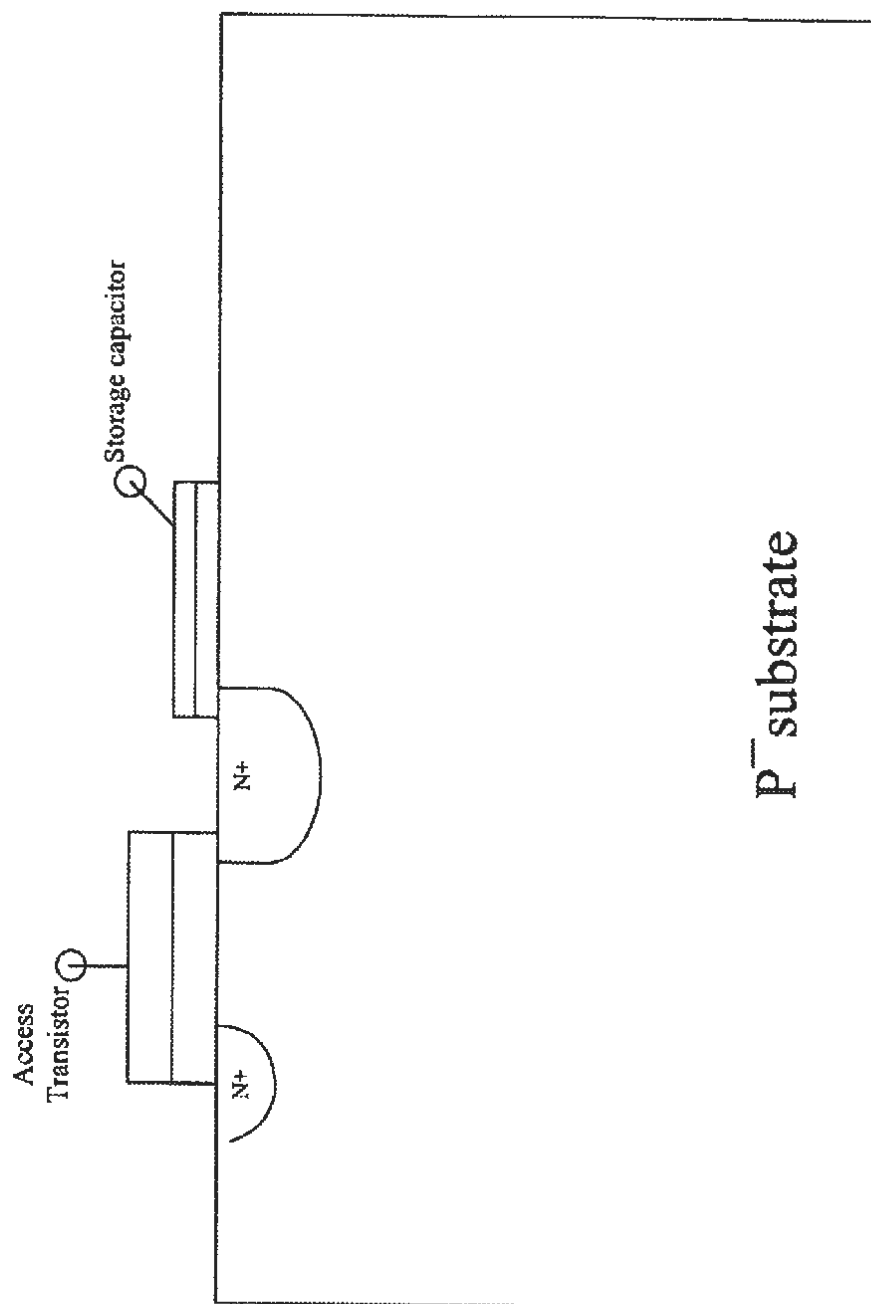


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

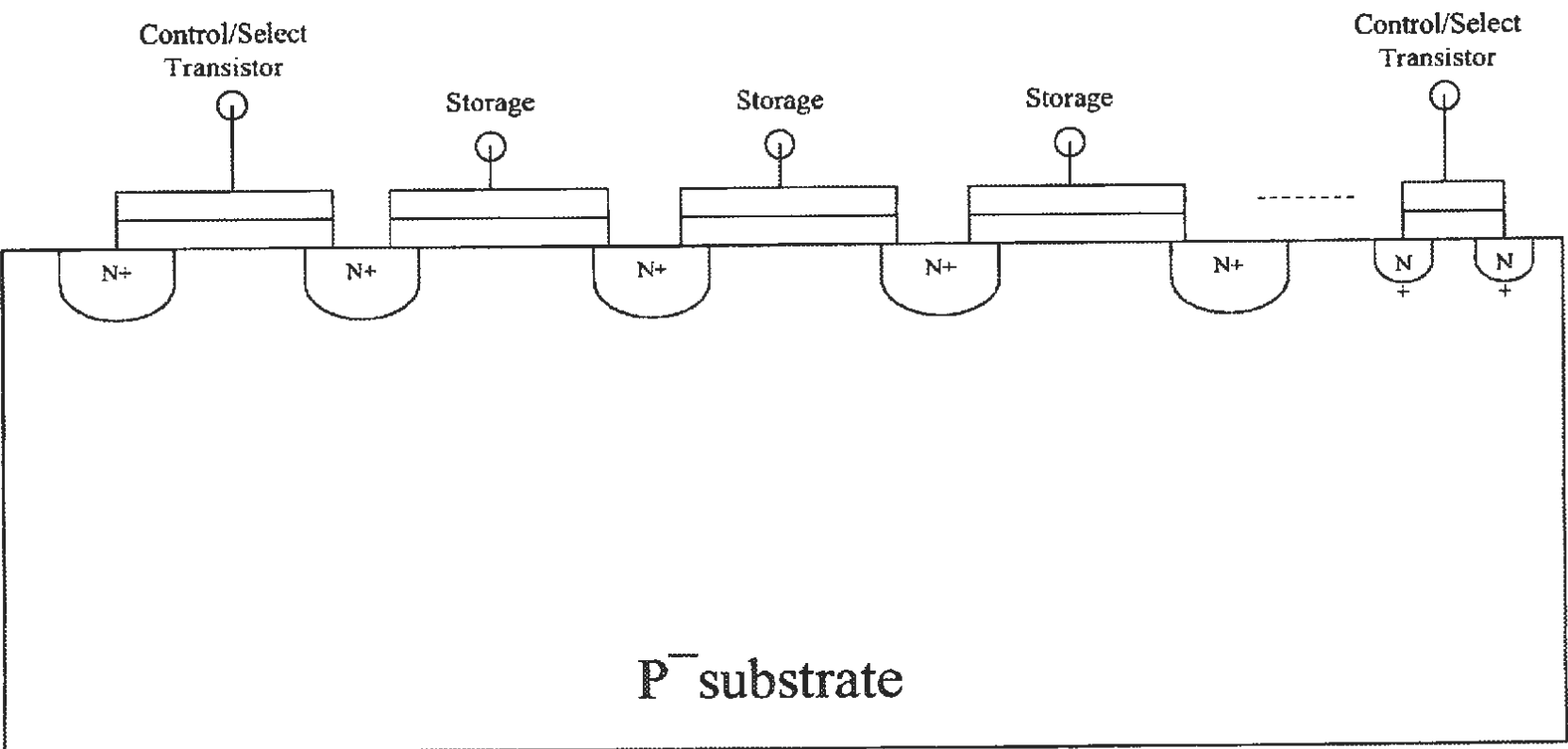


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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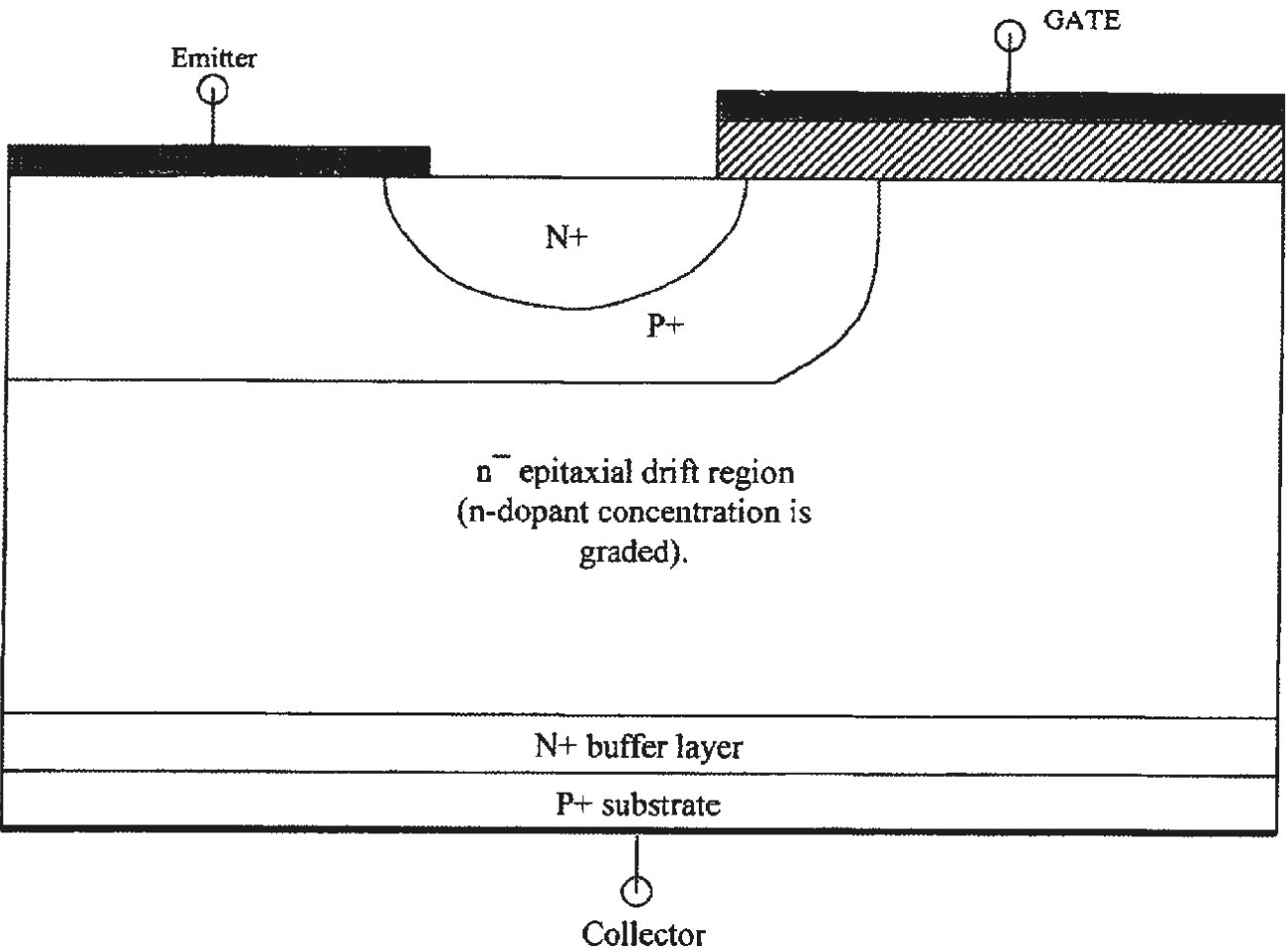


FIGURE 4 A dopant - concentration grinded drift region in a IGBT

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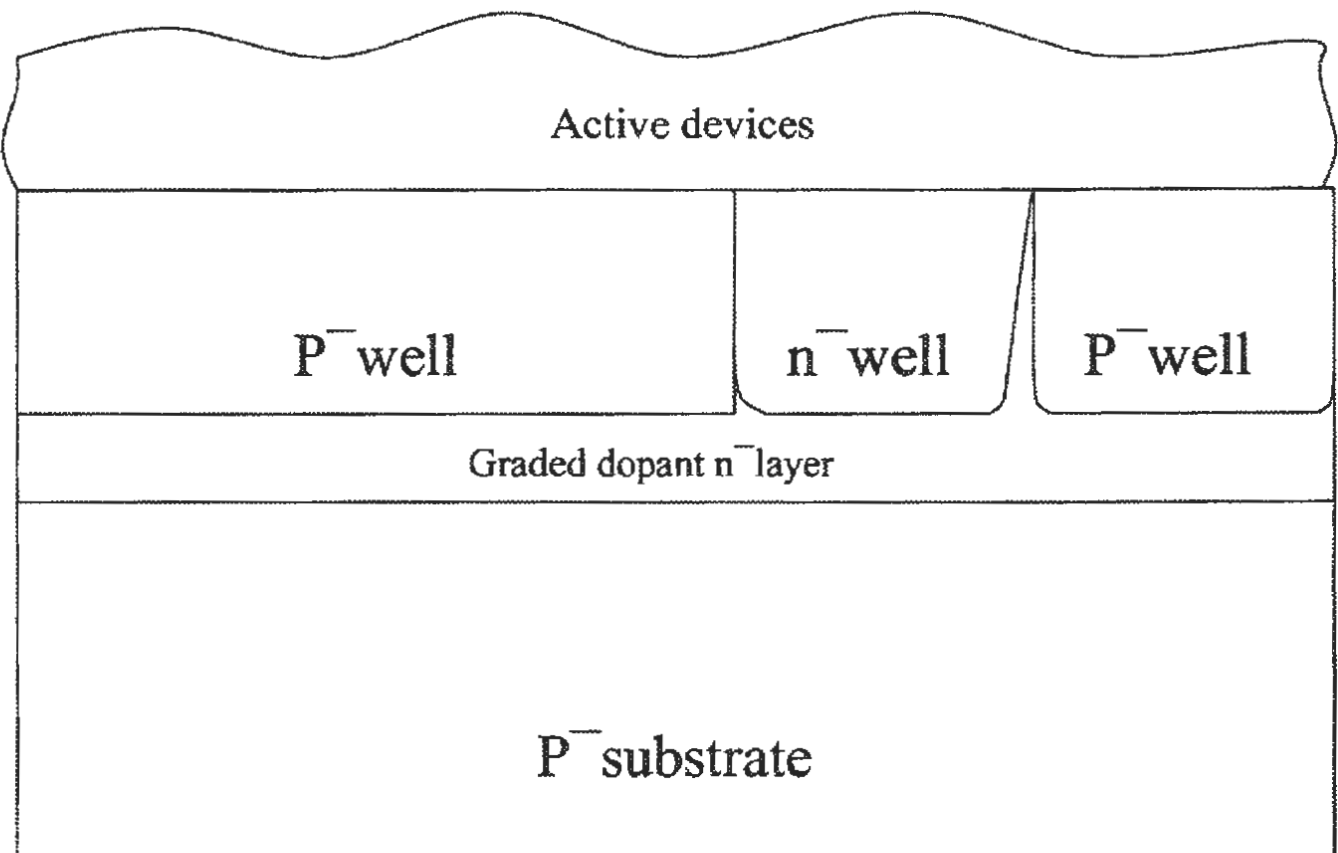


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

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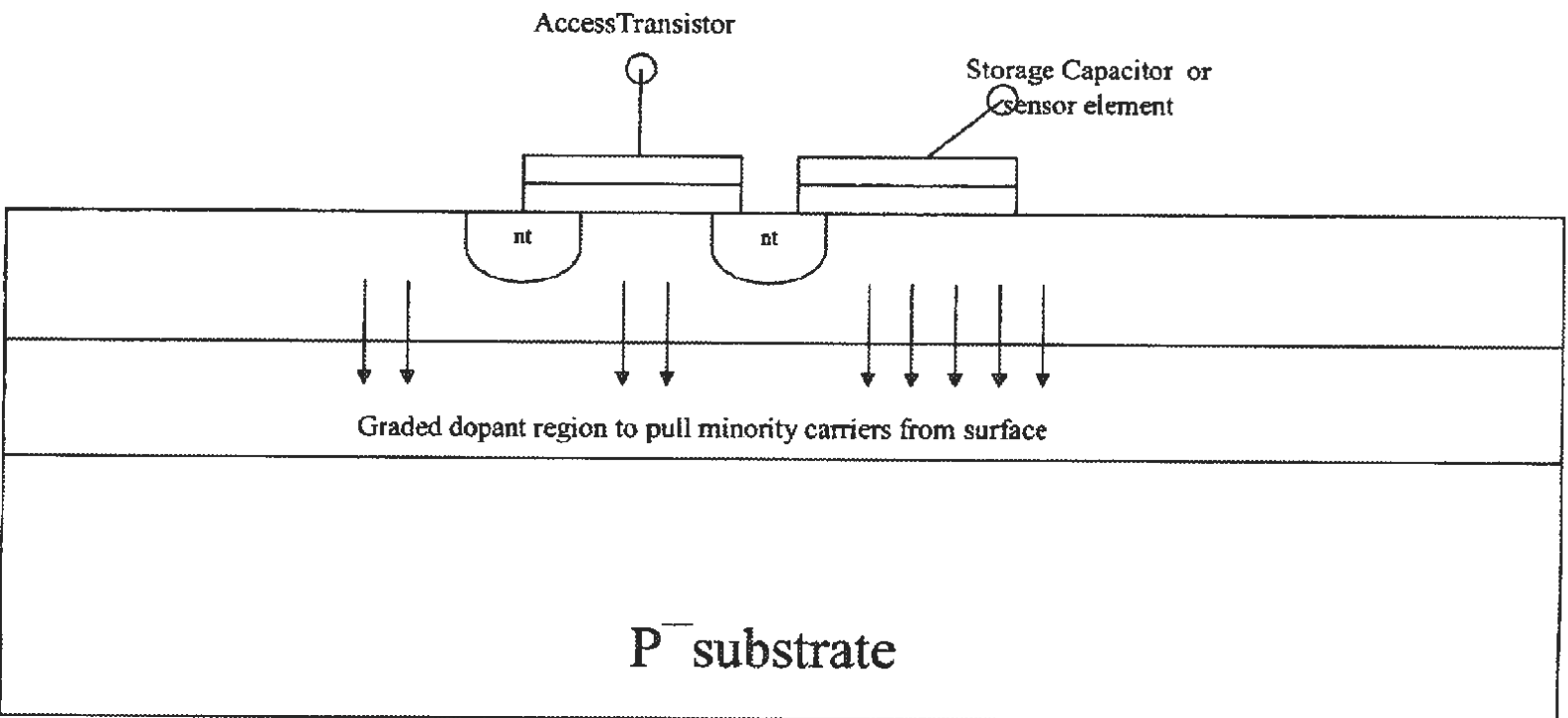


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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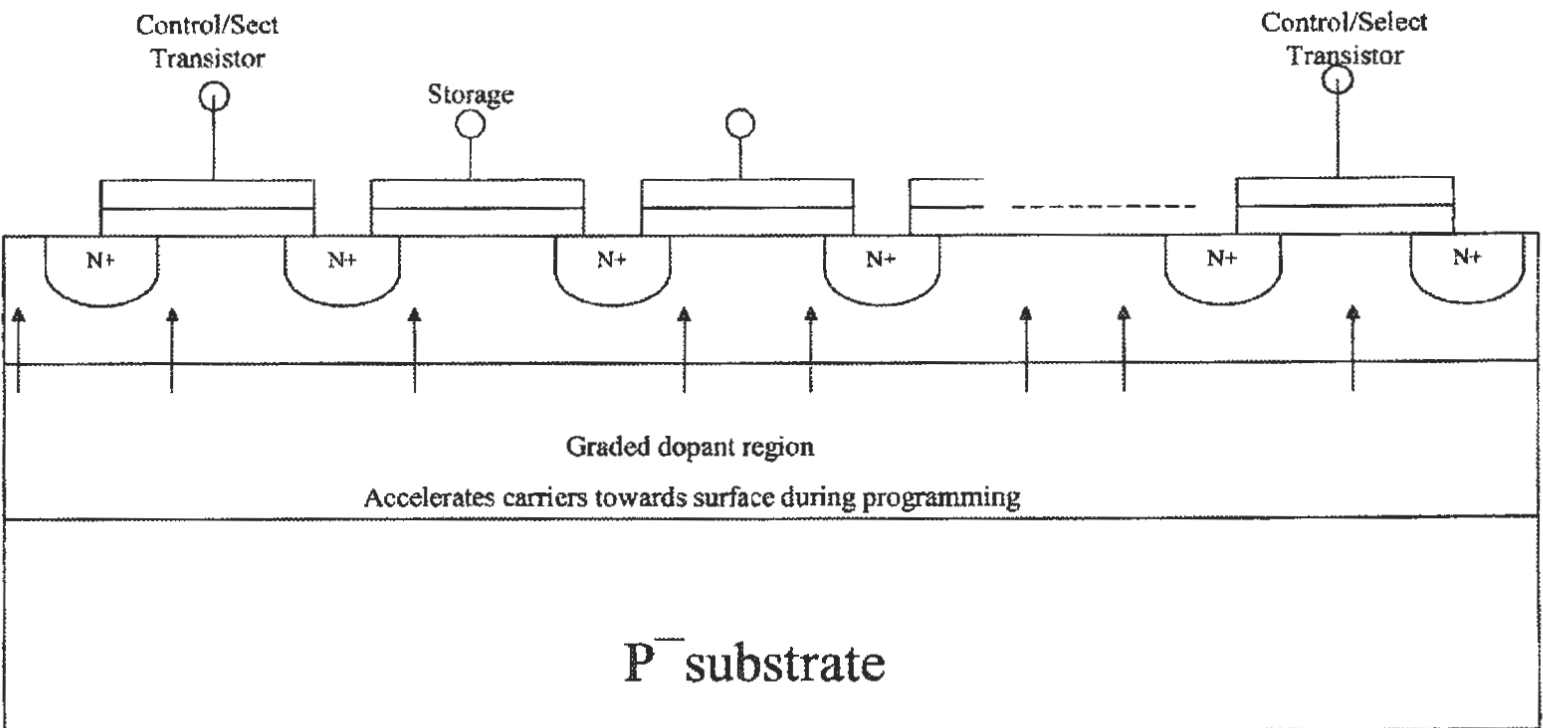


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, published on Jun. 16, 2016 as U.S. Publication No. 2016-0172447, now U.S. Pat. No. 9,647,070, issued on May 9, 2017. Application Ser. No. 14/931,636 is a continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, published on Feb. 5, 2015, as U.S. Publication No. 2015-0035004, now U.S. Pat. No. 9,190,502, issued on Nov. 17, 2015. Application Ser. No. 14/515,584 is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, published on Aug. 29, 2013, as U.S. Publication No. 2013-0221488. Application Ser. No. 13/854,319 is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, published on Jul. 12, 2007, as Publication No. 2007-0158790, now U.S. Pat. No. 8,421,195, issued on Apr. 16, 2013. Application Ser. No. 11/622,496 is a Division of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004, published on Mar. 9, 2006, as U.S. Publication No. 2006-0049464. U.S. Pat. Nos. 9,647,070, 9,190,502, and 8,421,195, and Patent Application Publication Nos. 2016-0172447, 2015-0035004, 2013-0221488, 2007-0158790, and 2006-0049464, are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped "drift epitaxial" region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epitaxial region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the

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sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁺ well in which p-channel transistors are subsequently fabricated and one p⁺ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application: VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction

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(1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The "average" base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^+ epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held "actively held high" nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating "subterranean" recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^+ layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer

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bonding or similar "transfer" mechanisms. This n^+ layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^+ well and p^+ wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the "channel pinch-off" is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

3. The semiconductor device of claim 1, wherein the substrate is an n-type substrate.

4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

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5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.

6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.

7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

9. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.

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10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.

11. The semiconductor device of claim 9, wherein the substrate is an n-type substrate.

12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.

15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.

16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.

17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.

* * * * *

EXHIBIT 4

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Rao

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(45) **Date of Patent: Aug. 4, 2020**

(54) **SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS**

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(2013.01); *H01L 27/10844* (2013.01)

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(58) **Field of Classification Search**
CPC *H01L 29/1095*
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See application file for complete search history.

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(73) Assignee: **Greenthread, LLC**, Dallas, TX (US)

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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(60) Continuation of application No. 15/590,282, filed on
May 9, 2017, now Pat. No. 10,510,842, which is a
continuation of application No. 14/931,636, filed on
Nov. 3, 2015, now Pat. No. 9,647,070, which is a
continuation of application No. 14/515,584, filed on
(Continued)

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(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

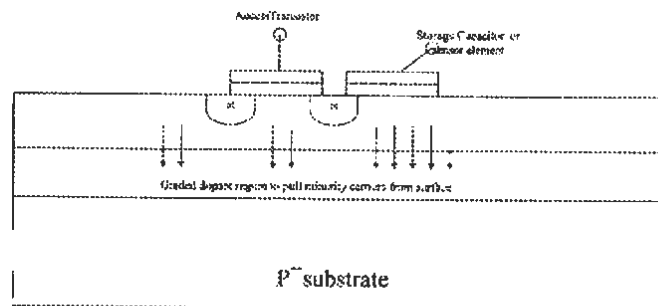
(51) **Int. Cl.**

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H01L 29/10 (2006.01)
H01L 29/36 (2006.01)
H01L 29/739 (2006.01)
H01L 27/146 (2006.01)
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27/14643 (2013.01); *H01L 29/36* (2013.01);

36 Claims, 10 Drawing Sheets



CMOS Substrate for a DRAM or Image sensor, with one embodiment of the invention

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Related U.S. Application Data

Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

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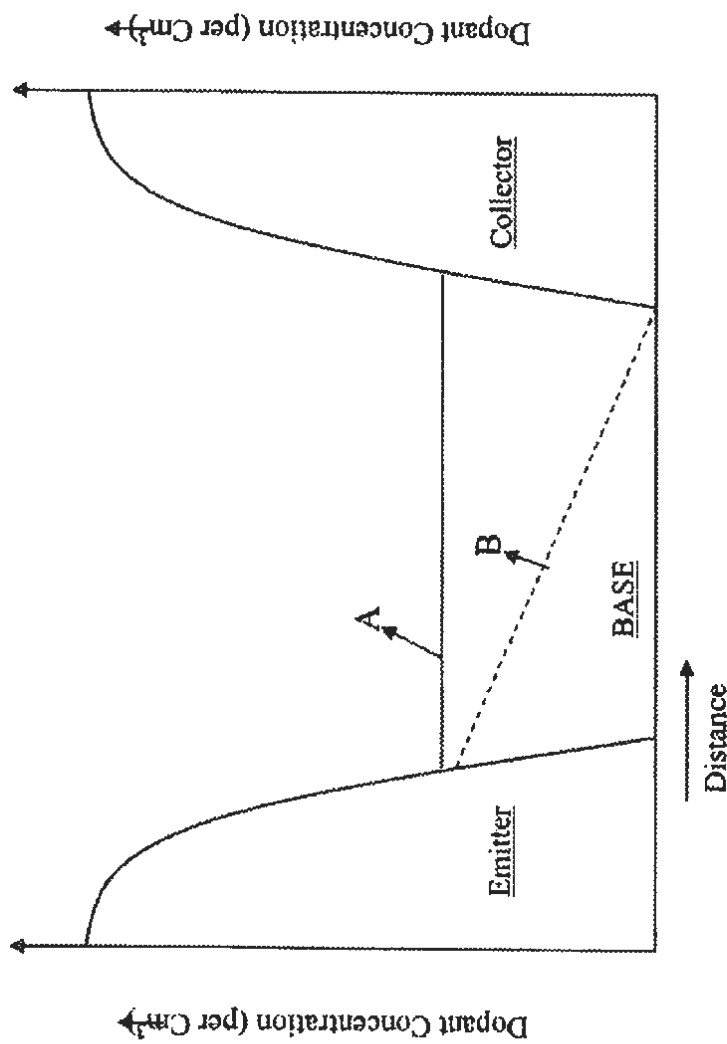


Figure 1 Prior Art

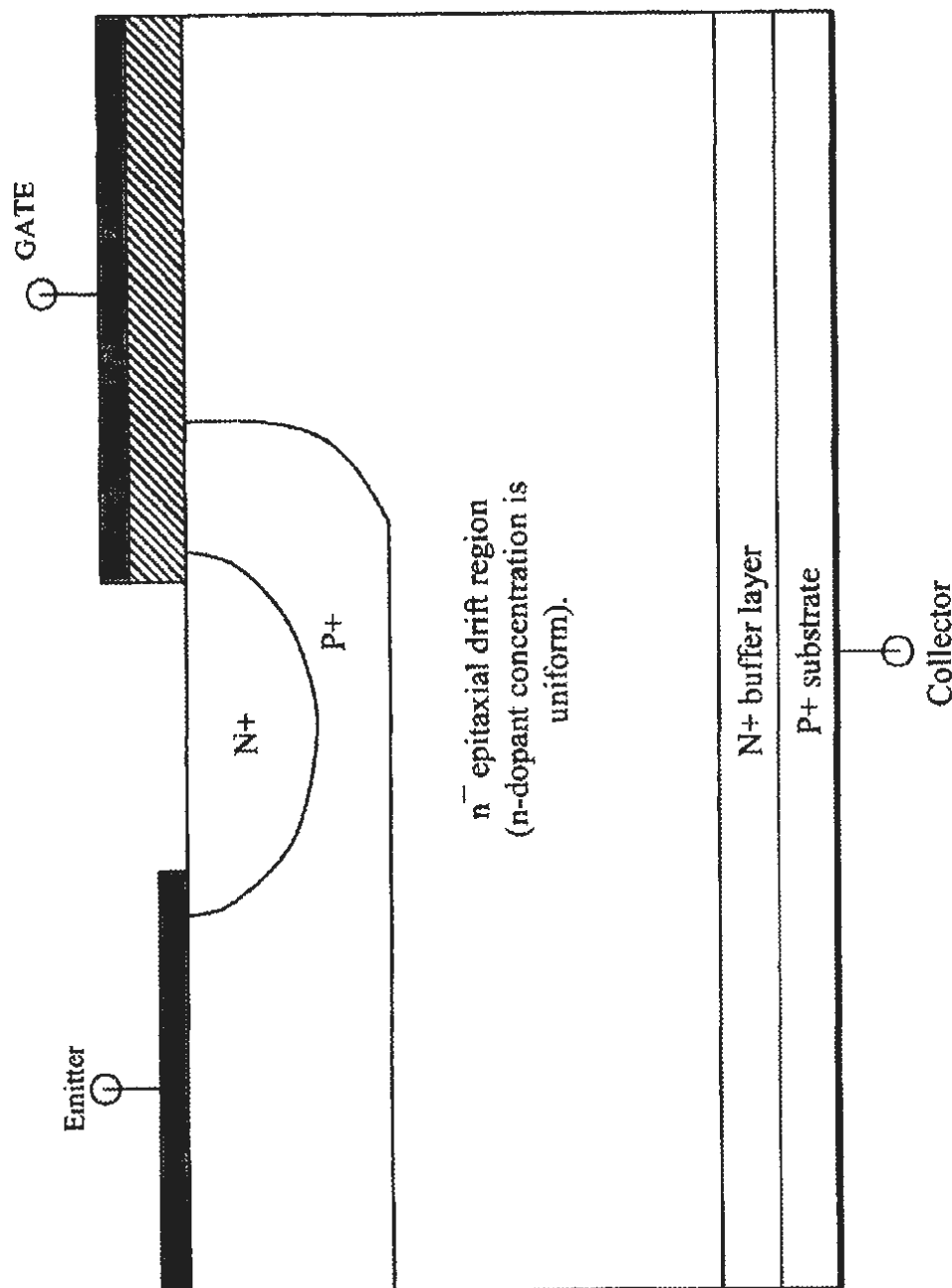


FIGURE 2 Prior art

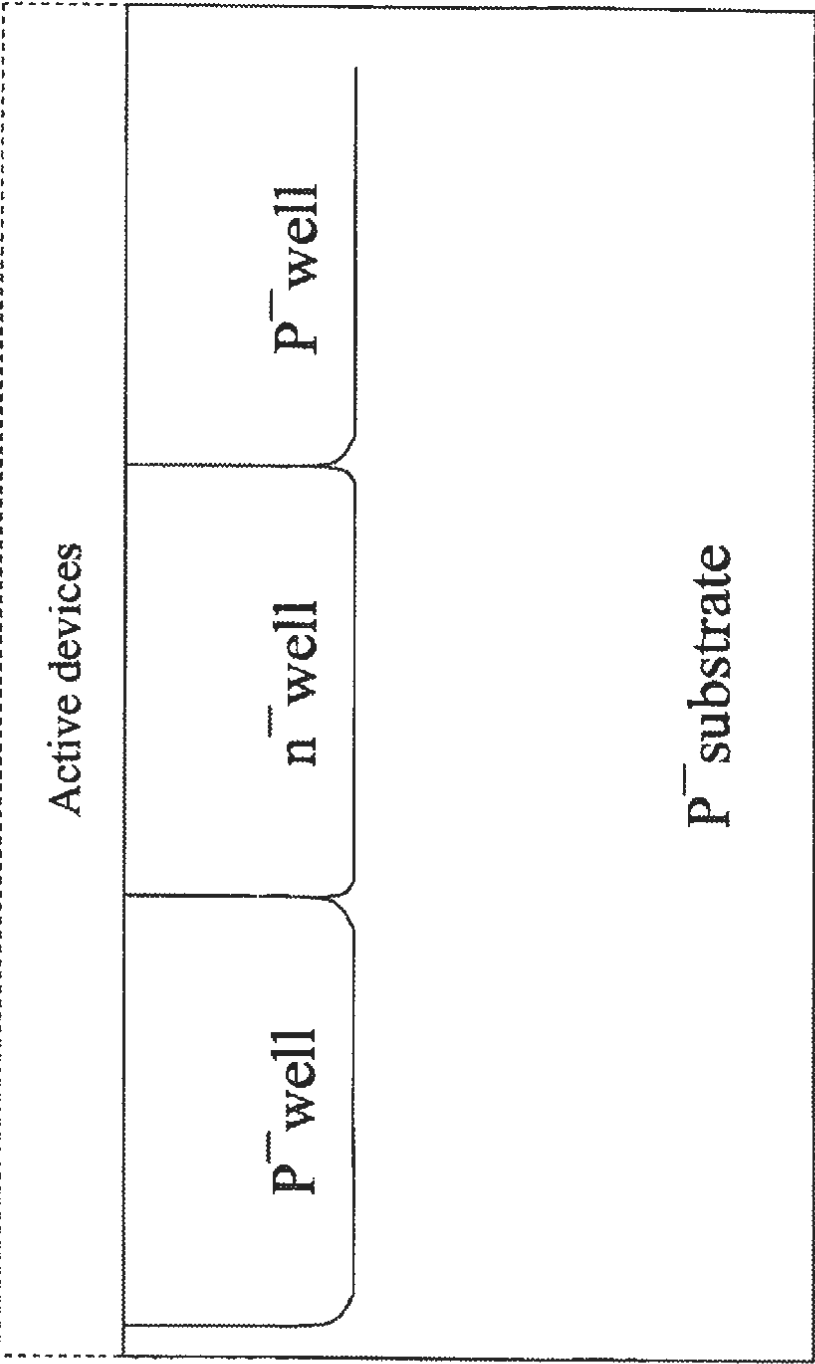


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

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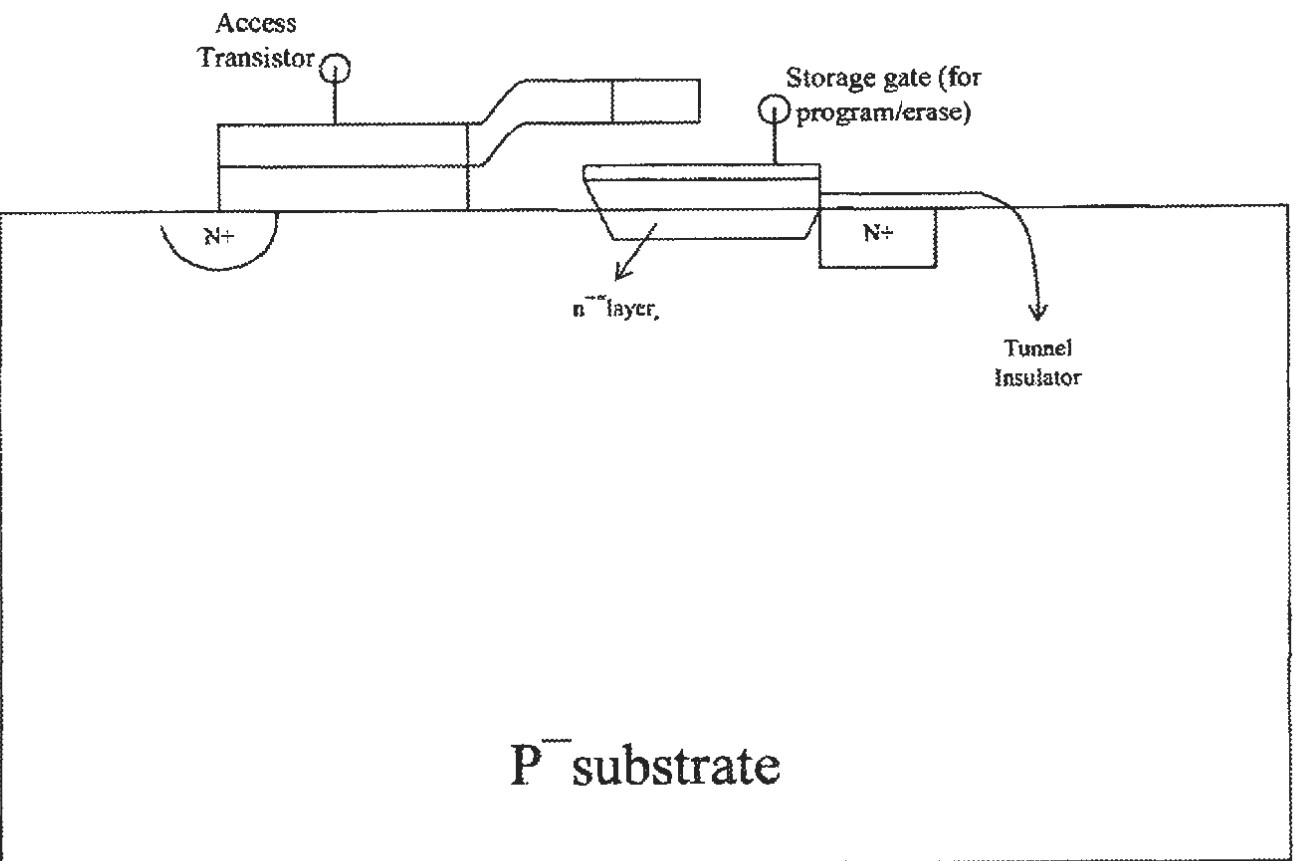


FIGURE 3B Prior art for a two-device EEPROM memory cell

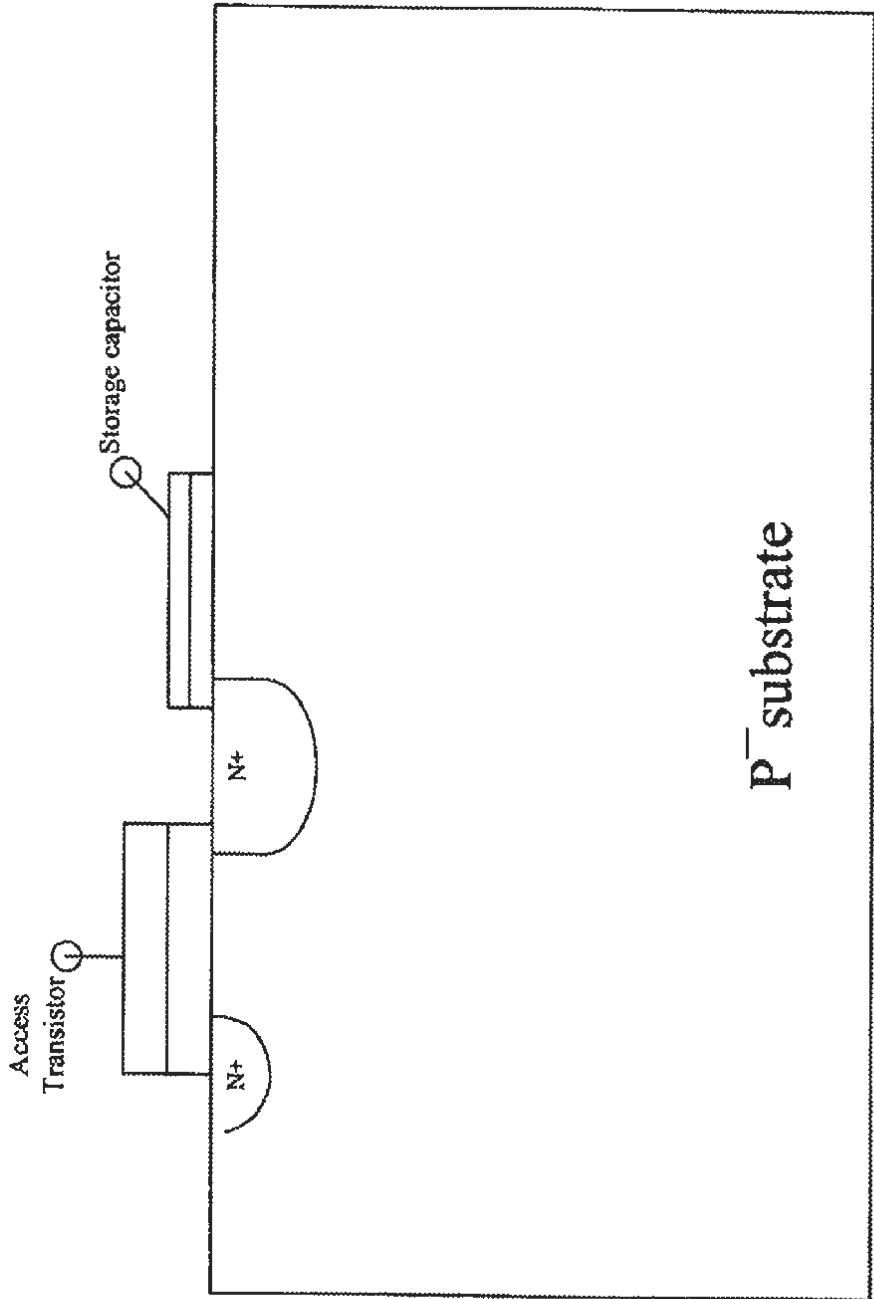


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

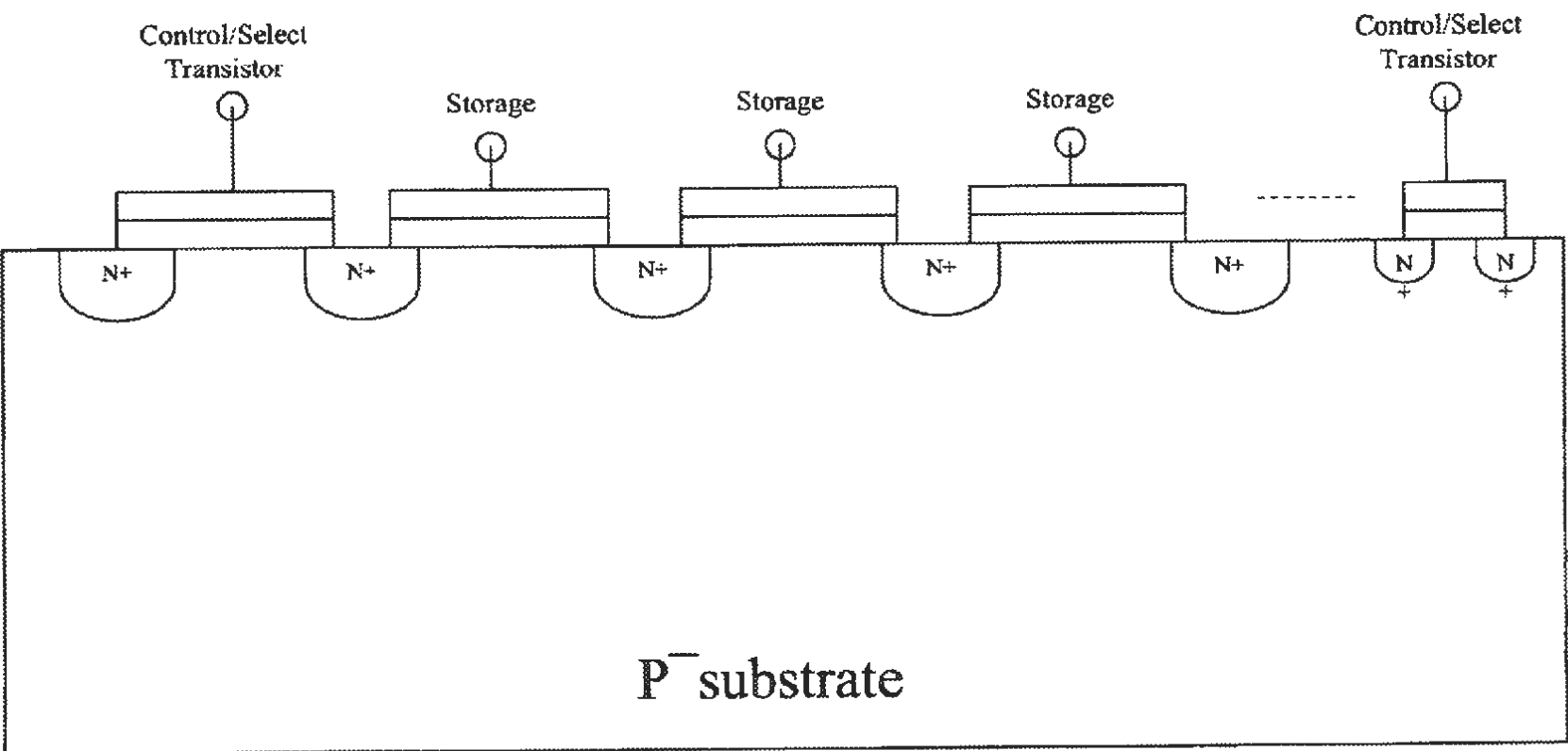


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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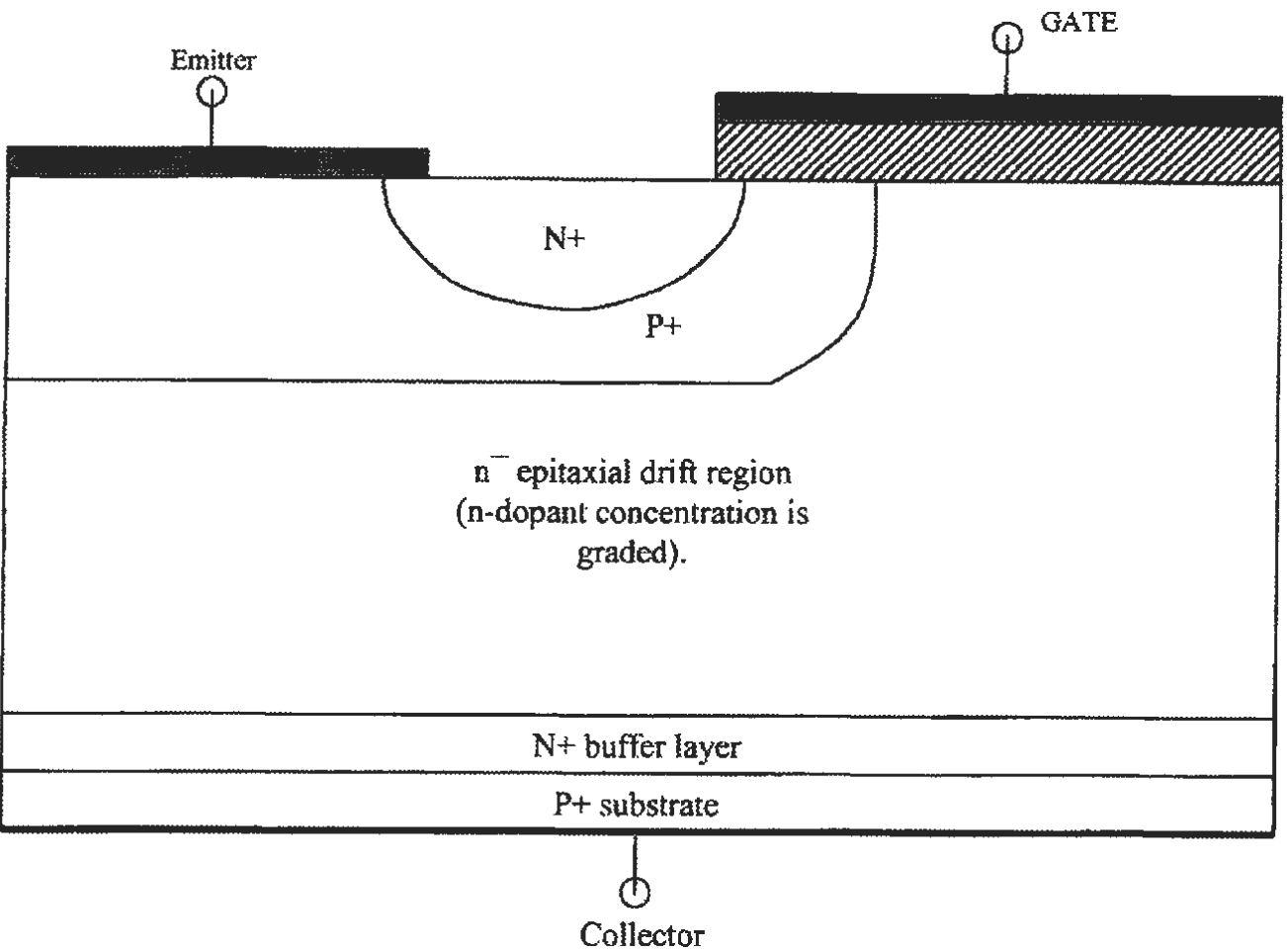


FIGURE 4 A dopant - concentration grinded drift region in a IGBT

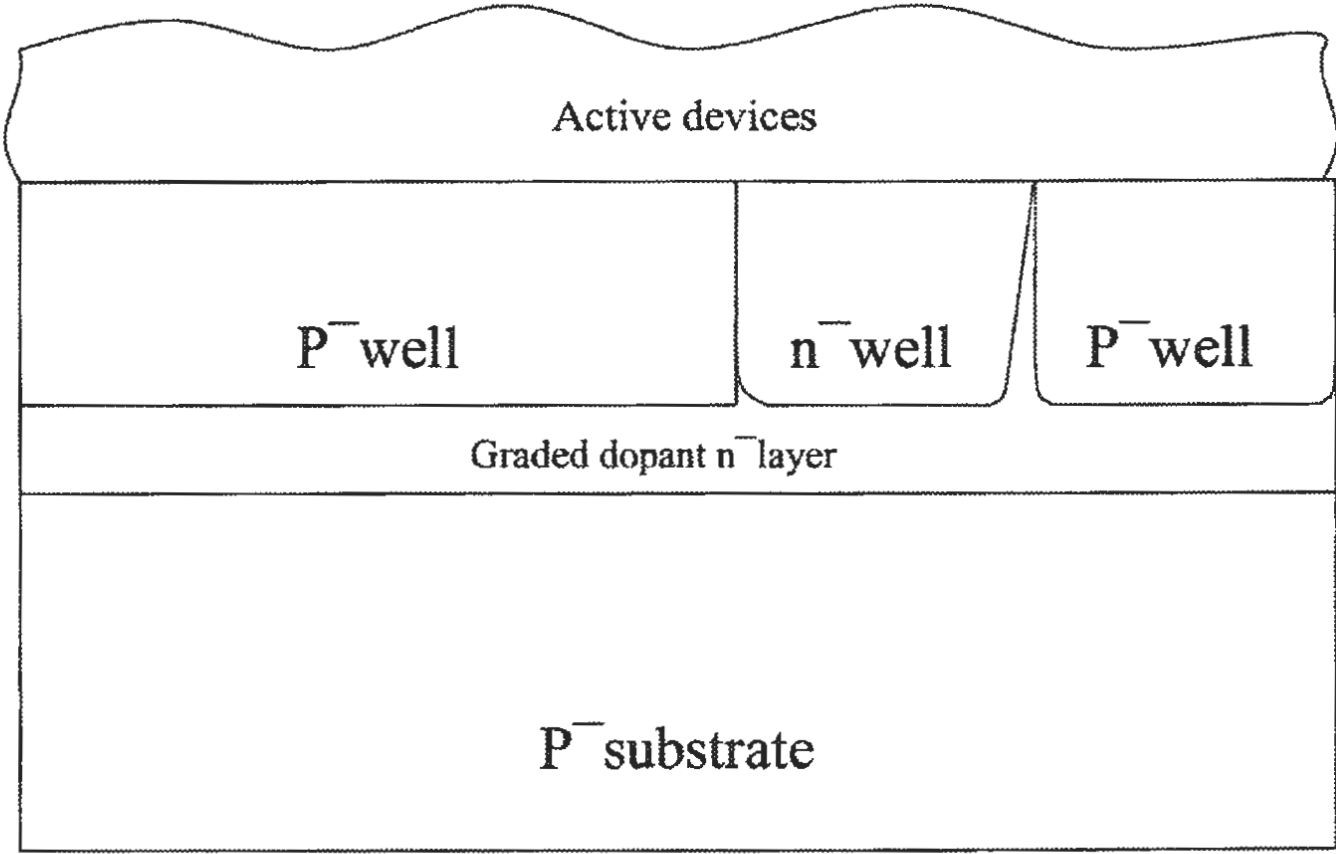


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

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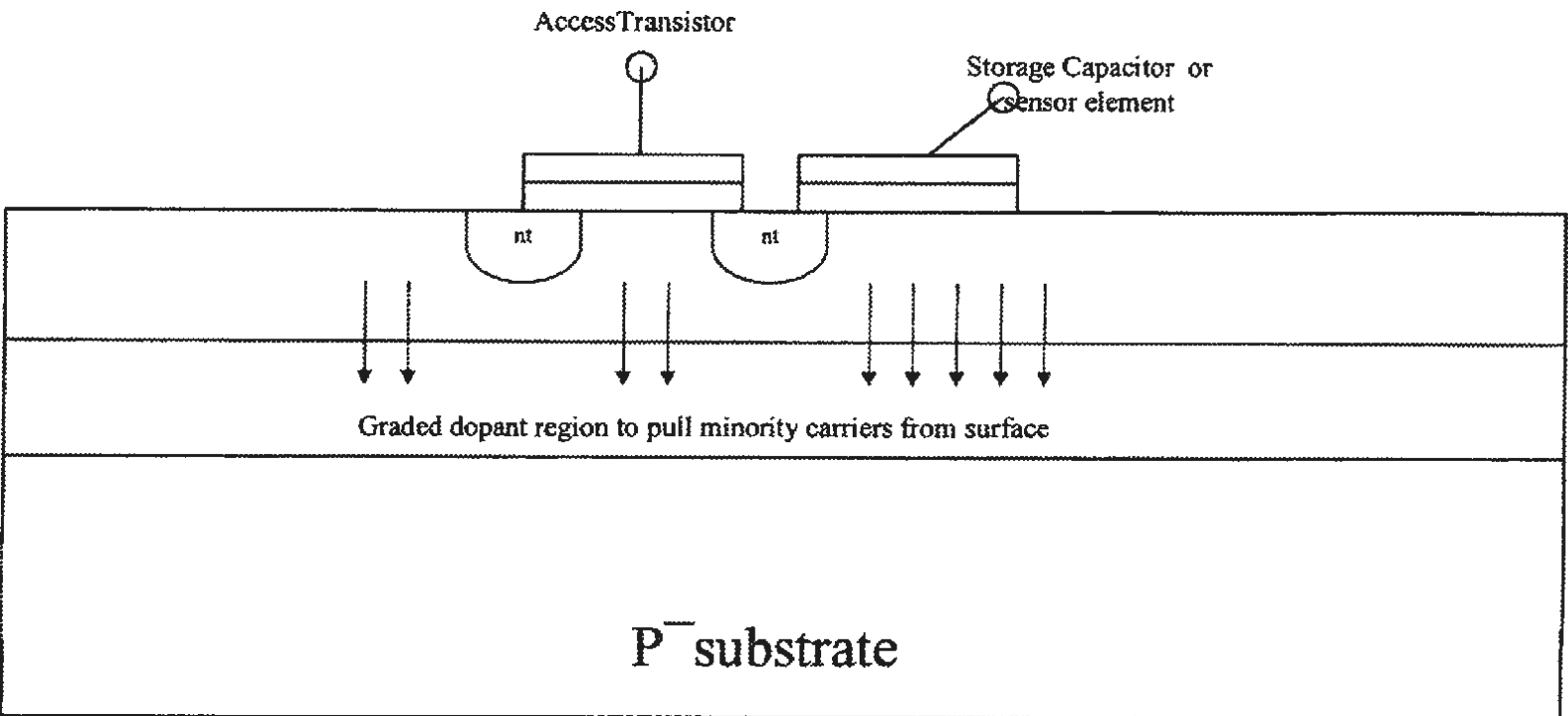


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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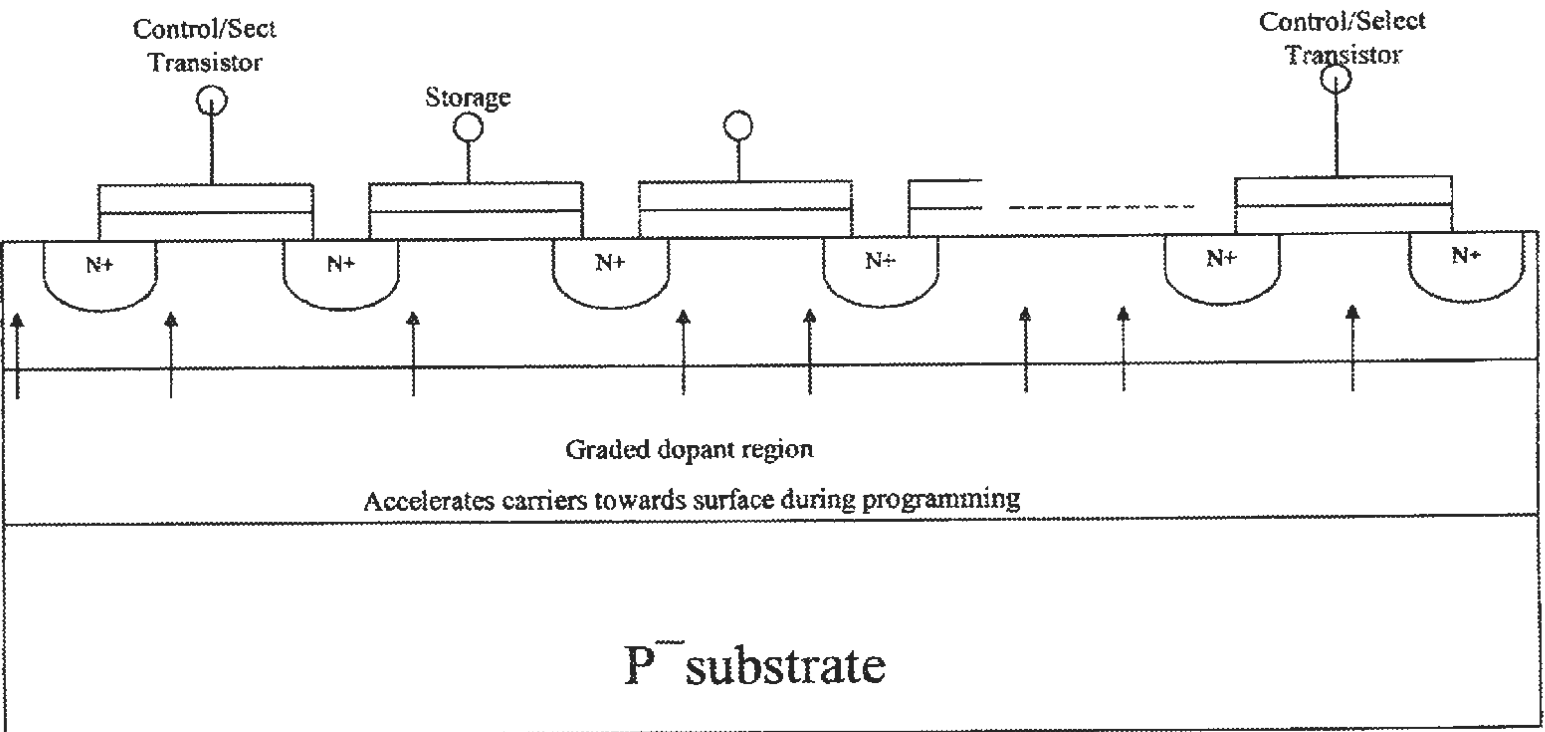


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

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This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi

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region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁻ well in which p-channel transistors are subsequently fabricated and one p⁻ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10¹⁸ to 10²⁰/cm³, whereas the base

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region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The "average" base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI): VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held "actively held high" nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating "subterranean" recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as

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possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the "channel pinch-off" is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device, comprising:

- a substrate of a first doping type at a first doping level having first and second surfaces;
- a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
- a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
- transistors formed in at least one of the first active region or second active region;
- at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and
- at least one well region adjacent to the first or second active region containing at least one graded dopant

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region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.

5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

10. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

11. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

12. The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.

14. The semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The semiconductor device of claim 1, wherein the device is a flash memory.

17. The semiconductor device of claim 1, wherein the device is a logic device.

18. The semiconductor device of claim 17, wherein the device is central processing unit.

19. The semiconductor device of claim 1, wherein the device is an image sensor.

20. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

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a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

21. The semiconductor device of claim 20, wherein the substrate is an n-type substrate.

22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.

23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.

27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

28. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

29. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

30. The semiconductor device of claim 20, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.

32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

33. The semiconductor device of claim 20, wherein the device is a flash memory.

34. The semiconductor device of claim 20, wherein the device is a logic device.

35. The semiconductor device of claim 34, wherein the device is central processing unit.

36. The semiconductor device of claim 20, wherein the device is an image sensor.

* * * * *

EXHIBIT 5

(12) **United States Patent**
Rao

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(45) **Date of Patent:** **Sep. 14, 2021**

(54) **SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS**

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(58) **Field of Classification Search**
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(Continued)

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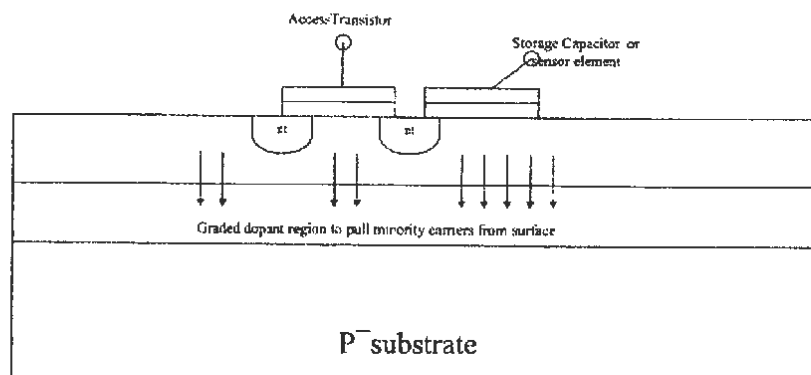
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(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

44 Claims, 10 Drawing Sheets



CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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Related U.S. Application Data

continuation of application No. 15/590,282, filed on May 9, 2017, now Pat. No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

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 IPR2020-00292—Exhibit 2012—Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 53-1 (Mar. 18, 2020).
 IPR2020-00292—Patent Owner Preliminary Response.

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U.S. Patent

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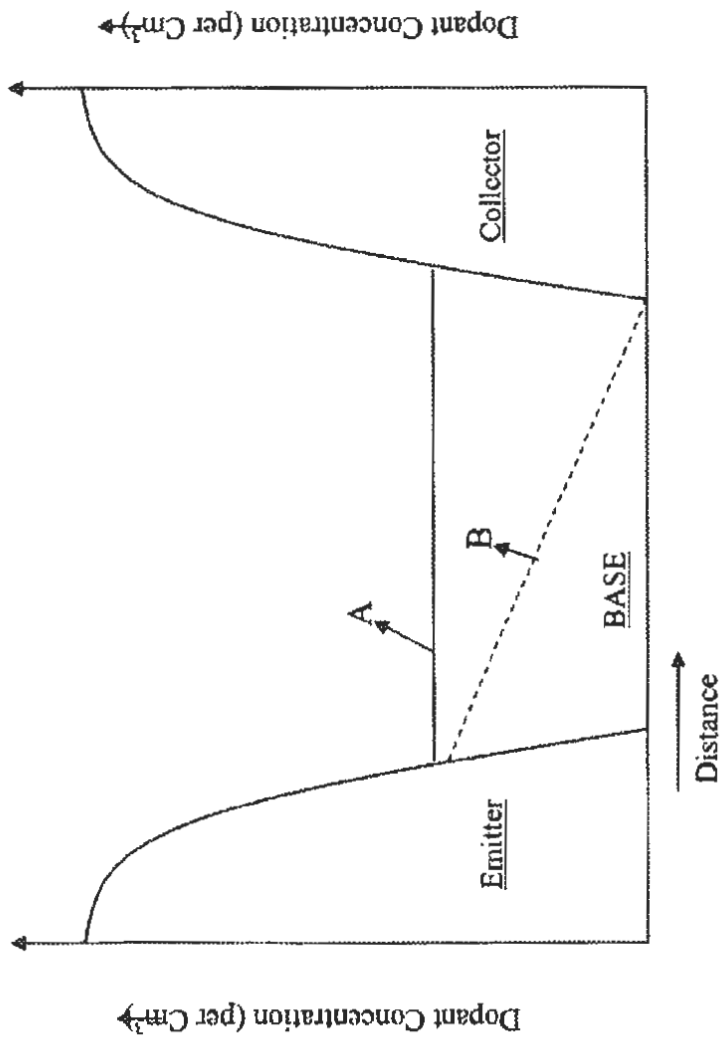


Figure 1 Prior Art

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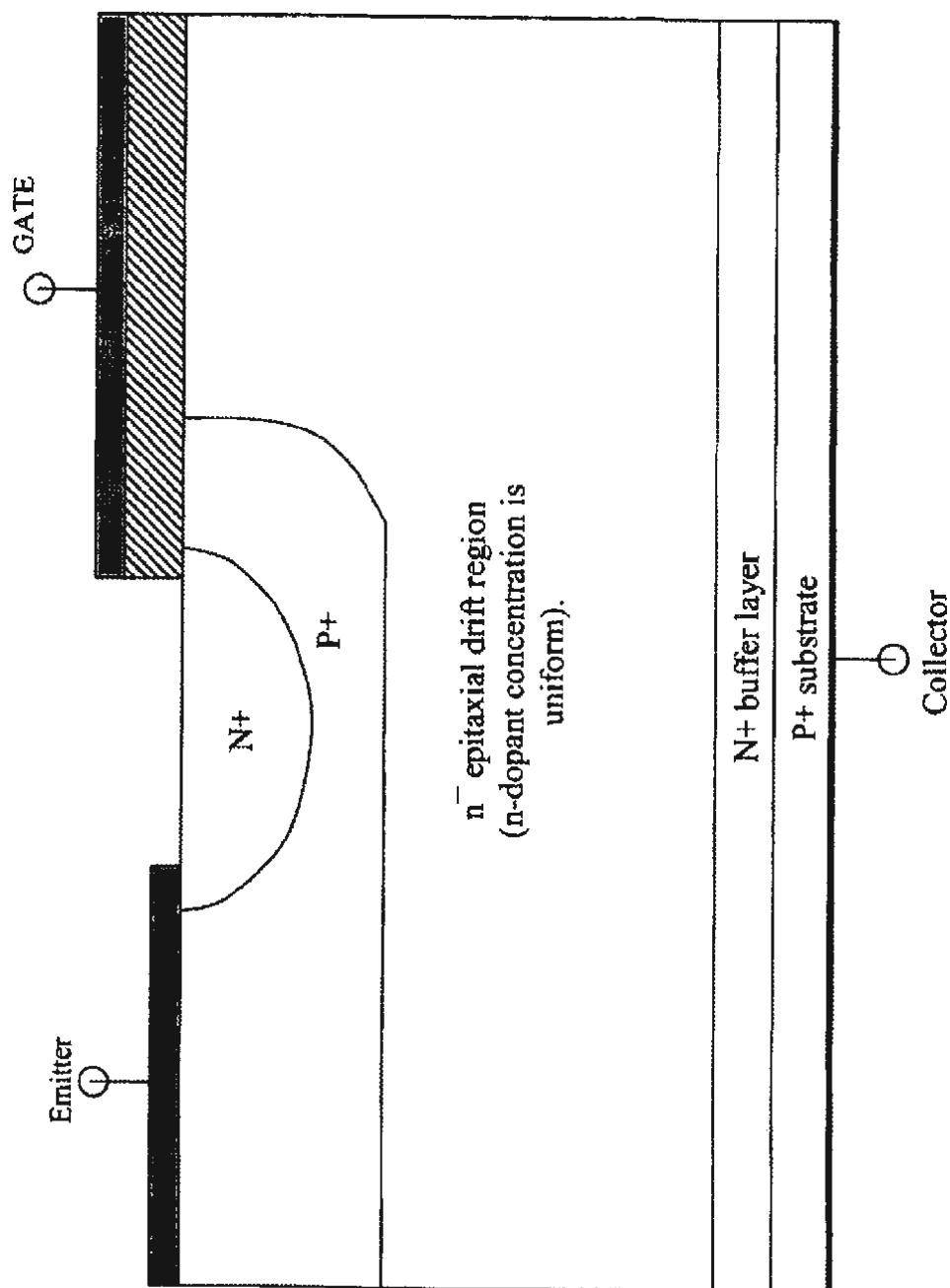


FIGURE 2 Prior art

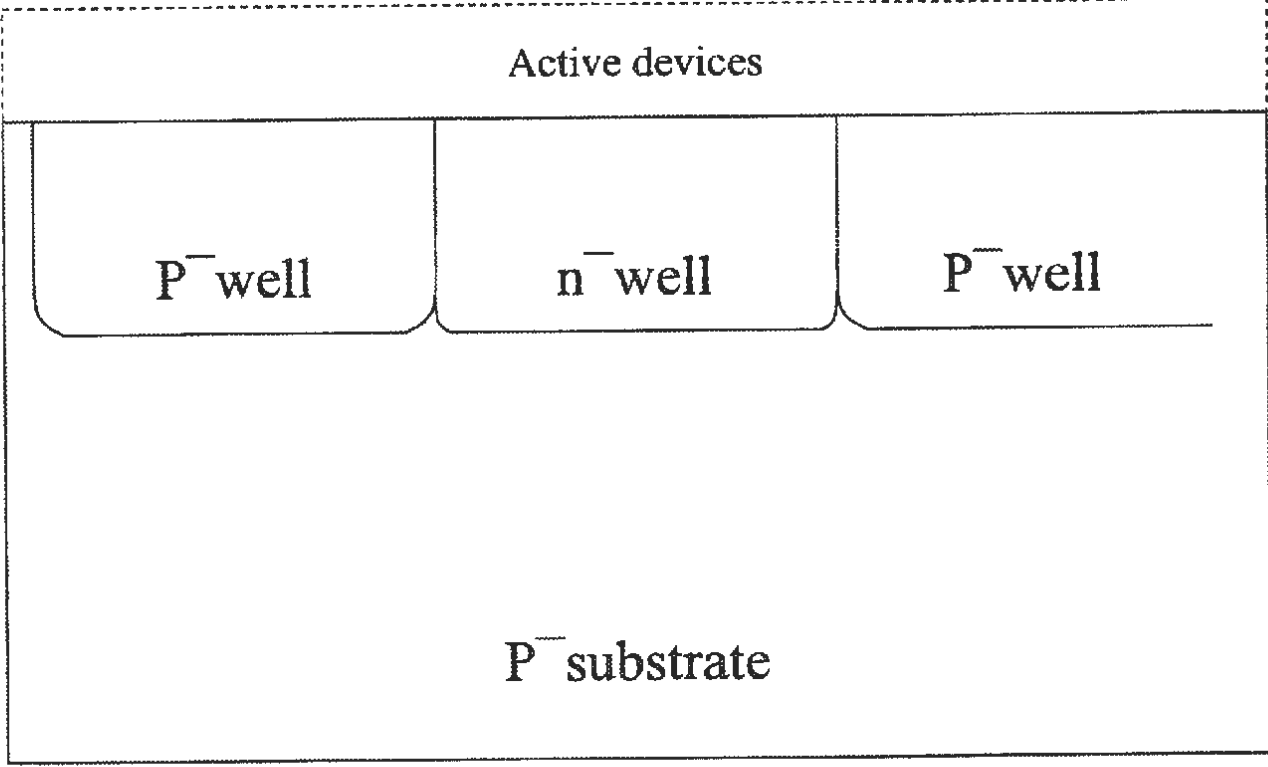


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

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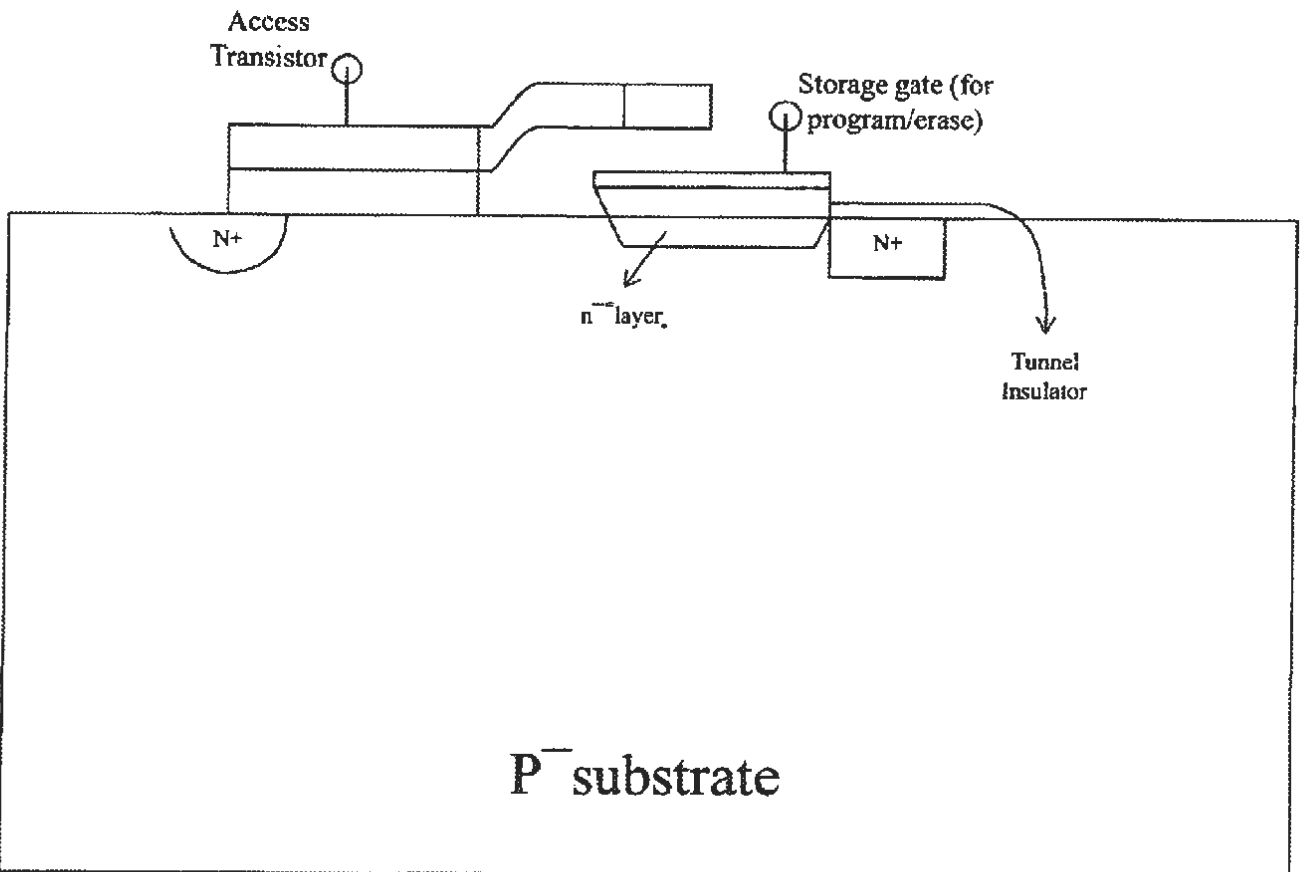


FIGURE 3B Prior art for a two-device EEPROM memory cell

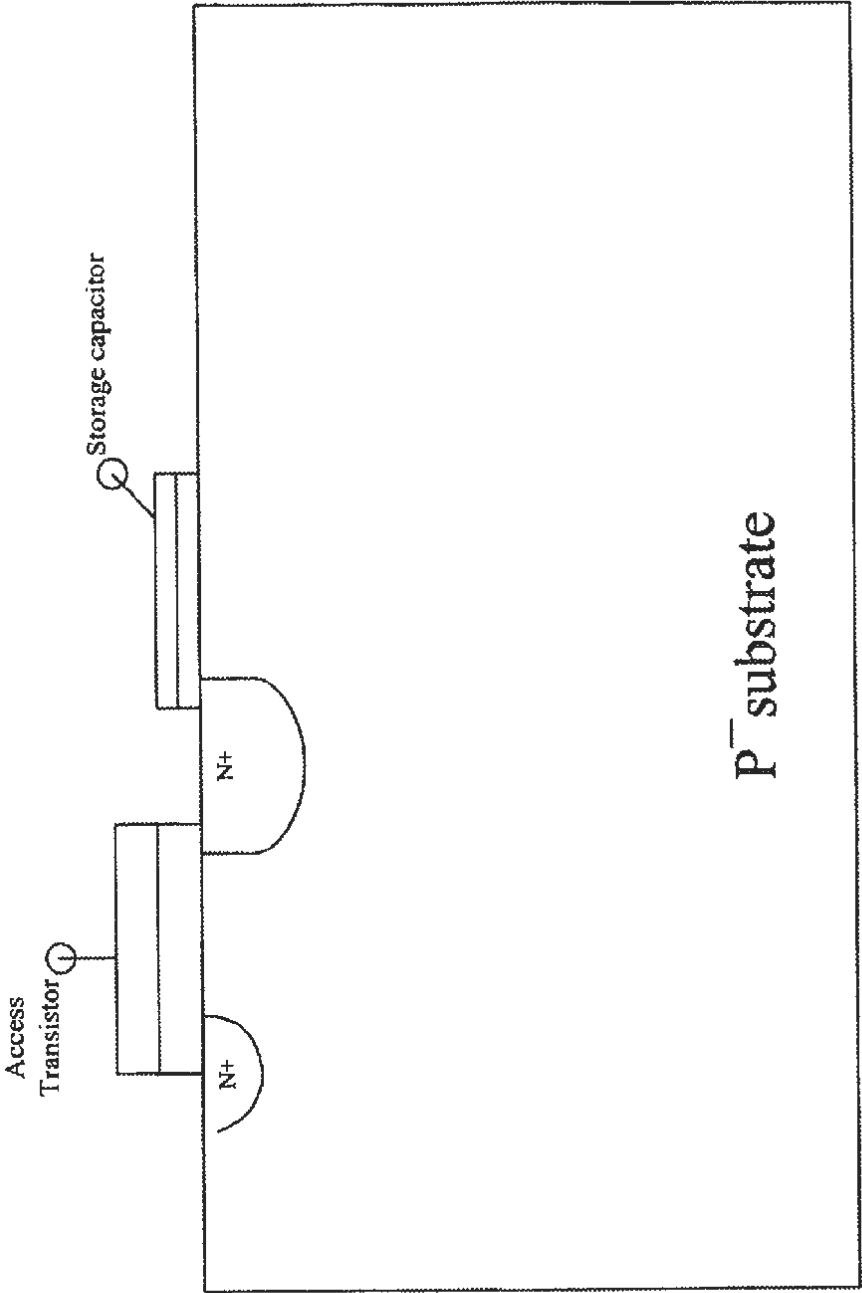


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

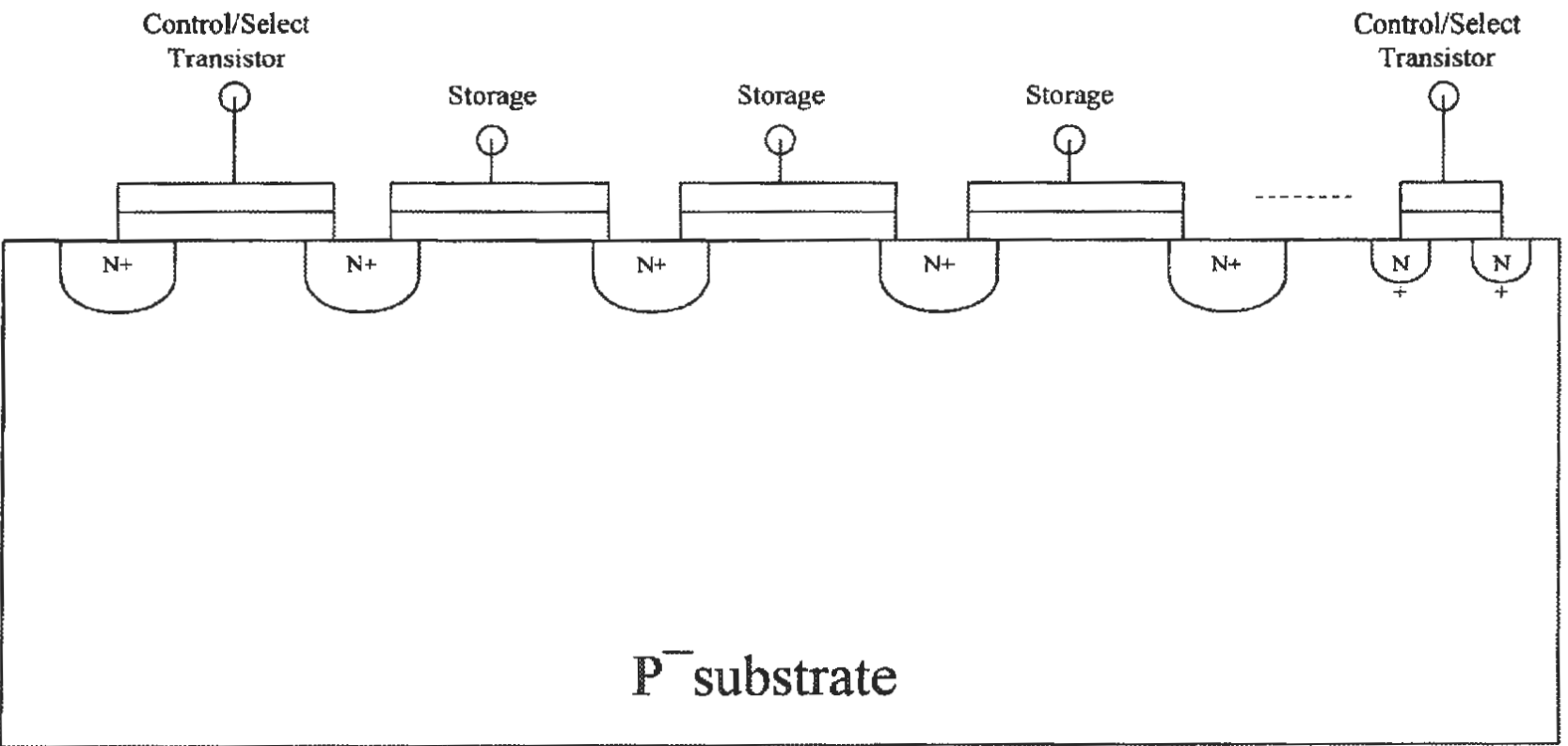


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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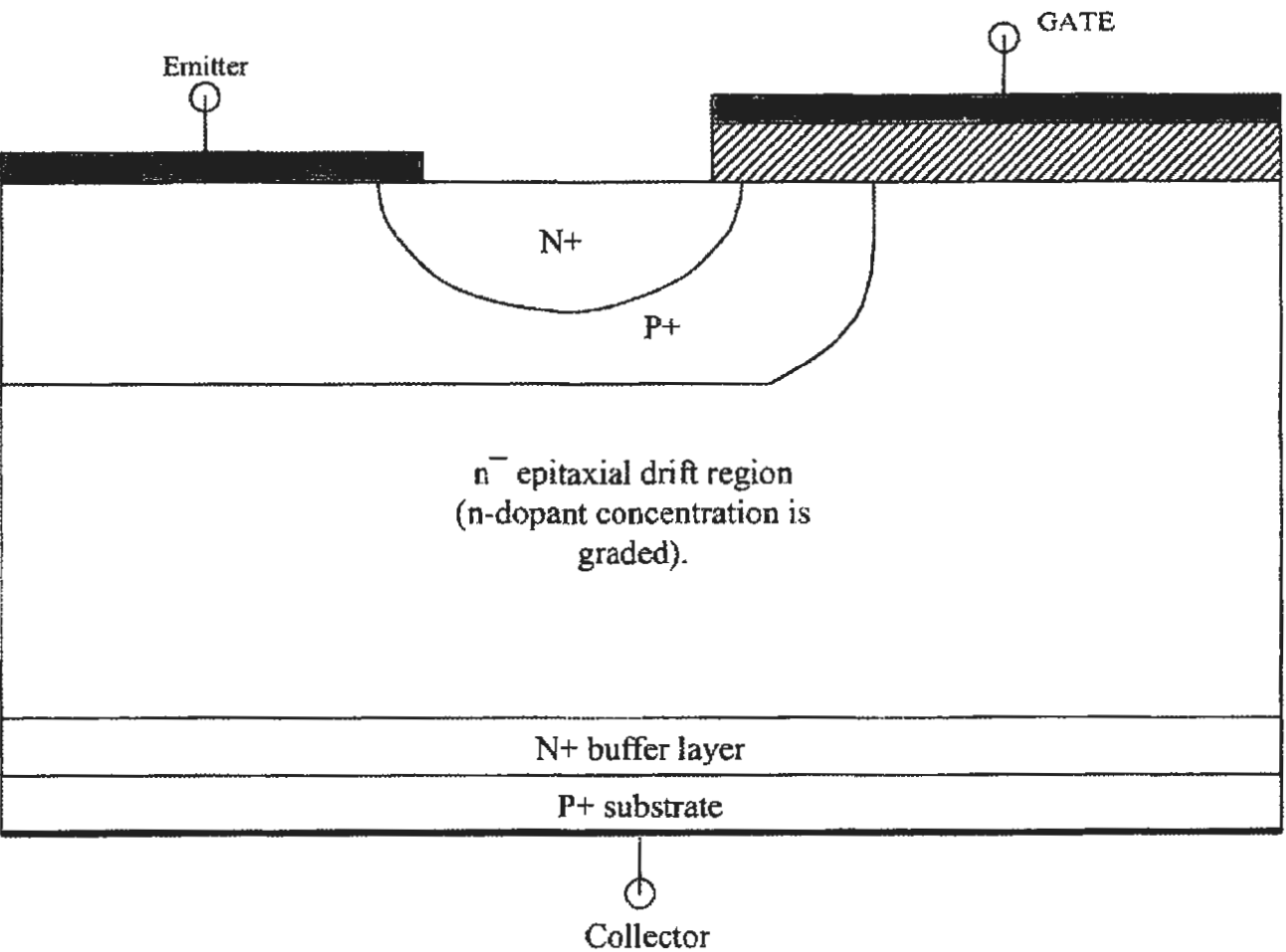


FIGURE 4 A dopant - concentration grinded drift region in a IGBT

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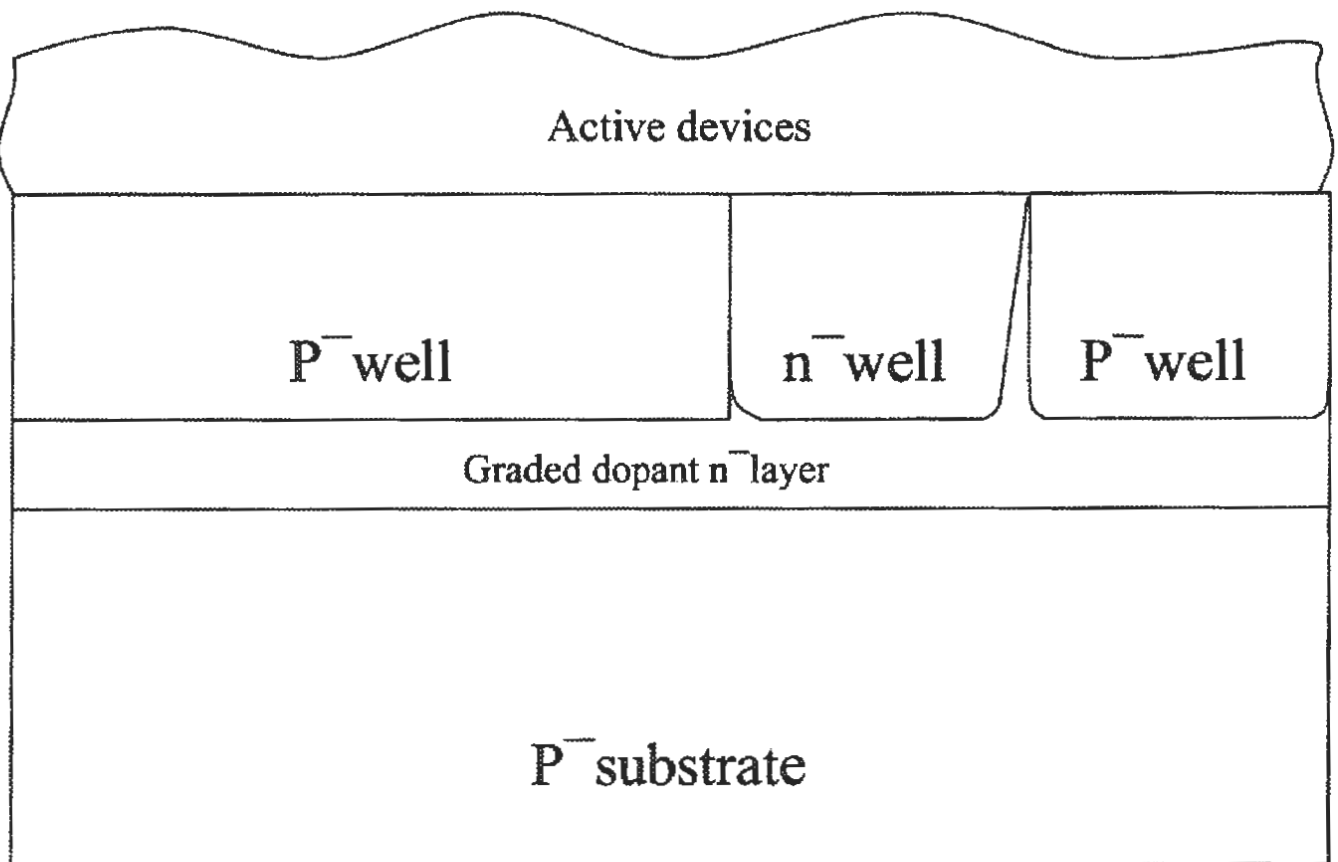


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

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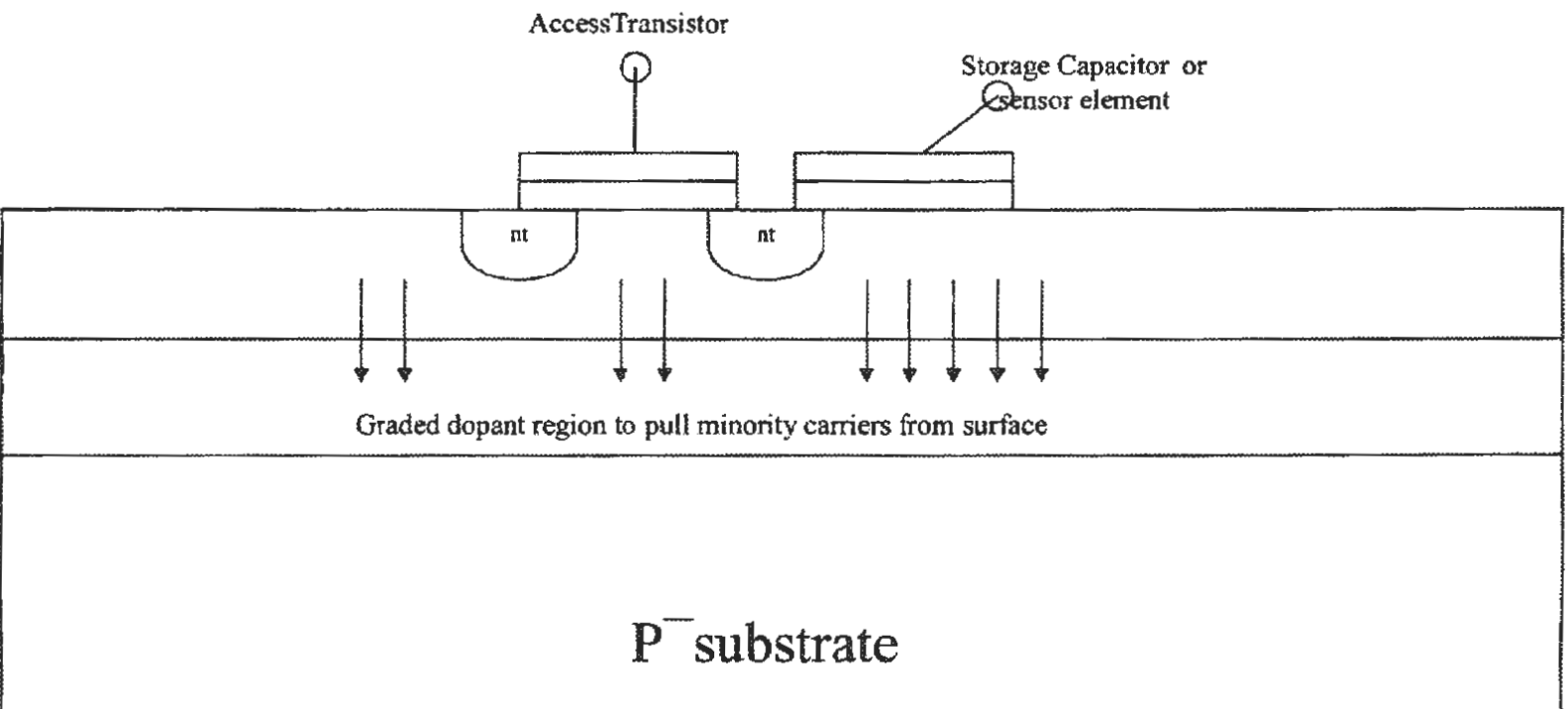


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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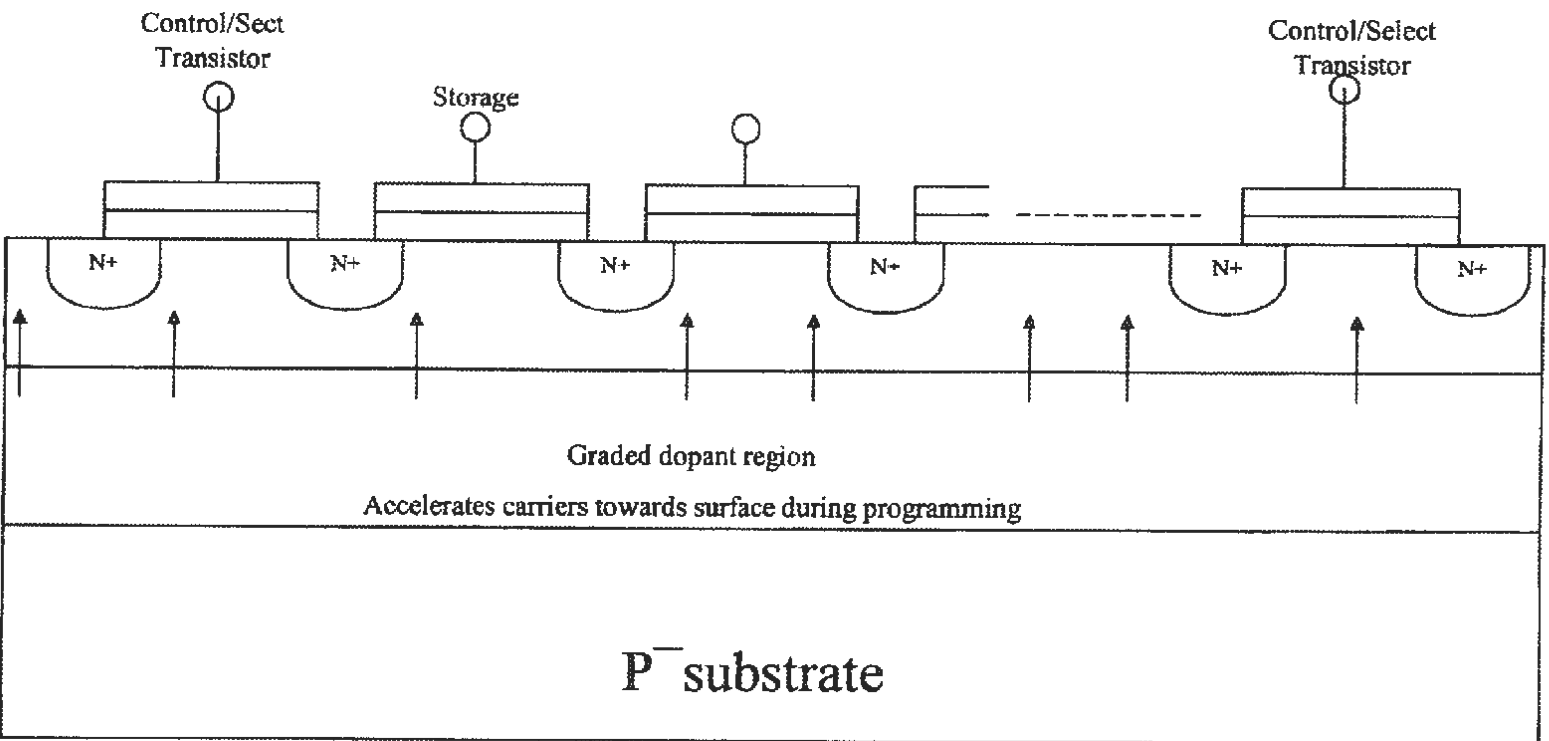


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 16/717,950, filed Dec. 17, 2019, which this a Continuation of U.S. patent application Ser. No. 15/590,282, filed May 9, 2017, which is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, which is Continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, which is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, which is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, which is a Divisional of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and

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hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

5 Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

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BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁺-well in which p-channel transistors are subsequently fabricated and one p⁺-well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or,

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frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The "average" base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n -epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held "actively held high" nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating "subterranean" recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n -layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n -layer can be a deeply-implemented layer. It can also be an epitaxial layer. As desired, the n -well and p -wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated

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towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the "channel pinch-off" is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A VLSI semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level having a surface;
 - a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region;
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
 - at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

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4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.

5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

10. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

11. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

12. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.

14. The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.

17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.

18. The VLSI semiconductor device of claim 1, wherein the device is central processing unit.

19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor.

20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.

21. A VLSI semiconductor device, comprising:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and

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at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate.

23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.

24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.

28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

29. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

30. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

31. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.

33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.

35. The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.

36. The VLSI semiconductor device of claim 21, wherein the device is central processing unit.

37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor.

38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.

39. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level; a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

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at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.

41. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level; a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

42. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level; a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded donor dopant

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concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

43. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level; a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

44. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of the surface layer;

a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and

at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

* * * * *

EXHIBIT 6

(12) **United States Patent**
Rao

(10) **Patent No.: US 11,316,014 B2**
(45) **Date of Patent: *Apr. 26, 2022**

(54) **SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS**

(71) Applicant: **GREENTHREAD, LLC**, Dallas, TX
(US)

(72) Inventor: **G. R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX
(US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

This patent is subject to a terminal dis-
claimer.

(21) Appl. No.: **17/371,839**

(22) Filed: **Jul. 9, 2021**

(65) **Prior Publication Data**

US 2021/0359086 A1 Nov. 18, 2021

Related U.S. Application Data

(60) Continuation of application No. 16/947,294, filed on
Jul. 27, 2020, now Pat. No. 11,121,222, which is a
(Continued)

(51) **Int. Cl.**
H01L 29/10 (2006.01)
H01L 27/11524 (2017.01)

(Continued)

(52) **U.S. Cl.**
CPC **H01L 29/1095** (2013.01); **H01L 27/11521**
(2013.01); **H01L 27/11524** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC **H01L 29/1095**
(Continued)

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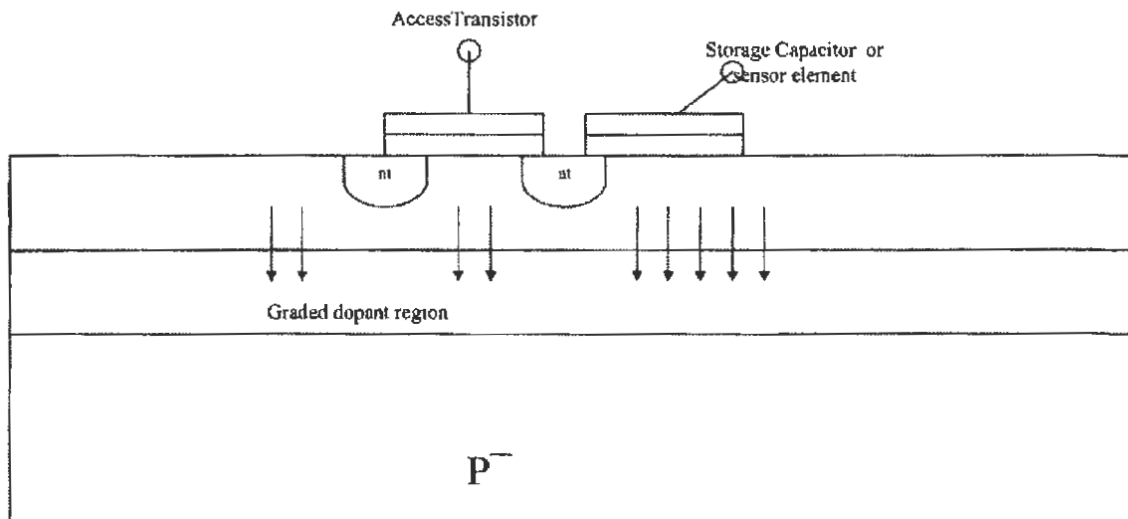
Primary Examiner - Ajay Arora

(74) *Attorney, Agent, or Firm Gregory M. Howison*

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uni-
form dopant concentration, either in the lateral or vertical
device active (and isolation) regions. By grading the dopant
concentration, the performance in various semiconductor
devices can be significantly improved. Performance
improvements can be obtained in application specific areas
like increase in frequency of operation for digital logic,
various power MOSFET and IGBT ICs, improvement in
refresh time for DRAMs, decrease in programming time for
nonvolatile memory, better visual quality including pixel
resolution and color sensitivity for imaging ICs, better
sensitivity for varactors in tunable filters, higher drive capa-
bilities for iFETs, and a host of other applications.

30 Claims, 10 Drawing Sheets



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Related U.S. Application Data

continuation of application No. 16/717,950, filed on Dec. 17, 2019, now Pat. No. 10,734,481, which is a continuation of application No. 15/590,282, filed on May 9, 2017, now Pat. No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) Int. Cl.

H01L 27/146 (2006.01)
H01L 27/11521 (2017.01)
H01L 29/739 (2006.01)
H01L 29/36 (2006.01)
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(52) U.S. Cl.

CPC H01L 27/14643 (2013.01); H01L 29/36 (2013.01); H01L 29/7395 (2013.01); H01L 27/0214 (2013.01); H01L 27/10844 (2013.01)

(58) Field of Classification Search

USPC 257/25
See application file for complete search history.

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U.S. Patent

Apr. 26, 2022

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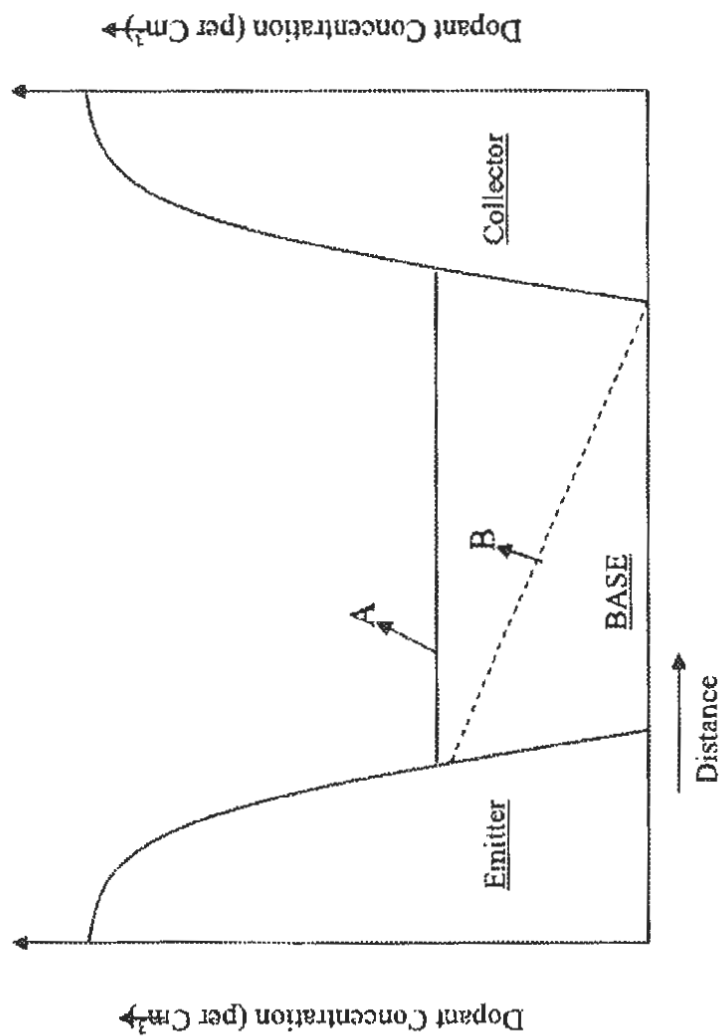


Figure 1 Prior Art

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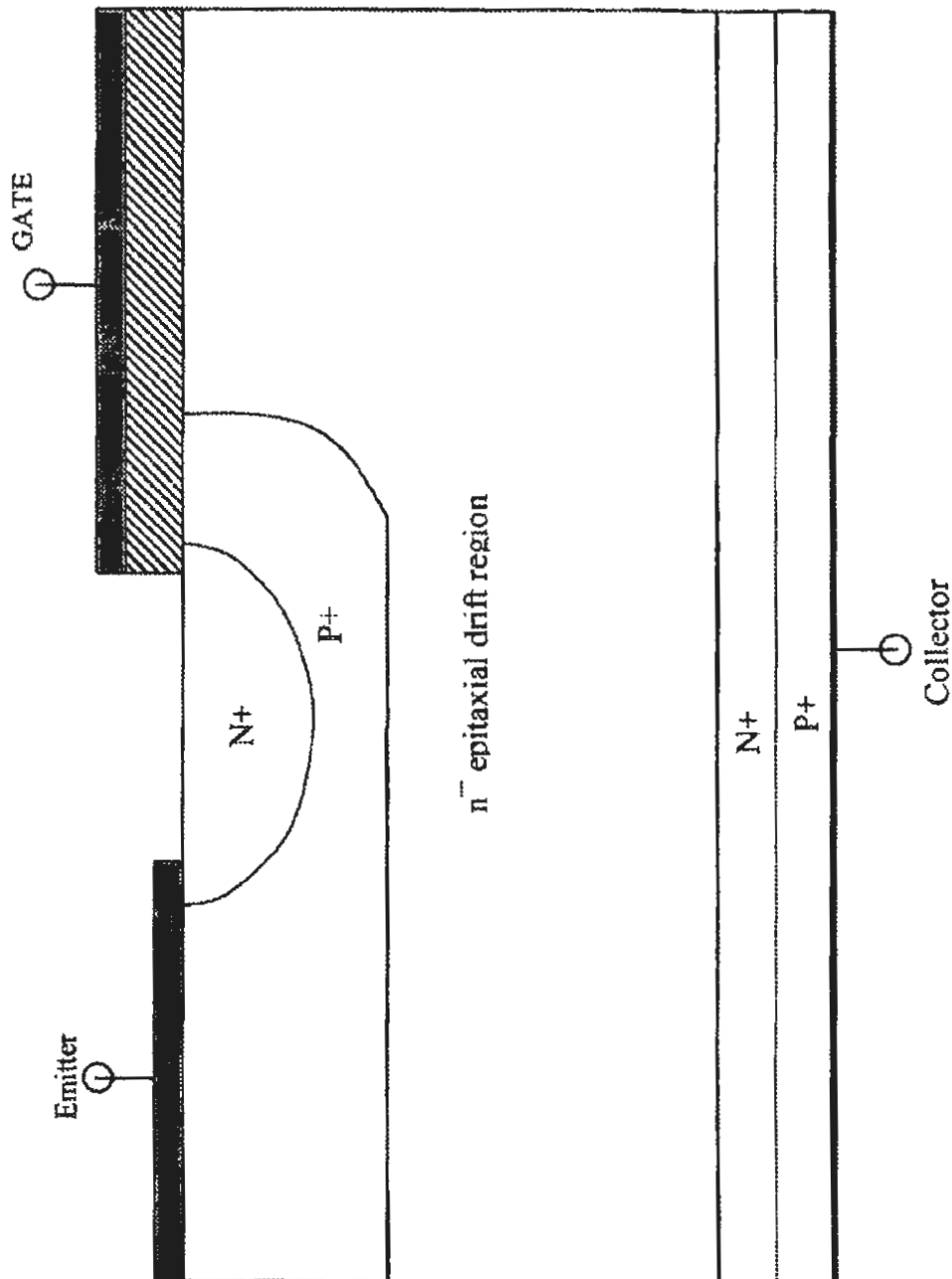


FIGURE 2 Prior art

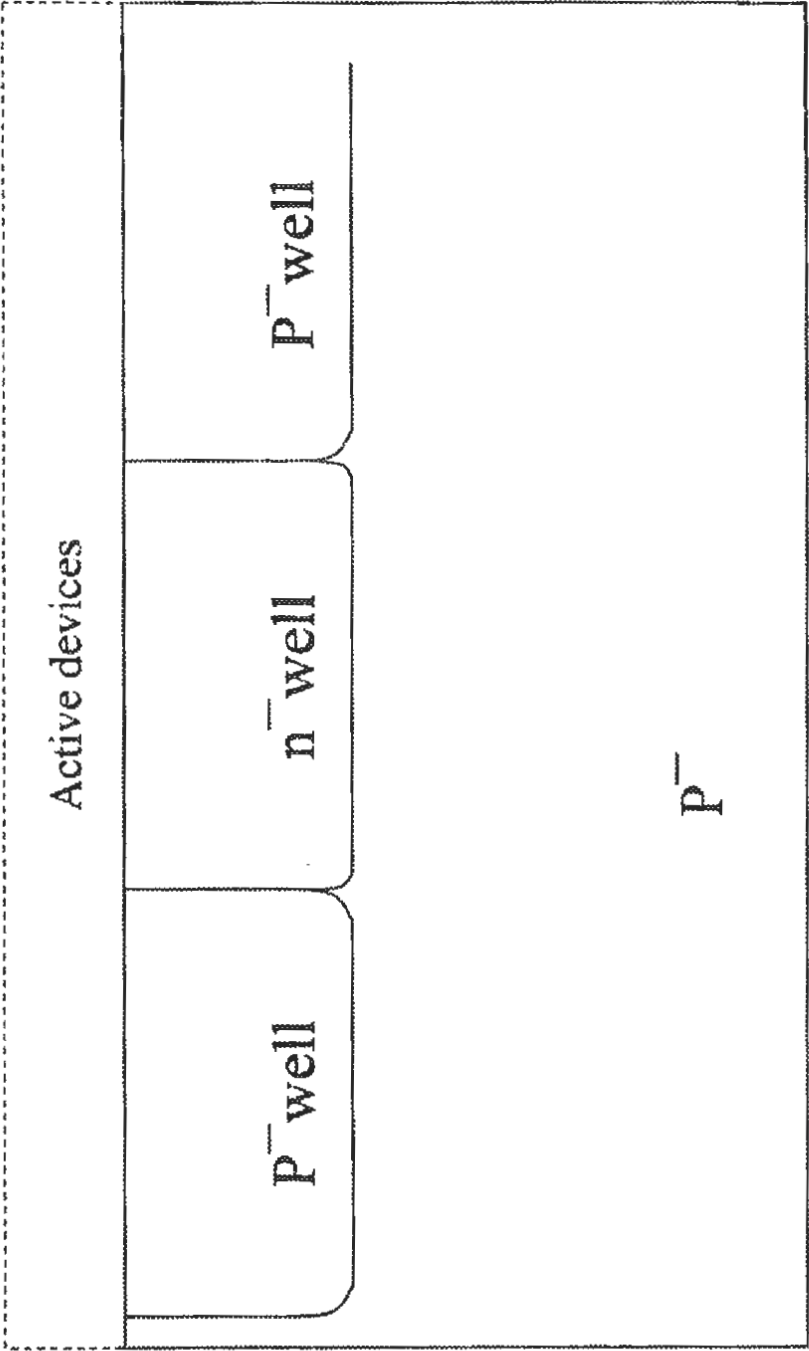


FIGURE 3A Prior art

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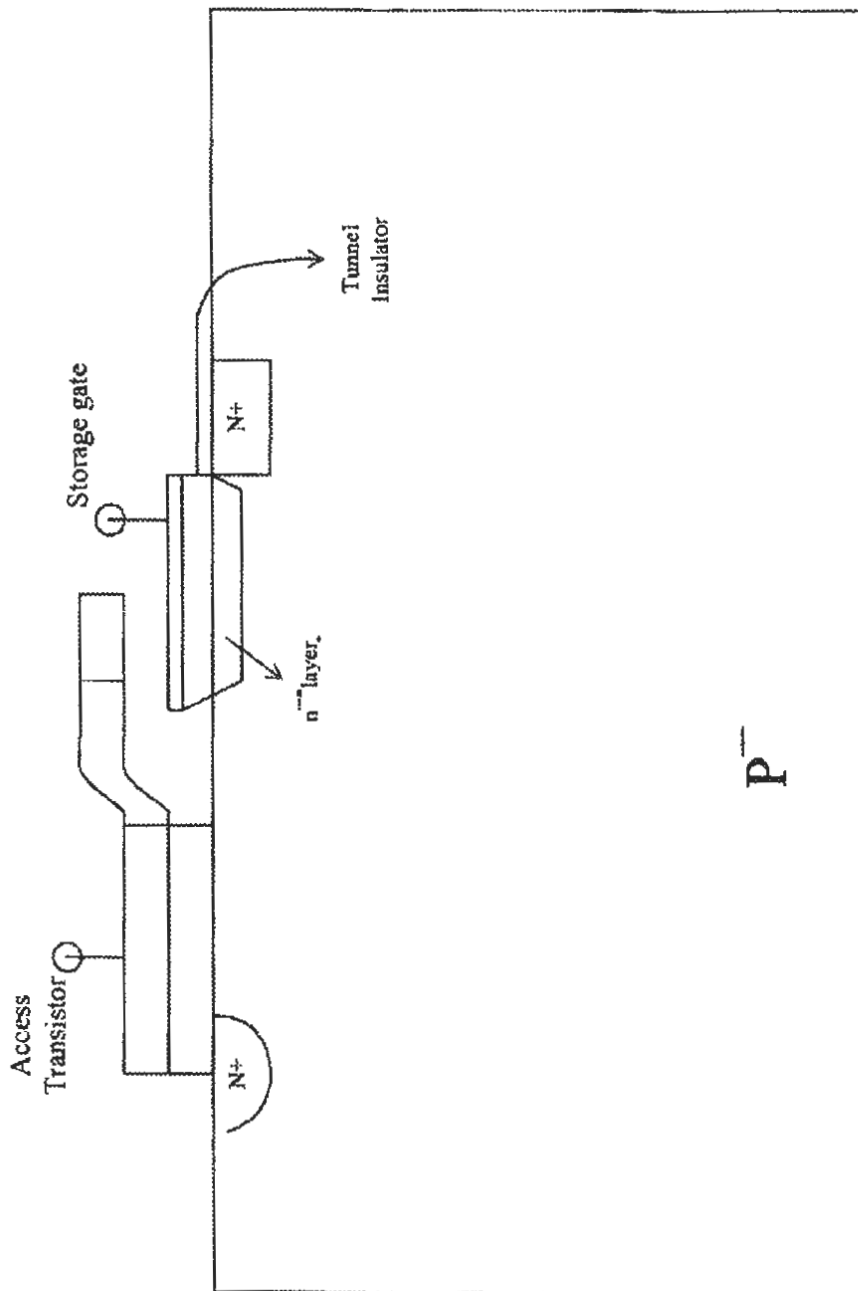


FIGURE 3B Prior art

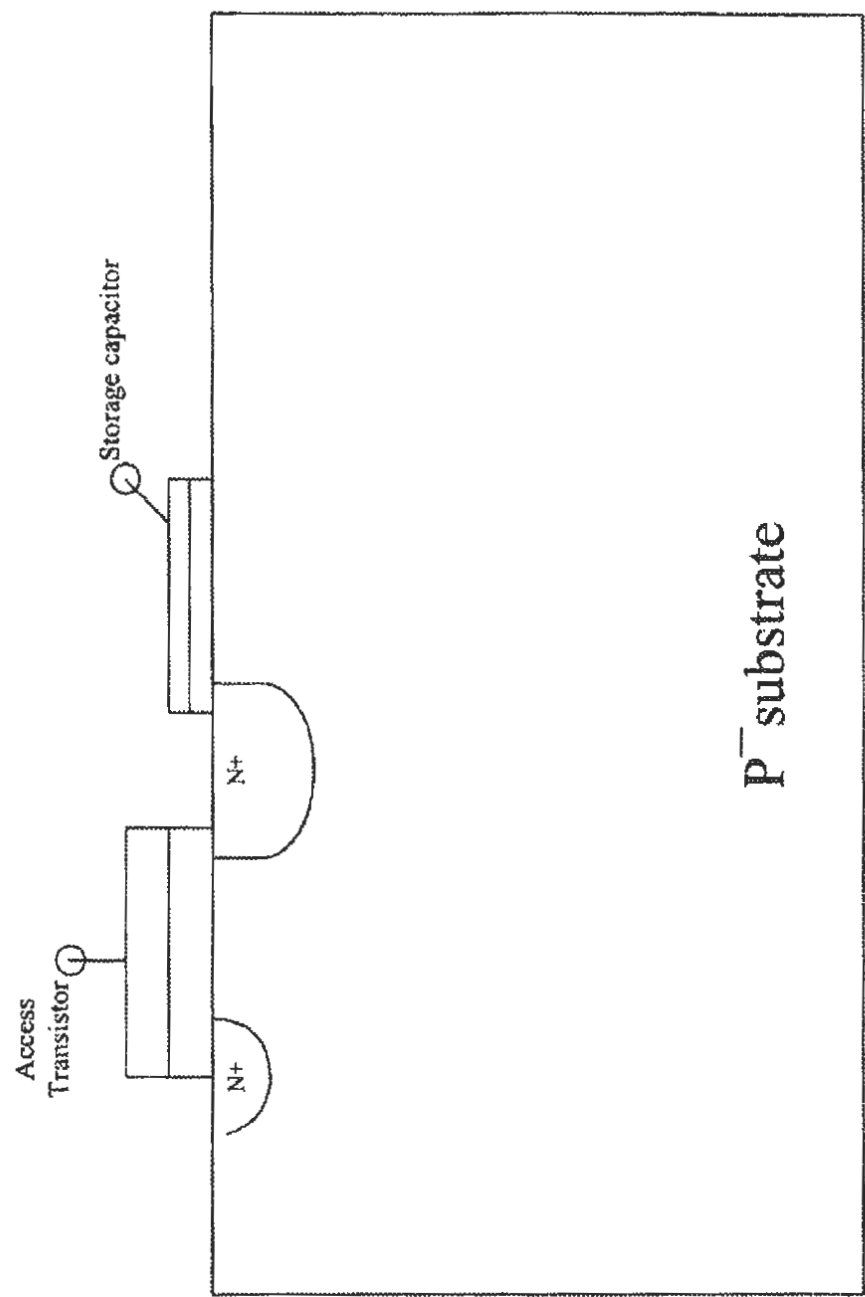


FIGURE 3C Prior art

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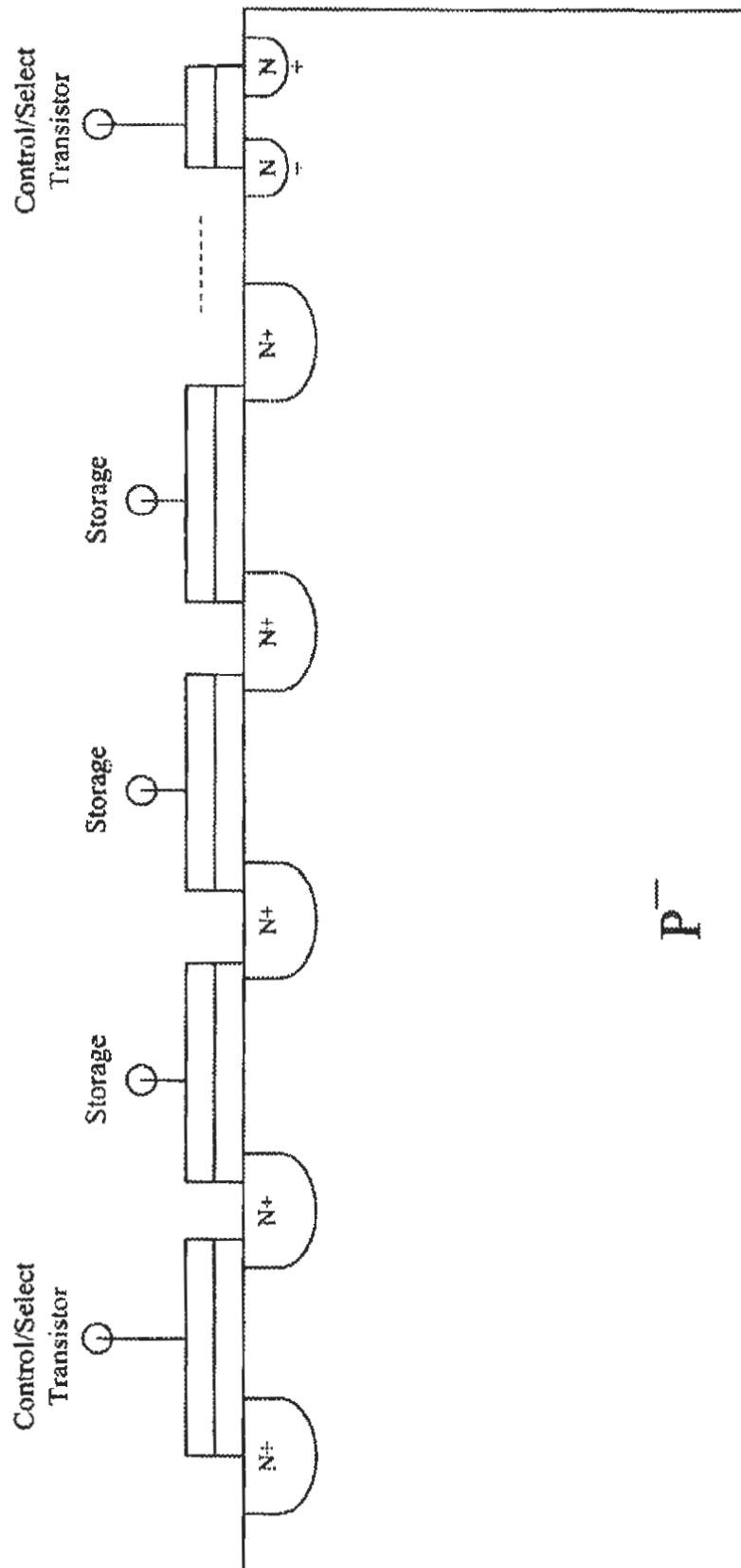


FIGURE 3D Prior art

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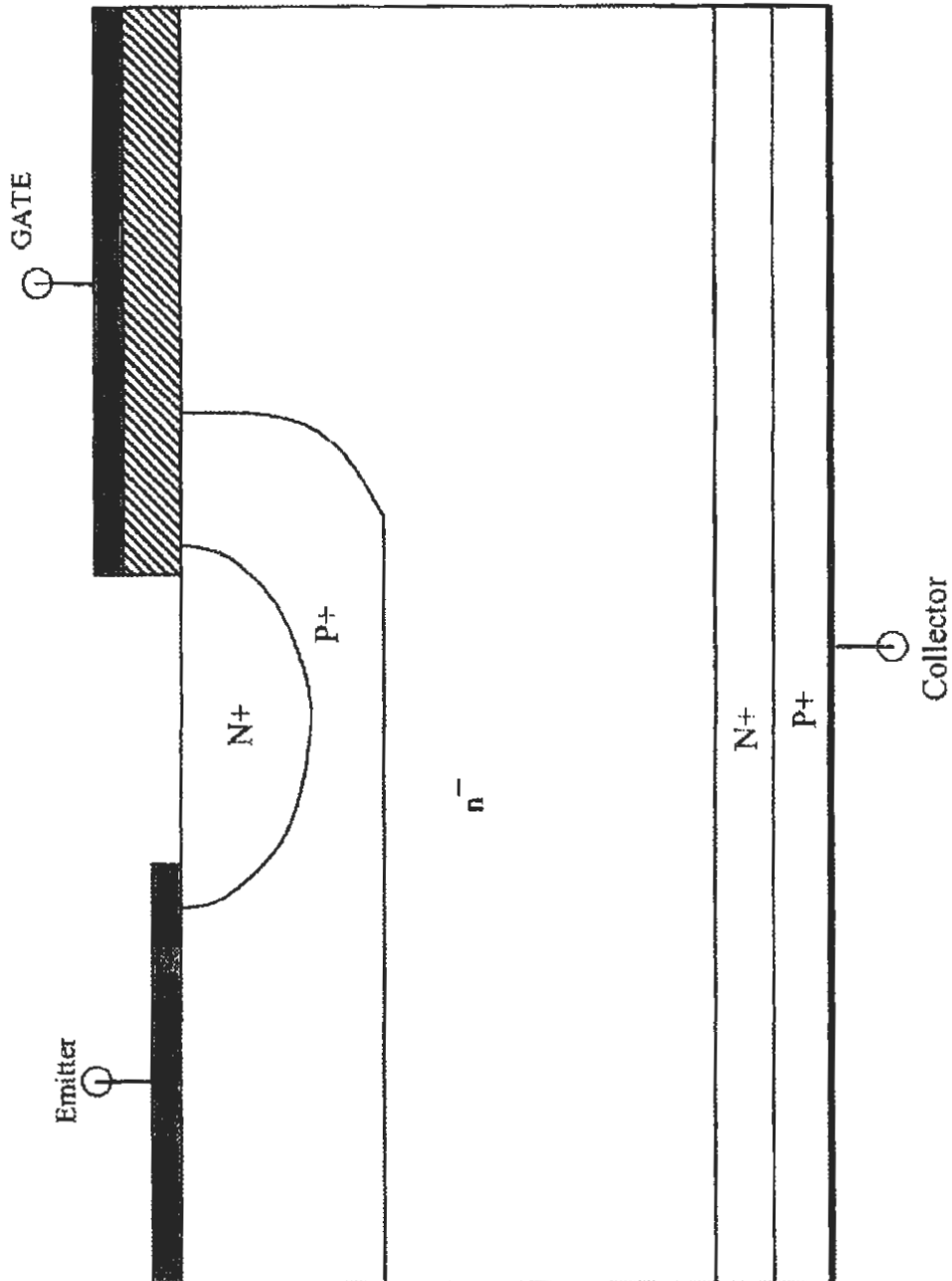


FIGURE 4

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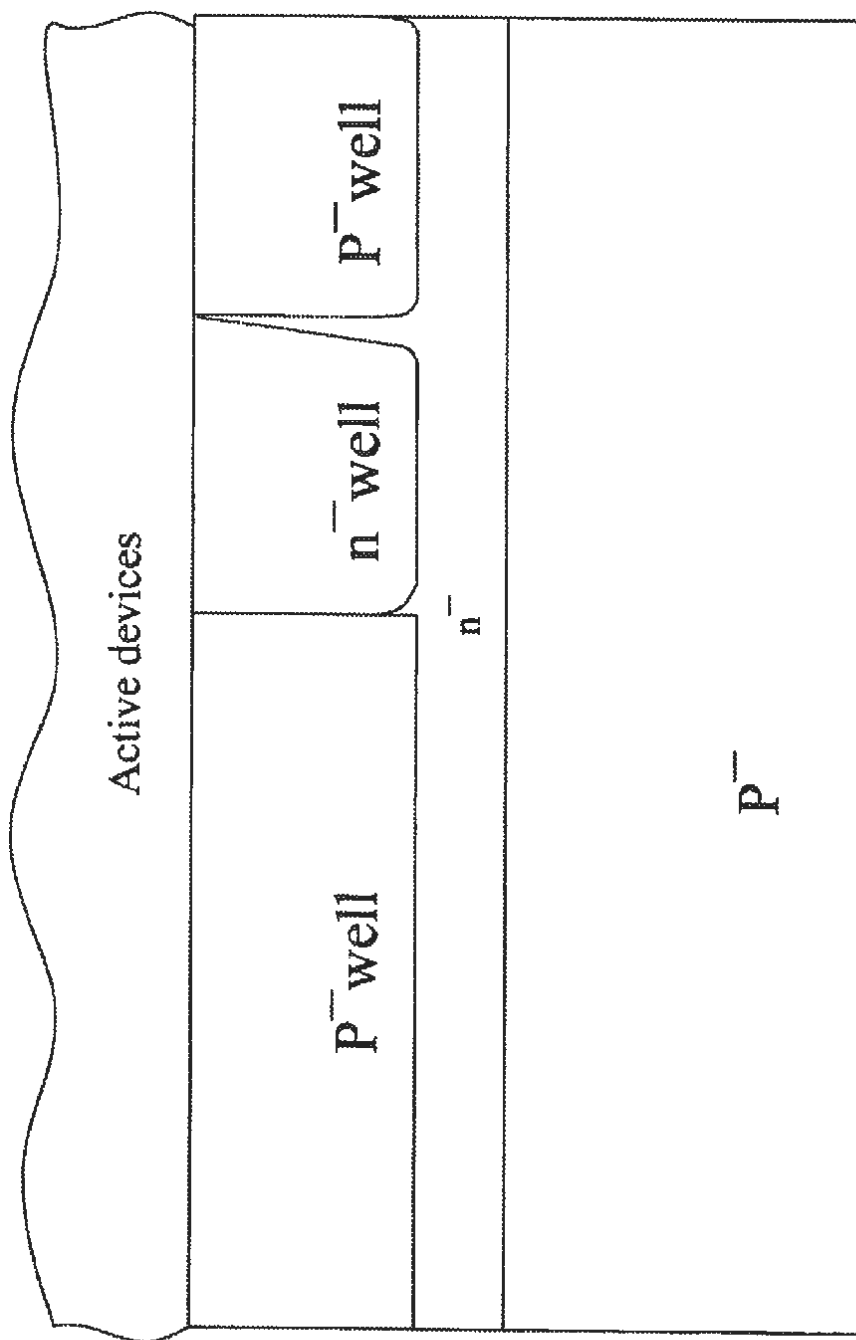


FIGURE 5A

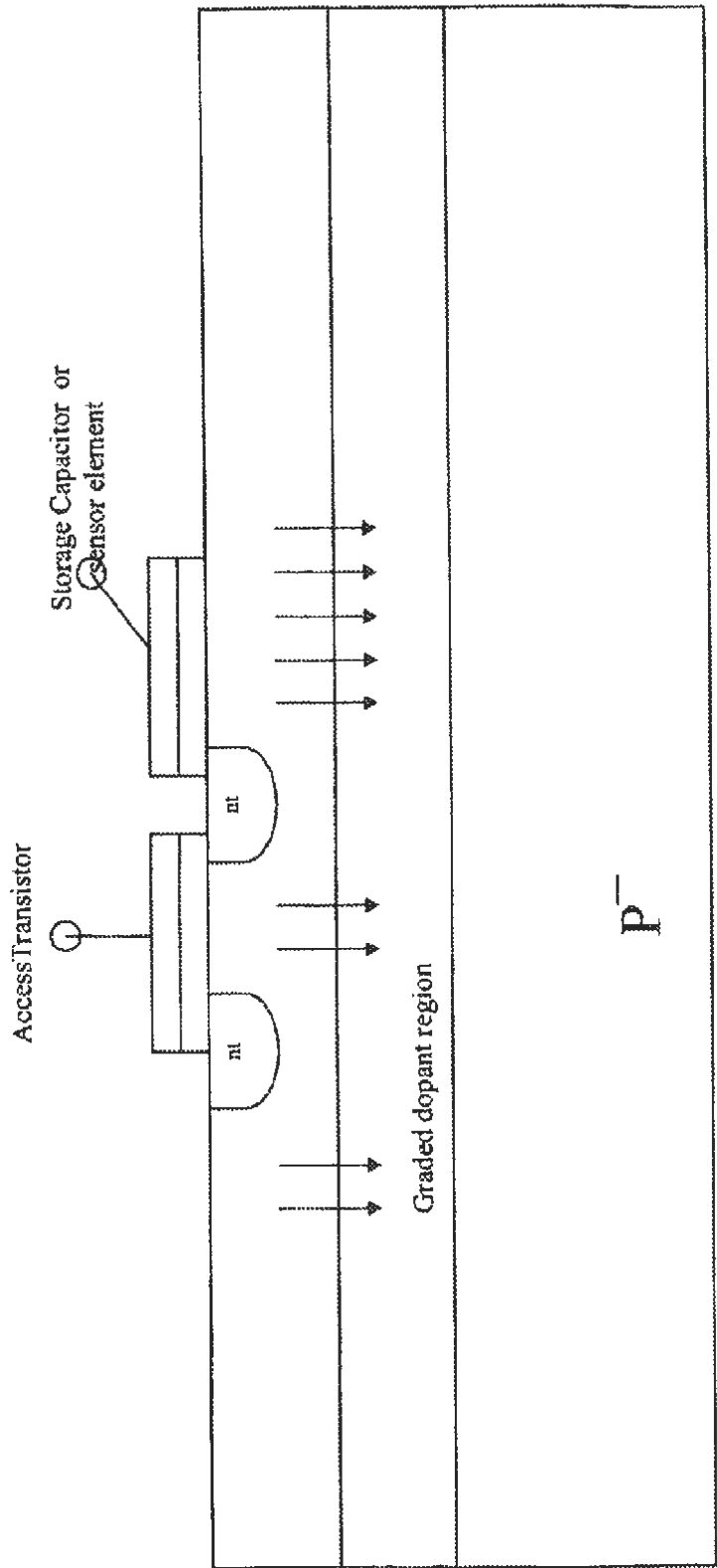


FIGURE 5B

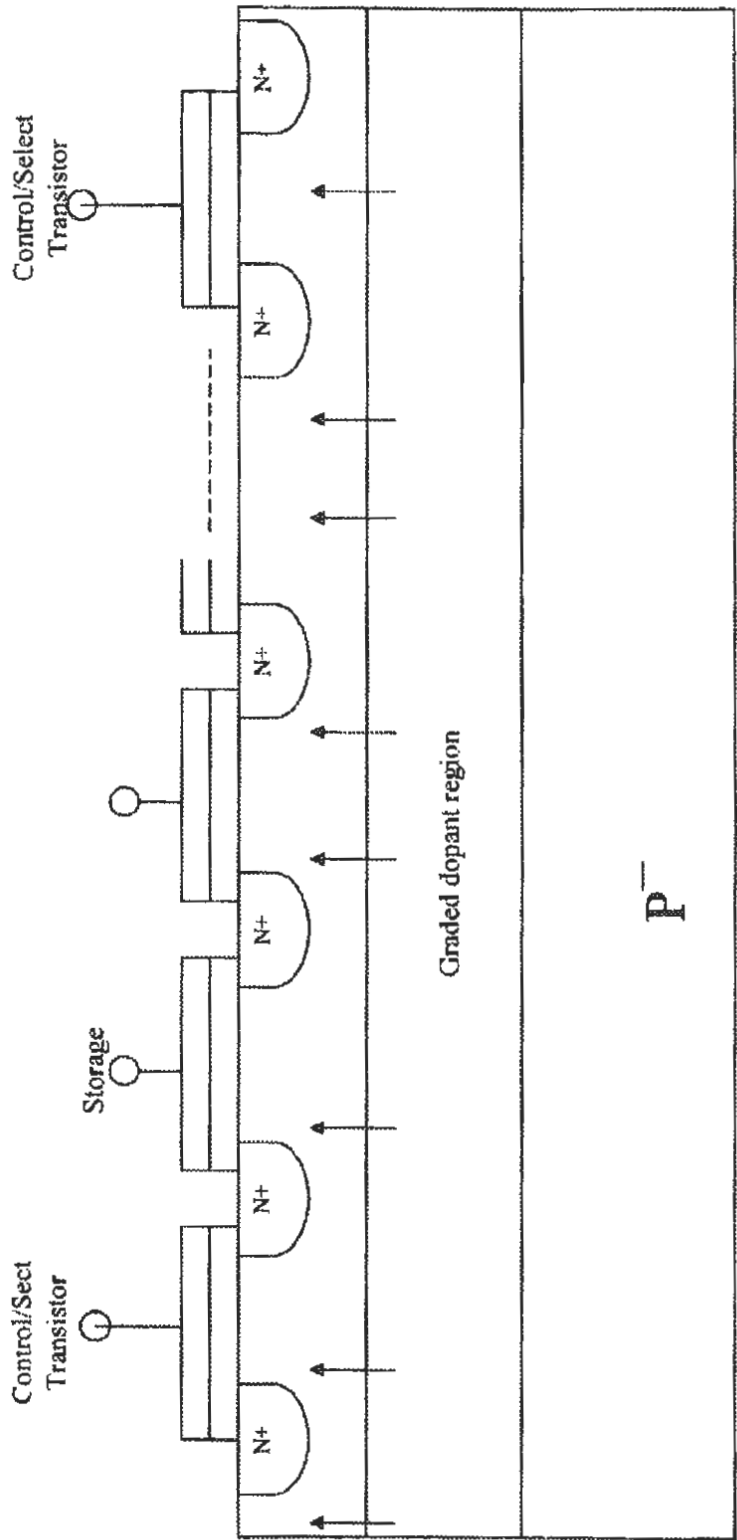


FIGURE 5C

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**SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS****CROSS-REFERENCE TO RELATED
APPLICATIONS**

This application is a Continuation of U.S. patent application Ser. No. 16/947,294, filed Jul. 27, 2020, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, which is a Continuation of U.S. patent application Ser. No. 16/717,950, filed Dec. 17, 2019, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 10,734,481 on Aug. 4, 2020. U.S. patent application Ser. No. 16/717,950 is a Continuation of U.S. patent application Ser. No. 15/590,282, filed May 9, 2017, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 10,510,842 on Dec. 17, 2019, which is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 9,647,070 on May 9, 2017, which is Continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 9,190,502 on Nov. 17, 2015, which is a Continuation of U.S. patent application Ser. No. 13/854,319 filed April 1, 2013, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, which is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 8,421,195 on Apr. 16, 2013, which is a Divisional of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors),

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still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates: FIG. 3A showing a typical prior art IC with two wells (one n⁺ well in which p-channel transistors are subsequently fabricated and one p⁺ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application: VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base

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region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The "average" base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held "actively held high" nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating "subterranean" recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as

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possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^+ wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the "channel pinch-off" is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. An electronic system, the system comprising:
 - at least one semiconductor device, the at least one semiconductor device including:
 - a substrate of a first doping type at a first doping level having a surface;
 - a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region;
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

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at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.

2. The system of claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.

3. The system of claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

4. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.

5. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.

7. The system of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The system of claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.

9. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.

10. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region of the at least one semiconductor device are both p-type and n-type.

11. The system of claim 1, wherein dopants of the graded dopant concentration in the second active region of the at least one semiconductor device are both p-type and n-type.

12. The system of claim 1, wherein dopants of the graded dopant region in the well region of the at least one semiconductor device are both p-type and n-type.

13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.

14. The system of claim 1, wherein the at least one semiconductor device is a dynamic random access memory (DRAM).

15. The system of claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The system of claim 1, wherein the at least one semiconductor device is a flash memory.

17. The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.

18. The system of claim 1, wherein the at least one semiconductor device is a central processing unit.

19. The system of claim 1, wherein the at least one semiconductor device is an image sensor.

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20. The system of claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.

21. An electronic system, comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The system of claim 21, wherein the substrate of the at least one semiconductor device is an n-type substrate.

23. The system of claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.

24. The system of claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

25. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.

26. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.

28. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.

29. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region of the at least one semiconductor device are both p-type and n-type.

30. The system of claim 21, wherein dopants of the graded dopant concentration in the second active region of the at least one semiconductor device are both p-type and n-type.

* * * * *

EXHIBIT 7

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3351825

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
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RECEIVING PARTY DATA	
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Postal Code:	75229-5400
PROPERTY NUMBERS Total: 9	
Property Type	Number
Application Number:	10934915
Patent Number:	8421195
Patent Number:	8106481
Application Number:	13854319
Application Number:	14515584
Application Number:	60982175
Application Number:	14335160
Application Number:	61509257
Application Number:	14525411
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NAME OF SUBMITTER:	GREGORY M. HOWISON

503305206

SIGNATURE:	/Gregory M. Howison, Reg. #30646/
DATE SIGNED:	05/13/2015
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ASSIGNMENT

WHEREAS, G.R. MOHAN RAO, an individual, residing at 1611 Willingham Drive, Allen, Texas 75013 ("Assignor"), has invented certain new and useful inventions set forth on the attached Exhibit A (collectively, the "Inventions"), for which certain applications for United States and foreign patents were filed as set forth on Exhibit A (collectively, the "Applications"), and from which certain United States patents have issued as set forth on Exhibit A (collectively, the "Patents"); and

WHEREAS, GREENTHREAD, LLC, a Texas Limited Liability Company, having a business address at 4544 Harrys Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the Applications and Patents and any and all foreign counterparts, divisions, continuations, continuation-in-parts, improvements, reexaminations, reissues, extensions, renewals, substitutes, provisional applications, certificates, all rights under the International Convention for the Protection of Industrial Property and prolongations of the Applications and Patents.

Now, THEREFORE, for other good and valuable consideration, Assignor, by these presents does hereby irrevocably sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right in and to:

- (a) the Applications and Patents in the United States and the entire right, title, and interest in and to any and all issued patents or patent applications which may be granted therefor and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents;
- (b) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of the Applications and Patents, including without limitation all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (c) all rights to collect royalties or other payments under or on account of the Applications and Patents and the foregoing subcategory (b).

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Applications, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for its sole use and benefit; and for the use and benefit of its legal representatives, to the full end of the term for which said patents may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest in and to the Inventions disclosed in

said Applications throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the inventions in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the inventions and all rights to register the inventions in appropriate registries, all foreign rights arising from pre-grant publication of the Applications; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Inventions in all countries.

[Signature Page to Follow]

G.R. Mohan Rao
G.R. Mohan Rao

April 27, 2015
Date

STATE OF: Texas

COUNTY OF: Dallas

BEFORE ME, a Notary Public, on this 27th day of April, 2017, personally appeared G.R. MOHAN RAO, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he/she executed same of his/her own free will for the purposes and consideration therein expressed.

[SEAL]

Kristy Lea Kyles
Notary Public
Commission Expires: 9-9-17

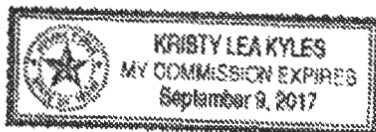


EXHIBIT A

	Atty. Ref.	Country	Serial No.	Patent No.	Title
1.	32625	US	10/934,915		Semiconductor Devices with Graded Dopant Regions
2.	32611	US	11/622,496	8,421,195	Semiconductor Devices with Graded Dopant Regions
3.	32612	US	12/549,283	8,106,481	Semiconductor Devices with Graded Dopant Regions
4.	32626	US	13/854,319		Semiconductor Devices with Graded Dopant Regions
5.	32613	US	14/515,584		Semiconductor Devices with Graded Dopant Regions
6.	32623	US	60/982,175		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
7.	32614	US	12/256,362	7,855,916	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
8.	32615	US	12/915,177	8,194,452	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
9.	32616	US	13/458,173	8,531,880	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
10.	32617	US	13/967,649	8,817,537	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
11.	32618	US	14/335,160		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
12.	32624	US	61/509,257		Lifetime Mixed Level Non-Volatile Memory System
13.	32619	US	13/455,267	8,891,298	Lifetime Mixed Level Non-Volatile Memory System
14.	32620	US	14/525,411		Lifetime Mixed Level Non-Volatile Memory System



United States Patent and Trademark Office

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1

Stylesheet Version v1.2

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	CONFIRMATORY ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
VERVAIN, LLC	03/07/2022
RECEIVING PARTY DATA	
Name:	GREENTHREAD, LLC
Street Address:	4544 HARRYS LANE
City:	DALLAS
State/Country:	TEXAS
Postal Code:	75229-5400
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	17371839
CORRESPONDENCE DATA	
Fax Number:	(972)628-3616
Phone:	9726283600

Email: admin@dalpat.com <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Correspondent Name: GREGORY M. HOWISON	
Address Line 1: P.O. DRAWER 800889	
Address Line 4: DALLAS, TEXAS 75380	
ATTORNEY DOCKET NUMBER:	GRTD60-35314
NAME OF SUBMITTER:	GREGORY M. HOWISON
Signature:	/Gregory M. Howison, Reg. #30646/
Date:	03/07/2022
Total Attachments: 2 source=GRT35314 Confirmatory Assignment exe#page1.tif source=GRT35314 Confirmatory Assignment exe#page2.tif	
RECEIPT INFORMATION EPAS ID: PAT7210634 Receipt Date: 03 07 2022	

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506780899 07/22/2021
PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6827716

SUBMISSION TYPE:	NEW ASSIGNMENT		
NATURE OF CONVEYANCE:	ASSIGNMENT		
CONVEYING PARTY DATA			
Name			Execution Date
MR G.R. MOHAN RAO			09/09/2017
RECEIVING PARTY DATA			
Name:	GREENTHREAD, LLC		
Street Address:	4544 HARRYS LANE		
City:	DALLAS		
State/Country:	TEXAS		
Postal Code:	75229		
PROPERTY NUMBERS Total: 1			
Property Type	Number		
Application Number:	17371839		
CORRESPONDENCE DATA			
Fax Number:	(972)628-3616		
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>			
Phone:	9726283624		
Email:	ipdocketing@munckwilson.com		
Correspondent Name:	GREGORY M HOWISON		
Address Line 1:	12770 COIT RD STE 600 STE 660		
Address Line 2:	STE 660		
Address Line 4:	DALLAS, TEXAS 75251		
NAME OF SUBMITTER:	GREGORY HOWISON		
SIGNATURE:	/Gregory Howison - Reg# 30646/		
DATE SIGNED:	07/22/2021		
Total Attachments: 4			
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source=GRT34138RaotoGreenthreadASSMTEXE#page4.tif			

506780899

ASSIGNMENT

WHEREAS, G.R. MOHAN RAO, an individual, residing at 1611 Willingham Drive, Allen, Texas 75013 ("Assignor"), has invented certain new and useful inventions set forth on the attached Exhibit A (collectively, the "Inventions"), for which certain applications for United States and foreign patents were filed as set forth on Exhibit A (collectively, the "Applications"), and from which certain United States patents have issued as set forth on Exhibit A (collectively, the "Patents"); and

WHEREAS, GREENTHREAD, LLC, a Texas Limited Liability Company, having a business address at 4544 Harrys Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the Applications and Patents and any and all foreign counterparts, divisions, continuations, continuation-in-parts, improvements, reexaminations, reissues, extensions, renewals, substitutes, provisional applications, certificates, all rights under the International Convention for the Protection of Industrial Property and prolongations of the Applications and Patents.

Now, THEREFORE, for other good and valuable consideration, Assignor, by these presents does hereby irrevocably sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right in and to:

- (a) the Applications and Patents in the United States and the entire right, title, and interest in and to any and all issued patents or patent applications which may be granted therefor and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents;
- (b) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of the Applications and Patents, including without limitation all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (c) all rights to collect royalties or other payments under or on account of the Applications and Patents and the foregoing subcategory (b).

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Applications, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for its sole use and benefit; and for the use and benefit of its legal representatives, to the full end of the term for which said patents may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest in and to the Inventions disclosed in

said Applications throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the inventions in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the inventions and all rights to register the inventions in appropriate registries, all foreign rights arising from pre-grant publication of the Applications; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Inventions in all countries.

[Signature Page to Follow]

G.R. Mohan Rao
G.R. Mohan Rao

April 27, 2017
Date

STATE OF: Texas §

COUNTY OF: Dallas §

BEFORE ME, a Notary Public, on this 27th day of April, 2017, personally appeared G.R. MOHAN RAO, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he/she executed same of his/her own free will for the purposes and consideration therein expressed.

[SEAL]

Kristy Lea Kyles
Notary Public
Commission Expires: 9-9-17

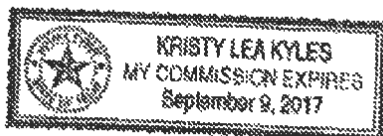


EXHIBIT A

	Atty. Ref.	Country	Serial No.	Patent No.	Title
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5.	32613	US	14/515,584		Semiconductor Devices with Graded Dopant Regions
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8.	32615	US	12/915,177	8,194,452	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
9.	32616	US	13/458,173	8,531,880	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
10.	32617	US	13/967,649	8,817,537	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
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12.	32624	US	61/509,257		Lifetime Mixed Level Non-Volatile Memory System
13.	32619	US	13/455,267	8,891,298	Lifetime Mixed Level Non-Volatile Memory System
14.	32620	US	14/525,411		Lifetime Mixed Level Non-Volatile Memory System

PATENT ASSIGNMENT

Page 4 of 4

RECORDED: 07/22/2021

PATENT Ex. 2026, p. 134 of 260
 REEL: 056950 FRAME: 0052
 Greenthread
 IPR2024-00552

506780678 07/22/2021
PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6827495

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	GREENTHREAD, LLC	08/19/2019
RECEIVING PARTY DATA		
Name:	VERVAIN, LLC	
Street Address:	724 MASON DELLS DRIVE	
City:	DALLAS	
State/Country:	TEXAS	
Postal Code:	75230	
PROPERTY NUMBERS Total: 1		
	Property Type	Number
	Application Number:	17371839
CORRESPONDENCE DATA		
Fax Number:	(972)628-3616	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	972-628-3624	
Email:	ipdocketing@munckwilson.com	
Correspondent Name:	GREGORY HOWISON	
Address Line 1:	12770 COIT ROAD SUITE 660	
Address Line 2:	SUITE 660	
Address Line 4:	DALLAS, TEXAS 75251	
NAME OF SUBMITTER:	GREGORY HOWISON	
SIGNATURE:	/Gregory Howison - Reg# 30646/	
DATE SIGNED:	07/22/2021	
Total Attachments: 2		
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ASSIGNOR Greenthread, LLC Philip W. John, Jr. Manager 6307 Bandera Ave, Apt B Dallas, Texas 75225-3617 Email: john@greenthreadllc.com	ASSIGNEE Vervain, LLC Philip W. John, Jr., Member 7424 Mason Dells Drive Dallas, Texas 75230-3244 Email: john@vervainllc.com
---	--

ASSIGNMENT AGREEMENT

This Assignment Agreement ("Assignment") is entered into by and between Vervain, LLC, a Texas limited liability company, hereinafter referred to as "Assignee," and Greenthread, LLC, a Texas limited liability company, hereinafter referred to as "Assignor," and shall become effective upon being duly signed by the authorized representative of Assignor ("Effective Date").

RECITALS:

Assignor and Assignee are entering into a Patent Assignment Agreement (the "Agreement").

Pursuant to the Agreement, Assignor hereby desires to assign to Assignee all of its rights, title and interest in and to the following United States patents and pending application:

1. U.S. Provisional Application Number ~~61/509,256~~ ^{61/509,257}, entitled, "Lifetime Mixed Level Nand Flash System," filed on July 19, 2011;
2. U.S. Patent Number 8,891,298, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on April 25, 2012, and issued on November 18, 2014;
3. U.S. Patent Number 9,196,385, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on October 28, 2014, and issued on November 24, 2015;
4. U.S. Patent Number 9,997,240, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on November 24, 2015, and issued on June 12, 2018, and
5. U.S. Patent Application Number 16/006,299, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on June 12, 2018, and is pending (collectively referred to hereinafter referred to as the "Patent").

For good and valuable consideration, Assignor and Assignee hereby agree as follows:

ASSIGNMENT:

1. Assignor hereby assigns to Assignee its entire worldwide right, title and interest in and to Assignor's Patent, including the entire worldwide right, title and interest in and to any reexamination or reissue of the Patent. This includes, without limitation, Assignor's right to prosecute, and receive, all damages, royalties, awards and compensation for past, present and/or future infringement.
2. Assignor agrees to do the following without further consideration, in order to carry out the intent of this Assignment:
 - i. Execute all oaths, assignments, applications, and other papers necessary or desirable to fully secure to Assignee the rights, titles and interests herein conveyed; and
 - ii. Generally do all lawful acts for vesting in Assignee the rights, titles, and interests herein conveyed.
3. Assignor has not made and will not hereafter make any assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed to Assignee.
4. Assignor hereby represents and warrants that Assignor has the authority to assign the applicable Patent pursuant to this Assignment.

The undersigned having read this Assignment and fully understanding the provisions of this Assignment, hereby executes this Assignment as of the Effective Date.

Greenthread, LLC (Assignor)
Philip W. John, Jr. Manager



Signature:

Printed Name: Philip W. John, Jr.

Date: August 9, 2019

GRTD60-35314

PATENT

CONFIRMATORY ASSIGNMENT

Whereas, **VERVAIN, LLC**, a Texas limited liability company, located at 724 Mason Dells Drive, Dallas, Texas 75230 ("Assignor"), hereby confirms that it has zero right, title and interest in and to the currently pending application entitled, **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS** (the "Invention"), for which United States Patent Application was filed on July 9, 2021 (Serial No. 17/371,839) (the "Application"), and confirms the Assignment previously Assigned and recorded at reel/frame 056950/0048 on July 22, 2021 from inventor G.R. Mohan RAO to Greenthread, LLC is the only valid Assignment and the Assignment recorded on July 22, 2021 from Greenthread, LLC to Vervain, LLC at reel/frame 056949/0013 was in error as it did not list the Application; and

Whereas, **GREENTHREAD, LLC**, a Texas Limited Liability Company, located at 4544 Harrys Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of confirming that the entire right, title, and interest in the Application is fully vested in Assignee, and desires confirmation that Assignee has never assigned any interest in and to the Application to Assignor and that Assignor has no rights to this Application, as no rights have ever been conveyed to Assignor.

Now, Therefore, for other good and valuable consideration, Assignor, by these presents does hereby sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right to the Application in the United States and the entire right, title, and interest in and to any and all Patents which may be granted therefore and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said application. Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Invention, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for his sole use and benefit; and for the use and benefit of his legal representatives, to the full end of the term for which said Patent(s) may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest to the Invention disclosed in said Application throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the Invention in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the Invention and all rights to register the Invention in appropriate registries, all foreign rights arising from pre-grant publication of the Application; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

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Assignor further authorizes and directs Assignee's attorneys to insert the serial number and filing date of said application now identified by the attorney docket number and title set forth above as soon as the same shall have been made known to them by the United States Patent and Trademark Office.

VERVAIN, LLC

By: Philip W. John Jr.
Name: Philip W. John Jr.
Title: MANAGER
Date: 3/7/2022

EXHIBIT 8

MPS Accused Products

The following list of Accused Products is exemplary, non-exhaustive, and non-limiting. Greenthread identifies the following specific products to illustrate categories or types of products that constitute a MPS Accused Products. Greenthread further asserts claims against all product variations and part numbers of the MPS Accused Products. All of the below exemplar product categories were identified by MPS at <https://www.monolithicpower.com/en/products.html>

MPS Accused Product Categories/Types	
1.	Switching converters and controllers
2.	Multi-phase controllers
3.	Power management integrated circuits
4.	USB switches
5.	Load switches
6.	MOFSET drivers
7.	Isolated gate drivers
8.	Digital isolators
9.	Isolated DC/DC converters
10.	Power modules
11.	Battery chargers and monitors
12.	Fuel gauges
13.	Stepper motor drivers
14.	Brushless DC pre-drivers
15.	Brushless DC motor controllers
16.	Brushed DC drivers
17.	Fan drivers
18.	Backlight drivers
19.	Audio drivers
20.	Analog-to-digital converters
21.	Angular position sensors
22.	Current sensors

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

U.S. Patent No. 10,510,842	Accused Products MPS Semiconductor 86905 SiC N-Channel MOSFET
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905"). The 86905 was analyzed in the below referenced report from Tech Insights. MPS MP86905 Intelli-Phase™ Solution with Integrated HS/LS-FETs and Driver Power Essentials Summary ("MP86905 Report"), available at https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2202-801&genealogyCode=MPS-MP9502. The 86905 was also analyzed in a supplemental report from Tech Insights ("MP86905 Supplemental Report"). See Exhibit 8 (Supplemental Report for PEF-2202-801). The complete reports are hereby incorporated by reference into each and every claim and claim element discussed. Selected pages are reproduced herein to aid in understanding. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). The claimed invention would have application in numerous types of MPS products, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOSFET drivers, isolated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, and current sensors, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The MPS Accused Products, of which MPS 86905 is one example, are semiconductor devices.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 μm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO_2) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (R_{on}) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 μm drain-to-drain pitch and ~0.66 μm total polysilicon gate length, while the LSFET is arranged with ~3.4 μm drain-to-drain pitch and ~0.60 μm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 μm on a 0.86 μm contacted gate pitch, indicating the use of likely 0.18 μm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm $\times$ 3.97 mm $\times$ 0.86 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm $\times$ 3.14 mm (10.61 mm ²)
Die size (edge seal)	3.36 mm $\times$ 3.12 mm (10.48 mm ²)
Minimum measured transistor gate length/pitch	0.40 μm /0.86 μm
Process generation	Likely 0.18 μm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

5

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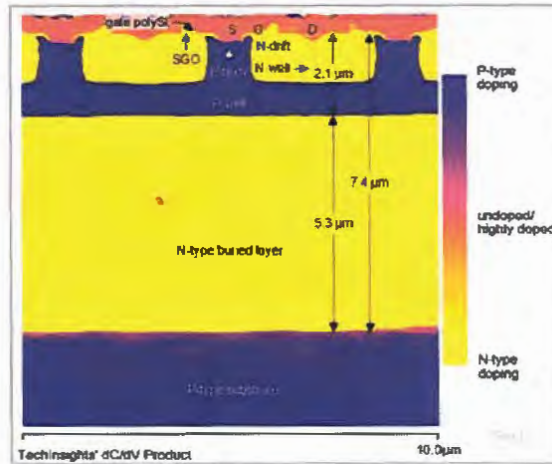
**Tech
Insights**

MP86905 Report at 5.

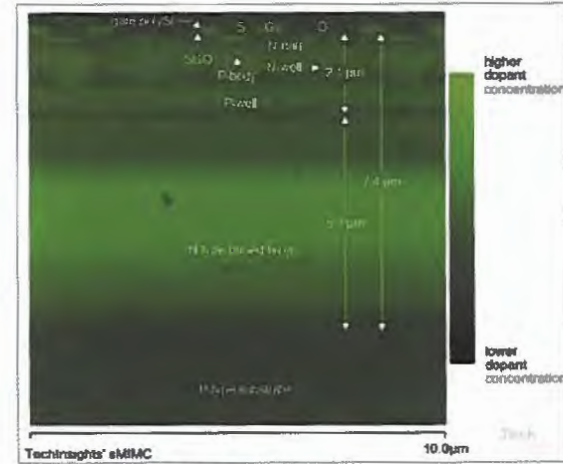
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts $\sim 2.1\ \mu\text{m}$ from the front surface, while the NBL measures $\sim 5.3\ \mu\text{m}$ thick and reaches $\sim 7.4\ \mu\text{m}$ deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A

Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

42

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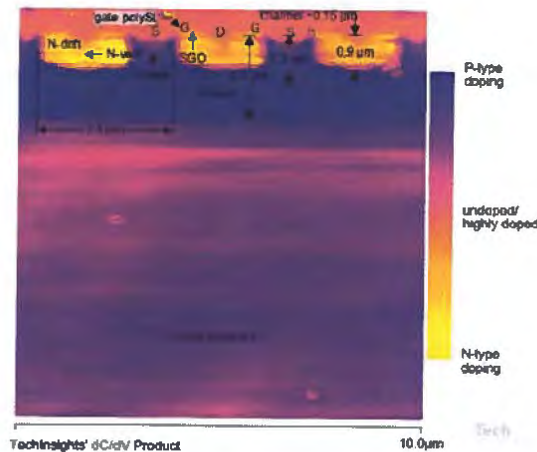
**Tech
Insights**

MP86905 Report at 42.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1 \mu\text{m}$ deep, the P-body is $\sim 1.3 \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9 \mu\text{m}$ deep, shallower than $1.2 \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15 \mu\text{m}$ in the LSFET array.

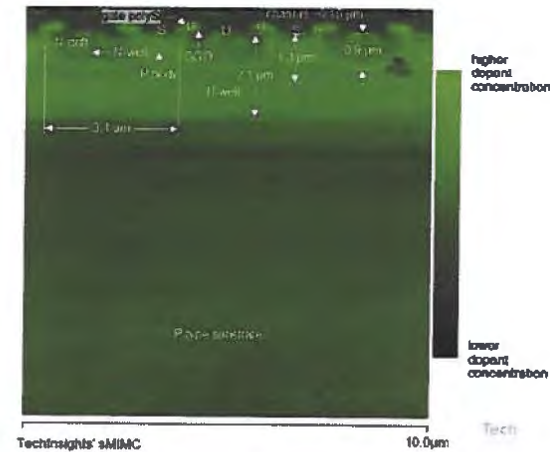


Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

2

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Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

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MP86905 Supplemental Report at 2.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm ($\pm 1.4\%$) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within $\pm 2\%$ of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of $0.3 \mu\text{m}$ (0.3%) for the micrometer's $100 \mu\text{m}$ pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately $\pm 5\%$ or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

3

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MP86905 Supplemental Report at 3.

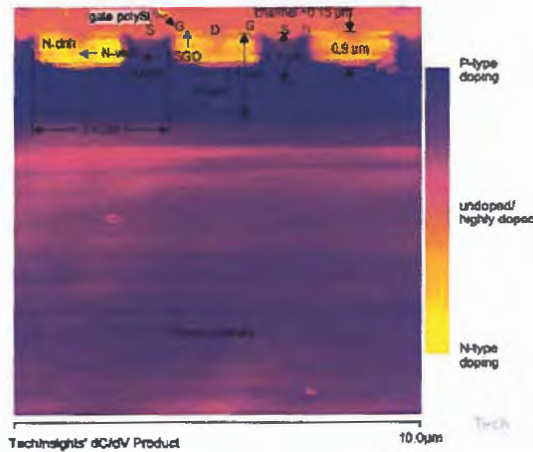
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;

The MPS Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary MPS Accused Product (the MPS 86905 discussed above) reveals the presence of such a substrate. For example, the MPS 86905 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

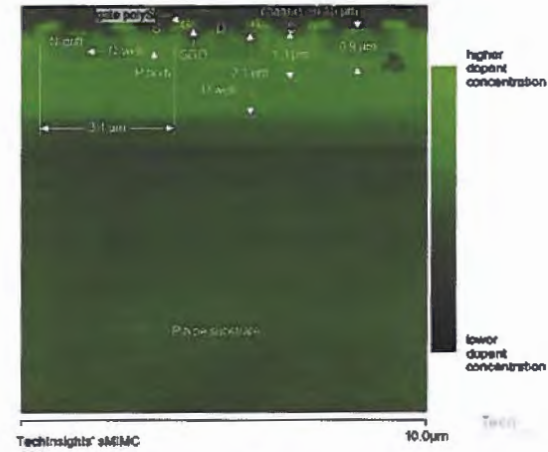
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1\ \mu\text{m}$ deep, the P-body is $\sim 1.3\ \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9\ \mu\text{m}$ deep, shallower than $1.2\ \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15\ \mu\text{m}$ in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png
LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png
LSFET Array – sMIM-C Cross-Section A-A

Tech Insights

2

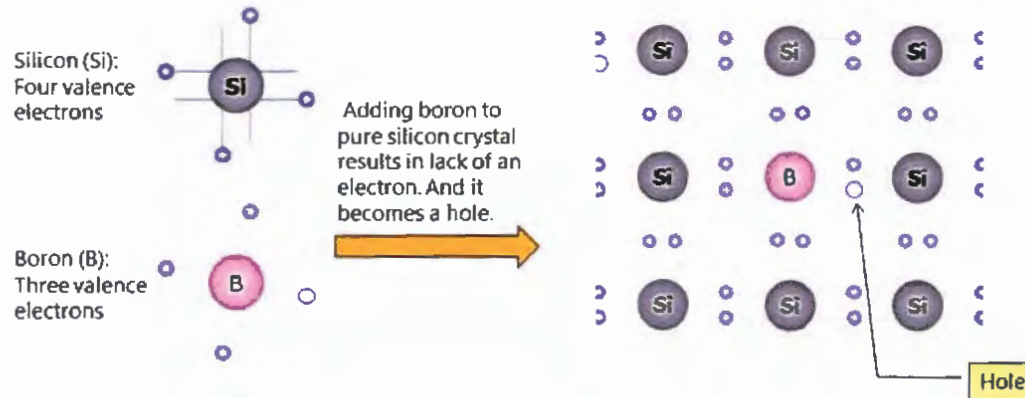
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MP86905 Supplemental Report at 2.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

What is a p-type Semiconductor?

A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "+" electrode in sequence.



* This hole is the carrier of a p-type semiconductor.

See <https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.>

[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which

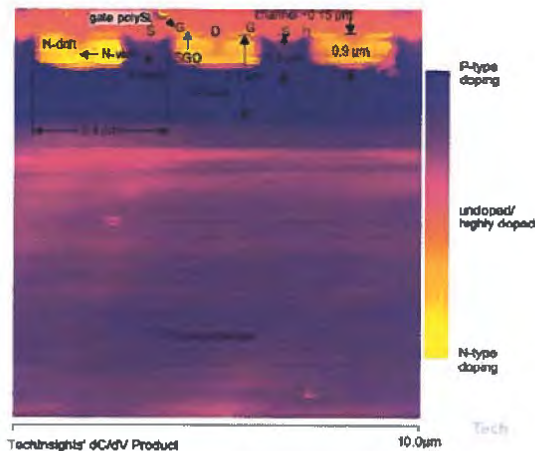
The MPS Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary MPS 86905 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "HSFET Array," and toward the top the source ("S"), gate ("g") and drain ("drain") where the transistors are, underneath each of the annotations are active regions. See also below showing "LSFET Array."

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

transistors can
be formed;

MP9502 Die LSFET Array – P- and N-Type Regions

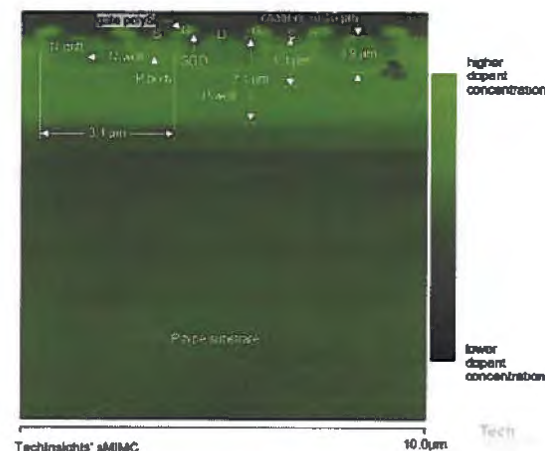
- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1 \mu\text{m}$ deep, the P-body is $\sim 1.3 \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9 \mu\text{m}$ deep, shallower than $1.2 \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15 \mu\text{m}$ in the LSFET array.



Technisights' dCAdV Product
Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png
LSFET Array – SCM Cross-Section A-A

2

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Technisights' sMIMC
Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png
LSFET Array – sMIM-C Cross-Section A-A

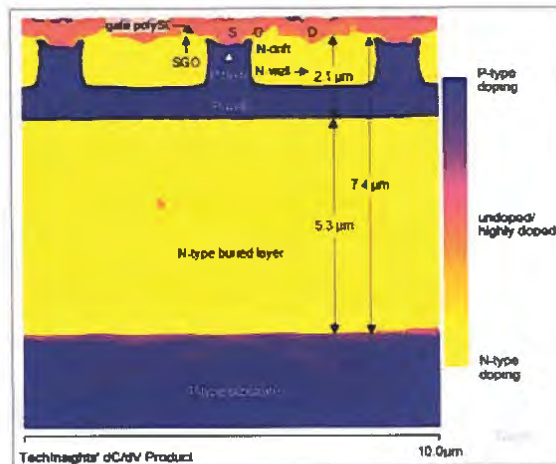
**Tech
Insights**

MP86905 Supplemental Report at 2.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

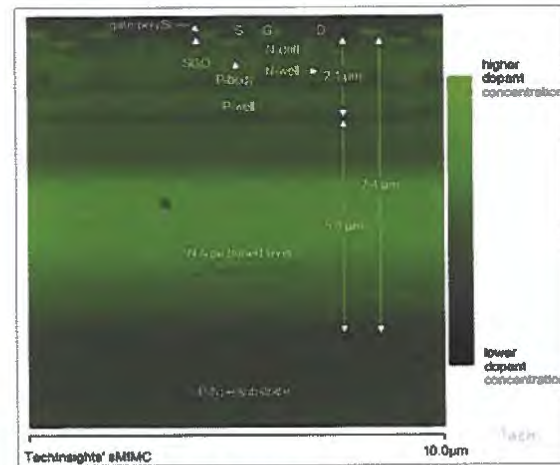
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts $\sim 2.1 \mu\text{m}$ from the front surface, while the NBL measures $\sim 5.3 \mu\text{m}$ thick and reaches $\sim 7.4 \mu\text{m}$ deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

42

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MP86905 Report at 42.

[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and

The MPS Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the HSFET and LSFET arrays shown in the images reproduced at Claim 1, Element 2 shows multiple transistors with active regions.

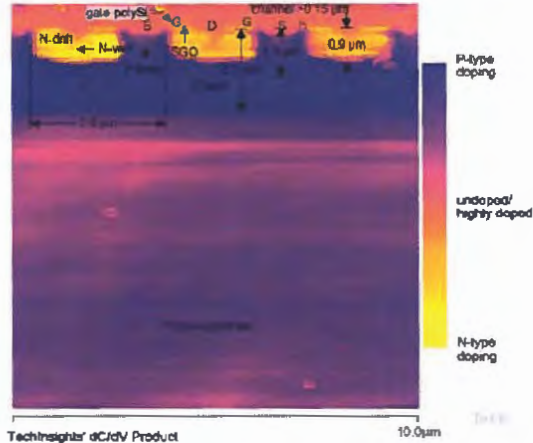
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. <i>See</i> above at Preamble, Elements 2-3 (discussing the HSFET AND LSFET arrays).
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The MPS Accused Products meet this limitation. <i>See</i> above at Element 1. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps, which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from MPS Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the sMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Zooming in on the sMIM-C image taken from page 43 of the Tech Insights report clearly shows vertical dopant grading in the active regions surrounding the source, gate, and drain. The image of the LSFET array (reproduced below) also shows grading near the source and drain and in wells.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

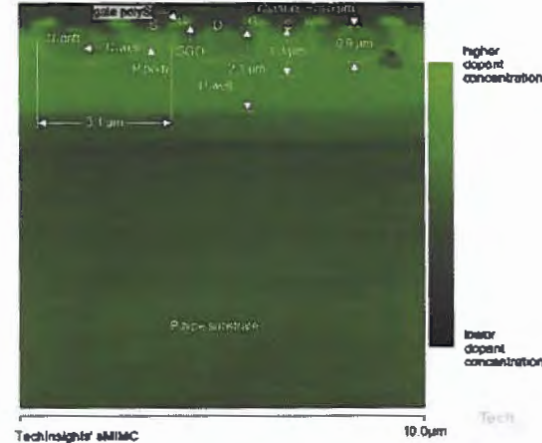
MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array
- The P-well is $\sim 2.1 \mu\text{m}$ deep, the P-body is $\sim 1.3 \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9 \mu\text{m}$ deep, shallower than $1.2 \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15 \mu\text{m}$ in the LSFET array.



Techninsight's dC/dV Product
 Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png
 LSFET Array – SCM Cross-Section A-A

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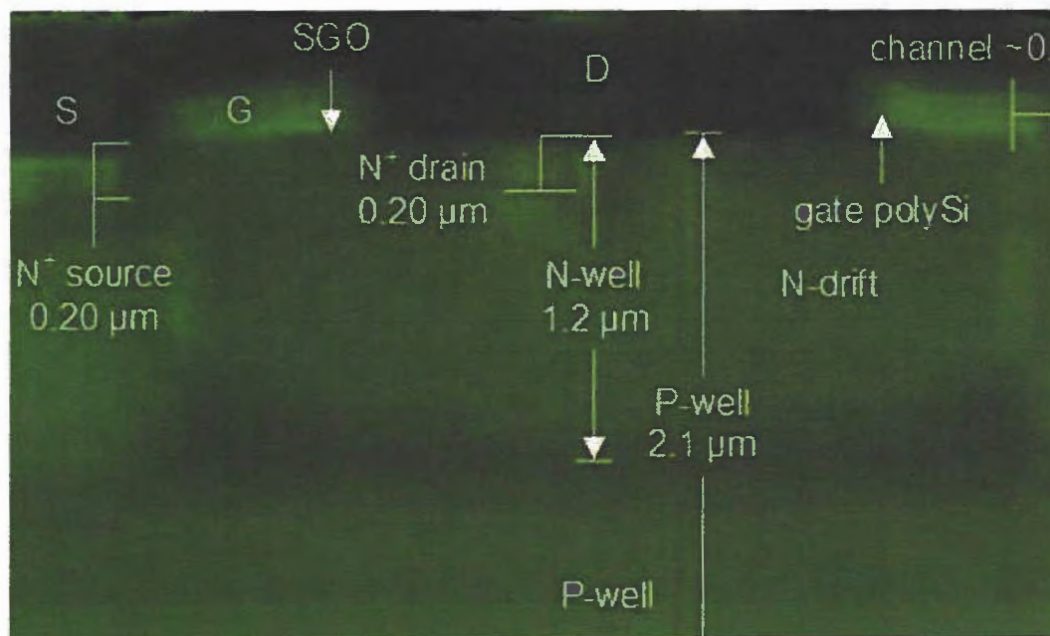
Techninsight's sMIMC
 Array_2_040622155352_SMIMC_FRW_10.0u_512p_400973.png
 LSFET Array – sMIM-C Cross-Section A-A

Tech
 Insights

MP86905 Supplemental Report at 2.

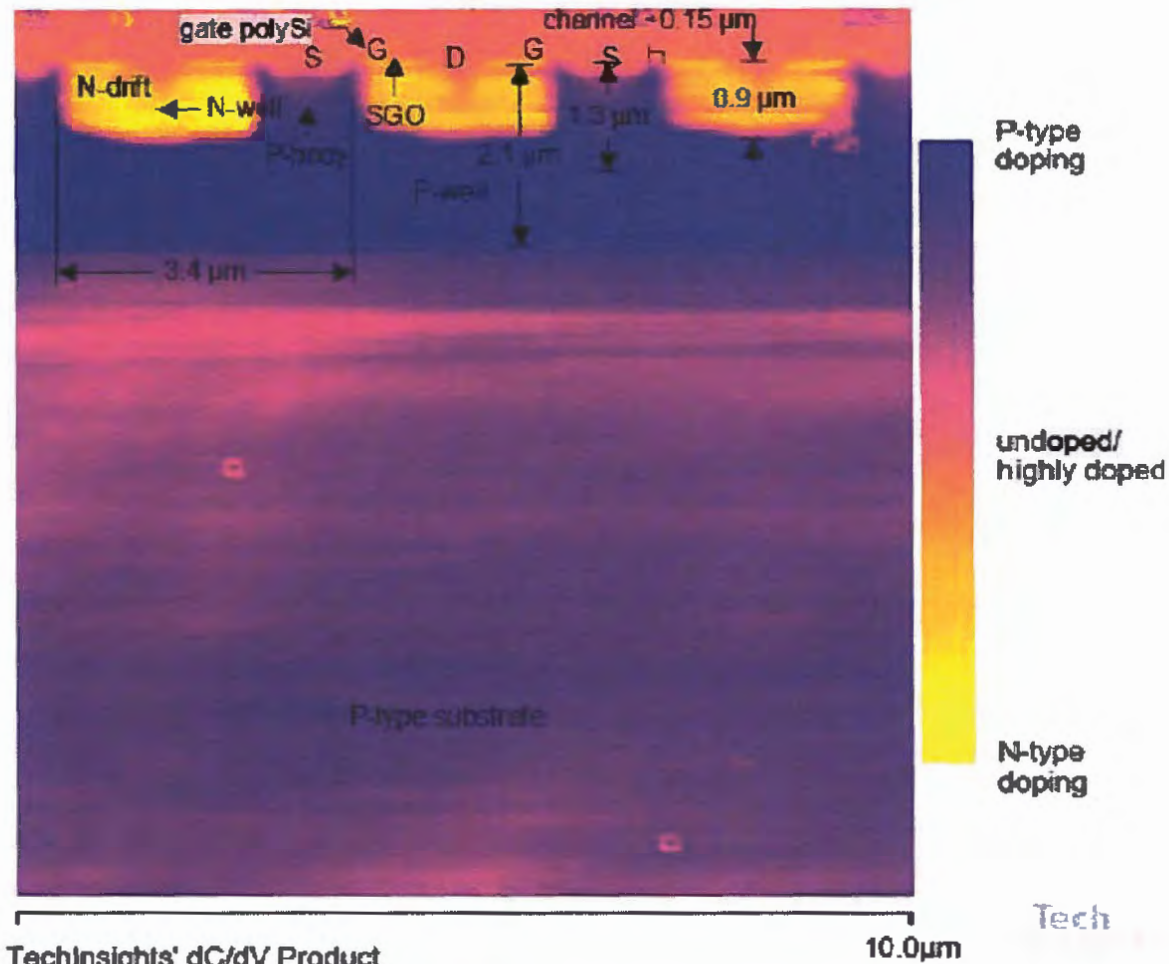
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

(Zoomed in near active regions on image from page 43)



MP86905 Report at 43.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)



TechInsights' dC/dV Product

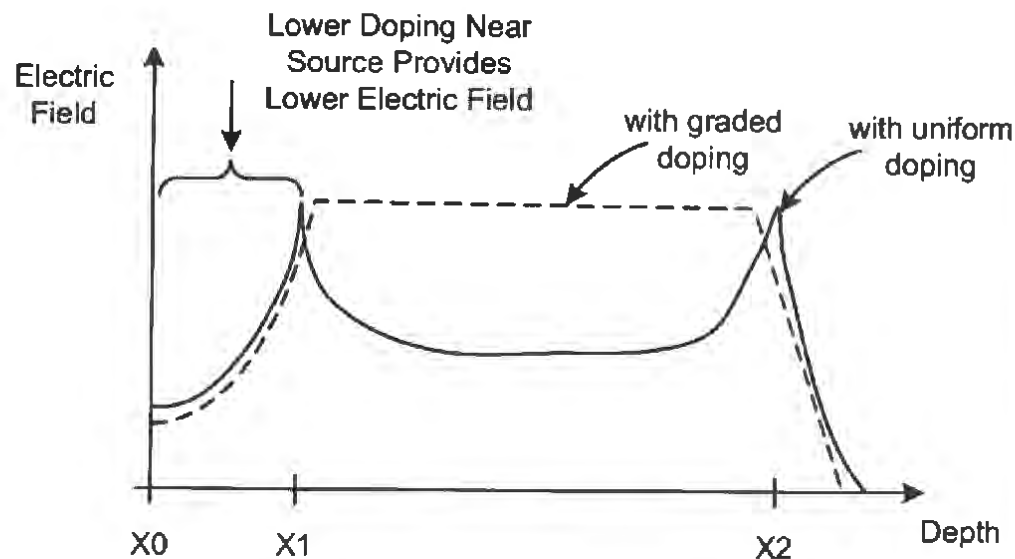
Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

MP86905 Report at 43.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Additionally, MPS' annual report states that it seeks patent protection based on its product designs designs: "In general, we have elected to pursue patent protection for aspects of our circuit and device designs that we believe are patentable." See MPS "2021 ANNUAL REPORT ON FORM 10-K" at 4. Therefore, the purported inventions described in MPS's patents are an indication of how its products operate. The descriptions of MPS's purported inventions in its patent applications confirm that its products meet this limitation. For example, Figure 5 of MPS U.S. Patent No. 8,704,292 (below) clearly shows the use of graded dopants in active and well regions for the purposes of creating electric fields to aid carrier movement. The patent recites that "The dashed line in FIG.5 shows a uniform electric field distribution associated with an example drift region doping profile."

**FIG. 5**

2. The semiconductor device of claim 1, wherein the substrate is a

Upon information and belief, the substrate of the semiconductor device of the MPS Accused Products is a p-type substance, as discussed above and shown in SCM/sMIM analysis above.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

p-type substrate.																															
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	Upon information and belief, the substrate of the MPS Accused Products has epitaxial silicon on top of a nonepitaxial substrate. For example, the device summary shown below includes an upper epitaxy layer. Device Summary - This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2]. - The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe - The MP9502 die substrate is ~155 μm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region - One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer. - The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3]. - The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 μm drain-to-drain pitch and ~0.66 μm total polysilicon gate length, while the LSFET is arranged with ~3.4 μm drain-to-drain pitch and ~0.60 μm total polysilicon gate length in total - In the logic region, the minimum observed gate length is 0.40 μm on a 0.86 μm contacted gate pitch, indicating the use of likely 0.18 μm process generation with relaxed feature dimensions. <table border="1"> <tr><td>Manufacturer</td><td>Monolithic Power Systems</td></tr> <tr><td>Part number</td><td>MP86905</td></tr> <tr><td>Foundry</td><td>Unknown</td></tr> <tr><td>Type</td><td>PMIC</td></tr> <tr><td>Date code</td><td>H39 (week 39 of 2017)</td></tr> <tr><td>Package type</td><td>23-pin FC-QFN</td></tr> <tr><td>Package markings</td><td>MPSH39 M86905 54U403</td></tr> <tr><td>Package dimensions</td><td>3.97 mm $\times$ 3.97 mm $\times$ 0.88 mm (thick)</td></tr> <tr><td>Die markings</td><td>MP9502 2013 <MPS logo></td></tr> <tr><td>Die size (whole die)</td><td>3.38 mm $\times$ 3.14 mm (10.61 mm²)</td></tr> <tr><td>Die size (edge seal)</td><td>3.36 mm $\times$ 3.12 mm (10.48 mm²)</td></tr> <tr><td>Minimum measured transistor gate length/pitch</td><td>0.40 μm/0.86 μm</td></tr> <tr><td>Process generation</td><td>Likely 0.18 μm process generation with relaxed feature dimensions</td></tr> <tr><td>Feature measured to determine process generation</td><td>Contacted gate pitch, use of CoSi contacts, STI isolation</td></tr> <tr><td>Maximum voltage [2]</td><td>18 V</td></tr> </table> 5 All content © 2022 TechInsights Inc. All rights reserved. Tech Insights	Manufacturer	Monolithic Power Systems	Part number	MP86905	Foundry	Unknown	Type	PMIC	Date code	H39 (week 39 of 2017)	Package type	23-pin FC-QFN	Package markings	MPSH39 M86905 54U403	Package dimensions	3.97 mm $\times$ 3.97 mm $\times$ 0.88 mm (thick)	Die markings	MP9502 2013 <MPS logo>	Die size (whole die)	3.38 mm $\times$ 3.14 mm (10.61 mm ²)	Die size (edge seal)	3.36 mm $\times$ 3.12 mm (10.48 mm ²)	Minimum measured transistor gate length/pitch	0.40 μm /0.86 μm	Process generation	Likely 0.18 μm process generation with relaxed feature dimensions	Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation	Maximum voltage [2]	18 V
Manufacturer	Monolithic Power Systems																														
Part number	MP86905																														
Foundry	Unknown																														
Type	PMIC																														
Date code	H39 (week 39 of 2017)																														
Package type	23-pin FC-QFN																														
Package markings	MPSH39 M86905 54U403																														
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Minimum measured transistor gate length/pitch	0.40 μm /0.86 μm																														
Process generation	Likely 0.18 μm process generation with relaxed feature dimensions																														
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation																														
Maximum voltage [2]	18 V																														
5. The semiconductor device of claim 1, wherein the first active	The MPS Accused Products meet this limitation. See above at Claim 2.																														

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

region and second active region contain one of either p-channel and n-channel devices.	
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The MPS Accused Products meet this limitation. As shown above, the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. <i>See</i> Tech Insights Report images reproduced above at Claim 1, Element 2.
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have graded dopants. <i>See</i> Tech Insights Report images reproduced above at Claim 1, Element 2 annotating "n-wells."

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the MPS's Accused Products. MPS's recent patent applications reference forming N regions and P regions by ion implantation. Information about the fabrication process for the MPS Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 1-3.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

which transistors can be formed in the surface thereof;	
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

concentration to aid carrier movement from the surface to the substrate.	
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and second active region contain	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 6.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the MPS Accused Products meet this limitation. <i>See</i> above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the MPS Accused Products meet this limitation. <i>See</i> above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 2-3.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

regions are formed adjacent the first surface of the substrate.	
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The MPS Accused Products meet this limitation. As discussed above for Claim 1, the MPS Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendant and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

U.S. Patent No. 10,734,481	Exemplary Accused Product MPS 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products constitute and are incorporated into semiconductor devices. This chart includes exemplary information regarding a representative example of the MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905"). The 86905 was analyzed in the below referenced report from Tech Insights. MPS MP86905 Intelli-Phase™ Solution with Integrated HS/LS-FETs and Driver Power Essentials Summary ("MP86905 Report"), available at https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2202-801&genealogyCode=MPS-MP9502. The 86905 was also analyzed in a supplemental report from Tech Insights ("MP86905 Supplemental Report"). See Exhibit 8 (Supplemental Report for PEF-2202-801). The complete reports are hereby incorporated by reference into each and every claim and claim element discussed. Selected pages are reproduced herein to aid in understanding. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart to achieve such performance enhancements (e.g., on and off switching times). The claimed invention would have application in numerous types of MPS products, including switching converters and controllers, multi-phase controllers, power management integrated circuits, USB switches, load switches, MOFSET drivers, insulated gate drivers, digital isolators, isolated DC/DC converters, power modules, battery chargers and monitors, fuel gauges, stepper motor drivers, brushless DC pre-drivers, brushless DC motor controllers, brushed DC drivers, fan drivers, backlight drivers, audio drivers, analog-to-digital converters, angular position sensors, and current sensors, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The MPS Accused Products, of which MPS 86905 is one example, are semiconductor devices.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 μm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (R_{on}) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 μm drain-to-drain pitch and ~0.66 μm total polysilicon gate length, while the LSFET is arranged with ~3.4 μm drain-to-drain pitch and ~0.60 μm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 μm on a 0.86 μm contacted gate pitch, indicating the use of likely 0.18 μm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm × 3.97 mm × 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm × 3.14 mm (10.61 mm ²)
Die size (edge seal)	3.36 mm × 3.12 mm (10.48 mm ²)
Minimum measured transistor gate length/pitch	0.40 μm /0.86 μm
Process generation	Likely 0.18 μm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

5

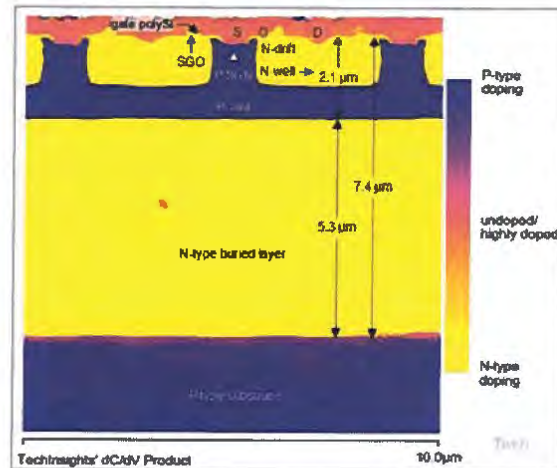
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MP86905 Report at 5.

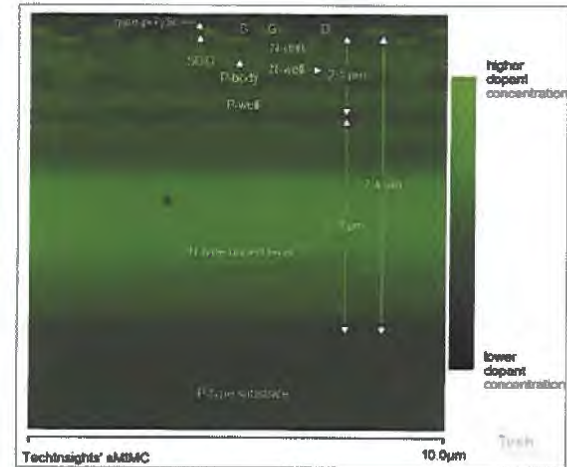
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts $\sim 2.1 \mu\text{m}$ from the front surface, while the NBL measures $\sim 5.3 \mu\text{m}$ thick and reaches $\sim 7.4 \mu\text{m}$ deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Technights' dCqV Product
Array_040522164608_PRODUCT_FRW_10.0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



Technights' sMIMC
Array_040522164608_SMIMC_FRW_10.0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

42

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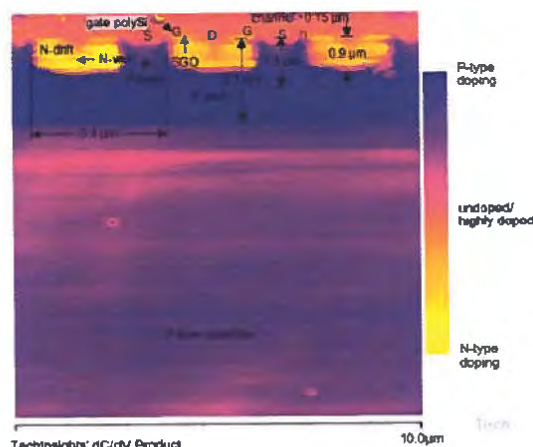
**Tech
Insights**

MP86905 Report at 42.

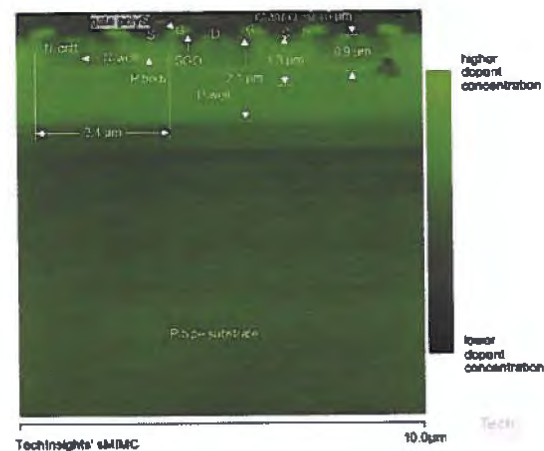
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1 \mu\text{m}$ deep, the P-body is $\sim 1.3 \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9 \mu\text{m}$ deep, shallower than $1.2 \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15 \mu\text{m}$ in the LSFET array.



LSFET Array – SCM Cross-Section A-A



LSFET Array – sMIM-C Cross-Section A-A

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2

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MP86905 Supplemental Report at 2.

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm ($\pm 1.4\%$) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within $\pm 2\%$ of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of $0.3 \mu\text{m}$ (0.3%) for the micrometer's $100 \mu\text{m}$ pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately $\pm 5\%$ or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (SMIM-C) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

3

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MP86905 Supplemental Report at 3.

[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;

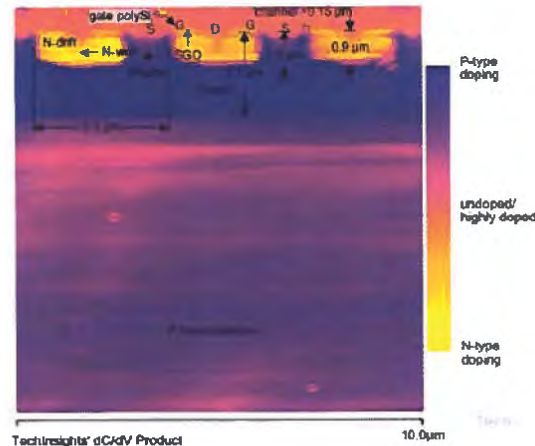
The MPS Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary MPS Accused Product (the MPS 86905 discussed above) reveals the presence of such a substrate.

For example, the MPS 86905 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1\ \mu\text{m}$ deep, the P-body is $\sim 1.3\ \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9\ \mu\text{m}$ deep, shallower than $1.2\ \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15\ \mu\text{m}$ in the LSFET array.

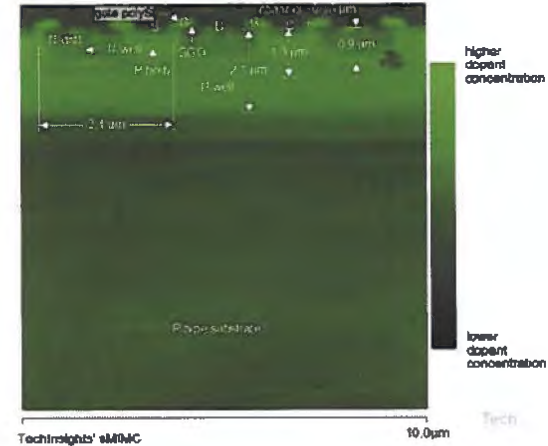


Array_2_040622155352_PRODUCT_FRW_10 0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

2

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Array_2_040622155352_SMIMC_FRW_10 0u_512p_400973.png

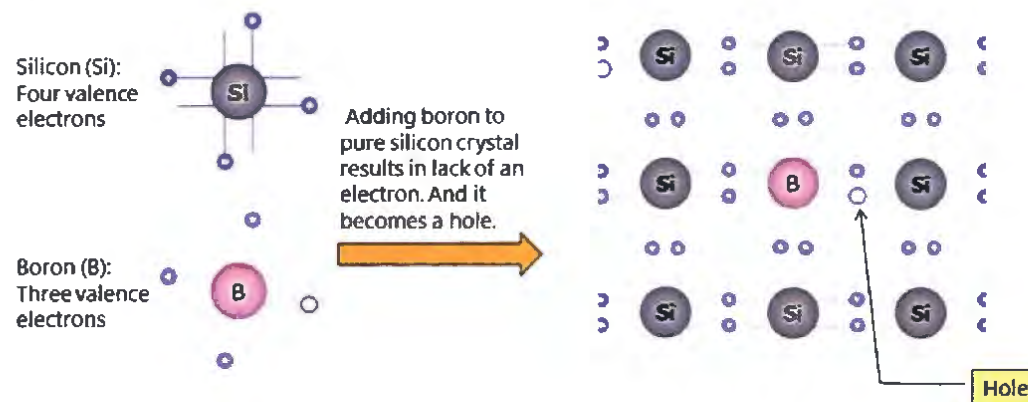
LSFET Array – sMIM-C Cross-Section A-A

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MP86905 Supplemental Report at 2.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)**What is a p-type Semiconductor?**

A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "+" electrode in sequence.



* This hole is the carrier of a p-type semiconductor.

See <https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.>

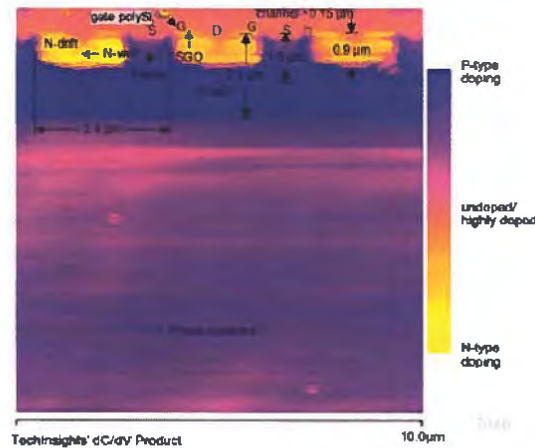
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

The MPS Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary MPS 86905 scanning capacitance/microwave impedance microscopy (SCM/SMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "HSFET Array," and toward the top the source ("S"), gate ("g") and drain ("drain") where the transistors are, underneath each of the annotations are active regions. See also below showing "LSFET Array."

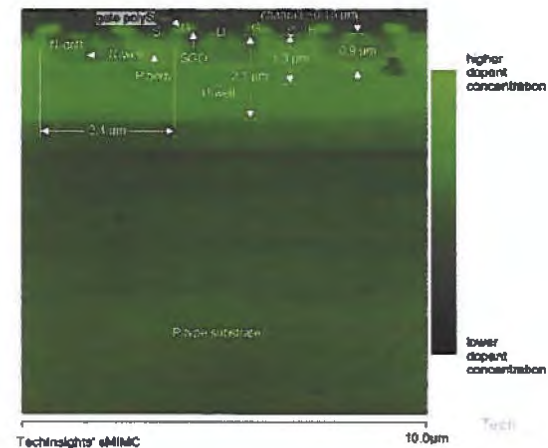
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1\ \mu\text{m}$ deep, the P-body is $\sim 1.3\ \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9\ \mu\text{m}$ deep, shallower than $1.2\ \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15\ \mu\text{m}$ in the LSFET array.



Array_2_040622155352_PRODUCT_FRW_10 0u_512p_400973.png
LSFET Array – SCM Cross-Section A-A



Array_2_040622155352_SMIMC_FRW_10 0u_512p_400973.png
LSFET Array – sMIM-C Cross-Section A-A

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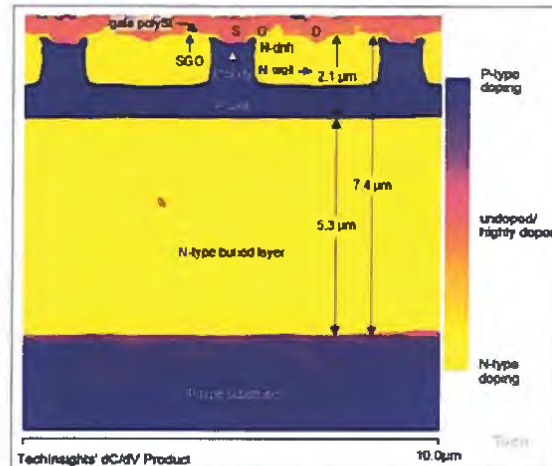
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MP86905 Supplemental Report at 2.

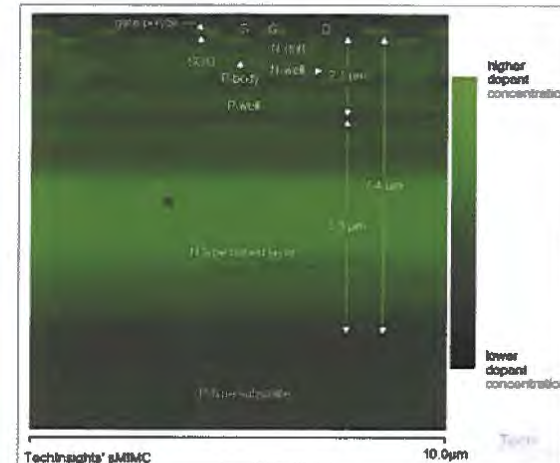
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts $\sim 2.1\ \mu\text{m}$ from the front surface, while the NBL measures $\sim 5.3\ \mu\text{m}$ thick and reaches $\sim 7.4\ \mu\text{m}$ deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



HSFET Array – SCM Cross-Section A-A



HSFET Array – sMIM-C Cross-Section A-A

brary

42

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MP86905 Report at 42.

[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region

The MPS Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the HSFET and LSFET arrays shown in the images reproduced at Claim 1, Element 2 shows multiple transistors with active regions.

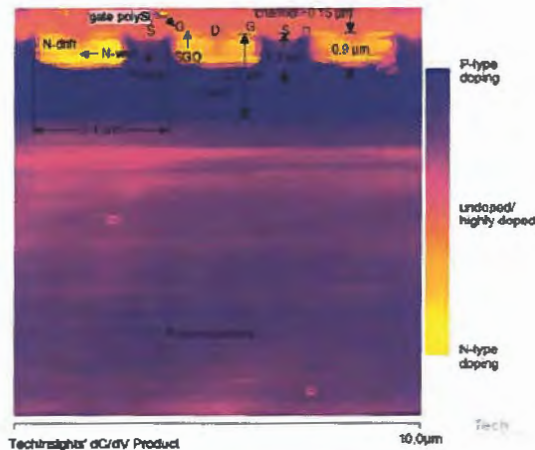
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. <i>See above at Preamble, Elements 2-3 (discussing the HSFET AND LSFET arrays).</i>
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The MPS Accused Products meet this limitation. <i>See above at Element 1.</i> For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps, which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from MPS Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the sMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. Zooming in on the sMIM-C image taken from page 43 of the Tech Insights report clearly shows vertical dopant grading in the active regions surrounding the source, gate, and drain. The image of the LSFET array (reproduced below) also shows grading near the source and drain and in wells.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1\ \mu\text{m}$ deep, the P-body is $\sim 1.3\ \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9\ \mu\text{m}$ deep, shallower than $1.2\ \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15\ \mu\text{m}$ in the LSFET array.

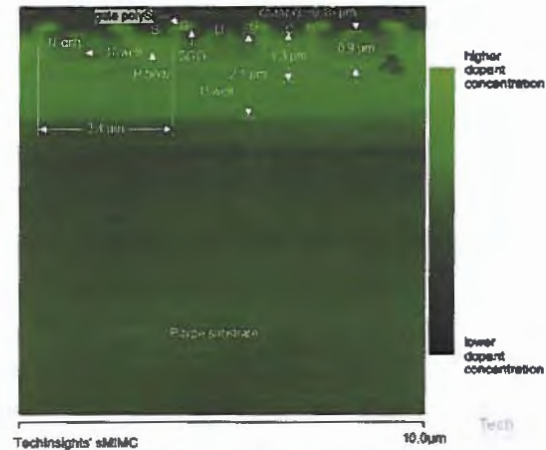


Technisights' dC/dV Product

10.0μm

Array_2_040622155352_PRODUCT_FRW_10 Du_512p_400973.png

LSFET Array – SCM Cross-Section A-A



Technisights' sMIMC

10.0μm

Array_2_040622155352_SMIMC_FRW_10 Du_512p_400973.png

LSFET Array – sMIM-C Cross-Section A-A

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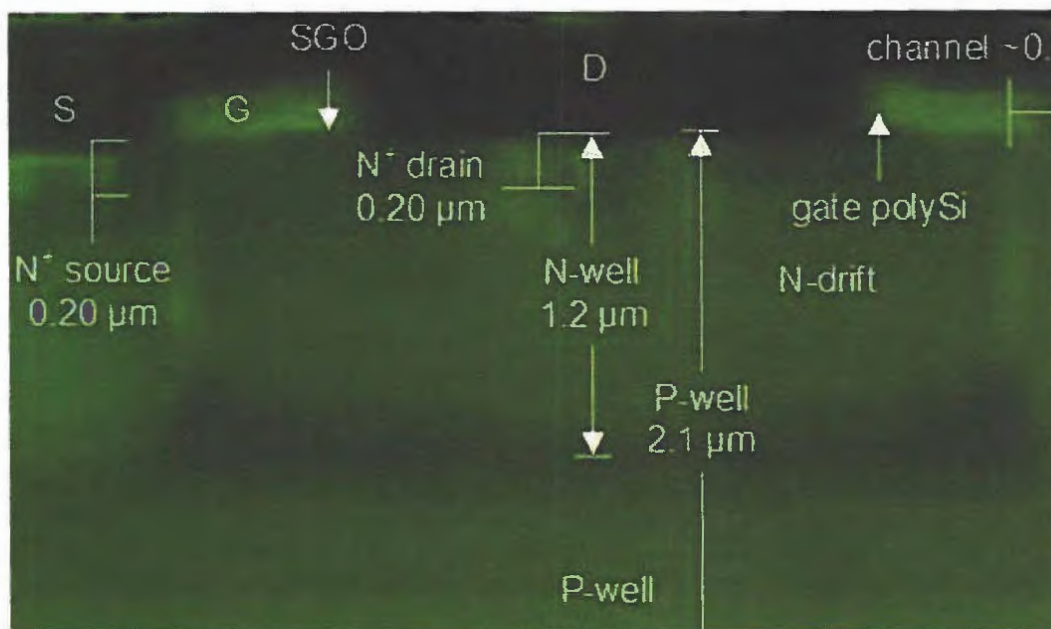
2

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MP86905 Supplemental Report at 2.

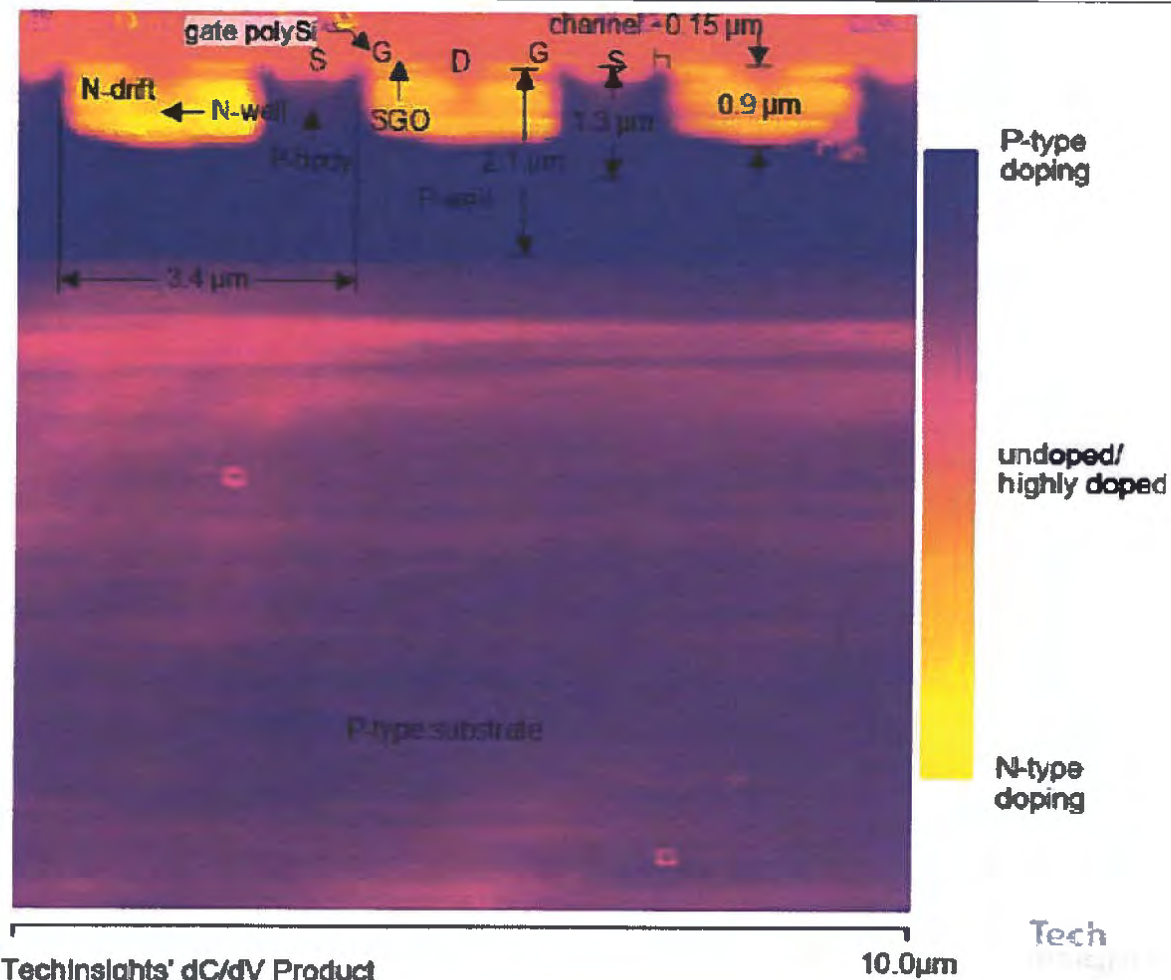
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

(Zoomed in near active regions on image from page 43)



MP86905 Report at 43.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)



TechInsights' dC/dV Product

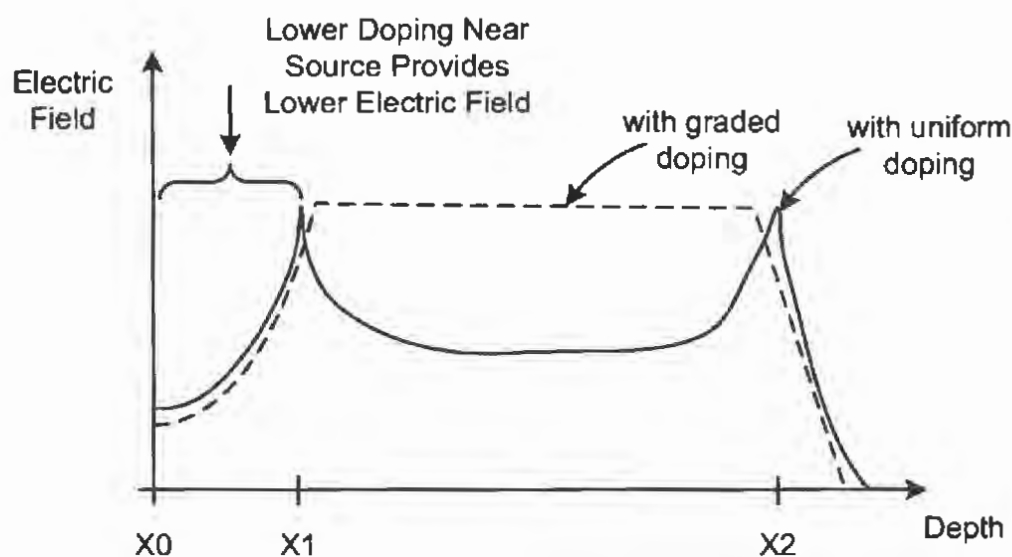
Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

MP86905 Report at 43.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

Additionally, MPS' annual report states that it seeks patent protection based on its product designs designs: "In general, we have elected to pursue patent protection for aspects of our circuit and device designs that we believe are patentable." See MPS "2021 ANNUAL REPORT ON FORM 10-K" at 4. Therefore, the purported inventions described in MPS's patents are an indication of how its products operate. The descriptions of MPS's purported inventions in its patent applications confirm that its products meet this limitation. For example, Figure 5 of MPS U.S. Patent No. 8,704,292 (below) clearly shows the use of graded dopants in active and well regions for the purposes of creating electric fields to aid carrier movement. The patent recites that "The dashed line in FIG.5 shows a uniform electric field distribution associated with an example drift region doping profile."



[Claim 1,
Element 6] at

The MPS Accused Products include a semiconductor device comprising at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. The images of the HSFET and LESFET arrays reproduced below (and above) clearly show dopant grading in the well regions. Likewise, Figure 5 from MPS's '292 patent

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

shows grading in a well region.

(Zoomed in near active regions on image from page 43)

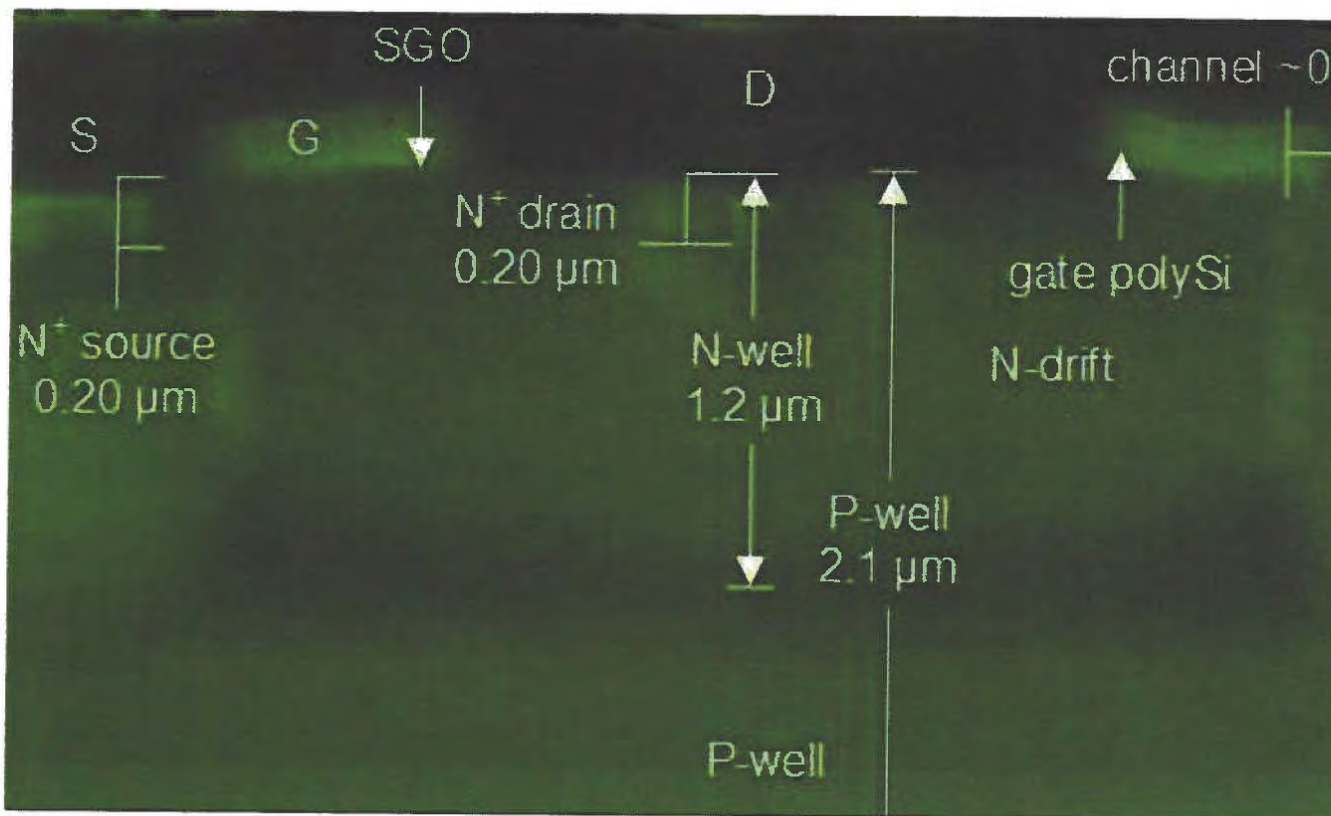
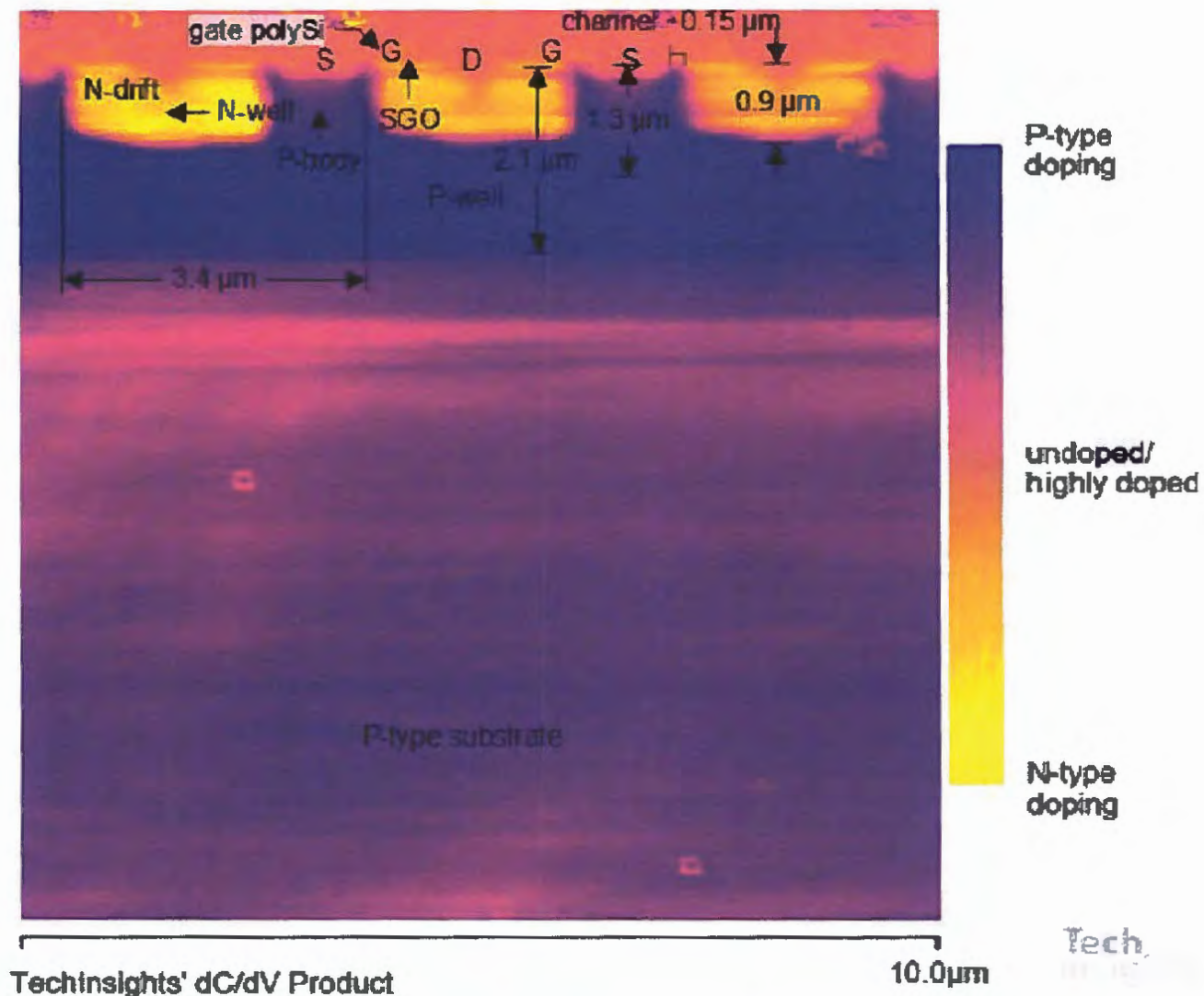


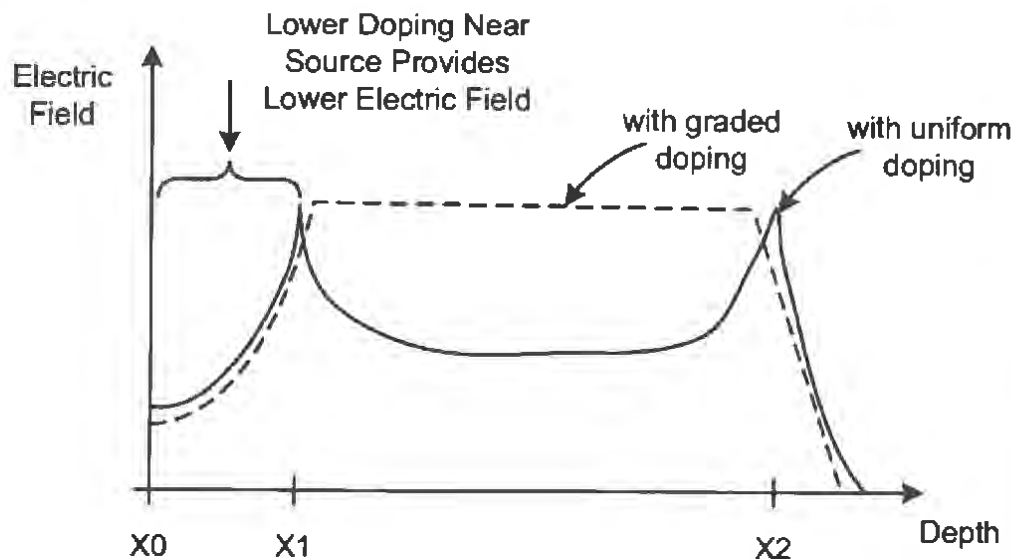
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)



Array_2_040622155352_PRODUCT_FRW_10.0u_512p_400973.png

LSFET Array – SCM Cross-Section A-A

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**FIG. 5**

2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

Upon information and belief, the substrate of the semiconductor device of the MPS Accused Products is a p-type substance, as discussed above and shown in SCM/sMIM analysis above.

3. The semiconductor device of claim 1, wherein the substrate has

Upon information and belief, the substrate of the MPS Accused Products has epitaxial silicon on top of a nonepitaxial substrate. For example, the device summary shown below includes an upper epitaxy layer.

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epitaxial silicon
on top of a
nonepitaxial
substrate.

Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 μm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (R_{on}) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 μm drain-to-drain pitch and ~0.66 μm total polysilicon gate length, while the LSFET is arranged with ~3.4 μm drain-to-drain pitch and ~0.60 μm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 μm on a 0.86 μm contacted gate pitch, indicating the use of likely 0.18 μm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm $\times$ 3.97 mm $\times$ 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm $\times$ 3.14 mm (10.61 mm ²)
Die size (edge seal)	3.36 mm $\times$ 3.12 mm (10.48 mm ²)
Minimum measured transistor gate length/pitch	0.40 μm /0.86 μm
Process generation	Likely 0.18 μm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

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4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.

The MPS Accused Products meet this limitation. See above at Claim 2.

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5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The MPS Accused Products meet this limitation. As shown above, the sources and drains are n-doped and therefore the device is p-channel. The first and second active regions accordingly contains p-channel devices. <i>See</i> Tech Insights Report images reproduced above at Claim 1, Element 2.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. The first active region and second active region have n-type dopant and contain p-channel devices in n-wells. The wells have graded dopants. <i>See</i> Tech Insights Report images reproduced above at Claim 1, Element 2 annotating "n-wells."
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the MPS's Accused Products. MPS's recent patent applications reference forming N regions and P regions by ion implantation. Information about the fabrication process for the MPS Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.
8. The semiconductor device of claim	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 1-3.

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1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. As shown by the images obtained by SPM/sMIM analysis (<i>see</i> above at Claim 1, Element 5), the MPS Accused Products show blocks of highly n-doped and p-doped wells.
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. As discussed above for Claim 1, the MPS Accused Products include first and second active regions. Upon information and belief, CMOS transistors are formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendant and are expected to be obtained through discovery.
15. The semiconductor device of claim 1, wherein the device is a	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 3 (regarding epitaxy) and Claim 13 (regarding CMOS).

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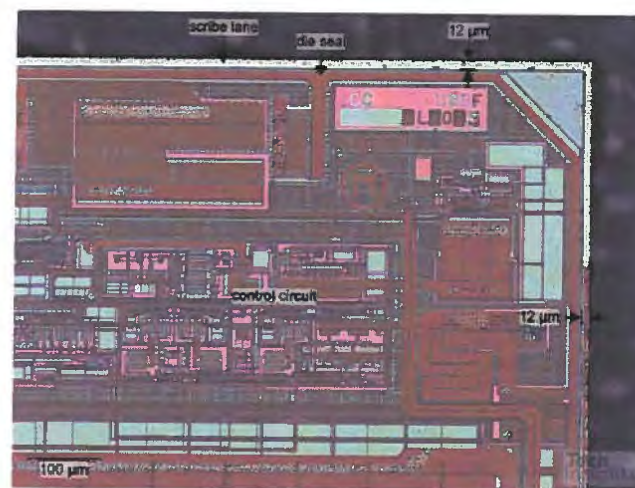
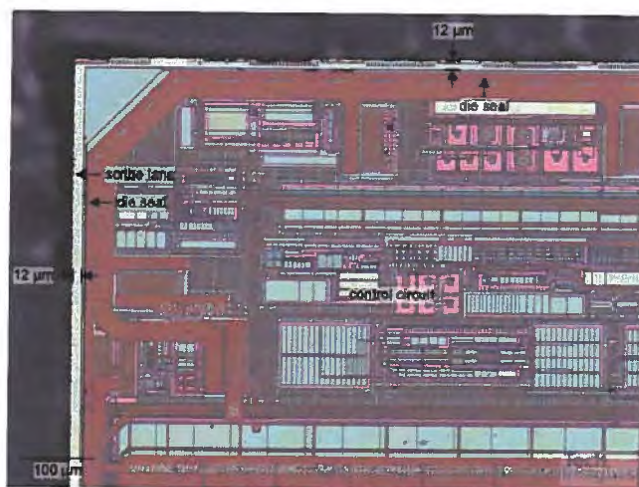
complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

17. The semiconductor device of claim 1, wherein the device is a logic device.

Upon information and belief, the MPS's Accused Products comprise a logic device. For example, the image below displays a "control circuit" region.

MP9502 Die Upper Corners

- The scribe lane measures ~12 μm wide all around the die.
- The control circuit is at the top portion of the die.



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[Claim 20,
Preamble] A
semiconductor

To the extent the preamble is a limitation, the MPS Accused Products include/comprise a semiconductor device. See above at Claim 1, Preamble.

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device, comprising:	
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be	The MPS Accused Products meet this limitation. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of Defendant and are expected to be obtained through discovery.

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formed in the surface thereof;	
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 6.

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the first surface to the second surface of the substrate.	
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The MPS Accused Products meet this limitation. See above at Claim 1, Element 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. See above at Claim 3.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. See above at Claim 4.
25. The semiconductor device of claim 20, wherein the first active region and second active region	The MPS Accused Products meet this limitation. See above at Claim 5.

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contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 6.
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 7.

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implantation process.	
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 13.
34. The semiconductor device of claim 20, wherein the device is a logic device.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 17.

Exhibit A-3 to Greenthread's Complaint

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[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a VLSI semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble) with transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendant and are expected to be obtained through discovery. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.

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active region or second active region;	
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. <i>See</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the MPS Accused Products are in the possession of the Defendant and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. <i>See</i> above at Claim 1, Element 6.
5. The VLSI semiconductor device of claim 1, wherein the	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6.

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first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. <i>See</i> above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The MPS Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. <i>See</i> above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the MPS Accused Products are in the possession of the Defendant and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The MPS Accused Products meet this limitation. As shown by SEM imaging (<i>see</i> Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. <i>See</i> above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 3.

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first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. As shown by SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SCM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5.

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first active region and second active region contain at least one of either p-channel and n-channel devices.	
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. <i>See Exhibit A-1, Claim 6.</i>
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. <i>See Exhibit A-1, Claim 7.</i>
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The MPS Accused Products meet this limitation. <i>See Exhibit A-2, Claim 9.</i>
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. <i>See Exhibit A-1, Claim 8.</i>
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The MPS Accused Products meet this limitation. <i>See Exhibit A-2, Claim 15.</i>

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34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5; <i>see</i> above at Claim 21, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

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one substrate area where there is no active region.	
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.

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[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having	The MPS Accused Products meet this limitation. SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a CMOS Semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 1.
[Claim 44, Element 2] a substrate;	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 44, Element 1.
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 5. Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The MPS Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants. Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a CMOS semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-3 is a semiconductor device (see Exhibit A-1, Claim 1, Preamble and Exhibit A-3, Claim 44, Preamble) with transistors, and is a CMOS semiconductor device upon information and belief. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The MPS Accused Products meet this limitation. See Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The MPS Accused Products meet this limitation. See Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The MPS Accused Products meet this limitation. See Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority	The MPS Accused Products meet this limitation. See Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (see Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. See also SCM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
carriers from said surface layer to said substrate; and	
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendant and are expected to be obtained through discovery. <i>See also</i> SCM/SMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The MPS Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the MPS Accused Products include a semiconductor device. The MPS Semiconductor 86905 Intelli-Phase Solution with integrated HS/LS-FETs and Driver ("86905") discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble) with transistors, and is a semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendant and are expected to be obtained through discovery. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The MPS Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendant and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the MPS Accused Products include an electronic system. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each MPS Accused Product is an electronic system. This chart includes exemplary information regarding a representative example of the MPS Accused Products, the MPS 86905. The MPS 86905 is representative of the MPS Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other MPS Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other MPS Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Similarly, the other MPS Accused Products (including MPS Accused Products) would have been designed in a similar manner as the MPS 86905 for purposes of this claim chart because to achieve such performance enhancements (e.g., on and off switching times). Therefore, upon information and belief the other MPS Accused Products contain similar features as the MPS 86905 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other MPS Accused Products contain similar features as the MPS 86905, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 4.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 5.
6. The system of Claim 1, wherein the first active region and second active region of the at least one	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 6.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
semiconductor device are each separated by at least one isolation region.	
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 15.
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 16.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 20.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
semiconductor device are in the lateral or vertical direction.	
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the MPS Accused Products include an electronic system. <i>See above at Claim 1, Preamble.</i>
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1a.</i>
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1b.</i>
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.</i>
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.</i>
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1e.</i>
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. See also SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</i>
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface	The MPS Accused Products meet this limitation. <i>See above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. See also SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.</i>

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 26.
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one	The MPS Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 28.

Exhibit A-6 to Greenthread's Complaint

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semiconductor device are either p-type or n-type.	



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Monolithic Power Systems MP86905 Intelli-Phase™ Solution with Integrated HS/LS-FETs and Driver

Power Essentials Summary

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**Tech
Insights**

Overview

This a Power Essentials (PEF) summary document, provided as a companion deliverable for Power Essentials projects. The complete PEF deliverable includes this document, which provides a summary of observed device metrics and salient features, the summary is supported by the following unannotated image folders:

- Package optical photographs, package X-ray images, die photographs, optical photos of die feature image set
- Plan-view images of the device delayed to the gate level
- Exploratory cross-sectional scanning electron microscope (SEM) images of the device structure
- Detailed cross-sectional scanning capacitance microscopy (SCM) and scanning microwave impedance microscopy (sMIM-C) analysis of the dopant structures
- Detailed cross-sectional transmission electron microscope (TEM) images of the power device structure
- Metal and dielectric layer composition identification based on TEM-EDS results

The image set for a standard PEF project is derived from a beveled sample for SEM planar analysis, one plane of cross-sectioning for SEM structural analysis, a single TEM sample for the detailed structural analysis, and planar and cross-sectional SCM and sMIM analysis. Value added information, such as additional planes of cross-sectioning, may be included on a case-by-case basis.

The Power Essentials deliverable provides basic competitive benchmarking information and enables cost-effective tracking of multiple competitors' technology.

Company Profile

- Monolithic Power Systems (MPS) is a global analog semiconductor company founded in 1997 by Michael Hsing and headquartered in Kirkland, Washington, U.S. The company provides semiconductor-based power electronics circuit for systems found in cloud computing, telecom infrastructures, automotive, industrial applications and consumer applications [1]. As of the end of December 2021, MPS reported an annual sales figure of \$1.21 billion and had 2,209 employees in 2020.



Device Summary

- This report presents a Power Essentials analysis of the MPS MP86905 silicon (Si)-based power management IC (PMIC). The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers and is ideally suited for multi-phase buck regulators. It offers 50 A continuous output current over a wide 4.5 V to 16 V operating input range [2].
- The MP86905 comprises a single die with MP9502 die markings, which are encapsulated in a 23-pin flip-chip quad-flat-no-lead (FC-QFN) package with likely copper (Cu) bumping directly to the leadframe.
- The MP9502 die substrate is ~155 μm thick including the upper epitaxy layer and uses Bipolar-CMOS-DMOS (BCD) technology. It features a single layer of polysilicon in the analyzed regions, three aluminum (Al) metal layers, tungsten (W) contacts and vias, cobalt silicide (CoSi) at the source, drain, and polysilicon contact regions. The pre-metal dielectric (PMD) uses silicon oxide (SiO) layers, while the inter-metal dielectric (IMD) layers uses oxide as well. Isolation structures include shallow trench isolation (STI) in the logic region.
- One group of high side MOSFET (HSFET) array and two groups of low side MOSFET (LSFET) array are used on the die. The structure and dopants of the HS/LS FET arrays are analyzed. Dopant analysis in the HS/LS FET array region shows the use of a P-type substrate, an N-type buried layer (NBL), a N-drift/N-well layer and a P-well layer.
- The stepped-gate-oxide (SGO) is used in the LDMOS devices on this die. The use of SGO allows a reduction of on-resistance (Ron) compared with the conventional STI LDMOS [3].
- The HSFET is arranged in a one-dimensional (1D) array with a ~4.0 μm drain-to-drain pitch and ~0.66 μm total polysilicon gate length, while the LSFET is arranged with ~3.4 μm drain-to-drain pitch and ~0.60 μm total polysilicon gate length in total.
- In the logic region, the minimum observed gate length is 0.40 μm on a 0.86 μm contacted gate pitch, indicating the use of likely 0.18 μm process generation with relaxed feature dimensions.

Manufacturer	Monolithic Power Systems
Part number	MP86905
Foundry	Unknown
Type	PMIC
Date code	H39 (week 39 of 2017)
Package type	23-pin FC-QFN
Package markings	MPSH39 M86905 54U403
Package dimensions	3.97 mm $\times$ 3.97 mm $\times$ 0.88 mm (thick)
Die markings	MP9502 2013 <MPS logo>
Die size (whole die)	3.38 mm $\times$ 3.14 mm (10.61 mm ²)
Die size (edge seal)	3.36 mm $\times$ 3.12 mm (10.48 mm ²)
Minimum measured transistor gate length/pitch	0.40 μm /0.86 μm
Process generation	Likely 0.18 μm process generation with relaxed feature dimensions
Feature measured to determine process generation	Contacted gate pitch, use of CoSi contacts, STI isolation
Maximum voltage [2]	18 V

**Tech
Insights**

Observed Critical Dimensions – CMOS/LDMOS

Feature	Material Composition	Dimension (μm)
Gate length	Polysilicon	0.40
Contacted gate pitch	–	0.86
SWS widths	SiO/SiN	15 nm/70 nm
Polysilicon thickness	Si	0.18
STI depth	SiO	0.36

CMOS

Feature	Material Composition	Dimension (μm)
Cell pitch	–	4.0/3.4 (HS/LS)
Channel length	–	~0.17
Polysilicon thickness	Si	0.18
Polysilicon width	Si	0.66/0.60 (HS/LS)
Gate dielectric thickness	SiO	8.5 nm
SWS widths	SiO/SiN	15 nm/70 nm
CESL thickness	SiN	33 nm
Gate and contact silicide depth	CoSi	≤ 30 nm
SGO thickness	SiO	40 nm
N ⁺ S/D depth	–	0.20
N-well/N-drift depth	–	1.2
P-well depth	–	2.1
P-body depth	–	1.3

Output Channel LDMOS

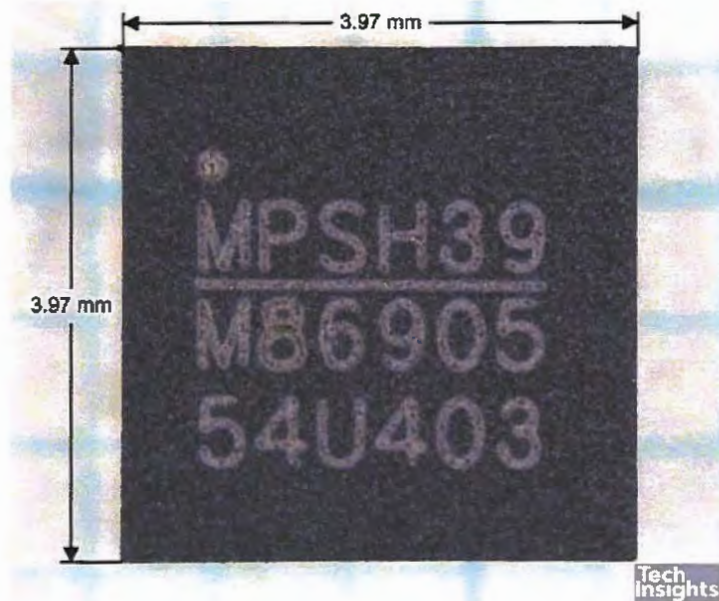
**Tech
Insights**

Observed Critical Dimensions – Metals/Dielectrics

Layer	Material Composition	Thickness (μm)
Passivation	SiN/SiO	0.75/0.80
IMD 2	SiO	1.40 (planarized)
IMD 1	SiO	1.40 (planarized)
PMD (PMD 2, PMD 1)	SiO	0.40/0.20 (planarized)
M3	TiN/Al/TiN	0.06/0.84/0.05
M2	TiN/Al/TiN	0.06/0.45/0.05
M1	TiN/Al/TiN	0.06/0.45/0.05
Die (total)	–	161

MP86905 Package Photographs

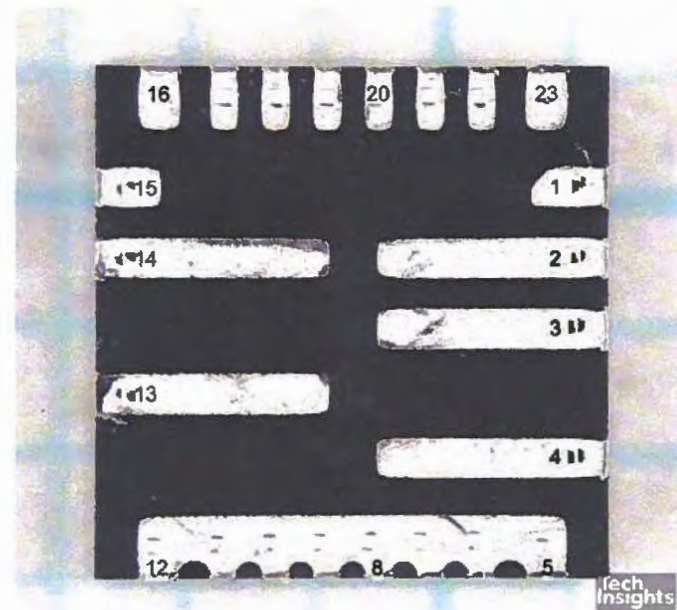
- Package markings include: MPSH39
M86905
54U403



MP86905GR-P_Pkg_Top_394747.png

Package – Top

- 23-pin FC-QFN package dimensions: 3.97 mm × 3.97 mm × 0.88 mm (thick)
- Detailed pin descriptions are presented on the next two pages.



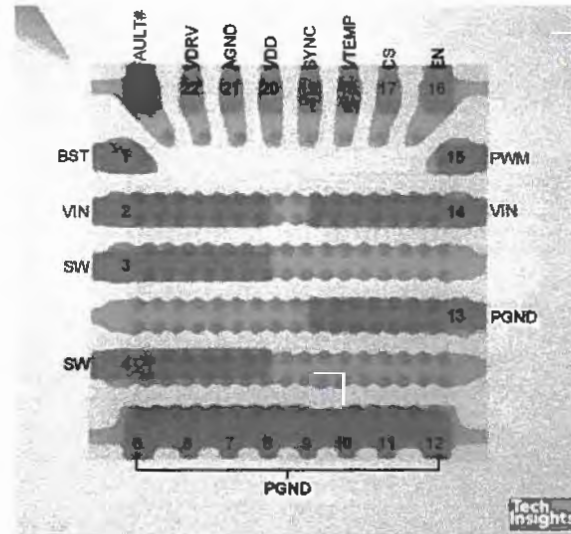
MP86905GR-P_Pkg_Bot_394747.png

Package – Bottom

**Tech
Insights**

MP86905 Package X-Rays

- Detailed pin descriptions are presented on the next page.



MP86905GR-P_XrayTop_394747.png



MP86905GR-P_XraySideB_394747.png

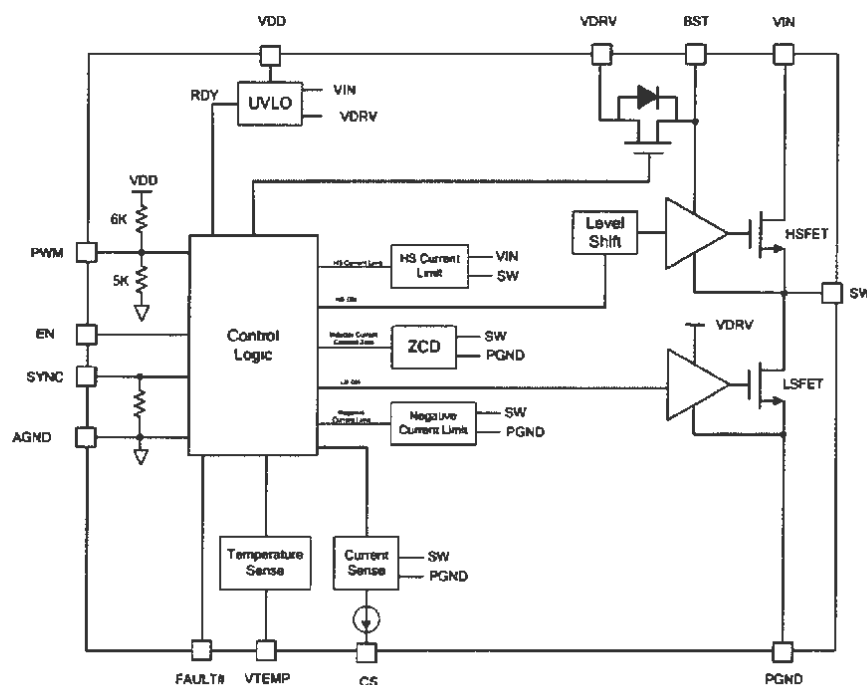


MP86905GR-P_XraySideA_394747.png

Package X-Rays

Tech
Insights

MP86905 Block Diagram with Pin Descriptions



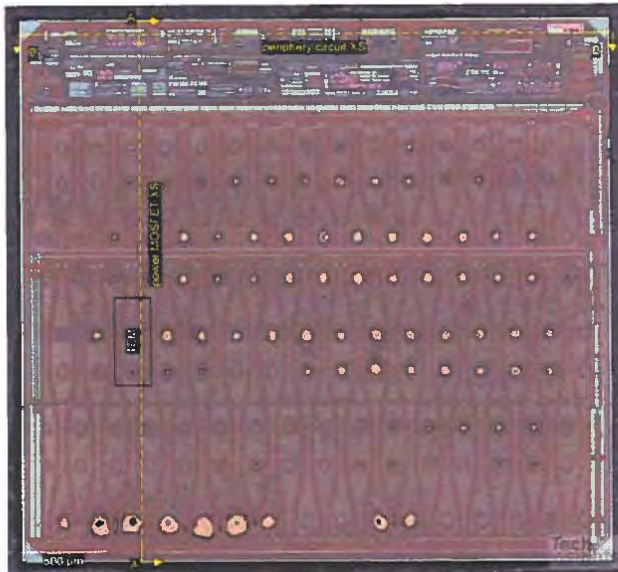
Block Diagram [2]

Pin #	Name	Description
1	BST	Bootstrap. BST requires a 0.1µF to 1µF capacitor to drive the high-side power switch's gate above the supply voltage. Connect the capacitor between BST and SW to form a floating supply across the power switch driver.
2, 14	VIN	Supply voltage. Place C_{IN} close to the device to support the switching current and reduce voltage spikes at input.
3, 4	SW	Phase node.
5 - 13	PGND	Power ground.
15	PWM	Pulse width modulation input. Leave PWM floating or drive PWM to mid-state to enter diode emulation mode.
16	EN	Enable. Pull EN low to disable the device and place SW in a high impedance state.
17	CS	Current sense output.
18	VTEMP	Junction temperature sense output.
19	SYNC	Diode emulation mode. Pull SYNC low to enable diode emulation mode.
20	VDD	Internal circuitry voltage. Connect VDD to VDRV through a 2.2Ω resistor and decouple with a 1µF capacitor to AGND.
21	AGND	Analog ground. Connect AGND to PGND on the VDD capacitor.
22	VDRV	Driver voltage. Connect VDRV to a 3.3V supply and decouple with a 1µF to 4.7µF ceramic capacitor close to VDRV to PGND.
23	FAULT#	Fault report. FAULT# is an open drain, active low. FAULT# pulls low when SW short detection, HS current limit, or over-temperature is triggered. During a cycle-by-cycle high-side current limit event, FAULT# is kept high until the fourth cycle.

Pin Function Descriptions [2]

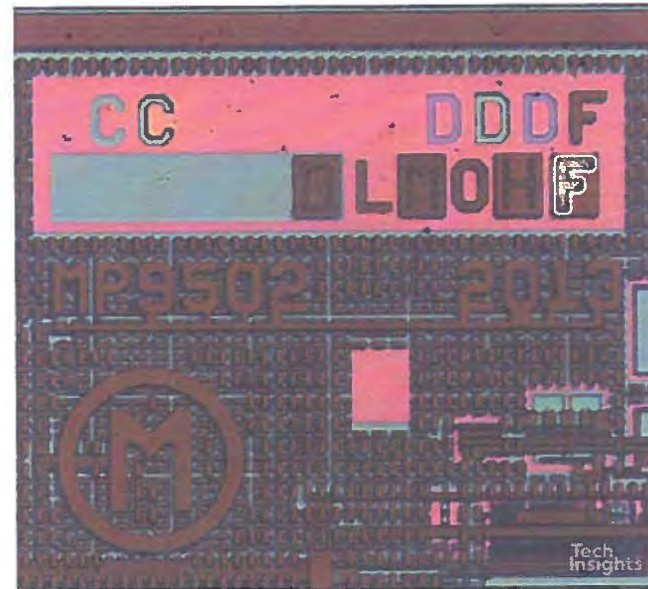
MP9502 Die Photograph and Die Markings

- Die size: 3.38 mm × 3.14 mm (10.61 mm²) (whole die)
3.36 mm × 3.12 mm (10.48 mm²) (edge seal)
- The die SEM and SCM/sMIM-C cross-section line (A-A), TEM cross-section region, and an additional SEM cross-section line (B-B) are annotated.



M86908_MP9502_345783_Oriented.png

Die Photograph



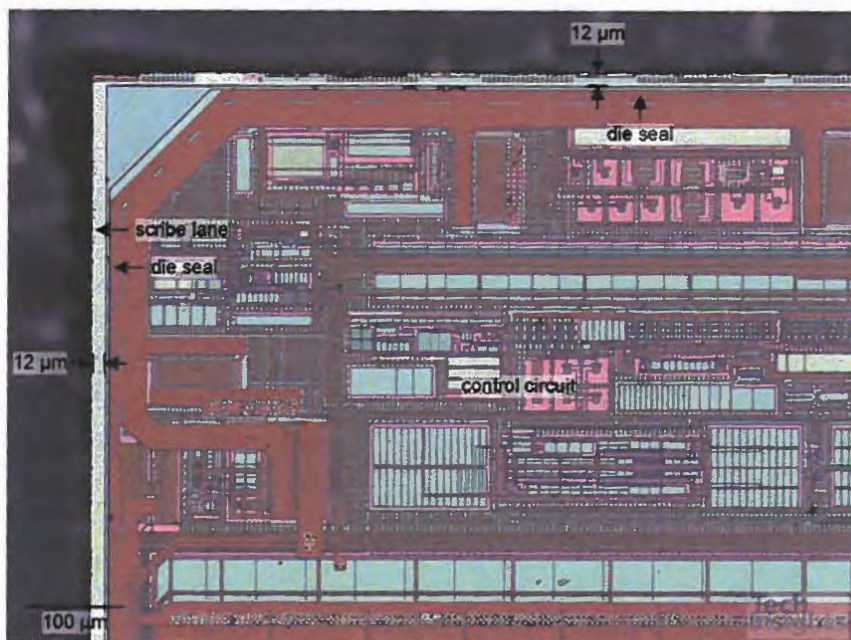
M86908_MP9502_345783_DieMk.png

Die Markings

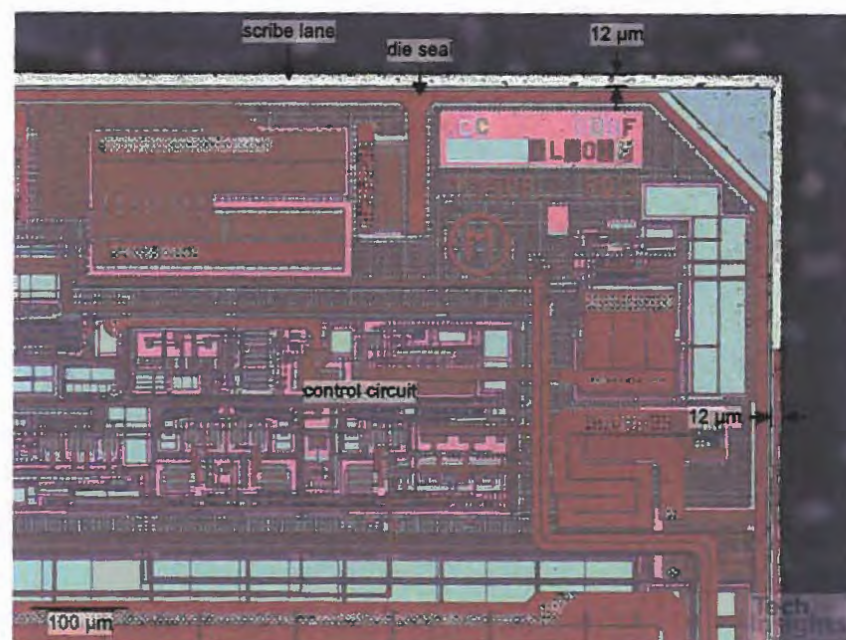
**Tech
Insights**

MP9502 Die Upper Corners

- The scribe lane measures ~12 μm wide all around the die.
- The control circuit is at the top portion of the die.



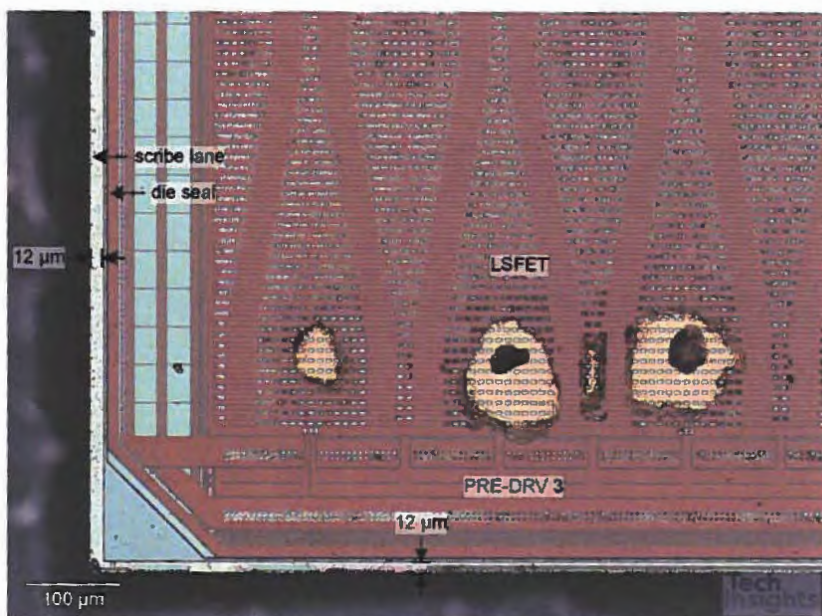
M86908_MP9502_345783_DieCornerA.png



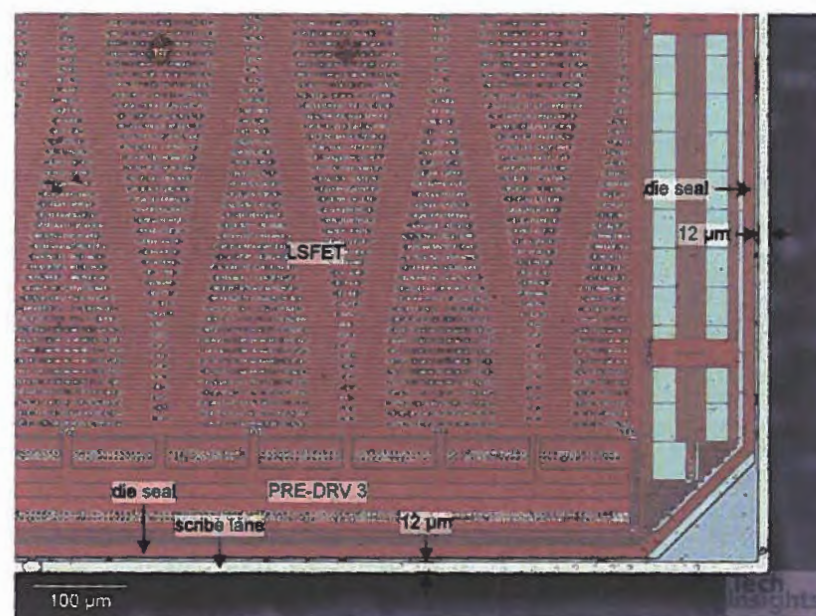
M86906_MP9502_345783_DieCornerB.png

MP9502 Die Lower Corners

- The scribe lane measures ~12 μm wide all around the die.
- The low side MOSFET (LSFET) array and PRE-DRV 3 are at the bottom portion of the die.



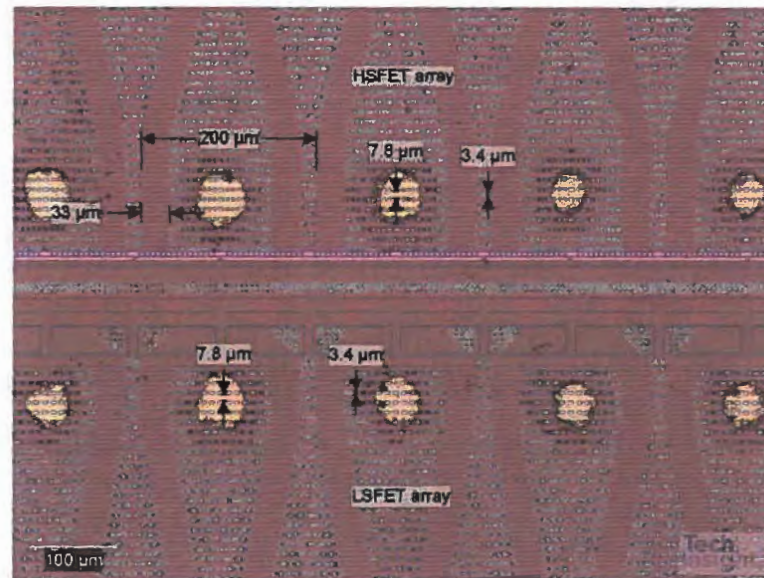
M86908_MP9502_345783_DieCornerD.png



M86908_MP9502_345783_DieCornerC.png

MP9502 MOSFET Die RDL Contacts

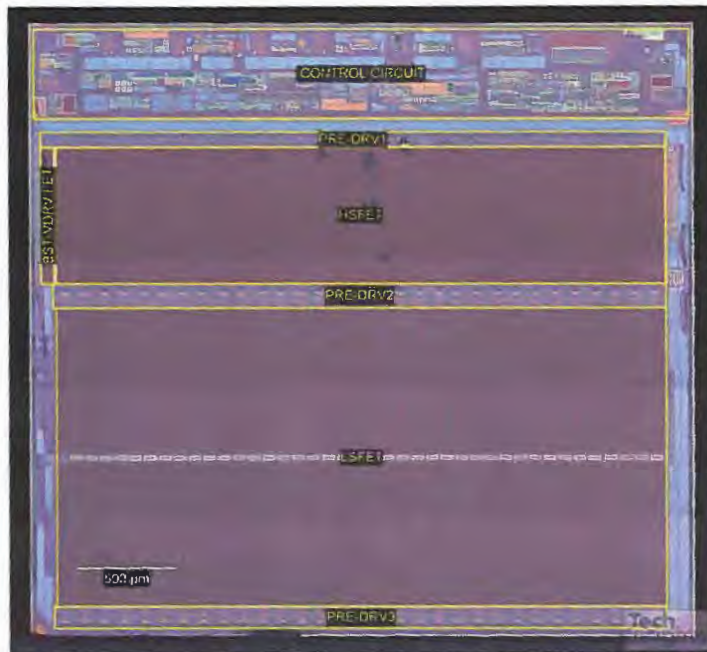
- Source/drain (S/D) groups of passivation openings are shown with the removed redistribution layer (RDL) contacts which are made through passivation openings.
- S/D groups of passivation openings have a spacing of 33 μm on a 200 μm pitch in the horizontal direction.
- S/D passivation openings have been placed horizontally with vertically minimal 7.8 μm spacing and 3.4 μm wide window.



M86908_MP9502_345783_BondPads.png

MP9502 Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table on the right.



MP86905GR-P_MP9502_394865_BPoly_Blocks.png

Functional Description	Length (mm)	Width (mm)	Area (mm ²)	Percentage of Die (%)
HSFET (High-side FET connected between VIN and SW pins)	0.70	3.10	2.18	20.8
LSFET (Low-side FET connected between SW and PGND pins)	1.53	3.10	4.73	45.1
PRE-DRV1 (Likely pre-drivers to the HSFET or LSFET)	0.08	3.18	0.25	2.4
PRE-DRV2 (Likely pre-drivers to the HSFET or LSFET)	0.12	3.12	0.39	3.7
PRE-DRV3 (Likely pre-drivers to the LSFET)	0.11	3.12	0.35	3.3
BST-VDRV FET (Likely a smaller version of FET connected between the BST pin and VDRV pin, this FET can also be used for temperature detection)	0.08	0.70	0.05	0.5
COTROL CIRCUIT (This analog control block consists of several analog circuits including, under-voltage lockout detection, over-temperature detection, over-voltage sensing and over-current sensing, bandgap, bias generator, current limiter and driving circuitry that drives the pre-drivers)	0.46	3.33	1.52	14.5
Total die utilization			9.47	90.3
Others (including capacitors that are not related to the circuit mentioned above and including small FETs on the right that looks like temperature detectors)		—	1.01	9.7
Total die	3.12	3.36	10.48	100.0

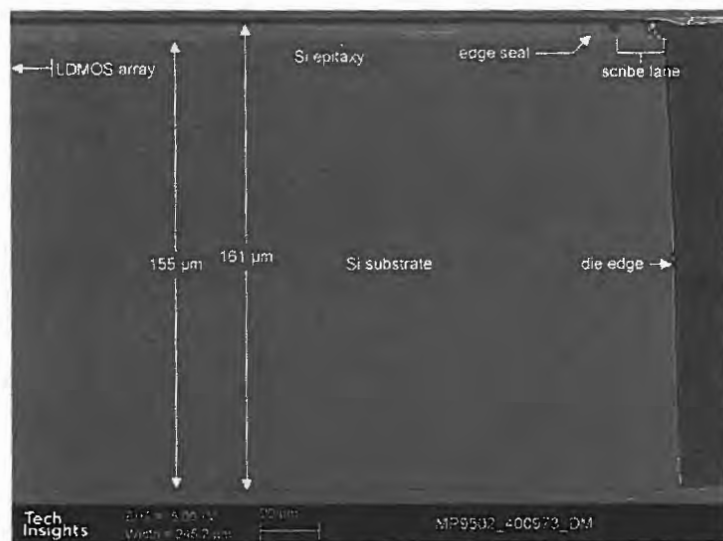
Tech
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General Structure Cross-Sectional Analysis

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Insights**

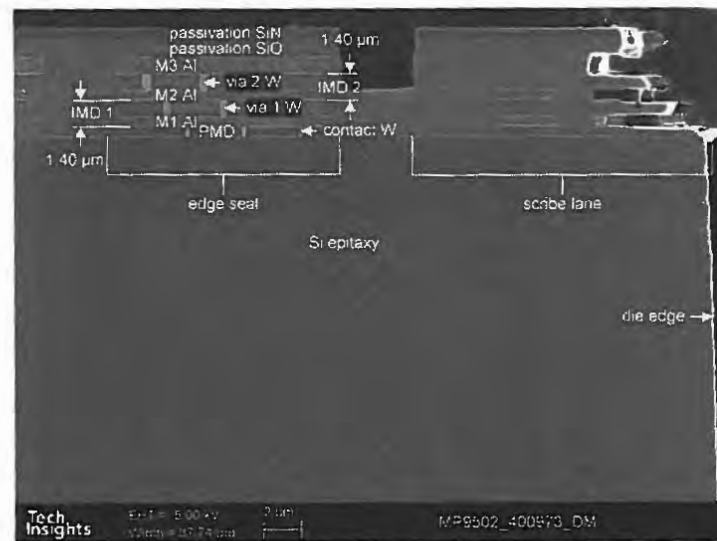
MP9502 Die Structural Overview

- The Si die substrate is ~155 μm thick including the upper epitaxy layer and ~161 μm thick in total.
- The die comprises three Al metallization layers with W vias and contacts.
- The crack stop at the die edge extends through the passivation into IMD 2.
- Both IMD 2 and IMD 1 are ~1.40 μm thick in the SEM sample.



Die Thickness_01_400973.png

Die Edge – SEM Cross-Section A-A



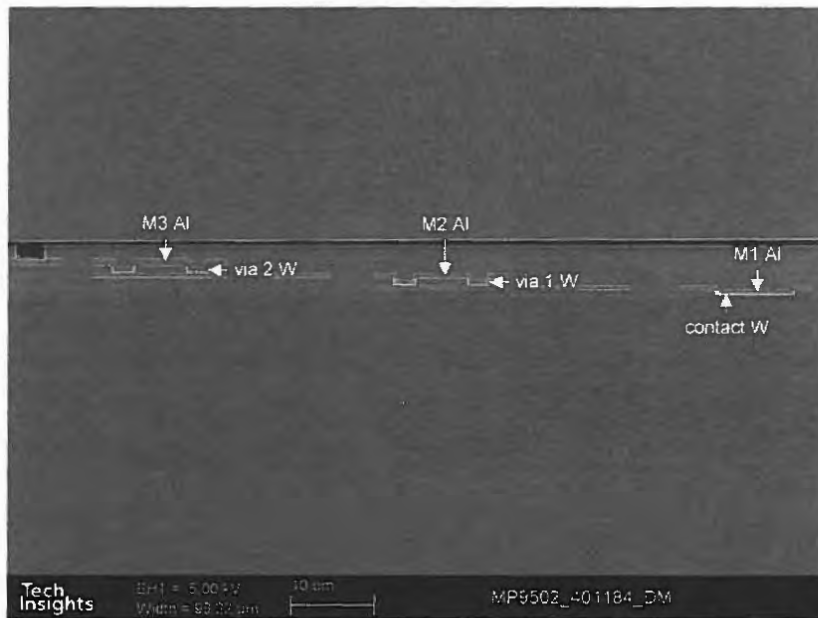
Die Edge_02_400973.png

Structural Overview at the Edge Seal – SEM Cross-Section A-A

Tech
Insights

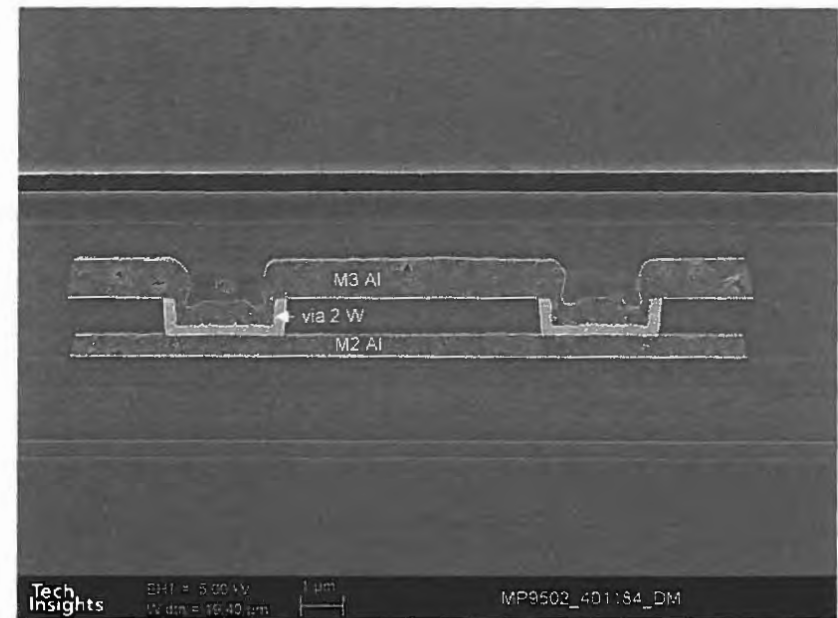
MP9502 Die Contact and Vias

- Wide via is formed with a conformal upper metal layer formed over the via trench lined with the via metallization, such as via 1 and via 2.



General Structure_43_401184.png

Wide Contact and Vias – SEM Cross-Section B-B



General Structure_42_401184.png

Wide Via 2 – SEM Cross-Section B-B

**Tech
Insights**

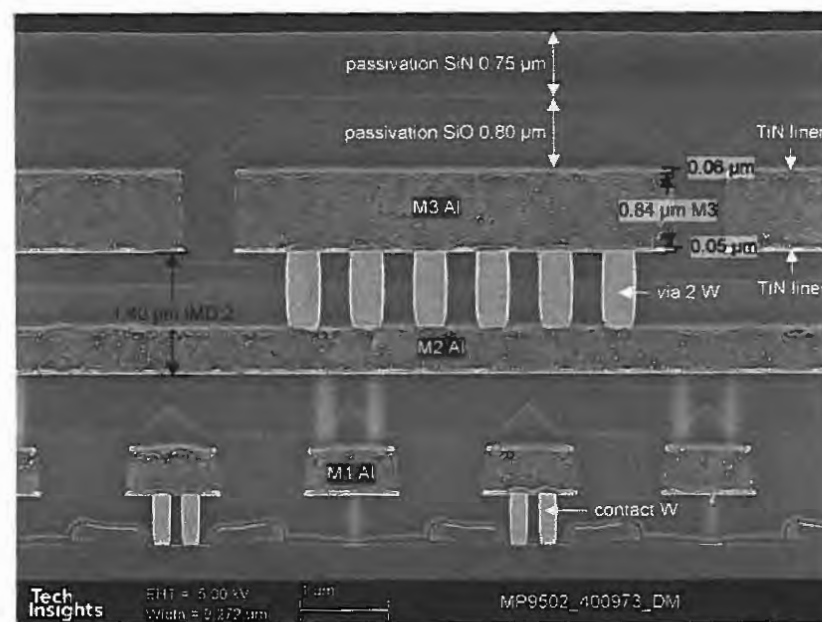
MP9502 Die Passivation, Metal 3, and IMD 2

- The passivation comprises an $\sim 0.80\ \mu\text{m}$ thick SiO and an $\sim 0.75\ \mu\text{m}$ thick SiN.
- Metal 3 comprises of an $\sim 0.84\ \mu\text{m}$ thick Al layer, with an $\sim 0.05\ \mu\text{m}$ thick bottom TiN liner, and $\sim 0.06\ \mu\text{m}$ thick top TiN liner.
- The IMD 2 layer comprises of an $\sim 1.4\ \mu\text{m}$ thick oxide.



20220329 1541 7000 x_400282.png

Passivation and Metal 3 – TEM Cross-Section



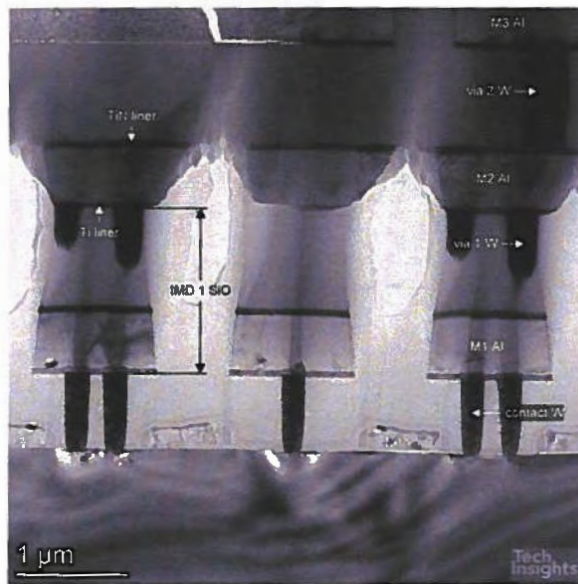
General Structure_40_400973.png

IMD 2 Details – SEM Cross-Section A-A

Tech
Insights

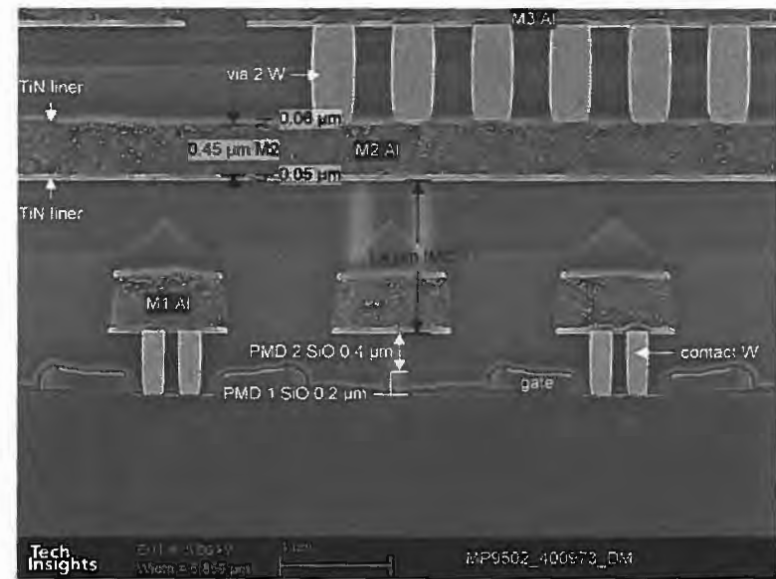
MP9502 Die Metal 2 and IMD 1

- Metal 2 comprises of an $\sim 0.45\ \mu\text{m}$ thick Al layer, with an $\sim 0.05\ \mu\text{m}$ thick bottom TiN liner and $\sim 0.06\ \mu\text{m}$ thick top TiN liner.
- The IMD 1 layer comprises of an $\sim 1.40\ \mu\text{m}$ thick oxide.
- The vias and contacts comprise W and have a TiN liner. The vias partially penetrate into the top TiN liner of the metal layer below.



20220329 1544 11000 x_400282.png

Metal 2 and IMD 1 – TEM Cross-Section

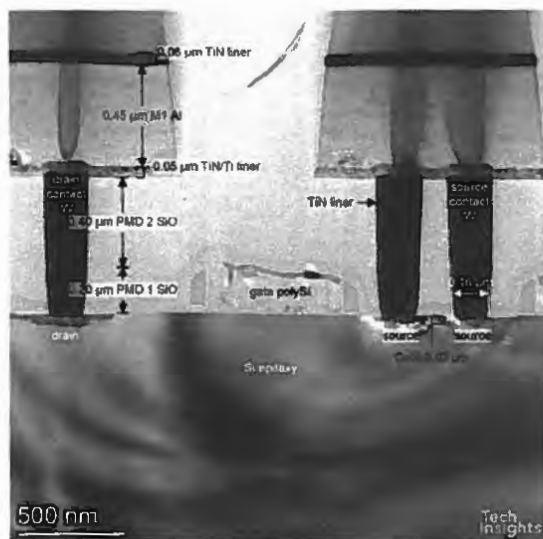


General Structure_42_400973.png

Metal 2 and IMD 1 – SEM Cross-Section A-A

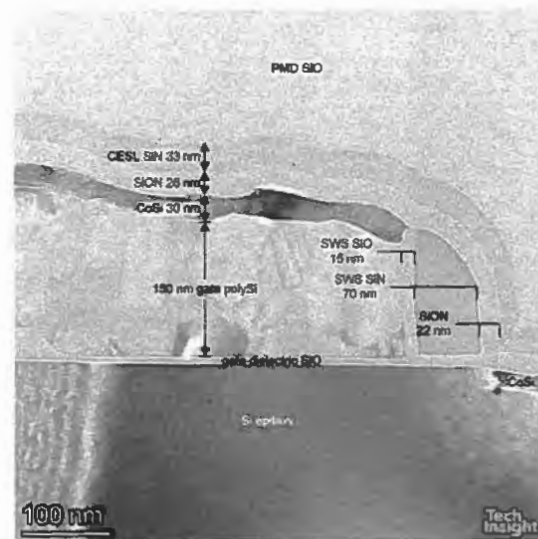
MP9502 Die Metal 1 and FEOL Structures

- Metal 1 comprises an $\sim 0.06 \mu\text{m}$ thick top TiN liner, an $\sim 0.45 \mu\text{m}$ thick Al layer, and bottom liners comprising $\sim 0.05 \mu\text{m}$ thick TiN layers.
- The PMD comprises an $\sim 0.4 \mu\text{m}$ thick oxide PMD 2 layer and an $\sim 0.2 \mu\text{m}$ thick oxide PMD 1 layer.
- The S/D contact is $\sim 0.16 \mu\text{m}$ wide at the bottom. The source, drain, and polysilicon contact regions use an $\sim 30 \text{ nm}$ thick CoSi layer.
- The gate polysilicon layer is $\sim 180 \text{ nm}$ thick, including $\sim 30 \text{ nm}$ thick CoSi layer.
- The sidewall spacer (SWS) comprises a 15 nm L-shaped SiO layer, a 70 nm D-shaped SiN layer.



20220329 1558 22500 x_400282.png

Metal 1 and PMD – TEM Cross-Section

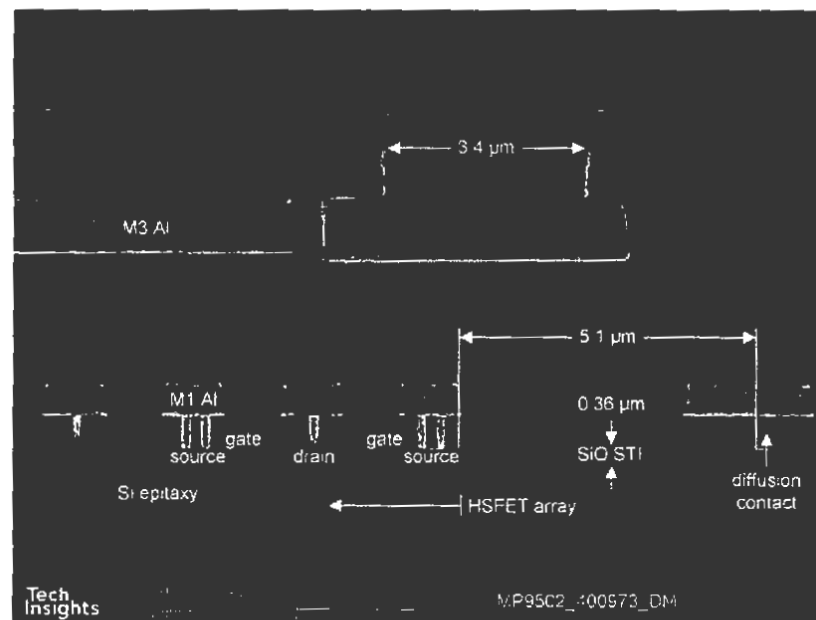


20220329 1602 94000 x 0001_400282.png

HS/LS FET Gate SWS – TEM Cross-Section

MP9502 Die Isolation Structures

- The MP9502 die employs SiO shallow trench isolation (STI) structures with $\sim 0.36\text{ }\mu\text{m}$ depth as isolation between periphery circuit and HS/LS FET array.



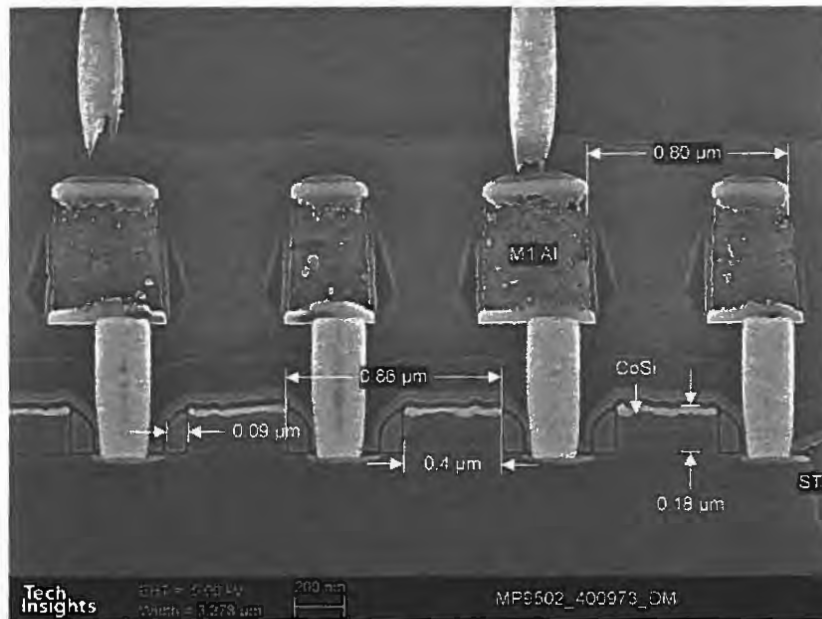
STI – SEM Cross-Section A-A

Periphery and Control Circuitry Device Analysis

Tech
Insights

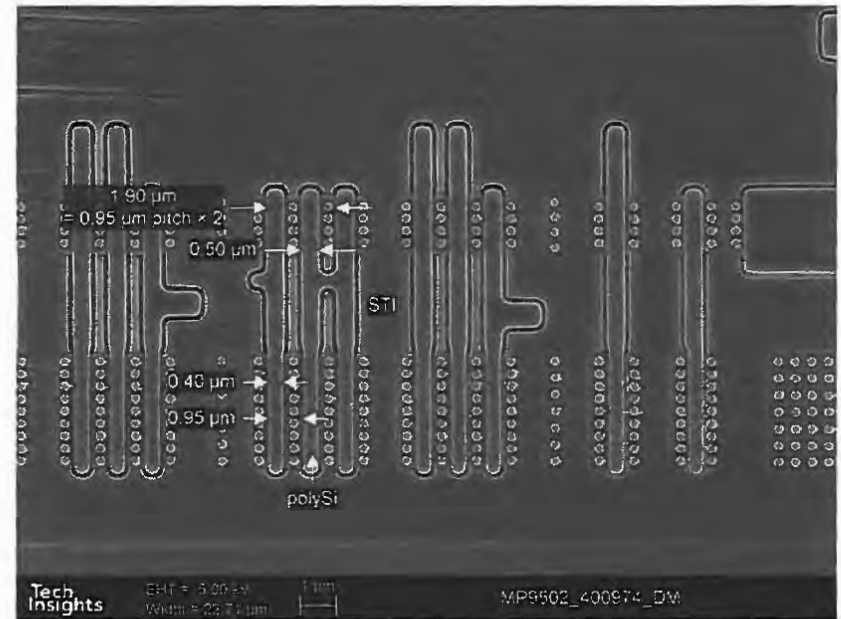
MP9502 Die Logic Transistors

- A minimum transistor gate length of $0.40\ \mu\text{m}$ is observed in the logic transistors, the minimum observed contacted gate pitch is $\sim 0.86\ \mu\text{m}$, and CoSi is used as gate silicide. These measurements are indicative of a likely relaxed $0.18\ \mu\text{m}$ process.



Transistors_11_400973.png

Minimum Observed Gate Length and Contacted Gate Pitch – SEM Cross-Section A-A

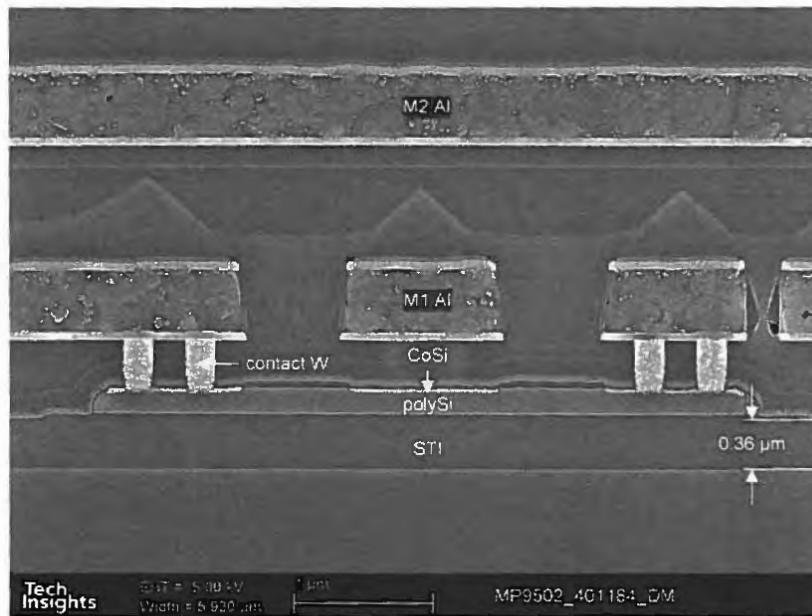


Periphery_Poly_5K_44_400974.png

Minimum Observed Gate Length – SEM Plan View at the Gate Level

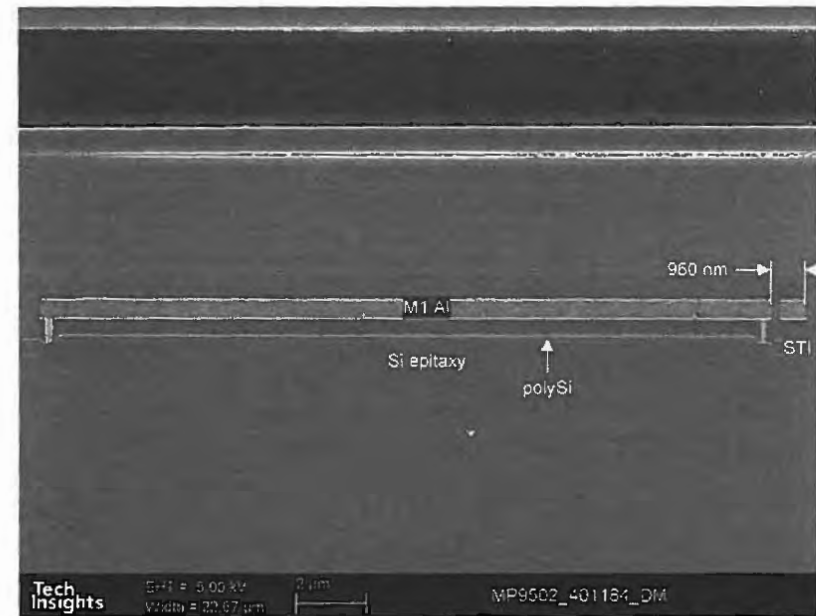
MP9502 Die Periphery Devices

- Observed periphery devices observed include BJTs (not analyzed), polysilicon resistors, and polysilicon MOS capacitors.
- Examples of polysilicon resistors and capacitors observed are shown below.



General Structure_20_401184.png

Polysilicon Resistors – SEM Cross-Section B-B



General Structure_26_401184.png

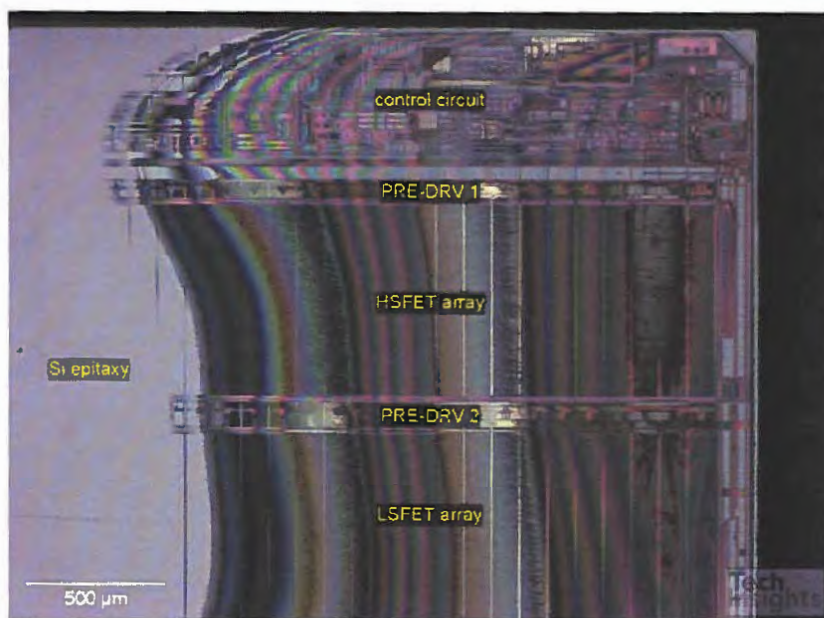
Polysilicon Capacitors – SEM Cross-Section B-B

**Tech
Insights**

HS/LS FET Planar Analysis

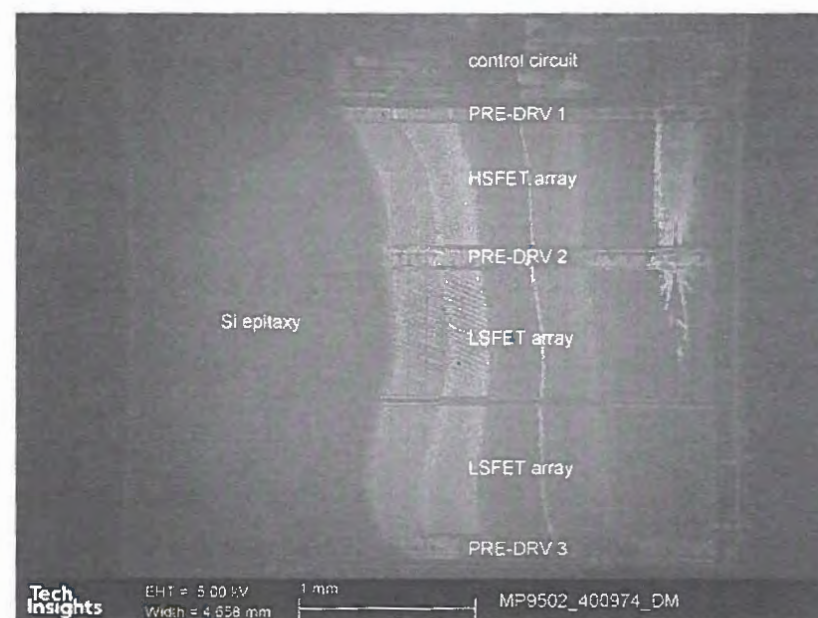
MP9502 Die HS/LS FET Array Overview

- One high side (HS) power MOSFET array and two low side (LS) power MOSFET arrays are arranged at the lower portion of the die.



Bevel Area_02_400974_5x1r.png

HS/LS FET Arrays – Optical Bevel



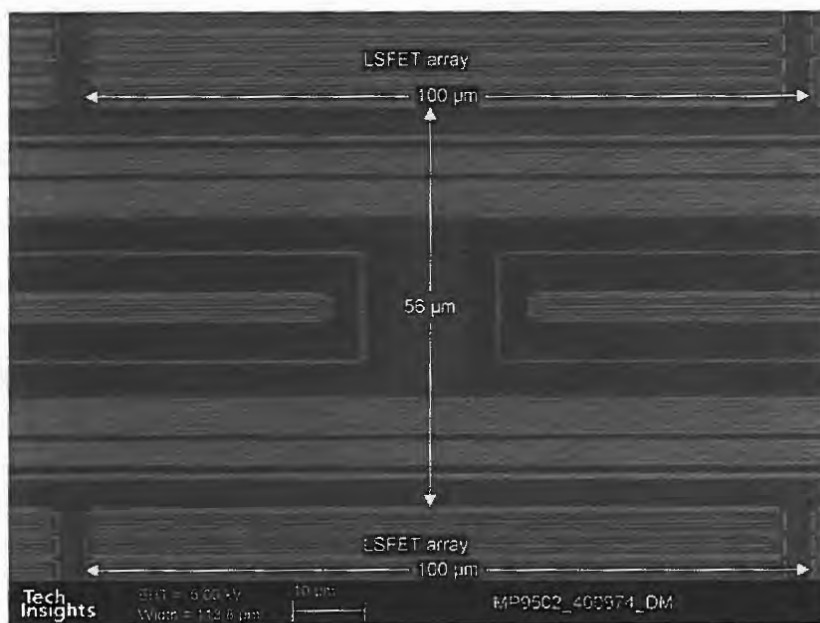
Bevel Section_01_400974.png

HS/LS FET Arrays – SEM Bevel

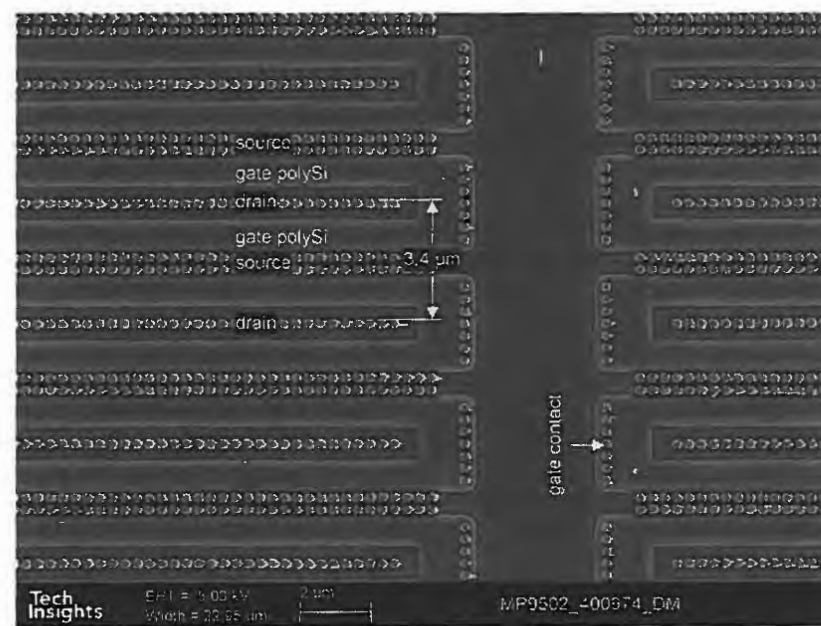
**Tech
Insights**

MP9502 Die LSFET Array

- The LSFET arrays measure $\sim 100\ \mu\text{m}$ pitch in the width direction, with a cell (drain-to-drain) pitch of $\sim 3.4\ \mu\text{m}$ in the LSFET array.
- Two groups of LSFET arrays are spaced $\sim 56\ \mu\text{m}$ apart vertically.



Gate Array_Interconnect_1K_26_400974.png
LSFET Array – SEM Plan View at the Gate Level

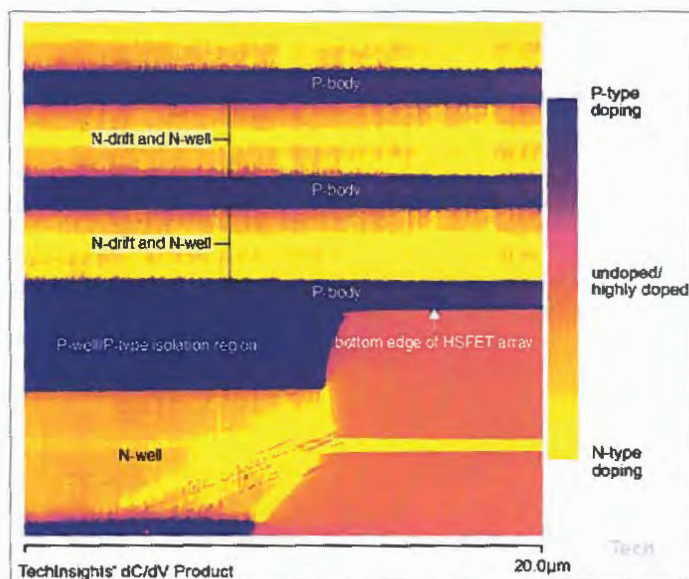


Gate Array_Poly_5K_08_400974.png
LS FET – SEM Plan View at the Gate Level

**Tech
Insights**

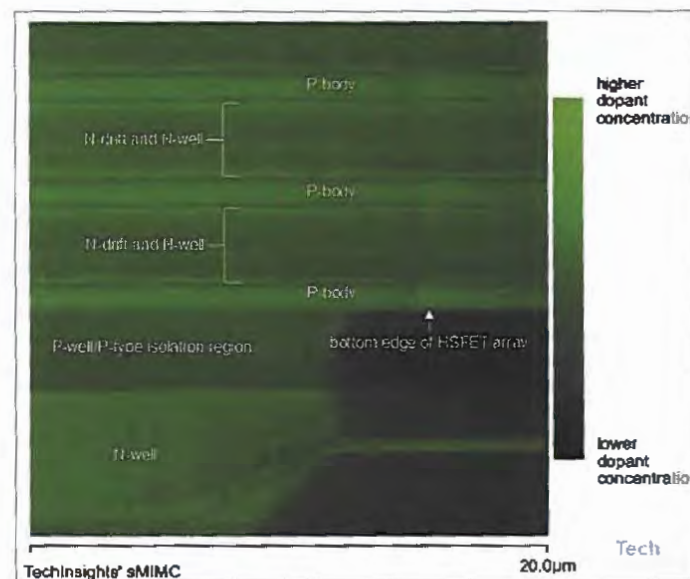
MP9502 Die HSFET Array Edge – P- and N-Type Regions

- Note: SCM imaging (left) is sensitive to dopant type, with N-type material giving a negative (yellow) response and P-type material giving a positive (blue) response. sMIM imaging (right) is sensitive to the dopant concentration level, with greater signal (brighter) corresponding to a higher dopant level, regardless of conductivity type.
- At the bottom edge of the HSFET array, a narrow N-well in the P-type isolation region is observed.



Array_edge_1to2_041122130327_PRODUCT_FRW_20 0u_512p_400974.png

Bottom Edge of the HSFET Array – SCM Bevel



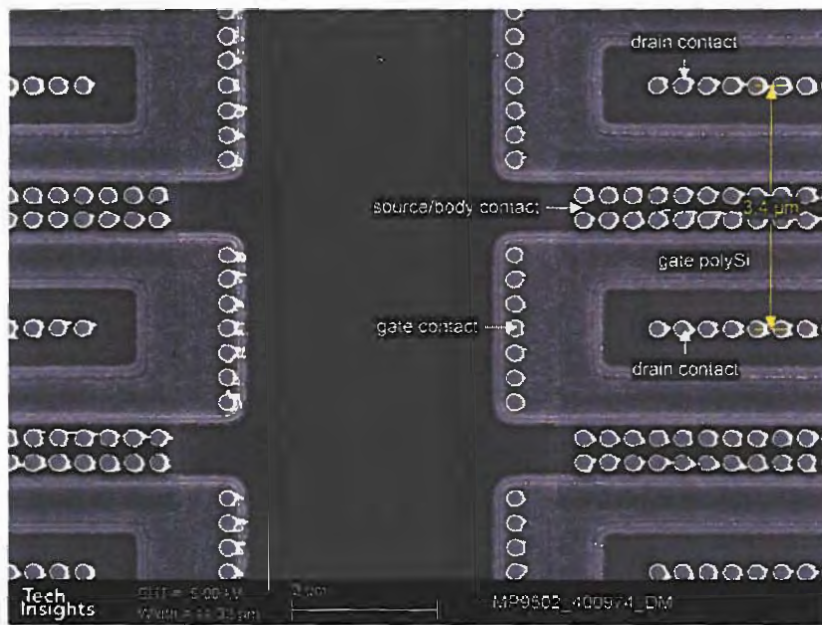
Array_edge_1to2_041122130327_SMIMC_FRW_20 0u_512p_400974.png

Bottom Edge of the HSFET Array – sMIM-C Bevel

**Tech
Insights**

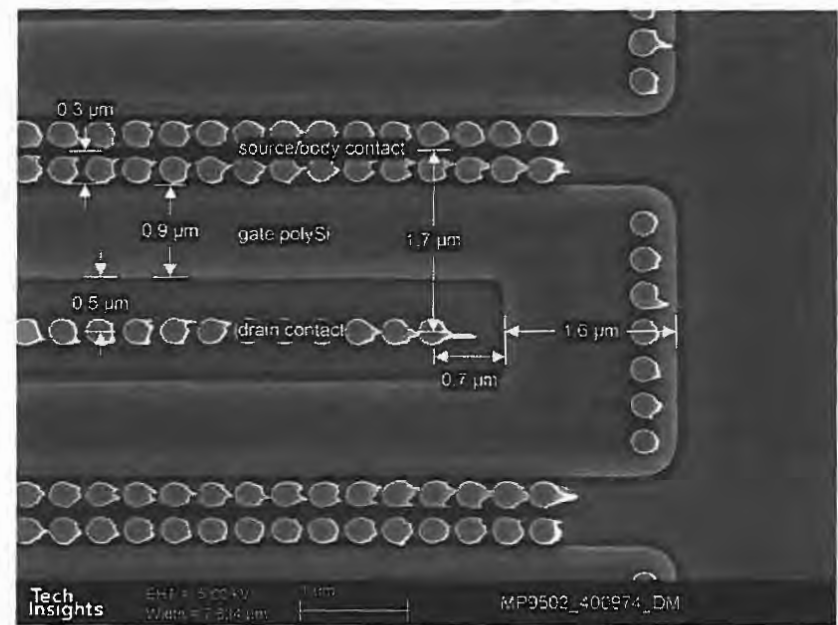
MP9502 Die LSFET Array – Polysilicon Level

- SEM bevel images below show the center region of the LSFET array at the polysilicon level.
- The cell (drain-to-drain) pitch measures $\sim 3.4 \mu\text{m}$, and the drain-to-source pitch measures $\sim 1.7 \mu\text{m}$ in the LSFET array.



Gate Array_Poly_10K_47_400974.png

LSFET Array – SEM Bevel at the Gate Level



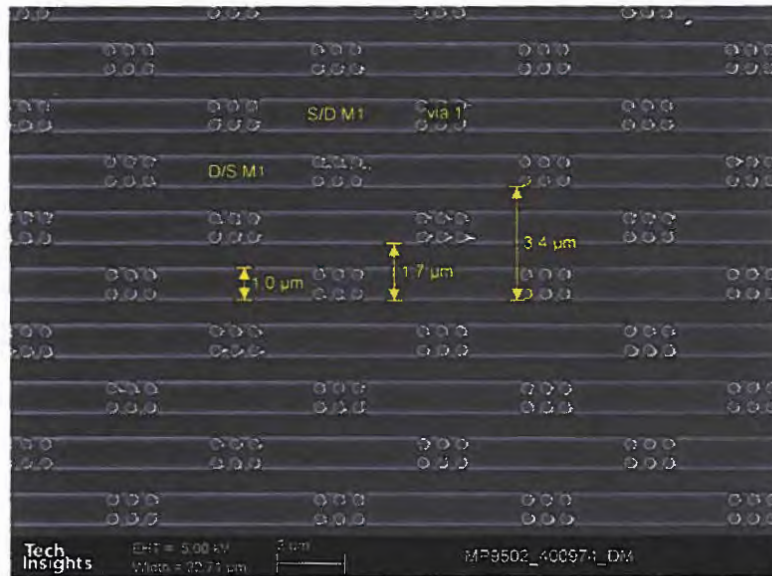
Gate Array_Poly_15K_09_400974.png

LSFET Array – SEM Bevel at the Gate Level

**Tech
Insights**

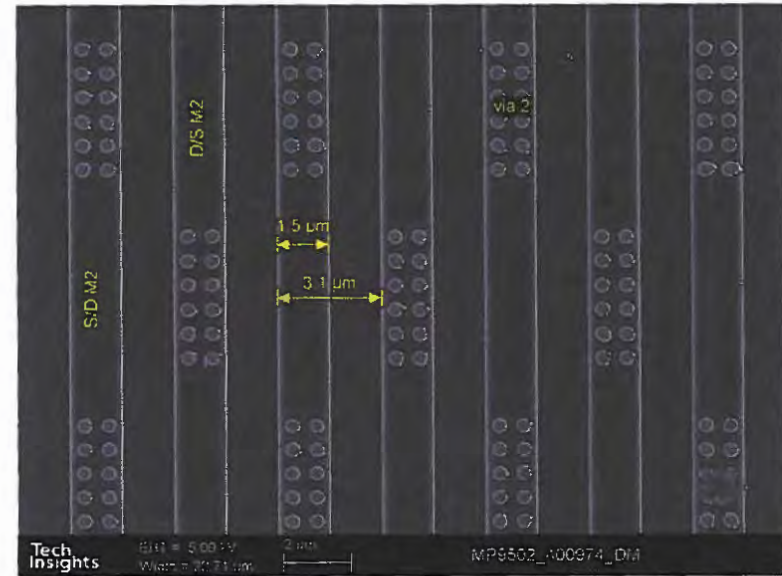
MP9502 Die LS FET Array – Metal 1 and Metal 2 Levels

- SEM bevel images below show the center region of the LSFET array at the metal 1 (M1) and metal 2 (M2) level.
- The M1 strips in the LSFET array area measure $1.0\ \mu\text{m}$ with a $1.7\ \mu\text{m}$ pitch, M2 strips measure $1.5\ \mu\text{m}$ with a $3.1\ \mu\text{m}$ pitch.
- The M1 and M2 strips are placed orthogonally with multiple rows and columns as the case of S/D vias 1 and 2.



Gate Array_M1_5K_13_400974.png

LSFET Array – SEM Bevel at the M1 Level



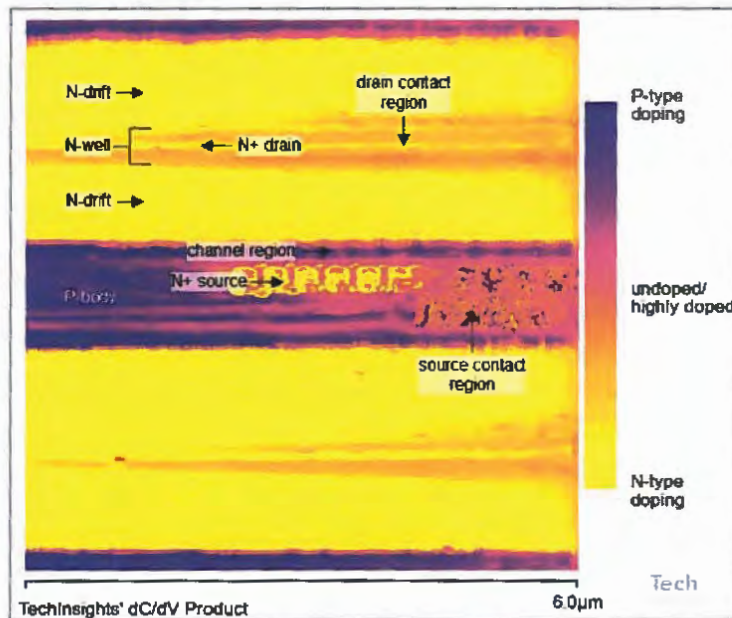
Gate Array_M2_5K_18_400974.png

LSFET Array – SEM Bevel at the M2 Level

**Tech
Insights**

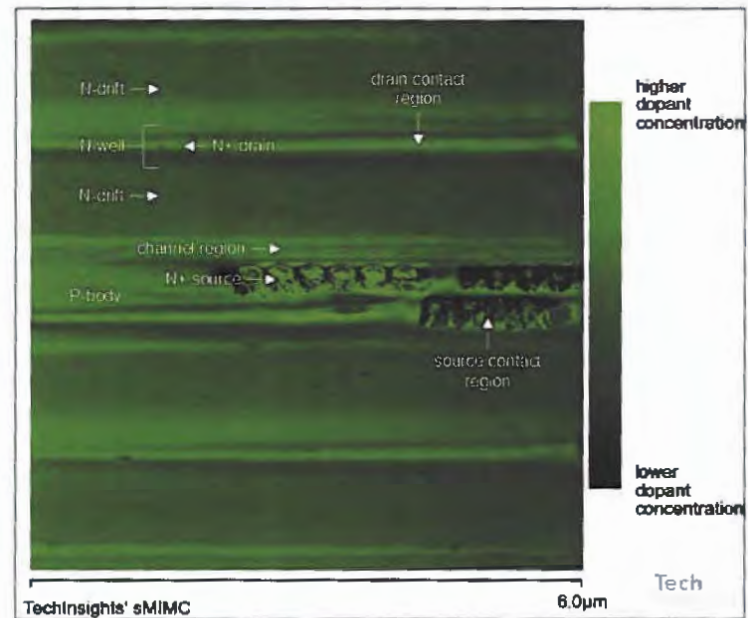
MP9502 Die LS FET Array – P- and N-Type Regions

- Strip doping regions can be seen along the length of the array. The N-type source region is only visible at the center-right side due to the bevel angle. It is more apparent in the cross-sectional analysis on page 38.



Array_below_poly_040822193718_PRODUCT_FRW_6 0u_512p_400974.png

LSFET Array – SCM Bevel



Array_below_poly_040822193718_SMIMC_FRW_6 0u_512p_400974.png

LSFET Array – sMIM-C Bevel

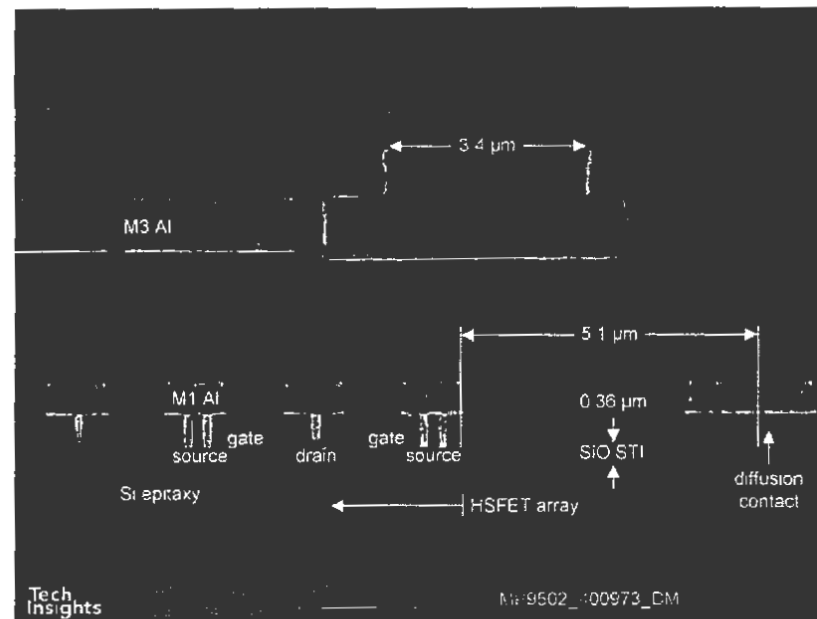
**Tech
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HS/LS FET Cross-Sectional Analysis

**Tech
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MP9502 Die HSFET Array Edge

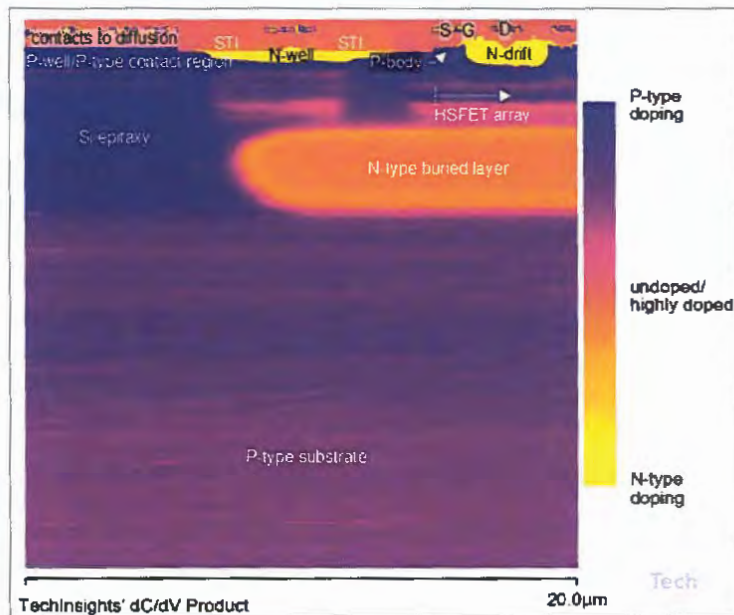
- SEM cross-sections of the bottom edge of the HSFET array are shown. On the top side, a starting source contact is followed by a 5.1 μm wide STI.
- S/D passivation openings have a 3.4 μm wide window.



Top Edge of a HSFET Array – SEM Cross-Section A-A

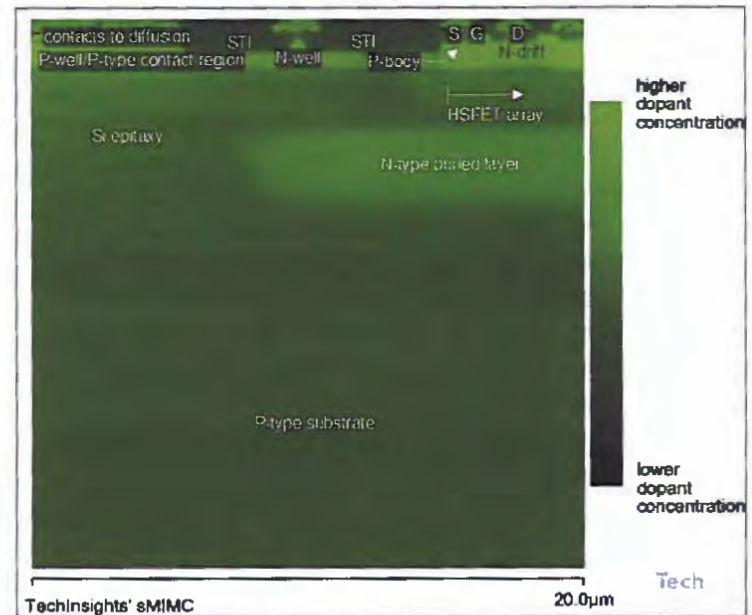
MP9502 Die HSFET Array Edge – P- and N-Type Regions

- SCM and sMIM-C analysis at the top edge region of HSFET array show the use of a P-type substrate, N-type buried layer (NBL), a P-well layer, likely epitaxial, and a P-well/P-type contact region between the output arrays.



Array_Edge_endarray1_040522190605_PRODUCT_FRW_20 0u_512p_400973.png

Edge of an HSFET Array – SCM Cross-Section A-A



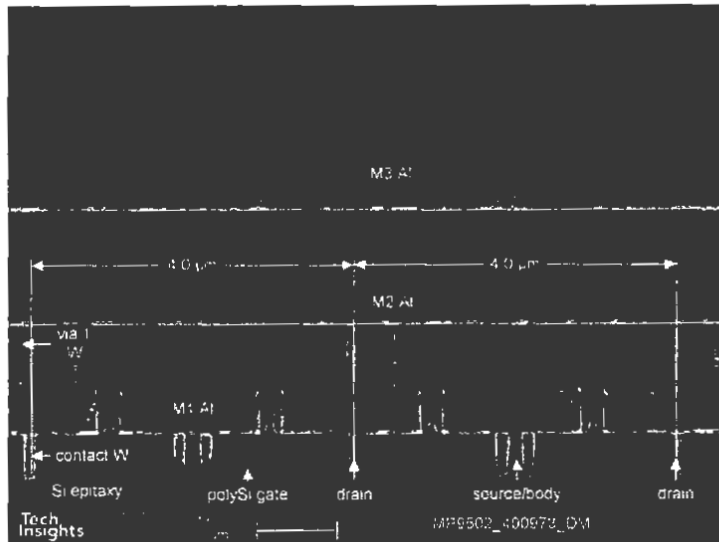
Array_Edge_endarray1_040522190605_sMIMC_FRW_20 0u_512p_400973.png

Edge of an HSFET Array – sMIM-C Cross-Section A-A

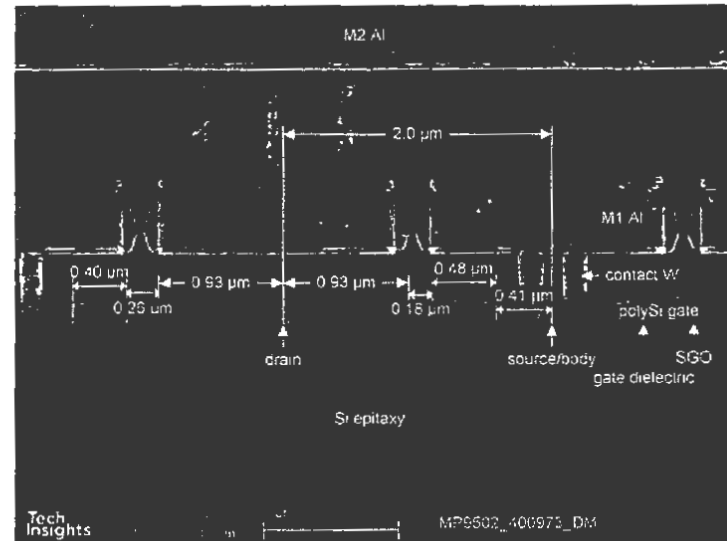
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MP9502 Die HSFET Array

- The stepped-gate-oxide (SGO) are fabricated on this die. The use of SGO allows a reduction of on-resistance (R_{on}) compared with the conventional STI LDMOS [3].
- In the HSFET array, the cell (drain-to-drain) pitch measures $\sim 4.0\ \mu\text{m}$, the gate to drain contact center spacing is $\sim 0.93\ \mu\text{m}$, the gate to source/body contact center spacing is $\sim 0.41\ \mu\text{m}$, the total polysilicon gate length is $\sim 0.66\ \mu\text{m}$.
- In the HSFET array, there are two sets of polysilicon gate length combinations, one is $\sim 0.40\ \mu\text{m}$ physical channel length and $\sim 0.26\ \mu\text{m}$ extended portion over the SGO, another is $\sim 0.48\ \mu\text{m}$ physical channel length and $\sim 0.18\ \mu\text{m}$ extended portion over the SGO.



HSFET Array – SEM Cross-Section A-A

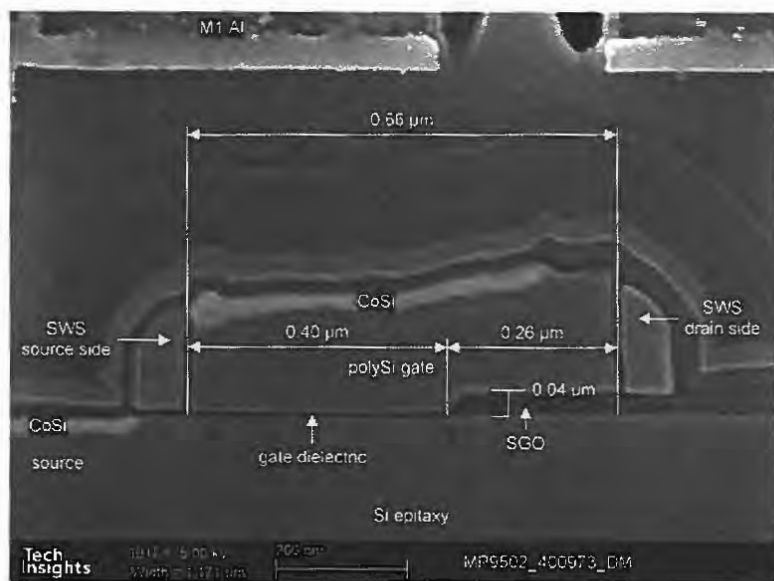


HSFET Array – SEM Cross-Section A-A

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MP9502 Die HSFET Array

- In the HSFET array, the gate polysilicon strip measures $\sim 0.66 \mu\text{m}$, including the physical channel length of $\sim 0.40 \mu\text{m}$ and the extended portion over the SGO in the analyzed region.
- The gate polysilicon is nominally $\sim 180 \text{ nm}$ thick, including the cobalt silicide (CoSi) layer.



Transistors_22_400973.png

HSFET Array – SEM Cross-Section A-A



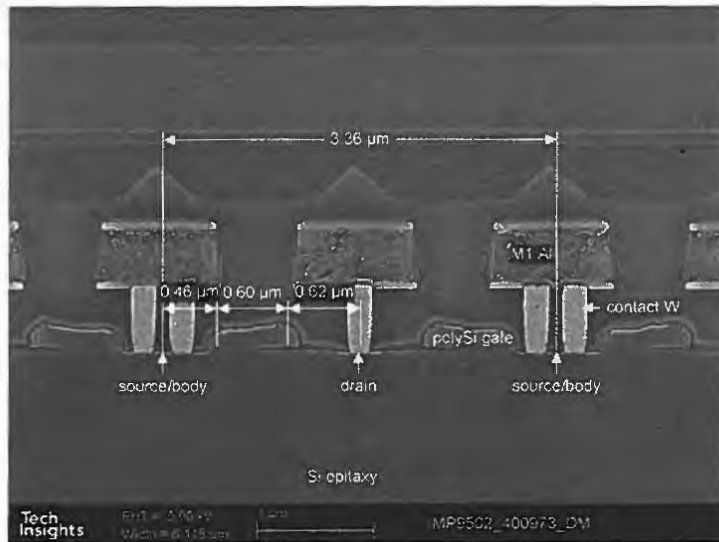
20220329 1601 46000 x_400282.png

HSFET Array – TEM Cross-Section

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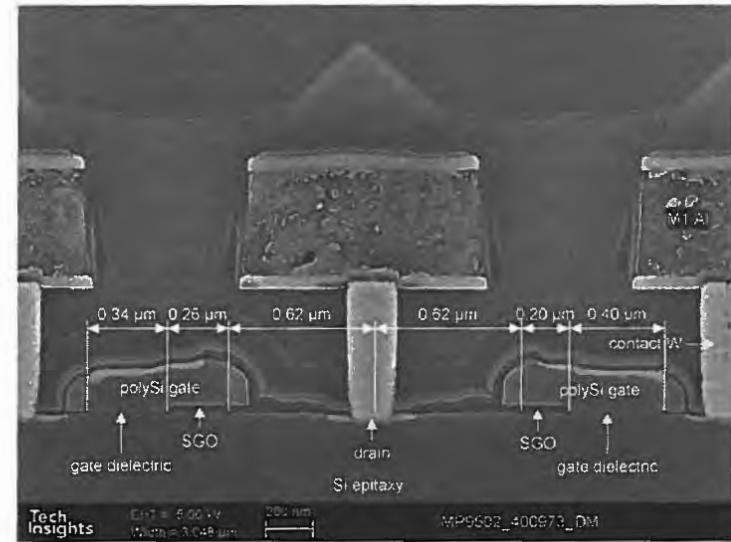
MP9502 Die LSFET Array

- The stepped-gate-oxide (SGO) are fabricated on this die. The use of SGO allows a reduction of on-resistance (R_{on}) compared with the conventional STI LDMOS [3].
- In the LSFET array, the cell (drain-to-drain) pitch measures $\sim 3.36 \mu\text{m}$, the gate to drain contact center spacing is $\sim 0.62 \mu\text{m}$, the gate to source/body contact center spacing is $\sim 0.46 \mu\text{m}$, the total polysilicon gate length is $\sim 0.60 \mu\text{m}$.
- In the LSFET array, there are two sets of polysilicon gate length combinations, one is $\sim 0.34 \mu\text{m}$ physical channel length and $\sim 0.26 \mu\text{m}$ extended portion over the SGO, another is $\sim 0.40 \mu\text{m}$ physical channel length and $\sim 0.20 \mu\text{m}$ extended portion over the SGO.



General Structure_47_400973.png

LSFET Array – SEM Cross-Section A-A



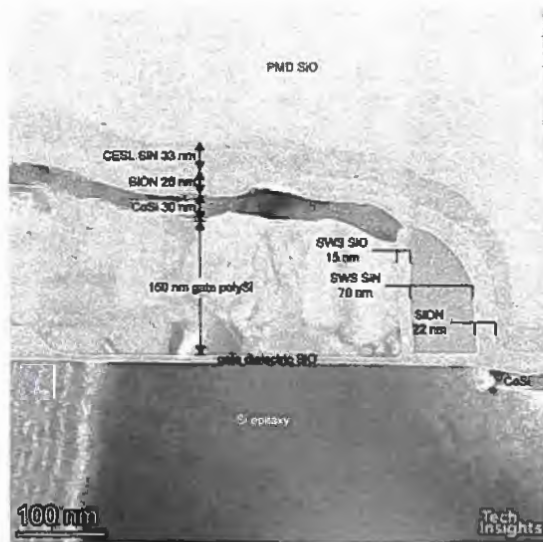
General Structure_48_400973.png

LSFET Array – SEM Cross-Section A-A

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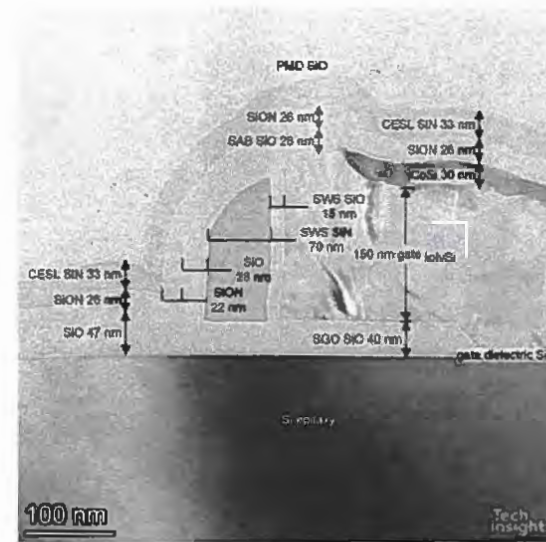
MP9502 Die HS/LS FET SWS

- The polysilicon contact regions use an, up to ~30 nm thick, CoSi layer.
- The sidewall spacer (SWS) comprises a 15 nm L-shaped SiO layer, a 70 nm D-shaped SiN layer, and a 22 nm D-shaped SiON on the S/D side.
- An additional 28 nm D-shaped SiO on the drain side only which is used as salicide block (SAB) layer. A 33 nm thick SiN CESL covers the transistors.
- The maximum thickness of oxide is ~47 nm in the region between polysilicon gate and drain contact.



20220329 1602 94000 x 0001_400282.png

HS/LS FET Gate SWS on Source Side – TEM Cross-Section



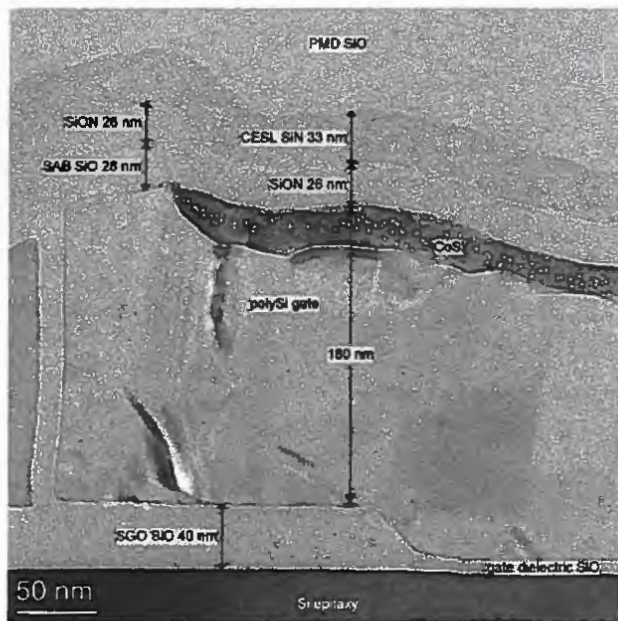
20220329 1601 94000 x_400282.png

HS/LS FET Gate SWS on Drain Side – TEM Cross-Section

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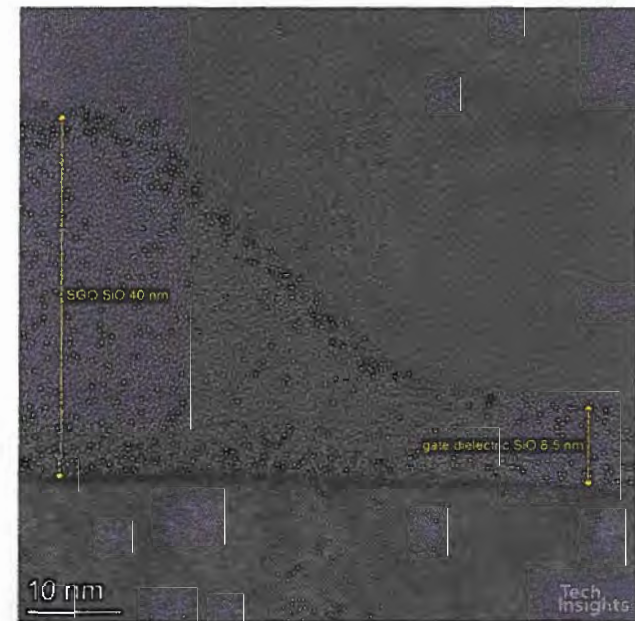
MP9502 Die HS/LS FET Gate Dielectric

- The gate features a ~40 nm thick SGO and an ~8.5 nm thick oxide as gate dielectric.



20220329 1605 150 kx 0001_400282.png

HS/LS FET Gate – TEM Cross-Section



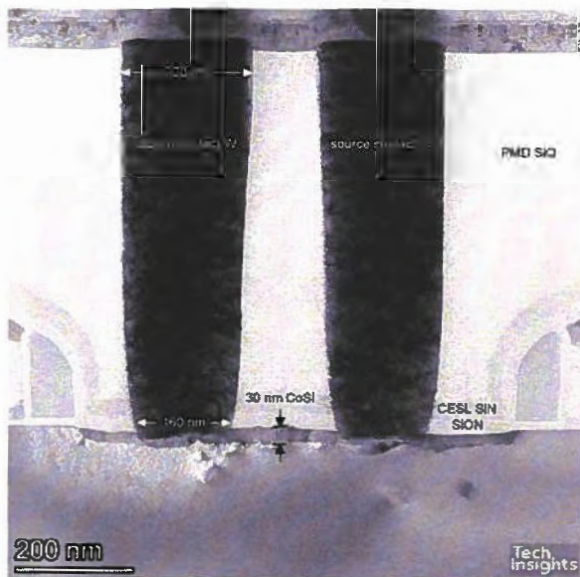
20220329 1616 820 kx 0001_400282.png

HS/LS FET Gate Dielectric – TEM Cross-Section

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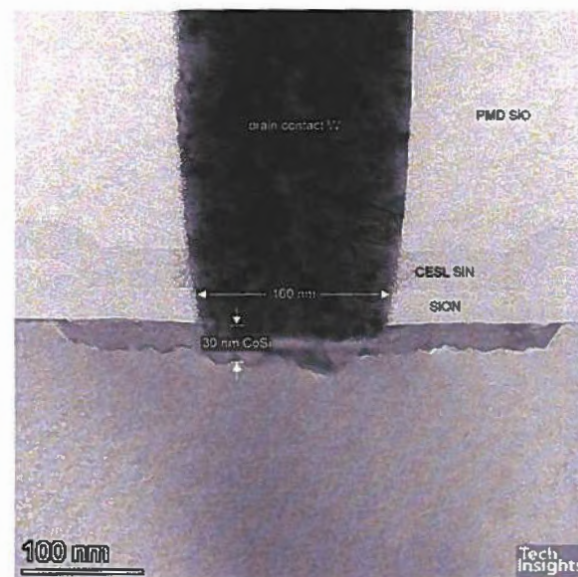
MP9502 Die HS/LS FET Contacts

- A CoSi region up to ~30 nm thick is observed in the source and drain contact regions.
- The S/D contact (W) partially penetrates into the top of the S/D ohmic contact layer (CoSi).
- The W contacts are ~0.22 μm in diameter at the widest portion and narrow down to 0.16 μm at the bottom.



20220329 1631 58000 x_400282.png

HS/LS FET Source Contacts – TEM Cross-Section



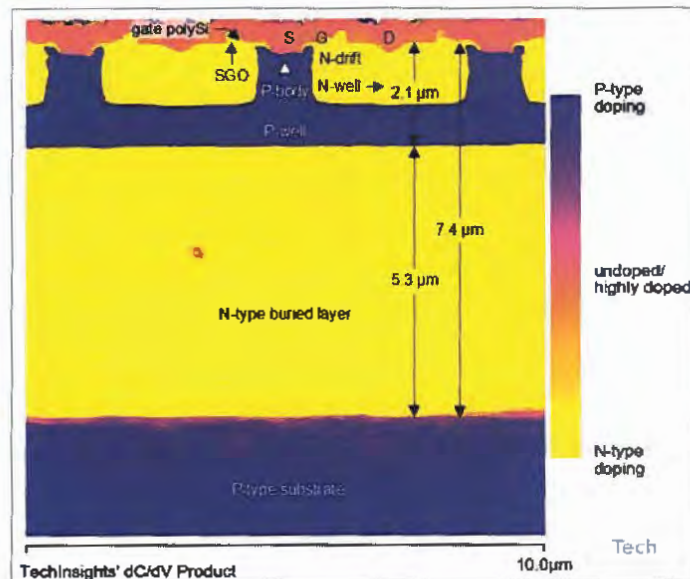
20220329 1555 120 kx_400282.png

HS/LS FET Drain Contact – TEM Cross-Section

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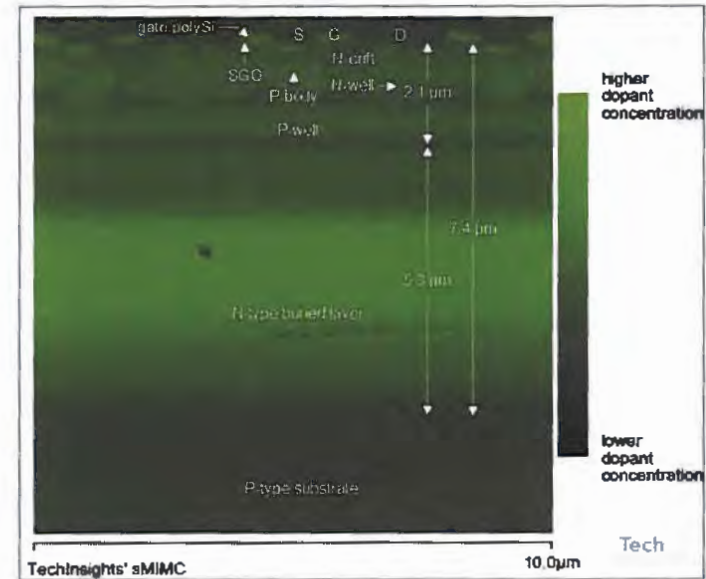
MP9502 Die HSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the HSFET array show the use of a P-type body region, N-type drift region, and a higher-doped N-well at the drain region.
- The P-well layer starts ~2.1 μm from the front surface, while the NBL measures ~5.3 μm thick and reaches ~7.4 μm deep.
- NBL seems to have two regions of higher-doped lower portion and lower-doped upper portion in the Si body.



Array_040522164608_PRODUCT_FRW_10 0u_512p_400973.png

HSFET Array – SCM Cross-Section A-A



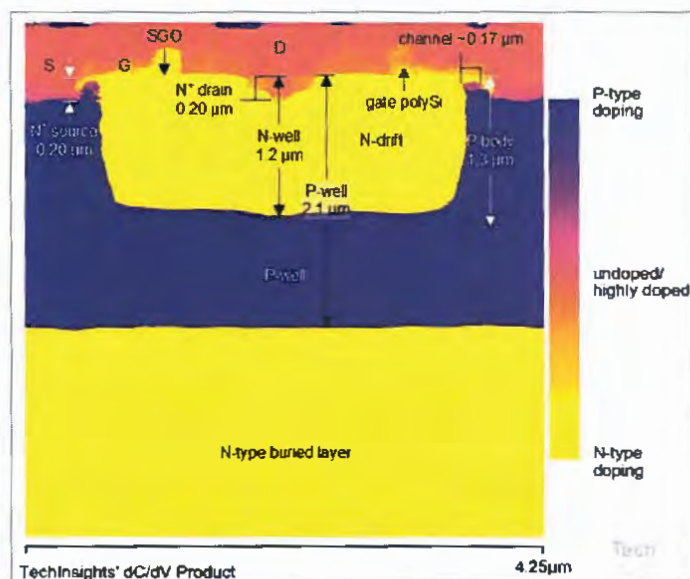
Array_040522164608_SMIMC_FRW_10 0u_512p_400973.png

HSFET Array – sMIM-C Cross-Section A-A

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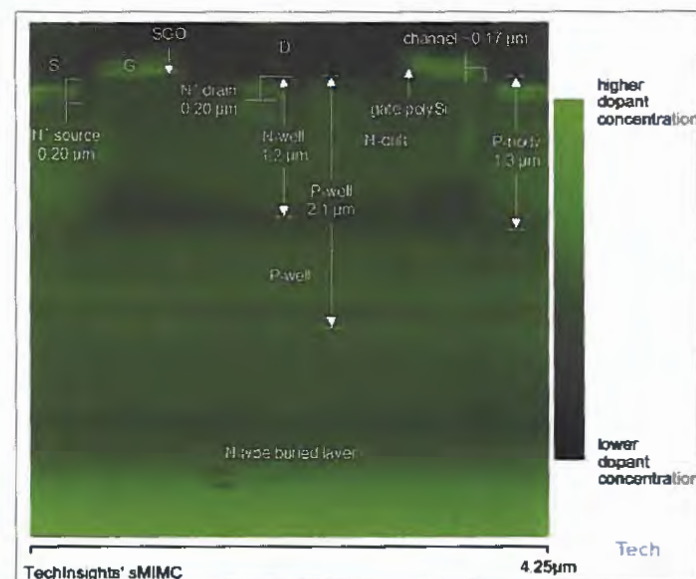
MP9502 Die HSFET – P- and N-Type Regions

- The N+ S/D regions are $\sim 0.20\ \mu\text{m}$ deep.
- The P-body is $\sim 1.3\ \mu\text{m}$ deep, while the drain N-well and N-drift region is $\sim 1.2\ \mu\text{m}$ deep.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.17\ \mu\text{m}$.



Array_040522171710_PRODUCT_FRW_4 25u_512p_400973.png

HSFET – SCM Cross-Section A-A



Array_040522171710_SMIMC_FRW_4 25u_512p_400973.png

HSFET – sMIMC Cross-Section A-A

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Comparison of 0.18 μm BCD Processes

- The MPS MP86905 analyzed in this report is compared with the following 0.18 μm BCD processes previous analyzed by TechInsights:

Feature	MPS MP86905	Maxim MAX77854 [4]	Texas Instruments BQ24260YFF [5]	Qualcomm PM8921 [6]
Device type	PMIC	PMIC	Li-Ion PMIC	PMIC
Mode of operation	PWM	Undetermined	PWM	Undetermined
Rated voltage/current	4.5-18 [*] V/50 A	Undetermined	4.2-28 [*] V/2.5 A	Undetermined
Foundry	Undetermined	Maxim	Texas Instruments	TSMC
Die area (whole die)	3.38 mm × 3.14 mm	4.72 mm × 4.17 mm	2.40 mm × 2.40 mm	6.20 mm × 6.49 mm
Process generation/technology	0.18 μm BCD	0.18 μm BCD S18	0.18 μm LBC8 BCD	0.18 μm BCD
LDMOS cell (drain-to-drain) pitch	HSFET: 4.0 μm LSFET: 3.4 μm	P-LDMOS: 7.2 μm N-LDMOS: 5.0 μm	N-LDMOS Array 1: 4.7 μm N-LDMOS Array 2: 6.8 μm N-LDMOS Array 3: 3.5 μm	P-LDMOS Array 6: 4.3 μm N-LDMOS Array 7: 4.3 μm N-LDMOS Array 5: 9.3 μm
LDMOS gate dielectric thickness	8.5 nm	14 nm	13 nm	14 nm
LDMOS electrical channel length	~0.17 μm	P-LDMOS: 0.64 μm N-LDMOS: 0.68 μm	~0.30 μm	P-LDMOS Array 6: ~0.4 μm (assumed) N-LDMOS Array 7: ~0.8 μm (assumed) N-LDMOS Array 5: ~1.6 μm (assumed)
Isolation type(s)	STI	STI	STI	STI
Silicide	CoSi	CoSi	CoSi	CoSi
Number of metal layers and material	3 Al	4 Al	3 Al	5 Al
Contacts/vias material	W/W	W/W	W/W	W/W
Number of polysilicon layers	1	1	1	1

* The absolute maximum rating voltage

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References

- [1] "Monolithic Power Systems," Monolithic Power Systems website, <https://www.monolithicpower.com/en/about-mps.html> (accessed April 15, 2022)
- [2] "MP86905 Intelli-Phase™ Solution with Integrated HS-/LS-FETs and Driver," MPS datasheet, https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP86905/ (accessed April 15, 2022)
- [3] "Study on 20 V LDMOS With Stepped-Gate-Oxide Structure for PMIC Applications: Design, Fabrication, and Characterization," S. -Y. Chen et al., IEEE Transactions on Electron Devices, Vol. 69, No. 2, pp. 878-881, Feb. 2022, doi: [10.1109/TED.2021.3131922](https://doi.org/10.1109/TED.2021.3131922).
- [4] "Maxim MAX77854 PMIC 180 nm BCD S18 Process Review," *Chipworks*, [PPR-1605-801](#), August 5, 2016
- [5] "Texas Instruments BQ24260YFF Li-Ion Power Management IC (T1 LBC8 Process) Process Review," *Chipworks*, [PPR-1404-801](#), January 7, 2015
- [6] "Qualcomm PM8921 PMIC (TSMC 180 nm BCD) Process Review," *Chipworks*, [PPR-1304-802](#), March 18, 2014

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm ($\pm 1.4\%$) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within $\pm 2\%$ of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of $0.3 \mu\text{m}$ (0.3%) for the micrometer's $100 \mu\text{m}$ pitch lines.

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Statement of Scope Variation

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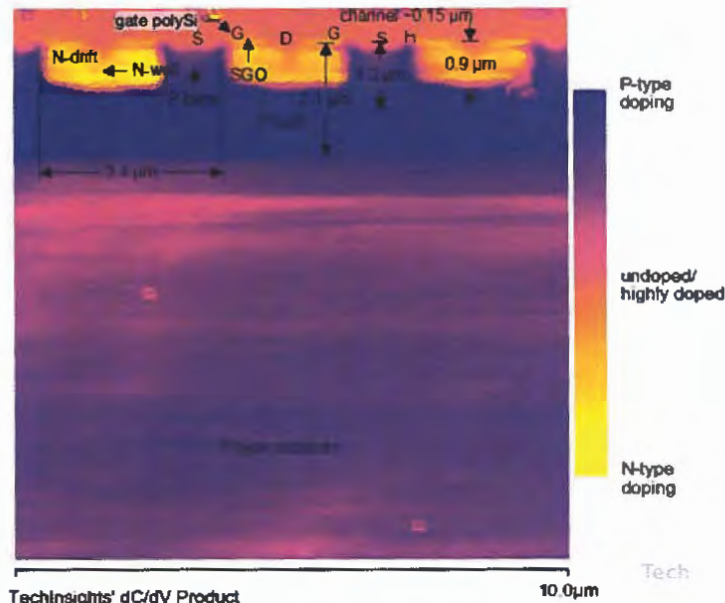
Supplemental Report for PEF-2202-801

(MPS MP86905 Monolithic Integrated HS/LS FETs and Driver
PMIC Power Essentials)

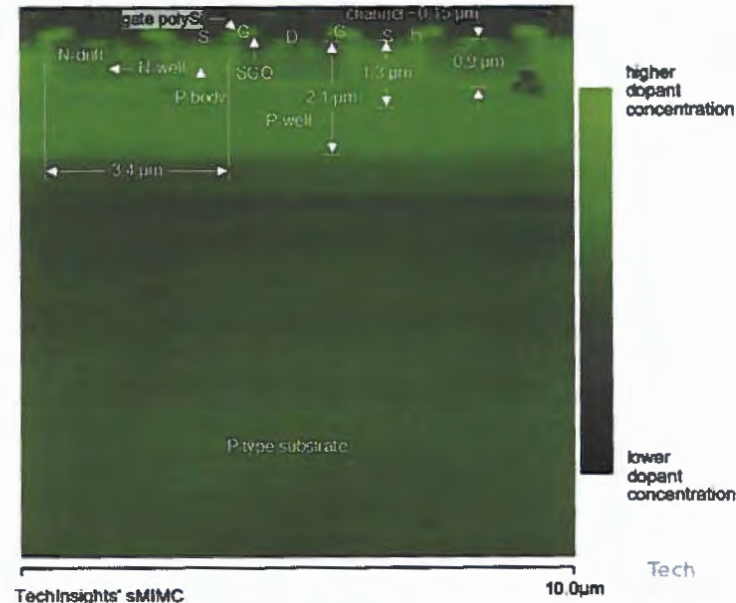
Power Essentials Summary

MP9502 Die LSFET Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the LSFET array show the use of a P-type body region, shallower N-drift/N-well in the drain region, and NBL is absent in the LSFET array.
- The P-well is $\sim 2.1 \mu\text{m}$ deep, the P-body is $\sim 1.3 \mu\text{m}$ deep, while the drain N-drift/N-well is $\sim 0.9 \mu\text{m}$ deep, shallower than $1.2 \mu\text{m}$ observed in the HSFET array.
- Both HSFET and LSFET array likely share the P-well and P-body masks, but use different mask for drain drift region.
- The effective channel length defined by dopant boundary is estimated to be $\sim 0.15 \mu\text{m}$ in the LSFET array.



LSFET Array – SCM Cross-Section A-A



LSFET Array – sMIM-C Cross-Section A-A

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