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(54) **WIRELESS LOCAL AREA NETWORK (WLAN) TECHNOLOGY AND APPLICATIONS INCLUDING TECHNIQUES OF UNIVERSAL FREQUENCY TRANSLATION**

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See application file for complete search history.

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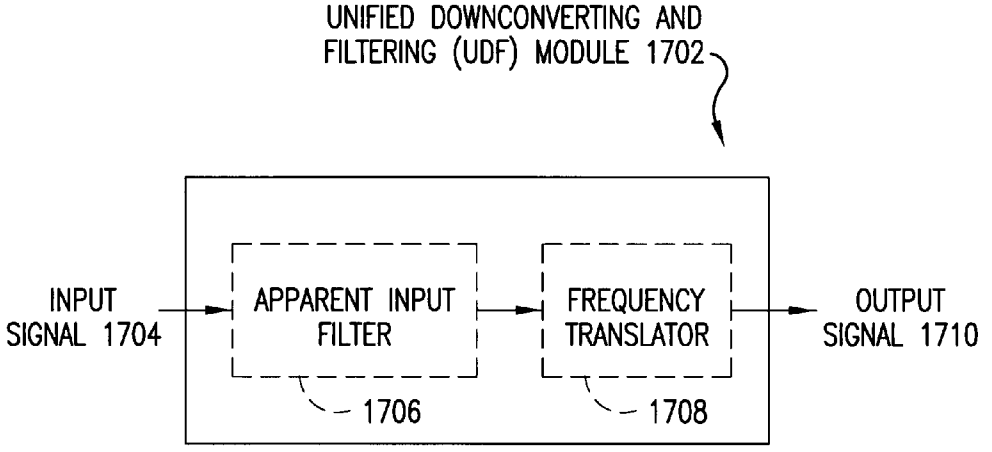
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(57) **ABSTRACT**

Frequency translation and applications of same are described herein, including wireless local area network (WLAN) applications such as IEEE Standard 802.11 WLANs. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

57 Claims, 371 Drawing Sheets



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English-language Abstract of Japanese Patent Publication No. 63-153691, from http://www1.ipdl.jpo.go.jp, 1 Page June 27, 1988—Date of publication of application).

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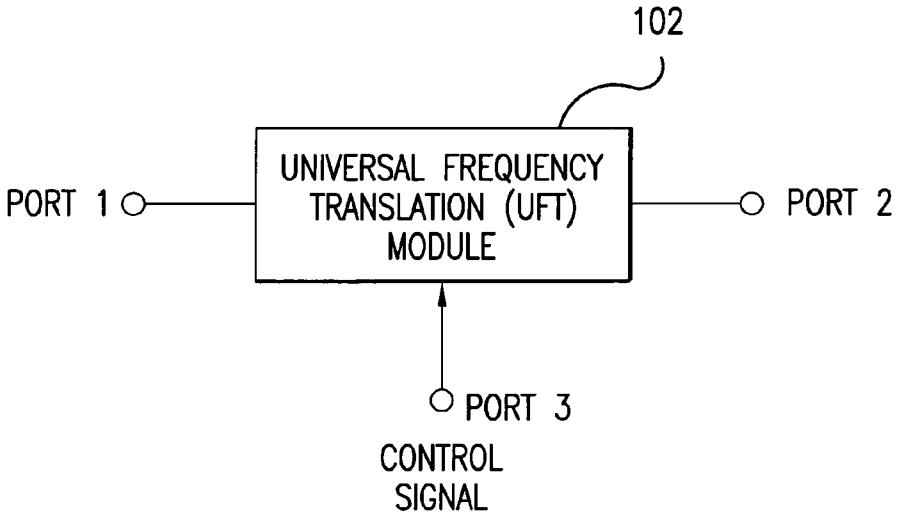

102
UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL

FIG.1A

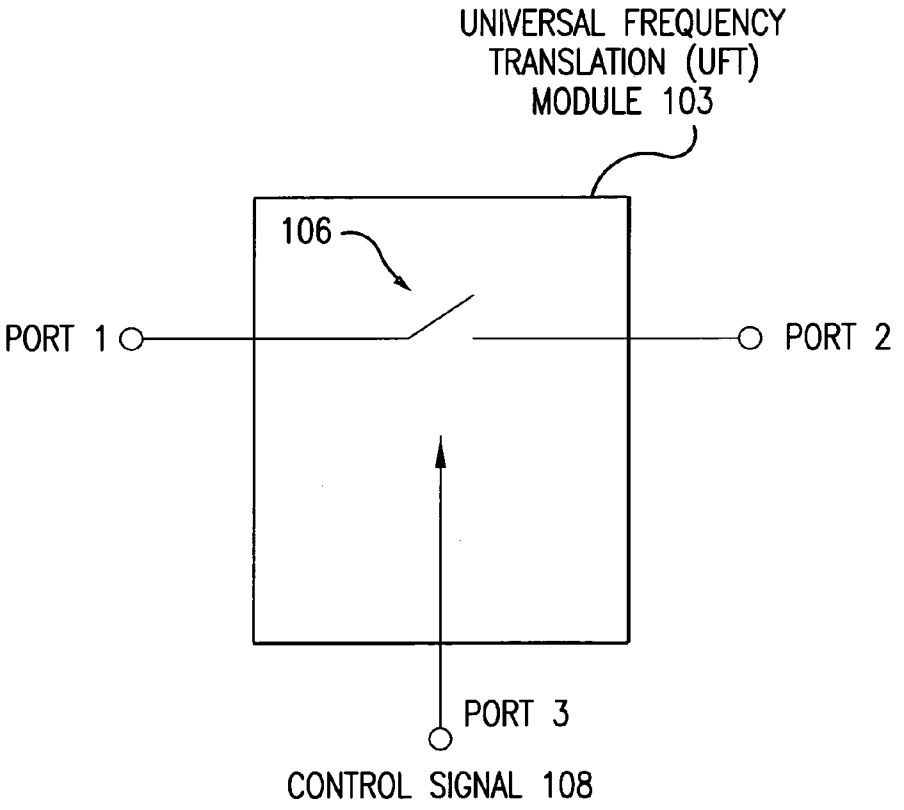

UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE 103
106
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL 108

FIG.1B

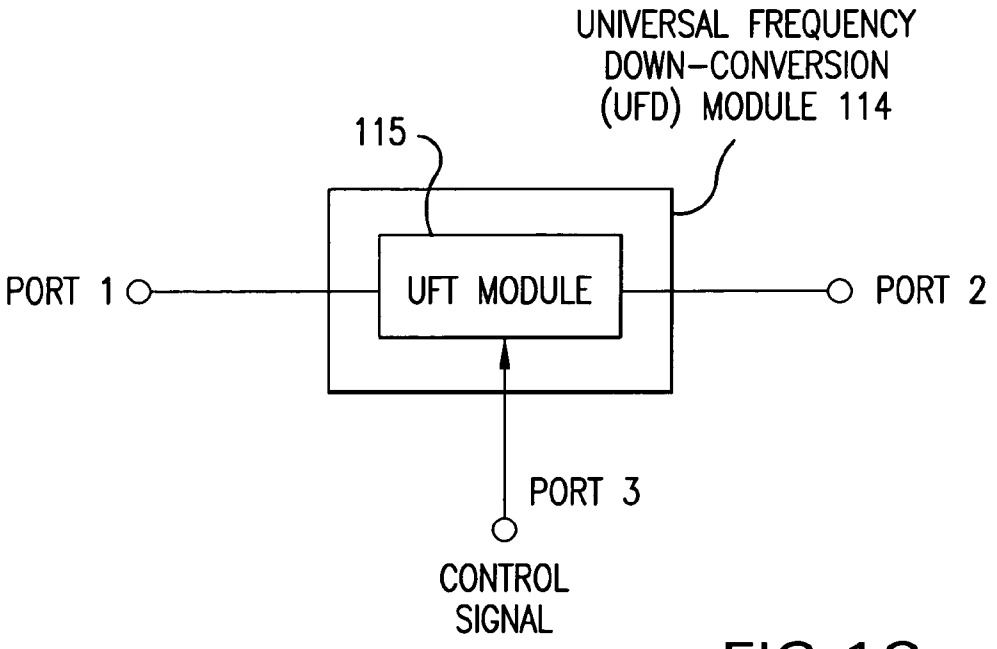

UNIVERSAL FREQUENCY
DOWN-CONVERSION
(UFD) MODULE 114
115
UFT MODULE
PORT 1
PORT 2
PORT 3
CONTROL
SIGNAL

FIG.1C

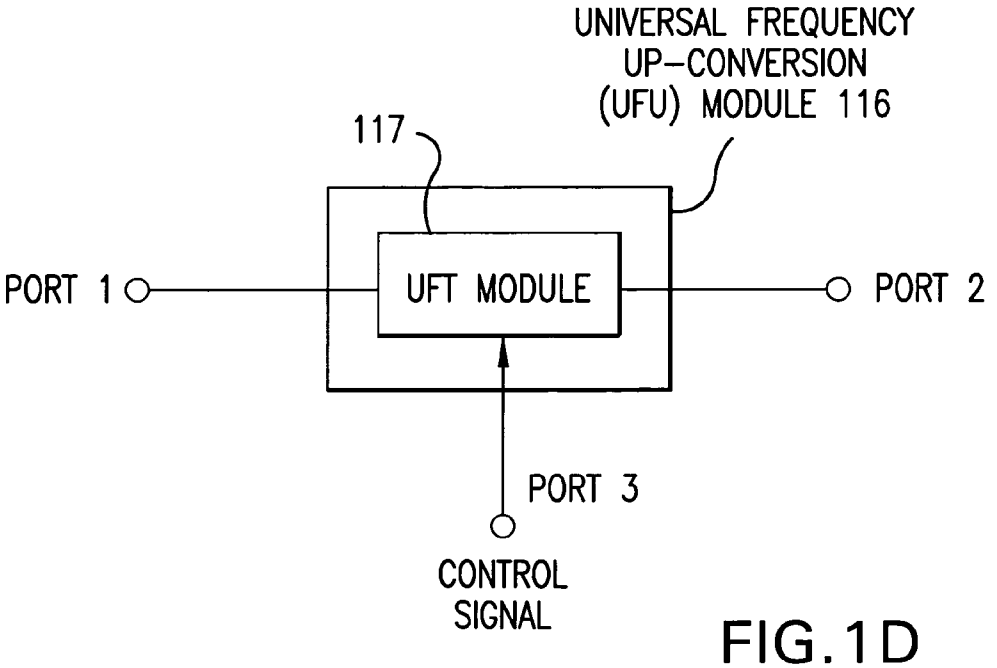

UNIVERSAL FREQUENCY
UP-CONVERSION
(UFU) MODULE 116
117
UFT MODULE
PORT 1
PORT 2
PORT 3
CONTROL
SIGNAL

FIG.1D

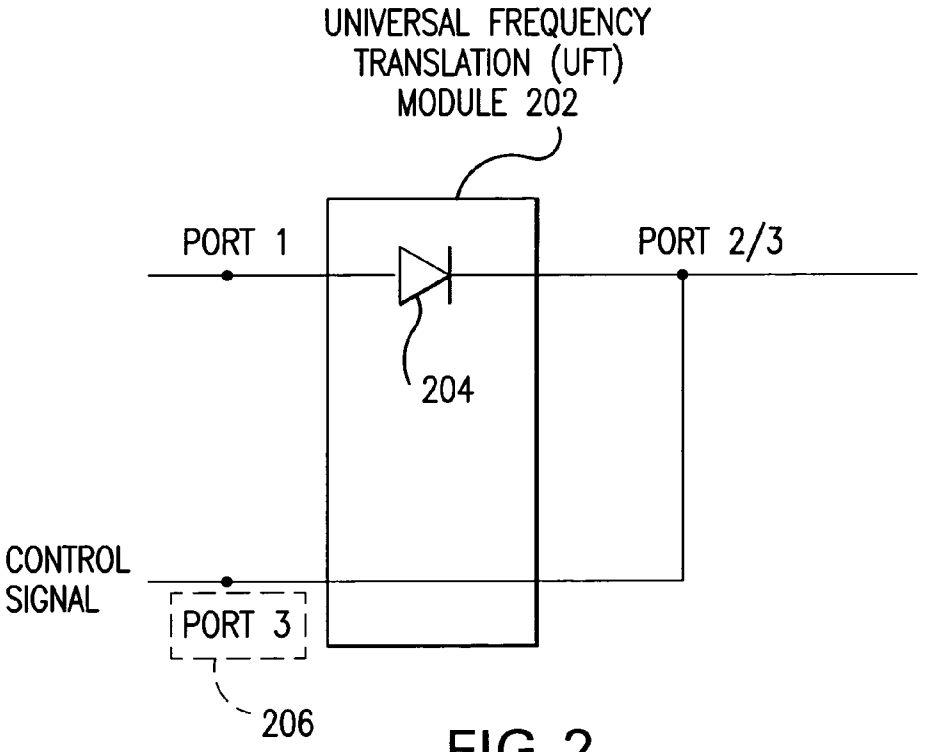

UNIVERSAL FREQUENCY
TRANSLATION (UFT)
MODULE 202
PORT 1
PORT 2/3
204
CONTROL
SIGNAL
PORT 3
206

FIG.2

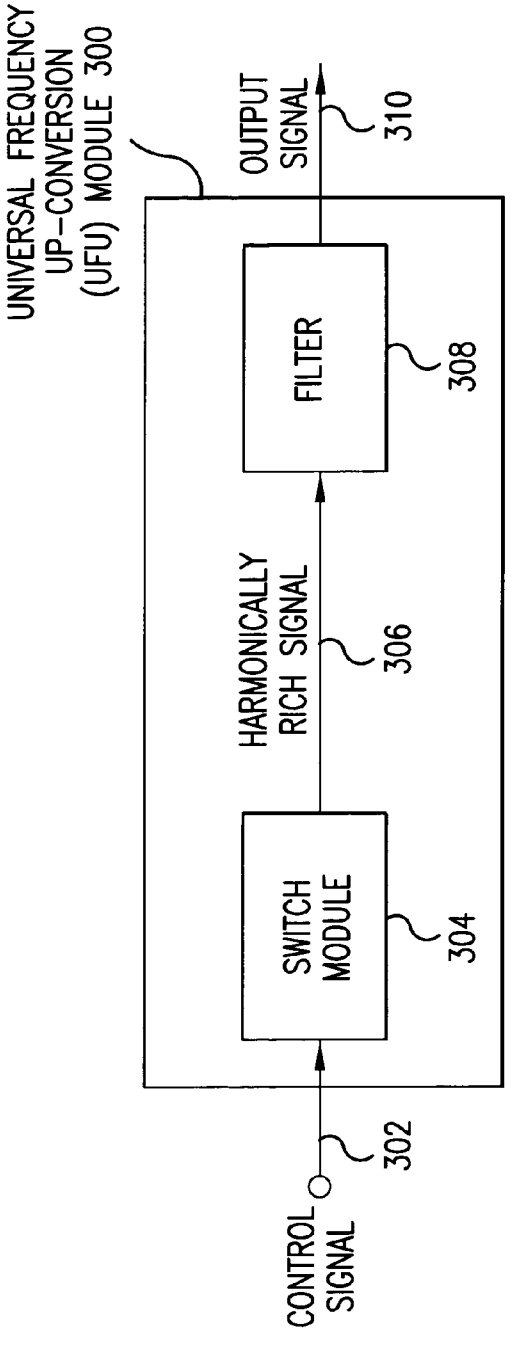

UNIVERSAL FREQUENCY UP-CONVERSION (UFU) MODULE 300
OUTPUT SIGNAL
310
FILTER
308
HARMONICALLY RICH SIGNAL
306
SWITCH MODULE
304
CONTROL SIGNAL
302

FIG.3

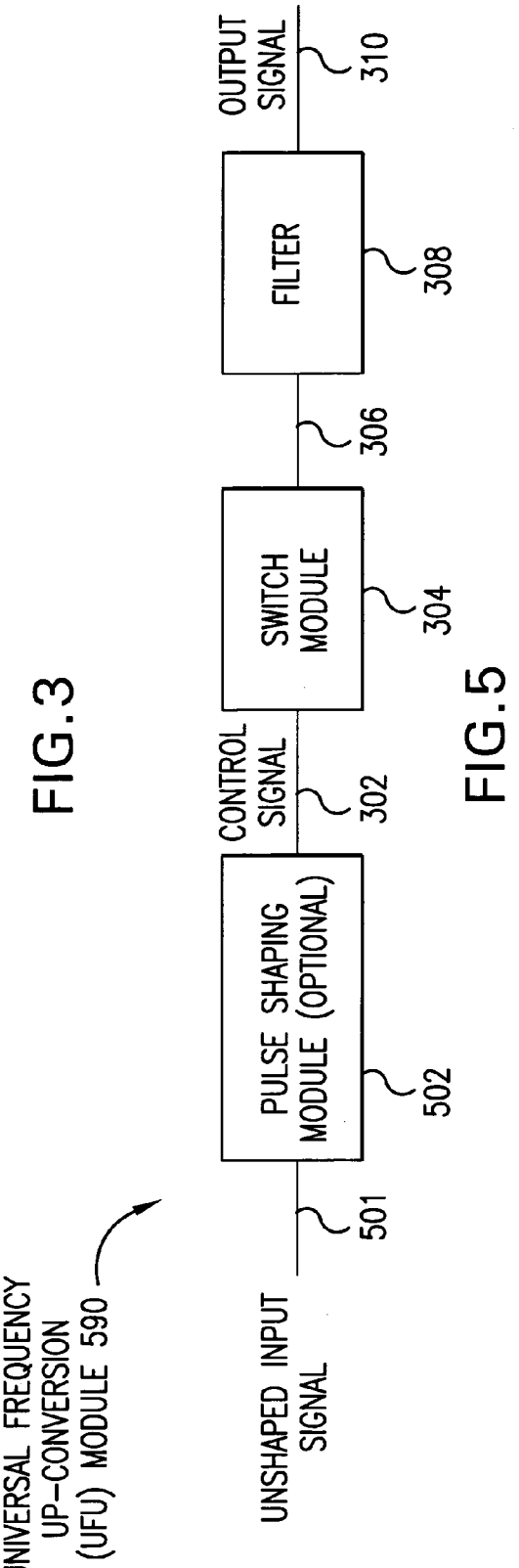

UNIVERSAL FREQUENCY UP-CONVERSION (UFU) MODULE 590
OUTPUT SIGNAL
310
FILTER
308
306
SWITCH MODULE
304
CONTROL SIGNAL
302
PULSE SHAPING MODULE (OPTIONAL)
502
501
UNSHAPED INPUT SIGNAL

FIG.5

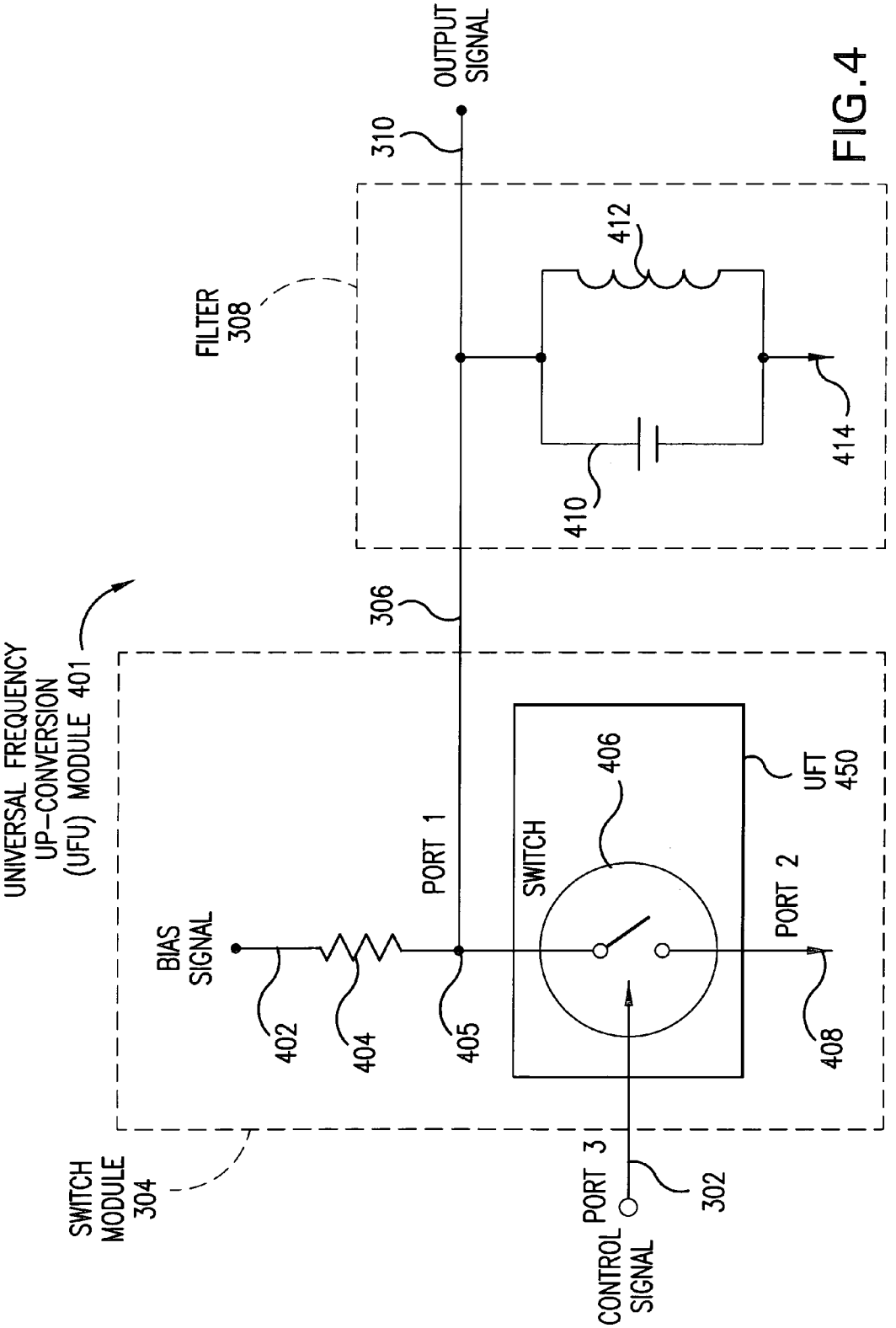

OUTPUT SIGNAL
310
FILTER 308
412
414
410
306
UNIVERSAL FREQUENCY UP-CONVERSION (UFU) MODULE 401
BIAS SIGNAL
402
404
405
PORT 1
SWITCH
406
PORT 2
UFT 450
408
SWITCH MODULE 304
PORT 3
CONTROL SIGNAL
302

FIG. 4

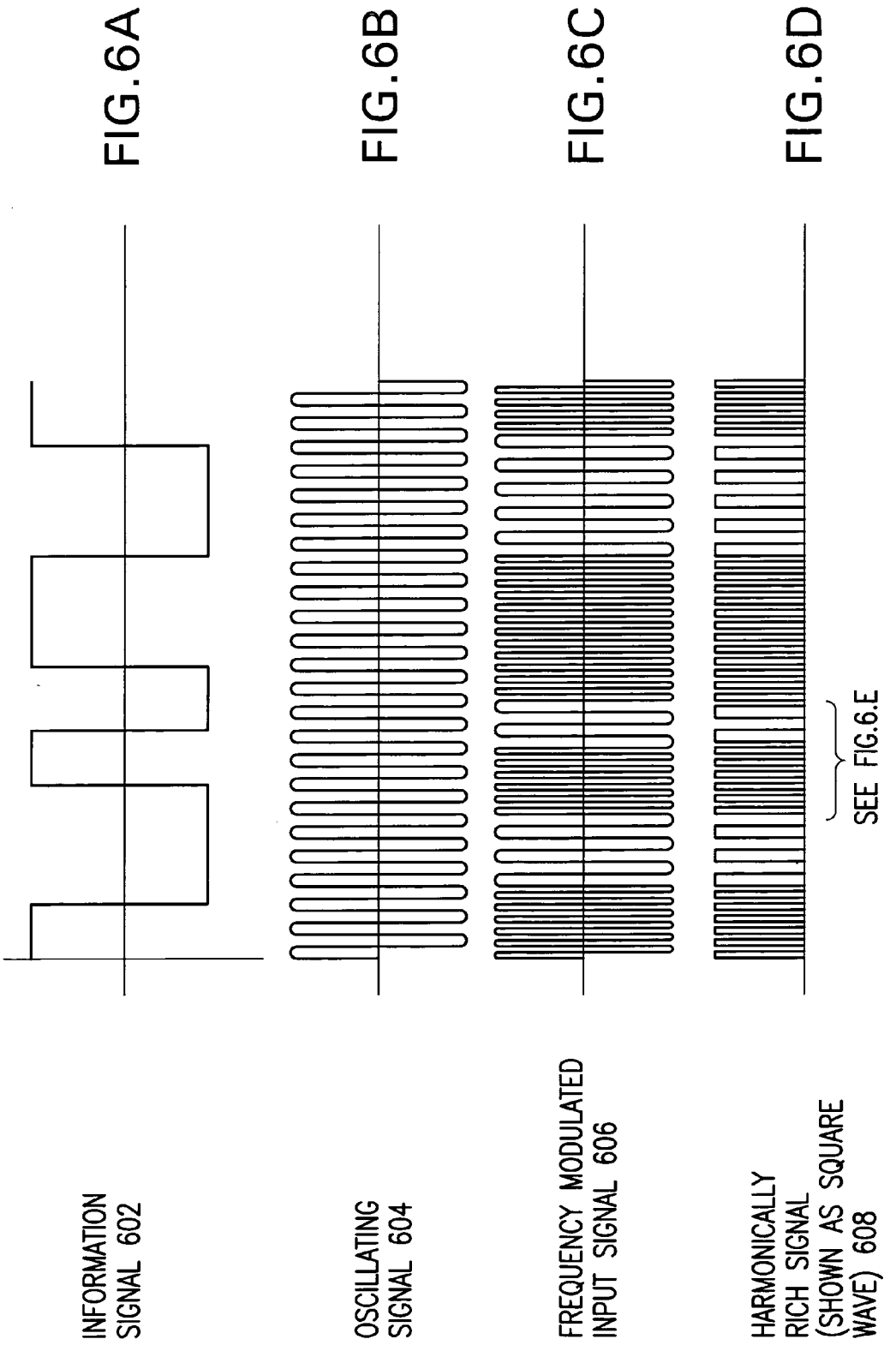

FIG.6A
FIG.6B
FIG.6C
FIG.6D
INFORMATION SIGNAL 602
OSCILLATING SIGNAL 604
FREQUENCY MODULATED INPUT SIGNAL 606
HARMONICALLY RICH SIGNAL (SHOWN AS SQUARE WAVE) 608
SEE FIG.6.E

FIG.6E

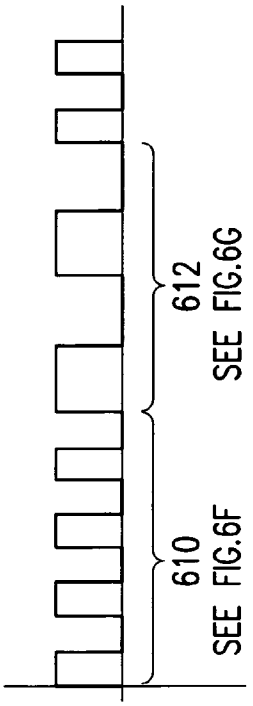


FIG.6F

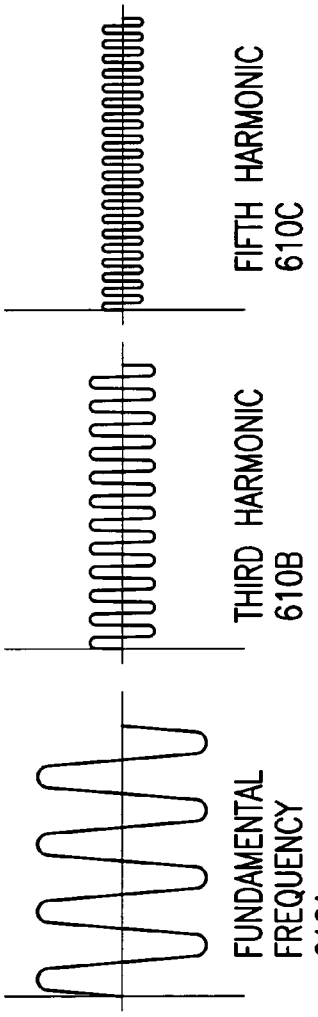
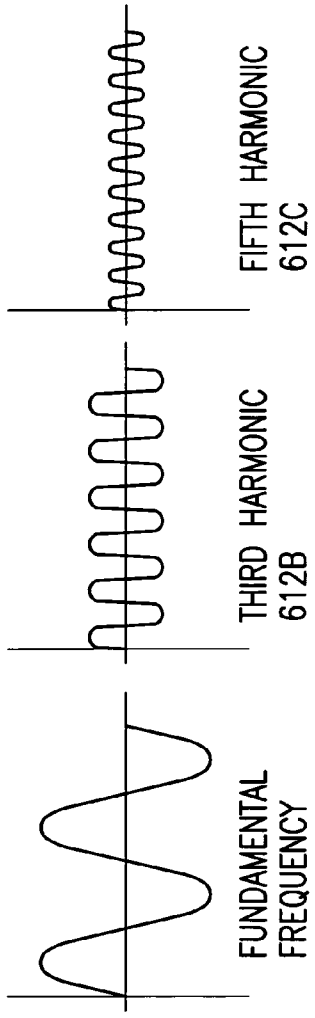


FIG.6G



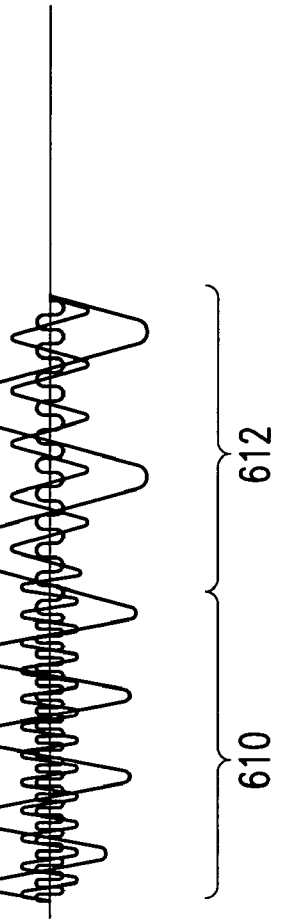

HARMONICS OF SIGNALS 610 AND 612 (SHOWN SIMULTANEOUSLY BUT NOT SUMMED)
610
612

FIG.6H

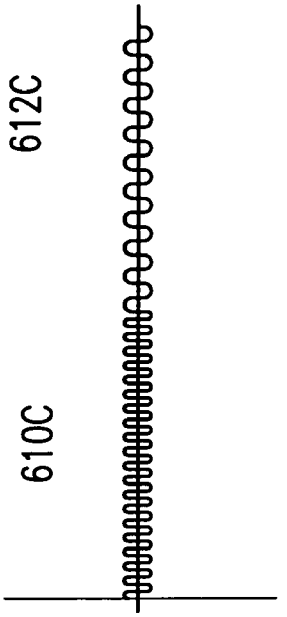

FILTERED OUTPUT SIGNAL 614
610C
612C

FIG.6I

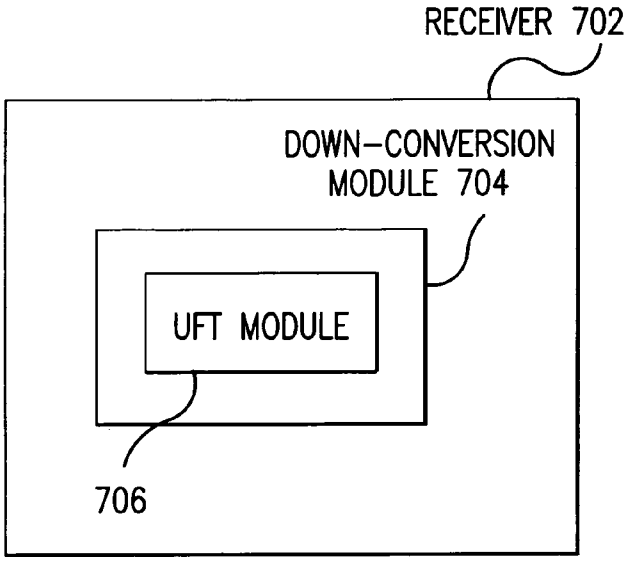


FIG.7

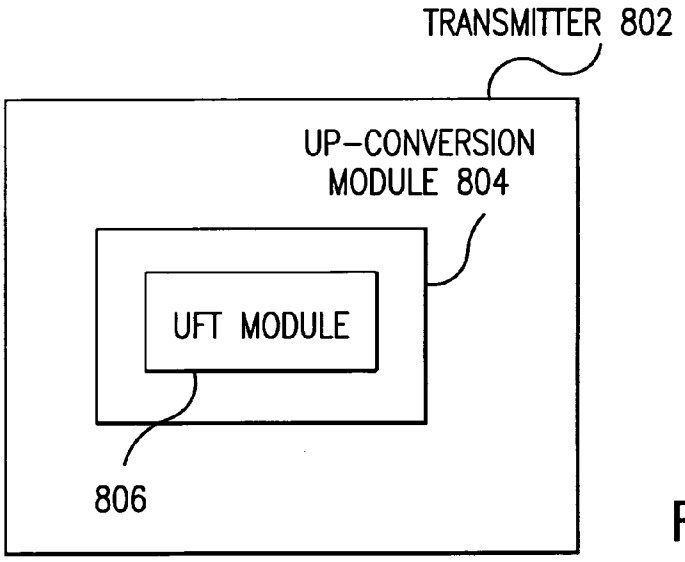


FIG.8

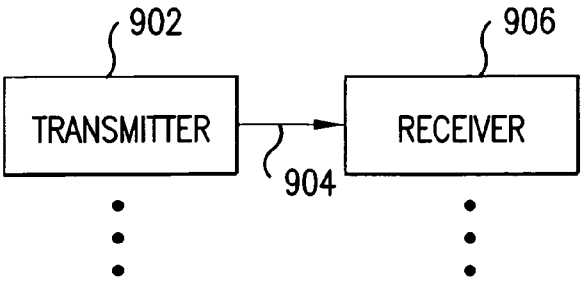


FIG.9

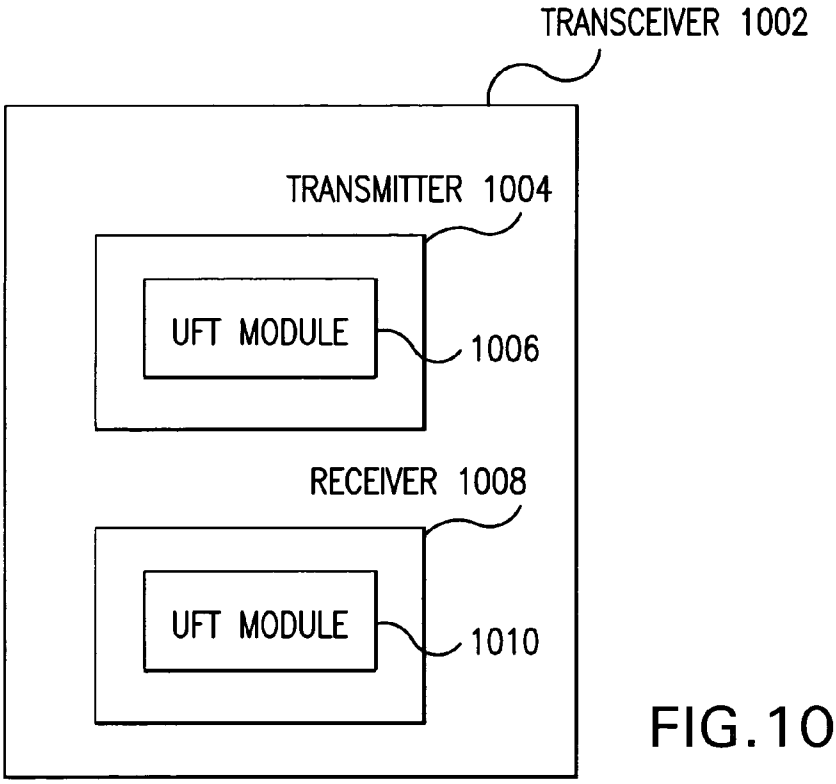

TRANSCEIVER 1002
TRANSMITTER 1004
UFT MODULE
1006
RECEIVER 1008
UFT MODULE
1010

FIG.10

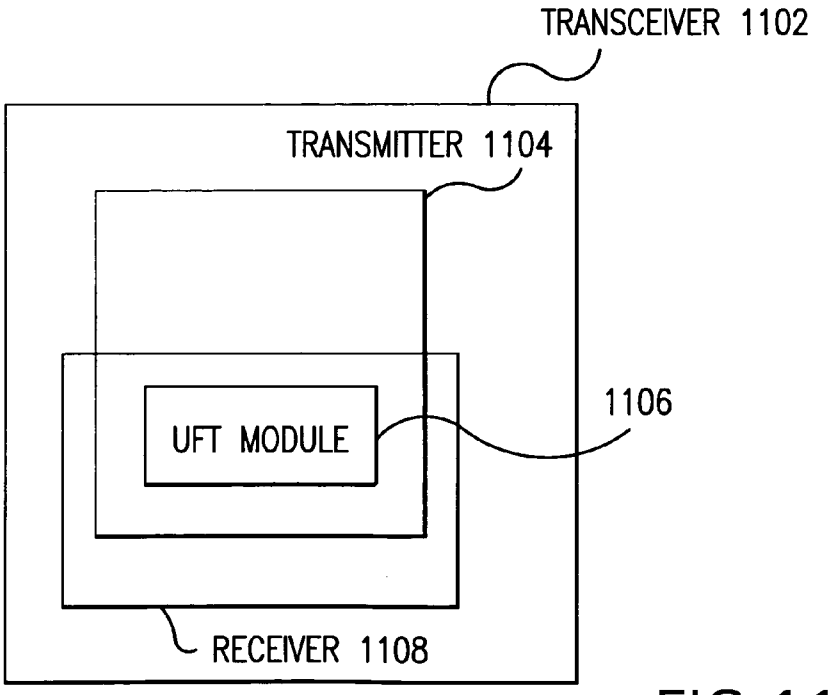

TRANSCEIVER 1102
TRANSMITTER 1104
UFT MODULE
1106
RECEIVER 1108

FIG.11

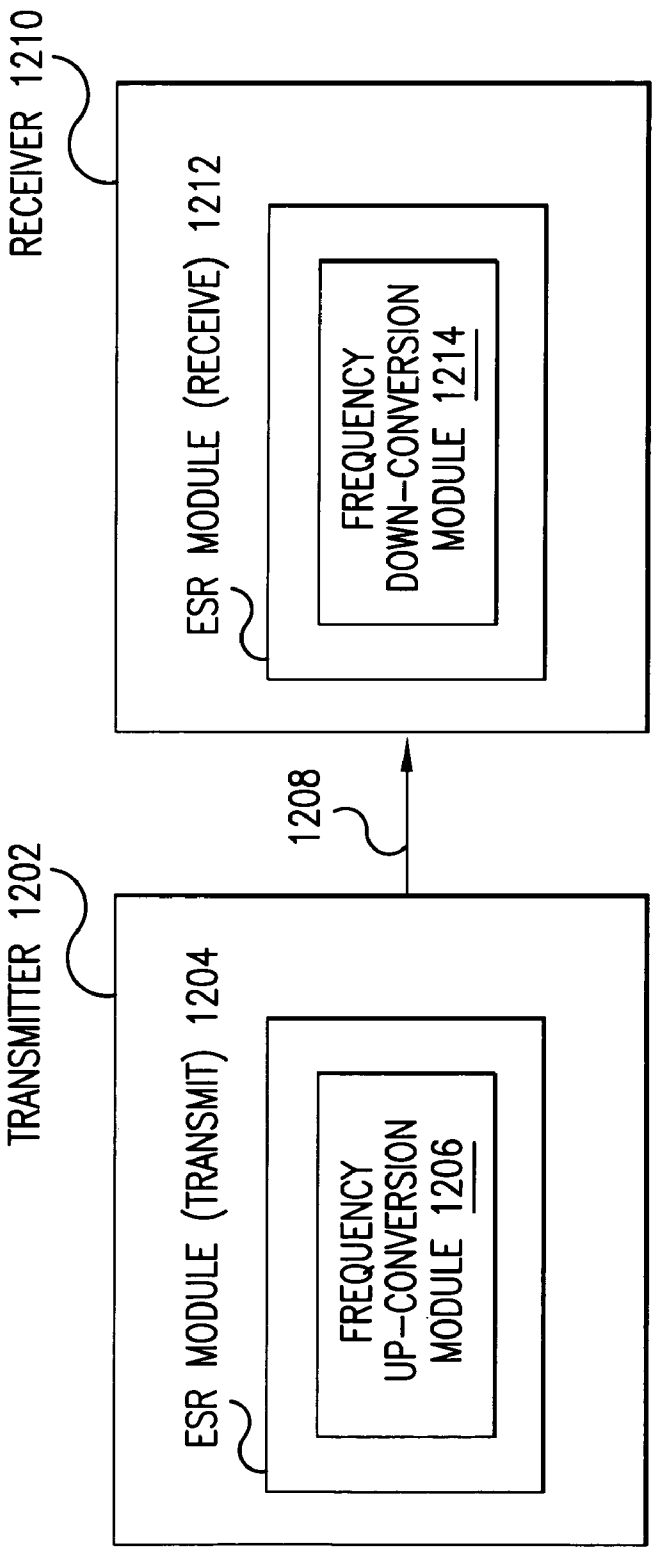

RECEIVER 1210
ESR MODULE (RECEIVE) 1212
FREQUENCY DOWN-CONVERSION MODULE 1214
1208
TRANSMITTER 1202
ESR MODULE (TRANSMIT) 1204
FREQUENCY UP-CONVERSION MODULE 1206

FIG. 12

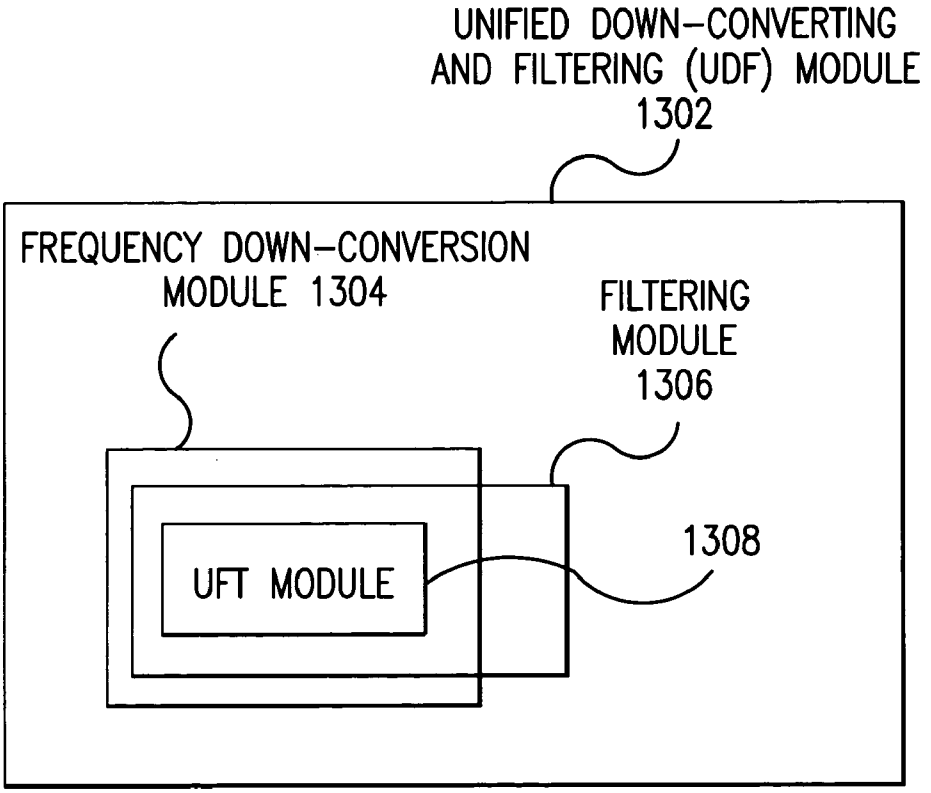

UNIFIED DOWN-CONVERTING
AND FILTERING (UDF) MODULE
1302
FREQUENCY DOWN-CONVERSION
MODULE 1304
FILTERING
MODULE
1306
1308
UFT MODULE

FIG.13

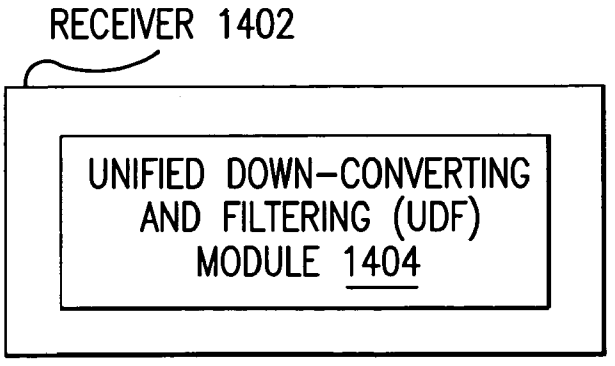

RECEIVER 1402
UNIFIED DOWN-CONVERTING
AND FILTERING (UDF)
MODULE 1404

FIG.14

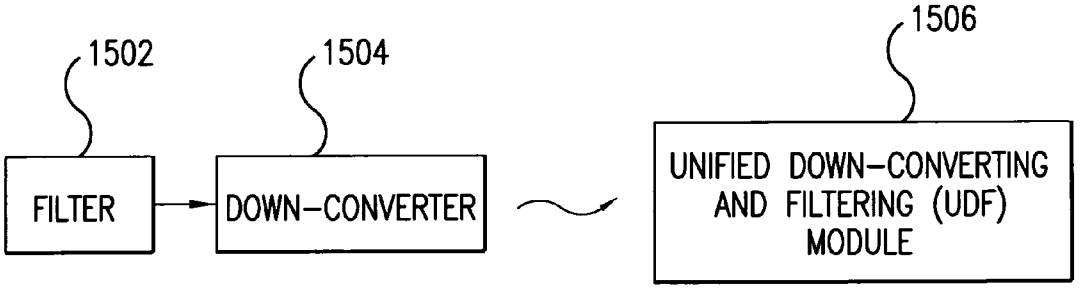


FIG.15A

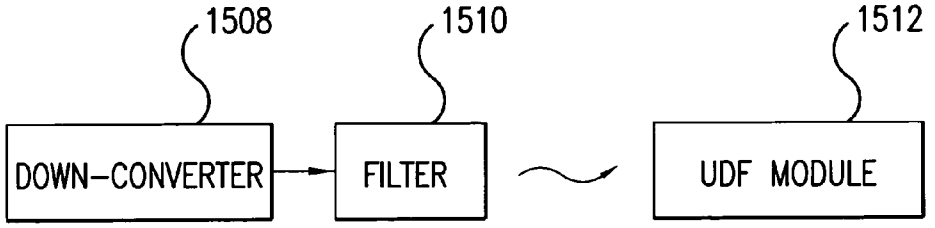


FIG.15B

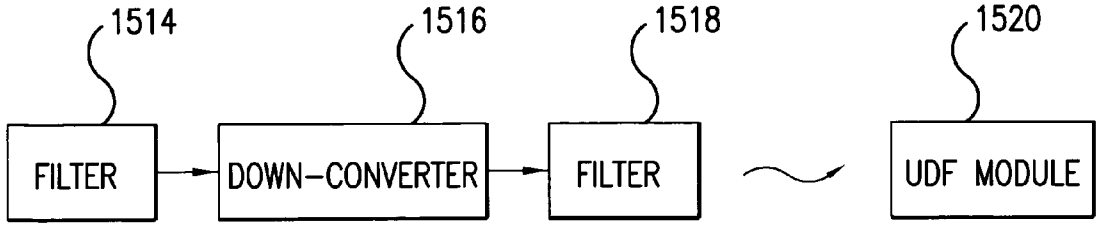


FIG.15C

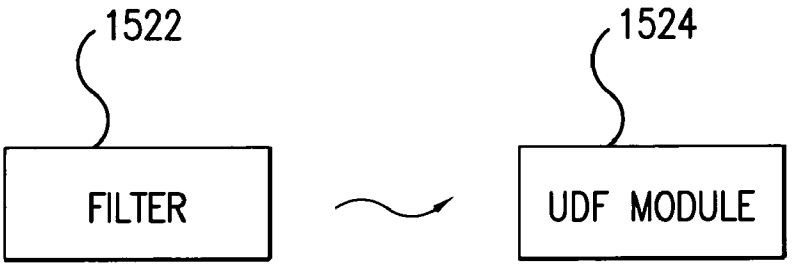


FIG.15D

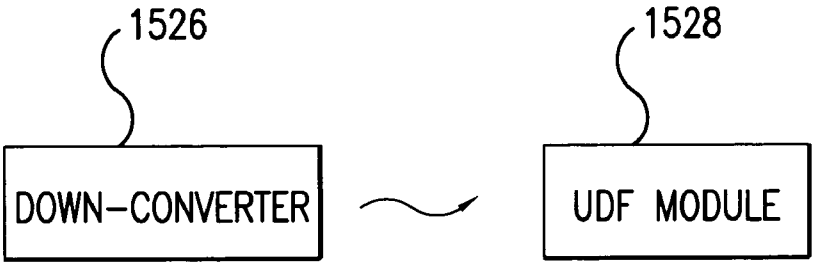


FIG.15E

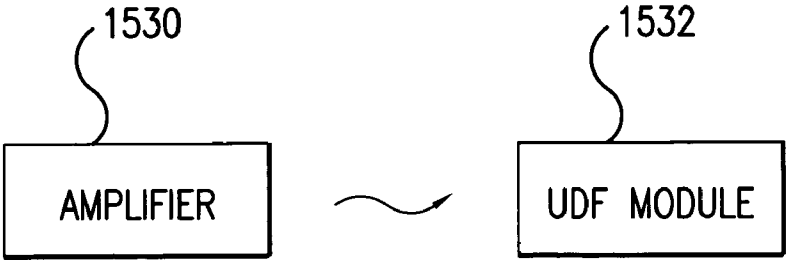


FIG.15F

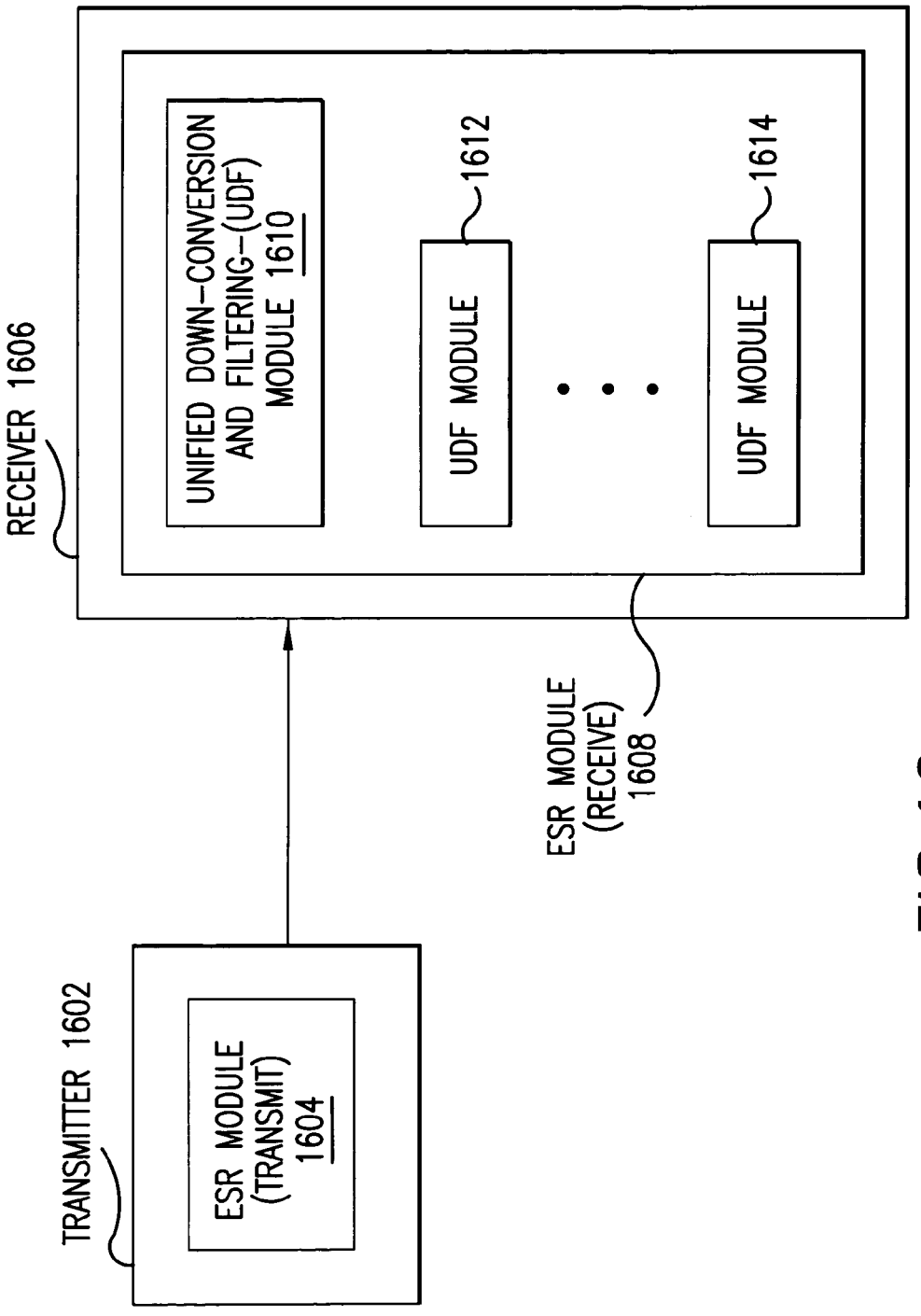

TRANSMITTER 1602
ESR MODULE (TRANSMIT) 1604
RECEIVER 1606
UNIFIED DOWN-CONVERSION AND FILTERING-(UDF) MODULE 1610
UDF MODULE
1612
UDF MODULE
1614
ESR MODULE (RECEIVE) 1608

FIG.16

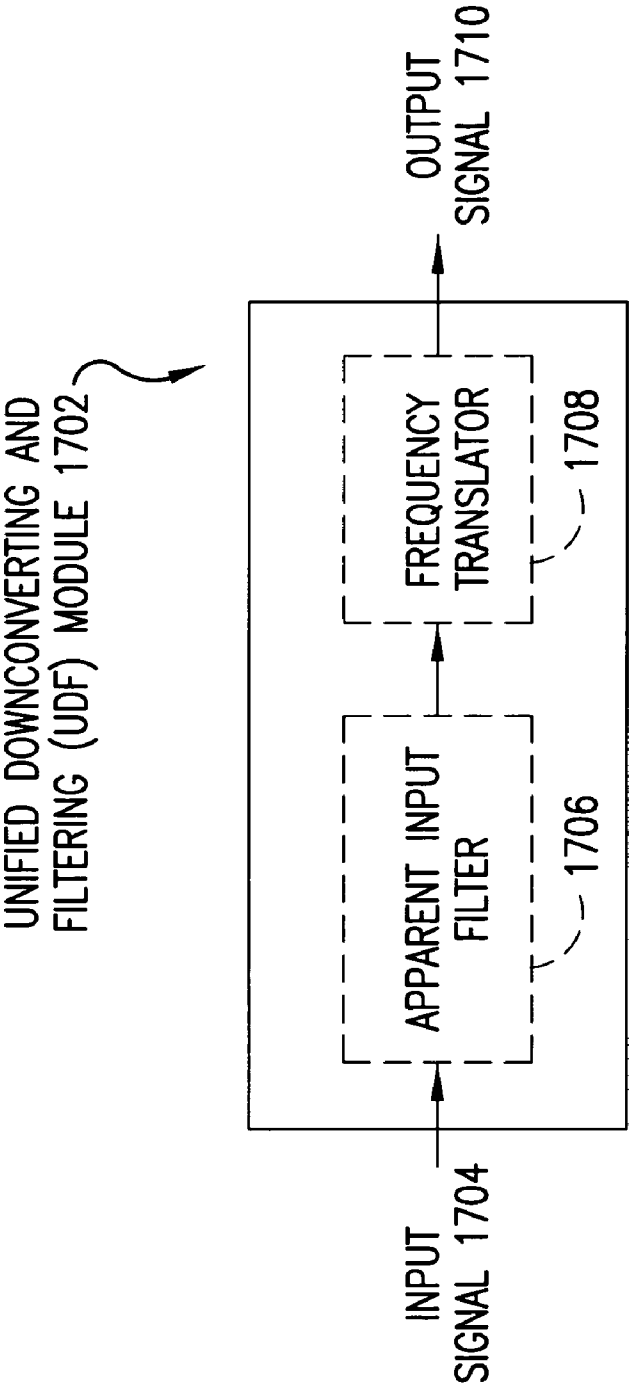

UNIFIED DOWNCONVERTING AND FILTERING (UDF) MODULE 1702
INPUT SIGNAL 1704
APPARENT INPUT FILTER
1706
FREQUENCY TRANSLATOR
1708
OUTPUT SIGNAL 1710

FIG. 17

1802

TIME / NODE	t−1 (RISING EDGE OF Φ_1)		t−1 (RISING EDGE OF Φ_2)		t (RISING EDGE OF Φ_1)		t (RISING EDGE OF Φ_2)		t+1 (RISING EDGE OF Φ_1)	
1902	VI_{t-1}	1804	VI_{t-1}	1808	VI_t	1816	VI_t	1826	VI_{t+1}	1838
1904	—		VI_{t-1}	1810	VI_{t-1}	1818	VI_t	1828	VI_t	1840
1906	VO_{t-1}	1806	VO_{t-1}	1812	VO_t	1820	VO_t	1830	VO_{t+1}	1842
1908	—		VO_{t-1}	1814	VO_{t-1}	1822	VO_t	1832	VO_t	1844
1910	—	1807	—		VO_{t-1}	1824	VO_{t-1}	1834	VO_t	1846
1912	—		—	1815	—		VO_{t-1}	1836	VO_{t-1}	1848
1918	—		—		—		—		VI_t − 0.1 * VO_t − 0.8 * VO_{t-1}	1850

FIG. 18

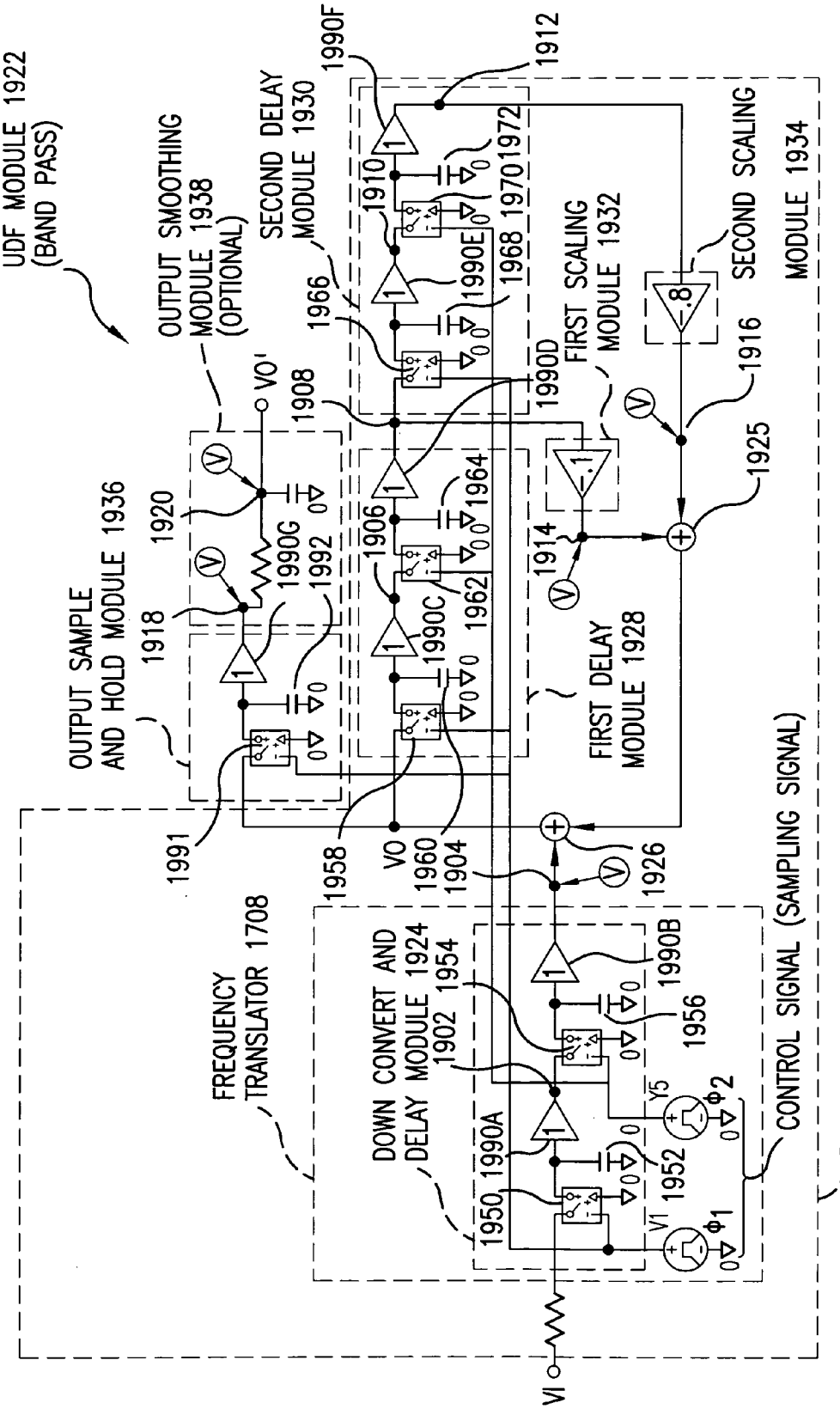

UDF MODULE 1922
(BAND PASS)
OUTPUT SMOOTHING
MODULE 1938
(OPTIONAL)
SECOND DELAY
MODULE 1930
FIRST SCALING
MODULE 1932
SECOND SCALING
MODULE 1934
OUTPUT SAMPLE
AND HOLD MODULE 1936
FIRST DELAY
MODULE 1928
FREQUENCY
TRANSLATOR 1708
DOWN CONVERT AND
DELAY MODULE 1924
CONTROL SIGNAL (SAMPLING SIGNAL)
INPUT FILTER 1706
VI
VO
VO'
1902
1904
1906
1908
1910
1912
1914
1916
1918
1920
1925
1926
1950
1952
1954
1956
1958
1960
1962
1964
1966
1968
1970
1972
1990A
1990B
1990C
1990D
1990E
1990F
1991
1992
.1
.8
Y1
Y5
Φ1
Φ2

FIG.19

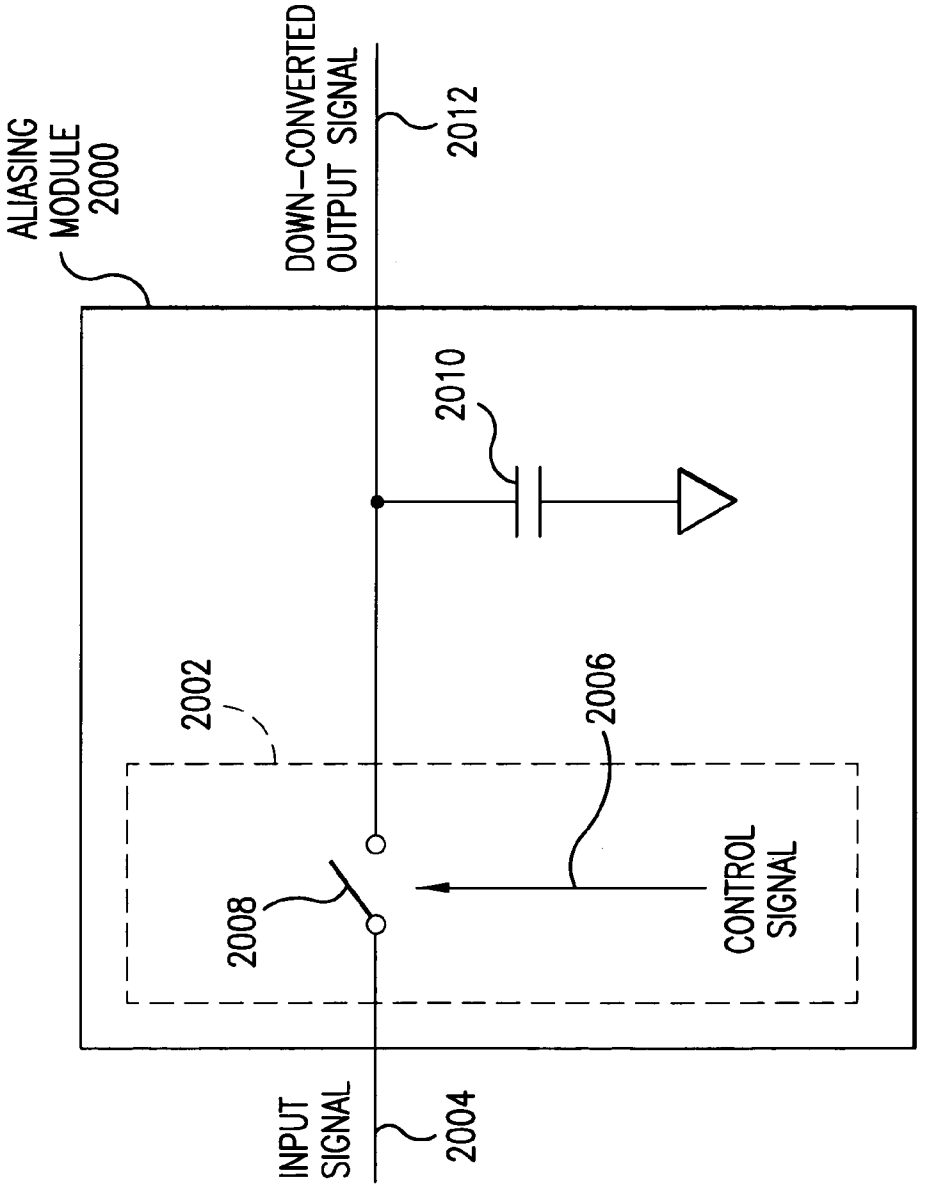

ALIASING MODULE 2000
DOWN-CONVERTED OUTPUT SIGNAL
2012
2010
2002
2006
2008
CONTROL SIGNAL
INPUT SIGNAL
2004

FIG.20A

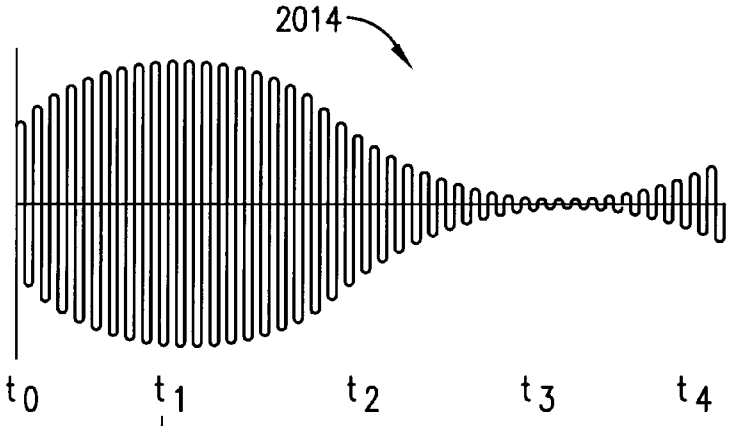


FIG.20B

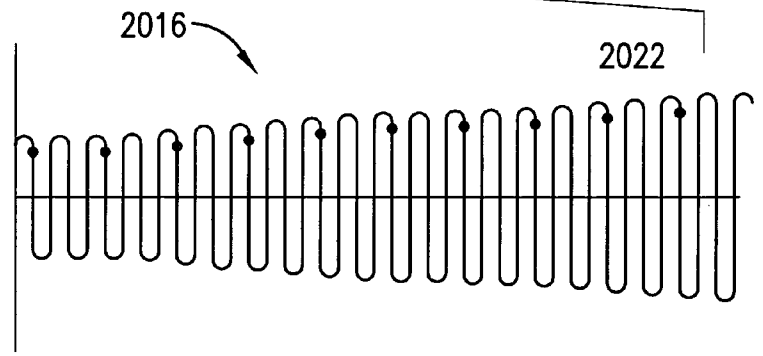


FIG.20C

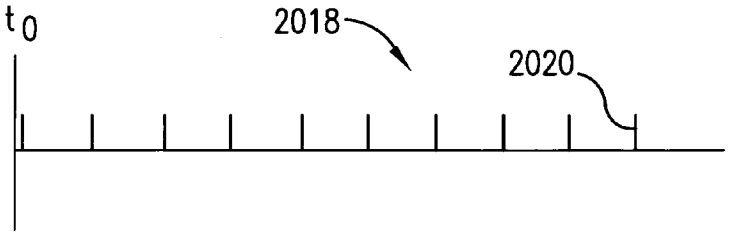


FIG.20D

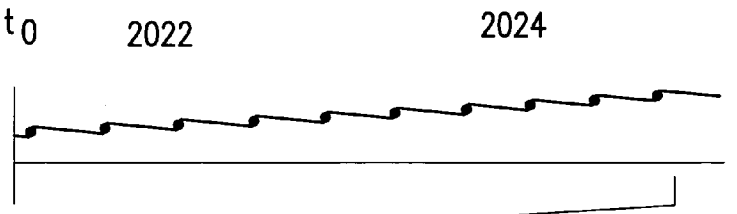


FIG.20E

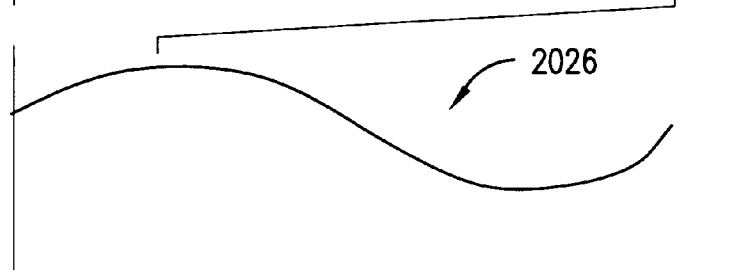


FIG.20F

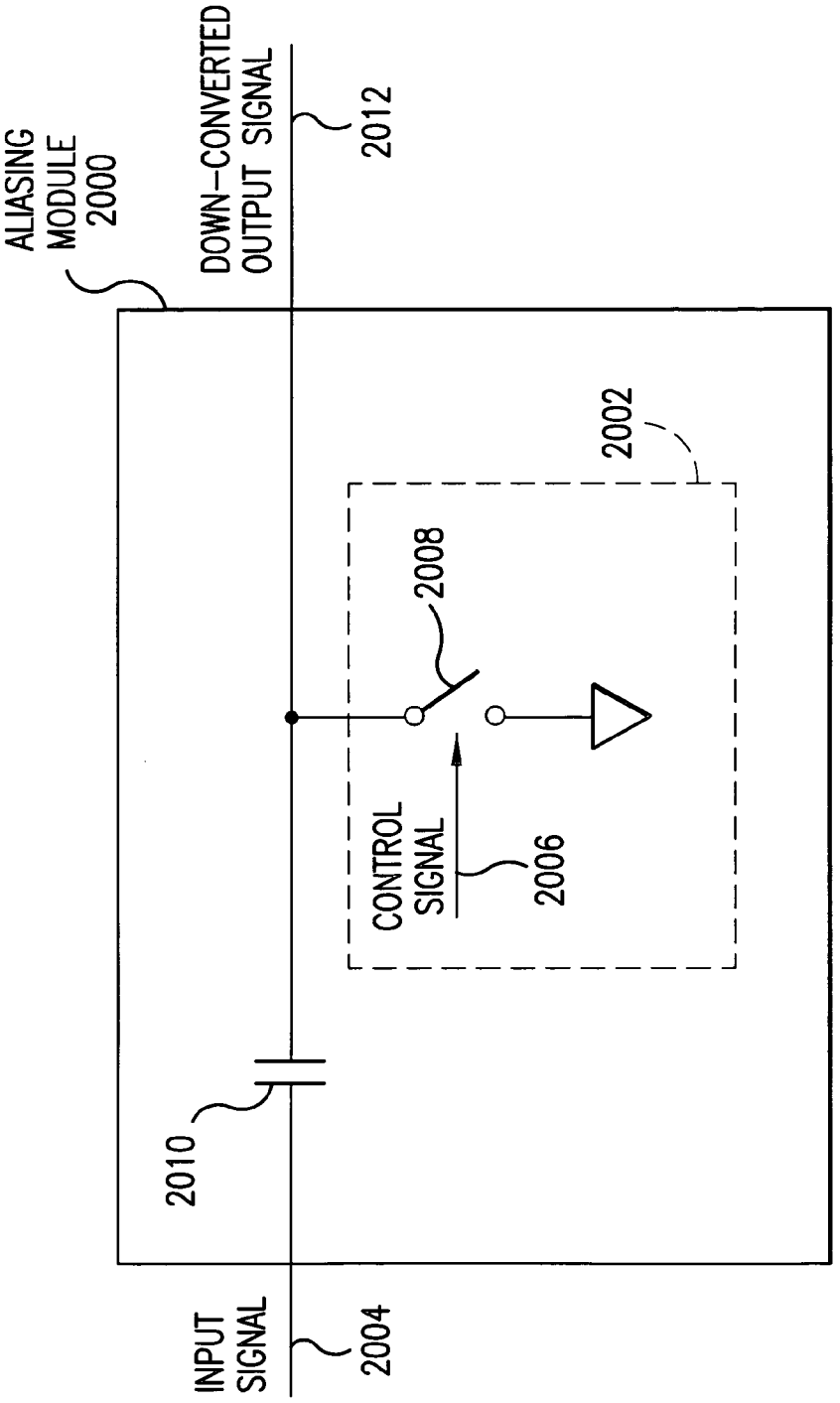

ALIASING MODULE 2000
DOWN-CONVERTED OUTPUT SIGNAL
2012
2002
2008
CONTROL SIGNAL
2006
2010
INPUT SIGNAL
2004

FIG.20G

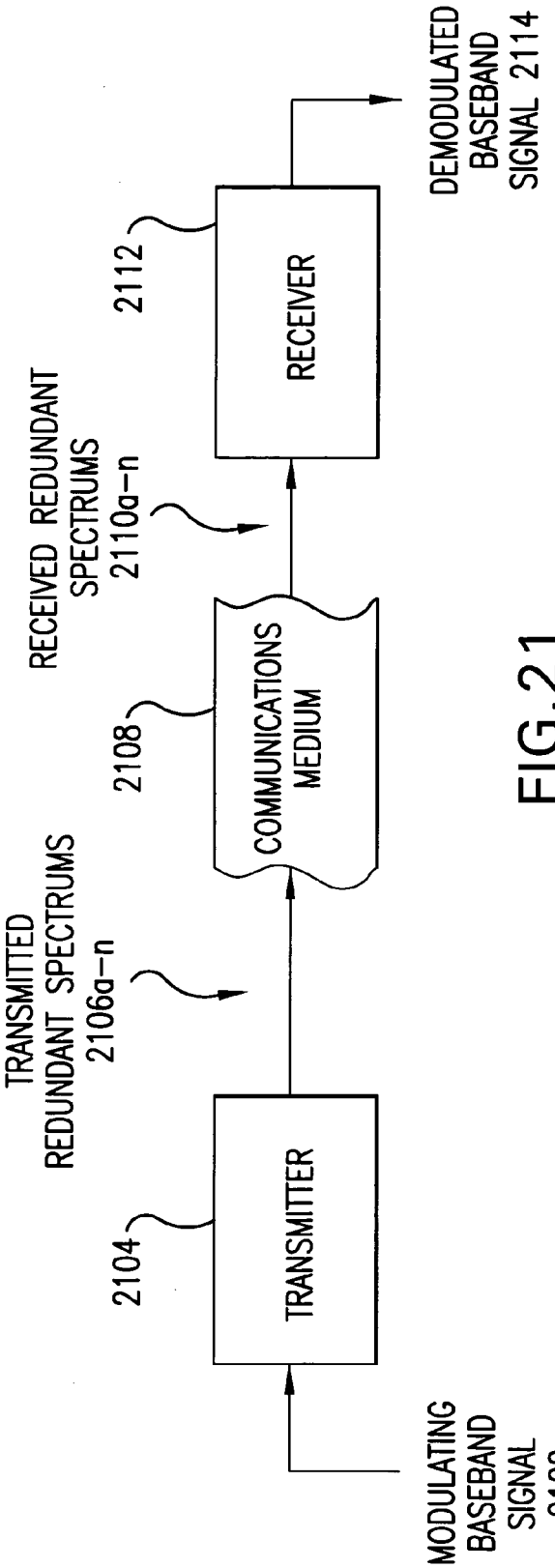

MODULATING BASEBAND SIGNAL 2102
2104
TRANSMITTER
TRANSMITTED REDUNDANT SPECTRUMS 2106a–n
2108
COMMUNICATIONS MEDIUM
RECEIVED REDUNDANT SPECTRUMS 2110a–n
2112
RECEIVER
DEMODULATED BASEBAND SIGNAL 2114

FIG.21

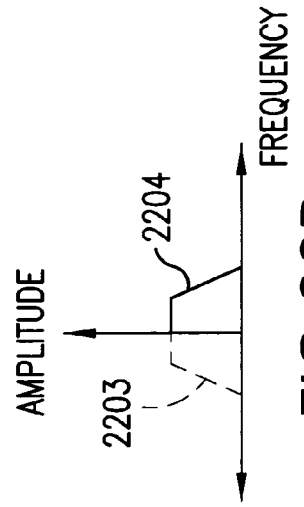


FIG.22B

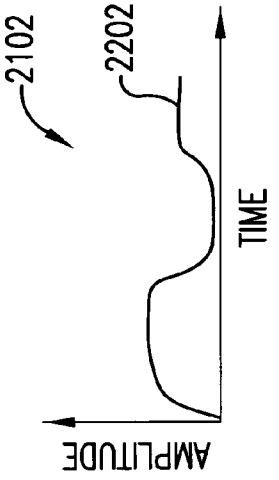


FIG.22A

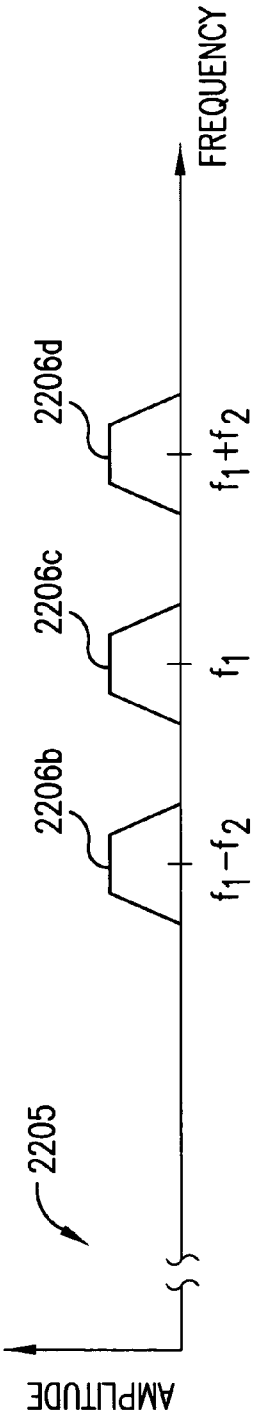


FIG.22C

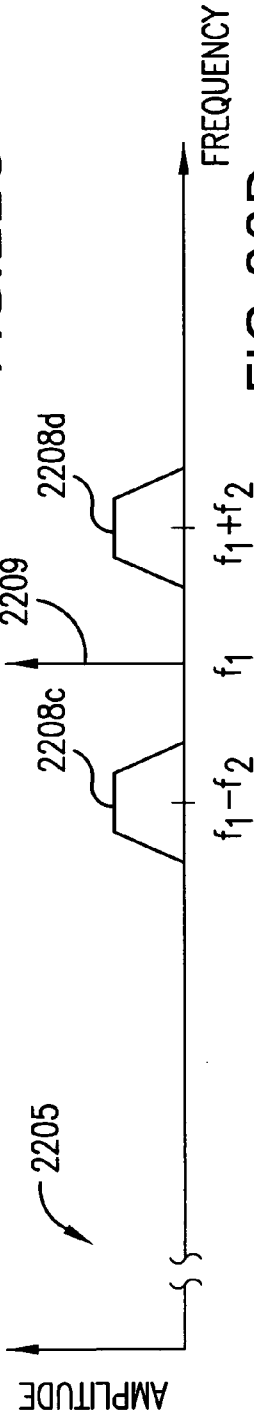


FIG.22D

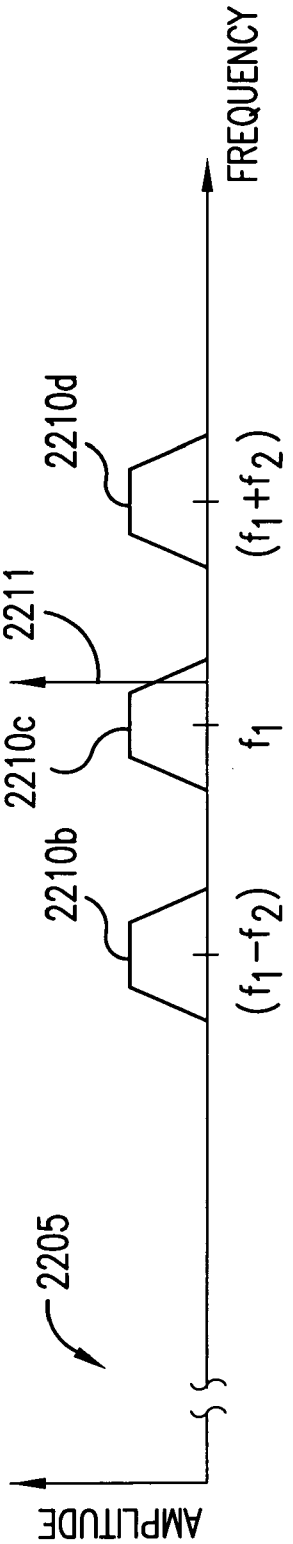


FIG.22E

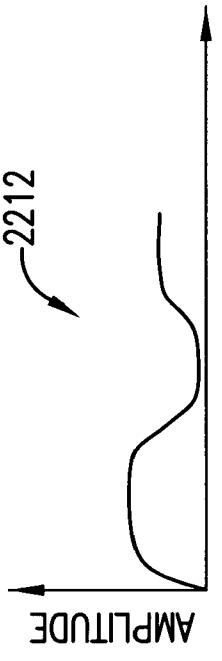


FIG.22F

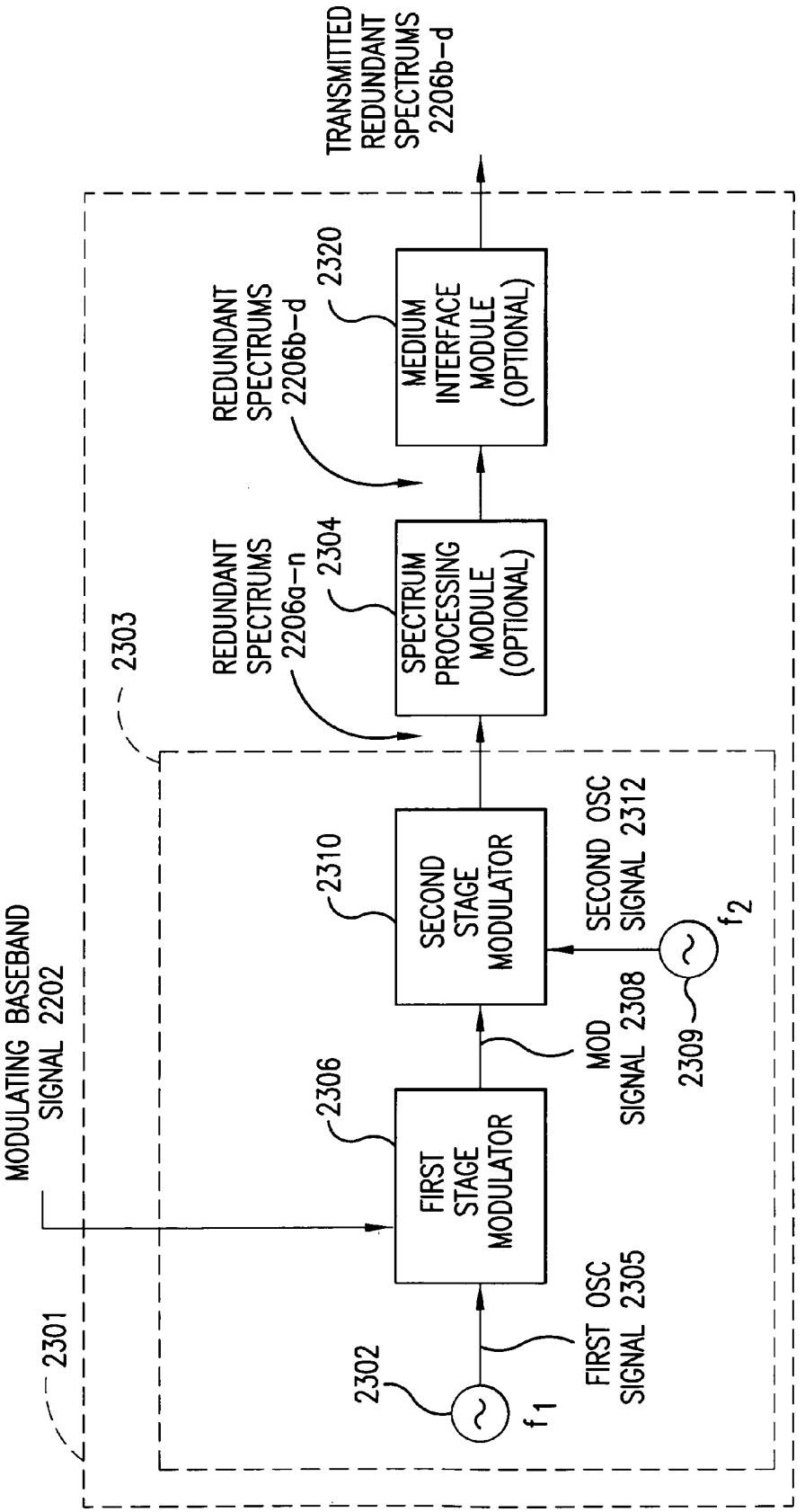

TRANSMITTED REDUNDANT SPECTRUMS 2206b-d
2320
MEDIUM INTERFACE MODULE (OPTIONAL)
REDUNDANT SPECTRUMS 2206b-d
2304
SPECTRUM PROCESSING MODULE (OPTIONAL)
REDUNDANT SPECTRUMS 2206a-n
2303
2310
SECOND STAGE MODULATOR
SECOND OSC SIGNAL 2312
f_2
2309
MOD SIGNAL 2308
2306
FIRST STAGE MODULATOR
MODULATING BASEBAND SIGNAL 2202
2301
2302
f_1
FIRST OSC SIGNAL 2305

FIG.23A

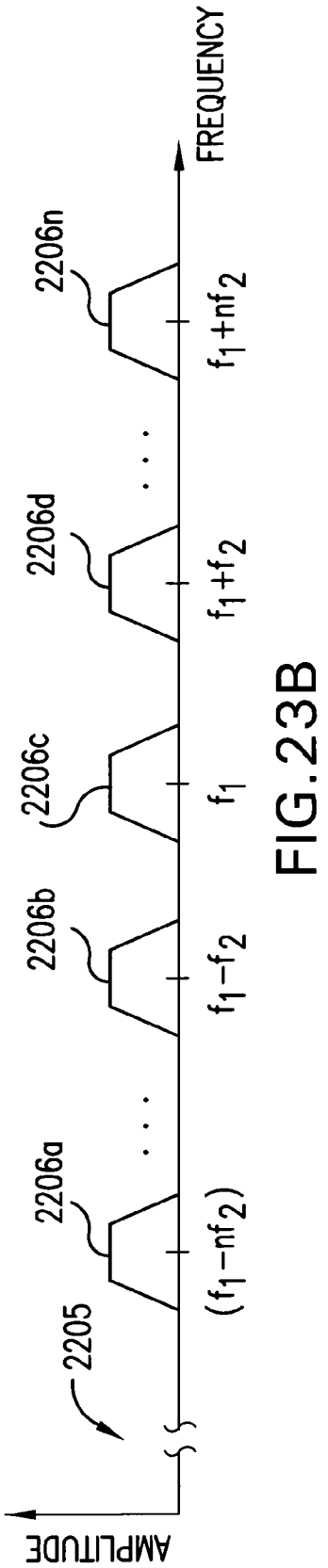


FIG.23B

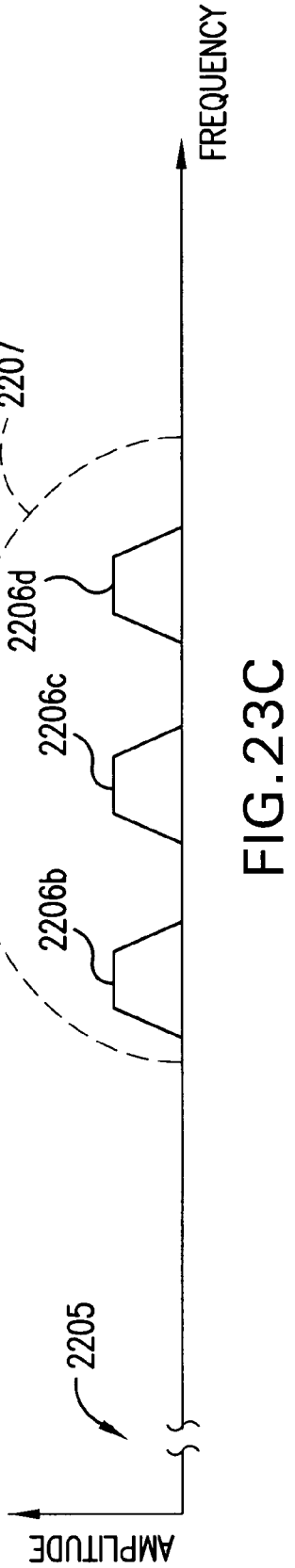


FIG.23C

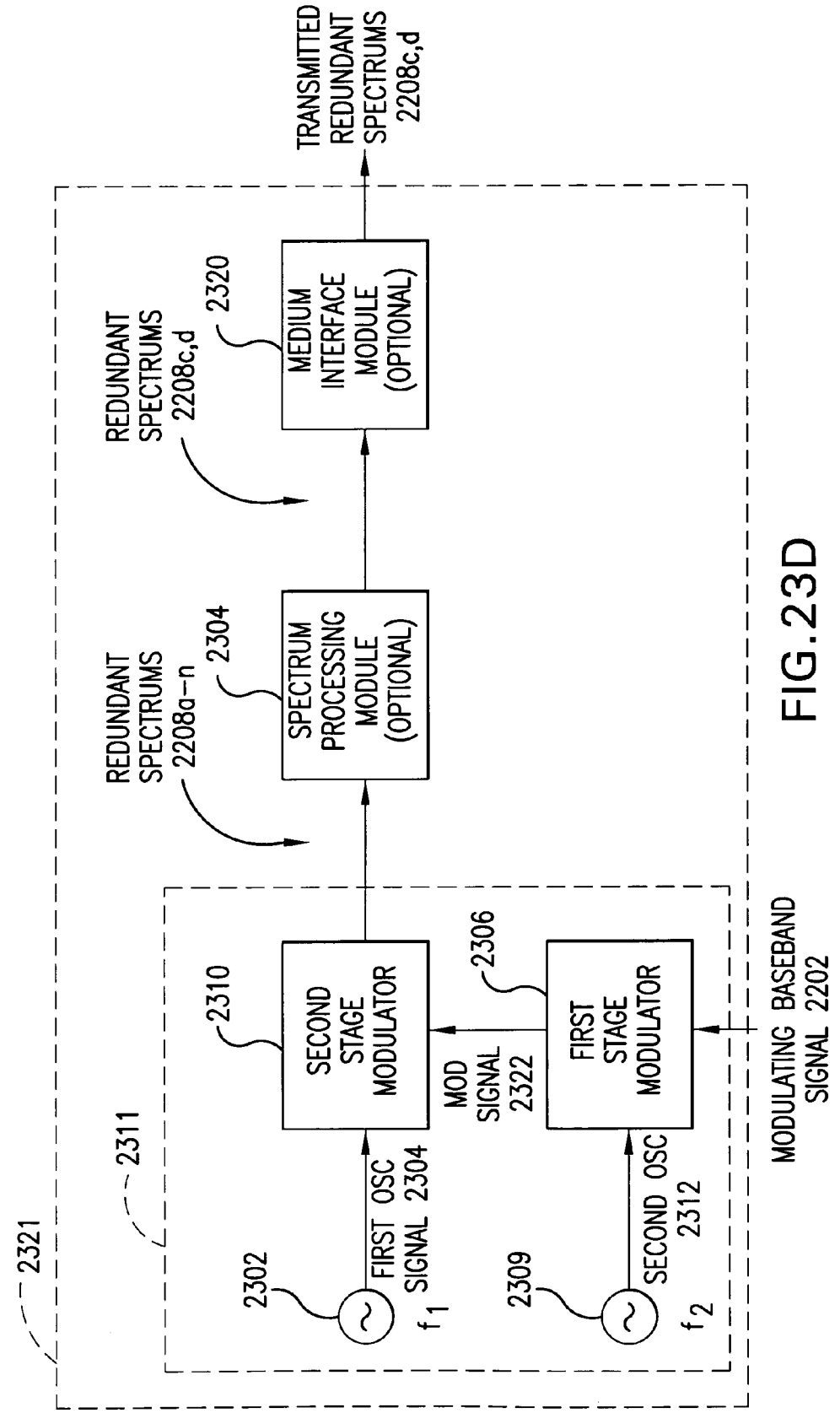

TRANSMITTED REDUNDANT SPECTRUMS 2208c,d
REDUNDANT SPECTRUMS 2208c,d
2320
MEDIUM INTERFACE MODULE (OPTIONAL)
REDUNDANT SPECTRUMS 2208a-n
2304
SPECTRUM PROCESSING MODULE (OPTIONAL)
2310
SECOND STAGE MODULATOR
2306
FIRST STAGE MODULATOR
MOD SIGNAL 2322
MODULATING BASEBAND SIGNAL 2202
2311
2321
2302
FIRST OSC SIGNAL 2304
f_1
2309
SECOND OSC 2312
f_2

FIG.23D

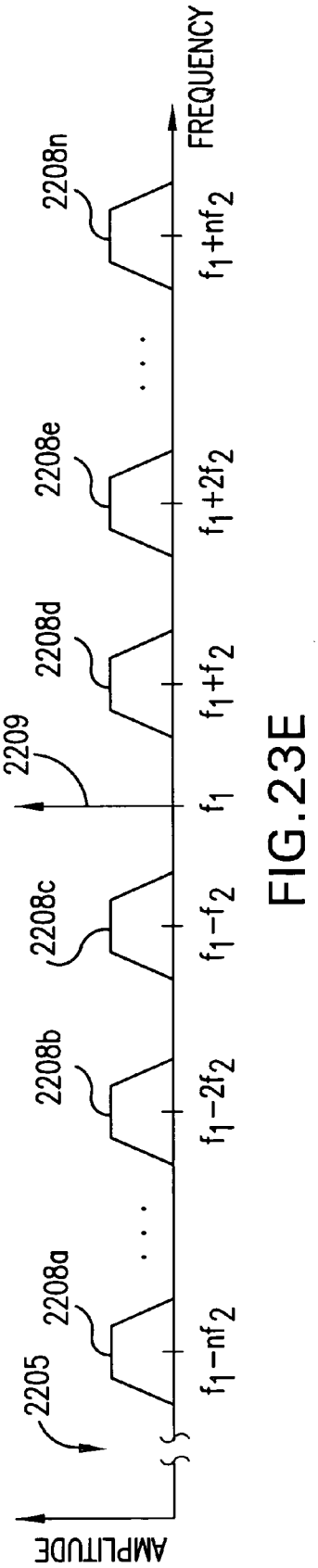


FIG.23E

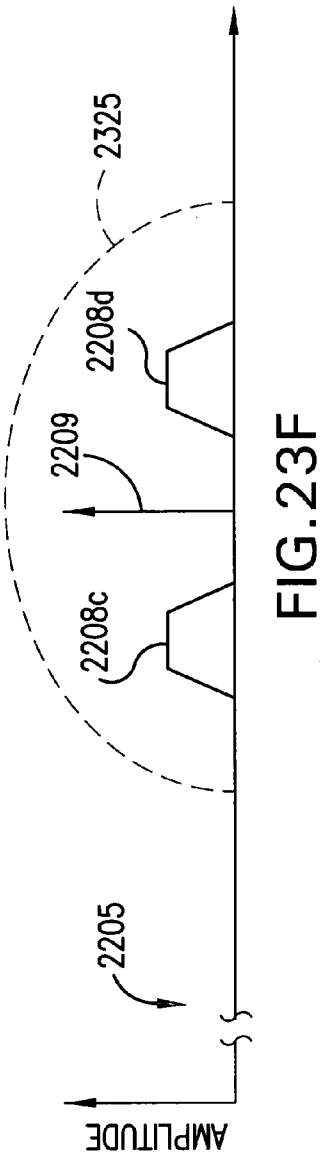


FIG.23F

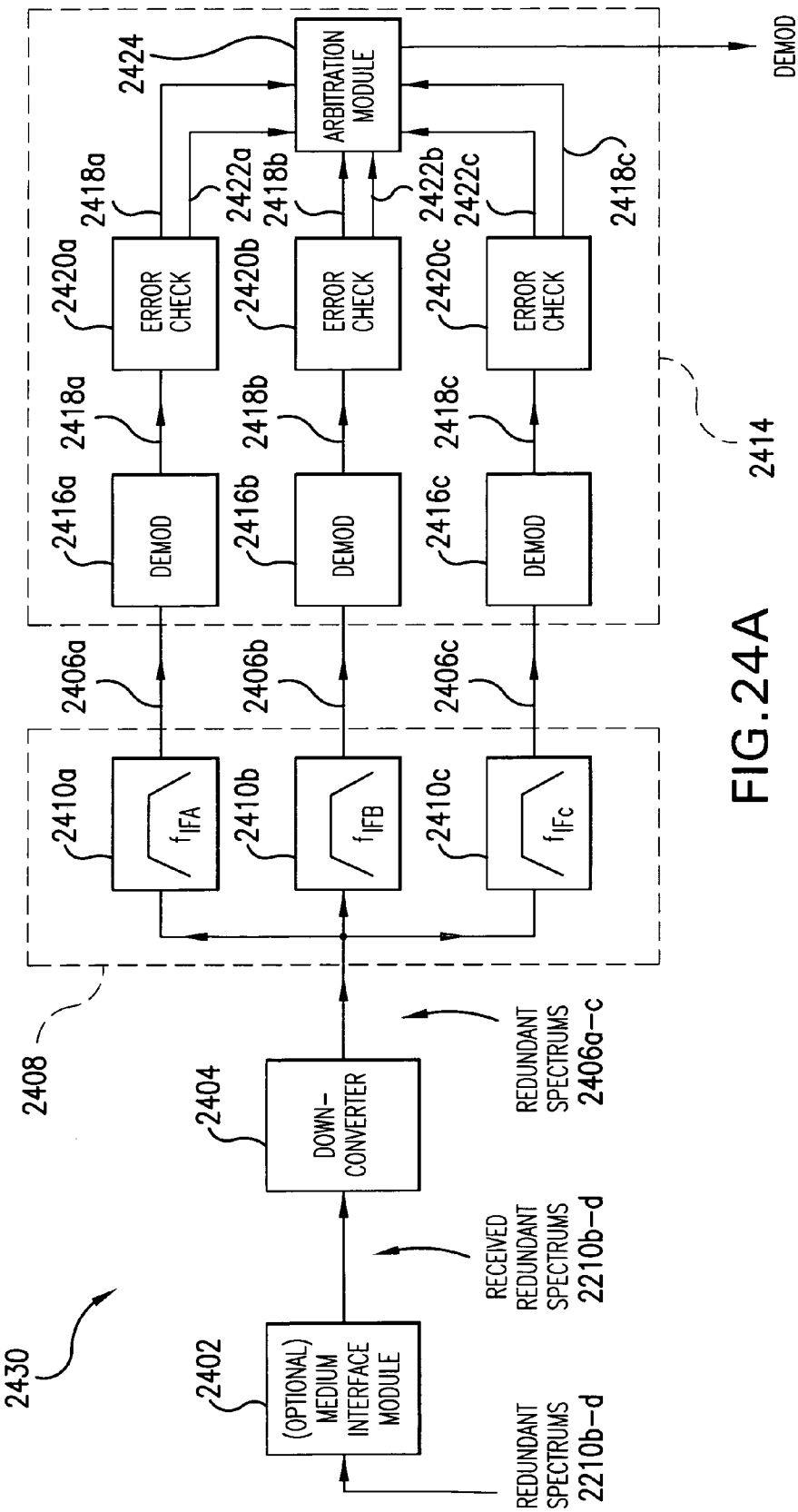

2430
2402
(OPTIONAL) MEDIUM INTERFACE MODULE
REDUNDANT SPECTRUMS 2210b–d
RECEIVED REDUNDANT SPECTRUMS 2210b–d
2404
DOWN-CONVERTER
REDUNDANT SPECTRUMS 2406a–c
2408
2410a
f_{IFA}
2410b
f_{IFB}
2410c
f_{IFc}
2406a
2406b
2406c
2414
2416a
DEMOD
2416b
DEMOD
2416c
DEMOD
2418a
2418b
2418c
2420a
ERROR CHECK
2420b
ERROR CHECK
2420c
ERROR CHECK
2422a
2422b
2422c
2424
ARBITRATION MODULE
DEMOD BASEBAND SIGNAL 2212

FIG.24A

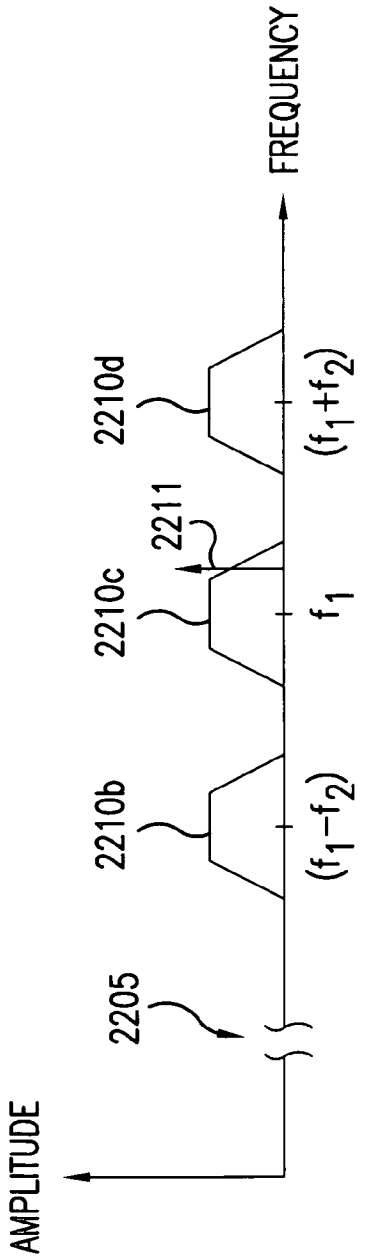


FIG.24B

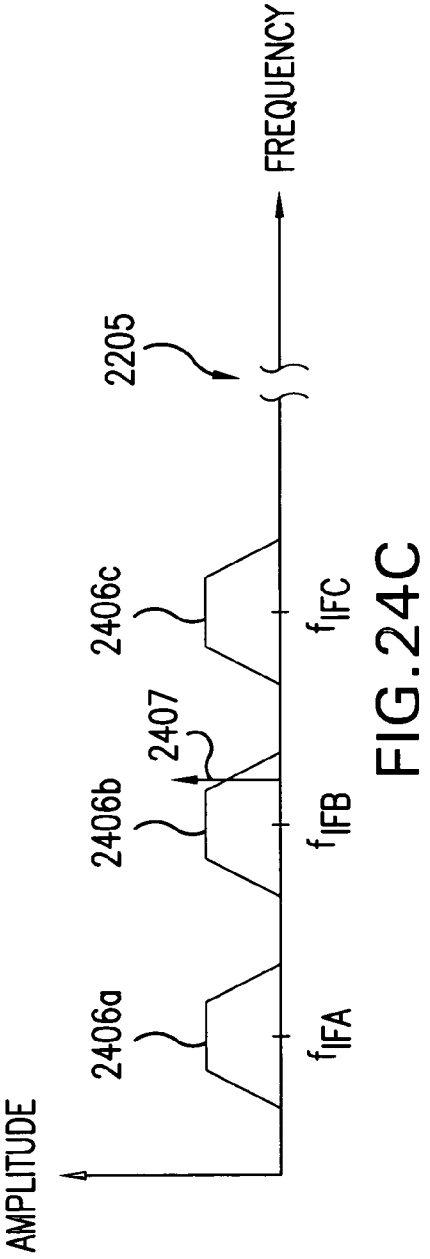


FIG.24C

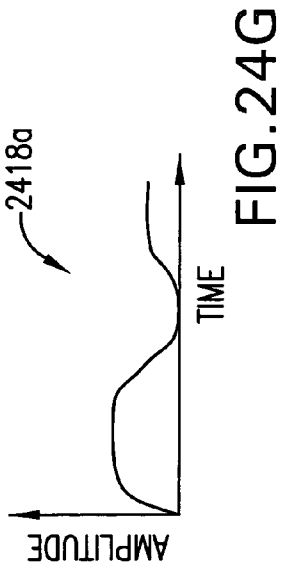


FIG.24G

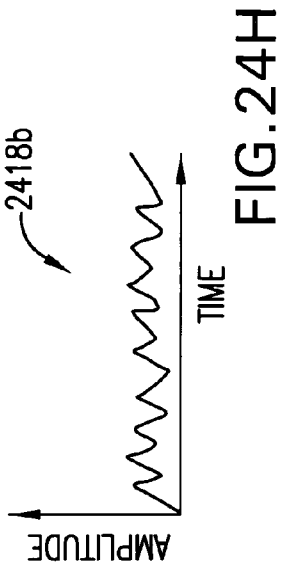


FIG.24H

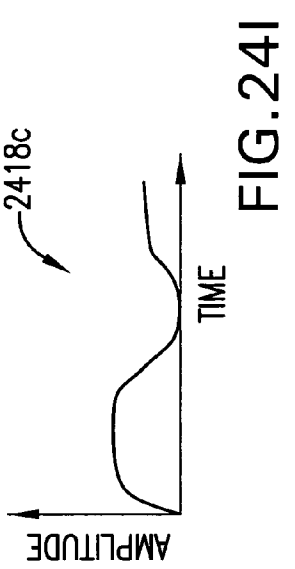


FIG.24I

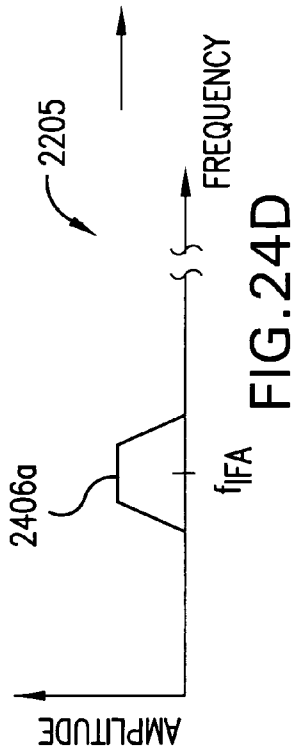


FIG.24D

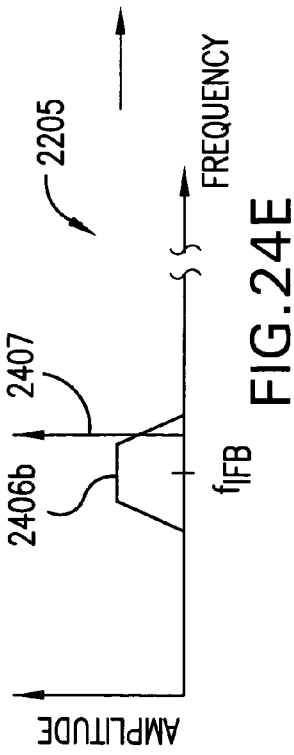


FIG.24E

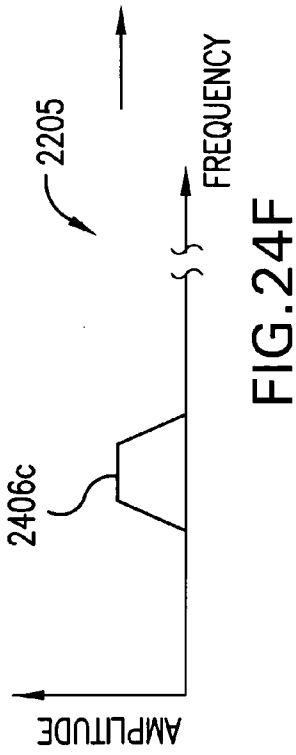


FIG.24F

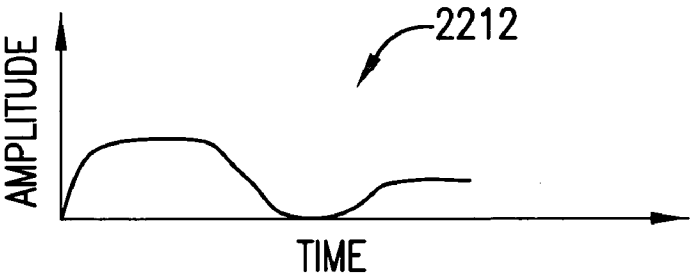


FIG. 24J

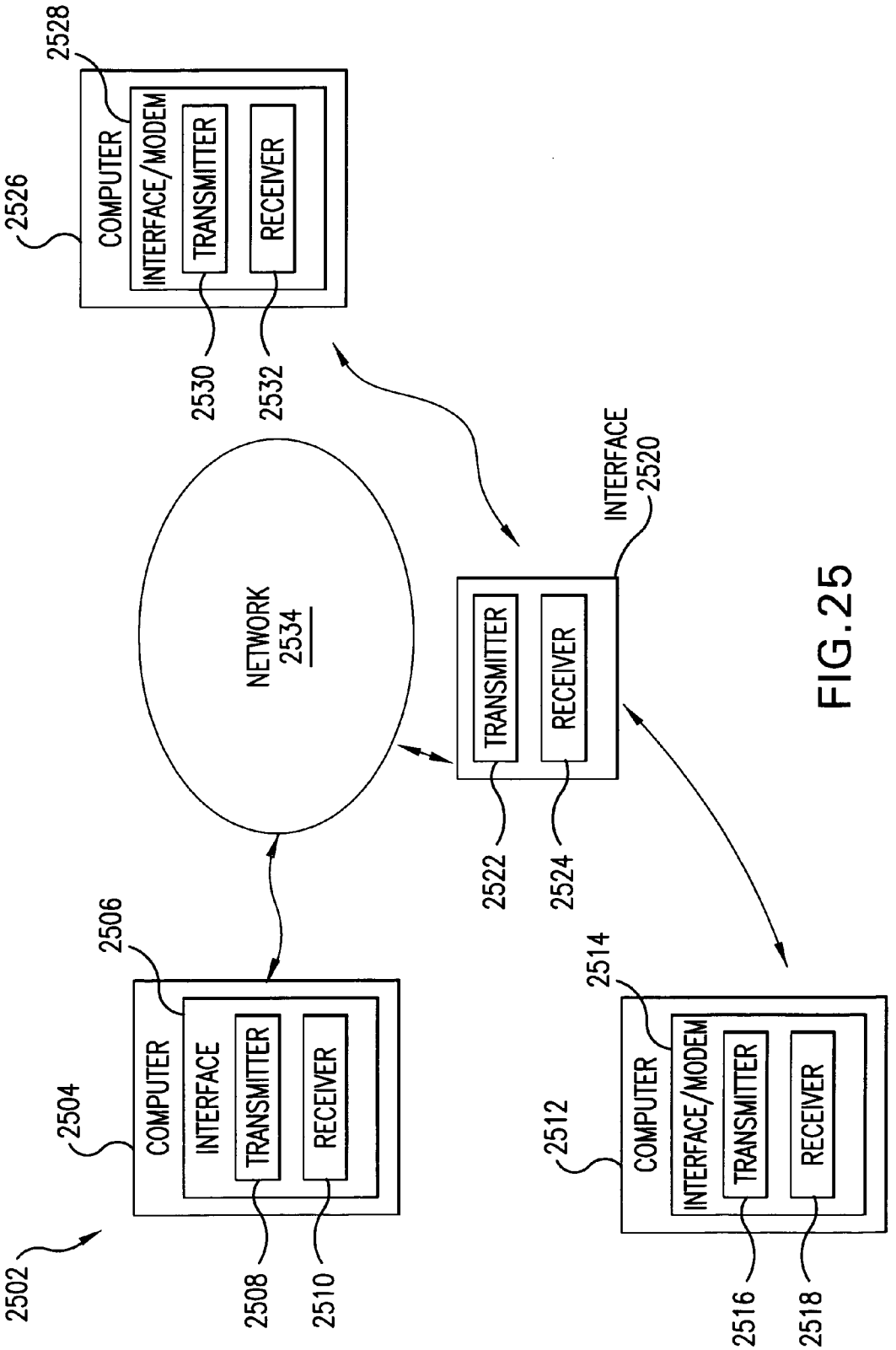

2528
COMPUTER
INTERFACE/MODEM
TRANSMITTER
RECEIVER
2526
2530
2532
NETWORK
2534
INTERFACE
2520
TRANSMITTER
RECEIVER
2522
2524
2506
2504
COMPUTER
INTERFACE
TRANSMITTER
RECEIVER
2502
2508
2510
2514
2512
COMPUTER
INTERFACE/MODEM
TRANSMITTER
RECEIVER
2516
2518

FIG.25

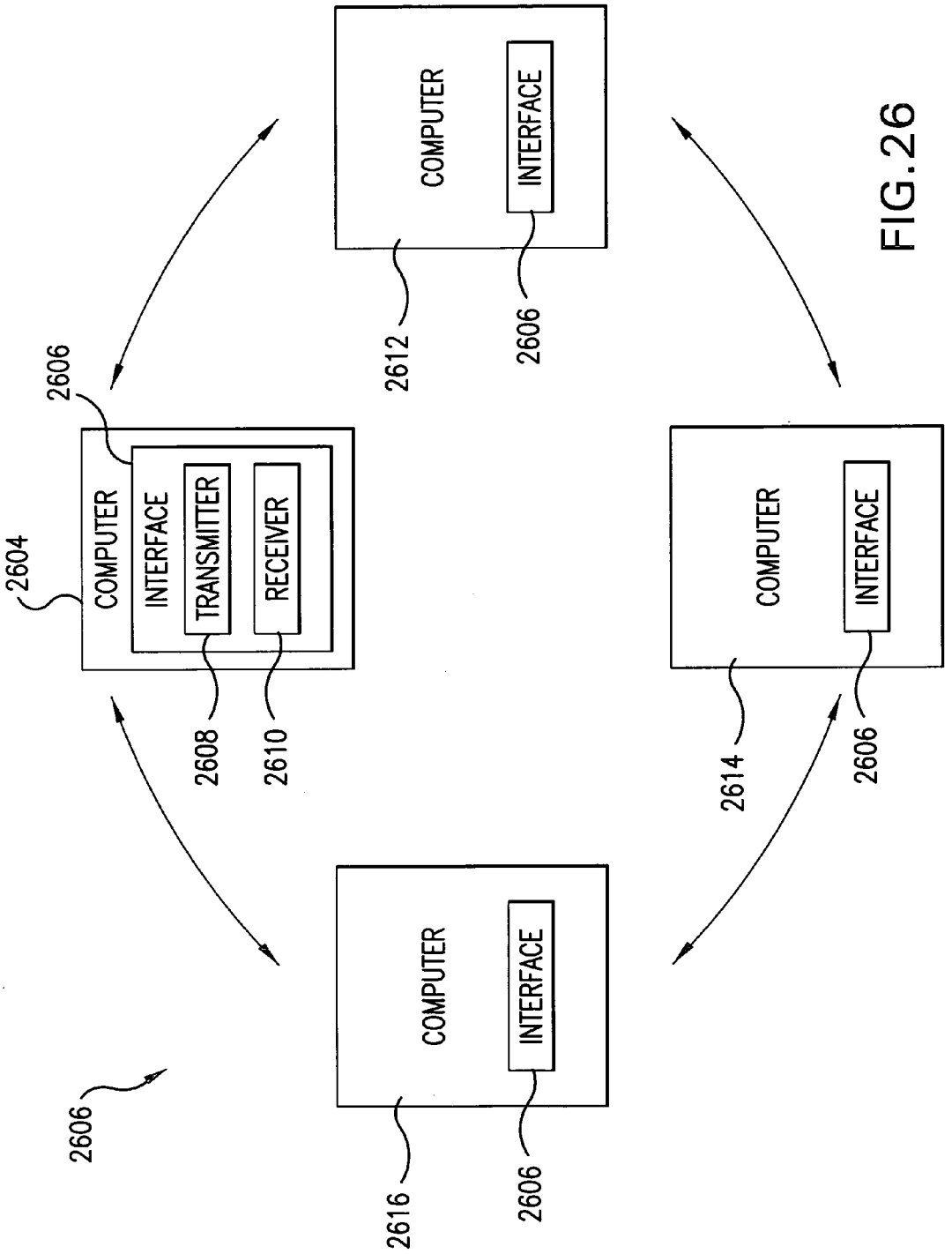

COMPUTER
INTERFACE
2612
2606
2606
2604
COMPUTER
INTERFACE
TRANSMITTER
RECEIVER
2608
2610
COMPUTER
INTERFACE
2614
2606
2606
COMPUTER
INTERFACE
2616
2606

FIG. 26

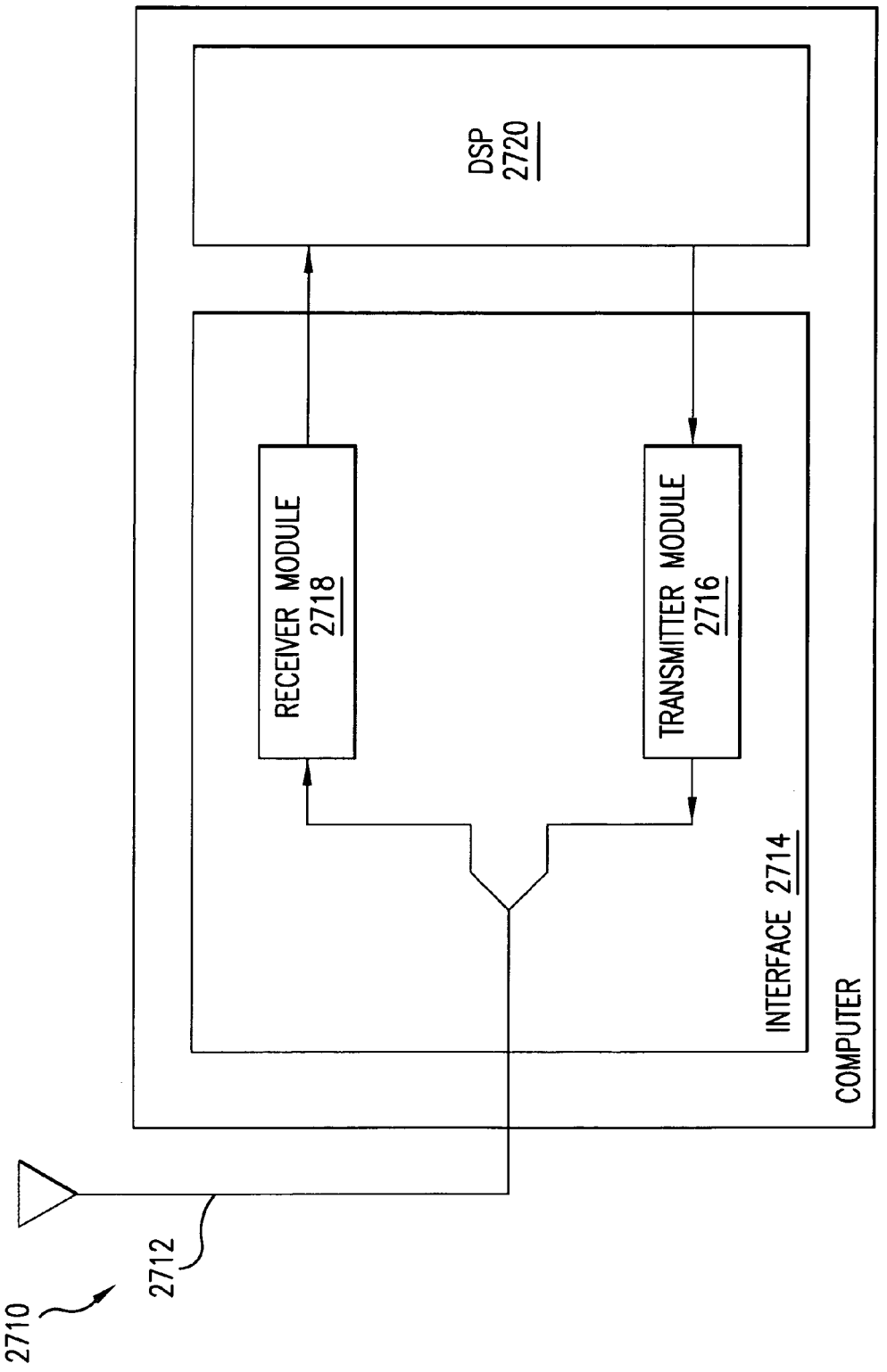

DSP
2720
RECEIVER MODULE
2718
TRANSMITTER MODULE
2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.27

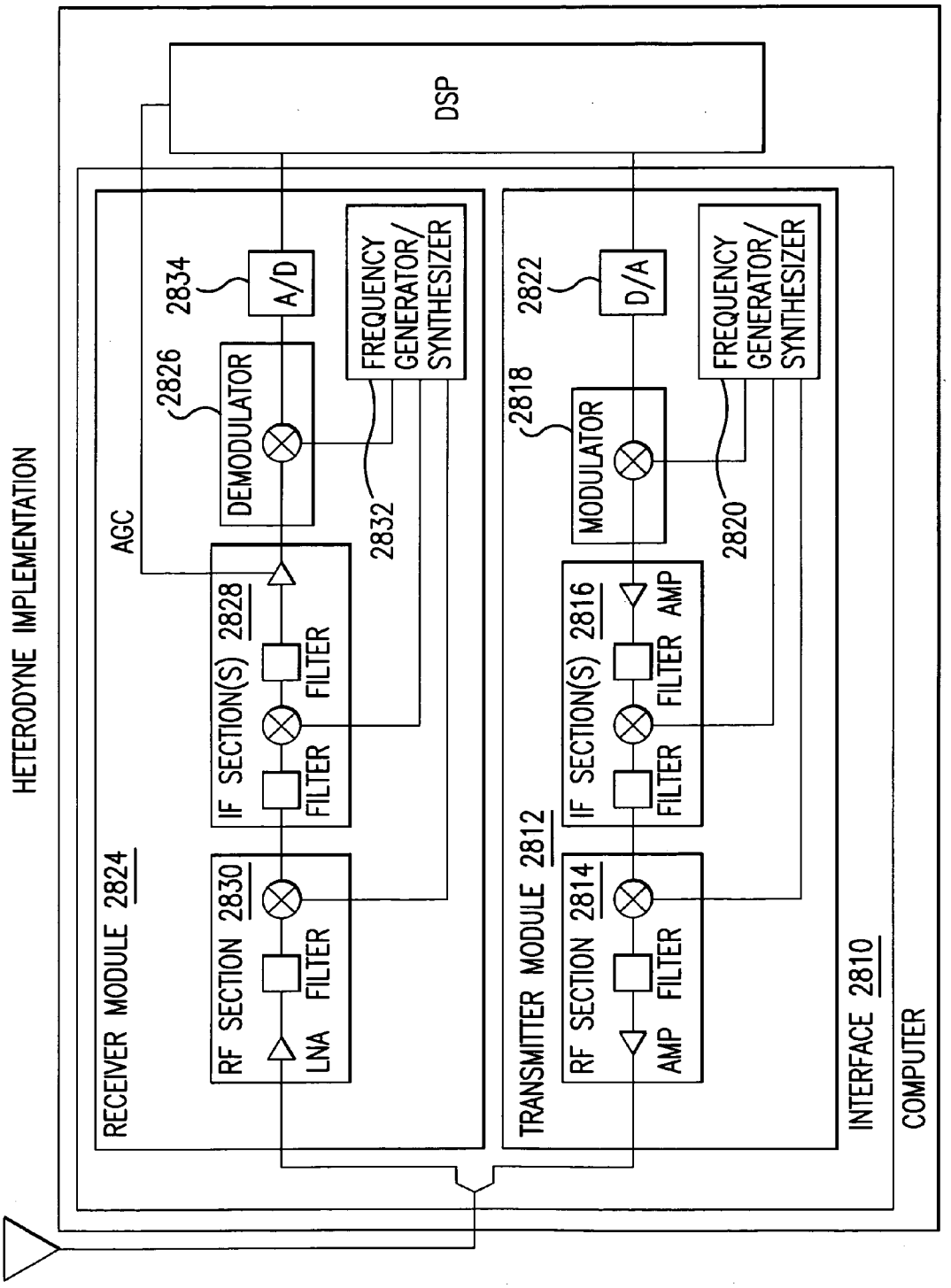

HETERODYNE IMPLEMENTATION
COMPUTER
INTERFACE 2810
DSP
RECEIVER MODULE 2824
AGC
RF SECTION 2830
LNA
FILTER
IF SECTION(S) 2828
FILTER
FILTER
DEMODULATOR
2826
2834
A/D
FREQUENCY GENERATOR/ SYNTHESIZER
2832
TRANSMITTER MODULE 2812
RF SECTION 2814
AMP
FILTER
IF SECTION(S) 2816
FILTER
FILTER
AMP
MODULATOR
2818
2822
D/A
FREQUENCY GENERATOR/ SYNTHESIZER
2820

FIG.28

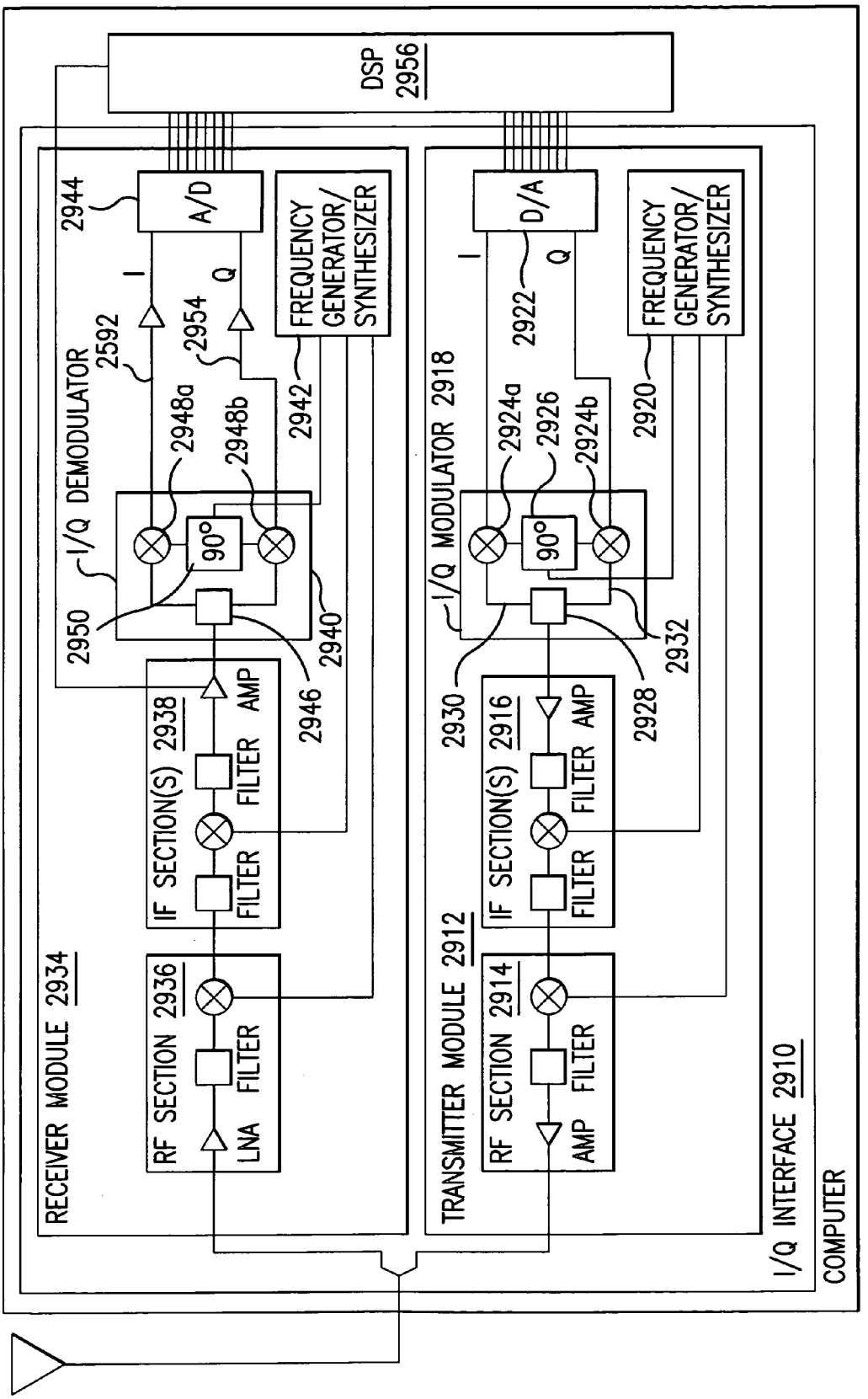

DSP 2956
RECEIVER MODULE 2934
TRANSMITTER MODULE 2912
I/Q INTERFACE 2910
COMPUTER
I/Q DEMODULATOR 2592
I/Q MODULATOR 2918
A/D 2944
D/A
FREQUENCY GENERATOR/ SYNTHESIZER 2942
FREQUENCY GENERATOR/ SYNTHESIZER 2920
I
Q
2954
2922
2948a
2948b
2924a
2926
2924b
90°
2950
2940
2946
2930
2932
2928
IF SECTION(S) 2938
IF SECTION(S) 2916
FILTER
AMP
RF SECTION 2936
RF SECTION 2914
LNA
AMP

FIG.29

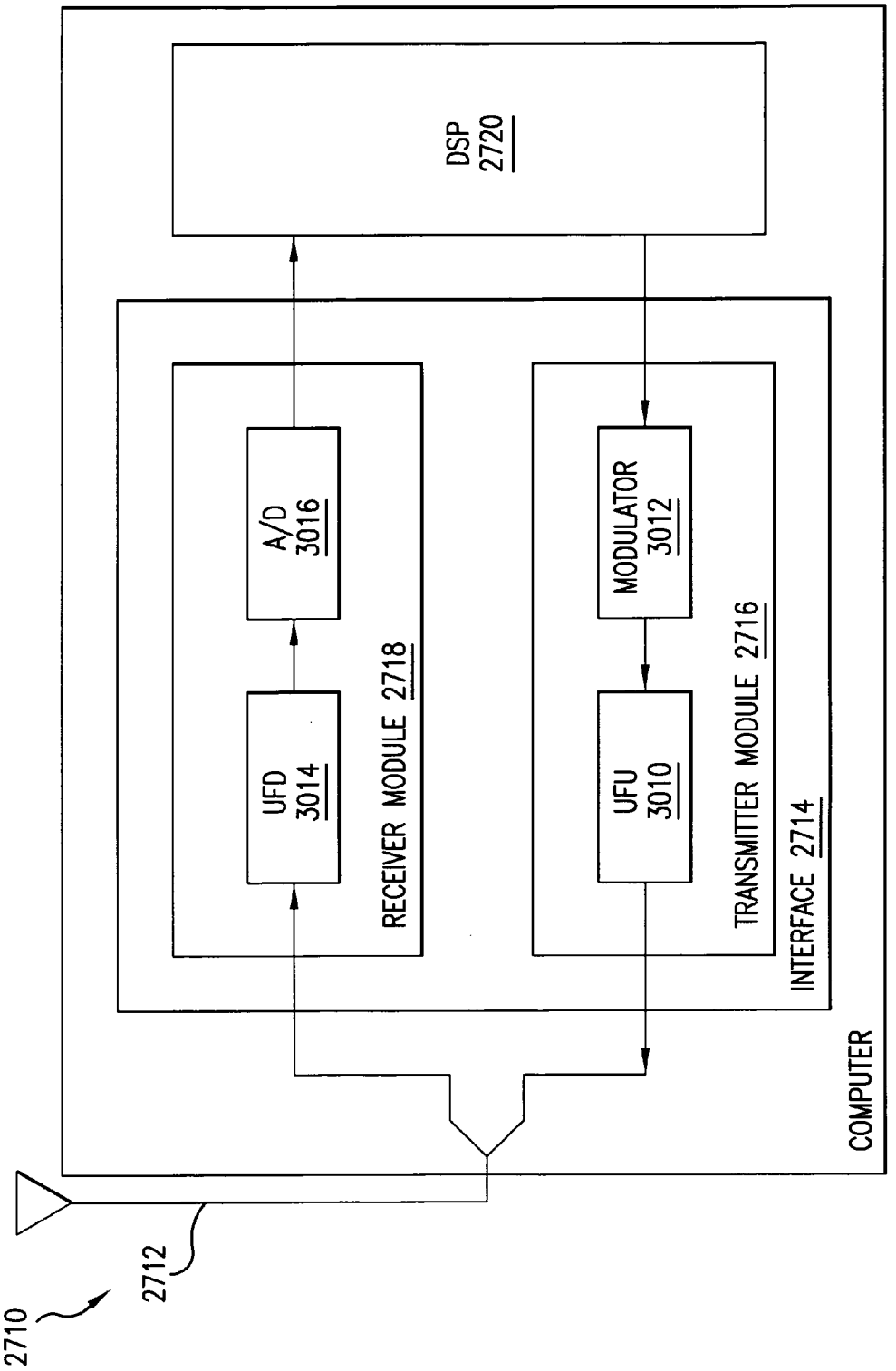

DSP
2720
A/D
3016
UFD
3014
RECEIVER MODULE 2718
MODULATOR
3012
UFU
3010
TRANSMITTER MODULE 2716
INTERFACE 2714
COMPUTER
2712
2710

FIG.30

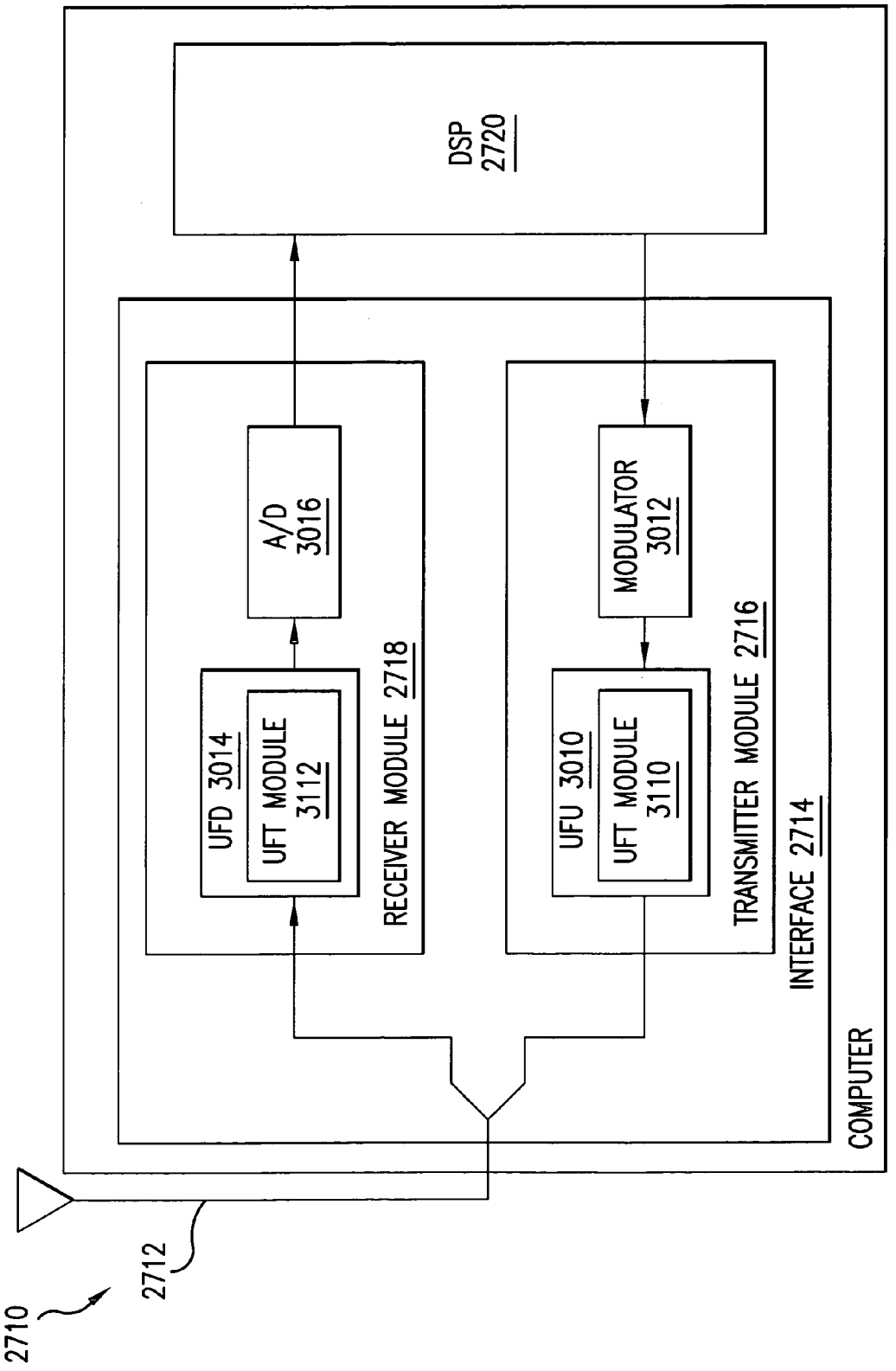
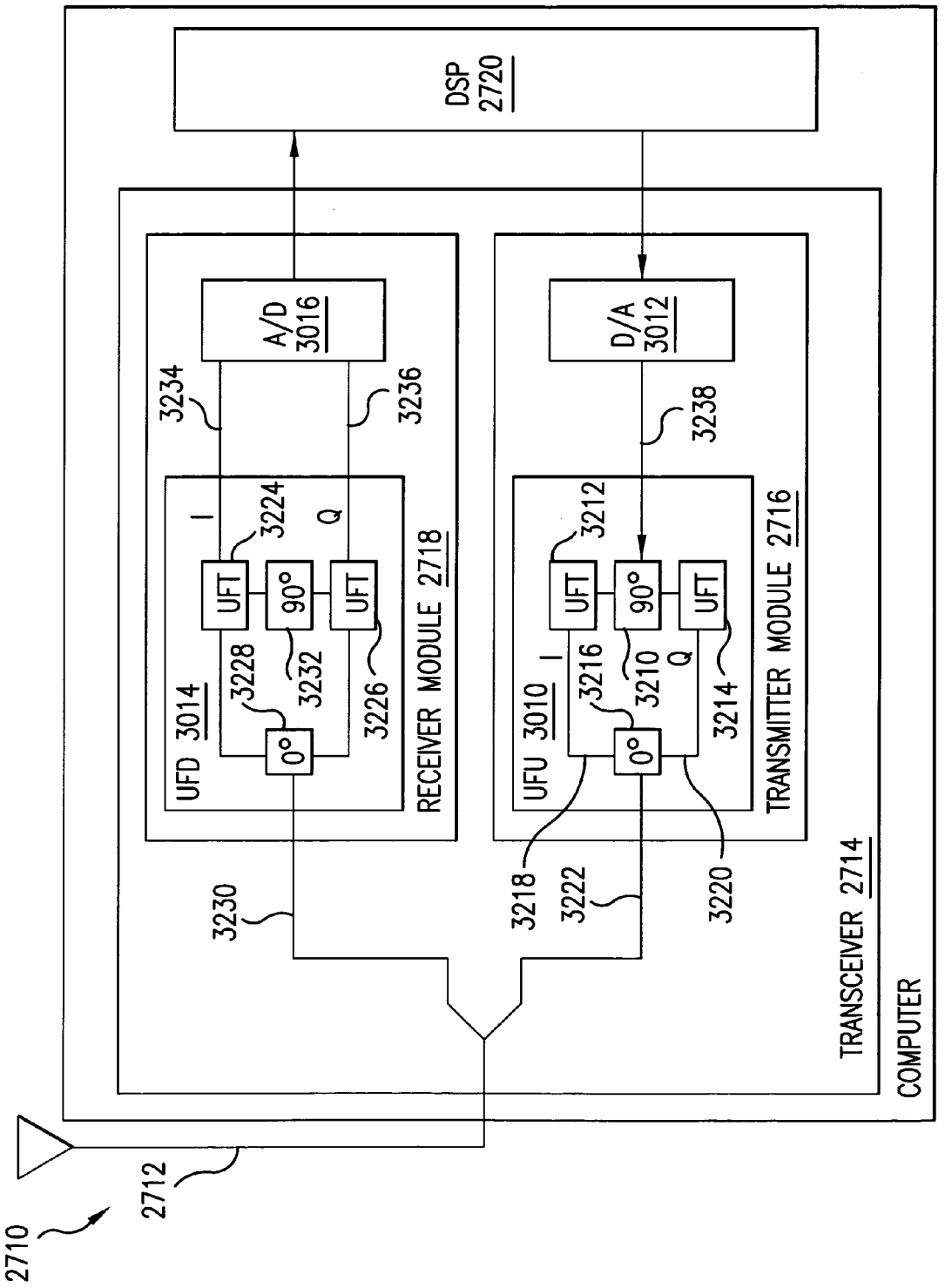

2710
2712
COMPUTER
INTERFACE 2714
DSP 2720
RECEIVER MODULE 2718
UFD 3014
UFT MODULE 3112
A/D 3016
TRANSMITTER MODULE 2716
UFU 3010
UFT MODULE 3110
MODULATOR 3012

FIG.31

FIG.32


DSP 2720
A/D 3016
D/A 3012
3234
3236
3238
I
Q
UFT
90°
0°
3224
3228
3232
3226
UFD 3014
RECEIVER MODULE 2718
3212
3216
3210
3214
UFU 3010
TRANSMITTER MODULE 2716
3230
3218
3222
3220
TRANSCEIVER 2714
COMPUTER
2712
2710

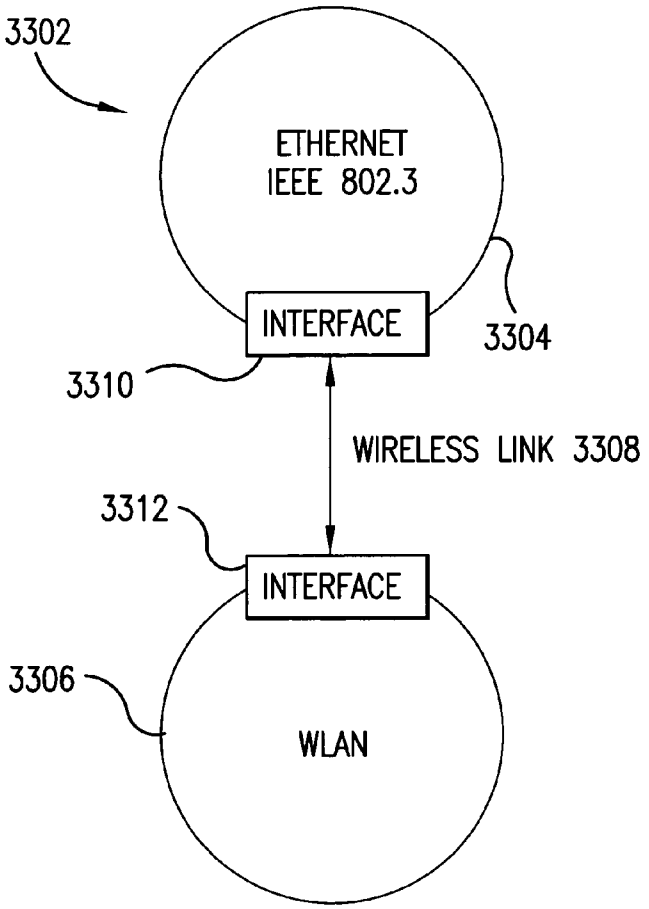

3302
ETHERNET
IEEE 802.3
INTERFACE
3304
3310
WIRELESS LINK 3308
3312
INTERFACE
3306
WLAN

FIG.33

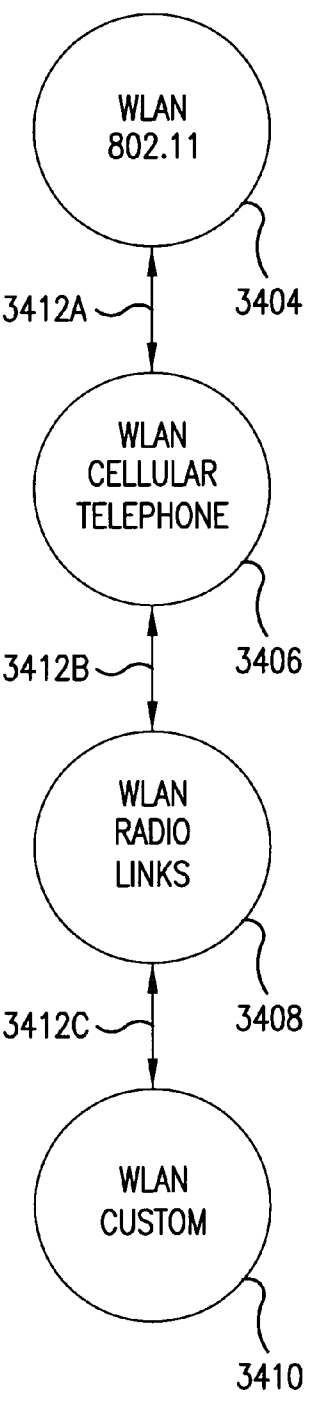

3402
WLAN
802.11
3412A
3404
WLAN
CELLULAR
TELEPHONE
3412B
3406
WLAN
RADIO
LINKS
3412C
3408
WLAN
CUSTOM
3410

FIG.34

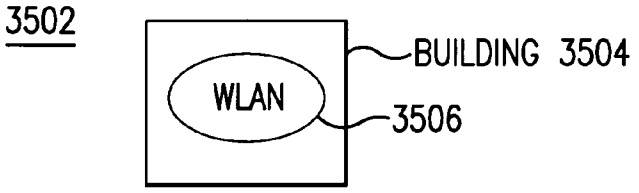


FIG.35

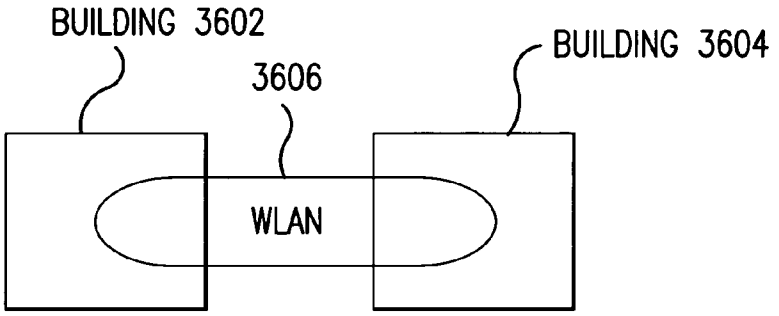


FIG.36

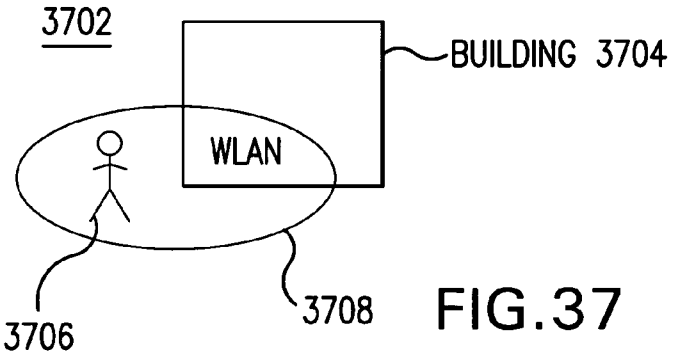


FIG.37

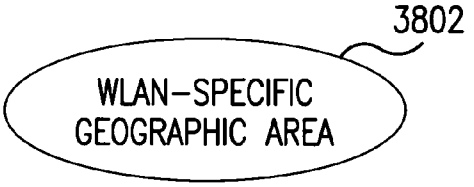


FIG.38

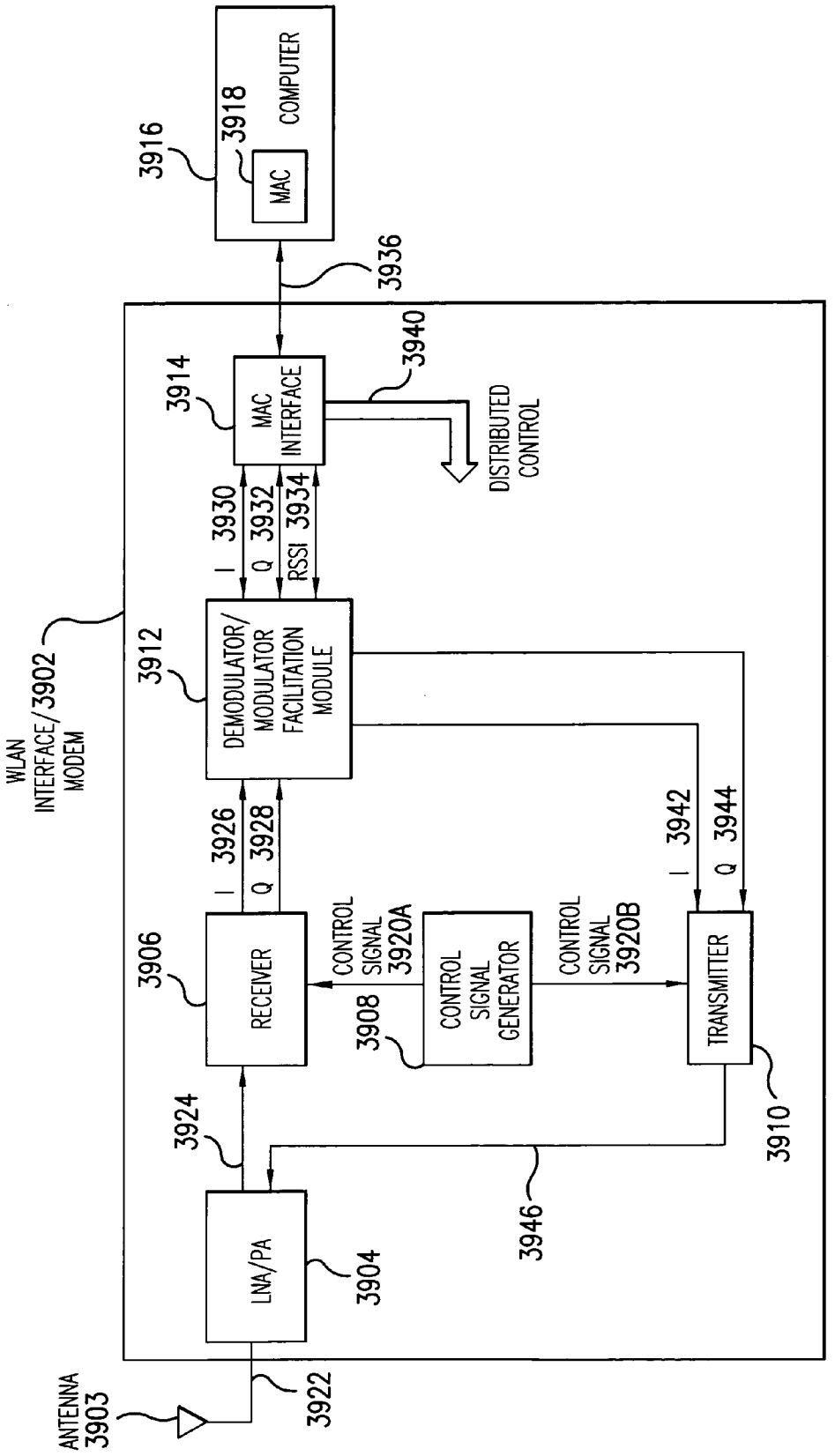

3916
3918
COMPUTER
MAC
3936
3940
3914
MAC INTERFACE
DISTRIBUTED CONTROL
3930
I
3932
Q
3934
RSSI
WLAN INTERFACE/MODEM 3902
3912
DEMODULATOR/ MODULATOR FACILITATION MODULE
3926
I
3928
Q
3942
I
3944
Q
3906
RECEIVER
CONTROL SIGNAL 3920A
3908
CONTROL SIGNAL GENERATOR
CONTROL SIGNAL 3920B
TRANSMITTER
3924
3910
3946
LNA/PA
3904
ANTENNA 3903
3922

FIG.39

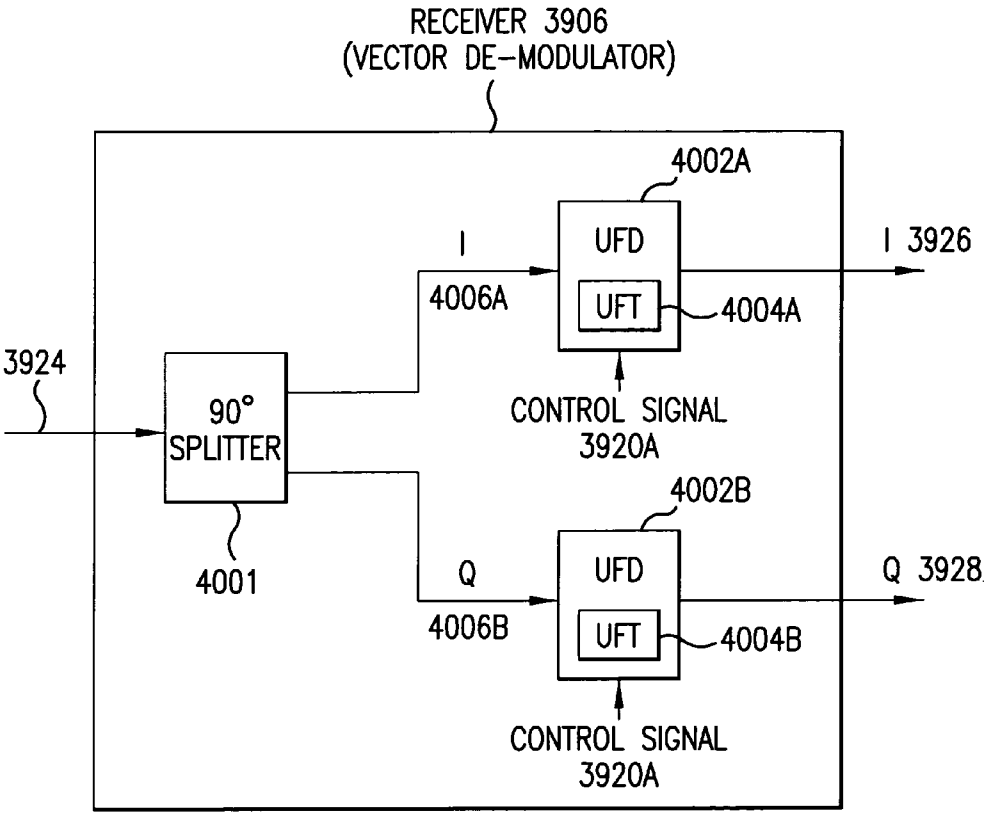

RECEIVER 3906
(VECTOR DE-MODULATOR)
4002A
UFD
UFT
4004A
I
4006A
I 3926
3924
90°
SPLITTER
4001
CONTROL SIGNAL
3920A
4002B
UFD
UFT
4004B
Q
4006B
Q 3928
CONTROL SIGNAL
3920A

FIG.40

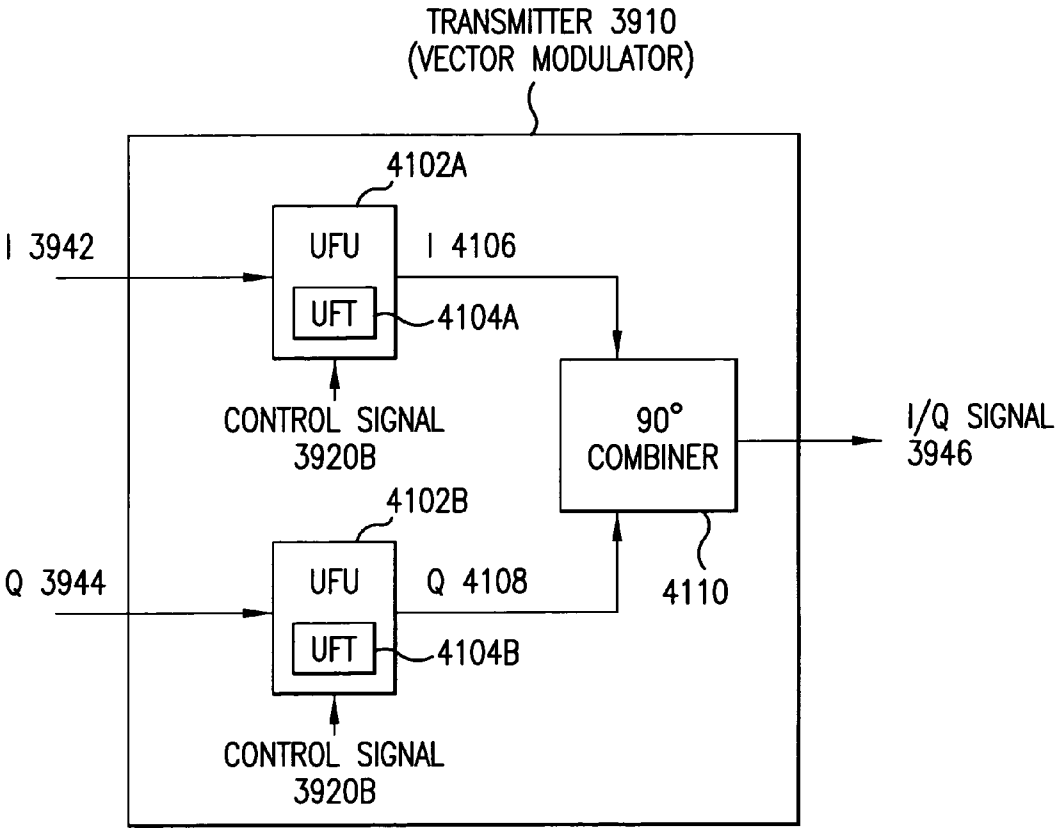

TRANSMITTER 3910
(VECTOR MODULATOR)
4102A
I 3942
UFU
I 4106
UFT
4104A
CONTROL SIGNAL
3920B
90°
COMBINER
I/Q SIGNAL
3946
4102B
Q 3944
UFU
Q 4108
4110
UFT
4104B
CONTROL SIGNAL
3920B

FIG.41

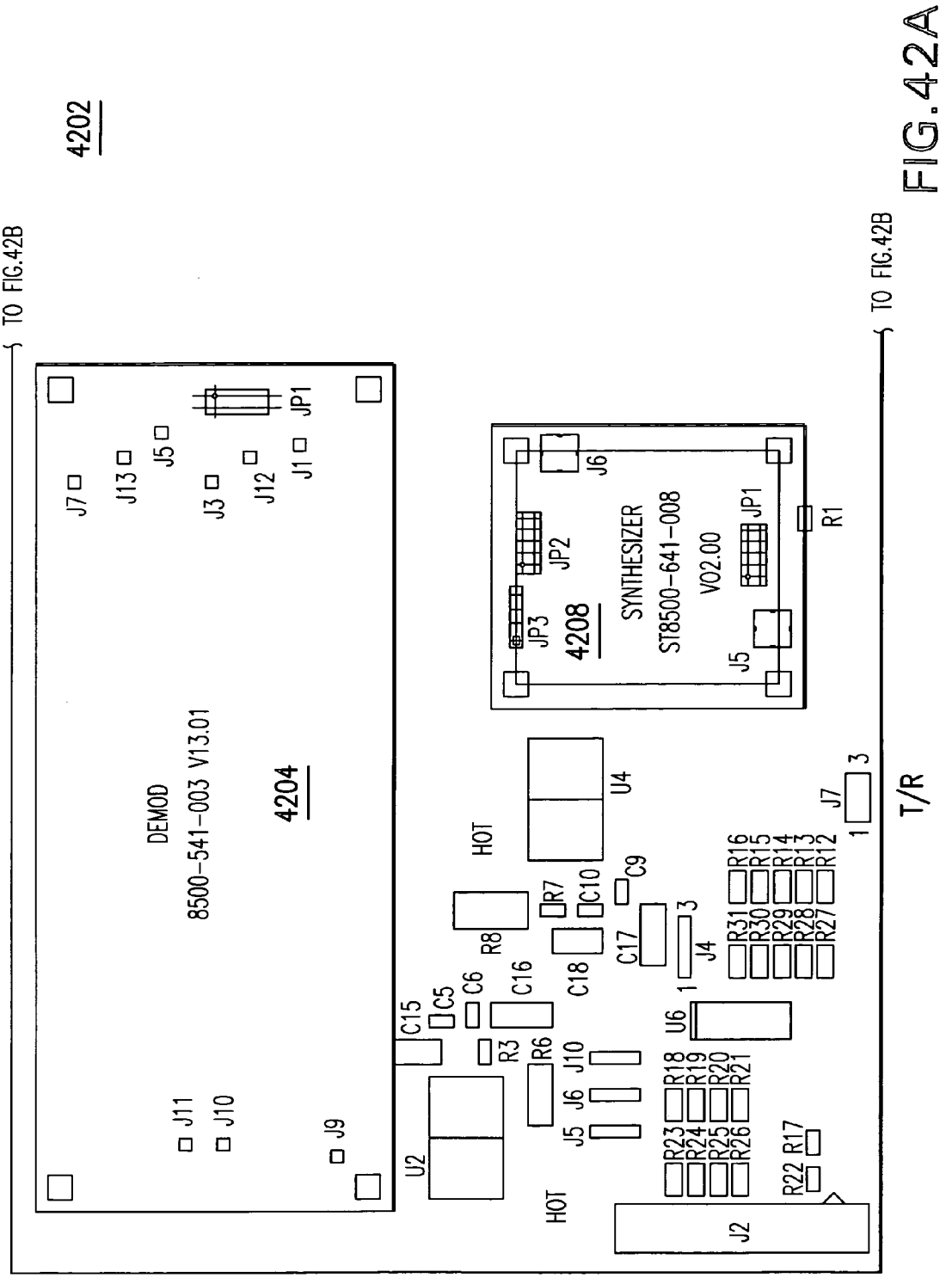

4202
TO FIG.42B
TO FIG.42B
DEMOD
8500-541-003 V13.01
4204
4208
SYNTHESIZER
ST8500-641-008
V02.00
HOT
HOT
T/R
J1
J2
J3
J4
J5
J6
J7
J9
J10
J11
J12
J13
JP1
JP2
JP3
U2
U4
U6
R1
R3
R6
R7
R8
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
C5
C6
C9
C10
C15
C16
C17
C18

FIG.42A

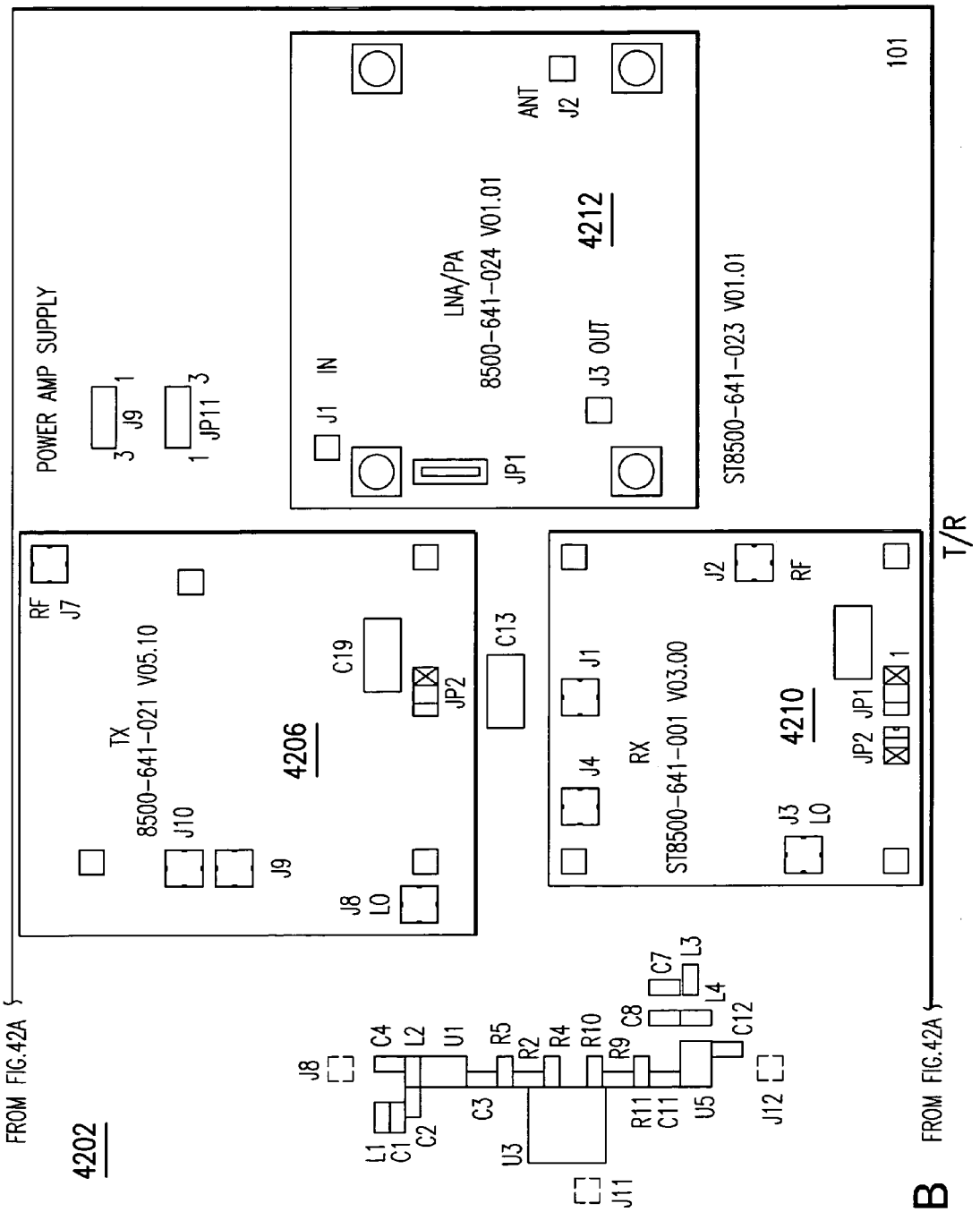

FROM FIG.42A
4202
POWER AMP SUPPLY
J9
JP11
J1 IN
LNA/PA
8500-641-024 V01.01
JP1
J3 OUT
4212
ANT
J2
ST8500-641-023 V01.01
101
RF
J7
TX
8500-641-021 V05.10
J10
J9
J8
LO
4206
C19
JP2
C13
J4
J1
RX
ST8500-641-001 V03.00
J3
LO
4210
JP2
JP1
J2
RF
T/R
FROM FIG.42A
J8
C4
L2
U1
R5
R2
R4
R10
R9
C8
C7
L3
L4
C12
C3
R11
C11
U5
J12
L1
C1
C2
U3
J11

FIG.42B

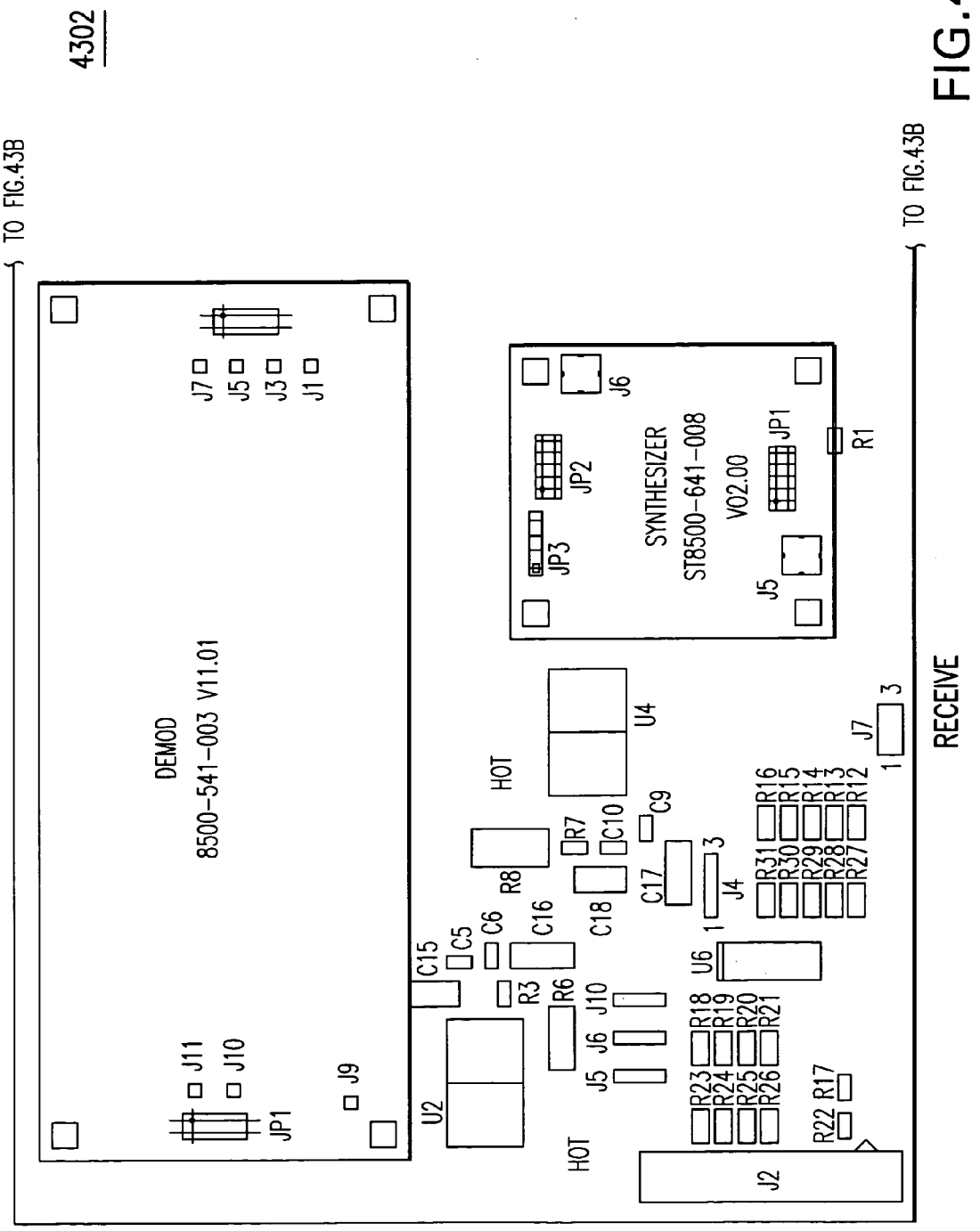

4302
TO FIG.43B
TO FIG.43B
DEMOD
8500-541-003 V11.01
SYNTHESIZER
ST8500-641-008
V02.00
RECEIVE
HOT
HOT
J1
J3
J5
J7
J9
J10
J11
JP1
J2
J4
J5
J6
J7
JP1
JP2
JP3
R1
U2
U4
U6
C5
C6
C9
C10
C15
C16
C17
C18
R3
R6
R7
R8
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31

FIG.43A

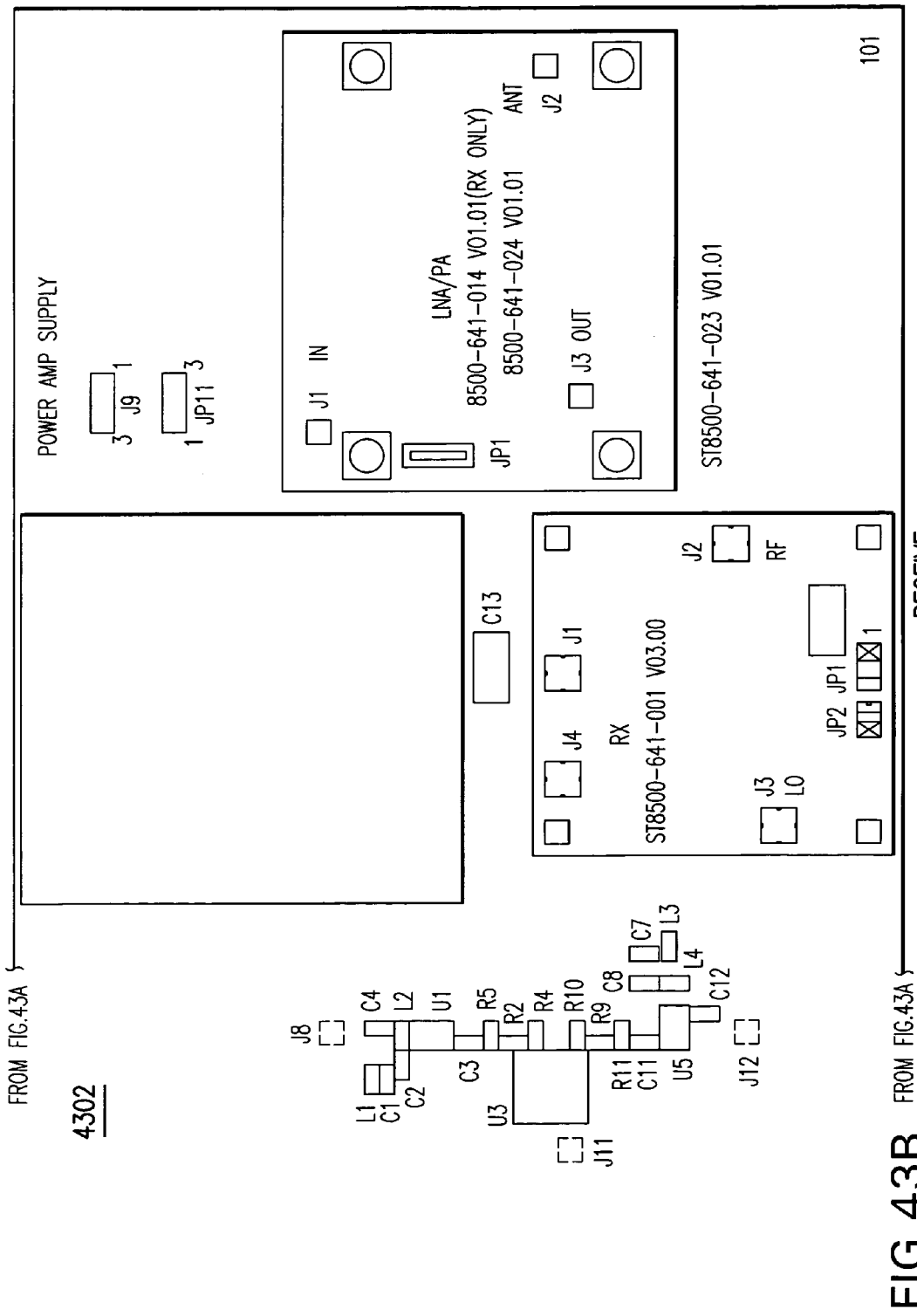

POWER AMP SUPPLY
J9
JP11
J1 IN
LNA/PA
8500-641-014 V01.01(RX ONLY)
8500-641-024 V01.01
JP1
J3 OUT
ANT
J2
ST8500-641-023 V01.01
101
C13
J1
J4
RX
ST8500-641-001 V03.00
J2
RF
JP1
JP2
J3
LO
RECEIVE
FROM FIG.43A
FROM FIG.43A
4302
J8
C4
L2
U1
R5
R2
R4
R10
R9
C8
C7
L3
L4
C12
C3
R11
C11
U5
J12
L1
C1
C2
U3
J11

FIG.43B

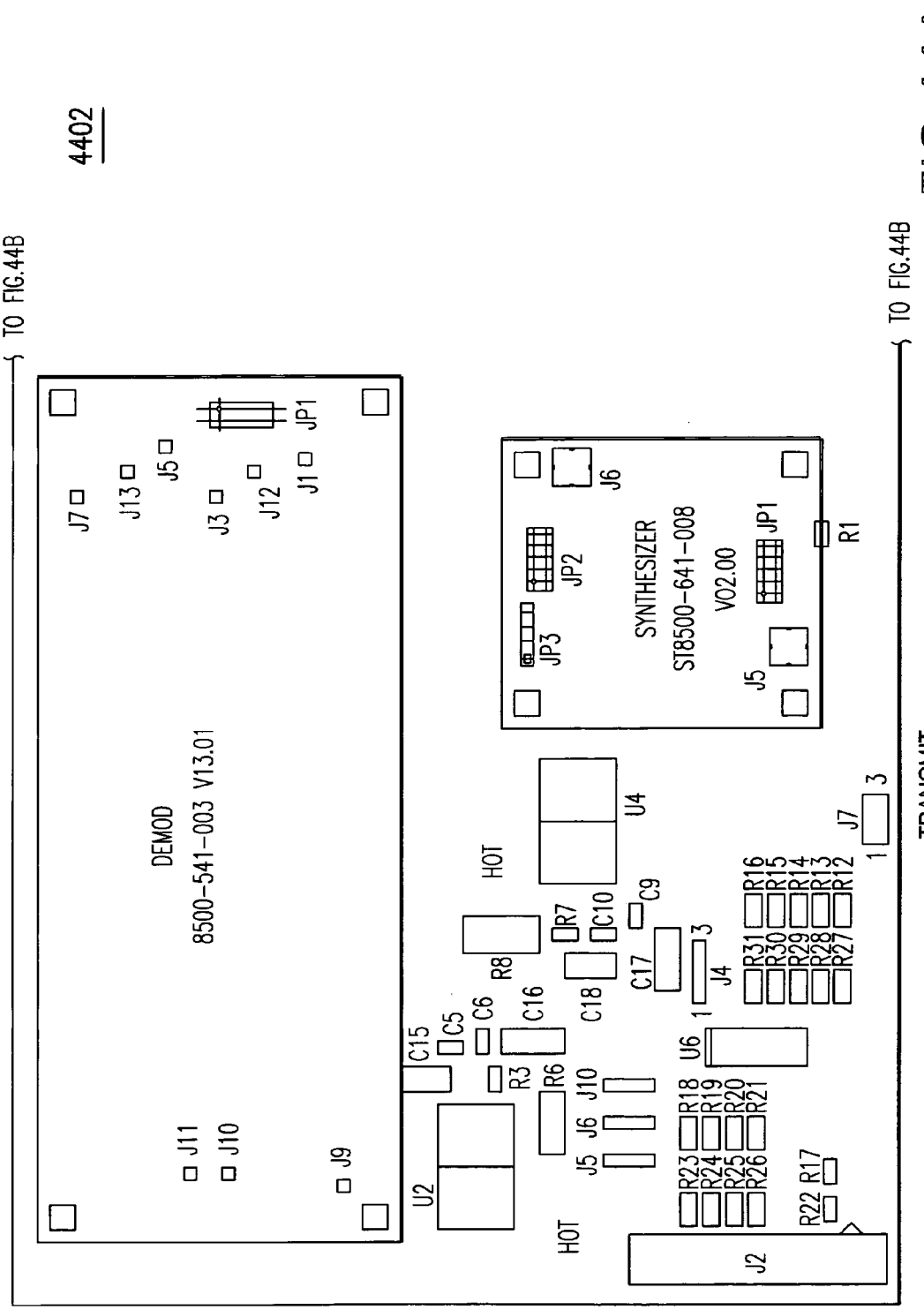

4402
TO FIG.44B
TO FIG.44B
DEMOD
8500-541-003 V13.01
SYNTHESIZER
ST8500-641-008
V02.00
TRANSMIT
HOT
HOT
J1
J2
J3
J4
J5
J6
J7
J9
J10
J11
J12
J13
JP1
JP2
JP3
R1
R3
R6
R7
R8
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
C5
C6
C9
C10
C15
C16
C17
C18
U2
U4
U6

FIG.44A

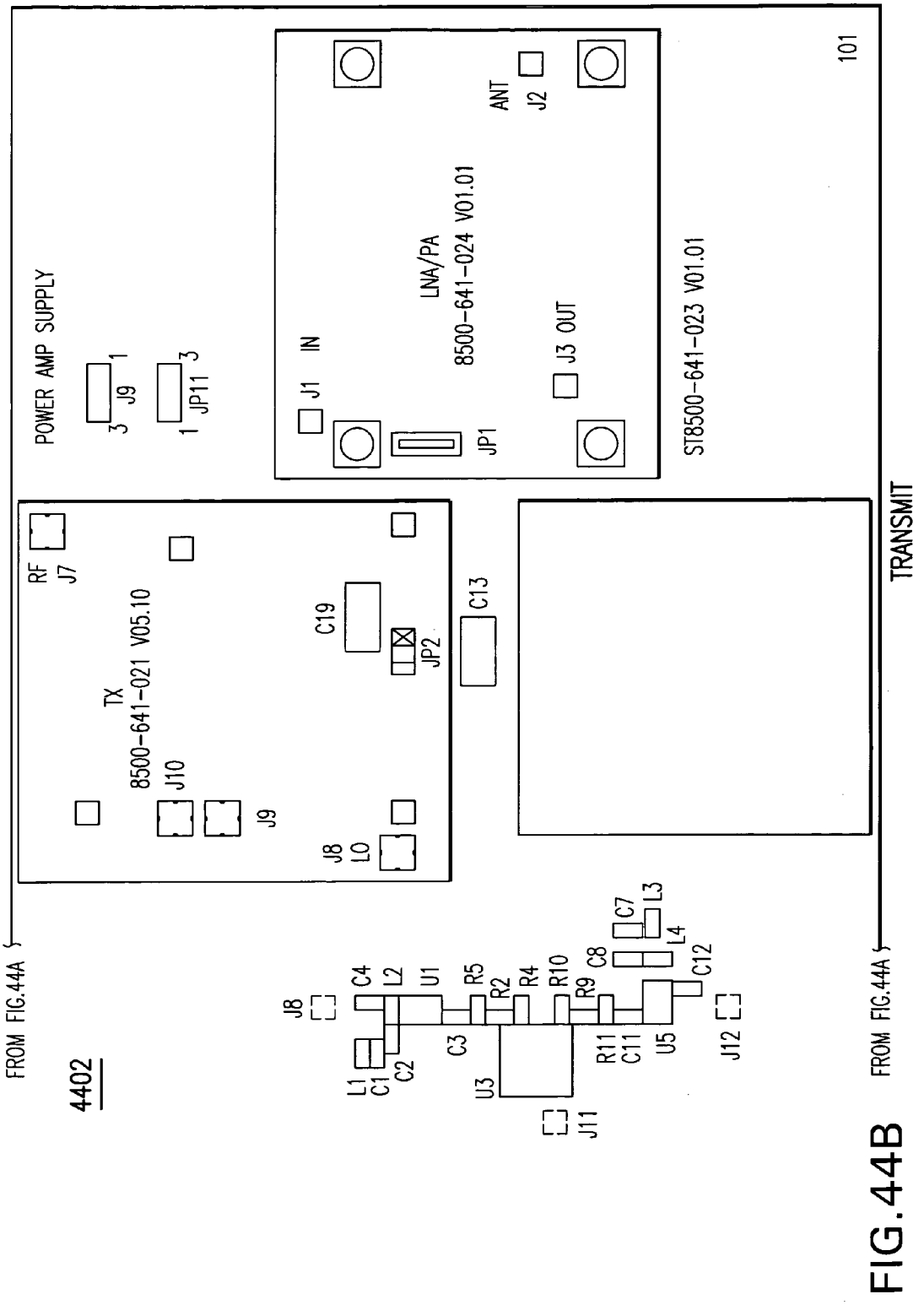

101
POWER AMP SUPPLY
J9
JP11
LNA/PA
8500-641-024 V01.01
J1 IN
J3 OUT
JP1
ANT
J2
ST8500-641-023 V01.01
RF
J7
TX
8500-641-021 V05.10
J10
J9
J8
LO
C19
JP2
C13
TRANSMIT
FROM FIG.44A
4402
J8
C4
L2
U1
R5
R2
R4
R10
R9
C8
C7
L3
L4
C12
C3
R11
C11
U5
J12
L1
C1
C2
U3
J11
FROM FIG.44A

FIG.44B

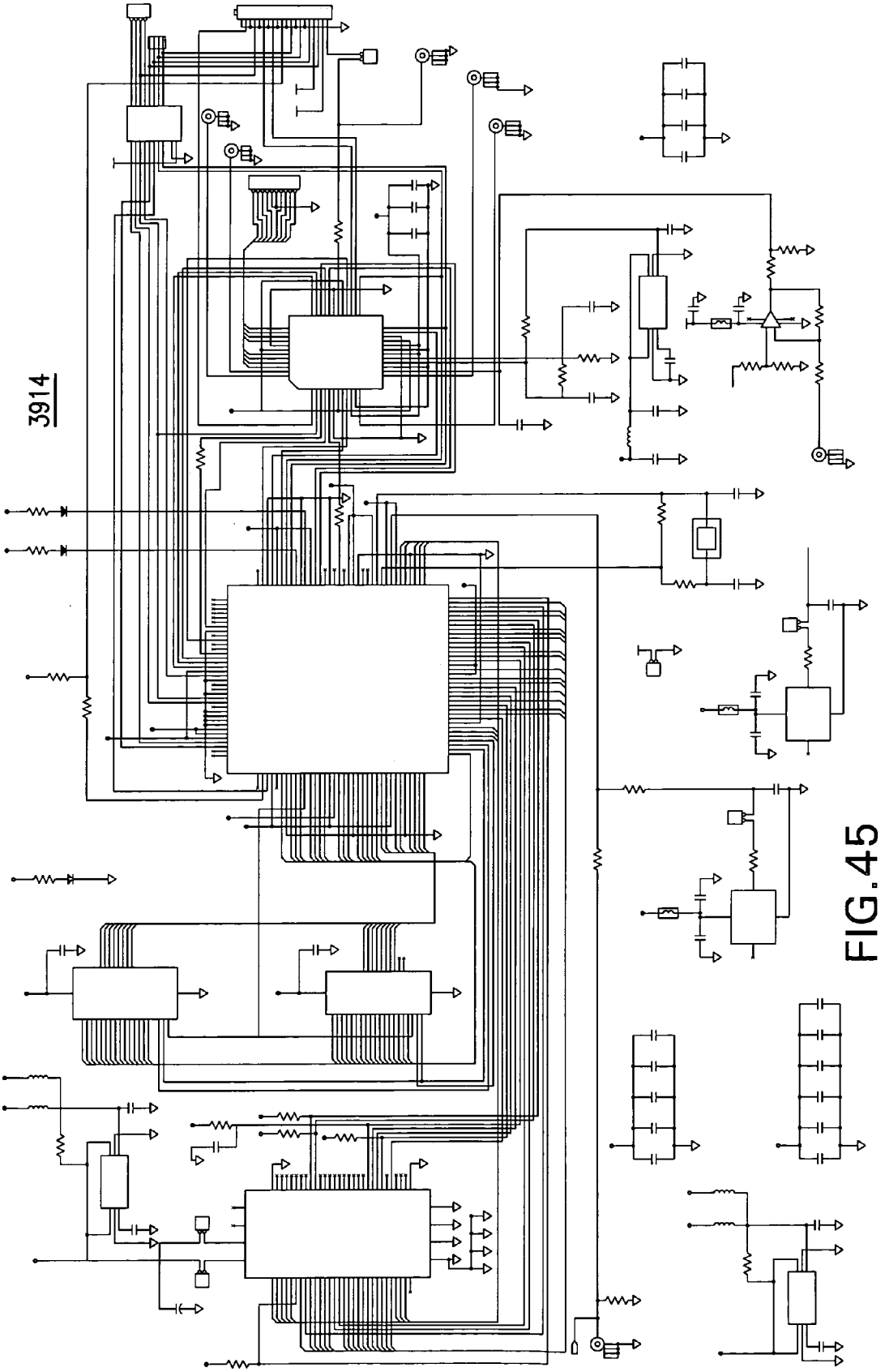


FIG.45

Item	Quantity	Reference	Part Description	Part Number	Manufacturer
1	1	C123	10uF CAP 6032, TANTALUM,20%	TAJT106K010R	KEMET
2	3	C263, C273, C275, C282	4.7uF CAP 6032, TANTALUM,20%	T491A475M006AS	KEMET
3	25	C120, C125, C126, C127, C128, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C147, C148, C149, C264, C272, C274, C279, C280, C281, C283	0.1uF CAP 0603,X7R,10%	GRM39X7R104K050AD	MURATA
4	3	C146, C269, C276	.01uF CAP 0603,X7R,10%	GRM39X7R103K050AD	MURATA
5	5	C124, C132, C133, C271, C278	100pF CAP 0603,X7R,10%	GRM39C0G101K050AD	MURATA
6	1	C129	47pF CAP 0603,X7R,10%	GRM39C0G470J100AD	MURATA
7	2	C270, C277	27pF CAP 0603,X7R,10%	GRM39C0G270K050AD	MURATA
8	1	C130	22pF CAP 0603,X7R,10%	GRM39C0G220K050AD	MURATA
9	1	C131	10pF CAP 0603,X7R,10%	GMR39C0G100D050AD	MURATA
10	1	DS1	LED GREEN	597-3311-420	DIALIGHT
11	1	DS2	LED YELLOW	597-3401-420	DIALIGHT
12	1	DS3	LED RED	597-3111-420	DIALIGHT
13	6	JP12, JP13, JP14, JP15, JP16, JP17	CONNECTOR HEADER 2PIN	2MS-19-33-01	SPECIALITY ELECTRONICS
14	1	JP11	CONNECTOR HEADER 4PIN	100/VH/TM1SQ/W.100/4	BLKCON

FIG.46A

15	7	J16, J20, J21, J22, J23, J24, J25	CONNECTOR 82MMCX	82MMCX-50-0-1	HUBER/SHUNER	
16	1	J18	CONNECTOR HEADER 10	TMS-110-01-G-S	SAMTEC	
17	1	J19	CONNECTOR WITH EJECTOR	EHT-1-10-01-S-D	SAMTEC	
18	1	P1	CONNECTOR 34X2PCMCIA	DICMJ-68S-SPC-M08	ITT CANON	
19	7	L59, L60, L61, L63, L64, L65, L66	FERRITE BEAD	BLM11A121S	MURATA	
20						
21	1	R112	10M, RESISTOR, 0603, 5%			
22	1	R114	390K, RESISTOR, 0603, 5%	ERJ-3GSYJ394V	PANASONIC	
23	1	R105	100K, RESISTOR, 0603, 5%	ERJ-3GSYJ104V	PANASONIC	
24	4	R106, R107, R108, R111	15K, RESISTOR, 0603, 5%	ERJ-3GSYJ153V	PANASONIC	
25	1	R116	9.1K, RESISTOR, 0603, 5%	ERJ-3GSYJ912V	PANASONIC	
26	1	R115	8.2K, RESISTOR, 0603, 5%	ERJ-3GSYJ822V	PANASONIC	
27	1	R113	3.9K, RESISTOR, 0603, 5%	ERJ-3GSYJ392V	PANASONIC	
28	1	R101	750, RESISTOR, 0630, 5%	ERJ-3GSYJ751V	PANASONIC	
29	1	R110	560, RESISTOR, 0603, 5%	ERJ-3GSYJ561V	PANASONIC	
30	2	R99, R100	330, RESISTOR, 0603, 5%	ERJ-3GSYJ331V	PANASONIC	
31	1	R119	50, RESISTOR, 0603, 5%	ERJ-3GSYJ500V	PANASONIC	
32	2	R128, R129	10, RESISTOR, 0603, 5%	ERJ-3GSYJ100V	PANASONIC	
33	8	R102, R103, R104, R109, R117, R118, R120, R127,	0, RESISTOR, 0603, 5%	RMJ3Z21J000ZT 3GSYJ000V	ERJ KOA PANASONIC	
34	6	R121, R122, R123, R124, R125, R126	TBD, RESISTOR, 0603, 5%	R	PANASONIC	
35	1	U10	SRAM	KM62256DLTG-5L M5M5256CVP-55LL	SAMSUNG MITSUBUSHI	
36	1	U12	MAC	AM79C930	AMD	

FIG.46B

37	1	U13	BASEBAND PROCESSOR	HFA3842A1	HARRIS
38	1	U14	FLASH RAM	AM29F010-55EC	AMD
39	1	U15	32 KHz CRYSTAL	CX-6V-SM2-32.768KHzC/1	STATEK
40	2	U45	BUS BUFFER	DS3862	NATIONAL
41	1	U48	REGULATOR 3.5 V	TK11235BMC	TOKO
42	1	U49	22MHz OSCILLATOR	FOX F3346-22MHz	FOX
43	1	U50	2 VOLT REFERENCE	TK11220BMC	TOKO
44	1	U51	40MHz OSCILLATOR	CXO-M-10N-40MHz A/1	STATEK

FIG.46C

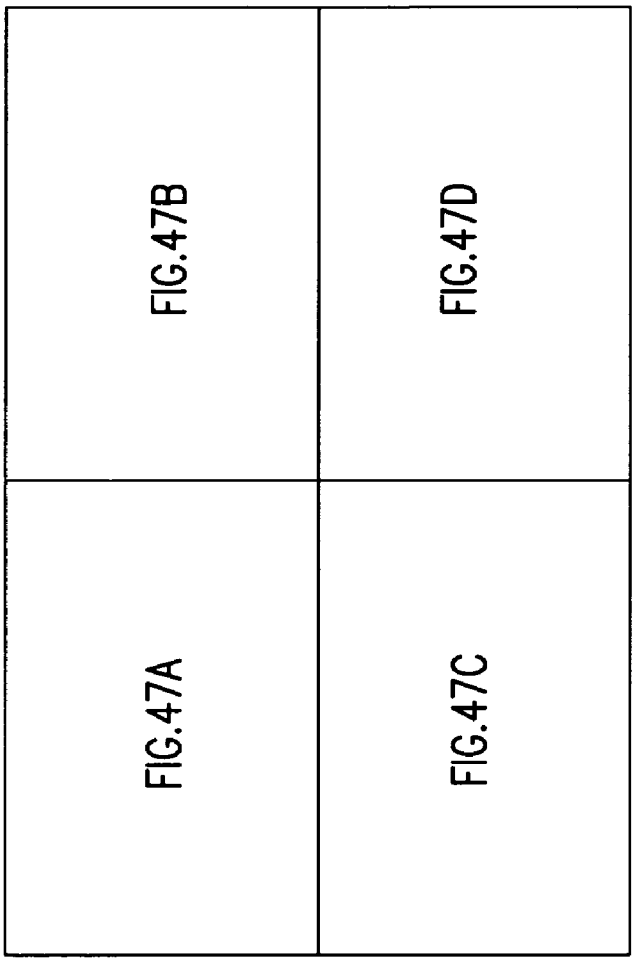


FIG.47

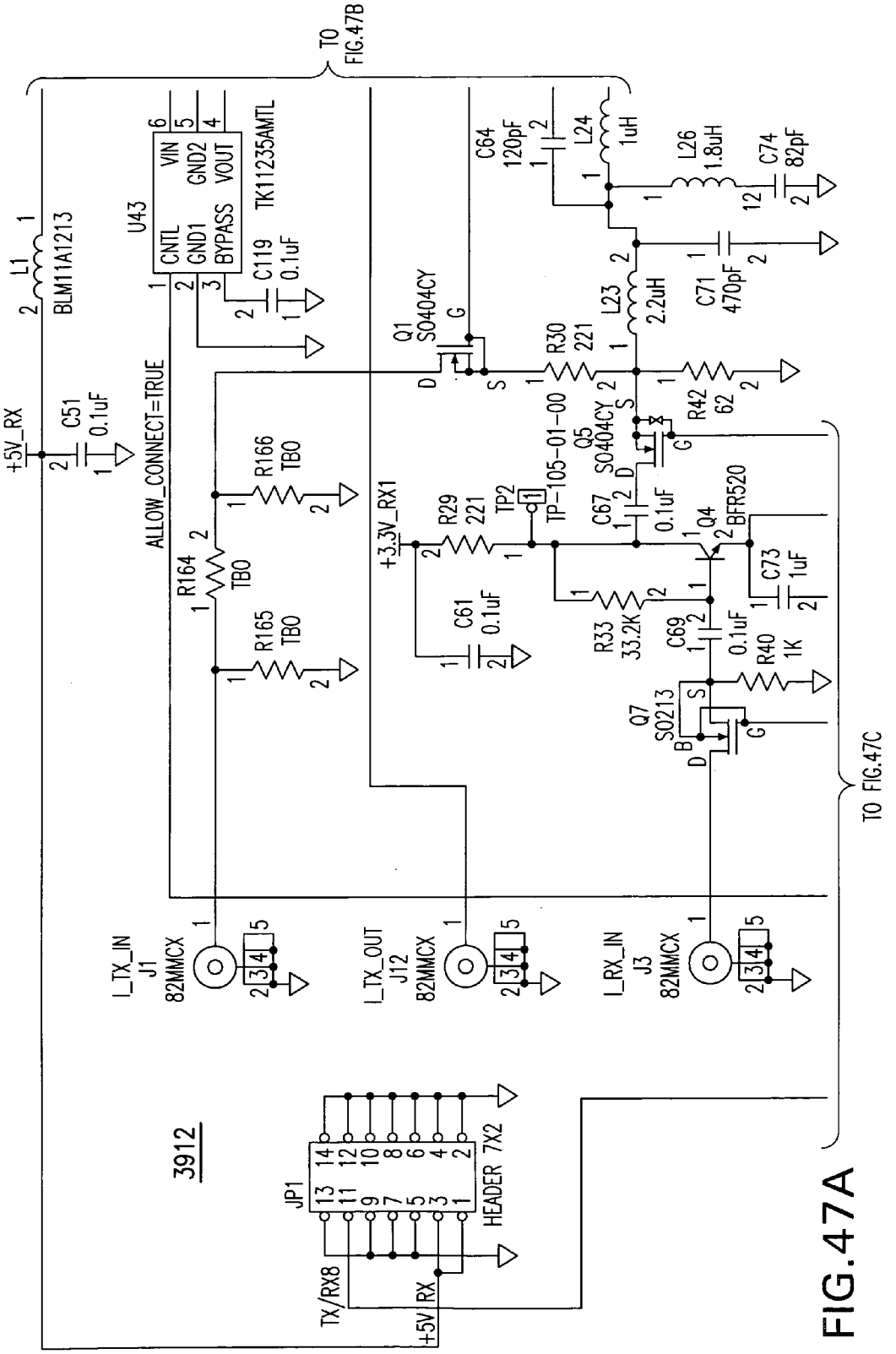

TO FIG.47B
+5V_RX
C51 0.1uF
L1 BLM11A1213
U43 TK11235AMTL
CNTL GND1 BYPASS VIN GND2 VOUT
C119 0.1uF
ALLOW_CONNECT=TRUE
R164 TBO
R165 TBO
R166 TBO
+3.3V_RX1
R29 221
TP2 TP-105-01-00
C61 0.1uF
Q1 SO404CY
R30 221
C64 120pF
L24 1uH
L23 2.2uH
L26 1.8uH
C71 470pF
C74 82pF
Q5 SO404CY
R42 62
C67 0.1uF
Q4 BFR520
C73 1uF
R33 33.2K
C69 0.1uF
R40 1K
Q7 SO213
I_TX_IN J1 82MMCX
I_TX_OUT J12 82MMCX
I_RX_IN J3 82MMCX
3912
JP1 HEADER 7X2
TX/RX8
+5V RX
TO FIG.47C

FIG.47A

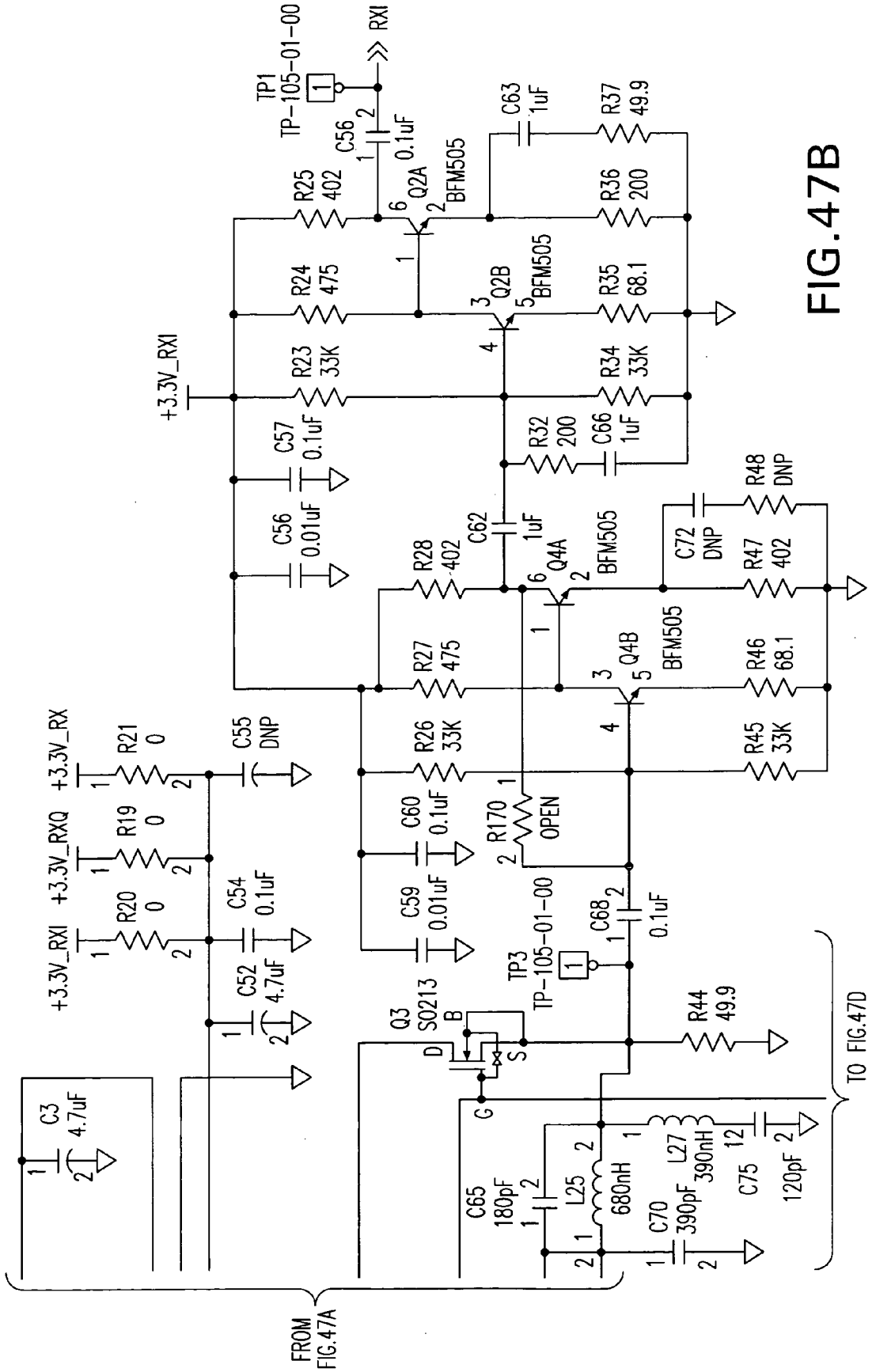

TP1
TP-105-01-00
RXI
C56
0.1uF
C63
1uF
R37
49.9
R25
402
Q2A
BFM505
R36
200
R24
475
Q2B
BFM505
R35
68.1
+3.3V_RXI
R23
33K
R34
33K
C57
0.1uF
R32
200
C66
1uF
C56
0.01uF
C62
1uF
R48
DNP
R28
402
Q4A
BFM505
C72
DNP
R47
402
R27
475
Q4B
BFM505
R46
68.1
+3.3V_RX
R21
0
C55
DNP
R26
33K
R45
33K
+3.3V_RXQ
R19
0
C60
0.1uF
R170
OPEN
+3.3V_RXI
R20
0
C54
0.1uF
C59
0.01uF
C68
0.1uF
C52
4.7uF
TP3
TP-105-01-00
Q3
SO213
R44
49.9
C3
4.7uF
C65
180pF
L25
680nH
C70
390pF
L27
390nH
C75
120pF
FROM
FIG.47A
TO FIG.47D

FIG.47B

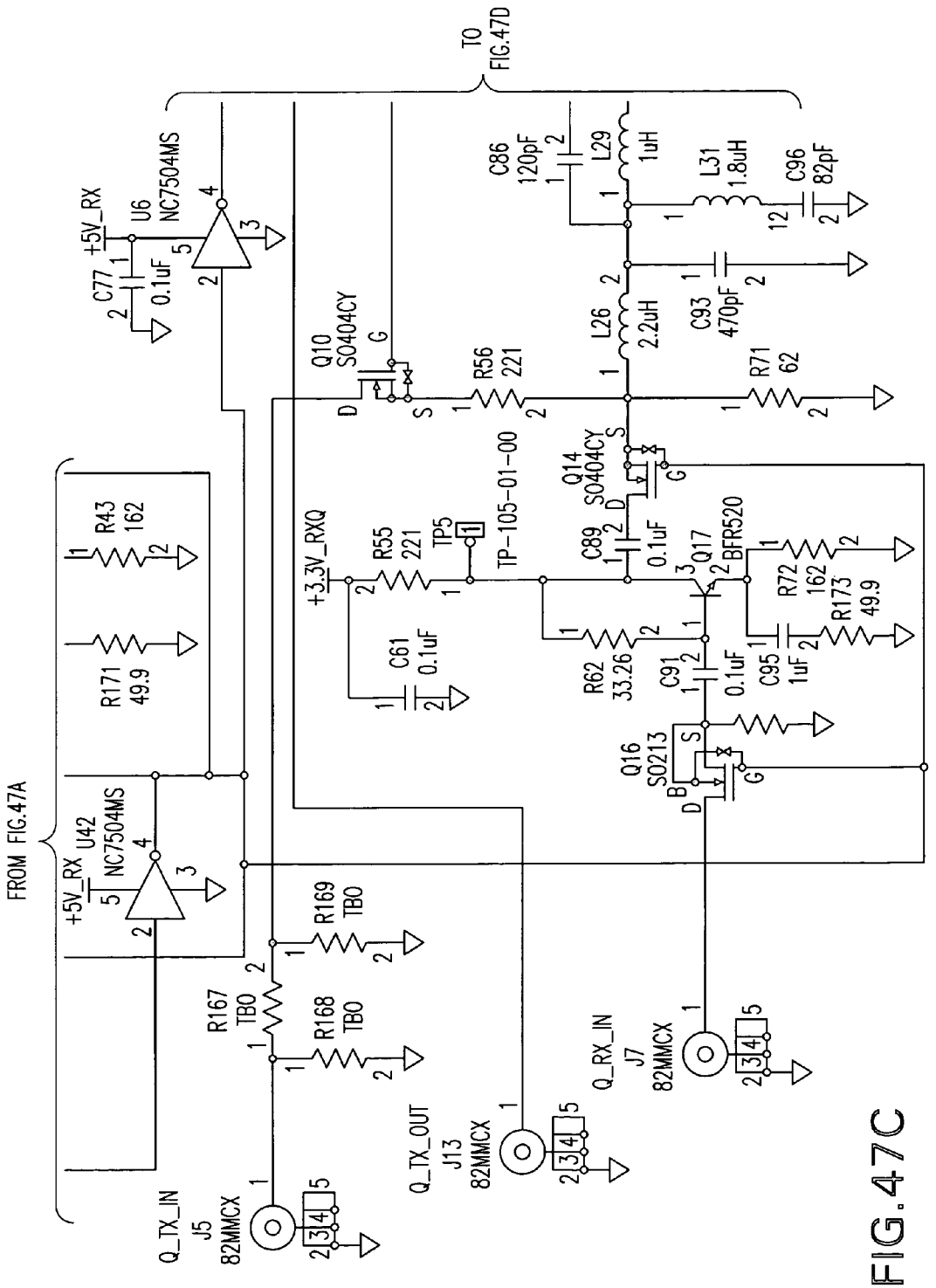

FROM FIG.47A
TO FIG.47D
+5V_RX
U42
NC7504MS
U6
NC7504MS
C77
0.1uF
R171
49.9
R43
162
R169
TBO
R167
TBO
R168
TBO
Q_TX_IN
J5
82MMCX
Q_TX_OUT
J13
82MMCX
+3.3V_RXQ
R55
221
TP5
TP-105-01-00
C61
0.1uF
Q10
SO404CY
R56
221
Q14
SO404CY
C89
0.1uF
Q17
BFR520
R62
33.26
C91
0.1uF
C95
1uF
R72
162
R173
49.9
Q16
SO213
Q_RX_IN
J7
82MMCX
C86
120pF
L29
1uH
L31
1.8uH
C96
82pF
L26
2.2uH
C93
470pF
R71
62

FIG.47C

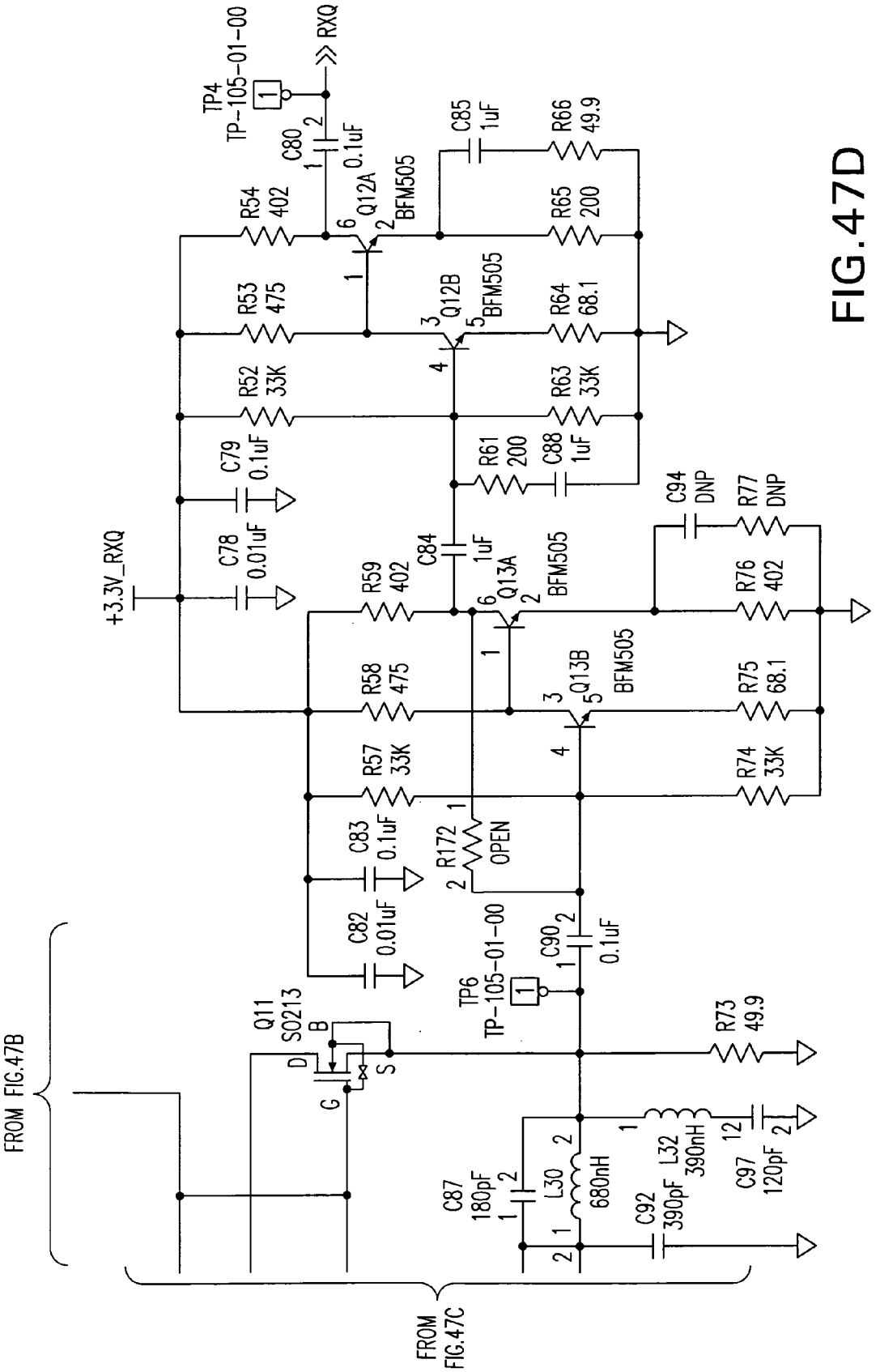

FROM FIG.47B
FROM FIG.47C
+3.3V_RXQ
TP4 TP-105-01-00
RXQ
C80 0.1uF
C85 1uF
R66 49.9
R54 402
Q12A BFM505
R65 200
R53 475
Q12B BFM505
R64 68.1
R52 33K
R63 33K
C79 0.1uF
C78 0.01uF
R61 200
C88 1uF
C94 DNP
R77 DNP
C84 1uF
R59 402
Q13A BFM505
R76 402
R58 475
Q13B BFM505
R75 68.1
R57 33K
R74 33K
C83 0.1uF
R172 OPEN
C82 0.01uF
C90 0.1uF
TP6 TP-105-01-00
Q11 SO213
R73 49.9
C87 180pF
L30 680nH
C92 390pF
L32 390nH
C97 120pF

FIG.47D

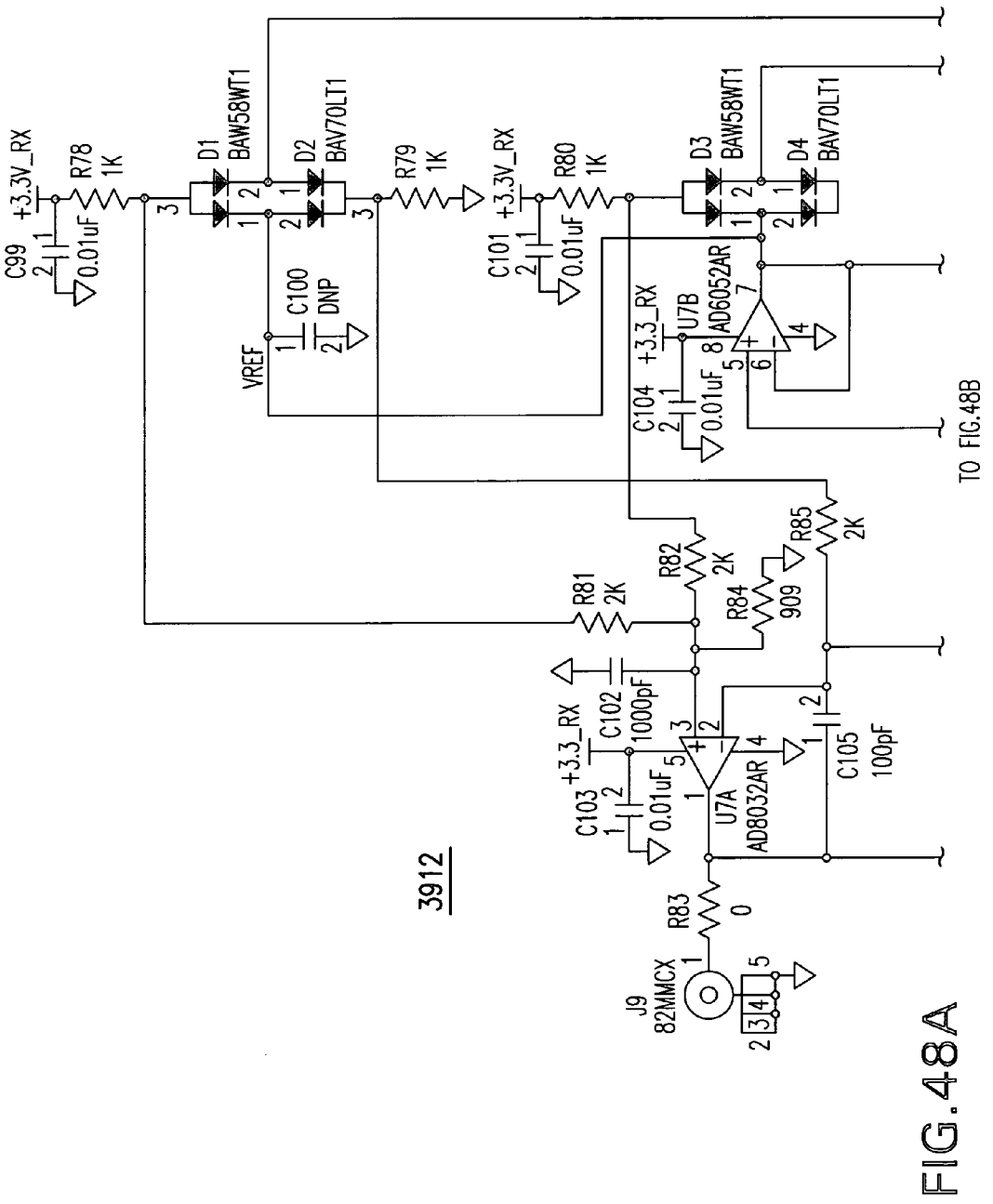

C99
+3.3V_RX
0.01uF
R78
1K
D1
BAW56WT1
D2
BAV70LT1
R79
1K
C100
DNP
VREF
C101
+3.3V_RX
0.01uF
R80
1K
D3
BAW56WT1
D4
BAV70LT1
C104
+3.3_RX
0.01uF
U7B
AD6052AR
TO FIG.48B
R81
2K
R82
2K
R84
909
R85
2K
C103
+3.3_RX
0.01uF
C102
1000pF
U7A
AD8032AR
C105
100pF
R83
0
J9
82MMCX
3912

FIG.48A

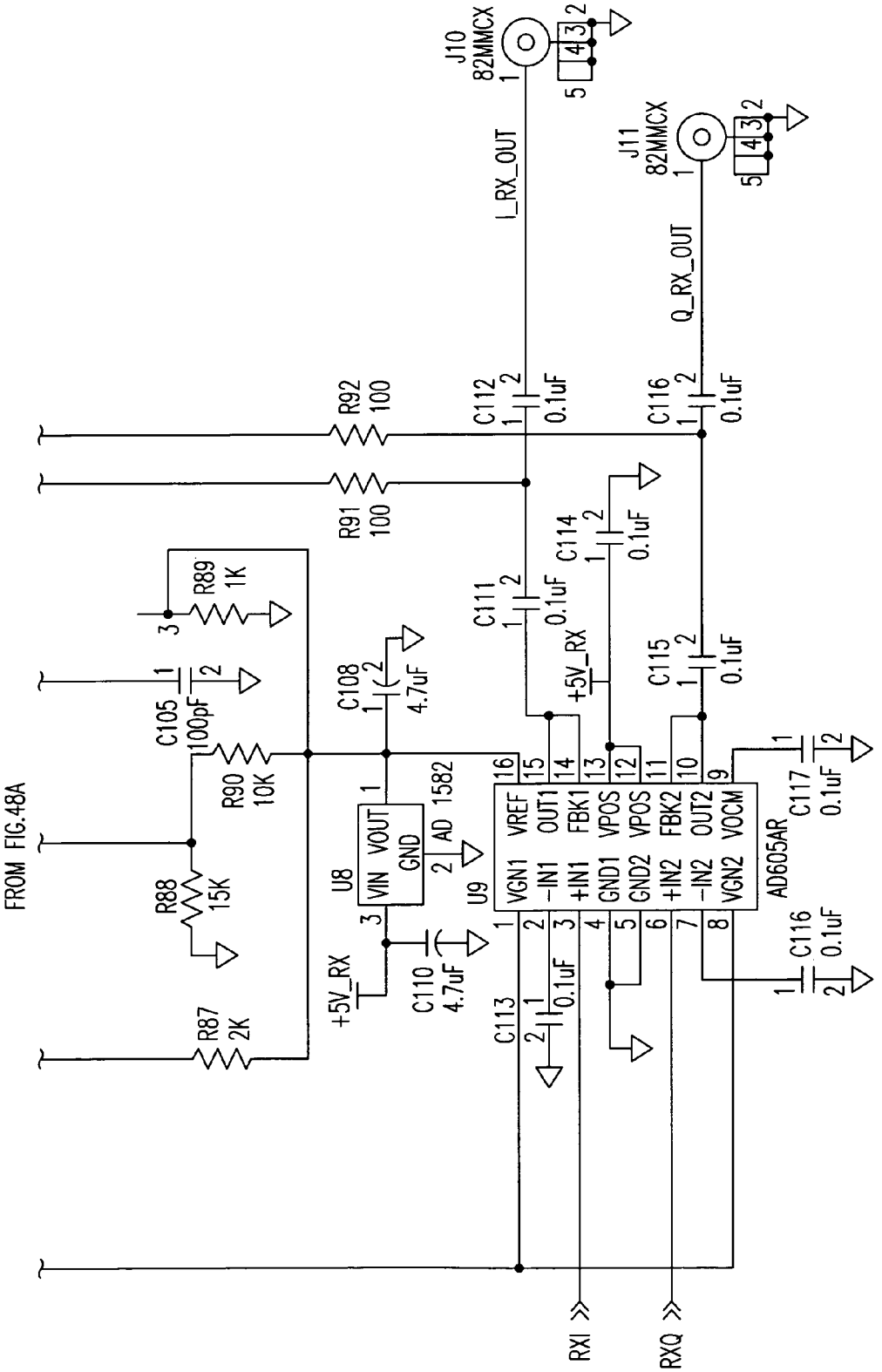

FROM FIG.48A
R87 2K
R88 15K
R90 10K
C105 100pF
R89 1K
C108 4.7uF
C110 4.7uF
U8
VIN VOUT GND
AD 1582
U9
+5V_RX
C111 0.1uF
C112 0.1uF
C113 0.1uF
C114 0.1uF
C115 0.1uF
C116 0.1uF
C117 0.1uF
R91 100
R92 100
J10 82MMCX
J11 82MMCX
I_RX_OUT
Q_RX_OUT
VGN1 -IN1 +IN1 GND1 GND2 +IN2 -IN2 VGN2
VREF OUT1 FBK1 VPOS VPOS FBK2 OUT2 VOCM
AD605AR
RXI >>
RXQ >>

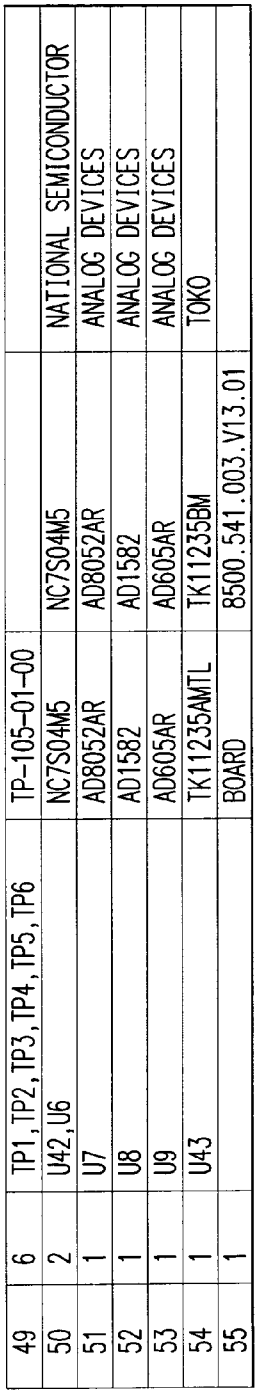
FIG.48B

ITEM	QUANT.	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	4	C3,C52,C108,C110	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	MURATA
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	1	C55	DNP	T491A475K006AS	KEMET
4	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	MURATA
		C103,C104			
5	8	C62,C63,C66,C73,C84,C85,	1uF	GRM40Y5V105Z016	MURATA
		C88,C95			
6	4	C64,C75,C86,C97	120pF	GRM39C0G121J050	MURATA
7	2	C65,C87	180pF	GRM39C0G181J050	MURATA
8	2	C70,C92	390pF	GRM39C0G391J050	MURATA
9	2	C71,C93	470pF	GRM39C0G471J050	MURATA
10	2	C72,C94	DNP	GRM40Y5V105Z016	MURATA
11	2	C74,C96	82pF	GRM39C0G820J050	MURATA
12	2	C100,C106	DNP	DNP	MURATA
13	2	C105,C102	1000pF	GRM39C0G102K050	MURATA
14	2	D3,D1	BAW56WT1	BAW56WT1	MOTOROLA
15	2	D4,D2	BAV70LT1	BAV70LT1	MOTOROLA
16	1	JP1	HEADER 7X2	FTSH-107-02-L-D	SAMTEC
17	9	J1,J3,J5,J7,J9,J10,J11,	82MMCX	82MMCX-50-0-1	SUHNER
		J12,J13			
18	1	L1	BLM11A121S	BLM11A121S	MURATA
19	2	L23,L28	2.2uH	LQG21N2R2K10	MURATA
20	2	L29,L24	1uH	LQG21N1R0K10	MURATA
21	2	L30,L25	680nH	LQG21NR68K10	MURATA

FIG.49A

22	2	L26,L31	1.8uH	LQG21N1R8K10	MURATA
23	2	L32,L27	390nH	LQG21NR39K10	MURATA
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	CALOGIC
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	PHILIPS
26	4	Q3,Q7,Q11,Q16	SD213	SD213	CALOGIC
27	2	Q17,Q8	BFR520	BFR520	PHILIPS
28	4	R19,R20,R21,R83	0	ERJ3GSY0R00	PANASONIC
29	8	R23,R26,R34,R45,R52,R57, R63,R74	33K	ERJ3GSYJ333	PANASONIC
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	PANASONIC
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	PANASONIC
32	4	R29,R30,R55,R56	221	ERJ3EKF2210	PANASONIC
33	2	R32,R61	200	ERJ3GSYJ201	PANASONIC
34	2	R33,R62	33.2K	ERJ3GSYJ333	PANASONIC
35	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	PANASONIC
36	2	R36,R65	200	ERJ3EKF2000	PANASONIC
37	6	R37,R44,R66,R73,R171, R173	49.9	ERJ3EKF49R9	PANASONIC
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	PANASONIC
39	2	R42,R71	62	ERJEGSYJ620	PANASONIC
40	2	R43,R72	162	ERJ3EKF1620	PANASONIC
41	2	R77,R48	DNP	ERJ3GSYJ330	PANASONIC
42	4	R81,R82,R85,R87	2K	ERJ3EKF2001	PANASONIC
43	1	R84	909	ERJ3EKF9090	PANASONIC
44	1	R88	15K	ERJ3EJF1502	PANASONIC
45	1	R90	10K	ERJ3EKF1002	PANASONIC
46	2	R91,R92	100	ERJ3EKF1000	PANASONIC
47	6	R164,R165,R166,R167,R168, R169	TBD		PANASONIC
48	2	R170,R172	OPEN		PANASONIC

FIG.49B



49	6	TP1, TP2, TP3, TP4, TP5, TP6	TP-105-01-00		
50	2	U42, U6	NC7S04M5	NC7S04M5	NATIONAL SEMICONDUCTOR
51	1	U7	AD8052AR	AD8052AR	ANALOG DEVICES
52	1	U8	AD1582	AD1582	ANALOG DEVICES
53	1	U9	AD605AR	AD605AR	ANALOG DEVICES
54	1	U43	TK11235AMTL	TK11235BM	TOKO
55	1		BOARD	8500.541.003.V13.01	

FIG.49C

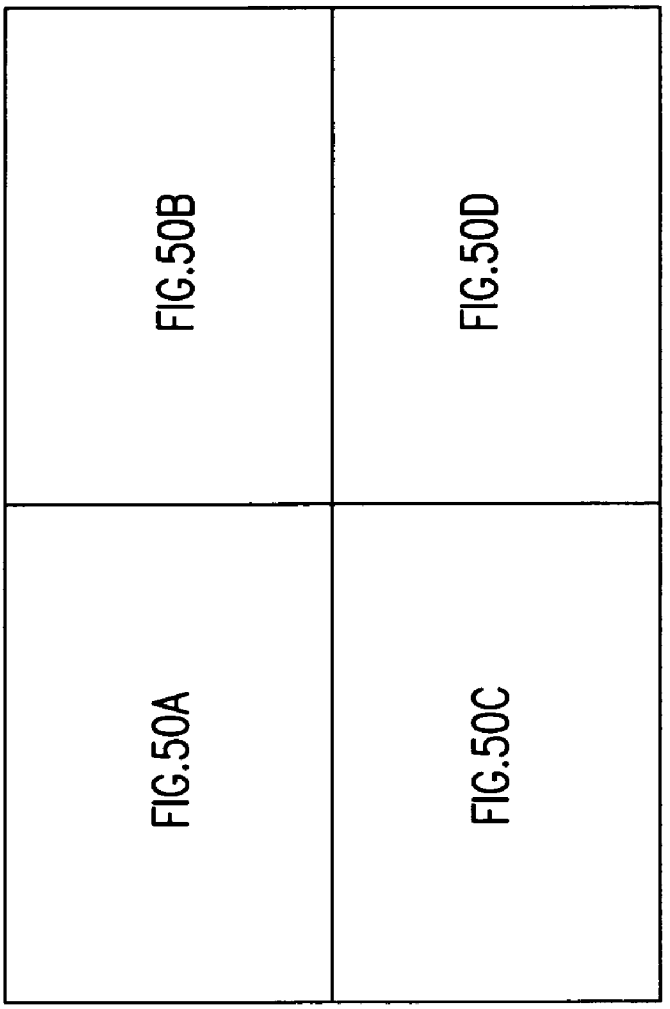


FIG.50

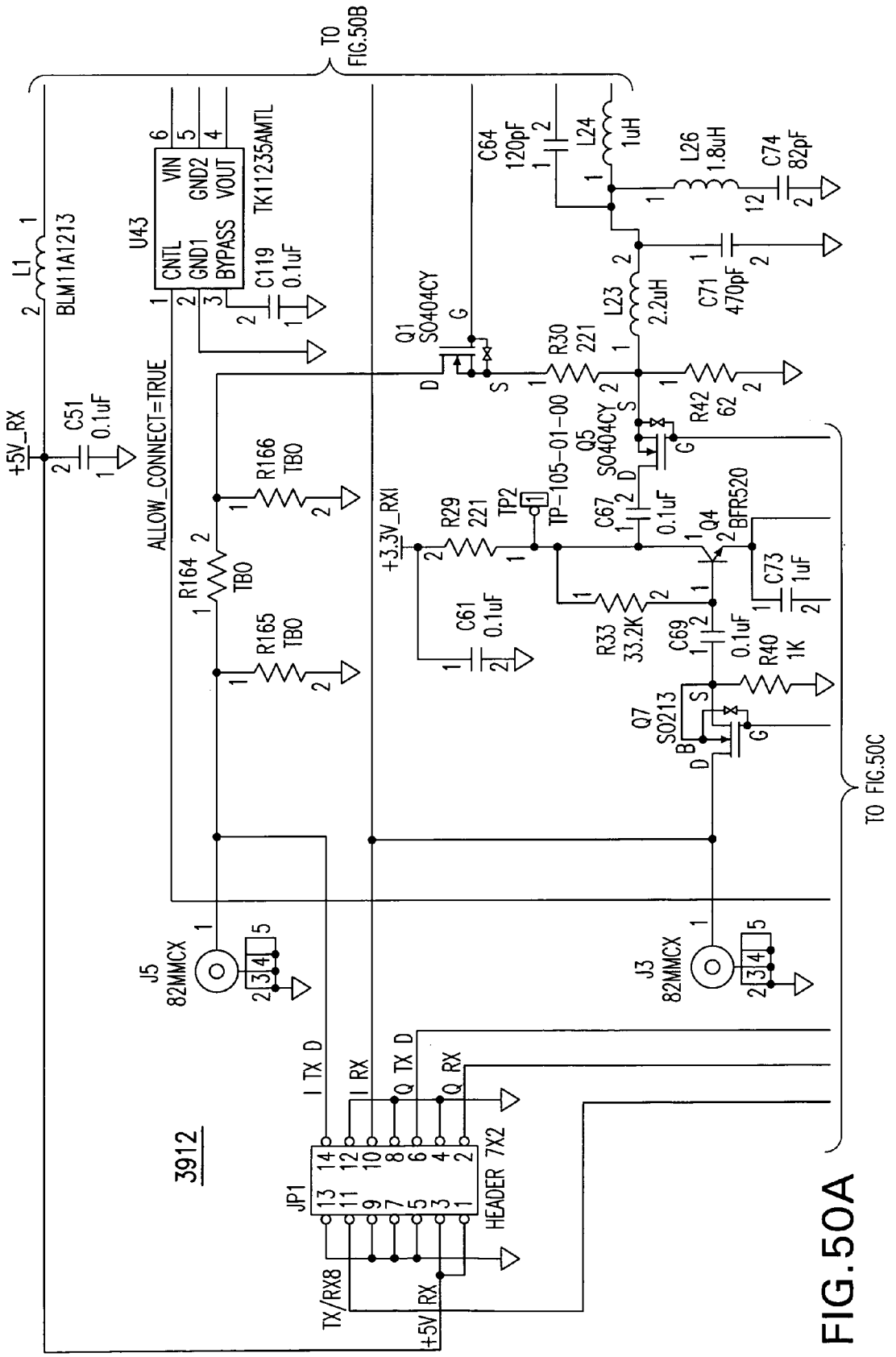

TO FIG.50B
+5V_RX
C51 0.1uF
L1 BLM11A1213
U43 TK11235AMTL
CNTL GND1 BYPASS VIN GND2 VOUT
C119 0.1uF
ALLOW_CONNECT=TRUE
R164 TBD
R165 TBD
R166 TBD
Q1 SO404CY
R30 221
C64 120pF
L24 1uH
L23 2.2uH
L26 1.8uH
C74 82pF
C71 470pF
R42 62
Q5 SO404CY
TP2 TP-105-01-00
R29 221
+3.3V_RXI
C67 0.1uF
Q4 BFR520
C73 1uF
C61 0.1uF
R33 33.2K
C69 0.1uF
R40 1K
Q7 SO213
J5 82MMCX
J3 82MMCX
I TX D
I RX
Q TX D
Q RX
JP1 HEADER 7X2
TX/RX8
+5V RX
3912
TO FIG.50C

FIG.50A

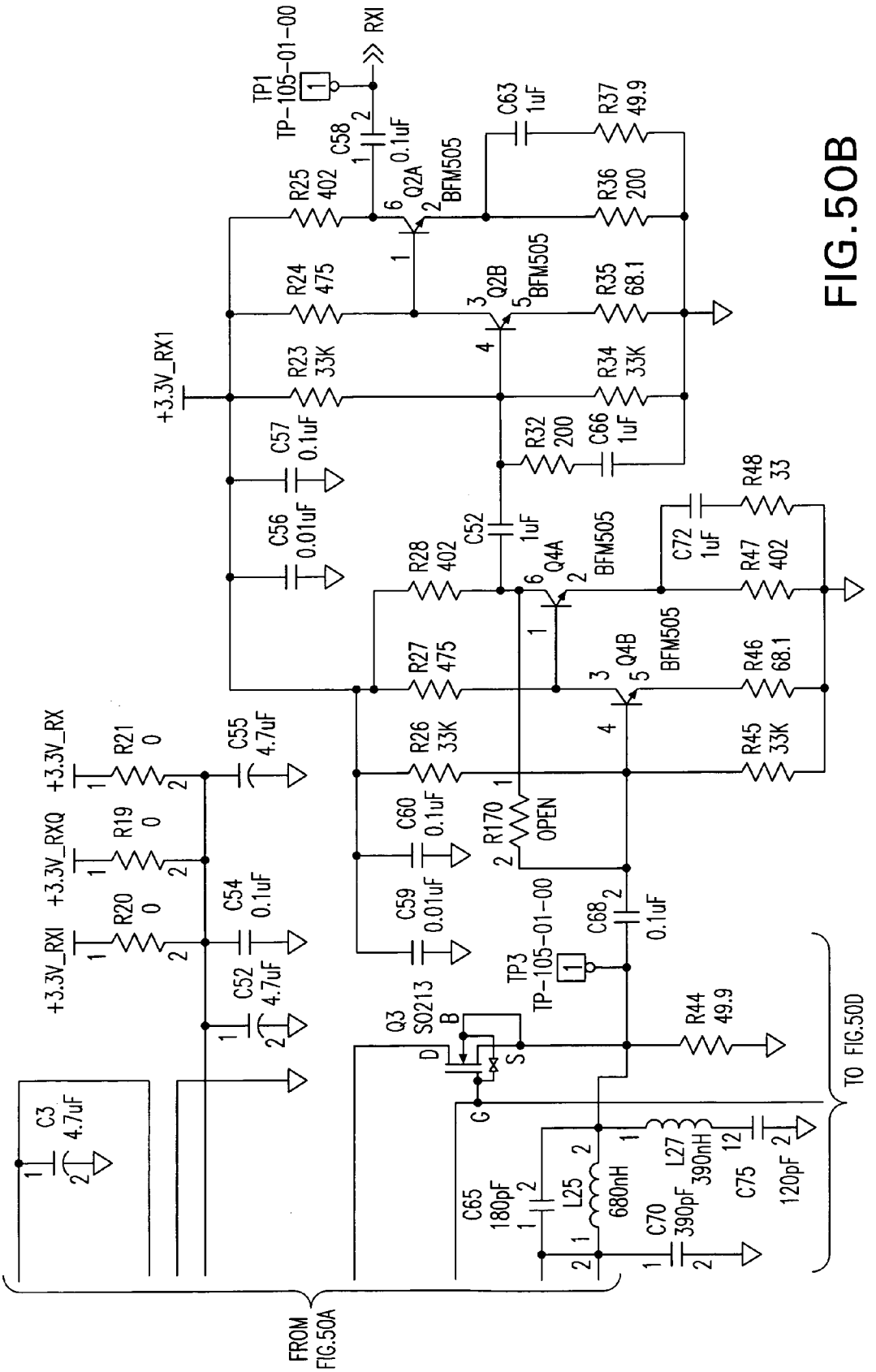

TP1
TP-105-01-00
RXI
C58
0.1uF
Q2A
BFM505
Q2B
BFM505
R25
402
R24
475
R23
33K
R36
200
R35
68.1
R34
33K
C63
1uF
R37
49.9
+3.3V_RX1
C57
0.1uF
C56
0.01uF
R32
200
C66
1uF
C52
1uF
R28
402
R27
475
R26
33K
Q4A
BFM505
Q4B
BFM505
C72
1uF
R47
402
R46
68.1
R45
33K
R48
33
+3.3V_RX
R21
0
C55
4.7uF
+3.3V_RXQ
R19
0
C54
0.1uF
+3.3V_RXI
R20
0
C52
4.7uF
C60
0.1uF
R170
OPEN
C59
0.01uF
C68
0.1uF
TP3
TP-105-01-00
Q3
SO213
R44
49.9
C3
4.7uF
C65
180pF
L25
680nH
C70
390pF
L27
390nH
C75
120pF
FROM
FIG.50A
TO FIG.50D

FIG.50B

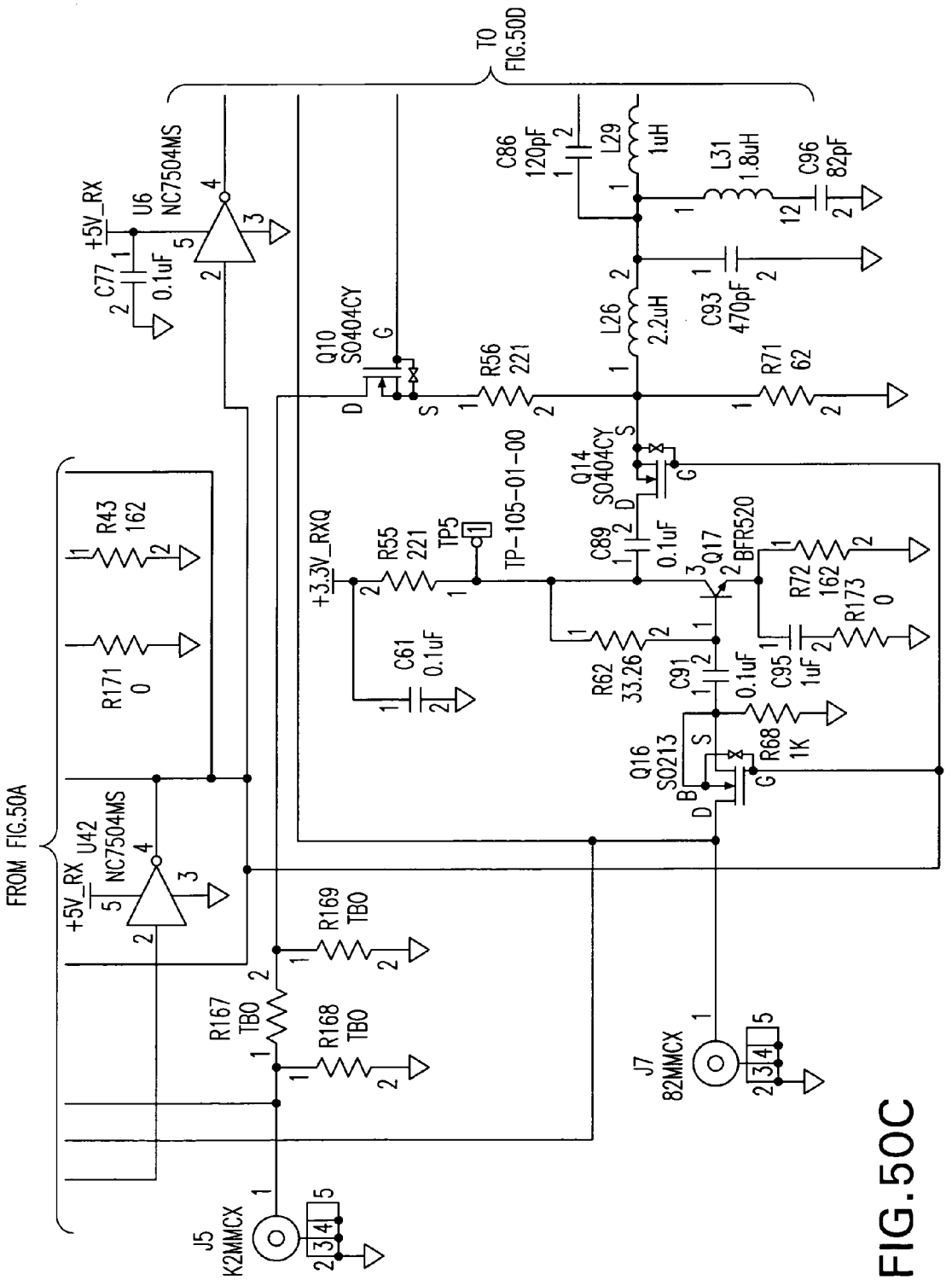

FROM FIG.50A
TO FIG.50D
+5V_RX
U42 NC7504MS
U6 NC7504MS
C77 0.1uF
R171 0
R43 162
R167 TBO
R168 TBO
R169 TBO
J5 K2MMCX
J7 82MMCX
+3.3V_RXQ
R55 221
TP5
TP-105-01-00
C61 0.1uF
Q10 SO404CY
R56 221
Q14 SO404CY
C89 0.1uF
Q17 BFR520
R62 33.26
C91 0.1uF
Q16 SO213
R68 1K
C95 1uF
R72 162
R173 0
C86 120pF
L29 1uH
L31 1.8uH
C96 82pF
L26 2.2uH
C93 470pF
R71 62

FIG.50C

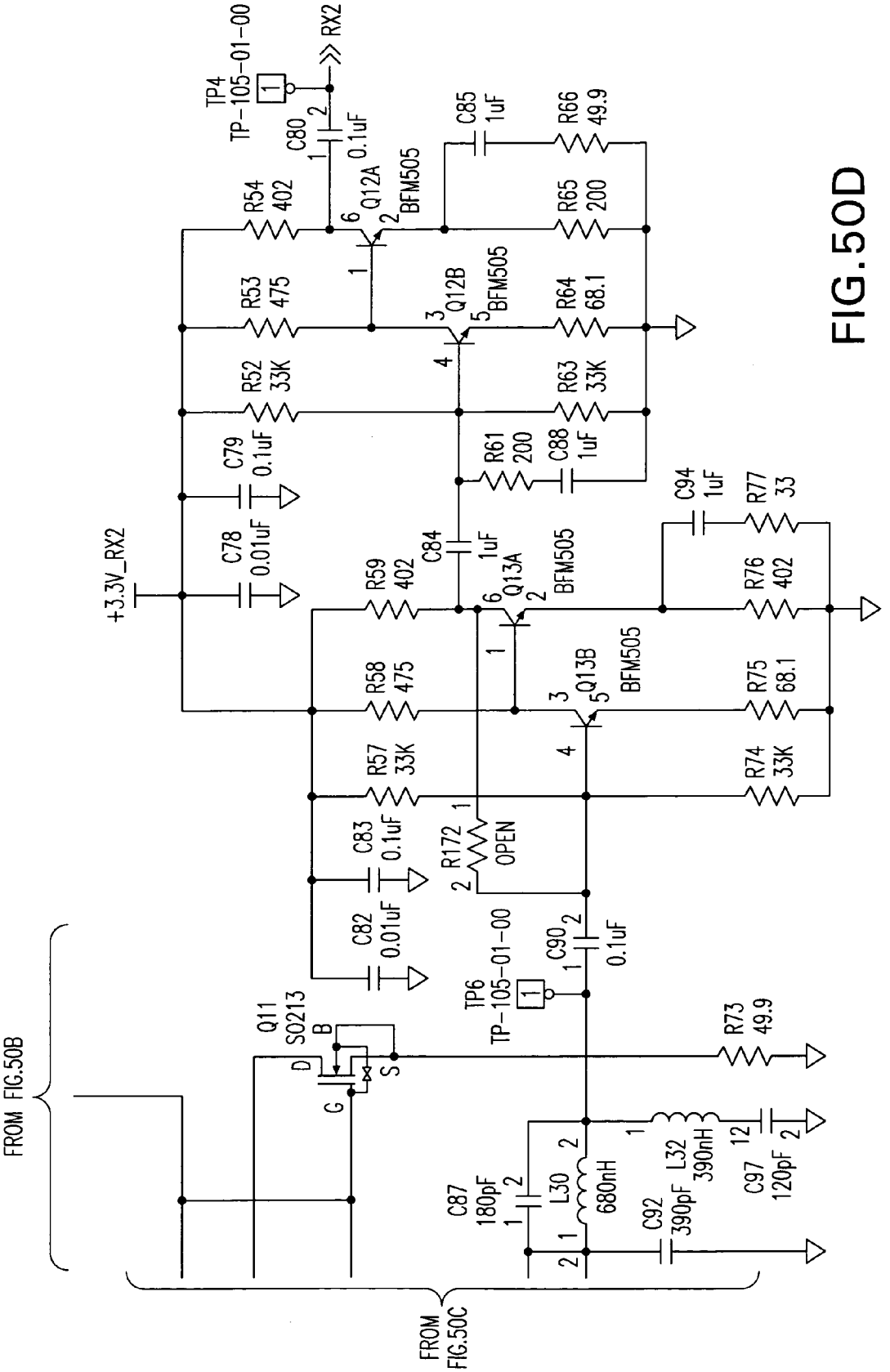

TP4
TP-105-01-00
RX2
C80
0.1uF
C85
1uF
R66
49.9
R54
402
Q12A
BFM505
R65
200
R53
475
Q12B
BFM505
R64
68.1
R52
33K
R63
33K
C79
0.1uF
C78
0.01uF
+3.3V_RX2
R61
200
C88
1uF
C94
1uF
R77
33
C84
1uF
R59
402
Q13A
BFM505
R76
402
R58
475
Q13B
BFM505
R75
68.1
R57
33K
R74
33K
R172
OPEN
C83
0.1uF
C82
0.01uF
C90
0.1uF
TP6
TP-105-01-00
Q11
SO213
R73
49.9
FROM FIG.50B
C87
180pF
L30
680nH
C92
390pF
L32
390nH
C97
120pF
FROM
FIG.50C

FIG.50D

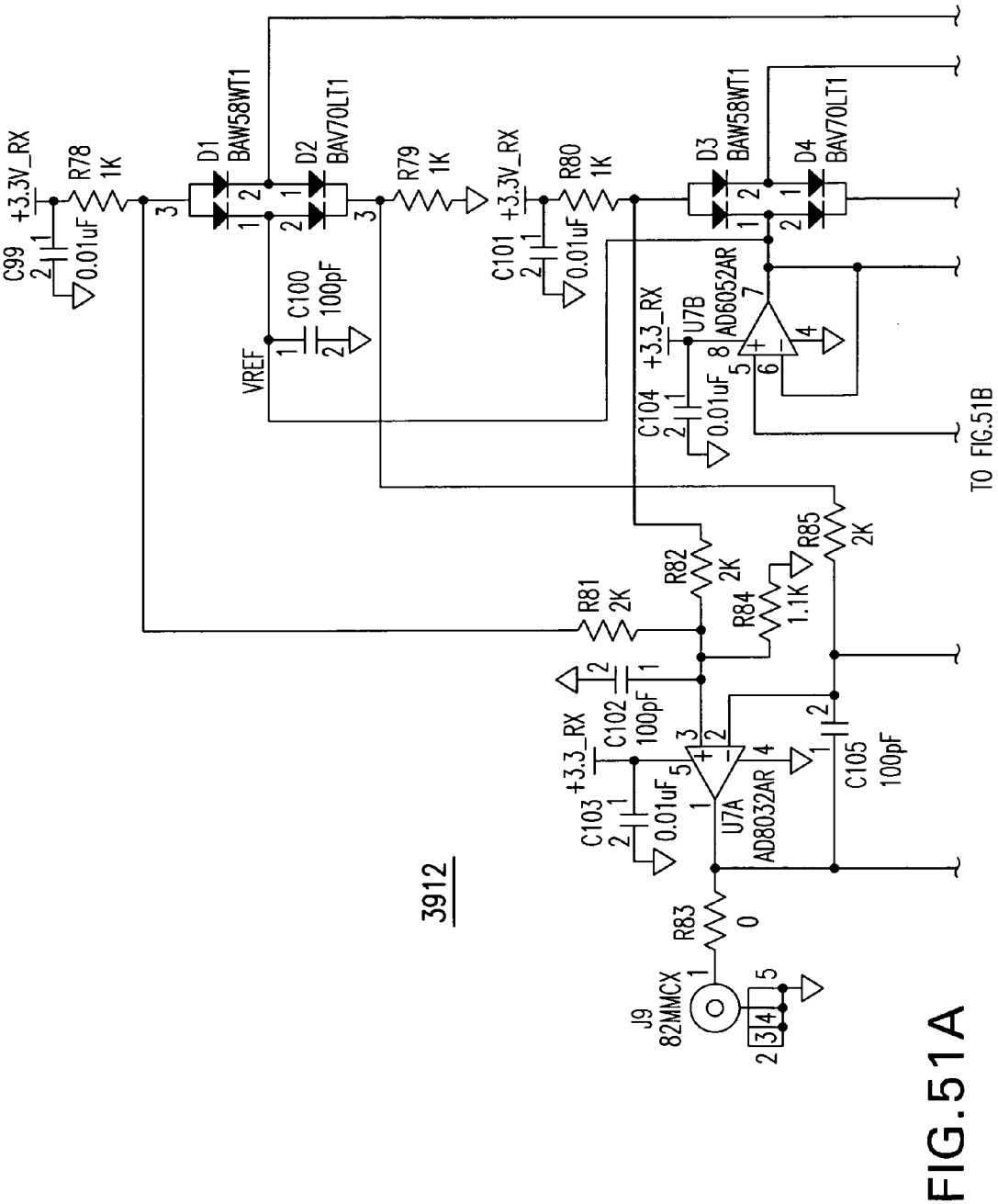

3912
C99
+3.3V_RX
R78
1K
0.01uF
D1
BAW56WT1
D2
BAV70LT1
C100
100pF
VREF
R79
1K
C101
+3.3V_RX
R80
1K
0.01uF
D3
BAW56WT1
D4
BAV70LT1
C104
+3.3_RX
U7B
AD8032AR
0.01uF
TO FIG.51B
R81
2K
R82
2K
R84
1.1K
R85
2K
C102
100pF
C103
+3.3_RX
0.01uF
U7A
AD8032AR
C105
100pF
R83
0
J9
82MMCX

FIG.51A

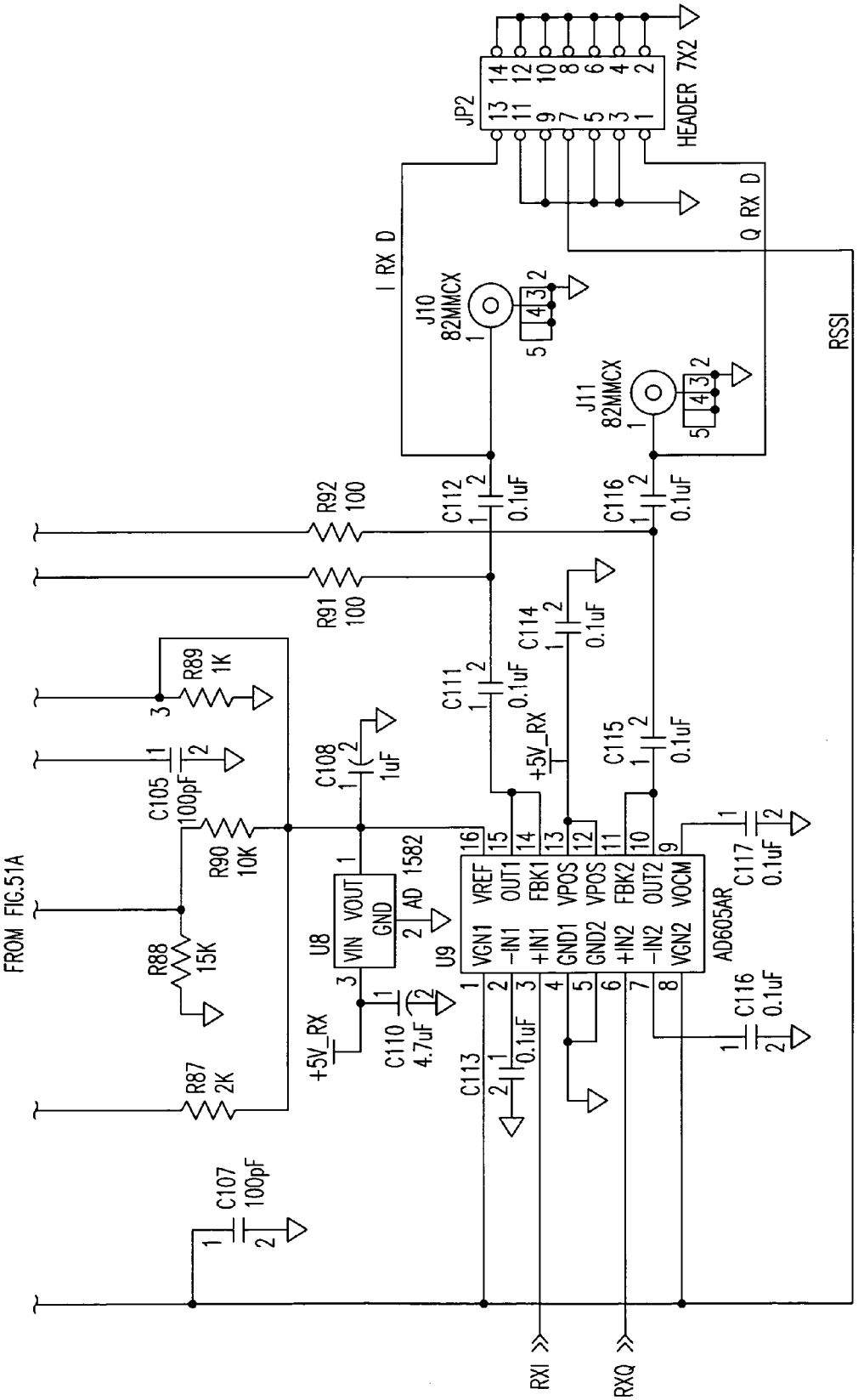

JP2
HEADER 7X2
I RX D
Q RX D
RSSI
J10
82MMCX
J11
82MMCX
R92
100
R91
100
C112
0.1uF
C116
0.1uF
C111
0.1uF
C114
0.1uF
C115
0.1uF
C117
0.1uF
C116
0.1uF
R89
1K
C105
100pF
C108
1uF
R90
10K
R88
15K
R87
2K
C107
100pF
C110
4.7uF
C113
0.1uF
+5V_RX
+5V_RX
FROM FIG.51A
U8
VIN VOUT
GND
AD 1582
U9
VGN1 VREF
-IN1 OUT1
+IN1 FBK1
GND1 VPOS
GND2 VPOS
+IN2 FBK2
-IN2 OUT2
VGN2 VOCM
AD605AR
RXI
RXQ

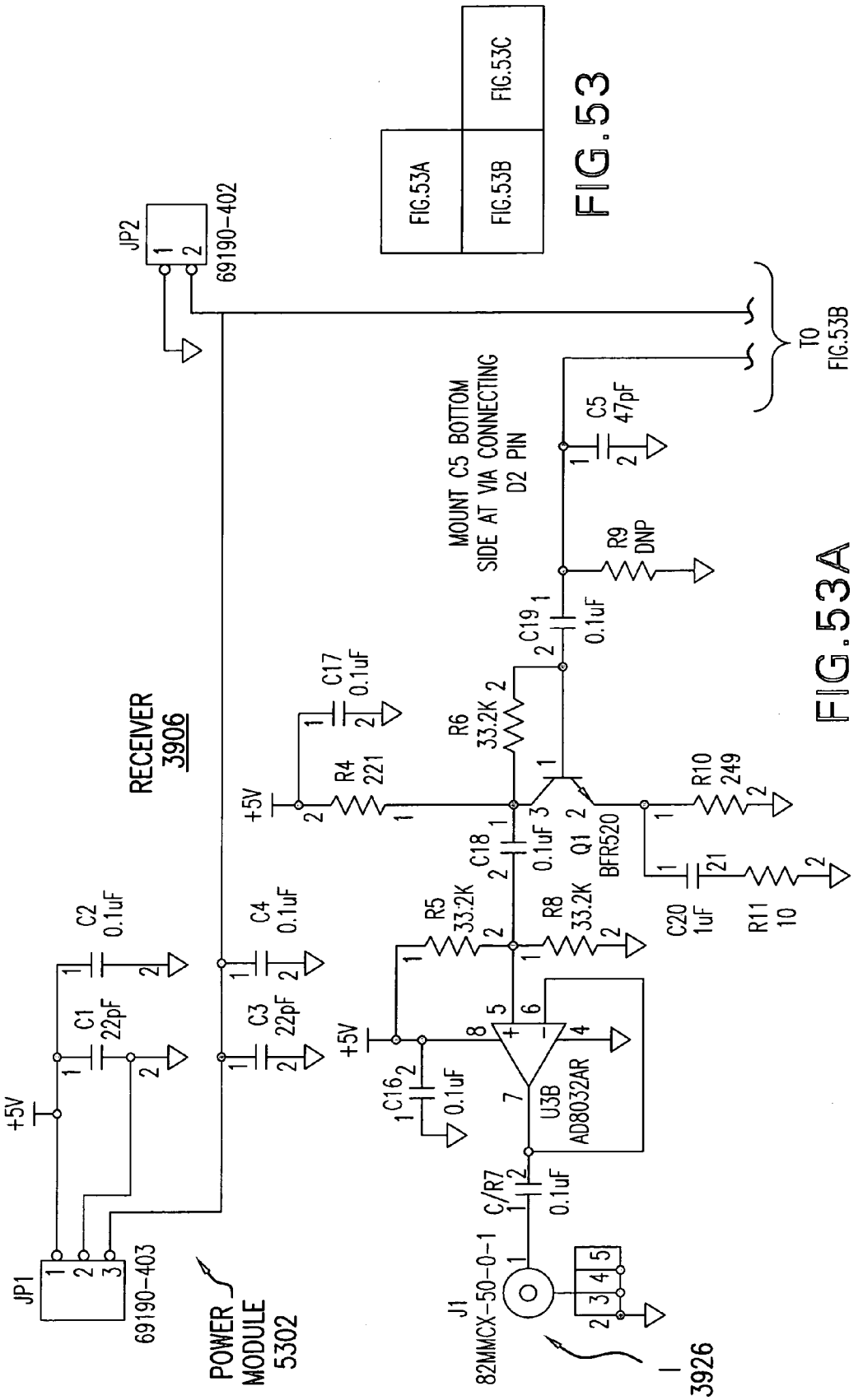
FIG.51B

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	3	C3,C52,C55	4.7uF	T491A475K006AS	KEMET
2	26	C51,C54,C57,C58,C60,C61,	0.1uF	GRM39Y5V104Z016	MURATA
		C67,C68,C69,C77,C79,C80,			
		C81,C83,C89,C90,C91,C111,			
		C112,C113,C114,C115,C116,			
		C117,C118,C119			
3	8	C56,C59,C78,C82,C99,C101,	0.01uF	GRM39X7R103K050	MURATA
		C103,C104			
4	10	C62,C63,C66,C72,C73,C84,	1uf	GRM40Y5V105Z016	MURATA
		C85,C88,C94,C95			
5	4	C64,C75,C86,C97	120pF	GRM39COG121J050	MURATA
6	2	C87,C65	180pF	GRM39COG181J050	MURATA
7	2	C70,C92	390pF	GRM39COG391J050	MURATA
8	2	C71,C93	470pF	GRM39COG471J050	MURATA
9	2	C96,C74	82pF	GRM39COG820J050	MURATA
10	5	C100,C102,C105,C106,C107	100pF	GRM39COG101K050	MURATA
11	1	C108	1uF		
12	1	C110	4.7uF		
13	2	D3,D1	BAW56WT1	BAW56WT1	MOTOROLA
14	2	D4,D2	BAV70LT1	BAV70LT1	MOTOROLA
15	2	JP2,JP1	HEADER 7X2		
16	6	J1,J3,J5,J7,J10,J11	82MMCX	142-0701-231	JOHNSON
17	1	J9	82MMCX	82MMCX-50-0-1	SUHNER
18	1	L1	BLM11A121S	BLM11A121S	MURATA
19	2	L28,L23	2.2uH	LQG21N2R2K10	MURATA
20	2	L24,L29	1uH	LQG21N1R0K10	MURATA
21	2	L30,L25	680nH	LQG21NR68K10	MURATA
22	2	L26,L31	1.8uH	LQG21N1R8K10	MURATA

FIG.52A

23	2	L27,L32	390nH	LQG21NR39K10	MURATA
24	4	Q1,Q5,Q10,Q14	SD404CY	SD404CY	CALOGIC
25	4	Q2,Q4,Q12,Q13	BFM505	BFM505	PHILIPS
26	4	Q3,Q7,Q11,Q16	SD213	SD213	CALOGIC
27	2	Q17,Q8	BFR520	BFR505	PHILIPS
28	5	R19,R20,R21,R171,R173	0		
29	8	R23,R26,R34,R45,R52,R57,	33K	ERJ3GSY333	PANASONIC
		R63,R74			
30	4	R24,R27,R53,R58	475	ERJ3EKF4750	PANASONIC
31	6	R25,R28,R47,R54,R59,R76	402	ERJ3EKF4020	PANASONIC
32	4	R29,R30,R55,R56	221	ERF3EKF2210	PANASONIC
33	2	R32,R61	200	ERJ3GSYJ201	PANASONIC
34	2	R33,R62	33.2K	ERJ3GSYJ333	PANASONIC
35	4	R35,R46,R64,R75	68.1	ERJ3EKF68R1	PANASONIC
36	2	R36,R65	200	ERJ3EKF2000	PANASONIC
37	2	R66,R37	49.9	ERJ3EKF49R9	PANASONIC
38	6	R40,R68,R78,R79,R80,R89	1K	ERJ3EKF1001	PANASONIC
39	2	R42,R71	62	ERJ3GSYJ620	PANASONIC
40	2	R43,R72	162	ERJ3EKF6810	PANASONIC
41	2	R44,R73	49.9	ERJ3EKF1001	PANASONIC
42	2	R77,R48	33	ERJ3GSYJ330	PANASONIC
43	4	R81,R82,R85,R87	2K	ERJ3EKF2001	PANASONIC
44	1	R83	0	ERJGSY0R00	PANASONIC
45	1	R84	1.1K	ERJ3EKF2001	PANASONIC
46	1	R88	15K	ERJ3EKF1502	PANASONIC
47	1	R90	10K	ERJ3EKF1002	PANASONIC
48	2	R91,R92	100	ERJ3EKF1000	PANASONIC
49	6	R164,R165,R166,R167,R168,	TBD		
		R169			
50	2	R170,R172	OPEN		
51	0	TP1,TP2,TP3,TP4,TP5,TP6	TP-105-01-00		
52	2	U42,U6	NC7S04M5		NATIONAL SEMICONDUCTOR
53	1	U7	AD8032AR	AD8032AR	ANALOG DEVICES
54	1	U8	AD1582	AD1582	ANALOG DEVICES
55	1	U9	AD605AR	AD605AR	ANALOG DEVICES
56	1	U43	TK11235AMTL	TK11235AMTL	TOKO

FIG.52B


FIG.53A
FIG.53B
FIG.53C
FIG.53
FIG.53A
JP2
69190-402
TO
FIG.53B
RECEIVER
3906
MOUNT C5 BOTTOM
SIDE AT VIA CONNECTING
D2 PIN
C5
47pF
R9
DNP
C19
0.1uF
C17
0.1uF
R6
33.2K
R4
221
+5V
C18
0.1uF
Q1
BFR520
R10
249
R11
10
C20
1uF
R5
33.2K
R8
33.2K
C2
0.1uF
C4
0.1uF
C1
22pF
C3
22pF
C16
0.1uF
U3B
AD8032AR
C/R7
0.1uF
J1
82MMCX-50-0-1
JP1
69190-403
POWER
MODULE
5302
3926

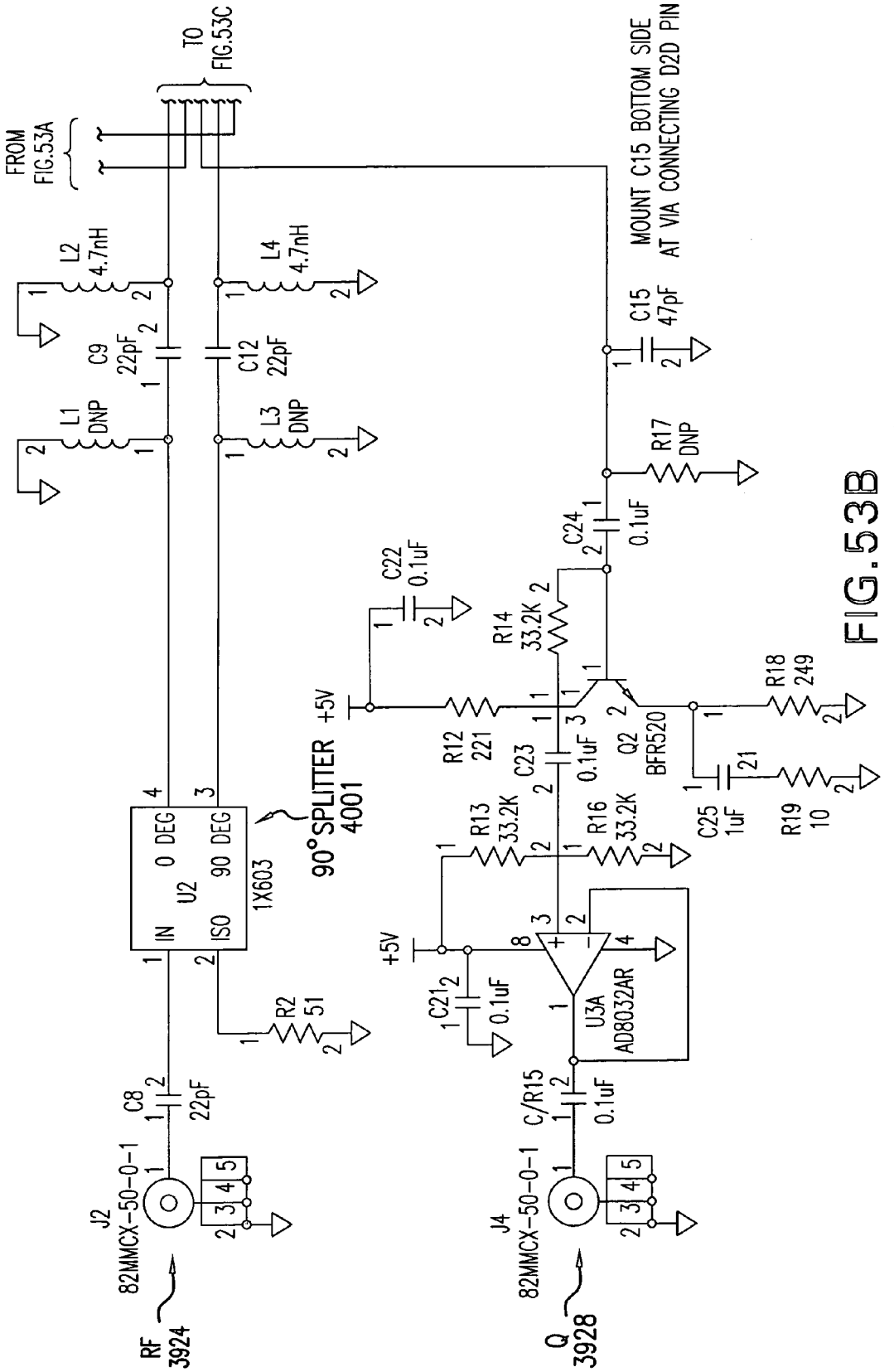

FROM FIG.53A
TO FIG.53C
L2 4.7nH
L4 4.7nH
C9 22pF
C12 22pF
L1 DNP
L3 DNP
C15 47pF
MOUNT C15 BOTTOM SIDE AT VIA CONNECTING D2D PIN
R17 DNP
C24 0.1uF
C22 0.1uF
R14 33.2K
+5V
R12 221
C23 0.1uF
Q2 BFR520
R18 249
R19 10
C25 1uF
90°SPLITTER 4001
U2 1X603
0 DEG
90 DEG
IN
ISO
R13 33.2K
R16 33.2K
C21 0.1uF
U3A AD8032AR
R2 51
C8 22pF
C/R15 0.1uF
J2 82MMCX-50-0-1
J4 82MMCX-50-0-1
RF 3924
Q 3928

FIG.53B

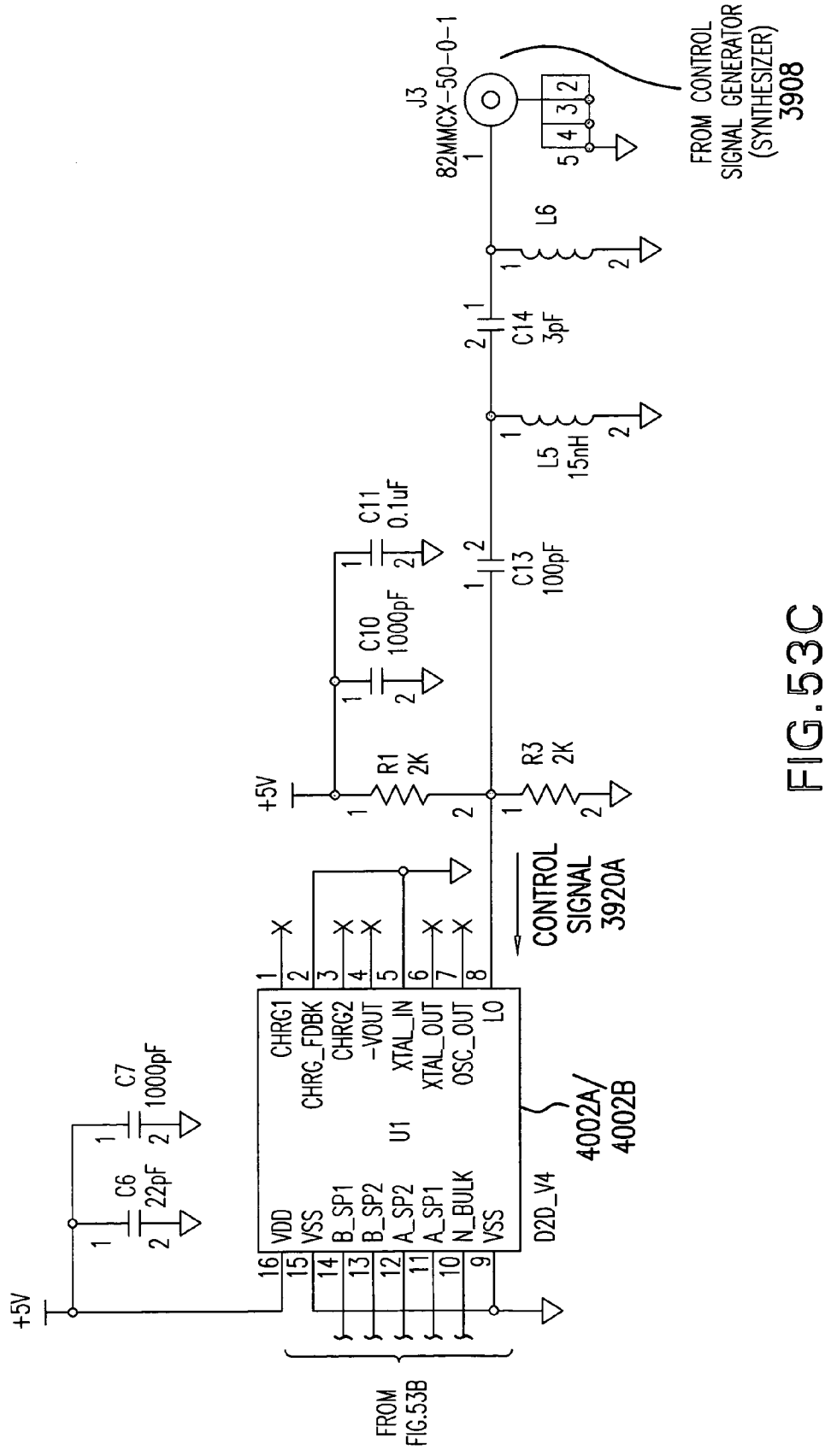

FROM FIG.53B
+5V
C6 22pF
C7 1000pF
U1
VDD
VSS
B_SP1
B_SP2
A_SP2
A_SP1
N_BULK
VSS
D2D_V4
CHRG1
CHRG_FDBK
CHRG2
-VOUT
XTAL_IN
XTAL_OUT
OSC_OUT
LO
4002A/ 4002B
CONTROL SIGNAL 3920A
+5V
R1 2K
R3 2K
C10 1000pF
C11 0.1uF
C13 100pF
L5 15nH
C14 3pF
L6
J3 82MMCX-50-0-1
FROM CONTROL SIGNAL GENERATOR (SYNTHESIZER) 3908

FIG. 53C

ITEM	QTY	REFERENCE	PART	PART NIMBER	MANUFACTURER
1	10	C/R7,C/R15,C16,C17,C18 C19,C21,C22,C23,C24	0.1uF	GRM39Y5V104Z016	MURATA
2	6	C1,C3,C6,C8,C9,C12	22pF	GRM39COG220J050	MURATA
3	3	C2,C4,C11	0.1uF	GRM39X7R104K016	MURATA
4	2	C5,C15	47pF	GRM39COG470J050	MURATA
5	2	C10,C7	1000pF	GRM39X7R102K050	MURATA
6	1	C13	100pF	GRM39X7R101J050	MURATA
7	1	C14	3pF	GRM40COG030B50V	MURATA
8	2	C20,C25	1uF	GRM40Y5V105Z016	MURATA
9	1	JP1	69190-403	69190-403	BERG
10	1	JP2	69190-402	69190-402	BERG
11	4	J1,J2,J3,J4	82MMCX-50-0-1	82MMCX-50-0-1	SUHNER
12	2	L3,L1	DNP	L	TOKO
13	2	L4,L2	4.7nH	LL1608-F4N7K	TOKO
14	1	L5	15nH	LL2012FH15NJ	TOKO
15	1	L6	DNP	DNP	TOKO
16	2	Q1,Q2	BFR520	BFR520	PHILIPS
17	2	R1,R3	2K	ERJ3GSYJ202	PANASONIC
18	1	R2	51	ERJ3GSYJ510	PANASONIC
19	2	R4,R12	221	ERJ3EKF2210	PANASONIC
20	6	R5,R6,R8,R13,R14,R16	33.2K	ERJ3EKF3322	PANASONIC
21	2	R9,R17	DNP	ERJ3EKF1001	PANASONIC
22	2	R10,R18	249	ERJ3EKF2490	PANASONIC
23	2	R11,R19	10	ERJ3GSYJ100	PANASONIC
24	1	U1	D2D_V4	D2D_V4	PARKER VISION
25	1	U2	1X603	1X603	ANAREN
26	1	U3	AD8032AR	AD8032AR	ANALOG DEVICES
27	1		BOARD	STB500.641.001 V03.00	

FIG.54

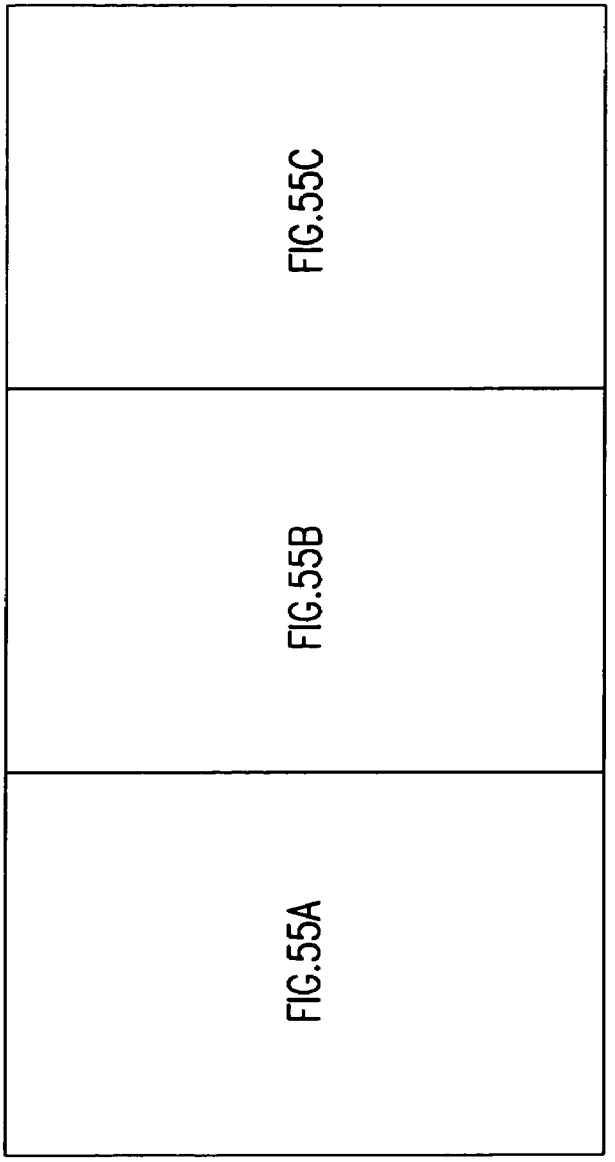


FIG.55

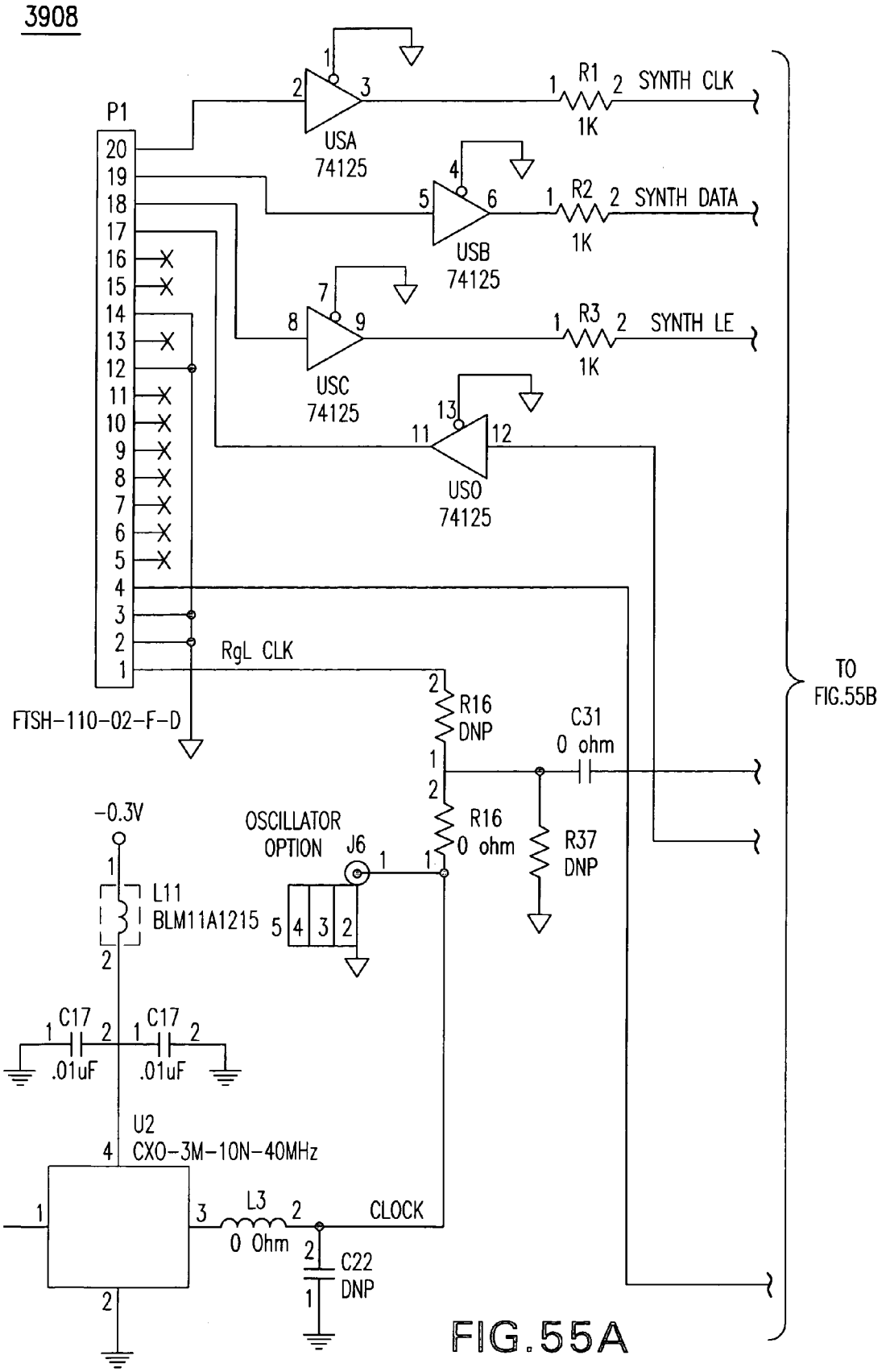

3908
P1
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
FTSH-110-02-F-D
USA
74125
USB
74125
USC
74125
USO
74125
R1
1K
SYNTH CLK
R2
1K
SYNTH DATA
R3
1K
SYNTH LE
RgL CLK
R16
DNP
C31
0 ohm
R16
0 ohm
R37
DNP
OSCILLATOR
OPTION
J6
-0.3V
L11
BLM11A1215
C17
.01uF
C17
.01uF
U2
CXO-3M-10N-40MHz
L3
0 Ohm
CLOCK
C22
DNP
TO
FIG.55B

FIG.55A

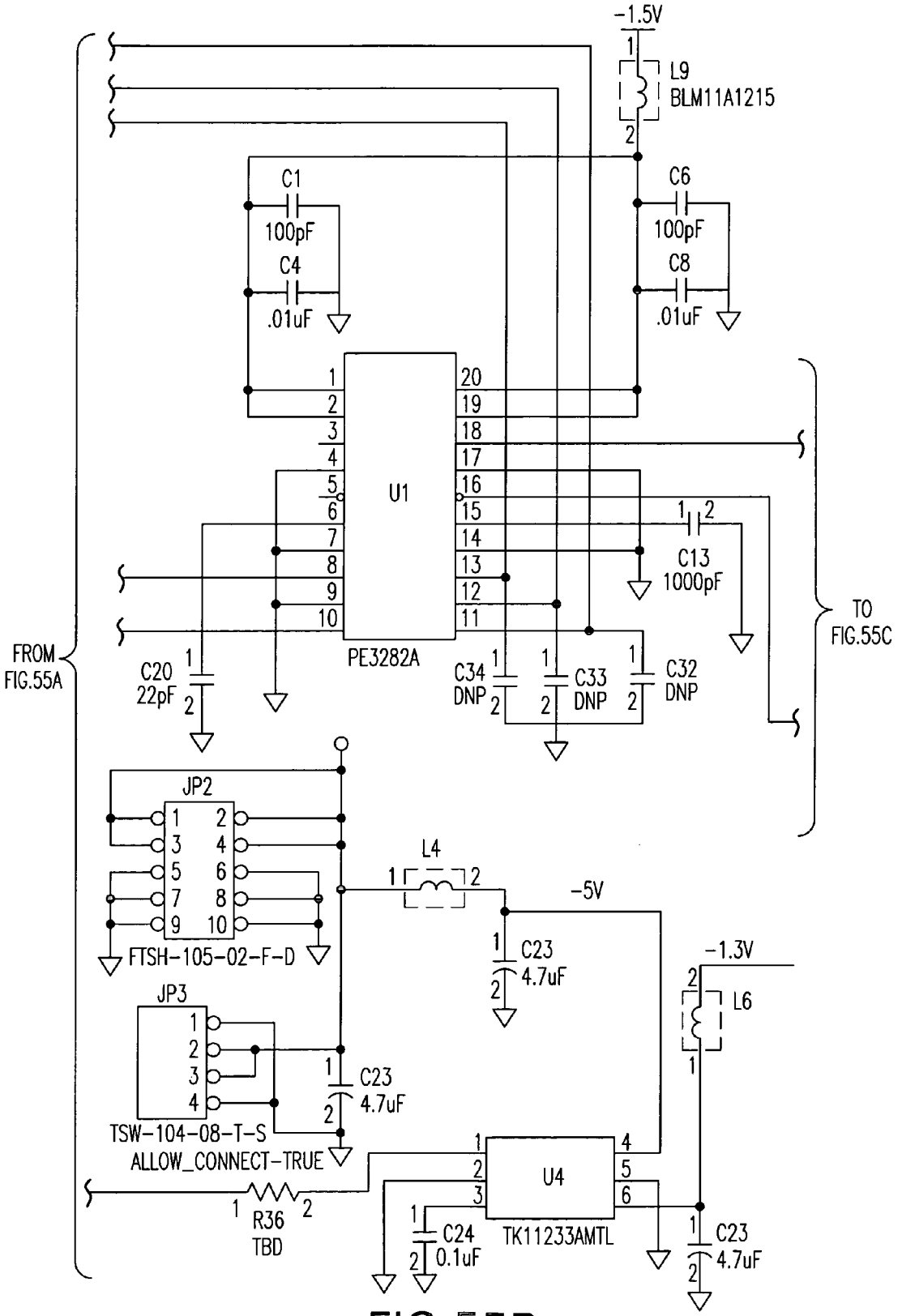

-1.5V
L9
BLM11A1215
C1
100pF
C4
.01uF
C6
100pF
C8
.01uF
U1
PE3282A
C13
1000pF
C20
22pF
C34
DNP
C33
DNP
C32
DNP
FROM
FIG.55A
TO
FIG.55C
JP2
FTSH-105-02-F-D
L4
-5V
C23
4.7uF
-1.3V
L6
JP3
TSW-104-08-T-S
ALLOW_CONNECT-TRUE
C23
4.7uF
U4
TK11233AMTL
R36
TBD
C24
0.1uF
C23
4.7uF

FIG.55B

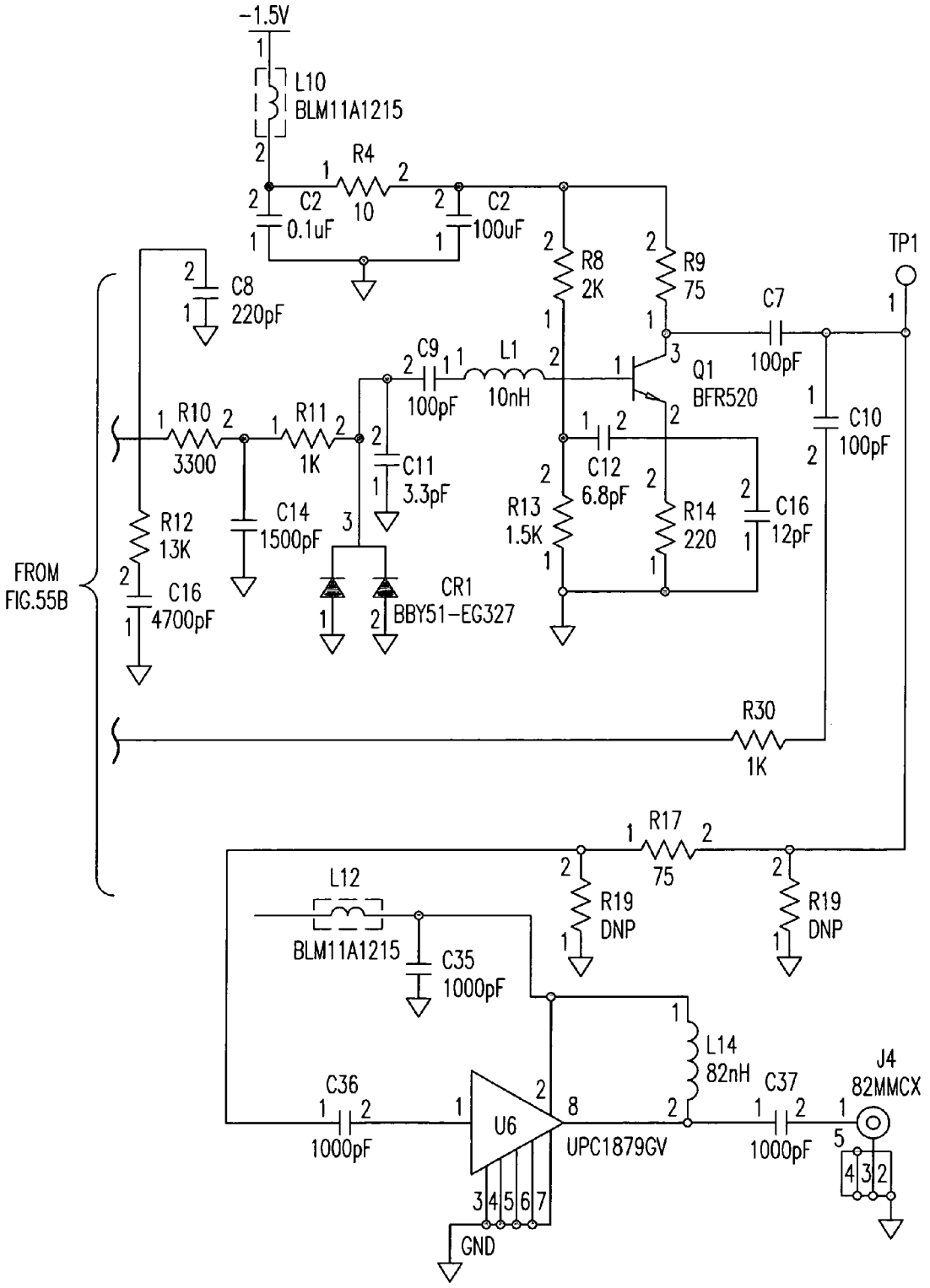

-1.5V
L10
BLM11A1215
R4
10
C2
0.1uF
C2
100uF
R8
2K
R9
75
TP1
C7
100pF
C8
220pF
C9
100pF
L1
10nH
Q1
BFR520
C10
100pF
R10
3300
R11
1K
C11
3.3pF
C12
6.8pF
R13
1.5K
R14
220
C16
12pF
R12
13K
C14
1500pF
C16
4700pF
CR1
BBY51-EG327
FROM
FIG.55B
R30
1K
R17
75
L12
BLM11A1215
C35
1000pF
R19
DNP
R19
DNP
L14
82nH
J4
82MMCX
C36
1000pF
U6
UPC1879GV
C37
1000pF
GND

FIG.55C

ITEM	QTY	REFERENCE	PART	DESCRIPTION	PART NUMBER	MANUFACT.
1	1	CR1	BBY51-E6327	DIODE,VARACTOR	BBY51-E6327	SIEMENS
2	6	C1,C3,C5,C7,C9,C10	100pF	CAPACITOR,CERAMIC,100pF,10%,COG,0603	GRM39COG101K050	MURATA
3	2	C29,C2	0.1uF	CAPACITOR,CERAMIC,.1uF,10%,X7R,0603	GRM39X7R104K016AD	MURATA
4	3	C4,C8,C17	.01uF	CAPACITOR,CERAMIC,.01uF,10%,X7R,0603	GRM39X7R103K050	MURATA
5	1	C6	220pF	CAPACITOR,CERAMIC,220pF,5%,COG,0603	GRM39COG221J025	MURATA
6	1	C11	3.3pF	CAPACITOR,CERAMIC,3.3pF,5%,COG,0603	GRM39COG3R3B100V	MURATA
7	1	C12	6.8pF	CAPACITOR,CERAMIC,6.8pF,+/-.25pF,COG,0603	GRM39COG6R8C100V	MURATA
8	4	C13,C35,C36,C37	1000pF	CAPACITOR,CERAMIC,1000pF,10%,X7R,0603	GRM39X7R102K016	MURATA
9	1	C14	1500pF	CAPACITOR,CERAMIC,1500Pf,10%,X7R,0603	GRM39X7R152K016	MURATA
10	1	C15	12pF	CAPACITOR,CERAMIC,12pF,5%,COG,0603	GRM39COG150J050	MURATA
11	1	C16	4700pF	CAPACITOR,CERAMIC,4700pF,10%,0603	GRM39X7R472K016	MURATA
12	2	C20,C18	22pF	CAPACITOR,CERAMIC,22pF,10%,COG,0603	GRM36COG220K050	MURATA
13	4	C22,C32,C33,C34	DNP	CAPACITOR,CERAMIC,,,,,0603		MURATA
14	3	C23,C24,C27	4.7uF	CAPACITOR,TANTALUM,4.7uF,10%,3216	T491A475K006AS	KEMET
15	3	R16,C31,R17	0 OHM	RESISTOR,ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
16	1	JP1	FTSH-110-02-F-D	HEADER,DUAL ROW 10X2,.050X.050	FTSH-110-02-F-D	SAMTEC
17	1	JP2	FTSH-105-02-F-D	HEADER,DUAL ROW 5X2,.050X.050	FTSH-105-02-F-D	SAMTEC
18	1	JP3	TSW-104-08-T-S	HEADER, SINGLE ROW 4 PIN, .100"	TSW-104-08-T-S	BERG
19	2	J5,J6	82MMCX	RF CONNECTOR	82MMCX-50-0-1	SUHNER
20	1	L1	18nH	INDUCTOR,18nH,10%, 0805	0805CS-180XJBC	COILCRAFT
21	1	L3	0 OHM	ZERO OHM JUMPER	RM73Z1JT	KOA
22	6	L4,L6,L9,L10,L11,L12	BLM11A121S	FERRITE BEAD, 0603	BLM11A121S	MURATA
23	1	L14	82nH	INDUCTOR, 82nH,10%,0805	LL2012-F82NK	TOKO
24	1	Q1	BFR520	TRANSISTOR, NPN	BFR520	PHILIPS
25	5	R1,R2,R3,R11,R30	1K	RESISTOR, 1K,5%,0603	ERF3GSYJ102	PANASONIC
26	1	R4	10	RESISTOR, 10 OHM,5%,0603	ERJ3GSYJ1R0	PANASONIC

FIG.56A

27	1	R8	2K	RESISTOR, 2K,5%,0603	ERJ3GSYJ202	PANASONIC
28	1	R9	75	RESISTOR, 75 OHM,5%,0603	ERJ3GSYJ750	PANASONIC
29	1	R10	3300	RESISTOR, 3.3K,5%,0603	ERJ3GSYJ332	PANASONIC
30	1	R12	13K	RESISTOR, 13K,5%,0603	ERJ3GSYJ133	PANASONIC
31	1	R13	1.5K	RESISTOR, 1.5K,5%,0603	ERJ3GSYJ152	PANASONIC
32	1	R14	220	RESISTOR, 220 OHM,5%,0603	ERJ3GSYJ221	PANASONIC
33	1	R15	DNP	RESISTOR, ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
34	2	R18,R19	DNP	RESISTOR, 91 OHM,5%,0603	ERJ3GSYJ910	PANASONIC
35	1	R36	TBD	RESISTOR, ZERO OHM,0603	ERJ3GSY0R00	PANASONIC
36	1	R37	DNP	RESISTOR,,,0603		PANASONIC
37	1	TP1	TEST POINT			
38	1	U1	PE3282A	IC,SYNTHESIZER	PE3282A	PEREGRINE
39	1	U2	CXO-3M-10N-40MHz	XTAL OSC,40MHz	CXO-3M-10N-40MHZ A/I	STATEK
40	1	U4	TK11233AMTL	VOLTAGE REGULATOR,3.5V	TK11235BM	TOKO
41	1	U5	74125	IC,BUFFER	MC74LCX125DT	MOTOROLA
42	1	U6	UPC1678GV	IC,RF AMPLIFIER	UPC1678GV	NEC
43	1		STB500.641.008 V02.00	BOARD		

FIG.56B

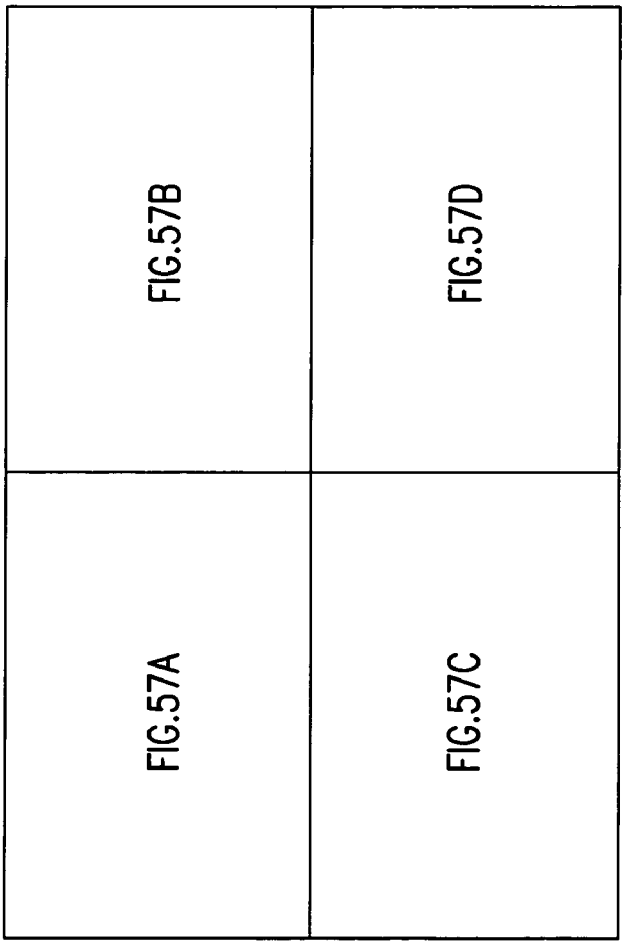


FIG.57

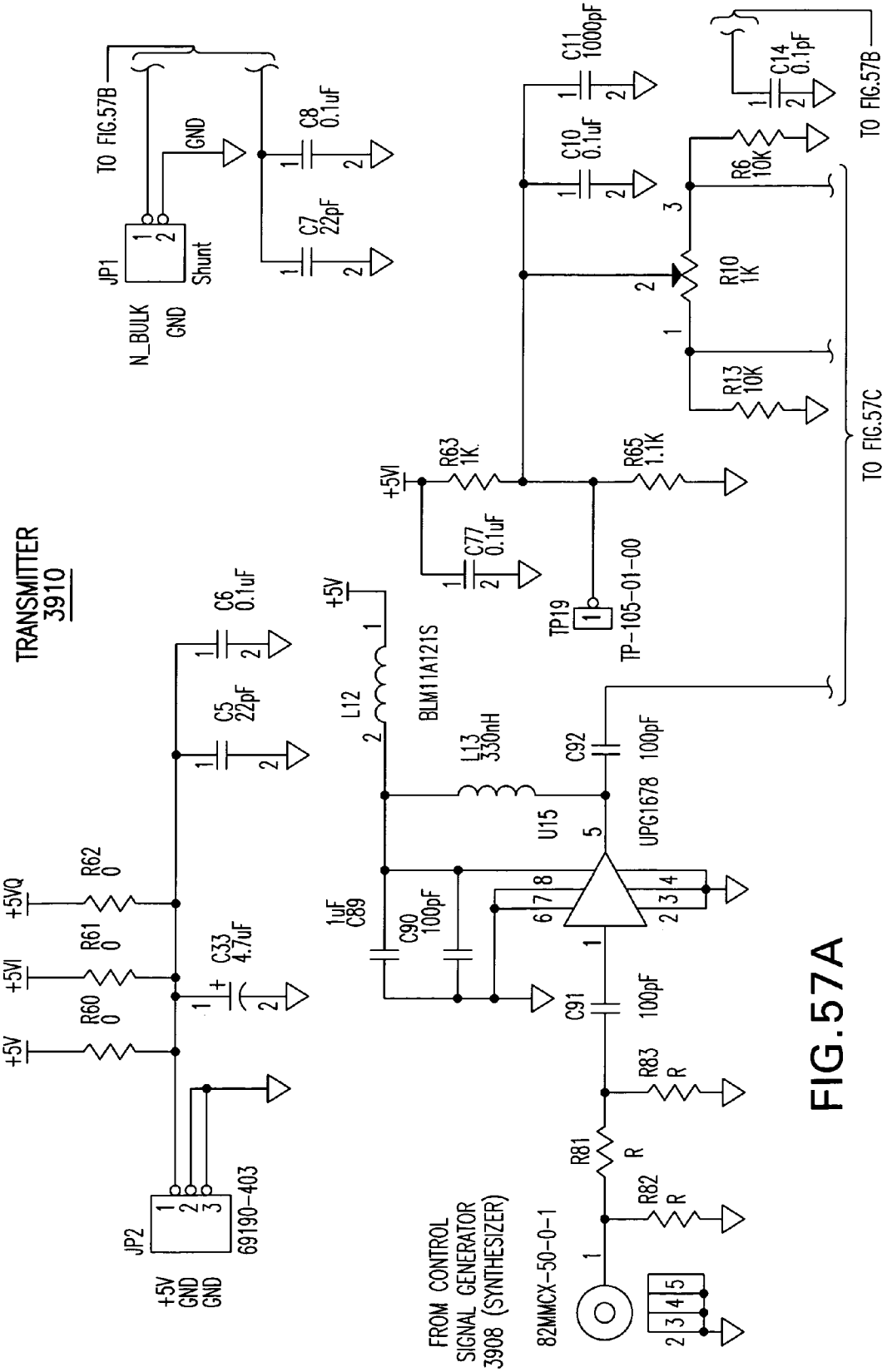

TRANSMITTER
3910
TO FIG.57B
GND
JP1
Shunt
N_BULK
GND
C8
0.1uF
C7
22pF
C11
1000pF
C10
0.1uF
C14
0.1pF
R6
10K
R10
1K
R13
10K
TO FIG.57B
TO FIG.57C
R63
1K
R65
1.1K
+5VI
C77
0.1uF
TP19
TP-105-01-00
+5V
L12
BLM11A121S
L13
330nH
C92
100pF
U15
UPG1678
C6
0.1uF
C5
22pF
C33
4.7uF
R62
0
R61
0
R60
0
+5VQ
+5VI
+5V
1uF
C89
C90
100pF
C91
100pF
R83
R
R81
R
R82
R
JP2
+5V
GND
GND
69190-403
FROM CONTROL
SIGNAL GENERATOR
3908 (SYNTHESIZER)
82MMCX-50-0-1

FIG.57A

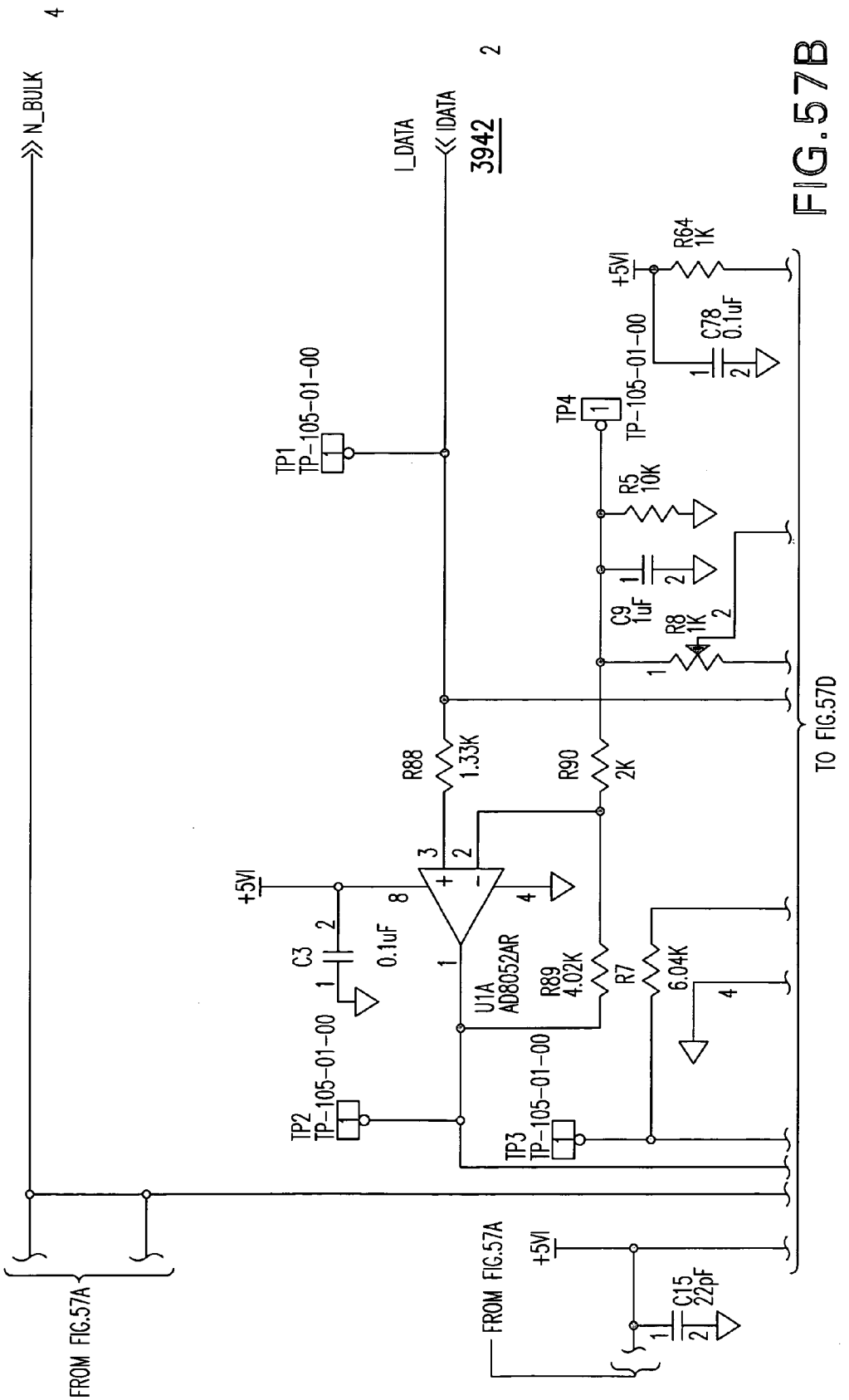

N_BULK
I_DATA
IDATA
3942
TP1
TP-105-01-00
TP2
TP-105-01-00
TP3
TP-105-01-00
TP4
TP-105-01-00
+5VI
C3
0.1uF
U1A
AD8052AR
R88
1.33K
R90
2K
R89
4.02K
R7
6.04K
R5
10K
R8
1K
C9
1uF
R64
1K
C78
0.1uF
C15
22pF
FROM FIG.57A
FROM FIG.57A
TO FIG.57D

FIG. 57B

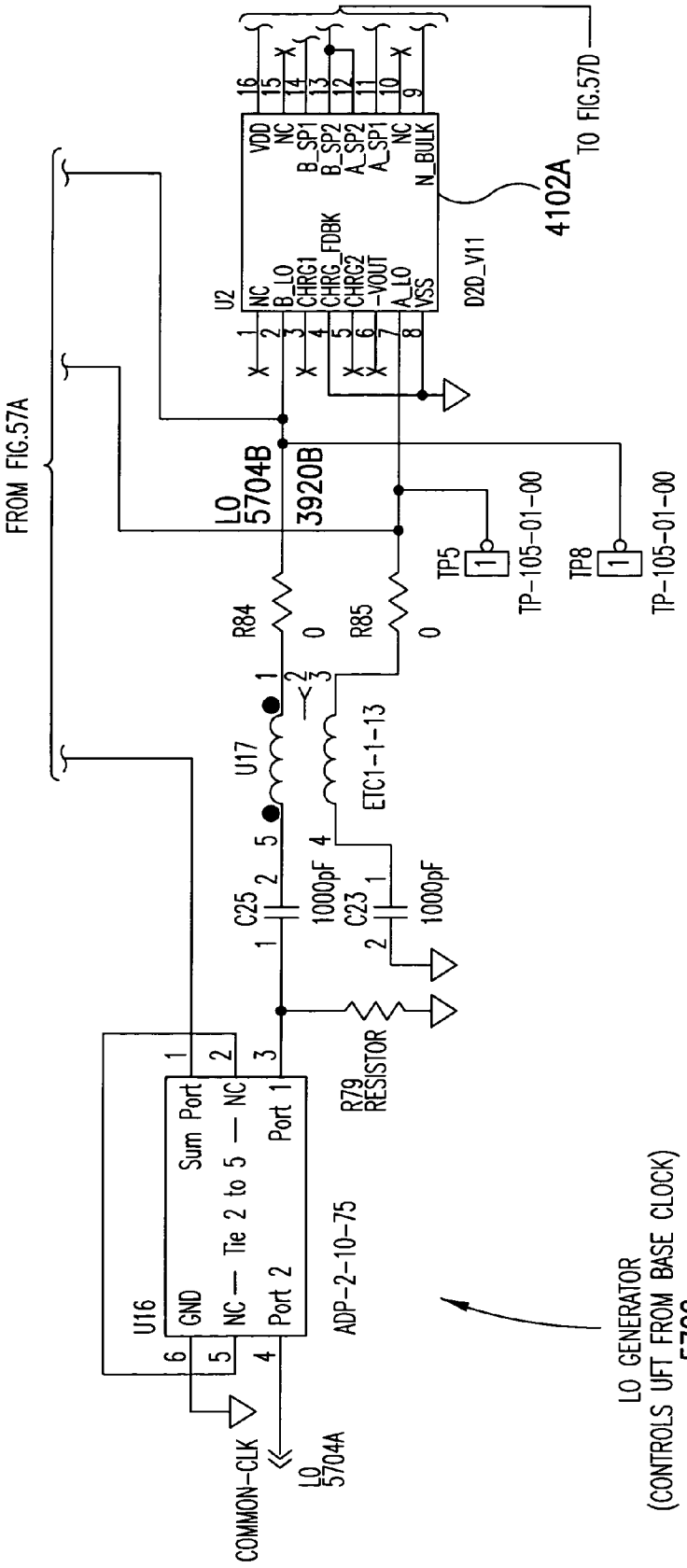

FROM FIG.57A
U2
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP2
A_SP1
NC
N_BULK
D2D_V11
4102A
TO FIG.57D
LO
5704B
3920B
R84
R85
0
0
TP5
TP8
TP-105-01-00
TP-105-01-00
U17
ETC1-1-13
C25
C23
1000pF
1000pF
R79
RESISTOR
U16
GND
NC — Tie 2 to 5 — NC
Port 2
Sum Port
Port 1
ADP-2-10-75
COMMON-CLK
LO
5704A
LO GENERATOR
(CONTROLS UFT FROM BASE CLOCK)
5702

FIG.57C

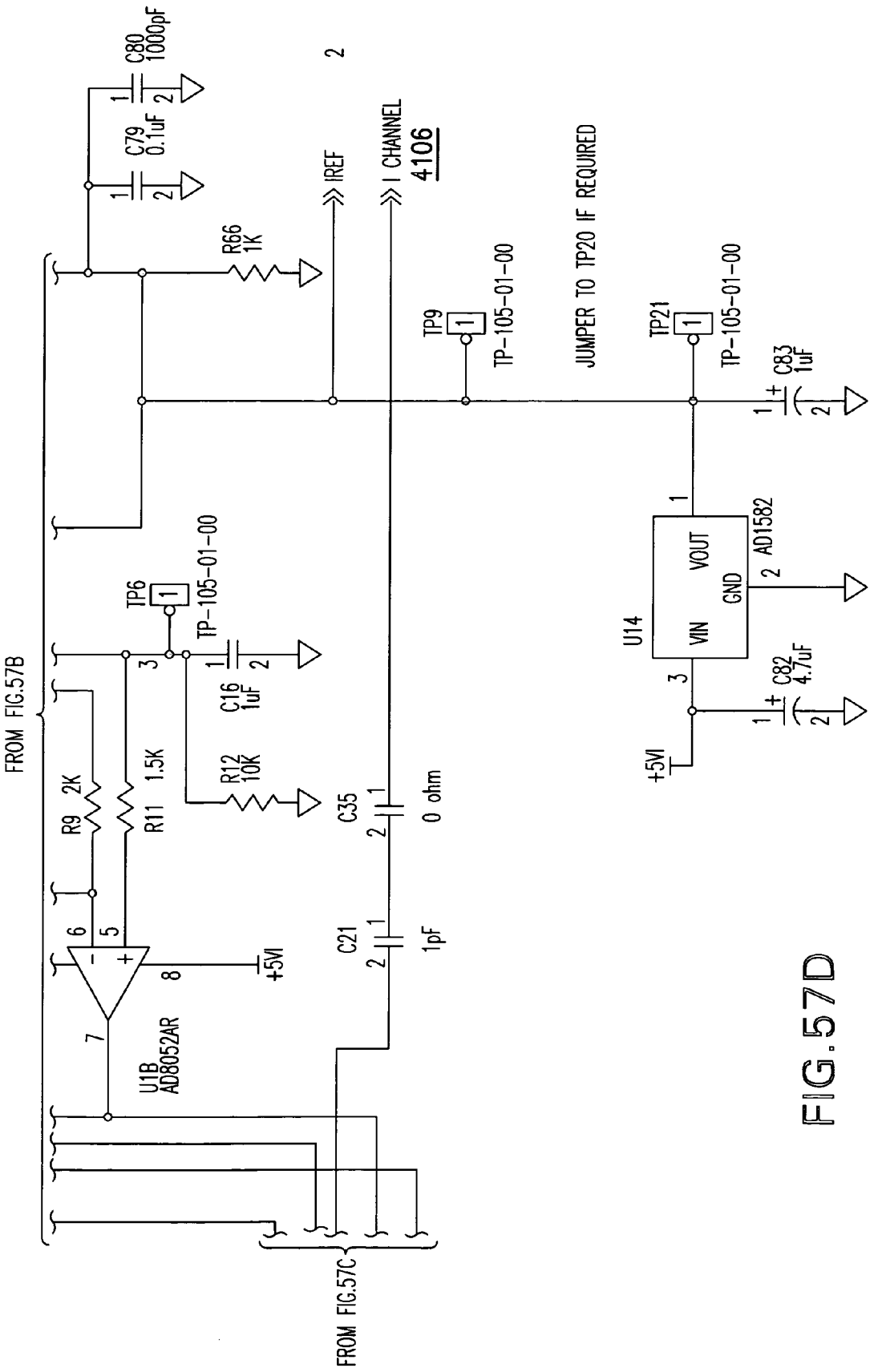

C80 1000pF
C79 0.1uF
R66 1K
IREF
I CHANNEL
4106
TP9
TP-105-01-00
JUMPER TO TP20 IF REQUIRED
TP21
TP-105-01-00
C83 1uF
U14
VIN
VOUT
GND
AD1582
C82 4.7uF
+5VI
TP6
TP-105-01-00
C16 1uF
R12 10K
R9 2K
R11 1.5K
C35
0 ohm
C21
1pF
U1B AD8052AR
FROM FIG.57B
FROM FIG.57C

FIG.57D

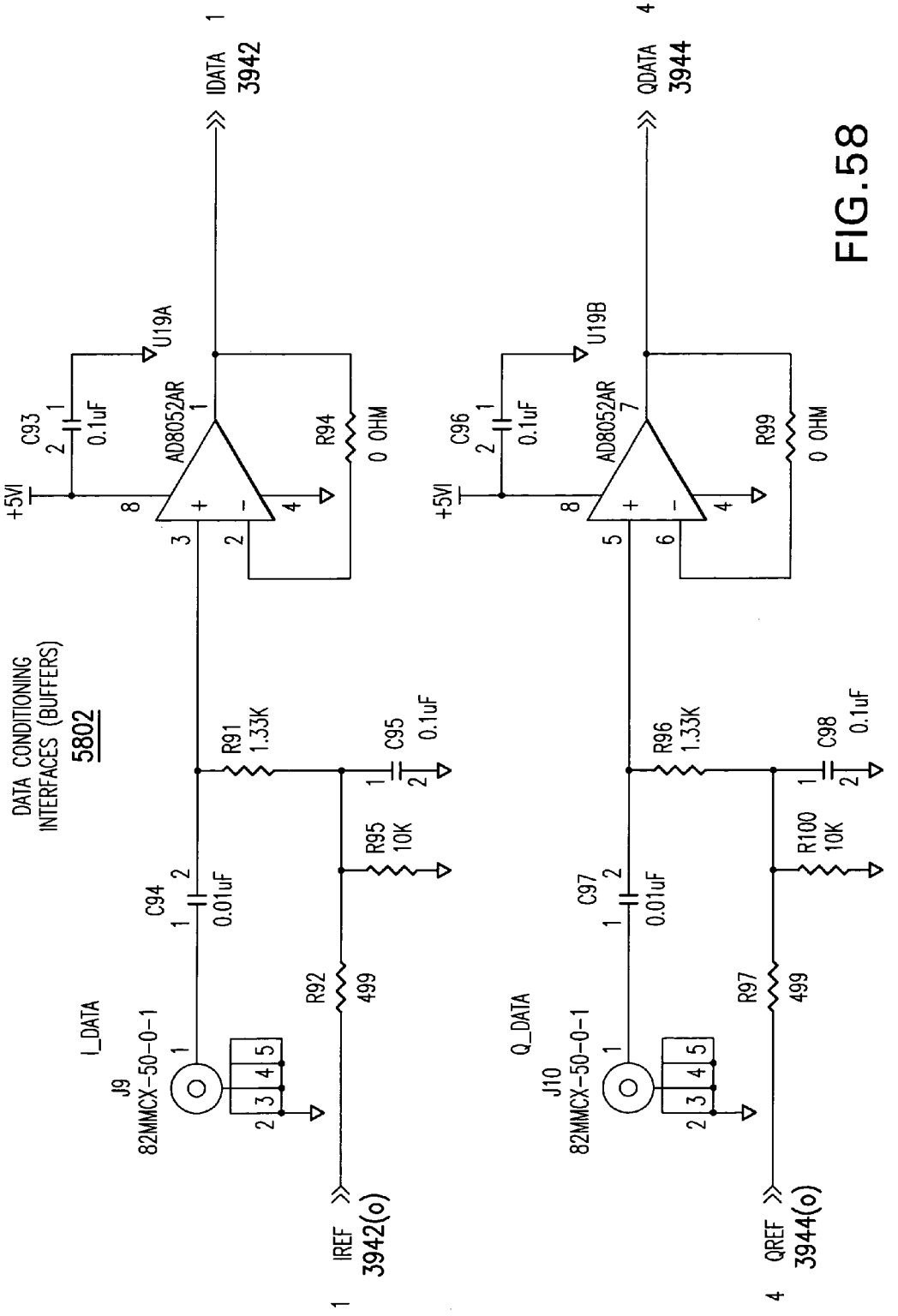

DATA CONDITIONING
INTERFACES (BUFFERS)
5802
I_DATA
J9
82MMCX-50-0-1
C94
0.01uF
R91
1.33K
C95
0.1uF
R95
10K
R92
499
IREF
3942(o)
U19A
AD8052AR
C93
0.1uF
+5VI
R94
0 OHM
IDATA
3942
Q_DATA
J10
82MMCX-50-0-1
C97
0.01uF
R96
1.33K
C98
0.1uF
R100
10K
R97
499
QREF
3944(o)
U19B
AD8052AR
C96
0.1uF
+5VI
R99
0 OHM
QDATA
3944

FIG.58

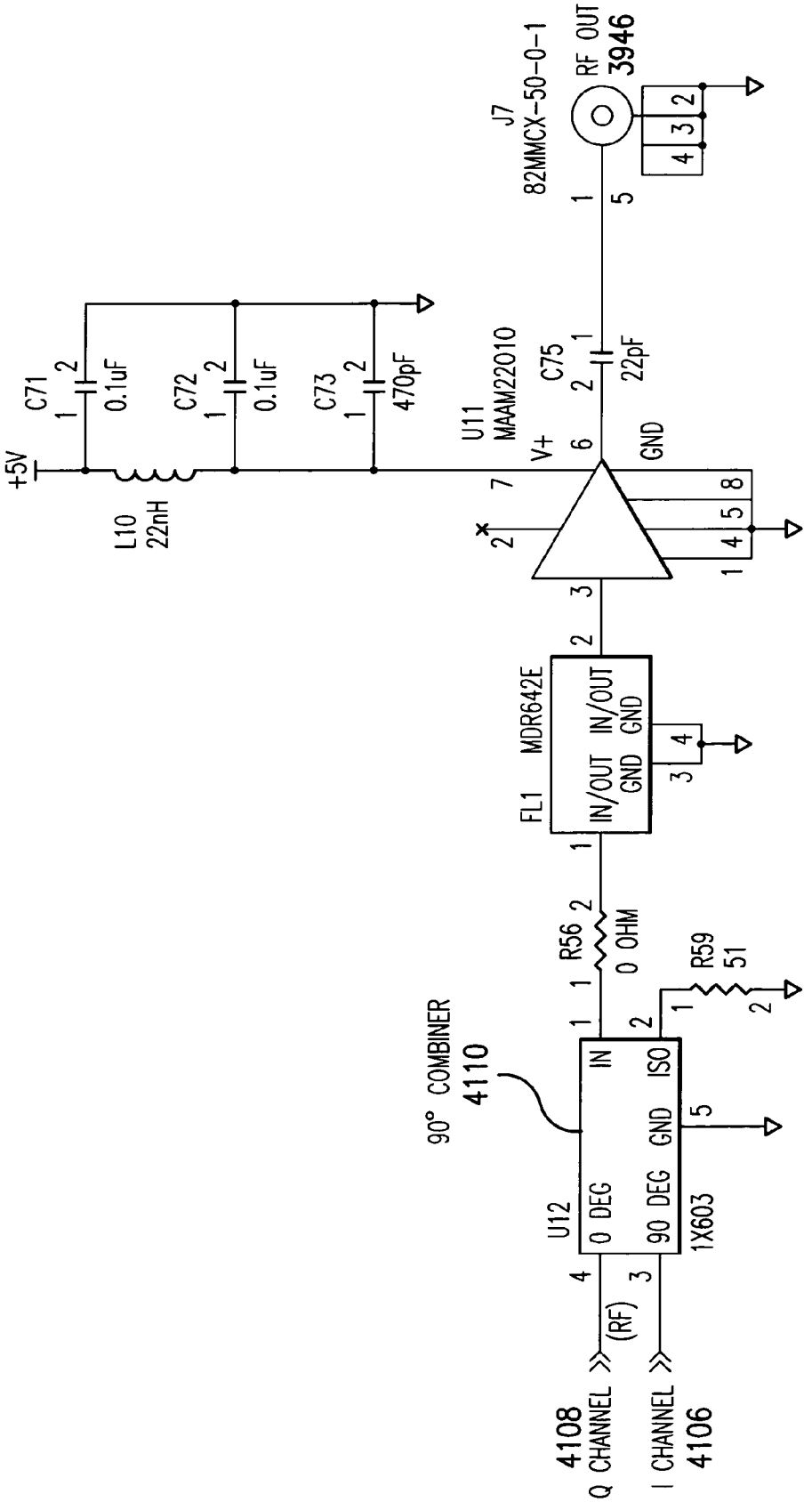

J7
82MMCX-50-0-1
RF OUT
3946
C71
0.1uF
C72
0.1uF
C73
470pF
+5V
L10
22nH
U11
MAAM22010
V+
GND
C75
22pF
FL1
MDR642E
IN/OUT
GND
R56
0 OHM
R59
51
90° COMBINER
4110
IN
ISO
GND
U12
0 DEG
90 DEG
1X603
(RF)
4108
Q CHANNEL
I CHANNEL
4106

FIG.59

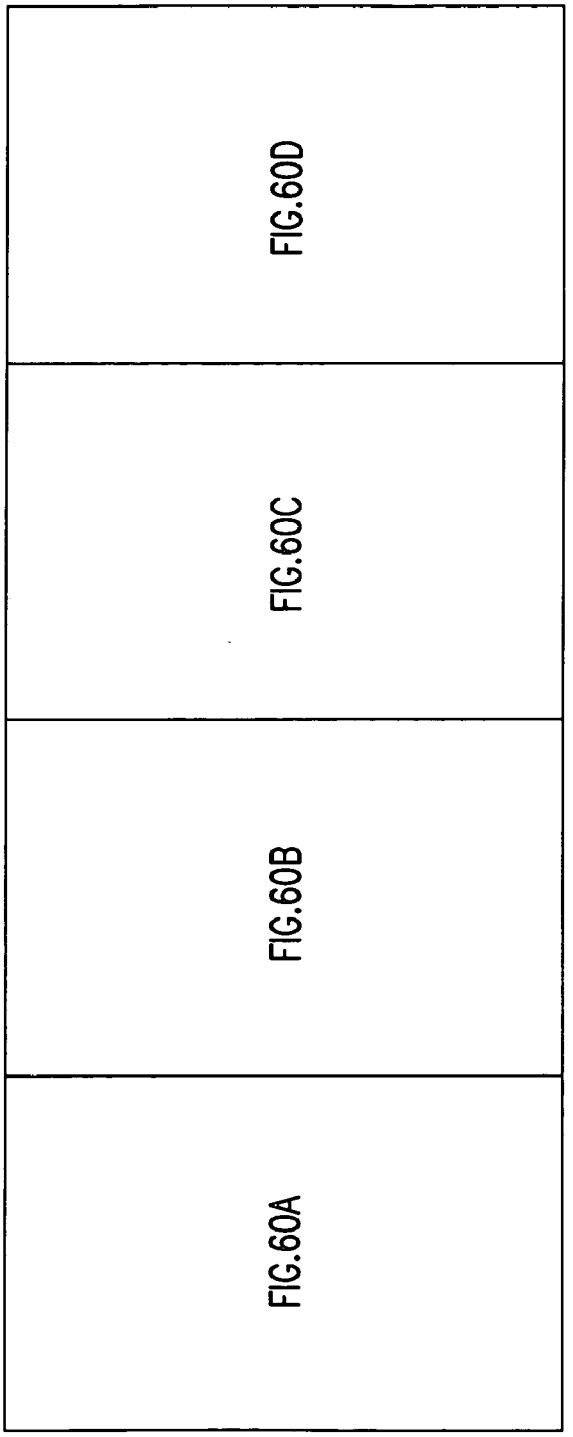


FIG.60

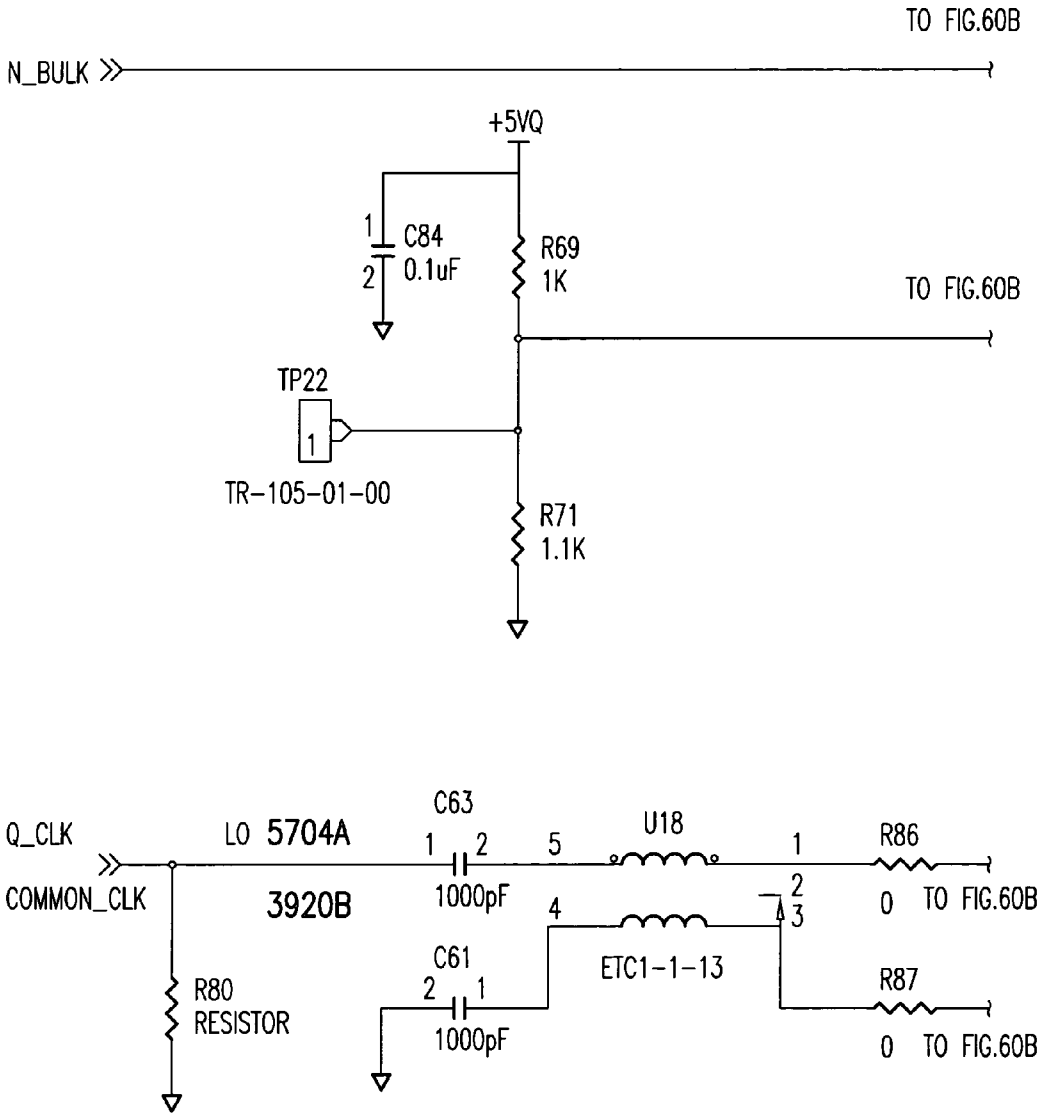

TO FIG.60B
N_BULK
+5VQ
C84
0.1uF
R69
1K
TO FIG.60B
TP22
TR-105-01-00
R71
1.1K
Q_CLK
COMMON_CLK
LO 5704A
3920B
C63
1000pF
U18
R86
0 TO FIG.60B
ETC1-1-13
C61
1000pF
R80
RESISTOR
R87
0 TO FIG.60B

FIG.60A

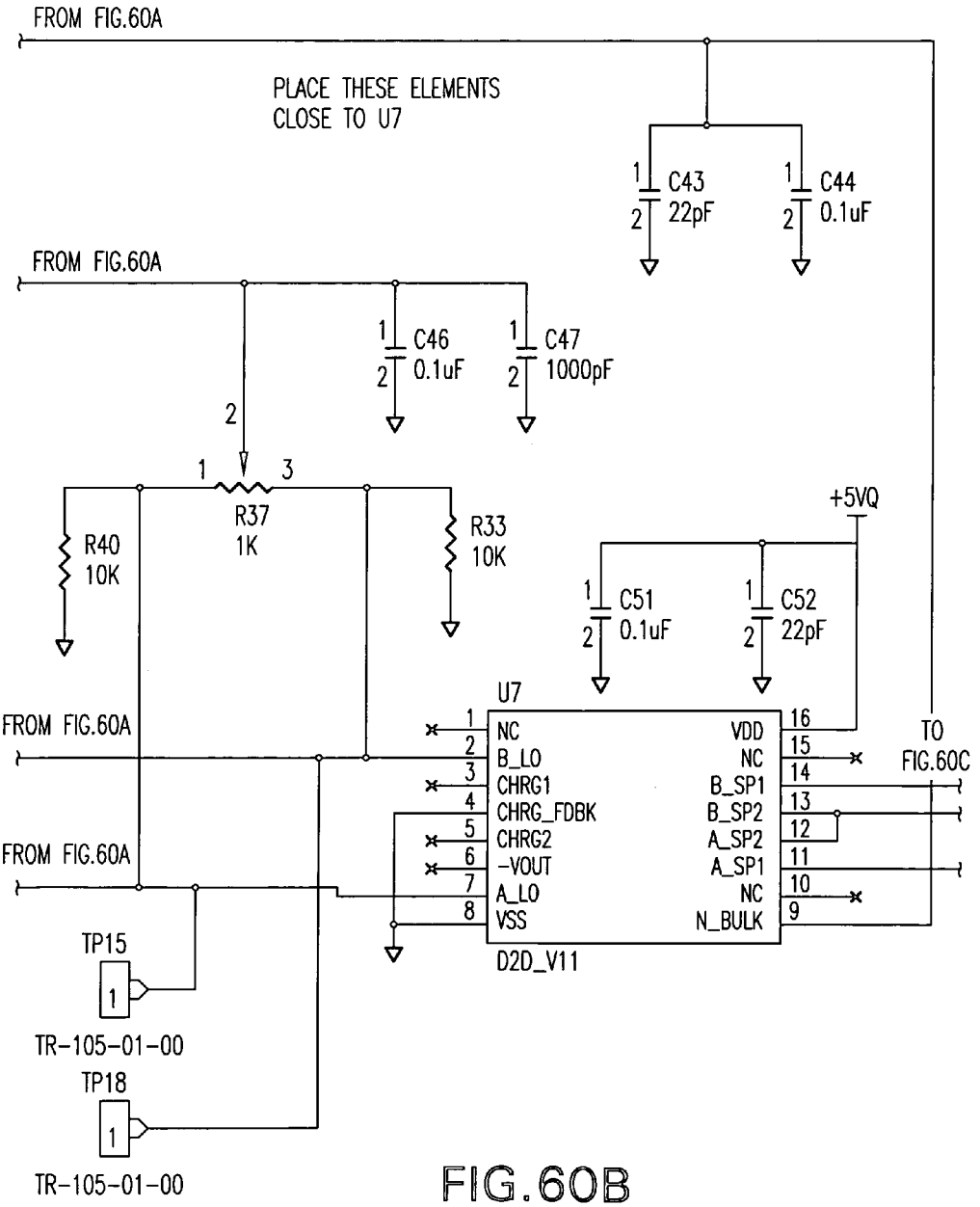

FROM FIG.60A
PLACE THESE ELEMENTS
CLOSE TO U7
C43
22pF
C44
0.1uF
FROM FIG.60A
C46
0.1uF
C47
1000pF
R37
1K
R40
10K
R33
10K
+5VQ
C51
0.1uF
C52
22pF
U7
FROM FIG.60A
FROM FIG.60A
NC
B_LO
CHRG1
CHRG_FDBK
CHRG2
-VOUT
A_LO
VSS
VDD
NC
B_SP1
B_SP2
A_SP2
A_SP1
NC
N_BULK
D2D_V11
TO
FIG.60C
TP15
TR-105-01-00
TP18
TR-105-01-00

FIG.60B

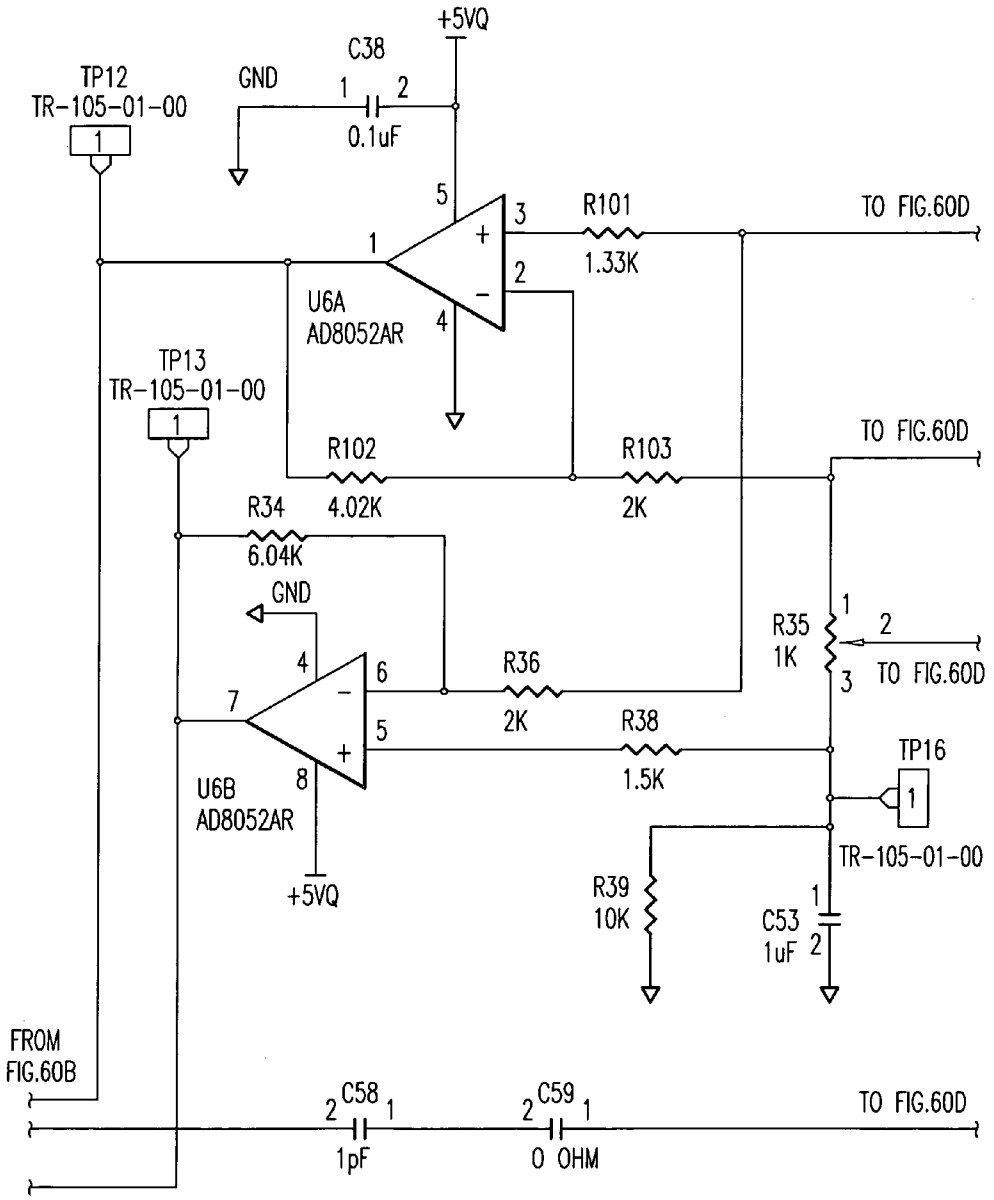

+5VQ
C38
TP12
TR-105-01-00
GND
1
2
0.1uF
5
3
R101
TO FIG.60D
1
+
1.33K
2
−
U6A
AD8052AR
4
TP13
TR-105-01-00
TO FIG.60D
R102
R103
R34
4.02K
2K
6.04K
GND
1
R35
2
1K
3
TO FIG.60D
4
6
R36
7
−
2K
R38
5
+
1.5K
TP16
8
U6B
AD8052AR
1
TR-105-01-00
+5VQ
R39
10K
1
C53
1uF
2
FROM
FIG.60B
2
C58
1
2
C59
1
TO FIG.60D
1pF
0 OHM

FIG.60C

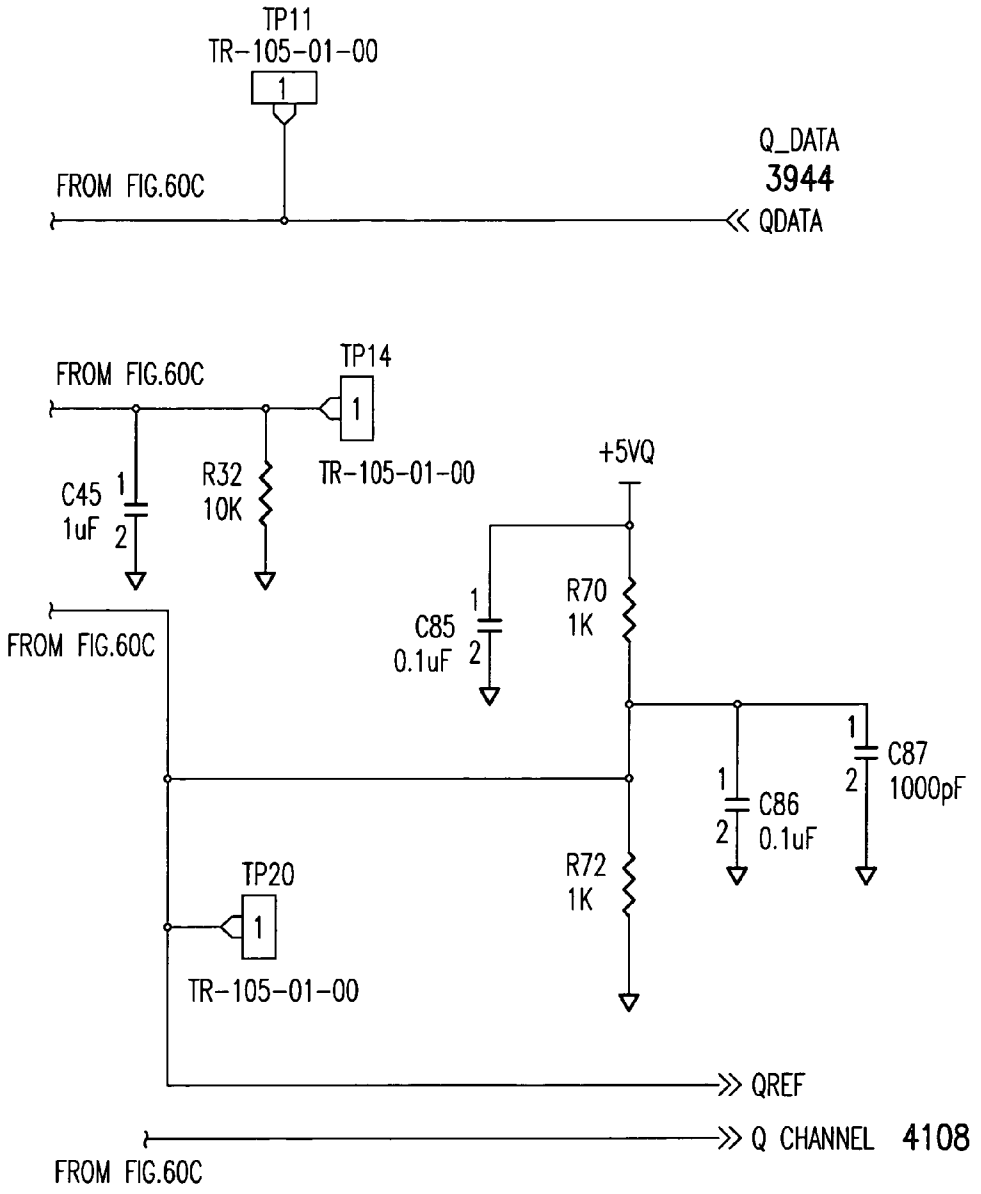

TP11
TR-105-01-00
1
Q_DATA
3944
FROM FIG.60C
QDATA
FROM FIG.60C
TP14
1
TR-105-01-00
C45
1uF
R32
10K
+5VQ
C85
0.1uF
R70
1K
FROM FIG.60C
C87
1000pF
C86
0.1uF
R72
1K
TP20
TR-105-01-00
QREF
Q CHANNEL
4108
FROM FIG.60C

FIG.60D

ITEM	QTY	REFERENCE	PART	PART NUMBER	MANUFACTURER
1	21	C3,C6,C8,C10,C14,C38,C44, C46,C51,C71,C72,C77,C78, C79,C84,C85,C86,C93,C95, C96,C98	0.1uF	GRM39X7R104K016	MURATA
2	6	C5,C7,C15,C43,C52,C75	22pF	GRM39COG220J050	MURATA
3	5	C9,C16,C45,C53,C89	1uF	GRM40Y5V105Z016	MURATA
4	8	C11,C23,C25,C47,C61,C63 C80,C87	1000pF	GRM39X7R102K050	MURATA
5	2	C58,C21	1pF	GRM39COG010B50V	MURATA
6	2	C82,C33	4.7uF	T491A475K006AS	KEMET
7	2	C59,C35	0 ohm	GRM39COGxxxx50V	MURATA
8	1	C73	470pF	GRM39COG471J050	MURATA
9	1	C83	1uF	T491A105M016AS	KEMET
10	3	C90,C91,C92	100pF	ECU-V1H101JCV	
11	2	C94,C97	0.01uF	GRM39X7R103K016	MURATA
12	1	FL1	MDR642E	MDR642E	SOSHIN
13	1	JP1	Shunt	69190-402	BERG
14	1	JP2	69190-403	69190-403	BERG
15	4	J7,J8,J9,J10	82MMCX-50-0-1	82MMCX-50-0-1	SUHNER
16	1	L10	22nH	LL1608-F22NK	COILCRAFT
17	1	L12	BLM11A121S	BLM11A121S	MURATA
18	1	L13	330nH	LL2012-FR33K	
19	10	R5,R6,R12,R13,R32,R33, R39,R40,R95,R100	10K	ERJ3EKF1002	PANASONIC
20	2	R34,R7	6.04K	ERJ3EKF6041	PANASONIC
21	4	R8,R10,R35,R37	1K	3224W-1-102	BOURNS
22	4	R9,R36,R90,R103	2K	ERJ3EKF2001	PANASONIC
23	2	R38,R11	1.5K	ERJ3EKF1501	PANASONIC
24	3	R56,R94,R99	0 ohm	ERJ3GSY0R00	PANASONIC

FIG.61A

25	1	R59	51	ERJ3GSYJ510	PANASONIC
26	7	R60,R61,R62,R84,R85,R86,	0	ERJ3GSY0R00	PANASONIC
		R87			
27	6	R63,R64,R66,R69,R70,R72	1K	ERJ3EKF1001	PANASONIC
28	2	R71,R65	1.1K	ERJ3EKF1101	PANASONIC
29	2	R80,R79	RESISTOR		
30	3	R81,R82,R83	R		
31	4	R88,R91,R96,R101	1.33K	ERJ3EKF1331	PANASONIC
32	2	R102,R89	4.02K	ERJ3EKF4021	PANASONIC
33	2	R92,R97	499	ERJ3EKF4990	PANASONIC
34	19	TP1,TP2,TP3,TP4,TP5,TP6,	TP-105-01-00		
		TP8,TP9,TP11,TP12,TP13,			
		TP14,TP15,TP16,TP18,TP19,			
		TP20,TP21,TP22			
35	3	U1,U6,U19	AD8052AR	AD8052AR	ANALOG DEVICES
36	2	U7,U2	D2D_V11	D2D_V11	PARKER VISION
37	1	U11	MAAM22010	MAAM22010	MACOM
38	1	U12	1X603	1X603	ANAREN
39	1	U14	AD1582	AD1582	ANALOG DEVICES
40	1	U15	UPG1678	UPG1678GV	NEC
41	1	U16	ADP-2-10-75	ADP-2-10-75	MINI-CIRCUITS
42	1		BOARD	8500.641.021	V05.10

FIG.61B

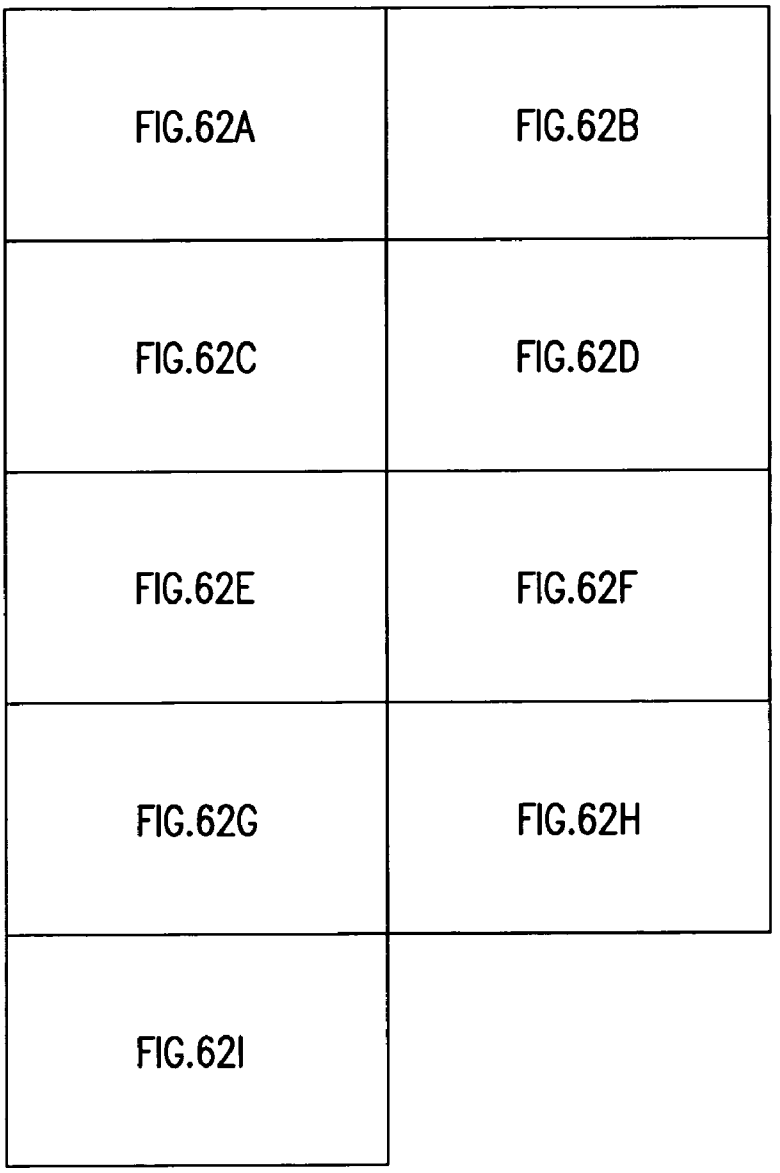

FIG.62A
FIG.62B
FIG.62C
FIG.62D
FIG.62E
FIG.62F
FIG.62G
FIG.62H
FIG.62I

FIG.62

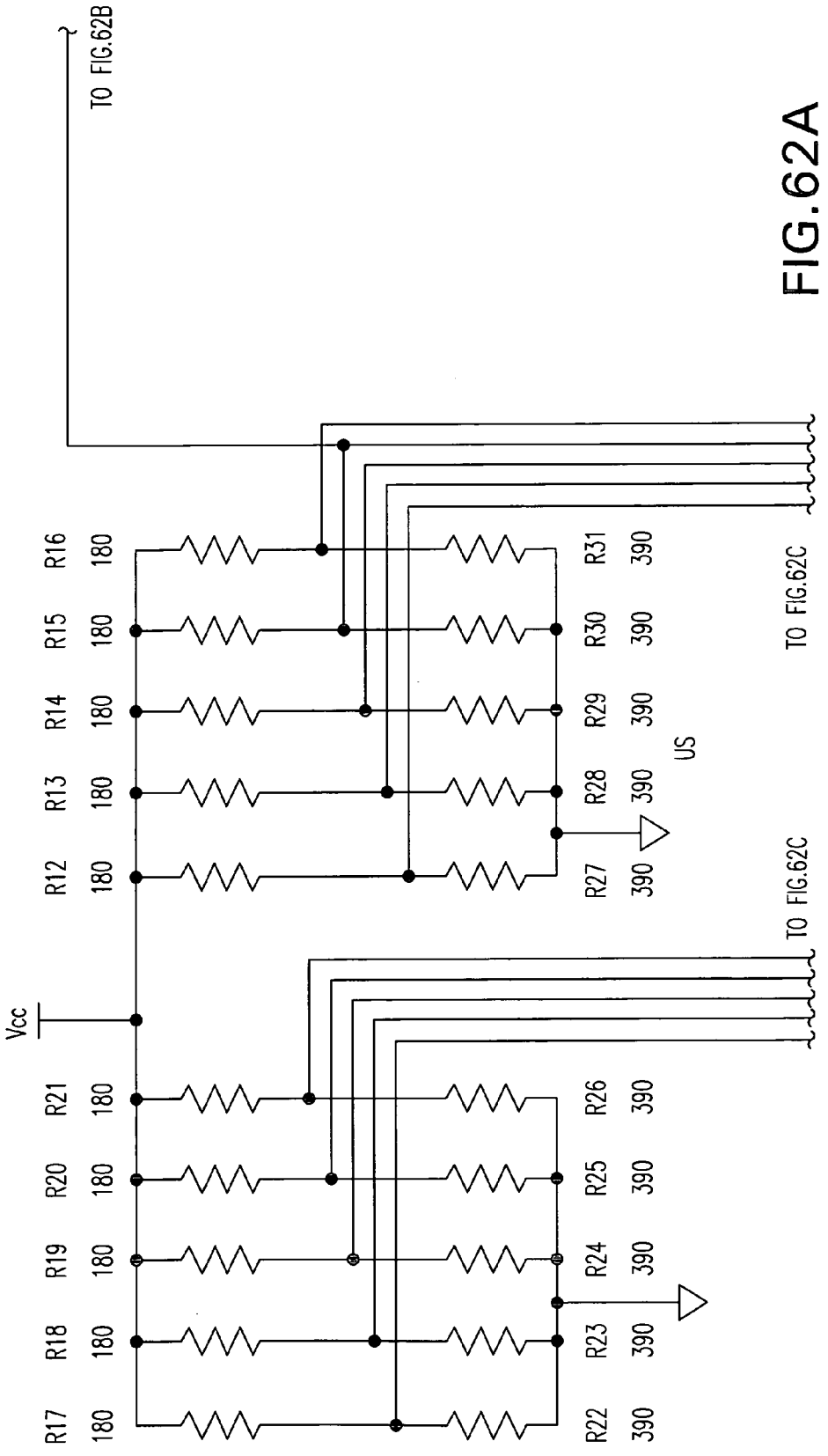
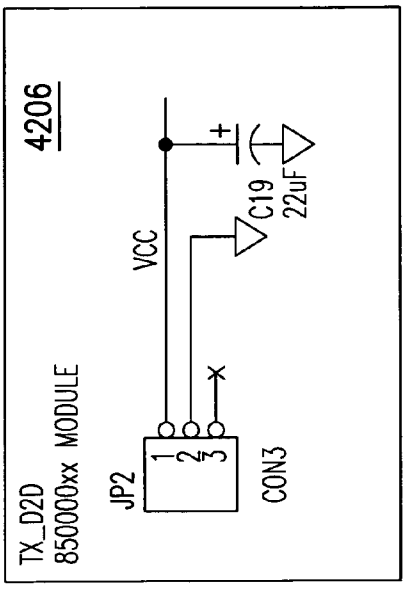
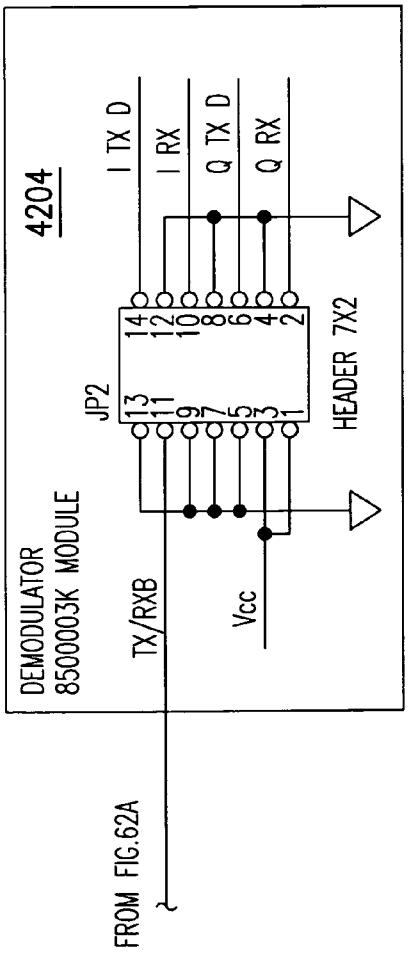

TO FIG.62B
TO FIG.62C
TO FIG.62C
Vcc
R16 180
R15 180
R14 180
R13 180
R12 180
R31 390
R30 390
R29 390
R28 390
R27 390
US
R21 180
R20 180
R19 180
R18 180
R17 180
R26 390
R25 390
R24 390
R23 390
R22 390

FIG.62A


TX_D2D
8500000x MODULE
4206
VCC
C19
22uF
JP2
CON3


DEMODULATOR
8500003K MODULE
4204
I TX D
I RX
Q TX D
Q RX
JP2
HEADER 7X2
TX/RXB
Vcc
FROM FIG.62A

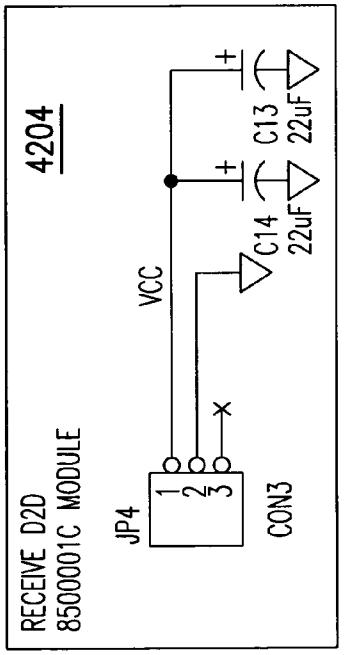

RECEIVE D2D
8500001C MODULE
4204
VCC
C14
22uF
C13
22uF
JP4
CON3

FIG.62B

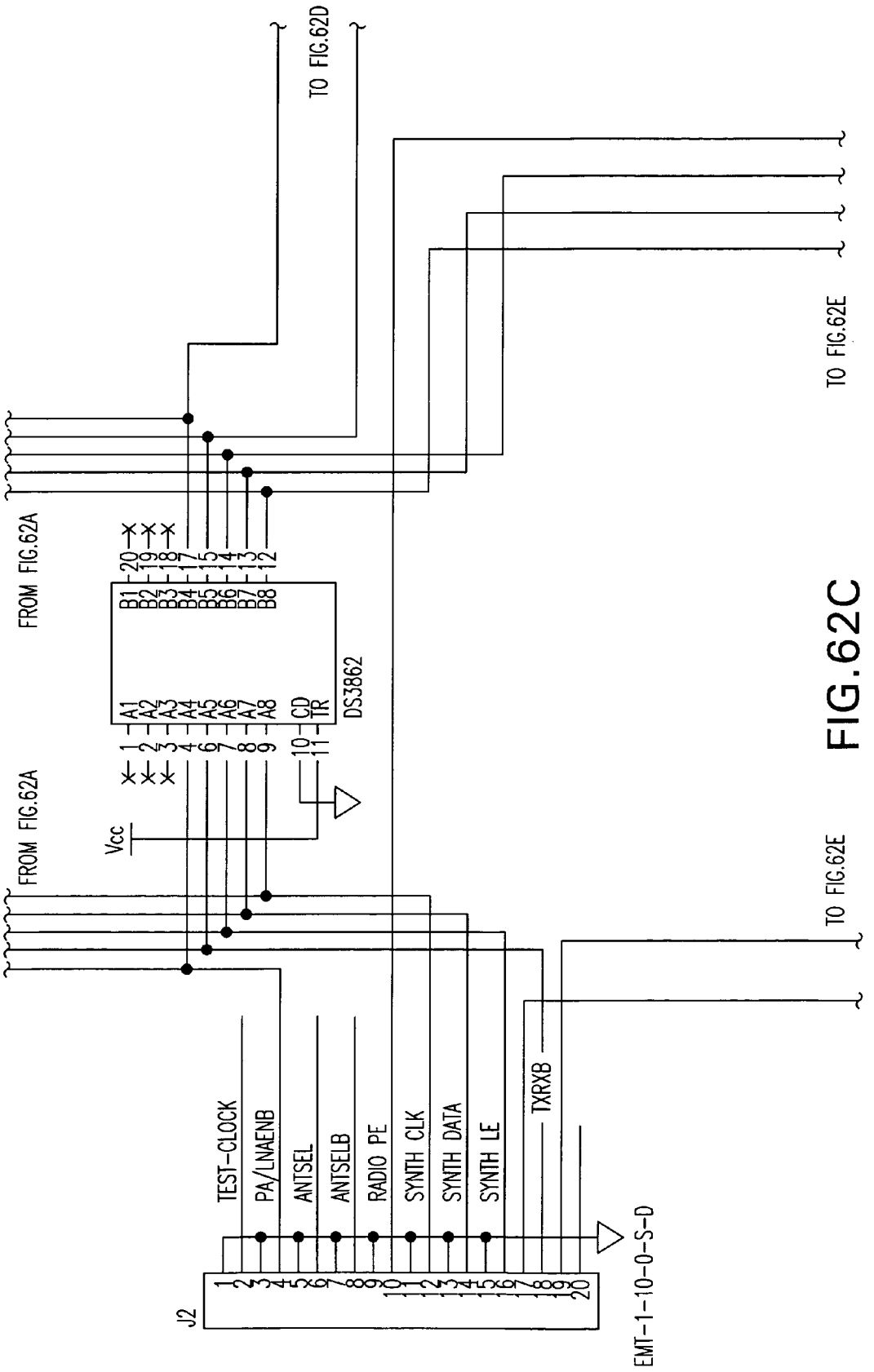

TO FIG.62D
TO FIG.62E
FROM FIG.62A
FROM FIG.62A
DS3862
Vcc
TEST-CLOCK
PA/LNAENB
ANTSEL
ANTSELB
RADIO PE
SYNTH CLK
SYNTH DATA
SYNTH LE
TXRXB
TO FIG.62E
J2
EMT-1-10-0-S-D

FIG.62C

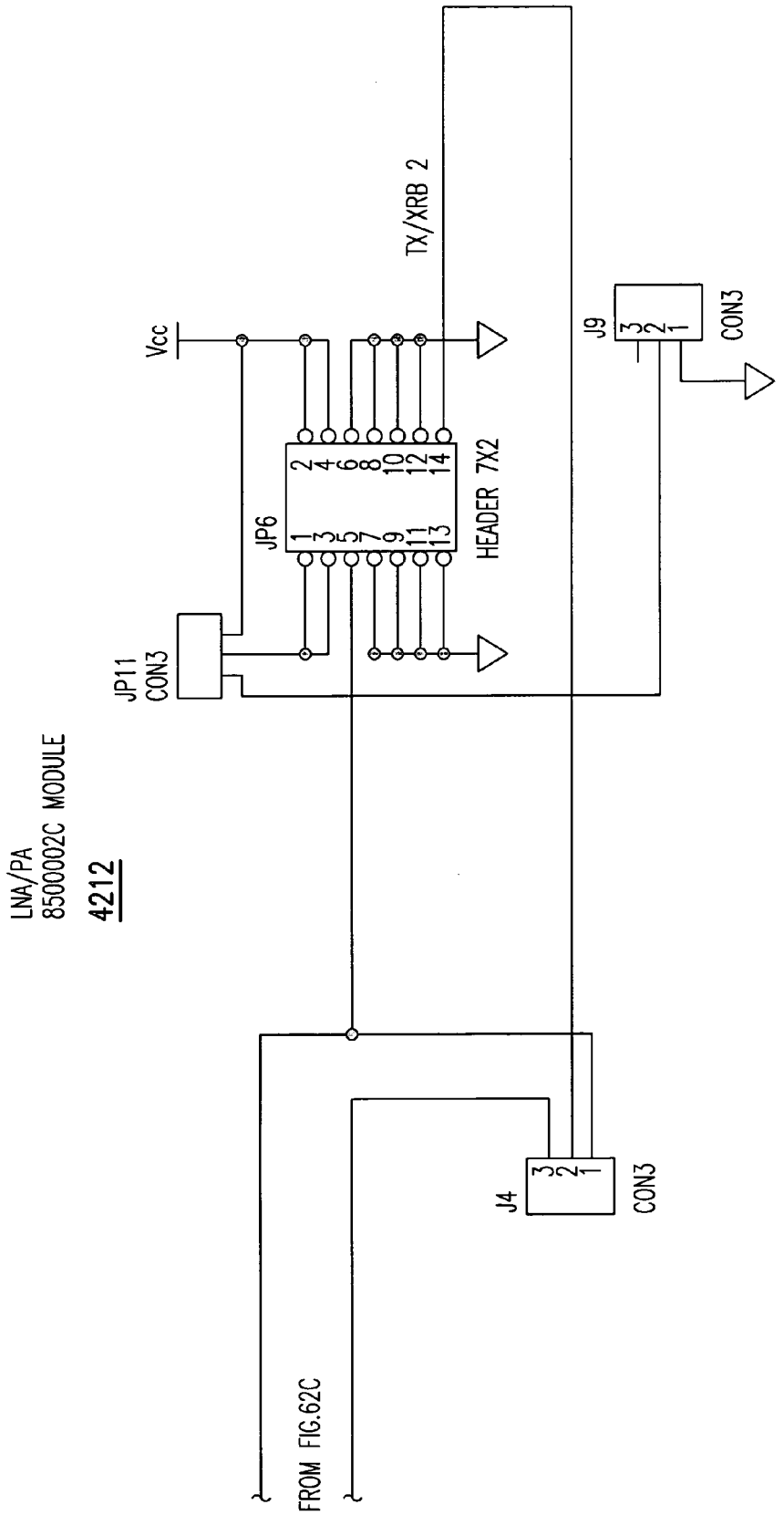

LNA/PA
8500002C MODULE
4212
JP11
CON3
JP6
HEADER 7X2
Vcc
TX/XRB 2
J9
CON3
J4
CON3
FROM FIG.62C

FIG.62D

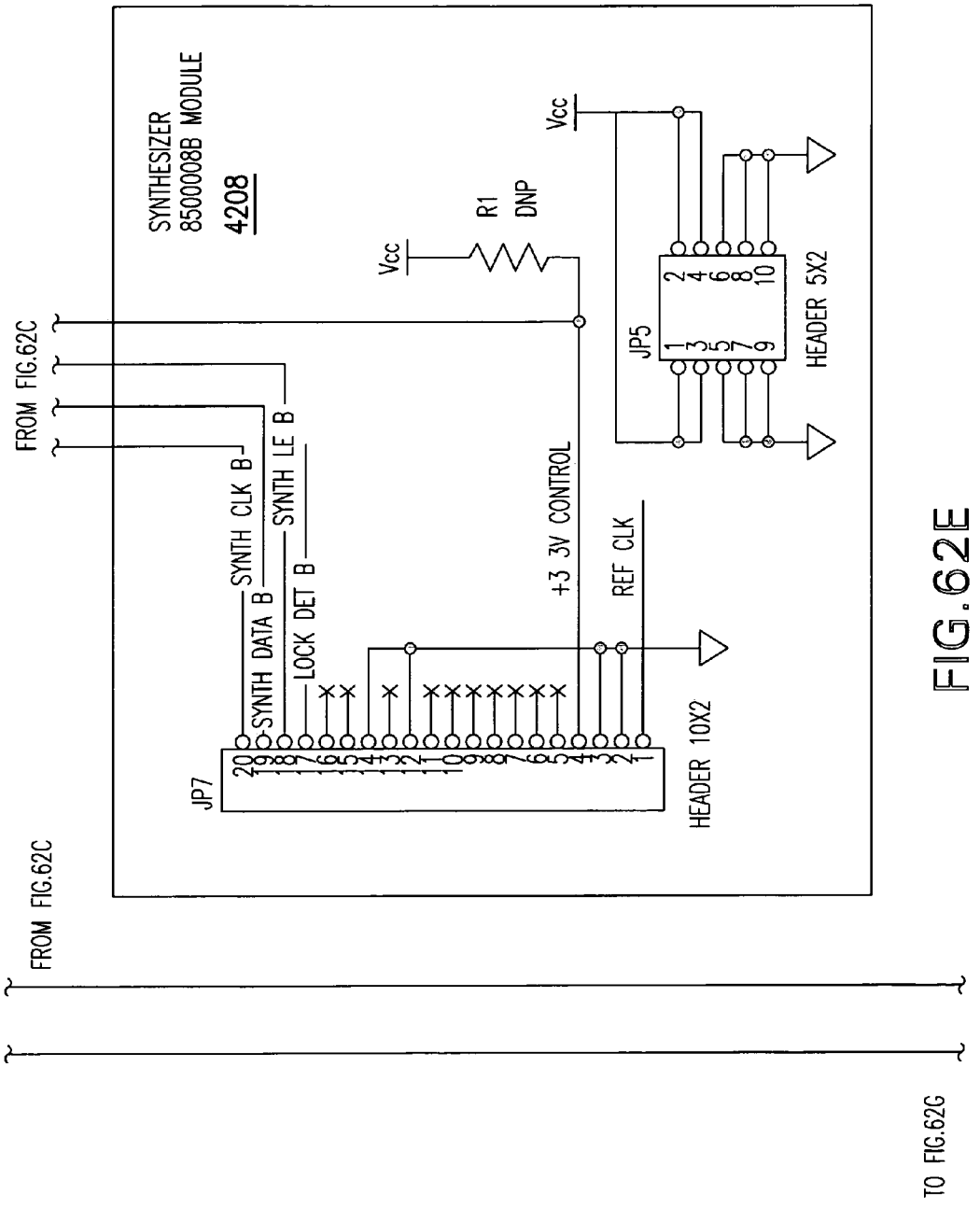

SYNTHESIZER
8500008B MODULE
4208
FROM FIG.62C
SYNTH CLK B
SYNTH LE B
SYNTH DATA B
LOCK DET B
+3 3V CONTROL
REF CLK
Vcc
R1
DNP
Vcc
JP5
HEADER 5X2
JP7
HEADER 10X2
FROM FIG.62C
TO FIG.62G

FIG.62E

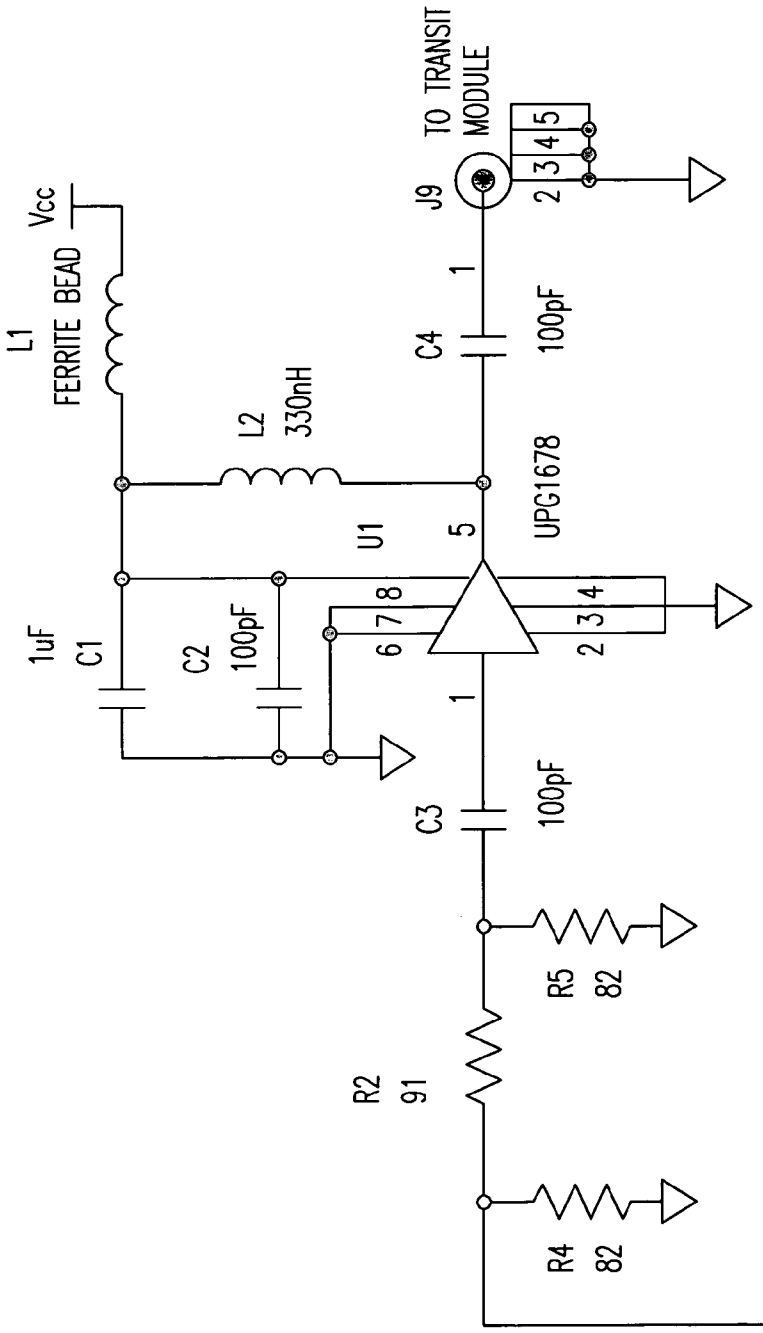

Vcc
L1
FERRITE BEAD
L2
330nH
C1
1uF
C2
100pF
U1
UPG1678
J9
TO TRANSIT MODULE
C4
100pF
C3
100pF
R5
82
R2
91
R4
82
TO FIG.62H

FIG.62F

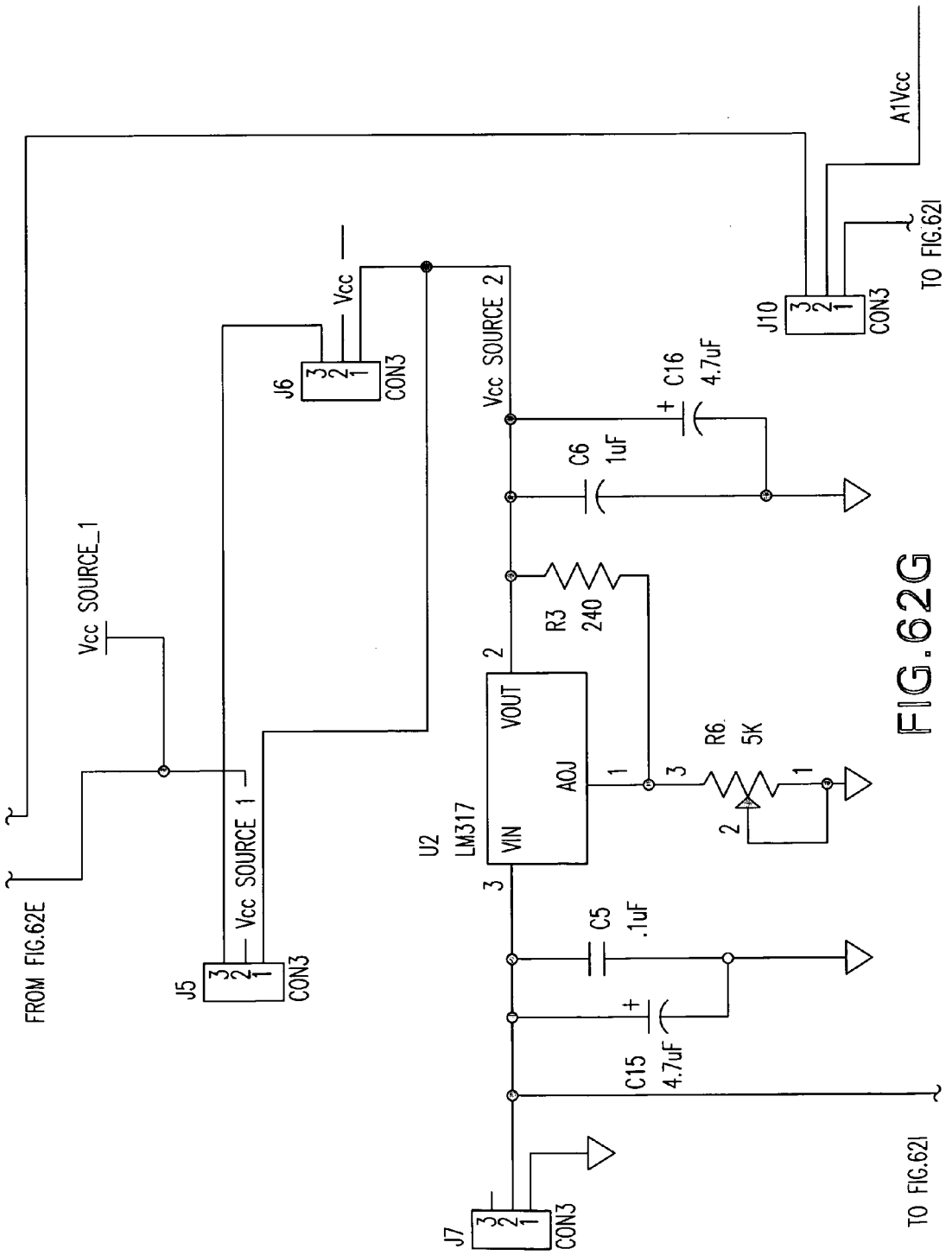

A1Vcc
TO FIG.62I
J10
CON3
Vcc
J6
CON3
Vcc SOURCE 2
C16
4.7uF
C6
1uF
Vcc SOURCE_1
R3
240
2
VOUT
U2
LM317
VIN
ADJ
3
1
R6
5K
FROM FIG.62E
Vcc SOURCE 1
J5
CON3
C5
.1uF
C15
4.7uF
J7
CON3
TO FIG.62I

FIG.62G

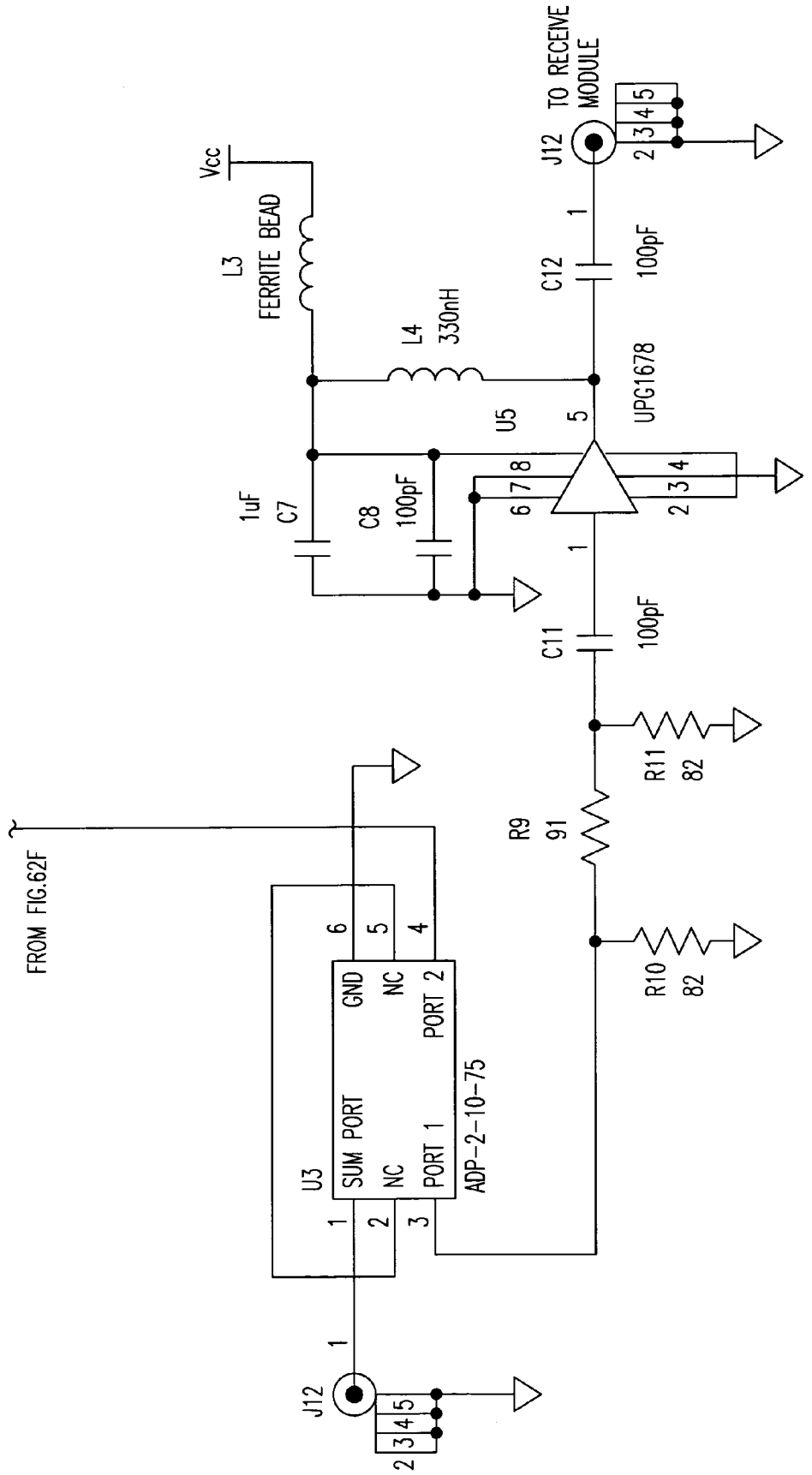

FROM FIG.62F
J12
1
2
3
4
5
U3
SUM PORT
NC
PORT 1
GND
NC
PORT 2
ADP-2-10-75
R10
82
R9
91
R11
82
C11
100pF
C8
100pF
C7
1uF
Vcc
L3
FERRITE BEAD
L4
330nH
C12
100pF
U5
UPG1678
J12
TO RECEIVE MODULE

FIG.62H

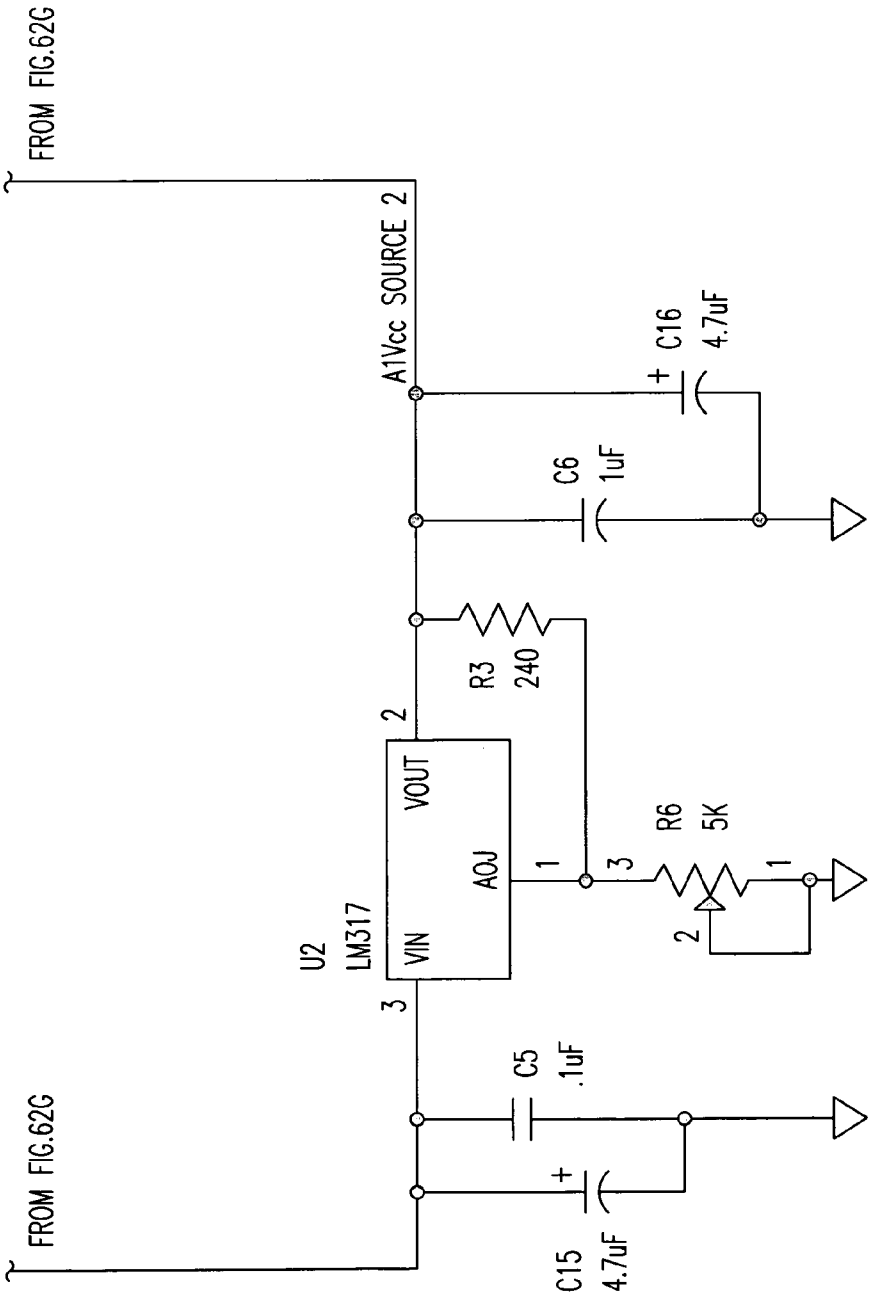

FROM FIG.62G
A1Vcc SOURCE 2
C16
4.7uF
C6
1uF
R3
240
2
U2
LM317
VOUT
AOJ
VIN
1
3
R6
5K
2
1
3
C5
.1uF
C15
4.7uF
FROM FIG.62G

FIG.62I

ITEM	QTY	REFERENCE	PART	DESCRIPTION	PART NUMBER	VENDOR
1	4	C1,C6,C7,C10	1uF	Cap, 1uF, +80-20%,0805	GRM40Y5V105Z016AD	MURATA
2	6	C2,C3,C4,C8,C11,C12	100pF	Cap, 100pF, 5%, COG, 0603	ECU-V1H101JCV	PANASONIC
3	2	C5,C9	.1uF	Cap, .1uF, +80-20%, Y5V, 0603		MURATA
4	3	C13,C14,C19	22uF	Cap, Tant, 22uF, 20%, 20V	T491D226M020AS	KEMET
5	4	C15,C16,C17,C18	4.7uF	Cap, Tant, 4.7uF, 20%, 20V	T491C475M020AS	KEMET
6	2	JP2,JP6	HEADER 7X2	Receptacle, 7x2pin, .050	SFMC-107-L1-S-D	SAMTEK
7	9	JP4, J4, J5, J6, J7, JP9, J9, J10, JP11	CON3	Header, 3pin, .100''	69190-403	BERG
8	1	JP7	HEADER 10X2	Receptacle, 10X2pin, .050	SFMC-110-L1-S-D	SAMTEK
9	1	JP8	HEADER 5X2	Receptacle, 5X2pin, .050	SFMC-105-L1-S-D	SAMTEK
10	1	J2	EHT-1-10-01-S-D	Header, ribbon, 10X2pin, 2mm	EHT-1-10-01-S-D	SAMTEK
11	3	J8,J11,J12	82MMCX-50-0-1	Connector,RF	82MMCX-50-0-1	SUHNER
12	2	L3,L1	Ferrite Bead	Ferrite Bead, 0805	BLM21A121S	MURATA
13	2	L4,L2	330nH	Ind, 330nH, 10%, 0805	LL2012-FR33K	TOKO
14	1	R1	DNP	Res, 0603		PANASONIC
15	2	R9,R2	91	Res, 91 Ohm, 5%, 0603	ERJ-3GSYJ910	PANASONIC
16	2	R7,R3	240	Res, 240 Ohm, 5%, 0603	ERJ-3GSYJ241	PANASONIC
17	4	R4,R5,R10,R11	82	Res, 82 Ohm, 5%, 0603	ERJ-3GSYJ820	PANASONIC
18	2	R8,R6	5K	Var Res, 5K, 10%	3296W001502	BOURNS
19	10	R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	180	Res, 180 Ohm, 5%, 0603	ERJ-3GSYJ181	PANASONIC
20	10	R22, R23, R24, R25, R26, R27, R28, R29, R30, R31	390	Res, 390 Ohm, 5%, 0603	ERJ-3GSYJ391	PANASONIC
21	2	U5,U1	UPG1678	IC, RF Buffer	UPG1678GV	NEC
22	2	U4,U2	LM317	IC, Voltage Regulator	LM317T	NATIONAL
23	1	U3	ADP-2-10-75	RF Splitter	ADP-2-10-75	MINICIRCUITS
24	1	U6	DS3862	IC, Buffer	DS3862WM	NATIONAL
25	1			BOARD	ST8500.641.023V0L01	

FIG.63

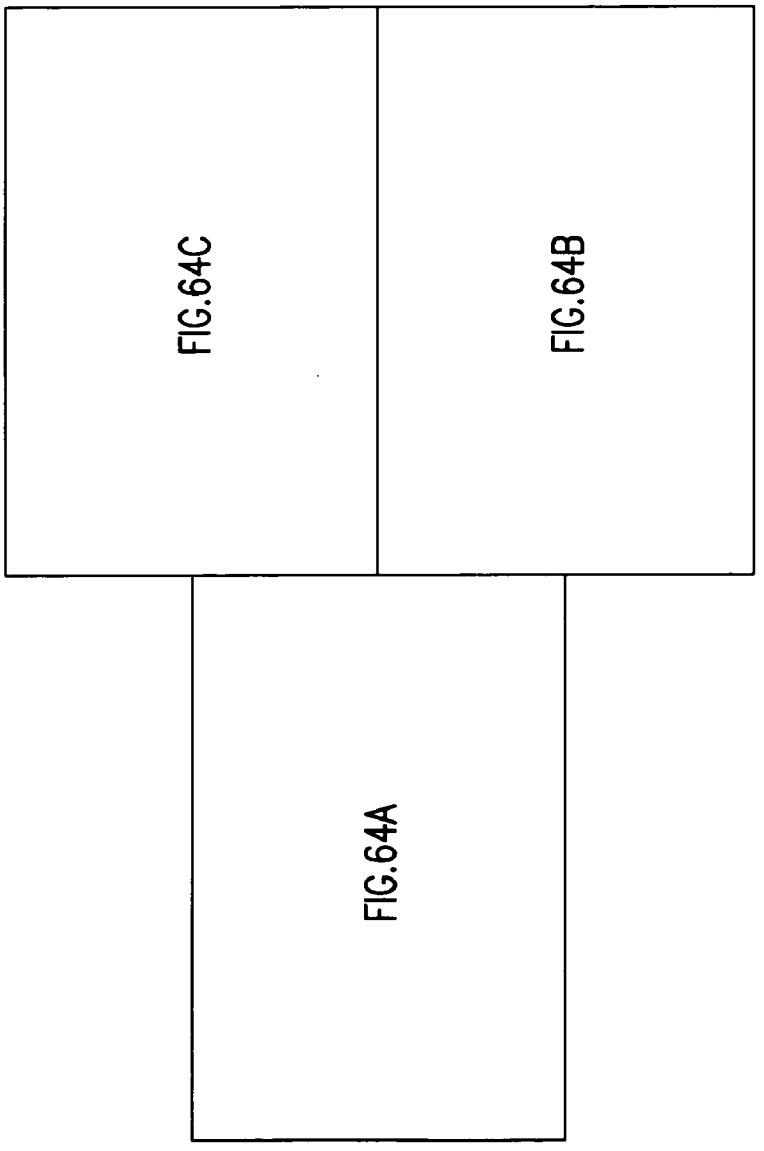


FIG.64

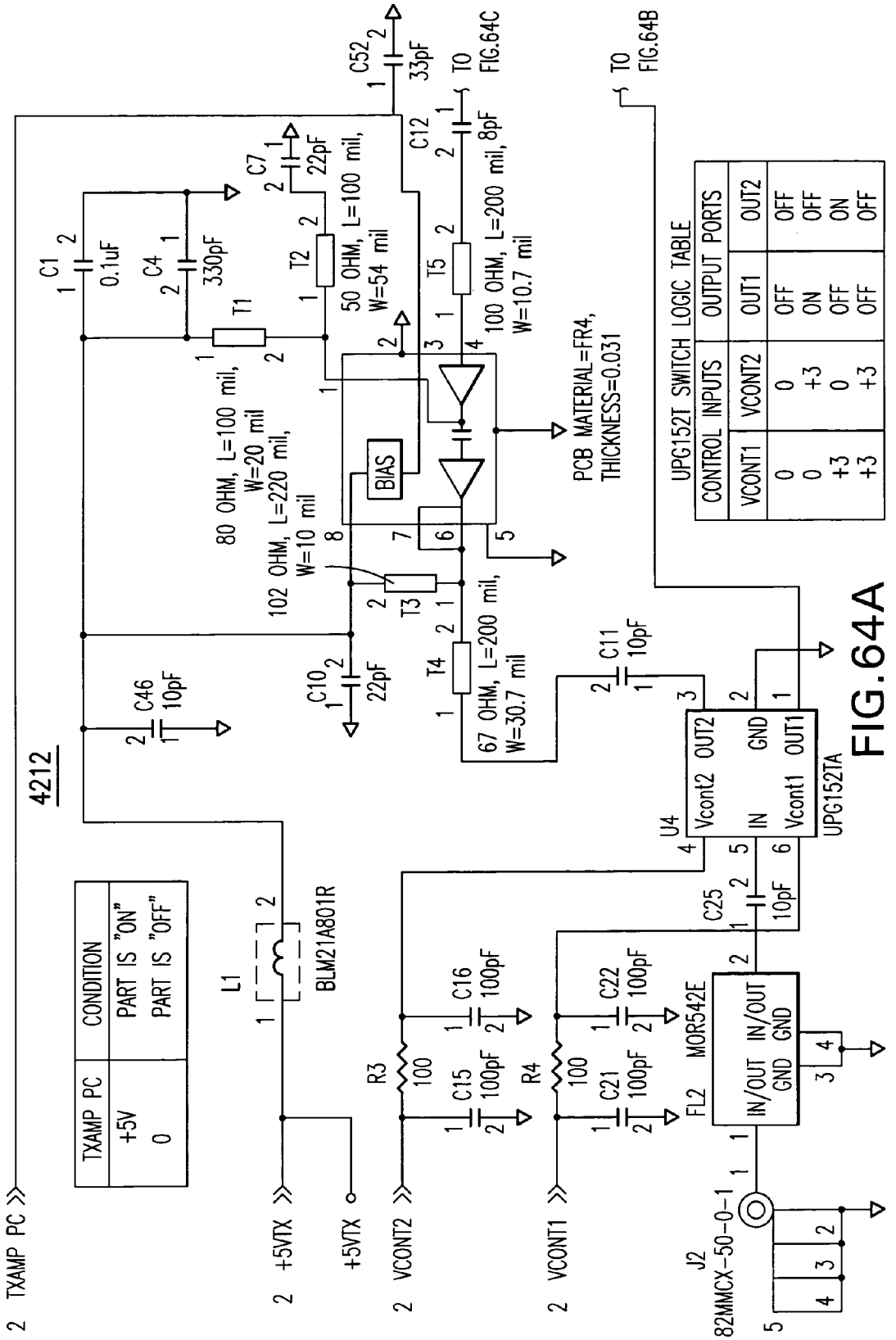

4212
2 TXAMP PC
TXAMP PC
+5V
0
CONDITION
PART IS "ON"
PART IS "OFF"
C1 0.1uF
C4 330pF
C46 10pF
T1
80 OHM, L=100 mil, W=20 mil
102 OHM, L=220 mil, W=10 mil
C10 22pF
T2
50 OHM, L=100 mil, W=54 mil
C7 22pF
C52 33pF
C12 8pF
T5
100 OHM, L=200 mil, W=10.7 mil
T0 FIG.64C
T0 FIG.64B
BIAS
T3
T4
67 OHM, L=200 mil, W=30.7 mil
PCB MATERIAL=FR4, THICKNESS=0.031
C11 10pF
L1
BLM21A801R
2 +5VTX
+5VTX
2 VCONT2
2 VCONT1
R3 100
R4 100
C15 100pF
C16 100pF
C21 100pF
C22 100pF
C25 10pF
U4
Vcont2 OUT2
IN GND
Vcont1 OUT1
UPG152TA
F12 MOR542E
IN/OUT IN/OUT
GND GND
J2
82MMCX-50-0-1
UPG152T SWITCH LOGIC TABLE
CONTROL INPUTS
OUTPUT PORTS
VCONT1
VCONT2
OUT1
OUT2
0 0 OFF OFF
0 +3 ON OFF
+3 0 OFF ON
+3 +3 OFF OFF

FIG.64A

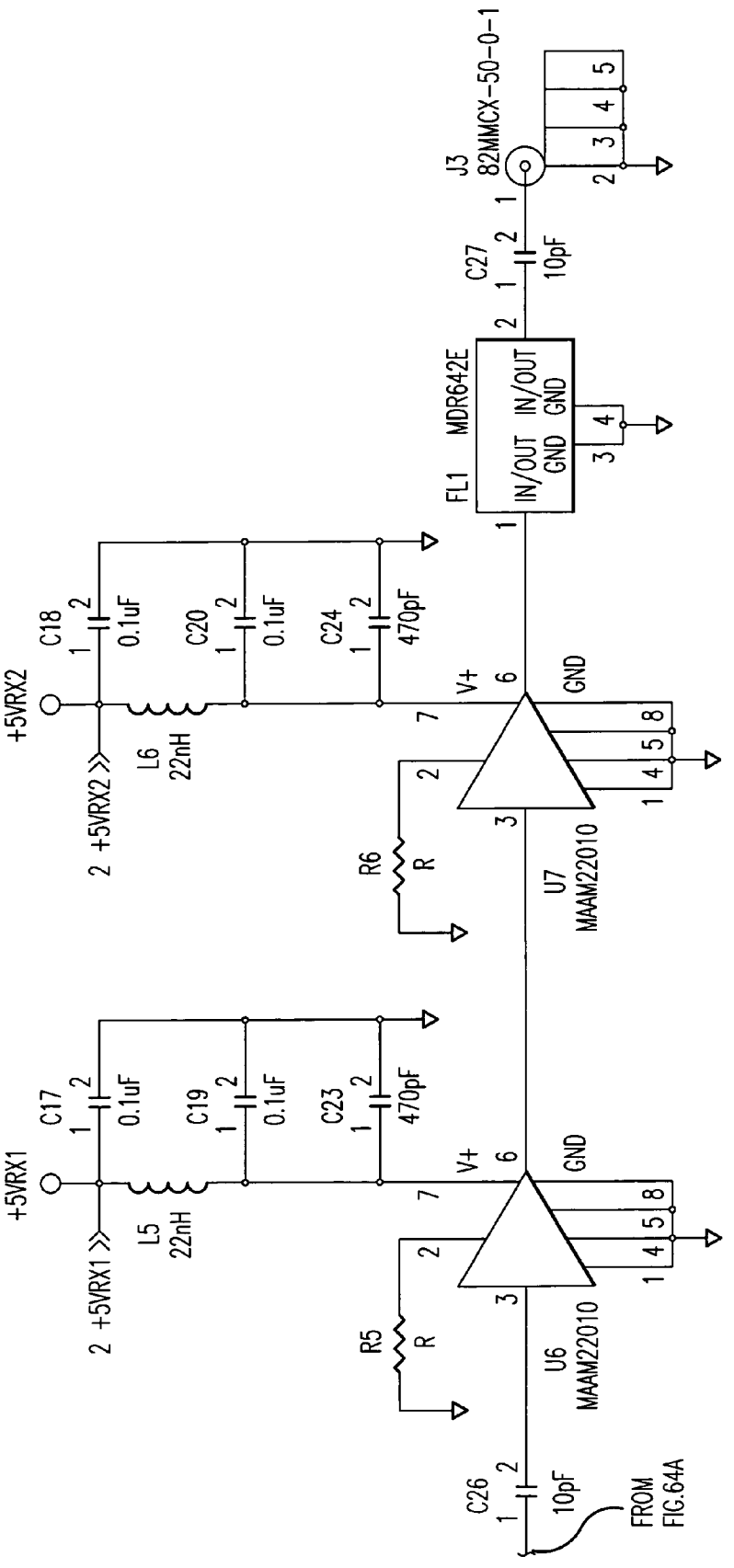

J3
82MMCX-50-0-1
C27
10pF
FL1
MDR642E
IN/OUT
GND
IN/OUT
GND
C18
0.1uF
C20
0.1uF
C24
470pF
+5VRX2
L6
22nH
2 +5VRX2
V+
GND
R6
R
U7
MAAM22010
C17
0.1uF
C19
0.1uF
C23
470pF
+5VRX1
L5
22nH
2 +5VRX1
R5
R
U6
MAAM22010
C26
10pF
FROM
FIG.64A

FIG.64B

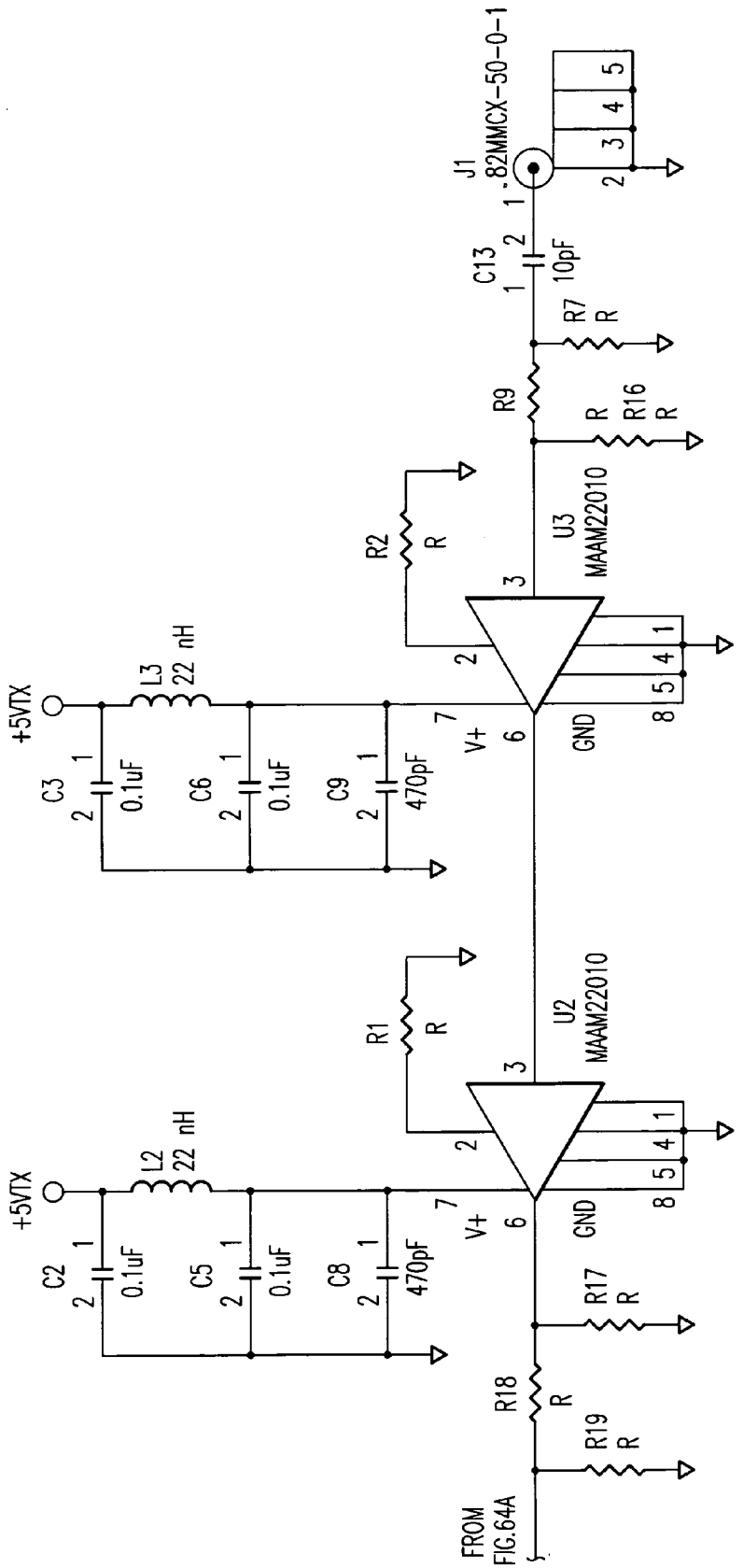

J1
.82MMCX-50-0-1
C13
10pF
R7
R
R9
R16
R
U3
MAAM22010
R2
R
+5VTX
L3
22 nH
C3
0.1uF
C6
0.1uF
C9
470pF
V+
GND
U2
MAAM22010
R1
R
+5VTX
L2
22 nH
C2
0.1uF
C5
0.1uF
C8
470pF
R17
R
R18
R
R19
R
FROM
FIG.64A

FIG.64C

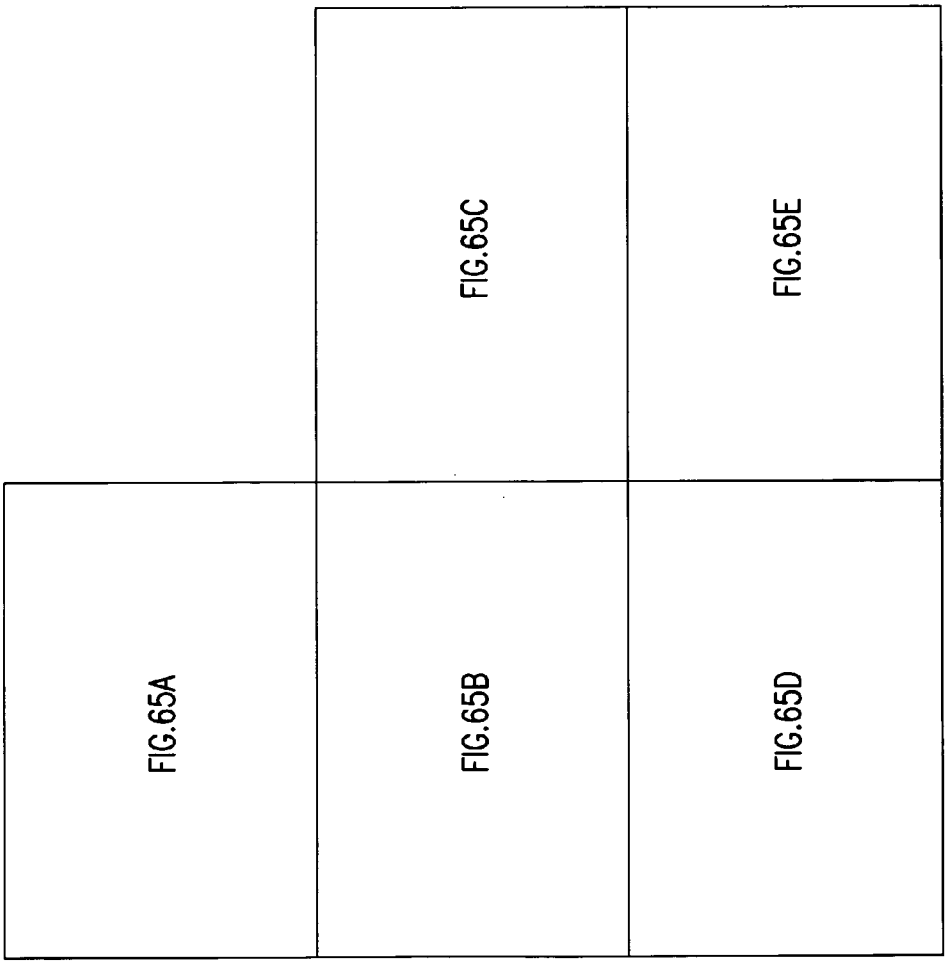


FIG.65

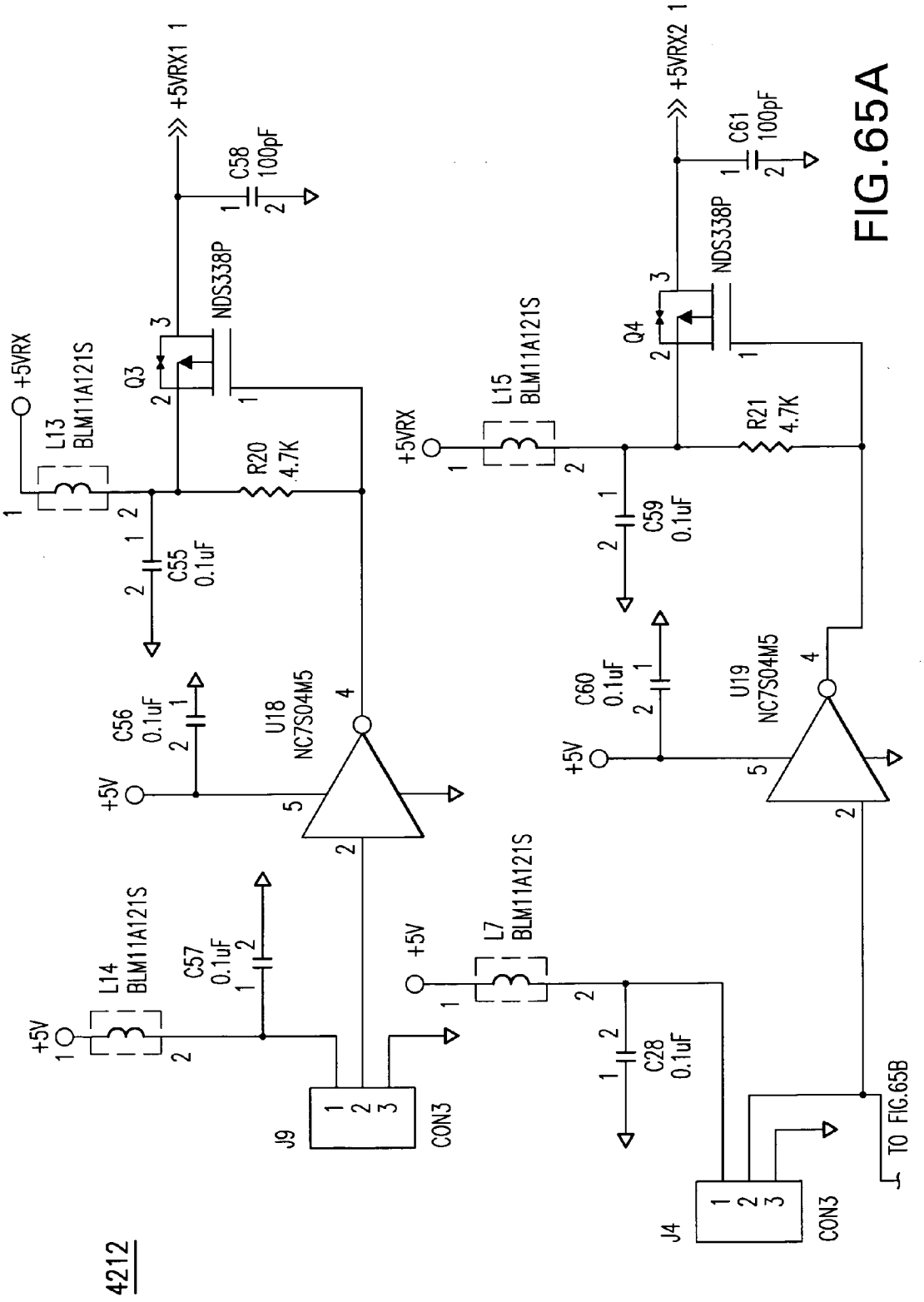

4212
+5VRX
L13 BLM11A121S
L14 BLM11A121S
L15 BLM11A121S
L7 BLM11A121S
Q3
NDS338P
Q4
NDS338P
R20 4.7K
R21 4.7K
C55 0.1uF
C56 0.1uF
C57 0.1uF
C59 0.1uF
C60 0.1uF
C28 0.1uF
C58 100pF
C61 100pF
+5V
U18 NC7S04M5
U19 NC7S04M5
>> +5VRX1
>> +5VRX2
J9
J4
CON3
TO FIG.65B

FIG.65A

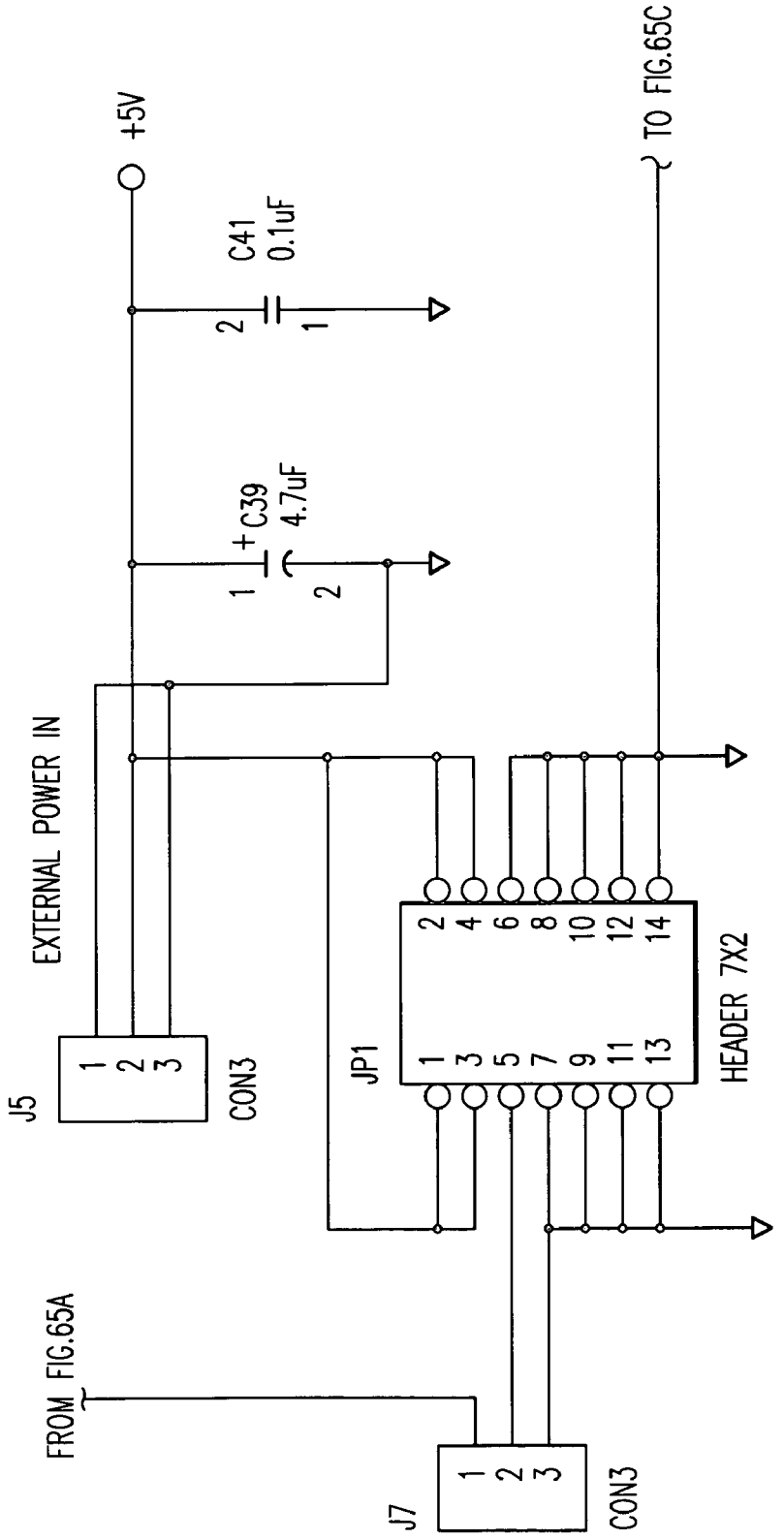

+5V
C41
0.1uF
2
1
+C39
4.7uF
1
2
TO FIG.65C
EXTERNAL POWER IN
J5
1
2
3
CON3
JP1
2
4
6
8
10
12
14
1
3
5
7
9
11
13
HEADER 7X2
FROM FIG.65A
J7
1
2
3
CON3

FIG.65B

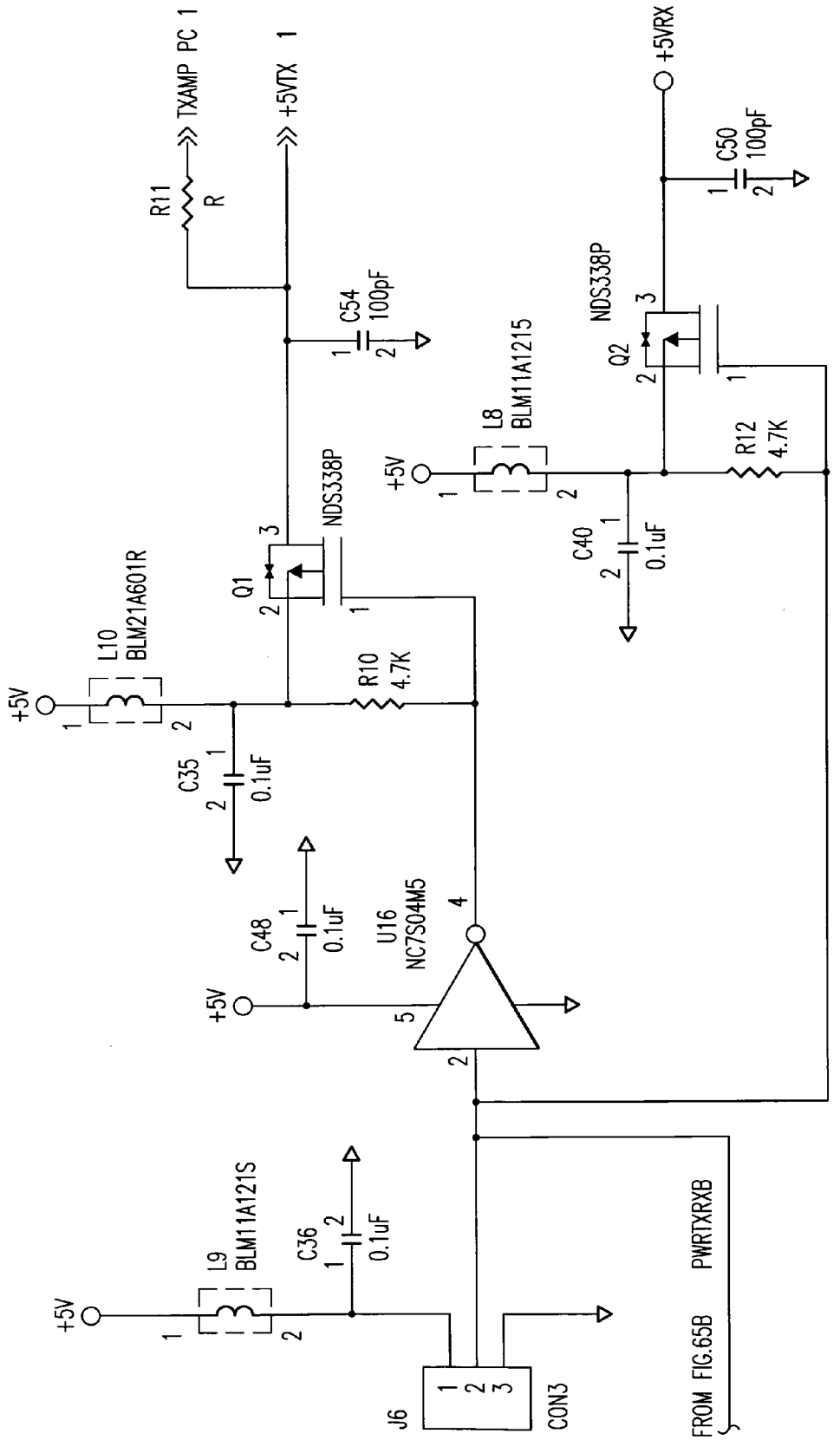

TXAMP PC 1
+5VTX 1
+5VRX
R11
R
C54
100pF
C50
100pF
NDS338P
Q2
L8
BLM11A1215
R12
4.7K
+5V
C40
0.1uF
NDS338P
Q1
L10
BLM21A601R
R10
4.7K
C35
0.1uF
C48
0.1uF
U16
NC7S04M5
L9
BLM11A121S
C36
0.1uF
J6
CON3
FROM FIG.65B
PWRTXRXB

FIG.65C

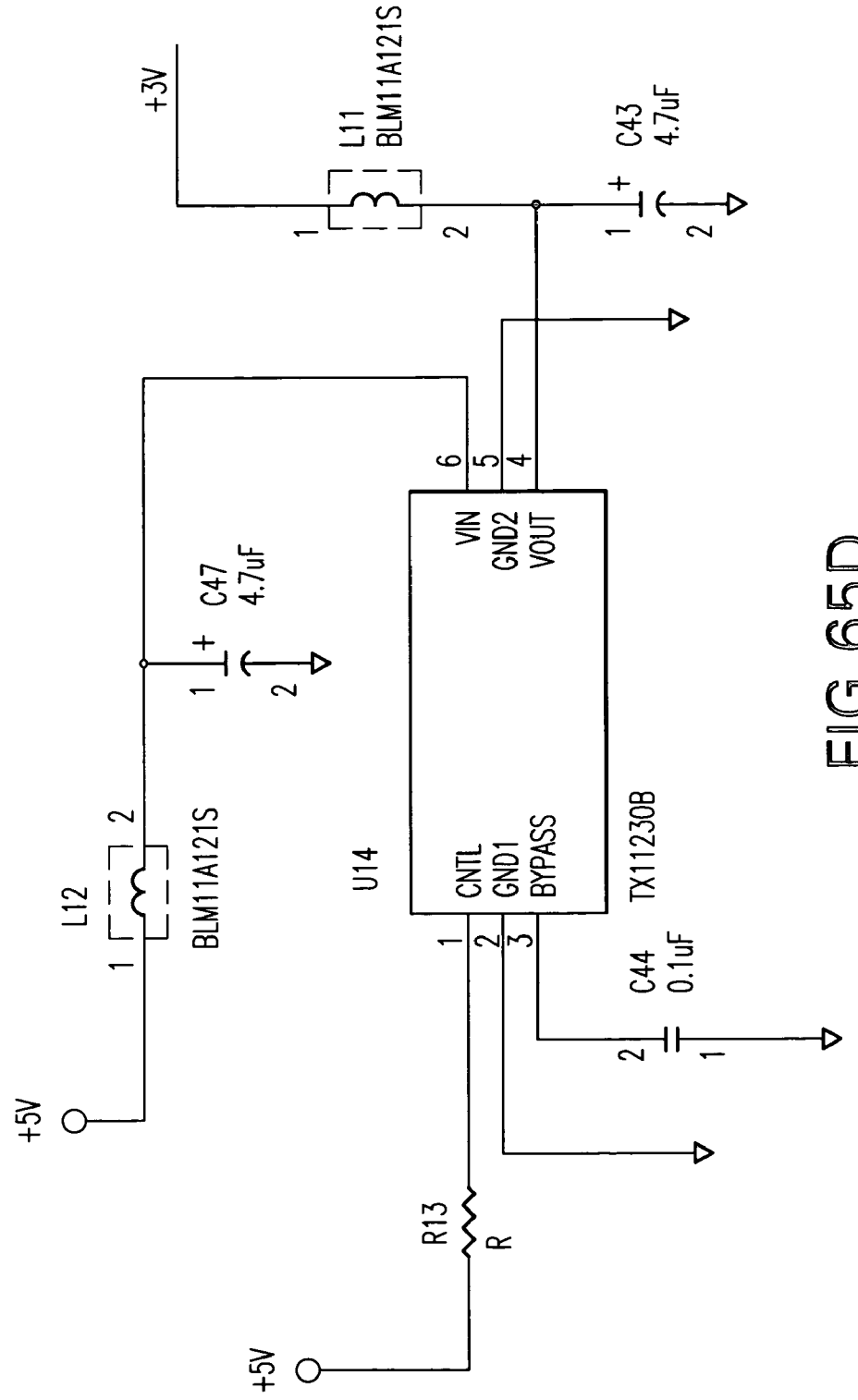

+3V
L11
BLM11A121S
C43
4.7uF
C47
4.7uF
L12
BLM11A121S
U14
VIN
GND2
VOUT
CNTL
GND1
BYPASS
TX11230B
C44
0.1uF
+5V
R13
R
+5V

FIG.65D

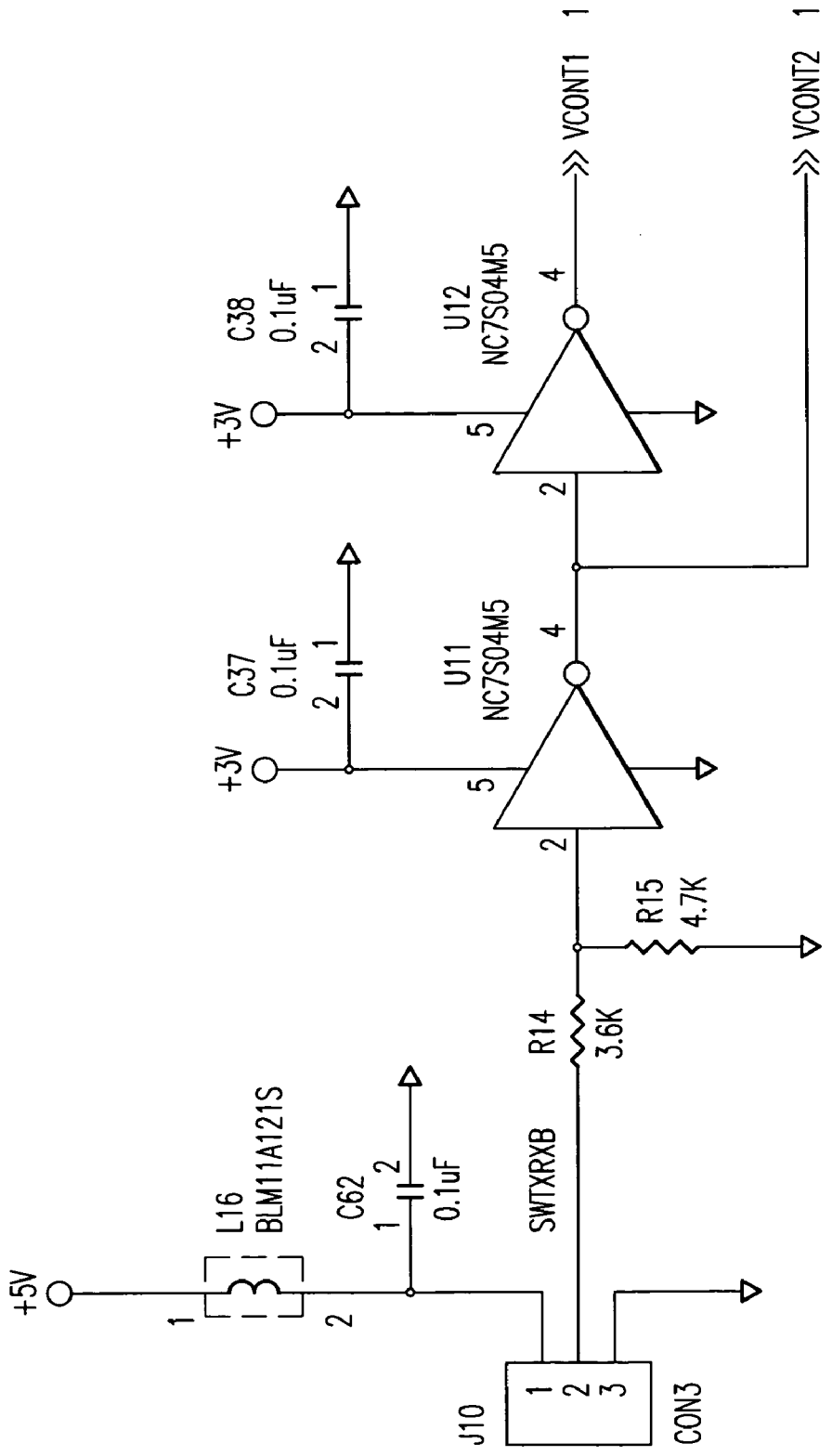

+5V
L16
BLM11A121S
C62
0.1uF
SWTXRXB
R14
3.6K
R15
4.7K
+3V
C37
0.1uF
U11
NC7S04M5
+3V
C38
0.1uF
U12
NC7S04M5
>> VCONT1
>> VCONT2
J10
CON3

FIG. 65E

ITEM	QTY	REFERENCE	PART	MANUFACT.	PART DESCRIPTION	PART NUMBER
1	24	C1,C2,C3,C5,C6,C17,C18, C19,C20,C28,C35,C36,C37, C38,C40,C41,C44,C48,C55, C56,C57,C59,C60,C62	0.1uF	MURATA	.1uF,0603,X7R,20%,16V	GRM39X7R104M016
2	1	C4	330pF	MURATA	330pF,0603,COG,10%,50	GRM39COG331K050
3	2	C10,C7	22pF	MURATA	22pF,0603,COG,10%,50	GRM30COG220K050
4	4	C8,C9,C23,C24	470pF	MURATA	470pF,0603,COG,10%,50	GRM39COG471K050
5	6	C11,C13,C25,C26,C27,C46	10pF	MURATA	10pF,0603,COG,10%,50	GRM39COG100K050
6	1	C12	8pF	MURATA	8pF,0603,COG,10%,50	GRM39COG080K050
7	8	C15,C16,C21,C22,C50,C54 C58,C61	100pF	MURATA	100pF,0603,COG,10%,50	GRM39COG101K050
8	3	C39,C43,C47	4.7uF	PANASONIC	4.7uF TANTALUM,16V	ECS-T1CY475R
9	1	C52	33pF	MURATA	330pF,0603,COG,10%,50	GRM3COG330K050
10	2	FL1,FL2	MDR642E	SOSHIN	2.4-2.5GHz BPF	MDR642E
11	1	JP1	HEADER 7X2	SAMTEC	DUAL ROW, 7 PINS PER ROW	FTSH-107-01-F-D
12	3	J1,J2,J3	82MMCX-50-0-1	SUHNER	RF CONNECTOR	82MMCX-50-0-1
13	6	J4,J5,J6,J7,J9,J10	CON3	BERG	3 PIN HEADER W RETENTIVE LEG	69190-403H
14	2	L10,L1	BLM21A601R	MURATA	600 OHMS@100MHz,500mA FERRITE BEAD	BLM21A601R
15	4	L2,L3,L5,L6	22nH	COILCRAFT	22nH,0805CS (2012),5%	0805CS-220X-BC
16	9	L7,L8,L9,L11,L12,L13,L14, L15,L16	BLM11A121S	MURATA	RF BEAD	BLM11A121S
17	4	Q1,Q2,Q3,Q4	NDS336P	NATIONAL	P-CHANNEL FET	NDS336P
18	12	R1,R2,R5,R6,R7,R9,R11, R13,R16,R17,R18,R19	R	PANASONIC		
19	2	R3,R4	100	PANASONIC	0603,100,5%,1/16W	ERJ-3GSY-J-101
20	5	R10,R12,R15,R20,R21	4.7K	PANASONIC	0603,4.7K,5%,1/16W	ERJ-3GSY-J-472

FIG.66A

21	1	R14	3.6K	PANASONIC	0603,3.6K,5%,1/16W	ERJ-3GSY-J-362
22	1	T1	80 OHM,L=100 MIL,W=20 MIL		80 OHM,L=100 MIL,W=20 MIL	
23	1	T2	50 OHM,L=100 MIL,W=54 MIL		50 OHM,L=100 MIL,W=54 MIL	
24	1	T3	102 OHM,L=220 MIL,W=10 MIL		102 OHM,L=220 MIL,W=10 MIL	
25	1	T4	67 OHM,L=200 MIL,W=30.7 MIL		67 OHM,L=200 MIL,W=30.7 MIL	
26	1	T5	100 OHM,L=200 MIL,W=10.7MIL		100 OHM,L=200 MIL,W=10.7 MIL	
27	4	U2,U3,U6,U7	MAAM22010	MACOM	2.4-2.5 GHz LNA	MAAM22010
28	1	U4	UPG152TA	NEC	RF SWITCH	UPG152TA
29	5	U11,U12,U16,U18,U19	NC7S04M5	NATIONAL	INVERTER	NC7S04M5
30	1	U14	TKN11230B	TOKO	VOLTAGE REGULATOR	TK11230B
31	1	U17	RF2128P	RFMD	MEDIUM POWER LINEAR AMPLIFIER	RF2128P
32	1				BOARD	B500.641.024 VOL.

FIG.66B

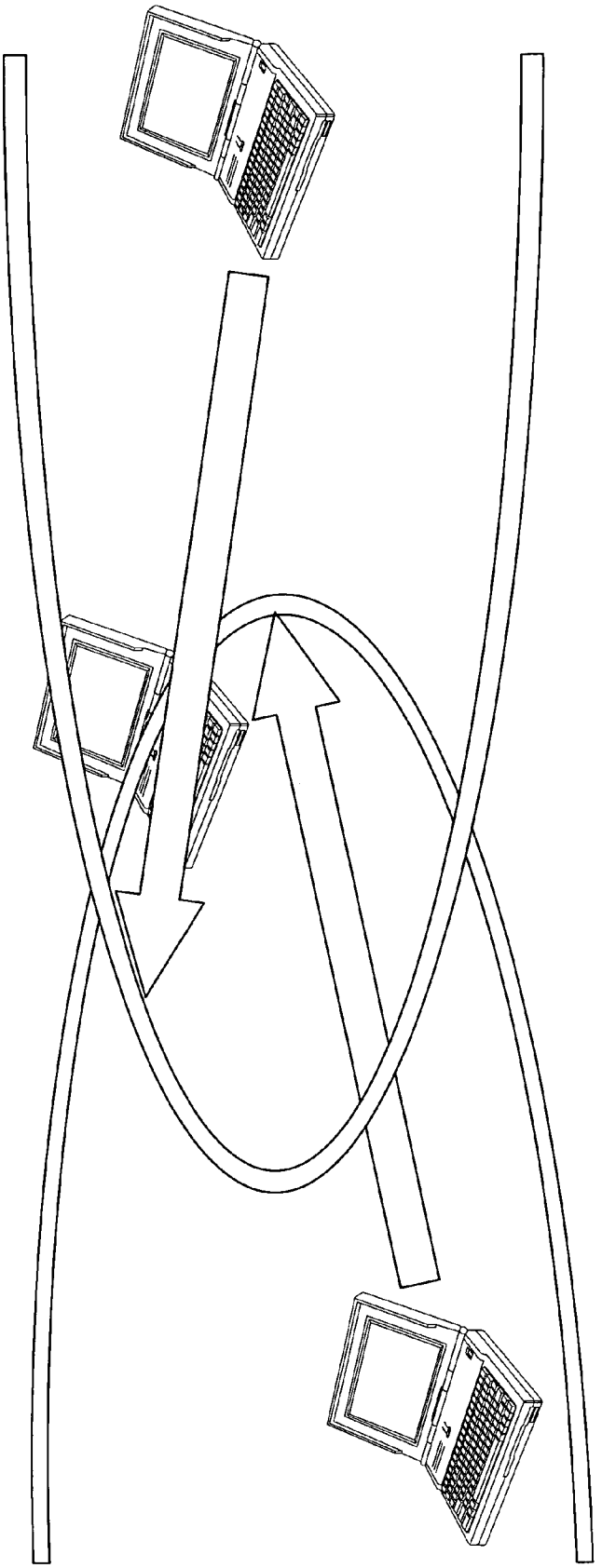


FIG.67

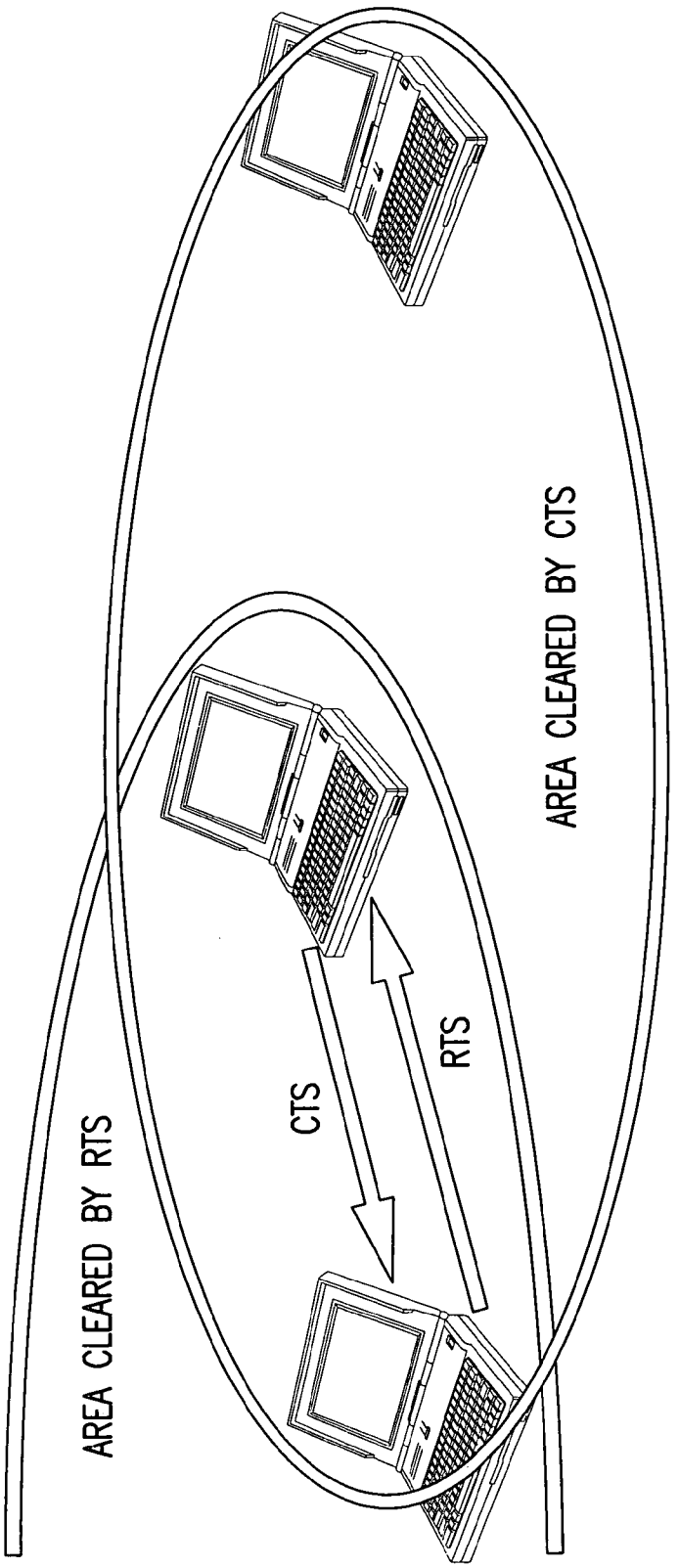


FIG.68

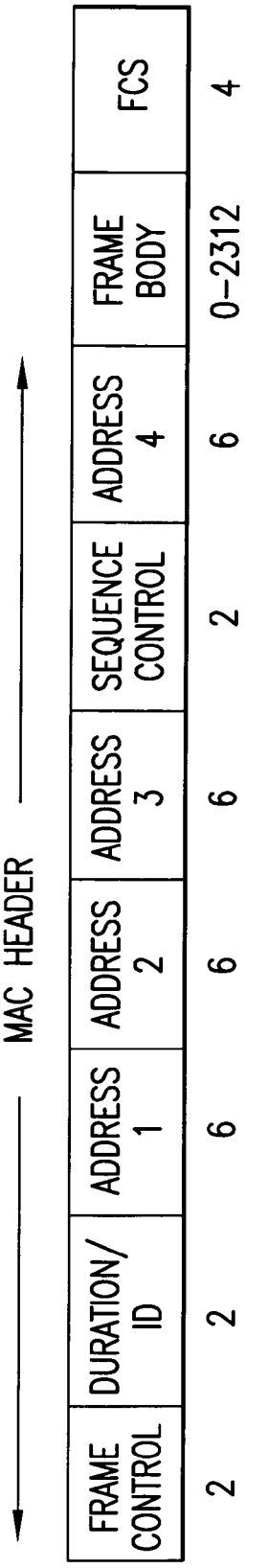

MAC HEADER
FRAME CONTROL
DURATION/ ID
ADDRESS 1
ADDRESS 2
ADDRESS 3
SEQUENCE CONTROL
ADDRESS 4
FRAME BODY
FCS
2
2
6
6
6
2
6
0–2312
4

FIG.69

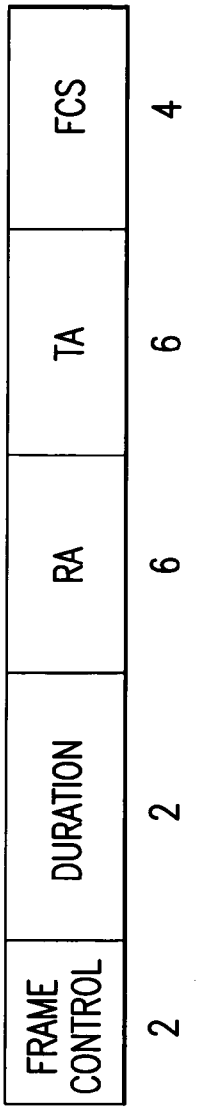

FRAME CONTROL
DURATION
RA
TA
FCS
2
2
6
6
4

FIG.70

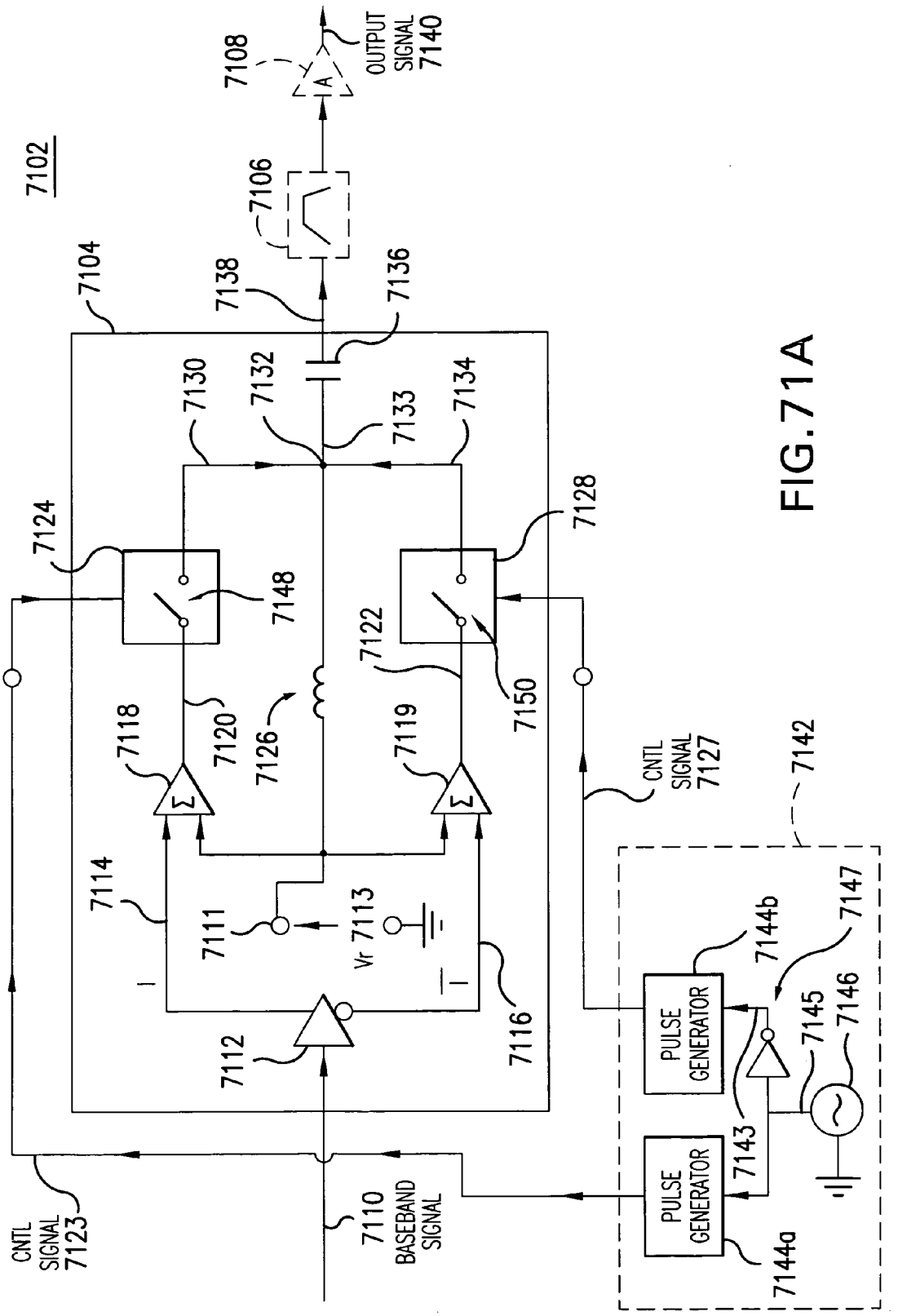

7102
7104
7106
7108
OUTPUT SIGNAL 7140
7110 BASEBAND SIGNAL
CNTL SIGNAL 7123
CNTL SIGNAL 7127
7111
7112
7113
7114
7116
7118
7119
7120
7122
7124
7126
7128
7130
7132
7133
7134
7136
7138
7142
7143
7144a
7144b
7145
7146
7147
7148
7150
PULSE GENERATOR
PULSE GENERATOR

FIG. 71A

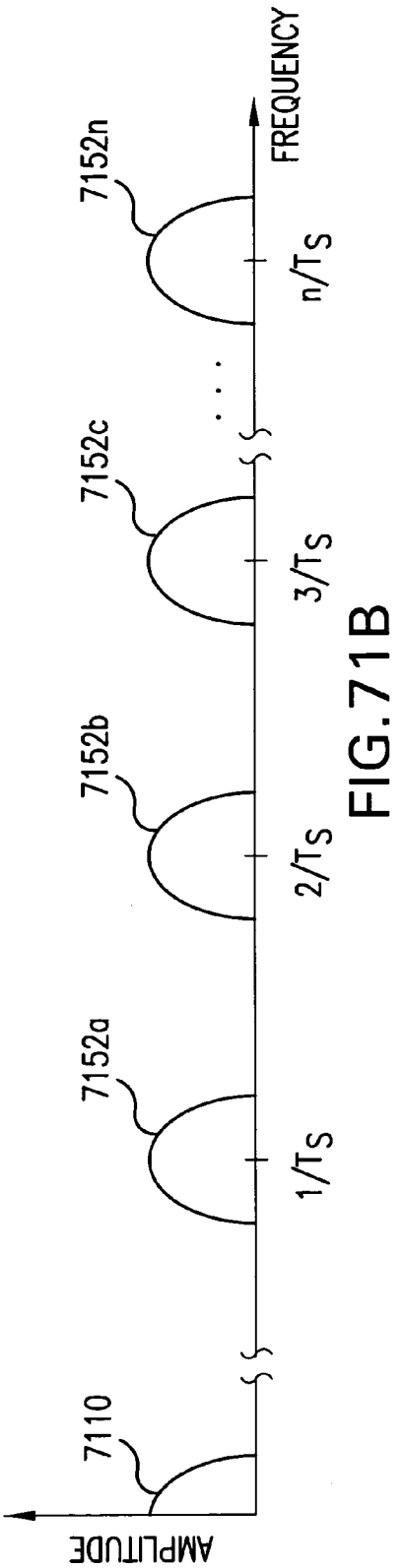


FIG.71B

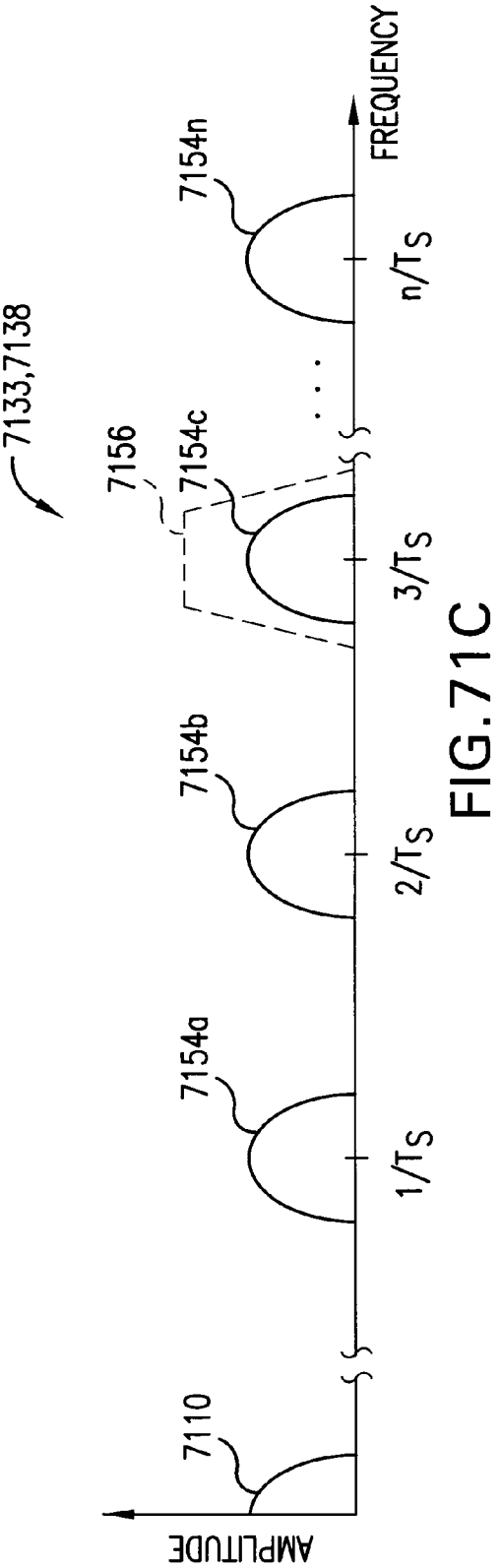


FIG.71C

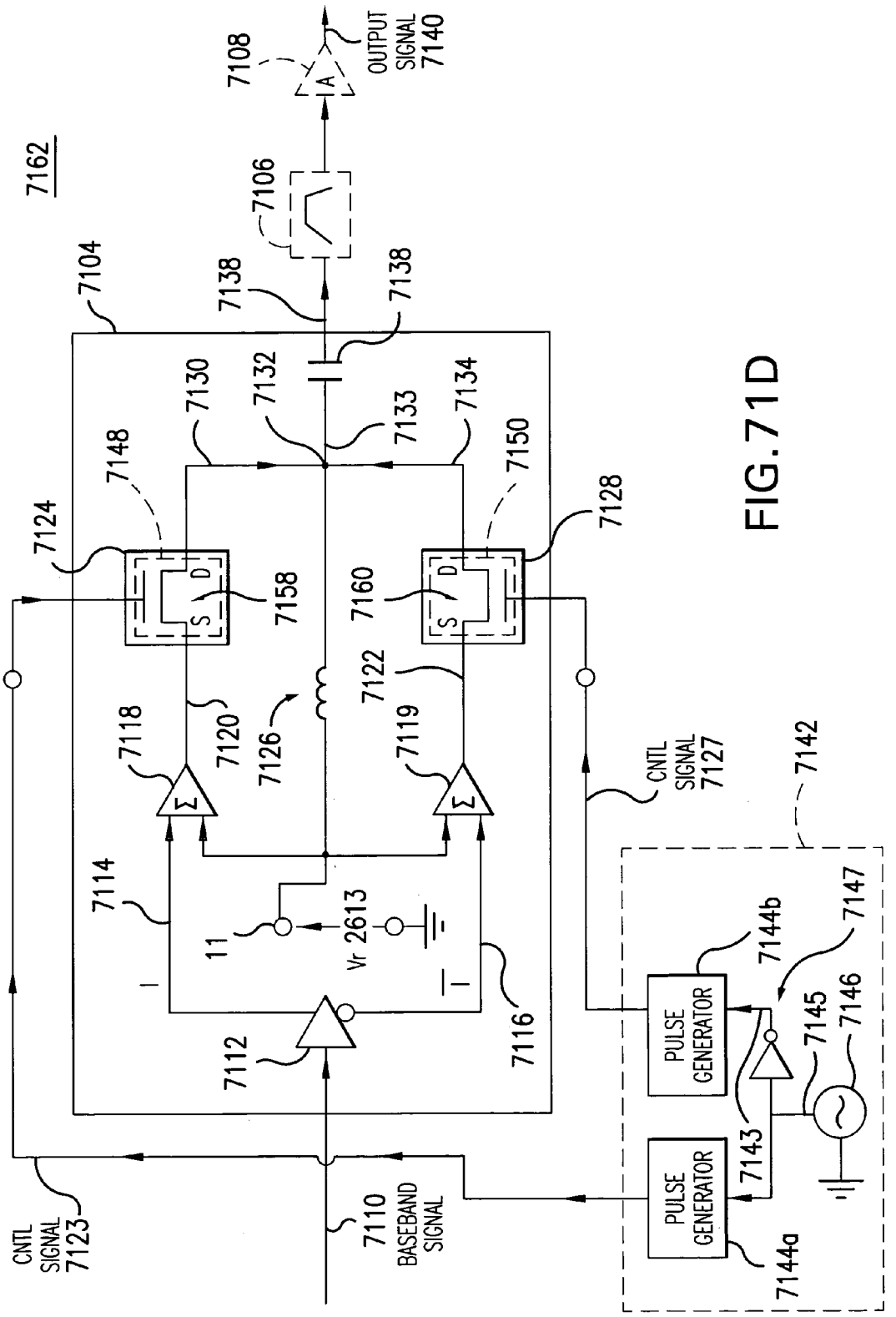

7162
7108
OUTPUT SIGNAL 7140
7106
7104
7138
7138
7130
7132
7133
7134
7148
7150
7124
7128
7158
7160
7122
7120
7126
7119
7118
7114
11
Vr 2613
7112
7116
CNTL SIGNAL 7127
7142
PULSE GENERATOR
PULSE GENERATOR
7144b
7147
7145
7146
7143
7144a
CNTL SIGNAL 7123
7110 BASEBAND SIGNAL

FIG. 71D

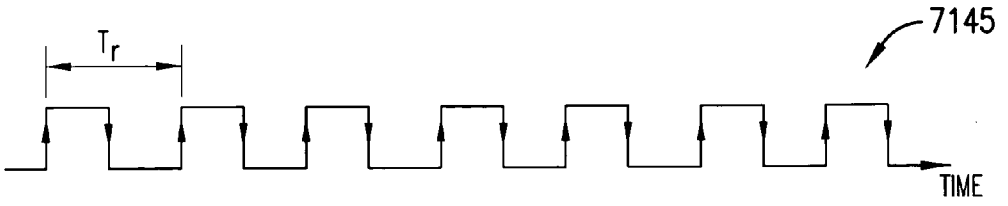


FIG.72A



FIG.72B



FIG.72C



FIG.72D

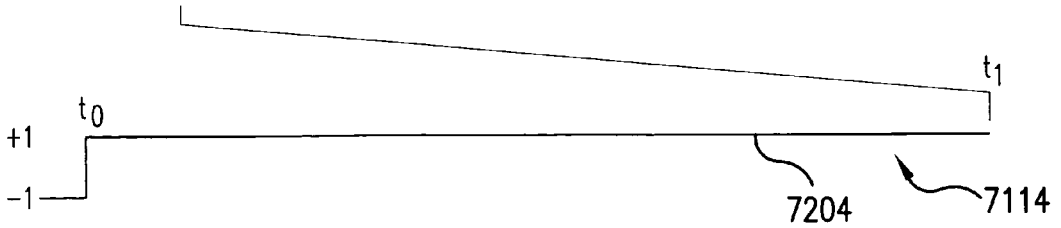


FIG.72E



FIG. 72F



FIG. 72G

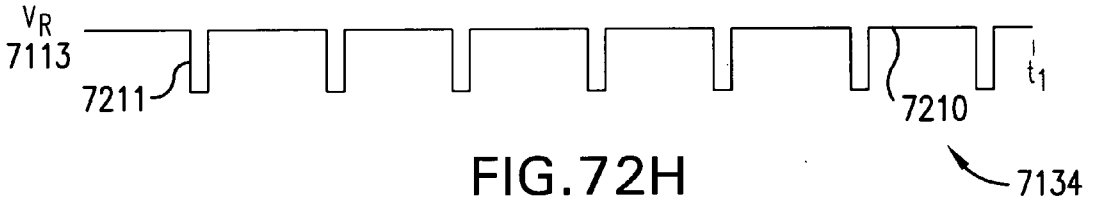


FIG. 72H

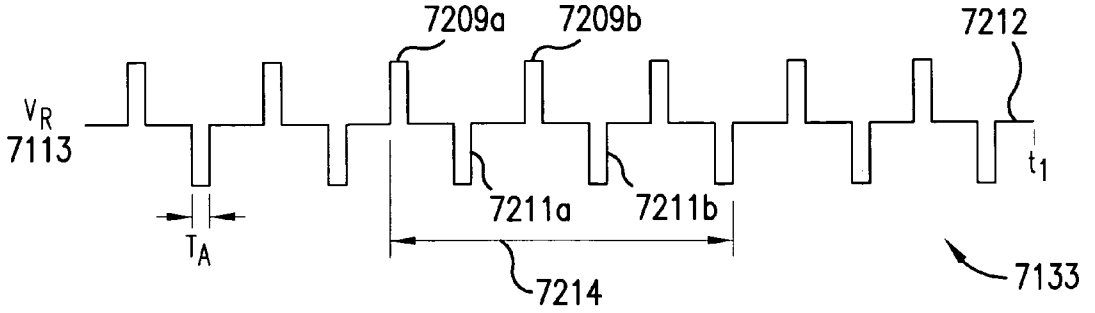


FIG. 72I

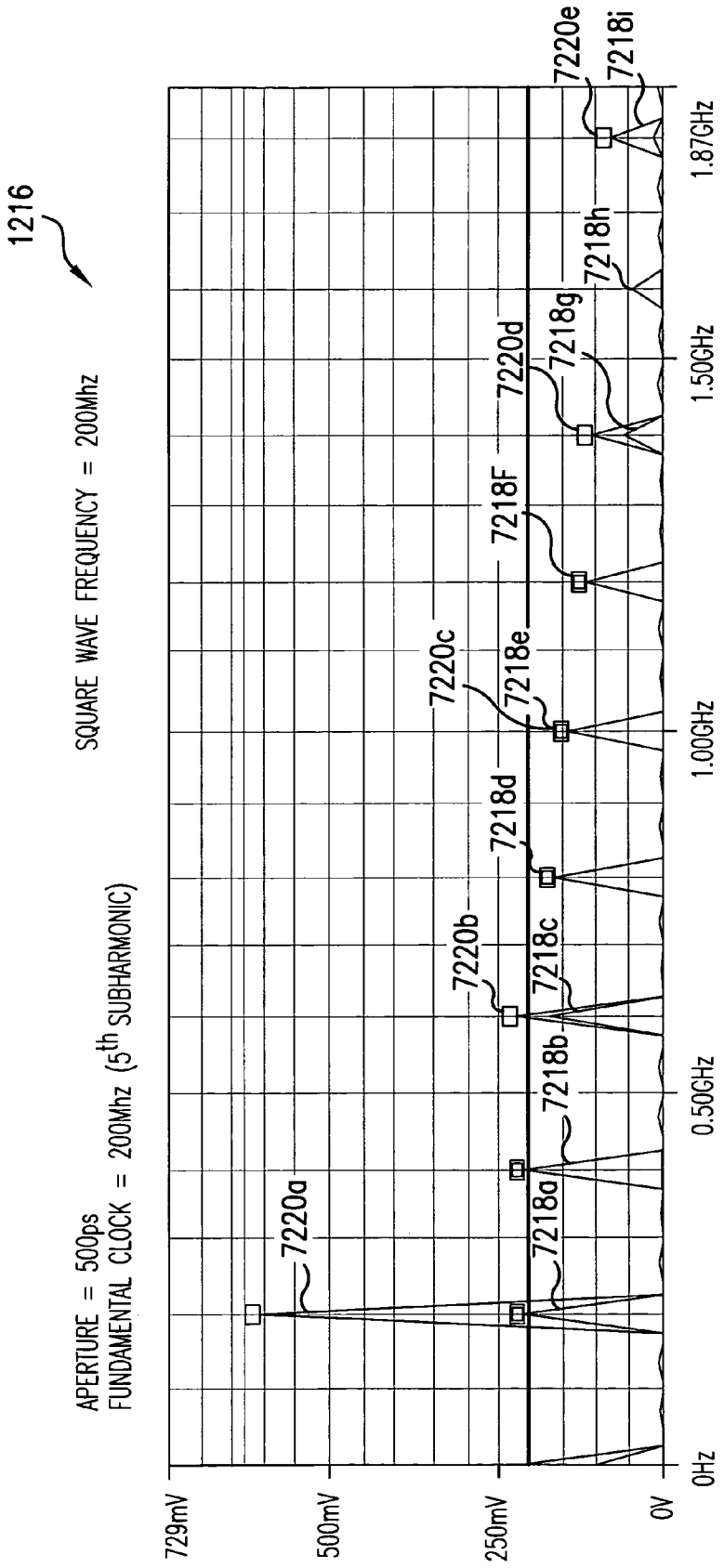

1216
SQUARE WAVE FREQUENCY = 200Mhz
APERTURE = 500ps
FUNDAMENTAL CLOCK = 200Mhz (5th SUBHARMONIC)
729mV
500mV
250mV
0V
0Hz
0.50GHz
1.00GHz
1.50GHz
1.87GHz
FREQUENCY
V
V (SQUARE_WAVE)
7220a
7220b
7220c
7220d
7220e
7218a
7218b
7218c
7218d
7218e
7218F
7218g
7218h
7218i

FIG. 72J

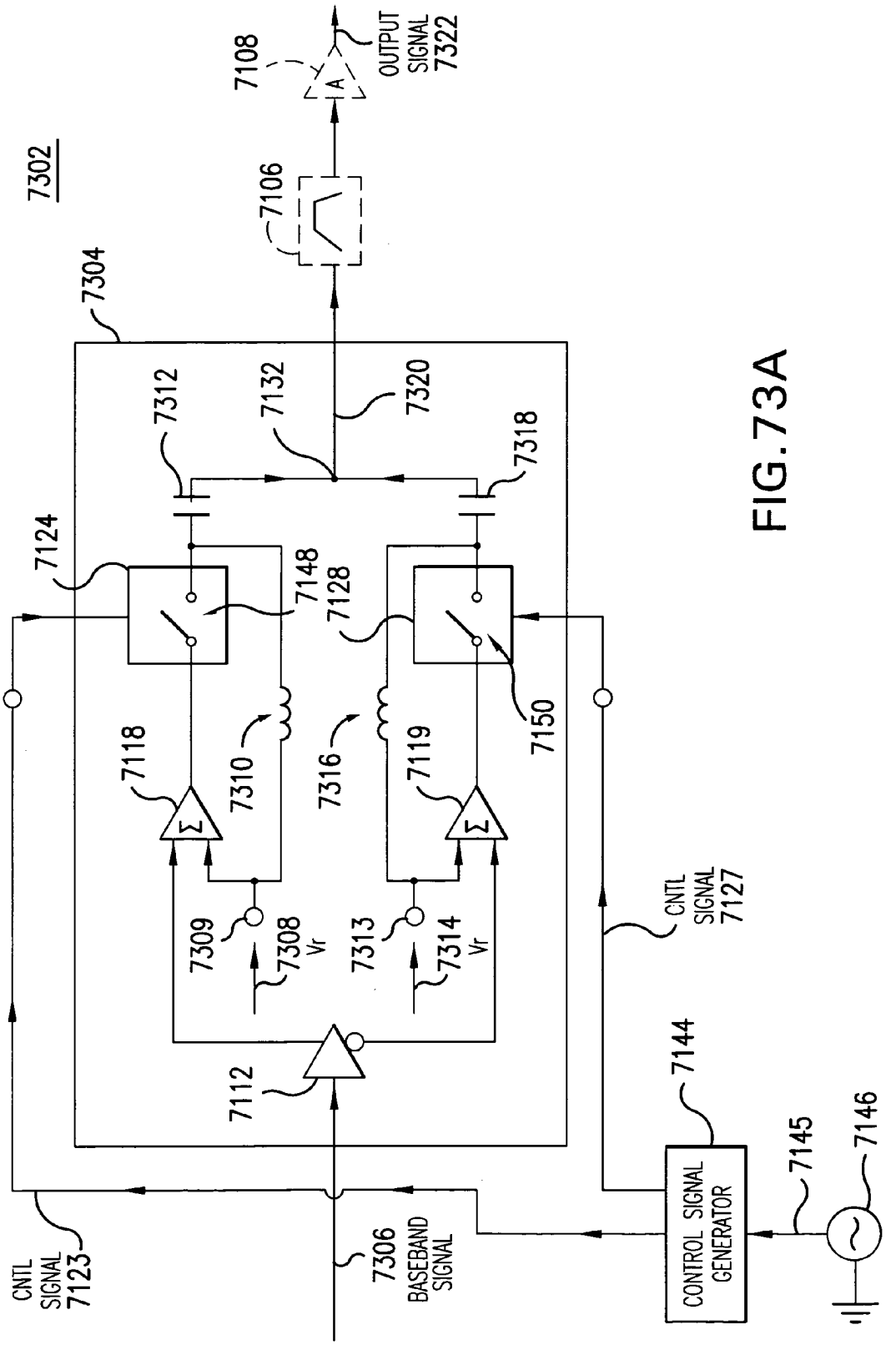

7302
7304
7108
A
OUTPUT SIGNAL 7322
7106
7312
7132
7320
7318
7124
7148
7128
7150
7118
7310
7316
7119
Σ
7309
7308
Vr
7313
7314
Vr
CNTL SIGNAL 7127
7112
7144
7145
7146
CONTROL SIGNAL GENERATOR
CNTL SIGNAL 7123
7306 BASEBAND SIGNAL

FIG. 73A

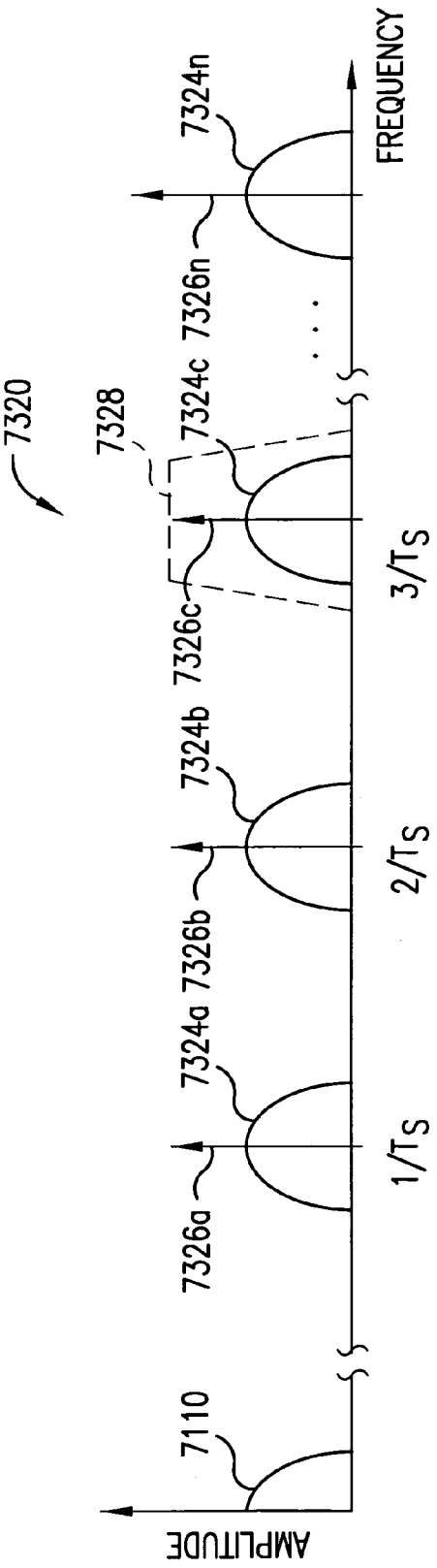

7320
7328
7324n
7326n
7324c
7326c
7324b
7326b
7324a
7326a
7110
FREQUENCY
AMPLITUDE
1/Ts
2/Ts
3/Ts

FIG. 73B

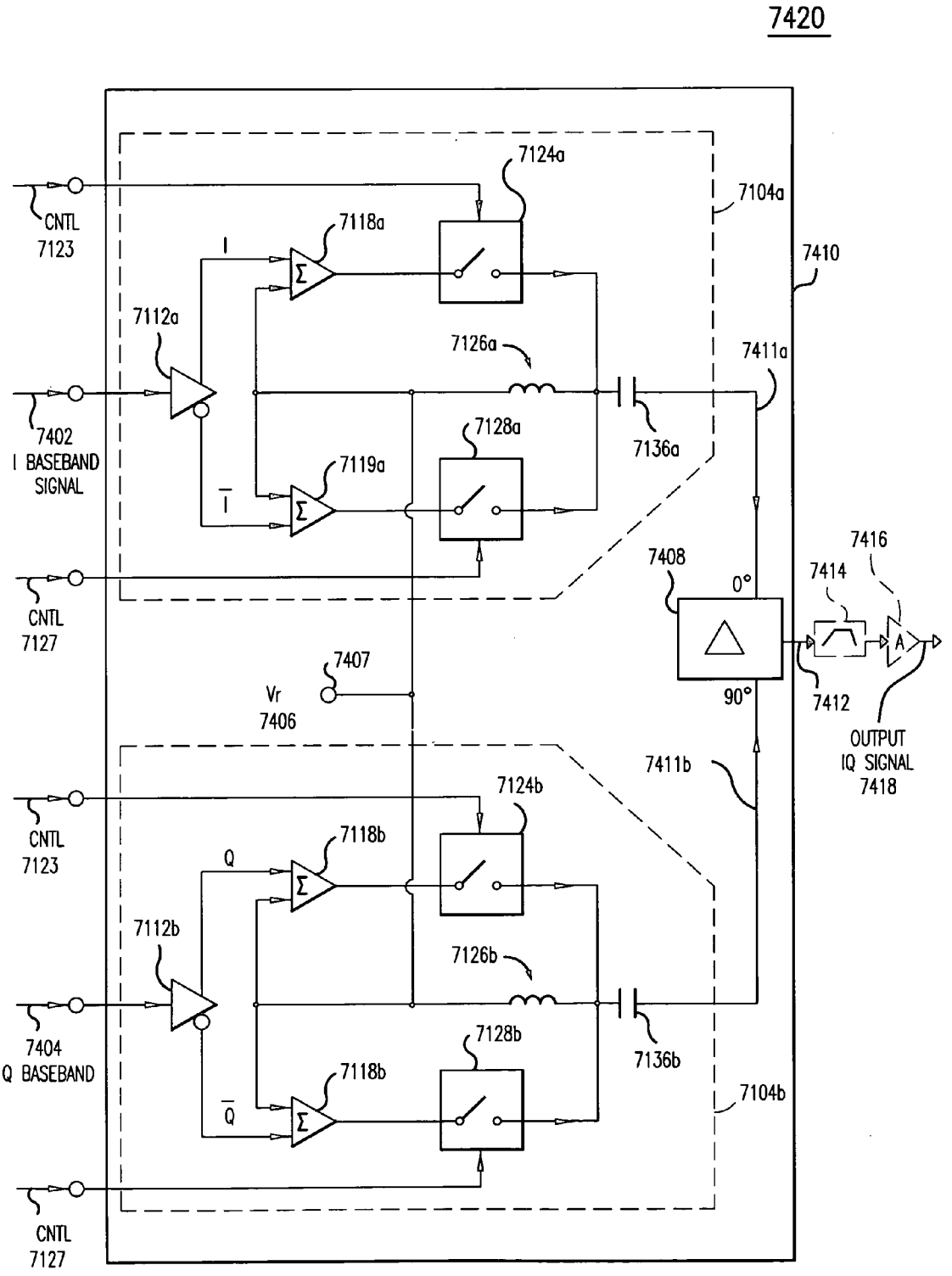

7420
7124a
7104a
7118a
7410
CNTL
7123
I
7112a
7126a
7411a
7402
I BASEBAND
SIGNAL
7128a
7136a
7119a
$\overline{I}$
7416
7408
7414
0°
CNTL
7127
7407
Vr
7406
90°
7412
OUTPUT
IQ SIGNAL
7418
7411b
7124b
CNTL
7123
7118b
Q
7112b
7126b
7404
Q BASEBAND
7128b
7136b
7118b
7104b
$\overline{Q}$
CNTL
7127

FIG.74

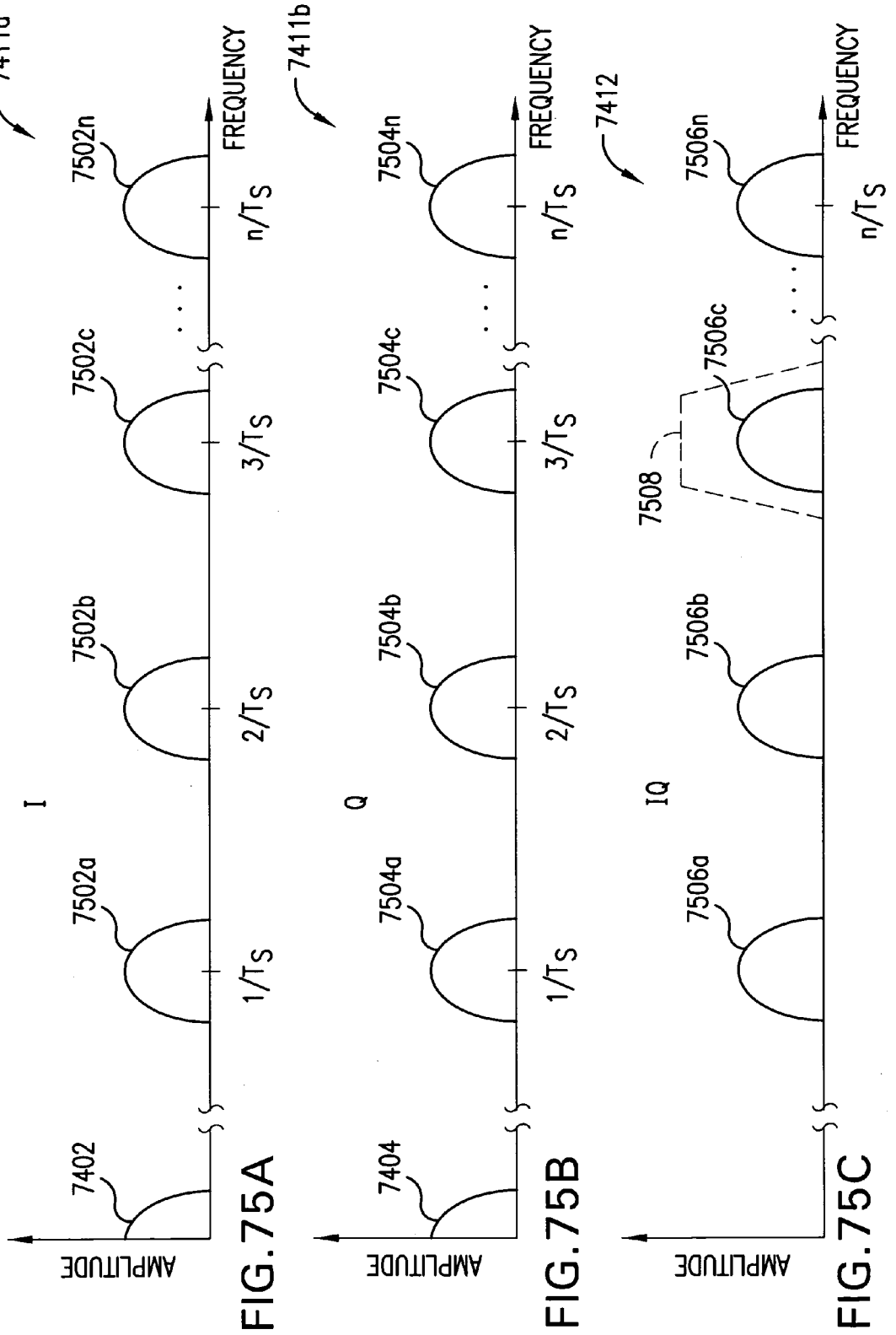


FIG. 75A

FIG. 75B

FIG. 75C

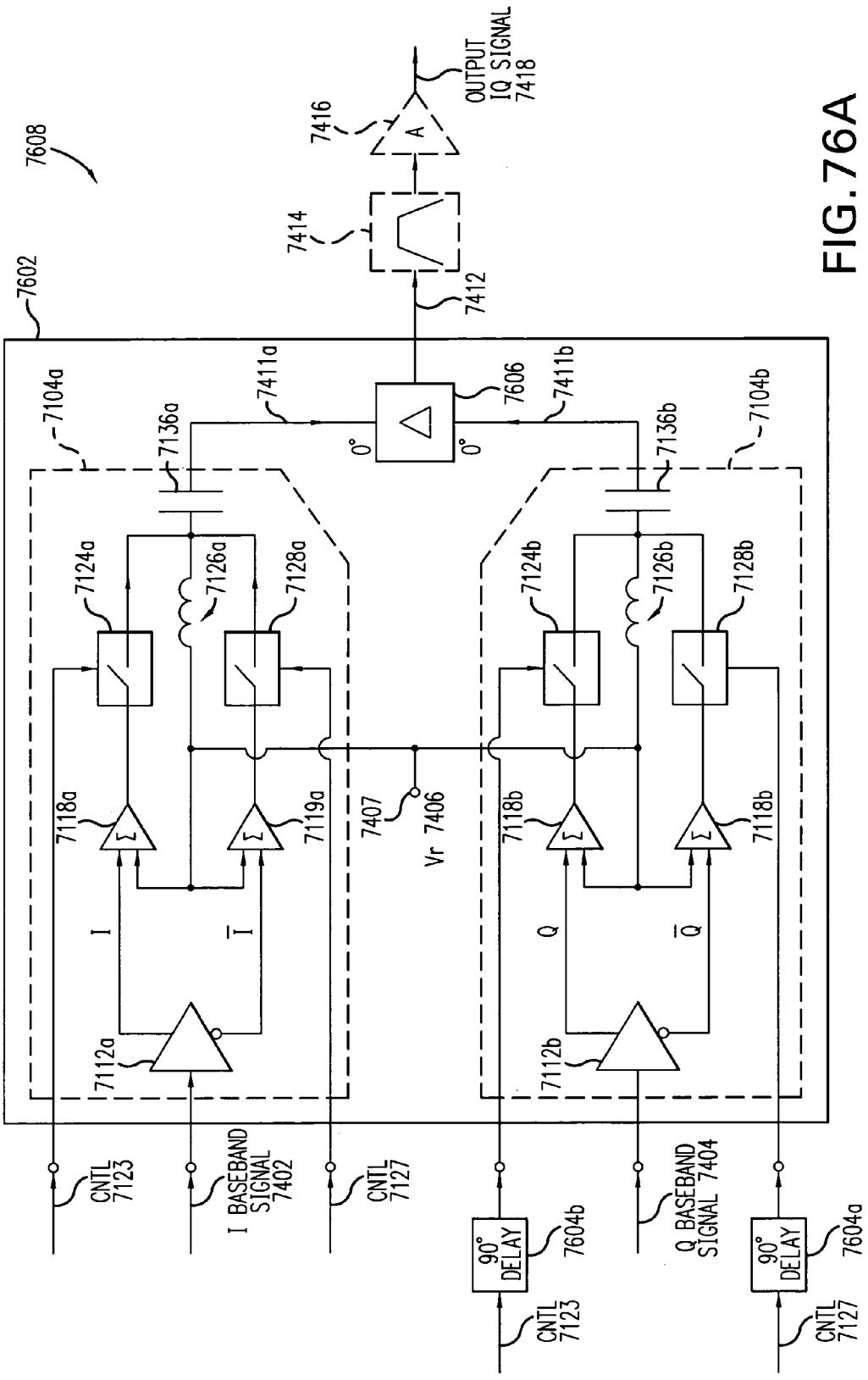

7608
7602
7416
7414
7412
OUTPUT IQ SIGNAL 7418
7104a
7104b
7136a
7136b
7411a
7411b
7606
0°
0°
7124a
7126a
7128a
7124b
7126b
7128b
7118a
7119a
7118b
7407
Vr 7406
I
Ī
Q
Q̄
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
90° DELAY 7604b
Q BASEBAND SIGNAL 7404
90° DELAY 7604a
CNTL 7123
CNTL 7127

FIG. 76A

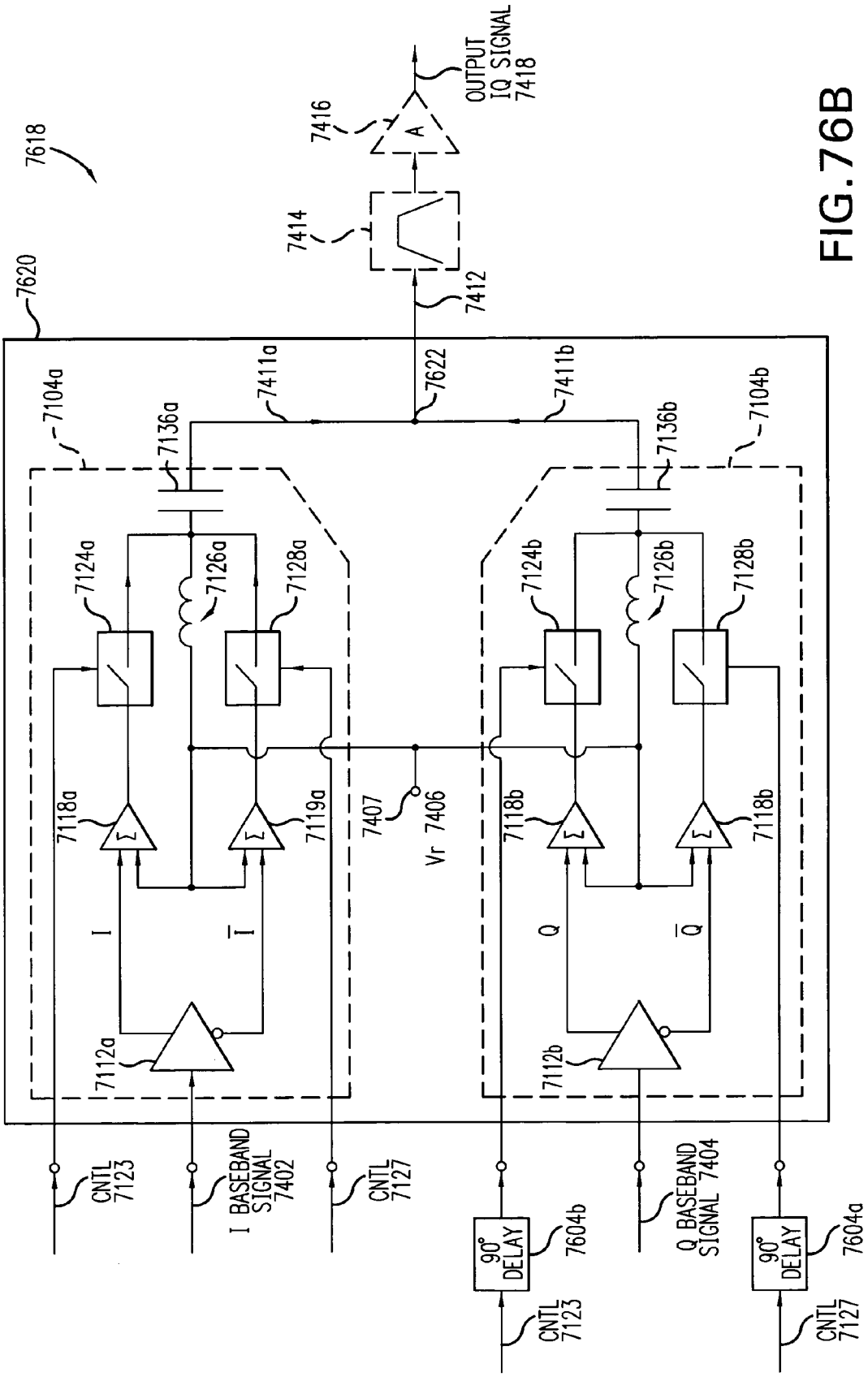

7618
7620
7416
A
OUTPUT IQ SIGNAL 7418
7414
7412
7622
7411a
7411b
7104a
7104b
7136a
7136b
7124a
7124b
7126a
7126b
7128a
7128b
7118a
7118b
7119a
7407
Vr 7406
I
Ī
Q
Q̄
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
90° DELAY
7604b
Q BASEBAND SIGNAL 7404
7604a

FIG. 76B

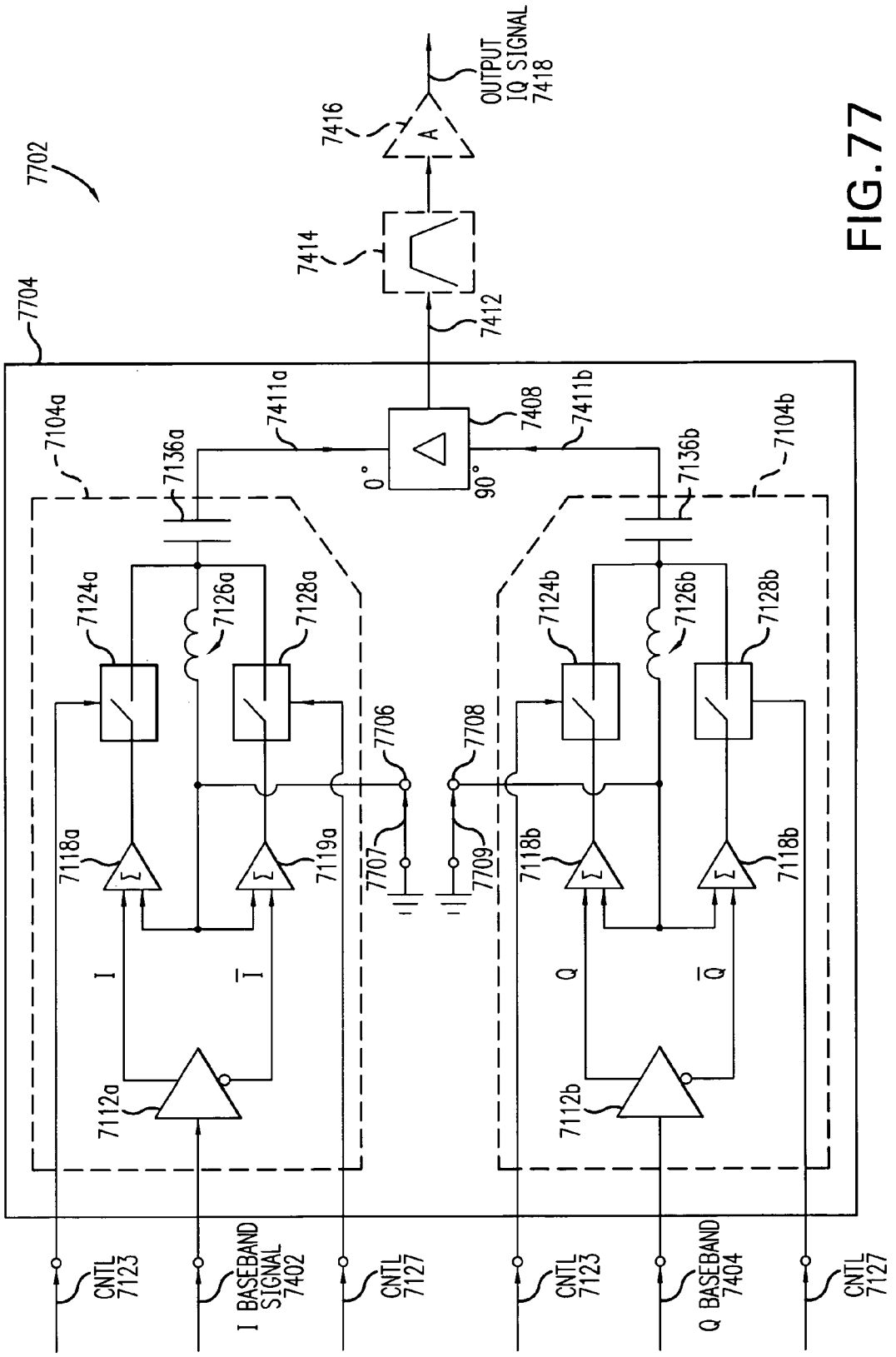

7702
7704
7416
A
OUTPUT IQ SIGNAL 7418
7414
7412
7104a
7136a
7411a
7408
7411b
0°
90°
7136b
7104b
7124a
7126a
7128a
7124b
7126b
7128b
7706
7708
7118a
Σ
7119a
7707
7709
7118b
I
Ī
Q
Q̄
7112a
7112b
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
CNTL 7123
Q BASEBAND 7404
CNTL 7127

FIG. 77

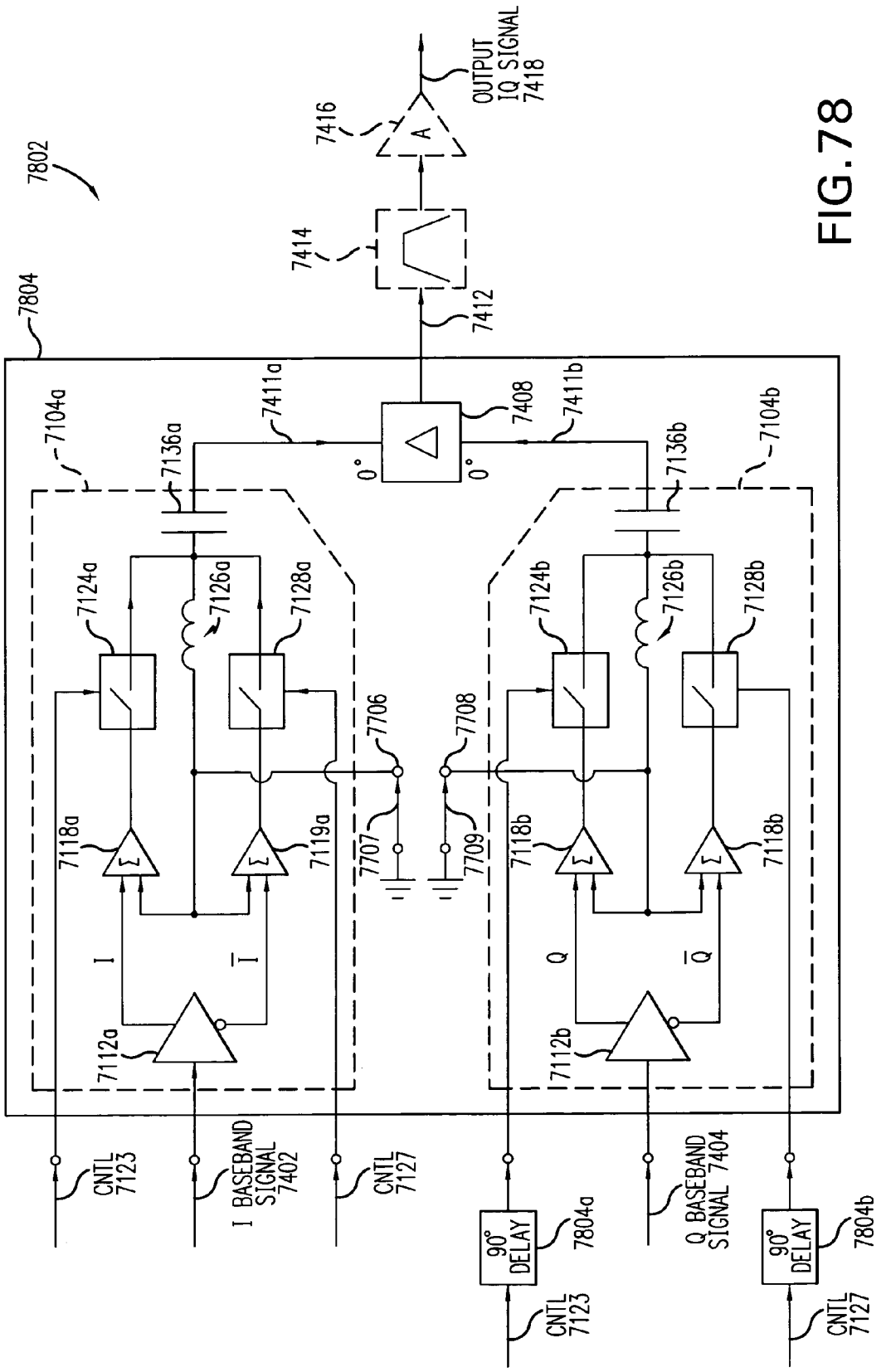

7802
7804
7104a
7104b
7136a
7136b
7411a
7411b
7408
7412
7414
7416
OUTPUT IQ SIGNAL 7418
0°
0°
7124a
7126a
7128a
7124b
7126b
7128b
7706
7708
7707
7709
7118a
7119a
7118b
7112a
7112b
I
Ī
Q
Q̄
CNTL 7123
I BASEBAND SIGNAL 7402
CNTL 7127
Q BASEBAND SIGNAL 7404
90° DELAY
7804a
7804b

FIG. 78

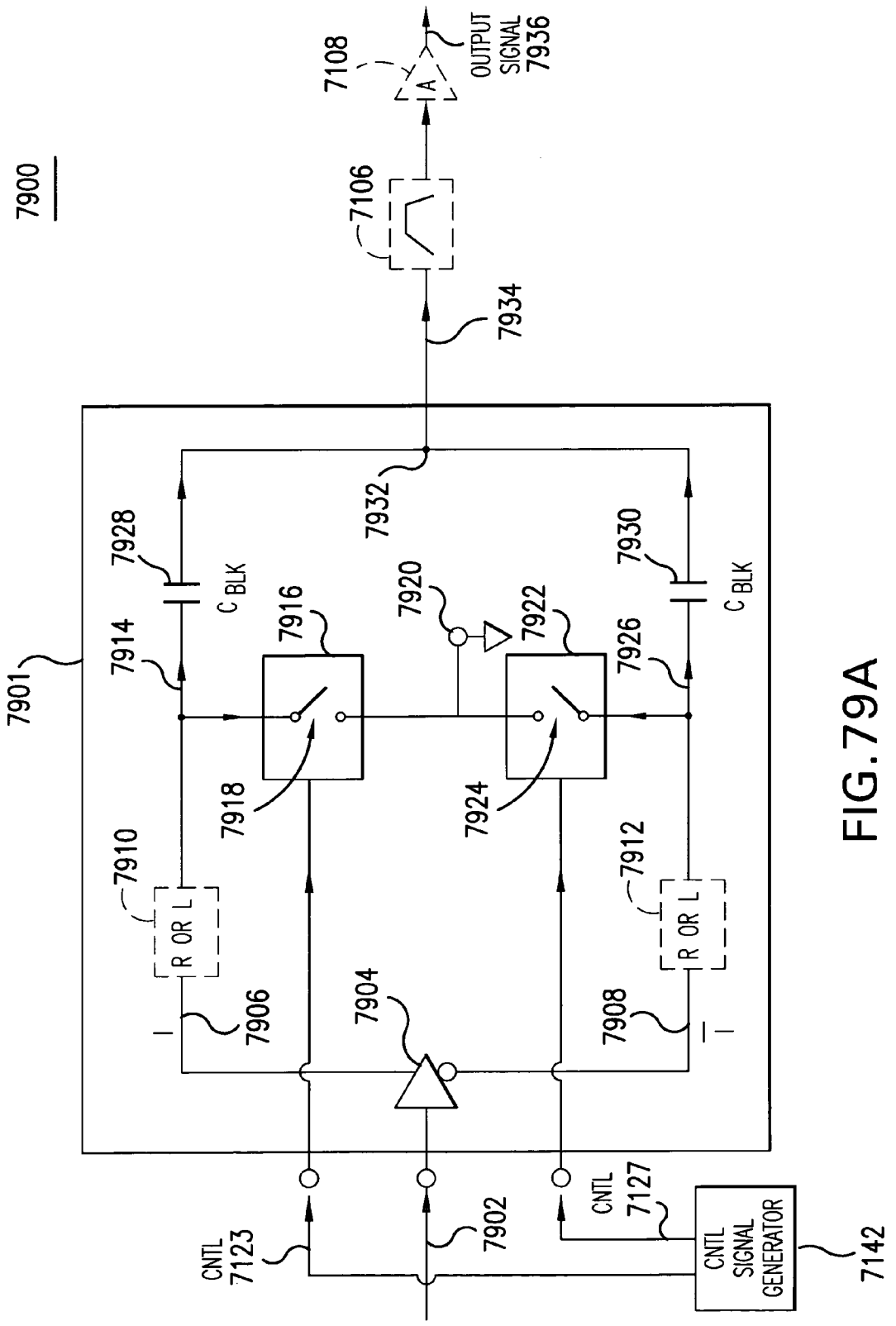

7900
7108
A
OUTPUT SIGNAL 7936
7106
7934
7932
7928
C BLK
7930
C BLK
7920
7916
7922
7914
7926
7901
7918
7924
7910
R OR L
7912
R OR L
7906
7904
7908
CNTL 7123
7902
CNTL 7127
CNTL SIGNAL GENERATOR
7142

FIG. 79A

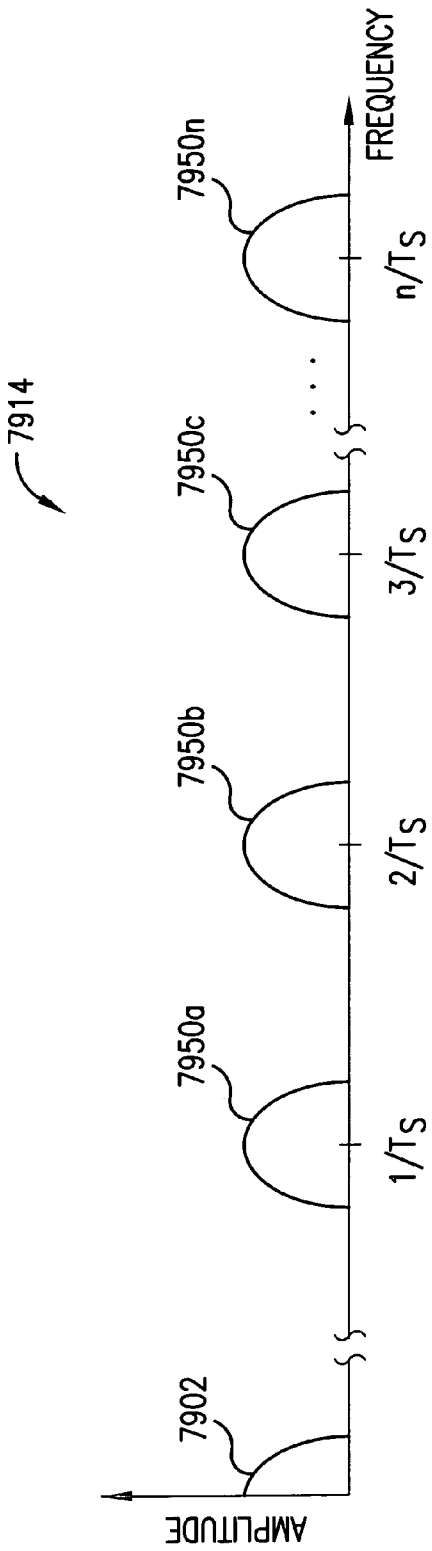


FIG. 79B

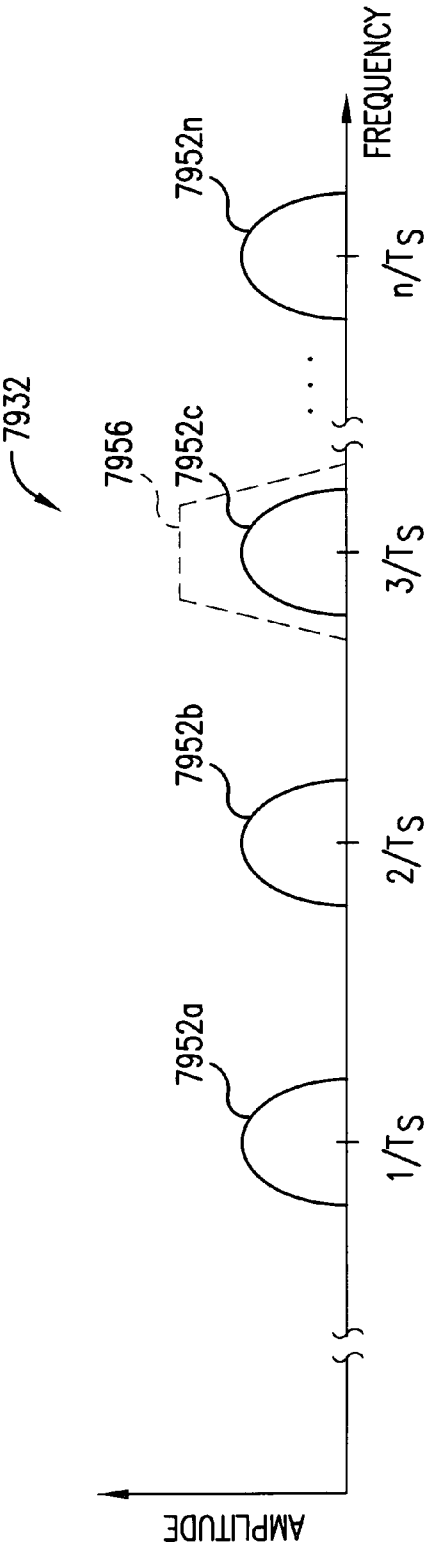


FIG. 79C

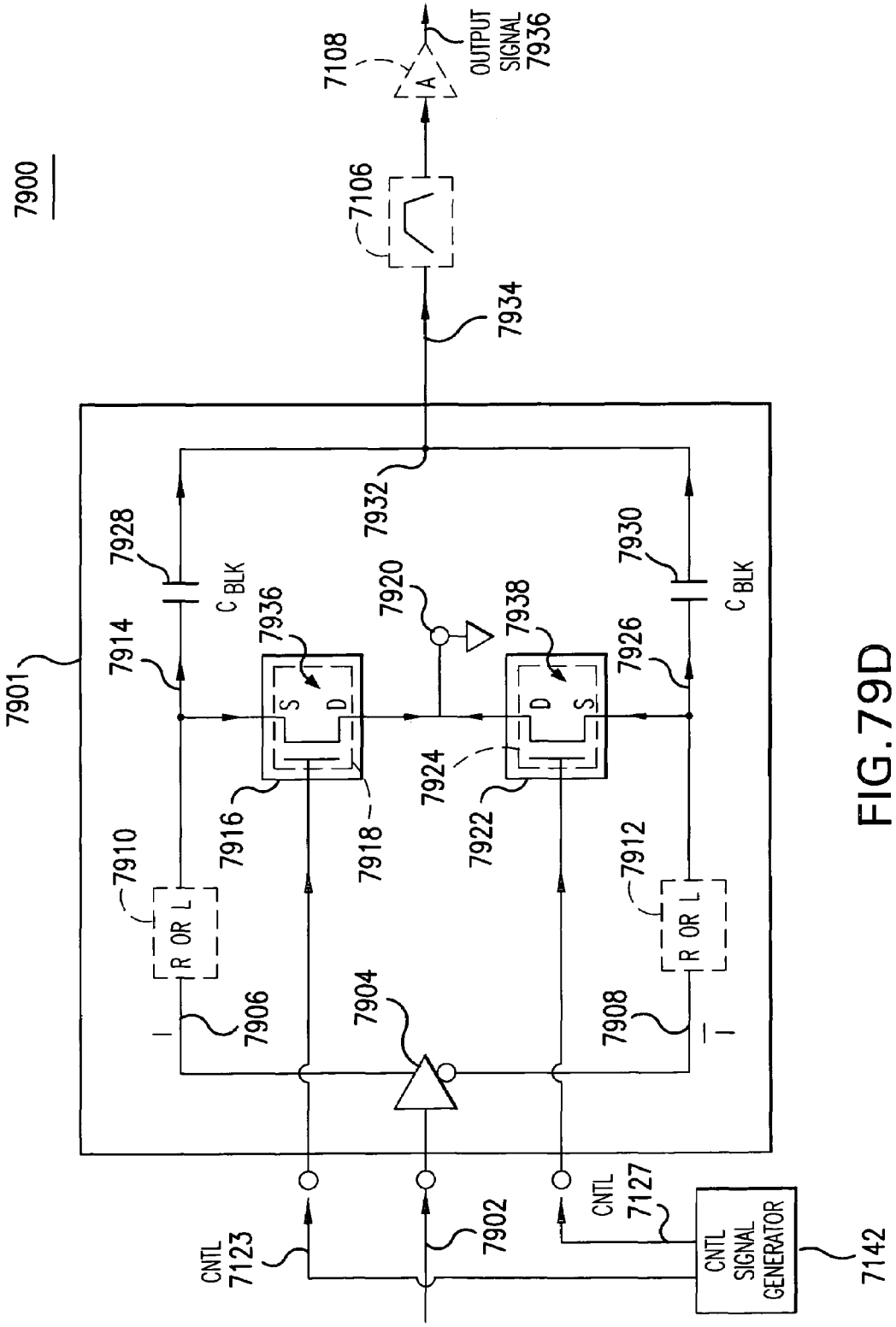

7900
7108
A
OUTPUT SIGNAL 7936
7106
7934
7901
7928
C BLK
7914
7936
S
D
7920
7938
D
S
7926
7930
C BLK
7932
7916
7918
7924
7922
7910
R OR L
7906
7904
7908
7912
R OR L
CNTL 7123
7902
CNTL 7127
CNTL SIGNAL GENERATOR
7142

FIG. 79D

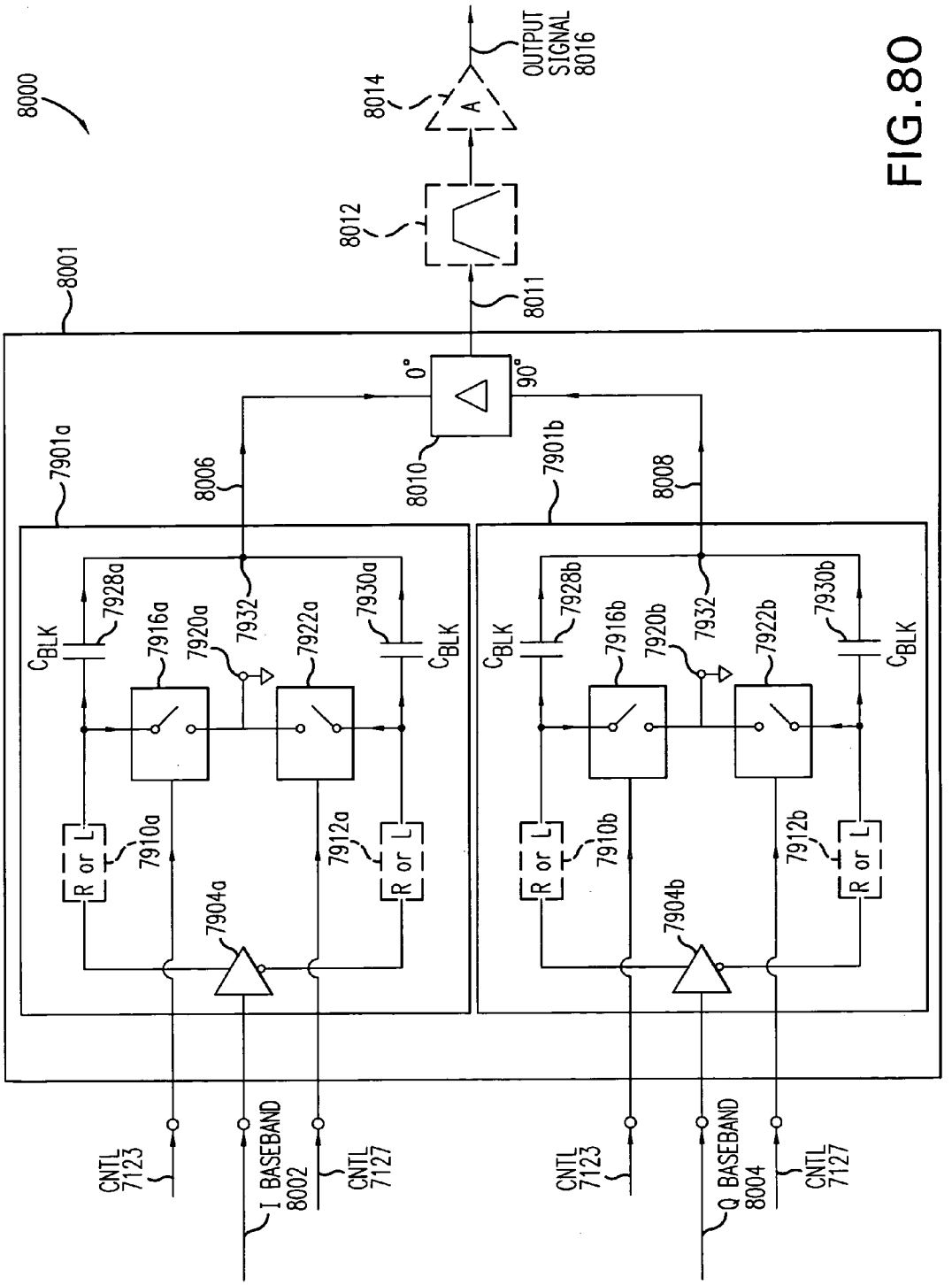

8000
8014
OUTPUT SIGNAL 8016
8012
8001
8011
0°
90°
8010
7901a
7901b
8006
8008
7928a
7916a
7920a
7932
7922a
7930a
C_{BLK}
7910a
7912a
R or L
7904a
7928b
7916b
7920b
7922b
7930b
7910b
7912b
7904b
CNTL 7123
I BASEBAND 8002
CNTL 7127
Q BASEBAND 8004

FIG.80

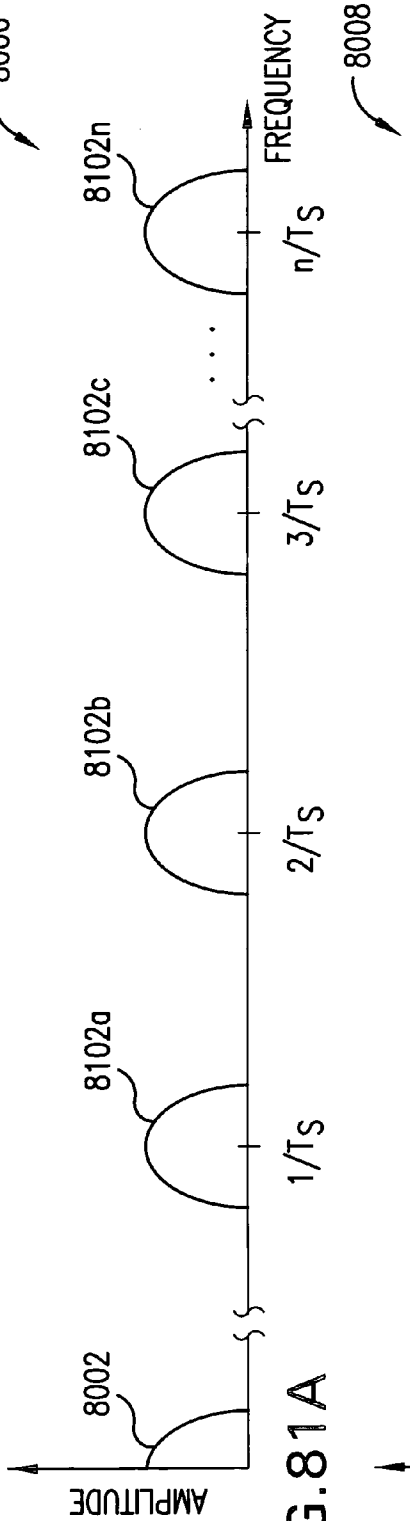


FIG.81A

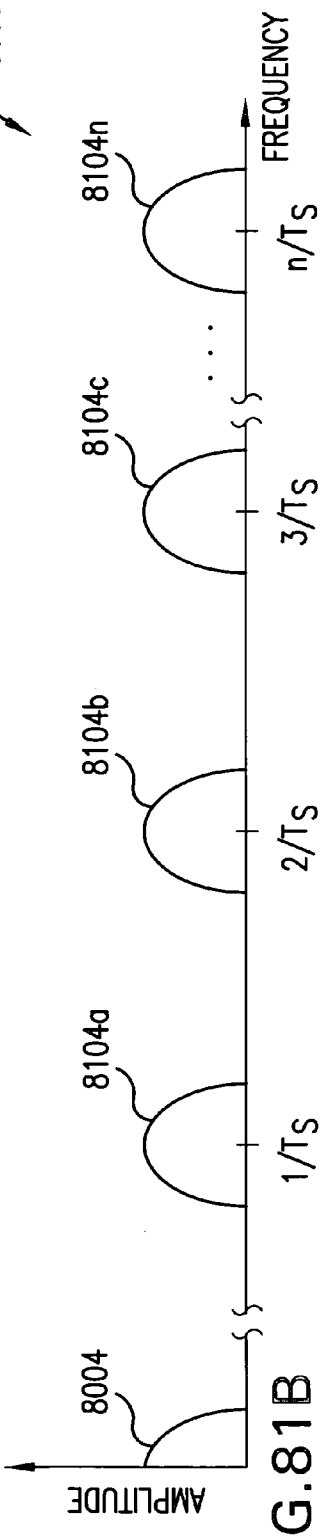


FIG.81B

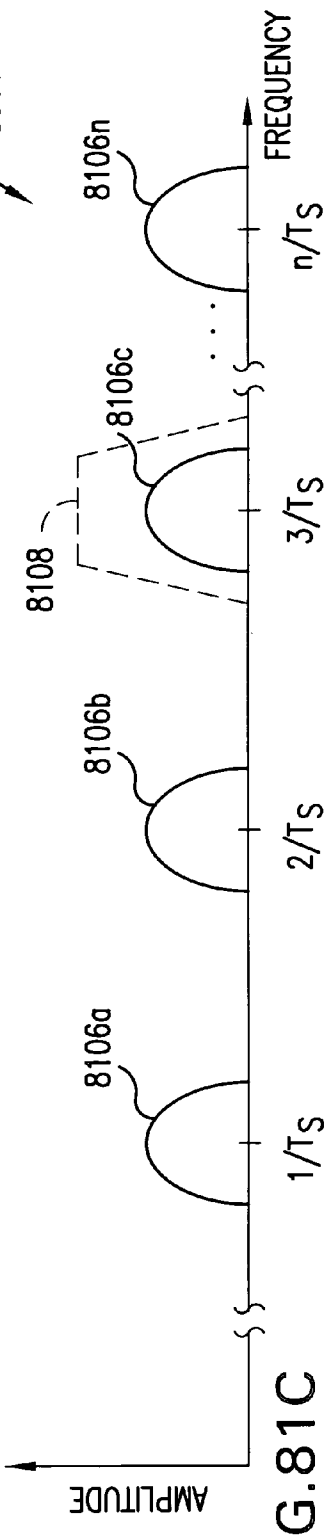


FIG.81C

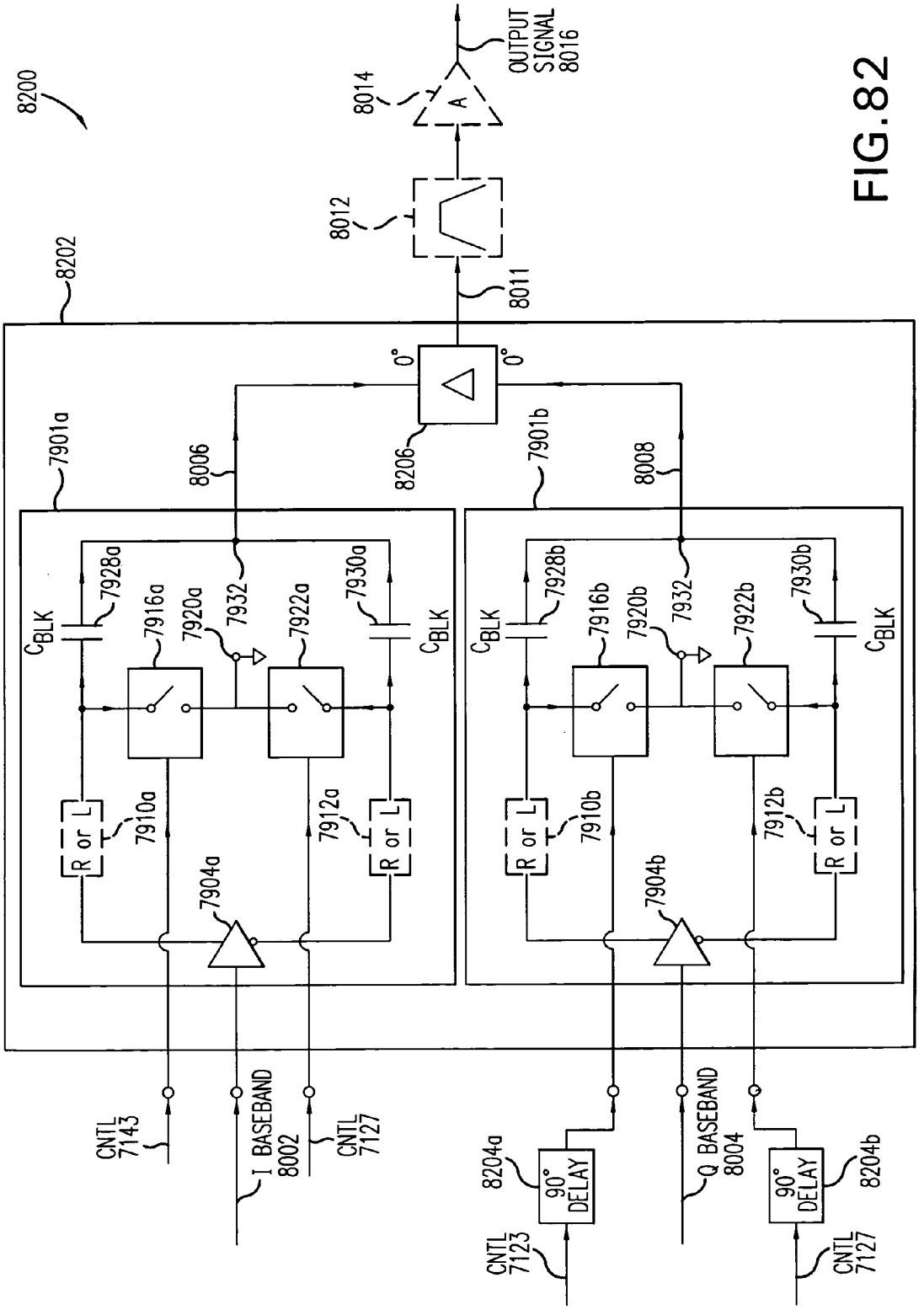

8200
8202
8014
A
OUTPUT SIGNAL 8016
8012
8011
0°
0°
8206
8006
8008
7901a
7901b
C_{BLK}
7928a
7916a
7920a
7932
7922a
7930a
7928b
7916b
7920b
7922b
7930b
R or L
7910a
7912a
7904a
7910b
7912b
7904b
CNTL 7143
I BASEBAND 8002
CNTL 7127
Q BASEBAND 8004
8204a
8204b
90° DELAY
CNTL 7123

FIG.82

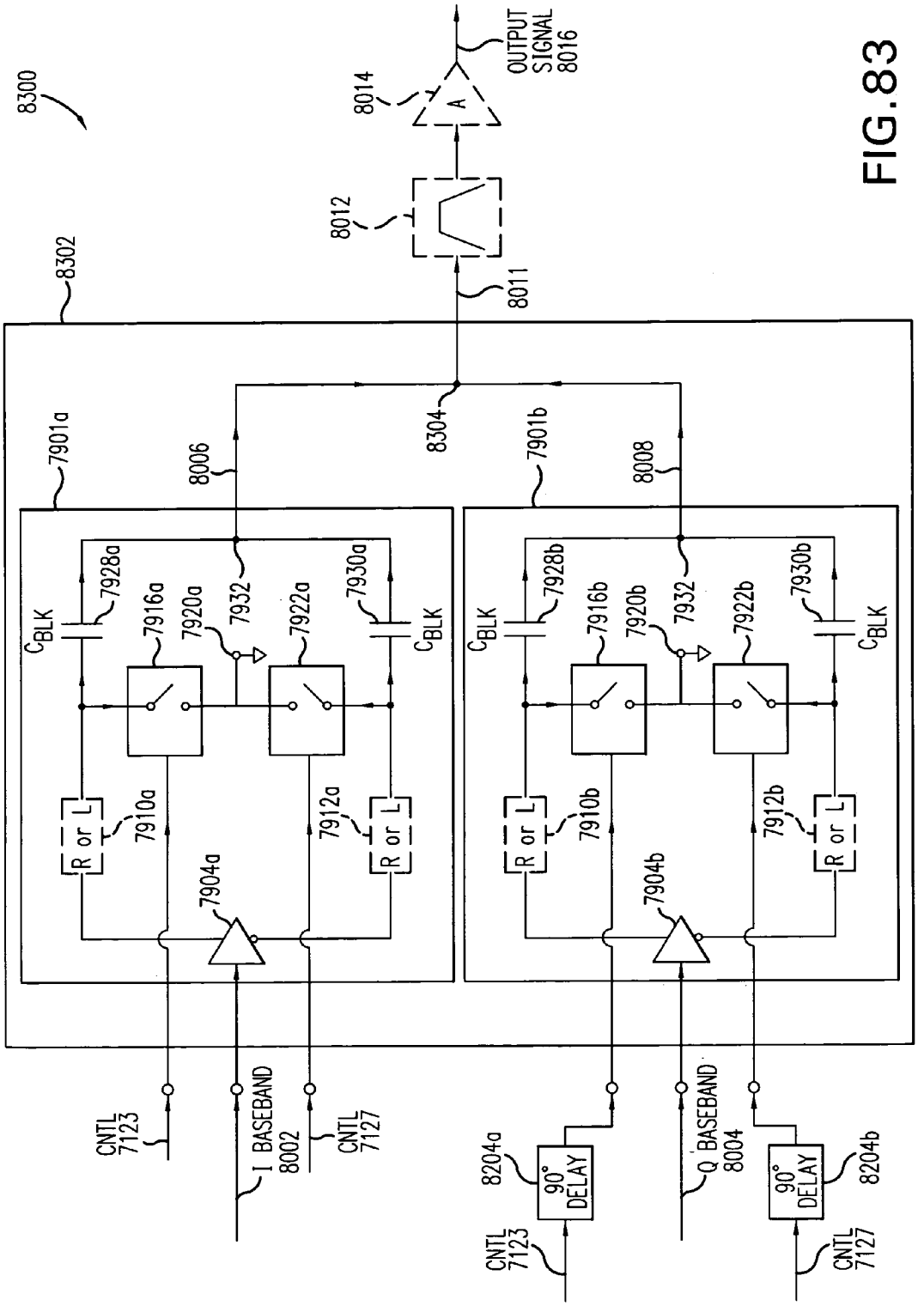

8300
8014
OUTPUT SIGNAL 8016
8012
8011
8302
8304
7901a
7901b
8006
8008
7928a
7916a
7920a
7932
7922a
7930a
7928b
7916b
7920b
7932
7922b
7930b
C_BLK
R or L
7910a
7912a
7904a
7910b
7912b
7904b
CNTL 7123
I BASEBAND 8002
CNTL 7127
Q BASEBAND 8004
8204a
8204b
90° DELAY

FIG.83

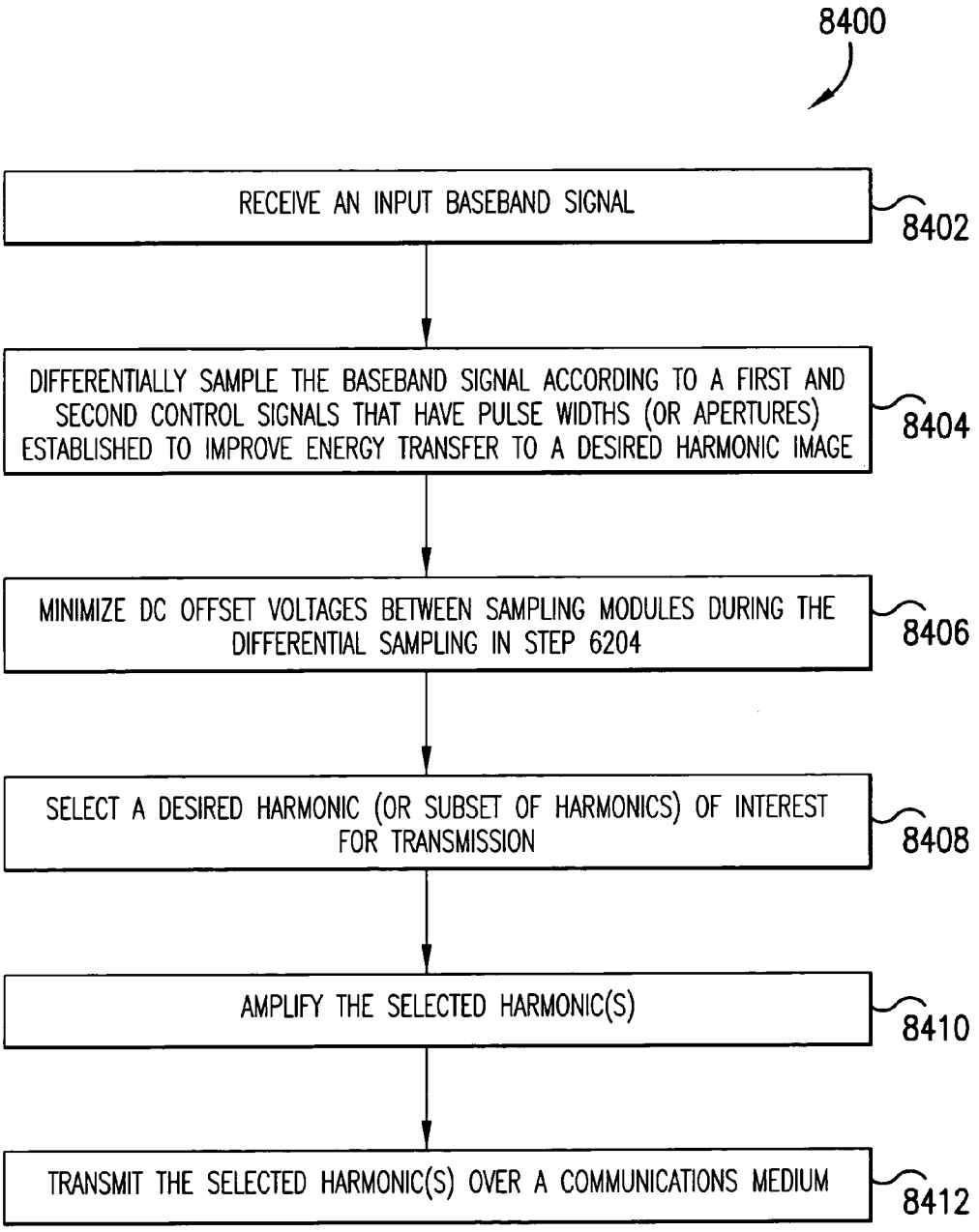

8400
RECEIVE AN INPUT BASEBAND SIGNAL
8402
DIFFERENTIALLY SAMPLE THE BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE
8404
MINIMIZE DC OFFSET VOLTAGES BETWEEN SAMPLING MODULES DURING THE DIFFERENTIAL SAMPLING IN STEP 6204
8406
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8408
AMPLIFY THE SELECTED HARMONIC(S)
8410
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8412

FIG.84

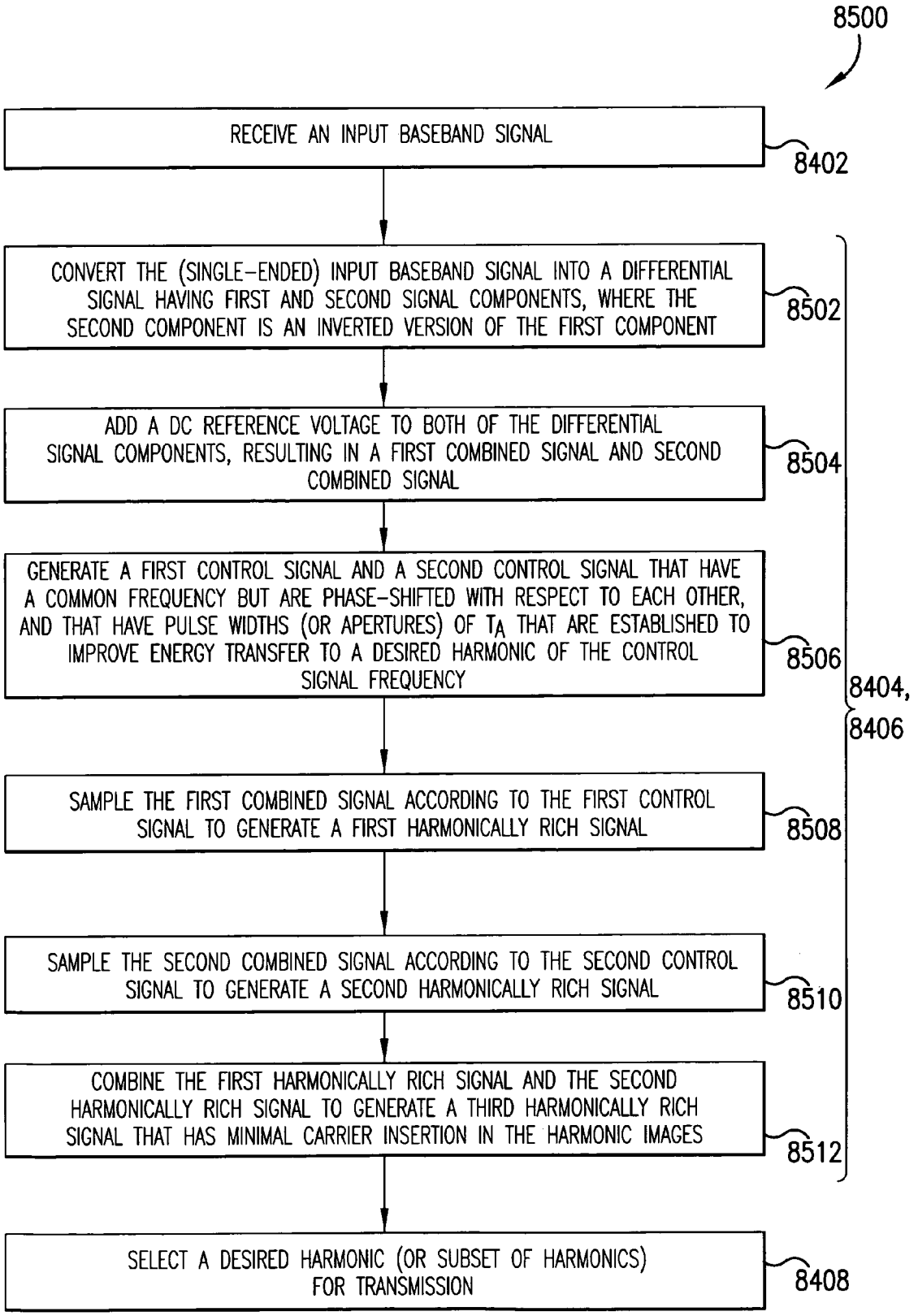

8500
RECEIVE AN INPUT BASEBAND SIGNAL
8402
CONVERT THE (SINGLE-ENDED) INPUT BASEBAND SIGNAL INTO A DIFFERENTIAL SIGNAL HAVING FIRST AND SECOND SIGNAL COMPONENTS, WHERE THE SECOND COMPONENT IS AN INVERTED VERSION OF THE FIRST COMPONENT
8502
ADD A DC REFERENCE VOLTAGE TO BOTH OF THE DIFFERENTIAL SIGNAL COMPONENTS, RESULTING IN A FIRST COMBINED SIGNAL AND SECOND COMBINED SIGNAL
8504
GENERATE A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL THAT HAVE A COMMON FREQUENCY BUT ARE PHASE-SHIFTED WITH RESPECT TO EACH OTHER, AND THAT HAVE PULSE WIDTHS (OR APERTURES) OF T_A THAT ARE ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC OF THE CONTROL SIGNAL FREQUENCY
8506
8404, 8406
SAMPLE THE FIRST COMBINED SIGNAL ACCORDING TO THE FIRST CONTROL SIGNAL TO GENERATE A FIRST HARMONICALLY RICH SIGNAL
8508
SAMPLE THE SECOND COMBINED SIGNAL ACCORDING TO THE SECOND CONTROL SIGNAL TO GENERATE A SECOND HARMONICALLY RICH SIGNAL
8510
COMBINE THE FIRST HARMONICALLY RICH SIGNAL AND THE SECOND HARMONICALLY RICH SIGNAL TO GENERATE A THIRD HARMONICALLY RICH SIGNAL THAT HAS MINIMAL CARRIER INSERTION IN THE HARMONIC IMAGES
8512
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) FOR TRANSMISSION
8408

FIG.85

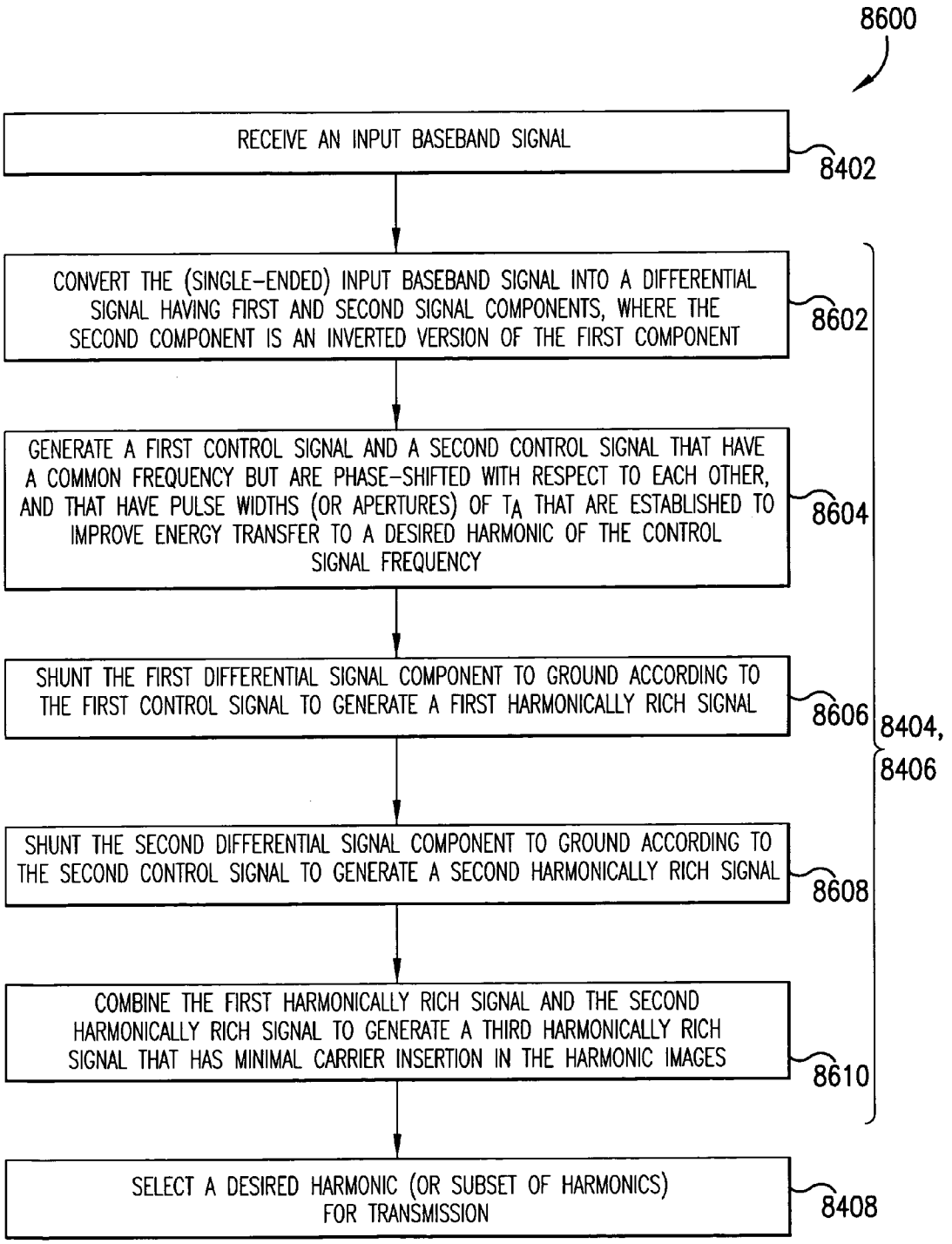

8600
RECEIVE AN INPUT BASEBAND SIGNAL
8402
CONVERT THE (SINGLE-ENDED) INPUT BASEBAND SIGNAL INTO A DIFFERENTIAL SIGNAL HAVING FIRST AND SECOND SIGNAL COMPONENTS, WHERE THE SECOND COMPONENT IS AN INVERTED VERSION OF THE FIRST COMPONENT
8602
GENERATE A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL THAT HAVE A COMMON FREQUENCY BUT ARE PHASE-SHIFTED WITH RESPECT TO EACH OTHER, AND THAT HAVE PULSE WIDTHS (OR APERTURES) OF T_A THAT ARE ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC OF THE CONTROL SIGNAL FREQUENCY
8604
SHUNT THE FIRST DIFFERENTIAL SIGNAL COMPONENT TO GROUND ACCORDING TO THE FIRST CONTROL SIGNAL TO GENERATE A FIRST HARMONICALLY RICH SIGNAL
8606
SHUNT THE SECOND DIFFERENTIAL SIGNAL COMPONENT TO GROUND ACCORDING TO THE SECOND CONTROL SIGNAL TO GENERATE A SECOND HARMONICALLY RICH SIGNAL
8608
COMBINE THE FIRST HARMONICALLY RICH SIGNAL AND THE SECOND HARMONICALLY RICH SIGNAL TO GENERATE A THIRD HARMONICALLY RICH SIGNAL THAT HAS MINIMAL CARRIER INSERTION IN THE HARMONIC IMAGES
8610
8404, 8406
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) FOR TRANSMISSION
8408

FIG.86

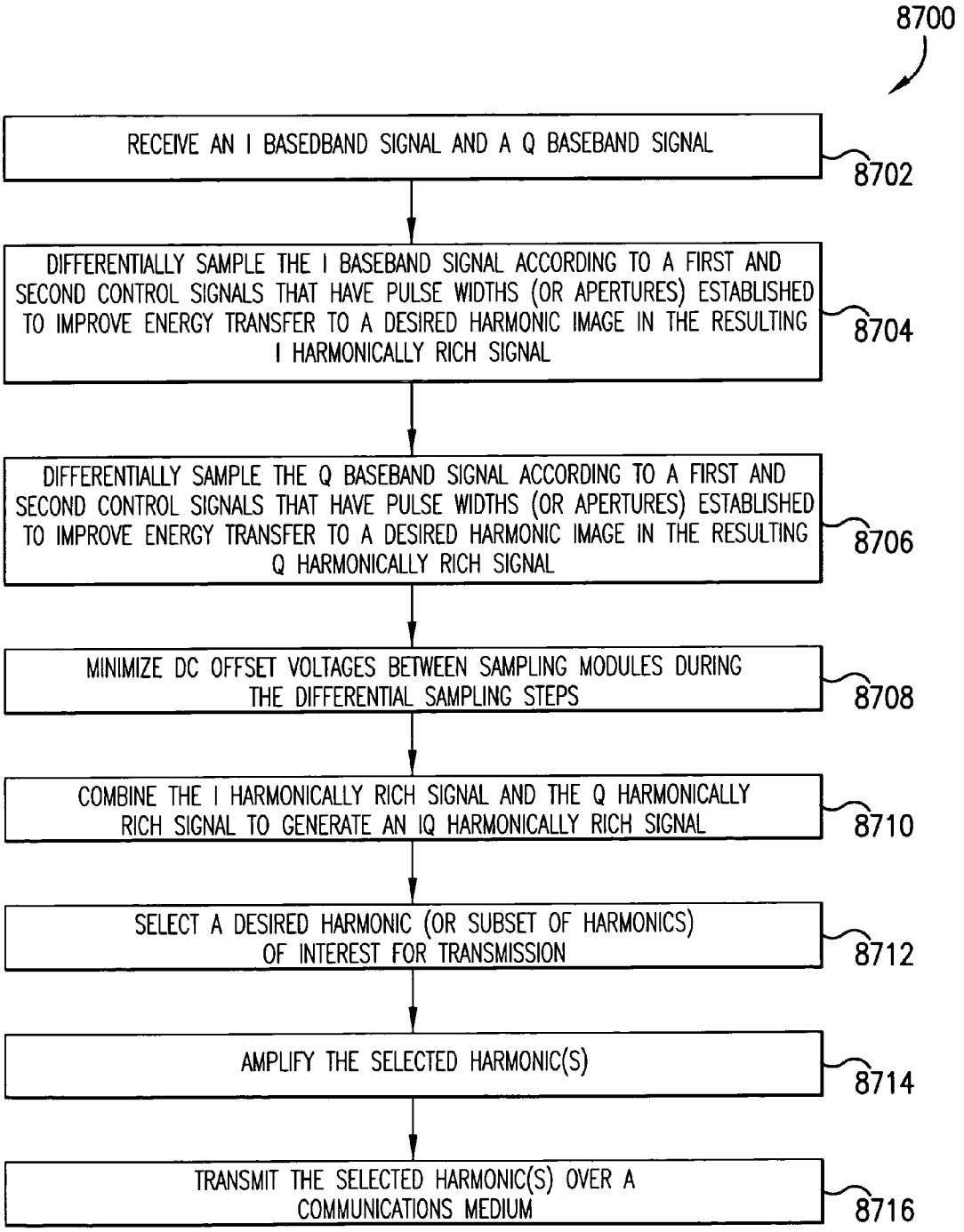

8700
RECEIVE AN I BASEDBAND SIGNAL AND A Q BASEBAND SIGNAL
8702
DIFFERENTIALLY SAMPLE THE I BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING I HARMONICALLY RICH SIGNAL
8704
DIFFERENTIALLY SAMPLE THE Q BASEBAND SIGNAL ACCORDING TO A FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING Q HARMONICALLY RICH SIGNAL
8706
MINIMIZE DC OFFSET VOLTAGES BETWEEN SAMPLING MODULES DURING THE DIFFERENTIAL SAMPLING STEPS
8708
COMBINE THE I HARMONICALLY RICH SIGNAL AND THE Q HARMONICALLY RICH SIGNAL TO GENERATE AN IQ HARMONICALLY RICH SIGNAL
8710
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8712
AMPLIFY THE SELECTED HARMONIC(S)
8714
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8716

FIG.87

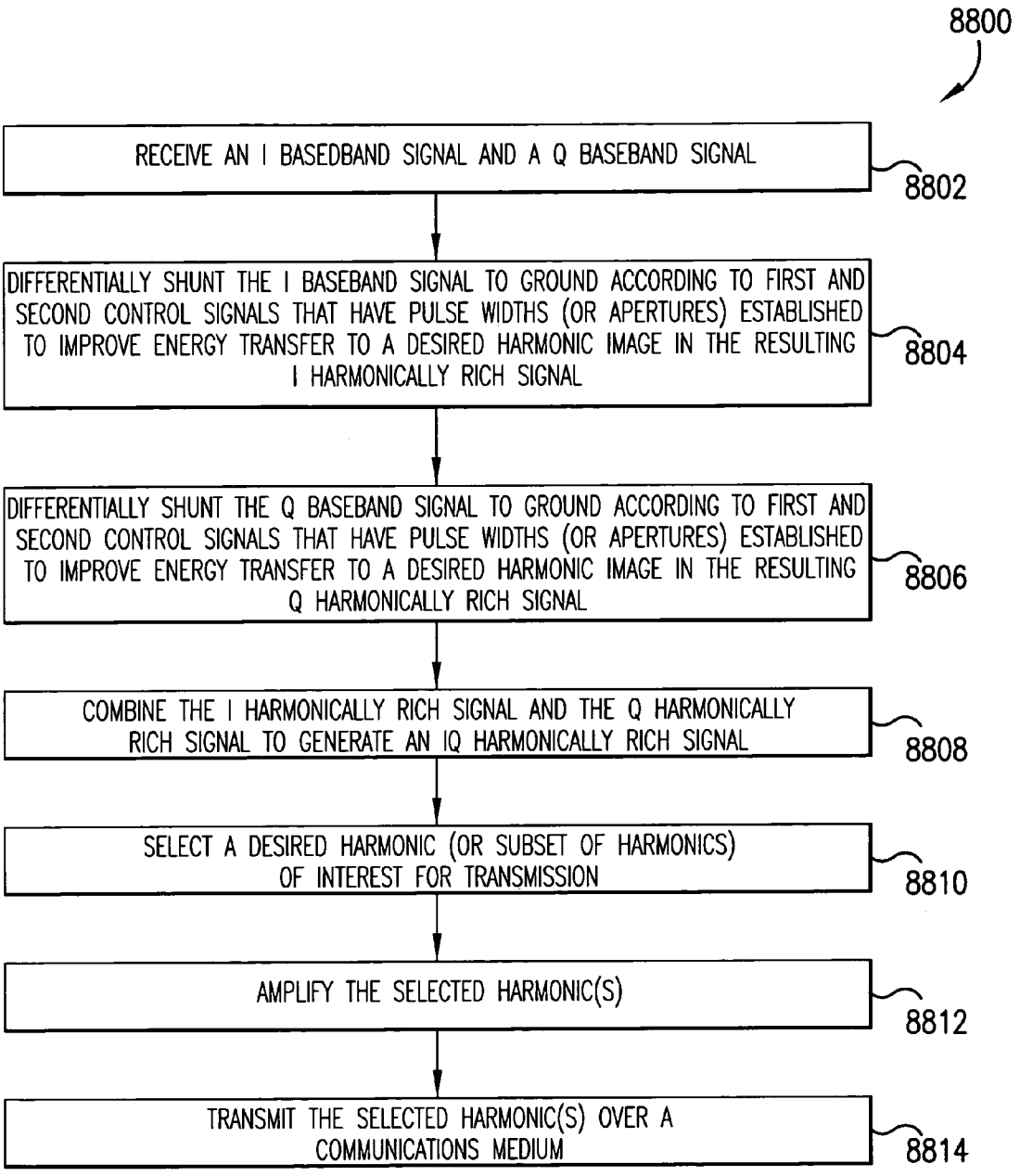

8800
RECEIVE AN I BASEDBAND SIGNAL AND A Q BASEBAND SIGNAL
8802
DIFFERENTIALLY SHUNT THE I BASEBAND SIGNAL TO GROUND ACCORDING TO FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING I HARMONICALLY RICH SIGNAL
8804
DIFFERENTIALLY SHUNT THE Q BASEBAND SIGNAL TO GROUND ACCORDING TO FIRST AND SECOND CONTROL SIGNALS THAT HAVE PULSE WIDTHS (OR APERTURES) ESTABLISHED TO IMPROVE ENERGY TRANSFER TO A DESIRED HARMONIC IMAGE IN THE RESULTING Q HARMONICALLY RICH SIGNAL
8806
COMBINE THE I HARMONICALLY RICH SIGNAL AND THE Q HARMONICALLY RICH SIGNAL TO GENERATE AN IQ HARMONICALLY RICH SIGNAL
8808
SELECT A DESIRED HARMONIC (OR SUBSET OF HARMONICS) OF INTEREST FOR TRANSMISSION
8810
AMPLIFY THE SELECTED HARMONIC(S)
8812
TRANSMIT THE SELECTED HARMONIC(S) OVER A COMMUNICATIONS MEDIUM
8814

FIG.88

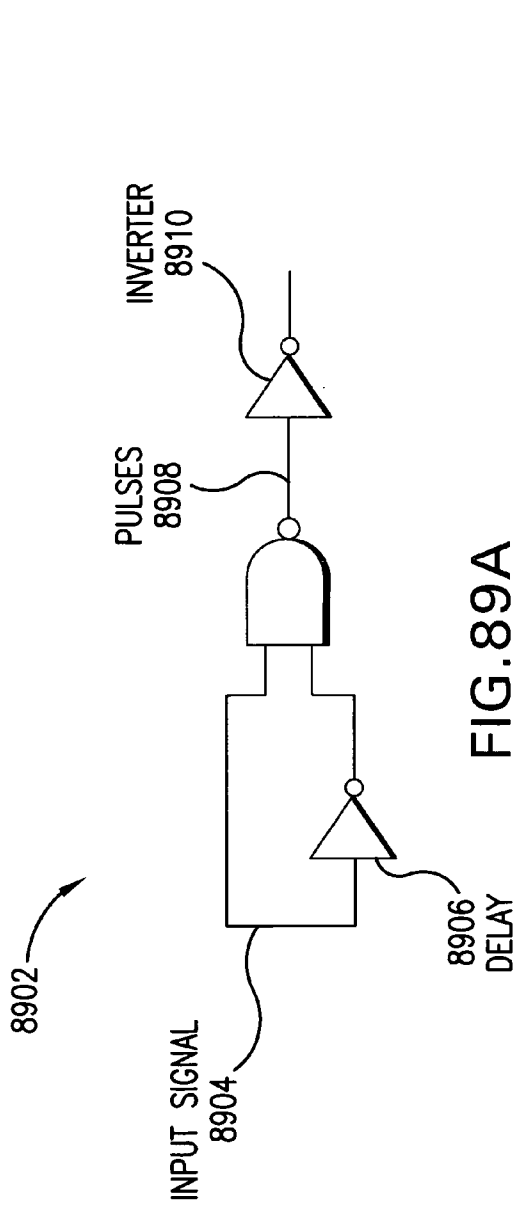


FIG.89A

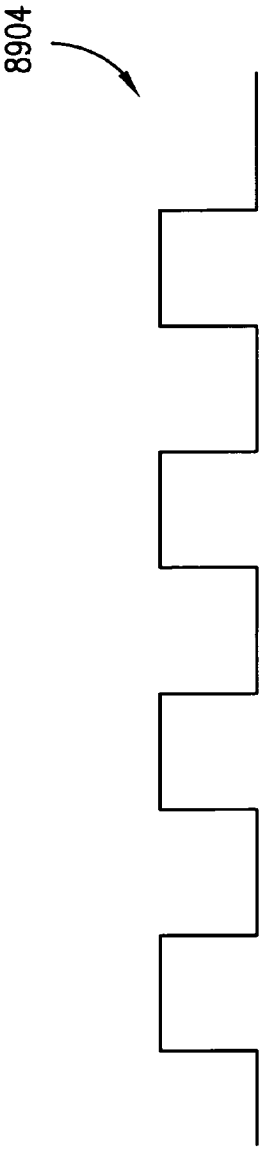


FIG.89B

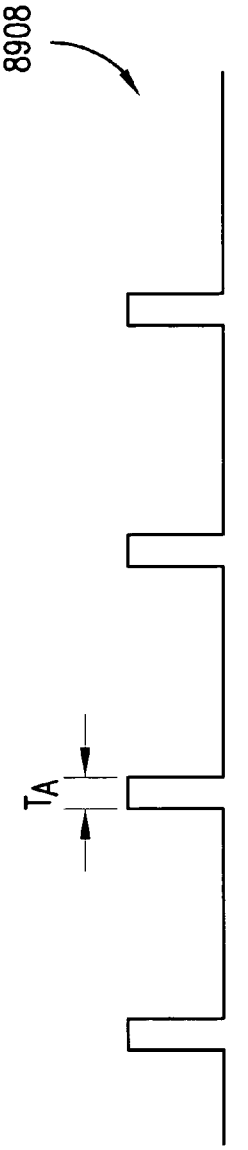


FIG.89C

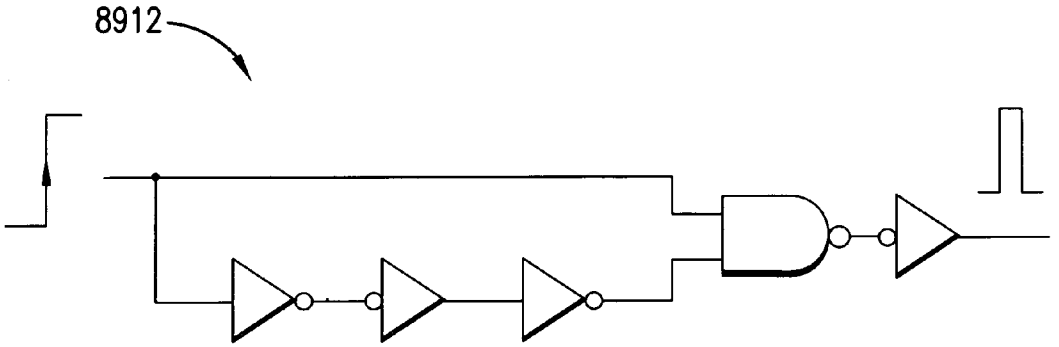


FIG.89D

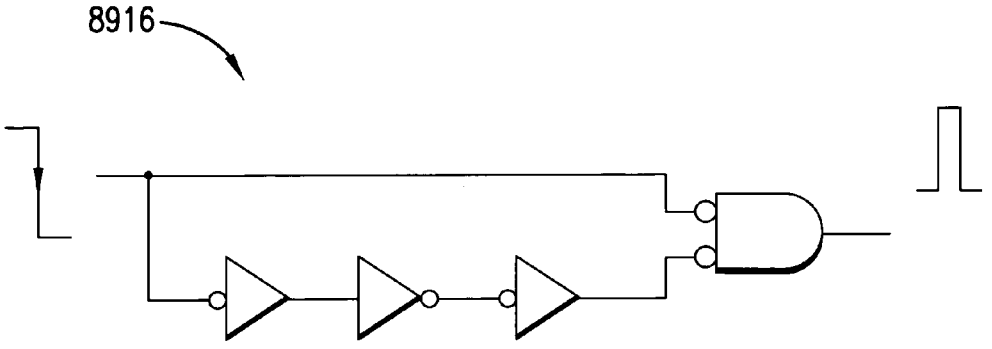


FIG.89E

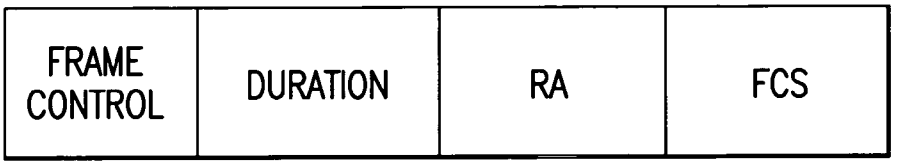

FRAME CONTROL
DURATION
RA
FCS
2
2
6
4

FIG.90

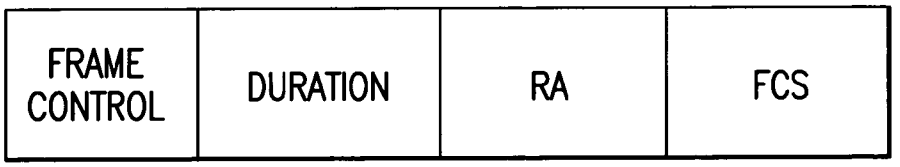

FRAME CONTROL
DURATION
RA
FCS
2
2
6
4

FIG.91

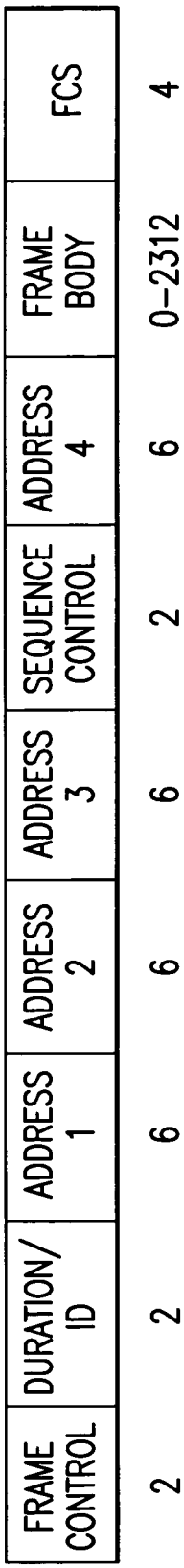

FRAME CONTROL
DURATION/ ID
ADDRESS 1
ADDRESS 2
ADDRESS 3
SEQUENCE CONTROL
ADDRESS 4
FRAME BODY
FCS
2
2
6
6
6
2
6
0-2312
4

FIG.92

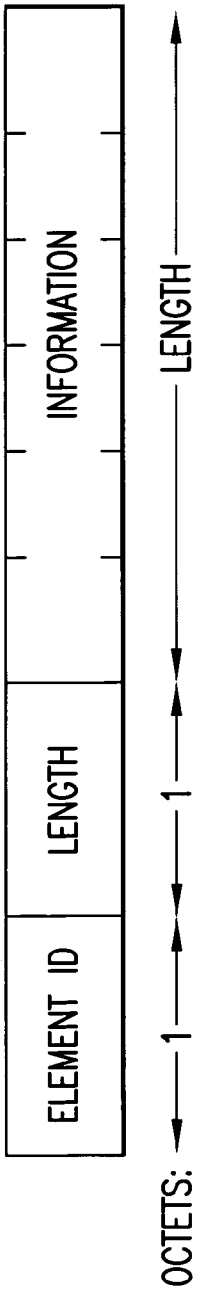

ELEMENT ID
LENGTH
INFORMATION
LENGTH
OCTETS:
1
1

FIG.93

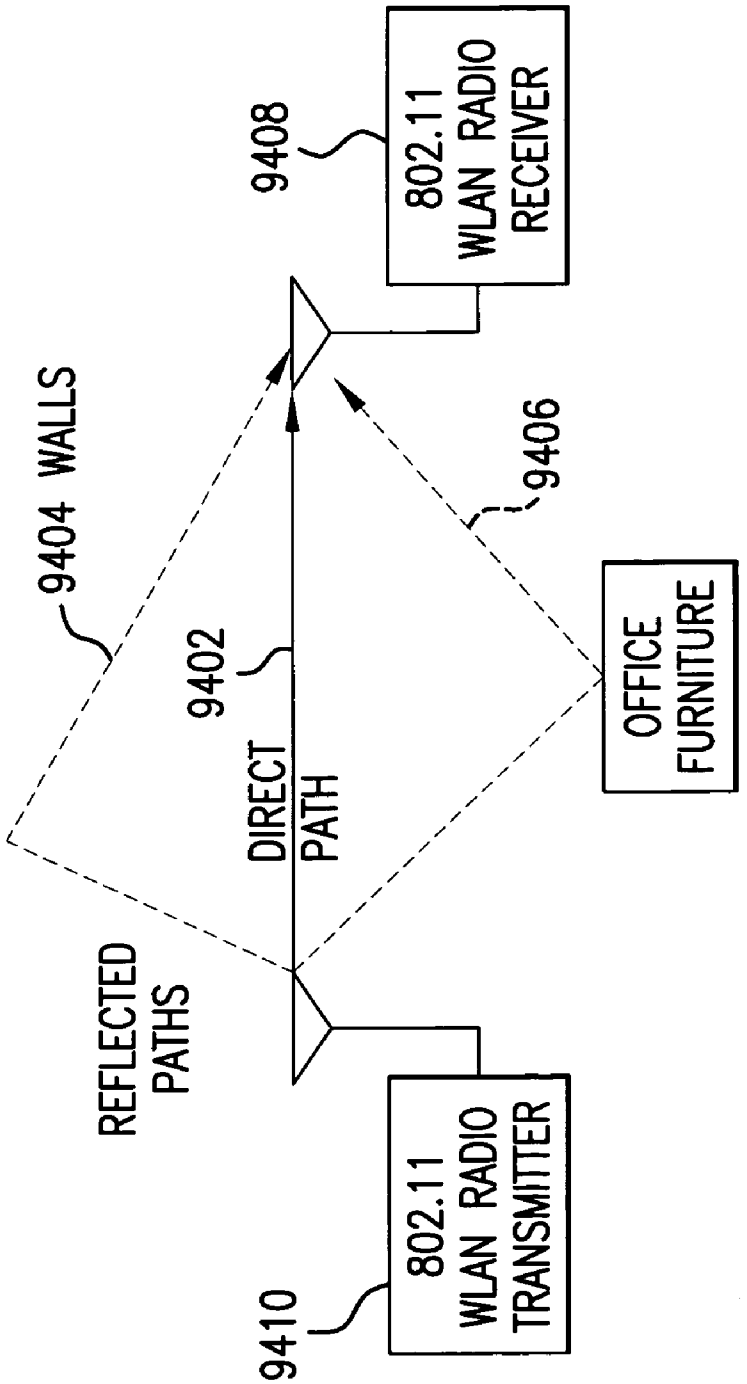

9408
802.11
WLAN RADIO
RECEIVER
9404 WALLS
9406
9402
DIRECT
PATH
OFFICE
FURNITURE
REFLECTED
PATHS
9410
802.11
WLAN RADIO
TRANSMITTER

FIG.94

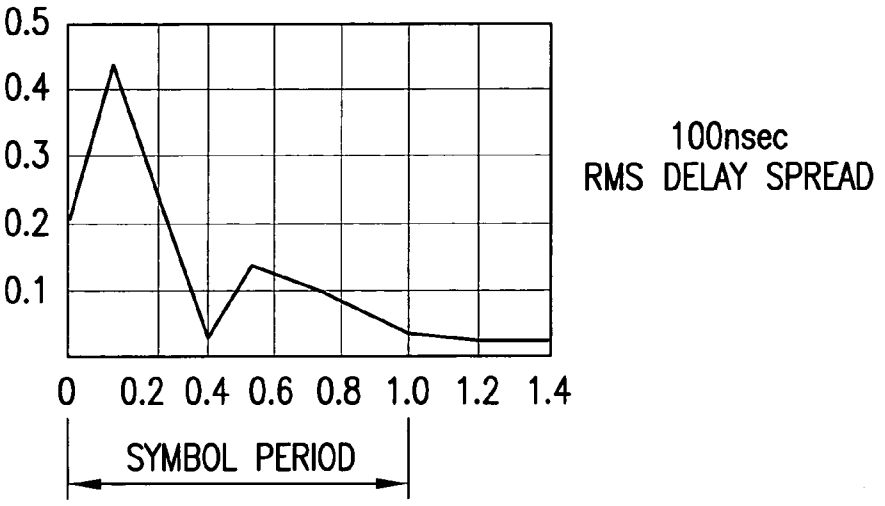

0.5
0.4
0.3
0.2
0.1
0 0.2 0.4 0.6 0.8 1.0 1.2 1.4
SYMBOL PERIOD
100nsec
RMS DELAY SPREAD

FIG.95

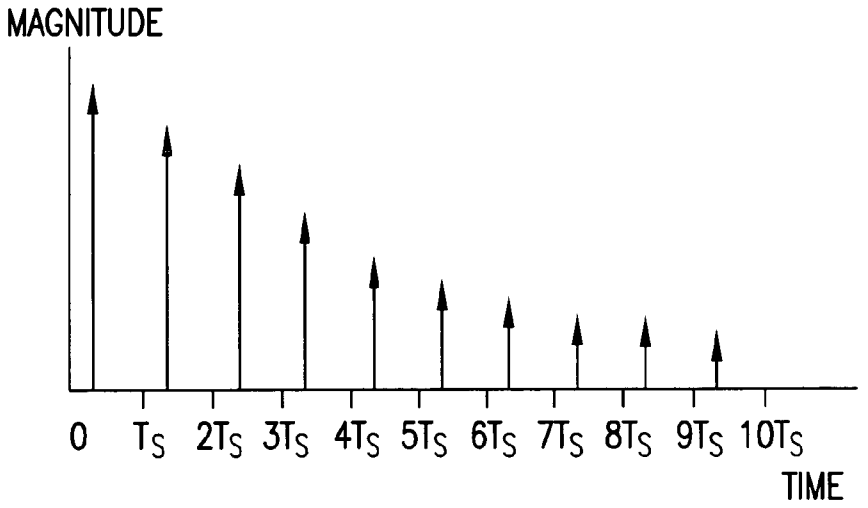

MAGNITUDE
0 TS 2TS 3TS 4TS 5TS 6TS 7TS 8TS 9TS 10TS
TIME

FIG.96

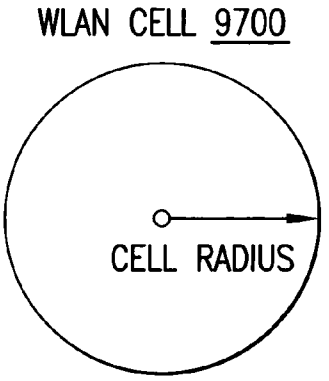
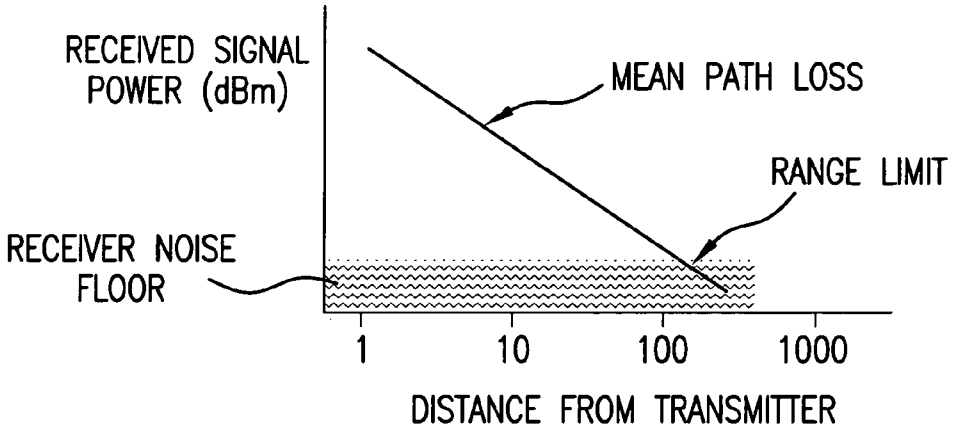


FIG.97



PATH LOSS (dB) = 20 LOG_{10} (4 x PI x D/LAMBDA)

WHERE:

r = D IS THE RADIUS OF THE WLAN CELL

LAMBDA = c/f WHERE: c = SPEED OF LIGHT (3 x $10^8 ms^{-1}$)

f = SIGNAL FREQUENCY IN Hz

FIG.98

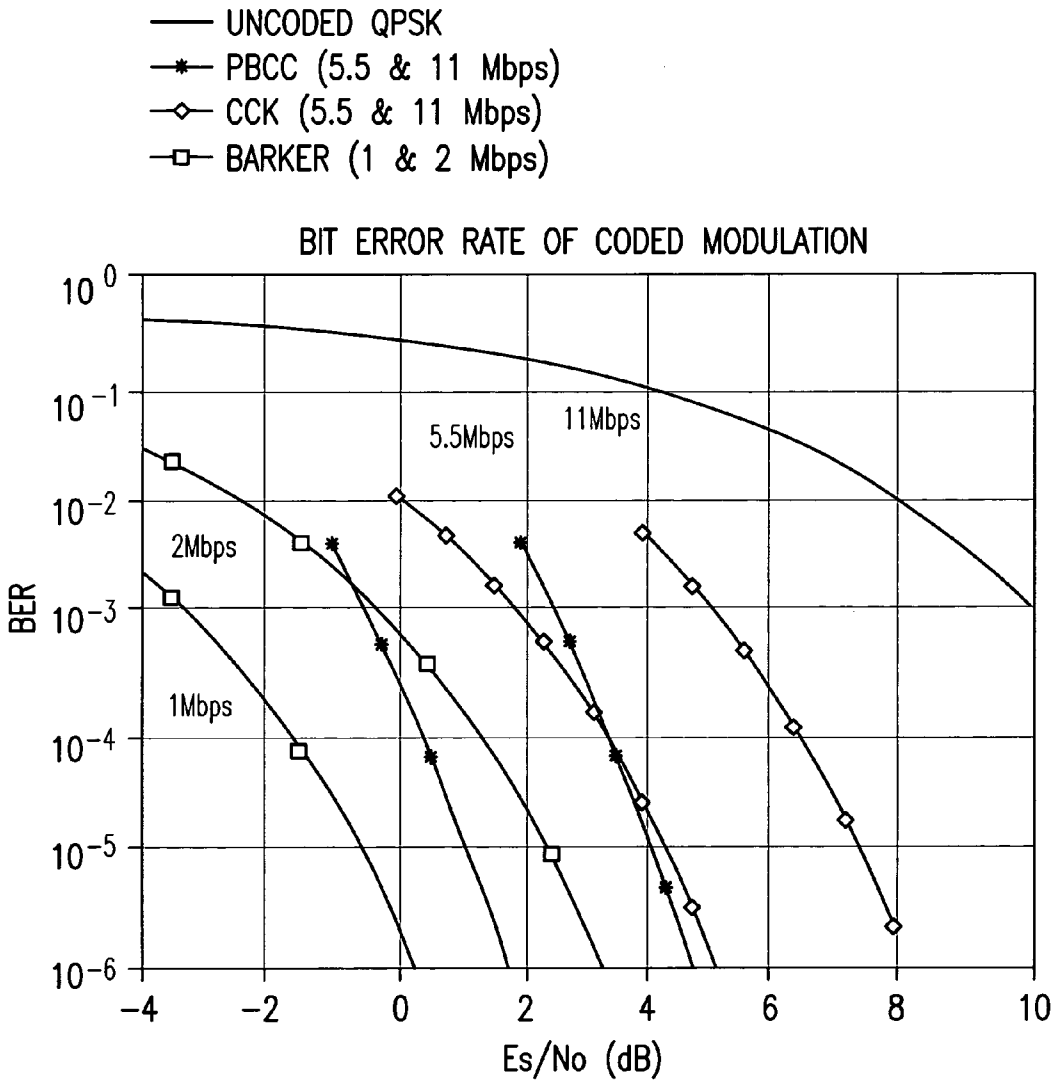

UNCODED QPSK
PBCC (5.5 & 11 Mbps)
CCK (5.5 & 11 Mbps)
BARKER (1 & 2 Mbps)
BIT ERROR RATE OF CODED MODULATION
BER
Es/No (dB)
5.5Mbps
11Mbps
2Mbps
1Mbps

FIG.99

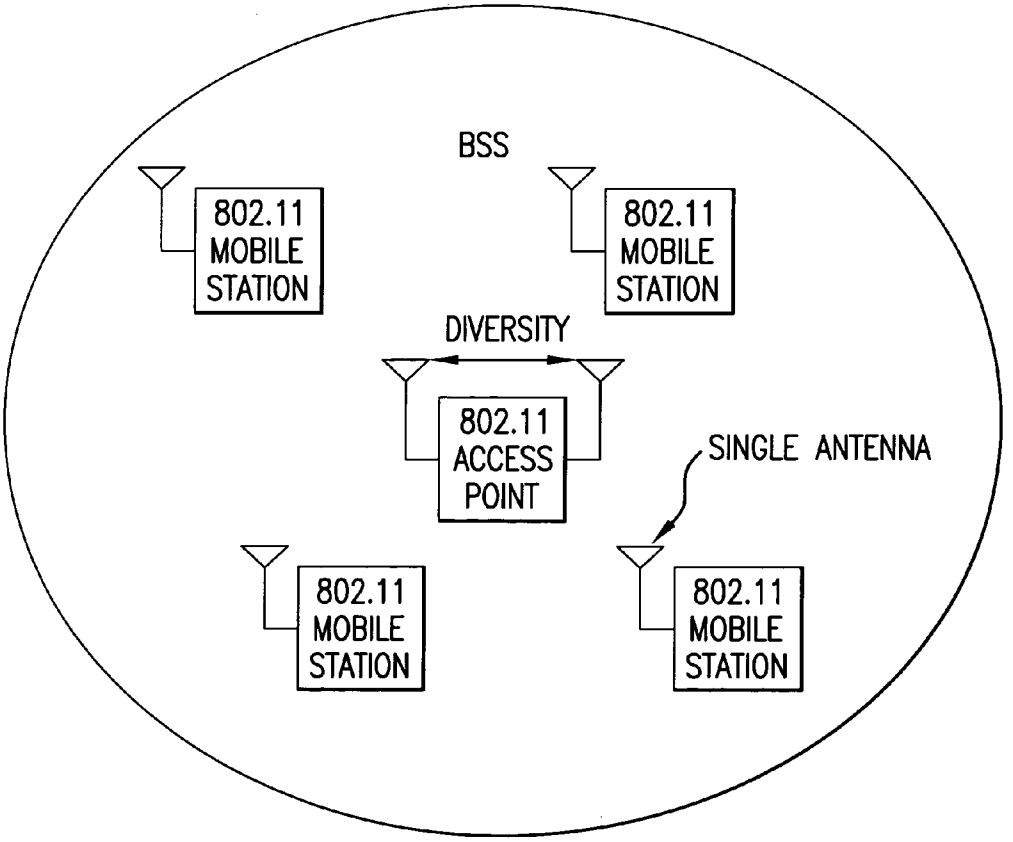

BSS
802.11
MOBILE
STATION
802.11
MOBILE
STATION
DIVERSITY
802.11
ACCESS
POINT
SINGLE ANTENNA
802.11
MOBILE
STATION
802.11
MOBILE
STATION

FIG.100

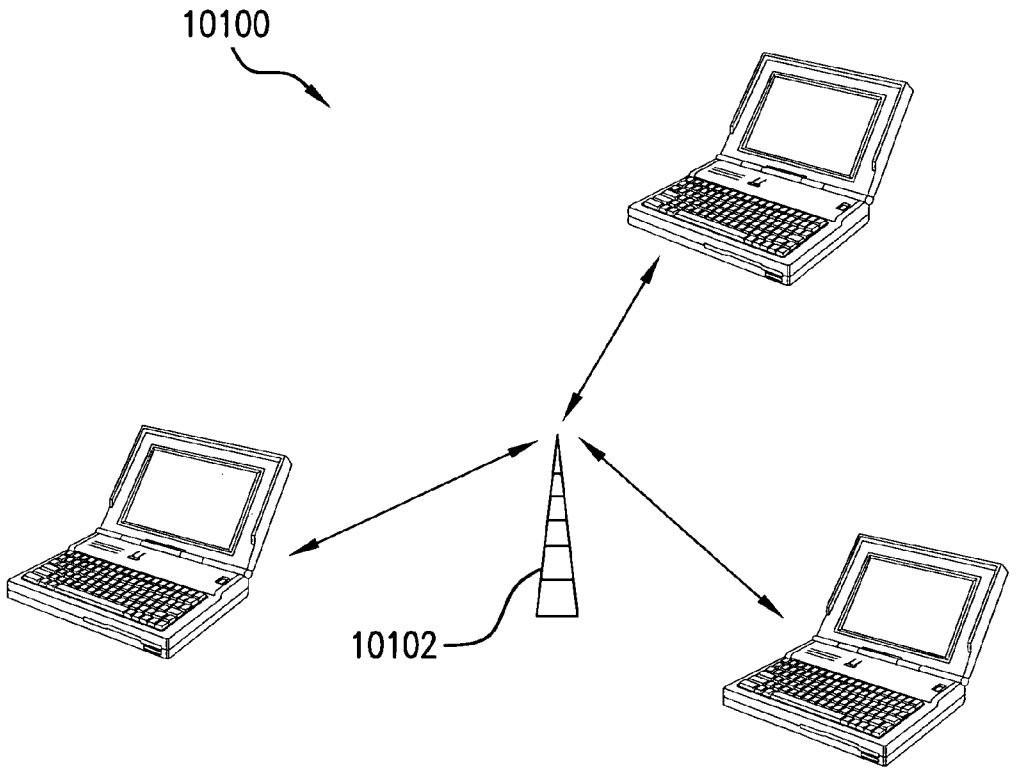


FIG.101A

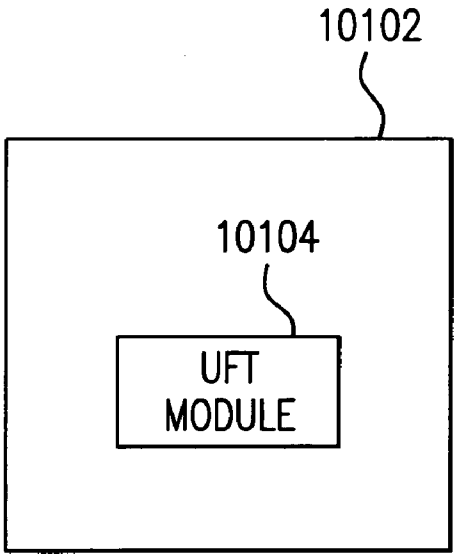


FIG.101B

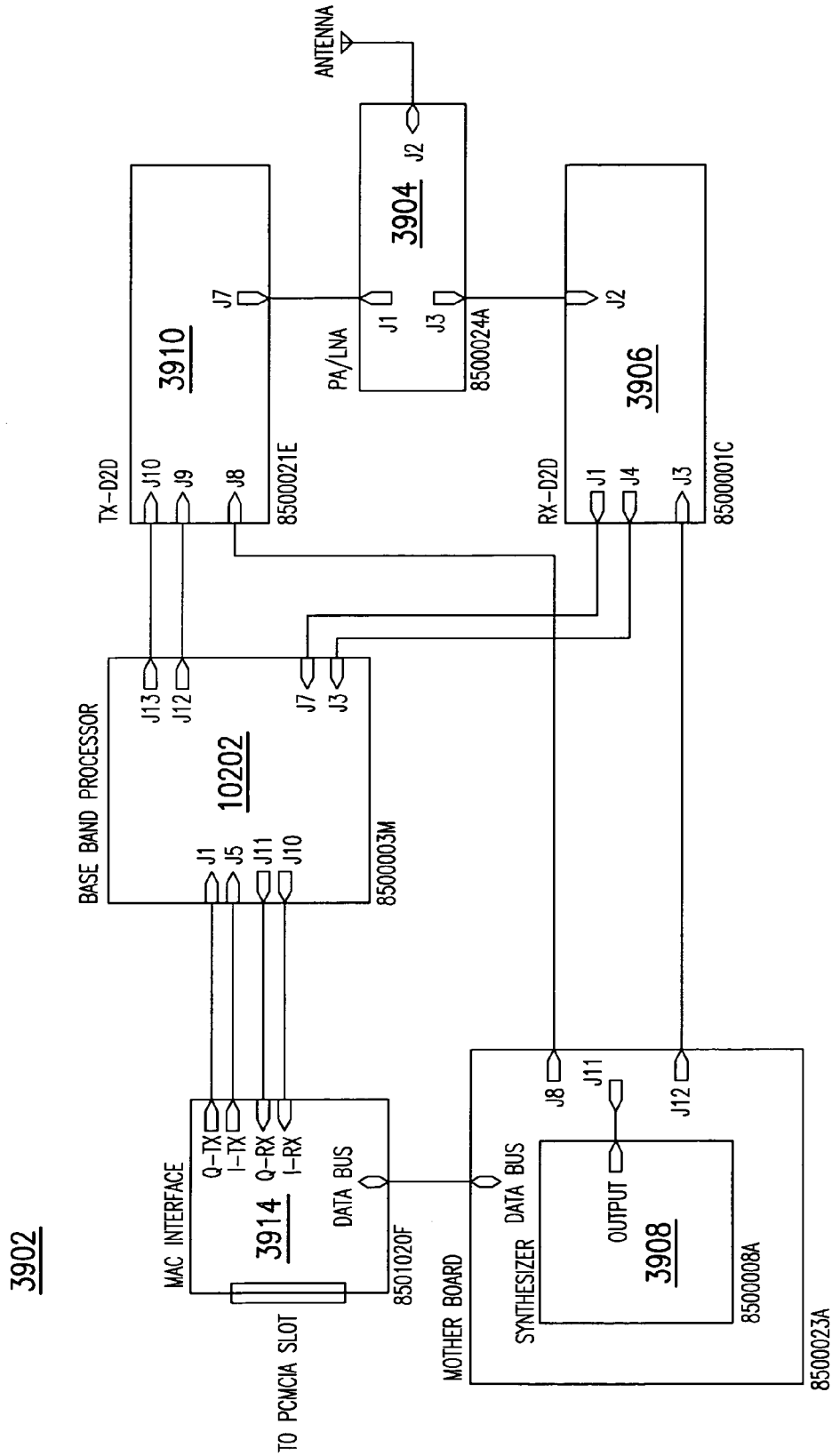

3902
ANTENNA
J2
3904
PA/LNA
J1
J3
8500024A
J7
3910
TX-D2D
J10
J9
J8
8500021E
J2
3906
RX-D2D
J1
J4
J3
8500001C
J13
J12
J7
J3
BASE BAND PROCESSOR
10202
J1
J5
J11
J10
8500003M
MAC INTERFACE
Q-TX
I-TX
Q-RX
I-RX
3914
DATA BUS
8501020F
TO PCMCIA SLOT
J8
J11
J12
MOTHER BOARD
SYNTHESIZER DATA BUS
OUTPUT
3908
8500008A
8500023A

FIG. 102

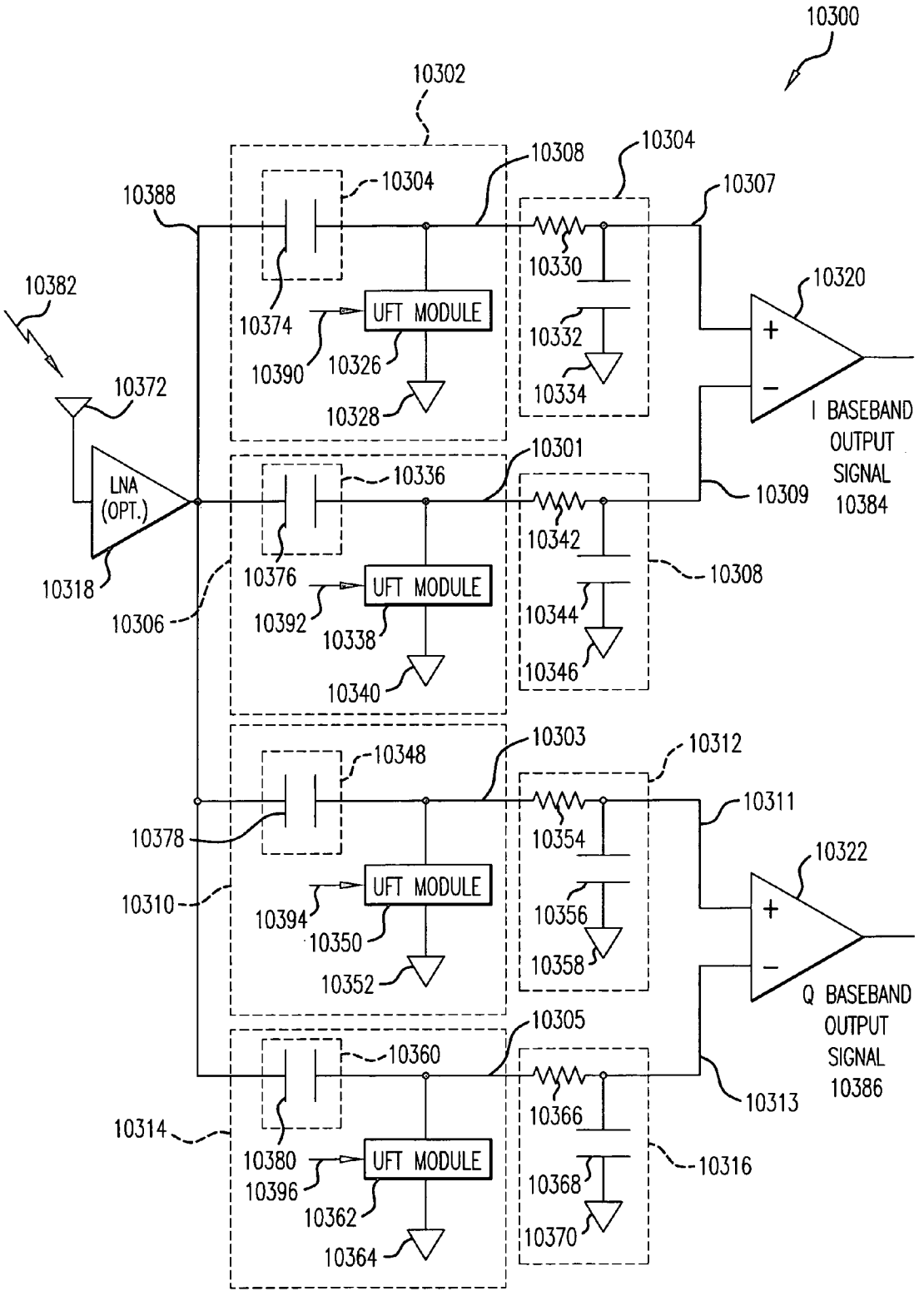

10300
10302
10304
10308
10304
10307
10388
10330
10320
10382
10374
UFT MODULE
10332
10390
10326
10372
10334
10328
I BASEBAND OUTPUT SIGNAL 10384
10301
10336
LNA (OPT.)
10309
10342
10376
10308
10318
UFT MODULE
10344
10392
10338
10306
10346
10340
10303
10312
10348
10311
10378
10354
10322
10310
UFT MODULE
10356
10394
10350
10358
10352
Q BASEBAND OUTPUT SIGNAL 10386
10305
10360
10313
10366
10314
10380
UFT MODULE
10316
10368
10396
10362
10370
10364

FIG.103

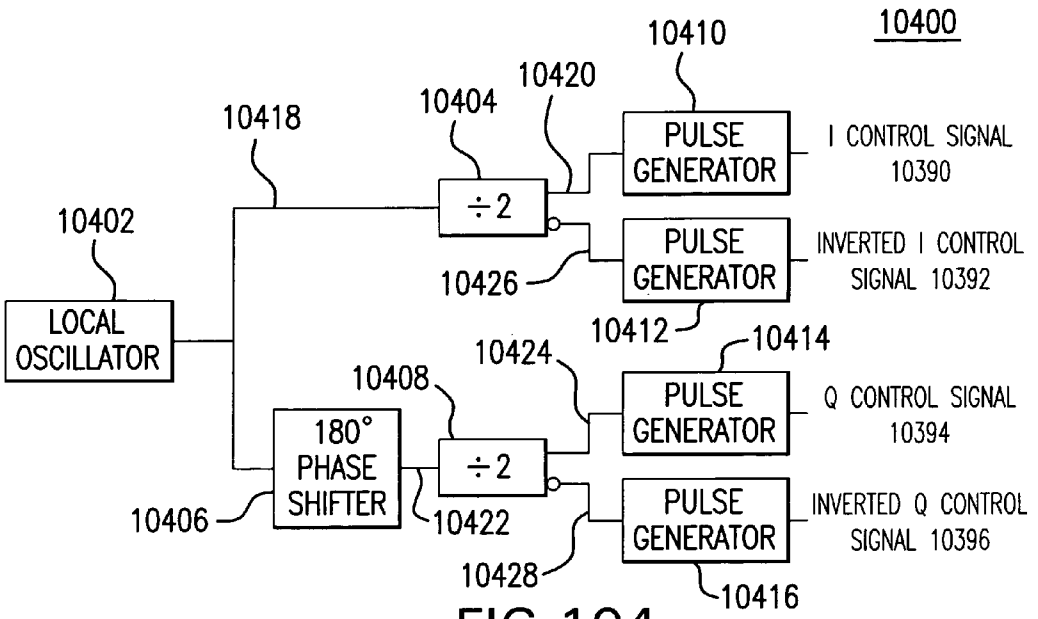


FIG.104

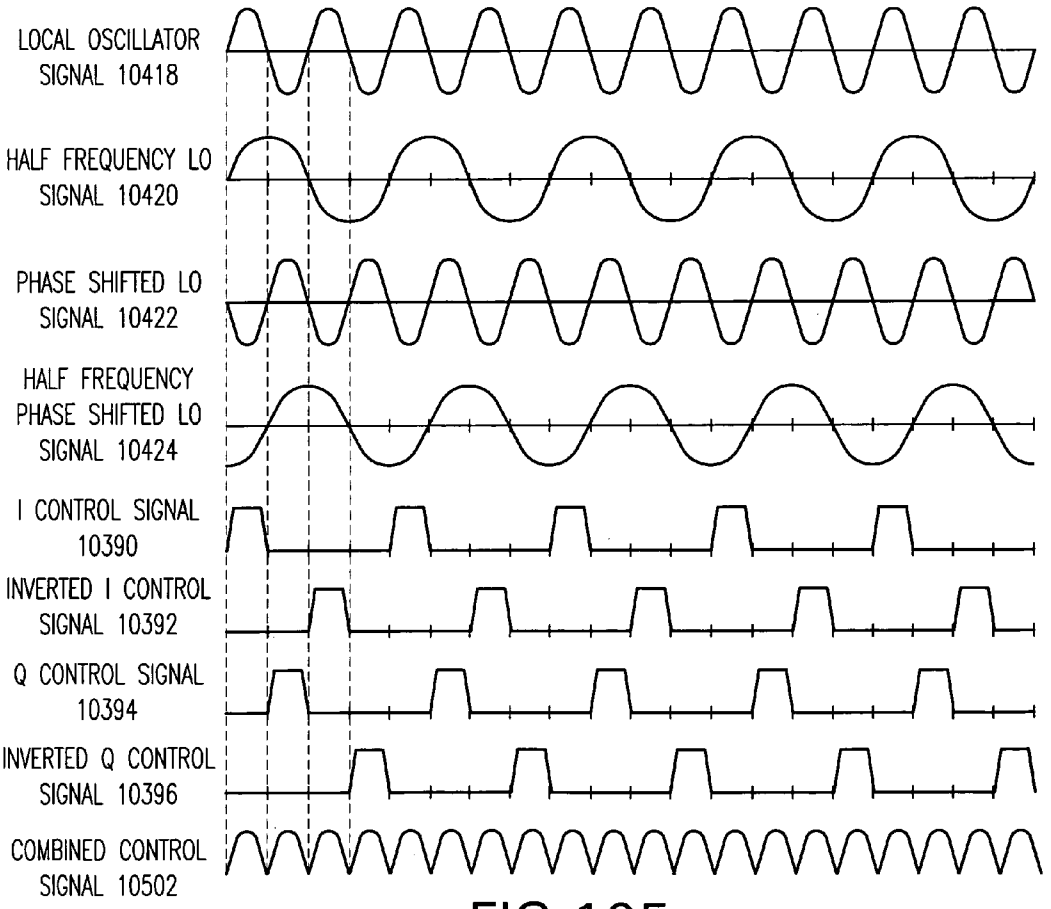


FIG.105

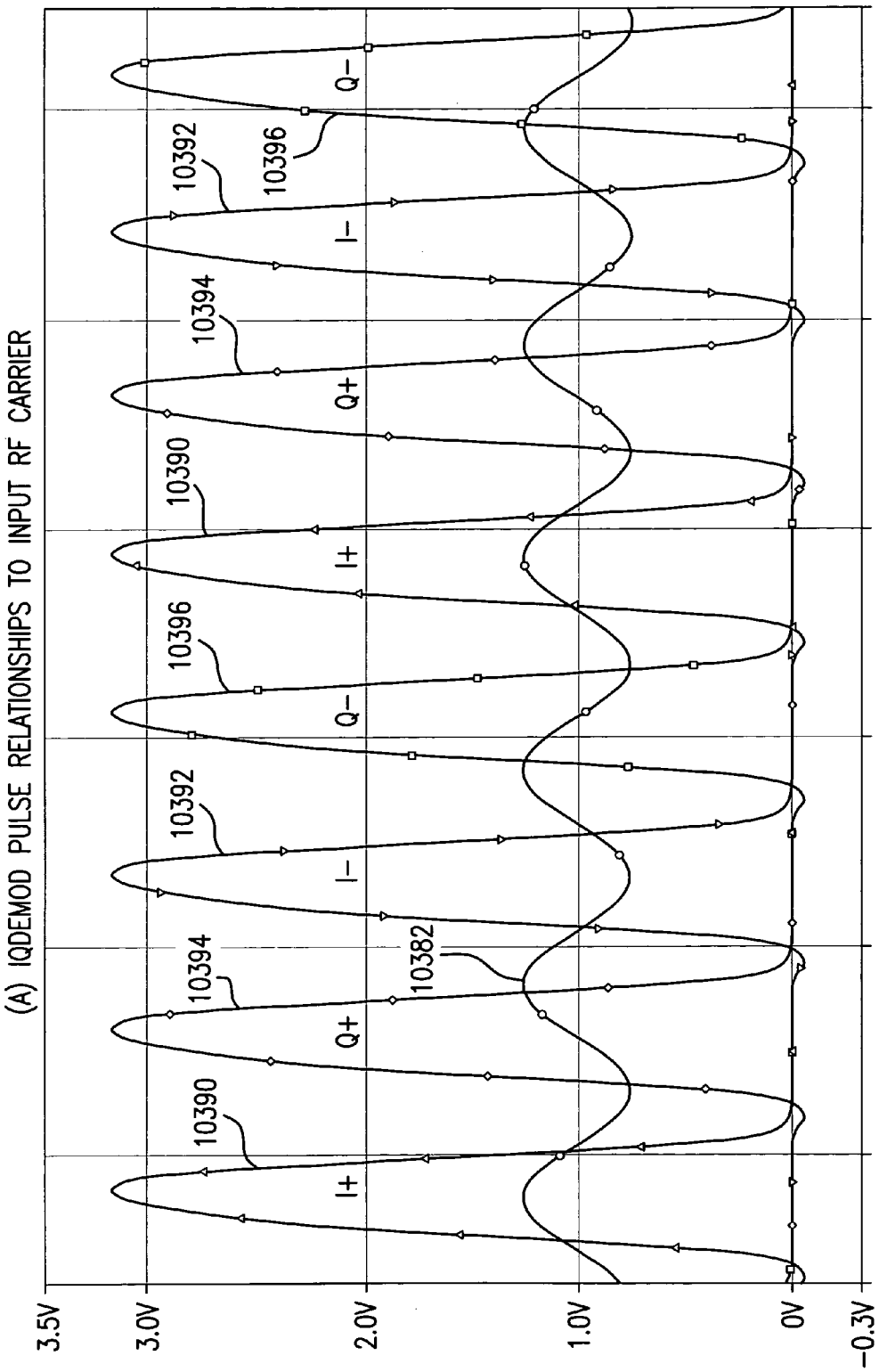

(A) IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER
3.5V
3.0V
2.0V
1.0V
0V
−0.3V
9.0ns
9.2ns
9.6ns
10.0ns
10.4ns
10.8ns
11.2ns
10390
10394
10392
10396
10382
I+
Q+
I−
Q−

FIG.106

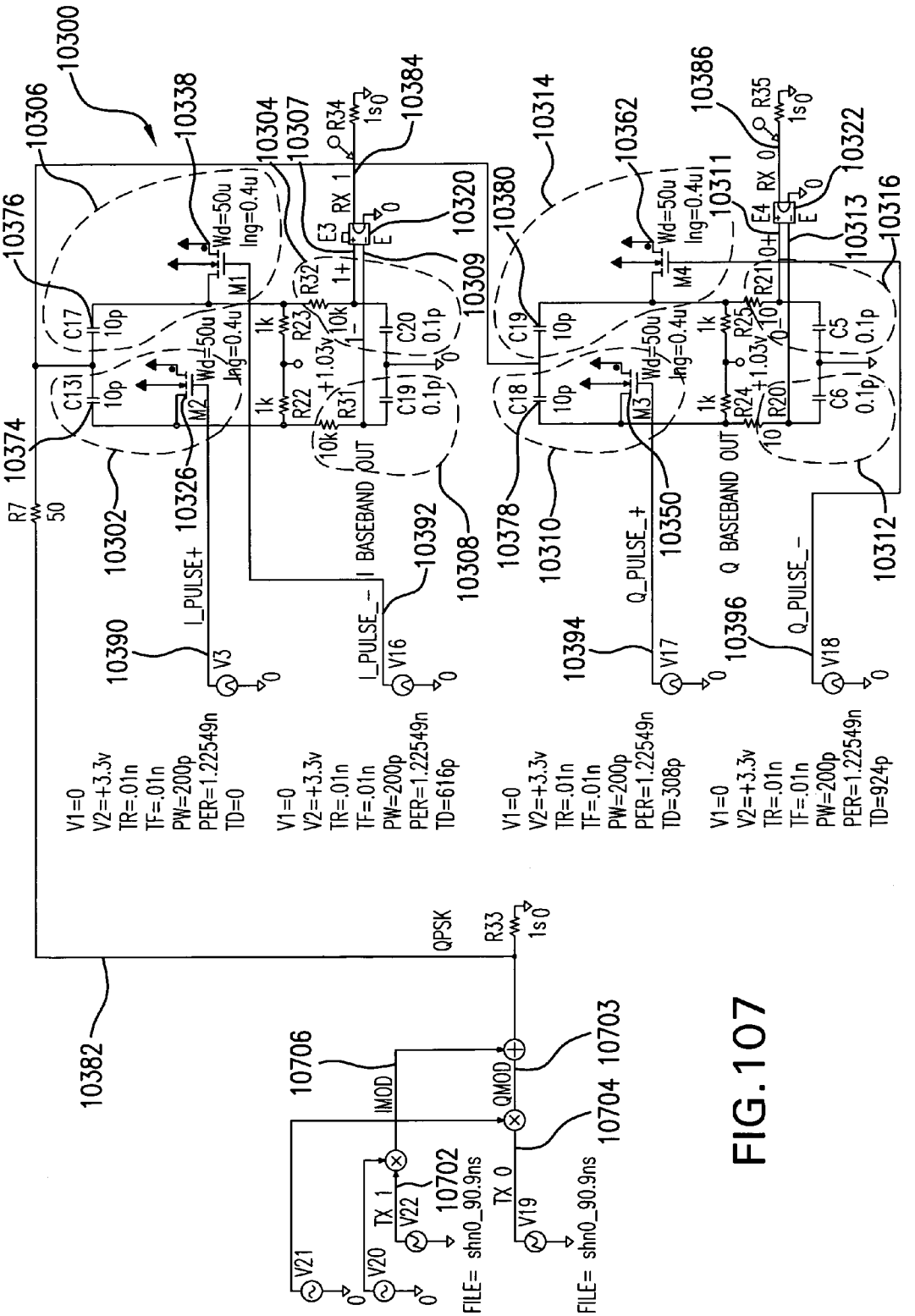

10300
10302
10304
10306
10307
10308
10309
10310
10311
10312
10313
10314
10316
10320
10322
10326
10338
10350
10362
10374
10376
10378
10380
10382
10384
10386
10390
10392
10394
10396
10703
10704
10706
10702
R7
50
C131
10p
C17
10p
C18
10p
C19
10p
M1
M2
M3
M4
Wd=50u
lng=0.4u
1k
R22
R23
R31
R32
10k
+1.03v
R34
R35
R24
R25
R20
R21
10
C19
0.1p
C20
0.1p
C5
0.1p
C6
0.1p
E3
E4
RX 1
RX 0
1+
1-
0+
0-
I BASEBAND OUT
Q BASEBAND OUT
I_PULSE+
I_PULSE_-
Q_PULSE_+
Q_PULSE_-
V3
V16
V17
V18
V1=0
V2=+3.3v
TR=.01n
TF=.01n
PW=200p
PER=1.22549n
TD=0
TD=616p
TD=308p
TD=924p
QPSK
R33
1s0
IMOD
QMOD
TX 1
TX 0
V22
V19
V21
V20
FILE= shn0_90.9ns

FIG. 107

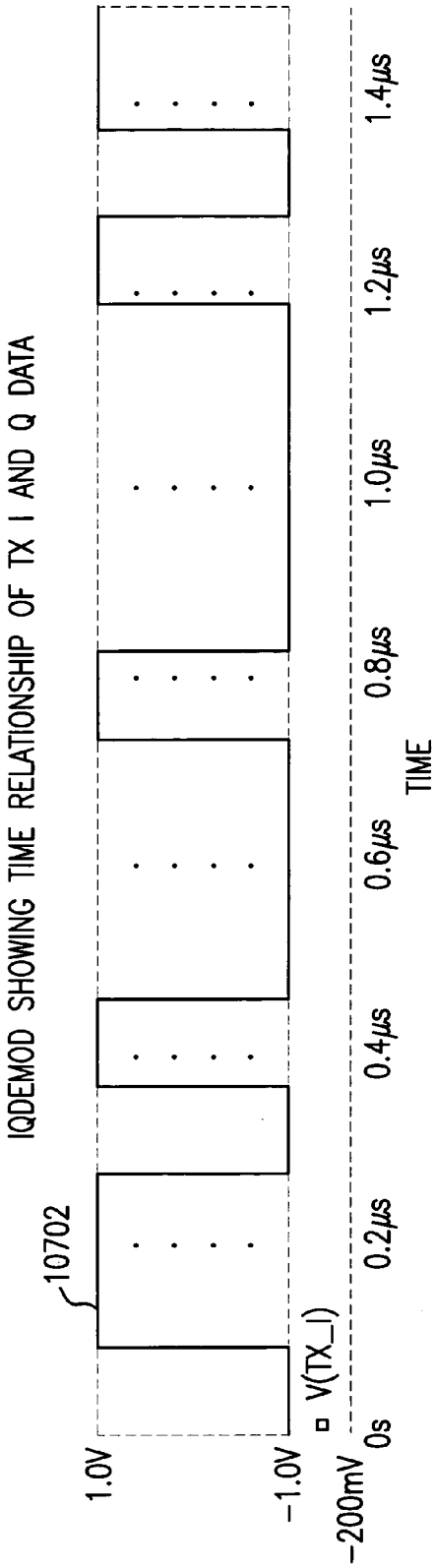


FIG.108

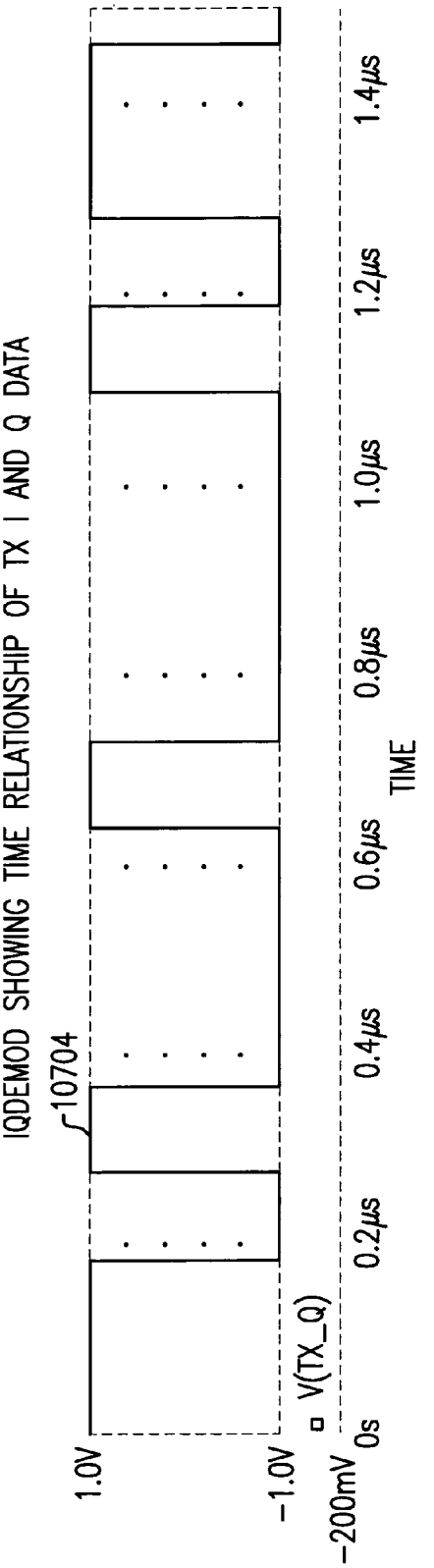


FIG.109

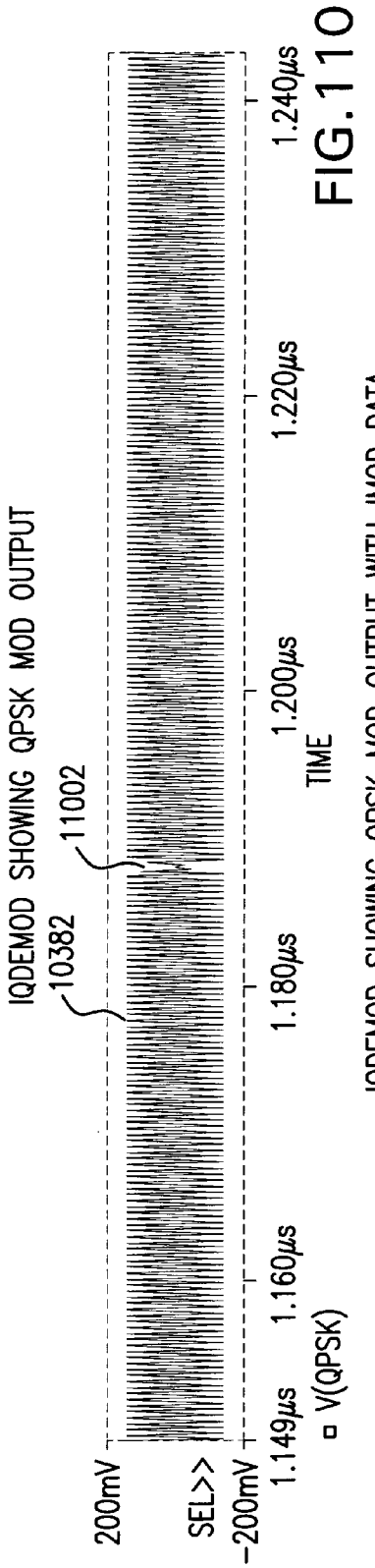


FIG.110

FIG.111

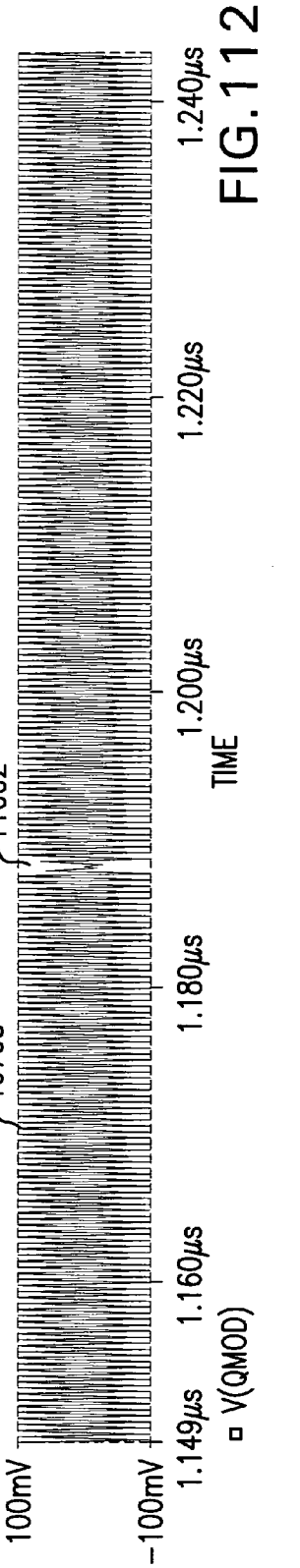


FIG.112

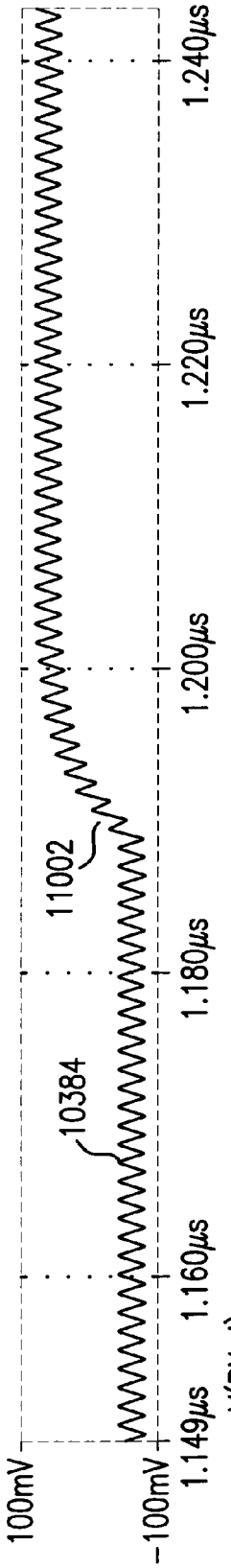


FIG.113

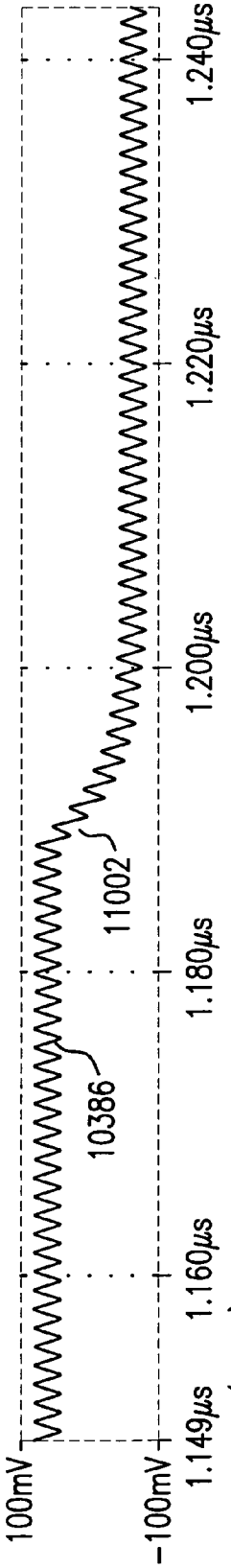


FIG.114

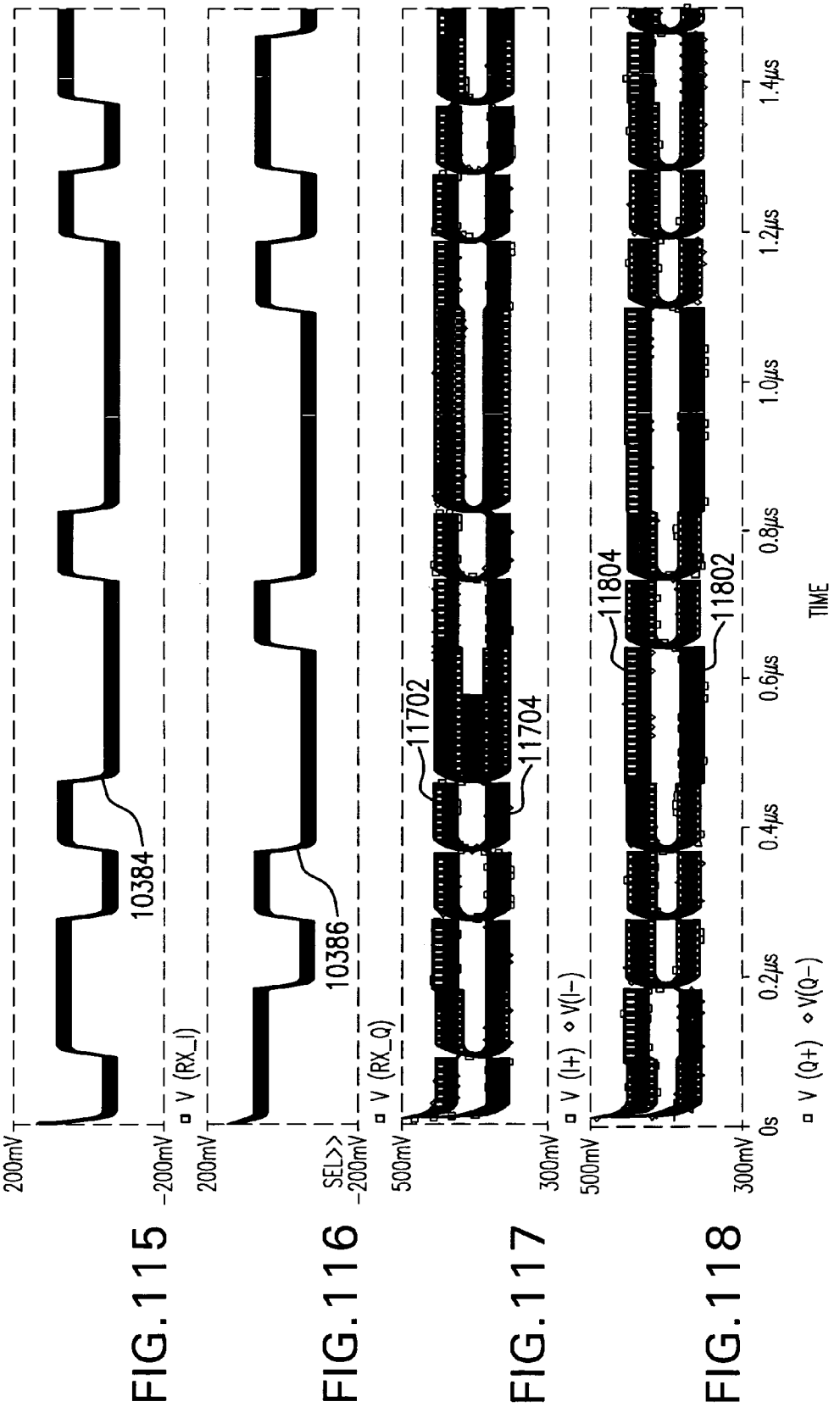


FIG. 115

FIG. 116

FIG. 117

FIG. 118

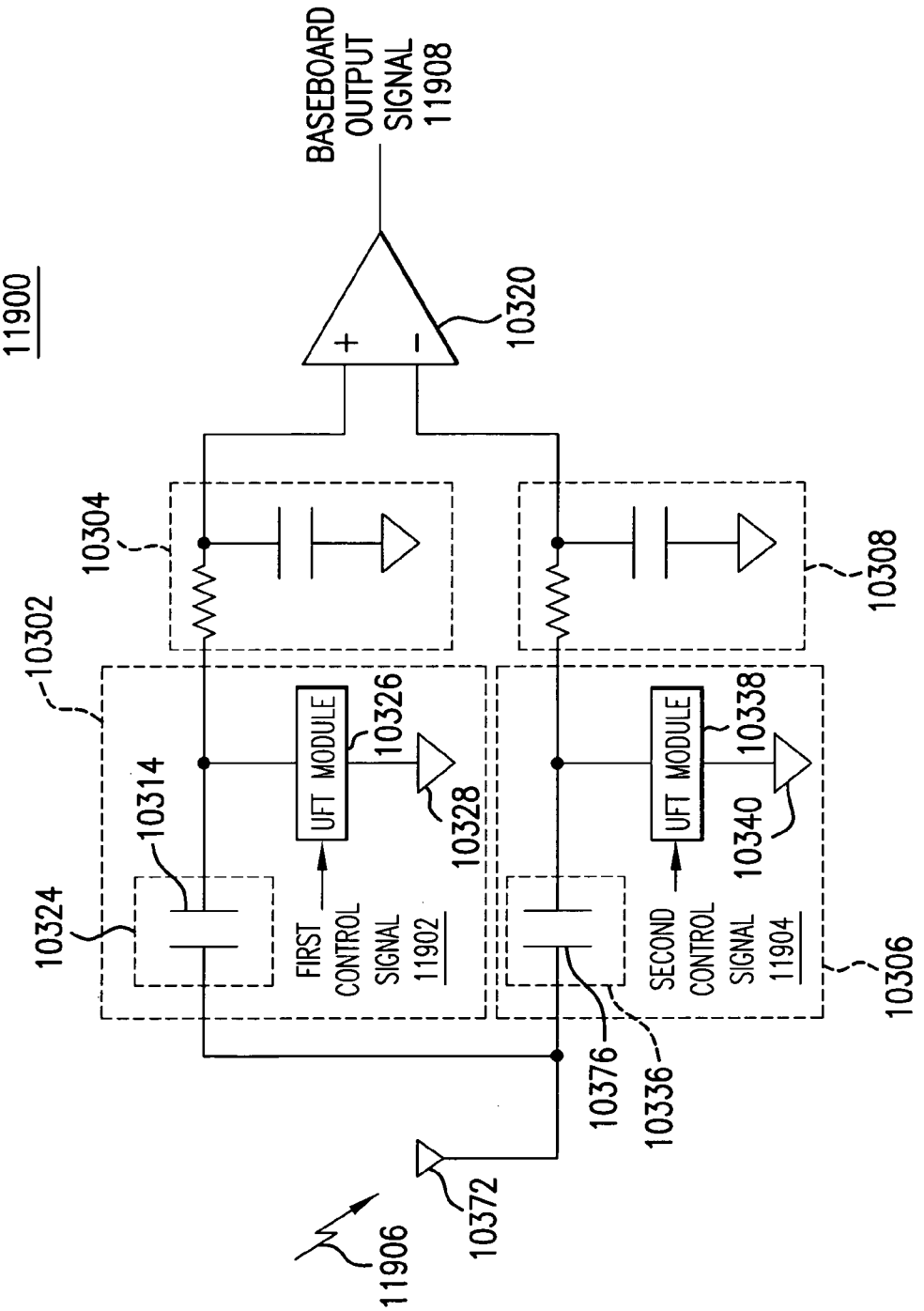

11900
BASEBOARD OUTPUT SIGNAL 11908
10320
10304
10308
10302
10326
UFT MODULE
10338
UFT MODULE
10314
10328
10340
10324
FIRST CONTROL SIGNAL 11902
SECOND CONTROL SIGNAL 11904
10306
10376
10336
10372
11906

FIG. 119

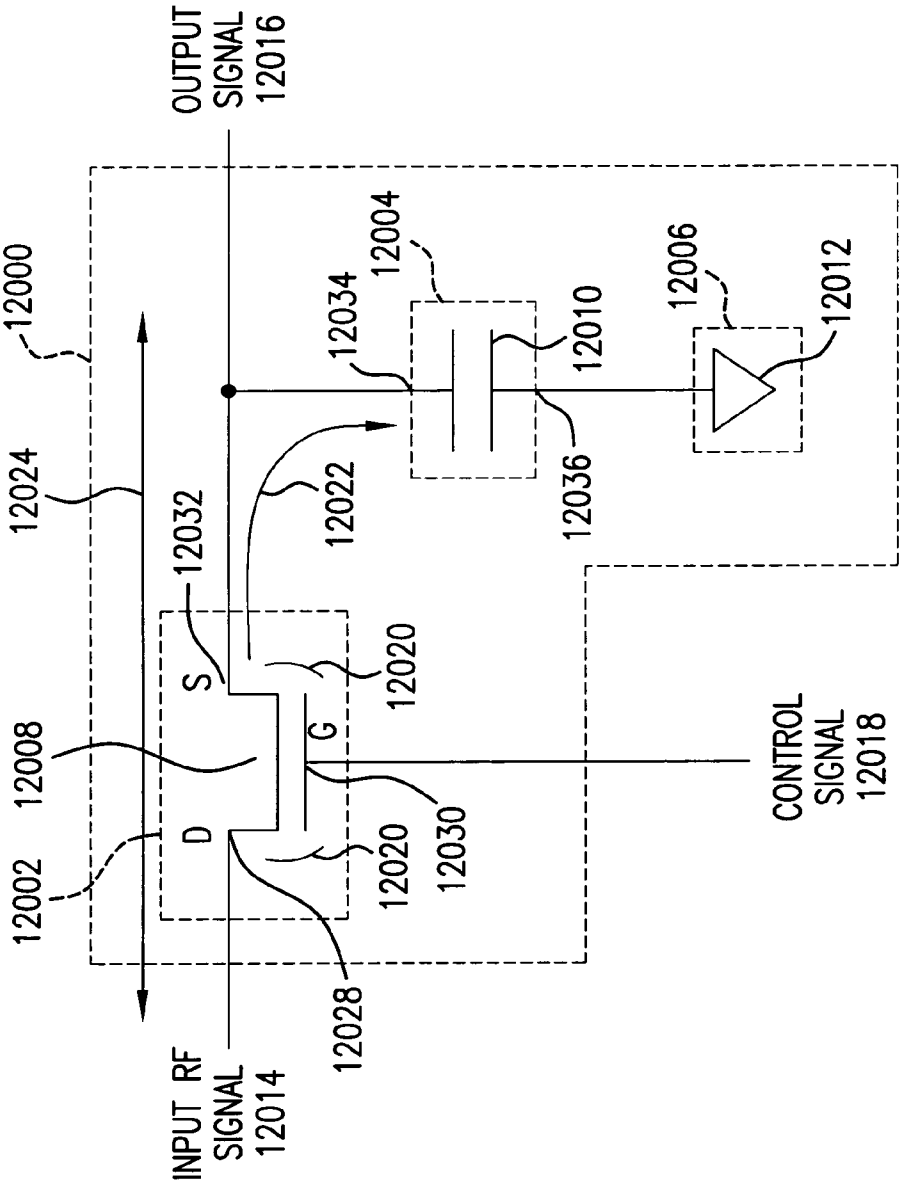

OUTPUT SIGNAL 12016
12000
12004
12034
12010
12006
12012
12024
12022
12036
12032
S
12020
12008
G
CONTROL SIGNAL 12018
12002
D
12020
12030
12028
INPUT RF SIGNAL 12014

FIG. 120

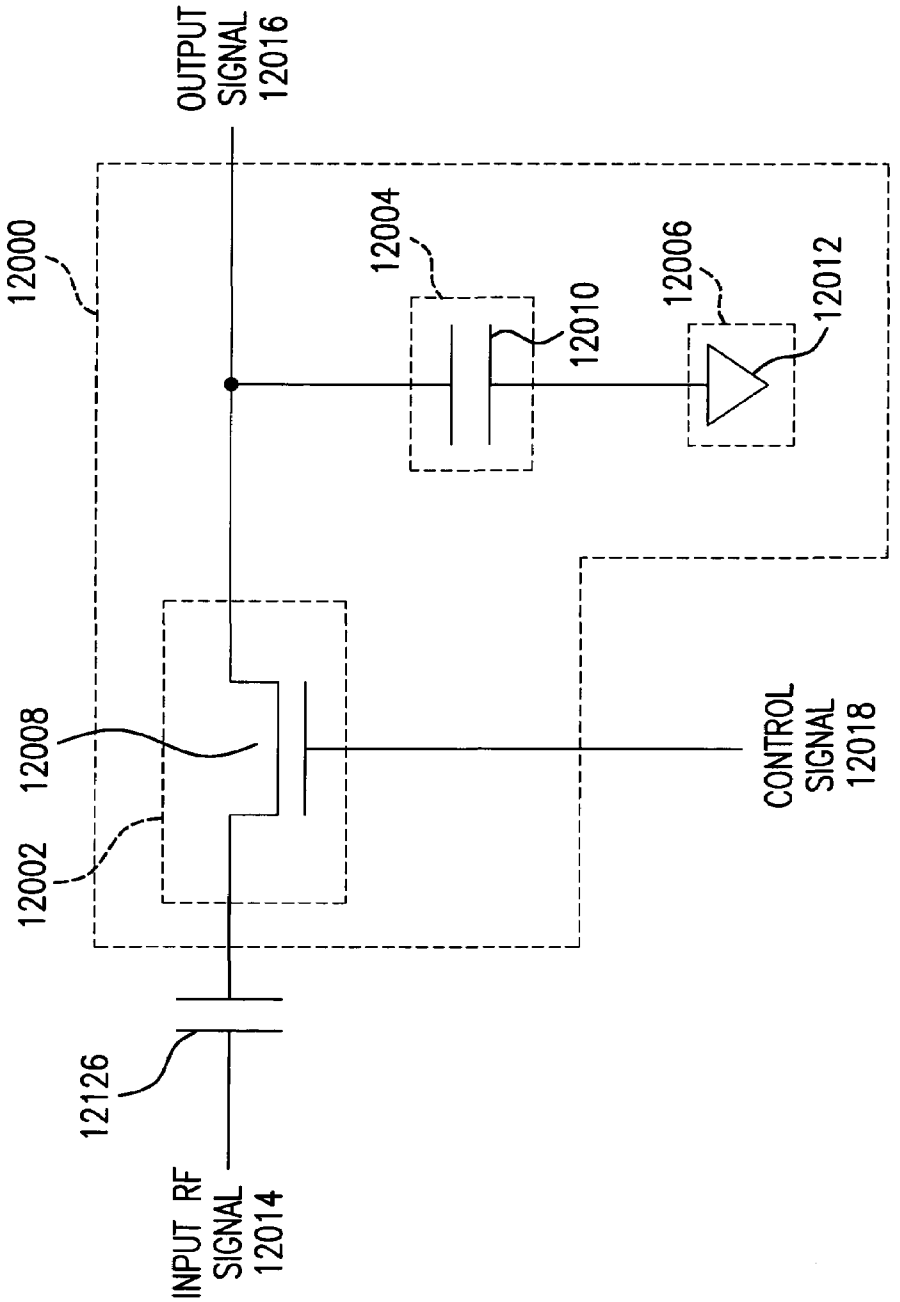

OUTPUT SIGNAL 12016
12000
12004
12010
12006
12012
12008
12002
CONTROL SIGNAL 12018
12126
INPUT RF SIGNAL 12014

FIG. 121

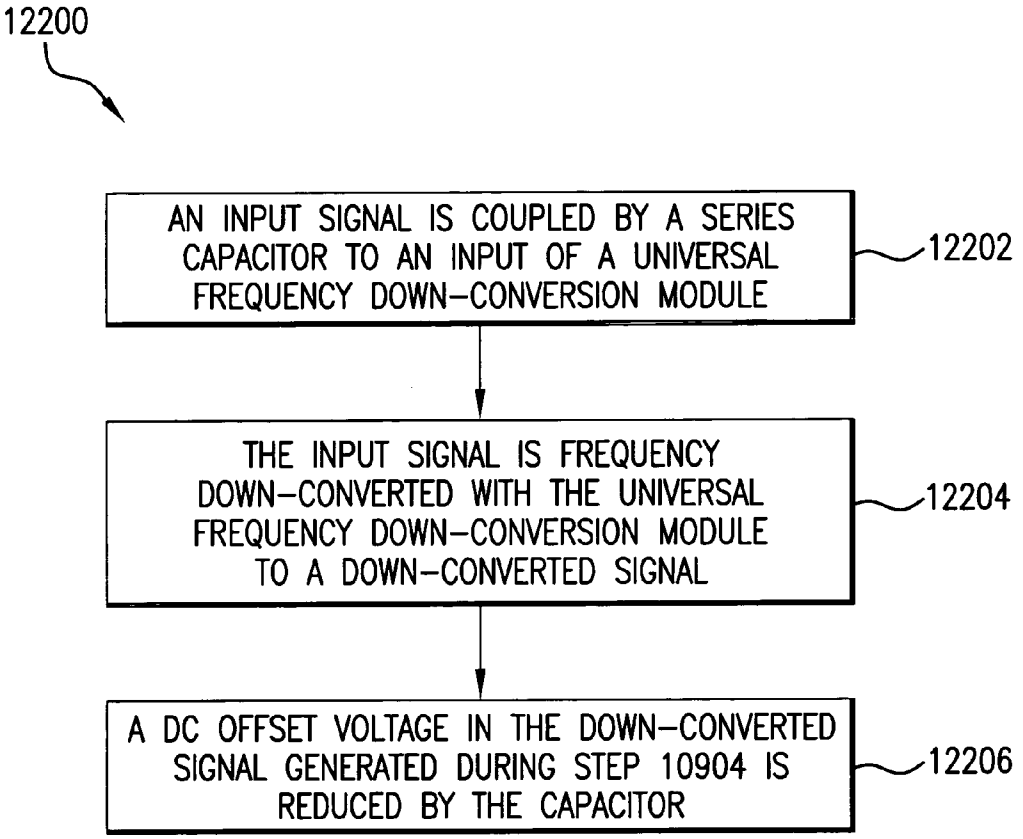

12200
AN INPUT SIGNAL IS COUPLED BY A SERIES CAPACITOR TO AN INPUT OF A UNIVERSAL FREQUENCY DOWN-CONVERSION MODULE
12202
THE INPUT SIGNAL IS FREQUENCY DOWN-CONVERTED WITH THE UNIVERSAL FREQUENCY DOWN-CONVERSION MODULE TO A DOWN-CONVERTED SIGNAL
12204
A DC OFFSET VOLTAGE IN THE DOWN-CONVERTED SIGNAL GENERATED DURING STEP 10904 IS REDUCED BY THE CAPACITOR
12206

FIG.122

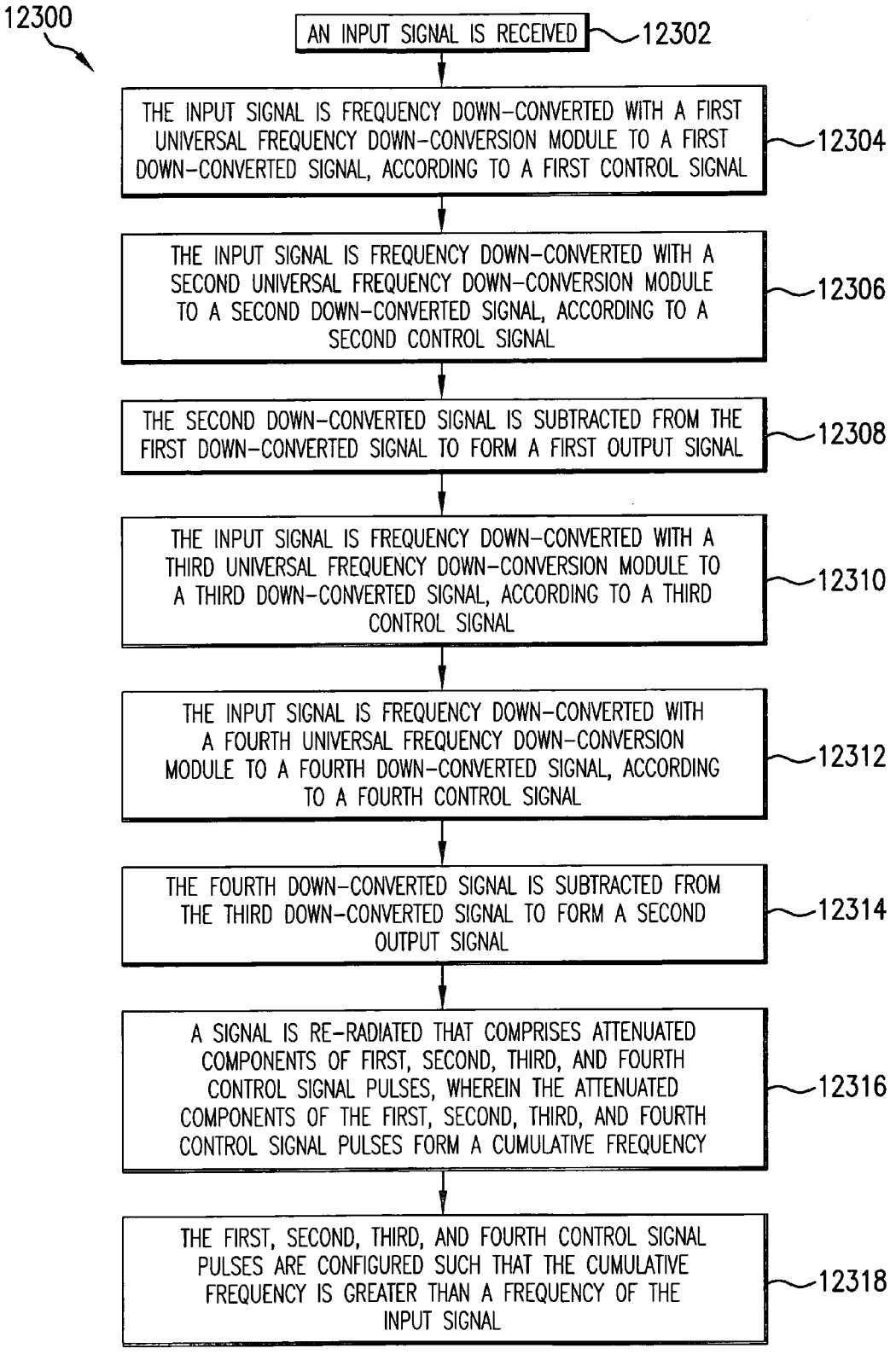

12300
AN INPUT SIGNAL IS RECEIVED
12302
THE INPUT SIGNAL IS FREQUENCY DOWN-CONVERTED WITH A FIRST UNIVERSAL FREQUENCY DOWN-CONVERSION MODULE TO A FIRST DOWN-CONVERTED SIGNAL, ACCORDING TO A FIRST CONTROL SIGNAL
12304
THE INPUT SIGNAL IS FREQUENCY DOWN-CONVERTED WITH A SECOND UNIVERSAL FREQUENCY DOWN-CONVERSION MODULE TO A SECOND DOWN-CONVERTED SIGNAL, ACCORDING TO A SECOND CONTROL SIGNAL
12306
THE SECOND DOWN-CONVERTED SIGNAL IS SUBTRACTED FROM THE FIRST DOWN-CONVERTED SIGNAL TO FORM A FIRST OUTPUT SIGNAL
12308
THE INPUT SIGNAL IS FREQUENCY DOWN-CONVERTED WITH A THIRD UNIVERSAL FREQUENCY DOWN-CONVERSION MODULE TO A THIRD DOWN-CONVERTED SIGNAL, ACCORDING TO A THIRD CONTROL SIGNAL
12310
THE INPUT SIGNAL IS FREQUENCY DOWN-CONVERTED WITH A FOURTH UNIVERSAL FREQUENCY DOWN-CONVERSION MODULE TO A FOURTH DOWN-CONVERTED SIGNAL, ACCORDING TO A FOURTH CONTROL SIGNAL
12312
THE FOURTH DOWN-CONVERTED SIGNAL IS SUBTRACTED FROM THE THIRD DOWN-CONVERTED SIGNAL TO FORM A SECOND OUTPUT SIGNAL
12314
A SIGNAL IS RE-RADIATED THAT COMPRISES ATTENUATED COMPONENTS OF FIRST, SECOND, THIRD, AND FOURTH CONTROL SIGNAL PULSES, WHEREIN THE ATTENUATED COMPONENTS OF THE FIRST, SECOND, THIRD, AND FOURTH CONTROL SIGNAL PULSES FORM A CUMULATIVE FREQUENCY
12316
THE FIRST, SECOND, THIRD, AND FOURTH CONTROL SIGNAL PULSES ARE CONFIGURED SUCH THAT THE CUMULATIVE FREQUENCY IS GREATER THAN A FREQUENCY OF THE INPUT SIGNAL
12318

FIG.123

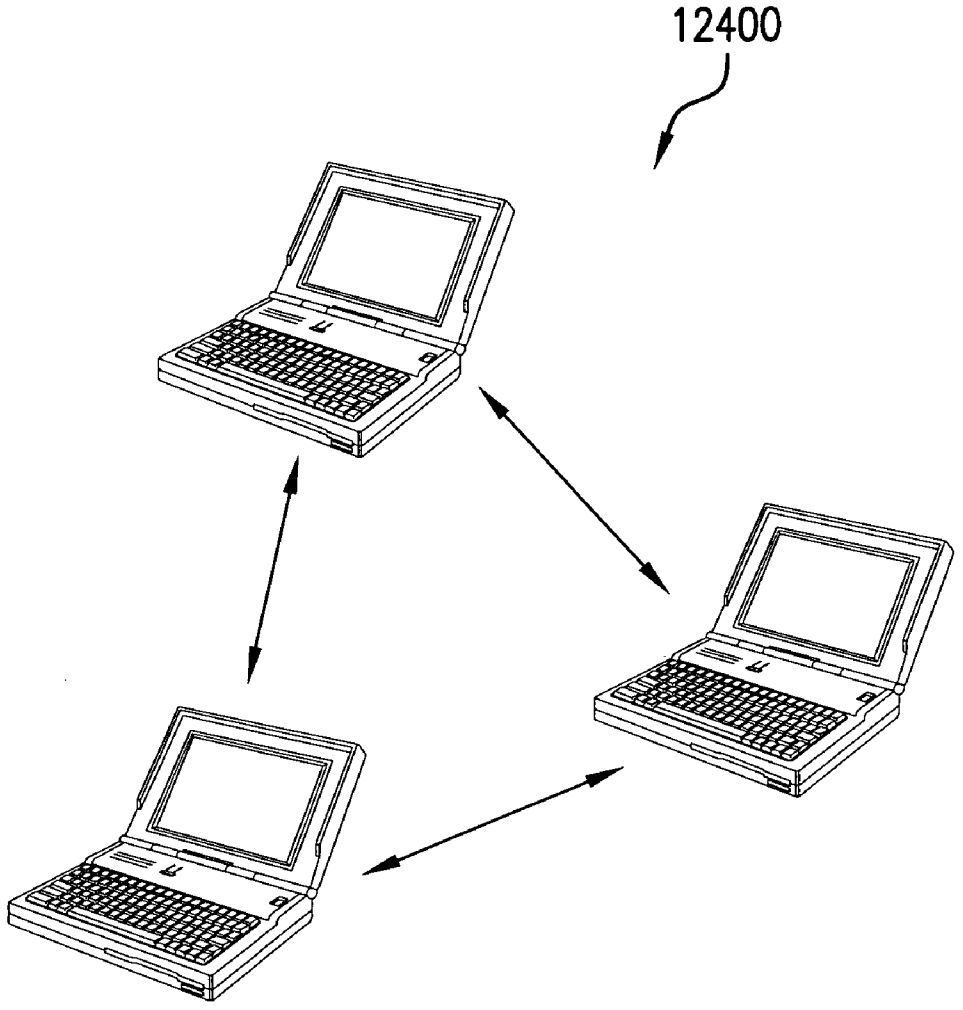


FIG. 124

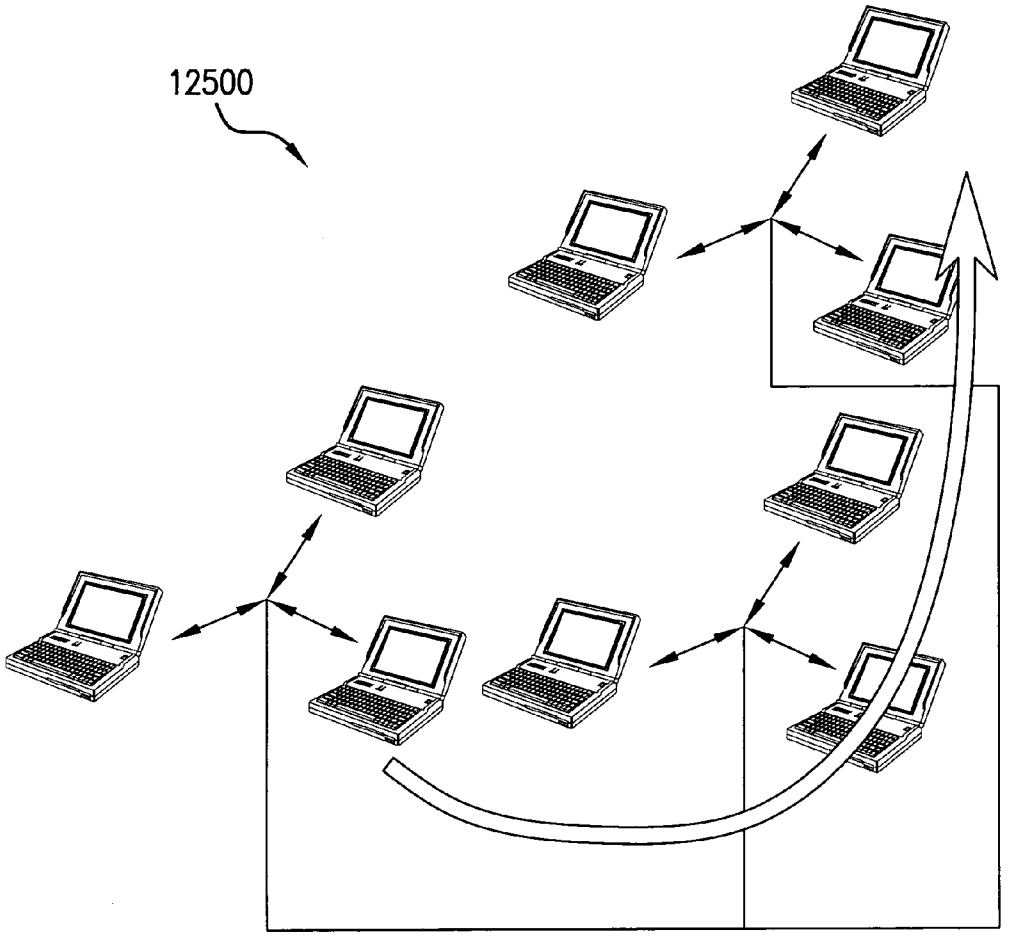


FIG. 125

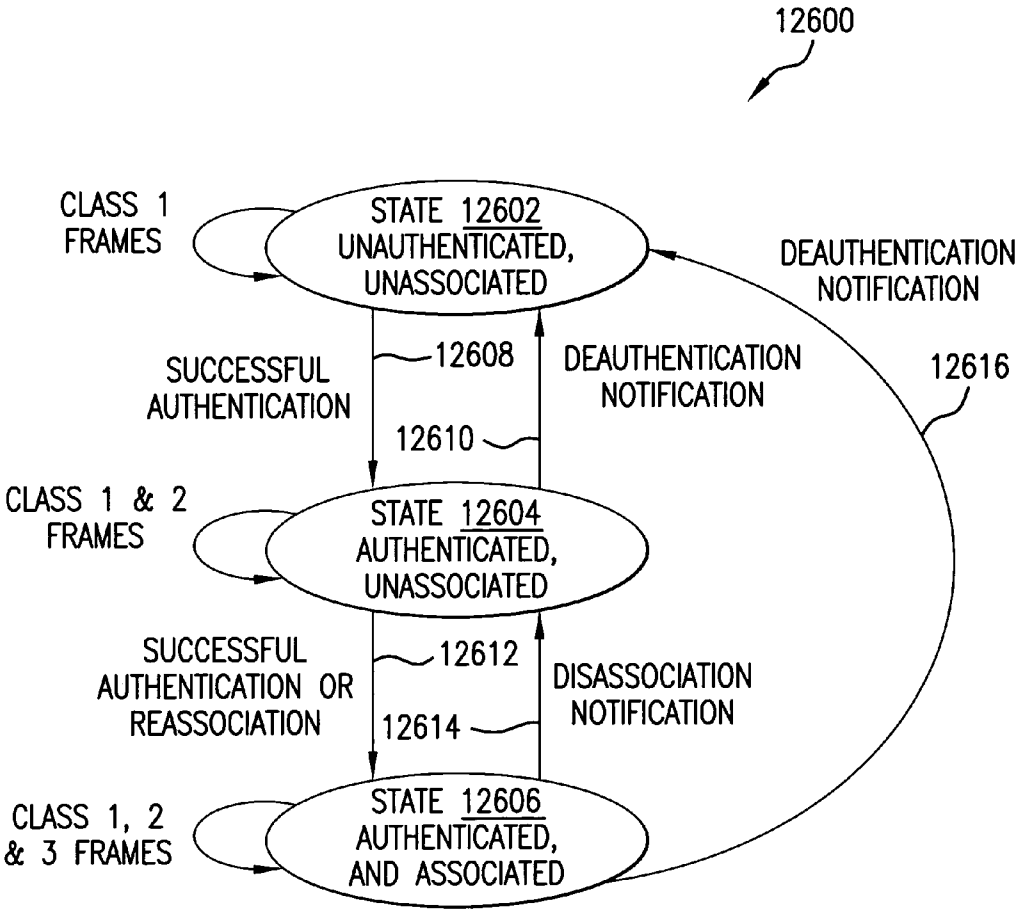

12600
CLASS 1 FRAMES
STATE 12602 UNAUTHENTICATED, UNASSOCIATED
DEAUTHENTICATION NOTIFICATION
SUCCESSFUL AUTHENTICATION
12608
DEAUTHENTICATION NOTIFICATION
12616
12610
CLASS 1 & 2 FRAMES
STATE 12604 AUTHENTICATED, UNASSOCIATED
SUCCESSFUL AUTHENTICATION OR REASSOCIATION
12612
DISASSOCIATION NOTIFICATION
12614
CLASS 1, 2 & 3 FRAMES
STATE 12606 AUTHENTICATED, AND ASSOCIATED

FIG.126

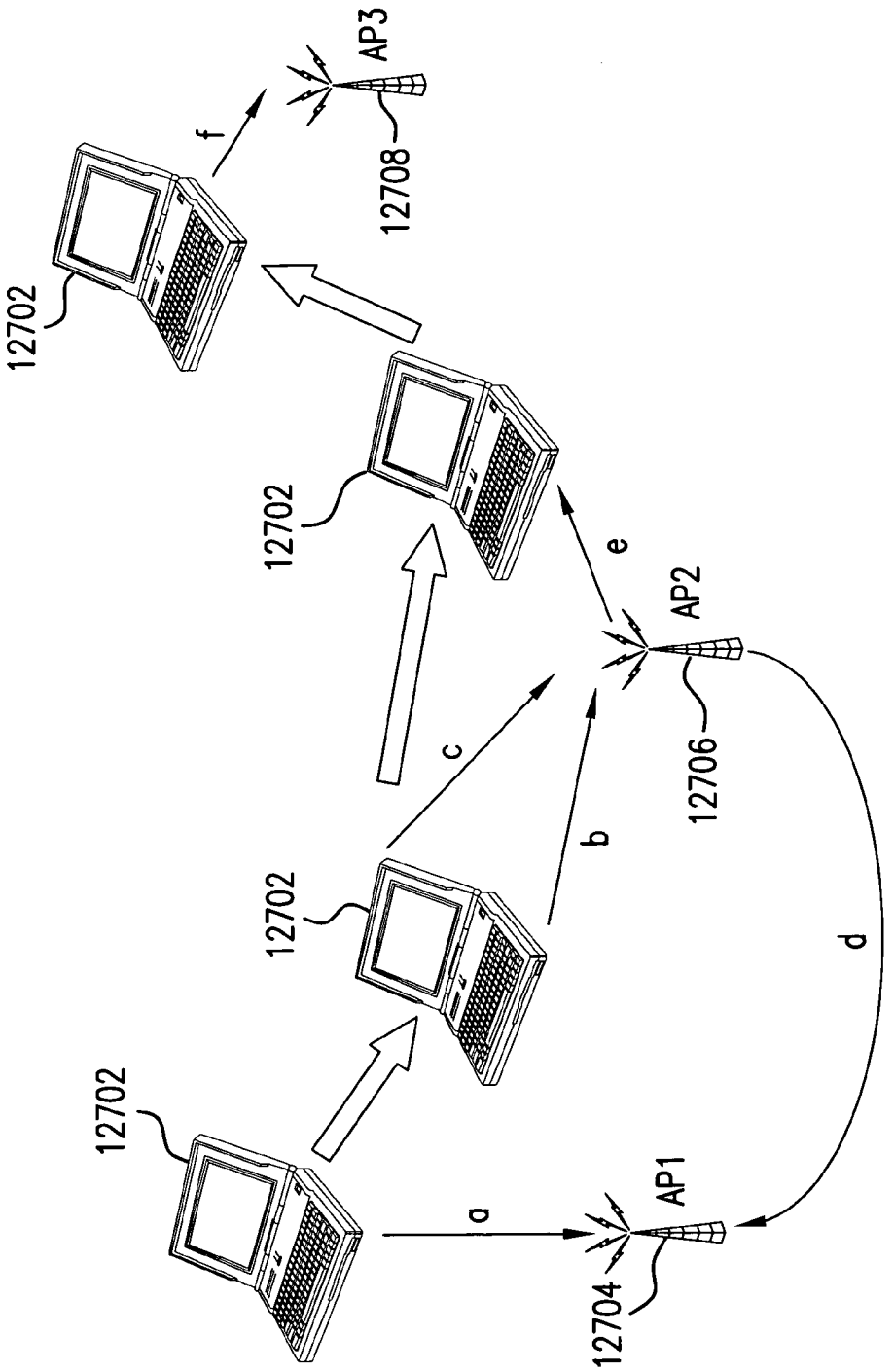

12702
12702
12702
12702
AP1
AP2
AP3
12704
12706
12708
a
b
c
d
e
f

FIG.127

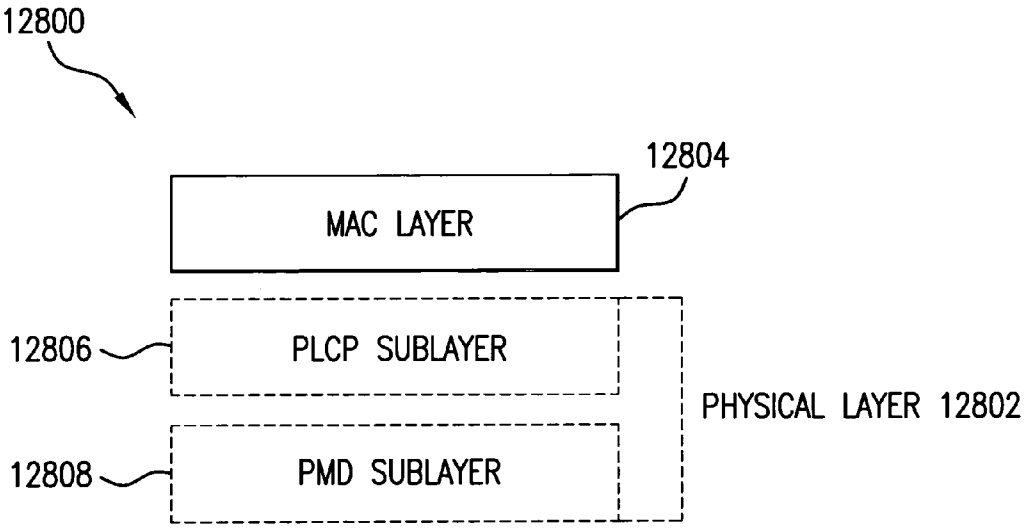

12800
12804
MAC LAYER
12806
PLCP SUBLAYER
PHYSICAL LAYER 12802
12808
PMD SUBLAYER

FIG.128A

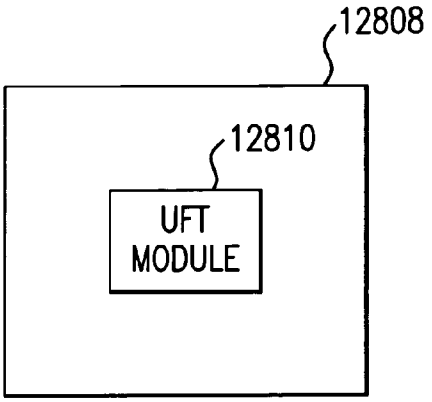


FIG.128B

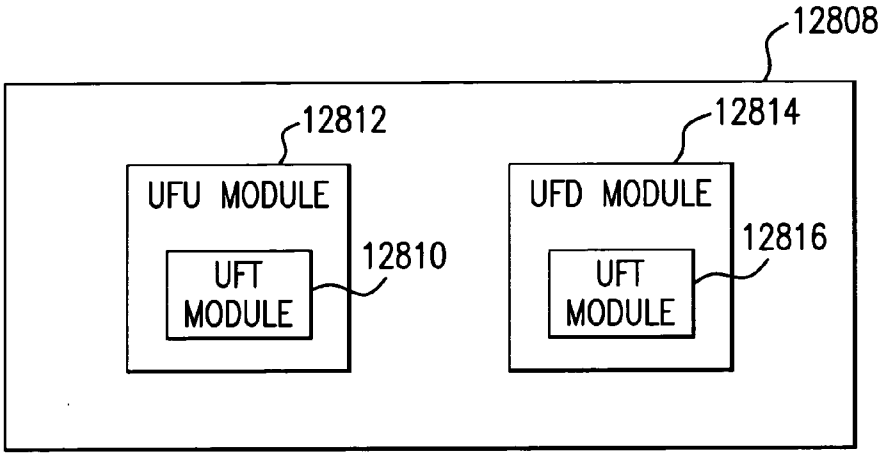


FIG.128C

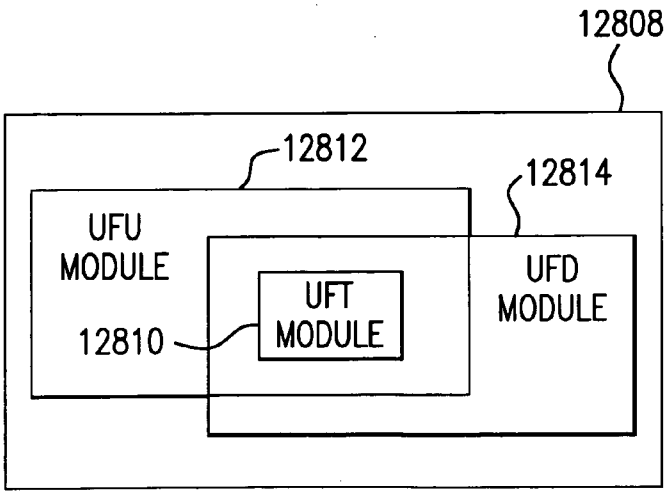


FIG.128D

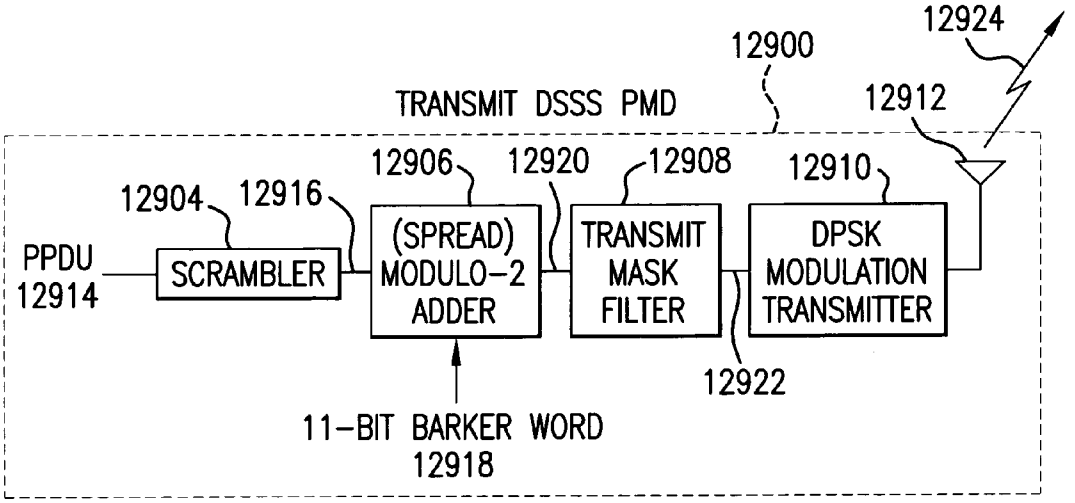


FIG.129A

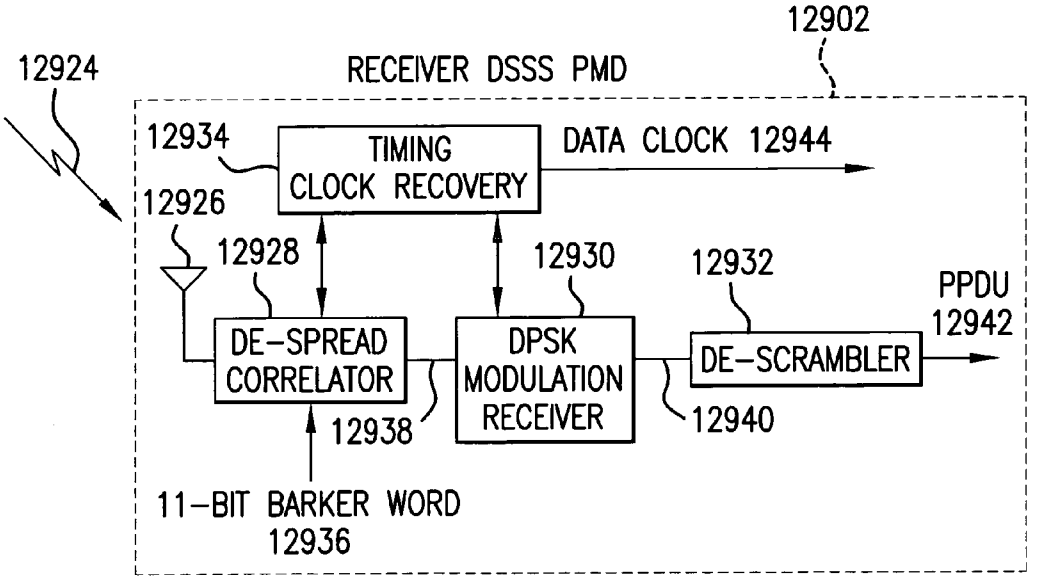


FIG.129B

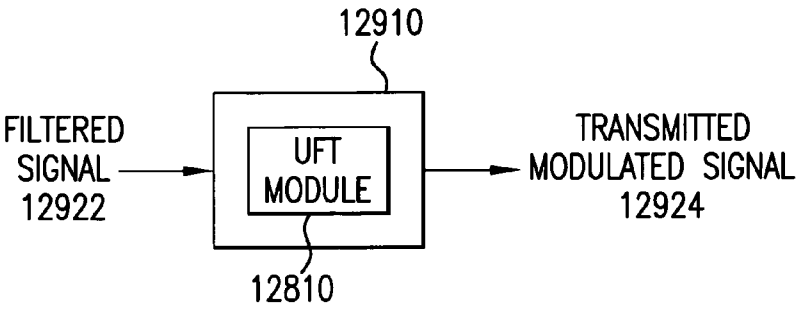


FIG.129C

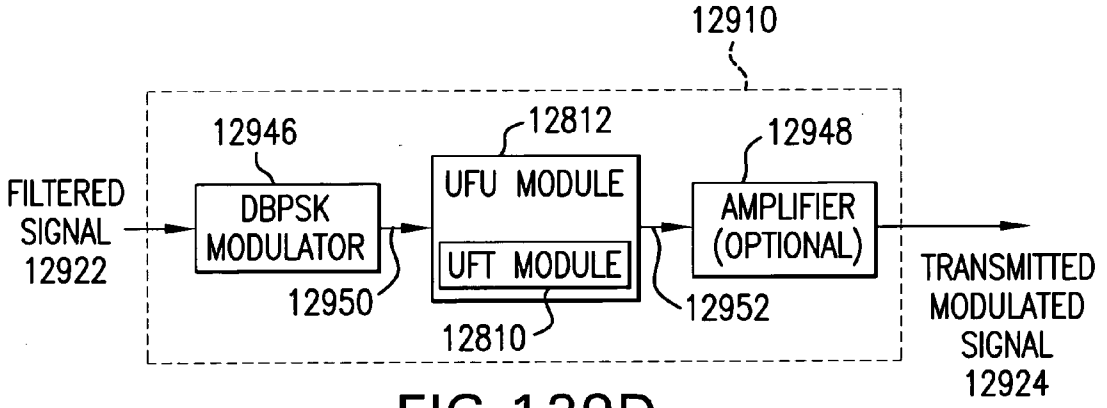


FIG.129D

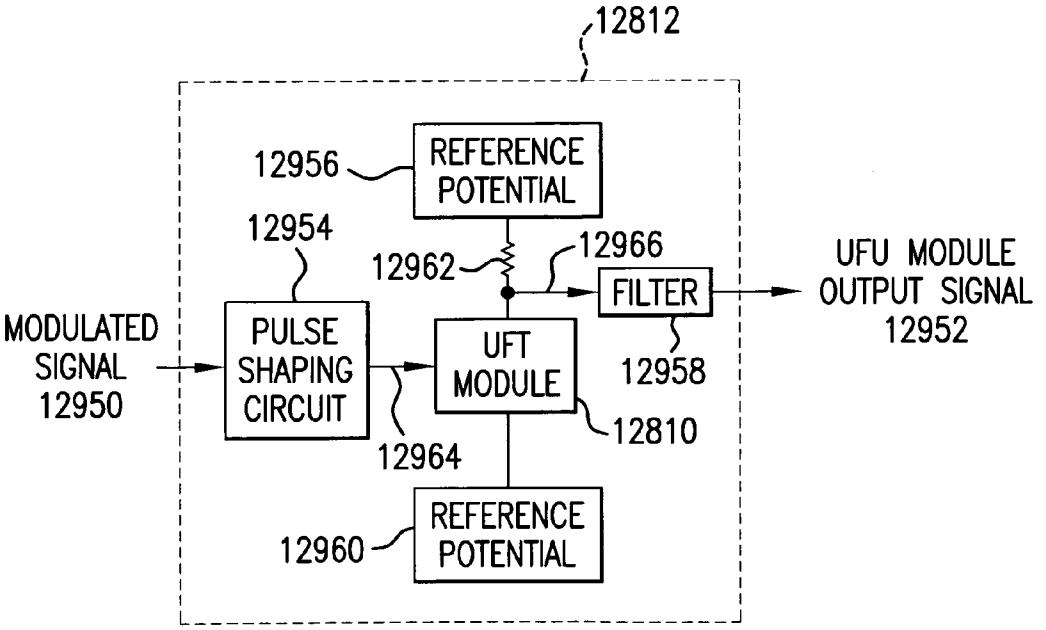


FIG.129E

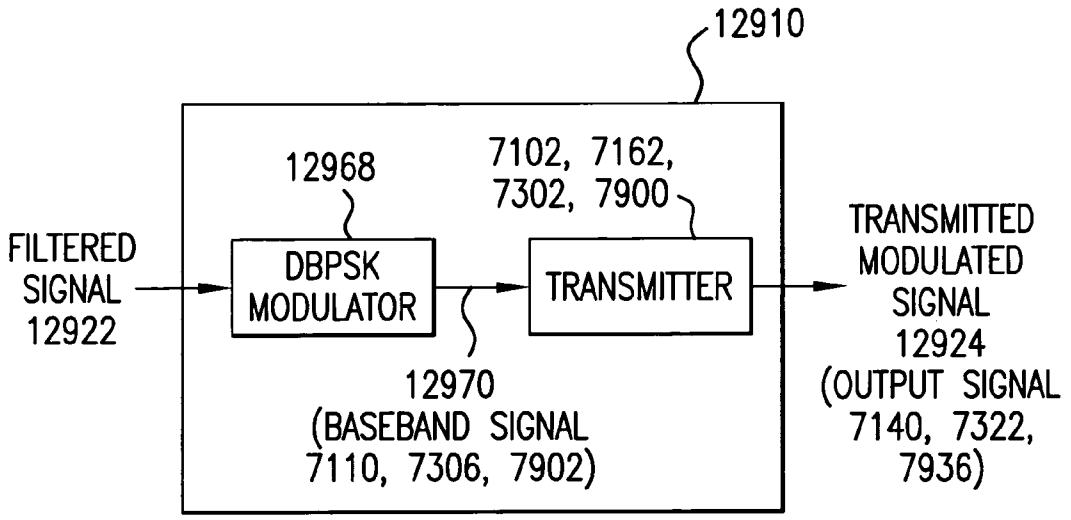


FIG.129F

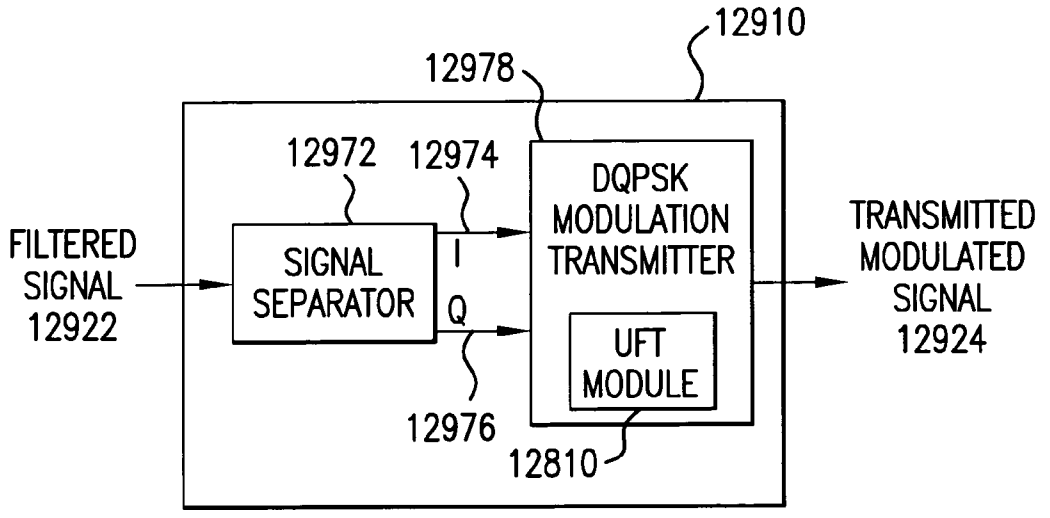


FIG.129G

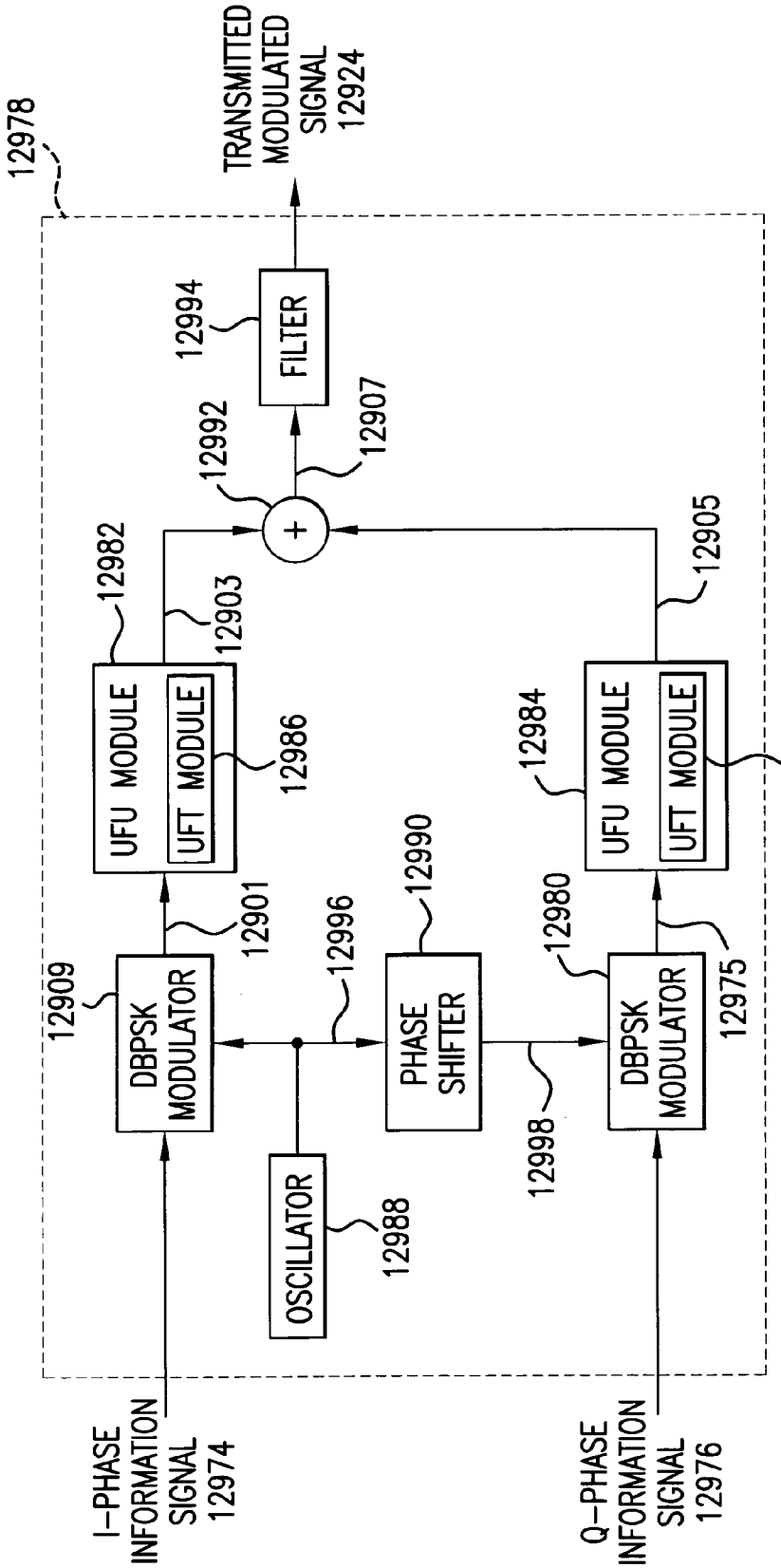

12978
TRANSMITTED MODULATED SIGNAL 12924
12994
FILTER
12907
12992
+
12905
12982
12903
UFU MODULE
UFT MODULE
12986
12984
UFU MODULE
UFT MODULE
12973
12990
12996
12901
12909
DBPSK MODULATOR
PHASE SHIFTER
12980
DBPSK MODULATOR
12975
12998
OSCILLATOR
12988
I-PHASE INFORMATION SIGNAL 12974
Q-PHASE INFORMATION SIGNAL 12976

FIG. 129H

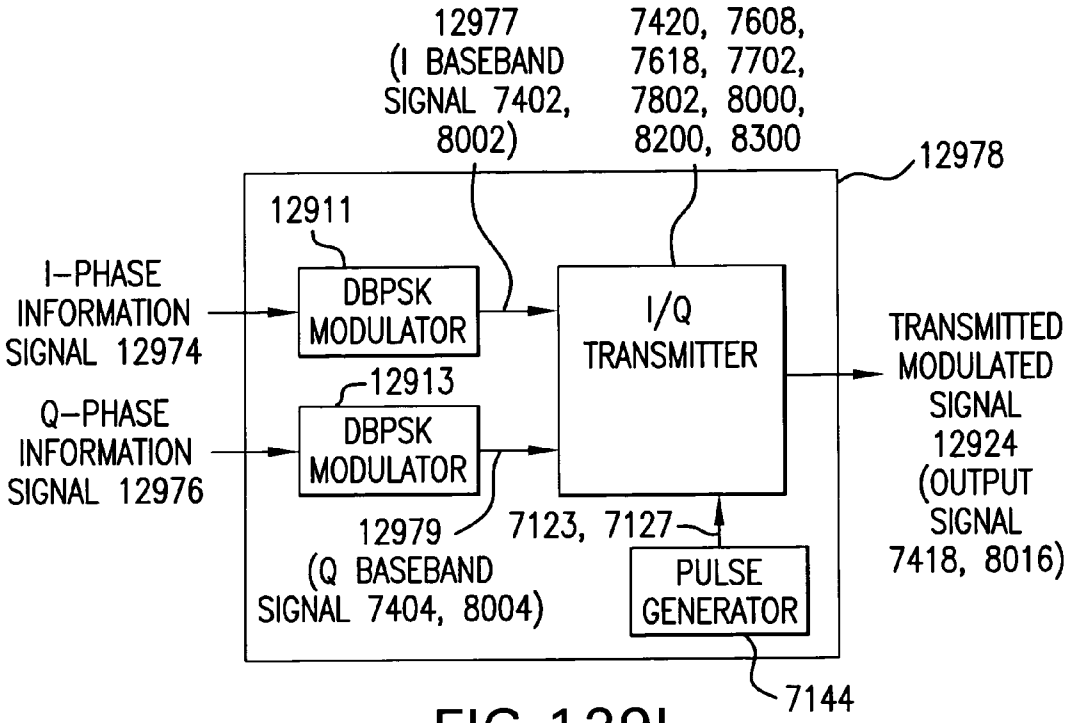


FIG.129I

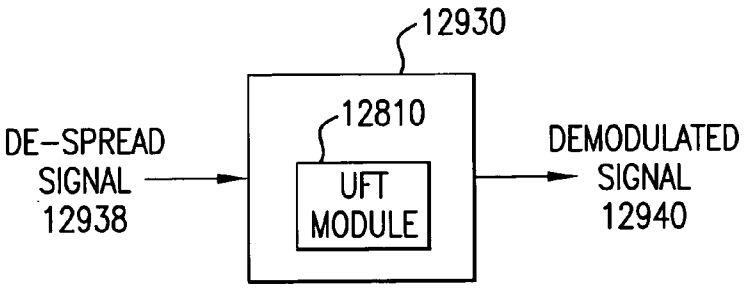


FIG.129J

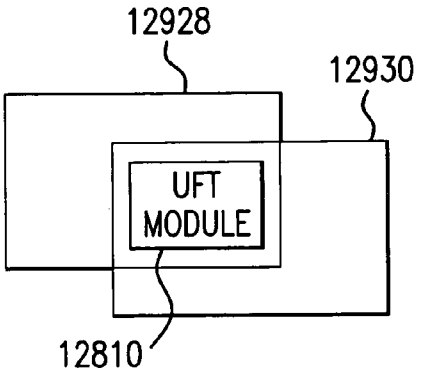


FIG.129K

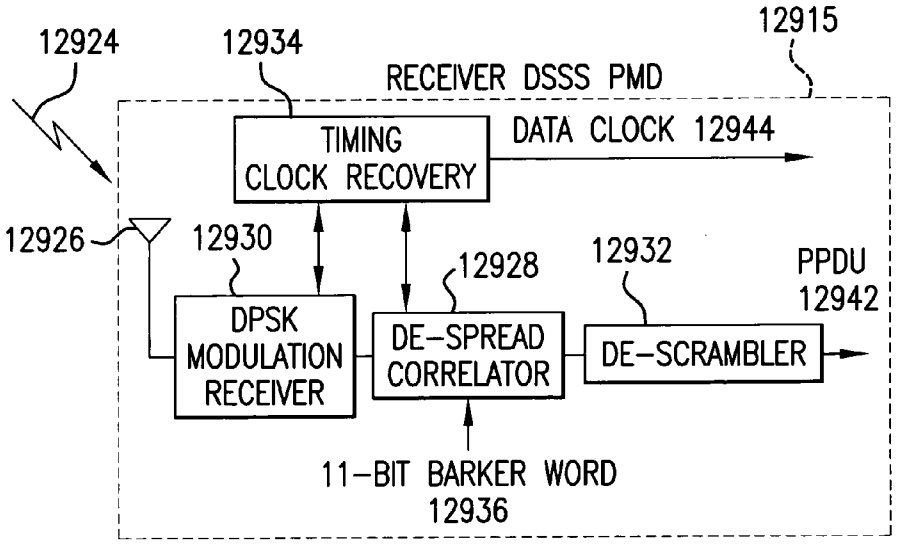


FIG.129L

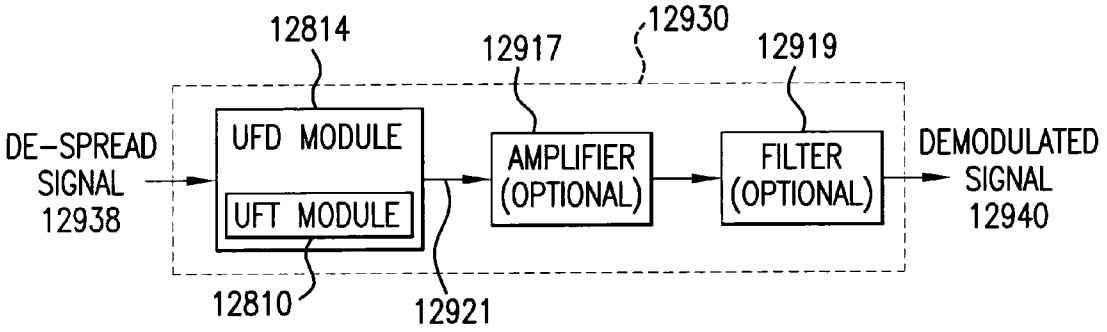


FIG.129M

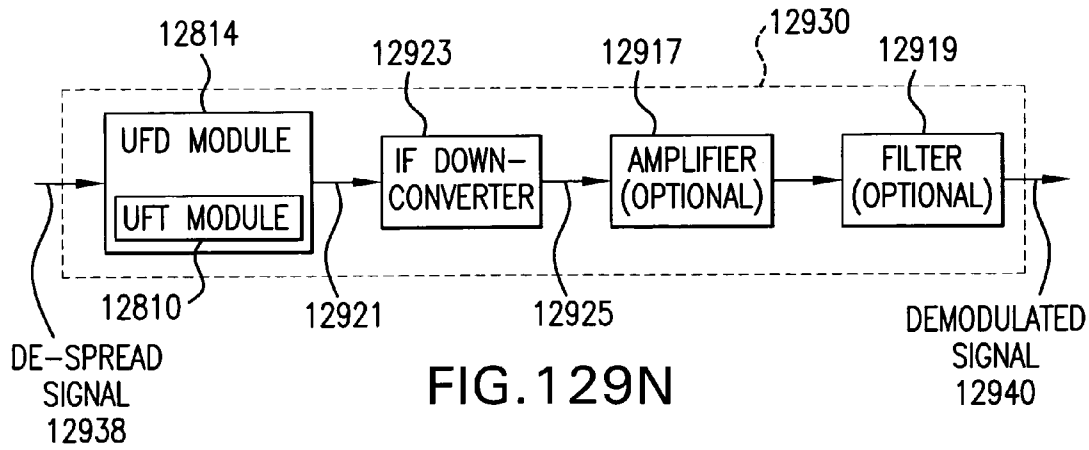


FIG.129N

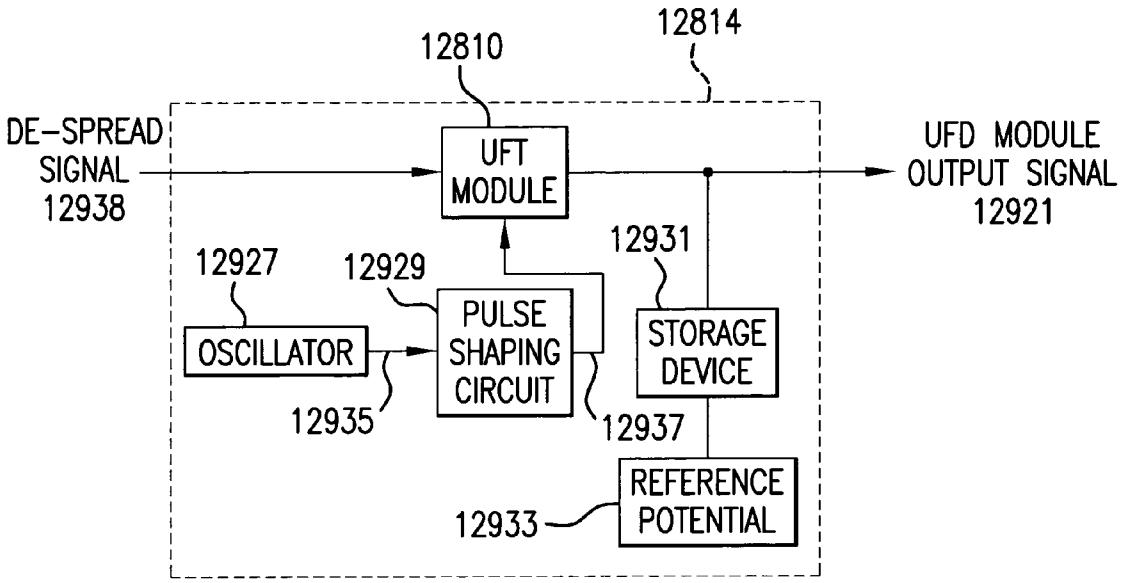


FIG.129O

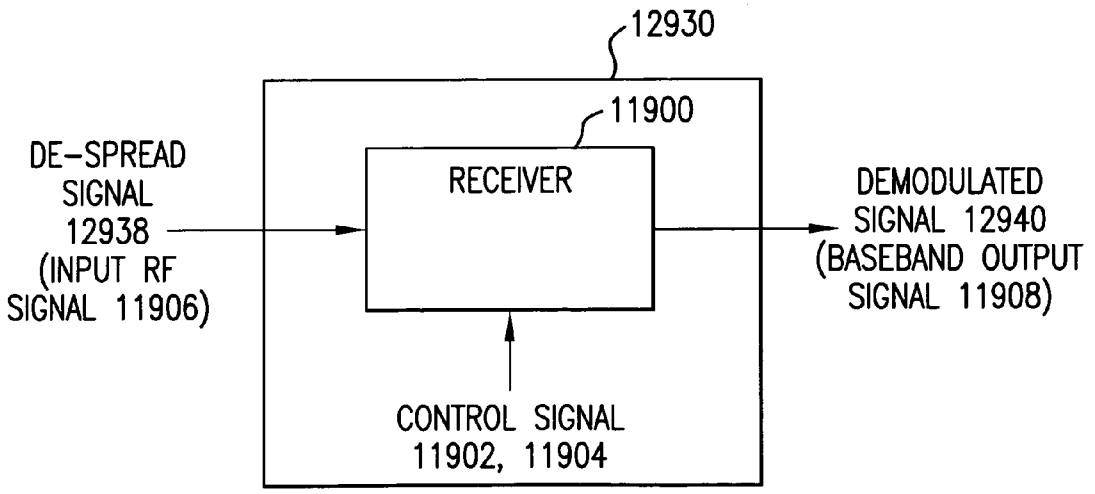


FIG.129P

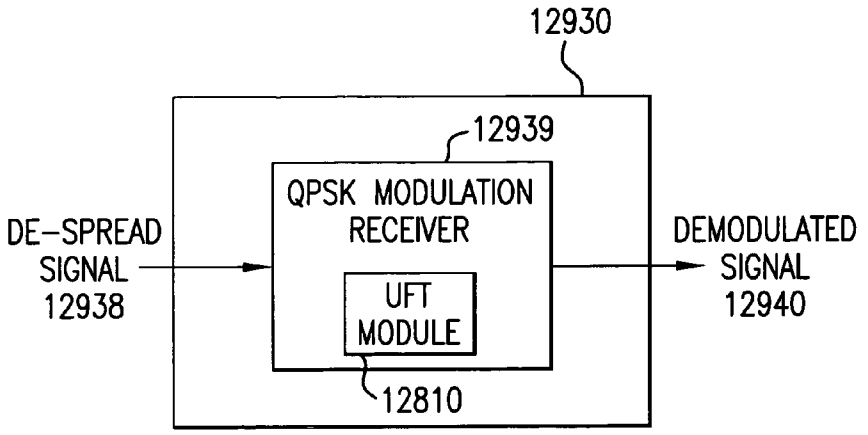


FIG.129Q

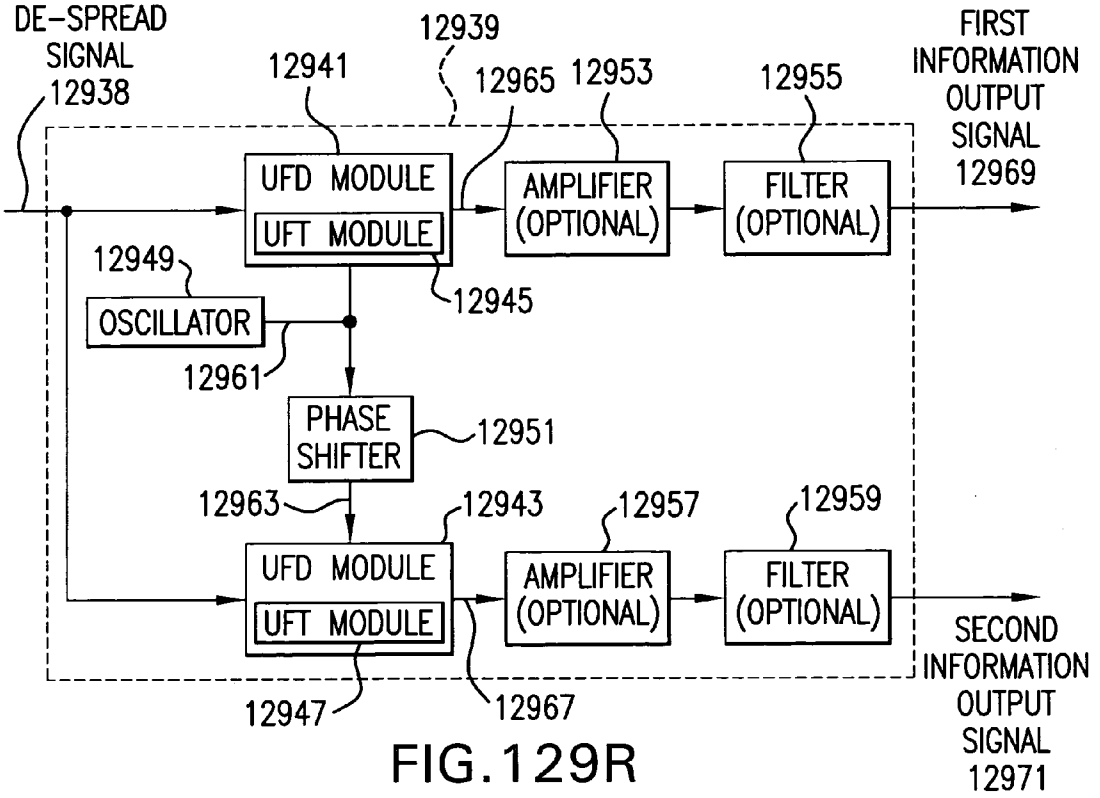


FIG.129R

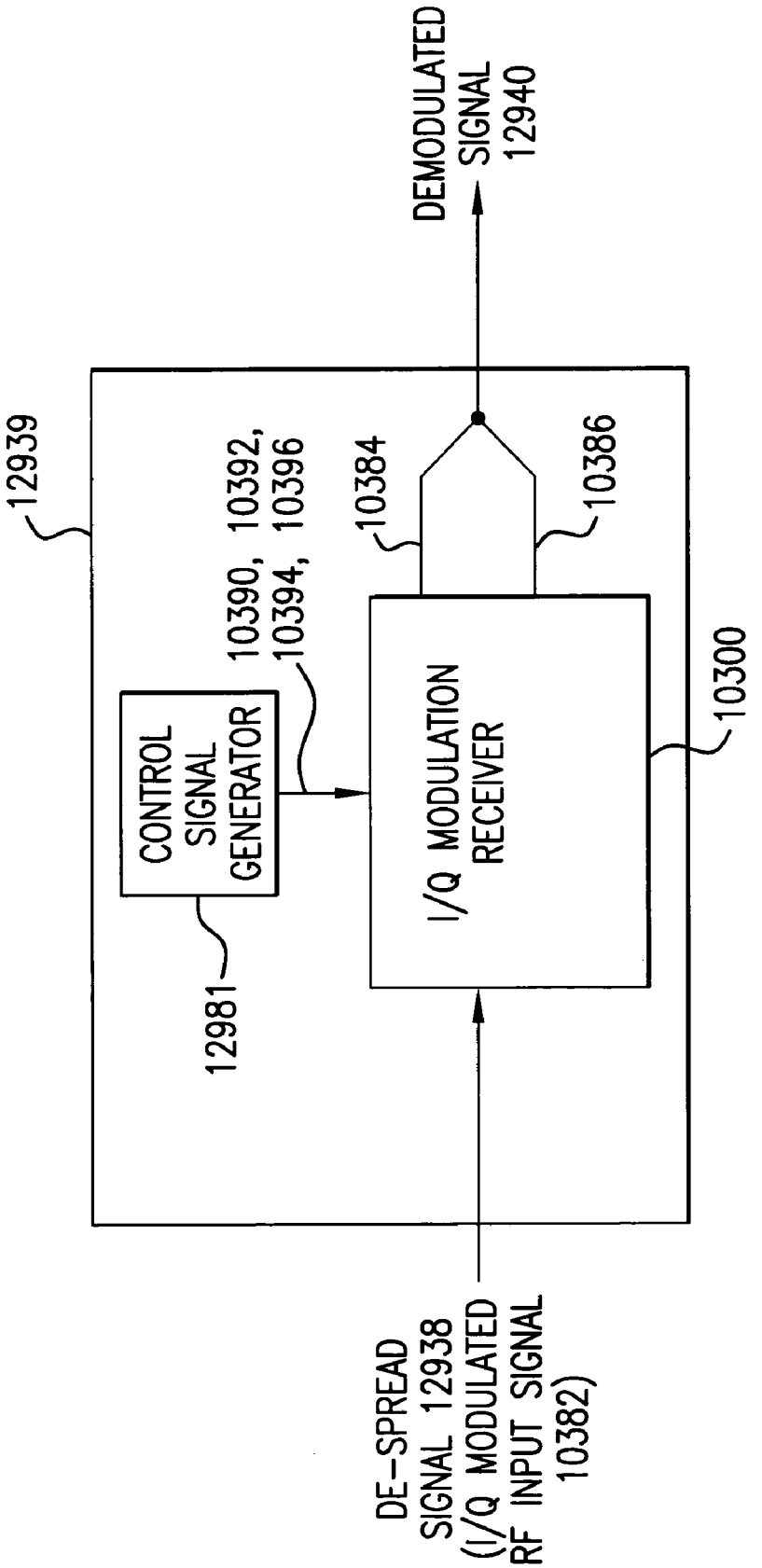

DEMODULATED SIGNAL 12940
12939
10384
10386
10392, 10396
10390, 10394,
CONTROL SIGNAL GENERATOR
I/Q MODULATION RECEIVER
10300
12981
DE-SPREAD SIGNAL 12938 (I/Q MODULATED RF INPUT SIGNAL 10382)

FIG.129S

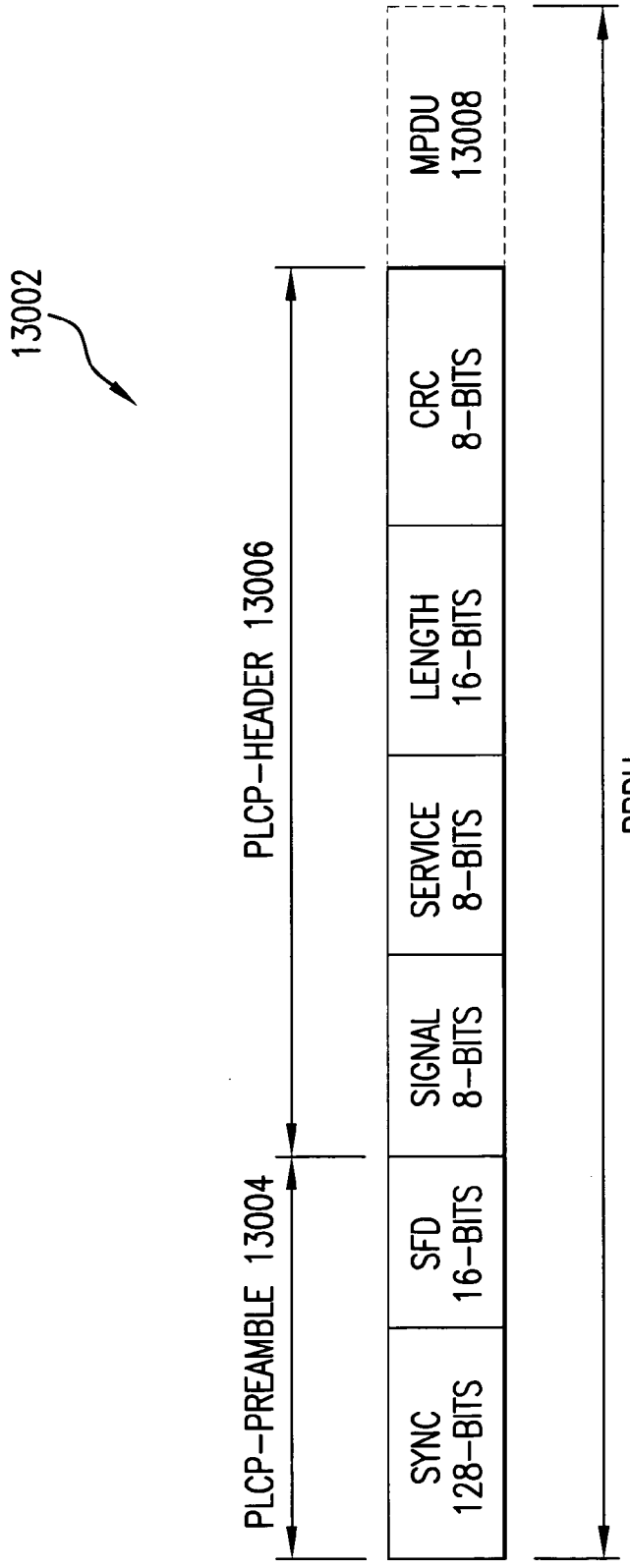

13002
PLCP–PREAMBLE 13004
PLCP–HEADER 13006
SYNC 128–BITS
SFD 16–BITS
SIGNAL 8–BITS
SERVICE 8–BITS
LENGTH 16–BITS
CRC 8–BITS
MPDU 13008
PPDU

FIG.130

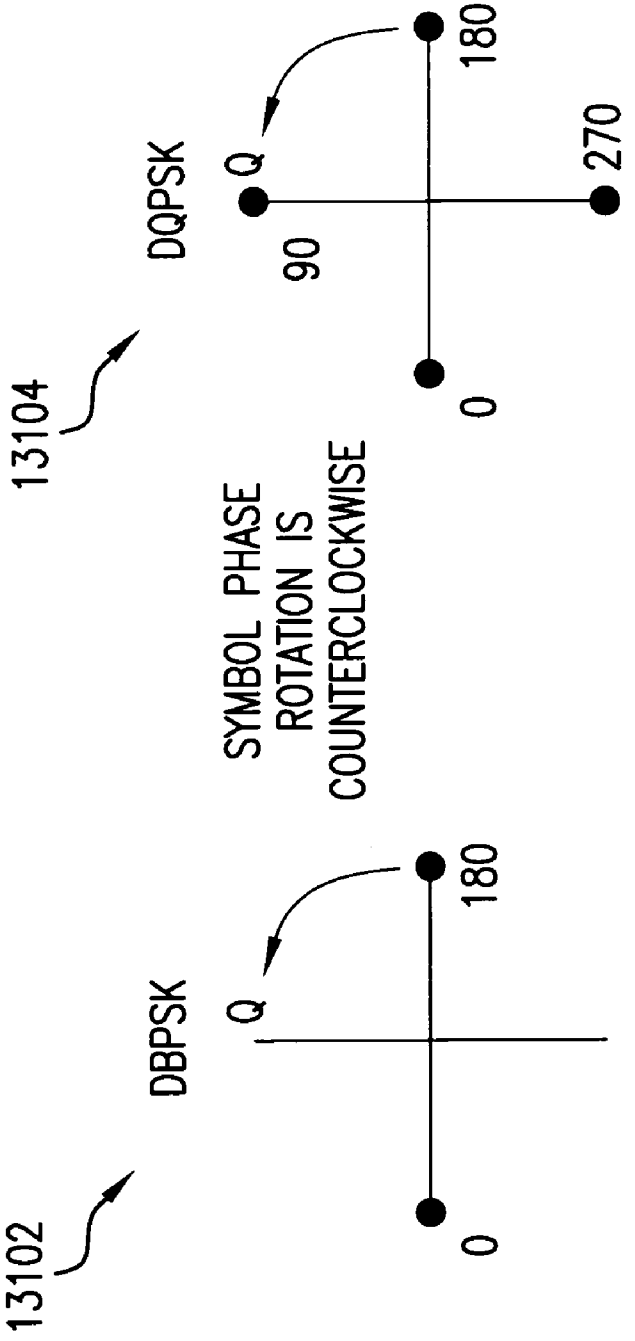

13102
DBPSK
Q
180
0
13104
DQPSK
Q
180
270
90
0
SYMBOL PHASE
ROTATION IS
COUNTERCLOCKWISE

FIG. 131

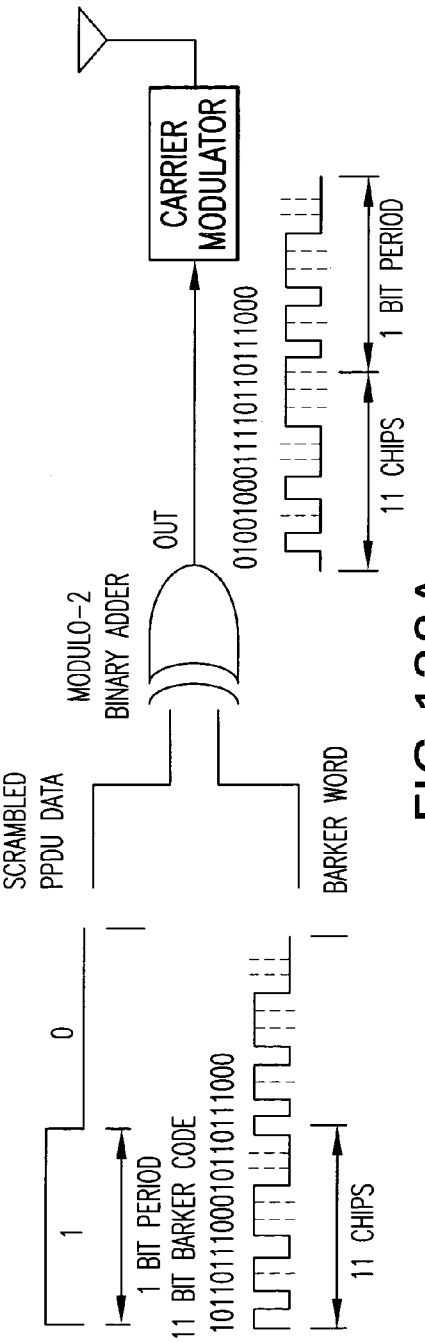
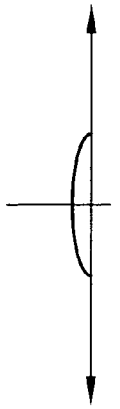


FIG.132A



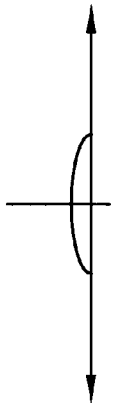
TRANSMITTER BASEBAND SIGNAL BEFORE SPREADING

FIG.132B



RECEIVER BASEBAND SIGNAL BEFORE CORRELATION

FIG.132D



TRANSMITTER BASEBAND SIGNAL AFTER SPREADING

FIG.132C

RECEIVER BASEBAND SIGNAL AFTER CORRELATION

FIG.132E

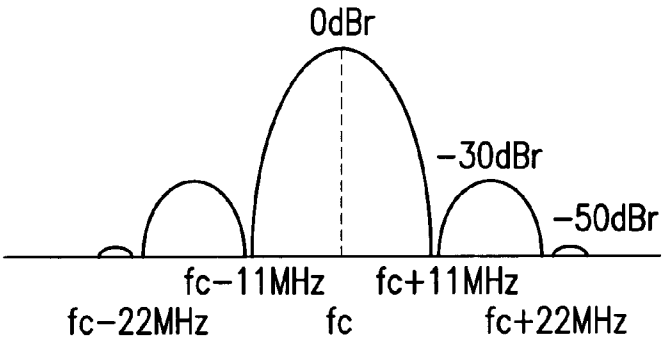


FIG.133

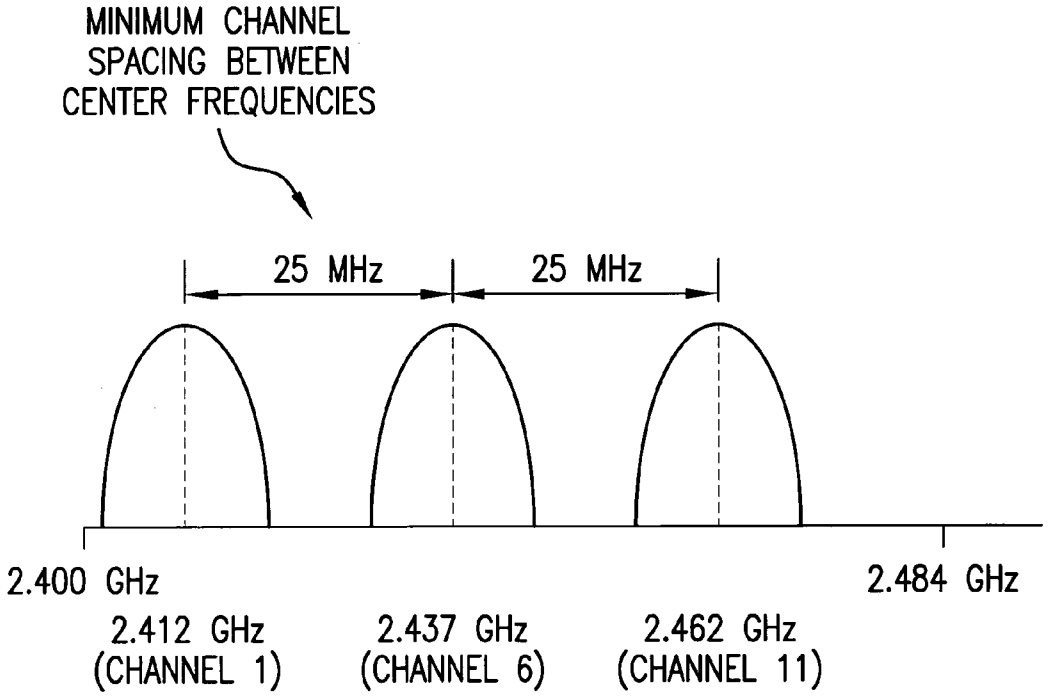


FIG.134

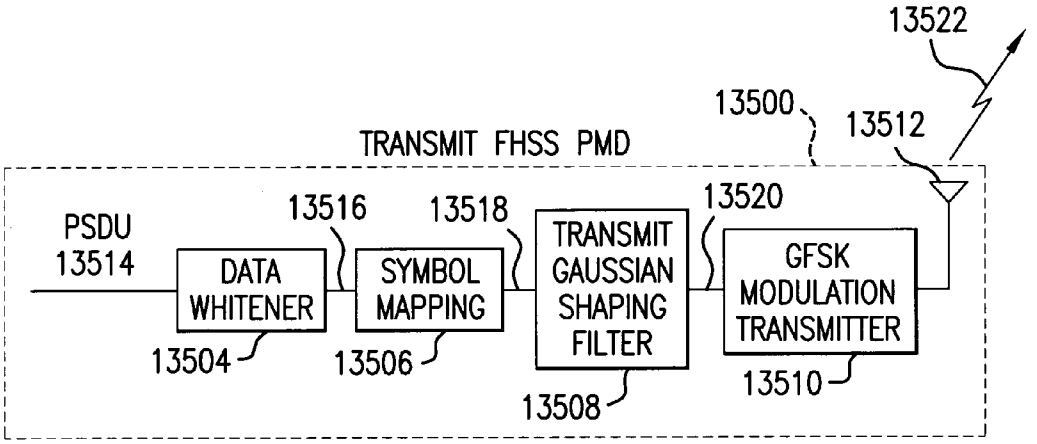


FIG.135A

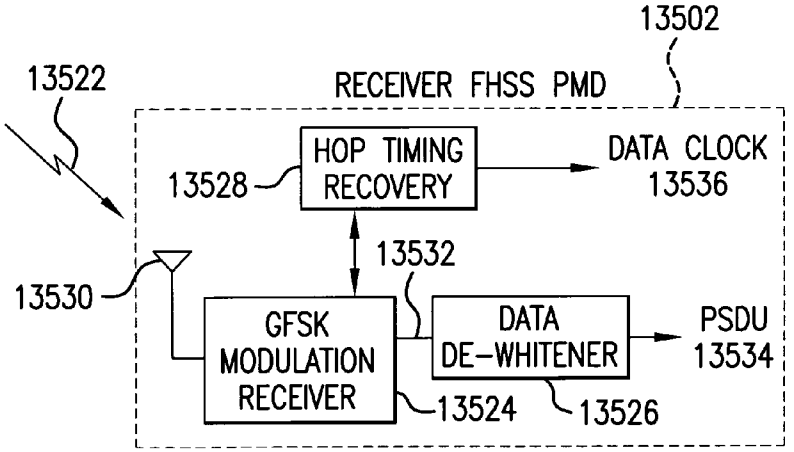


FIG.135B

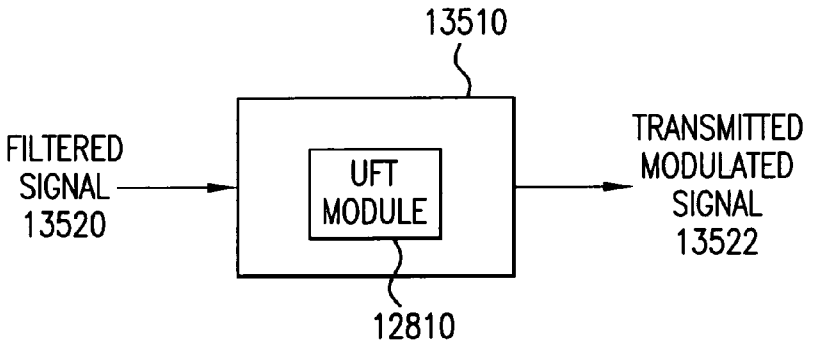


FIG.135C

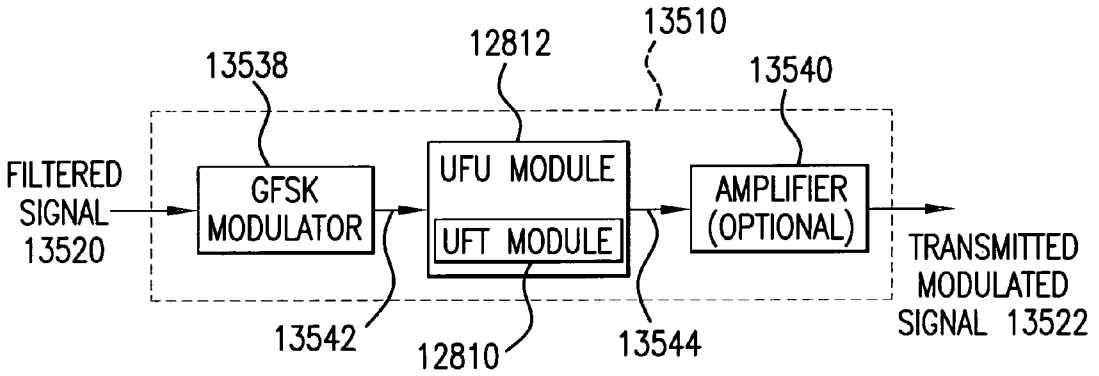


FIG.135D

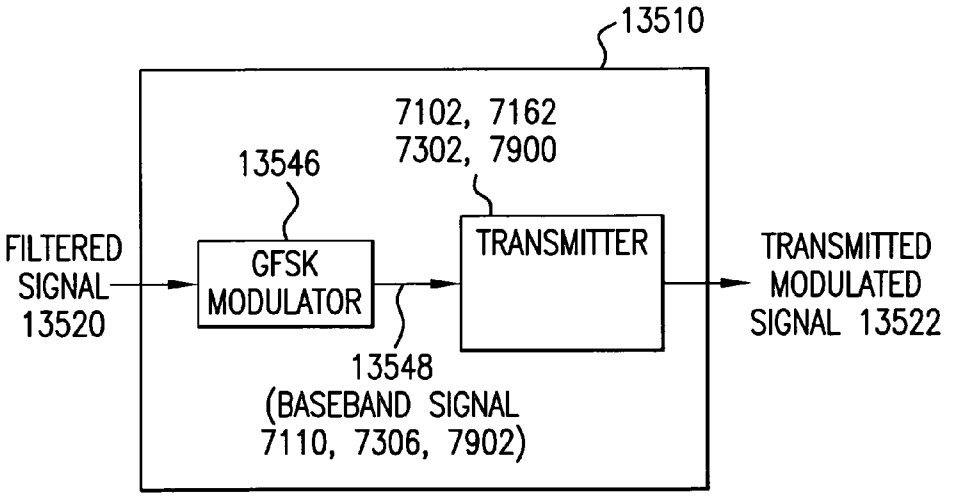


FIG.135E

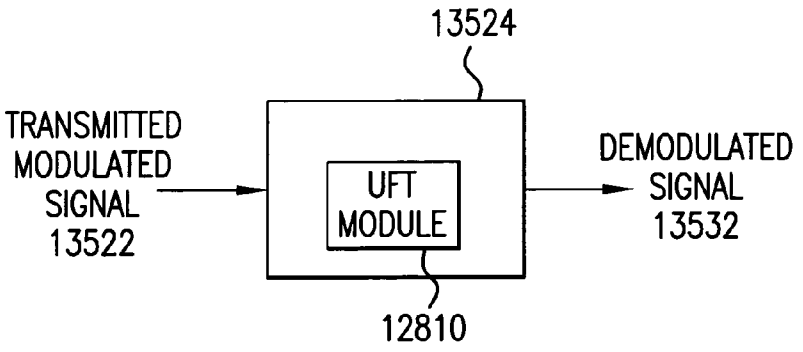


FIG.135F

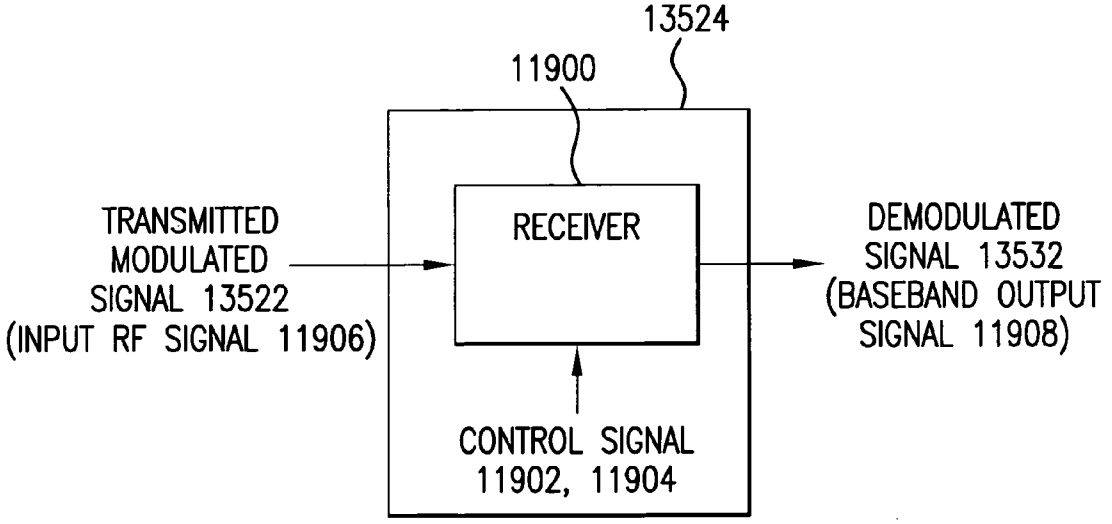


FIG.135G

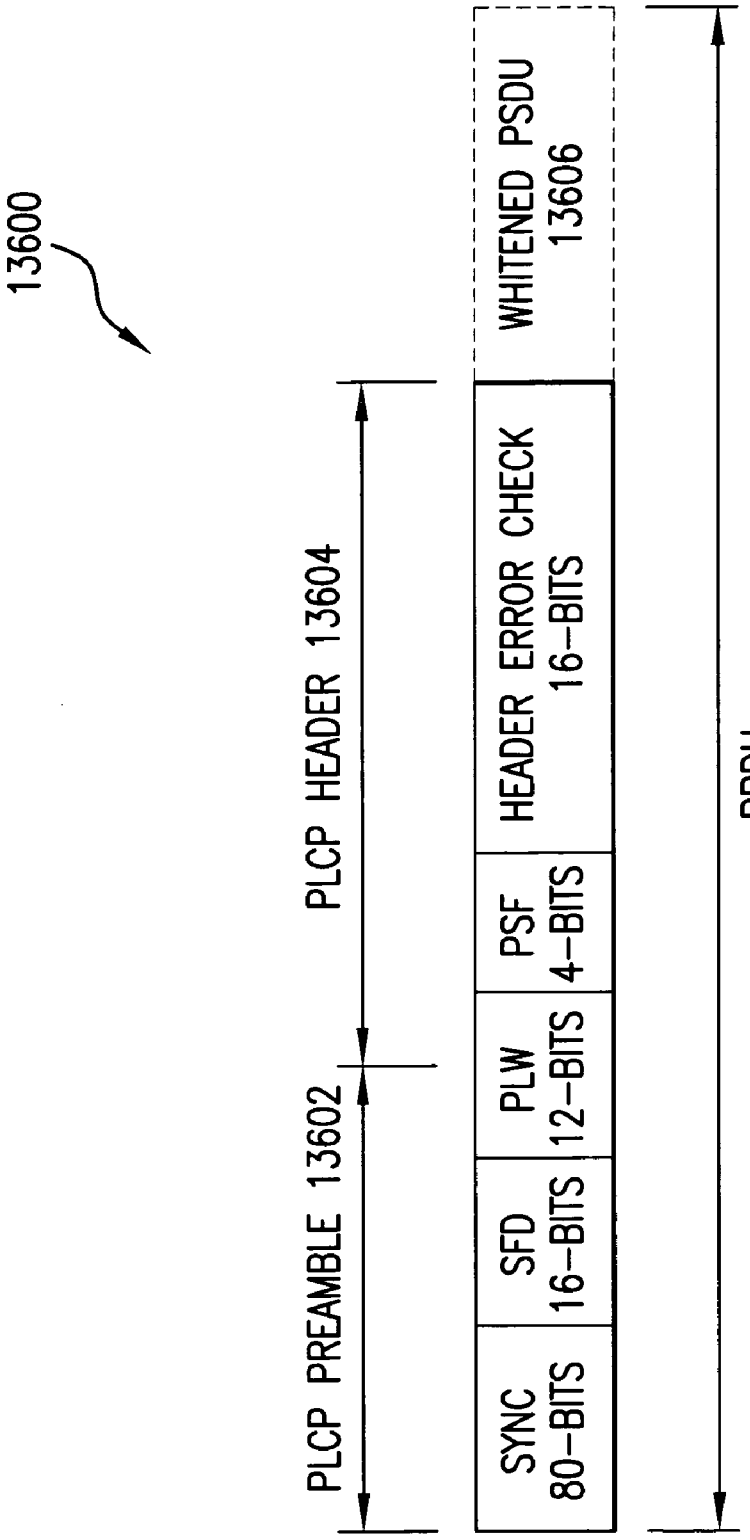

13600
PLCP PREAMBLE 13602
PLCP HEADER 13604
SYNC 80-BITS
SFD 16-BITS
PLW 12-BITS
PSF 4-BITS
HEADER ERROR CHECK 16-BITS
WHITENED PSDU 13606
PPDU

FIG.136

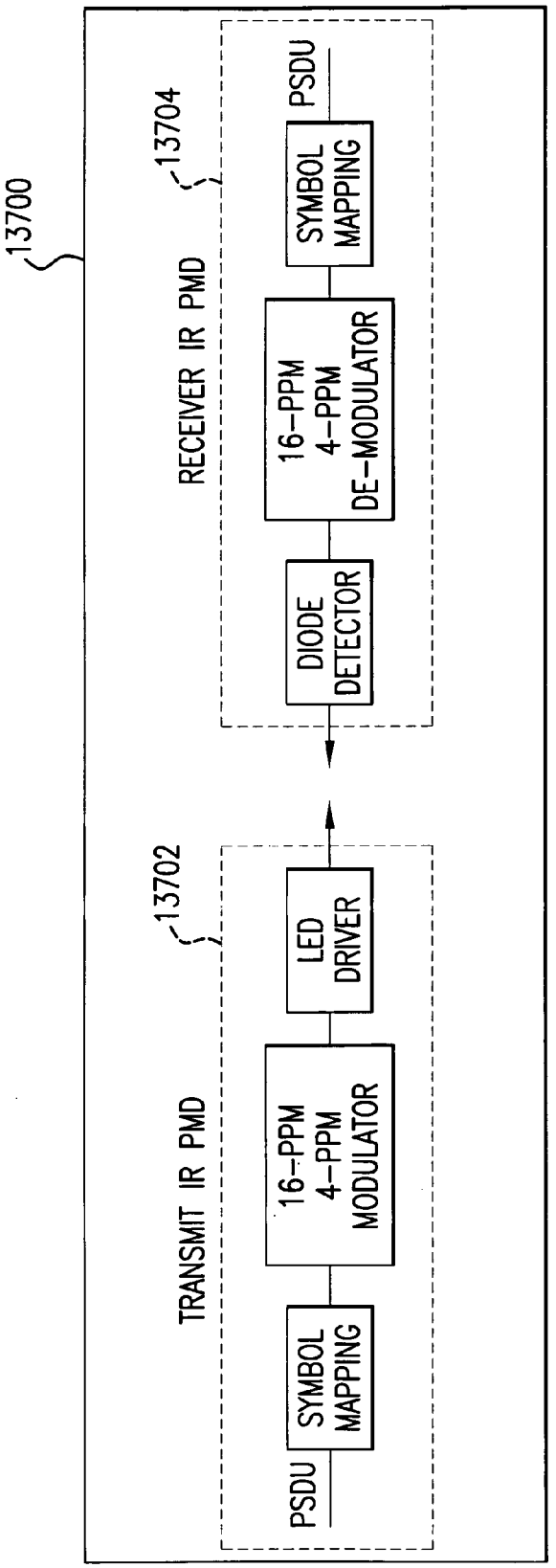

13700
13704
RECEIVER IR PMD
PSDU
SYMBOL MAPPING
16-PPM 4-PPM DE-MODULATOR
DIODE DETECTOR
13702
TRANSMIT IR PMD
LED DRIVER
16-PPM 4-PPM MODULATOR
SYMBOL MAPPING
PSDU

FIG.137

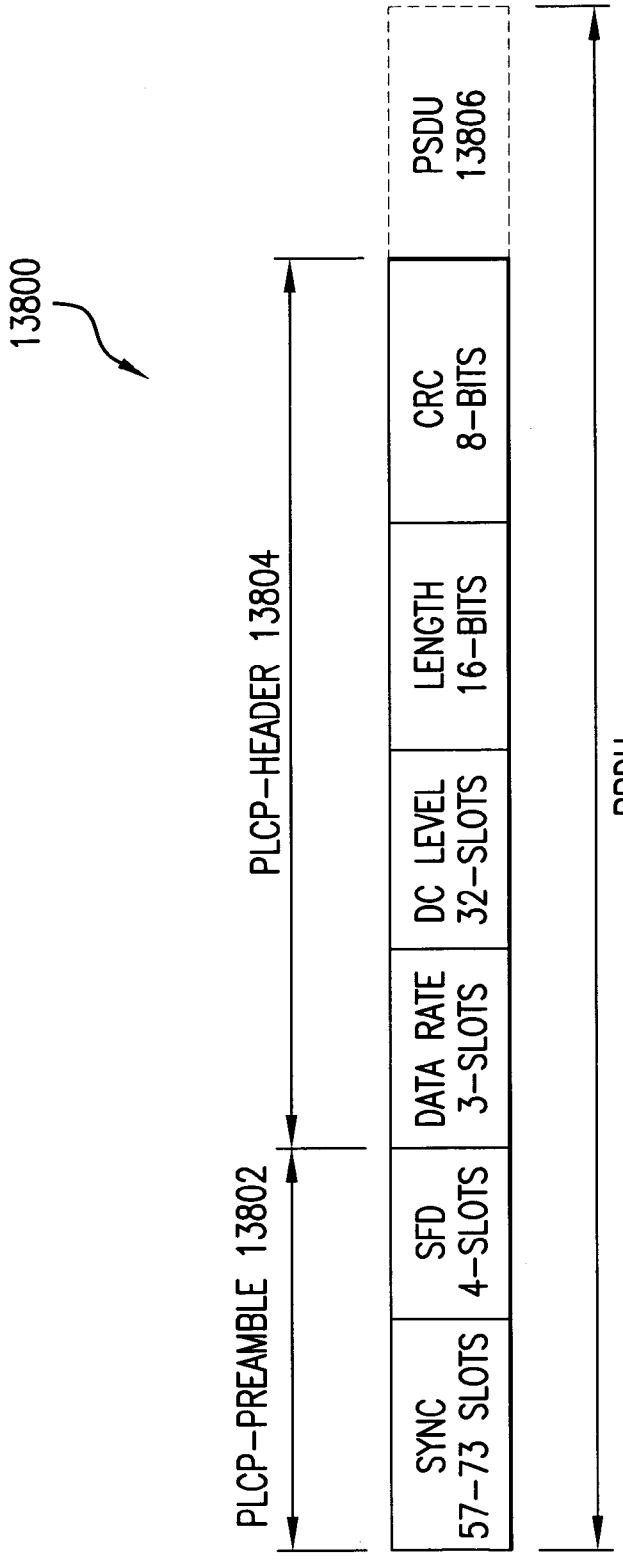

13800
PLCP-PREAMBLE 13802
PLCP-HEADER 13804
PPDU
SYNC 57-73 SLOTS
SFD 4-SLOTS
DATA RATE 3-SLOTS
DC LEVEL 32-SLOTS
LENGTH 16-BITS
CRC 8-BITS
PSDU 13806

FIG.138

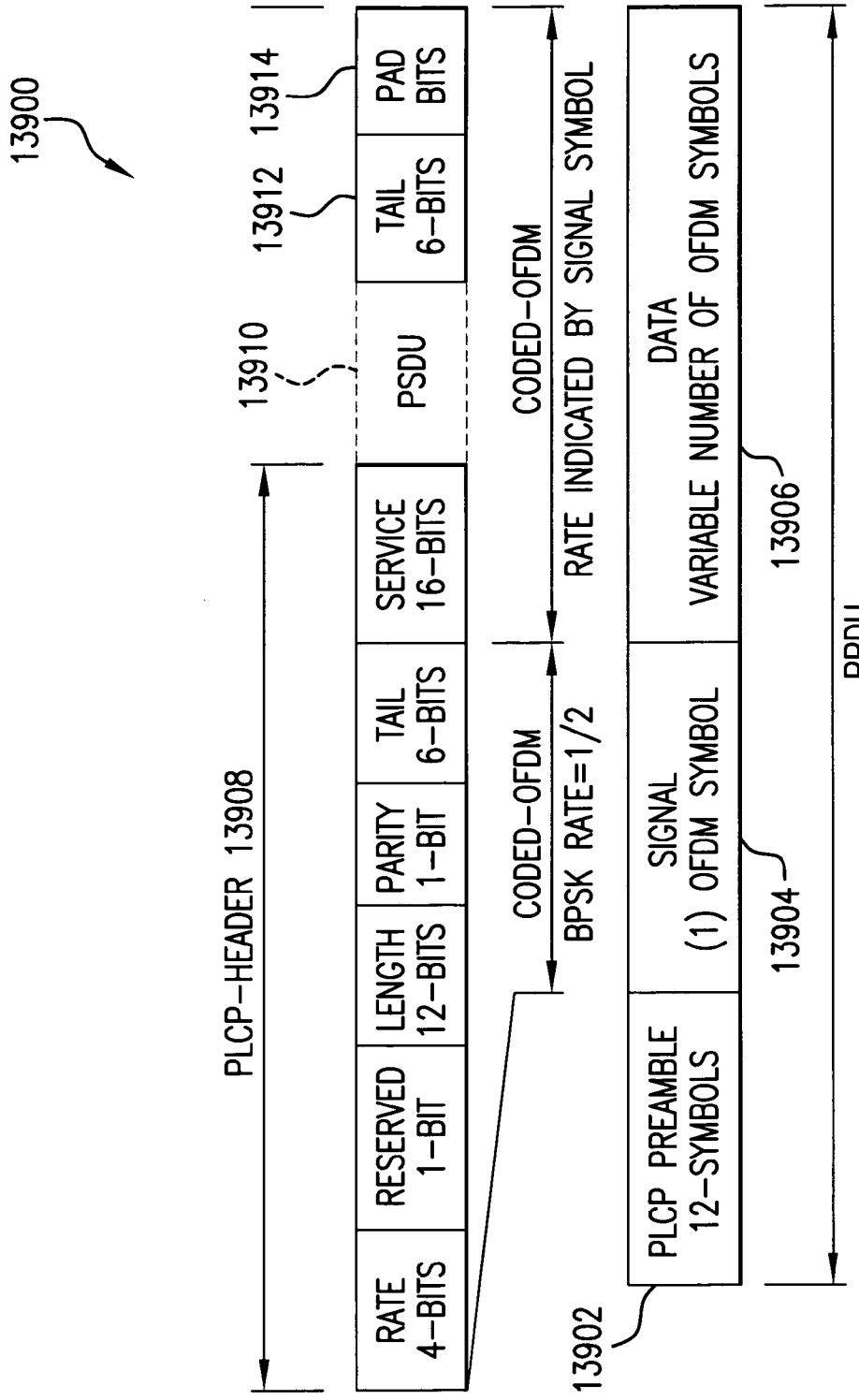

13900
PLCP-HEADER 13908
RATE 4-BITS
RESERVED 1-BIT
LENGTH 12-BITS
PARITY 1-BIT
TAIL 6-BITS
SERVICE 16-BITS
13910
PSDU
13912
TAIL 6-BITS
13914
PAD BITS
CODED-OFDM
BPSK RATE=1/2
RATE INDICATED BY SIGNAL SYMBOL
13902
PLCP PREAMBLE 12-SYMBOLS
SIGNAL (1) OFDM SYMBOL
DATA VARIABLE NUMBER OF OFDM SYMBOLS
13904
13906
PPDU

FIG.139

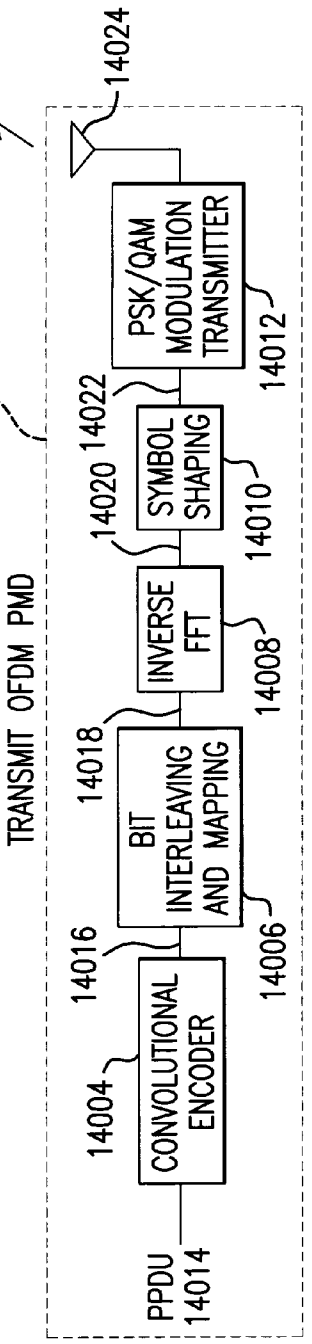


FIG. 140A

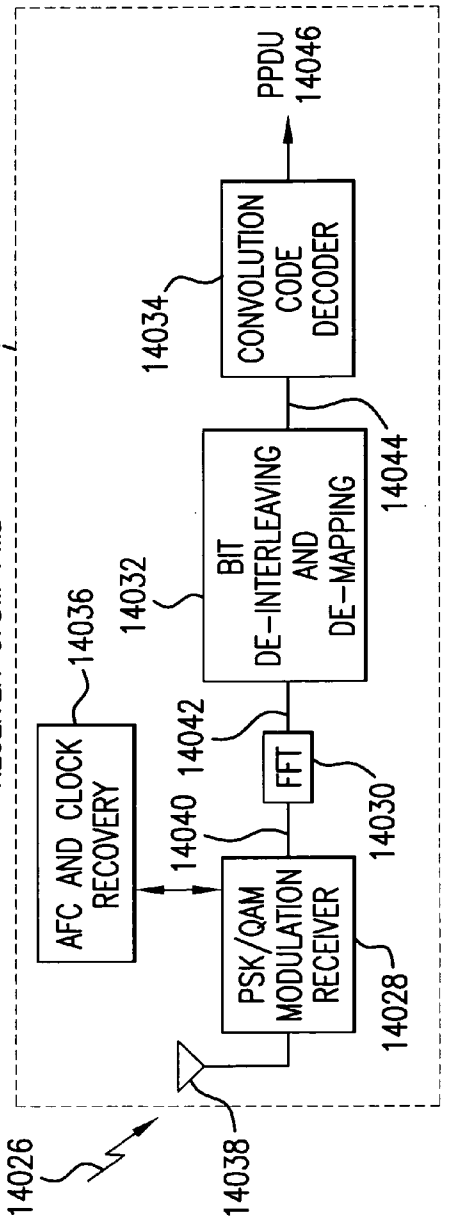


FIG. 140B

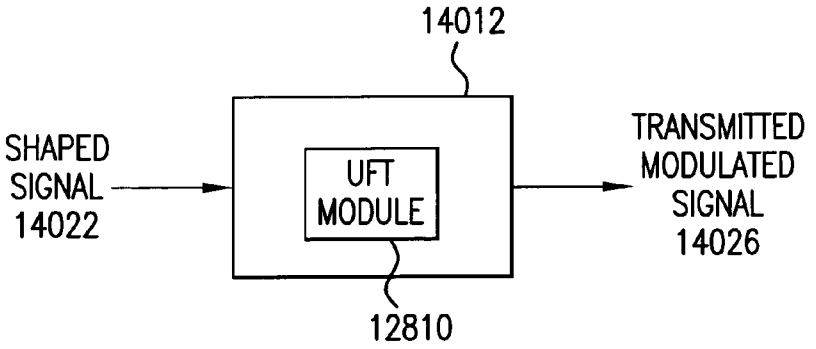


FIG.140C

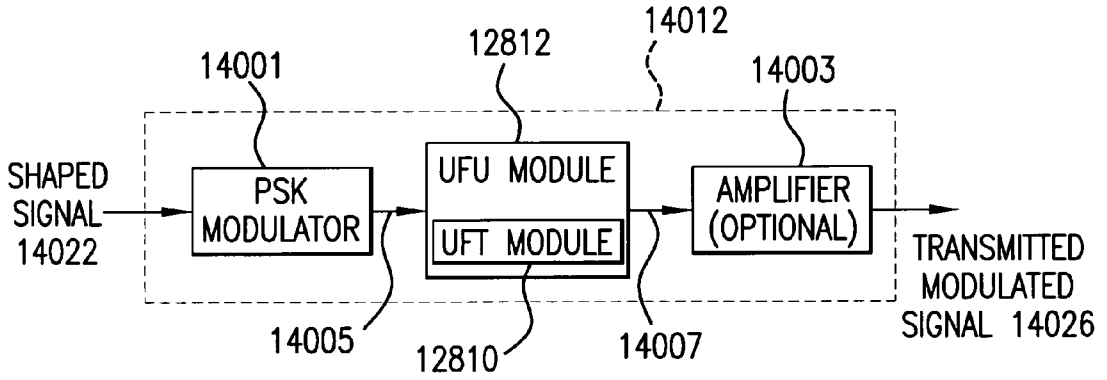


FIG.140D

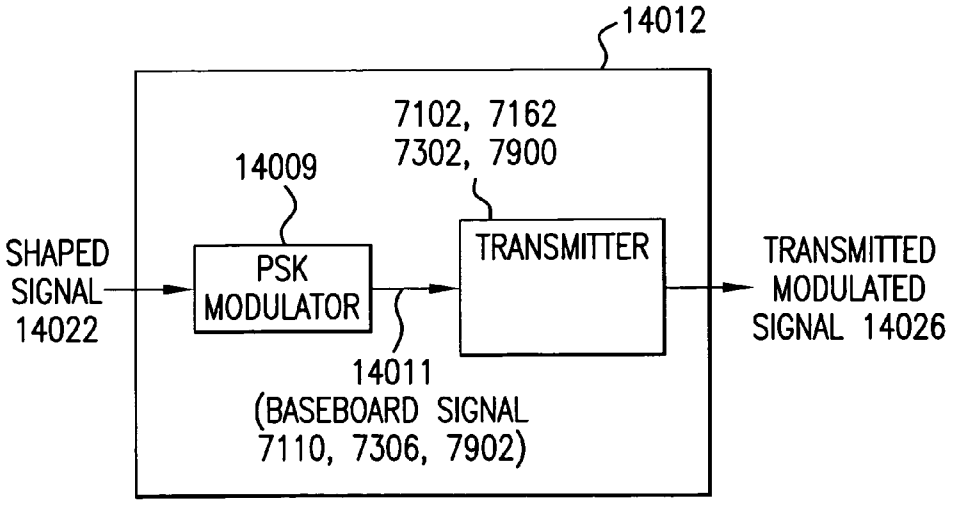


FIG.140E

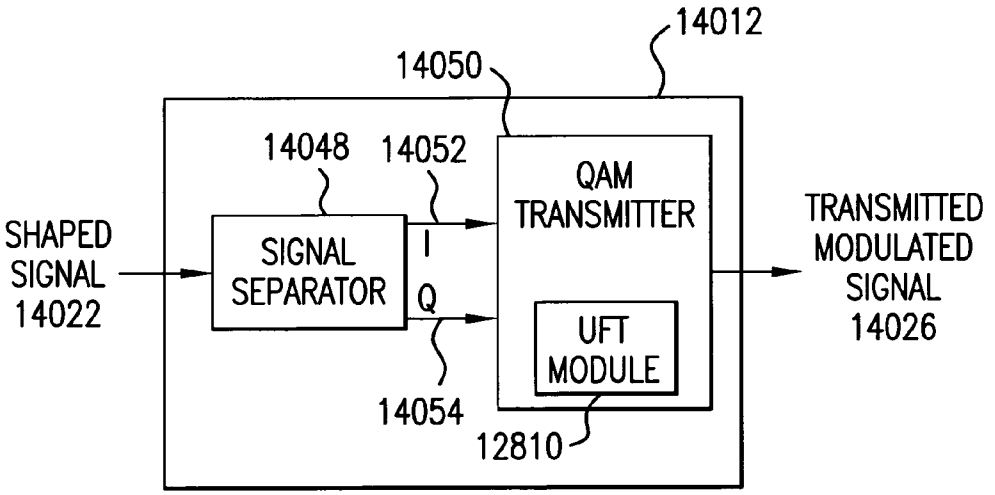

14012
14050
14048
14052
QAM
TRANSMITTER
SHAPED
SIGNAL
14022
SIGNAL
SEPARATOR
I
Q
UFT
MODULE
TRANSMITTED
MODULATED
SIGNAL
14026
14054
12810

FIG. 140F

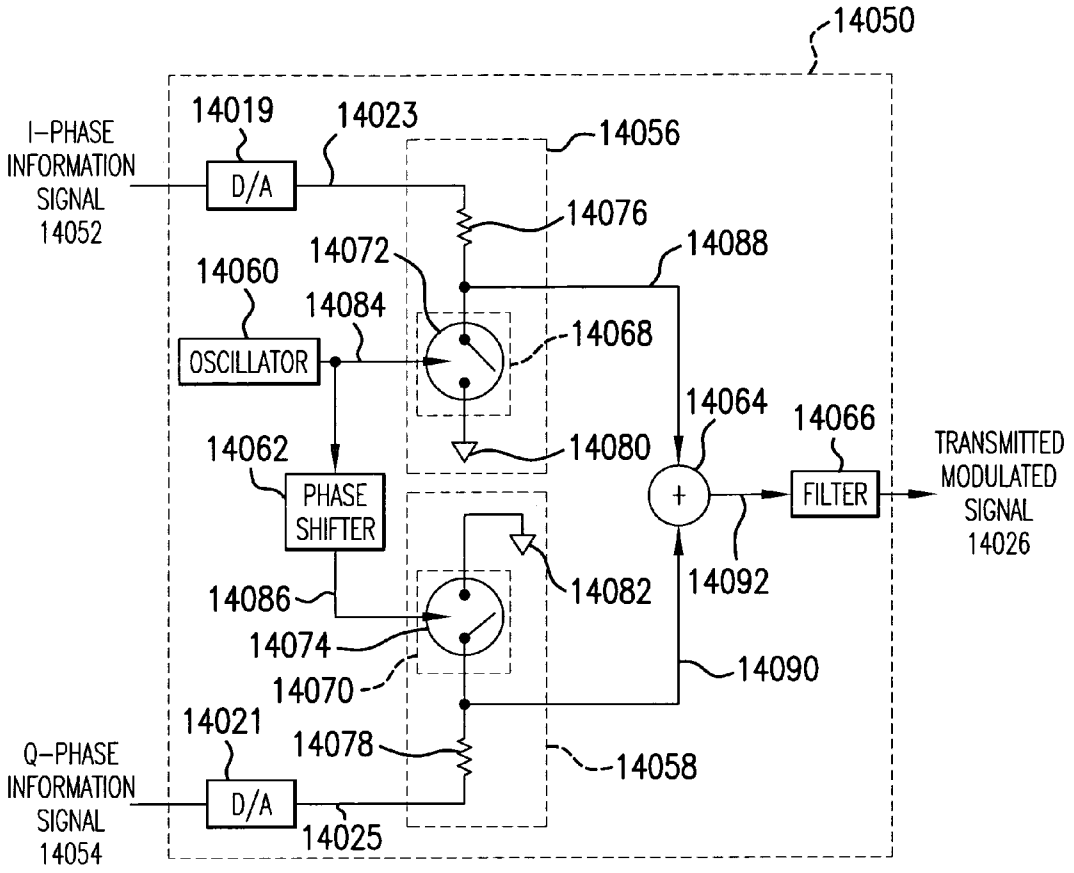


FIG. 140G

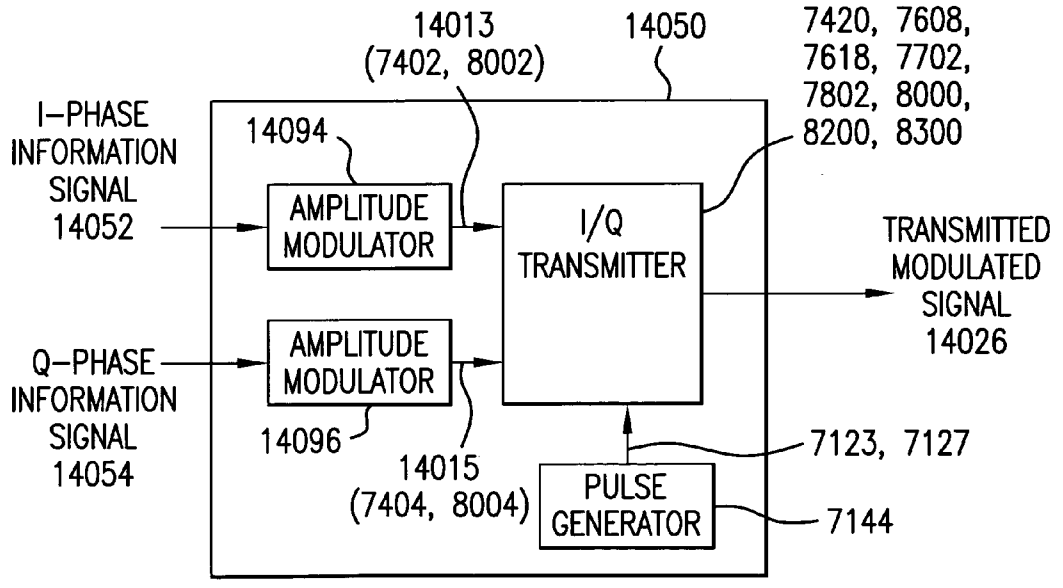


FIG. 140H

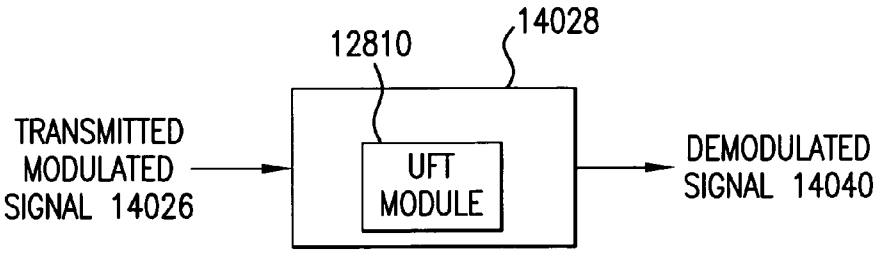


FIG.140I

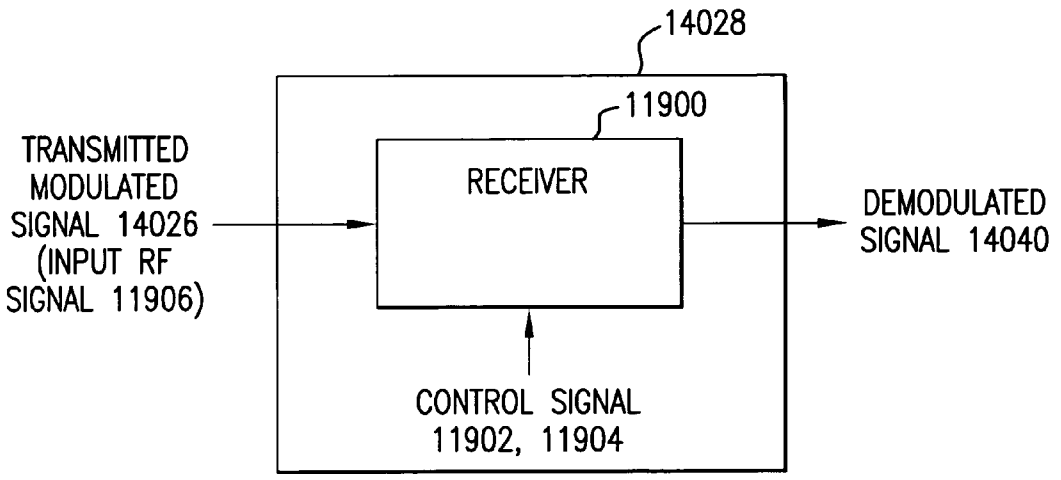


FIG.140J

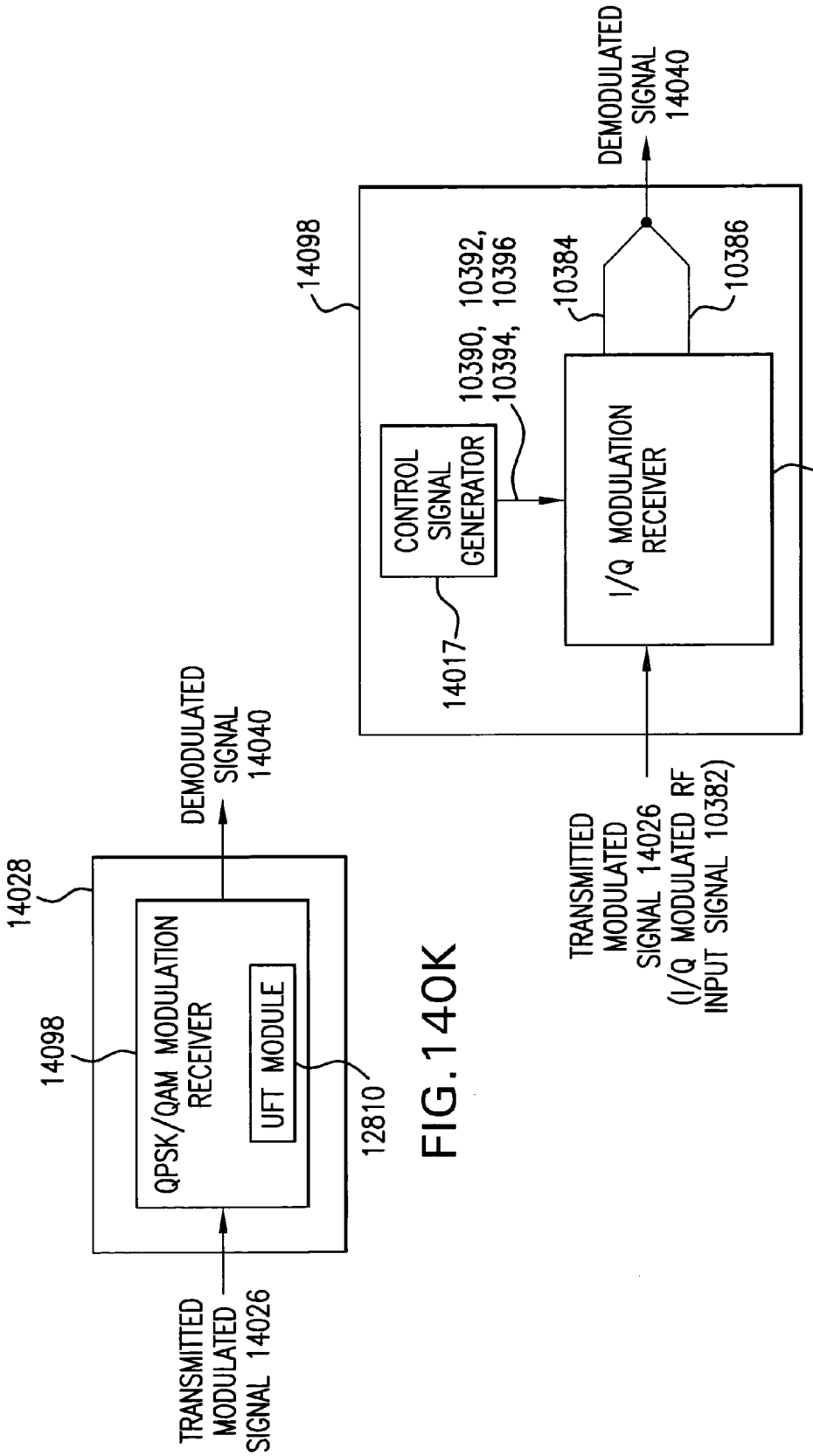


FIG. 140K

FIG. 140L

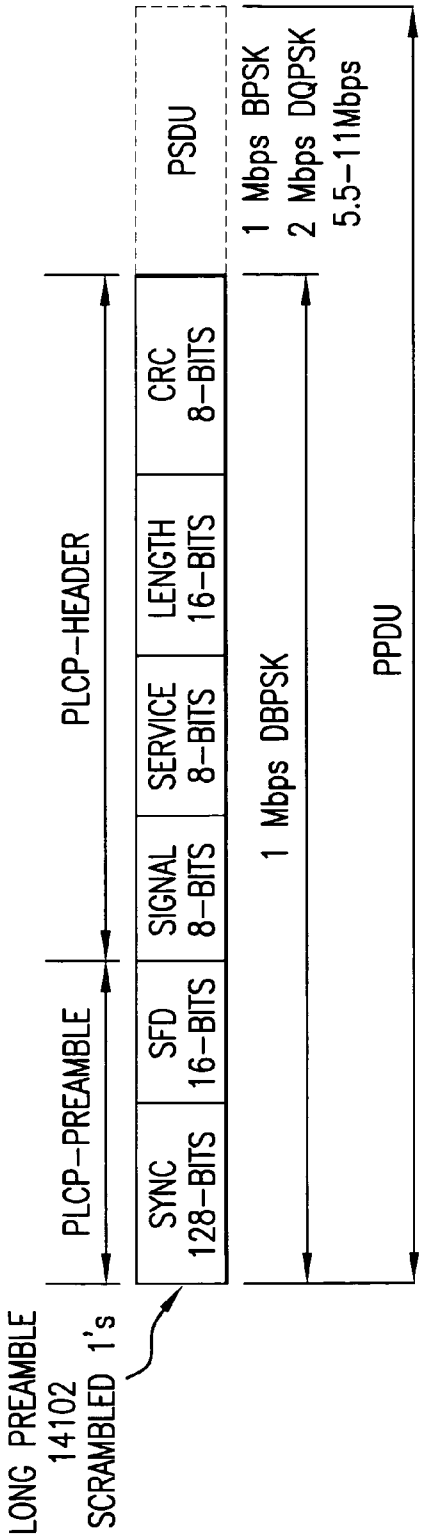


FIG.141A

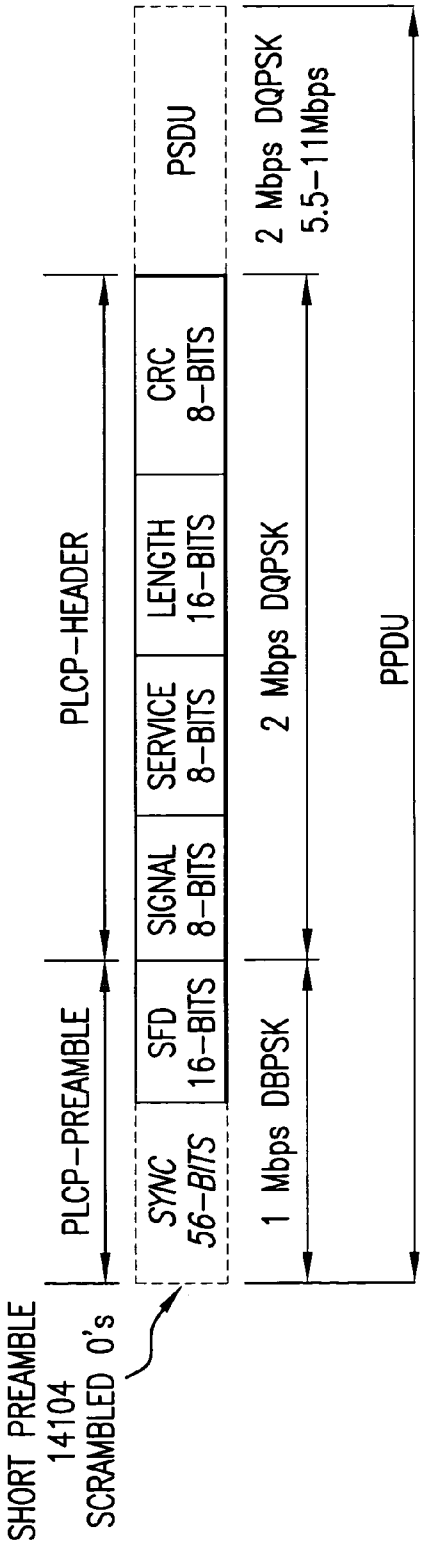


FIG.141B

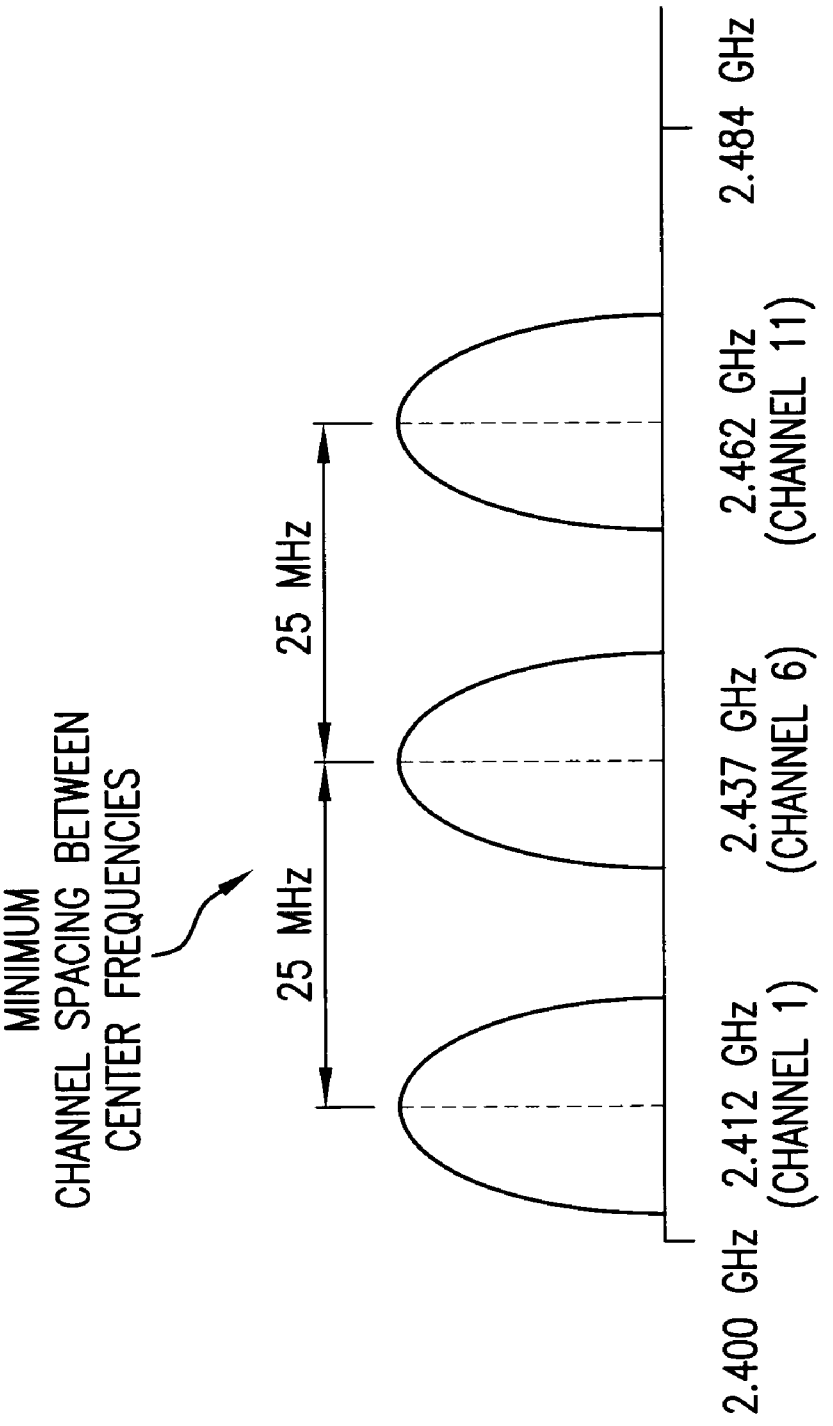

MINIMUM
CHANNEL SPACING BETWEEN
CENTER FREQUENCIES
25 MHz
25 MHz
2.400 GHz
2.412 GHz
(CHANNEL 1)
2.437 GHz
(CHANNEL 6)
2.462 GHz
(CHANNEL 11)
2.484 GHz

FIG.142

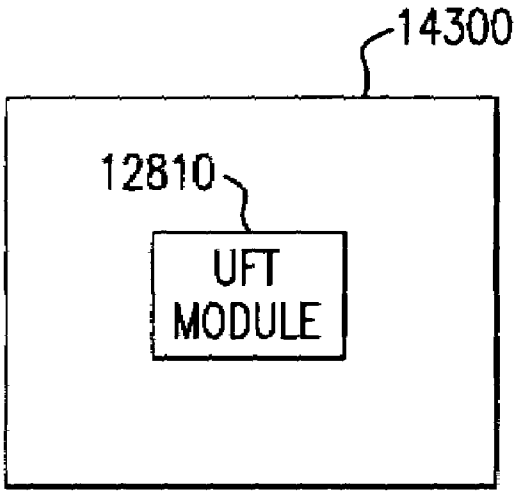


FIG. 143A

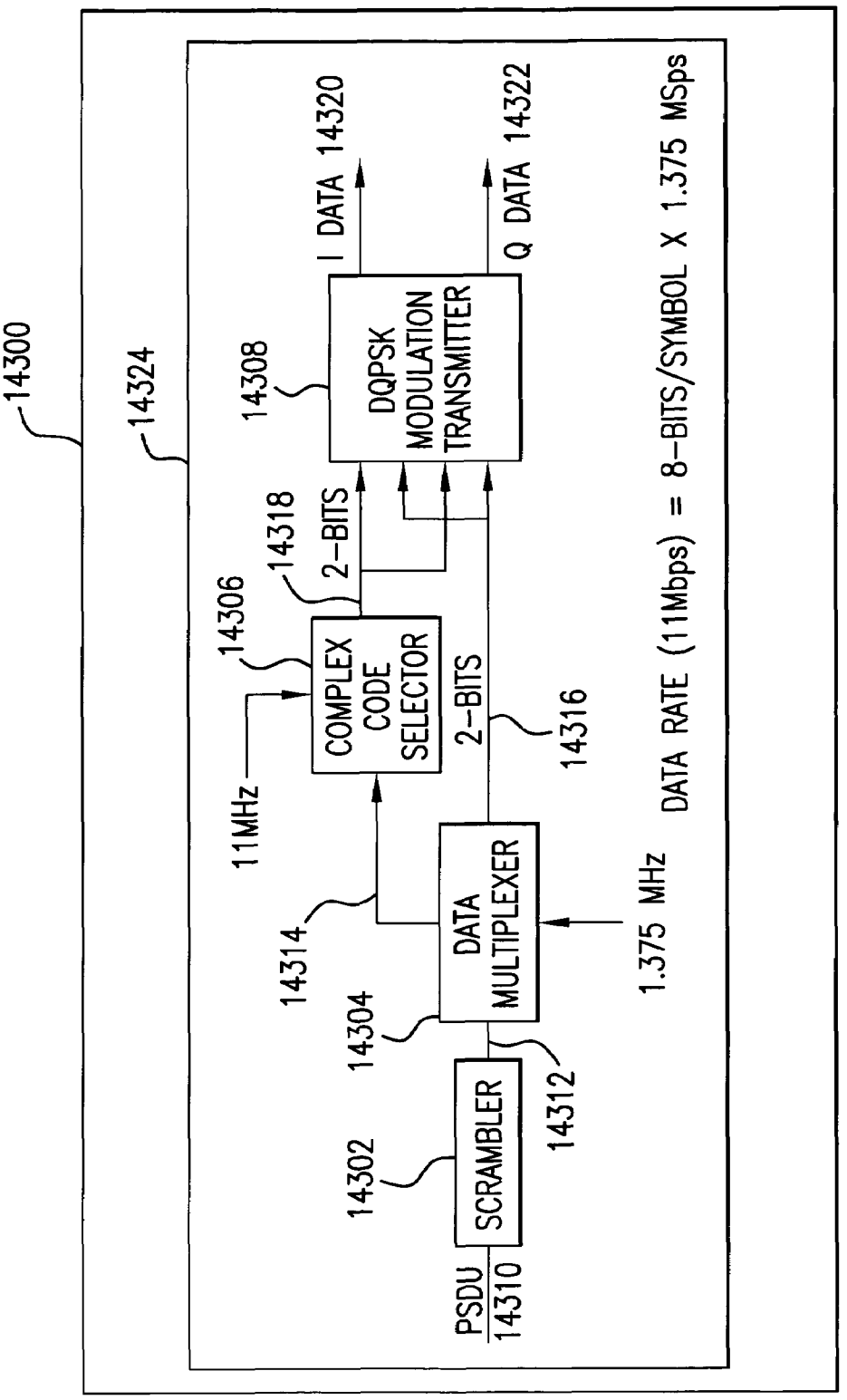

14300
14324
14308
DQPSK MODULATION TRANSMITTER
I DATA 14320
Q DATA 14322
14318
2-BITS
14306
COMPLEX CODE SELECTOR
11MHz
14314
2-BITS
14316
DATA MULTIPLEXER
1.375 MHz
DATA RATE (11Mbps) = 8-BITS/SYMBOL X 1.375 MSps
14304
14312
14302
SCRAMBLER
PSDU 14310

FIG.143B

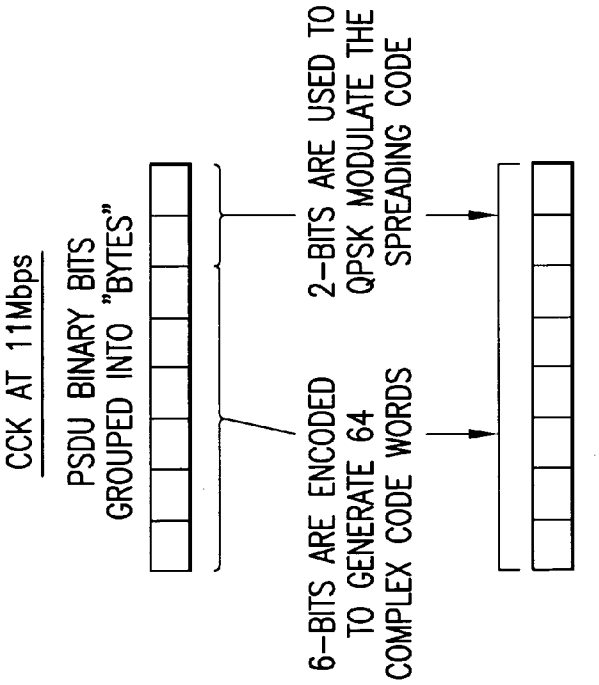


FIG.144B

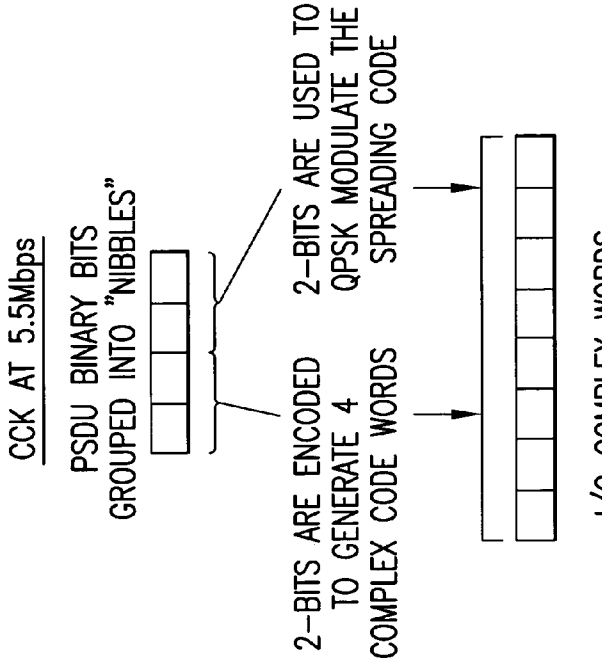


FIG.144A

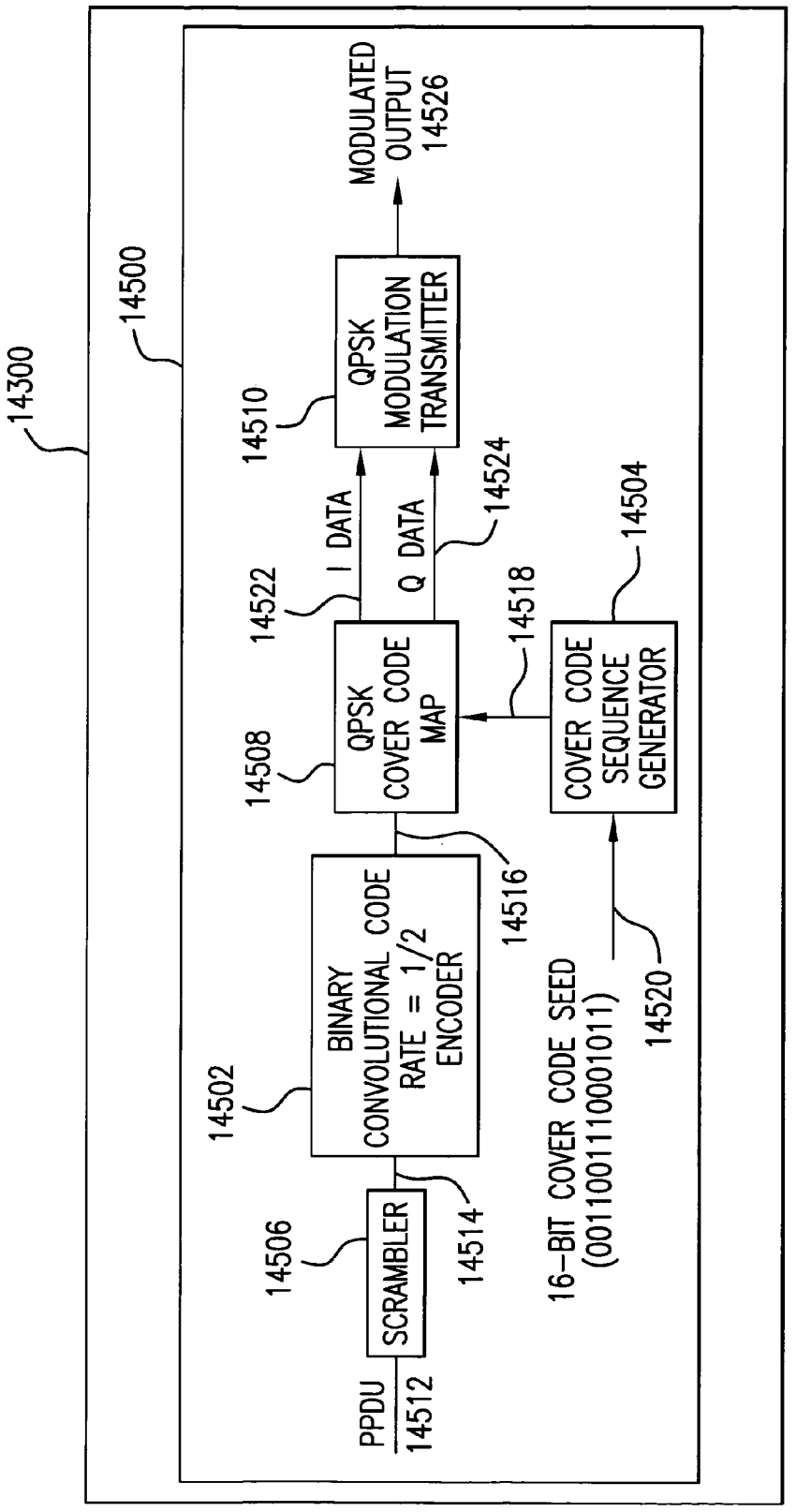

14300
14500
MODULATED OUTPUT 14526
QPSK MODULATION TRANSMITTER
14510
I DATA
Q DATA
14524
14522
14504
14518
QPSK COVER CODE MAP
COVER CODE SEQUENCE GENERATOR
14508
BINARY CONVOLUTIONAL CODE RATE = 1/2 ENCODER
14516
14502
SCRAMBLER
14506
14514
PPDU
14512
16-BIT COVER CODE SEED (0011001110001011)
14520

FIG.145A

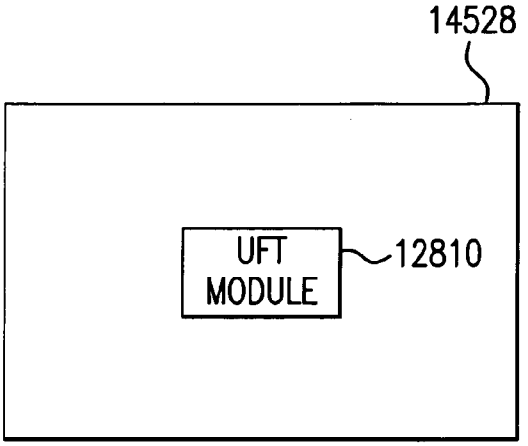


FIG.145B

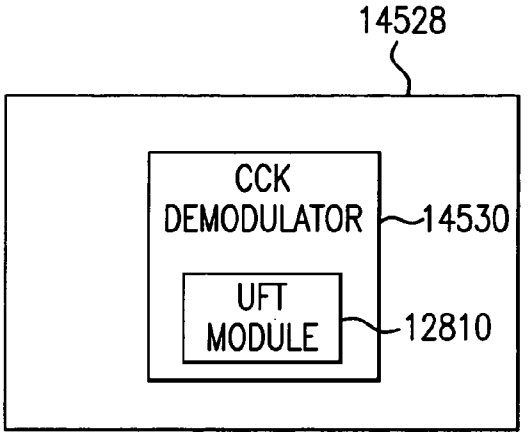


FIG.145C

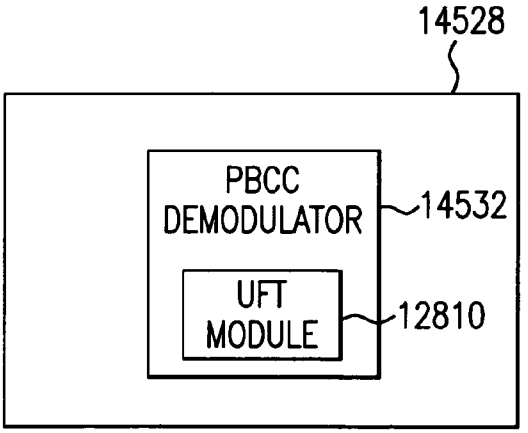


FIG.145D

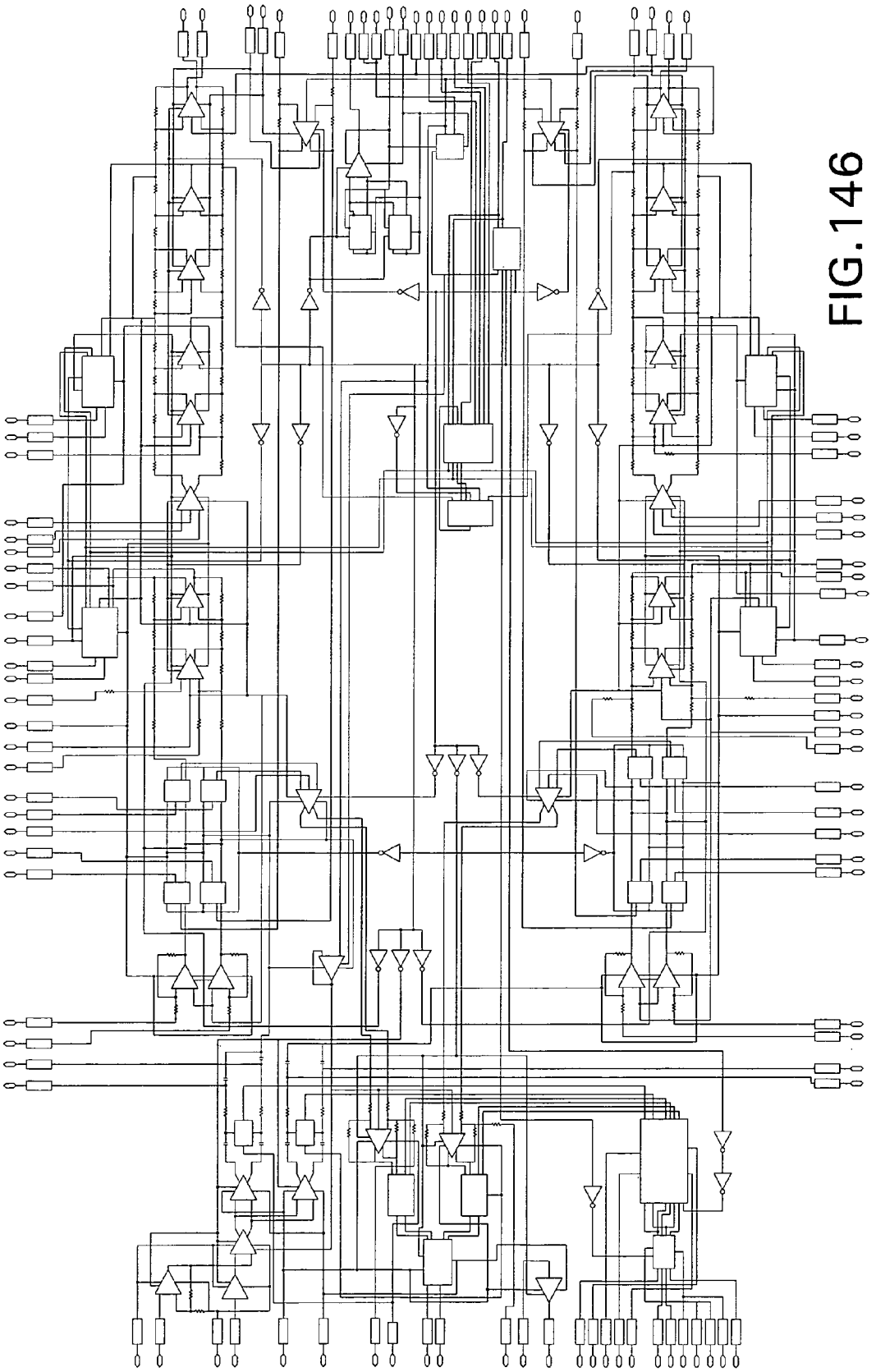


FIG. 146

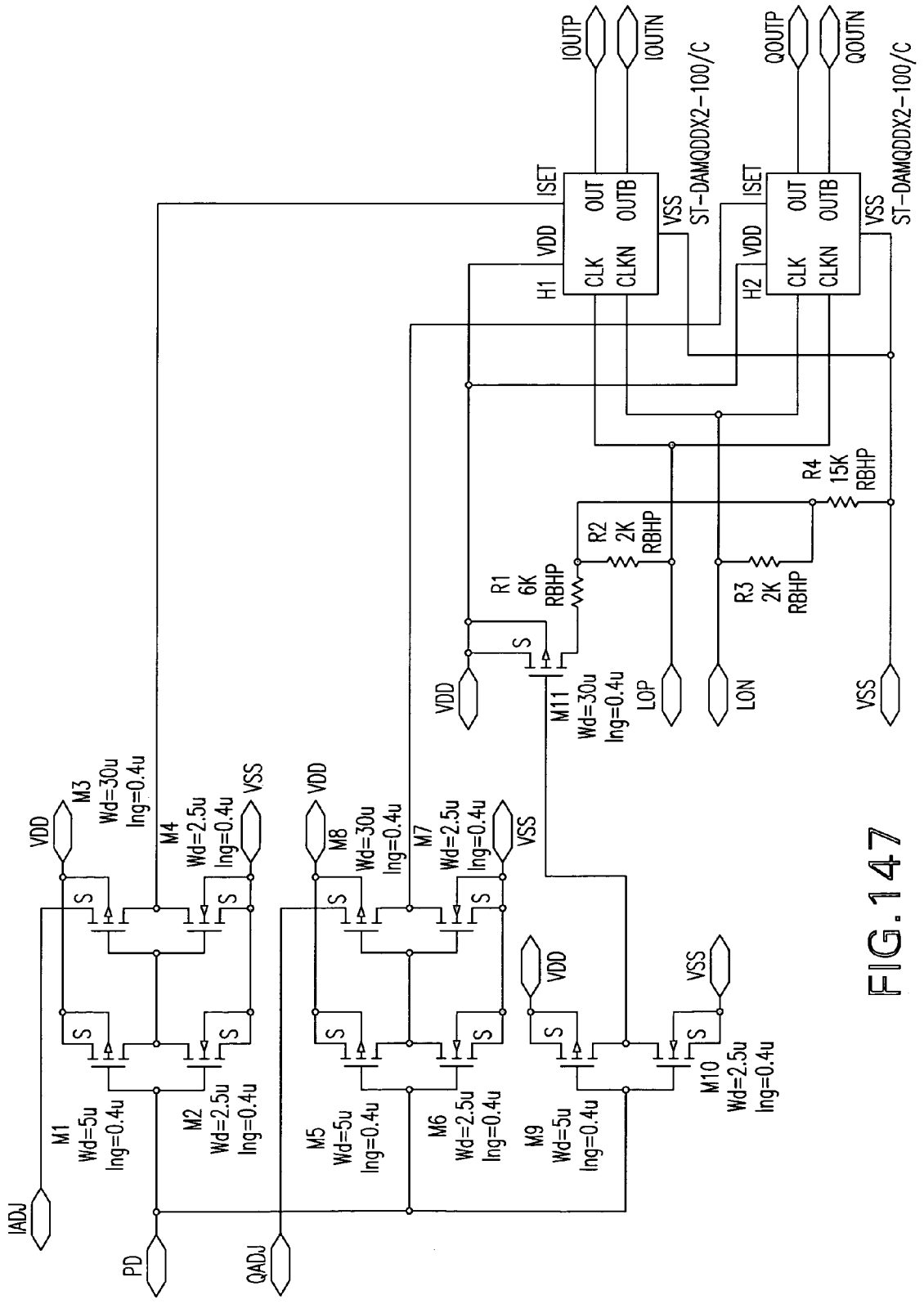

IOUTP
IOUTN
QOUTP
QOUTN
ISET
OUT
OUTB
VDD
CLK
CLKN
VSS
H1
H2
ST-DAMQDDX2-100/C
R1 6K RBHP
R2 2K RBHP
R3 2K RBHP
R4 15K RBHP
M11 Wd=30u lng=0.4u
LOP
LON
M1 Wd=5u lng=0.4u
M2 Wd=2.5u lng=0.4u
M3 Wd=30u lng=0.4u
M4 Wd=2.5u lng=0.4u
M5 Wd=5u lng=0.4u
M6 Wd=2.5u lng=0.4u
M7 Wd=2.5u lng=0.4u
M8 Wd=30u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
IADJ
QADJ
PD
S

FIG. 147

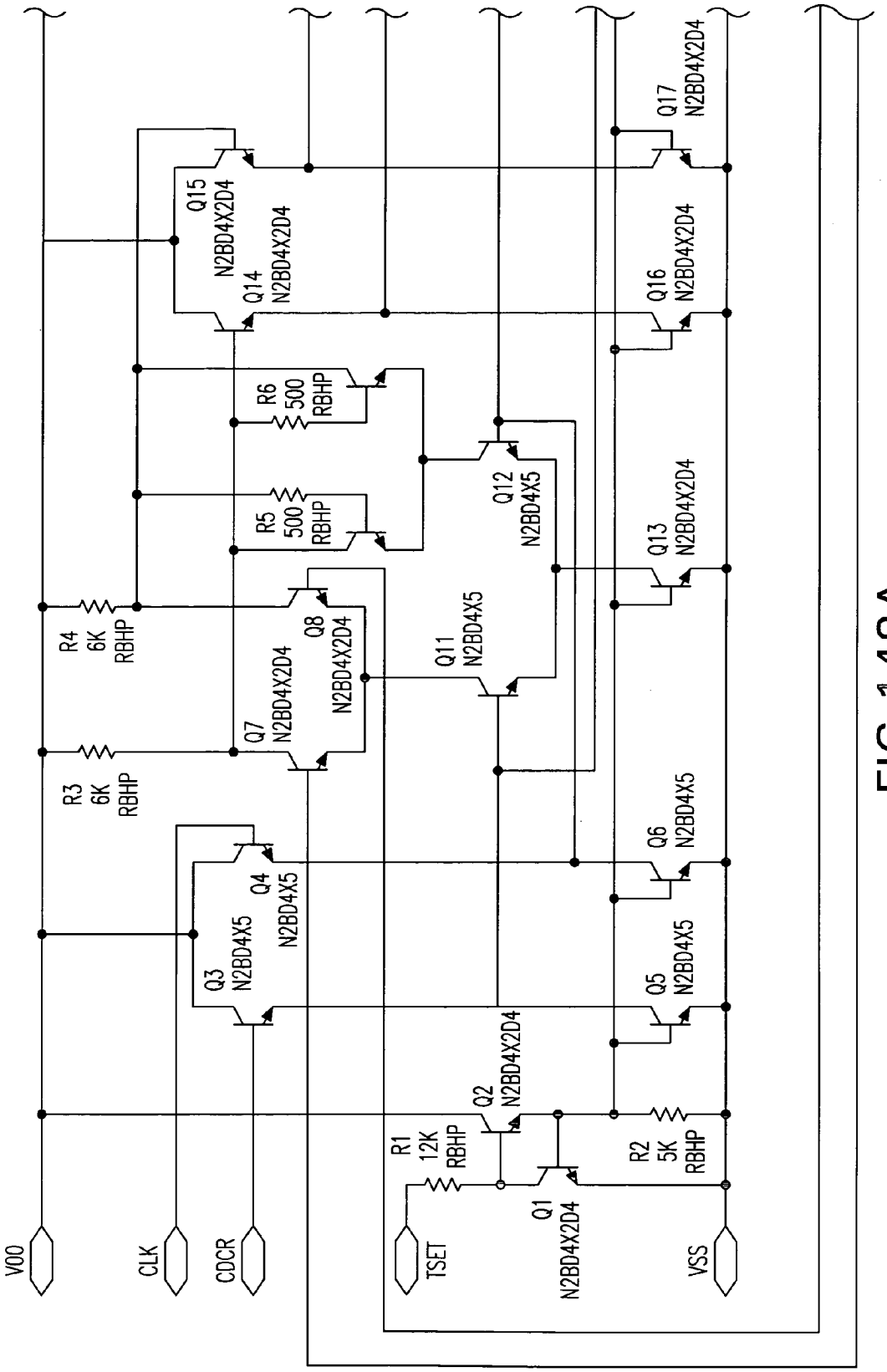

VDD
CLK
CDCR
TSET
VSS
R1 12K RBHP
R2 5K RBHP
R3 6K RBHP
R4 6K RBHP
R5 500 RBHP
R6 500 RBHP
Q1 N2BD4X2D4
Q2 N2BD4X2D4
Q3 N2BD4X5
Q4 N2BD4X5
Q5 N2BD4X5
Q6 N2BD4X5
Q7 N2BD4X2D4
Q8 N2BD4X2D4
Q11 N2BD4X5
Q12 N2BD4X5
Q13 N2BD4X2D4
Q14 N2BD4X2D4
Q15 N2BD4X2D4
Q16 N2BD4X2D4
Q17 N2BD4X2D4

FIG. 148A

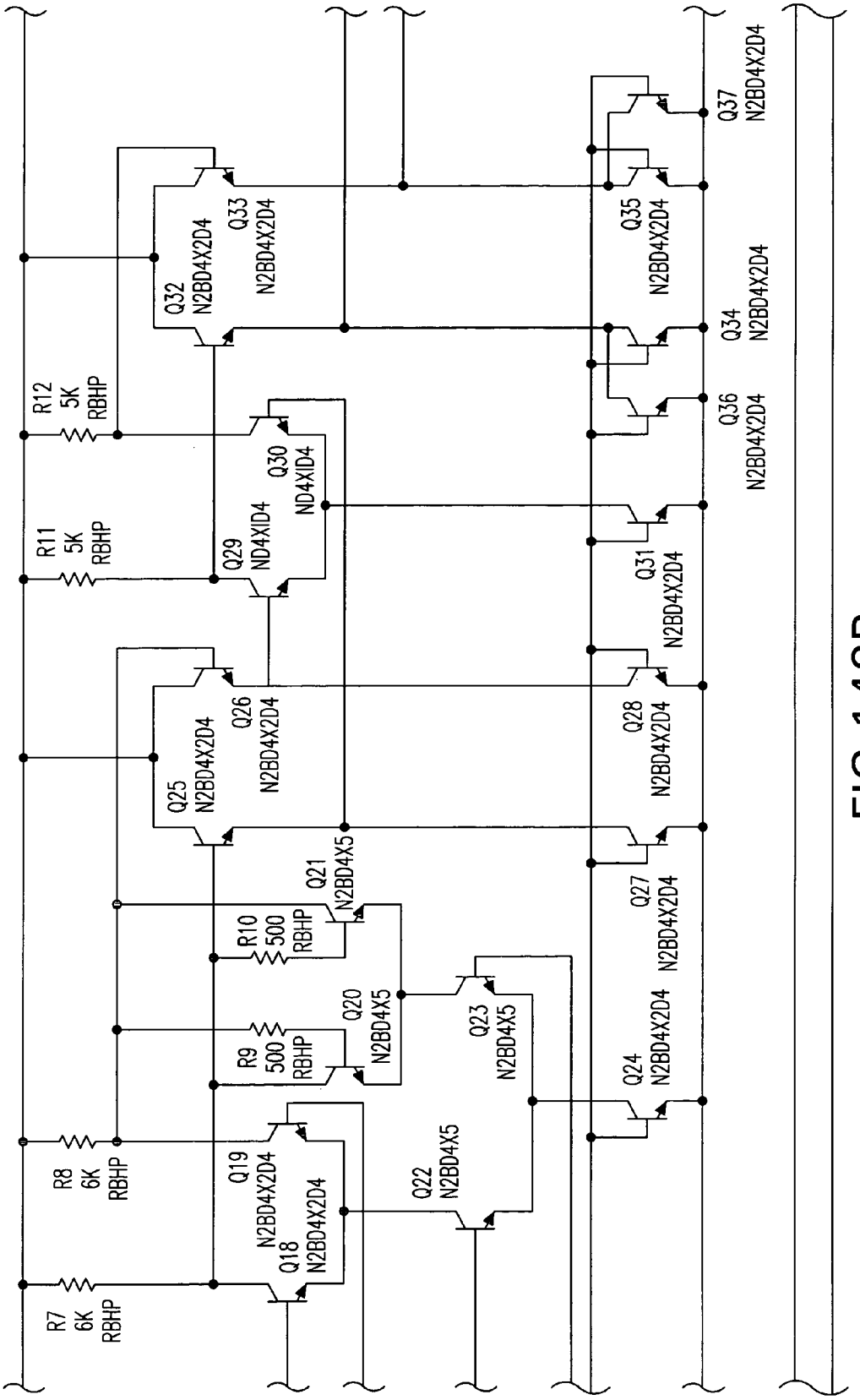

R7 6K RBHP
R8 6K RBHP
R9 500 RBHP
R10 500 RBHP
R11 5K RBHP
R12 5K RBHP
Q18 N2BD4X2D4
Q19 N2BD4X2D4
Q20 N2BD4X5
Q21 N2BD4X5
Q22 N2BD4X5
Q23 N2BD4X5
Q24 N2BD4X2D4
Q25 N2BD4X2D4
Q26 N2BD4X2D4
Q27 N2BD4X2D4
Q28 N2BD4X2D4
Q29 ND4XID4
Q30 ND4XID4
Q31 N2BD4X2D4
Q32 N2BD4X2D4
Q33 N2BD4X2D4
Q34 N2BD4X2D4
Q35 N2BD4X2D4
Q36 N2BD4X2D4
Q37 N2BD4X2D4

FIG.148B

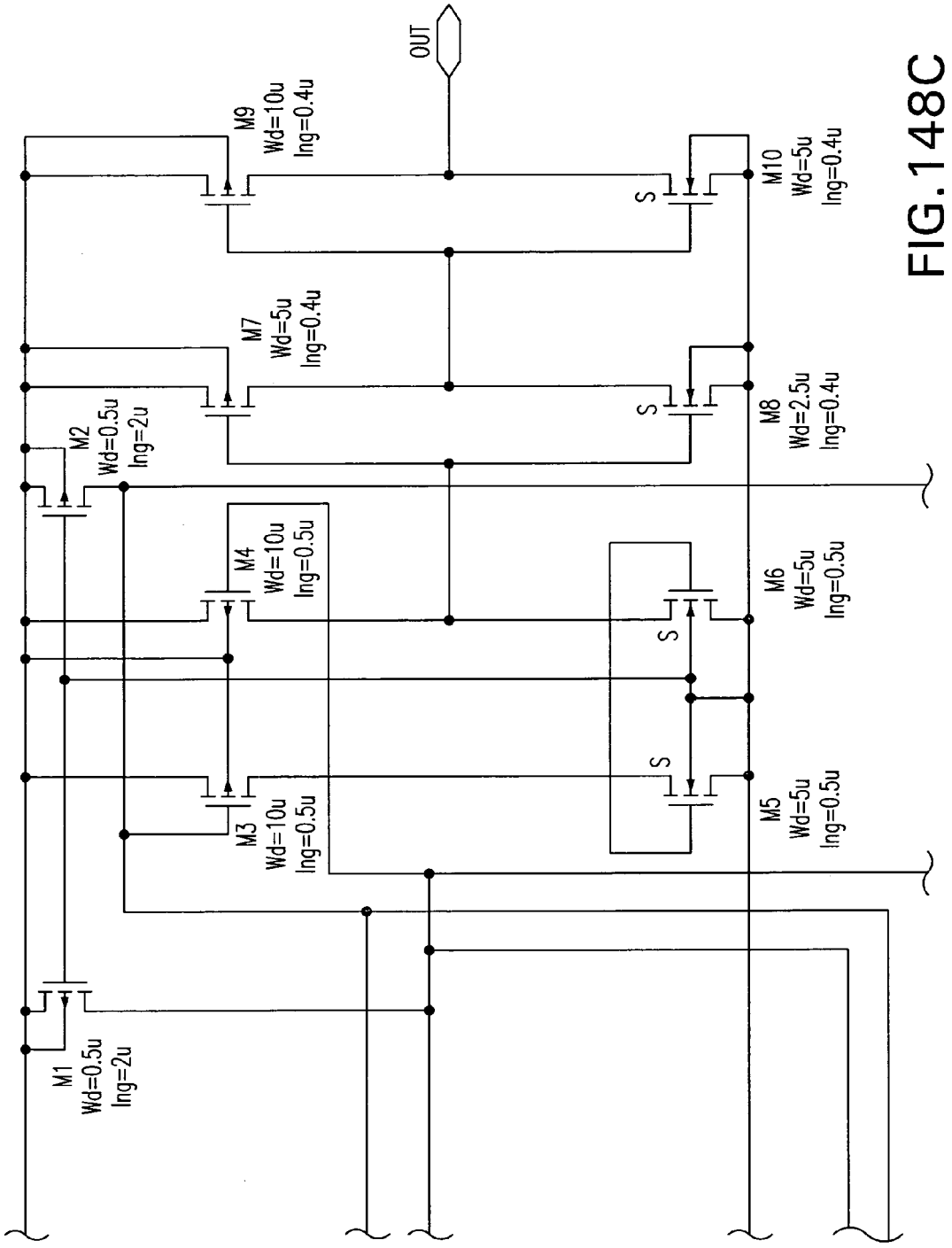

OUT
M9
Wd=10u
lng=0.4u
M10
Wd=5u
lng=0.4u
M7
Wd=5u
lng=0.4u
M8
Wd=2.5u
lng=0.4u
M2
Wd=0.5u
lng=2u
M4
Wd=10u
lng=0.5u
M6
Wd=5u
lng=0.5u
M3
Wd=10u
lng=0.5u
M5
Wd=5u
lng=0.5u
M1
Wd=0.5u
lng=2u
S

FIG. 148C

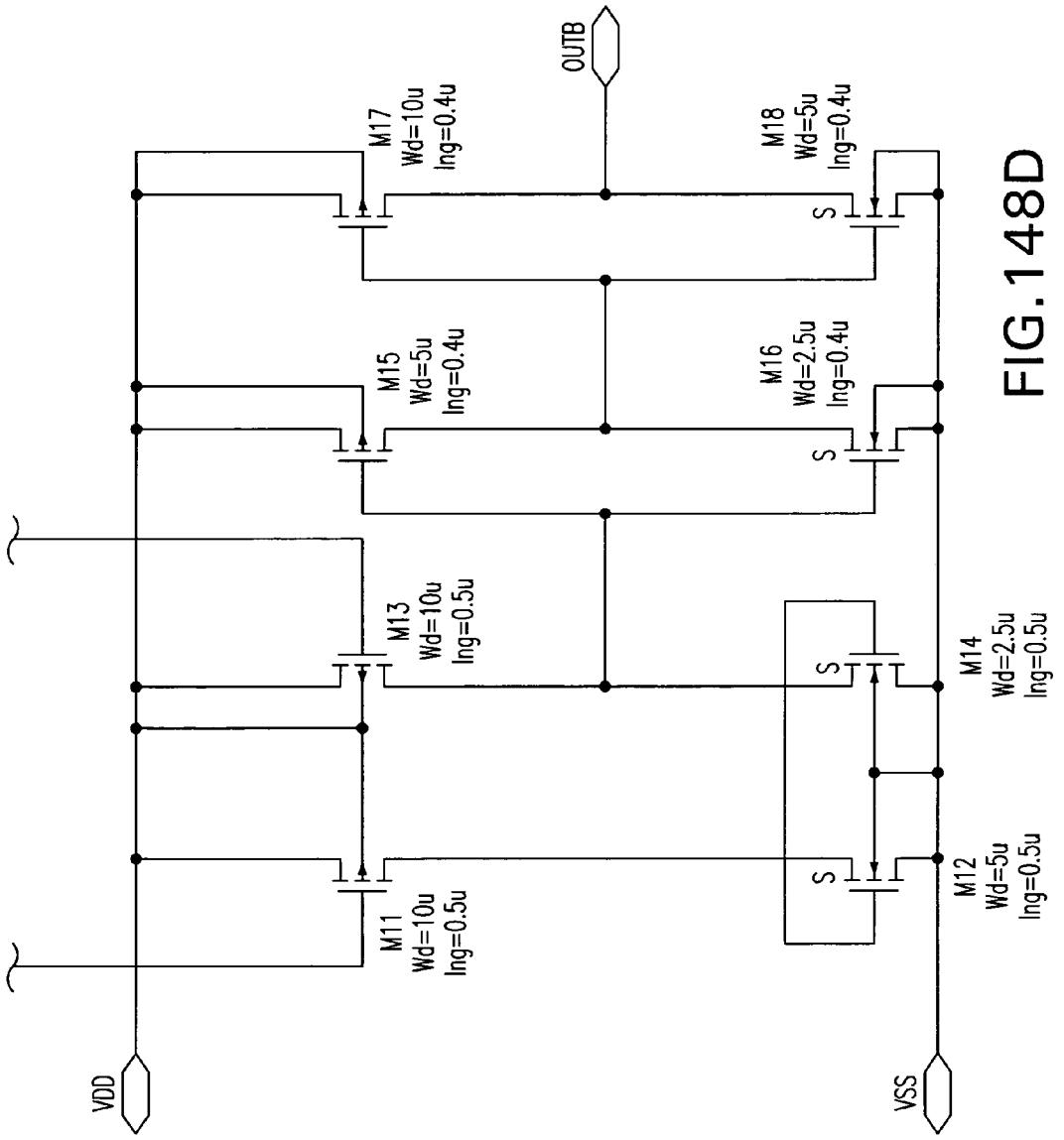

OUTB
M17
Wd=10u
lng=0.4u
M18
Wd=5u
lng=0.4u
M15
Wd=5u
lng=0.4u
M16
Wd=2.5u
lng=0.4u
M13
Wd=10u
lng=0.5u
M14
Wd=2.5u
lng=0.5u
M11
Wd=10u
lng=0.5u
M12
Wd=5u
lng=0.5u
VDD
VSS

FIG. 148D

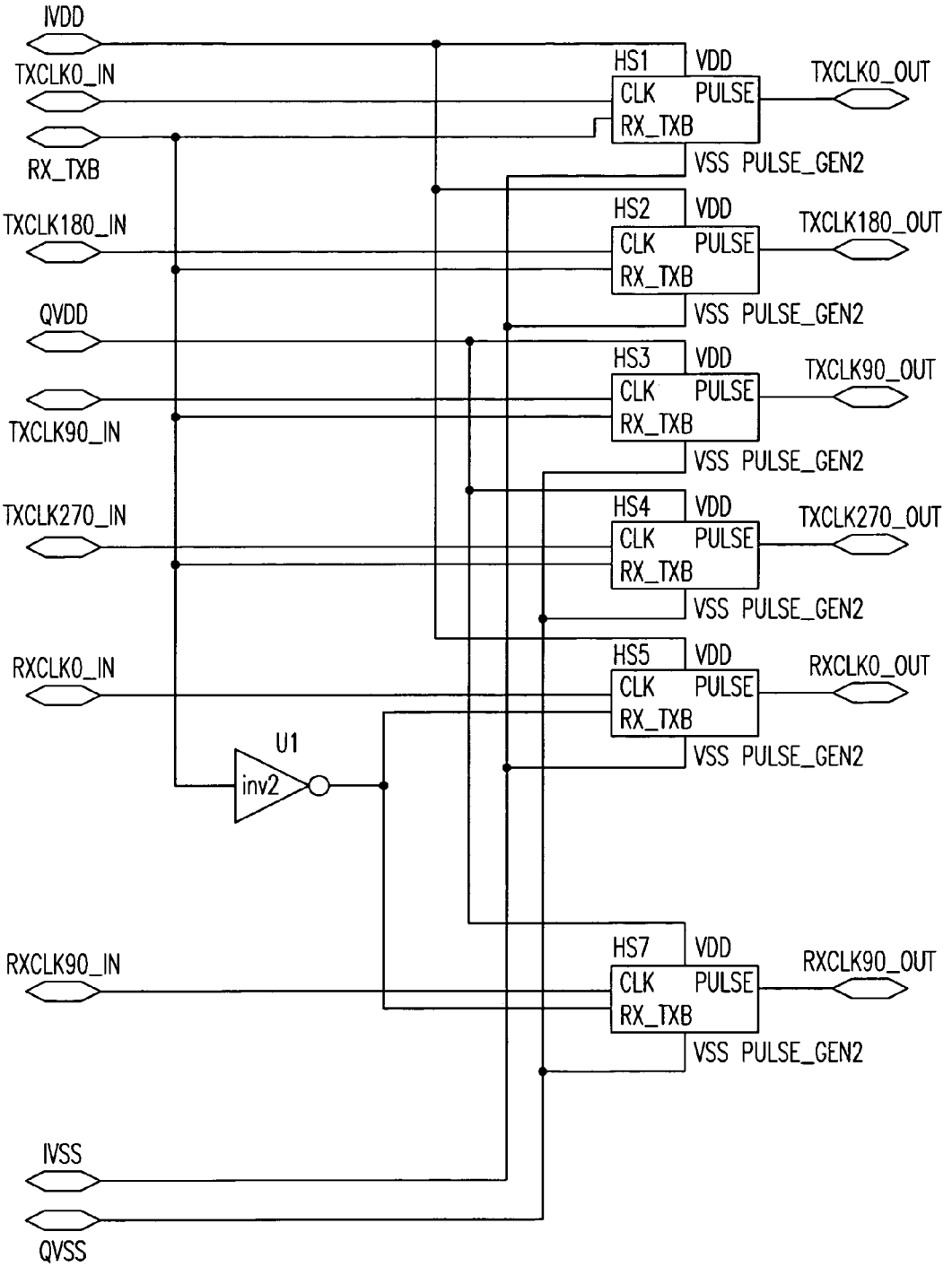

IVDD
TXCLK0_IN
RX_TXB
TXCLK180_IN
QVDD
TXCLK90_IN
TXCLK270_IN
RXCLK0_IN
RXCLK90_IN
IVSS
QVSS
U1
inv2
HS1
HS2
HS3
HS4
HS5
HS7
VDD
CLK
PULSE
RX_TXB
VSS PULSE_GEN2
TXCLK0_OUT
TXCLK180_OUT
TXCLK90_OUT
TXCLK270_OUT
RXCLK0_OUT
RXCLK90_OUT

FIG.149

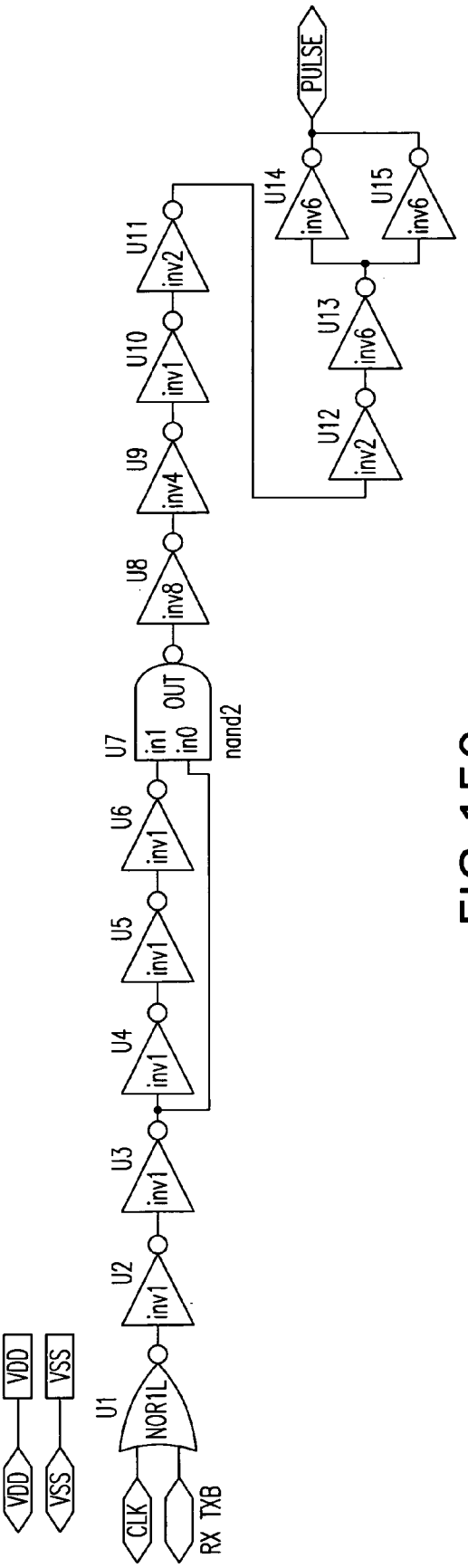

PULSE
U14
inv6
U15
inv6
U13
inv6
U12
inv2
U11
inv2
U10
inv1
U9
inv4
U8
inv8
U7
in1
in0
OUT
nand2
U6
inv1
U5
inv1
U4
inv1
U3
inv1
U2
inv1
U1
NOR1L
VDD
VSS
VDD
VSS
CLK
RX TXB

FIG. 150

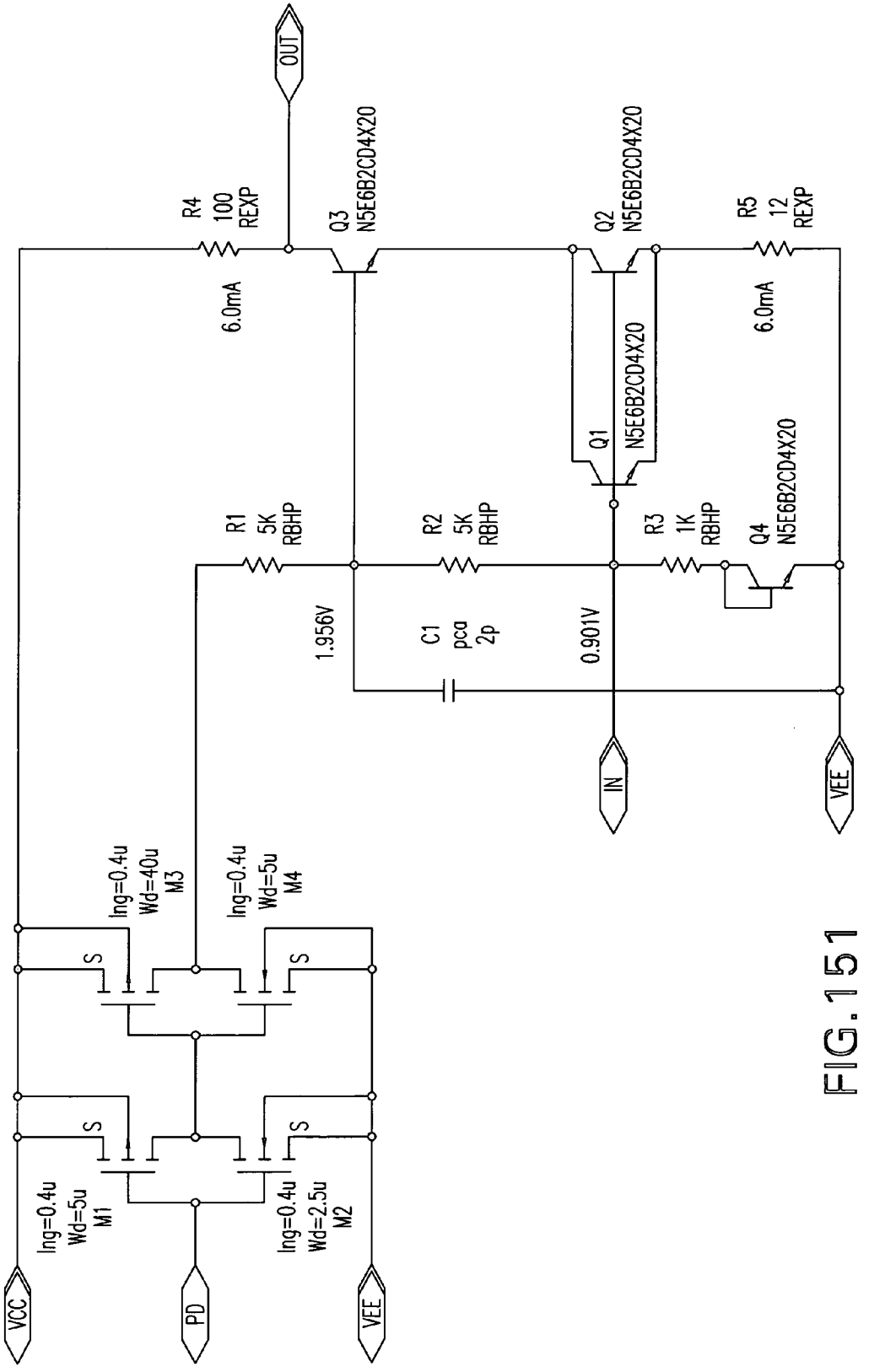

OUT
R4
100
REXP
Q3
N5E6B2CD4X20
Q2
N5E6B2CD4X20
R5
12
REXP
6.0mA
Q1
N5E6B2CD4X20
6.0mA
R1
5K
RBHP
R2
5K
RBHP
R3
1K
RBHP
Q4
N5E6B2CD4X20
1.956V
C1
pca
2p
0.901V
IN
VEE
lng=0.4u
Wd=40u
M3
lng=0.4u
Wd=5u
M4
S
S
S
S
lng=0.4u
Wd=5u
M1
lng=0.4u
Wd=2.5u
M2
VCC
PD
VEE

FIG. 151

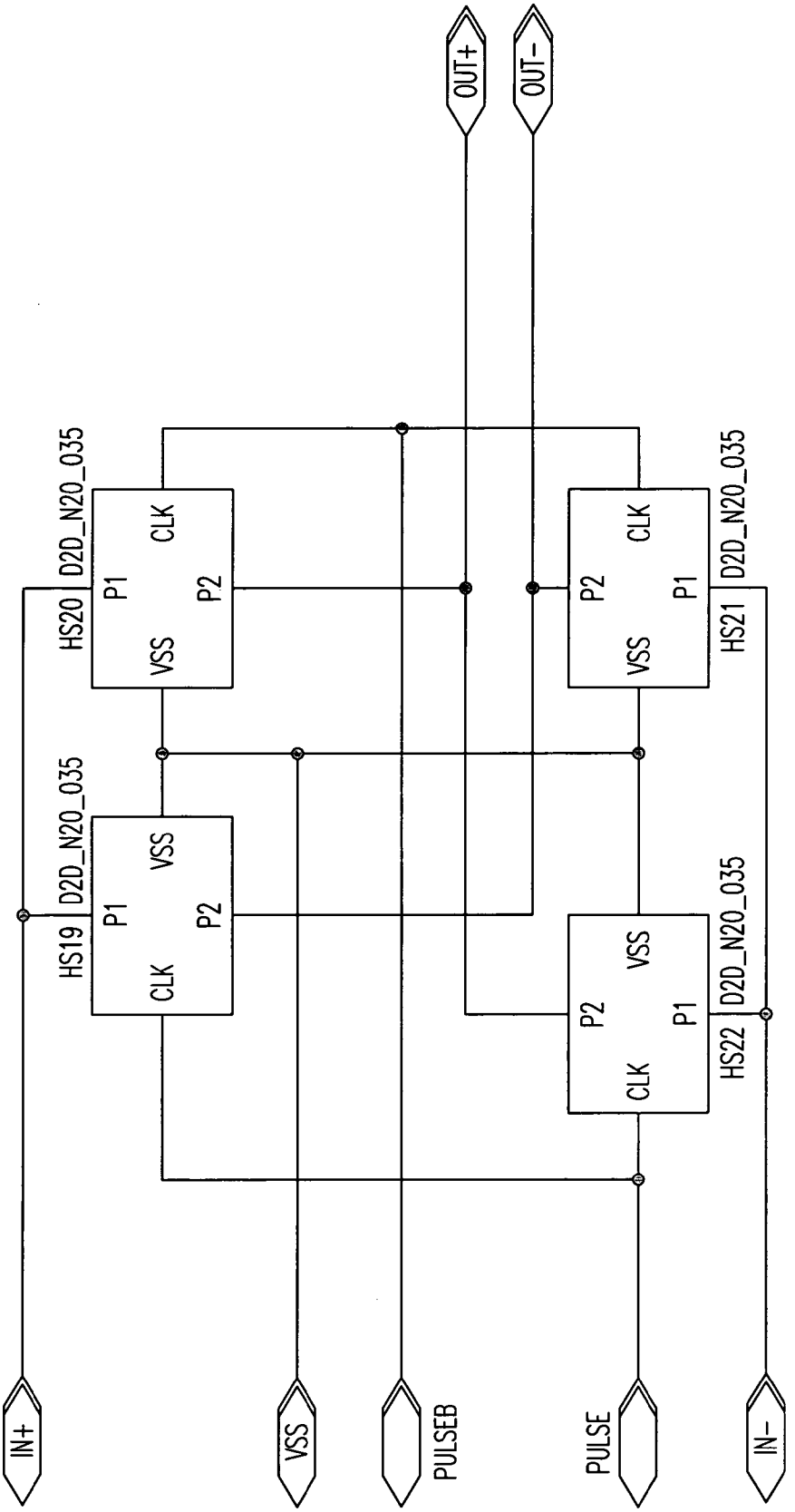

OUT+
OUT-
D2D_N20_035
HS20
P1
CLK
P2
VSS
D2D_N20_035
HS21
P2
CLK
P1
VSS
D2D_N20_035
HS19
P1
VSS
P2
CLK
D2D_N20_035
HS22
P2
VSS
P1
CLK
IN+
VSS
PULSEB
PULSE
IN-

FIG. 152

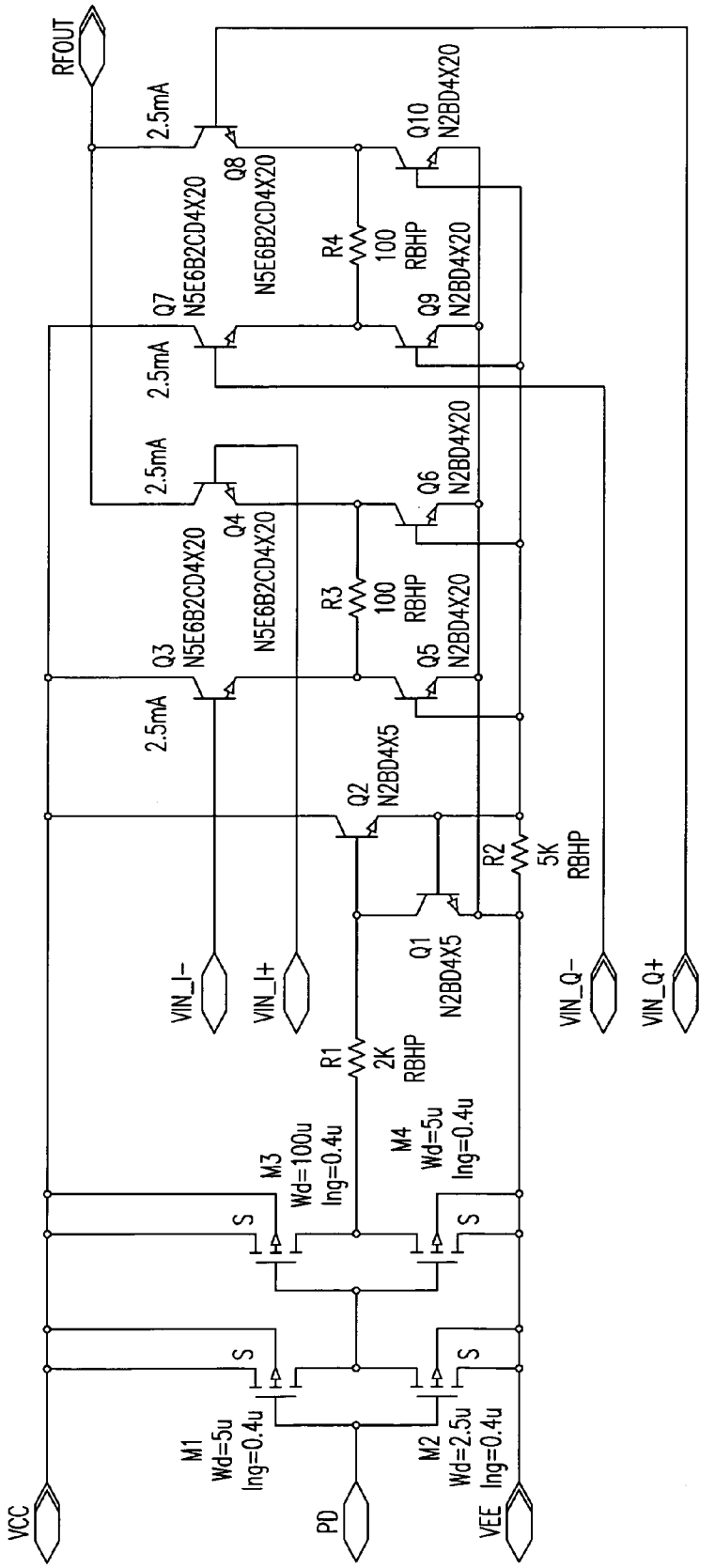

RFOUT
2.5mA
Q8
N5E6B2CD4X20
Q10
N2BD4X20
R4
100
RBHP
Q7
N5E6B2CD4X20
Q9
N2BD4X20
2.5mA
2.5mA
Q6
N2BD4X20
Q4
N5E6B2CD4X20
R3
100
RBHP
Q3
N5E6B2CD4X20
Q5
N2BD4X20
2.5mA
Q2
N2BD4X5
R2
5K
RBHP
Q1
N2BD4X5
VIN_I-
VIN_I+
VIN_Q-
VIN_Q+
R1
2K
RBHP
M3
Wd=100u
lng=0.4u
M4
Wd=5u
lng=0.4u
S
S
S
S
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
VCC
PD
VEE

FIG. 153

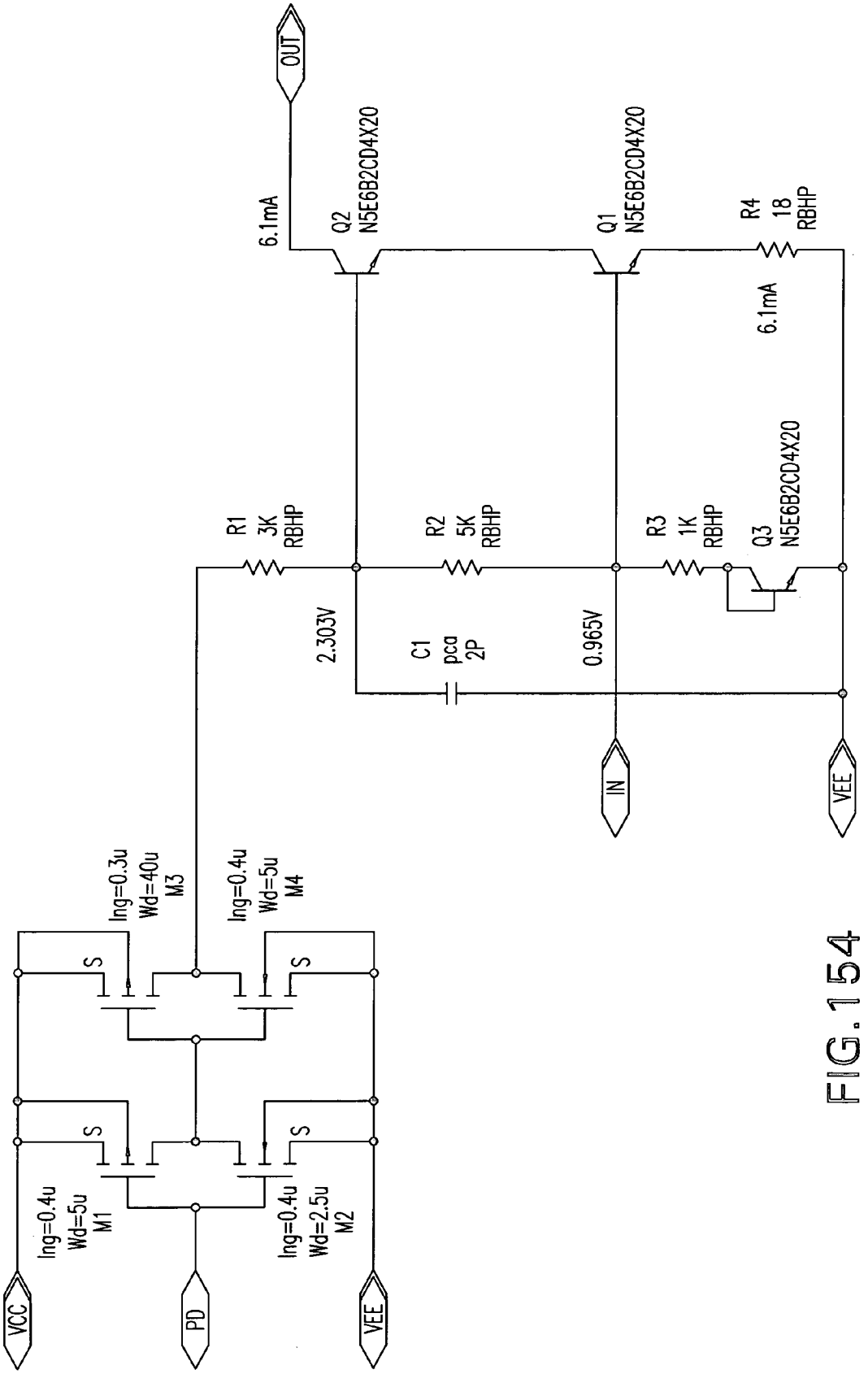

OUT
6.1mA
Q2
N5E6B2CD4X20
Q1
N5E6B2CD4X20
R4
18
RBHP
6.1mA
R1
3K
RBHP
R2
5K
RBHP
R3
1K
RBHP
Q3
N5E6B2CD4X20
2.303V
C1
pca
2P
0.965V
IN
VEE
lng=0.3u
Wd=40u
M3
lng=0.4u
Wd=5u
M4
S
S
S
S
lng=0.4u
Wd=5u
M1
lng=0.4u
Wd=2.5u
M2
VCC
PD
VEE

FIG. 154

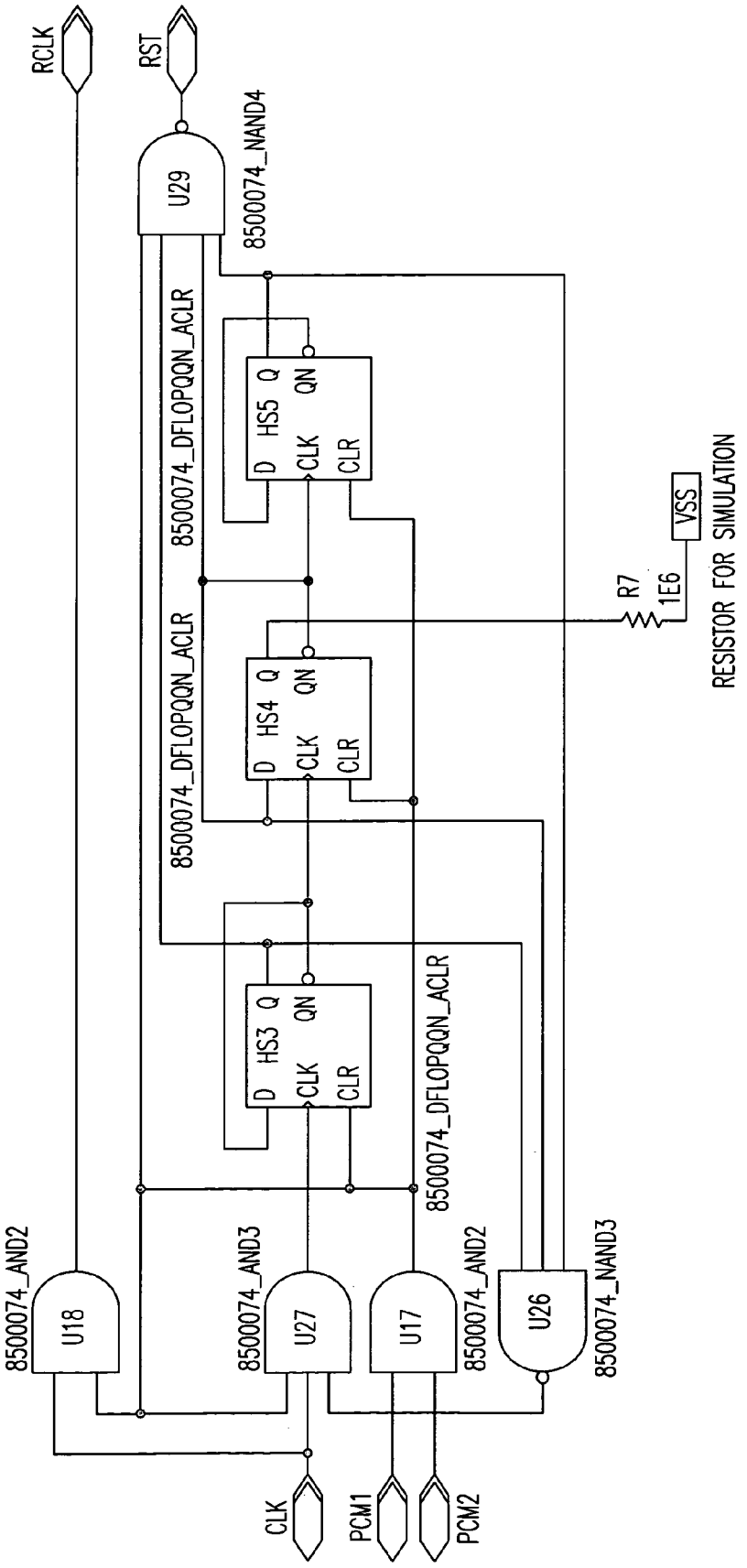

RCLK
RST
U29
8500074_NAND4
8500074_DFLOPQQN_ACLR
D HS5 Q
CLK QN
CLR
D HS4 Q
CLK QN
CLR
D HS3 Q
CLK QN
CLR
R7
1E6
VSS
RESISTOR FOR SIMULATION
8500074_AND2
U18
8500074_AND3
U27
U17
8500074_AND2
U26
8500074_NAND3
CLK
PCM1
PCM2

FIG. 155

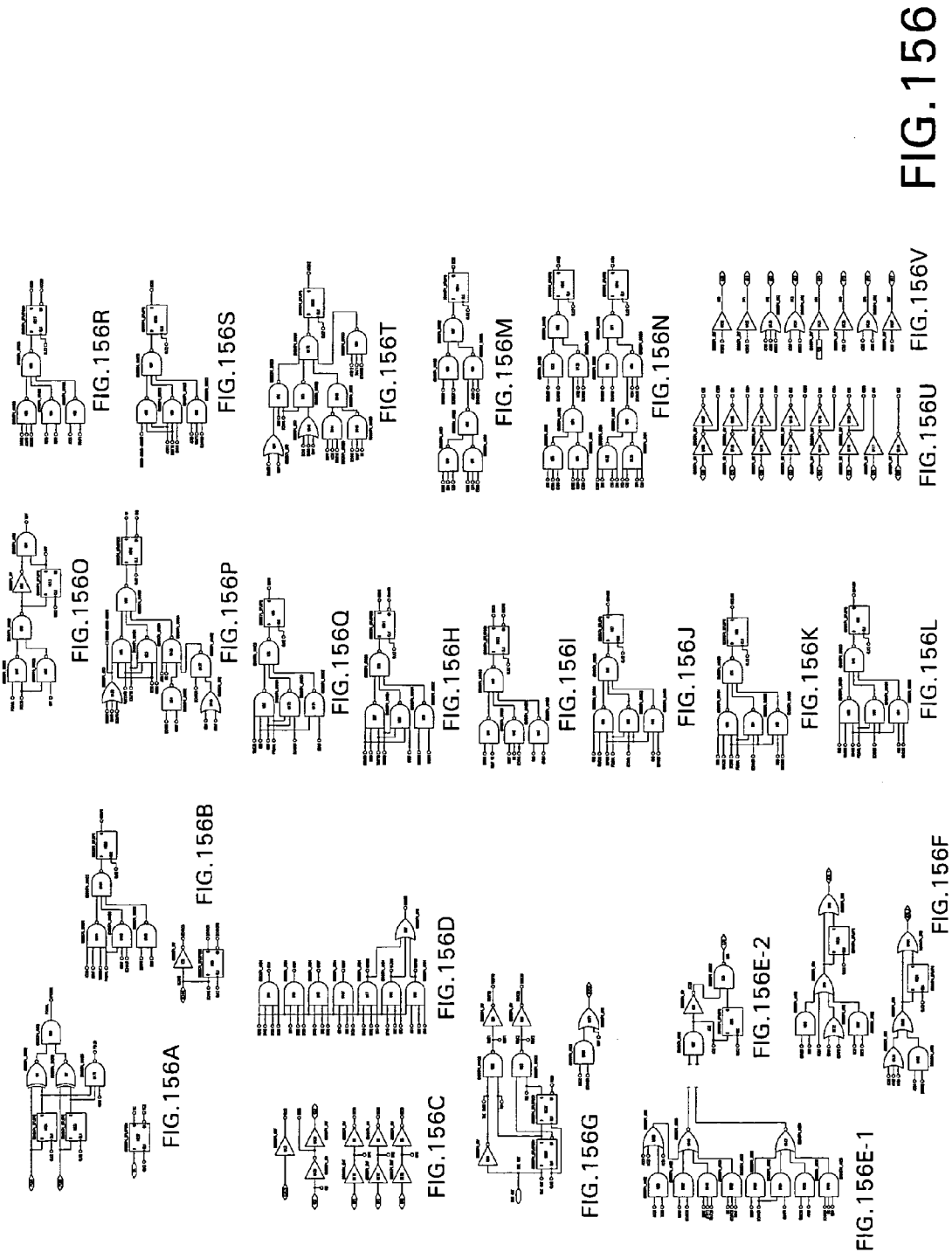
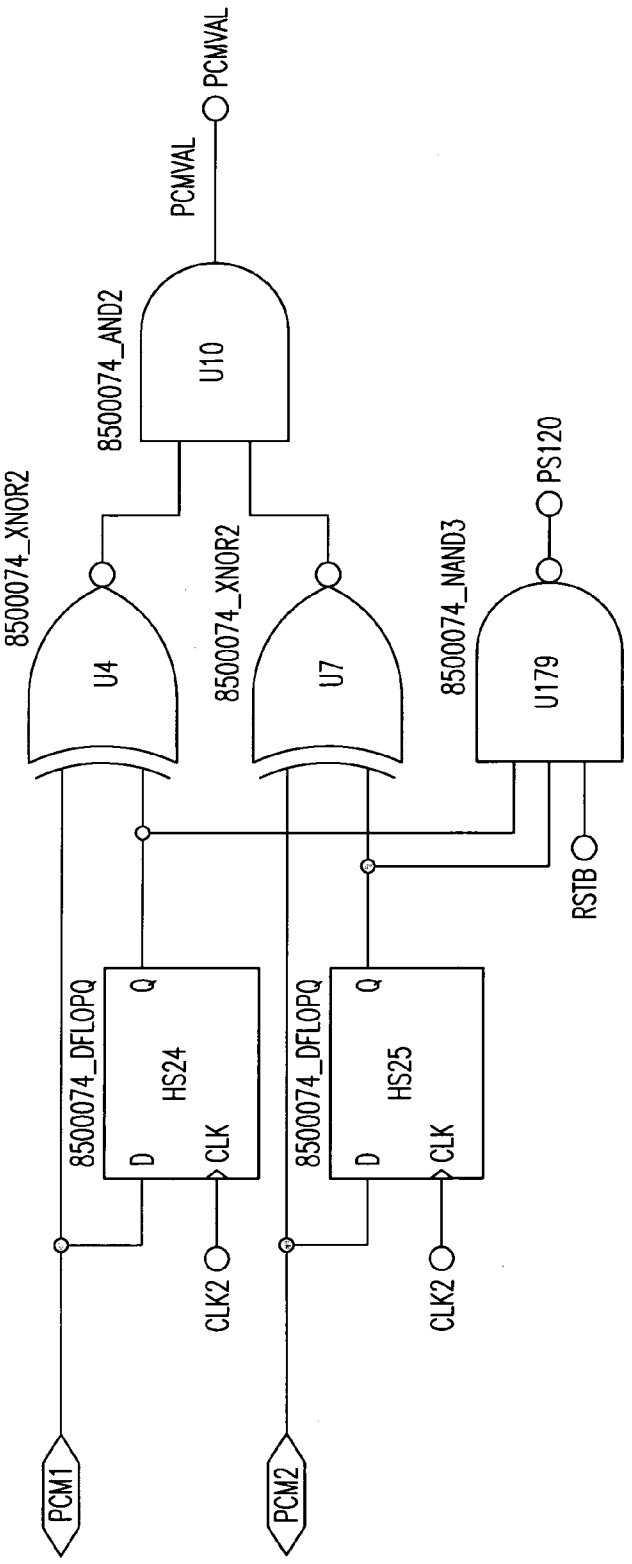

FIG.156A
FIG.156B
FIG.156C
FIG.156D
FIG.156E-1
FIG.156E-2
FIG.156F
FIG.156G
FIG.156H
FIG.156I
FIG.156J
FIG.156K
FIG.156L
FIG.156M
FIG.156N
FIG.156O
FIG.156P
FIG.156Q
FIG.156R
FIG.156S
FIG.156T
FIG.156U
FIG.156V

FIG.156


PCMVAL
PCMVAL
8500074_AND2
U10
8500074_XNOR2
U4
8500074_XNOR2
U7
8500074_NAND3
U179
PS120
RSTB
8500074_DFLOPQ
HS24
D
Q
CLK
8500074_DFLOPQ
HS25
D
Q
CLK
CLK2
CLK2
PCM1
PCM2

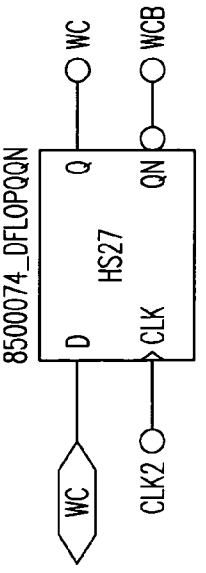

WC
WCB
8500074_DFLOPQQN
HS27
D
Q
QN
CLK
WC
CLK2

FIG. 156A

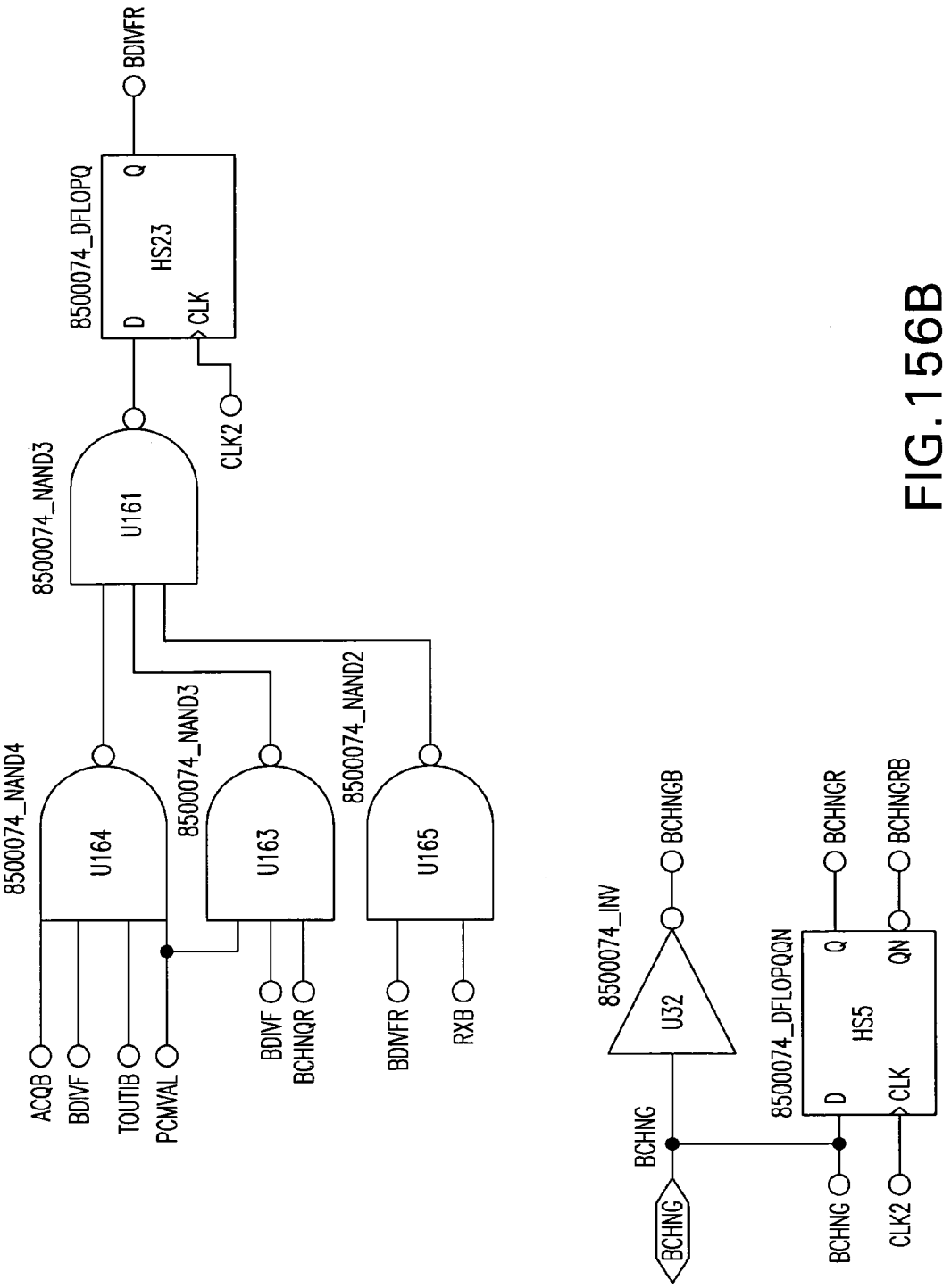

BDIVFR
8500074_DFLOPQ
HS23
D
Q
CLK
CLK2
8500074_NAND3
U161
8500074_NAND4
U164
8500074_NAND3
U163
8500074_NAND2
U165
ACQB
BDIVF
TOUTIB
PCMVAL
BDIVF
BCHNQR
BDIVFR
RXB
8500074_INV
U32
BCHNGB
BCHNG
BCHNG
8500074_DFLOPQQN
HS5
D
Q
QN
CLK
BCHNGR
BCHNGRB
BCHNG
CLK2

FIG. 156B

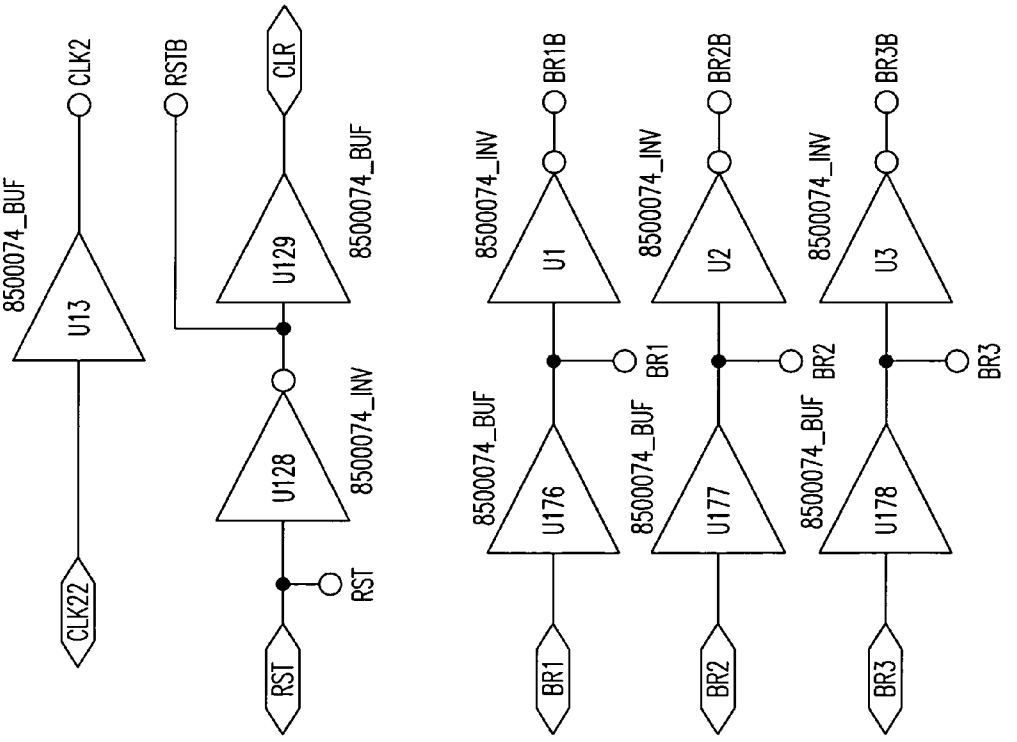

8500074_BUF
U13
CLK2
CLK22
RSTB
CLR
U129
8500074_BUF
U128
8500074_INV
RST
RST
8500074_INV
U1
BR1B
8500074_BUF
U176
BR1
BR1
8500074_INV
U2
BR2B
8500074_BUF
U177
BR2
BR2
8500074_INV
U3
BR3B
8500074_BUF
U178
BR3
BR3

FIG.156C

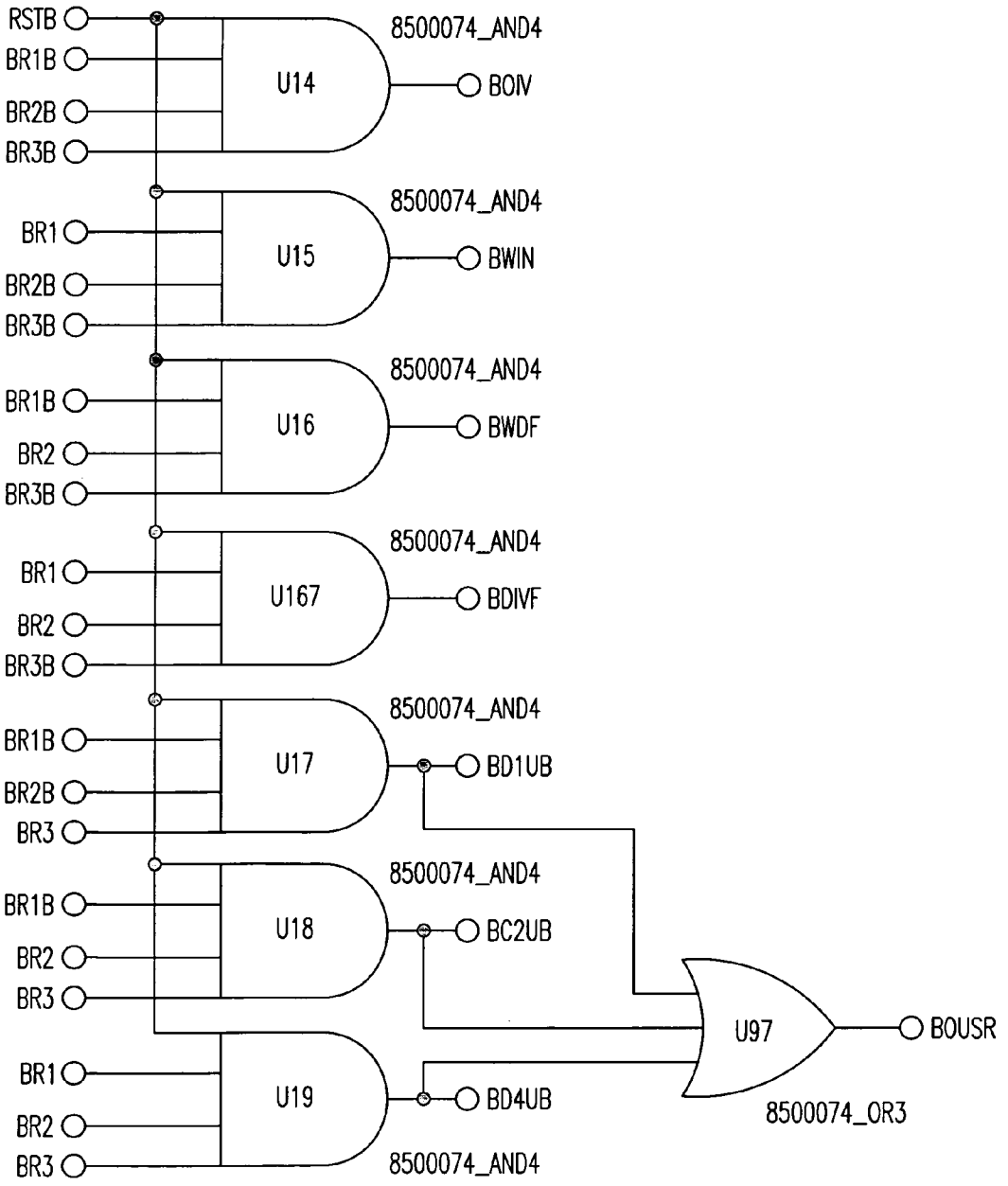

RSTB
BR1B
BR2B
BR3B
U14
8500074_AND4
BOIV
BR1
BR2B
BR3B
U15
8500074_AND4
BWIN
BR1B
BR2
BR3B
U16
8500074_AND4
BWDF
BR1
BR2
BR3B
U167
8500074_AND4
BDIVF
BR1B
BR2B
BR3
U17
8500074_AND4
BD1UB
BR1B
BR2
BR3
U18
8500074_AND4
BC2UB
BR1
BR2
BR3
U19
BD4UB
8500074_AND4
U97
BOUSR
8500074_OR3

FIG.156D

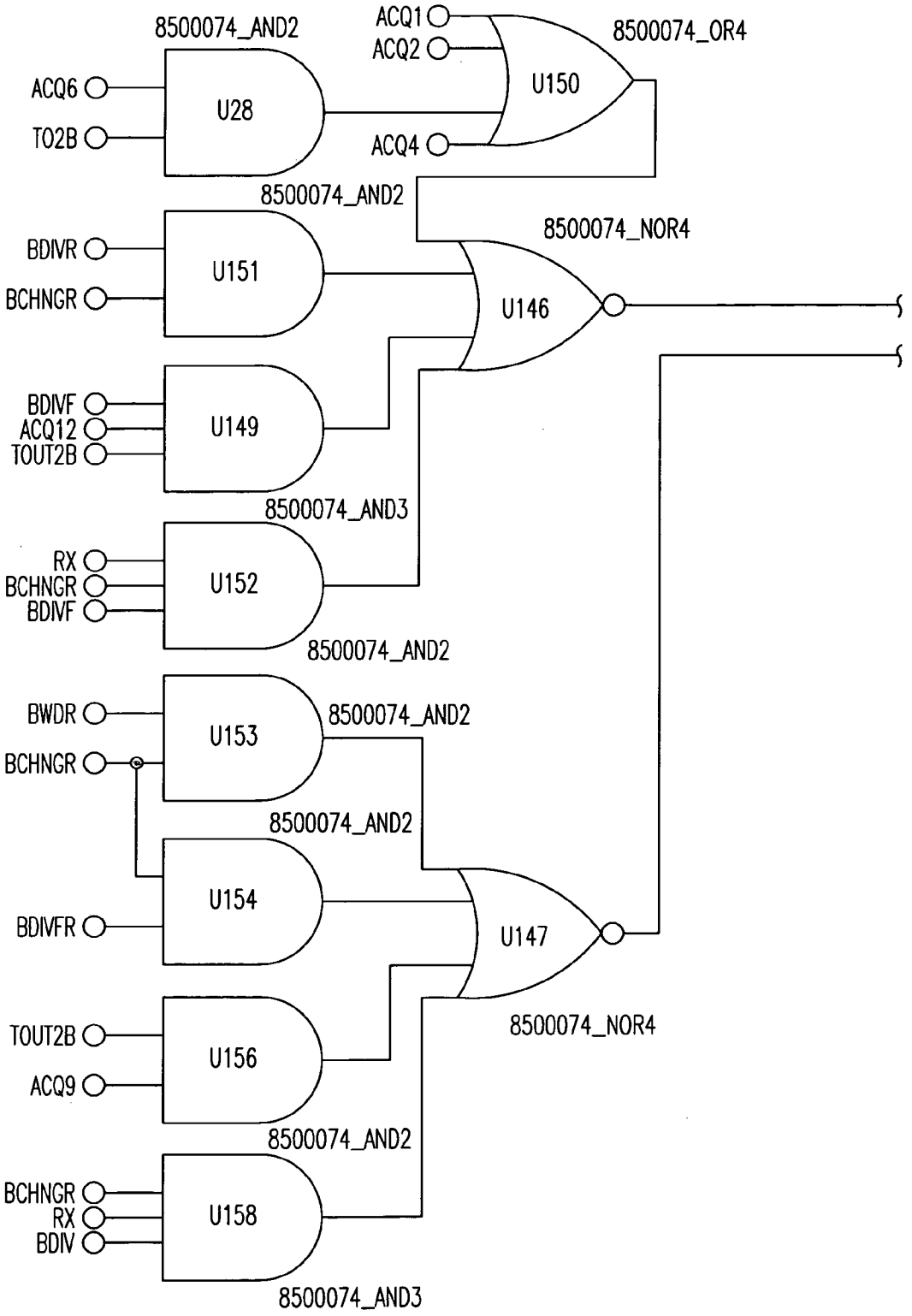

8500074_AND2
U28
ACQ6
T02B
ACQ1
ACQ2
ACQ4
U150
8500074_OR4
8500074_AND2
U151
BDIVR
BCHNGR
8500074_NOR4
U146
U149
BDIVF
ACQ12
TOUT2B
8500074_AND3
U152
RX
BCHNGR
BDIVF
8500074_AND2
U153
BWDR
BCHNGR
8500074_AND2
8500074_AND2
U154
BDIVFR
U147
U156
TOUT2B
ACQ9
8500074_NOR4
8500074_AND2
U158
BCHNGR
RX
BDIV
8500074_AND3

FIG.156E-1

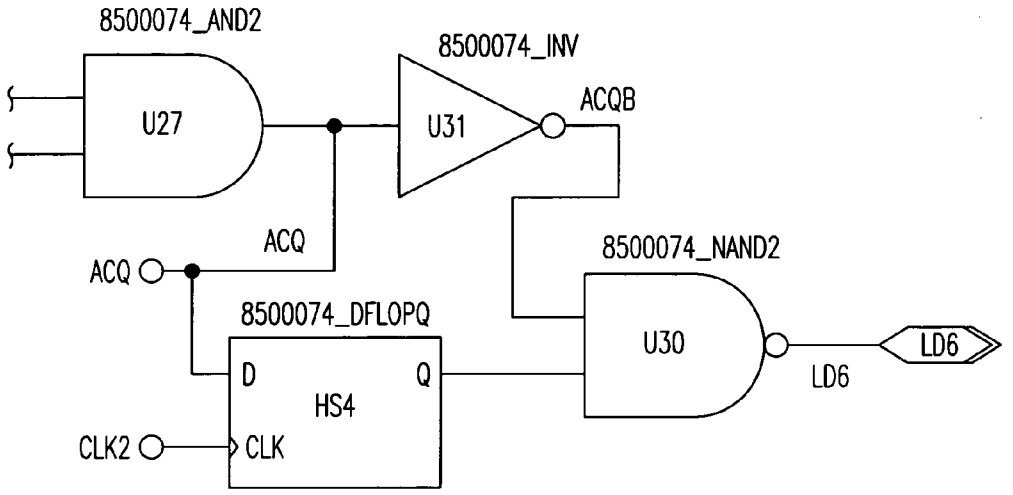

8500074_AND2
U27
8500074_INV
U31
ACQB
ACQ
ACQ
8500074_NAND2
8500074_DFLOPQ
U30
LD6
LD6
D
Q
HS4
CLK2
CLK

FIG.156E-2

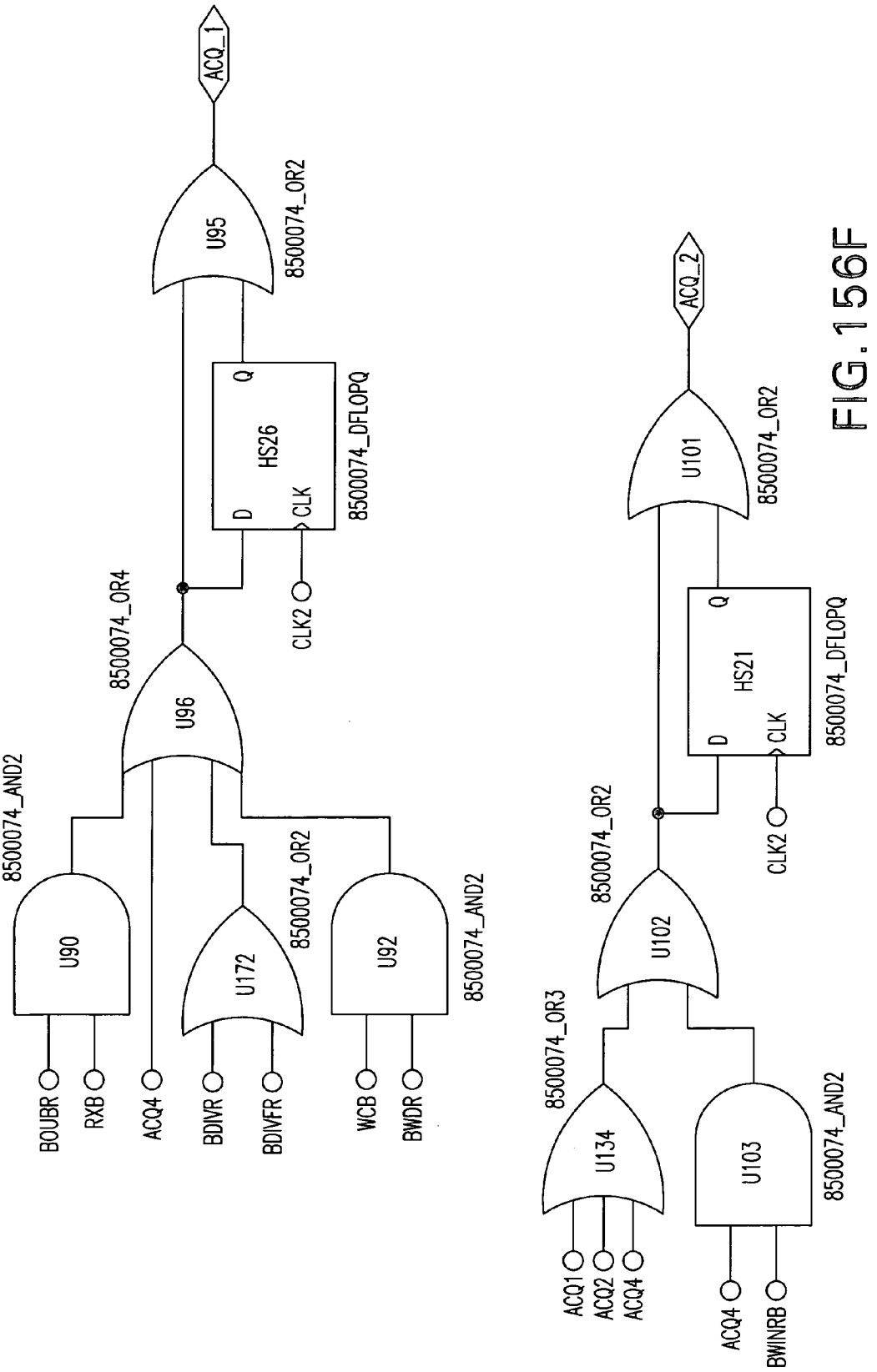

ACQ_1
U95
8500074_OR2
HS26
D
Q
CLK
8500074_DFLOPQ
CLK2
8500074_OR4
U96
8500074_AND2
U90
BOUBR
RXB
ACQ4
8500074_OR2
U172
BDIVR
BDIVFR
8500074_AND2
U92
WCB
BWDR
ACQ_2
U101
8500074_OR2
HS21
D
Q
CLK
8500074_DFLOPQ
CLK2
8500074_OR2
U102
8500074_OR3
U134
ACQ1
ACQ2
ACQ4
8500074_AND2
U103
ACQ4
BWINRB

FIG. 156F

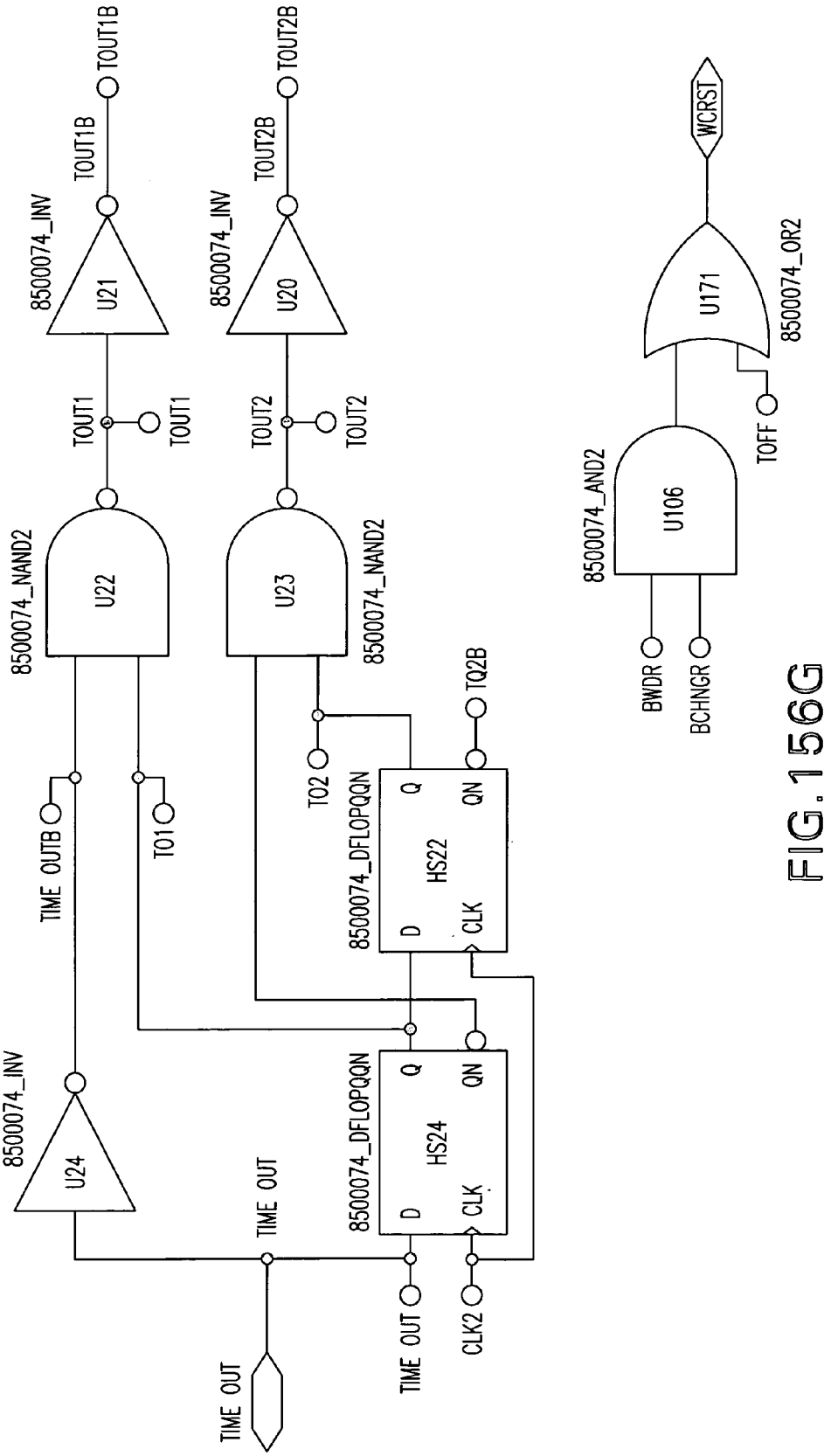

WCRST
8500074_OR2
U171
TOFF
8500074_AND2
U106
BWDR
BCHNGR
TOUT1B
TOUT2B
8500074_INV
U21
U20
TOUT1
TOUT2
8500074_NAND2
U22
U23
TIME_OUTB
T01
T02
TQ2B
8500074_DFLOPQQN
HS22
D
CLK
Q
QN
8500074_INV
U24
TIME_OUT
HS24
CLK2

FIG. 156G

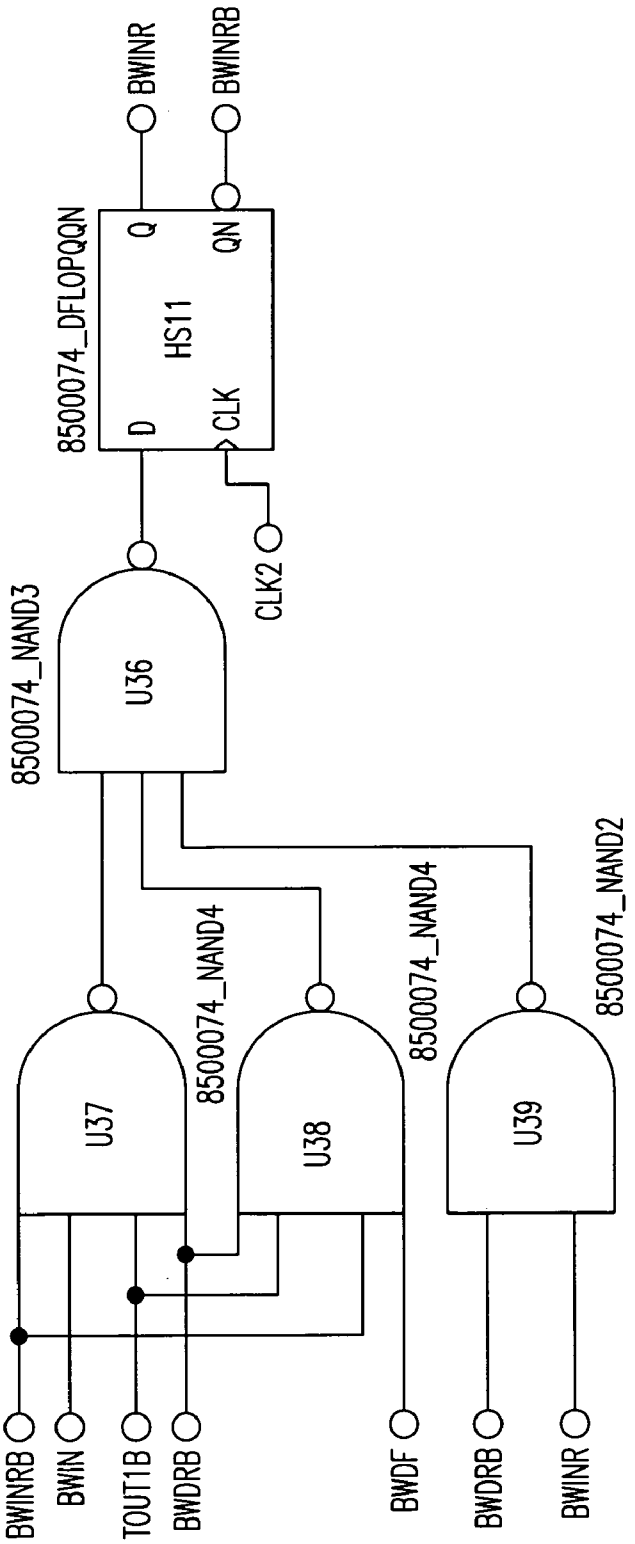

BWINR
BWINRB
8500074_DFLOPQQN
HS11
Q
QN
D
CLK
CLK2
8500074_NAND3
U36
8500074_NAND4
U37
8500074_NAND4
U38
8500074_NAND2
U39
BWINRB
BWIN
TOUT1B
BWDRB
BWDF
BWDRB
BWINR

FIG.156H

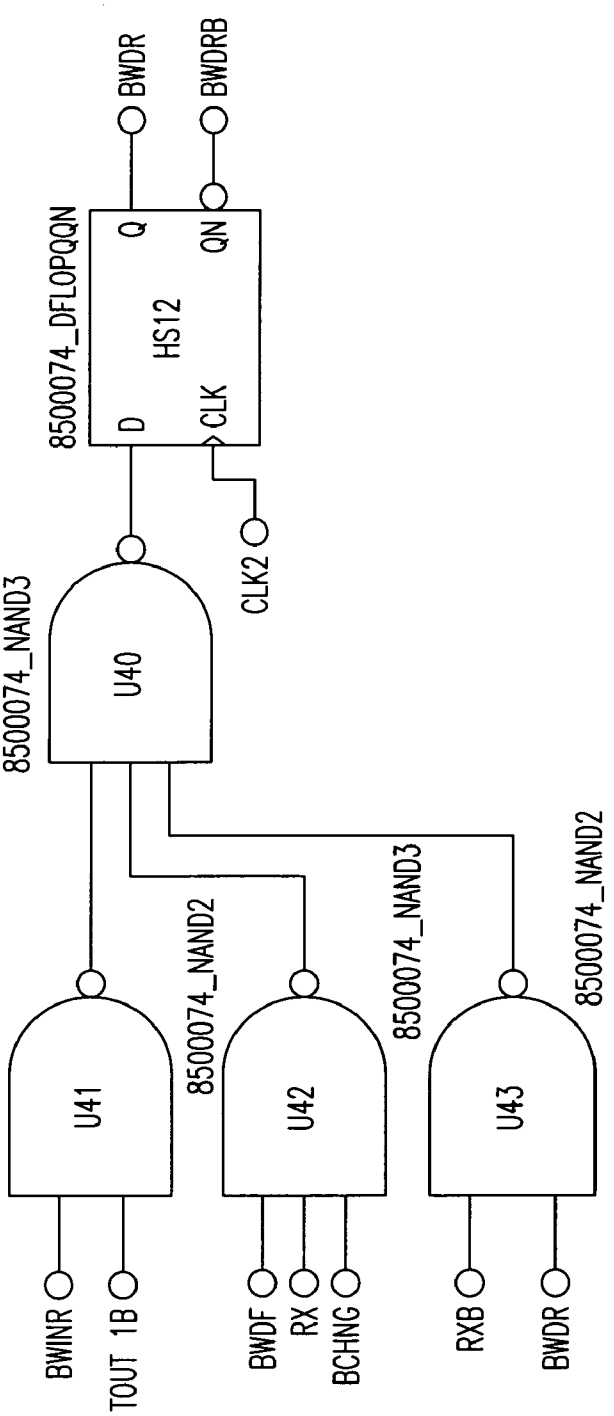

BWDR
BWDRB
8500074_DFLOPQQN
Q
QN
HS12
D
CLK
CLK2
8500074_NAND3
U40
8500074_NAND2
8500074_NAND3
8500074_NAND2
U41
U42
U43
BWINR
TOUT 1B
BWDF
RX
BCHNG
RXB
BWDR

FIG.156I

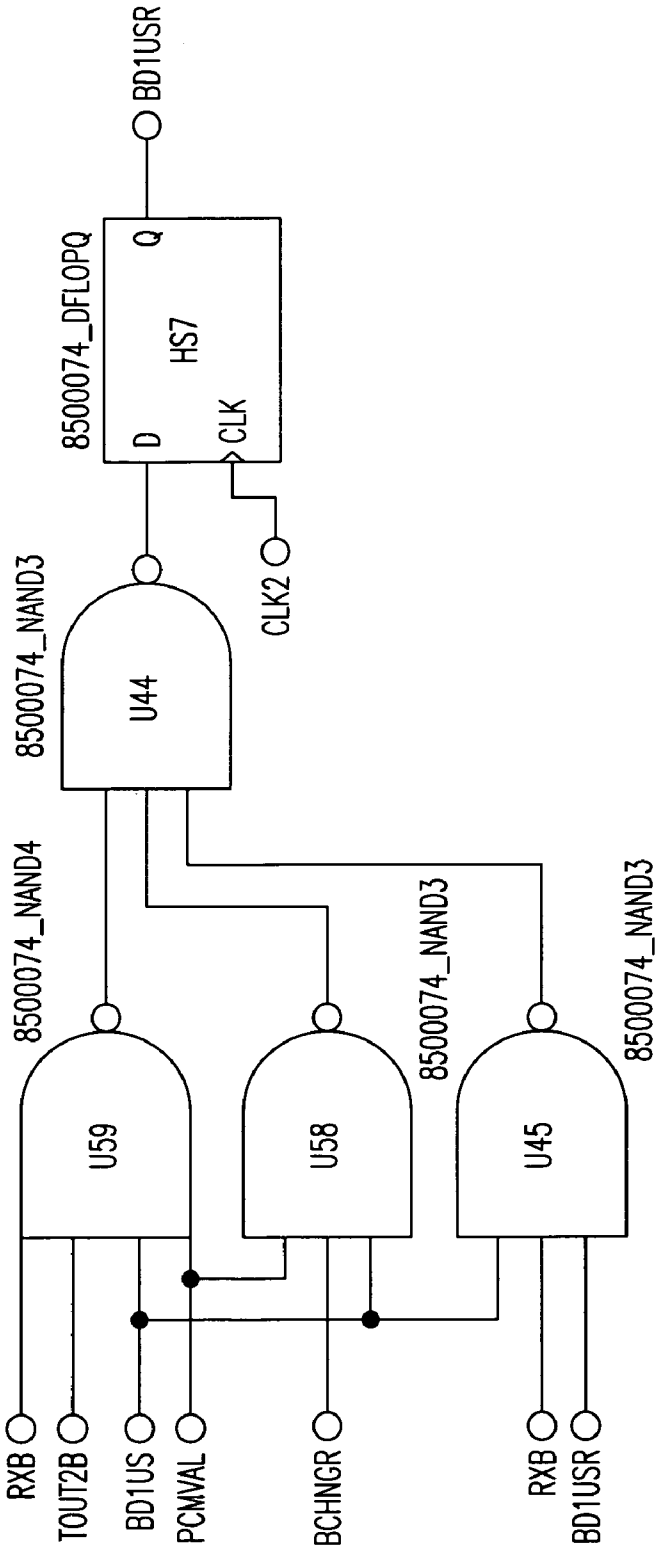

BD1USR
8500074_DFLOPQ
HS7
Q
D
CLK
CLK2
8500074_NAND3
U44
8500074_NAND4
U59
8500074_NAND3
U58
8500074_NAND3
U45
RXB
TOUT2B
BD1US
PCMVAL
BCHNGR
RXB
BD1USR

FIG.156J

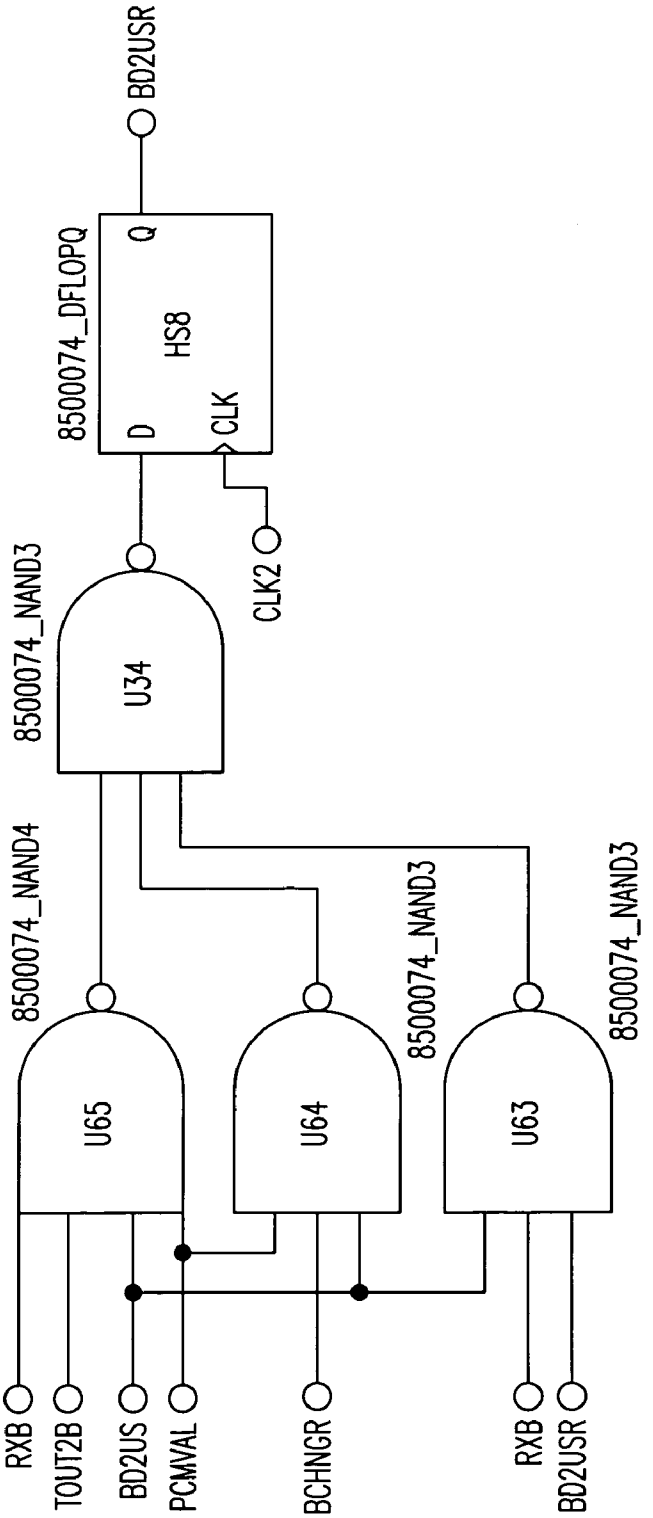

BD2USR
8500074_DFLOPQ
HS8
Q
D
CLK
CLK2
8500074_NAND3
U34
8500074_NAND4
U65
8500074_NAND3
U64
8500074_NAND3
U63
RXB
TOUT2B
BD2US
PCMVAL
BCHNGR
RXB
BD2USR

FIG.156K

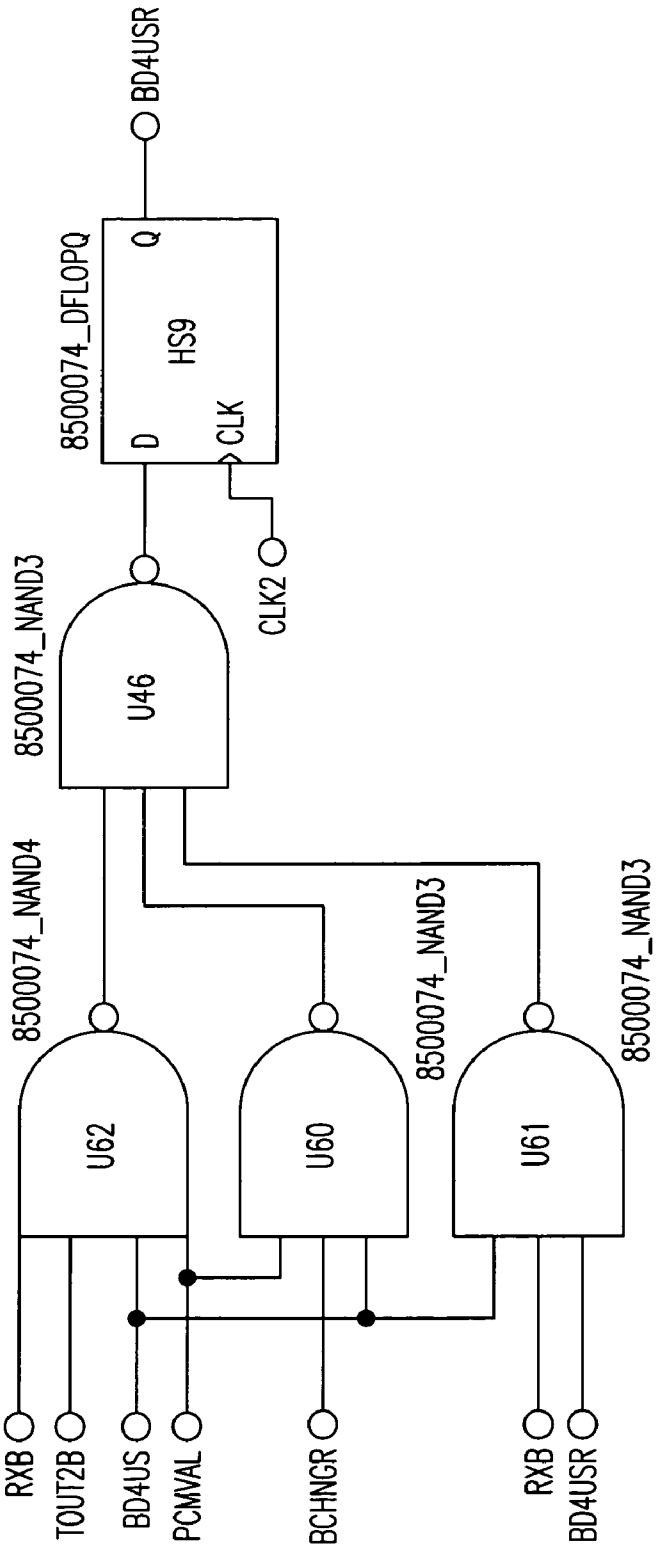

BD4USR
8500074_DFLOPQ
HS9
D
CLK
Q
CLK2
8500074_NAND3
U46
8500074_NAND4
U62
U60
U61
8500074_NAND3
8500074_NAND3
RXB
TOUT2B
BD4US
PCMVAL
BCHNGR
RXB
BD4USR

FIG.156L

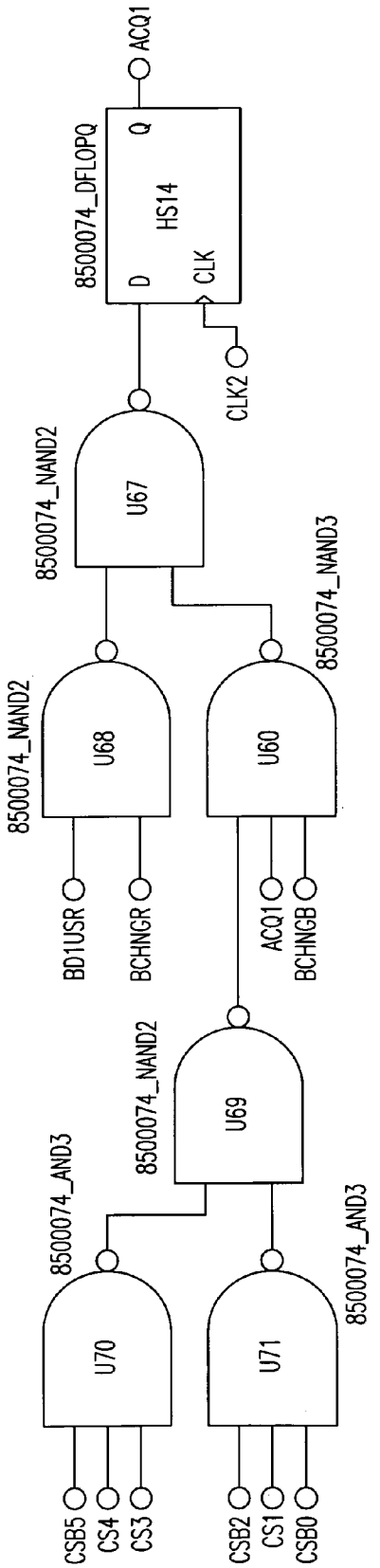

ACQ1
8500074_DFLOPQ
Q
HS14
D
CLK
CLK2
8500074_NAND2
U67
8500074_NAND2
U68
8500074_NAND3
U60
BD1USR
BCHNGR
ACQ1
BCHNGB
8500074_NAND2
U69
8500074_AND3
U70
8500074_AND3
U71
CSB5
CS4
CS3
CSB2
CS1
CSB0

FIG. 156M

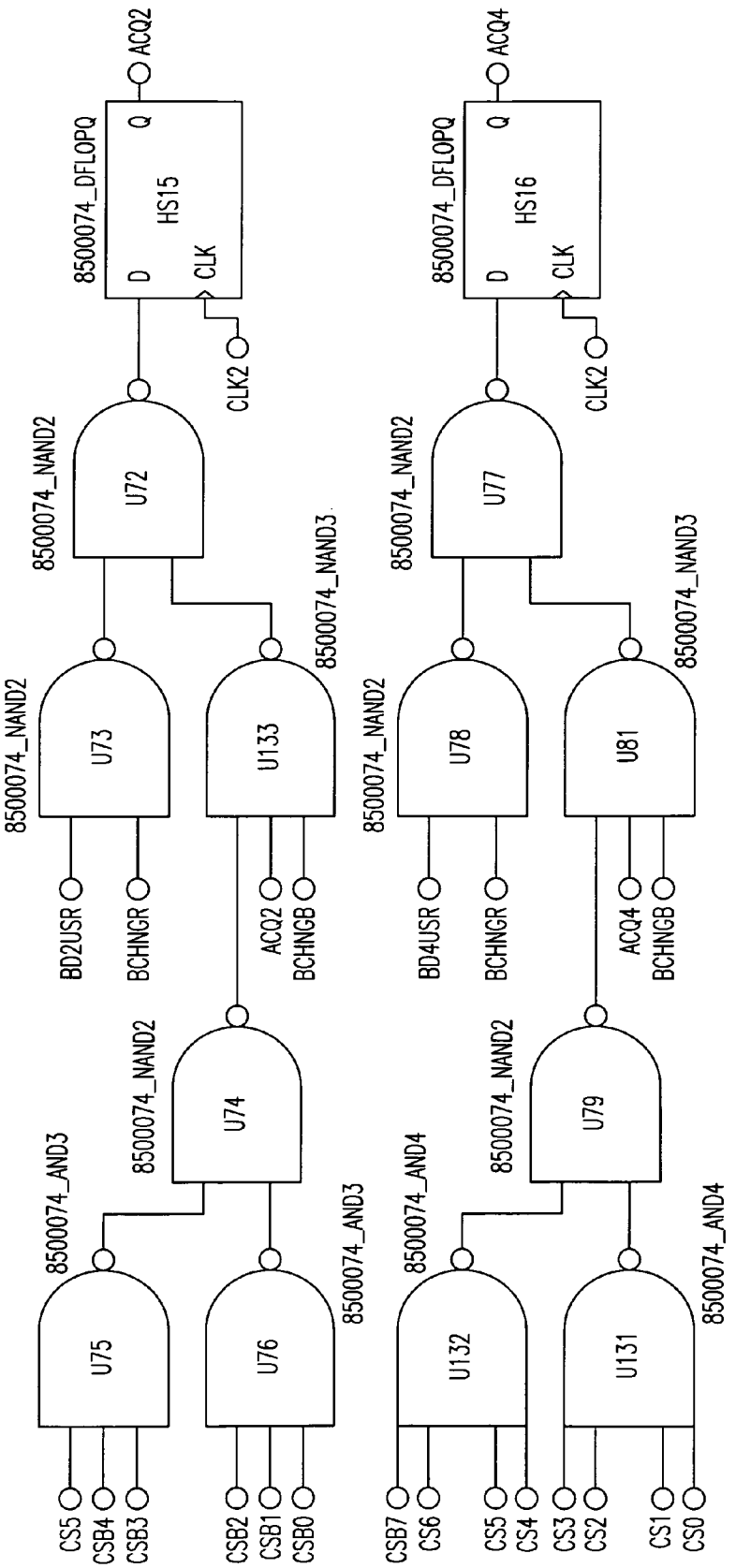

8500074_DFLOPQ
HS15
D
CLK
Q
ACQ2
CLK2
8500074_NAND2
U72
8500074_NAND3
U73
U133
BD2USR
BCHNGR
ACQ2
BCHNGB
8500074_NAND2
U74
8500074_AND3
U75
U76
CS5
CSB4
CSB3
CSB2
CSB1
CSB0
8500074_DFLOPQ
HS16
ACQ4
8500074_NAND2
U77
8500074_NAND3
U78
U81
BD4USR
BCHNGR
ACQ4
BCHNGB
8500074_NAND2
U79
8500074_AND4
U132
U131
CSB7
CS6
CS5
CS4
CS3
CS2
CS1
CS0

FIG. 156N

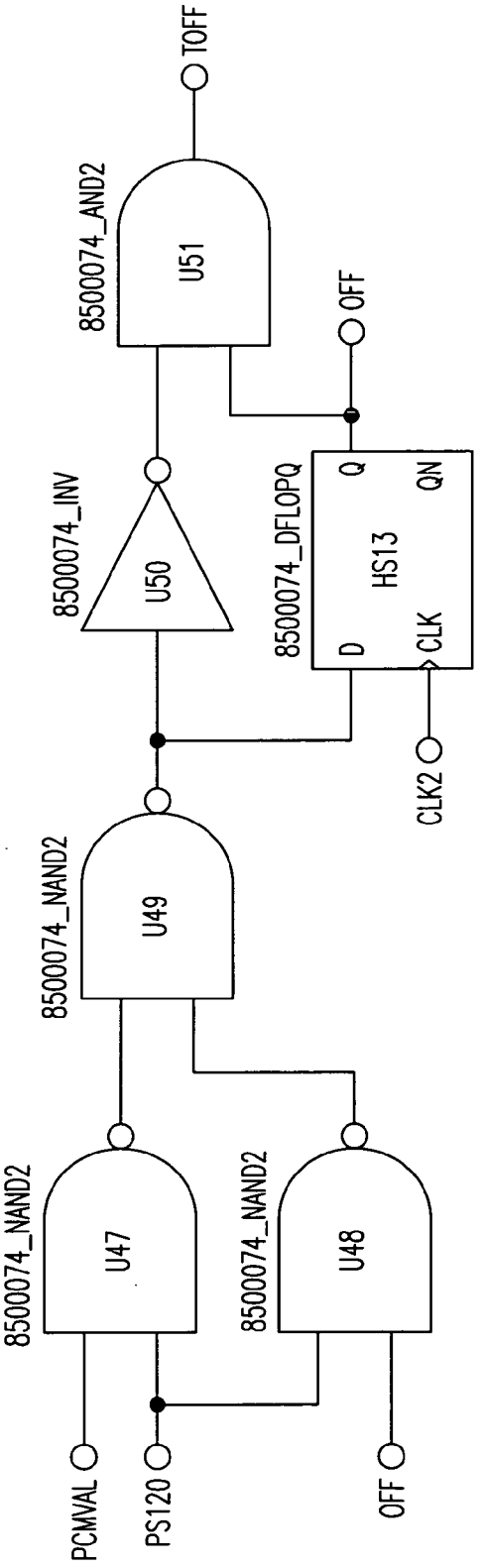

TOFF
8500074_AND2
U51
OFF
8500074_INV
U50
8500074_DFLOPQ
HS13
Q
QN
D
CLK
CLK2
8500074_NAND2
U49
8500074_NAND2
U47
8500074_NAND2
U48
PCMVAL
PS120
OFF

FIG. 156O

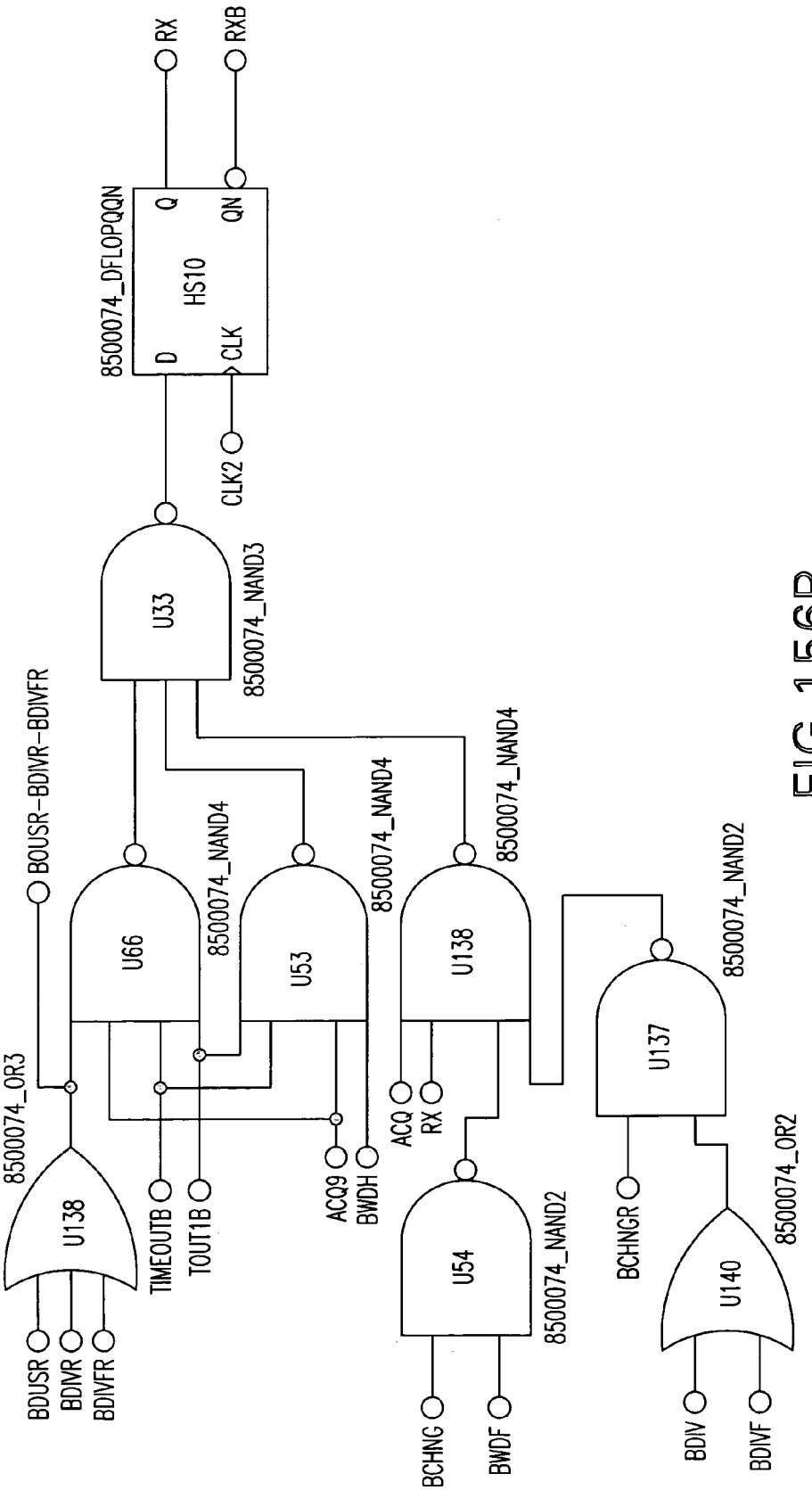

RX
RXB
8500074_DFLOPQQN
HS10
D
CLK
Q
QN
CLK2
U33
8500074_NAND3
BOUSR-BDIVR-BDIVFR
U66
8500074_NAND4
U53
8500074_NAND4
U138
8500074_NAND4
8500074_OR3
U138
TIMEOUTB
TOUT1B
ACQ9
BWDH
ACQ
RX
U54
8500074_NAND2
U137
8500074_NAND2
BCHNGR
U140
8500074_OR2
BDUSR
BDIVR
BDIVFR
BCHNG
BWDF
BDIV
BDIVF

FIG. 156P

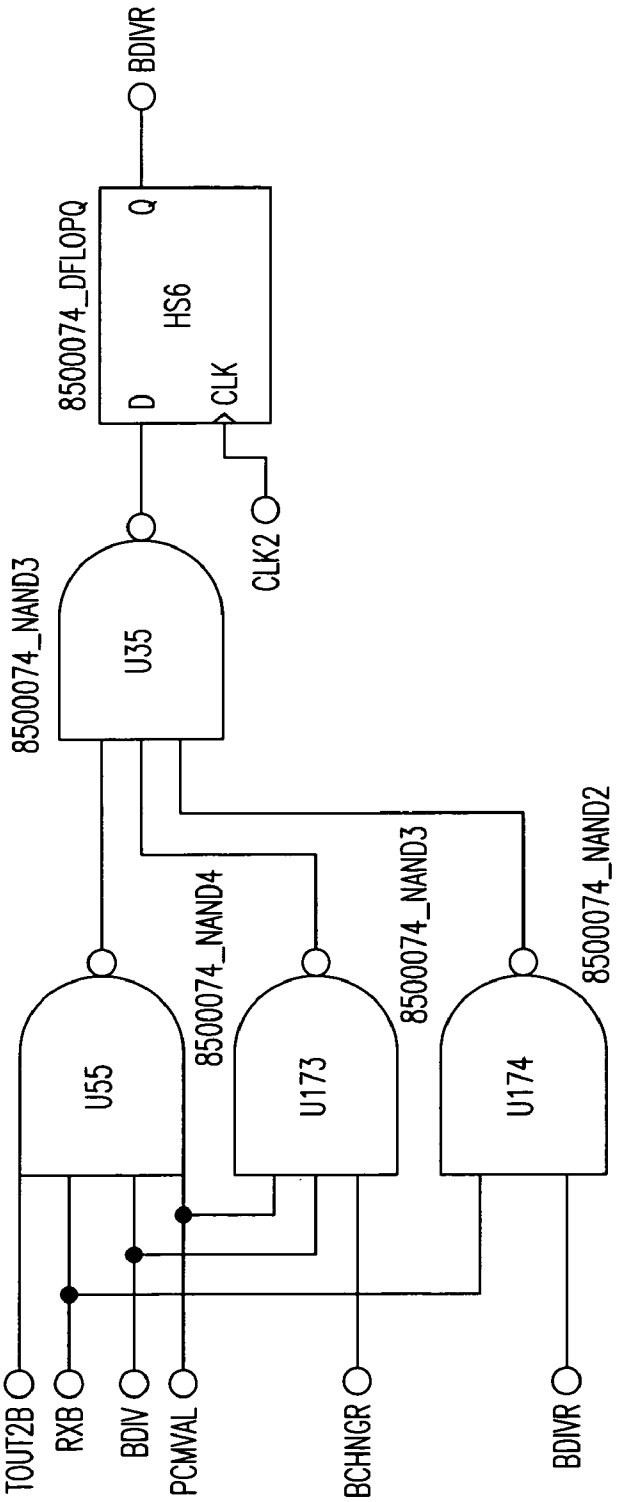

BDIVR
8500074_DFLOPQ
HS6
Q
D
CLK
CLK2
8500074_NAND3
U35
8500074_NAND4
U55
8500074_NAND3
U173
8500074_NAND2
U174
TOUT2B
RXB
BDIV
PCMVAL
BCHNGR
BDIVR

FIG.156Q

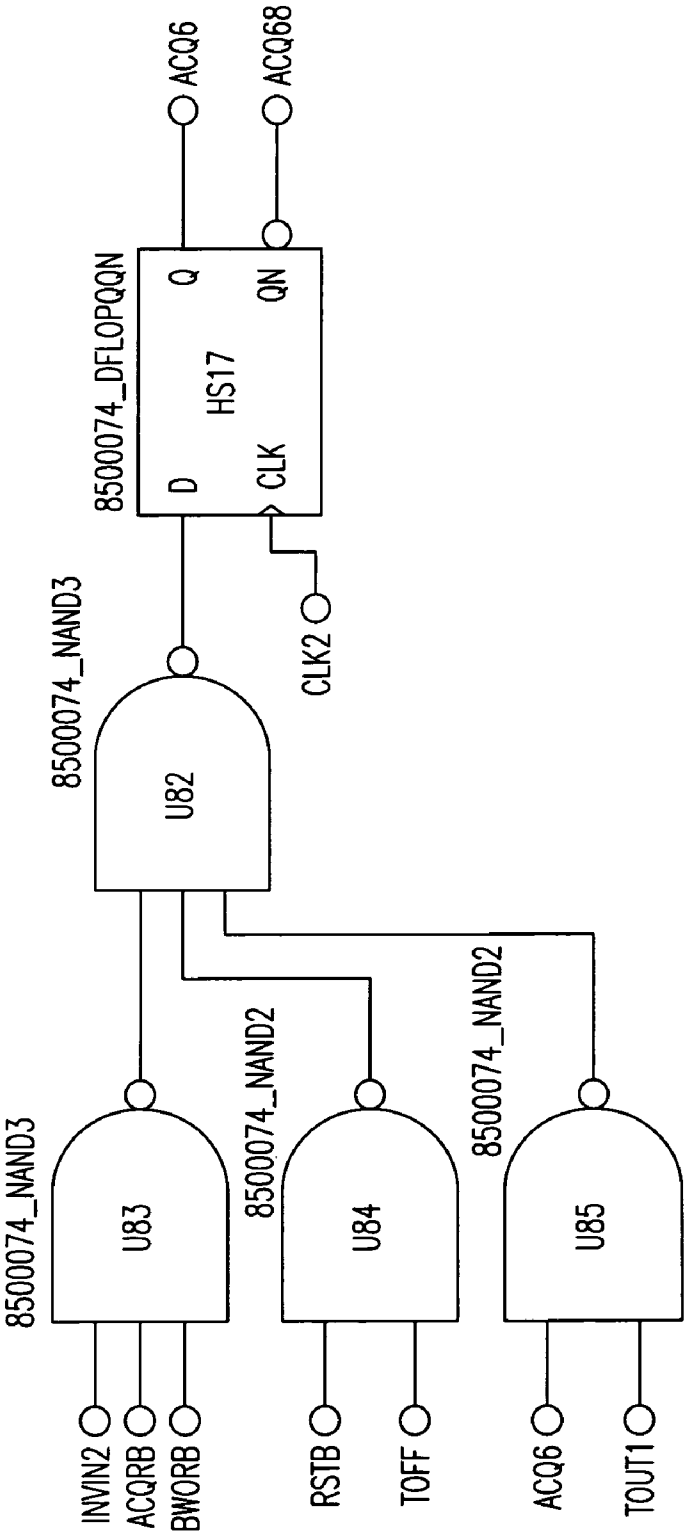

ACQ6
ACQ68
8500074_DFLOPQQN
HS17
D
CLK
Q
QN
CLK2
8500074_NAND3
U82
8500074_NAND3
U83
8500074_NAND2
U84
8500074_NAND2
U85
INVIN2
ACQRB
BWORB
RSTB
TOFF
ACQ6
TOUT1

FIG. 156R

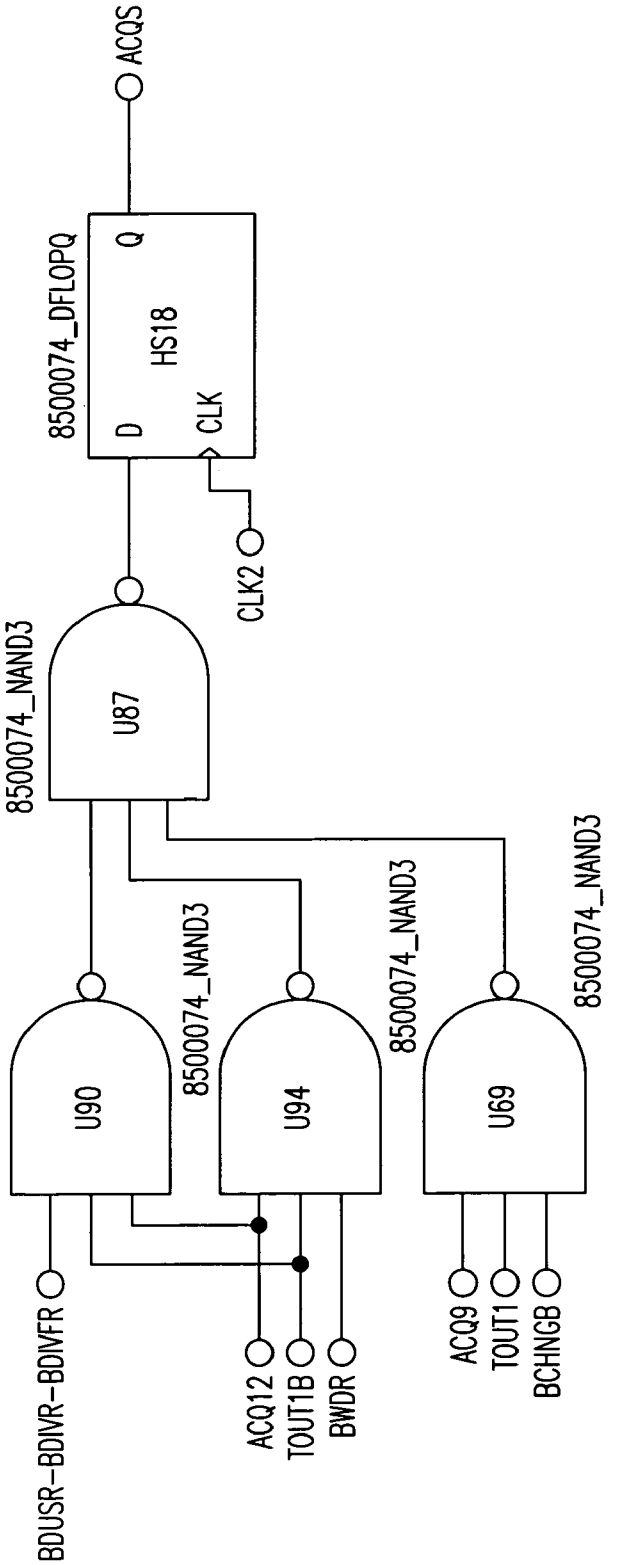

ACQS
8500074_DFLOPQ
Q
HS18
D
CLK
CLK2
8500074_NAND3
U87
U90
U94
U69
BDUSR-BDIVR-BDIVFR
ACQ12
TOUT1B
BWDR
ACQ9
TOUT1
BCHNGB

FIG.156S

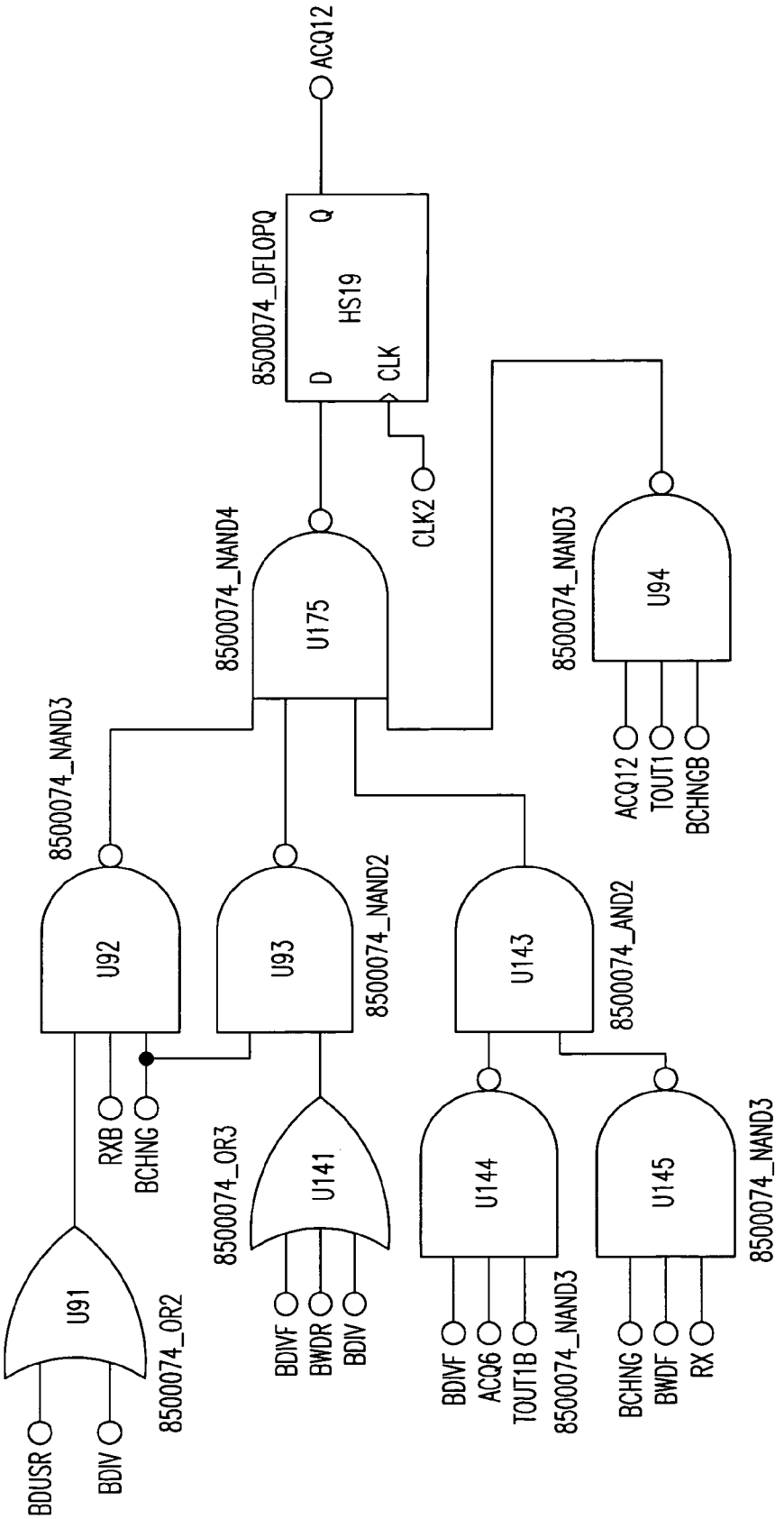

ACQ12
8500074_DFLOPQ
D
HS19
Q
CLK
CLK2
8500074_NAND4
U175
8500074_NAND3
U94
ACQ12
TOUT1
BCHNGB
8500074_NAND3
U92
8500074_NAND2
U93
8500074_AND2
U143
RXB
BCHNG
8500074_OR3
U141
U144
U145
8500074_NAND3
U91
8500074_OR2
BDUSR
BDIV
BDIVF
BWDR
BDIV
BDIVF
ACQ6
TOUT1B
8500074_NAND3
BCHNG
BWDF
RX

FIG.156T

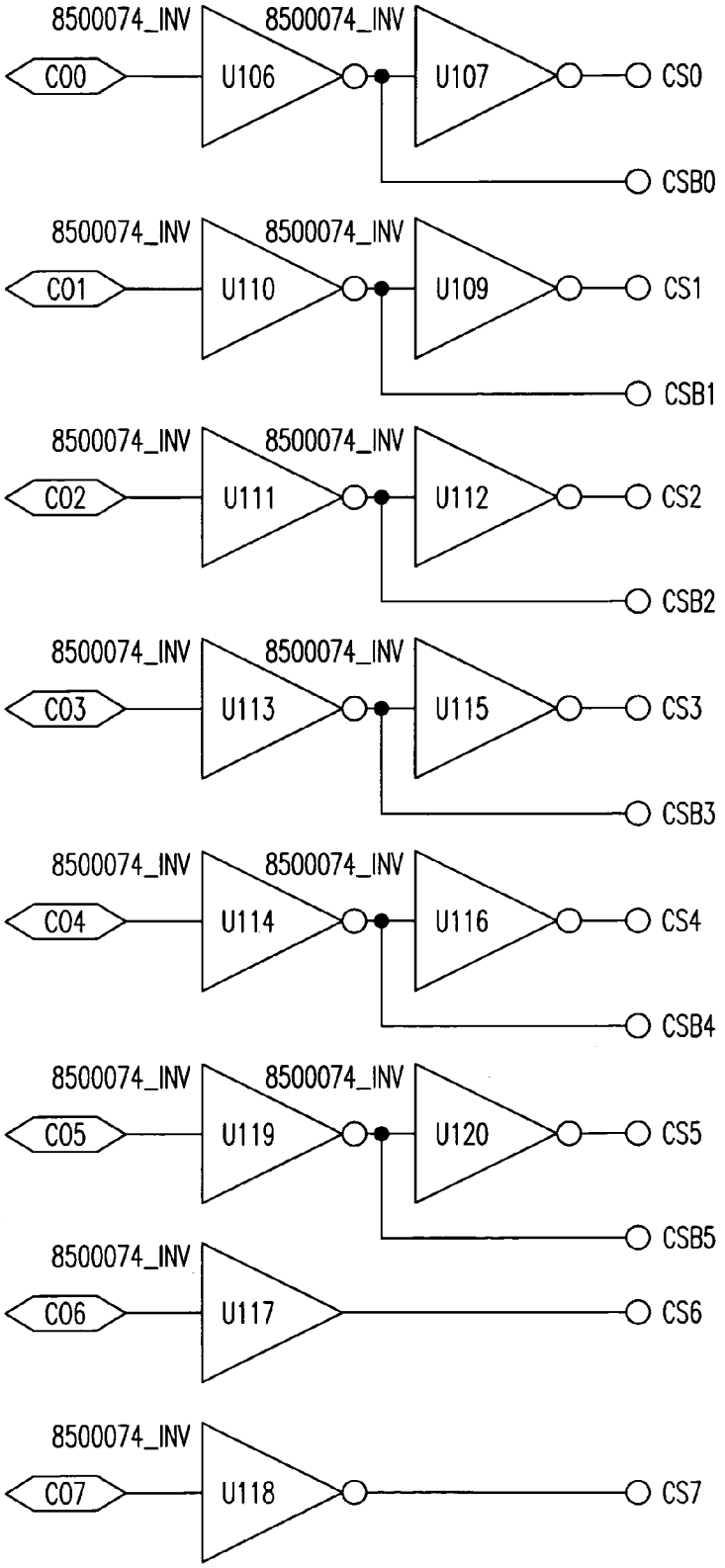

8500074_INV
8500074_INV
C00
U106
U107
CS0
CSB0
8500074_INV
8500074_INV
C01
U110
U109
CS1
CSB1
8500074_INV
8500074_INV
C02
U111
U112
CS2
CSB2
8500074_INV
8500074_INV
C03
U113
U115
CS3
CSB3
8500074_INV
8500074_INV
C04
U114
U116
CS4
CSB4
8500074_INV
8500074_INV
C05
U119
U120
CS5
CSB5
8500074_INV
C06
U117
CS6
8500074_INV
C07
U118
CS7

FIG.156U

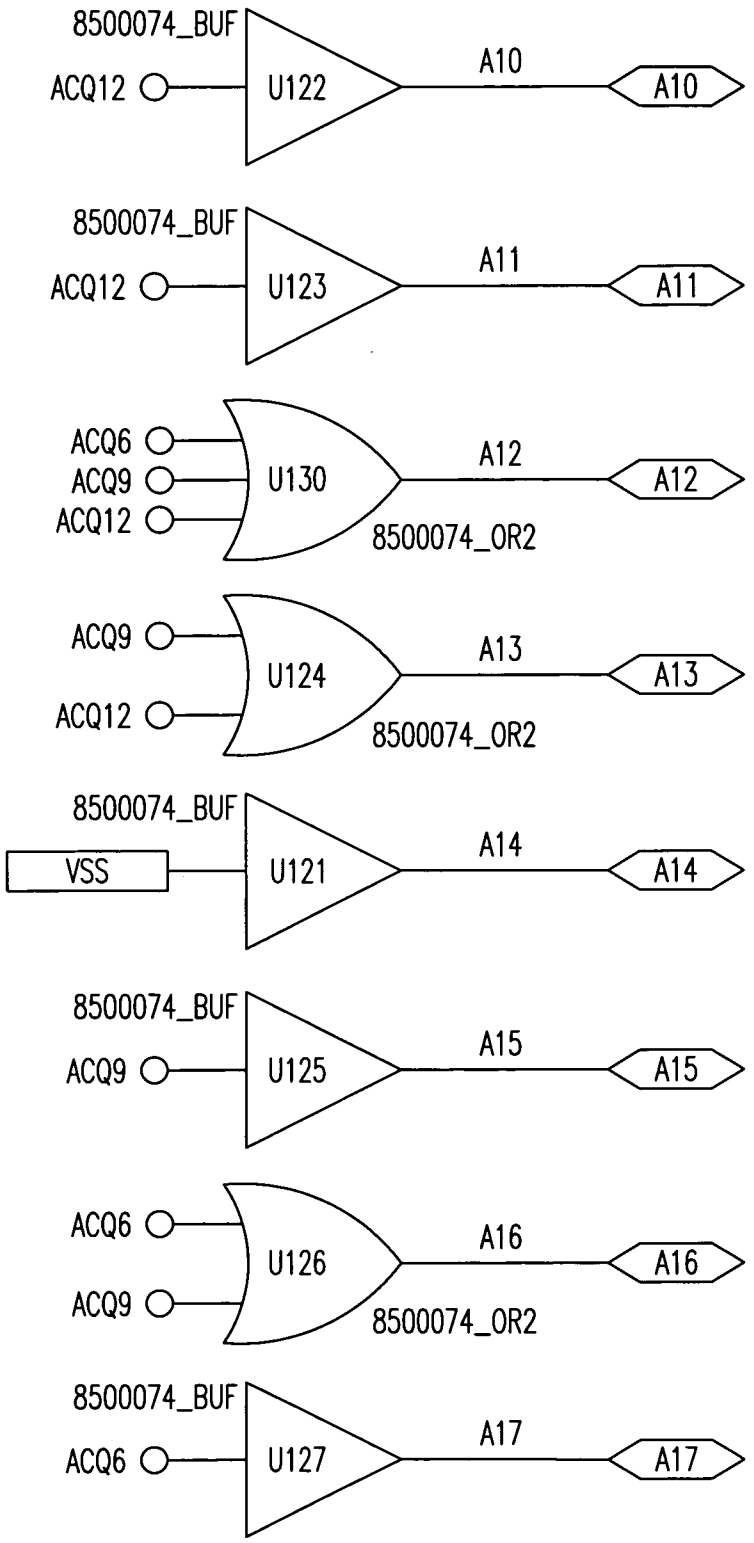

8500074_BUF
ACQ12
U122
A10
A10
8500074_BUF
ACQ12
U123
A11
A11
ACQ6
ACQ9
ACQ12
U130
A12
A12
8500074_OR2
ACQ9
ACQ12
U124
A13
A13
8500074_OR2
8500074_BUF
VSS
U121
A14
A14
8500074_BUF
ACQ9
U125
A15
A15
ACQ6
ACQ9
U126
A16
A16
8500074_OR2
8500074_BUF
ACQ6
U127
A17
A17

FIG.156V

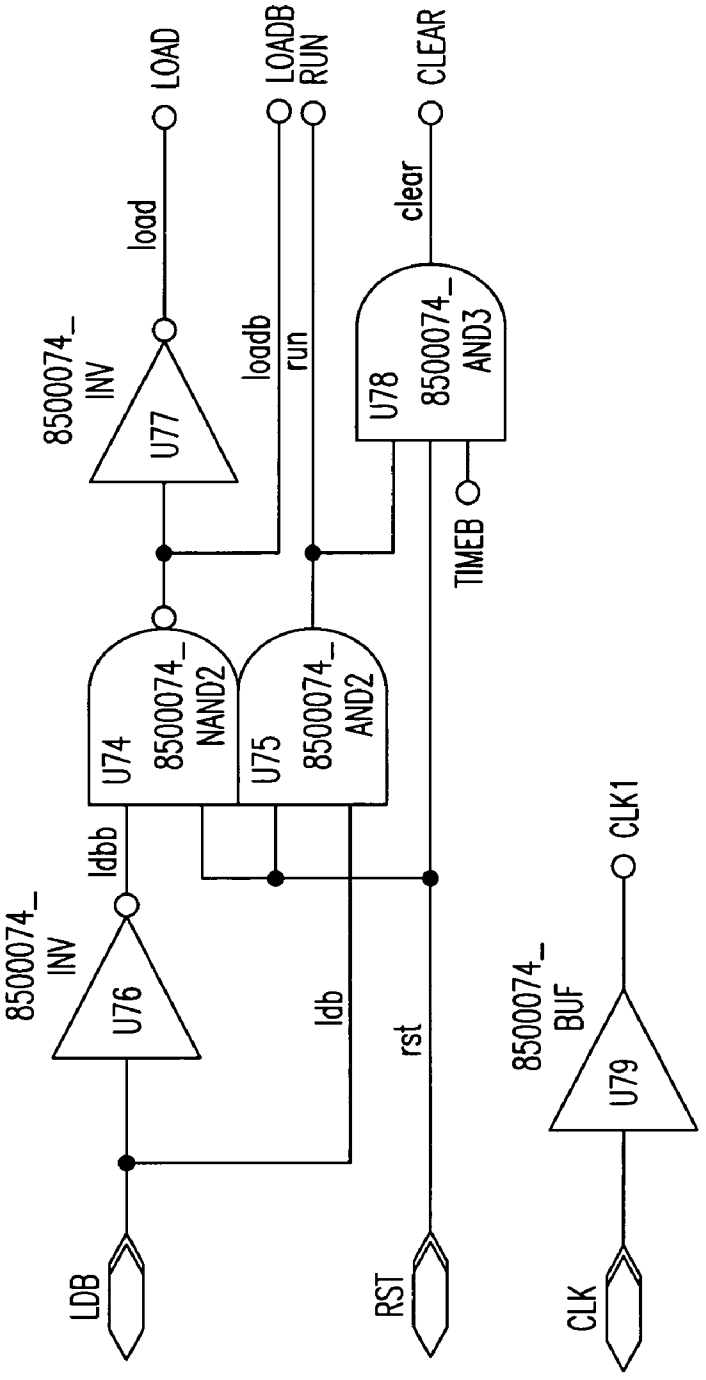

LOAD
LOADB
RUN
CLEAR
load
loadb
run
clear
8500074_
INV
U77
U78
8500074_
AND3
TIMEB
U74
8500074_
NAND2
U75
8500074_
AND2
ldbb
8500074_
INV
U76
ldb
rst
LDB
RST
CLK1
8500074_
BUF
U79
CLK

FIG.157A

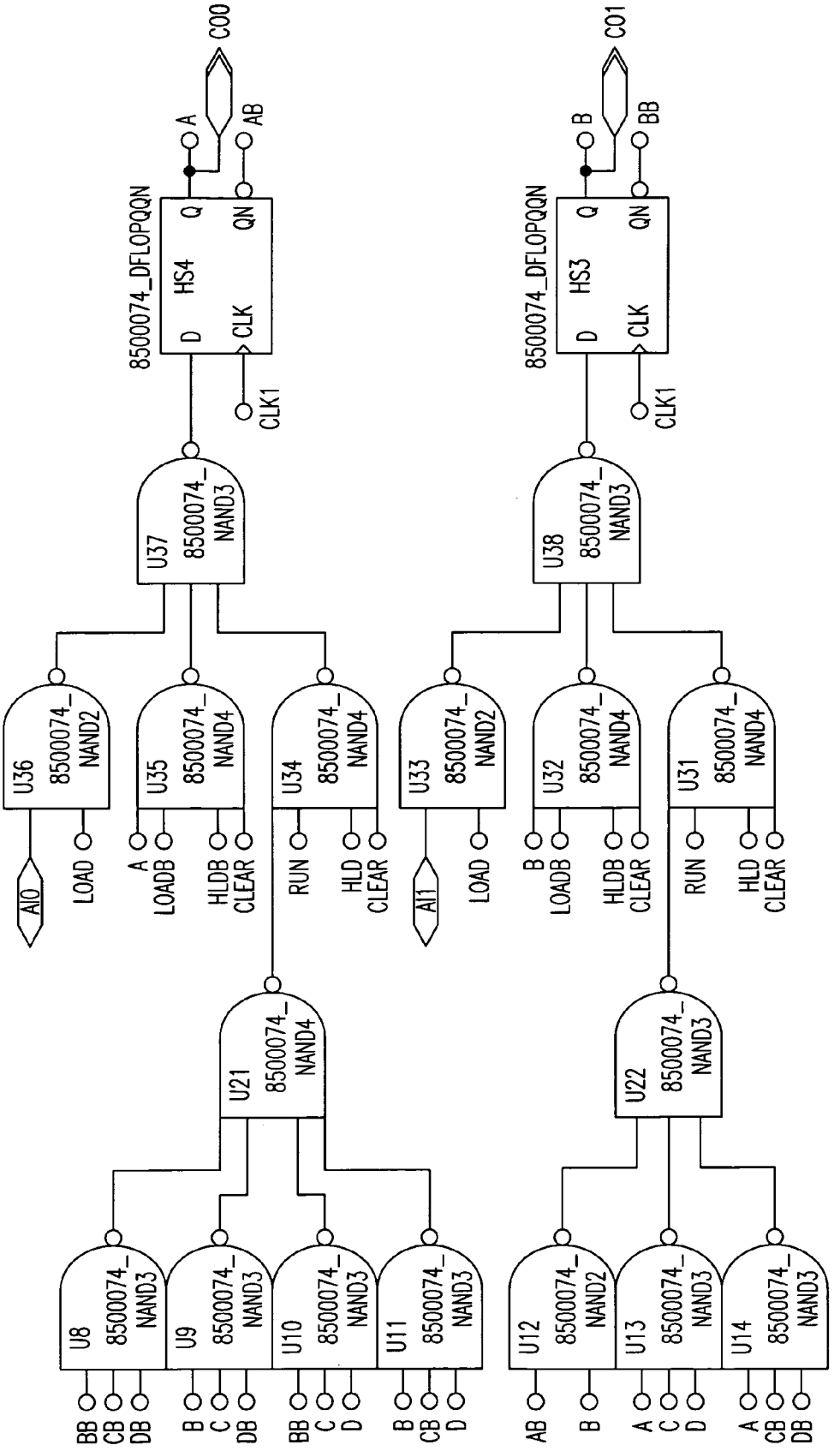

C00
A
AB
8500074_DFLOPQQN
D
HS4
Q
QN
CLK
CLK1
C01
B
BB
8500074_DFLOPQQN
D
HS3
Q
QN
CLK
CLK1
U37
8500074_
NAND3
U38
8500074_
NAND3
U36
8500074_
NAND2
U35
8500074_
NAND4
U34
8500074_
NAND4
U33
8500074_
NAND2
U32
8500074_
NAND4
U31
8500074_
NAND4
AI0
LOAD
A
LOADB
HLDB
CLEAR
RUN
HLD
CLEAR
AI1
LOAD
B
LOADB
HLDB
CLEAR
RUN
HLD
CLEAR
U21
8500074_
NAND4
U22
8500074_
NAND3
U8
8500074_
NAND3
U9
8500074_
NAND3
U10
8500074_
NAND3
U11
8500074_
NAND3
U12
8500074_
NAND2
U13
8500074_
NAND3
U14
8500074_
NAND3
BB
CB
DB
B
C
DB
BB
C
D
B
CB
D
AB
B
A
C
D
A
CB
DB

FIG.157B

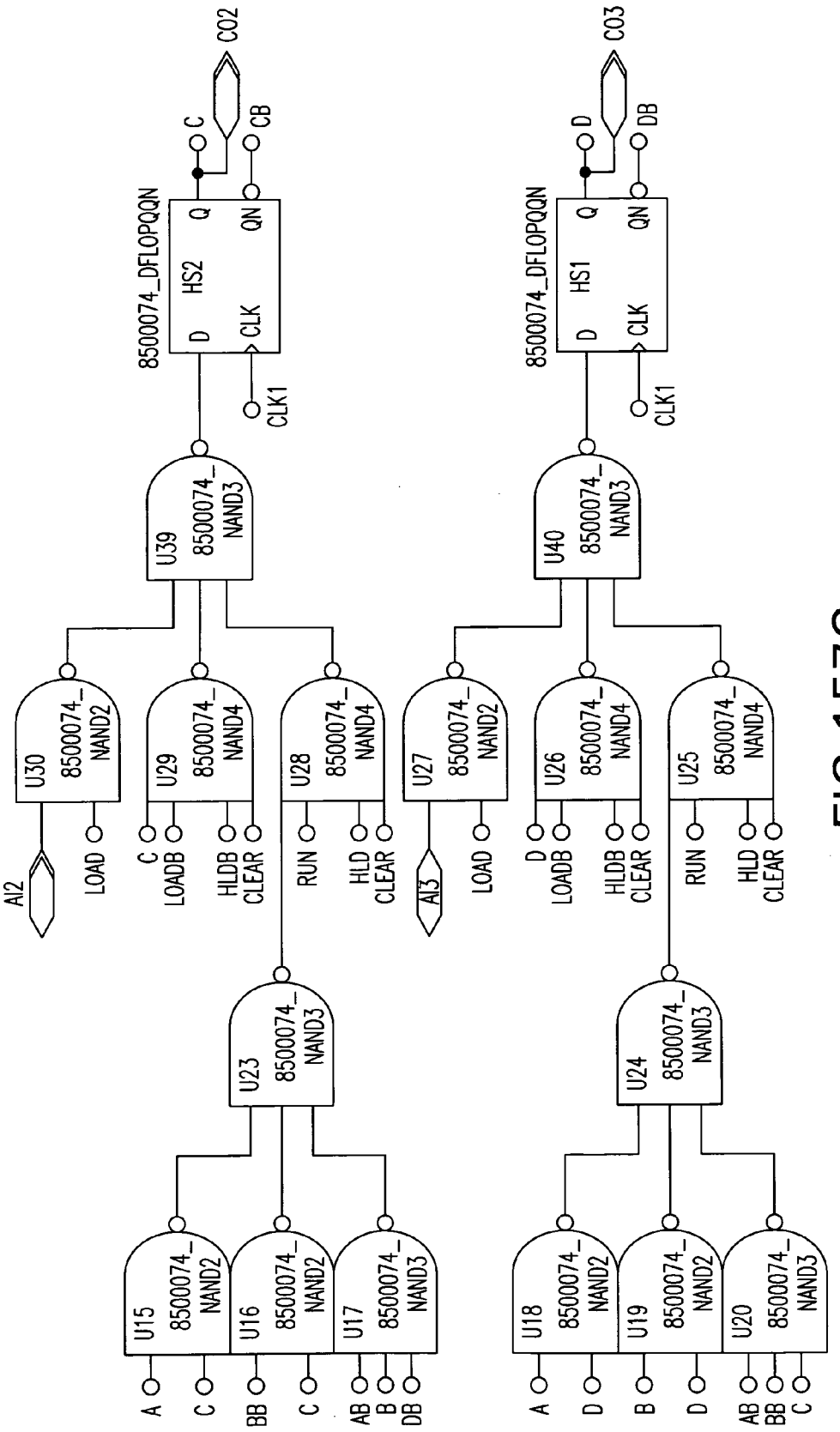

CO2
C
CB
8500074_DFLOPQQN
HS2
D
Q
QN
CLK
CLK1
U39
8500074_NAND3
U30
8500074_NAND2
AI2
LOAD
U29
8500074_NAND4
C
LOADB
HLDB
CLEAR
U28
8500074_NAND4
RUN
HLD
CLEAR
U23
8500074_NAND3
U15
8500074_NAND2
A
C
U16
8500074_NAND2
BB
C
U17
8500074_NAND3
AB
B
DB
CO3
D
DB
8500074_DFLOPQQN
HS1
D
Q
QN
CLK
CLK1
U40
8500074_NAND3
U27
8500074_NAND2
AI3
LOAD
U26
8500074_NAND4
D
LOADB
HLDB
CLEAR
U25
8500074_NAND4
RUN
HLD
CLEAR
U24
8500074_NAND3
U18
8500074_NAND2
A
D
U19
8500074_NAND2
B
D
U20
8500074_NAND3
AB
BB
C

FIG.157C

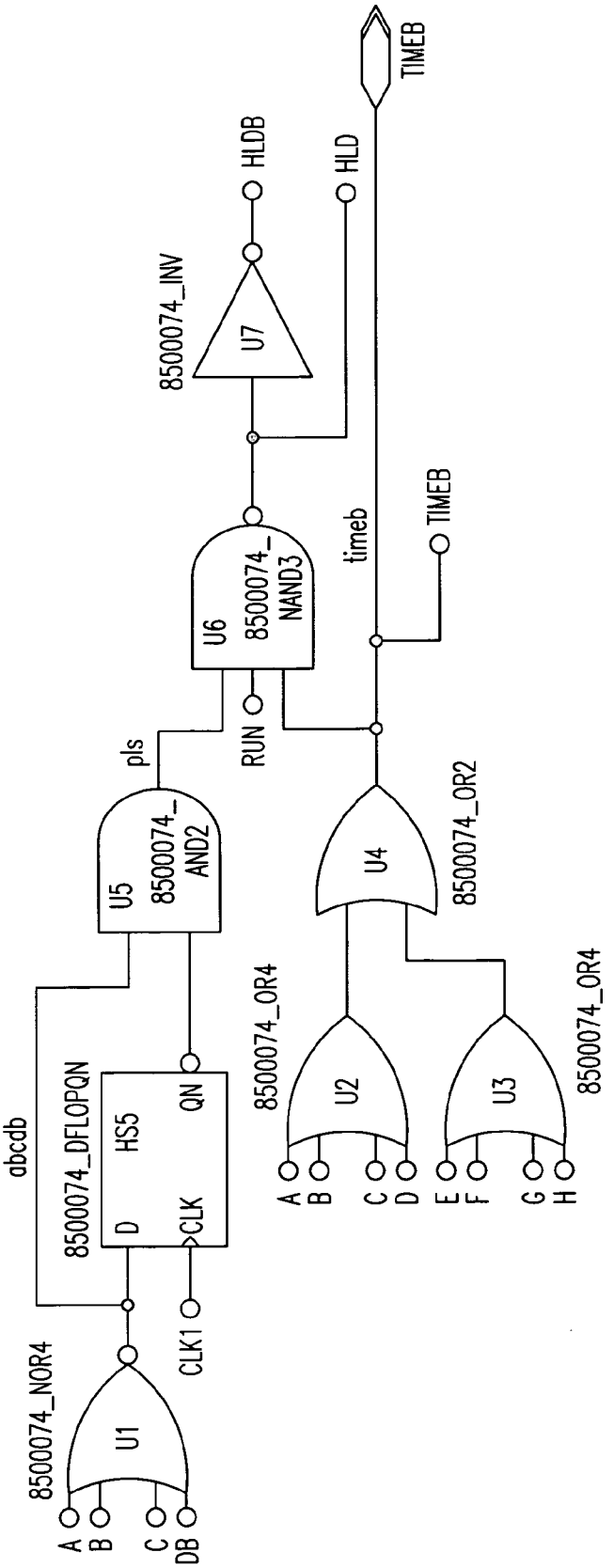

TIMEB
HLDB
HLD
8500074_INV
U7
timeb
TIMEB
U6
8500074_
NAND3
RUN
pls
U5
8500074_
AND2
U4
8500074_OR2
8500074_OR4
U2
8500074_OR4
U3
dbcdb
8500074_DFLOPQN
D
HS5
QN
CLK
CLK1
8500074_NOR4
U1
A
B
C
DB
A
B
C
D
E
F
G
H

FIG. 157D

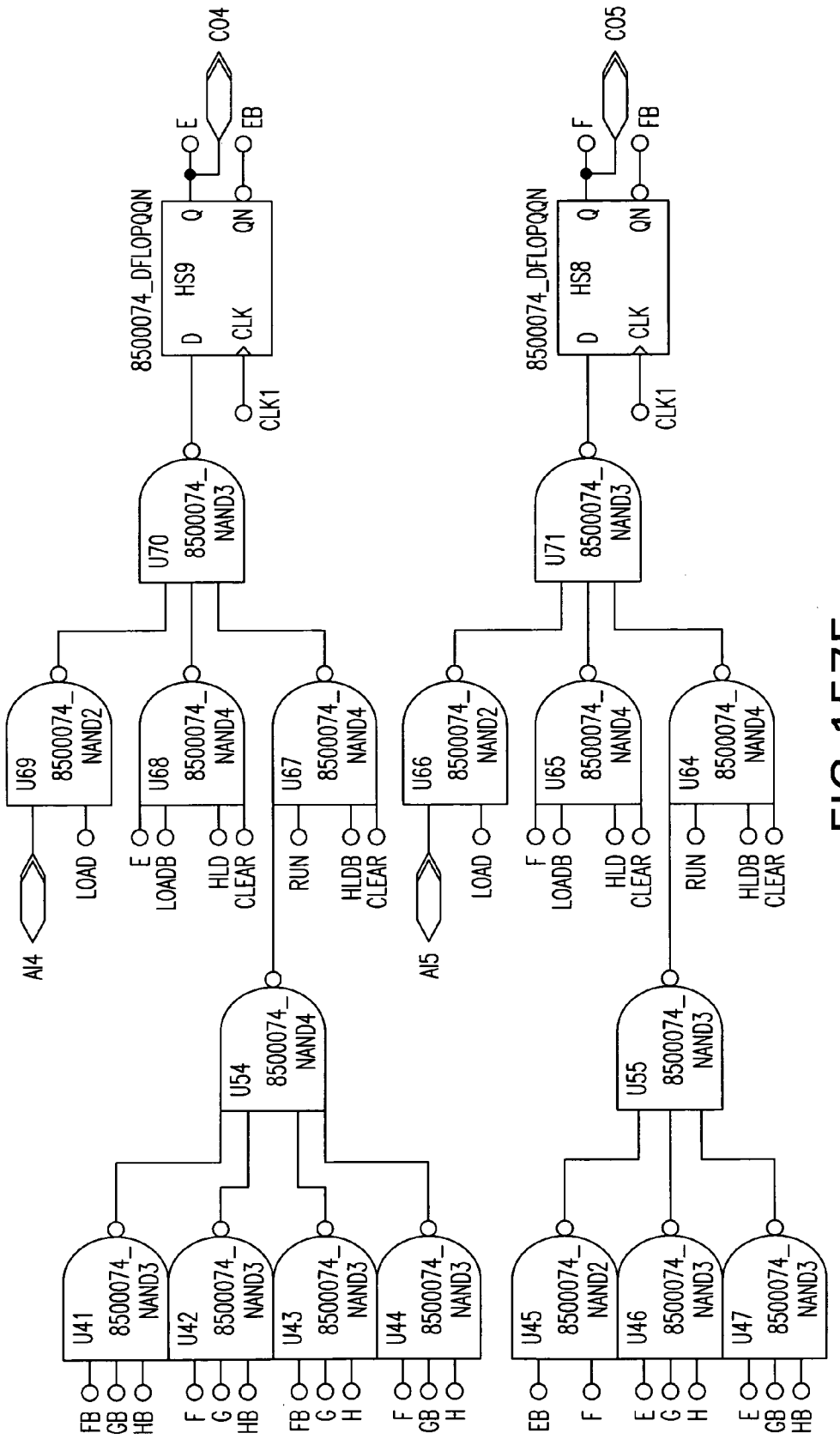

C04
E
EB
8500074_DFLOPQQN
D
HS9
CLK
Q
QN
CLK1
U70
8500074_
NAND3
U69
8500074_
NAND2
U68
8500074_
NAND4
U67
8500074_
NAND4
AI4
LOAD
E
LOADB
HLD
CLEAR
RUN
HLDB
CLEAR
U54
8500074_
NAND4
U41
8500074_
NAND3
U42
8500074_
NAND3
U43
8500074_
NAND3
U44
8500074_
NAND3
FB
GB
HB
F
G
HB
FB
G
H
F
GB
H
C05
F
FB
8500074_DFLOPQQN
D
HS8
CLK
Q
QN
CLK1
U71
8500074_
NAND3
U66
8500074_
NAND2
U65
8500074_
NAND4
U64
8500074_
NAND4
AI5
LOAD
F
LOADB
HLD
CLEAR
RUN
HLDB
CLEAR
U55
8500074_
NAND3
U45
8500074_
NAND2
U46
8500074_
NAND3
U47
8500074_
NAND3
EB
F
E
G
H
E
GB
HB

FIG.157E

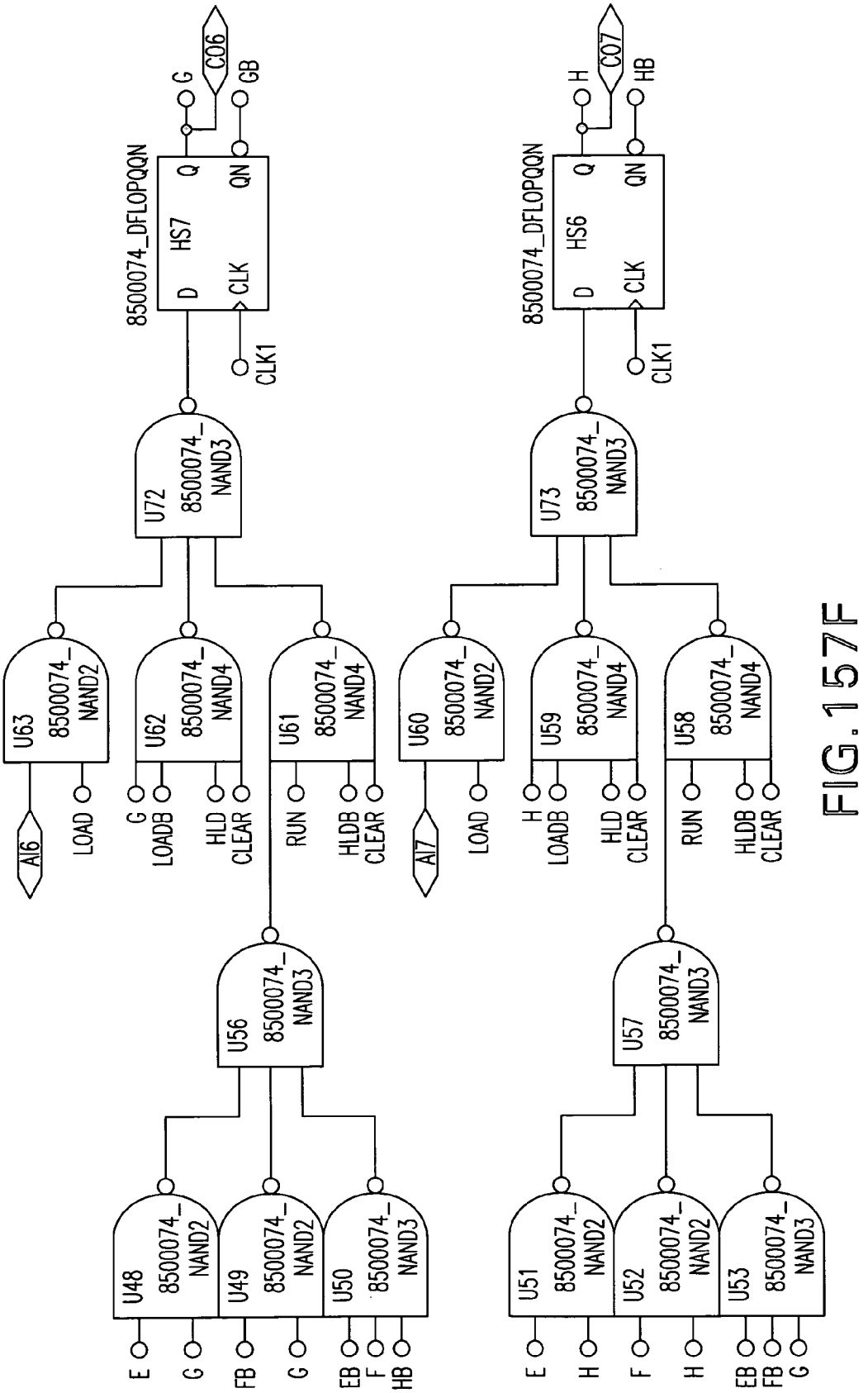

8500074_DFLOPQQN
HS7
D
CLK
Q
QN
G
GB
C06
CLK1
U72
8500074_NAND3
U63
8500074_NAND2
U62
8500074_NAND4
U61
8500074_NAND4
AI6
LOAD
G
LOADB
HLD
CLEAR
RUN
HLDB
CLEAR
U56
8500074_NAND3
U48
8500074_NAND2
U49
8500074_NAND2
U50
8500074_NAND3
E
G
FB
G
EB
F
HB
8500074_DFLOPQQN
HS6
D
CLK
Q
QN
H
HB
C07
CLK1
U73
8500074_NAND3
U60
8500074_NAND2
U59
8500074_NAND4
U58
8500074_NAND4
AI7
LOAD
H
LOADB
HLD
CLEAR
RUN
HLDB
CLEAR
U57
8500074_NAND3
U51
8500074_NAND2
U52
8500074_NAND2
U53
8500074_NAND3
E
H
F
H
EB
FB
G

FIG. 157F

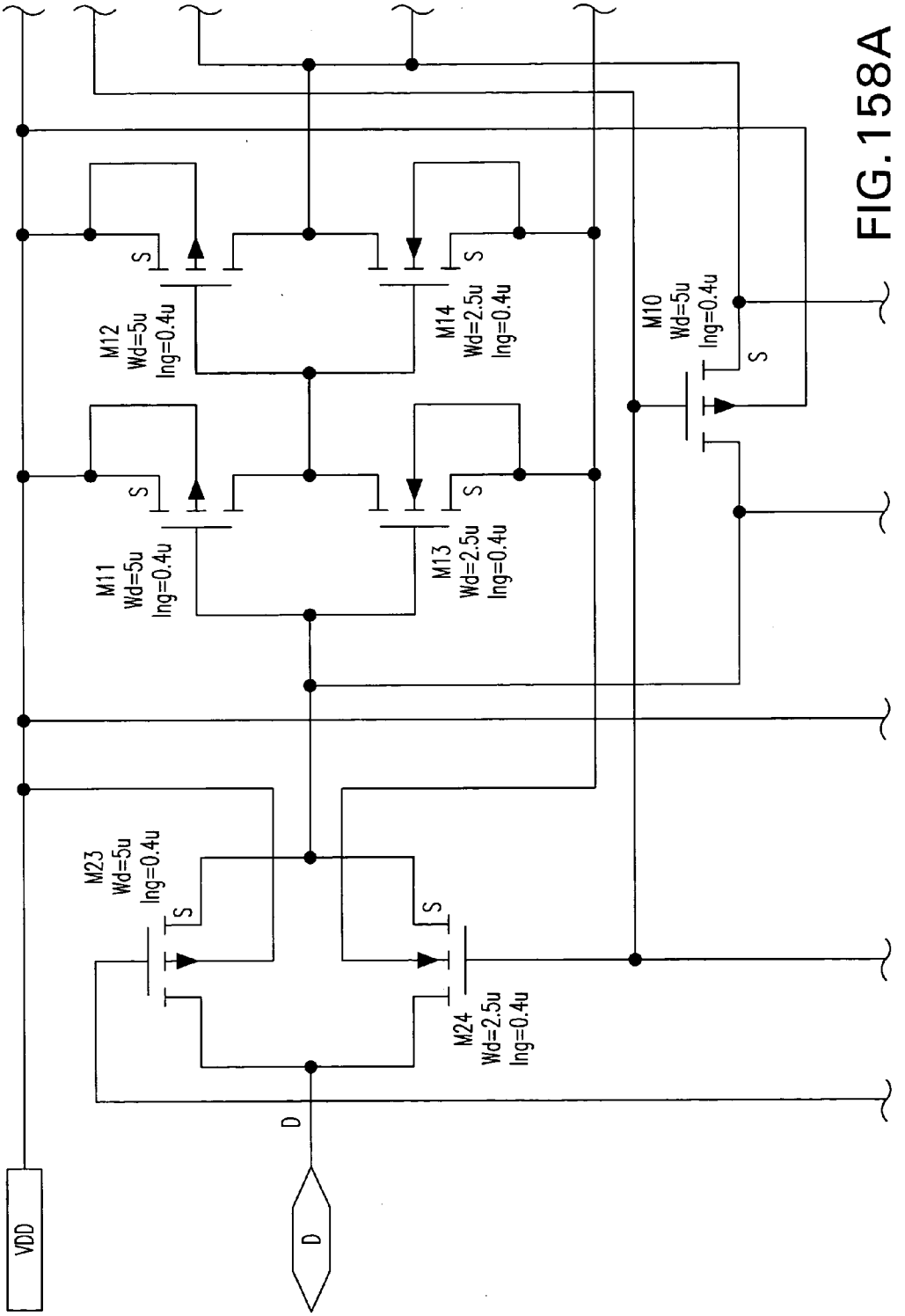

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.158A

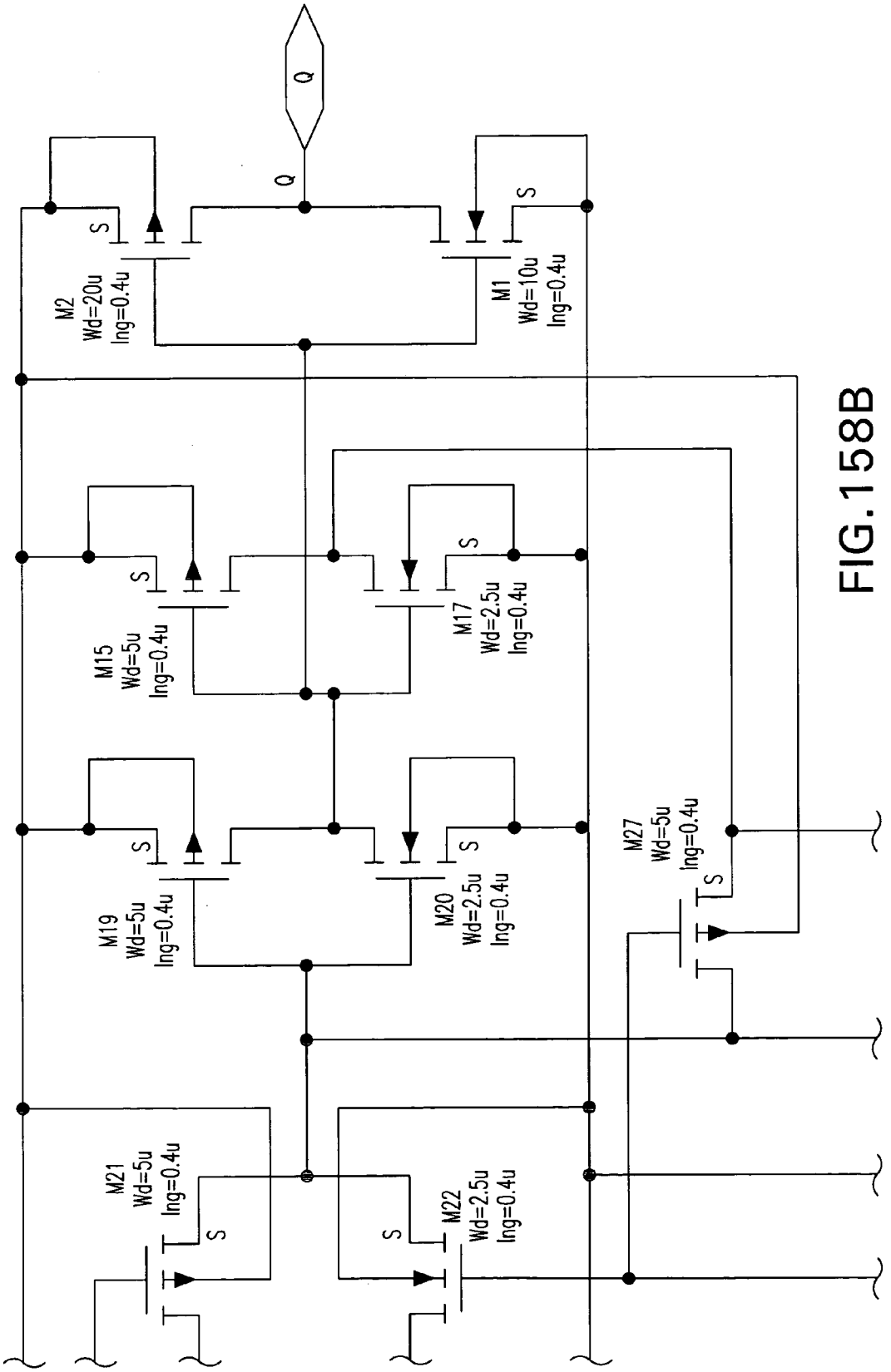

Q
Q
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u

FIG. 158B

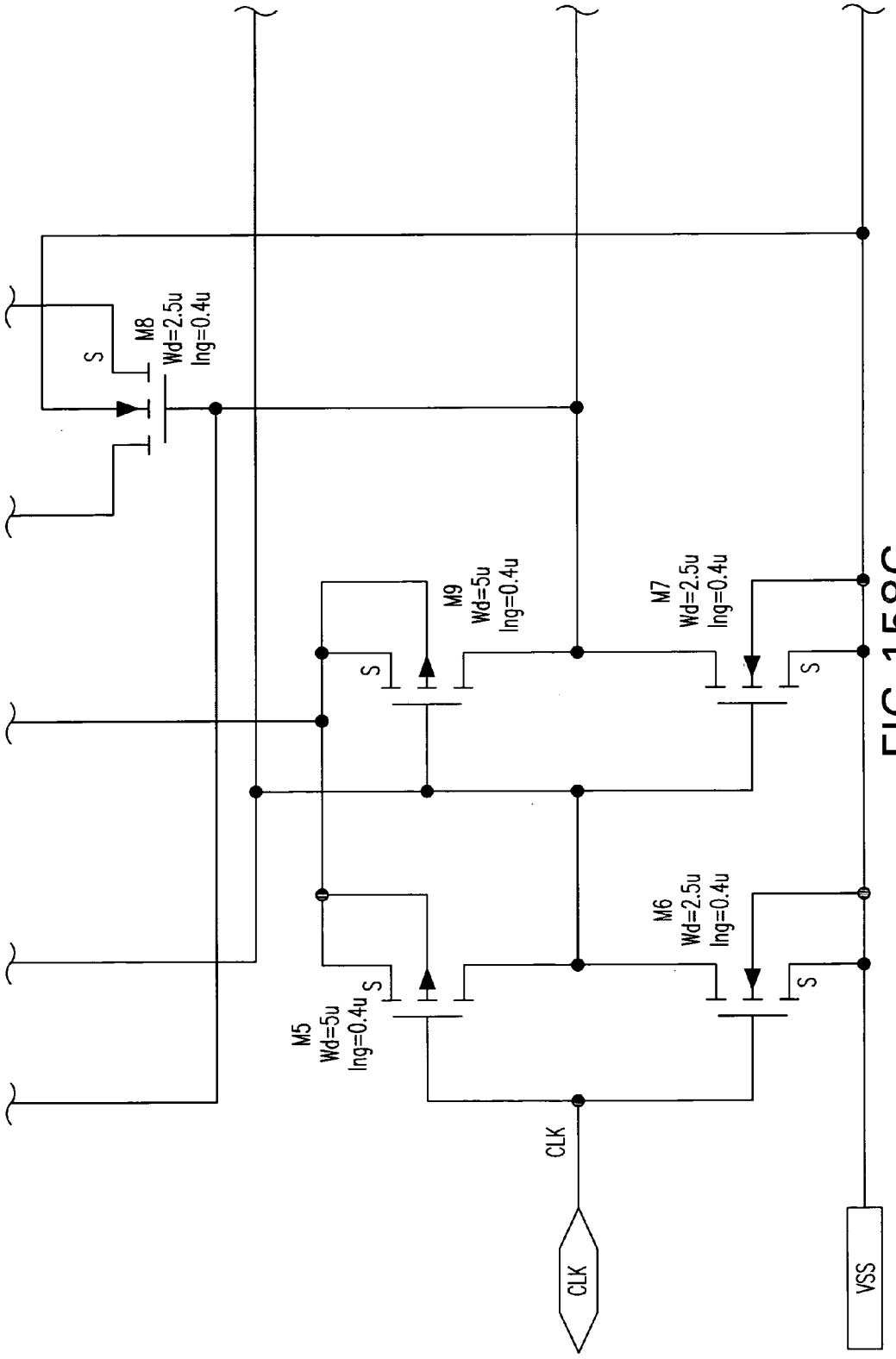

M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M5
Wd=5u
lng=0.4u
CLK
CLK
VSS

FIG. 158C

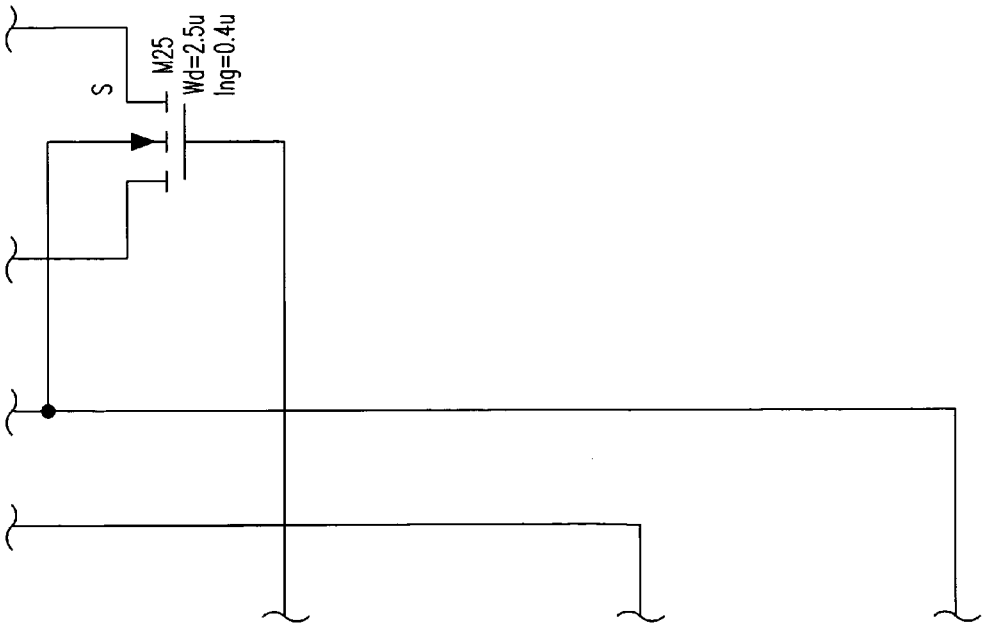


FIG.158D

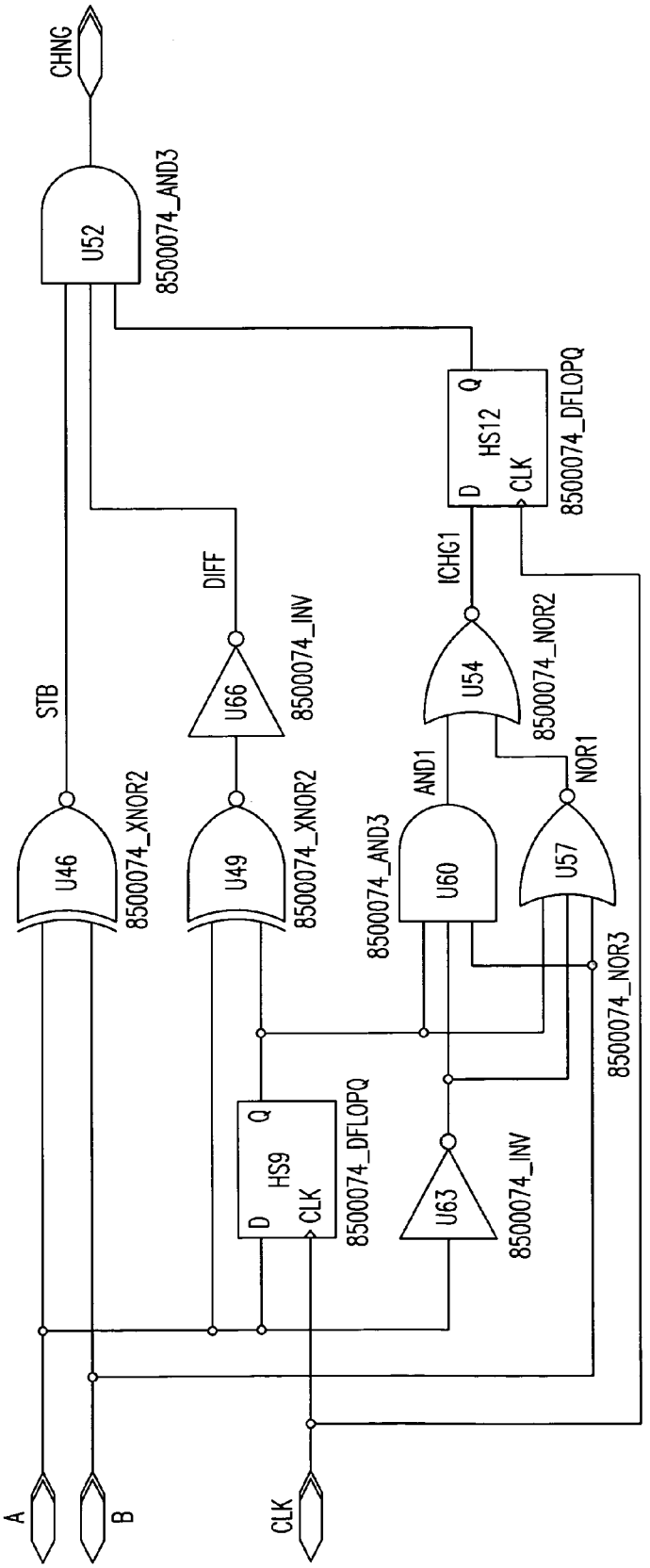

CHNG
U52
8500074_AND3
STB
U46
8500074_XNOR2
DIFF
U66
8500074_INV
U49
8500074_XNOR2
HS9
D
Q
CLK
8500074_DFLOPQ
U63
8500074_INV
AND1
8500074_AND3
U60
ICHG1
U54
8500074_NOR2
NOR1
U57
8500074_NOR3
HS12
D
Q
CLK
8500074_DFLOPQ
A
B
CLK

FIG. 159

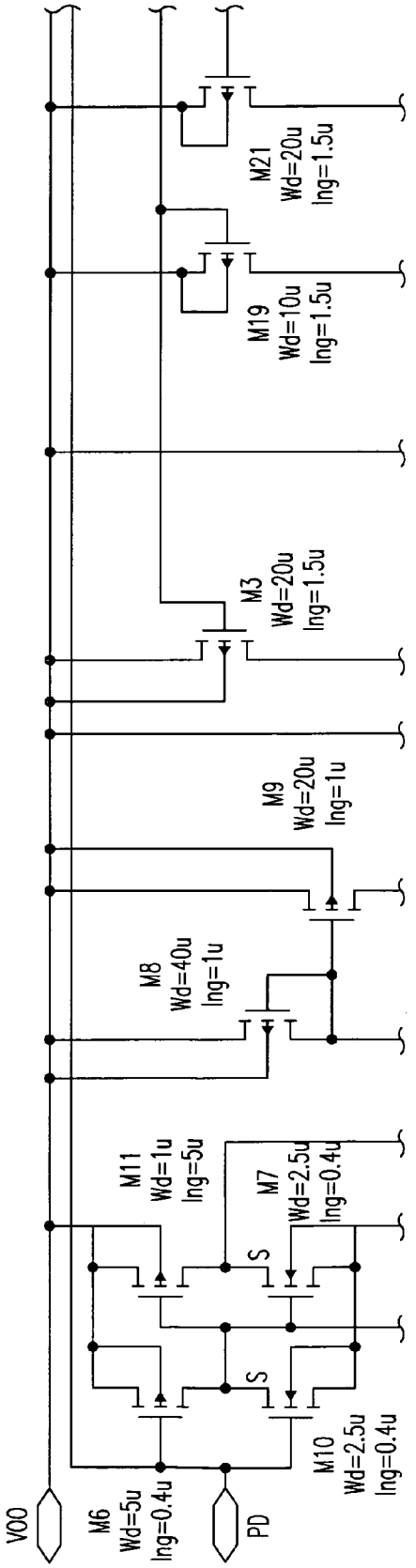

M21
Wd=20u
lng=1.5u
M19
Wd=10u
lng=1.5u
M3
Wd=20u
lng=1.5u
M9
Wd=20u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
M6
Wd=5u
lng=0.4u
VDD
PD

FIG.160A

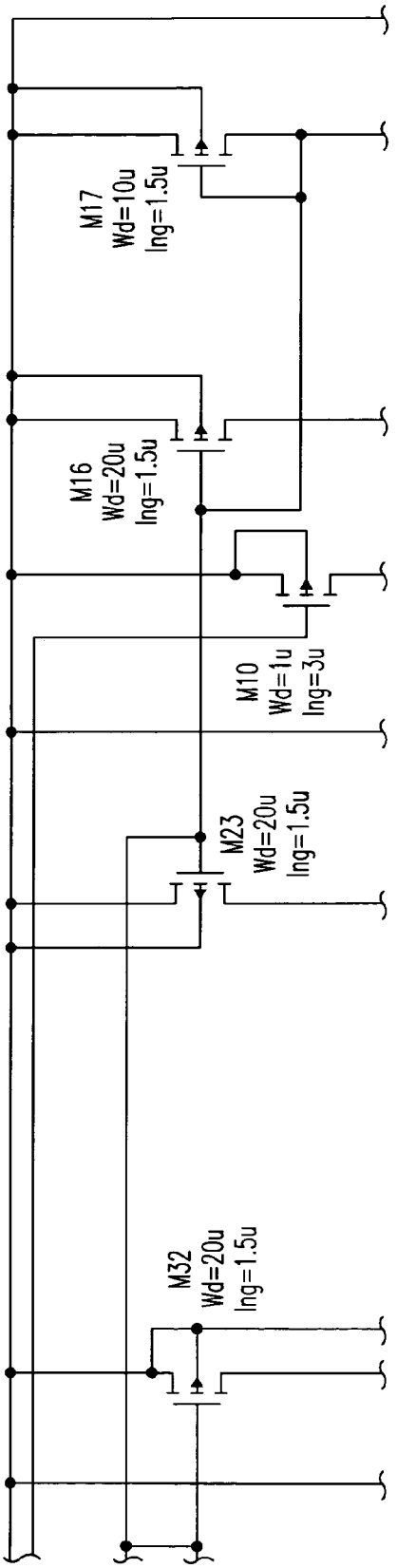

M17
Wd=10u
lng=1.5u
M16
Wd=20u
lng=1.5u
M10
Wd=1u
lng=3u
M23
Wd=20u
lng=1.5u
M32
Wd=20u
lng=1.5u

FIG. 160B

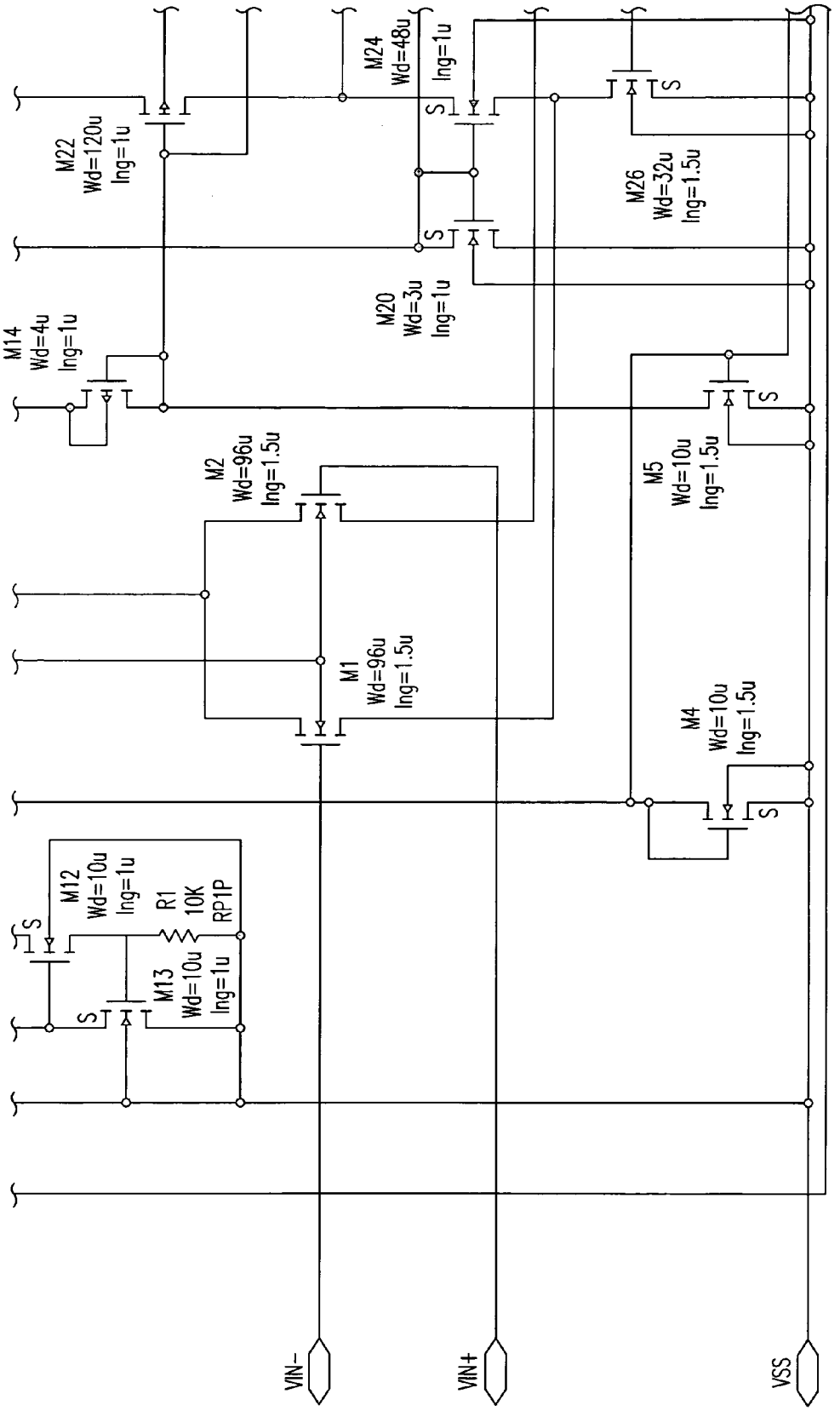

M24
Wd=48u
lng=1u
M22
Wd=120u
lng=1u
M26
Wd=32u
lng=1.5u
M20
Wd=3u
lng=1u
M14
Wd=4u
lng=1u
M2
Wd=96u
lng=1.5u
M5
Wd=10u
lng=1.5u
M1
Wd=96u
lng=1.5u
M4
Wd=10u
lng=1.5u
M12
Wd=10u
lng=1u
R1
10K
RP1P
M13
Wd=10u
lng=1u
S
VIN-
VIN+
VSS

FIG. 160C

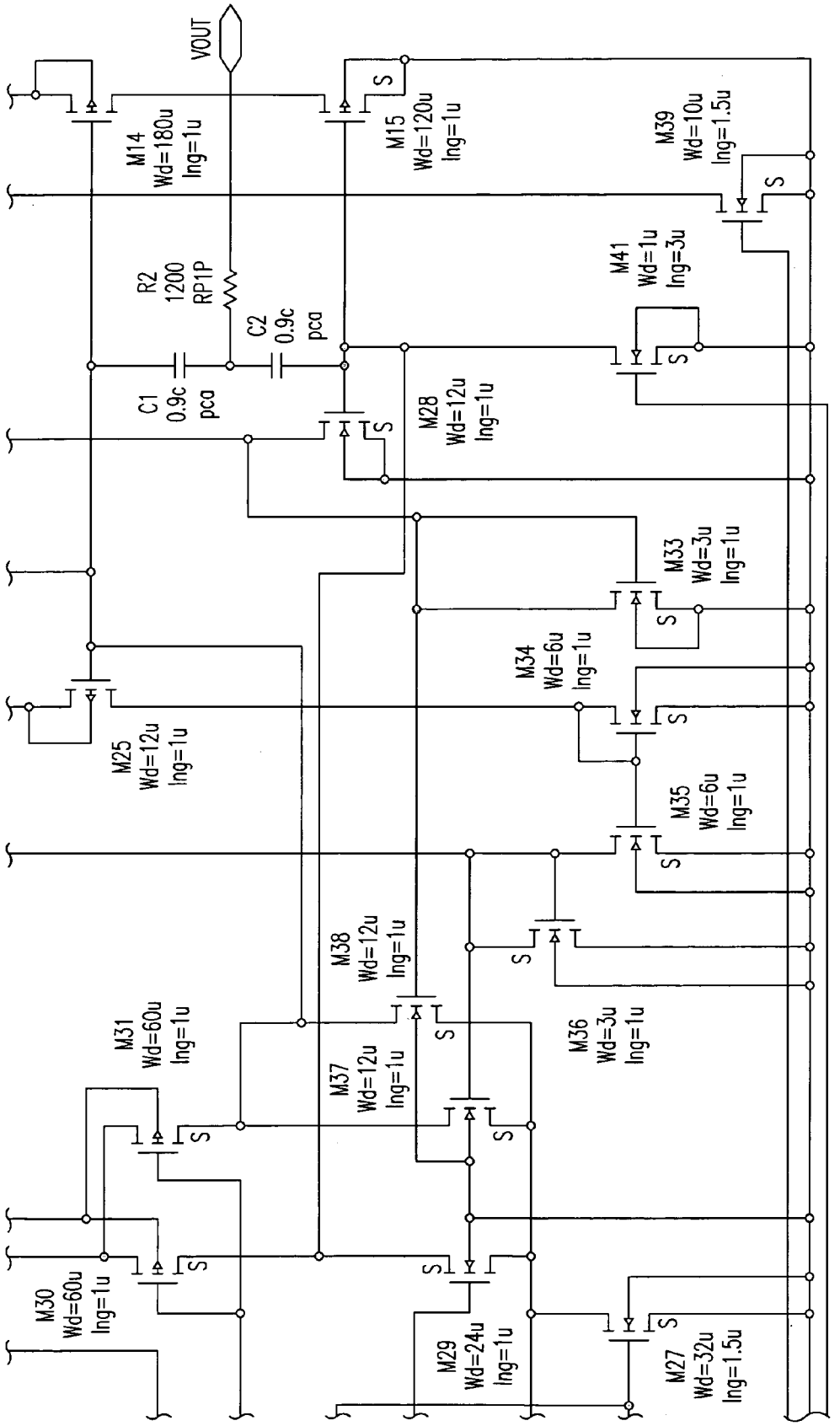

VOUT
M14 Wd=180u lng=1u
M15 Wd=120u lng=1u
M39 Wd=10u lng=1.5u
R2 1200 RP1P
C2 0.9c pca
C1 0.9c pca
M41 Wd=1u lng=3u
M28 Wd=12u lng=1u
M33 Wd=3u lng=1u
M34 Wd=6u lng=1u
M25 Wd=12u lng=1u
M35 Wd=6u lng=1u
M38 Wd=12u lng=1u
M31 Wd=60u lng=1u
M36 Wd=3u lng=1u
M37 Wd=12u lng=1u
M30 Wd=60u lng=1u
M29 Wd=24u lng=1u
M27 Wd=32u lng=1.5u

FIG. 160D

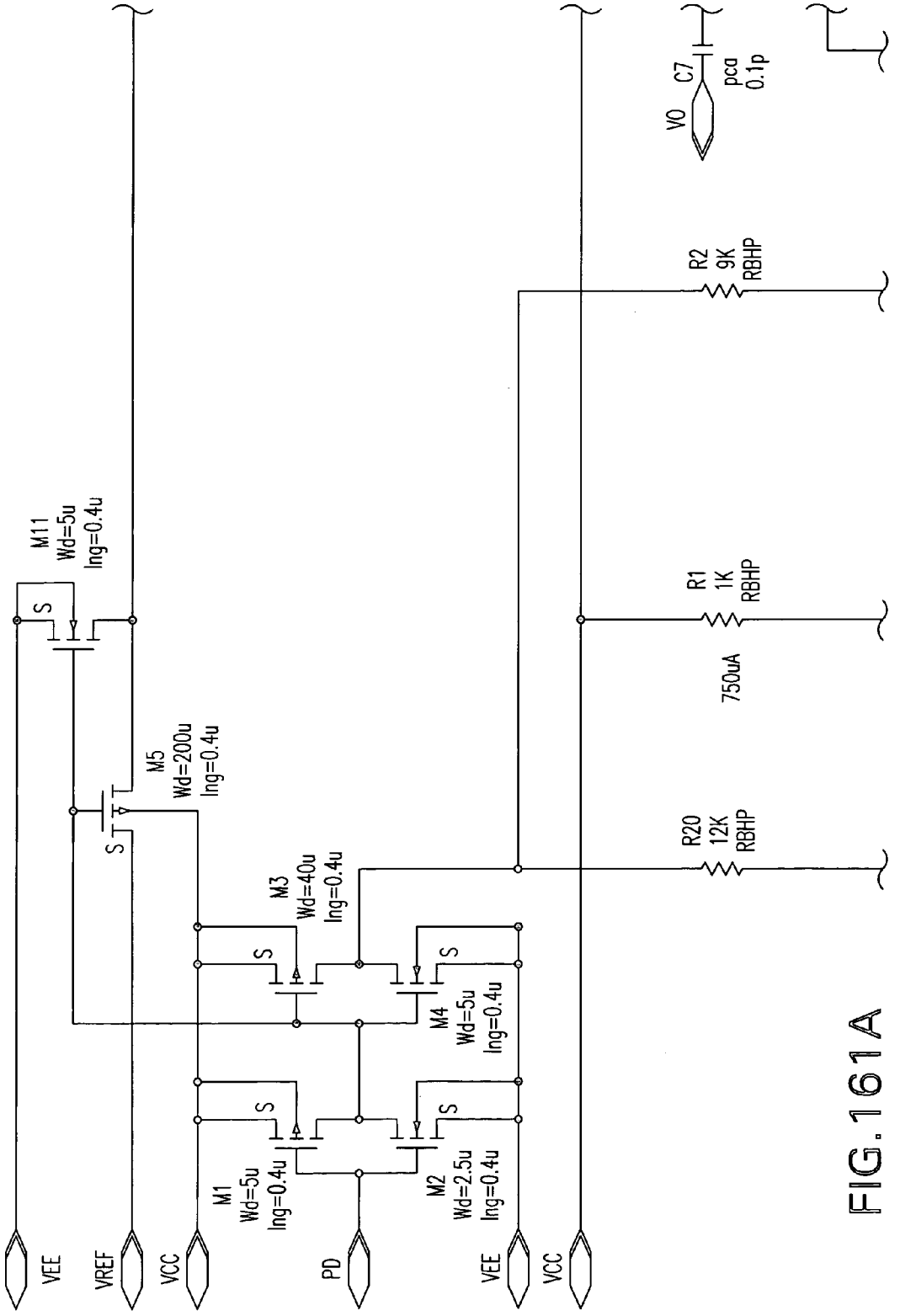

VEE
VREF
VCC
PD
VEE
VCC
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
M3
Wd=40u
lng=0.4u
M4
Wd=5u
lng=0.4u
M5
Wd=200u
lng=0.4u
M11
Wd=5u
lng=0.4u
S
R20
12K
RBHP
R1
1K
RBHP
750uA
R2
9K
RBHP
V0
C7
pca
0.1p

FIG. 161A

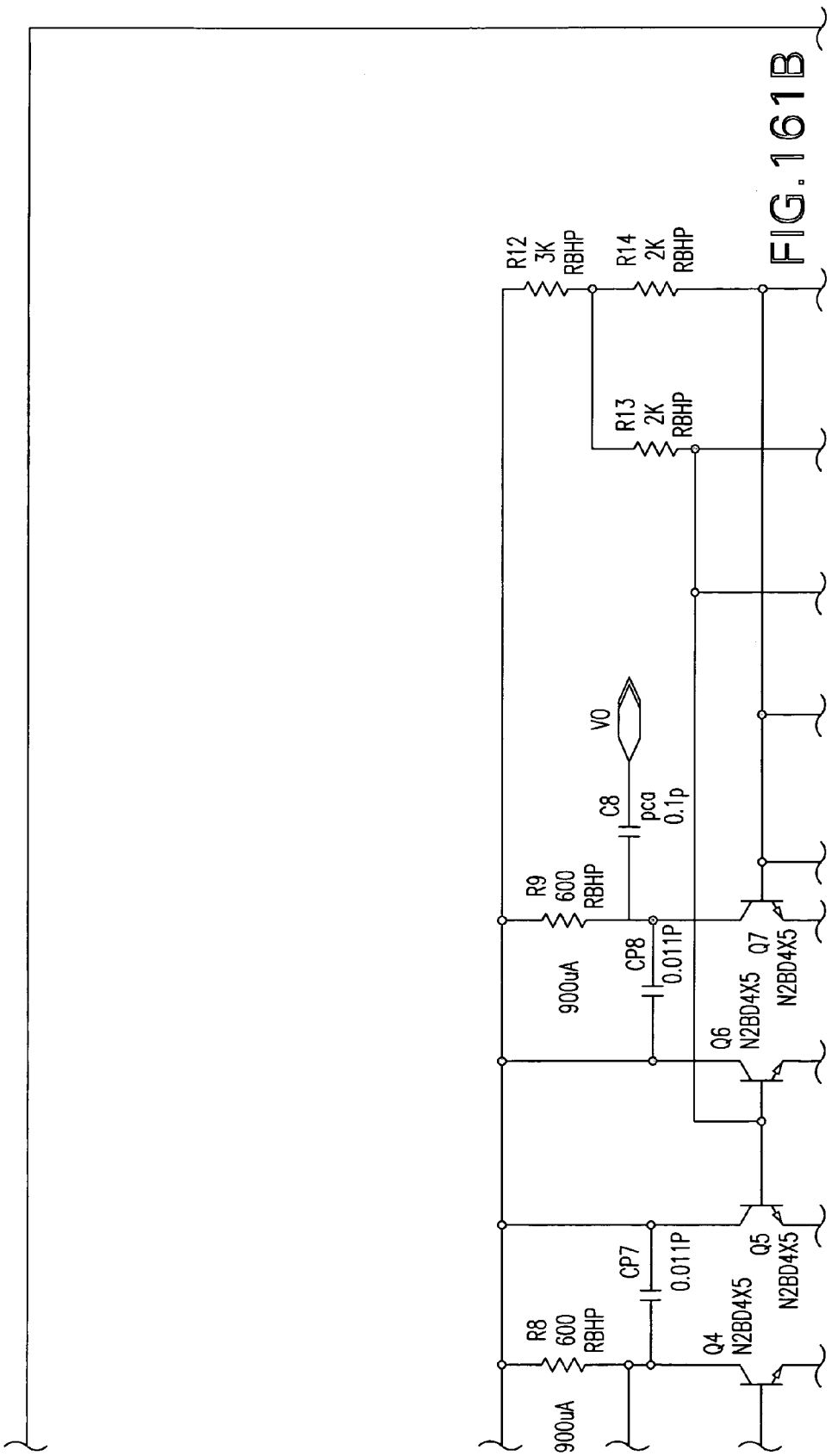

R12
3K
RBHP
R14
2K
RBHP
R13
2K
RBHP
VO
C8
pca
0.1p
R9
600
RBHP
900uA
CP8
0.011P
Q7
N2BD4X5
Q6
N2BD4X5
CP7
0.011P
Q5
N2BD4X5
R8
600
RBHP
900uA
Q4
N2BD4X5

FIG. 161B

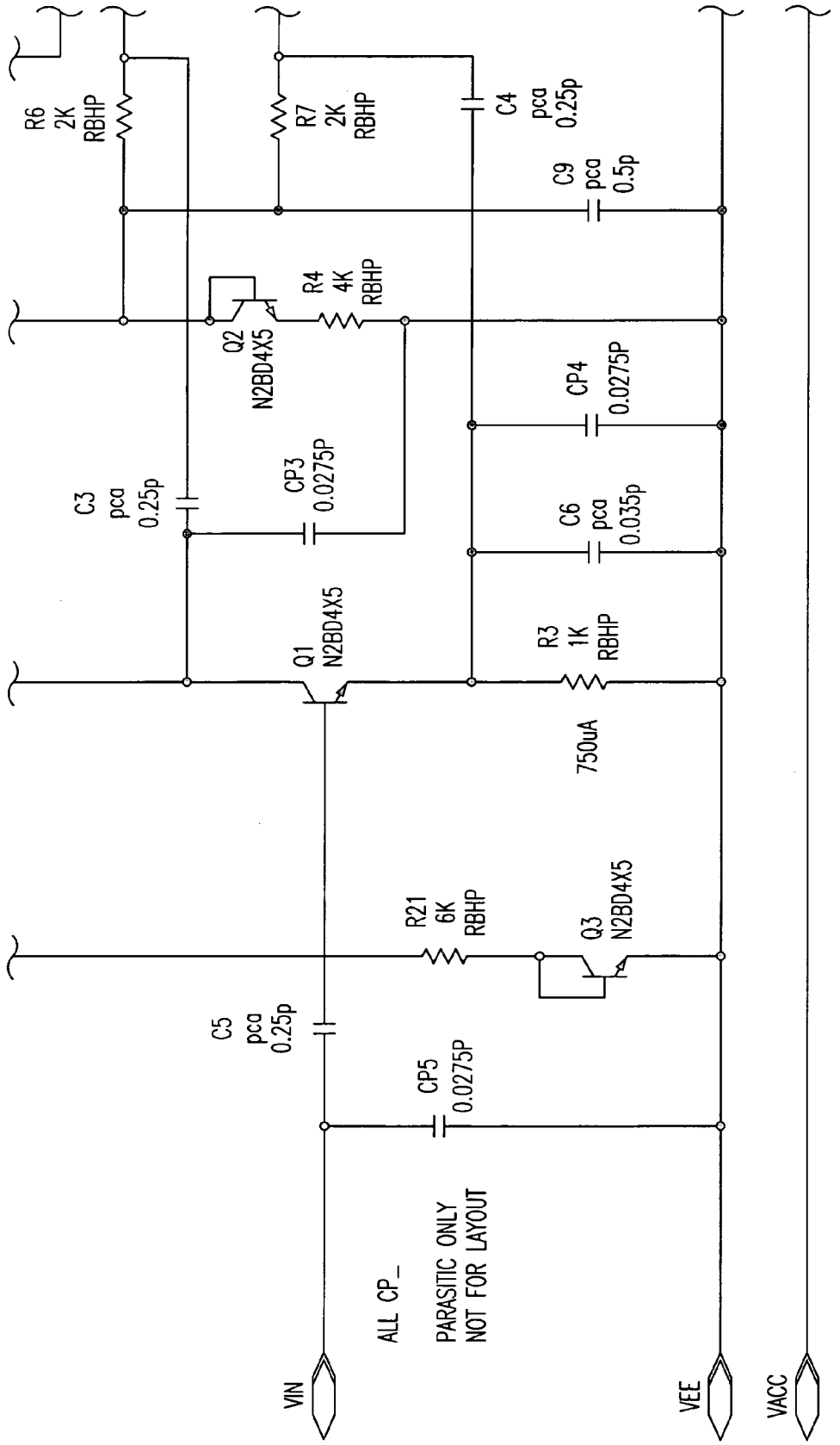

R6
2K
RBHP
R7
2K
RBHP
C4
pca
0.25p
C9
pca
0.5p
R4
4K
RBHP
Q2
N2BD4X5
CP4
0.0275P
C3
pca
0.25p
CP3
0.0275P
C6
pca
0.035p
Q1
N2BD4X5
R3
1K
RBHP
750uA
R21
6K
RBHP
Q3
N2BD4X5
C5
pca
0.25p
CP5
0.0275P
ALL CP_
PARASITIC ONLY
NOT FOR LAYOUT
VIN
VEE
VACC

FIG. 161C

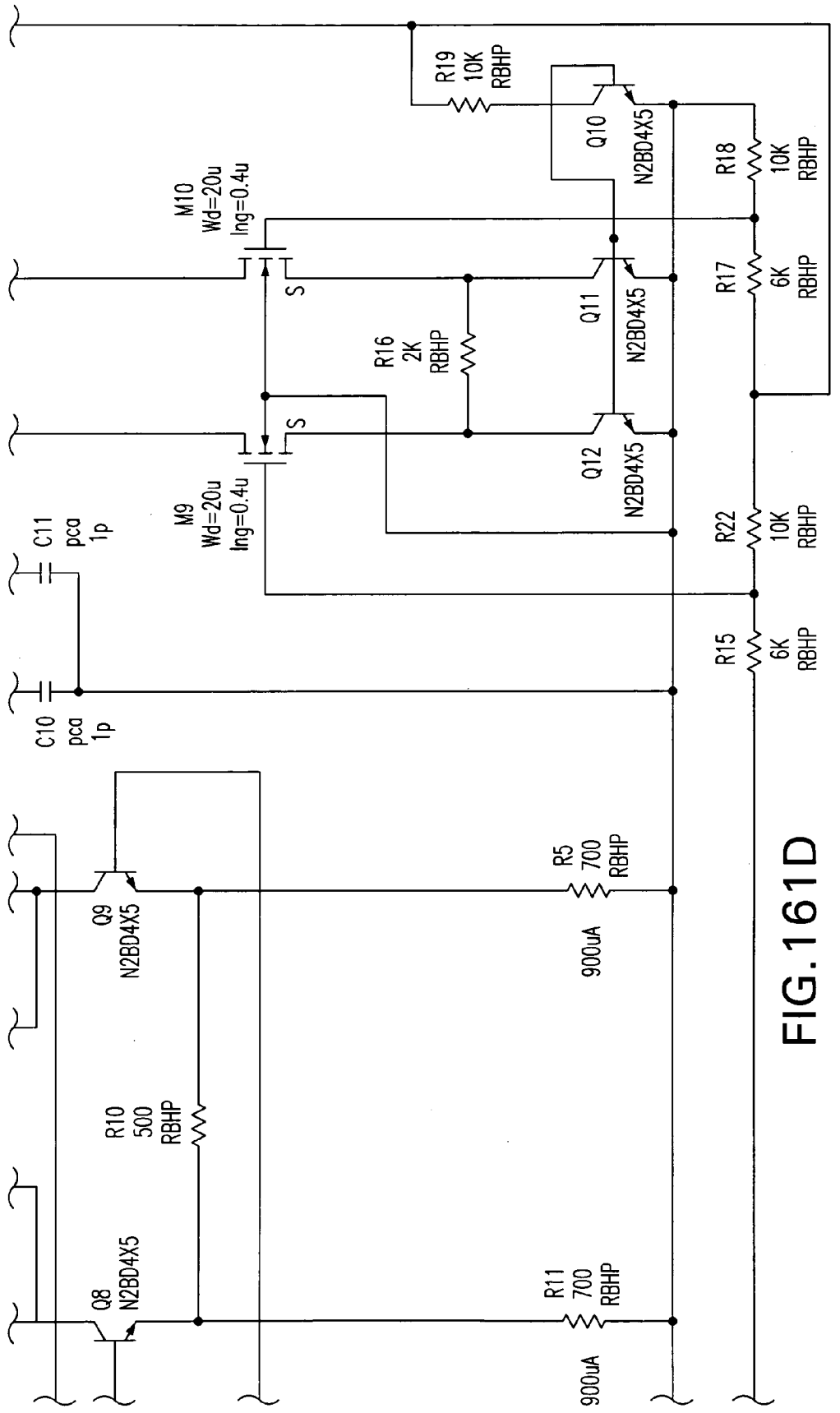

R19
10K
RBHP
Q10
N2BD4X5
R18
10K
RBHP
M10
Wd=20u
lng=0.4u
S
R17
6K
RBHP
Q11
N2BD4X5
R16
2K
RBHP
S
Q12
N2BD4X5
M9
Wd=20u
lng=0.4u
C11
pca
1p
R22
10K
RBHP
R15
6K
RBHP
C10
pca
1p
R5
700
RBHP
Q9
N2BD4X5
900uA
R10
500
RBHP
Q8
N2BD4X5
R11
700
RBHP
900uA

FIG.161D

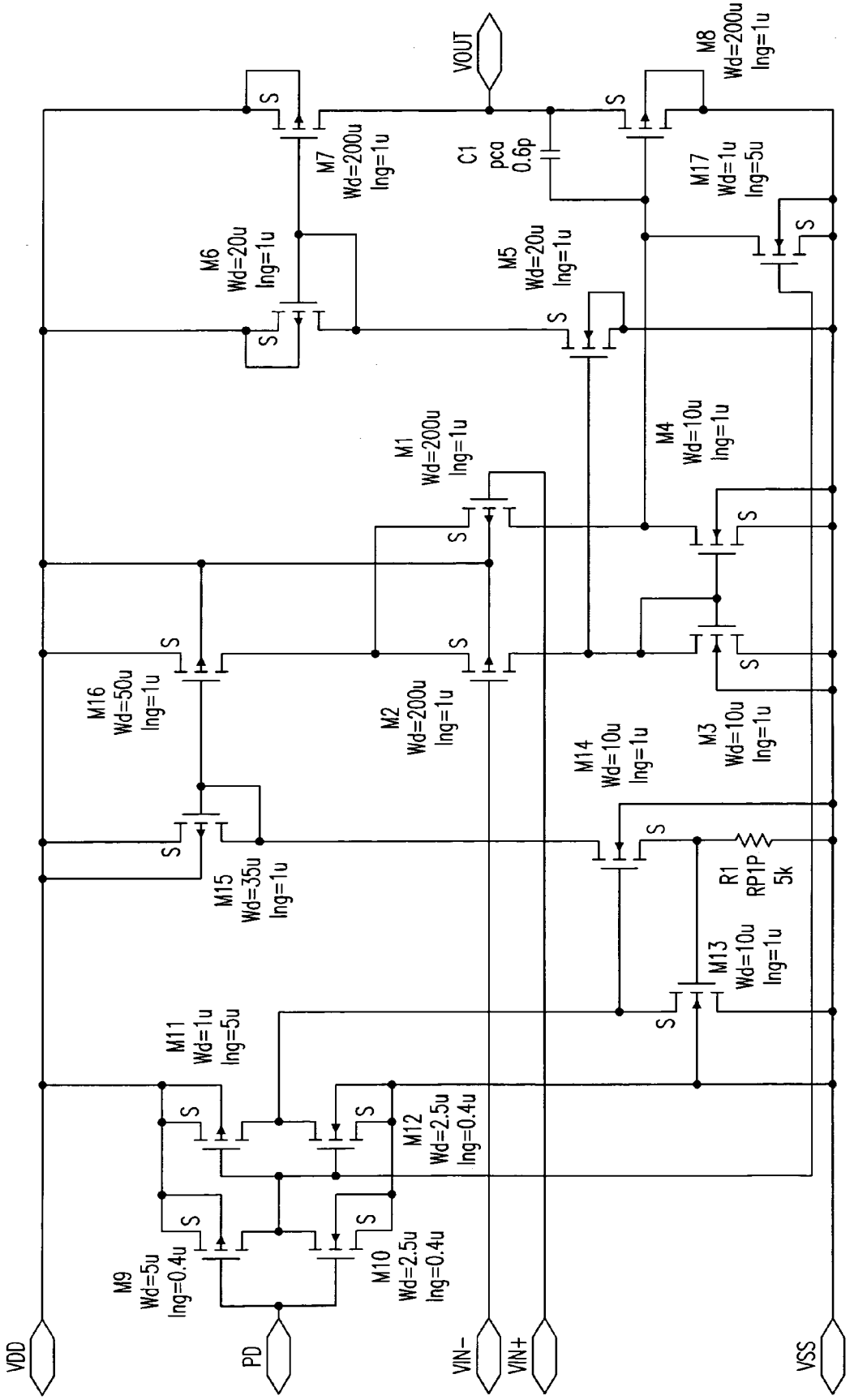

VOUT
M8 Wd=200u lng=1u
M7 Wd=200u lng=1u
C1 pca 0.6p
M17 Wd=1u lng=5u
M6 Wd=20u lng=1u
M5 Wd=20u lng=1u
M1 Wd=200u lng=1u
M4 Wd=10u lng=1u
M16 Wd=50u lng=1u
M2 Wd=200u lng=1u
M3 Wd=10u lng=1u
M14 Wd=10u lng=1u
M15 Wd=35u lng=1u
R1 RP1P 5k
M13 Wd=10u lng=1u
M11 Wd=1u lng=5u
M12 Wd=2.5u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG. 162

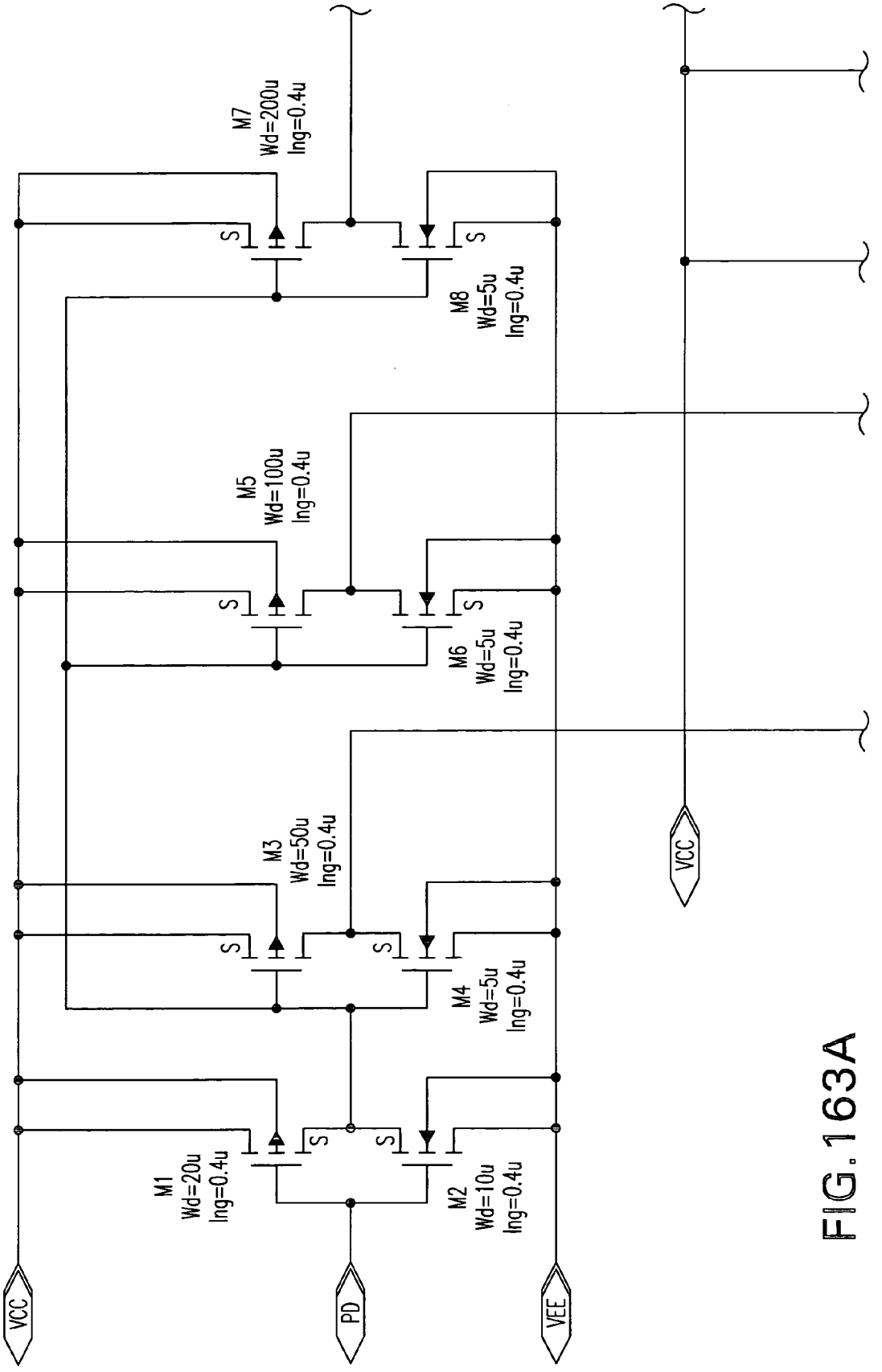
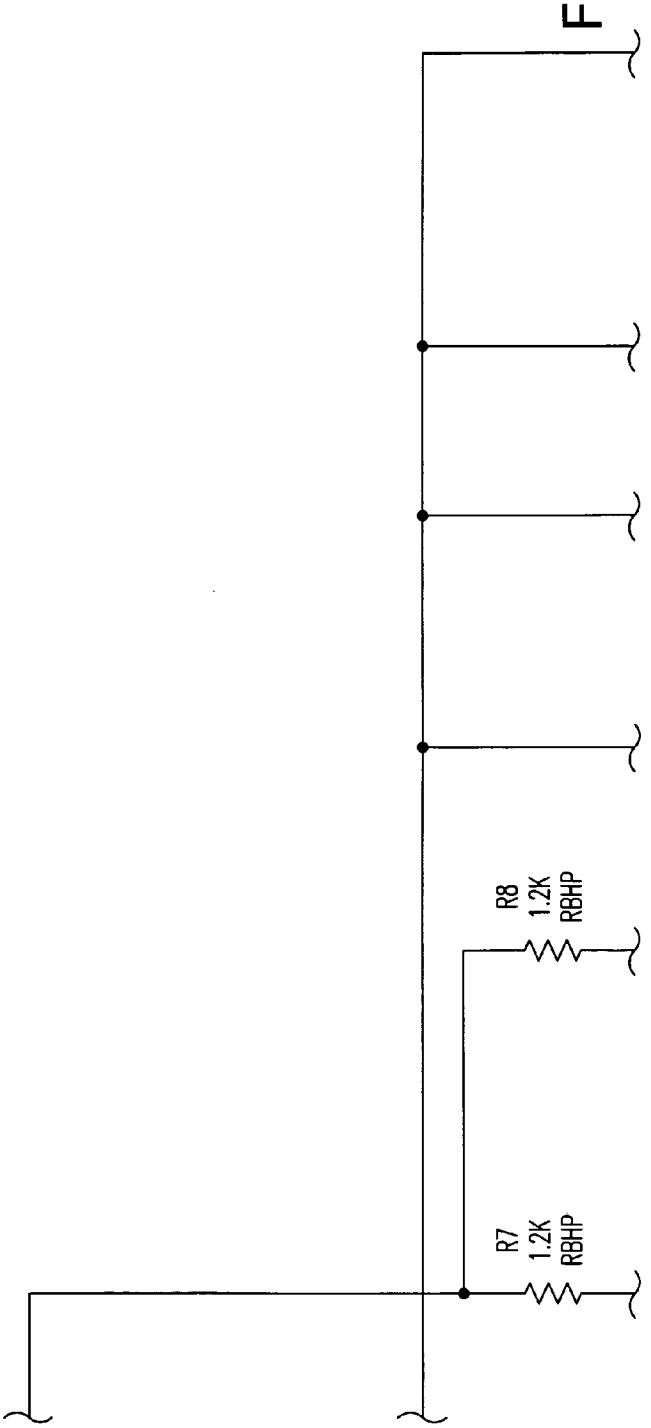

M7
Wd=200u
lng=0.4u
M8
Wd=5u
lng=0.4u
M5
Wd=100u
lng=0.4u
M6
Wd=5u
lng=0.4u
M3
Wd=50u
lng=0.4u
M4
Wd=5u
lng=0.4u
M1
Wd=20u
lng=0.4u
M2
Wd=10u
lng=0.4u
S
VCC
PD
VEE
VCC

FIG. 163A

FIG.163B



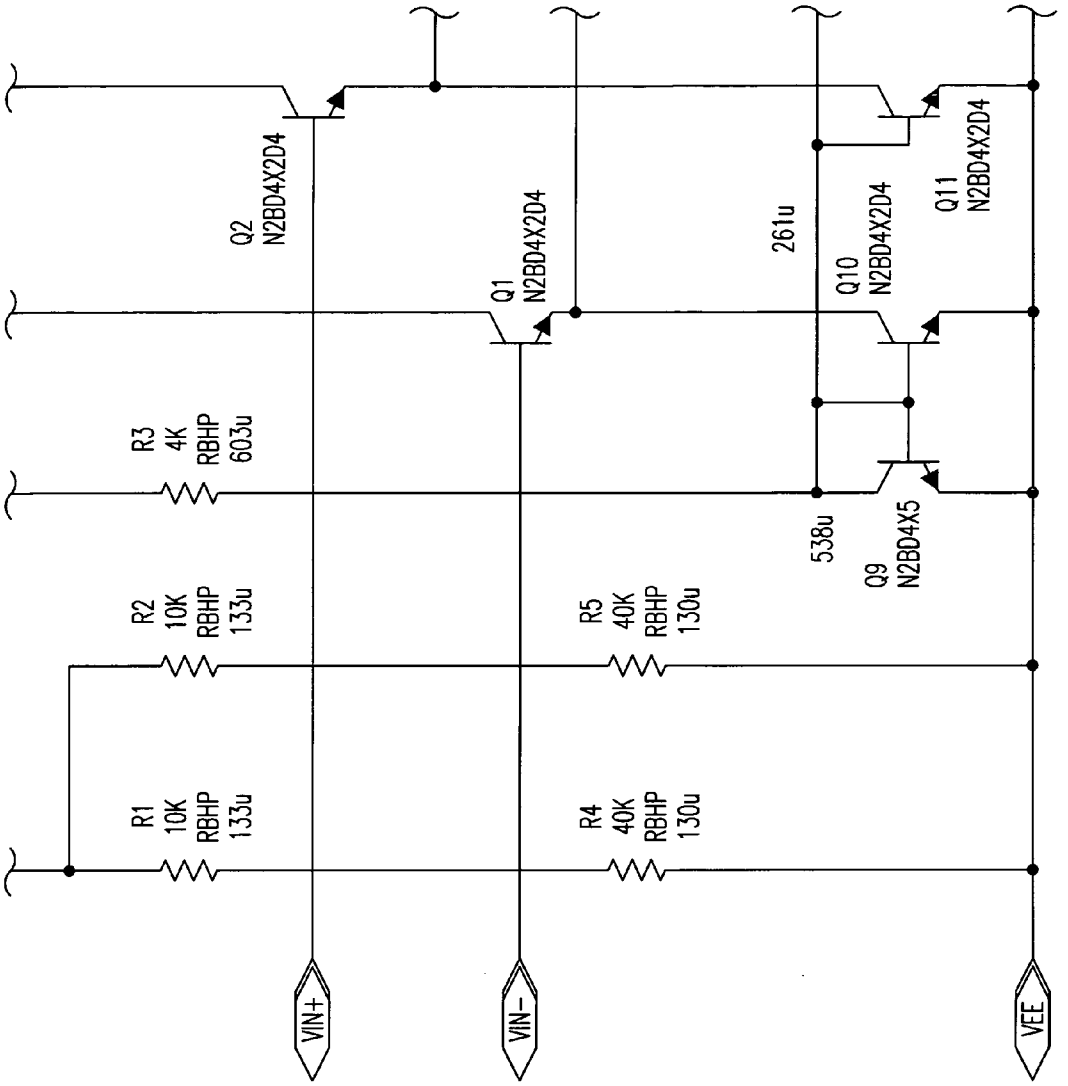

Q2
N2BD4X2D4
Q1
N2BD4X2D4
261u
Q10
N2BD4X2D4
Q11
N2BD4X2D4
R3
4K
RBHP
603u
538u
Q9
N2BD4X5
R2
10K
RBHP
133u
R5
40K
RBHP
130u
R1
10K
RBHP
133u
R4
40K
RBHP
130u
VIN+
VIN-
VEE

FIG.163C

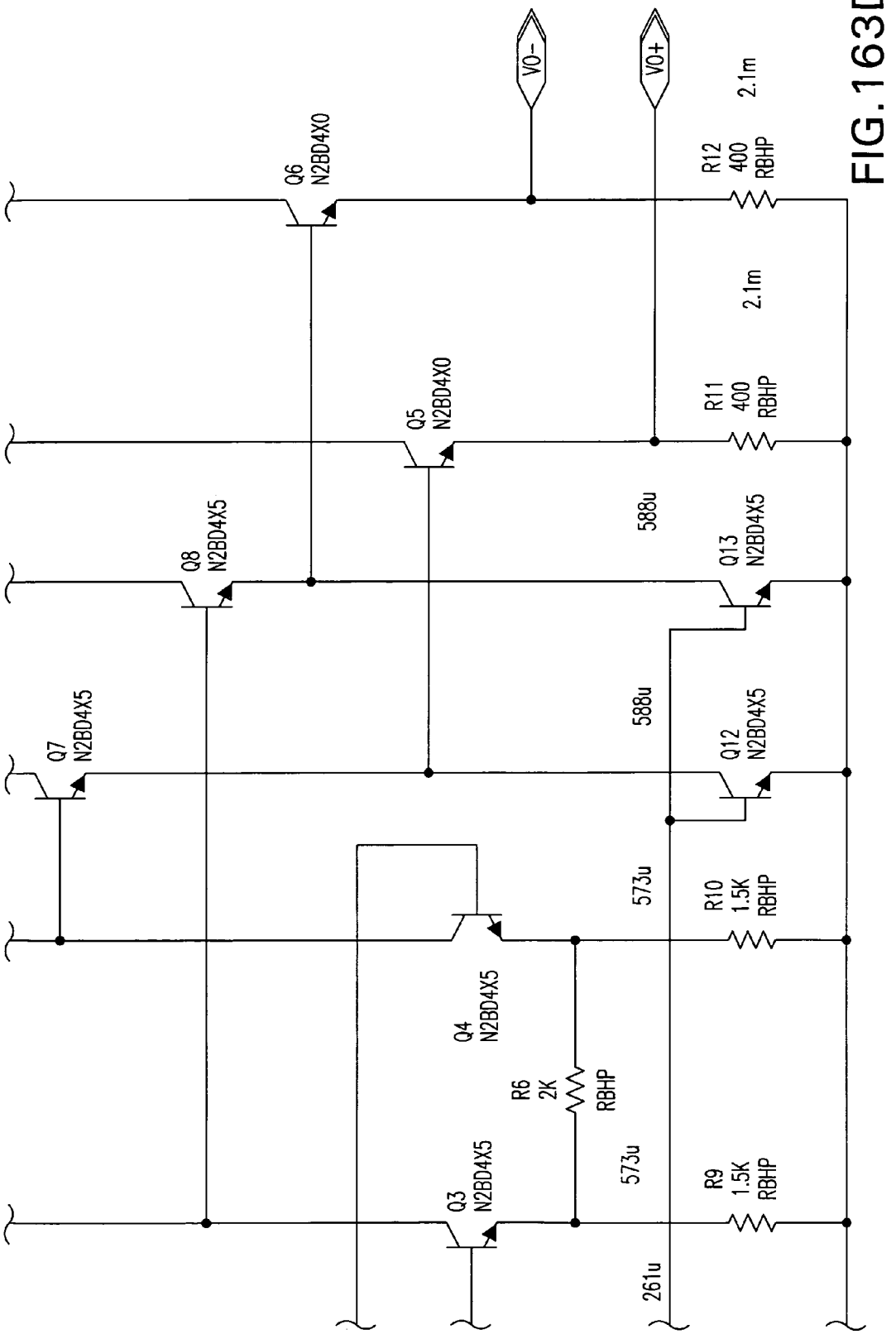

VO-
VO+
Q6 N2BD4X0
Q5 N2BD4X0
Q8 N2BD4X5
Q7 N2BD4X5
Q4 N2BD4X5
Q3 N2BD4X5
Q13 N2BD4X5
Q12 N2BD4X5
R12 400 RBHP 2.1m
R11 400 RBHP 2.1m
R10 1.5K RBHP
R9 1.5K RBHP
R6 2K RBHP
588u
588u
573u
573u
261u

FIG.163D

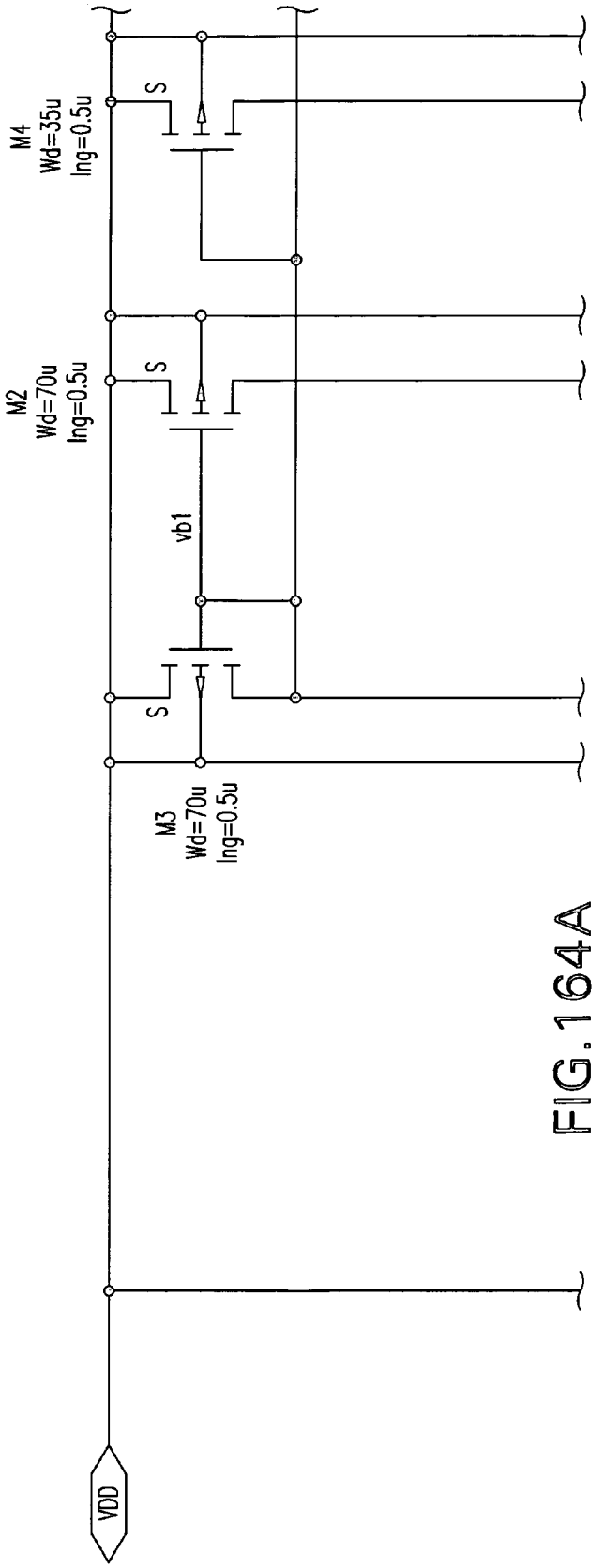


FIG. 164A

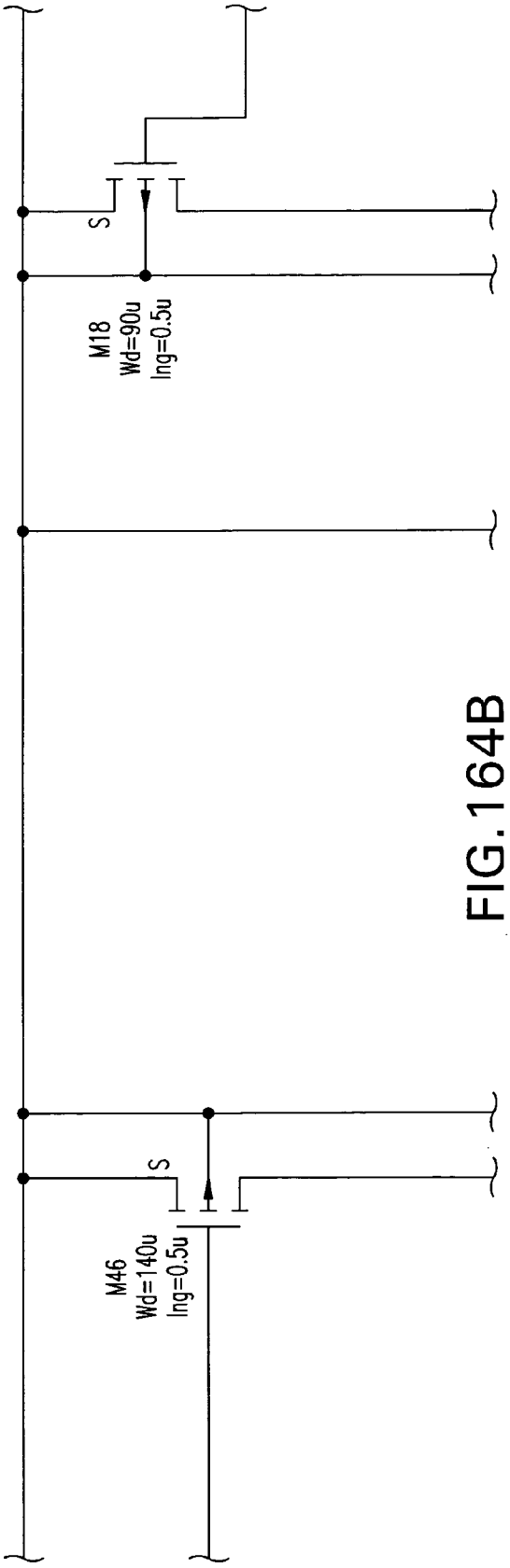


FIG. 164B

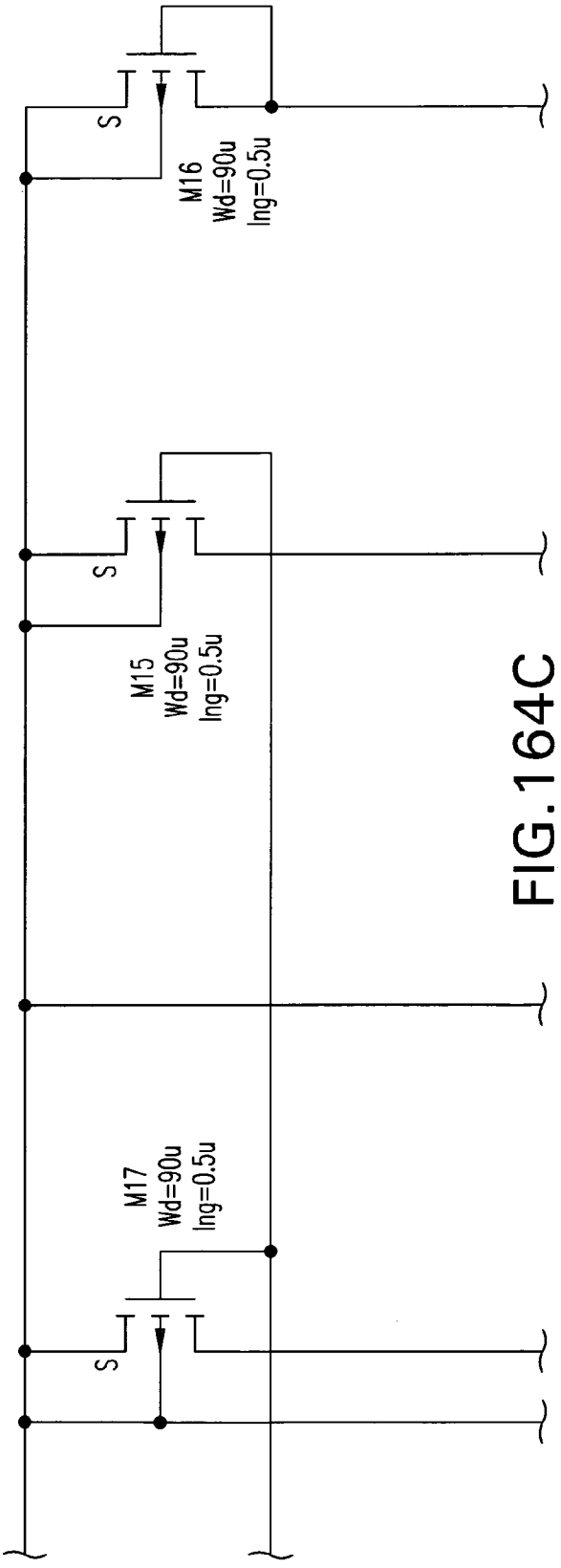


FIG.164C

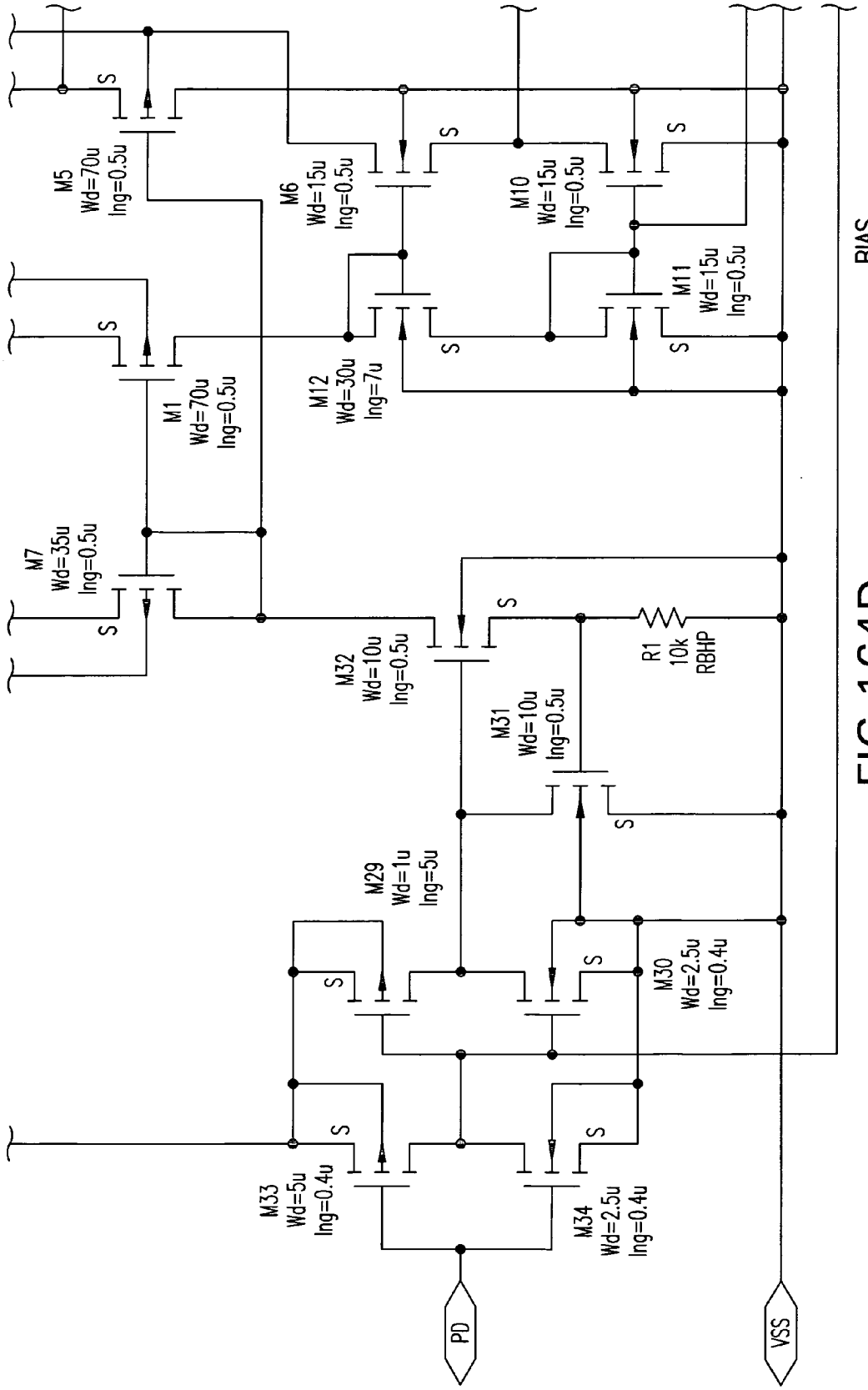

M5
Wd=70u
lng=0.5u
M6
Wd=15u
lng=0.5u
M10
Wd=15u
lng=0.5u
M11
Wd=15u
lng=0.5u
BIAS
M1
Wd=70u
lng=0.5u
M12
Wd=30u
lng=7u
M7
Wd=35u
lng=0.5u
M32
Wd=10u
lng=0.5u
R1
10k
RBHP
M31
Wd=10u
lng=0.5u
M29
Wd=1u
lng=5u
M30
Wd=2.5u
lng=0.4u
M33
Wd=5u
lng=0.4u
M34
Wd=2.5u
lng=0.4u
PD
VSS

FIG.164D

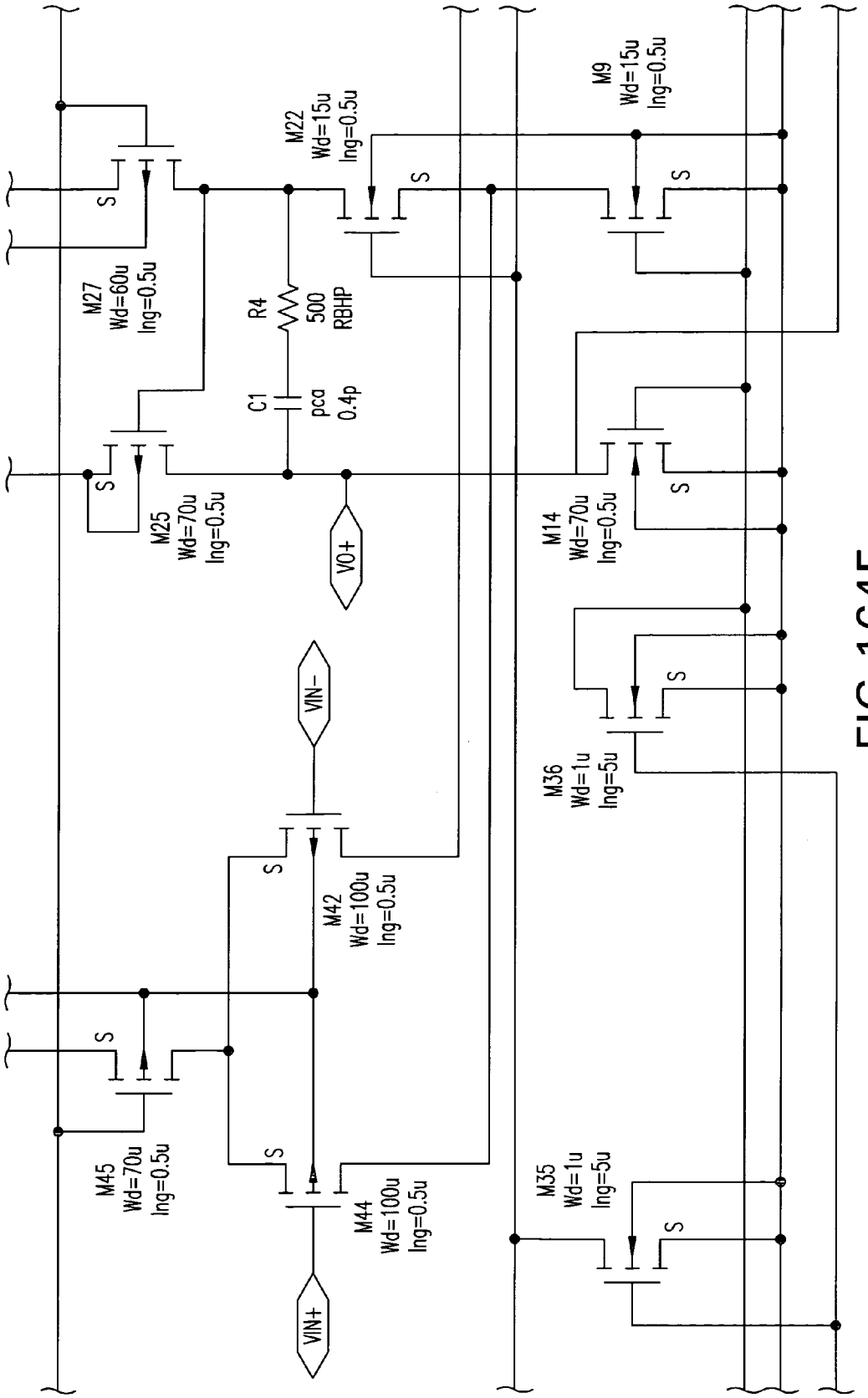

M22
Wd=15u
lng=0.5u
M9
Wd=15u
lng=0.5u
M27
Wd=60u
lng=0.5u
R4
500
RBHP
C1
pca
0.4p
M25
Wd=70u
lng=0.5u
VO+
M14
Wd=70u
lng=0.5u
VIN-
M36
Wd=1u
lng=5u
M42
Wd=100u
lng=0.5u
M45
Wd=70u
lng=0.5u
M44
Wd=100u
lng=0.5u
M35
Wd=1u
lng=5u
VIN+
S

FIG.164E

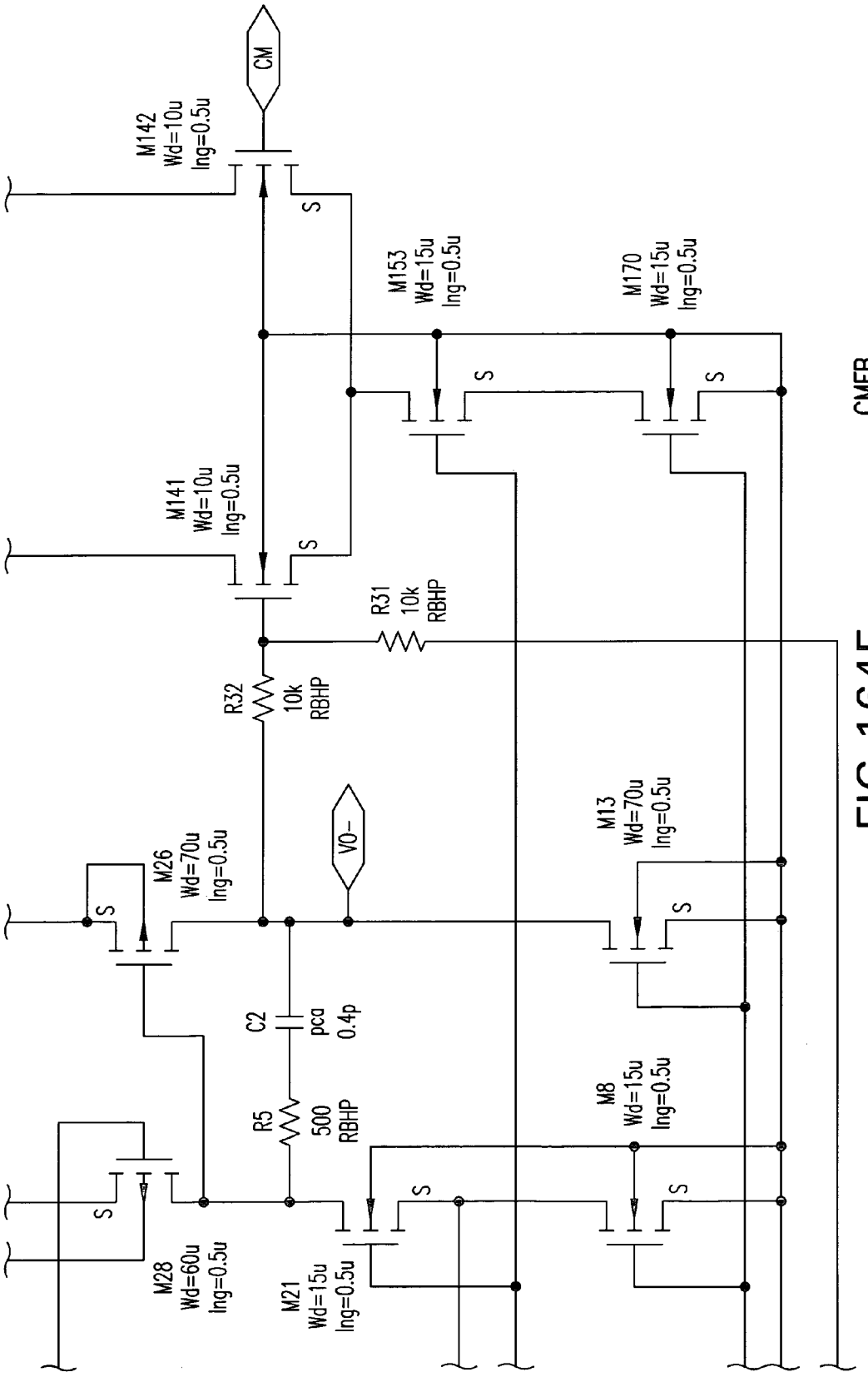

CM
M142
Wd=10u
lng=0.5u
M153
Wd=15u
lng=0.5u
M170
Wd=15u
lng=0.5u
CMFB
M141
Wd=10u
lng=0.5u
R31
10k
RBHP
R32
10k
RBHP
VO-
M26
Wd=70u
lng=0.5u
M13
Wd=70u
lng=0.5u
C2
pca
0.4p
R5
500
RBHP
M8
Wd=15u
lng=0.5u
M28
Wd=60u
lng=0.5u
M21
Wd=15u
lng=0.5u
S

FIG.164F

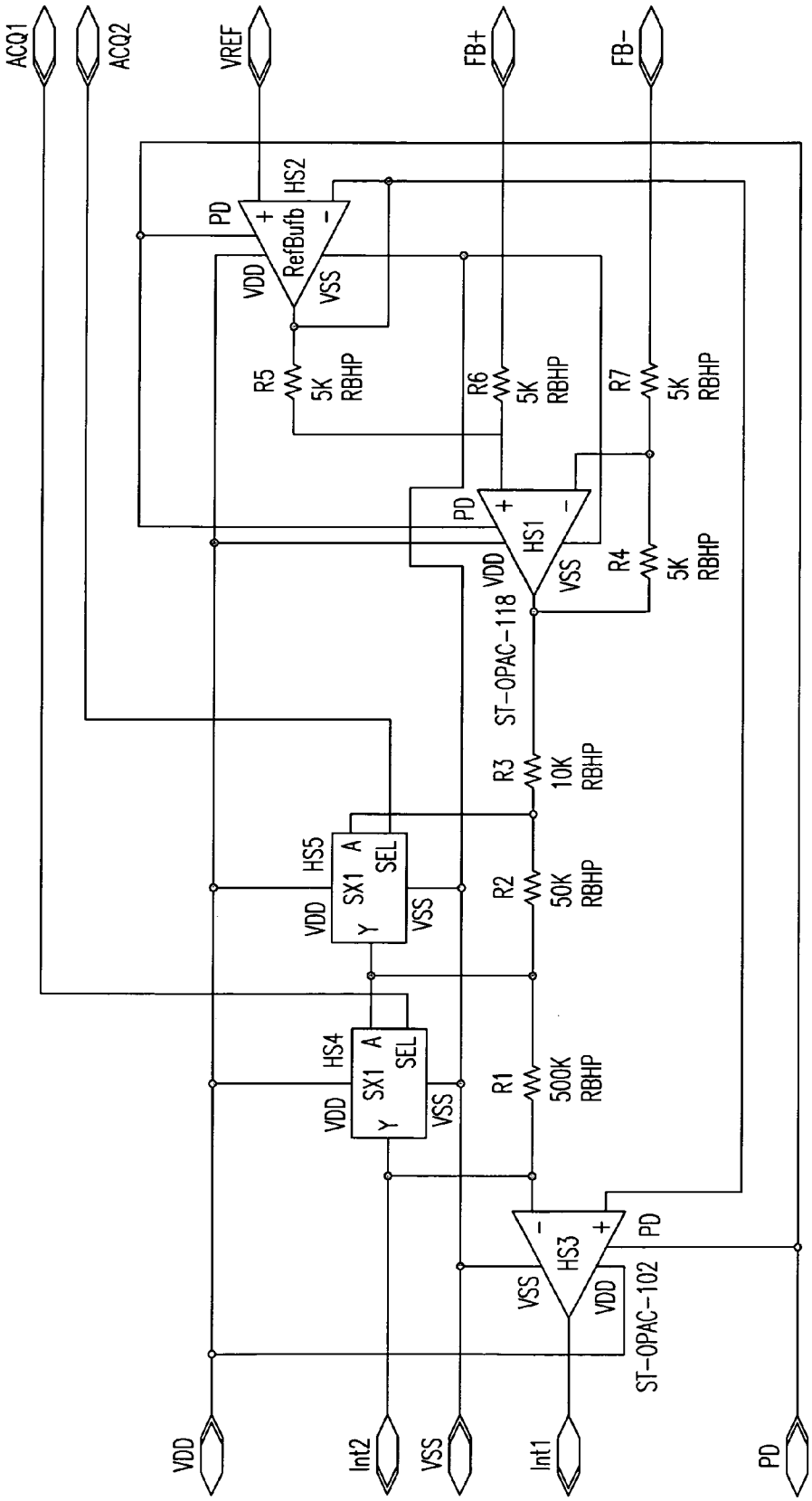

ACQ1
ACQ2
VREF
FB+
FB-
PD
HS2
RefBufb
VDD
VSS
R5
5K
RBHP
R6
5K
RBHP
R7
5K
RBHP
HS1
R4
5K
RBHP
ST-OPAC-118
R3
10K
RBHP
HS5
SX1
A
SEL
Y
R2
50K
RBHP
HS4
R1
500K
RBHP
HS3
ST-OPAC-102
Int2
Int1

FIG. 165

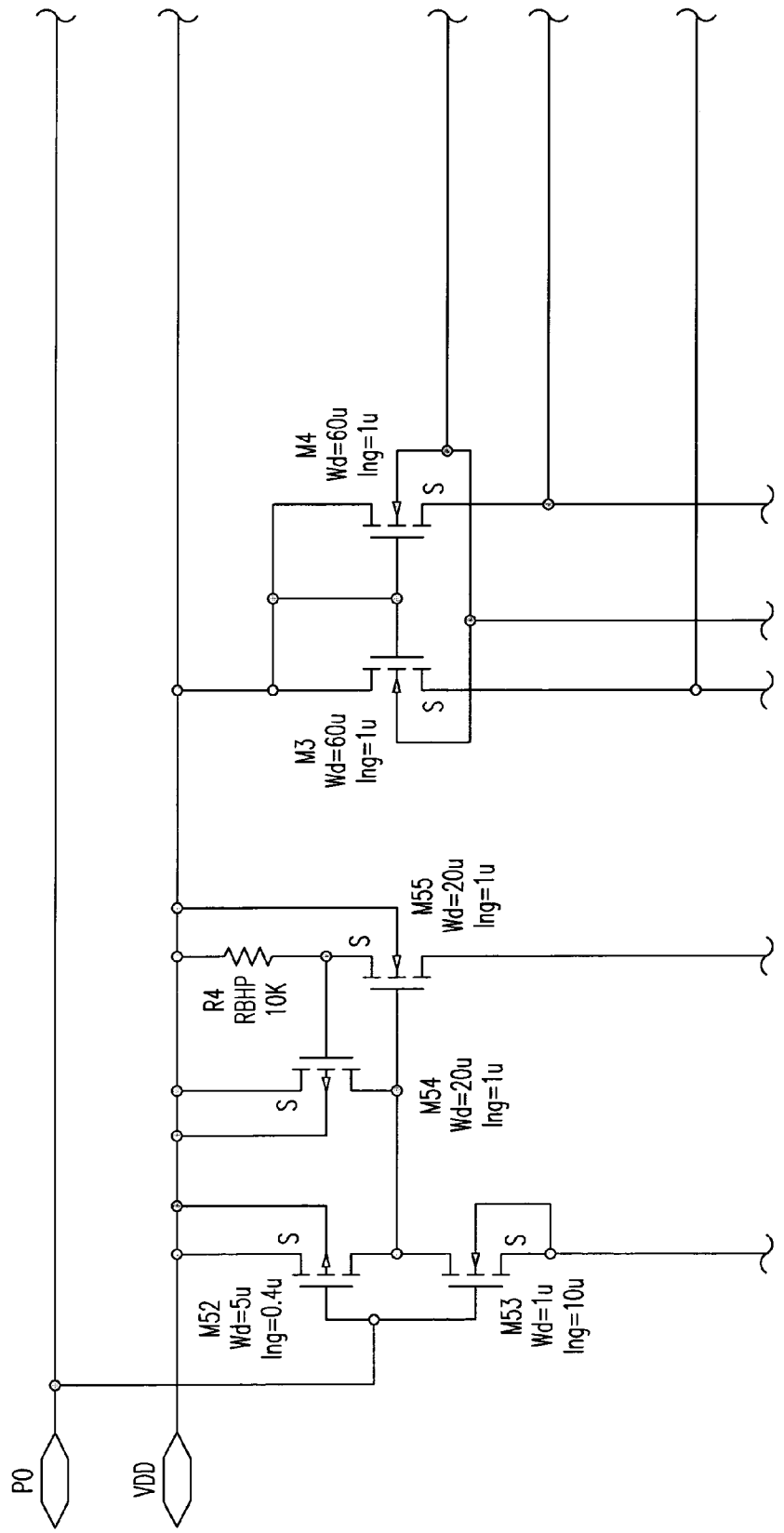

M4
Wd=60u
lng=1u
S
M3
Wd=60u
lng=1u
M55
Wd=20u
lng=1u
R4
RBHP
10K
M54
Wd=20u
lng=1u
M52
Wd=5u
lng=0.4u
M53
Wd=1u
lng=10u
P0
VDD

FIG. 166A

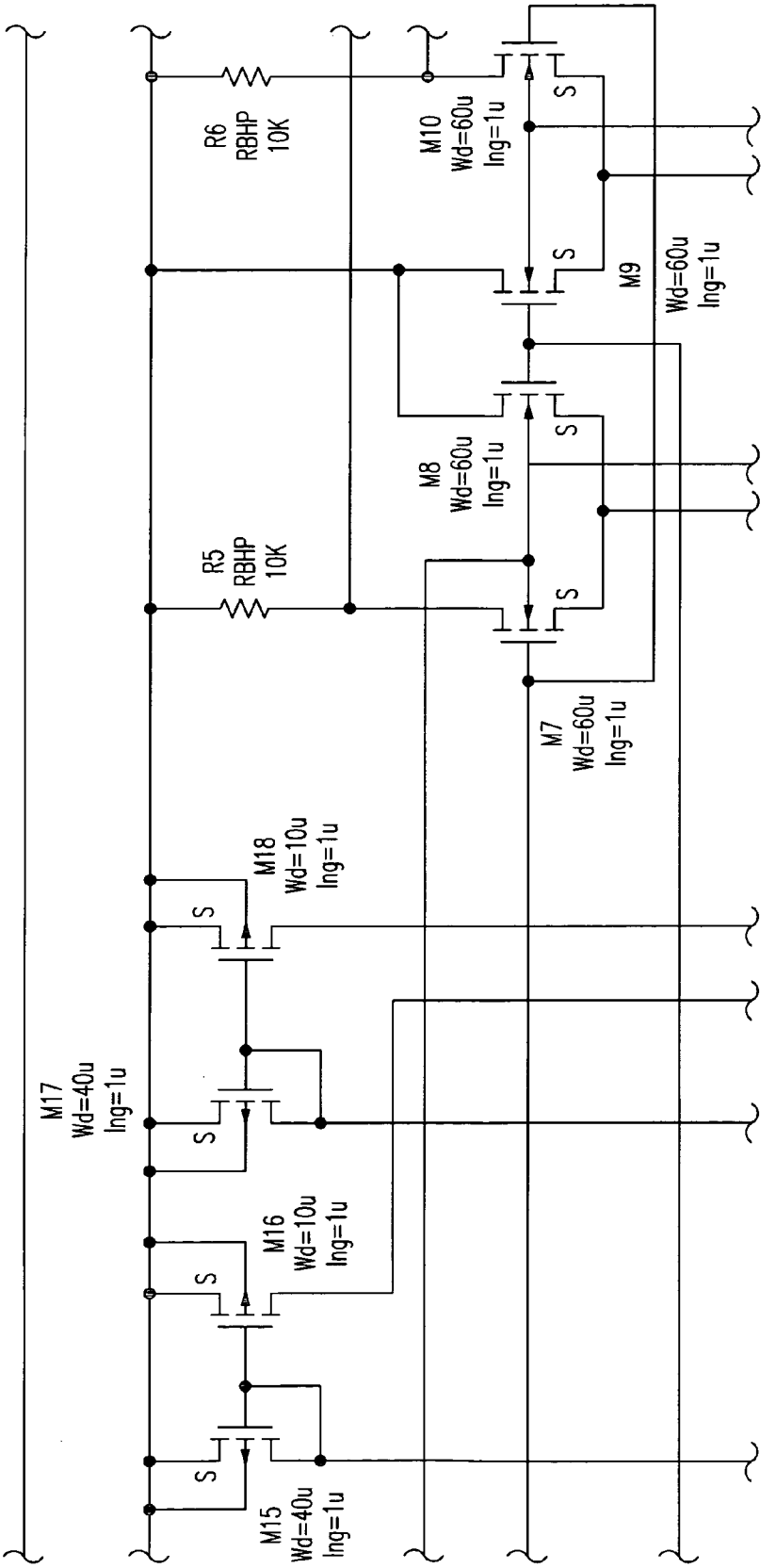

R6
RBHP
10K
R5
RBHP
10K
M10
Wd=60u
lng=1u
M9
Wd=60u
lng=1u
M8
Wd=60u
lng=1u
M7
Wd=60u
lng=1u
M18
Wd=10u
lng=1u
M17
Wd=40u
lng=1u
M16
Wd=10u
lng=1u
M15
Wd=40u
lng=1u
S

FIG.166B

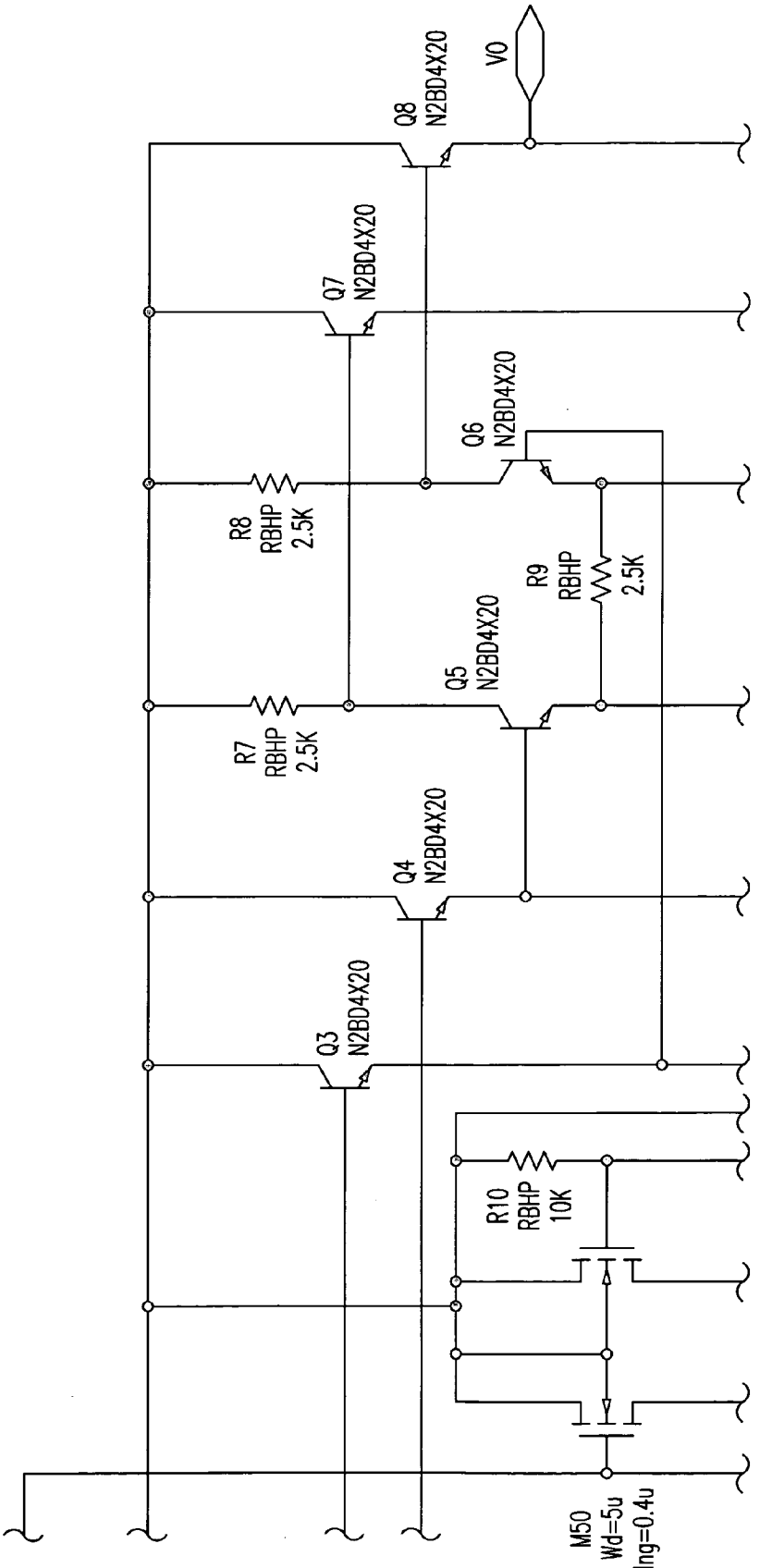

VO
Q8 N2BD4X20
Q7 N2BD4X20
Q6 N2BD4X20
R8 RBHP 2.5K
R9 RBHP 2.5K
Q5 N2BD4X20
R7 RBHP 2.5K
Q4 N2BD4X20
Q3 N2BD4X20
R10 RBHP 10K
M50 Wd=5u lng=0.4u

FIG. 166C

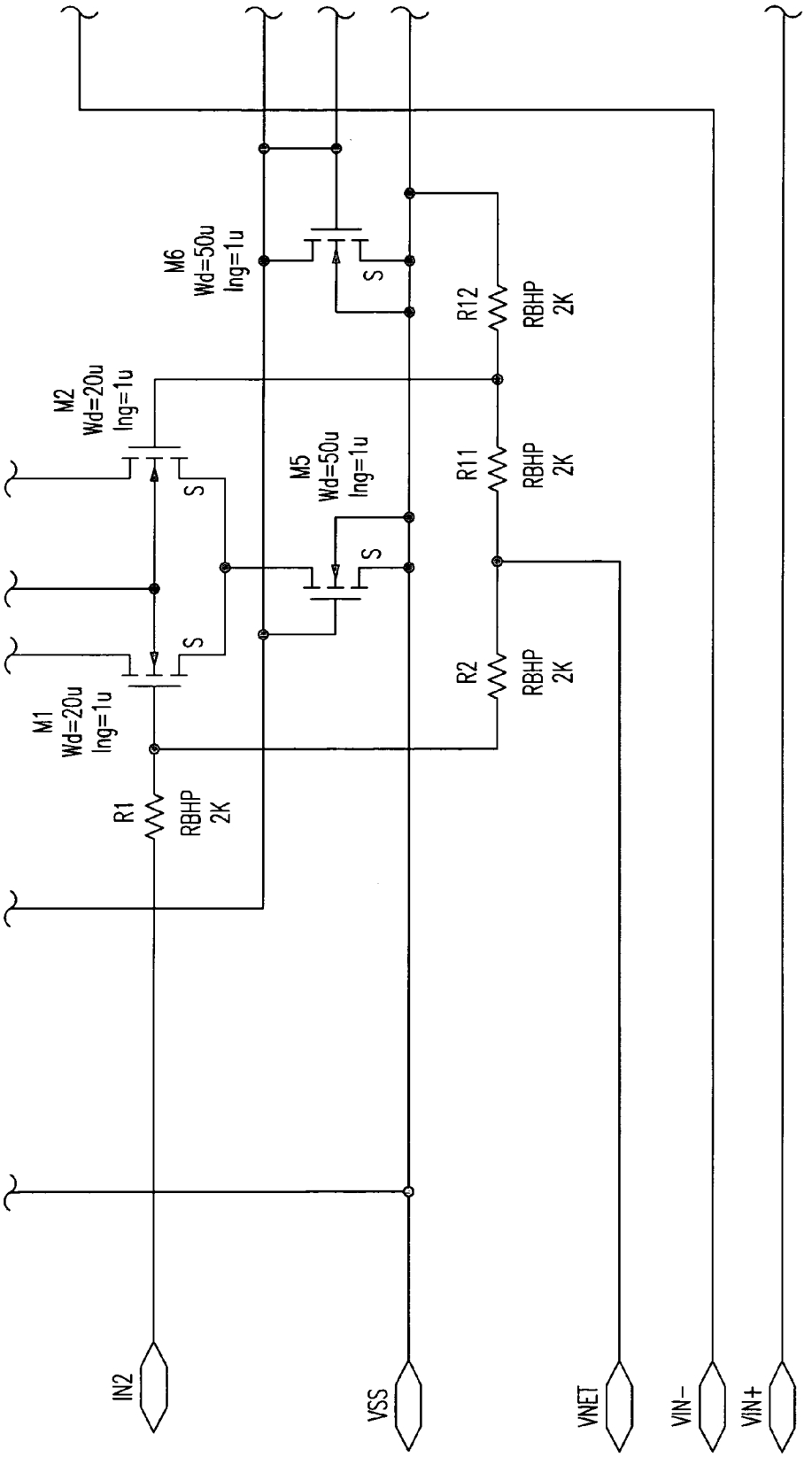

M6
Wd=50u
lng=1u
S
R12
RBHP
2K
M2
Wd=20u
lng=1u
M5
Wd=50u
lng=1u
R11
RBHP
2K
S
S
S
R2
RBHP
2K
M1
Wd=20u
lng=1u
R1
RBHP
2K
IN2
VSS
VNET
VIN-
VIN+

FIG. 166D

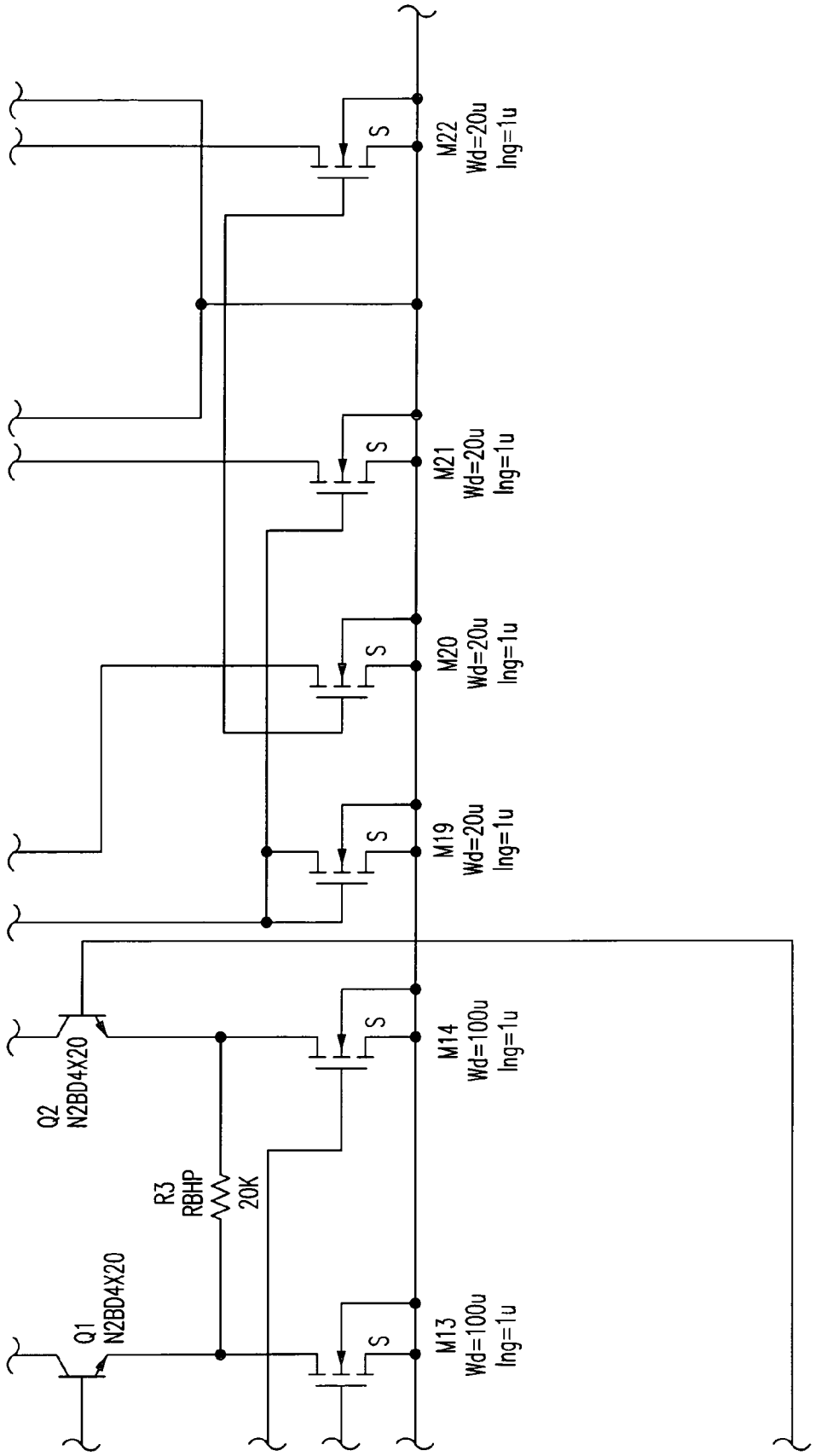

M22
Wd=20u
lng=1u
M21
Wd=20u
lng=1u
M20
Wd=20u
lng=1u
M19
Wd=20u
lng=1u
M14
Wd=100u
lng=1u
M13
Wd=100u
lng=1u
Q2
N2BD4X20
Q1
N2BD4X20
R3
RBHP
20K
S

FIG.166E

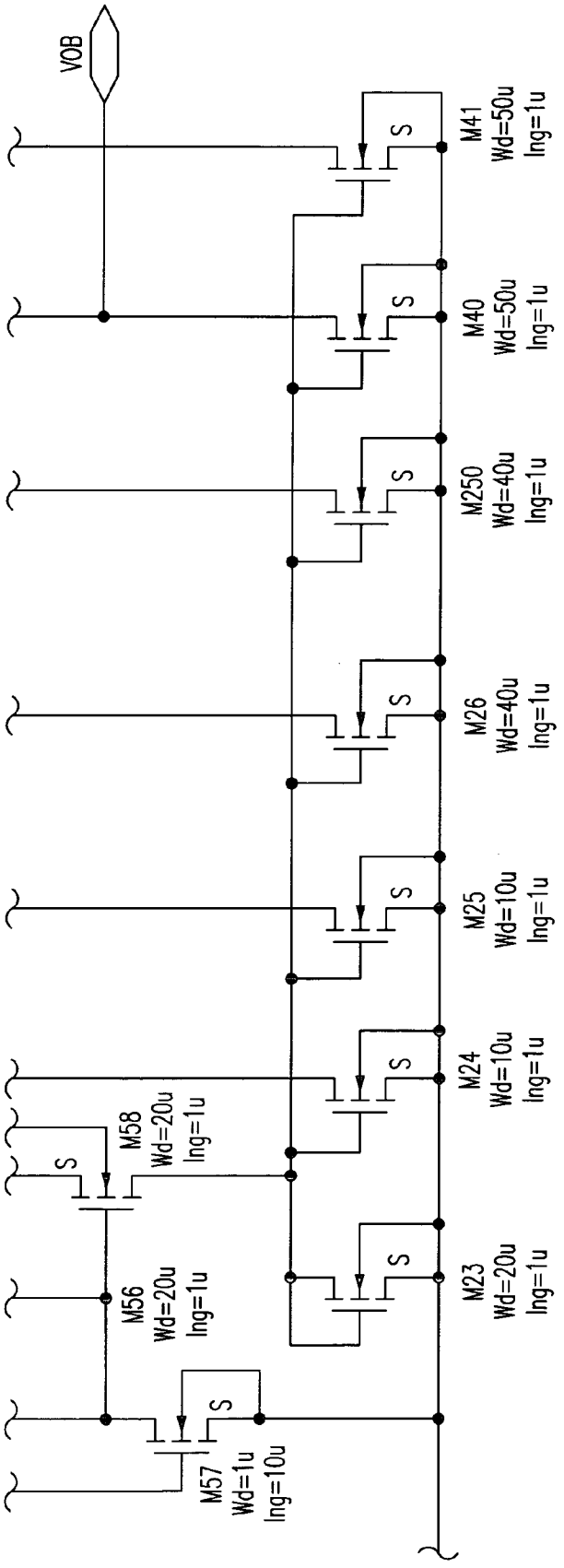

VOB
M41
Wd=50u
lng=1u
M40
Wd=50u
lng=1u
M250
Wd=40u
lng=1u
M26
Wd=40u
lng=1u
M25
Wd=10u
lng=1u
M24
Wd=10u
lng=1u
M23
Wd=20u
lng=1u
M58
Wd=20u
lng=1u
M56
Wd=20u
lng=1u
M57
Wd=1u
lng=10u
S

FIG.166F

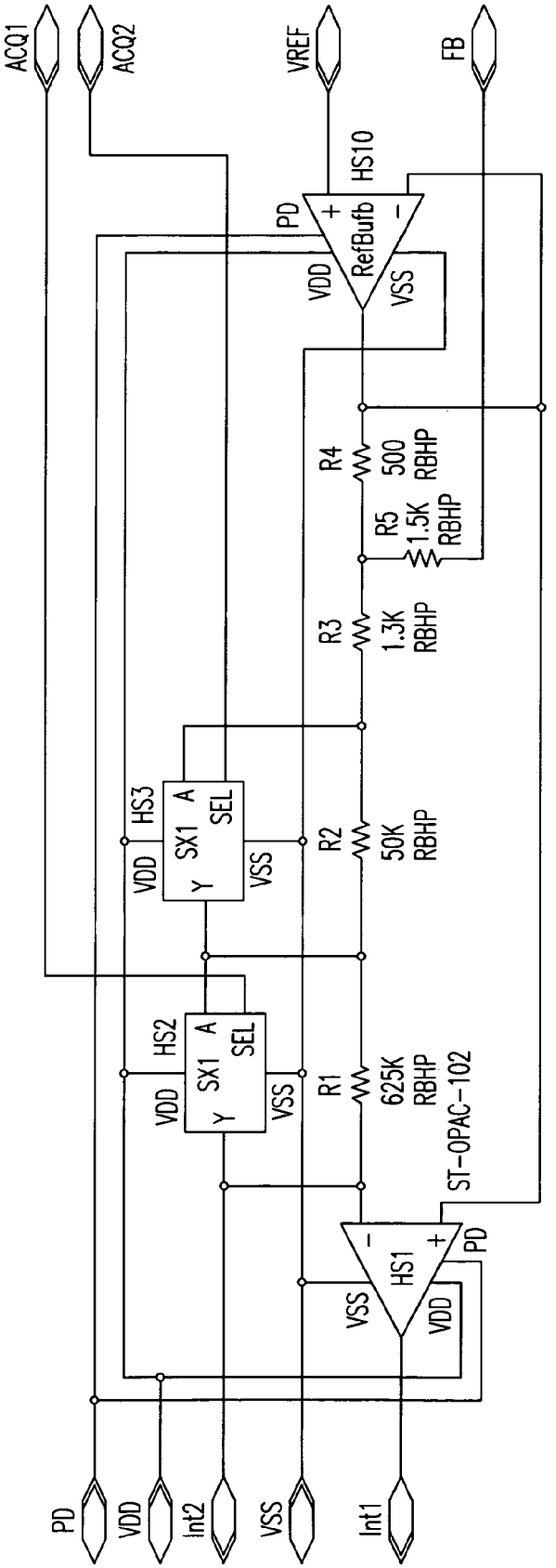

ACQ1
ACQ2
VREF
FB
HS10
PD
RefBufb
VDD
VSS
R4
500
RBHP
R5
1.5K
RBHP
R3
1.3K
RBHP
HS3
SX1
A
SEL
Y
R2
50K
RBHP
HS2
R1
625K
RBHP
ST-OPAC-102
HS1
PD
Int2
Int1

FIG. 167

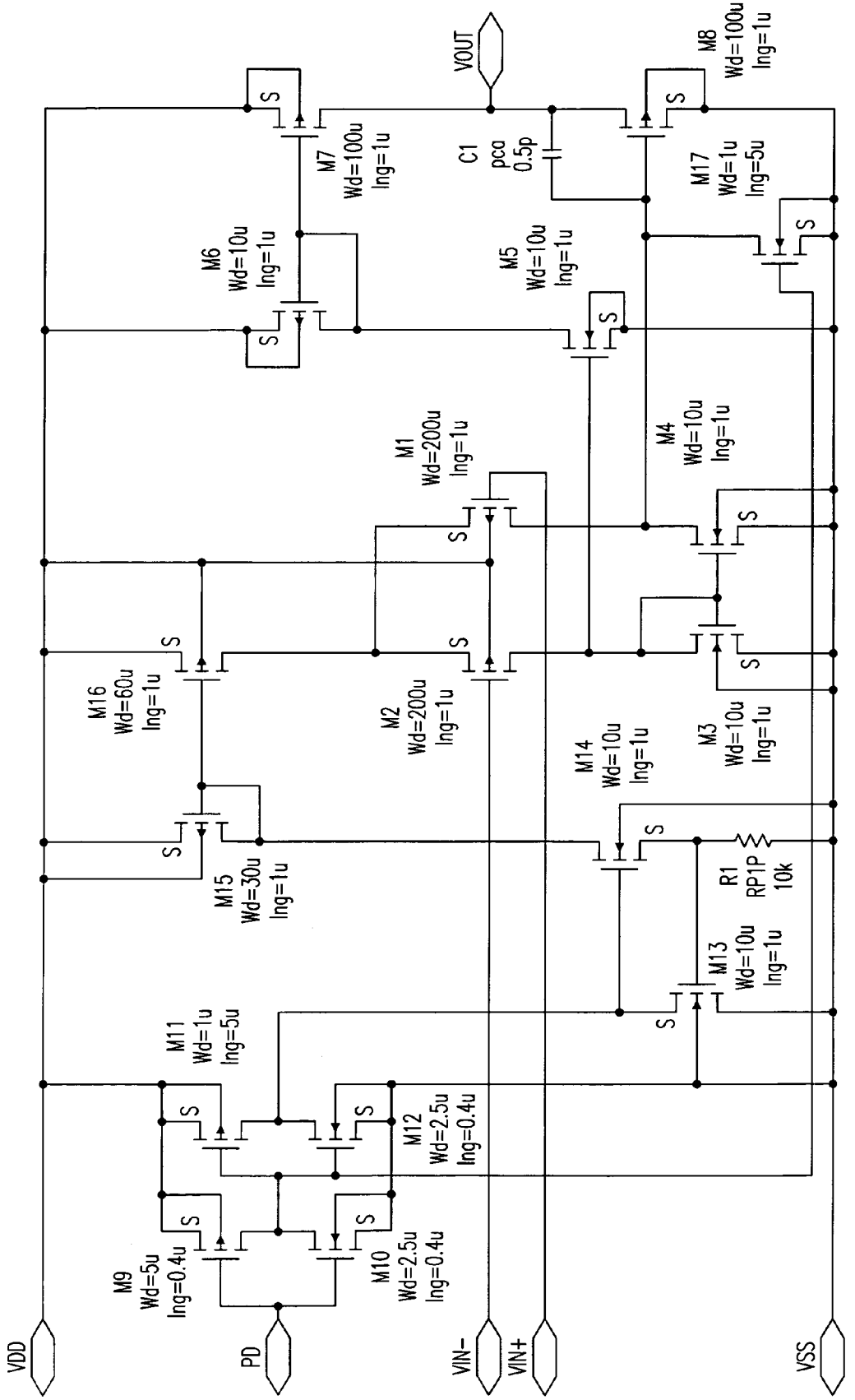

VOUT
M8 Wd=100u lng=1u
M7 Wd=100u lng=1u
C1 pca 0.5p
M17 Wd=1u lng=5u
M6 Wd=10u lng=1u
M5 Wd=10u lng=1u
M1 Wd=200u lng=1u
M4 Wd=10u lng=1u
M16 Wd=60u lng=1u
M2 Wd=200u lng=1u
M14 Wd=10u lng=1u
M3 Wd=10u lng=1u
M15 Wd=30u lng=1u
R1 RP1P 10k
M13 Wd=10u lng=1u
M11 Wd=1u lng=5u
M12 Wd=2.5u lng=0.4u
M9 Wd=5u lng=0.4u
M10 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG.168

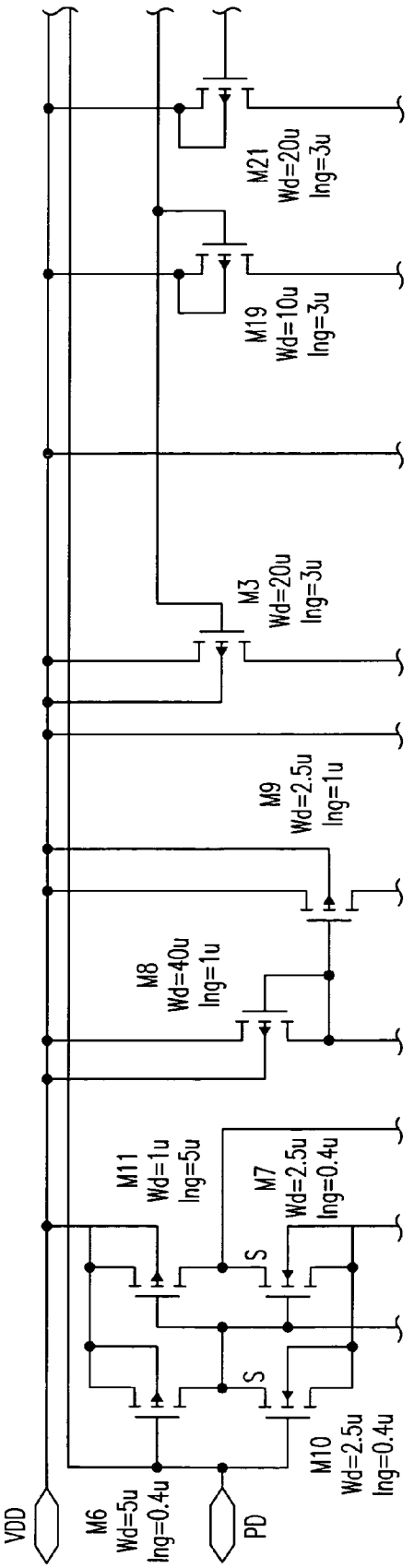

M21
Wd=20u
lng=3u
M19
Wd=10u
lng=3u
M3
Wd=20u
lng=3u
M9
Wd=2.5u
lng=1u
M8
Wd=40u
lng=1u
M11
Wd=1u
lng=5u
M7
Wd=2.5u
lng=0.4u
S
S
M10
Wd=2.5u
lng=0.4u
VDD
M6
Wd=5u
lng=0.4u
PD

FIG.169A

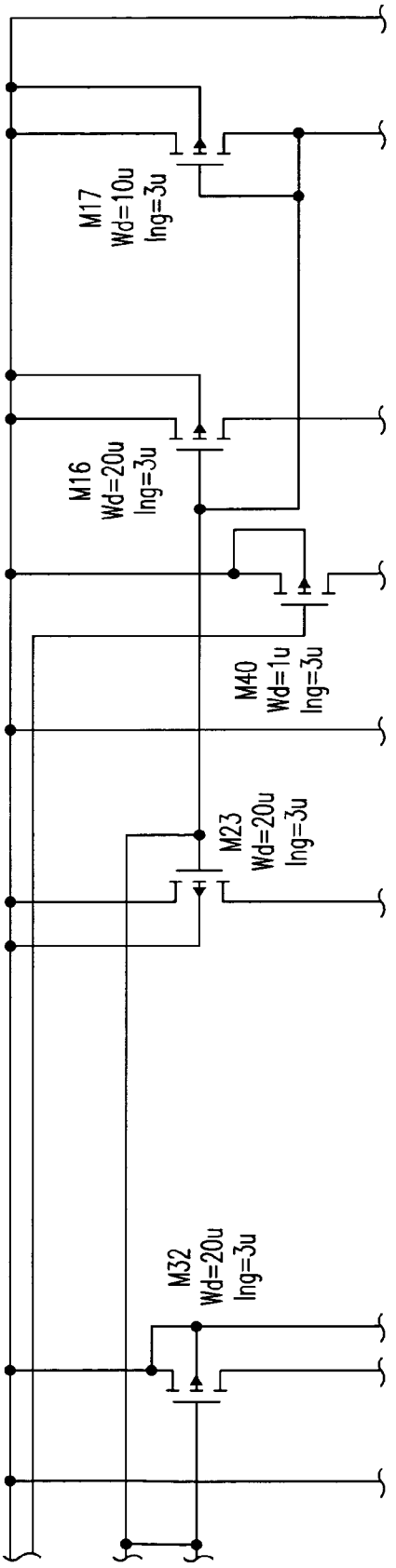

M17
Wd=10u
lng=3u
M16
Wd=20u
lng=3u
M40
Wd=1u
lng=3u
M23
Wd=20u
lng=3u
M32
Wd=20u
lng=3u

FIG. 169B

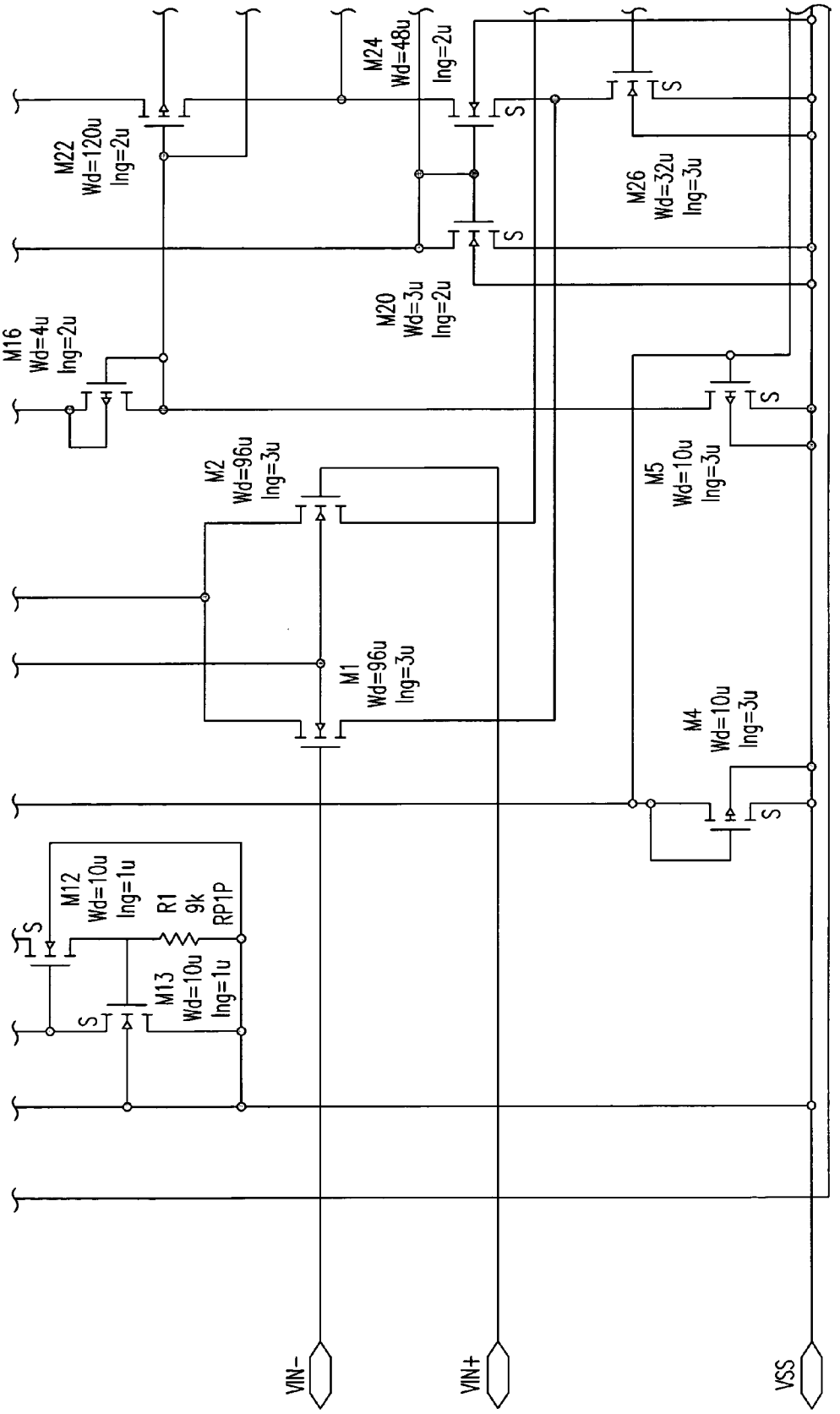

M22
Wd=120u
lng=2u
M24
Wd=48u
lng=2u
M26
Wd=32u
lng=3u
M16
Wd=4u
lng=2u
M20
Wd=3u
lng=2u
M2
Wd=96u
lng=3u
M5
Wd=10u
lng=3u
M1
Wd=96u
lng=3u
M4
Wd=10u
lng=3u
M12
Wd=10u
lng=1u
R1
9k
RP1P
M13
Wd=10u
lng=1u
S
VIN-
VIN+
VSS

FIG. 169C

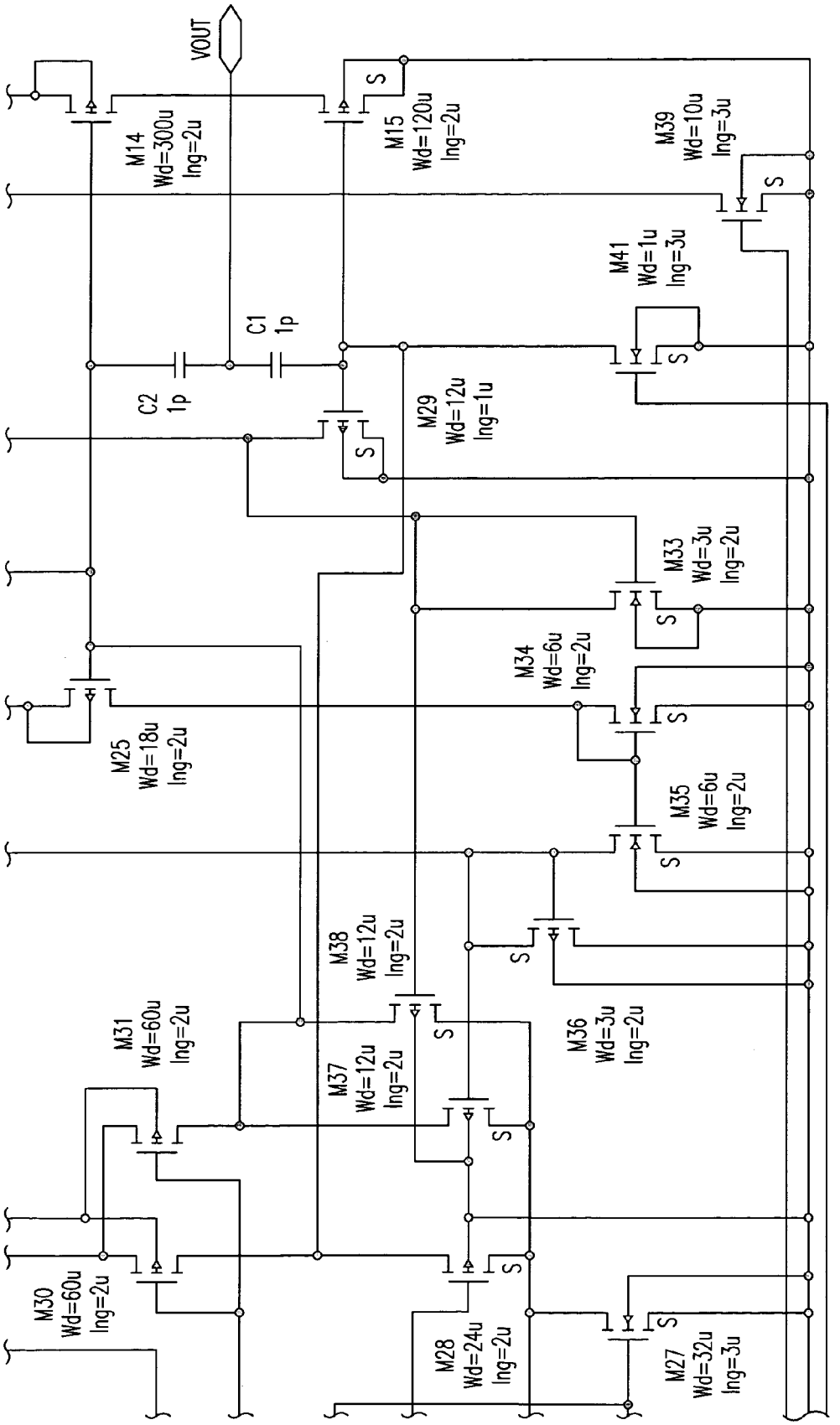

VOUT
M14 Wd=300u lng=2u
M15 Wd=120u lng=2u
M39 Wd=10u lng=3u
M41 Wd=1u lng=3u
C1 1p
C2 1p
M29 Wd=12u lng=1u
M33 Wd=3u lng=2u
M34 Wd=6u lng=2u
M25 Wd=18u lng=2u
M35 Wd=6u lng=2u
M38 Wd=12u lng=2u
M31 Wd=60u lng=2u
M36 Wd=3u lng=2u
M37 Wd=12u lng=2u
M30 Wd=60u lng=2u
M28 Wd=24u lng=2u
M27 Wd=32u lng=3u
S

FIG. 169D

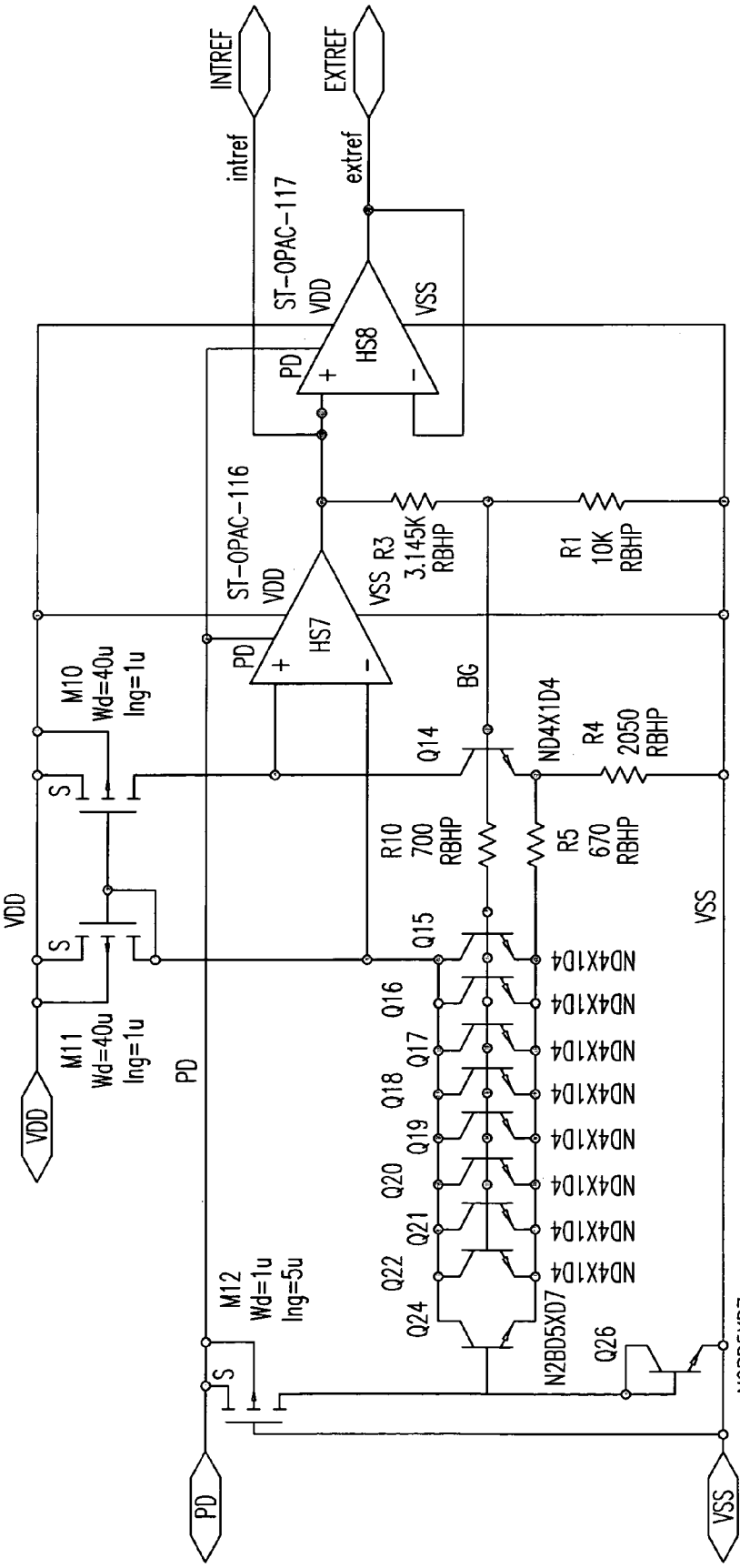

INTREF
EXTREF
intref
extref
ST-OPAC-117
VDD
VSS
PD
HS8
ST-OPAC-116
HS7
R3
3.145K
RBHP
R1
10K
RBHP
M10
Wd=40u
lng=1u
BG
Q14
ND4X1D4
R4
2050
RBHP
R10
700
RBHP
R5
670
RBHP
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q24
Q26
N2BD5XD7
M11
M12
Wd=1u
lng=5u
S

FIG. 170

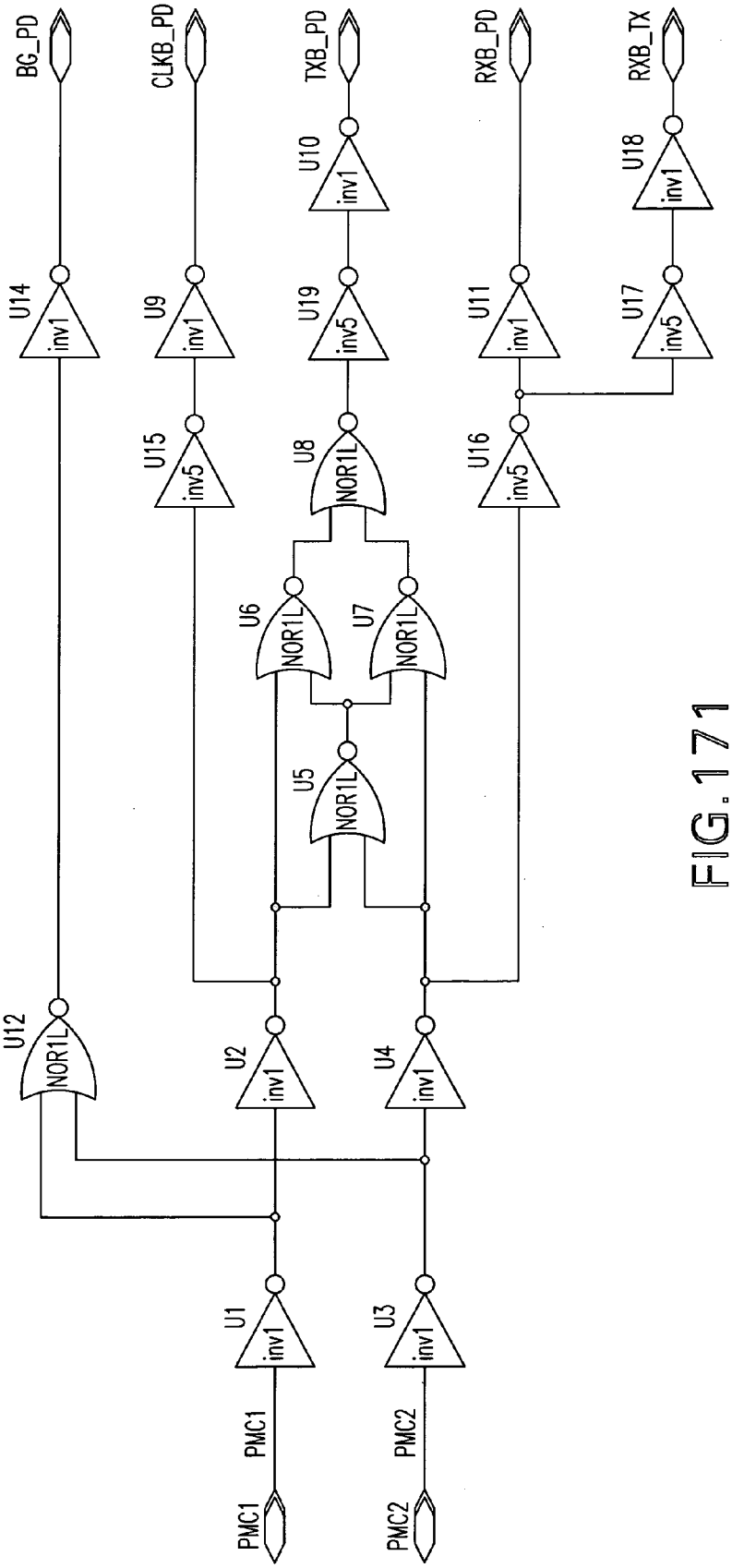

BG_PD
CLKB_PD
TXB_PD
RXB_PD
RXB_TX
U14
inv1
U9
inv1
U10
inv1
U11
inv1
U18
inv1
U15
inv5
U19
inv5
U17
inv5
U8
NOR1L
U16
inv5
U6
NOR1L
U7
NOR1L
U5
NOR1L
U12
NOR1L
U2
inv1
U4
inv1
U1
inv1
U3
inv1
PMC1
PMC2
PMC1
PMC2

FIG. 171

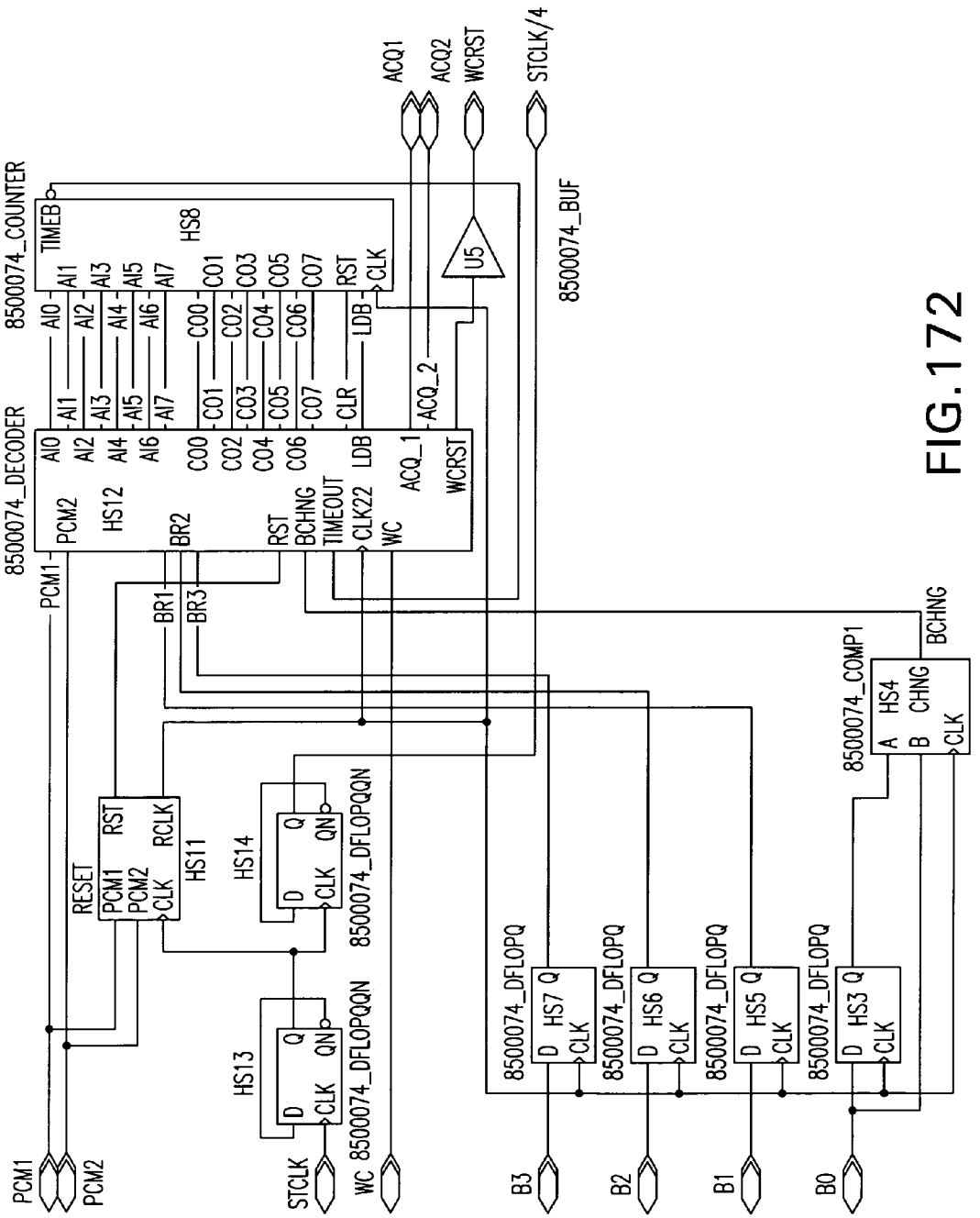

ACQ1
ACQ2
WCRST
STCLK/4
8500074_COUNTER
TIMEB
HS8
AI0
AI1
AI2
AI3
AI4
AI5
AI6
AI7
CO0
CO1
CO2
CO3
CO4
CO5
CO6
CO7
RST
CLK
LDB
U5
8500074_BUF
8500074_DECODER
PCM2
HS12
BR2
BR1
BR3
PCM1
CLR
ACQ_1
ACQ_2
WCRST
RST
BCHNG
TIMEOUT
CLK22
WC
LDB
BCHNG
8500074_COMP1
A HS4
B CHNG
CLK
RESET
PCM1
PCM2
CLK
RST
RCLK
HS11
HS14
D
Q
CLK
QN
8500074_DFLOPQQN
HS13
8500074_DFLOPQ
D HS7 Q
D HS6 Q
D HS5 Q
D HS3 Q
CLK
PCM1
PCM2
STCLK
WC
B3
B2
B1
B0

FIG. 172

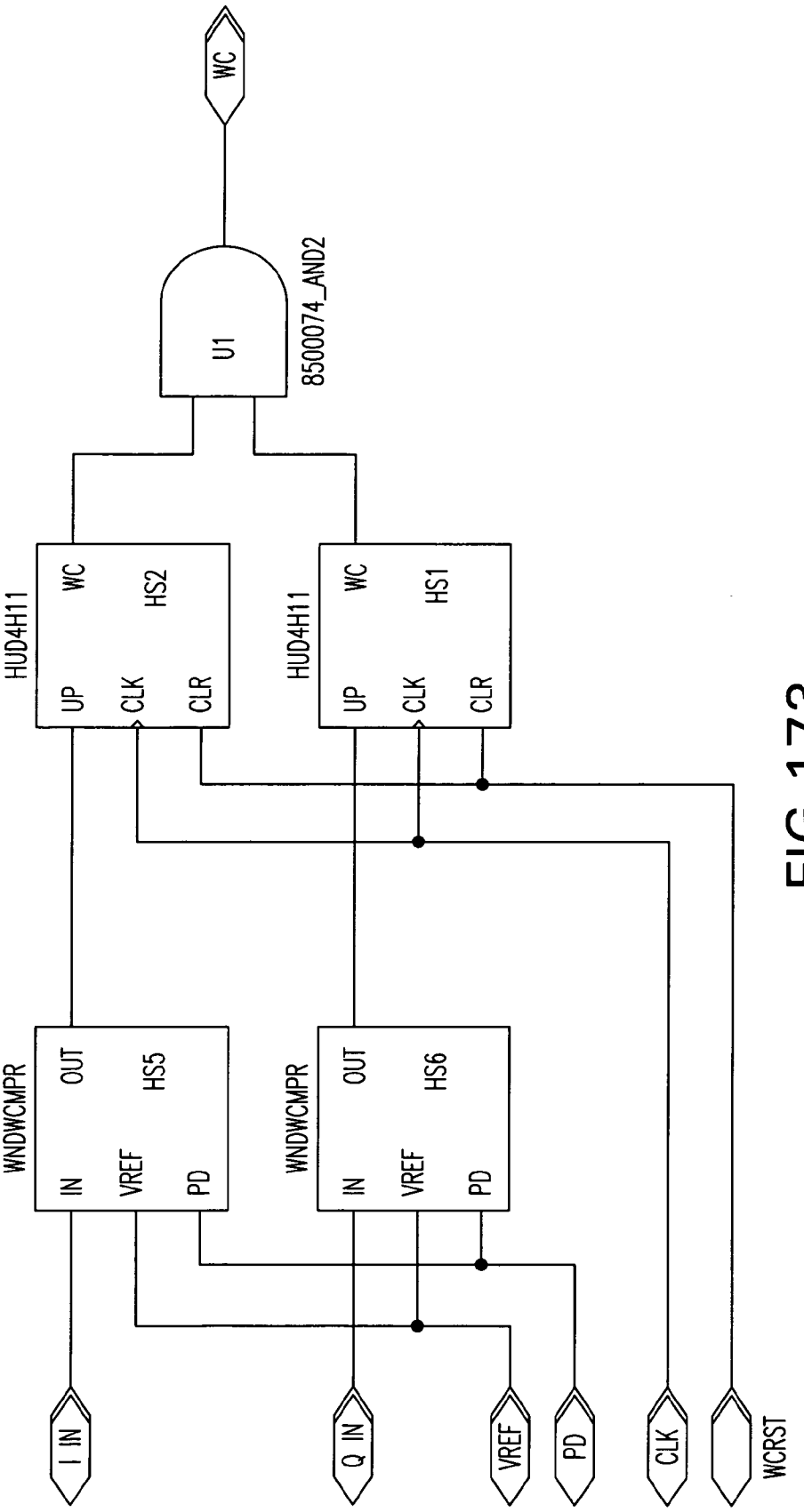

WC
U1
8500074_AND2
HUD4H11
WC
HS2
UP
CLK
CLR
HUD4H11
WC
HS1
UP
CLK
CLR
WNDWCMPR
OUT
HS5
IN
VREF
PD
WNDWCMPR
OUT
HS6
IN
VREF
PD
I IN
Q IN
VREF
PD
CLK
WCRST

FIG. 173

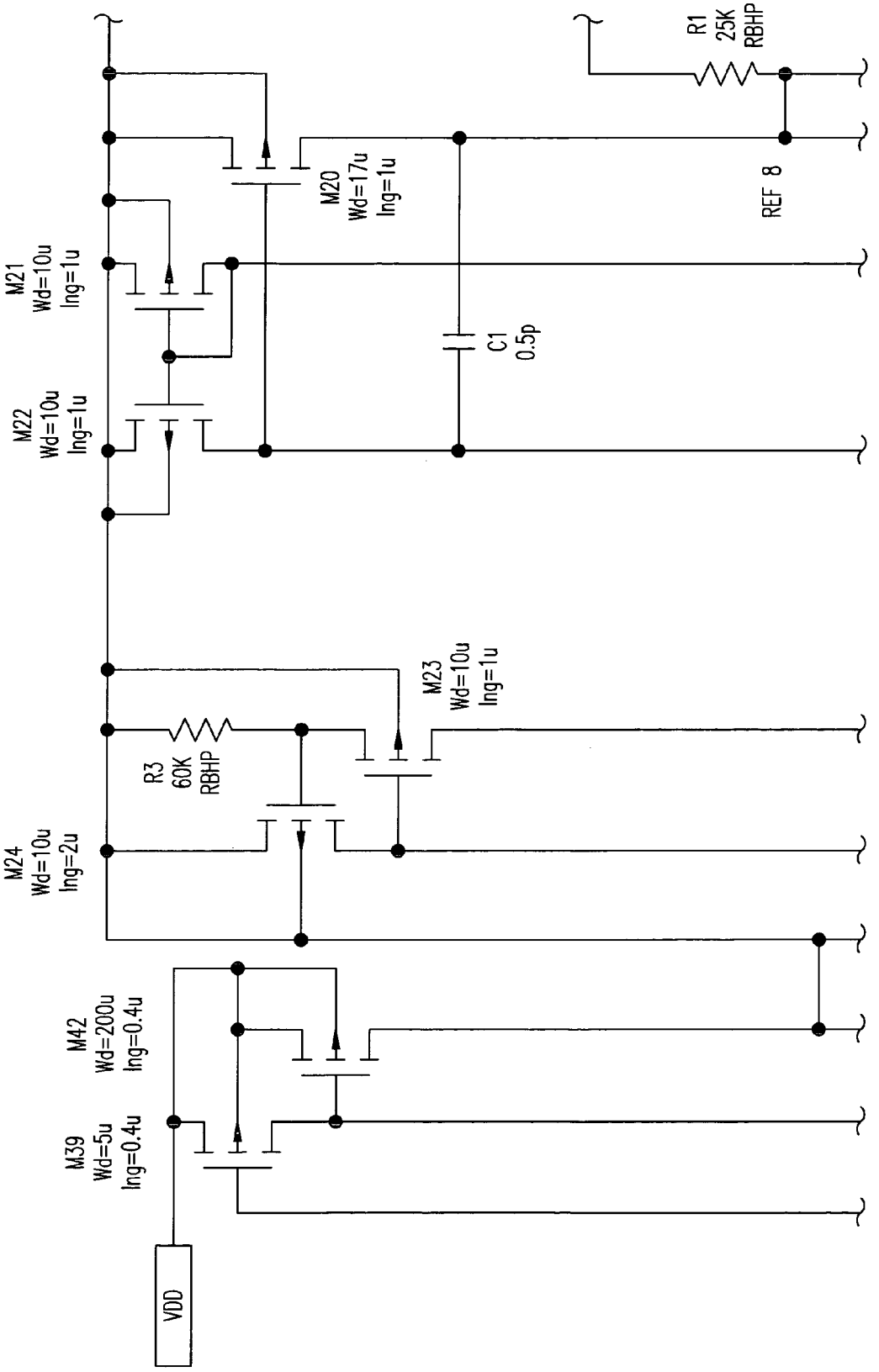

R1
25K
RBHP
M20
Wd=17u
lng=1u
REF 8
M21
Wd=10u
lng=1u
C1
0.5p
M22
Wd=10u
lng=1u
M23
Wd=10u
lng=1u
R3
60K
RBHP
M24
Wd=10u
lng=2u
M42
Wd=200u
lng=0.4u
M39
Wd=5u
lng=0.4u
VDD

FIG.174A

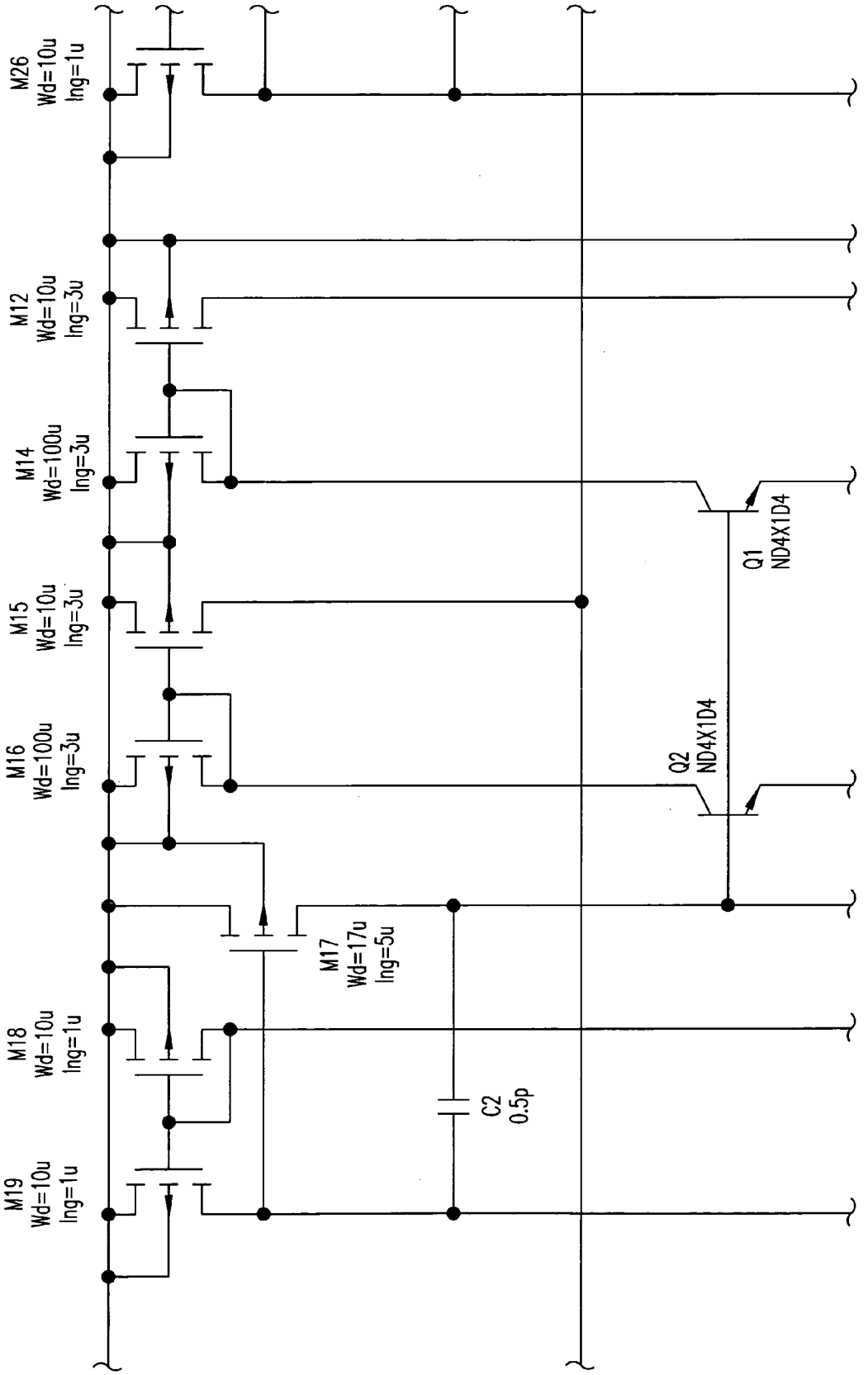

M26
Wd=10u
lng=1u
M12
Wd=10u
lng=3u
M14
Wd=100u
lng=3u
M15
Wd=10u
lng=3u
M16
Wd=100u
lng=3u
M17
Wd=17u
lng=5u
M18
Wd=10u
lng=1u
M19
Wd=10u
lng=1u
C2
0.5p
Q1
ND4X1D4
Q2
ND4X1D4

FIG. 174B

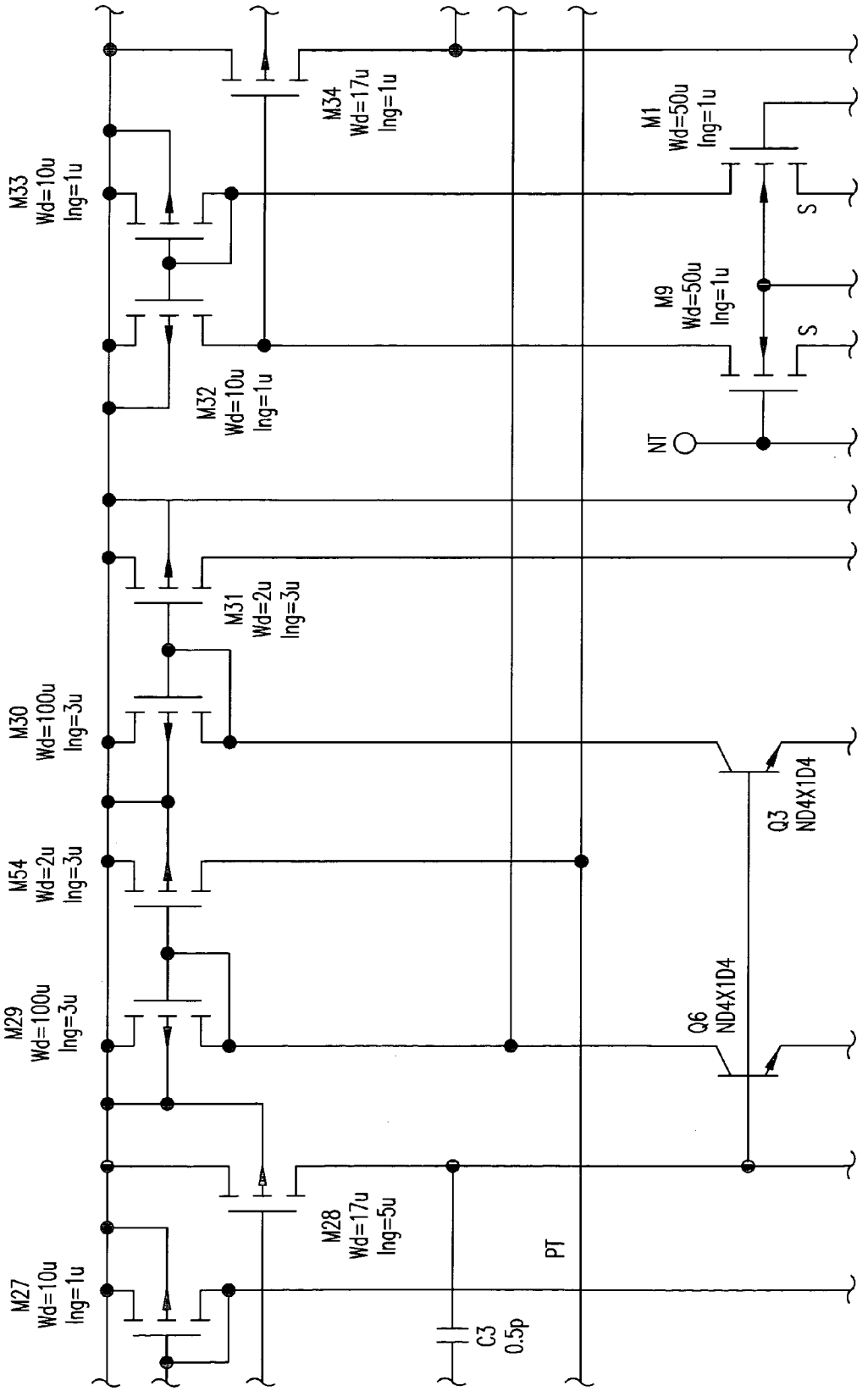

M33
Wd=10u
lng=1u
M34
Wd=17u
lng=1u
M1
Wd=50u
lng=1u
S
M9
Wd=50u
lng=1u
S
M32
Wd=10u
lng=1u
NT
M31
Wd=2u
lng=3u
M30
Wd=100u
lng=3u
Q3
ND4X1D4
M54
Wd=2u
lng=3u
M29
Wd=100u
lng=3u
Q6
ND4X1D4
M28
Wd=17u
lng=5u
PT
M27
Wd=10u
lng=1u
C3
0.5p

FIG.174C

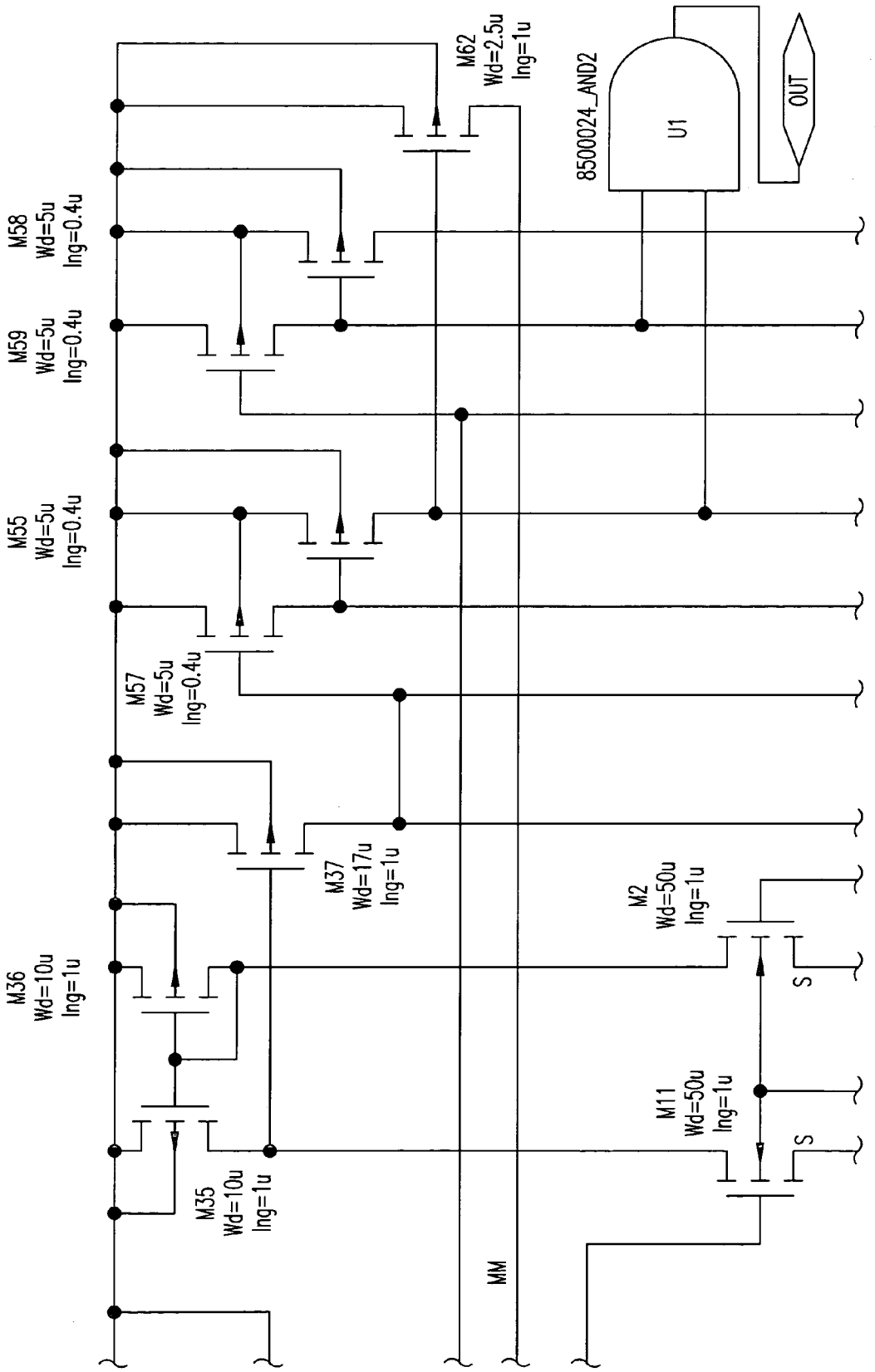

M62
Wd=2.5u
lng=1u
8500024_AND2
U1
OUT
M58
Wd=5u
lng=0.4u
M59
Wd=5u
lng=0.4u
M55
Wd=5u
lng=0.4u
M57
Wd=5u
lng=0.4u
M37
Wd=17u
lng=1u
M36
Wd=10u
lng=1u
M35
Wd=10u
lng=1u
M2
Wd=50u
lng=1u
M11
Wd=50u
lng=1u
S
S
MM

FIG. 174D

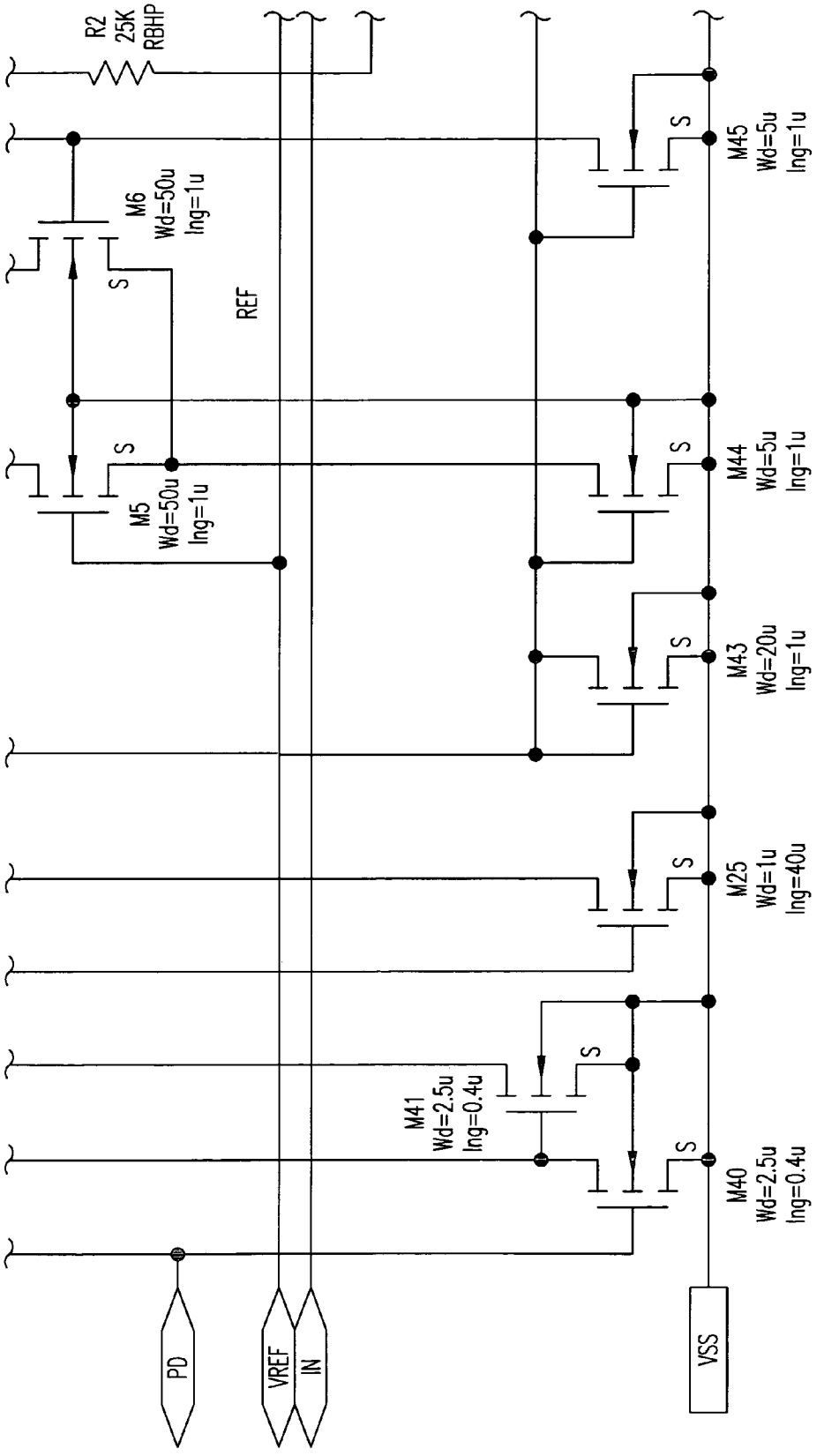

R2
25K
RBHP
M6
Wd=50u
lng=1u
M5
Wd=50u
lng=1u
REF
M45
Wd=5u
lng=1u
M44
Wd=5u
lng=1u
M43
Wd=20u
lng=1u
M25
Wd=1u
lng=40u
M41
Wd=2.5u
lng=0.4u
M40
Wd=2.5u
lng=0.4u
S
PD
VREF
IN
VSS
OP AMP
BIAS
2 INVERTERS

FIG. 174E

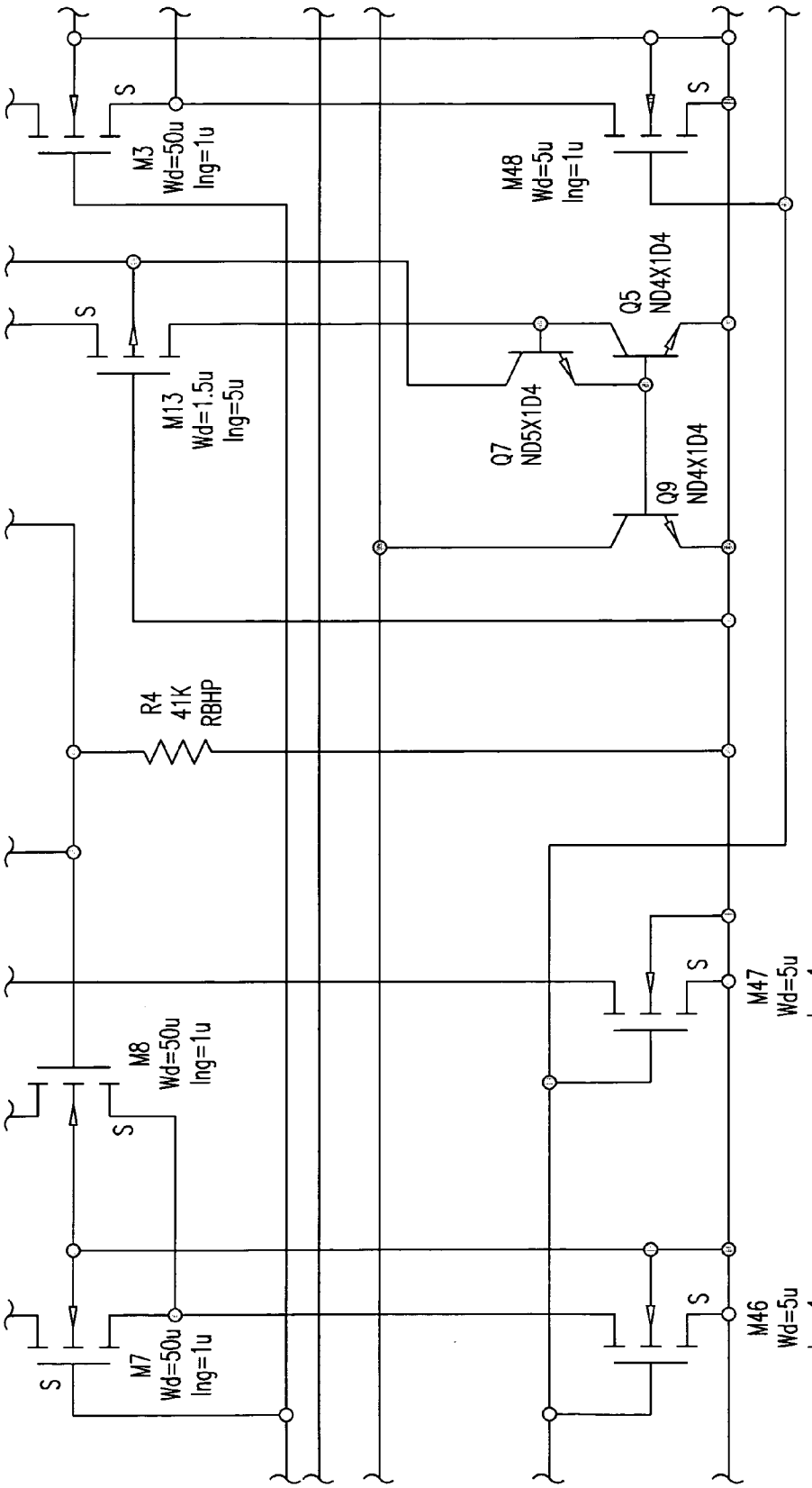

M3
Wd=50u
lng=1u
M48
Wd=5u
lng=1u
Q5
ND4X1D4
M13
Wd=1.5u
lng=5u
Q7
ND5X1D4
Q9
ND4X1D4
R4
41K
RBHP
M8
Wd=50u
lng=1u
M7
Wd=50u
lng=1u
M47
Wd=5u
lng=1u
M46
Wd=5u
lng=1u
S
OP AMP
OP AMP
THRESHOLD
CURRENT
SOURCE

FIG. 174F

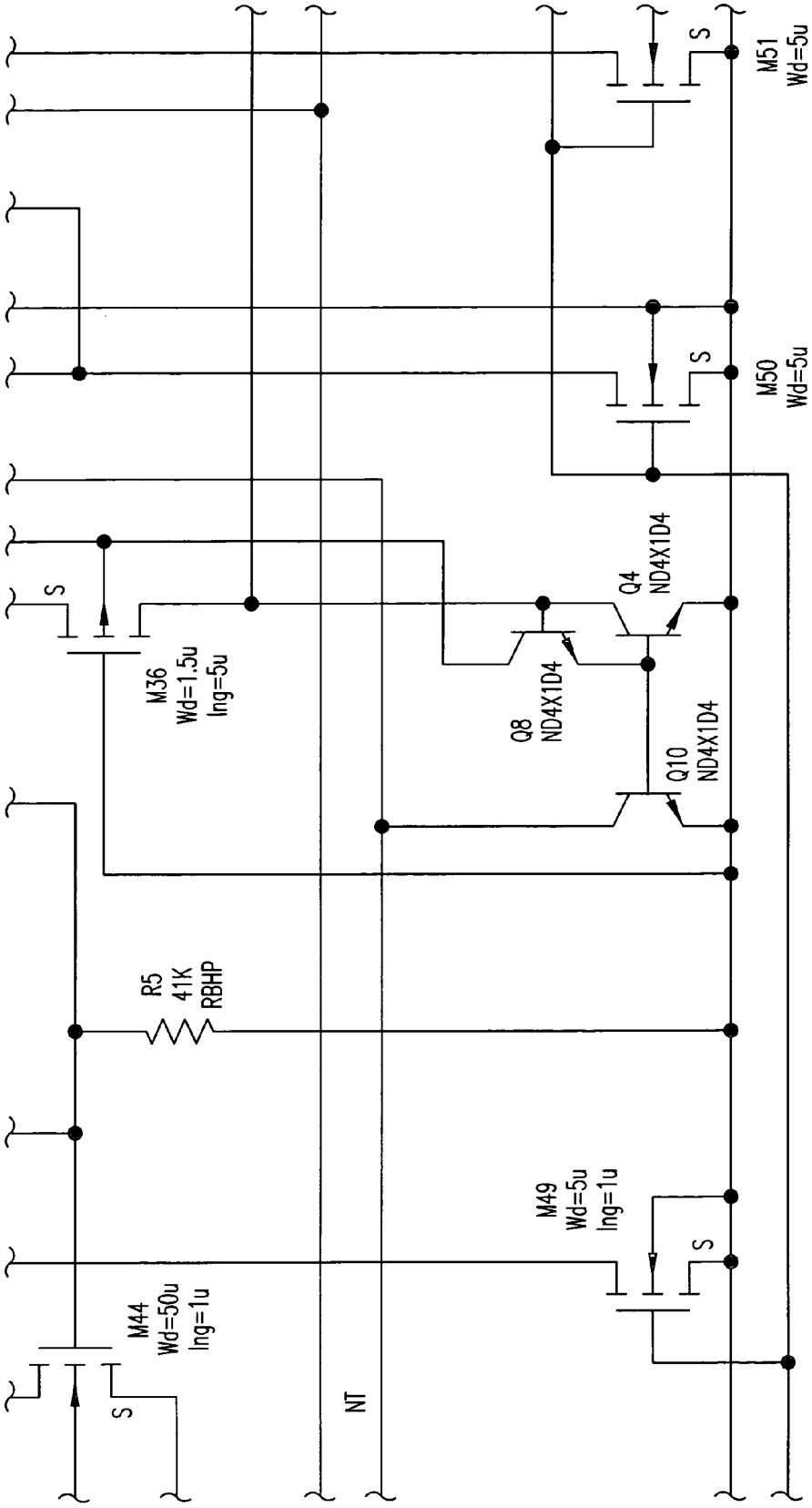

M51
Wd=5u
lng=1u
M50
Wd=5u
lng=1u
OP AMP
Q4
ND4X1D4
Q8
ND4X1D4
Q10
ND4X1D4
M36
Wd=1.5u
lng=5u
R5
41K
RBHP
M49
Wd=5u
lng=1u
M44
Wd=50u
lng=1u
S
NT
HYSTERESIS
CURRENT
SOURCE

FIG. 174G

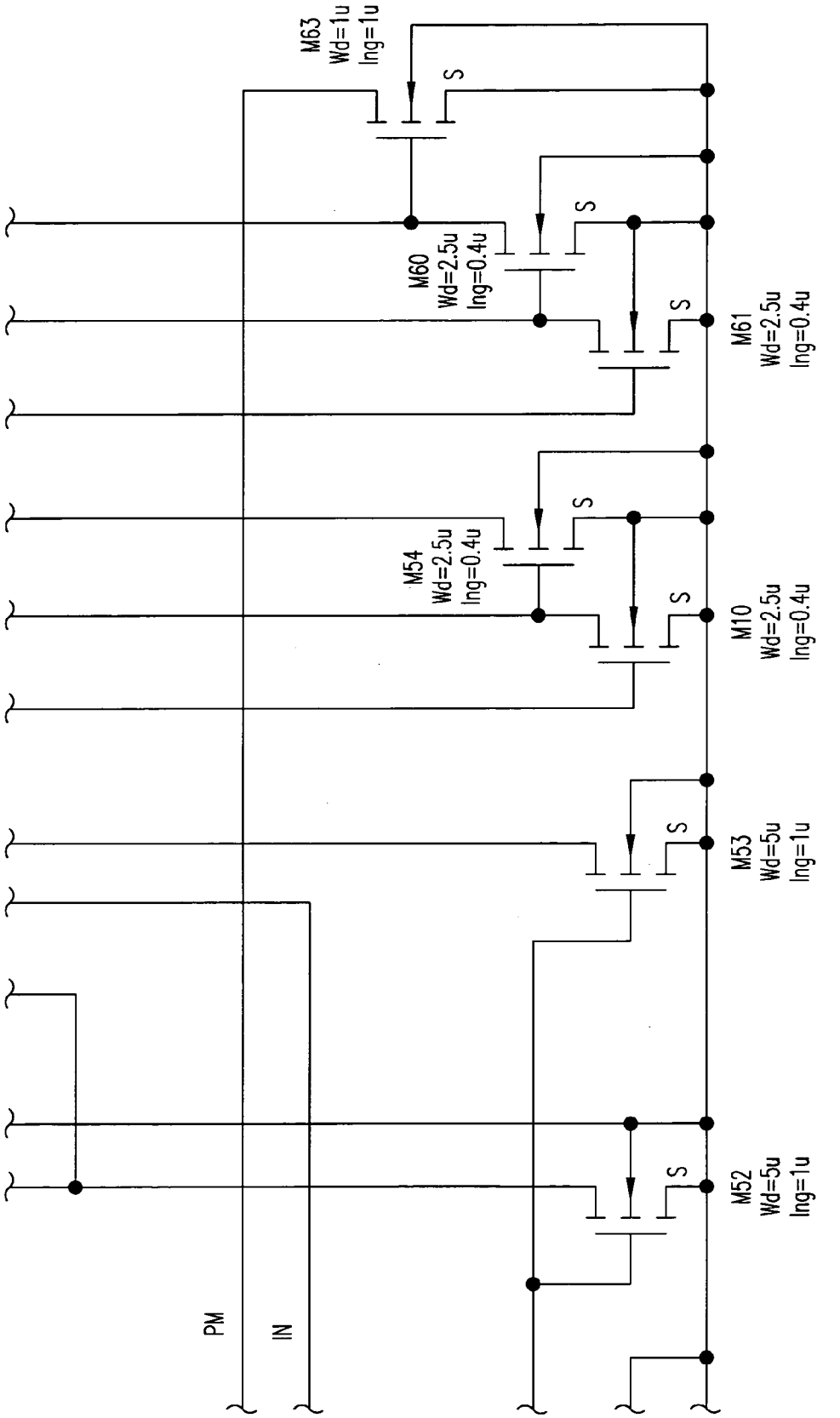

M63
Wd=1u
lng=1u
S
M60
Wd=2.5u
lng=0.4u
M61
Wd=2.5u
lng=0.4u
M54
Wd=2.5u
lng=0.4u
M10
Wd=2.5u
lng=0.4u
M53
Wd=5u
lng=1u
M52
Wd=5u
lng=1u
PM
IN
4 INVERTERS
OP AMP

FIG.174H

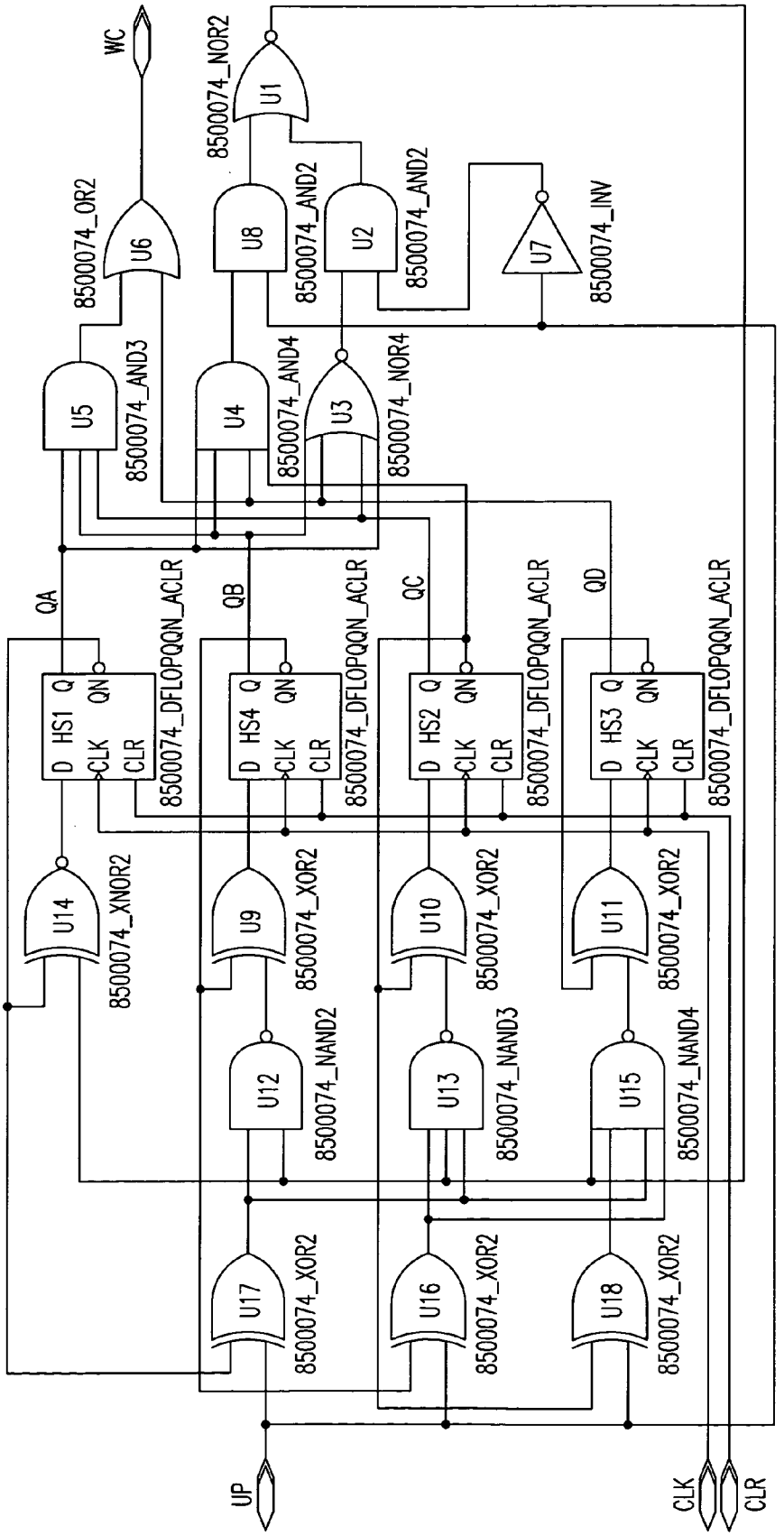

WC
8500074_NOR2
U1
8500074_OR2
U6
U8
8500074_AND2
U2
8500074_AND2
U7
8500074_INV
U5
8500074_AND3
U4
8500074_AND4
U3
8500074_NOR4
QA
QB
QC
QD
D HS1 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
D HS4 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
D HS2 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
D HS3 Q
CLK QN
CLR
8500074_DFLOPQQN_ACLR
U14
8500074_XNOR2
U9
8500074_XOR2
U10
8500074_XOR2
U11
8500074_XOR2
U12
8500074_NAND2
U13
8500074_NAND3
U15
8500074_NAND4
U17
8500074_XOR2
U16
8500074_XOR2
U18
8500074_XOR2
UP
CLK
CLR

FIG. 175

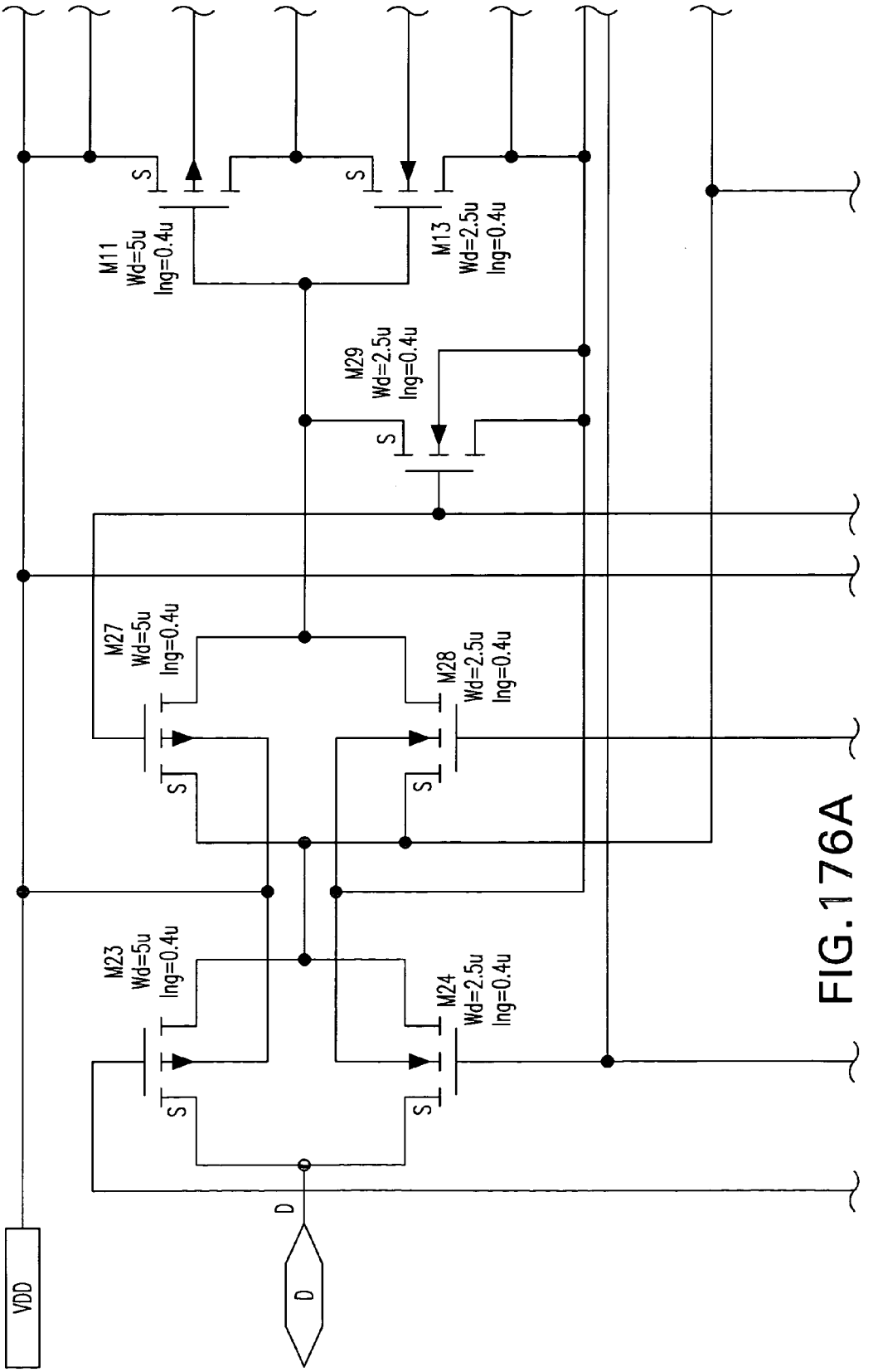

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.176A

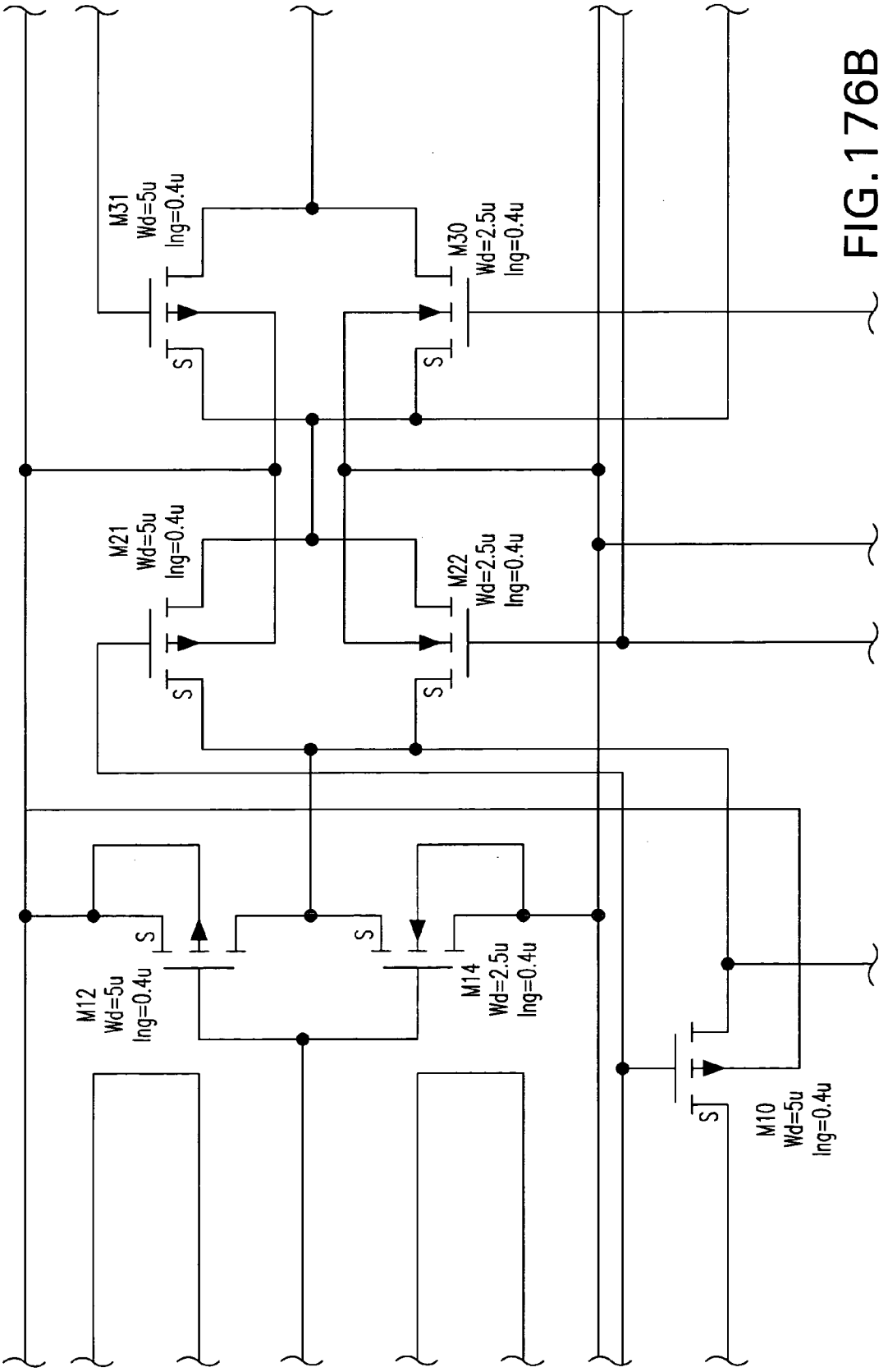

M31
Wd=5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
S

FIG. 176B

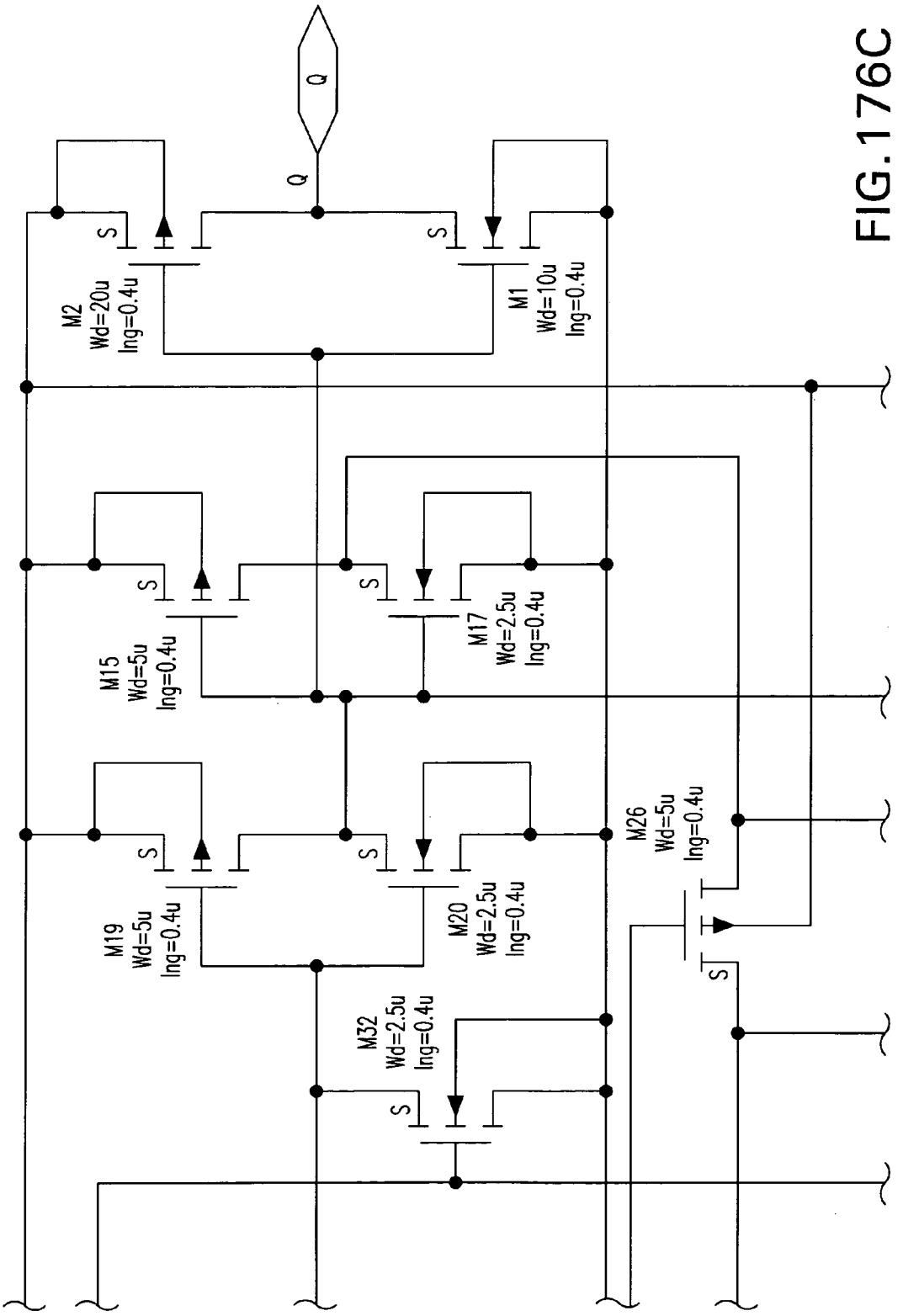

Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S
M26
Wd=5u
lng=0.4u

FIG.176C

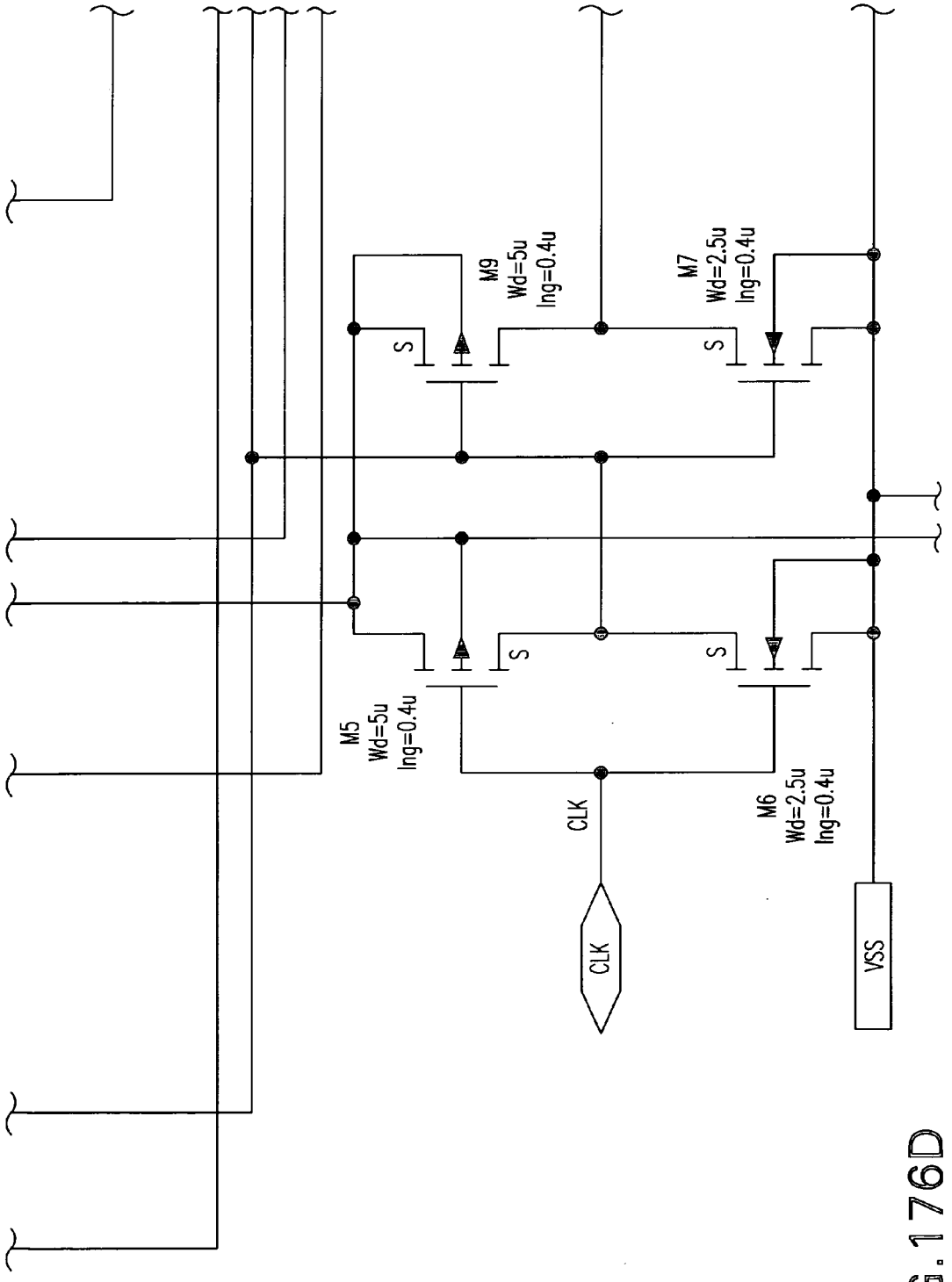

M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
CLK
CLK
VSS

FIG. 176D

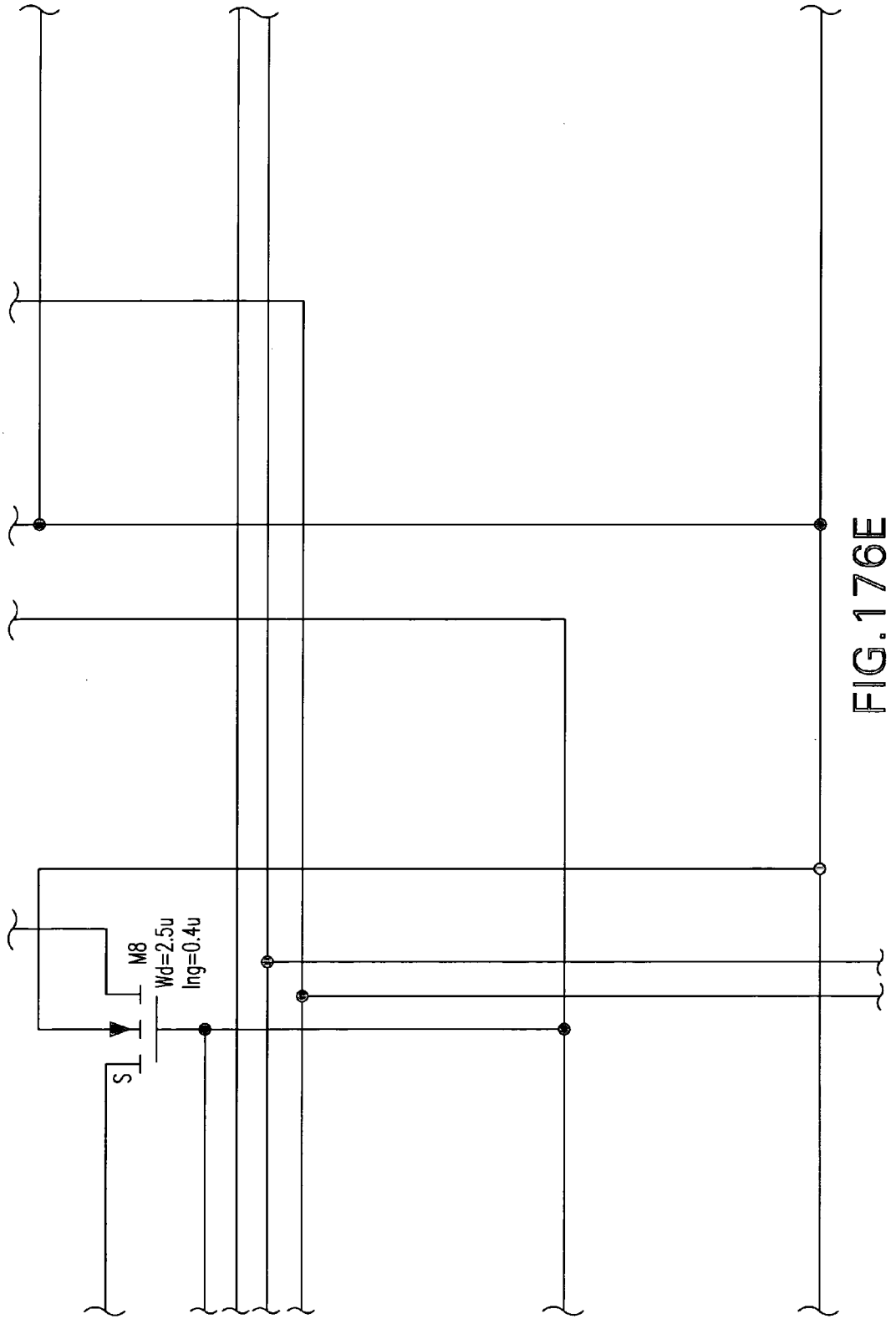


FIG. 176E

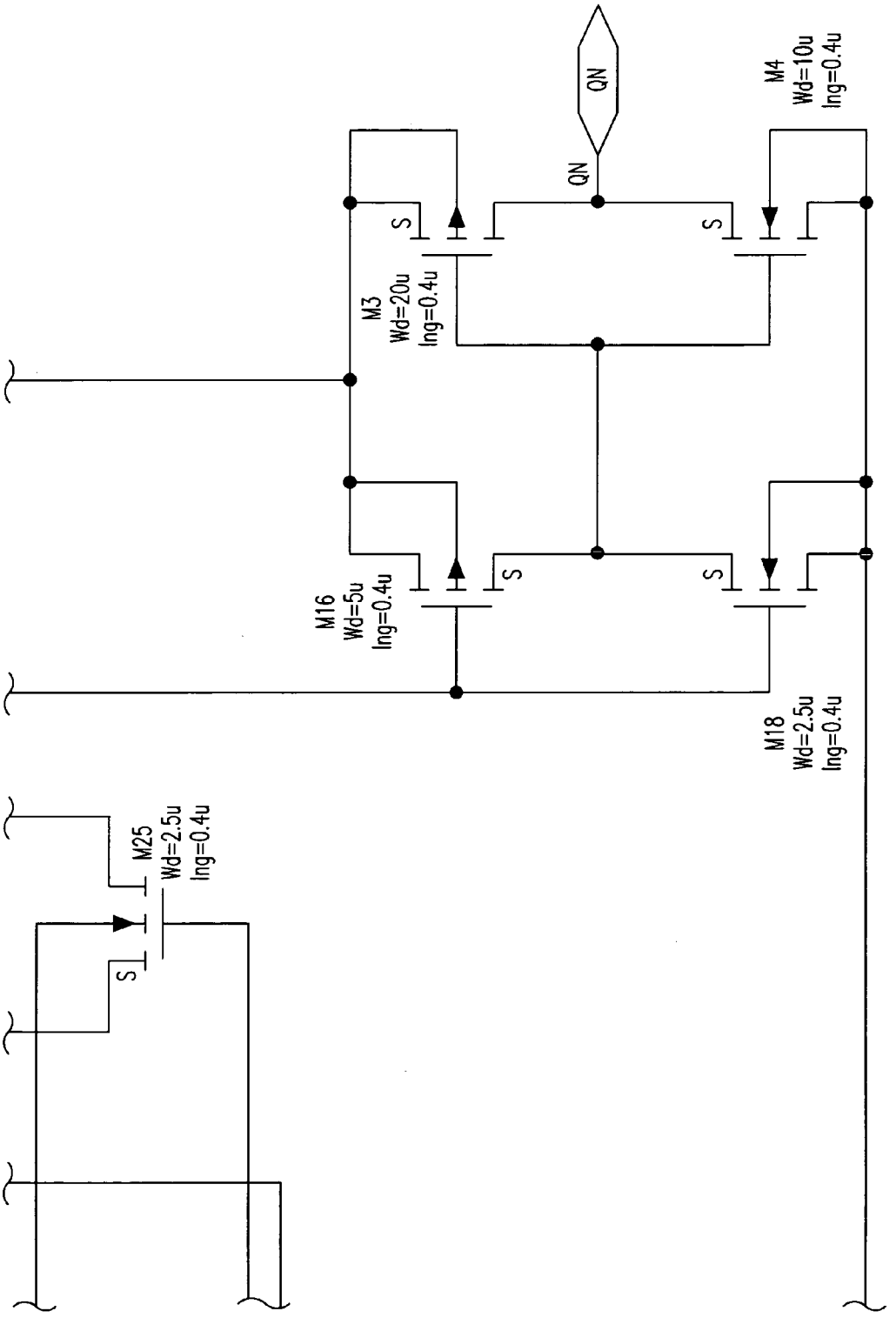

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S

FIG.176F

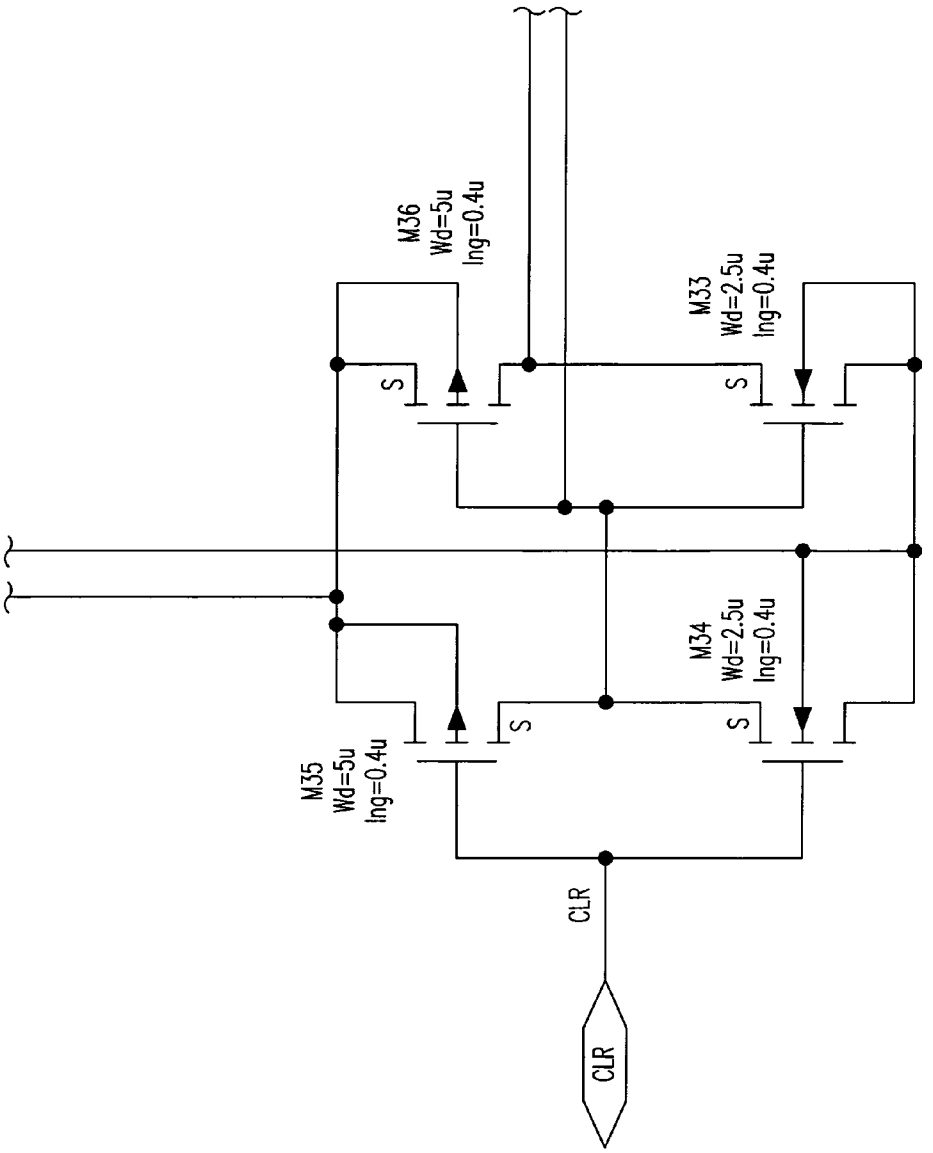
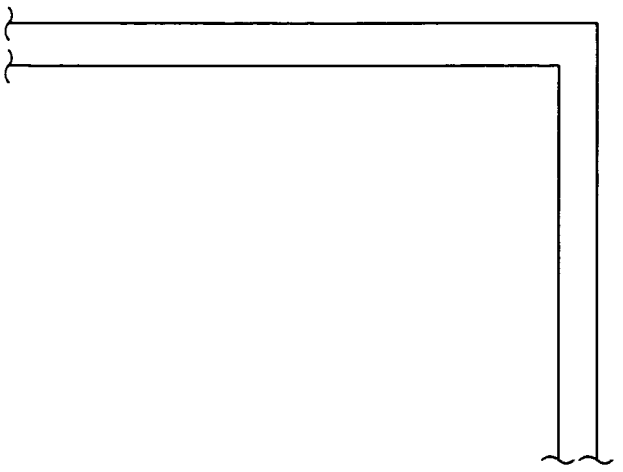

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
S
S
M34
Wd=2.5u
lng=0.4u
M35
Wd=5u
lng=0.4u
S
S
CLR
CLR

FIG.176G

FIG. 176H



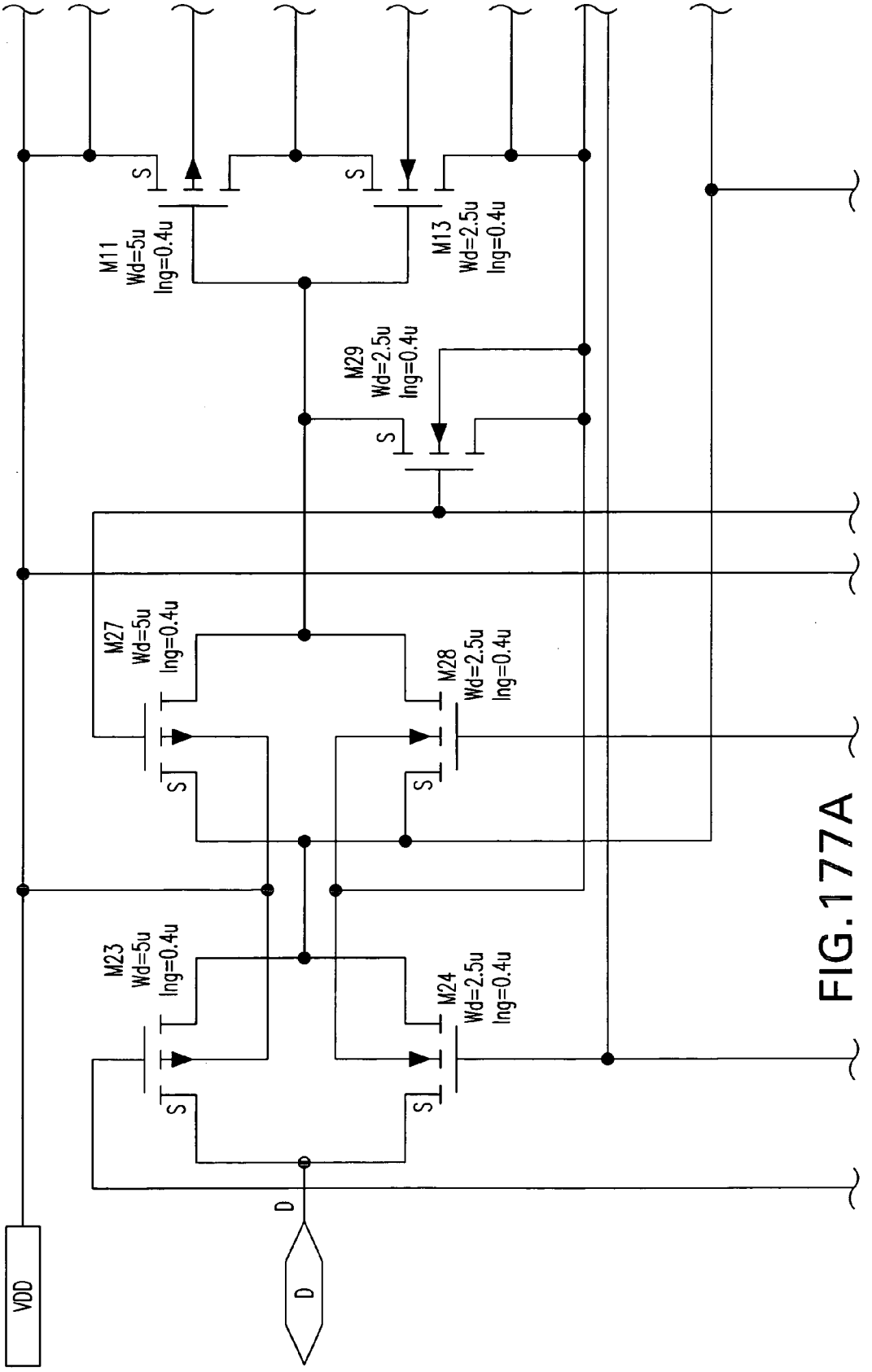

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.177A

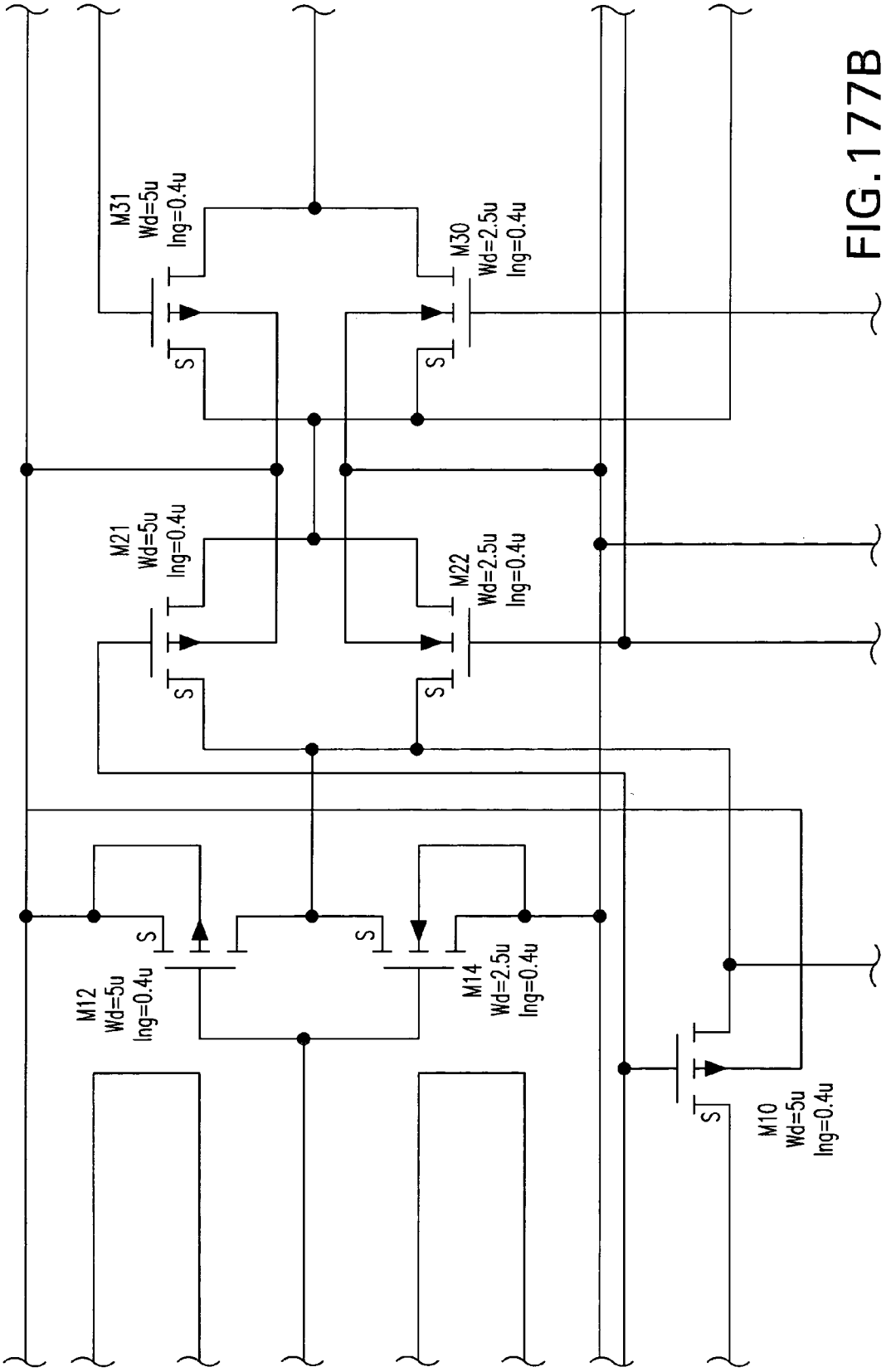

M31
Wd=5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
S

FIG. 177B

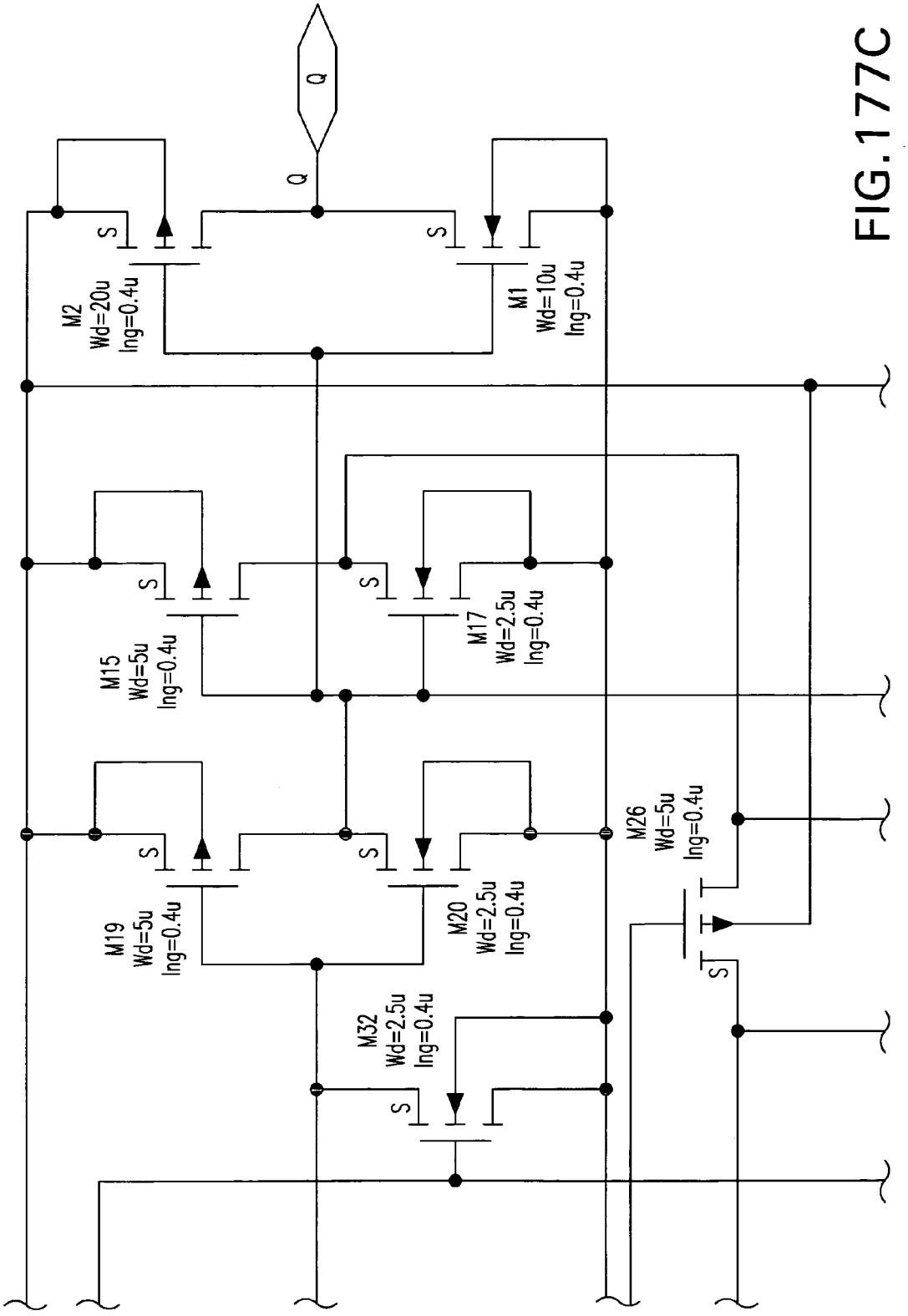

Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S

FIG.177C

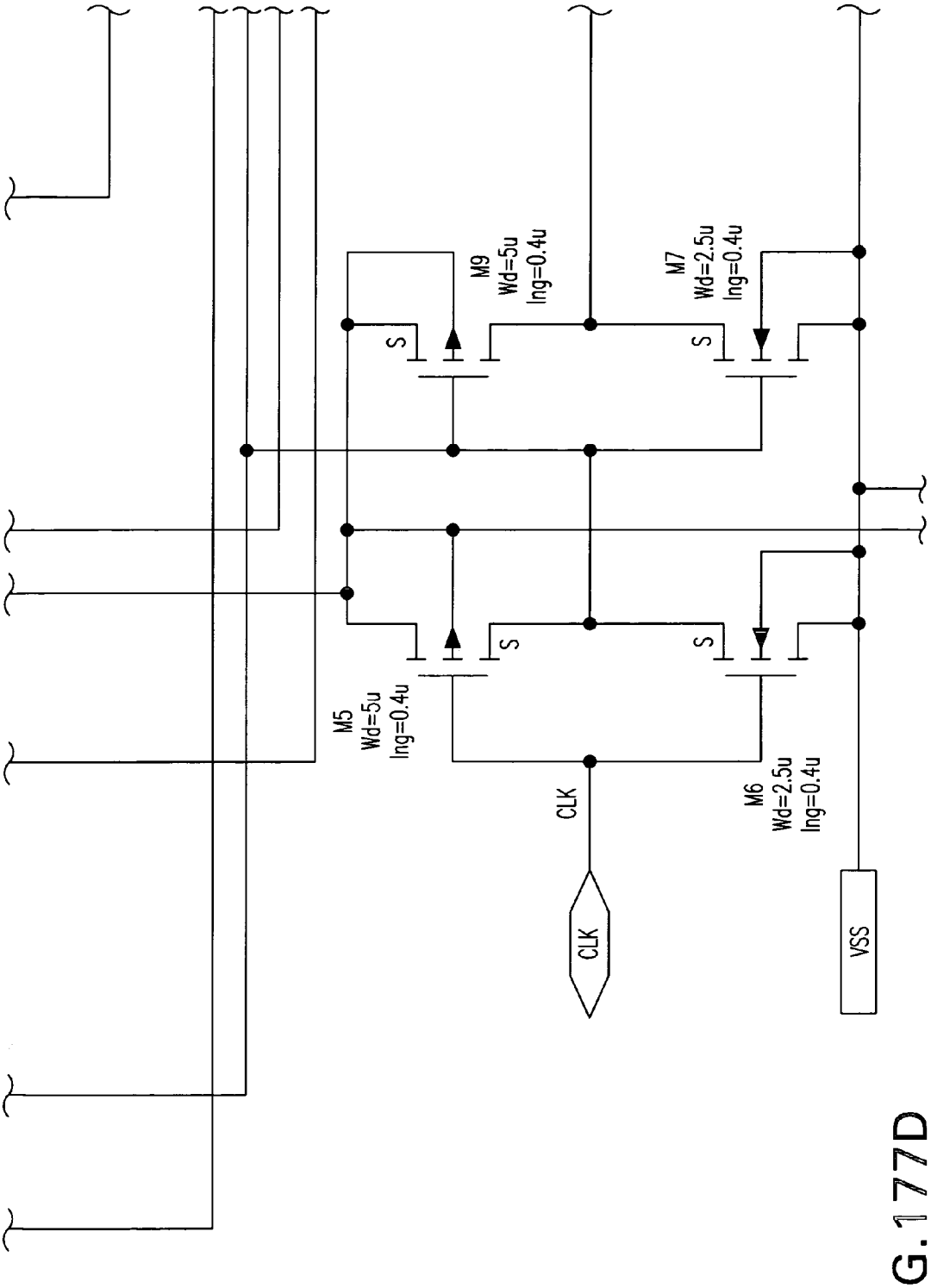

M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
CLK
CLK
VSS

FIG. 177D

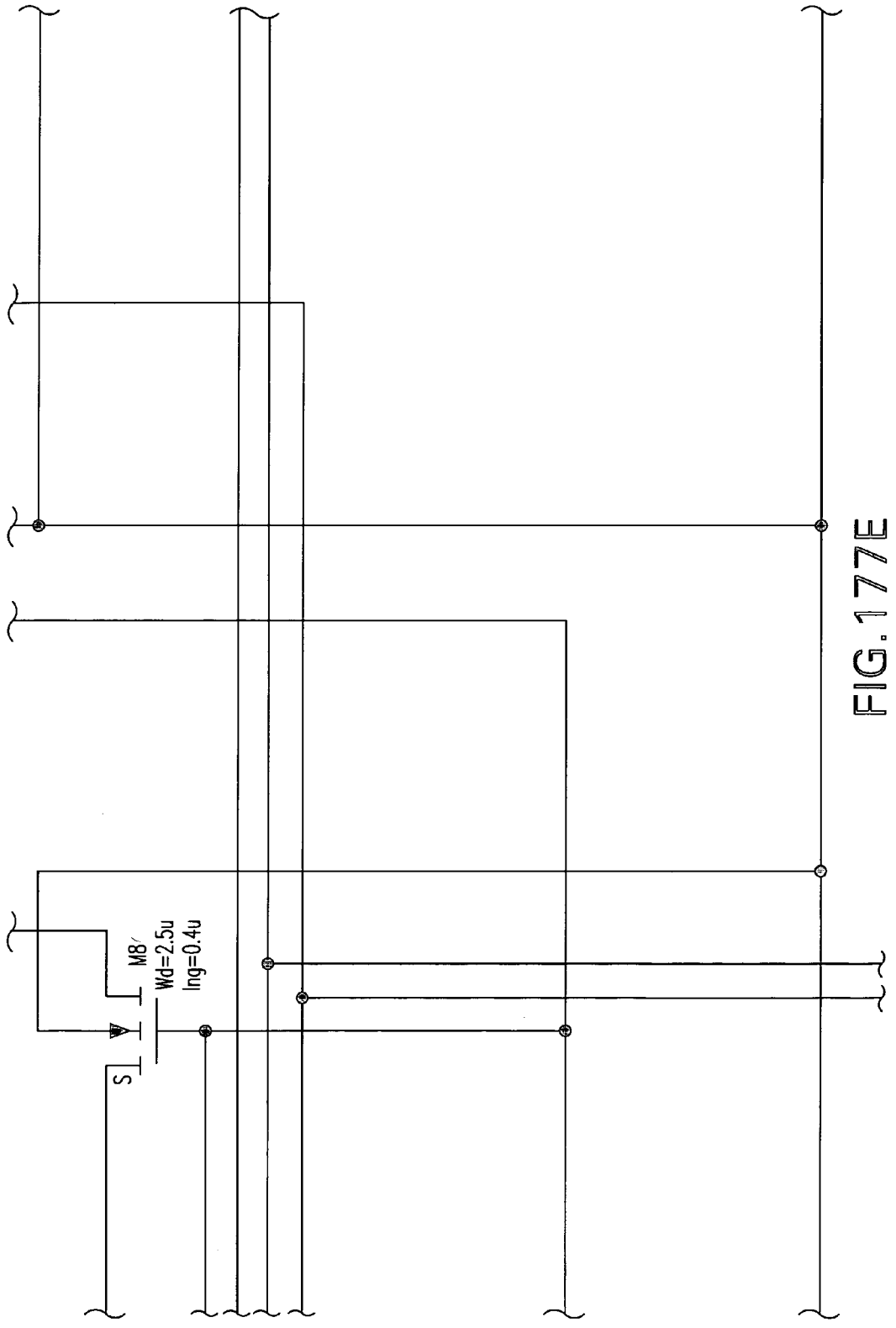


FIG. 177E

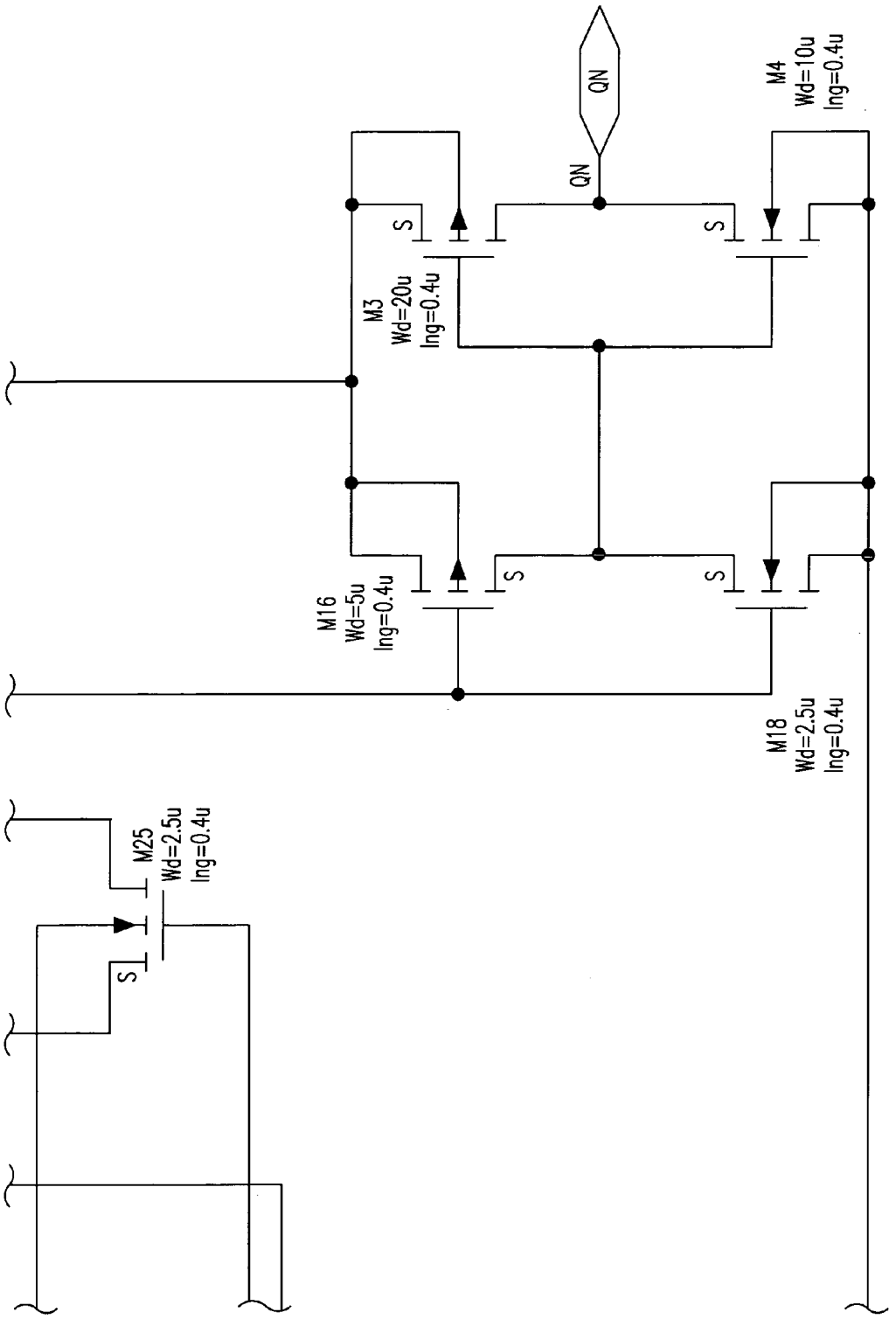

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S
S
S
S
S

FIG. 177F

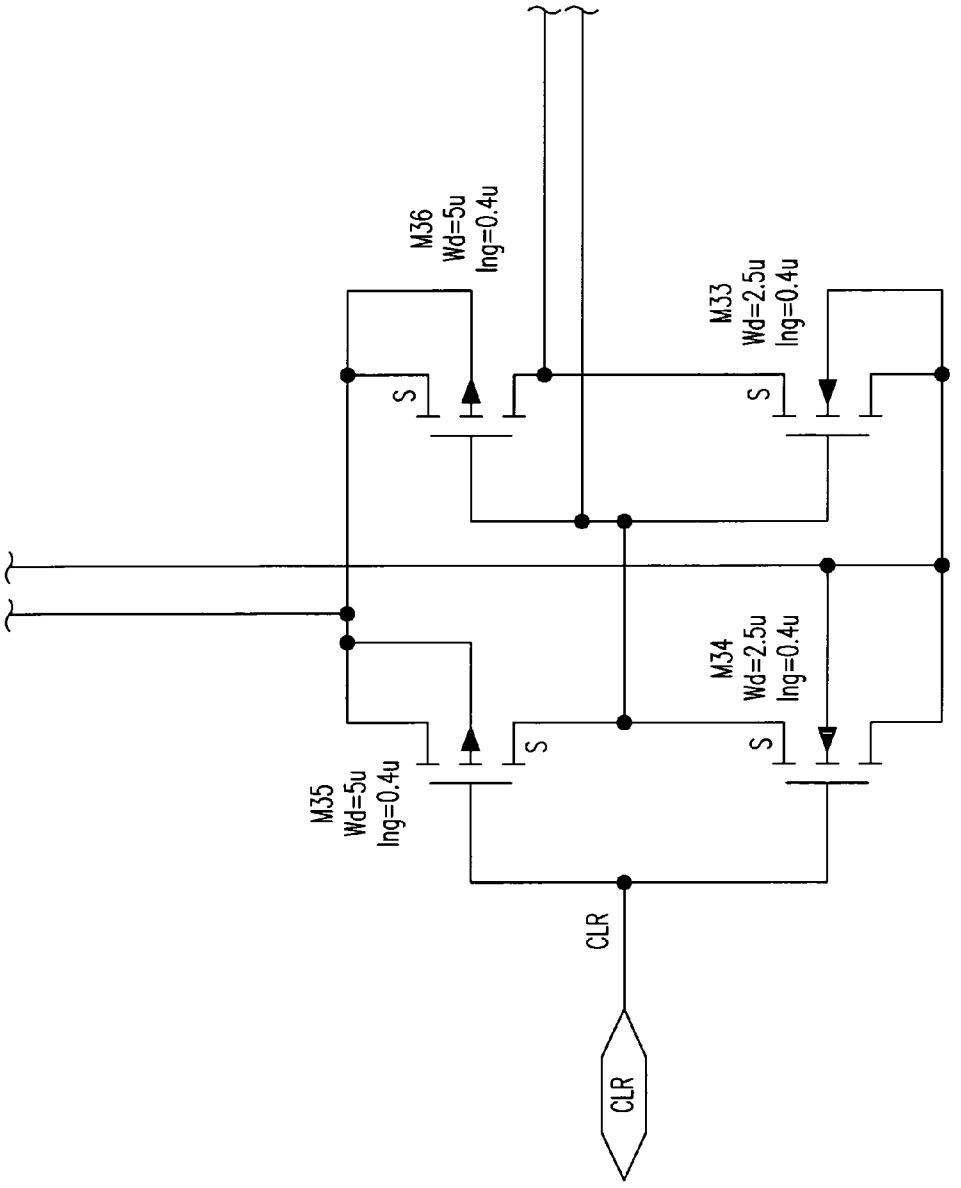
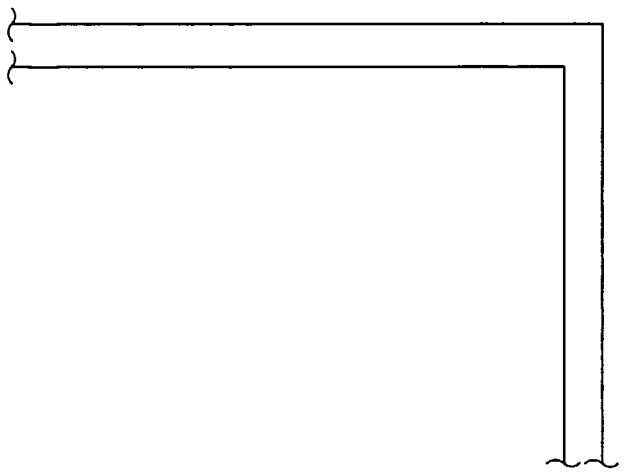

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
M34
Wd=2.5u
lng=0.4u
M35
Wd=5u
lng=0.4u
S
CLR
CLR

FIG.177G

FIG. 177H



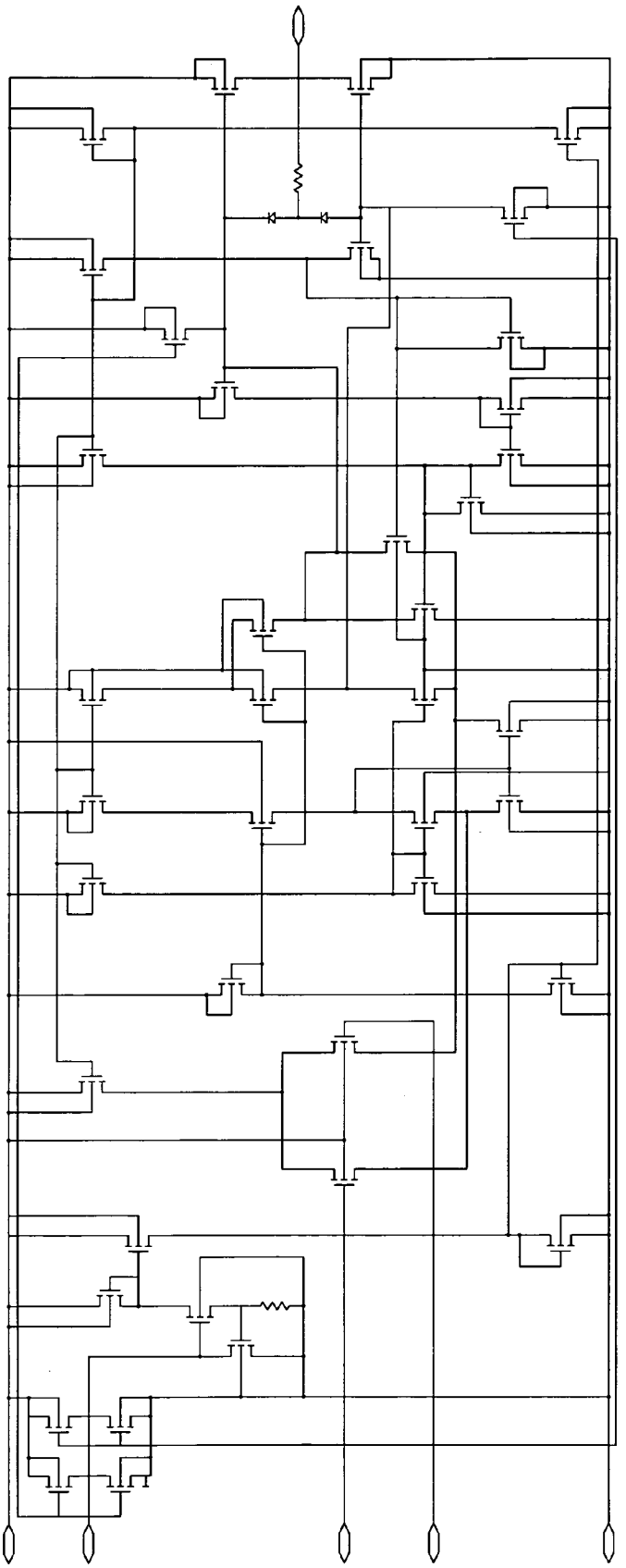


FIG. 178

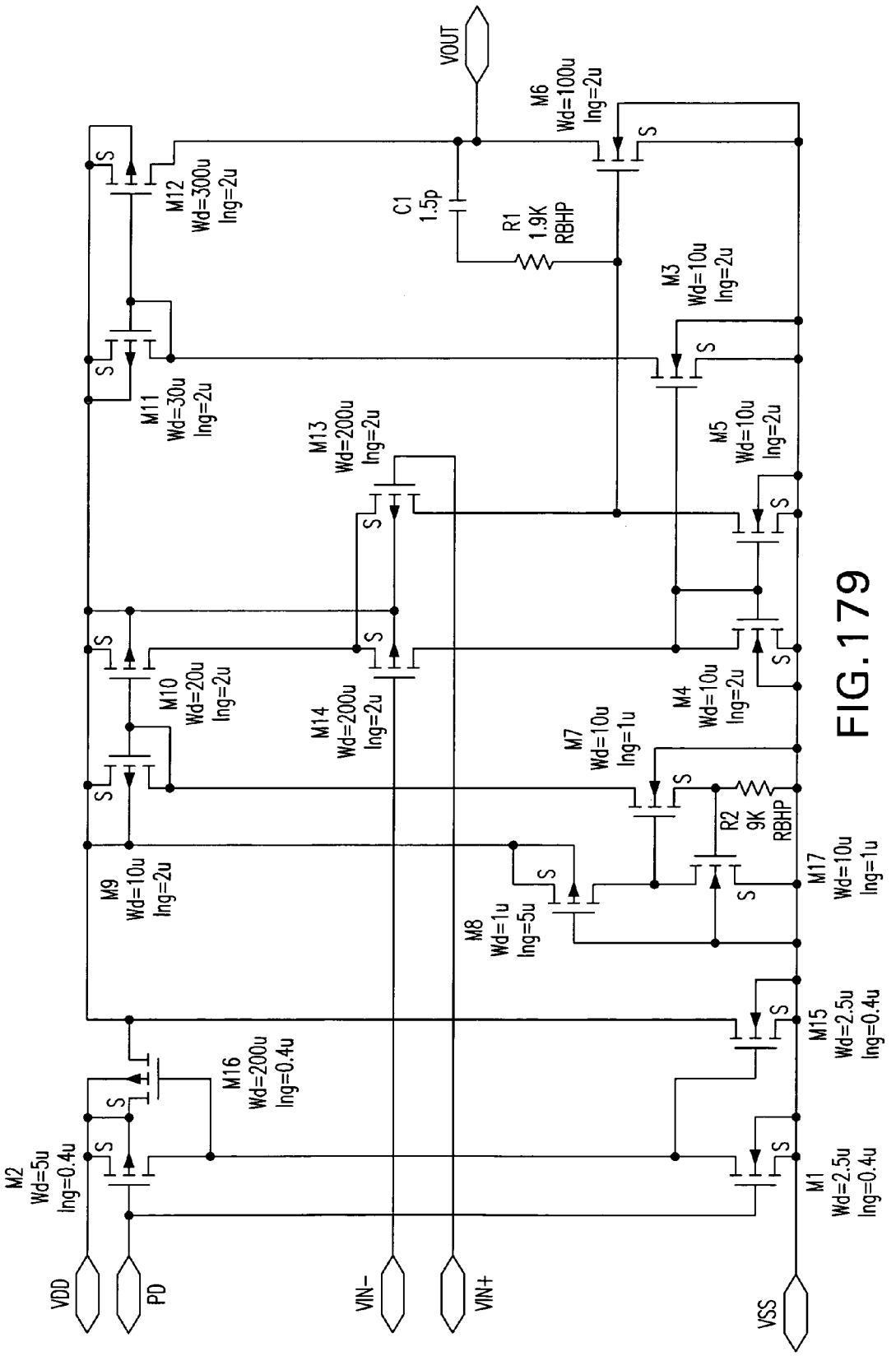

VOUT
M6 Wd=100u lng=2u
M12 Wd=300u lng=2u
C1 1.5p
R1 1.9K RBHP
M3 Wd=10u lng=2u
M11 Wd=30u lng=2u
M13 Wd=200u lng=2u
M5 Wd=10u lng=2u
M10 Wd=20u lng=2u
M14 Wd=200u lng=2u
M4 Wd=10u lng=2u
M7 Wd=10u lng=1u
R2 9K RBHP
M9 Wd=10u lng=2u
M8 Wd=1u lng=5u
M17 Wd=10u lng=1u
M15 Wd=2.5u lng=0.4u
M16 Wd=200u lng=0.4u
M2 Wd=5u lng=0.4u
M1 Wd=2.5u lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG. 179

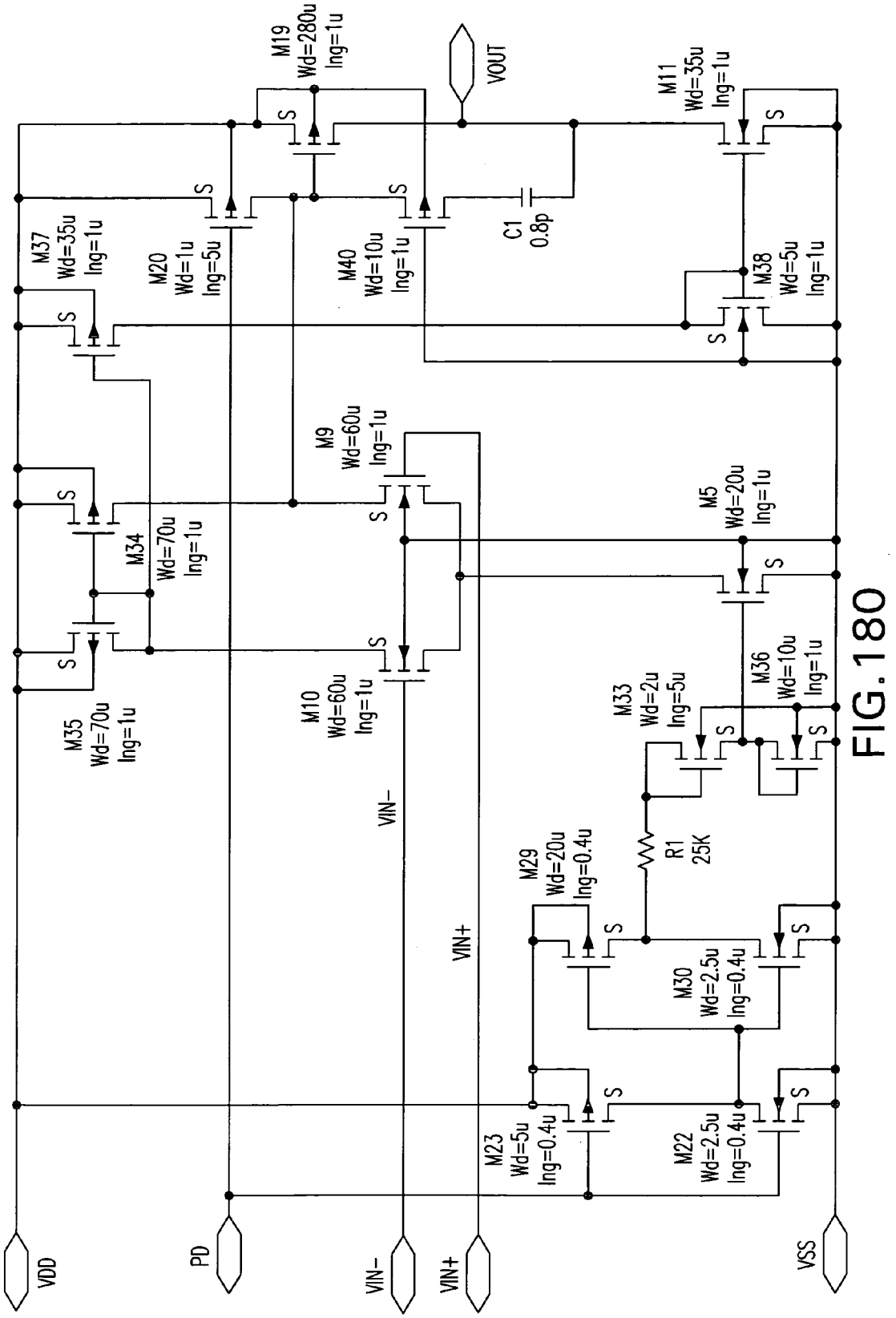

M19
Wd=280u
lng=1u
VOUT
M11
Wd=35u
lng=1u
M37
Wd=35u
lng=1u
M20
Wd=1u
lng=5u
M40
Wd=10u
lng=1u
C1
0.8p
M38
Wd=5u
lng=1u
M9
Wd=60u
lng=1u
M5
Wd=20u
lng=1u
M34
Wd=70u
lng=1u
M35
Wd=70u
lng=1u
M10
Wd=60u
lng=1u
M33
Wd=2u
lng=5u
M36
Wd=10u
lng=1u
VIN-
R1
25K
M29
Wd=20u
lng=0.4u
VIN+
M30
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
VDD
PD
VIN-
VIN+
VSS

FIG. 180

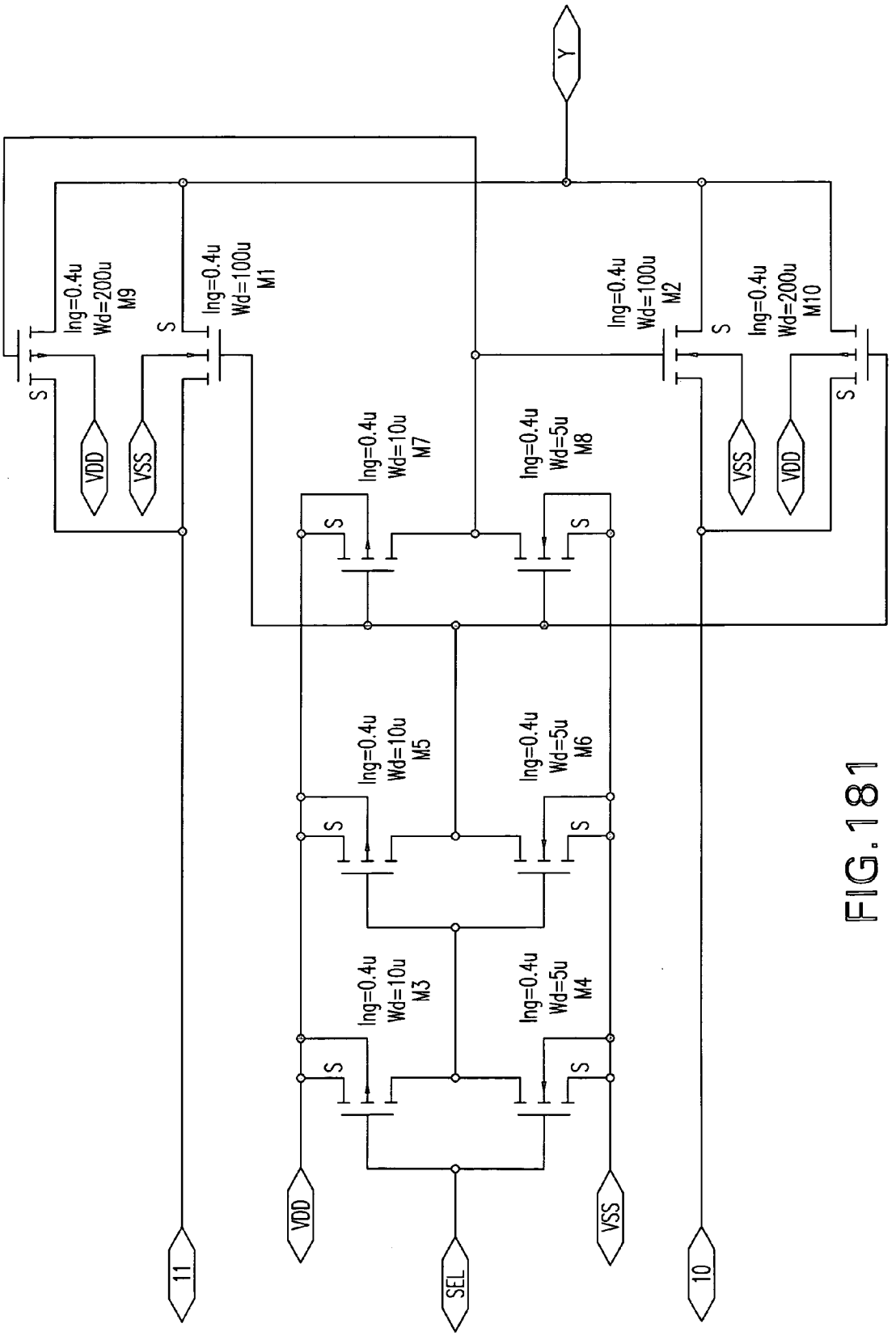

Y
lng=0.4u
Wd=200u
M9
lng=0.4u
Wd=100u
M1
lng=0.4u
Wd=100u
M2
lng=0.4u
Wd=200u
M10
lng=0.4u
Wd=10u
M7
lng=0.4u
Wd=5u
M8
lng=0.4u
Wd=10u
M5
lng=0.4u
Wd=5u
M6
lng=0.4u
Wd=10u
M3
lng=0.4u
Wd=5u
M4
S
VDD
VSS
11
SEL
10

FIG. 181

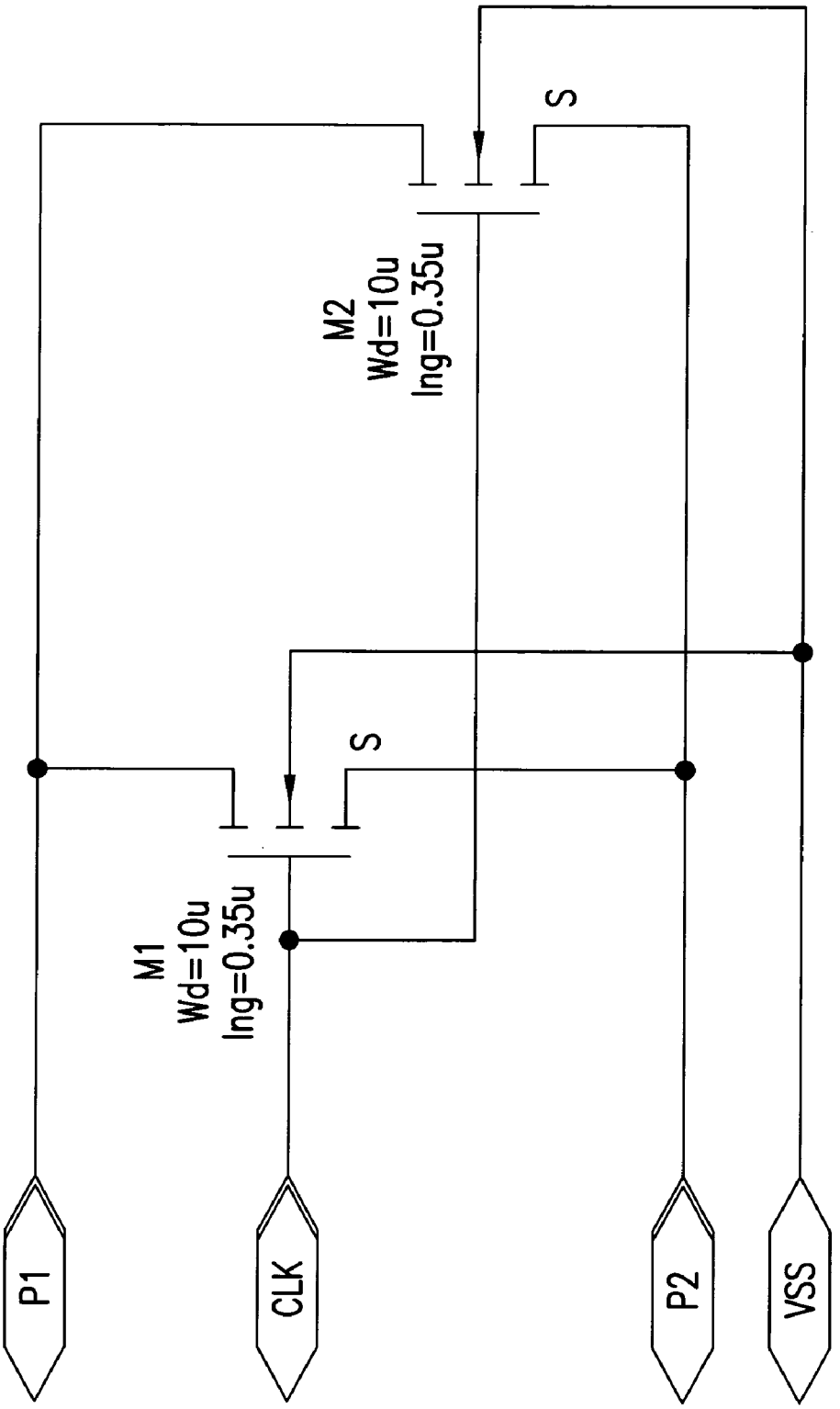


FIG.182

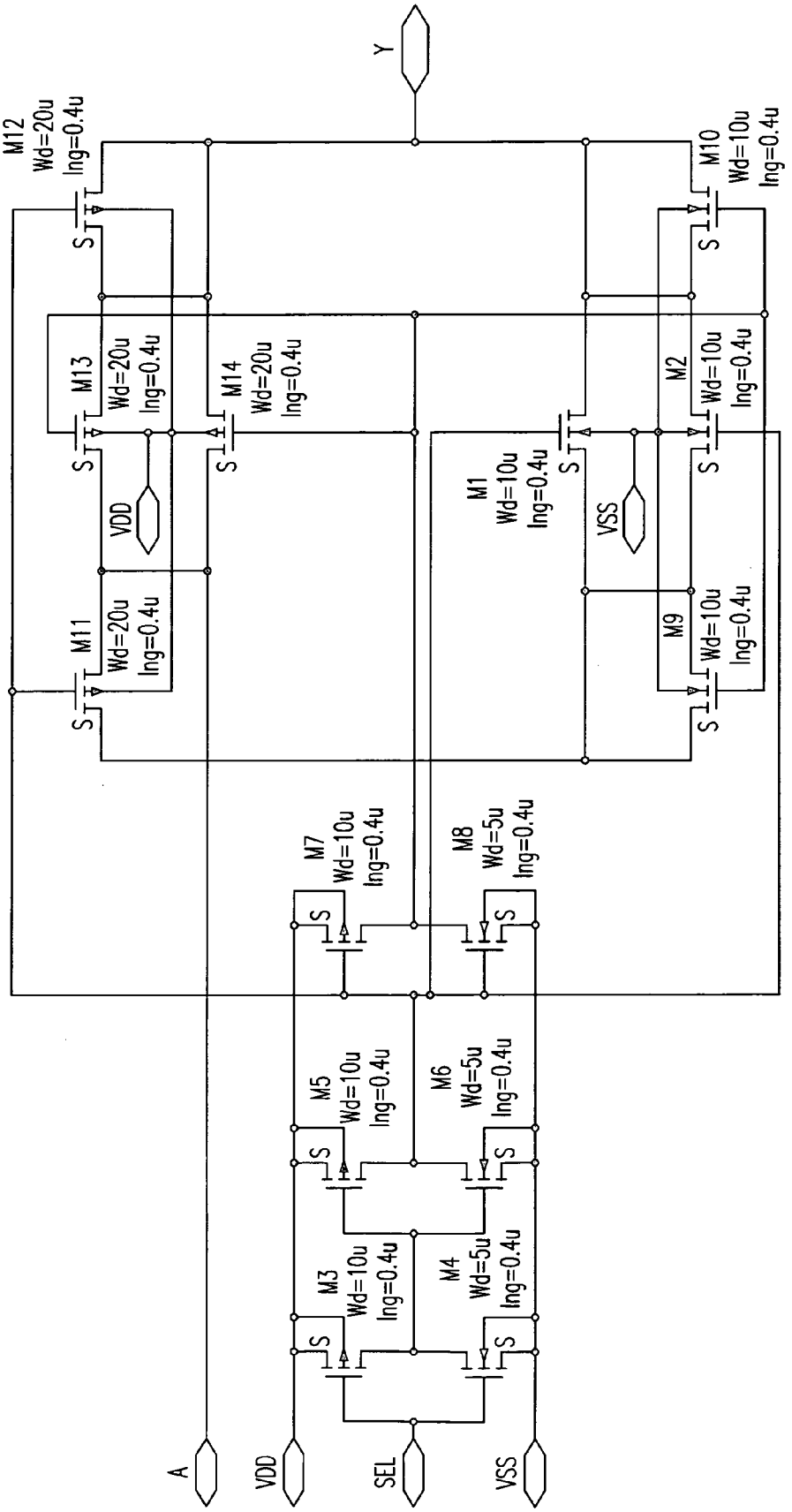

Y
M12 Wd=20u lng=0.4u
M10 Wd=10u lng=0.4u
M13 Wd=20u lng=0.4u
M14 Wd=20u lng=0.4u
M2 Wd=10u lng=0.4u
M1 Wd=10u lng=0.4u
VDD
VSS
M11 Wd=20u lng=0.4u
M9 Wd=10u lng=0.4u
M7 Wd=10u lng=0.4u
M8 Wd=5u lng=0.4u
M5 Wd=10u lng=0.4u
M6 Wd=5u lng=0.4u
M3 Wd=10u lng=0.4u
M4 Wd=5u lng=0.4u
S
A
VDD
SEL
VSS

FIG. 183

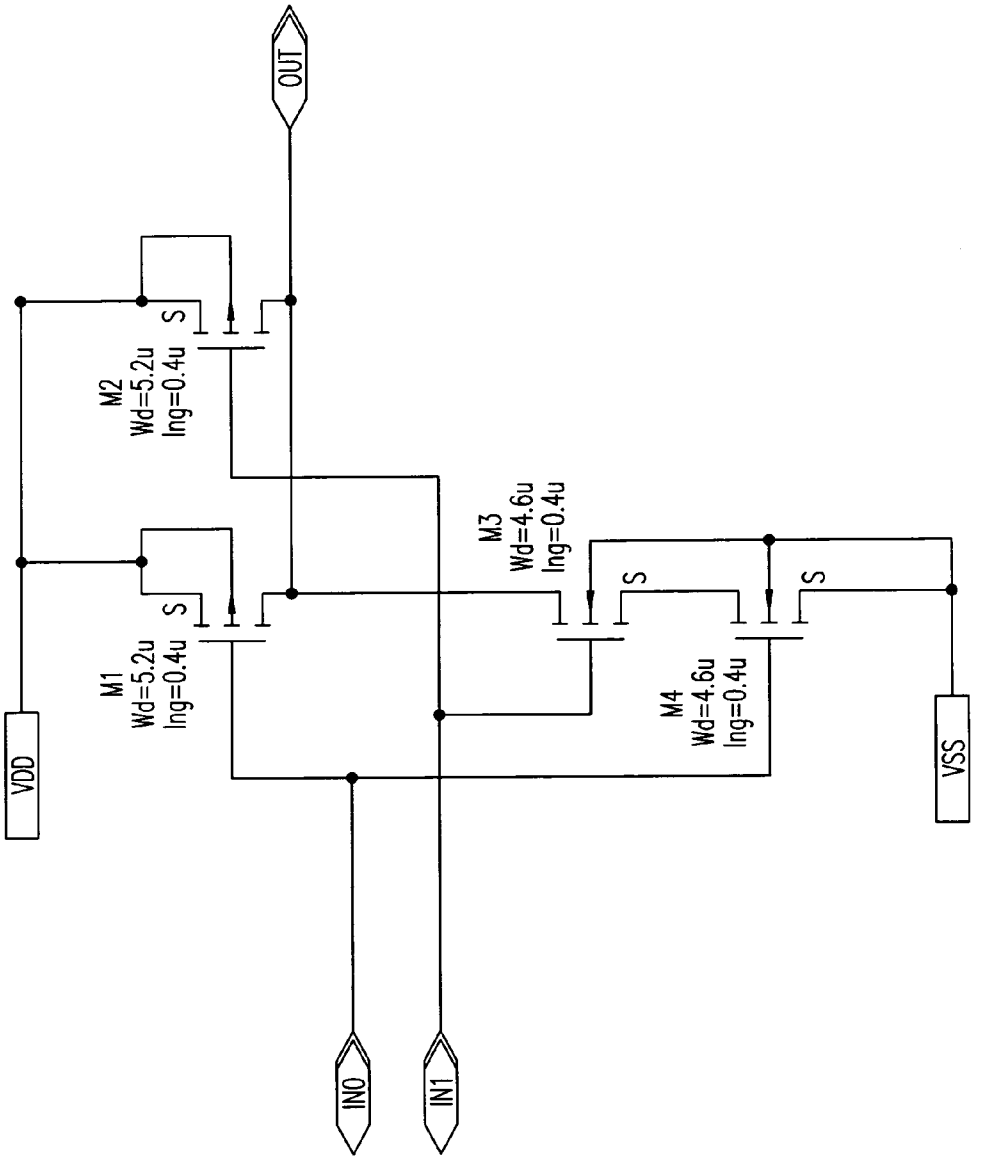

OUT
M2
Wd=5.2u
lng=0.4u
S
M3
Wd=4.6u
lng=0.4u
S
S
M1
Wd=5.2u
lng=0.4u
S
M4
Wd=4.6u
lng=0.4u
VDD
VSS
IN0
IN1

FIG.184

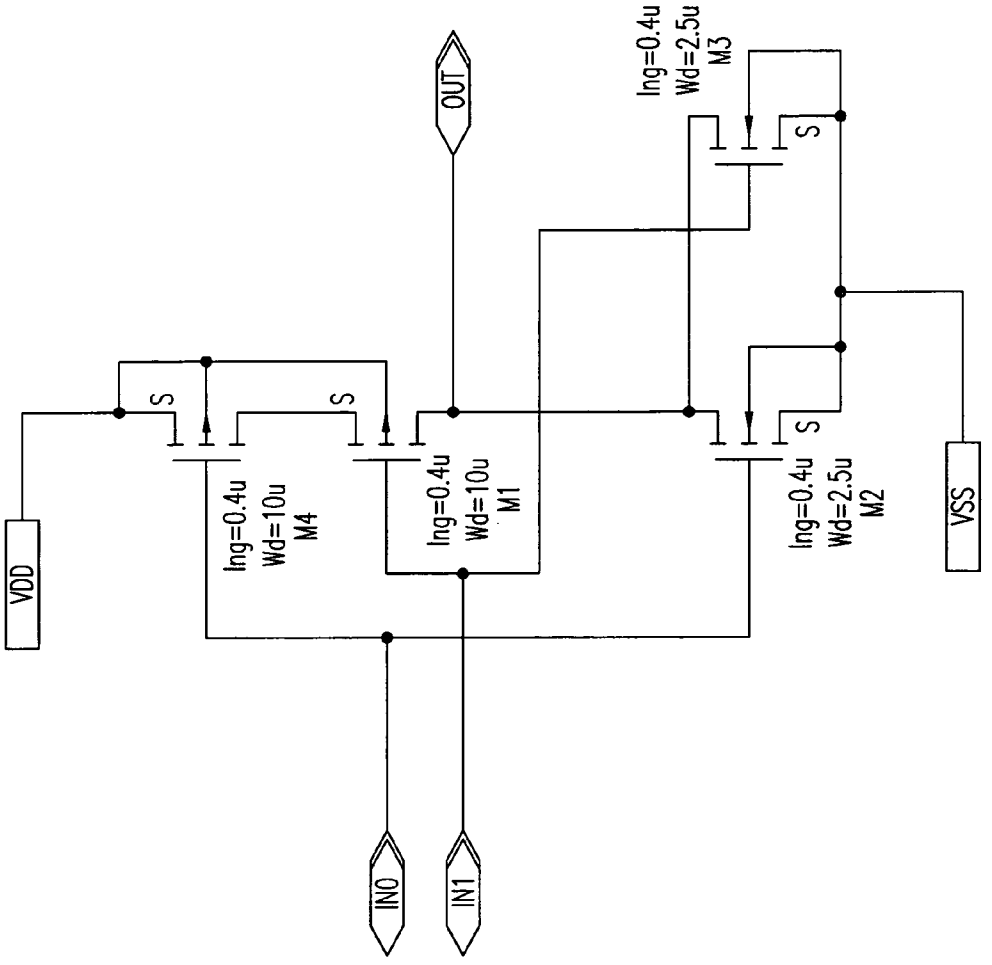

VDD
lng=0.4u
Wd=10u
M4
S
S
lng=0.4u
Wd=10u
M1
OUT
lng=0.4u
Wd=2.5u
M3
S
S
lng=0.4u
Wd=2.5u
M2
VSS
IN0
IN1

FIG.185

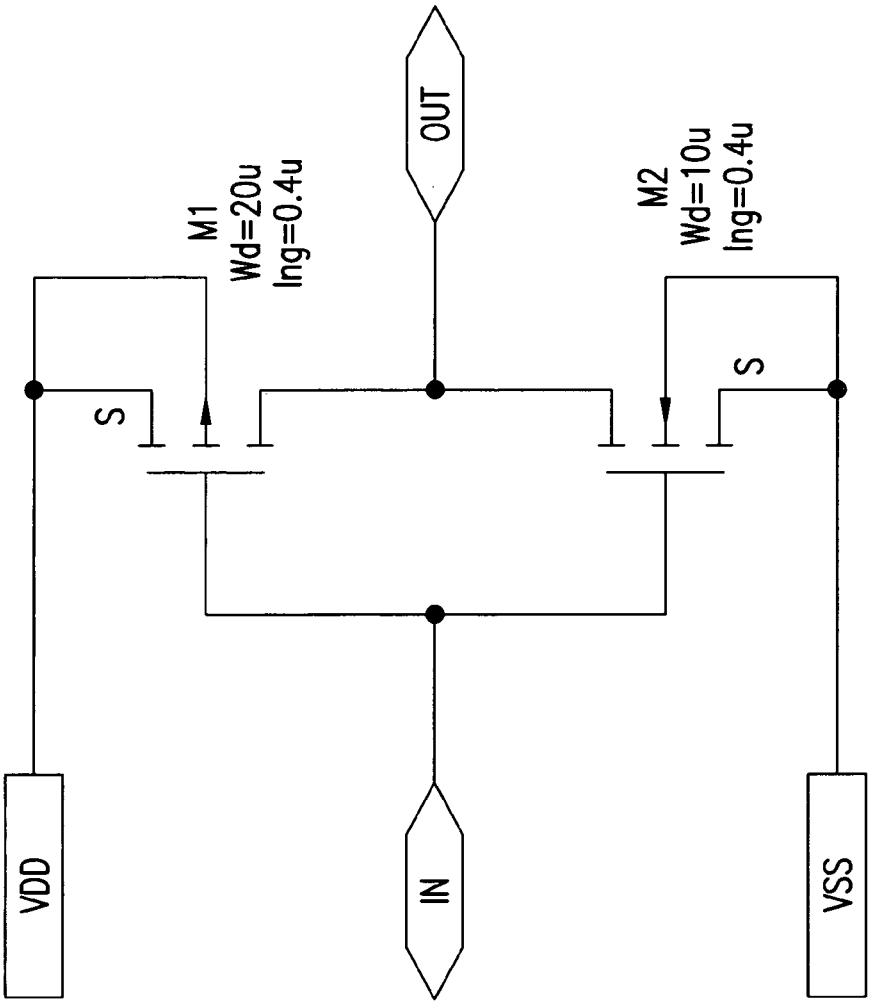


FIG.186

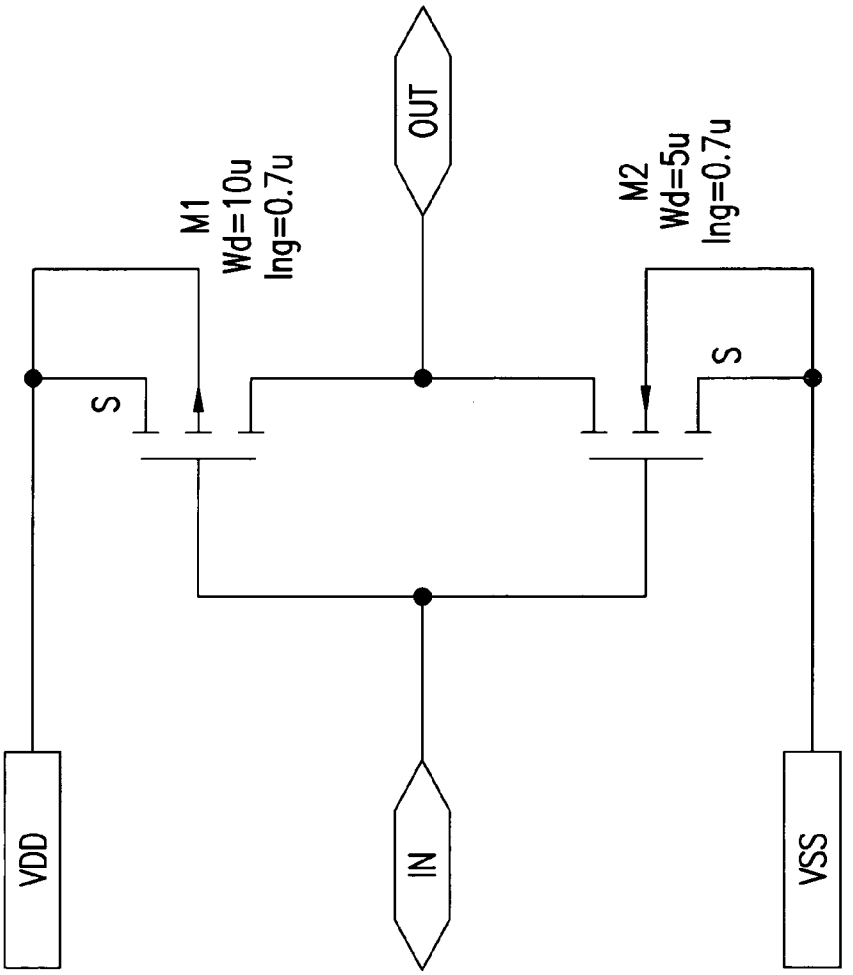


FIG.187

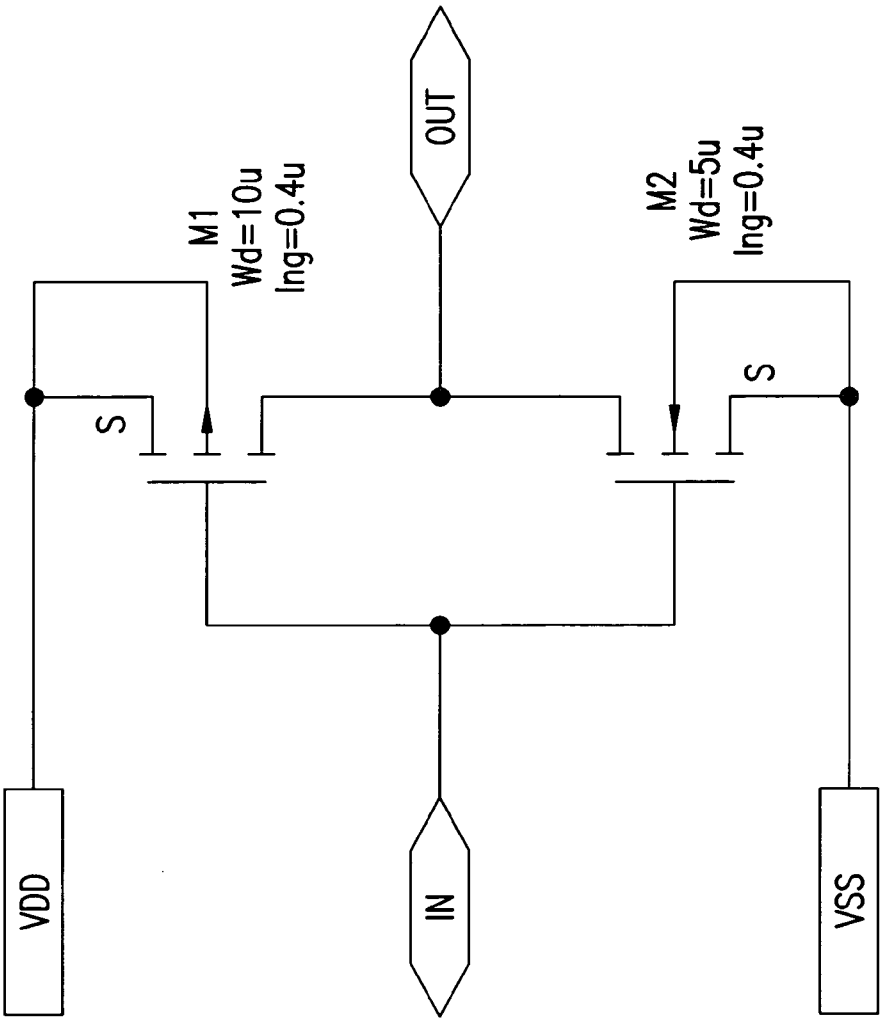


FIG. 188

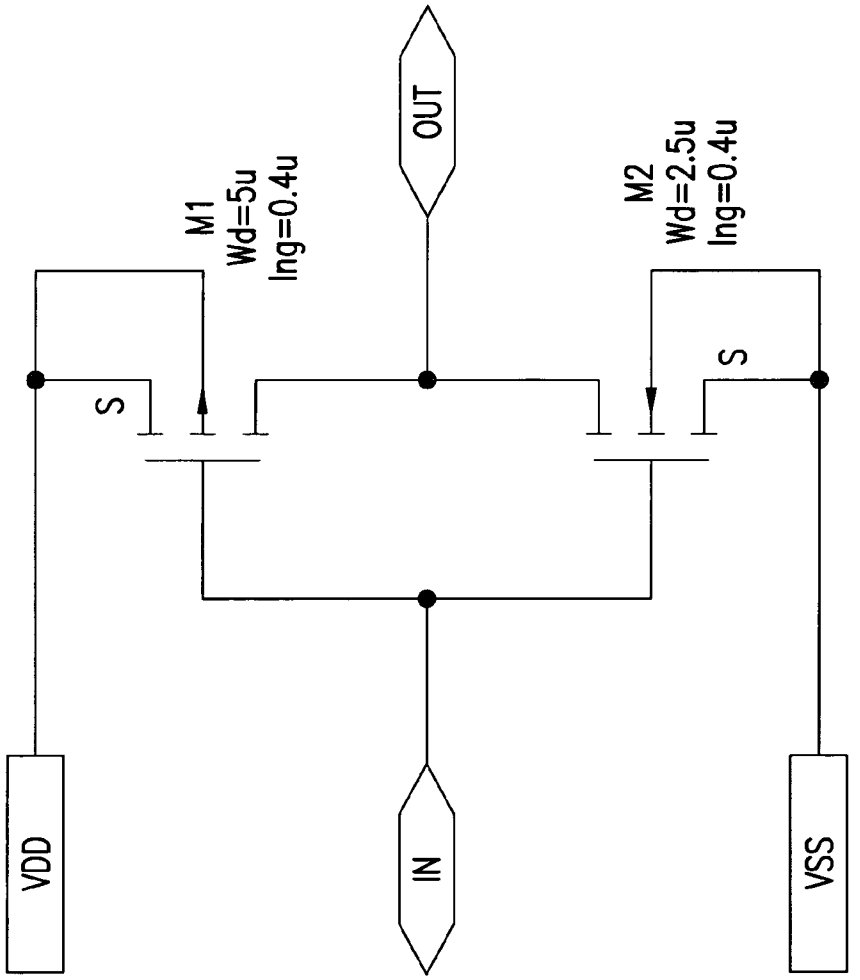


FIG.189

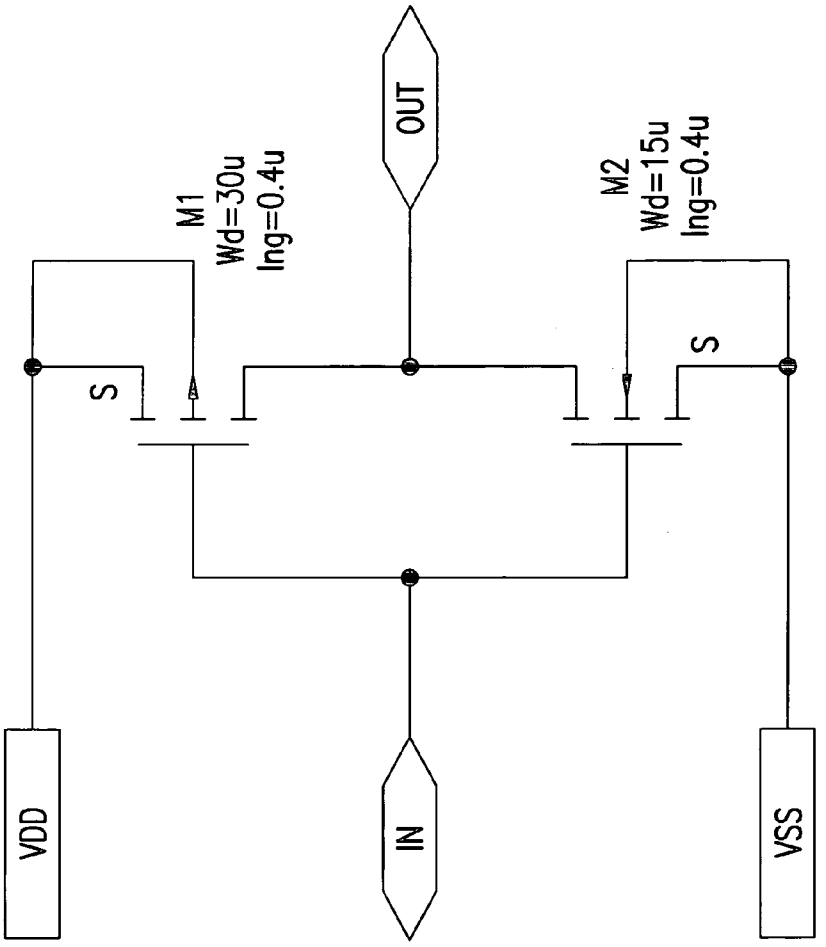


FIG. 190

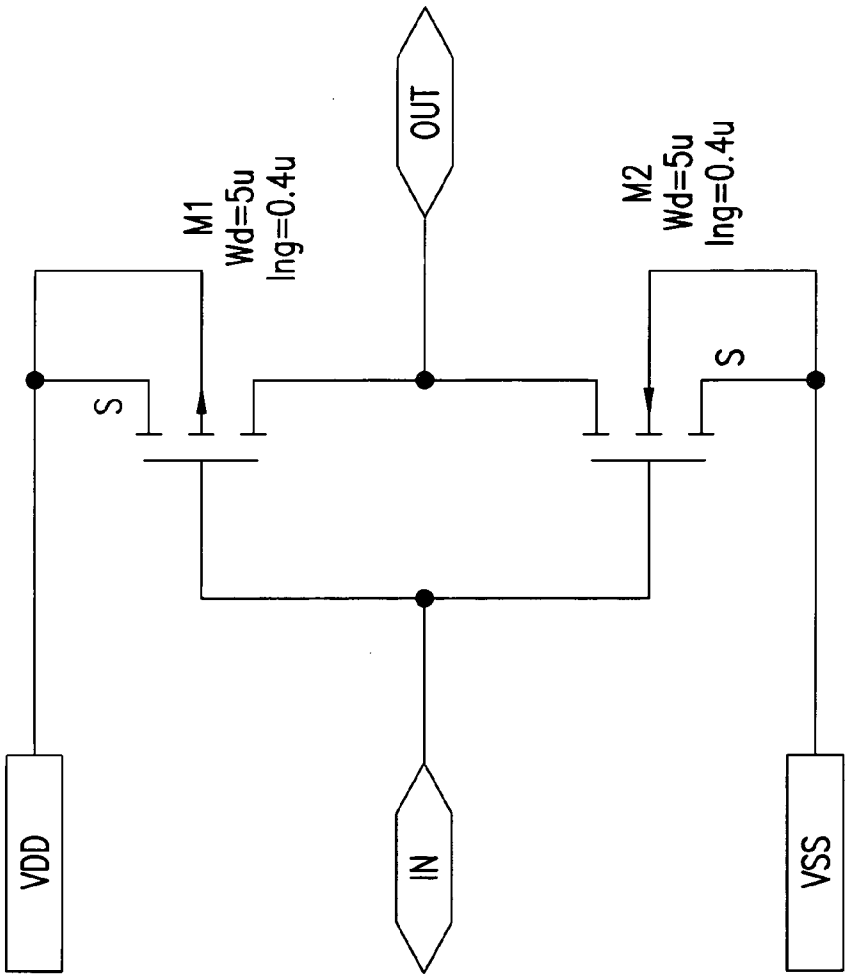


FIG. 191

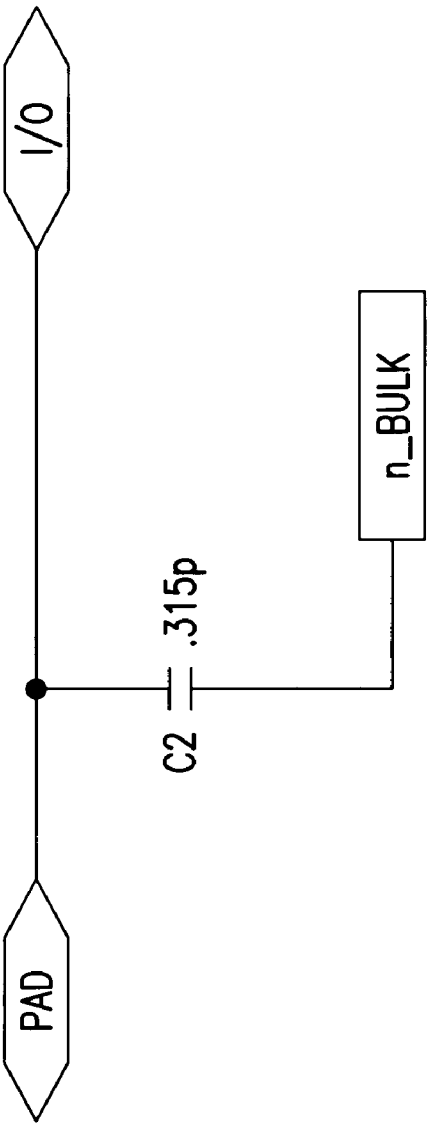


FIG. 192

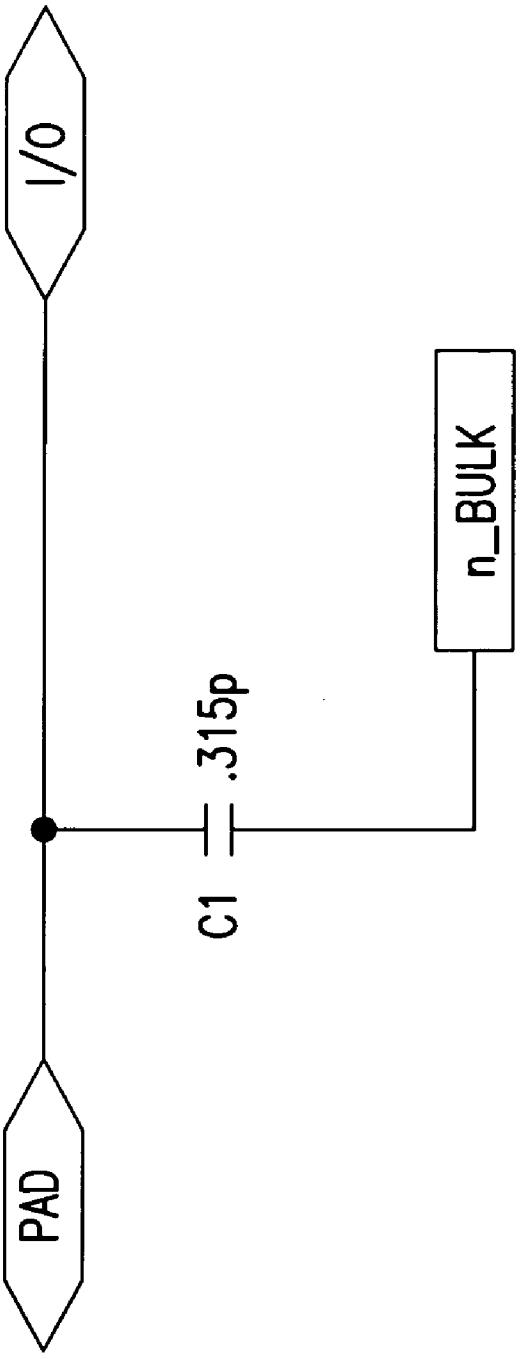


FIG. 193

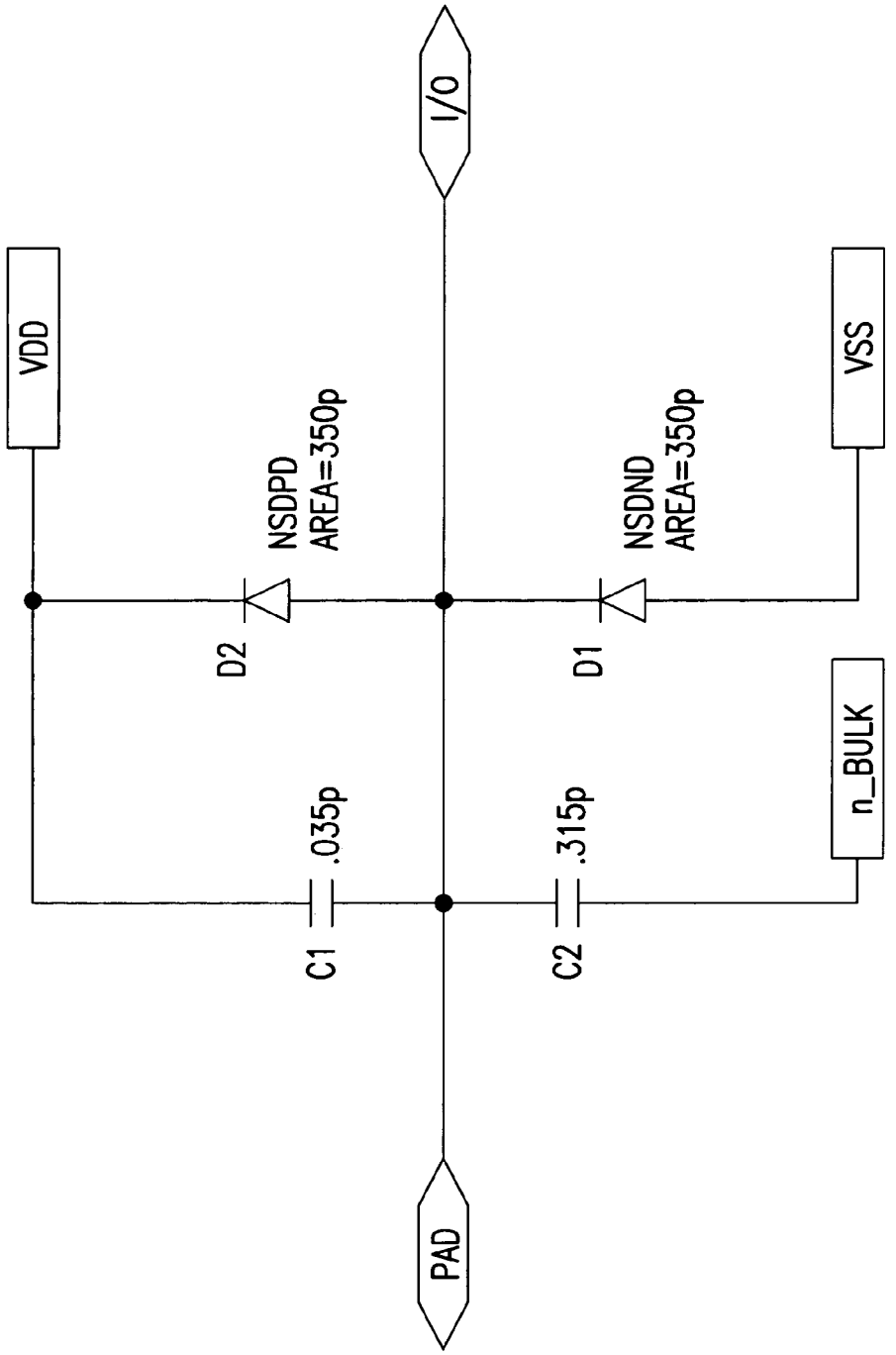

I/O
VDD
VSS
NSDPD
AREA=350p
NSDND
AREA=350p
D2
D1
n_BULK
.035p
.315p
C1
C2
PAD

FIG.194

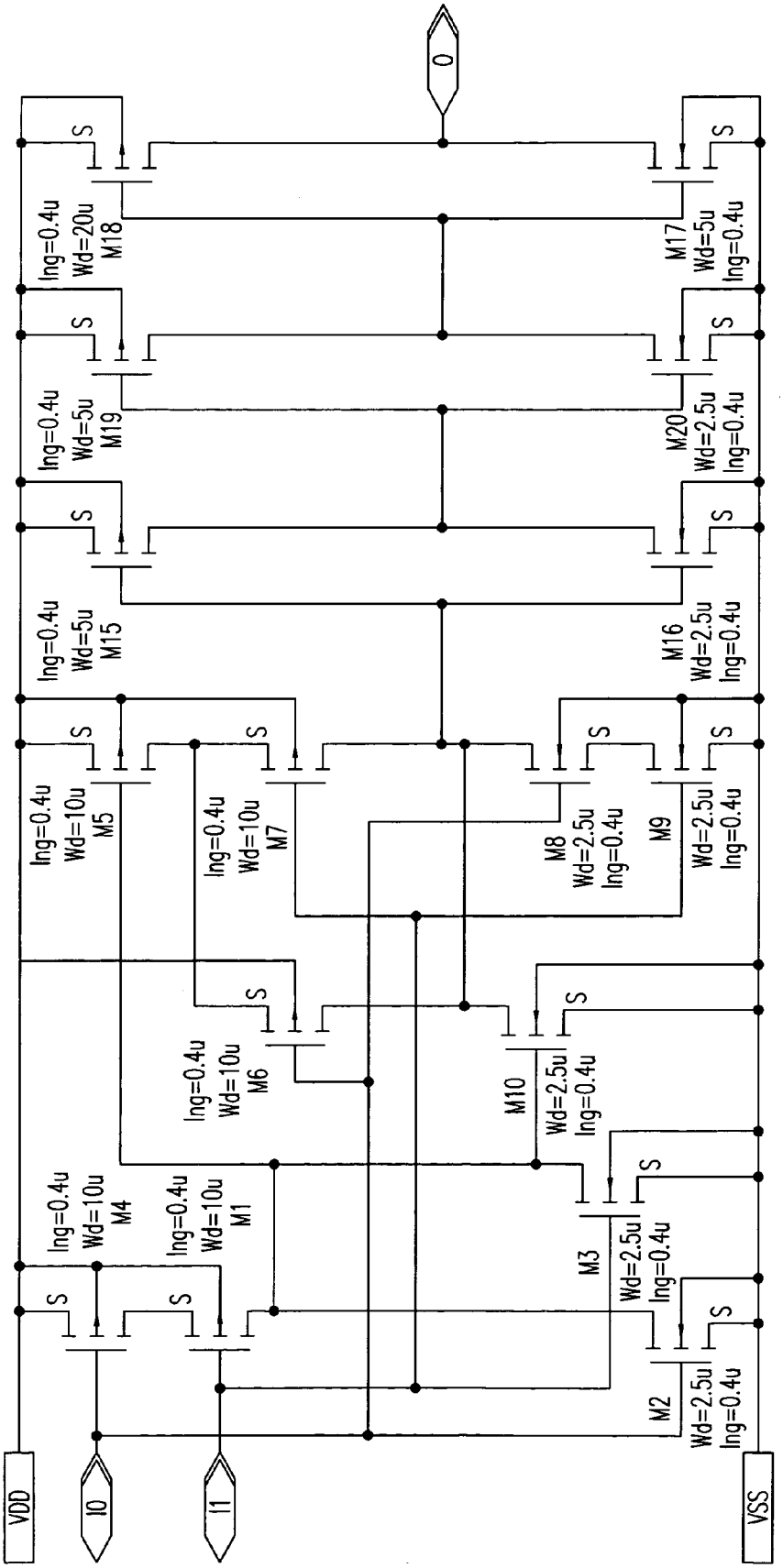

O
lng=0.4u Wd=20u M18
M17 Wd=5u lng=0.4u
lng=0.4u Wd=5u M19
M20 Wd=2.5u lng=0.4u
lng=0.4u Wd=5u M15
M16 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M5
lng=0.4u Wd=10u M7
M8 Wd=2.5u lng=0.4u
M9 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M6
M10 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M4
lng=0.4u Wd=10u M1
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
VDD
I0
I1
VSS

FIG. 195

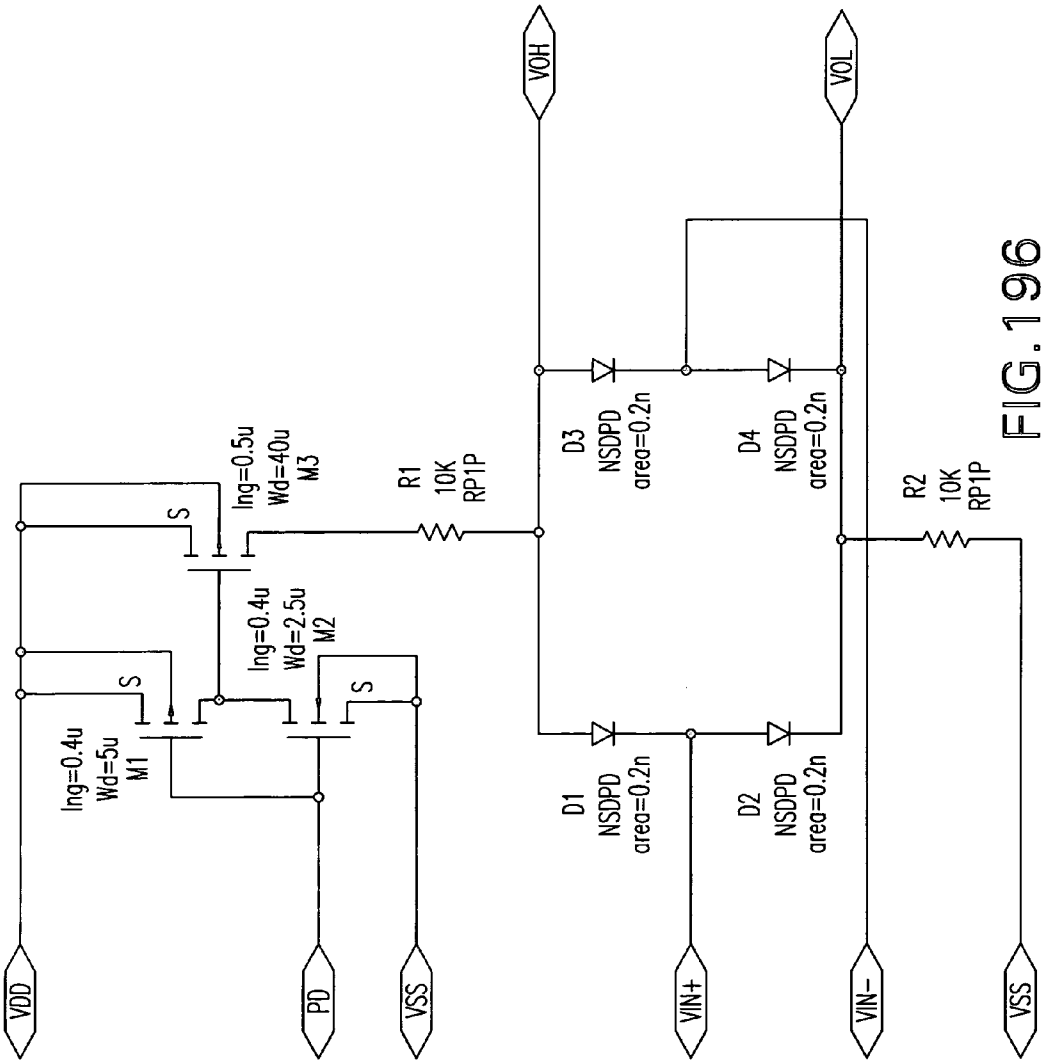

VOH
VOL
D3
NSDPD
area=0.2n
D4
NSDPD
area=0.2n
R1
10K
RP1P
R2
10K
RP1P
lng=0.5u
Wd=40u
M3
S
lng=0.4u
Wd=2.5u
M2
S
S
lng=0.4u
Wd=5u
M1
D1
NSDPD
area=0.2n
D2
NSDPD
area=0.2n
VDD
PD
VSS
VIN+
VIN-
VSS

FIG. 196

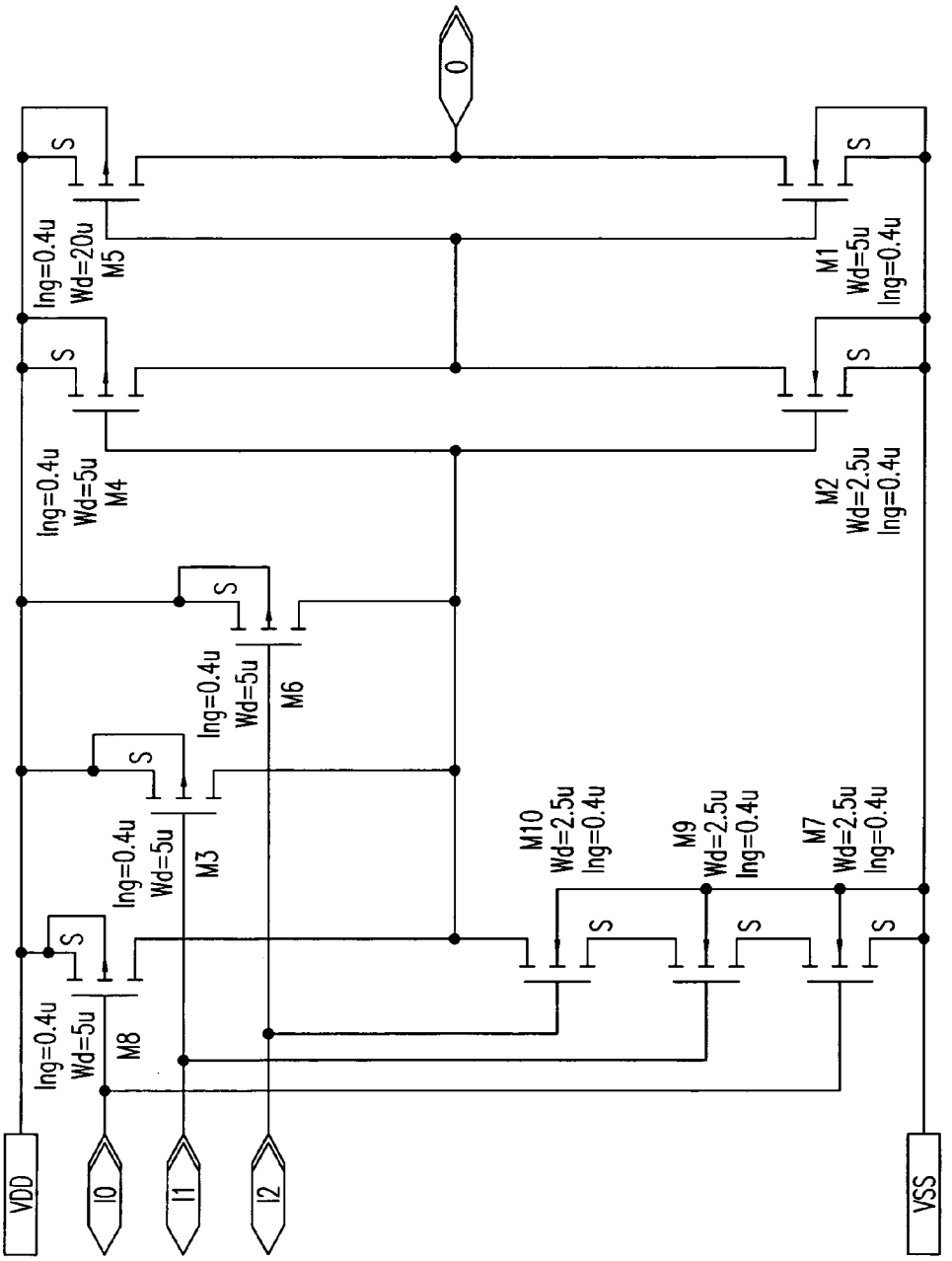

O
S
lng=0.4u
Wd=20u
M5
M1
Wd=5u
lng=0.4u
M4
M2
Wd=2.5u
M6
M3
M10
M9
M7
M8
VDD
I0
I1
I2
VSS

FIG. 197

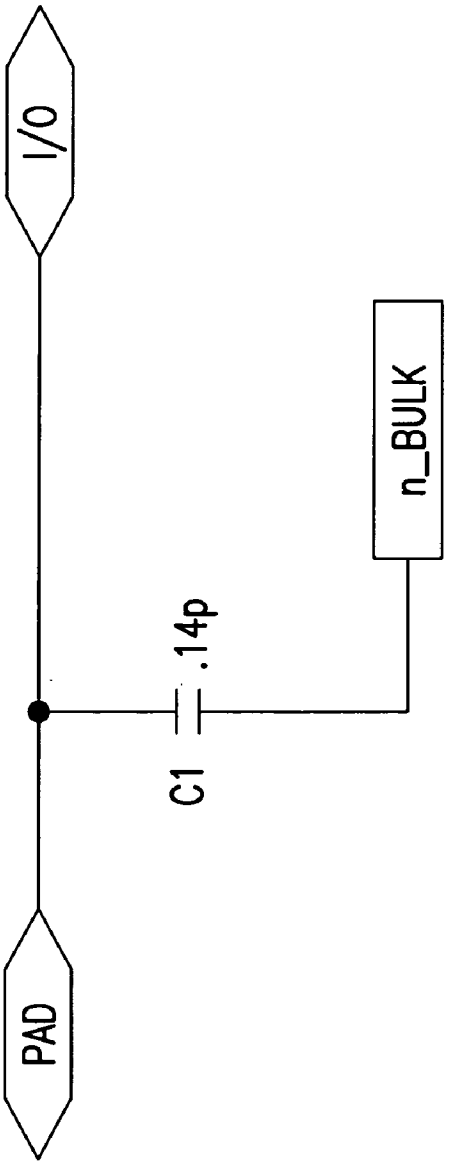


FIG. 198

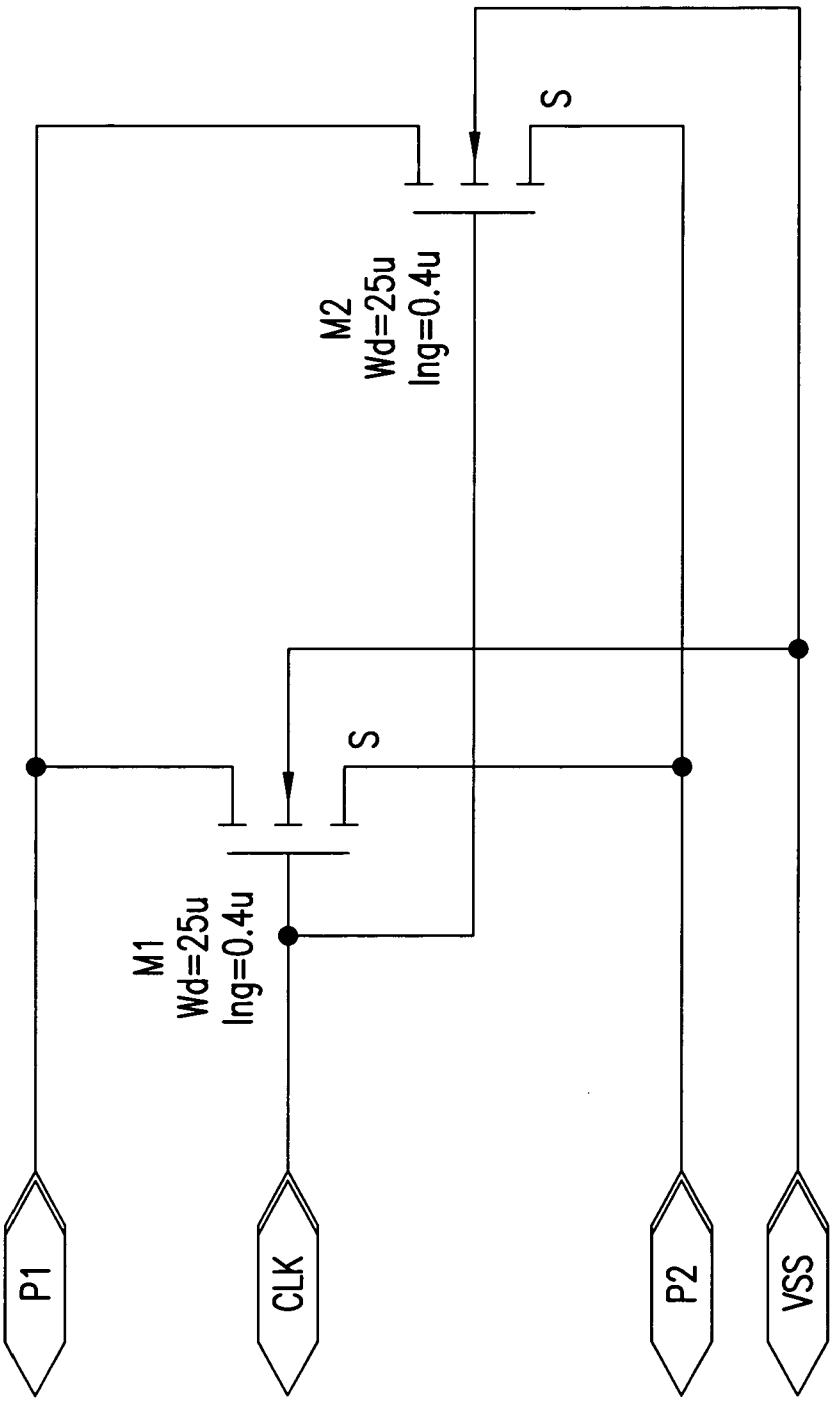


FIG.199

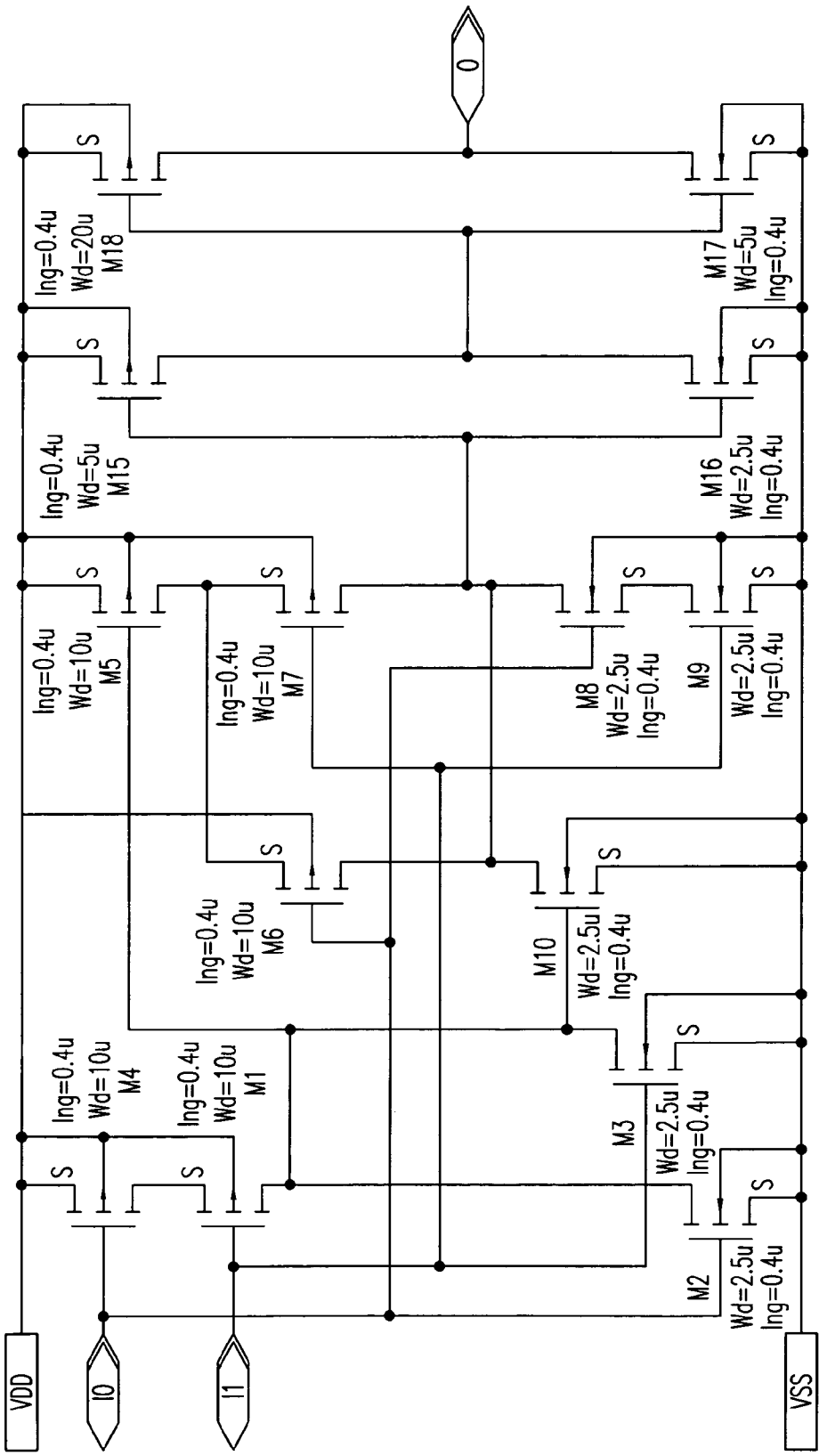

0
lng=0.4u Wd=20u M18
M17 Wd=5u lng=0.4u
lng=0.4u Wd=5u M15
M16 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M5
lng=0.4u Wd=10u M7
M8 Wd=2.5u lng=0.4u
M9 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M6
M10 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M4
lng=0.4u Wd=10u M1
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
VDD
I0
I1
VSS

FIG. 200

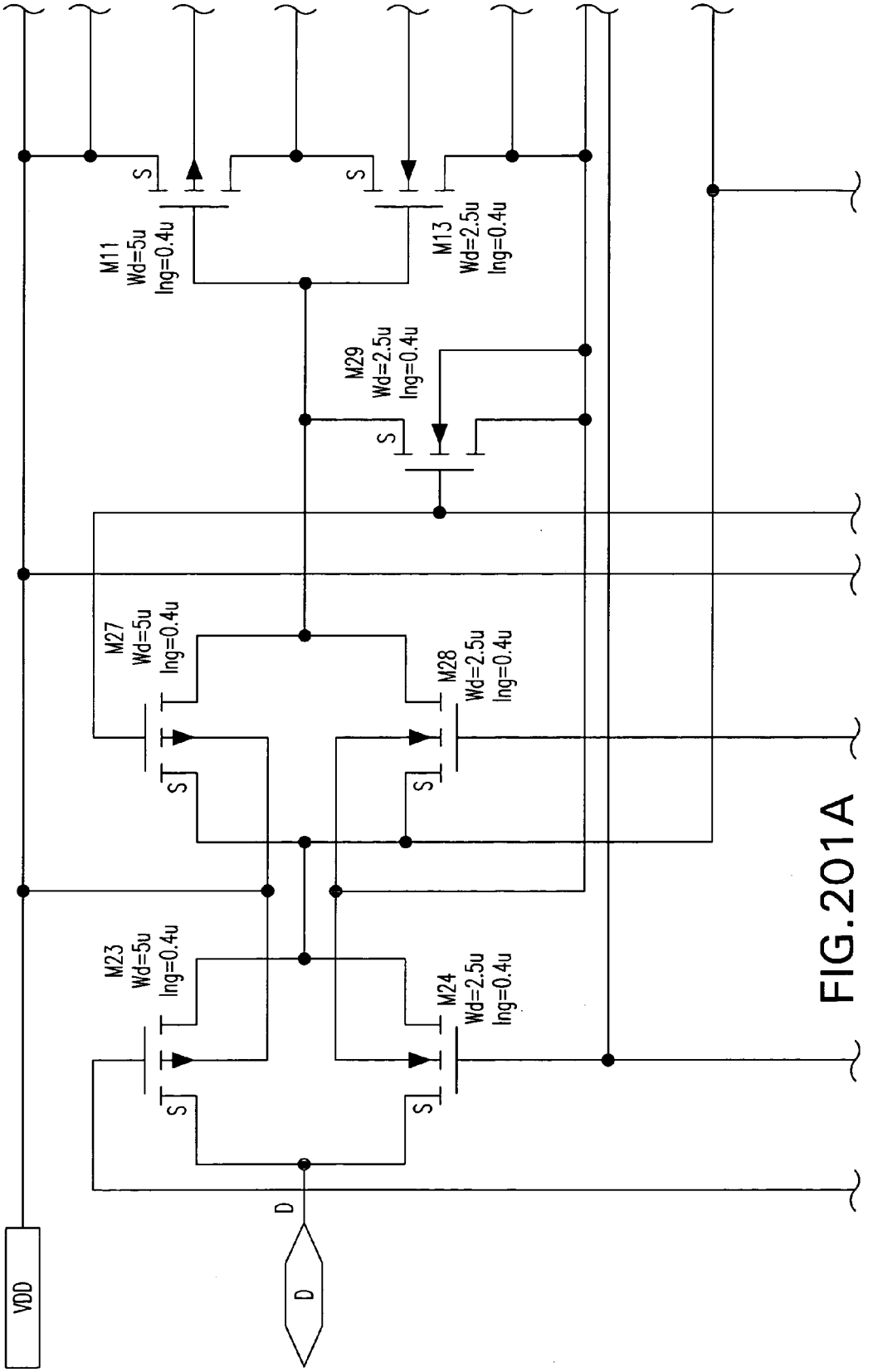

M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M29
Wd=2.5u
lng=0.4u
M27
Wd=5u
lng=0.4u
M28
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.201A

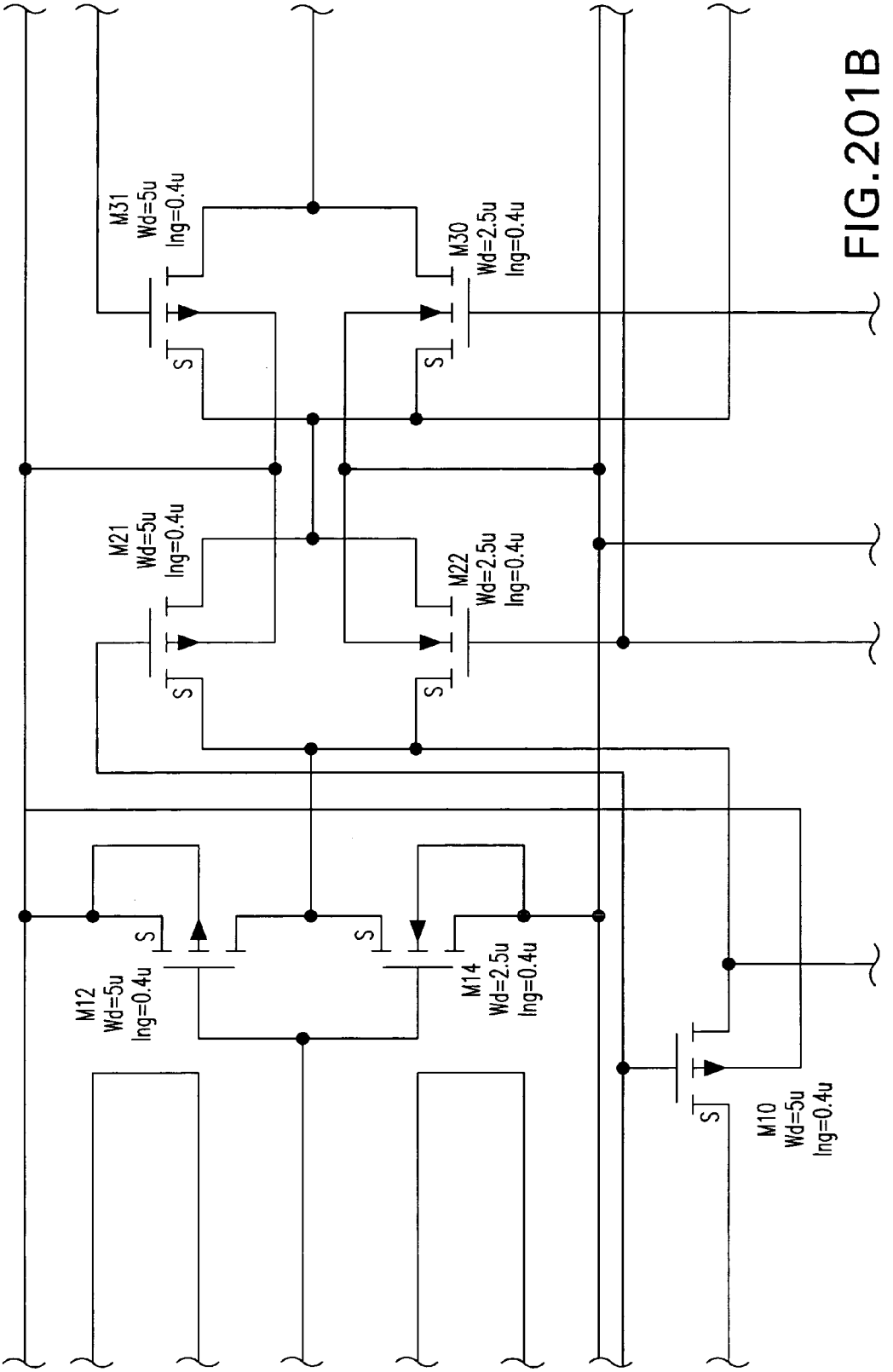

M31
Wd=5u
lng=0.4u
M30
Wd=2.5u
lng=0.4u
M21
Wd=5u
lng=0.4u
M22
Wd=2.5u
lng=0.4u
M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
S

FIG.201B

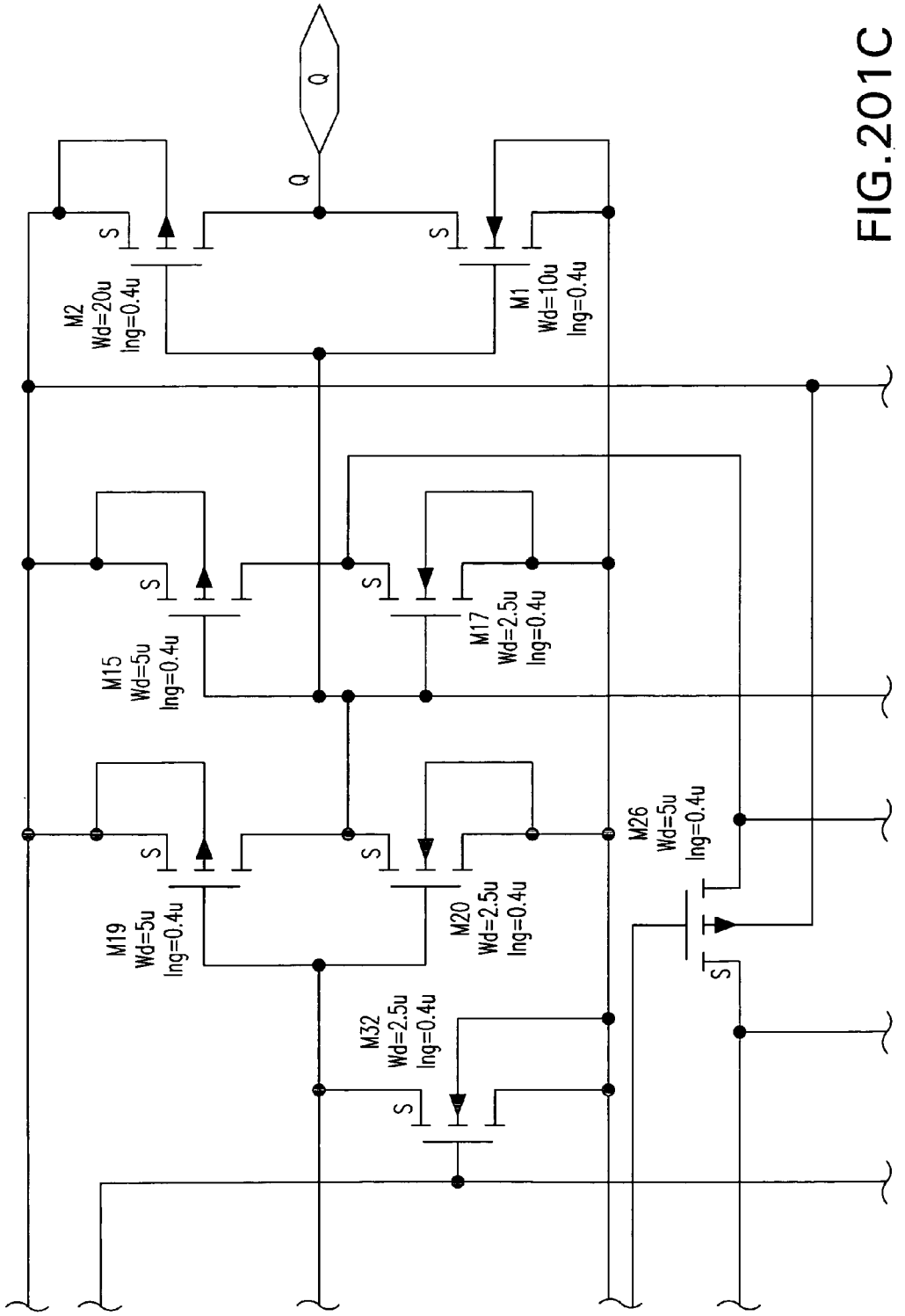

Q
Q
S
S
M2
Wd=20u
lng=0.4u
M1
Wd=10u
lng=0.4u
S
S
M15
Wd=5u
lng=0.4u
M17
Wd=2.5u
lng=0.4u
S
S
M19
Wd=5u
lng=0.4u
M20
Wd=2.5u
lng=0.4u
M26
Wd=5u
lng=0.4u
S
M32
Wd=2.5u
lng=0.4u
S

FIG.201C

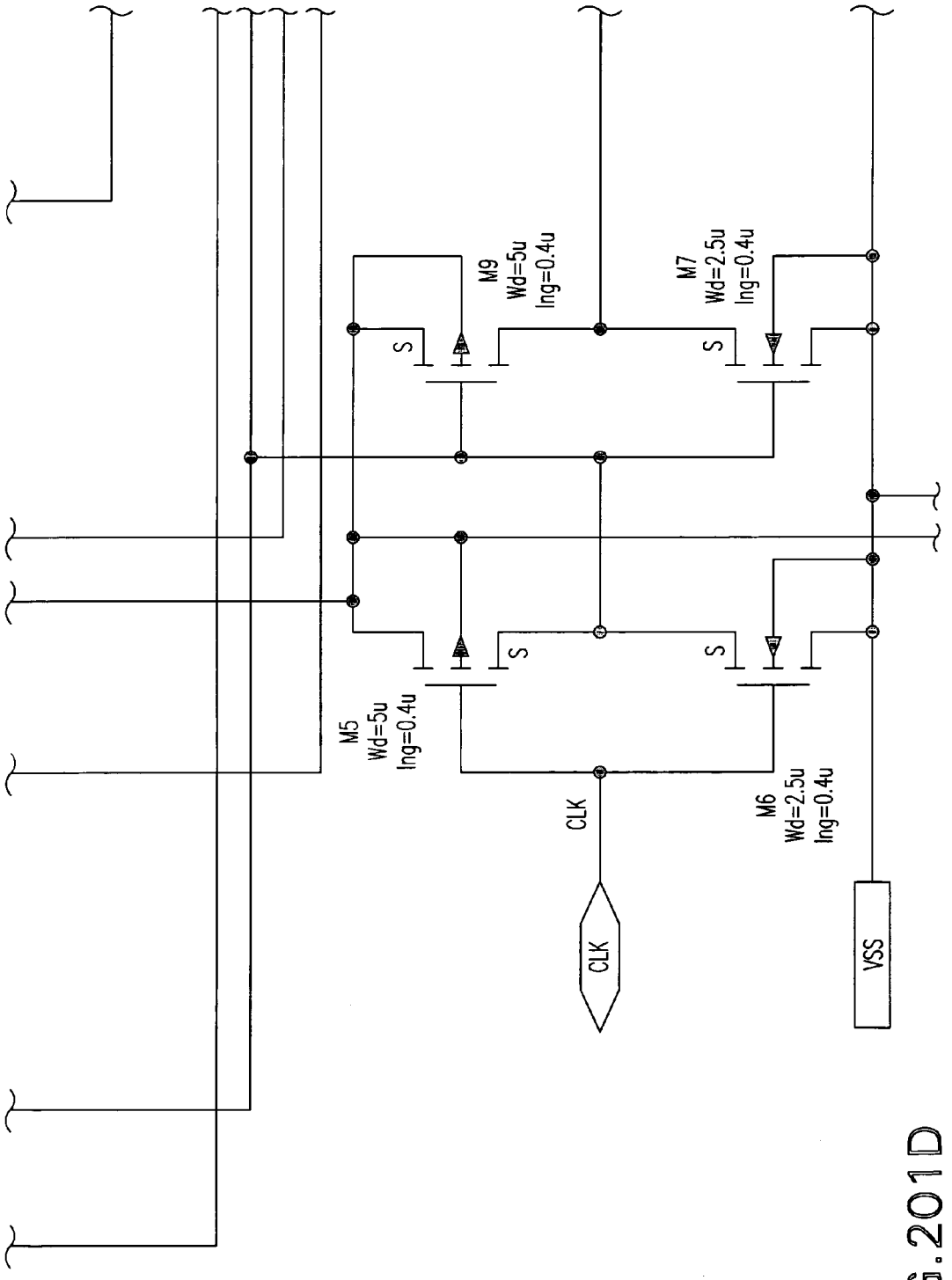

M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
S
S
S
S
M5
Wd=5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
CLK
CLK
VSS

FIG.201D

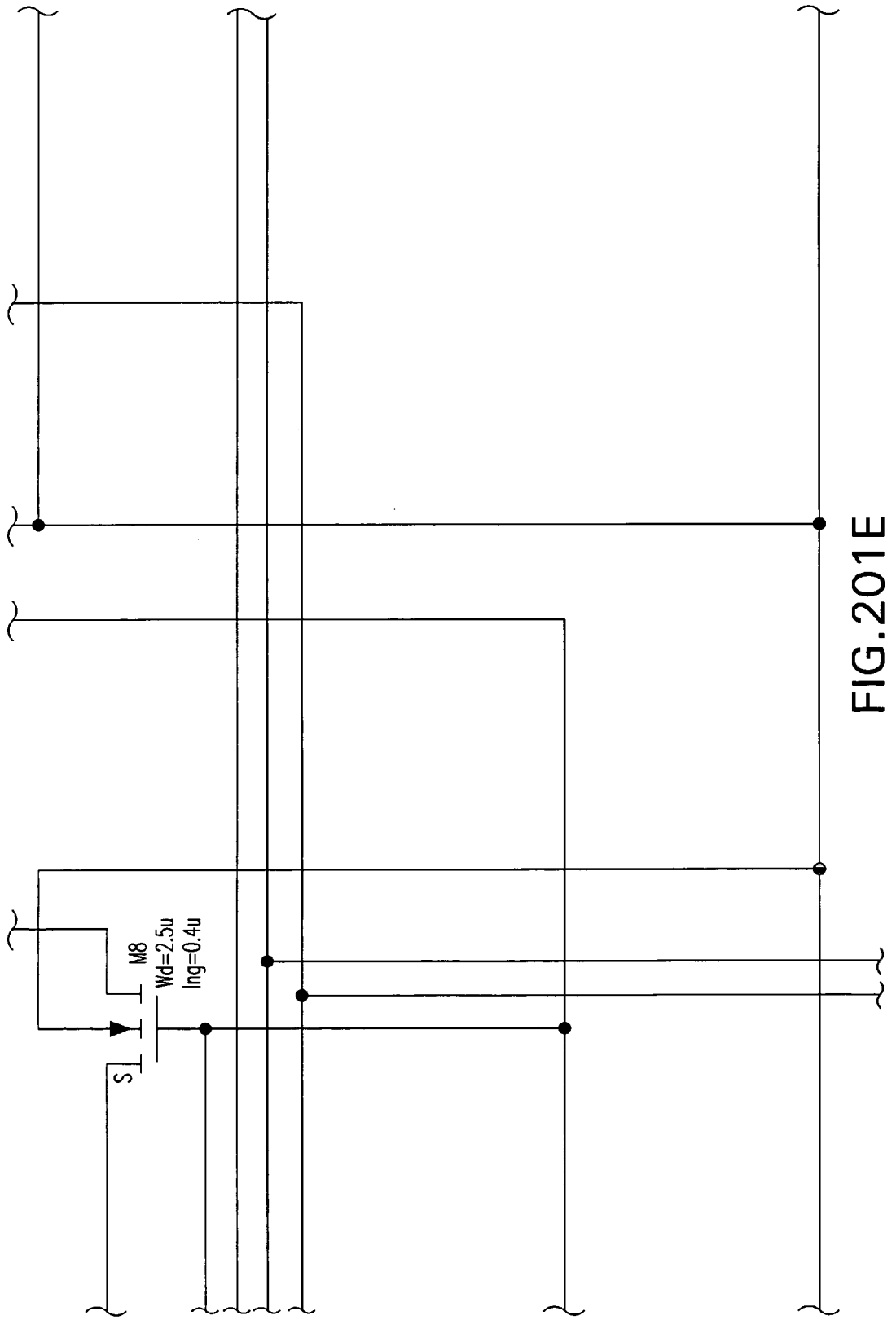


FIG.201E

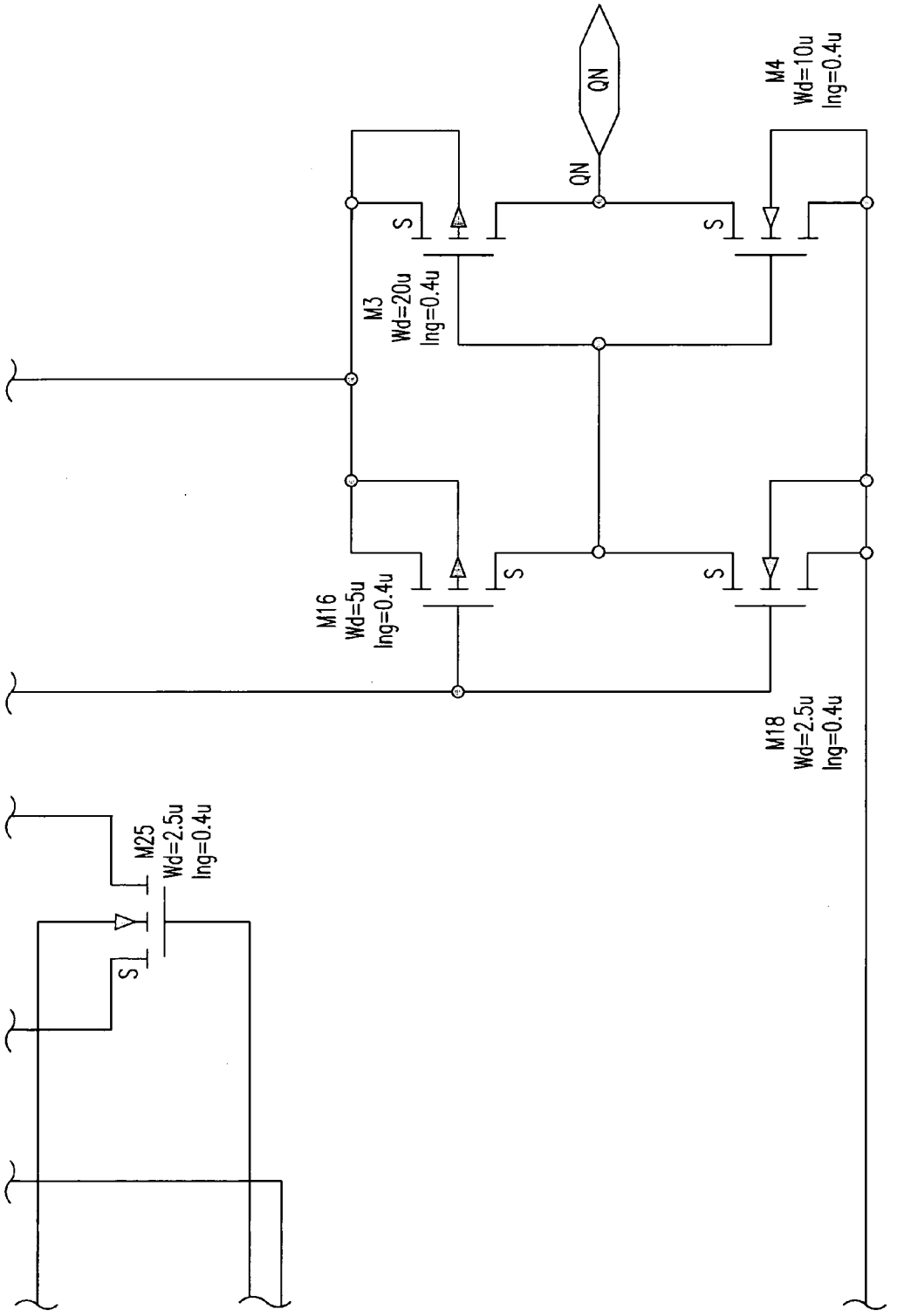

QN
QN
M4
Wd=10u
lng=0.4u
M3
Wd=20u
lng=0.4u
M16
Wd=5u
lng=0.4u
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S
S
S
S
S

FIG. 201F

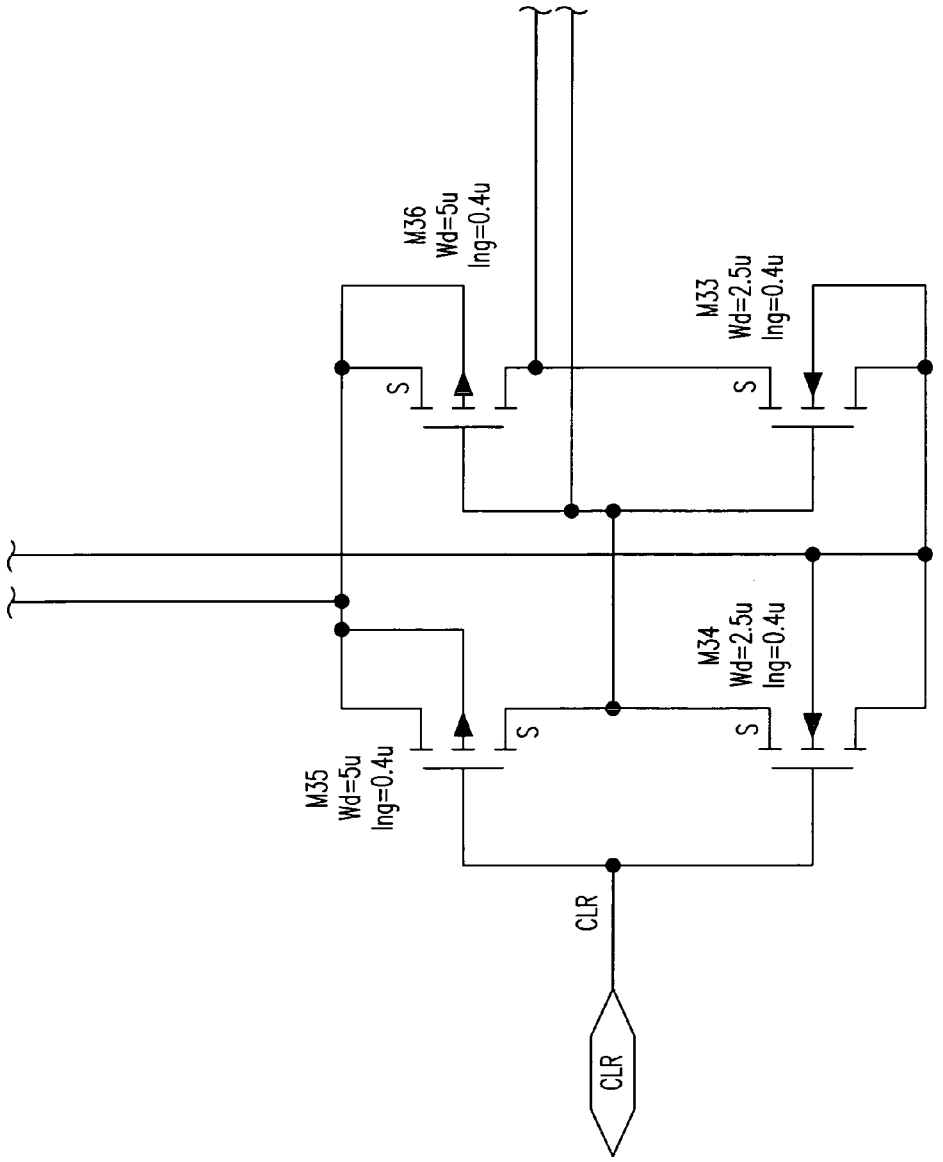
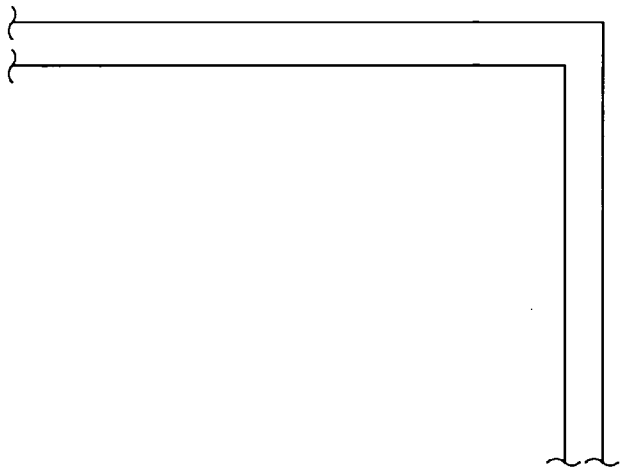

M36
Wd=5u
lng=0.4u
M33
Wd=2.5u
lng=0.4u
M34
Wd=2.5u
lng=0.4u
M35
Wd=5u
lng=0.4u
S
CLR
CLR

FIG.201G

FIG.201H



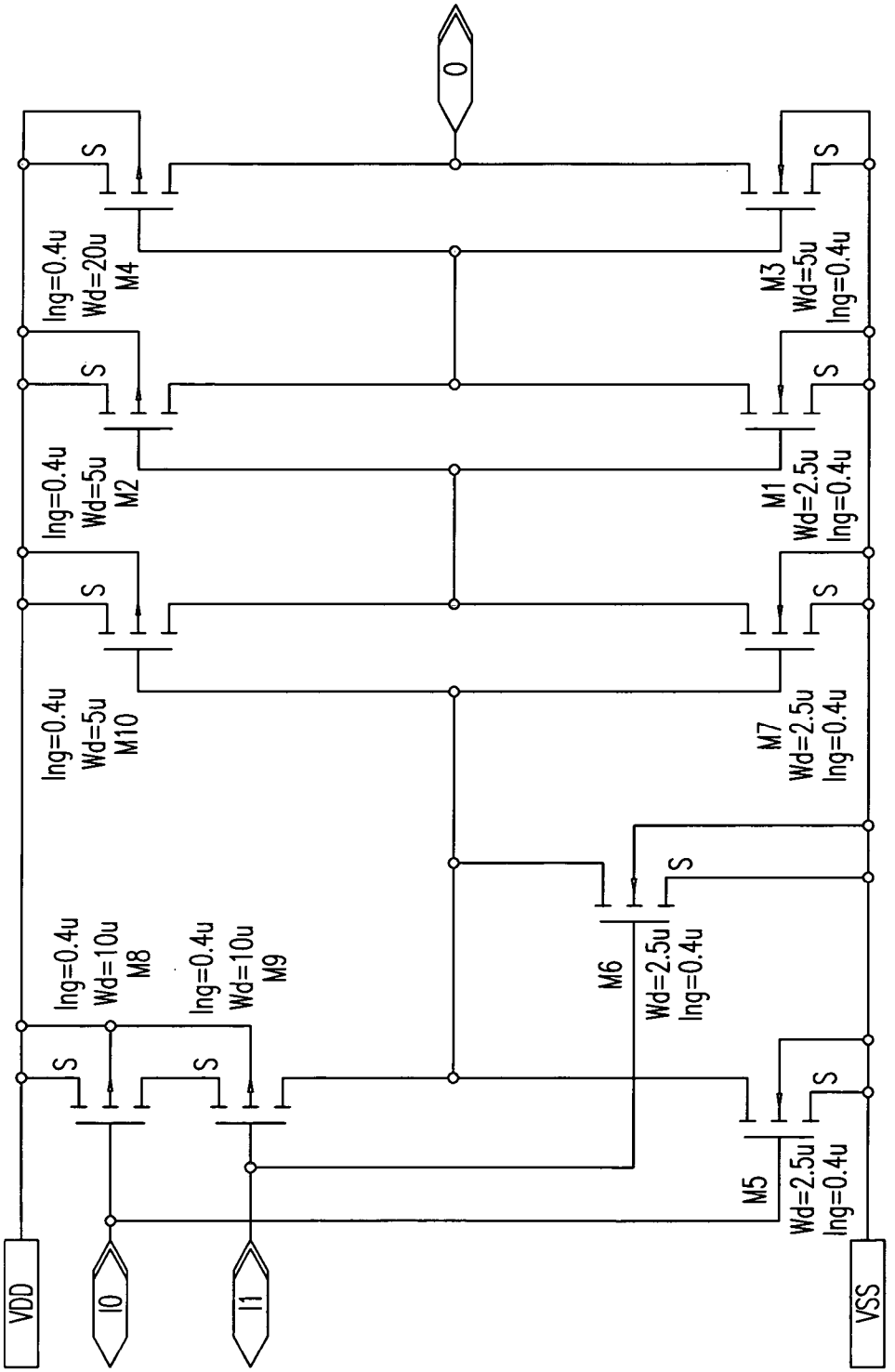

0
S
lng=0.4u
Wd=20u
M4
M3
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M2
M1
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M10
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=10u
M8
lng=0.4u
Wd=10u
M9
M5
Wd=2.5u
lng=0.4u
VDD
I0
I1
VSS

FIG. 202

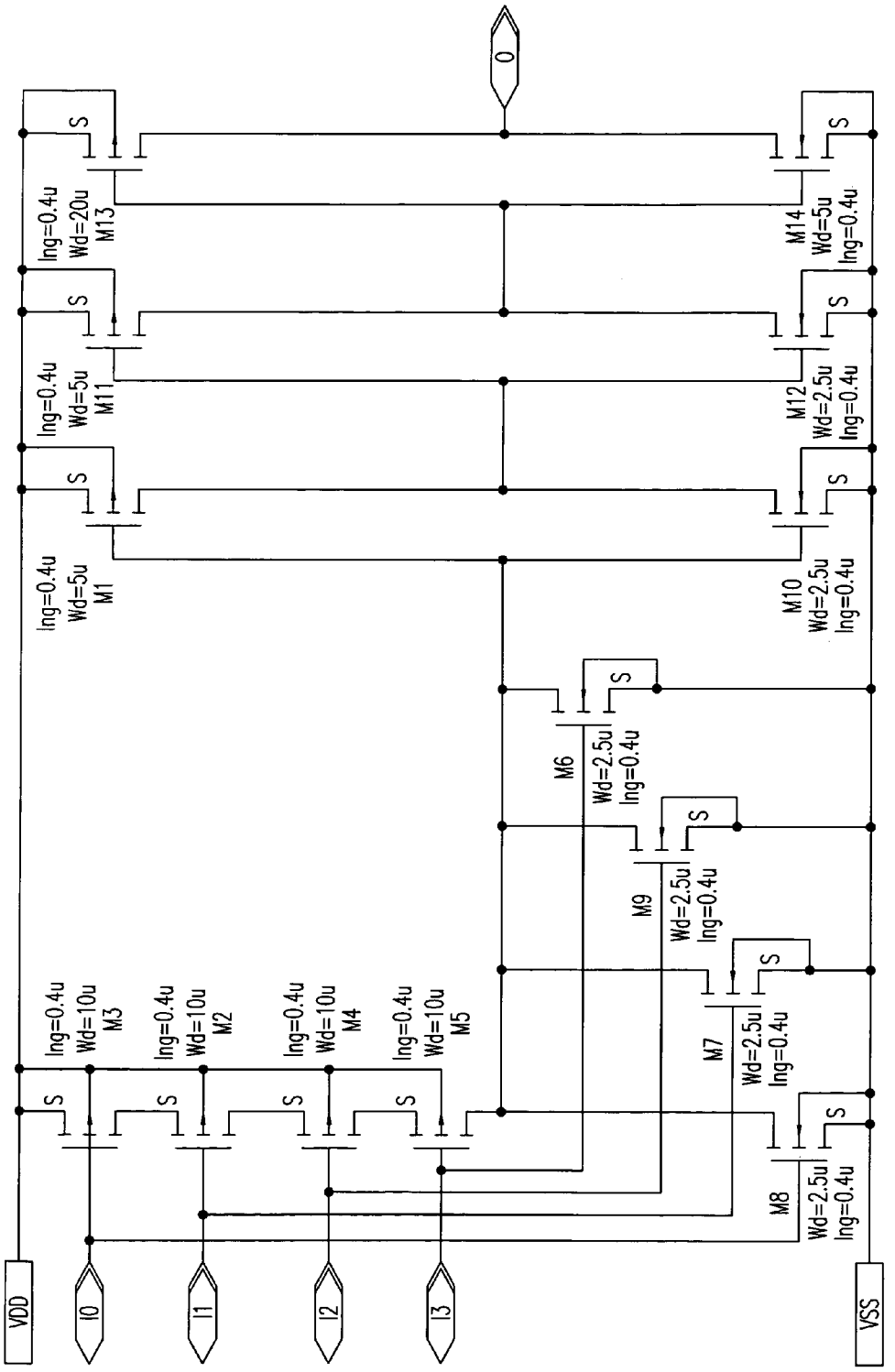

O
M13 lng=0.4u Wd=20u
M14 Wd=5u lng=0.4u
M11 lng=0.4u Wd=5u
M12 Wd=2.5u lng=0.4u
M1 lng=0.4u Wd=5u
M10 Wd=2.5u lng=0.4u
M6 Wd=2.5u lng=0.4u
M9 Wd=2.5u lng=0.4u
M7 Wd=2.5u lng=0.4u
M8 Wd=2.5u lng=0.4u
M3 lng=0.4u Wd=10u
M2 lng=0.4u Wd=10u
M4 lng=0.4u Wd=10u
M5 lng=0.4u Wd=10u
S
VDD
I0
I1
I2
I3
VSS

FIG.203

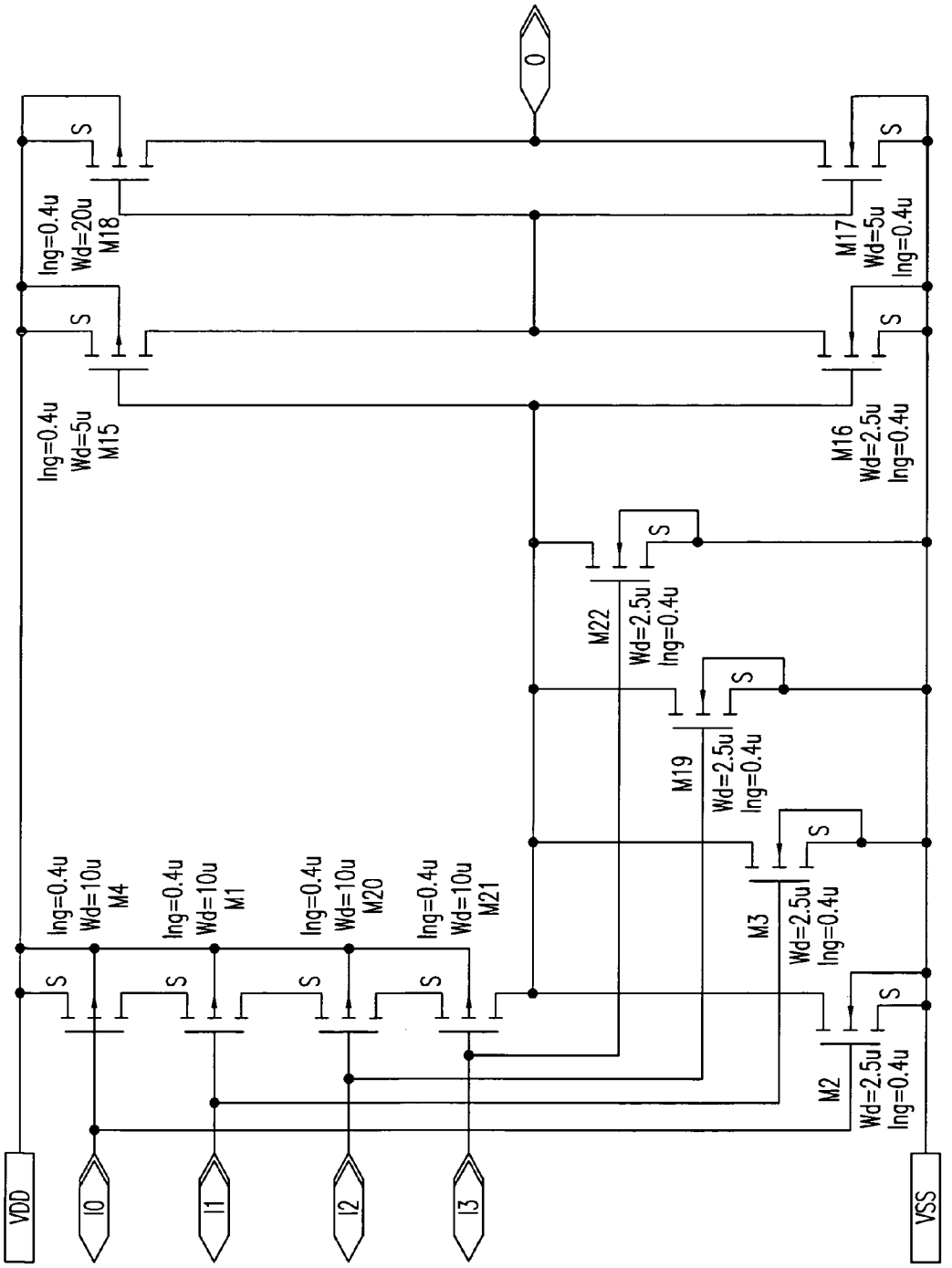

O
lng=0.4u Wd=20u M18
M17 Wd=5u lng=0.4u
lng=0.4u Wd=5u M15
M16 Wd=2.5u lng=0.4u
M22 Wd=2.5u lng=0.4u
M19 Wd=2.5u lng=0.4u
M3 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
lng=0.4u Wd=10u M4
lng=0.4u Wd=10u M1
lng=0.4u Wd=10u M20
lng=0.4u Wd=10u M21
VDD
I0
I1
I2
I3
VSS

FIG.204

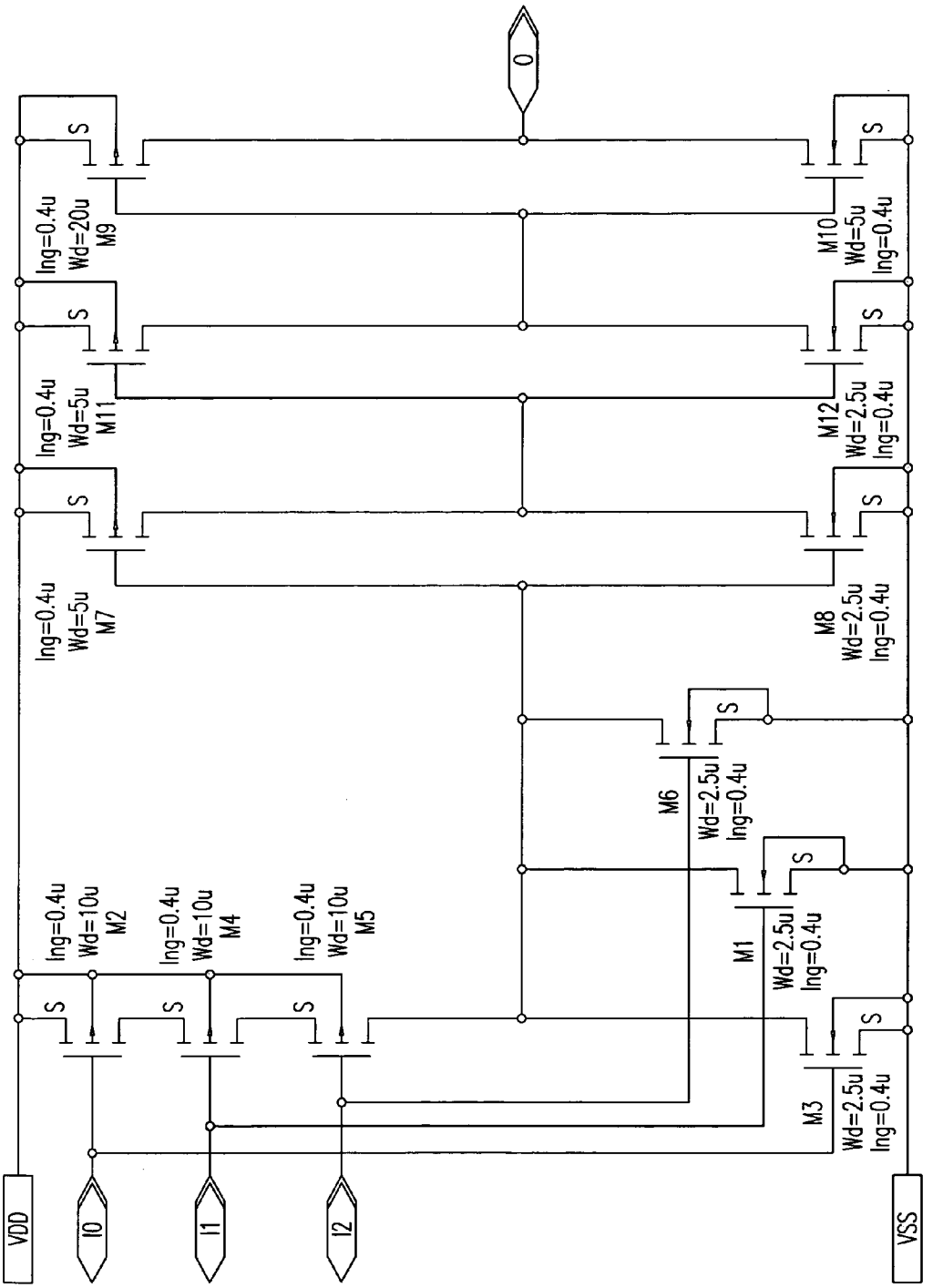

O
lng=0.4u
Wd=20u
M9
M10
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M11
M12
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M7
M8
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M1
Wd=2.5u
lng=0.4u
M3
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=10u
M2
lng=0.4u
Wd=10u
M4
lng=0.4u
Wd=10u
M5
S
VDD
I0
I1
I2
VSS

FIG. 205

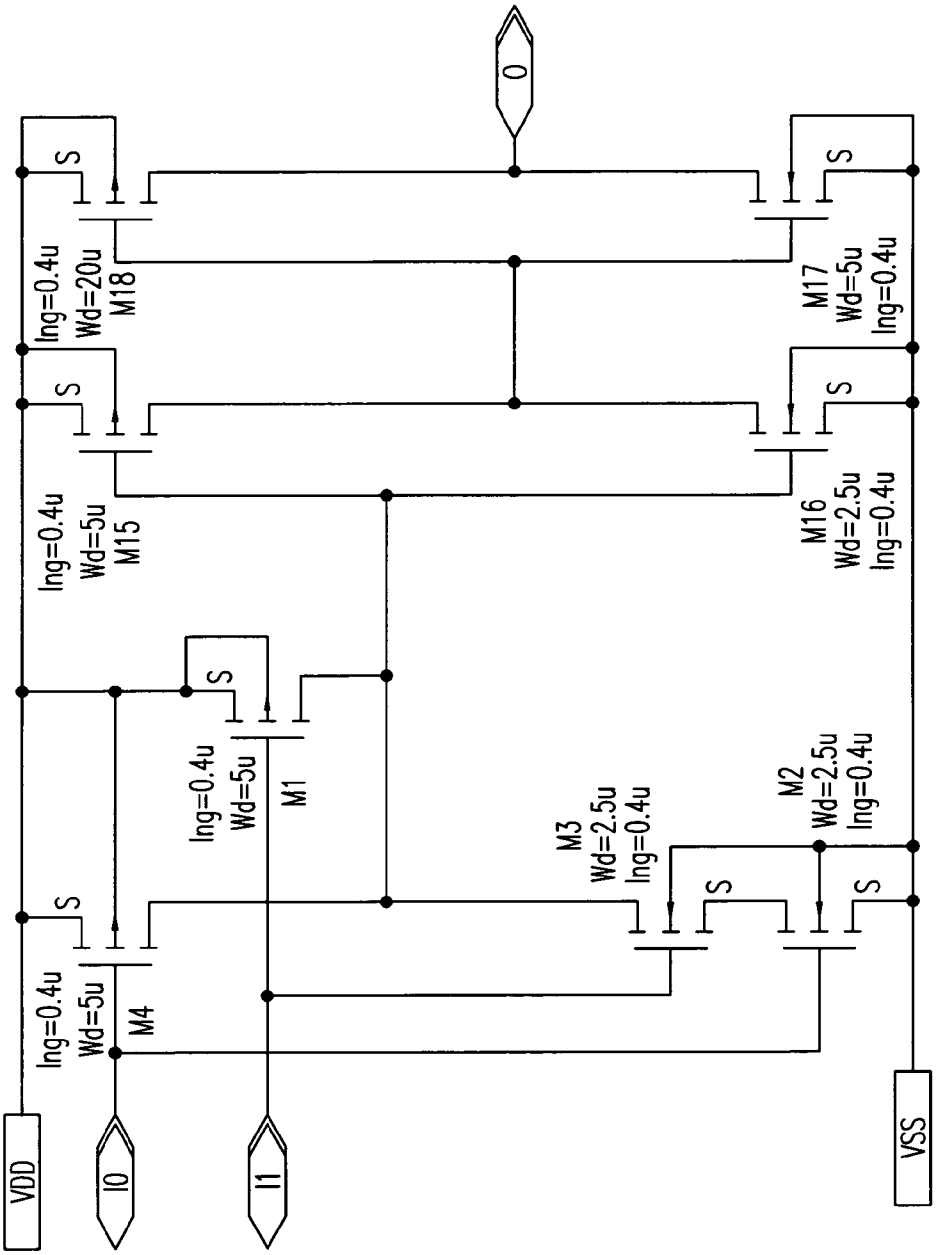

0
S
lng=0.4u
Wd=20u
M18
M17
Wd=5u
lng=0.4u
lng=0.4u
Wd=5u
M15
M16
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M1
M3
Wd=2.5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
lng=0.4u
Wd=5u
M4
VDD
I0
I1
VSS

FIG.206

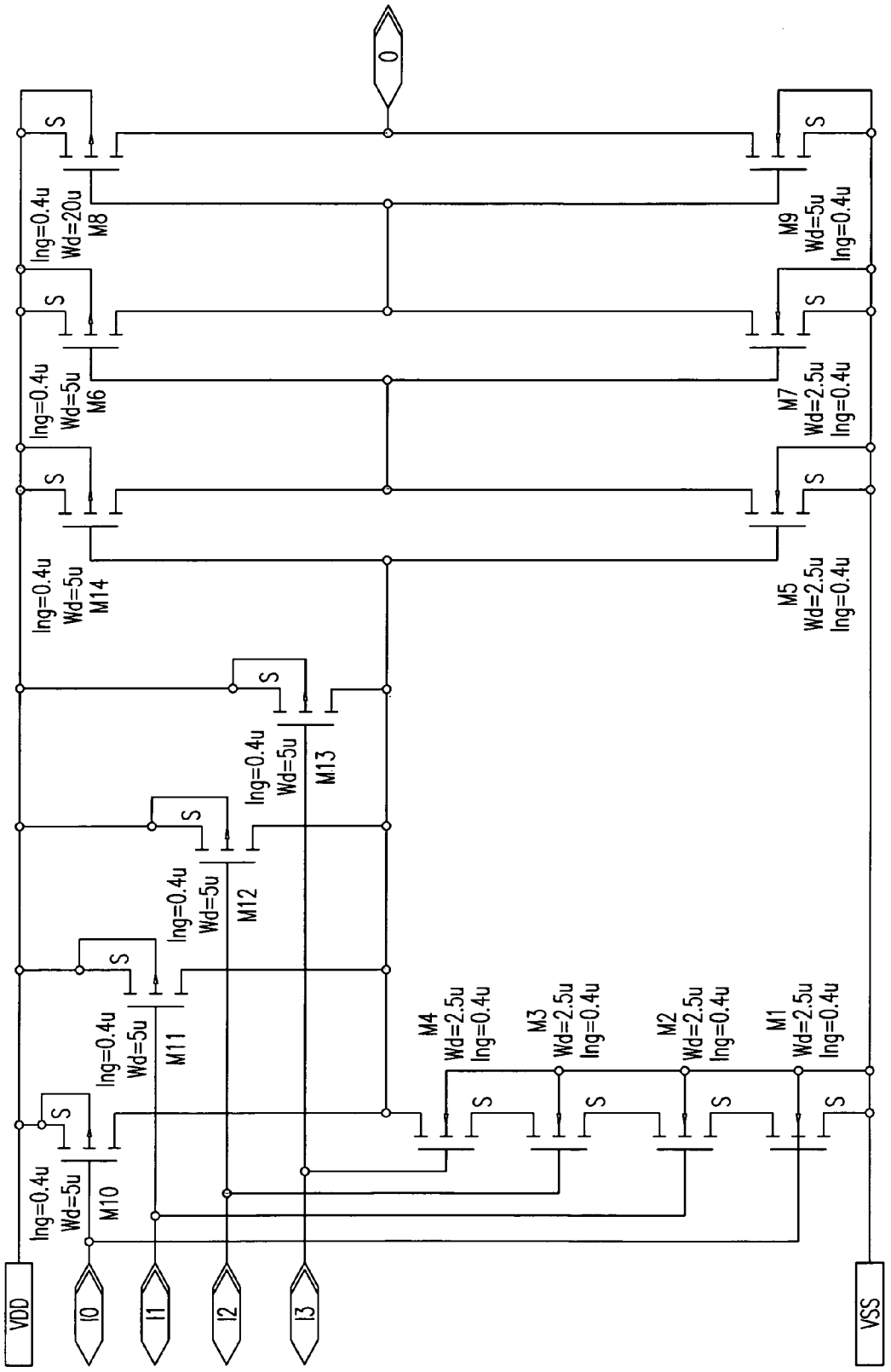

O
VDD
I0
I1
I2
I3
VSS
M1 Wd=2.5u lng=0.4u
M2 Wd=2.5u lng=0.4u
M3 Wd=2.5u lng=0.4u
M4 Wd=2.5u lng=0.4u
M5 Wd=2.5u lng=0.4u
M6 lng=0.4u Wd=5u
M7 Wd=2.5u lng=0.4u
M8 lng=0.4u Wd=20u
M9 Wd=5u lng=0.4u
M10 lng=0.4u Wd=5u
M11 lng=0.4u Wd=5u
M12 lng=0.4u Wd=5u
M13 lng=0.4u Wd=5u
M14 lng=0.4u Wd=5u
S

FIG. 207

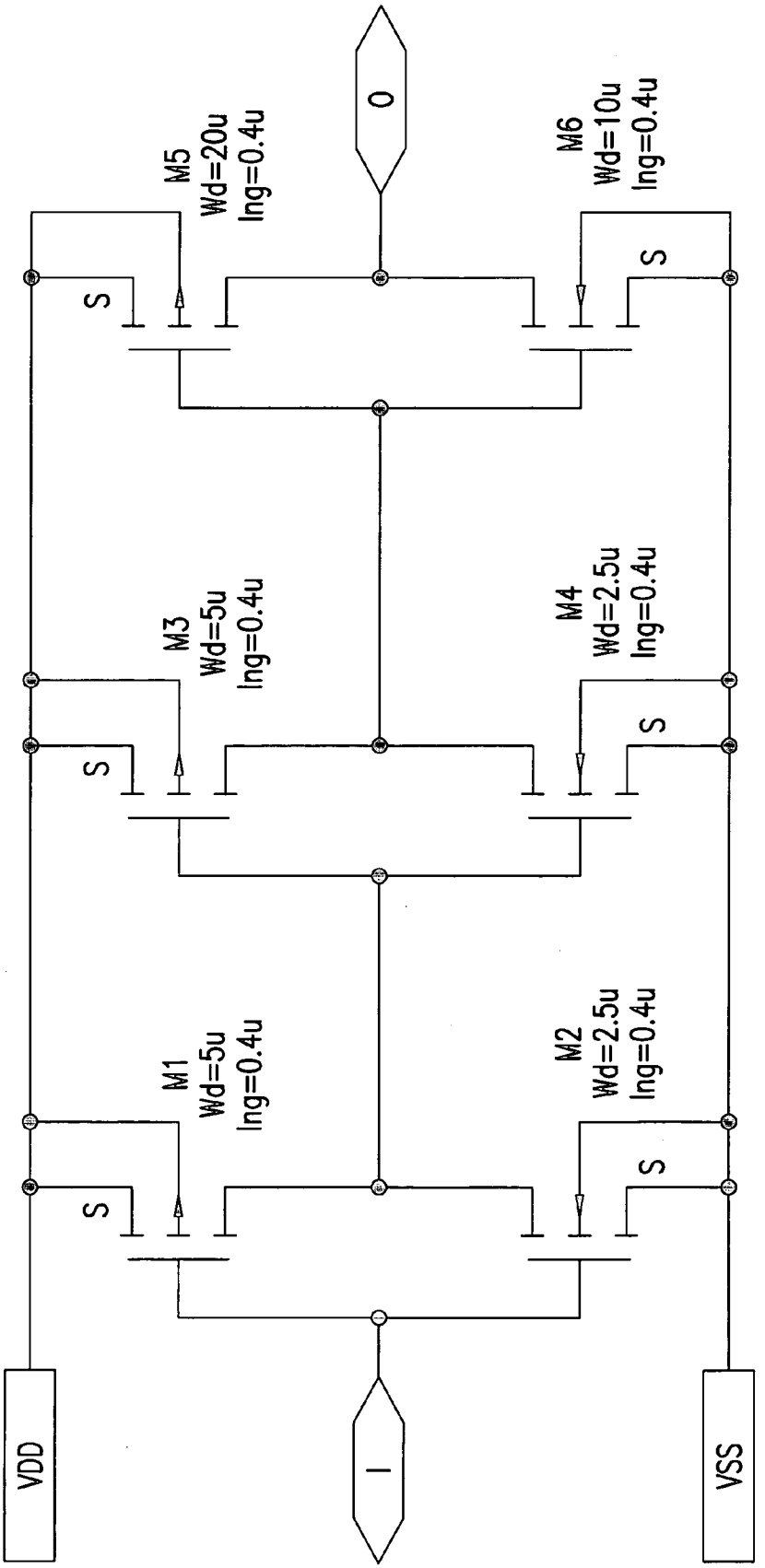

O
M5
Wd=20u
lng=0.4u
M6
Wd=10u
lng=0.4u
S
S
M3
Wd=5u
lng=0.4u
M4
Wd=2.5u
lng=0.4u
S
S
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
S
S
VDD
I
VSS

FIG.208

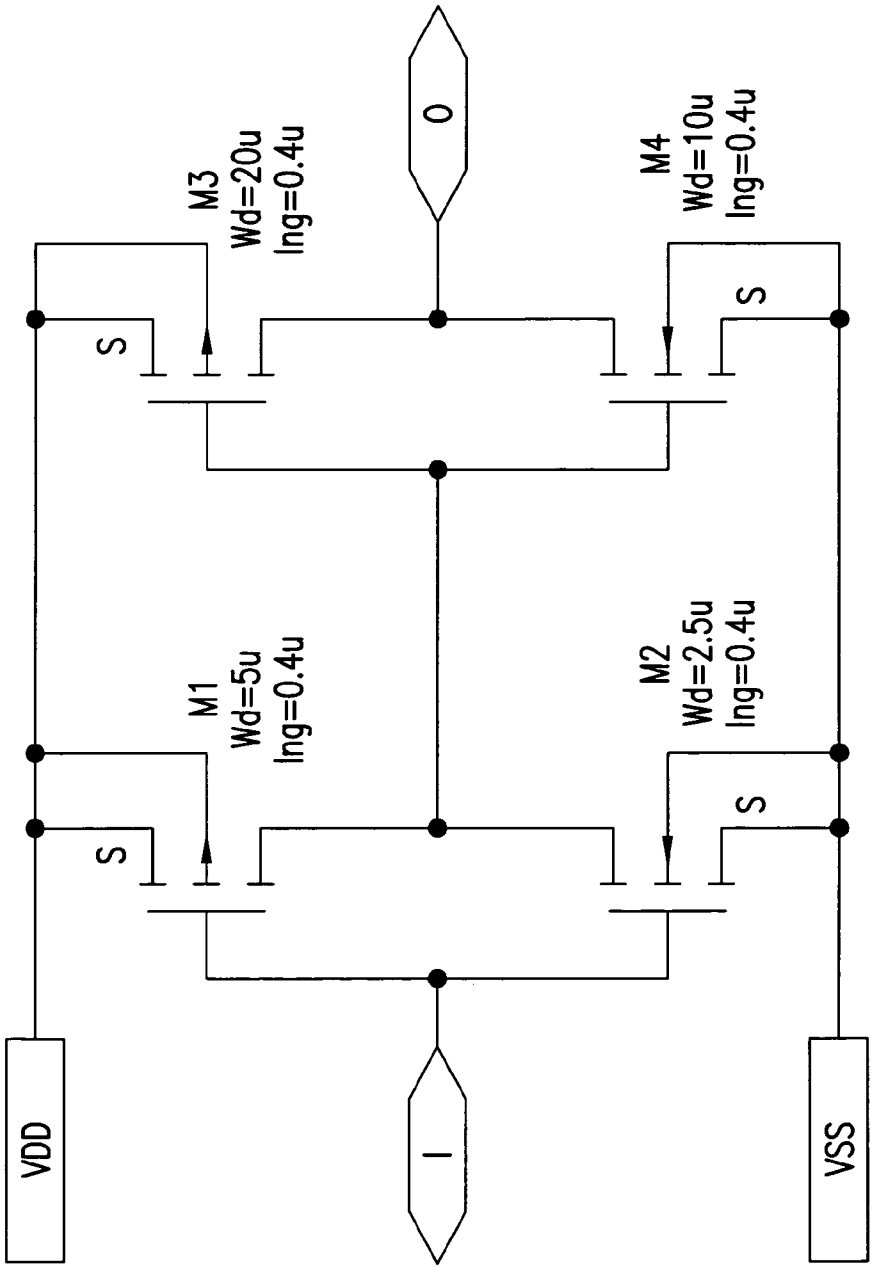

O
M3
Wd=20u
lng=0.4u
M4
Wd=10u
lng=0.4u
S
S
M1
Wd=5u
lng=0.4u
M2
Wd=2.5u
lng=0.4u
S
S
VDD
I
VSS

FIG.209

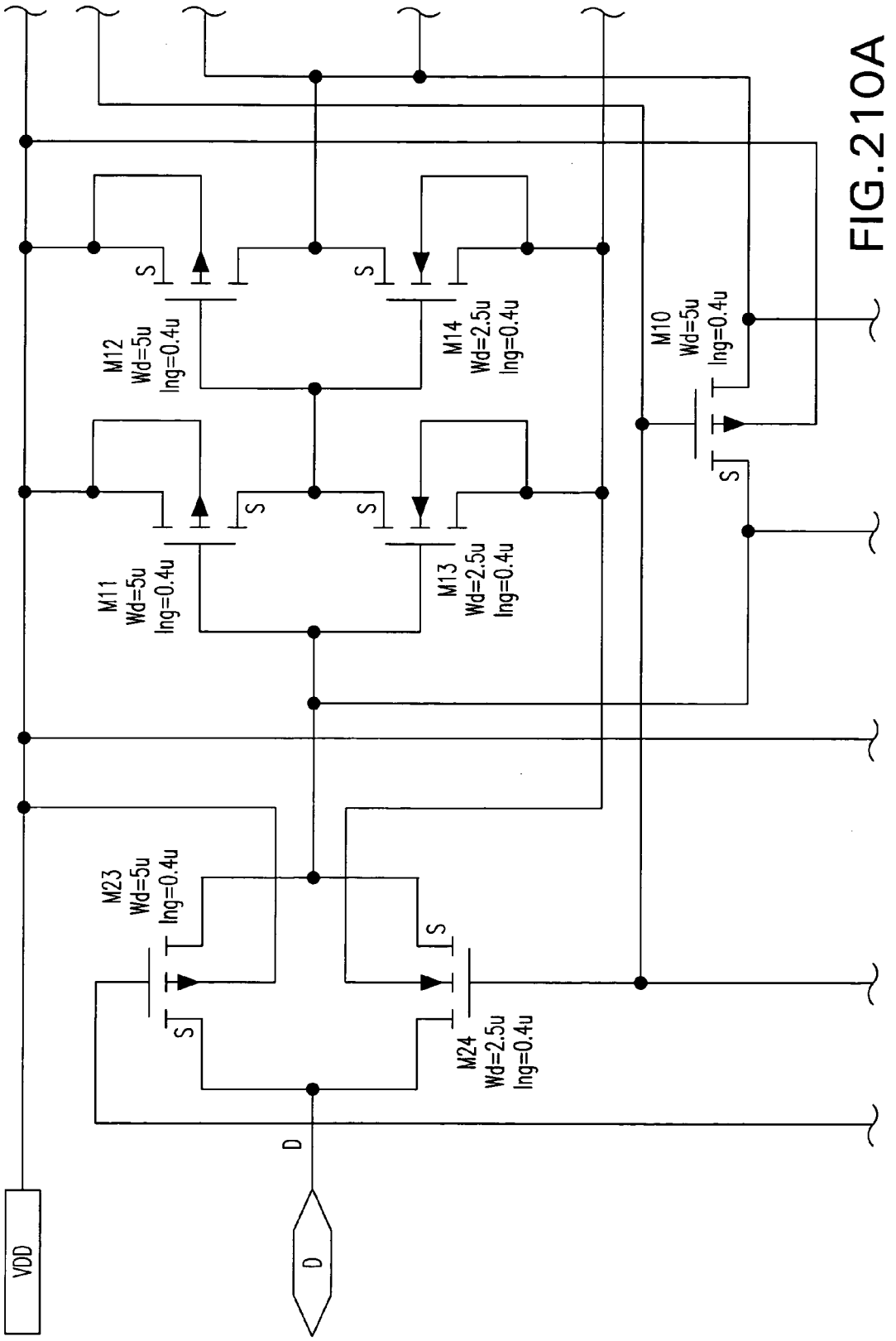

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.210A

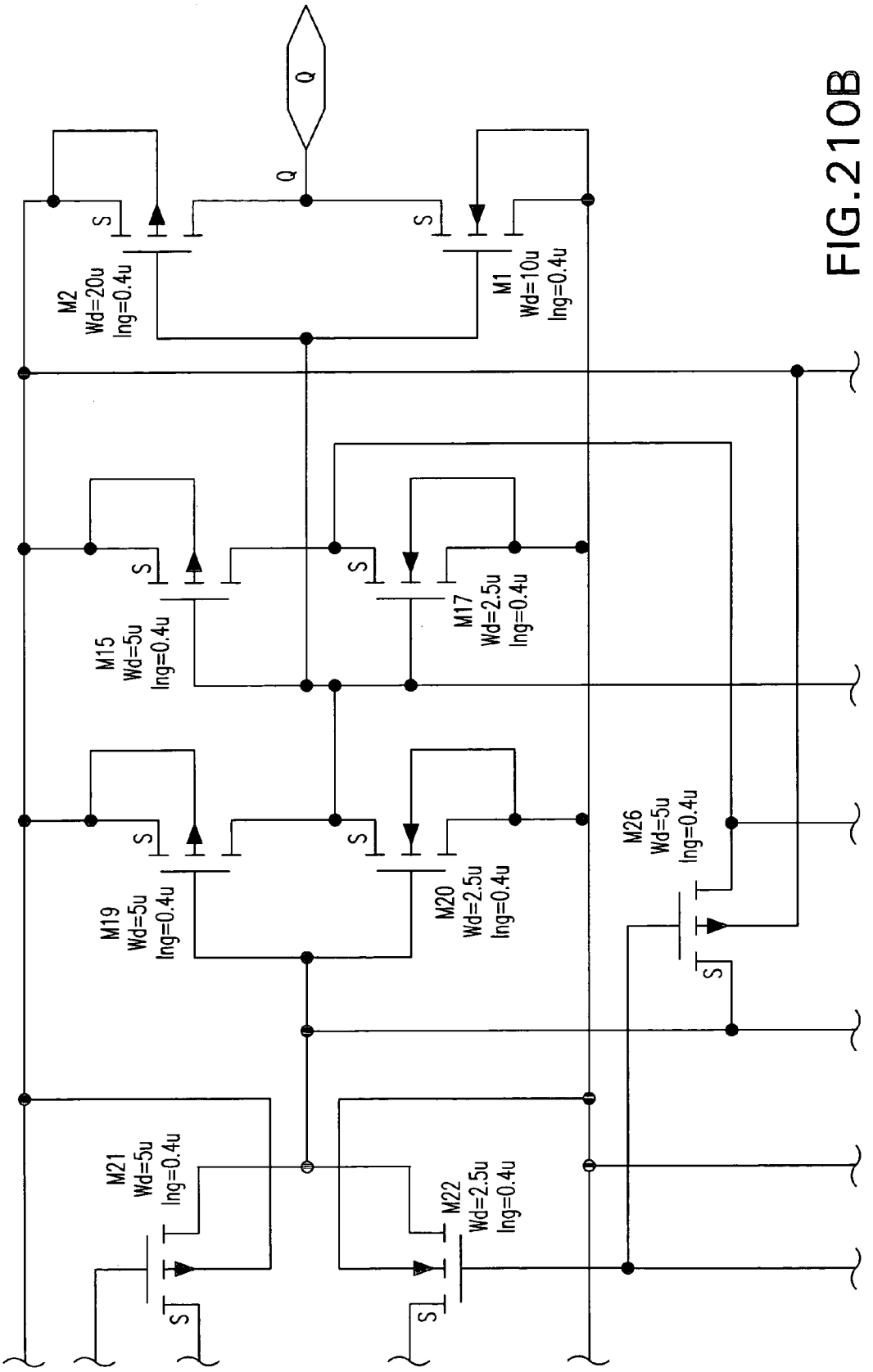

Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
S
M26
Wd=5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
S
M22
Wd=2.5u
lng=0.4u

FIG.210B

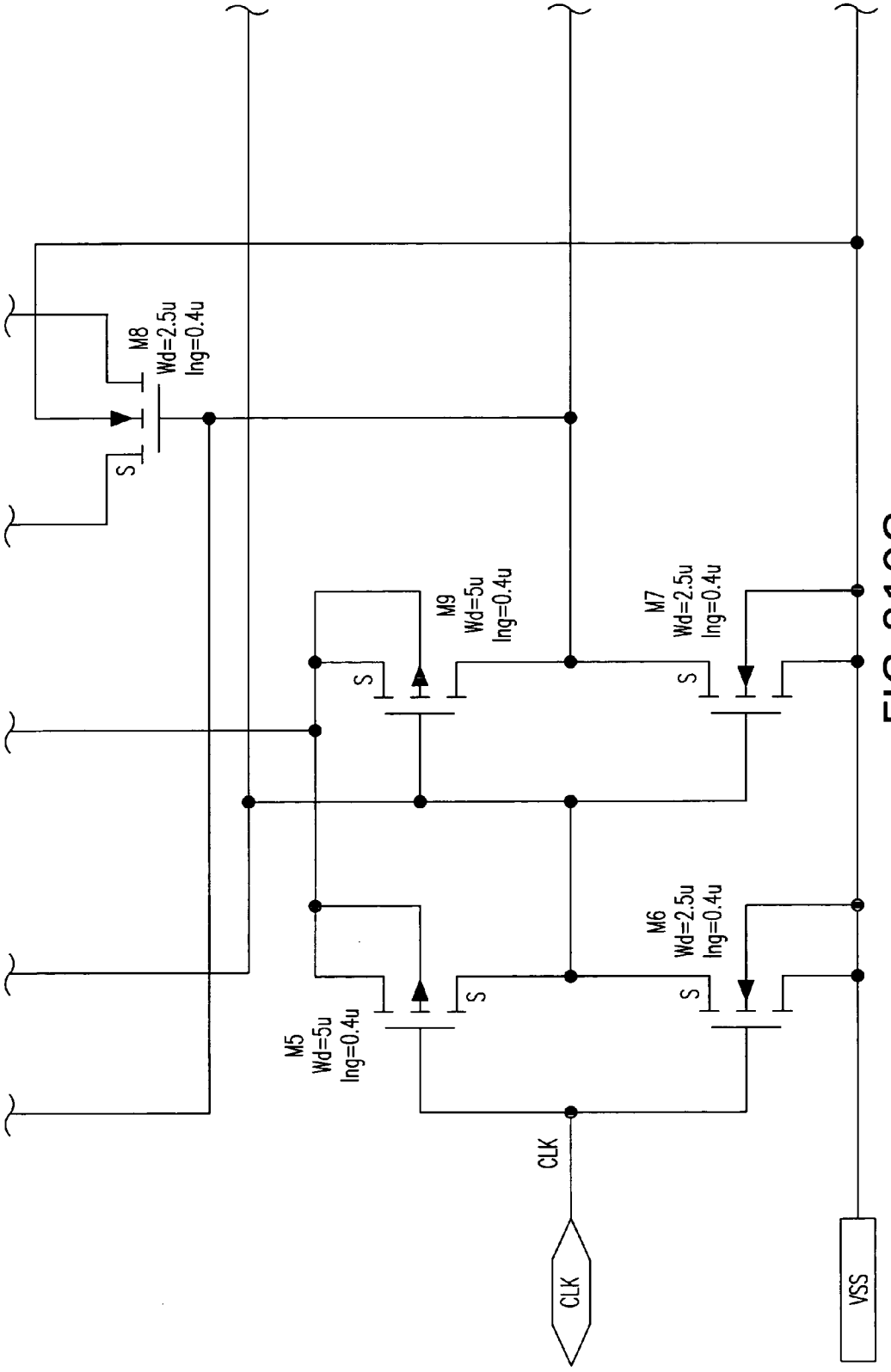

M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M5
Wd=5u
lng=0.4u
CLK
CLK
VSS

FIG.210C

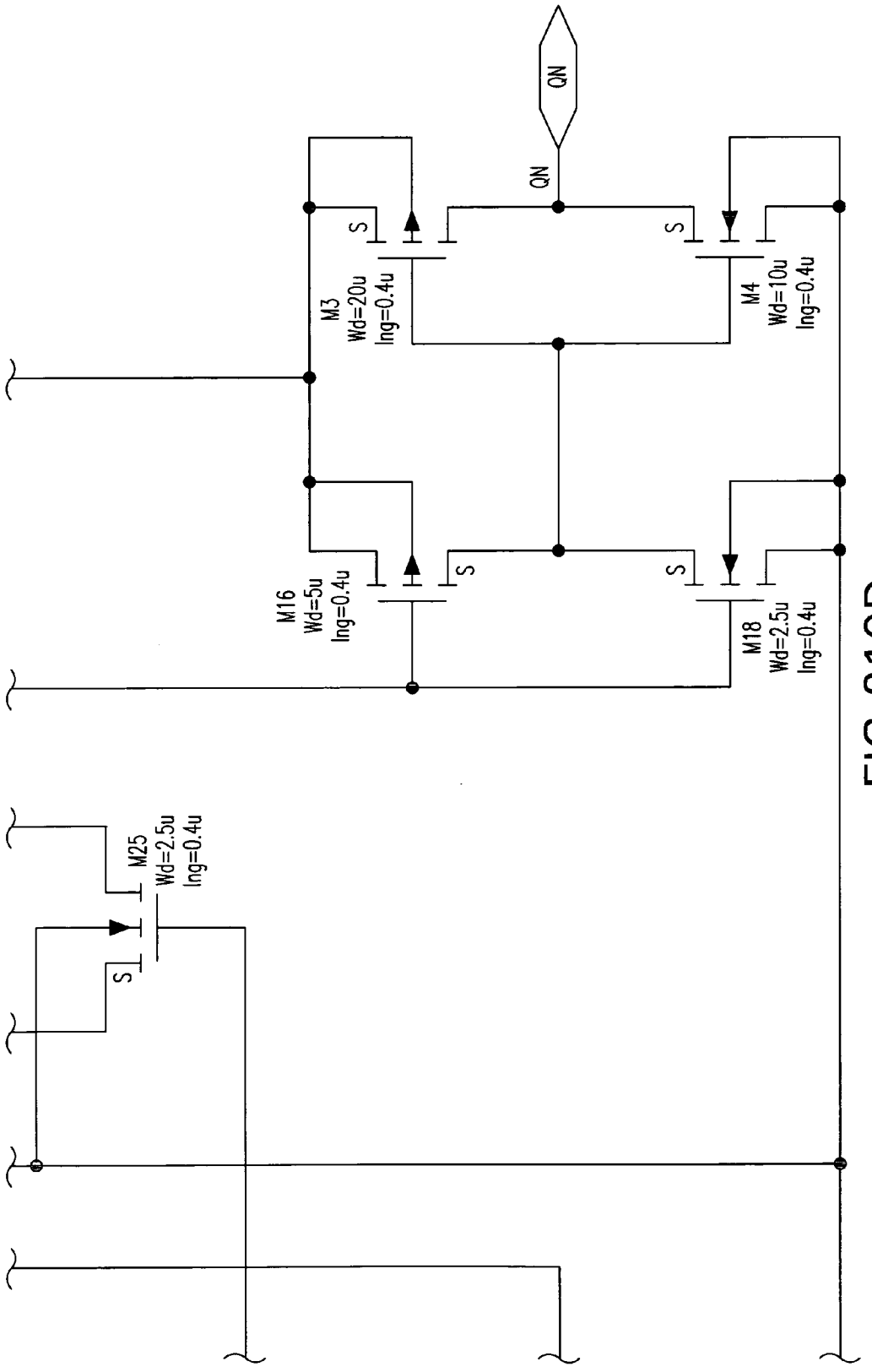

QN
QN
S
S
M3
Wd=20u
lng=0.4u
M4
Wd=10u
lng=0.4u
M16
Wd=5u
lng=0.4u
S
S
M18
Wd=2.5u
lng=0.4u
M25
Wd=2.5u
lng=0.4u
S

FIG.210D

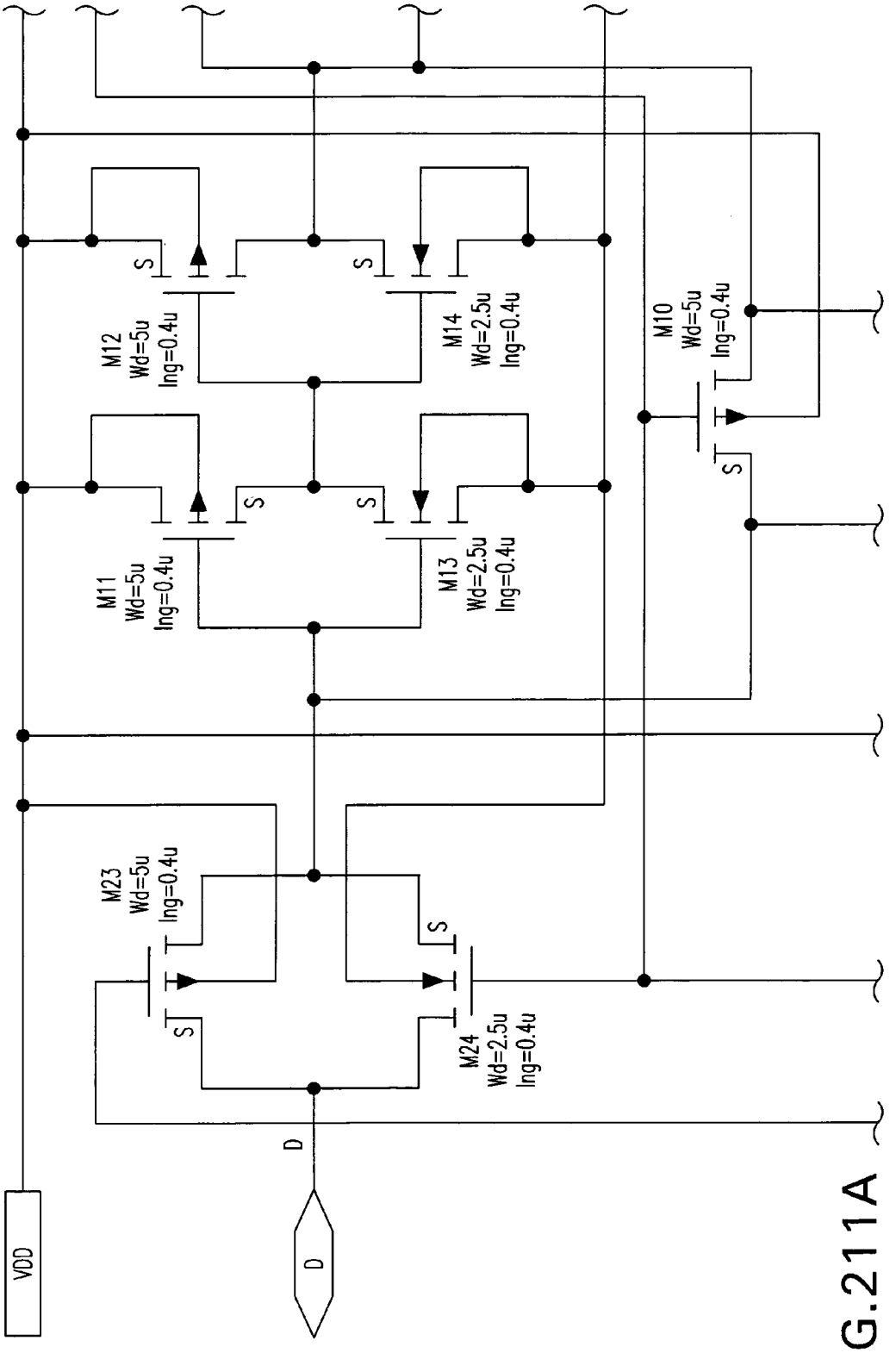

M12
Wd=5u
lng=0.4u
M14
Wd=2.5u
lng=0.4u
M10
Wd=5u
lng=0.4u
M11
Wd=5u
lng=0.4u
M13
Wd=2.5u
lng=0.4u
M23
Wd=5u
lng=0.4u
M24
Wd=2.5u
lng=0.4u
S
D
VDD

FIG.211A

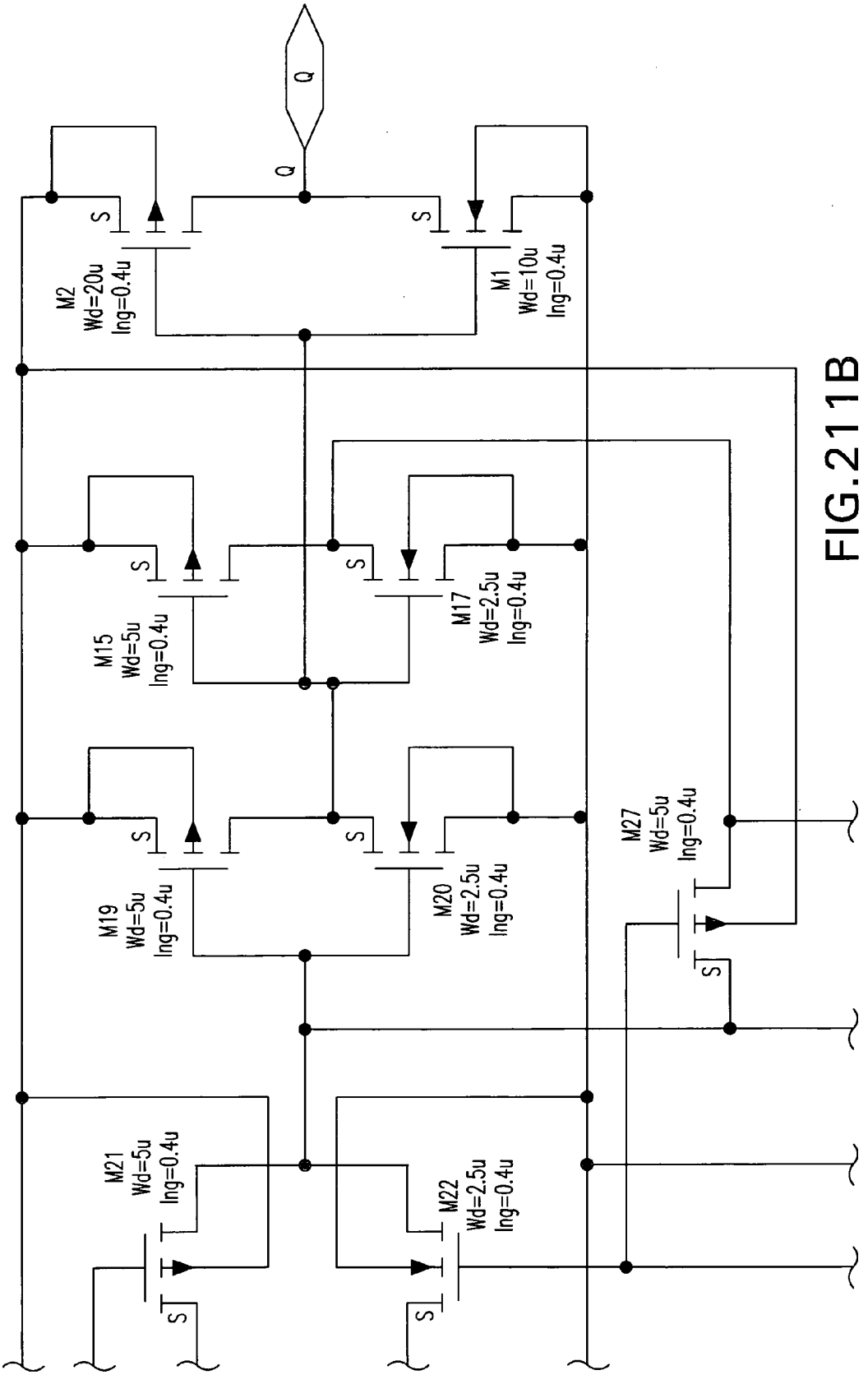

Q
Q
S
M2
Wd=20u
lng=0.4u
S
M1
Wd=10u
lng=0.4u
S
M15
Wd=5u
lng=0.4u
S
M17
Wd=2.5u
lng=0.4u
S
M19
Wd=5u
lng=0.4u
S
M20
Wd=2.5u
lng=0.4u
S
M27
Wd=5u
lng=0.4u
S
M21
Wd=5u
lng=0.4u
S
M22
Wd=2.5u
lng=0.4u

FIG.211B

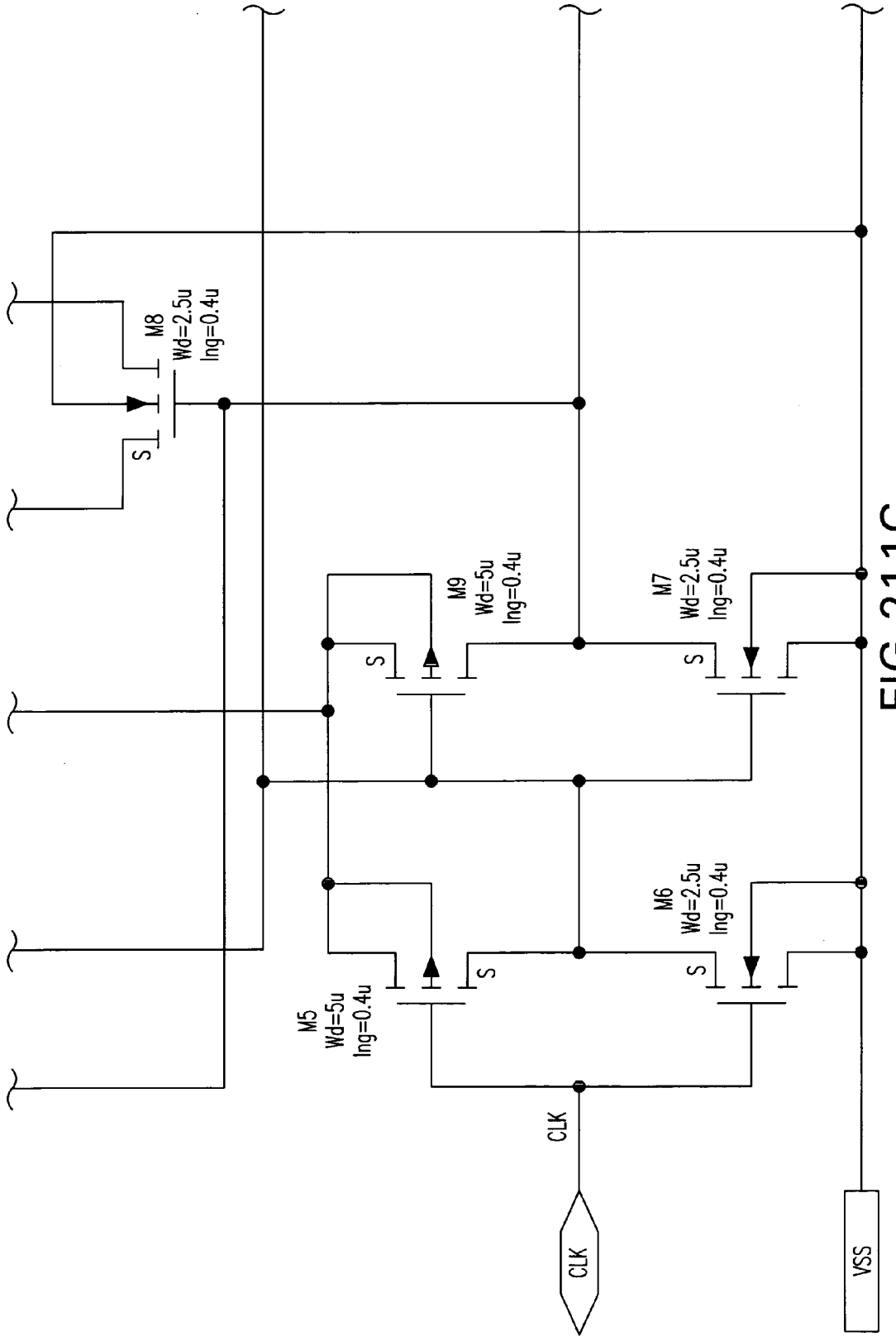

M8
Wd=2.5u
lng=0.4u
S
M9
Wd=5u
lng=0.4u
M7
Wd=2.5u
lng=0.4u
M6
Wd=2.5u
lng=0.4u
M5
Wd=5u
lng=0.4u
CLK
CLK
VSS

FIG.211C

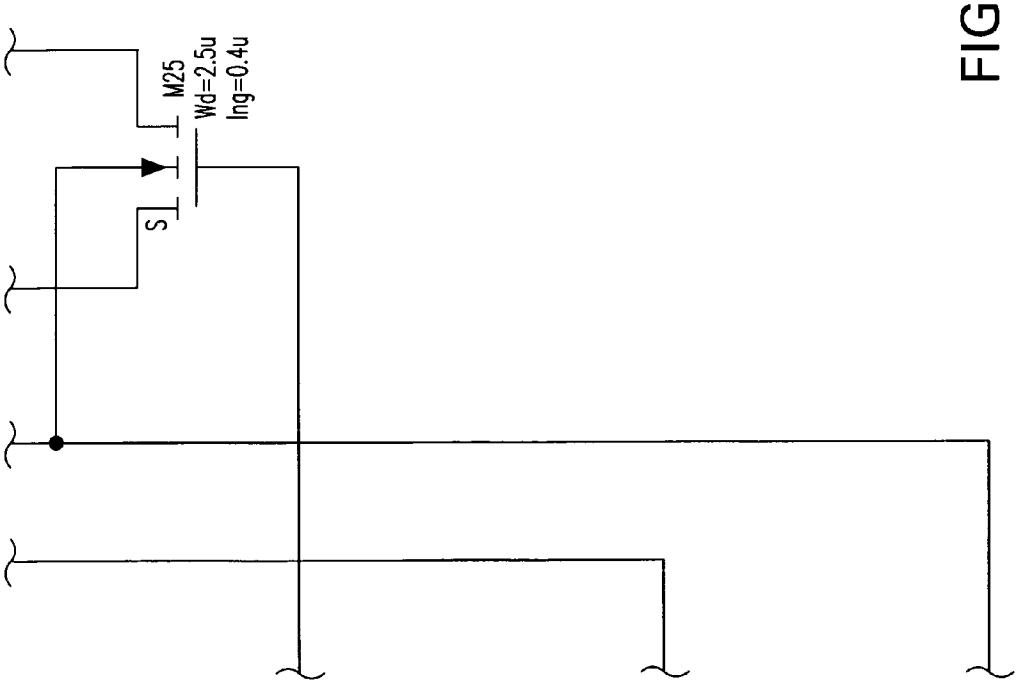


FIG.211D

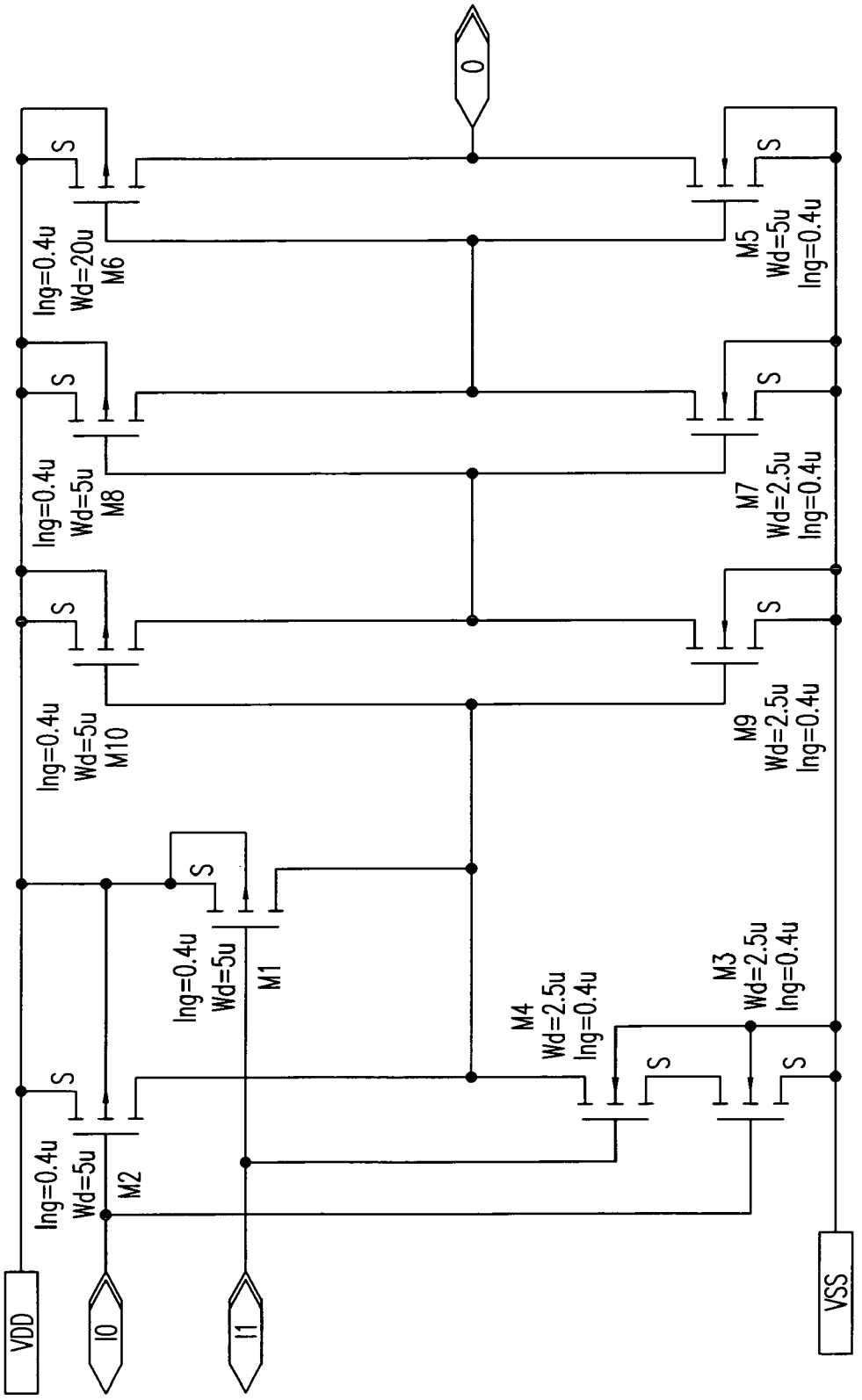

0
S
lng=0.4u
Wd=20u
M6
M5
Wd=5u
lng=0.4u
M8
M7
Wd=2.5u
M10
M9
M1
M4
M3
M2
VDD
I0
I1
VSS

FIG.212

WIRELESS LOCAL AREA NETWORK (WLAN) TECHNOLOGY AND APPLICATIONS INCLUDING TECHNIQUES OF UNIVERSAL FREQUENCY TRANSLATION

This application claims priority to U.S. Provisional Application No. 60/147,129, filed Aug. 4, 1999, which is incorporated by reference herein in its entirety.

CROSS-REFERENCE TO OTHER APPLICATIONS

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed Oct. 21, 1998, now U.S. Pat. No. 6,061,551.

"Method and System for Down-Converting Electromagnetic Signals having Optimized Switch Structures," Ser. No. 09/293,095, filed Apr. 16, 1999, now U.S. Pat. No 6,580,902.

"Method and System for Down-Converting Electromagnetic. Signals Including Resonant Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, filed Apr. 16, 1999, now U.S. Pat. No. 6,687,493.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed Oct. 21, 1998, now U.S. Pat. No. 6,091,940.

"Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," Ser. No. 09/293,580, filed Apr. 16, 1999, now U.S. Pat. No. 6,542,722.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed Oct. 21, 1998, now U.S. Pat. No. 6,061,555.

"Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed Oct. 21, 1998, now U.S. Pat. No. 6,049,706.

"Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, filed Apr. 16, 1999, now U.S. Pat. No. 6,560,301.

"Applications of Universal Frequency Translation," Ser. No. 09/261,129, filed Mar. 3, 1999, now U.S. Pat. No. 6,370,371.

"Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, filed Mar. 14, 2000, now U.S. Pat. No. 6,853,690.

"DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, filed Mar. 14, 2000, now U.S. Pat. No. 6,879,817.

"Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships," Ser. No. 09/550,644, filed Apr. 14, 2000.

"Wireless Local Area Network (WLAN) Using Universal Frequency Translation," Serial No. 09/632,855, filed Aug. 4, 2000.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally related to frequency translation, and applications of same, such as, but not limited to wireless local area networks (WLANs).

2. Related Art

Various communication components exist for performing frequency down-conversion, frequency up-conversion, and filtering in the area of wireless local area networks (WLANs). Also, schemes exist for signal reception in the face of potential jamming signals.

SUMMARY OF THE INVENTION

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

BRIEF DESCRIPTION OF THE FIGURES

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. **1**A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

FIG. **1**B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

FIG. **1**C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention.

FIG. **1**D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

FIG. **2** is a block diagram of a universal frequency translation (UFT) module according to an alternative embodiment of the invention.

FIG. **3** is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

FIG. **4** is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

FIG. **5** is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention.

FIGS. **6**A–**6**I illustrate example waveforms used to describe the operation of the UFU module.

FIG. **7** illustrates a UFT module used in a receiver according to an embodiment of the invention.

FIG. **8** illustrates a UFT module used in a transmitter according to an embodiment of the invention.

FIG. **9** illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention.

FIG. **10** illustrates a transceiver according to an embodiment of the invention.

FIG. **11** illustrates a transceiver according to an alternative embodiment of the invention.

FIG. **12** illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention.

FIG. **13** illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention.

FIG. **14** illustrates an example receiver implemented using a UDF module according to an embodiment of the invention.

FIGS. **15**A–**15**F illustrate example applications of the UDF module according to embodiments of the invention.

FIG. **16** illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention.

FIG. **17** illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention.

FIG. **18** is a table of example values at nodes in the UDF module of FIG. **17**.

FIG. **19** is a detailed diagram of an example UDF module according to an embodiment of the invention.

FIGS. **20**A and **20**G are example aliasing modules according to embodiments of the invention.

FIGS. **20**B–**20**F are example waveforms used to describe the operation of the aliasing modules of FIGS. **20**A and **20**G.

FIG. **21** illustrates an enhanced signal reception system according to an embodiment of the invention.

FIGS. **22**A–**22**F are example waveforms used to describe the system of FIG. **21**.

FIG. **23**A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention.

FIGS. **23**B and **23**C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention.

FIG. **23**D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention.

FIGS. **23**E and **23**F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention.

FIG. **24**A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention.

FIGS. **24**B–**24**J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention.

FIG. **25** illustrates a block diagram of an example computer network.

FIG. **26** illustrates a block diagram of an example computer network.

FIG. **27** illustrates a block diagram of an example wireless interface.

FIG. **28** illustrates an example heterodyne implementation of the wireless interface illustrated in FIG. **27**.

FIG. **29** illustrates an example in-phase/quadrature-phase (I/Q) heterodyne implementation of the interface illustrated in FIG. **27**.

FIG. **30** illustrates an example high level block diagram of the interface illustrated in FIG. **27**, in accordance with an embodiment of the present invention.

FIG. **31** illustrates a example block diagram of the interface illustrated in FIG. **29**, in accordance with an embodiment of the invention.

FIG. **32** illustrates an example I/Q implementation of the interface illustrated in FIG. **31**.

FIGS. **33**–**38** illustrate example environments encompassed by embodiments of the invention.

FIG. **39** illustrates a block diagram of a WLAN interface according to an embodiment of the invention.

FIG. **40** illustrates a WLAN receiver according to an embodiment of the invention.

FIG. **41** illustrates a WLAN transmitter according to an embodiment of the invention.

FIGS. **42**–**44** are example implementations of a WLAN interface. FIG. **42** includes FIGS. **42**A and **42**B which should be referred to for references to FIG. **42** in the specification. FIG. **43** includes FIGS. **43**A and **43**B which should be referred to for references to FIG. **43** in the specification. FIG. **44** includes FIGS. **44**A and **44**B which should be referred to for references to FIG. **44** in the specification.

FIGS. **45** and **46**A–C relate to an example MAC interface for an example WLAN interface embodiment.

FIGS. **47**, **48**, and **49**A–C relate to an example demodulator/modulator facilitation module for an example WLAN interface embodiment. FIG. **47** includes FIGS. **47**A–D which should be referred to for references to FIG. **47** in the specification. FIG. **48** includes FIGS. **48**A–B which should be referred to for references to FIG. **48** in the specification.

FIGS. **50**, **51**, **52**A, and **52**B relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment. FIG. **50** includes FIGS. **50** and **50**A–D which should be referred to for references to FIG. **50** in the specification. FIG. **51** inlcudes FIGS. **51**A–B which should be referred to for references to FIG. **51** in the specification.

FIGS. **53** and **54** relate to an example receiver for an example WLAN interface embodiment. FIG. **53** includes FIGS. **53**A–C which should be referred to for references to FIG. **53** in the specification.

FIGS. **55**, **56**A, and **56**B relate to an example synthesizer for an example WLAN interface embodiment. FIG. **55** inlcudes FIGS. **55**A–C which should be referred to for references to FIG. **55** in the specification.

FIGS. **57**, **58**, **59**, **60**, **61**A, and **61**B relate to an example transmitter for an example WLAN interface embodiment. FIG. **57** includes FIGS. **57**A–D which should be referred to for references to FIG. **57** in the specification. FIG. **60** includes FIGS. **60**A–D which should be referred to for references to FIG. **60** in the specification.

FIGS. **62** and **63** relate to an example motherboard for an example WLAN interface embodiment. FIG. **62** includes FIGS. **62**A–I which should be referred to for references to FIG. **62** in the specification.

FIGS. **64**, **65**, and **66** relate to example LNAs for an example WLAN interface embodiment. FIG. **64** includes FIGS. **64**A–C which should be referred to for references to FIG. **64** in the specification. FIG. **65** includes FIGS. **65**A–E which should be referred to for references to FIG. **65** in the specification. FIG. **66** includes FIGS. **66**A–B which should be referred to for references to FIG. **66** in the specification.

FIGS. **67**–**68** illustrate example WLAN station configurations with hidden nodes.

FIG. **69** illustrates a general IEEE 802.11 frame format.

FIG. **70** illustrates a request to send frame.

FIG. **71**A illustrates a transmitter according to embodiments of the present invention.

FIG. **71**B illustrates an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. **71**C illustrates an exemplary frequency spectrum for a harmonically rich signal that has multiple images that repeat at harmonics of the sampling frequency $1/T_S$, according to an embodiment of the present invention.

FIG. **71**D illustrates an example embodiment of the modulator of FIG. **71**B where the controlled switches in the UFT modules are field effect transistors (FET), according to an embodiment of the present invention.

FIG. **72**A illustrates an exemplary clock signal.

FIGS. **72**B–**72**C illustrates exemplary control signals, according to embodiments of the present invention.

FIGS. **72**D–**72**I illustrate various example signal diagrams (vs. time) that are representative of an embodiment of the invention.

FIG. **72**J depicts a frequency plot that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal given a 200 MHZ harmonic clock, according to embodiments of the present invention.

FIG. **73**A illustrates a transmitter that up-converts a baseband signal to an output signal having carrier insertion, according to an embodiment of the present invention.

FIG. **73**B illustrates an exemplary frequency spectrum for a harmonically rich signal that has multiple harmonic images, according to an embodiment of the present invention.

FIG. **74** illustrates an I/Q transmitter with an in-phase (I) and quadrature (O) configuration according to embodiments of the invention.

FIG. **75**A depicts an exemplary frequency spectrum for the harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. **75**B depicts an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. **75**C illustrates an exemplary frequency spectrum for combined harmonically rich signal having images, according to an embodiment of the present invention.

FIG. **76**A illustrates a transmitter that is a second embodiment for an I Q transmitter having a balanced configuration, according to an embodiment of the present invention.

FIG. **76**B illustrates a transmitter, according to an embodiment of the present invention.

FIG. **77** illustrates a transmitter to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules, according to an embodiment of the present invention.

FIG. **78** illustrates a transmitter that is a second embodiment of an I/Q transmitter having two DC terminals to cause DC offset, and therefore carrier insertion, according to an embodiment of the present invention.

FIG. **79**A illustrates a universal transmitter that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration, according to an embodiment of the present invention.

FIG. **79**B illustrates an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. **79**C illustrates an exemplary frequency spectrum for a harmonically rich signal that has multiple images that repeat at harmonics of the sampling frequency $1/T_S$, according to an embodiment of the present invention.

FIG. **79**D illustrates an embodiment of the modulator of FIG. **79**A, where the controlled switches in the UFT modules are field effect transistors (FET), according to the present invention.

FIG. **80** illustrates an I/Q transmitter embodiment, according to the present invention.

FIG. **81**A depicts an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. **81**B depicts an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. **81**C illustrates an exemplary frequency spectrum for an I/Q harmonically rich signal having images, according to an embodiment of the present invention, according to an embodiment of the present invention.

FIG. **82** illustrates an I/Q transmitter having a balanced configuration, according to an embodiment of the present invention.

FIG. **83** illustrates a transmitter, according to an embodiment of the present invention.

FIG. **84** shows a flowchart describing operation of the universal transmitter of FIG. **71**A, according to an exemplary embodiment of the present invention.

FIG. **85** illustrates a flowchart describing operation of the balanced modulator of FIG. **71**A, according to an exemplary embodiment of the present invention.

FIG. **86** illustrates a flowchart describing operation of the balanced modulator of FIG. **79**A, according to an exemplary embodiment of the present invention.

FIG. **87** illustrates a flowchart describing operation of the balanced modulator and other components of FIG. **74**, according to an exemplary embodiment of the present invention.

FIG. **88** illustrates a flowchart describing operation of the I/Q modulator of FIG. **80**, according to an exemplary embodiment of the present invention.

FIGS. **89**A–**89**E illustrate example embodiments for a pulse generator.

FIG. **90** illustrates an example clear to send frame.

FIG. **91** illustrates an example acknowledge (ACK) frame.

FIG. **92** illustrates an example data frame.

FIG. **93** illustrates an example information element.

FIG. **94** illustrates an example of the occurrence of multipath.

FIG. **95** illustrates an example graph showing delay spread versus symbol period.

FIG. **96** illustrates an exemplary channel impulse response.

FIG. **97** illustrates an exemplary WLAN cell.

FIG. **98** illustrates an example graph and equations related to path loss.

FIG. **99** illustrates an example graph providing a comparison of the theoretical Es/No vs Bit Error Rate (BER) curves for uncoded QPSK, PBCC 5.5–11 Mbps, CCK 5.5–11 Mbps, and Barker 1 and 2 Mbps.

FIG. **100** illustrates antenna diversity at the access point (AP).

FIG. **101**A illustrates an IBSS with mobile stations that communicate through an AP.

FIG. **101**B illustrates an AP **10102** that includes a universal frequency translation module.

FIG. **102** is an example PCMCIA test bed assembly for a WLAN interface according to an embodiment of the invention.

FIG. **103** illustrates an exemplary I/Q modulation receiver, according to an embodiment of the present invention.

FIG. **104** illustrates a I/Q modulation control signal generator, according to an embodiment of the present invention.

FIG. **105** illustrates example waveforms related to the I/Q modulation control signal generator of FIG. **104**.

FIG. **106** illustrates example control signal waveforms overlaid upon an input RF signal.

FIG. **107** illustrates a I/Q modulation receiver circuit diagram, according to an embodiment of the present invention.

FIGS. **108**–**118** illustrate example waveforms related to the receiver of FIG. **107**.

FIG. **119** illustrates a single channel receiver, according to an embodiment of the present invention.

FIG. **120** illustrates some aspects of charge injection related to embodiments of the present invention.

FIG. **121** illustrates an exemplary circuit configuration for reducing DC offset voltage caused by charge injection, according to an embodiment of the present invention.

FIG. **122** depicts a flowchart that illustrates operational steps for down-converting an input signal and reducing a DC offset voltage, according to an embodiment of the present invention.

FIG. **123** depicts a flowchart that illustrates operational steps for down-converting a RF I/Q modulated signal and reducing DC offset voltages, according to an embodiment of the present invention.

FIG. **124** illustrates an example IBSS with mobile stations that must be in direct communication range to communicate with each other.

FIG. **125** illustrates an exemplary ESS.

FIG. **126** illustrates a state diagram showing the relationship between state variables and services.

FIG. **127** illustrates a station moving between APs.

FIG. **128**A illustrates an OSI model including a PHY layer.

FIGS. **128**B–**128**D illustrate exemplary block diagrams of PMD sublayers incorporating universal frequency translation technology, according to embodiments of the present invention.

FIG. **129**A illustrates an exemplary DSSS PMD transmitter.

FIG. **129**B illustrates an exemplary DSSS PMD receiver.

FIG. **129**C illustrates an exemplary block diagrams of a DPSK modulation mode transmitter, according to an embodiment of the present invention.

FIGS. **129**D–**129**F illustrate exemplary block diagrams related to DBPSK modulation mode transmitters, according to embodiments of the present invention.

FIGS. **129**G–**129**I illustrate exemplary block diagrams related to DQPSK modulation mode transmitters, according to embodiments of the present invention.

FIG. **129**J illustrates an exemplary block diagrams of a DBPSK/DQPSK modulation mode receiver, according to an embodiment of the present invention.

FIG. **129**K illustrates an exemplary block diagram of a de-spread correlator and a DBPSK/DQPSK demodulator sharing components, according to embodiments of the present invention.

FIG. **129**L illustrates an exemplary block diagram of a receiver DSSS PMD, according to an embodiment of the present invention.

FIGS. **129**M–**129**P illustrate exemplary block diagrams related to DBPSK modulation mode receivers, according to embodiments of the present invention.

FIGS. **129**Q–**129**S illustrate exemplary block diagrams related to DQPSK modulation mode transmitters, according to embodiments of the present invention.

FIG. **130** illustrates a PPDU frame.

FIG. **131** illustrates constellation patterns related to DBPSK and DQPSK modulation.

FIG. **132**A illustrates application of an 11-bit Barker word and information bits to a modulo-2 adder (XOR function).

FIGS. **132**B–**132**E illustrate transmitter and receiver signals before and after spreading.

FIG. **133** illustrates a filtered SinX/X function.

FIG. **134** illustrates a DSSS channel arrangement for North America.

FIGS. **135**A and **135**B illustrate block diagrams showing elements of the FHSS PMD transmitter and receiver, respectively.

FIG. **135**C illustrates an exemplary block diagram of a 2-level/4-level GFSK modulator, according to an embodiment of the present invention.

FIGS. **135**D–**135**E illustrate exemplary block diagrams related to the 2-level/4-level GFSK modulator of FIG. **135**C, according to embodiments of the present invention.

FIG. **135**F illustrates an exemplary block diagram of a 2-level/4-level GFSK demodulator, according to an embodiment of the present invention.

FIG. **135**G illustrates an exemplary block diagrams related to the 2-level/4-level GFSK modulator of FIG. **135**F, according to an embodiment of the present invention.

FIG. **136** illustrates a PLCP protocol data unit (PPDU) related to a DSSS PHY.

FIG. **137** illustrates a block diagram of an exemplary IR PMD sublayer.

FIG. **138** illustrates a PPDU related to an IR PHY.

FIG. **139** illustrates a PPDU related to an OFDM PHY.

FIGS. **140**A and **140**B illustrate exemplary block diagrams of an IEEE 802.11a OFDM PMD transmitter and receiver, respectively.

FIGS. **140**C illustrates an exemplary PSK/QAM modulator, according to an embodiment of the present invention.

FIGS. **140**D–**140**E illustrate exemplary block diagrams for transmitting BPSK modulated signals related to the PSK/QAM modulator of FIG. **140**C, according to embodiments of the present invention.

FIGS. **140**F–**140**H illustrate exemplary block diagrams for transmitting QAM modulated signals related to the PSK/QAM modulator of FIG. **140**C, according to embodiments of the present invention.

FIG. **140**I illustrates an exemplary PSK/QAM demodulator, according to an embodiment of the present invention.

FIG. **140**J illustrates an exemplary block diagram for receiving BPSK modulated signals related to the PSK/QAM demodulator of FIG. **140**I, according to an embodiment of the present invention.

FIGS. **140**K–**140**L illustrate exemplary block diagrams for receiving QPSK/QAM modulated signals related to the PSK/QAM demodulator of FIG. **1401**, according to embodiments of the present invention.

FIG. **141**A illustrates a PPDU with a long PLCP preamble.

FIG. **141**B illustrates a PPDU with a short preamble.

FIG. **142** illustrates an example of a typical HR/DSSS channel arrangement for non-interfering channels for North America.

FIG. **143**A illustrates an exemplary transmit HR/DSSS PMD, according to an embodiment of the present invention.

FIG. **143**B illustrates an exemplary block diagram for a CCK modulator.

FIGS. **144**A and **144**B illustrate use of scrambled binary bits of the PSDU for 5.5 Mbps and 11 Mbps operation.

FIG. **145**A illustrates an exemplary PBCC modulator.

FIG. **145**B illustrates a receiver HR/DSSS PMD, according to an embodiment of the present invention.

FIG. **145**C illustrates a receiver HR/DSSS PMD that includes a CCK demodulator, according to an embodiment of the present invention.

FIG. **145**D illustrates a receiver HR/DSSS PMD that includes a PBCC demodulator, according to an embodiment of the present invention.

FIGS. **146**–**212** illustrate schematics showing an integrated circuit implementation of an exemplary embodiment of the present invention. FIG. **148** includes FIGS. **148**A–D which should be referred to for references to FIG. **148** in the specification. FIG. **156** includes FIGS. **156** and **156**A–V which should be referred to for references to FIG. **156** in the specification. FIG. **157** includes FIGS. **157**A–F which should be referred to for references to FIG. **157** in the specification. FIG. **158** includes FIGS. **158**A–D which should be referred to for references to FIG. **158** in the specification. FIG. **160** includes FIGS. **160**A–D which should be referred to for references to FIG. **160** in the specification. FIG. **161** includes FIGS. **161**A–D which should be referred to for references to FIG. **161** in the specification. FIG. **163** includes FIGS. **163**A–D which should be referred to for references to FIG. **163** in the specification. FIG. **164** includes FIGS. **164**A–F which should be referred to for references to FIG. **164** in the specification. FIG. **166** includes FIGS. **166**A–F whouch should be referred to for references to FIG. **166** in the specification. FIG. **169** inlcude FIGS. **169**A–D which should be referred to for references to FIG. **169** in the specification. FIG. **174** includes FIGS. **174**A–H which should be referred to for references to FIG. **174** in the specification. FIG. **176** includes FIGS. **176**A–H which should be referred to for references to FIG. **176** in the specification. FIG. **177** includes FIGS. **177**A–H which should be referred to for references to FIG. **177** in the specification. FIG. **201** includes FIGS. **201**A–H which should be referred to for references to FIG. **201** in the specification. FIG. **210** includes FIGS. **210**A–D which should be referred to for references to FIG. **210** in the specification. FIG. **211** includes FIGS. **211**A–D which should be referred to for references to FIG. **211** in the specification.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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8. Conclusions

1. Universal Frequency Translation

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-

conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. **1**A illustrates a universal frequency translation (UFT) module **102** according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. **1**A, some embodiments of the UFT module **102** include three ports (nodes), designated in FIG. **1**A as Port **1**, Port **2**, and Port **3**. Other UFT embodiments include other than three ports.

Generally, the UFT module **102** (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module **102** (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module **103** is generally illustrated in FIG. **1**B. Generally, the UFT module **103** includes a switch **106** controlled by a control signal **108**. The switch **106** is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. **2** illustrates an example UFT module **202**. The example UFT module **202** includes a diode **204** having two ports, designated as Port **1** and Port **2**/**3**. This embodiment does not include a third port, as indicated by the dotted line around the "Port **3**" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the—usefulness and performance of such applications. For example, a UFT module **115** can be used in a universal frequency down-conversion (UFD) module **114**, an example of which is shown in FIG. **1**C. In this capacity, the UFT module **115** frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. **1**D, a UFT module **117** can be used in a universal frequency up-conversion (UFU) module **116**. In this capacity, the UFT module **117** frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. Frequency Down-Conversion

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998, the full disclosure of which is incorporated herein by reference, as well as other applications cited above. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. **20**A illustrates an aliasing module **2000** (also called a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module **2002** which down-converts an EM input signal **2004**. In particular embodiments, aliasing module **2000** includes a switch **2008** and a capacitor **2010**. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch **2008** is in series with input signal **2004** and capacitor **2010** is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. **20**G), the capacitor **2010** is in series with the input signal **2004** and the switch **2008** is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module **2000** with UFT module **2002** can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal **2004**.

In one implementation, aliasing module **2000** down-converts the input signal **2004** to an intermediate frequency (IF) signal. In another implementation, the aliasing module **2000** down-converts the input signal **2004** to a demodulated baseband signal. In yet another implementation, the input signal **2004** is a frequency modulated (FM) signal, and the aliasing module **2000** down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal **2006** includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal **2004**. In this embodiment, the control signal **2006** is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal **2004**. Preferably, the frequency of control signal **2006** is much less than the input signal **2004**.

A train of pulses **2018** as shown in FIG. **20**D controls the switch **2008** to alias the input signal **2004** with the control signal **2006** to generate a down-converted output signal **2012**. More specifically, in an embodiment, switch **2008** closes on a first edge of each pulse **2020** of FIG. **20**D and opens on a second edge of each pulse. When the switch **2008** is closed, the input signal **2004** is coupled to the capacitor **2010**, and charge is transferred from the input signal to the capacitor **2010**. The charge stored during successive pulses forms down-converted output signal **2012**.

Exemplary waveforms are shown in FIGS. **20**B–**20**F.

FIG. **20**B illustrates an analog amplitude modulated (AM) carrier signal **2014** that is an example of input signal **2004**. For illustrative purposes, in FIG. **20**C, an analog AM carrier signal portion **2016** illustrates a portion of the analog AM carrier signal **2014** on an expanded time scale. The analog AM carrier signal portion **2016** illustrates the analog AM carrier signal **2014** from time t_0 to time t_1.

FIG. **20**D illustrates an exemplary aliasing signal **2018** that is an example of control signal **2006**. Aliasing signal **2018** is on approximately the same time scale as the analog AM carrier signal portion **2016**. In the example shown in FIG. **20**D, the aliasing signal **2018** includes a train of pulses **2020** having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses **2020** repeat at an aliasing rate, or pulse repetition rate of aliasing signal **2018**. The aliasing rate is determined as described below, and further described in U.S.

Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998.

As noted above, the train of pulses **2020** (i.e., control signal **2006**) control the switch **2008** to alias the analog AM carrier signal **2016** (i.e., input signal **2004**) at the aliasing rate of the aliasing signal **2018**. Specifically, in this embodiment, the switch **2008** closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch **2008** is closed, input signal **2004** is coupled to the capacitor **2010**, and charge is transferred from the input signal **2004** to the capacitor **2010**. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples **2022** form down-converted signal portion **2024** (FIG. **20**E) that corresponds to the analog AM carrier signal portion **2016** (FIG. **20**C) and the train of pulses **2020** (FIG. **20**D). The charge stored during successive under-samples of AM carrier signal **2014** form the down-converted signal **2024** (FIG. **20**E) that is an example of down-converted output signal **2012** (FIG. **20**A). In FIG. **20**F, a demodulated baseband signal **2026** represents the demodulated baseband signal **2024** after filtering on a compressed time scale. As illustrated, down-converted signal **2026** has substantially the same "amplitude envelope" as AM carrier signal **2014**. Therefore, FIGS. **20**B–**20**F illustrate down-conversion of AM carrier signal **2014**.

The waveforms shown in FIGS. **20**B–**20**F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998.

The aliasing rate of control signal **2006** determines whether the input signal **2004** is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal **2004**, the aliasing rate of the control signal **2006**, and the down-converted output signal **2012** are illustrated below:

(Freq. of input signal **2004**)=*n*·(Freq. of control signal **2006**)±(Freq. of down-converted output signal **2012**)

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal **2004** (e.g., n=0.5, 1, 2, 3, . . .).

When the aliasing rate of control signal **2006** is off-set from the frequency of input signal **2004**, or off-set from a harmonic or sub-harmonic thereof, input signal **2004** is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal **2004**. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal **2004** includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal **2006** would be calculated as follows:

$(Freq_{input}-Freq_{IF})/n=Freq_{control}$ (901 MHZ-1 MHZ)/n=900/n

For n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998.

Alternatively, when the aliasing rate of the control signal **2006** is substantially equal to the frequency of the input signal **2004**, or substantially equal to a harmonic or sub-harmonic thereof, input signal **2004** is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal **2004**. As a result, the under-samples form a constant output baseband signal. If the input signal **2004** includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal **2006** would be calculated as follows:

$(Freq_{input}-Freq_{IF})/n=Freq_{control}$ (900 MHZ–0 MHZ)/n=900 MHZ/n

For n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1+F_2)\div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal **2006** would be calculated as follows:

$$\text{Frequency of the input} = (F_1 + F_2) \div 2$$
$$= (899\ \text{MHZ} + 901\ \text{MHZ}) \div 2 = 900\ \text{MHZ}$$

Frequency of the down-converted signal=0 (i.e., baseband)

$(Freq_{input}-Freq_{IF})/n=Freq_{control}$ (900 MHZ–0 MHZ)/n=900 MHZ/n

For n=0.5, 1, 2, 3, etc., the frequency of the control signal **2006** should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK

signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal **2006** should be substantially equal to:

(900 MHZ−0 MHZ)/*n*=900 MHZ/n, or (901 MHZ−0 MHZ)/*n*=901 MHZ/*n*.

For the former case of 900 MHZ/n, and for n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for n=0.5, 1, 2, 3, 4, etc., the frequency of the control signal **2006** should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998.

In an embodiment, the pulses of the control signal **2006** have negligible apertures that tend towards zero. This makes the UFT module **2002** a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal **2006** have non-negligible apertures that tend away from zero. This makes the UFT module **2002** a lower input impedance device. This allows the lower input impedance of the UFT module **2002** to be substantially matched with a source impedance of the input signal **2004**. This also improves the energy transfer from the input signal **2004** to the down-converted output signal **2012**, and hence the efficiency and signal to noise (s/n) ratio of UFT module **2002**.

Exemplary systems and methods for generating and optimizing the control signal **2006**, and for otherwise improving energy transfer and s/n ratio, are disclosed in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998.

2.1 Charge Injection Reduction Embodiment

In this section, an embodiment, according to the present invention, is provided for reducing or eliminating DC offset due at least to charge injection. FIG. **120** illustrates some aspects of charge injection related to the present invention. FIG. **120** shows a UFD module **12000** comprising a UFT module **12002**, a storage device **12004**, and a reference potential **12006**. In an embodiment, UFT module **12002** comprises a MOSFET **12008**, and storage device **12004** comprises a capacitor **12010**, although the invention is not limited to this example.

An input RF signal **12014** is received by a first terminal **12028** of MOSFET **12008**. A control signal **12018** is received by a second terminal **12030** of MOSFET **12008**. A third terminal **12032** of MOSFET **12008** is coupled to a first terminal **12034** of storage device **12004**. A second terminal **12036** of storage device **12004** is coupled to reference potential **12006** such as a ground **12012**, or some other potential. In an embodiment, MOSFET **12008** contained within UFT module **12002** opens and closes as a function of control signal **12018**. As a result of the opening and closing of this switch, a down-converted signal, referred to as output signal **12016**, results.

A well known phenomenon called charge injection may occur in such a switching environment. As control signal **12018** applies a pulse waveform to the gate of MOSFET **12008**, MOSFET **12008** is caused to open and close. During this operation, charge allowed to flow along a DC path **12024** may build on the gate-to-drain and/or gate-to-source junctions of MOSFET **12008**, as indicated on FIG. **120** as charge buildup **12020** (note that the source and drain terminals of MOSFET **12008** are essentially interchangeable). Charge buildup **12020** may leak from MOSFET **12008** through leakage path **12022**, and become stored on capacitor **12010**. This charge that becomes stored on capacitor **12010** may cause a change in the voltage across capacitor **12010**. This voltage change may accordingly appear on output signal **12016** as a potentially non-negligible DC offset voltage. This non-negligible DC offset voltage on output signal **12016** may lead to difficulties in recovering the baseband information content of output signal **12016**. Hence, it would be advantageous to reduce or prevent this potential generation of DC offset voltage caused by this interaction of control signal **12018** with UFD module **12000**.

FIG. **121** illustrates an exemplary circuit configuration for reducing unwanted DC offset voltage caused by charge injection, according to an embodiment of the present invention.

FIG. **121** shows UFD module **12000** of FIG. **120**, with a capacitor **12126** coupled between input RF signal **12014** and UFD module **12000**. Capacitor **12126** is preferably a small valued capacitor, such as, but not limited to, 10 pF. The value for capacitor **12126** will vary depending upon the application, and accordingly its characteristics are implementation and application specific. Capacitor **12126** prevents DC current from flowing along the path shown as DC path **12024** in FIG. **120**, and thus reduces or prevents the flow of charge to, and build up of charge on capacitor **12010**. This in turn reduces or prevents a DC offset voltage resulting from the above described charge injection from appearing on output signal **12016**. Hence, the baseband information content of output signal **12016** may be more accurately ascertained.

FIG. **122** depicts a flowchart **12200** that illustrates operational steps corresponding to FIG. **121**, for down-converting an input signal and reducing a DC offset voltage, according to an embodiment of the present invention. The invention is not limited to this operational description. Rather, it will be apparent to persons skilled in the relevant art(s) from the teachings herein that other operational control flows are within the scope and spirit of the present invention. It is noted that the ordering of steps is flexible, and not limited to that shown in the flowcharts, and described herein. In the following discussion, the steps in FIG. **122** will be described.

In step **12202**, an input signal is coupled by a series capacitor to an input of a universal frequency down-conversion module.

In step **12204**, the input signal is frequency down-converted with the universal frequency down-conversion module to a down-converted signal. The input signal is down-converted according to a control signal. The control signal under-samples the input signal.

In step **12206**, a DC offset voltage in the down-converted signal generated during step **12204** is reduced. In an embodiment, the DC offset voltage is generated at least by charge injection effects due to interaction of the control signal with the universal frequency down-conversion module, as further described above.

It should be understood that the above examples are provided for illustrative purposes only. The invention is not

limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

2.2 Example I/Q Modulation Receiver Embodiments

FIG. **103** illustrates an exemplary I/Q modulation receiver **10300**, according to an embodiment of the present invention. I/Q modulation receiver **10300** has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation.

I/Q modulation receiver **10300** comprises a first UFD module **10302**, a first optional filter **10304**, a second UFD module **10306**, a second optional filter **10308**, a third UFD module **10310**, a third optional filter **10312**, a fourth UFD module **10314**, a fourth filter **10316**, an optional LNA **10318**, a first differential amplifier **10320**, a second differential amplifier **10322**, and an antenna **10372**.

I/Q modulation receiver **10300** receives, down-converts, and demodulates a I/Q modulated RF input signal **10382** to an I baseband output signal **10384**, and a Q baseband output signal **10386**. I/Q modulated RF input signal comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal **10384** comprises the first baseband information signal. Q baseband output signal **10386** comprises the second baseband information signal.

Antenna **10372** receives I/Q modulated RF input signal **10382**. I/Q modulated RF input signal **10382** is output by antenna **10372** and received by optional LNA **10318**. When present, LNA **10318** amplifies I/Q modulated RF input signal **10382**, and outputs amplified I/Q signal **10388**.

First UFD module **10302** receives amplified I/Q signal **10388**. First UFD module **10302** down-converts the I-phase signal portion of amplified input I/Q signal **10388** according to an I control signal **10390**. First UFD module **10302** outputs an I output signal **10398**.

In an embodiment, first UFD module **10302** comprises a first storage module **10324**, a first UFT module **10326**, and a first voltage reference **10328**. In an embodiment, a switch contained within first UFT module **10326** opens and closes as a function of I control signal **10390**. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module **10324** to and from first voltage reference **10328**, a down-converted signal, referred to as I output signal **10398**, results. First voltage reference **10328** may be any reference voltage, and is preferably ground. I output signal **10398** is stored by first storage module **10324**.

In a preferred embodiment, first storage module **10324** comprises a first capacitor **10374**. In addition to storing I output signal **10398**, first capacitor **10374** reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on I output signal **10398**, in a similar fashion to that of capacitor **12126** shown in FIG. **121**. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor **12126**.

I output signal **10398** is received by optional first filter **10304**. When present, first filter **10304** is a high pass filter to at least filter I output signal **10398** to remove any carrier signal "bleed through". In a preferred embodiment, when present, first filter **10304** comprises a first resistor **10330**, a first filter capacitor **10332**, and a first filter voltage reference **10334**. Preferably, first resistor **10330** is coupled between I output signal **10398** and a filtered I output signal **10307**, and first filter capacitor **10332** is coupled between filtered I output signal **10307** and first filter voltage reference **10334**. Alternately, first filter **10304** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). First filter **10304** outputs filtered I output signal **10307**.

Second UFD module **10306** receives amplified I/Q signal **10388**. Second UFD module **10306** down-converts the inverted I-phase signal portion of amplified input I/Q signal **10388** according to an inverted I control signal **10392**. Second UFD module **10306** outputs an inverted I output signal **10301**.

In an embodiment, second UFD module **10306** comprises a second storage module **10336**, a second UFT module **10338**, and a second voltage reference **10340**. In an embodiment, a switch contained within second UFT module **10338** opens and closes as a function of inverted I control signal **10392**. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module **10336** to and from second voltage reference **10340**, a down-converted signal, referred to as inverted I output signal **10301**, results. Second voltage reference **10340** may be any reference voltage, and is preferably ground. Inverted I output signal **10301** is stored by second storage module **10336**.

In a preferred embodiment, second storage module **10336** comprises a second capacitor **10376**. In addition to storing inverted I output signal **10301**, second capacitor **10376** reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted I output signal **10301**, in a similar fashion to that of capacitor **12126** shown in FIG. **121**. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor **12126**.

Inverted I output signal **10301** is received by optional second filter **10308**. When present, second filter **10308** is a high pass filter to at least filter inverted I output signal **10301** to remove any carrier signal "bleed through". In a preferred embodiment, when present, second filter **10308** comprises a second resistor **10342**, a second filter capacitor **10344**, and a second filter voltage reference **10346**. Preferably, second resistor **10342** is coupled between inverted I output signal **10301** and a filtered inverted I output signal **10309**, and second filter capacitor **10344** is coupled between filtered inverted I output signal **10309** and second filter voltage reference **10346**. Alternately, second filter **10308** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Second filter **10308** outputs filtered inverted I output signal **10309**.

First differential amplifier **10320** receives filtered I output signal **10307** at its non-inverting input and receives filtered inverted I output signal **10309** at its inverting input. First differential amplifier **10320** subtracts filtered inverted I output signal **10309** from filtered I output signal **10307**, amplifies the result, and outputs I baseband output signal **10384**. Other suitable subtractor and/or amplification modules may be substituted for first differential amplifier **10320**, and second differential amplifier **10322**, as would be understood by persons skilled in the relevant art(s) from the teachings herein. Because filtered inverted I output signal **10309** is substantially equal to an inverted version of filtered I output signal **10307**, I baseband output signal **10384** is substantially equal to filtered I output signal **10309**, with its amplitude doubled. Furthermore, filtered I output signal **10307** and filtered inverted I output signal **10309** may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion

circuitry, including first UFD module **10302** and second UFD module **10306**, respectively. When first differential amplifier **10320** subtracts filtered inverted I output signal **10309** from filtered I output signal **10307**, these noise and DC offset contributions substantially cancel each other.

Third UFD module **10310** receives amplified I/Q signal **10388**. Third UFD module **10310** down-converts the Q-phase signal portion of amplified input I/Q signal **10388** according to an Q control signal **10394**. Third UFD module **10310** outputs an Q output signal **10303**.

In an embodiment, third UFD module **10310** comprises a third storage module **10348**, a third UFT module **10350**, and a third voltage reference **10352**. In an embodiment, a switch contained within third UFT module **10350** opens and closes as a function of Q control signal **10394**. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module **10348** to and from third voltage reference **10352**, a down-converted signal, referred to as Q output signal **10303**, results. Third voltage reference **10352** may be any reference voltage, and is preferably ground. Q output signal **10303** is stored by third storage module **10348**.

In a preferred embodiment, third storage module **10348** comprises a third capacitor **10378**. In addition to storing Q output signal **10303**, third capacitor **10378** reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on Q output signal **10303**, in a similar fashion to that of capacitor **12126** shown in FIG. **121**. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor **12126**.

Q output signal **10303** is received by optional third filter **10312**. When present, third filter **10312** is a high pass filter to at least filter Q output signal **10303** to remove any carrier signal "bleed through". In a preferred embodiment, when present, third filter **10312** comprises a third resistor **10354**, a third filter capacitor **10358**, and a third filter voltage reference **10358**. Preferably, third resistor **10354** is coupled between Q output signal **10303** and a filtered Q output signal **10311**, and third filter capacitor **10356** is coupled between filtered Q output signal **10311** and third filter voltage reference **10358**. Alternately, third filter **10312** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Third filter **10312** outputs filtered Q output signal **10311**.

Fourth UFD module **10314** receives amplified I/Q signal **10388**. Fourth UFD module **10314** down-converts the inverted Q-phase signal portion of amplified input I/Q signal **10388** according to an inverted Q control signal **10396**. Fourth UFD module **10314** outputs an inverted Q output signal **10305**.

In an embodiment, fourth UFD module **10314** comprises a fourth storage module **10360**, a fourth UFT module **10362**, and a fourth voltage reference **10364**. In an embodiment, a switch contained within fourth UFT module **10362** opens and closes as a function of inverted Q control signal **10396**. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module **10360** to and from fourth voltage reference **10364**, a down-converted signal, referred to as inverted Q output signal **10305**, results. Fourth voltage reference **10364** may be any reference voltage, and is preferably ground. Inverted Q output signal **10305** is stored by fourth storage module **10360**.

In a preferred embodiment, fourth storage module **10360** comprises a fourth capacitor **10380**. In addition to storing inverted Q output signal **10305**, fourth capacitor **10380** reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted Q output signal **10305**, in a similar fashion to that of capacitor **12126** shown in FIG. **121**. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor **12126**.

Inverted Q output signal **10305** is received by optional fourth filter **10316**. When present, fourth filter **10316** is a high pass filter to at least filter inverted Q output signal **10305** to remove any carrier signal "bleed through". In a preferred embodiment, when present, fourth filter **10316** comprises a fourth resistor **10366**, a fourth filter capacitor **10368**, and a fourth filter voltage reference **10370**. Preferably, fourth resistor **10366** is coupled between inverted Q output signal **10305** and a filtered inverted Q output signal **10313**, and fourth filter capacitor **10368** is coupled between filtered inverted Q output signal **10313** and fourth filter voltage reference **10370**. Alternately, fourth filter **10316** may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Fourth filter **10316** outputs filtered inverted Q output signal **10313**.

Second differential amplifier **10322** receives filtered Q output signal **10311** at its non-inverting input and receives filtered inverted Q output signal **10313** at its inverting input. Second differential amplifier **10322** subtracts filtered inverted Q output signal **10313** from filtered Q output signal **10311**, amplifies the result, and outputs Q baseband output signal **10386**. Because filtered inverted Q output signal **10313** is substantially equal to an inverted version of filtered Q output signal **10311**, Q baseband output signal **10386** is substantially equal to filtered Q output signal **10313**, with its amplitude doubled. Furthermore, filtered Q output signal **10311** and filtered inverted Q output signal **10313** may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third UFD module **10310** and fourth UFD module **10314**, respectively. When second differential amplifier **10322** subtracts filtered inverted Q output signal **10313** from filtered Q output signal **10311**, these noise and DC offset contributions substantially cancel each other.

FIG. **123** depicts a flowchart **12300** that illustrates operational steps corresponding to FIG. **103**, for down-converting a RF I/Q modulated signal and reducing DC offset voltages, according to an embodiment of the present invention. The invention is not limited to this operational description. Rather, it will be apparent to persons skilled in the relevant art(s) from the teachings herein that other operational control flows are within the scope and spirit of the present invention. In the following discussion, the steps in FIG. **123** will be described.

In step **12302**, an input signal is received, wherein the input signal comprises an RF I/Q modulated signal.

In step **12304**, the input signal is frequency down-converted with a first universal frequency down-conversion module to a first down-converted signal, according to a first control signal. In an embodiment, the input signal is frequency down-converted to a non-inverted I-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a first phase of the in-phase signal portion of the RF I/Q modulated signal is under-sampled. In an embodiment, the RF I/Q modulated signal may be under-sampled every 3.0 cycles of a frequency of the RF I/Q modulated signal by the first control signal. Furthermore, in embodiments, a first DC offset voltage in the first down-converted signal is reduced by a capacitor of the first universal frequency down-conversion module.

In step **12306**, the input signal is frequency down-converted with a second universal frequency down-conversion module to a second down-converted signal, according to a second control signal. In an embodiment, the input signal is frequency down-converted to an inverted Q-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a second phase of the in-phase signal portion of the RF I/Q modulated signal is under-sampled, wherein the second phase of the in-phase signal portion is of an opposite phase to the first phase under-sampled of the in-phase signal portion. The RF I/Q modulated signal may be sampled 1.5 cycles of a frequency of the RF I/Q modulated signal after under-sampling the RF I/Q modulated signal in step **12304**, for example. Furthermore, in embodiments, a second DC offset voltage in the second down-converted signal is reduced by a capacitor of the second universal frequency down-conversion module.

In step **12308**, the second down-converted signal is subtracted from the first down-converted signal to form a first output signal. In embodiments, a first DC offset voltage in the first down-converted signal and a second DC offset voltage in the second down-converted signal cancel one another.

In step **12310**, the input signal is frequency down-converted with a third universal frequency down-conversion module to a third down-converted signal, according to a third control signal. In an embodiment, the input signal is frequency down-converted to a non-inverted Q-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a third phase of the quadrature-phase signal portion of the RF I/Q modulated signal is under-sampled. The RF I/Q modulated signal may be under-sampled 0.75 cycles of the frequency of the RF I/Q modulated signal after under-sampling of the RF I/Q modulated signal occurs in step **12304**, for example. Furthermore, in embodiments, a third DC offset voltage in the third down-converted signal is reduced by a capacitor of the third universal frequency down-conversion module.

In step **12312**, the input signal is frequency down-converted with a fourth universal frequency down-conversion module to a fourth down-converted signal, according to a fourth control signal. In an embodiment, the input signal is frequency down-converted to an inverted I-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a fourth phase of the quadrature-phase signal portion of the RF I/Q modulated signal is under-sampled, wherein the fourth phase of the quadrature-phase signal portion is of an opposite phase to the third phase under-sampled of the quadrature-phase signal portion. In an embodiment, the RF I/Q modulated signal may be sampled 1.5 cycles of the frequency of the RF I/Q modulated signal after under-sampling of the RF I/Q modulated signal occurs in step **12304**, for example. Furthermore, in embodiments, a fourth DC offset voltage in the fourth down-converted signal is reduced by a capacitor of fourth universal frequency down-conversion module.

In step **12314**, the fourth down-converted signal is subtracted from the third down-converted signal to form a second output signal. In embodiments, a third DC offset voltage in the third down-converted signal and a fourth DC offset voltage in the fourth down-converted signal cancel one another.

In step **12316**, a signal is re-radiated that comprises attenuated components of first, second, third, and fourth control signal pulses, wherein the attenuated components of the first, second, third, and fourth control signal pulses form a cumulative frequency, as discussed above.

In step **12318**, the first, second, third, and fourth control signal pulses are configured such that the cumulative frequency is greater than a frequency of the input signal, as discussed above.

2.2.1 Example I/Q Modulation Control Signal Generator Embodiments

FIG. **104** illustrates an exemplary block diagram for I/Q modulation control signal generator **10400**, according to an embodiment of the present invention. I/Q modulation control signal generator **10400** generates I control signal **10390**, inverted I control signal **10392**, Q control signal **10394**, and inverted Q control signal **10396** used by I/Q modulation receiver **10300** of FIG. **103**. I control signal **10390** and inverted I control signal **10392** operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal **10394** and inverted Q control signal **10396** act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator **10400** has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator **10400** comprises a local oscillator **10402**, a first divide-by-two module **10404**, a 180 degree phase shifter **10406**, a second divide-by-two module **10408**, a first pulse generator **10410**, a second pulse generator **10412**, a third pulse generator **10414**, and a fourth pulse generator **10416**.

Local oscillator **10402** outputs an oscillating signal **10418**. FIG. **105** shows an exemplary oscillating signal **10418**.

First divide-by-two module **10404** receives oscillating signal **10418**, divides oscillating signal **10418** by two, and outputs a half frequency LO signal **10420** and a half frequency inverted LO signal **10426**. FIG. **105** shows an exemplary half frequency LO signal **10420**. Half frequency inverted LO signal **10426** is an inverted version of half frequency LO signal **10420**. First divide-by-two module **10404** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

180 degree phase shifter **10406** receives oscillating signal **10418**, shifts the phase of oscillating signal **10418** by 180 degrees, and outputs phase-shifted LO signal **10422**. 180 degree phase shifter **10406** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s). In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module **10408** receives phase-shifted LO signal **10422**, divides phase-shifted LO signal **10422** by two, and outputs a half frequency phase-shifted LO signal **10424** and a half frequency inverted phase-shifted LO signal **10428**. FIG. **105** shows an exemplary half frequency phase-shifted LO signal **10424**. Half frequency inverted phase-shifted LO signal **10428** is an inverted version of half frequency phase-shifted LO signal **10424**. Second divide-by-two module **10408** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

First pulse generator **10410** receives half frequency LO signal **10420**, generates an output pulse whenever a rising

edge is received on half frequency LO signal **10420**, and outputs I control signal **10390**. FIG. **105** shows an exemplary I control signal **10390**.

Second pulse generator **10412** receives half frequency inverted LO signal **10426**, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal **10426**, and outputs inverted I control signal **10392**. FIG. **105** shows an exemplary inverted I control signal **10392**.

Third pulse generator **10414** receives half frequency phase-shifted LO signal **10424**, generates an output pulse whenever a rising edge is received on half frequency phase-shifted LO signal **10424**, and outputs Q control signal **10394**. FIG. **105** shows an exemplary Q control signal **10394**.

Fourth pulse generator **10416** receives half frequency inverted phase-shifted LO signal **10428**, generates an output pulse whenever a rising edge is received on half frequency inverted phase-shifted LO signal **10428**, and outputs inverted Q control signal **10396**. FIG. **105** shows an exemplary inverted Q control signal **10396**.

In a preferred embodiment, control signals **10390**, **10392**, **10394** and **10396** output pulses having a width equal to one-half of a period of I/Q modulated RF input signal **10382**. The invention, however, is not limited to these pulse widths, and control signals **10390**, **10392**, **10394**, and **10396** may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal **10382**.

First, second, third, and fourth pulse generators **10410**, **10412**, **10414**, and **10416** may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

As shown in FIG. **105**, control signals **10390**, **10392**, **10394**, and **10396** comprise pulses that are non-overlapping. Furthermore, in this example, pulses appear on these signals in the following order: I control signal **10390**, Q control signal **10394**, inverted I control signal **10392**, and inverted Q control signal **10396**. Potential circuit re-radiation from I/Q modulation receiver **10300** may comprise frequency components from a combination of these control signals.

For example, FIG. **106** shows an overlay of pulses from 1 control signal **10390**, Q control signal **10394**, inverted I control signal **10392**, and inverted Q control signal **10396**. When pulses from these control signals leak to through first, second, third, and fourth UFD modules **10302**, **10306**, **10310**, and **10314** of to antenna **10382** (shown in FIG. **103**), they may be radiated from I/Q modulation receiver **10300**, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals **10390**, **10392**, **10394**, and **10396**. FIG. **105** shows an example combined control signal **10502**.

FIG. **106** also shows an example I/Q modulation RF input signal **10382** overlaid upon control signals **10390**, **10392**, **10394**, and **10396**. As shown in FIG. **106**, pulses on I control signal **10390** overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal **10382**. Pulses on inverted I control signal **10392** overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal **10382**. Pulses on Q control signal **10394** overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal **10382**. Pulses on inverted Q control signal **10396** overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal **10382**.

As FIG. **106** further shows in this example, the frequency ratio between the combination of control signals **10390**, **10392**, **10394**, and **10396** and I/Q modulation RF input signal **10382** is 4:3. Because the frequency of the potentially re-radiated signal, combined control signal **10502**, is substantially different from that of the signal being down-converted, I/Q modulation RF input signal **10382**, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver **10300** reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant art(s) from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator **10400** will be apparent to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the present invention.

2.2.2 Detailed Example I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. **107** illustrates a more detailed example circuit implementation of I/Q modulation receiver **10300**, according to an embodiment of the present invention. FIGS. **108**–**118** show waveforms related to an example implementation of I/Q modulation receiver **10300** of FIG. **107**.

FIGS. **108** and **109** show first and second input data signals **10702** and **10704** to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. **111** and **112** show the signals of FIGS. **108** and **109** after modulation with a RF carrier signal frequency, respectively, as I-modulated signal **10706** and Q-modulated signal **10708**.

FIG. **110** shows an I/Q modulation RF input signal **10382** formed from I-modulated signal **10706** and Q-modulated signal **10708** of FIGS. **111** and **112**, respectively.

FIG. **117** shows an overlaid view of filtered I output signal **11702** and filtered inverted I output signal **11704**.

FIG. **118** shows an overlaid view of filtered Q output signal **11802** and filtered inverted Q output signal **11804**.

FIGS. **113** and **114** show I baseband output signal **10384** and Q baseband output signal **10386**, respectfully. A data transition **11002** is indicated in both I baseband output signal **10384** and Q baseband output signal **10386**. The corresponding data transition **11002** is indicated in I-modulated signal **10706** of FIG. **111**, Q-modulated signal **10708** of FIG. **112**, and I/Q modulation RF input signal **10382** of FIG. **110**.

FIGS. **115** and **116** show I baseband output signal **10384** and Q baseband output signal **10386** over a wider time interval.

2.2.3 Example Single Channel Receiver Embodiment

FIG. **119** illustrates an exemplary single channel receiver **11900**, corresponding to either the I or Q channel of I/Q modulation receiver **10300**, according to an embodiment of the present invention. Single channel receiver **11900** can down-convert an input RF signal **11906** modulated according to AM, PM, FM, and other modulation schemes. Refer to Section 2.2 above for further description on the operation of single channel receiver **11900**.

3. Frequency Up-Conversion

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system **300** is illustrated in FIG. **3**. The frequency up-conversion system **300** is now described.

An input signal **302** (designated as "Control Signal" in FIG. **3**) is accepted by a switch module **304**. For purposes of example only, assume that the input signal **302** is a FM input signal **606**, an example of which is shown in FIG. **6**C. FM input signal **606** may have been generated by modulating information signal **602** onto oscillating signal **604** (FIGS. **6**A and **6**B). It should be understood that the invention is not limited to this embodiment. The information signal **602** can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module **304** is a harmonically rich signal **306**, shown for example in FIG. **6**D as a harmonically rich signal **608**. The harmonically rich signal **608** has a continuous and periodic waveform.

FIG. **6**E is an expanded view of two sections of harmonically rich signal **608**, section **610** and section **612**. The harmonically rich signal **608** may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular wavefomm" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal **608** is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal **608**. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. **6**F and FIG. **6**G show separately the sinusoidal components making up the first, third, and fifth harmonics of section **610** and section **612**. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal **608** is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. **6**H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal **306** and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal **306**. According to an embodiment of the invention, the input signal **606** may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter **308** filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal **310**, shown for example as a filtered output signal **614** in FIG. **6**I.

FIG. **4** illustrates an example universal frequency up-conversion (UFU) module **401**. The UFU module **401** includes an example switch module **304**, which comprises a bias signal **402**, a resistor or impedance **404**, a universal frequency translator (UFT) **450**, and a ground **408**. The UFT **450** includes a switch **406**. The input signal **302** (designated as "Control Signal" in FIG. **4**) controls the switch **406** in the UFT **450**, and causes it to close and open. Harmonically rich signal **306** is generated at a node **405** located between the resistor or impedance **404** and the switch **406**.

Also in FIG. **4**, it can be seen that an example filter **308** is comprised of a capacitor **410** and an inductor **412** shunted to a ground **414**. The filter is designed to filter out the undesired harmonics of harmonically rich signal **306**.

The invention is not limited to the UFU embodiment shown in FIG. **4**.

For example, in an alternate embodiment shown in FIG. **5**, an unshaped input signal **501** is routed to a pulse shaping module **502**. The pulse shaping module **502** modifies the unshaped input signal **501** to generate a (modified) input signal **302** (designated as the "Control Signal" in FIG. **5**). The input signal **302** is routed to the switch module **304**, which operates in the manner described above. Also, the filter **308** of FIG. **5** operates in the manner described above. The purpose of the pulse shaping module **502** is to define the pulse width of the input signal **302**. Recall that the input signal **302** controls the opening and closing of the switch **406** in switch module **304**. During such operation, the pulse width of the input signal **302** establishes the pulse width of the harmonically rich signal **306**. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal **306** are a function of at least the pulse width of the harmonically rich signal **306**. As such, the pulse width of the input signal **302** contributes to setting the relative amplitudes of the harmonics of harmonically rich signal **306**.

Further details of up-conversion as described in this section are presented in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, incorporated herein by reference in its entirety.

3.1 Universal Transmitter with 2 UFT Modules

FIG. **71**A illustrates a transmitter **7102** according to embodiments of the present invention. Transmitter **7102** includes a balanced modulator/up-converter **7104**, a control signal generator **7142**, an optional filter **7106**, and an optional amplifier **7108**. Transmitter **7102** up-converts a baseband signal **7110** to produce an output signal **7140** that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator **7104** receives the baseband signal **7110** and samples the baseband signal in a differential and balanced fashion to generate a harmonically rich signal **7138**. The harmonically rich signal **7138** includes multiple harmonic images, where each image contains the baseband information in the baseband signal **7110**. The optional bandpass filter **7106** may be included to select a harmonic of interest (or a subset of harmonics) in the signal **7138** for transmission. The optional amplifier **7108** may be included to amplify the selected harmonic prior to transmission. The universal transmitter is further described at a high level by the flowchart **8400** that is shown in FIG. **84**. A more detailed structural and operational description of the balanced modulator follows thereafter.

Referring to flowchart **8400**, in step **8402**, the balanced modulator **7104** receives the baseband signal **7110**.

In step **8404**, the balanced modulator **7104** samples the baseband signal in a differential and balanced fashion according to a first and second control signals that are phase shifted with respect to each other. The resulting harmonically rich signal **7138** includes multiple harmonic images that repeat at harmonics of the sampling frequency, where each image contains the necessary amplitude and frequency information to reconstruct the baseband signal **7110**.

In embodiments of the invention, the control signals include pulses having pulse widths (or apertures) that are established to improve energy transfer to a desired harmonic of the harmonically rich signal **7138**. In further embodiments of the invention, DC offset voltages are minimized between sampling modules as indicated in step **8406**,

thereby minimizing carrier insertion in the harmonic images of the harmonically rich signal **7138**.

In step **8408**, the optional bandpass filter **7106** selects the desired harmonic of interest (or a subset of harmonics) in from the harmonically rich signal **7138** for transmission.

In step **8410**, the optional amplifier **7108** amplifies the selected harmonic(s) prior to transmission.

In step **8412**, the selected harmonic(s) is transmitted over a communications medium.

3.1.1 Balanced Modulator Detailed Description

Referring to the example embodiment shown in FIG. **71**A, the balanced modulator **7104** includes the following components: a buffer/inverter **7112**; summer amplifiers **7118**, **7119**; UFT modules **7124** and **7128** having controlled switches **7148** and **7150**, respectively; an inductor **7126**; a blocking capacitor **7136**; and a DC terminal **7111**. As stated above, the balanced modulator **7104** differentially samples the baseband signal **7110** to generate a harmonically rich signal **7138**. More specifically, the UFT modules **7124** and **7128** sample the baseband signal in differential fashion according to control signals **7123** and **7127**, respectively. A DC reference voltage **7113** is applied to terminal **7111** and is uniformly distributed to the UFT modules **7124** and **7128**. The distributed DC voltage **7113** prevents any DC offset voltages from developing between the UFT modules, which can lead to carrier insertion in the harmonically rich signal **7138**. The operation of the balanced modulator **7104** is discussed in greater detail with reference to flowchart **8500** (FIG. **85**), as follows.

In step **8402**, the buffer/inverter **7112** receives the input baseband signal **7110** and generates input signal **7114** and inverted input signal **7116**. Input signal **7114** is substantially similar to signal **7110**, and inverted signal **7116** is an inverted version of signal **7114**. As such, the buffer/inverter **7112** converts the (single-ended) baseband signal **7110** into differential input signals **7114** and **7116** that will be sampled by the UFT modules. Buffer/inverter **7112** can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step **8504**, the summer amplifier **7118** sums the DC reference voltage **7113** applied to terminal **7111** with the input signal **7114**, to generate a combined signal **7120**. Likewise, the summer amplifier **7119** sums the DC reference voltage **7113** with the inverted input signal **7116** to generate a combined signal **7122**. Summer amplifiers **7118** and **7119** can be implemented using known op amp summer circuits, and can be designed to have a specified gain or attenuation, including unity gain, although the invention is not limited to this example. The DC reference voltage **7113** is also distributed to the outputs of both UFT modules **7124** and **7128** through the inductor **7126** as is shown.

In step **8506**, the control signal generator **7142** generates control signals **7123** and **7127** that are shown by way of example in FIG. **72**B and FIG. **72**C, respectively. As illustrated, both control signals **7123** and **7127** have the same period T_S as a master clock signal **7145** (FIG. **72**A), but have a pulse width (or aperture) of T_A. In the example, control signal **7123** triggers on the rising pulse edge of the master clock signal **7145**, and control signal **7127** triggers on the falling pulse edge of the master clock signal **7145**. Therefore, control signals **7123** and **7127** are shifted in time by 180 degrees relative to each other. In embodiments of invention, the master clock signal **7145** (and therefore the control signals **7123** and **7127**) have a frequency that is a sub-harmonic of the desired output signal **7140**. The invention is not limited to the example of FIGS. **72**A–**72**C.

In one embodiment, the control signal generator **7142** includes an oscillator **7146**, pulse generators **7144***a* and **7144***b*, and an inverter **7147** as shown. In operation, the oscillator **7146** generates the master clock signal **7145**, which is illustrated in FIG. **72**A as a periodic square wave having pulses with a period of T_S. Other clock signals could be used including but not limited to sinusoidal waves, as will be understood by those skilled in the relevant art(s). Pulse generator **7144***a* receives the master clock signal **7145** and triggers on the rising pulse edge, to generate the control signal **7123**. Inverter **7147** inverts the clock signal **7145** to generate an inverted clock signal **7143**. The pulse generator **7144***b* receives the inverted clock signal **7143** and triggers on the rising pulse edge (which is the falling edge of clock signal **7145**), to generate the control signal **7127**.

FIGS. **89**A–E illustrate example embodiments for the pulse generator **7144**. FIG. **89**A illustrates a pulse generator **8902**. The pulse generator **8902** generates pulses **8908** having pulse width TA from an input signal **8904**. Example input signals **8904** and pulses **8908** are depicted in FIGS. **89**B and **89**C, respectively. The input signal **8904** can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave etc. The pulse width (or aperture) TA of the pulses **8908** is determined by delay **8906** of the pulse generator **8902**. The pulse generator **8902** also includes an optional inverter **8910**, which is optionally added for polarity considerations as understood by those skilled in the arts. The example logic and implementation shown for the pulse generator **8902** is provided for illustrative purposes only, and is not limiting. The actual logic employed can take many forms. Additional examples of pulse generation logic are shown in FIGS. **89**D and **89**E. FIG. **89**D illustrates a rising edge pulse generator **8912** that triggers on the rising edge of input signal **8904**. FIG. **89**E illustrates a falling edge pulse generator **8916** that triggers on the falling edge of the input signal **8904**.

In step **8508**, the UFT module **7124** samples the combined signal **7120** according to the control signal **7123** to generate harmonically rich signal **7130**. More specifically, the switch **7148** closes during the pulse widths T_A of the control signal **7123** to sample the combined signal **7120** resulting in the harmonically rich signal **7130**. FIG. **71**B illustrates an exemplary frequency spectrum for the harmonically rich signal **7130** having harmonic images **7152***a–n*. The images **7152** repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image **7152** contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7110**. As discussed further below, the relative amplitude of the frequency images is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic **7152** can be increased (or decreased) by adjusting the pulse width T_A of the control signal **7123**. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGS. **3**–**6**. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, and incorporated herein by reference.

In step **8510**, the UFT module **7128** samples the combined signal **7122** according to the control signal **7127** to generate

harmonically rich signal **7134**. More specifically, the switch **7150** closes during the pulse widths T_A of the control signal **7127** to sample the combined signal **7122** resulting in the harmonically rich signal **7134**. The harmonically rich signal **7134** includes multiple frequency images of baseband signal **7110** that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal **7130**. However, the images in the signal **7134** are phase-shifted compared to those in signal **7130** because of the inversion of signal **7116** compared to signal **7114**, and because of the relative phase shift between the control signals **7123** and **7127**.

In step **8512**, the node **7132** sums the harmonically rich signals **7130** and **7134** to generate harmonically rich signal **7133**. FIG. **71**C illustrates an exemplary frequency spectrum for the harmonically rich signal **7133** that has multiple images **7154***a–n* that repeat at harmonics of the sampling frequency $1/T_S$. Each image **7154** includes the necessary amplitude, frequency and phase information to reconstruct the baseband signal **7110**. The capacitor **7136** operates as a DC blocking capacitor and substantially passes the harmonics in the harmonically rich signal **7133** to generate harmonically rich signal **7138** at the output of the modulator **7104**.

In step **8408**, the optional filter **7106** can be used to select a desired harmonic image for transmission. This is represented for example by a passband **7156** that selects the harmonic image **7154***c* for transmission in FIG. **71**C.

An advantage of the modulator **7104** is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules **7124** and **7128**. DC offset is minimized because the reference voltage **7113** contributes a consistent DC component to the input signals **7120** and **7122** through the summing amplifiers **7118** and **7119**, respectively. Furthermore, the reference voltage **7113** is also directly coupled to the outputs of the UFT modules **7124** and **7128** through the inductor **7126** and the node **7132**. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal **7138**. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

3.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description

In order to further describe the invention, FIGS. **72**D–**72**I illustrate various example signal diagrams (vs. time) that are representative of the invention. These signal diagrams are meant for example purposes only and are not meant to be limiting. FIG. **72**D illustrates a signal **7202** that is representative of the input baseband signal **7110** (FIG. **71**A). FIG. **72**E illustrates a step function **7204** that is an expanded portion of the signal **7202** from time t_0 to t_1, and represents signal **7114** at the output of the buffer/inverter **7112**. Similarly, FIG. **72**F illustrates a signal **7206** that is an inverted version of the signal **7204**, and represents the signal **7116** at the inverted output of buffer/inverter **7112**. For analysis purposes, a step function is a good approximation for a portion of a single bit of data (for the baseband signal **7110**) because the clock rates of the control signals **7123** and **7127** are significantly higher than the data rates of the baseband signal **7110**. For example, if the data rate is in the KHz frequency range, then the clock rate will preferably be in MHZ frequency range in order to generate an output signal in the GHz frequency range.

Still referring to FIGS. **72**D–I, FIG. **72**G illustrates a signal **7208** that an example of the harmonically rich signal **7130** when the step function **7204** is sampled according to the control signal **7123** in FIG. **72**B. The signal **7208** includes positive pulses **7209** as referenced to the DC voltage **7113**. Likewise, FIG. **72**H illustrates a signal **7210** that is an example of the harmonically rich signal **7134** when the step function **7206** is sampled according to the control signal **7127**. The signal **7210** includes negative pulses **7211** as referenced to the DC voltage **7113**, which are time-shifted relative to positive pulses **7209** in signal **7208**.

Still referring to FIGS. **72**D–I, the FIG. **721** illustrates a signal **7212** that is the combination of signal **7208** (FIG. **72**G) and the signal **7210** (FIG. **72**H), and is an example of the harmonically rich signal **7133** at the output of the summing node **7132**. As illustrated, the signal **7212** spends approximately as much time above the DC reference voltage **7113** as below the DC reference voltage **7113** over a limited time period. For example, over a time period **7214**, the energy in the positive pulses **7209***a–b* is canceled out by the energy in the negative pulses **7211***a–b*. This is indicative of minimal (or zero) DC offset between the UFT modules **7124** and **7128**, which results in minimal carrier insertion during the sampling process.

Still referring to FIG. **721**, the time axis of the signal **7212** can be phased in such a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is readily calculated to obtain:

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4 \sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right). \quad \text{Equation 1}$$

where:

T_S=period of the master clock **7145**

T_A=pulse width of the control signals **7123** and **7127**

n=harmonic number

As shown by Equation 1, the relative amplitude of the frequency images is generally a function of the harmonic number n, and the ratio of T_A/T_S. As indicated, the T_A/T_S ratio represents the ratio of the pulse width of the control signals relative to the period of the sub-harmonic master clock. The T_A/T_S ratio can be optimized in order to maximize the amplitude of the frequency image at a given harmonic. For example, if a passband waveform is desired to be created at 5× the frequency of the sub-harmonic clock, then a baseline power for that harmonic extraction may be calculated for the fifth harmonic (n=5) as:

$$I_c(t) = \left(\frac{4 \sin\left(\frac{5\pi T_A}{T_s}\right)}{5\pi} \right) \cdot \sin(5\omega_s t). \quad \text{Equation 2}$$

As shown by Equation 2, $I_C(t)$ for the harmonic is a sinusoidal function having an amplitude that is proportional to the sin ($5\pi T_A/T_S$). The signal amplitude can be maximized by setting $T_A=(1/10 \cdot T_S)$ so that sin ($5\pi T_A/T_S$)=sin ($\pi/2$)=1. Doing so results in the equation:

$$I_c(t)|_{n=5} = \frac{4}{5\pi}(\sin(5\omega_s t)). \quad \text{Equation 3}$$

This component is a frequency at 5× of the sampling frequency of sub-harmonic clock, and can be extracted from the Fourier series via a bandpass filter (such as bandpass filter **7106**) that is centered around $5f_s$. The extracted frequency component can then be optionally amplified by the amplifier **7108** prior to transmission on a wireless or wireline communications channel or channels.

Equation 3 can be extended to reflect the inclusion of a message signal as illustrated by equation 4 below:

$$m(t)\cdot I_c(t)|_{\substack{n=5\\ \theta=\theta(t)}} = \frac{4\cdot m(t)}{5\pi}(\sin(5\omega_s t + 5\theta(t))). \quad \text{Equation 4}$$

Equation 4 illustrates that a message signal can be carried in harmonically rich signals **7133** such that both amplitude and phase can be modulated. In other words, m(t) is modulated for amplitude and θ(t) is modulated for phase. In such cases, it should be noted that θ(t) is augmented modulo n while the amplitude modulation m(t) is simply scaled. Therefore, complex waveforms may be reconstructed from their Fourier series with multiple aperture UFT combinations.

As discussed above, the signal amplitude for the 5th harmonic was maximized by setting the sampling aperture width T_A=1/10 T_S, where T_S is the period of the master clock signal. This can be restated and generalized as setting T_A=½ the period (or π radians) at the harmonic of interest. In other words, the signal amplitude of any harmonic n can be maximized by sampling the input waveform with a sampling aperture of T_A=½ the period of the harmonic of interest (n). Based on this discussion, it is apparent that varying the aperture changes the harmonic and amplitude content of the output waveform. For example, if the sub-harmonic clock has a frequency of 200 MHZ, then the fifth harmonic is at 1 Ghz. The amplitude of the fifth harmonic is maximized by setting the aperture width T_A=500 picoseconds, which equates to ½ the period (or π radians) at 1 Ghz.

FIG. **72**J depicts a frequency plot **7216** that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal **7133** given a 200 MHZ harmonic clock. The frequency plot **7216** compares two frequency spectrums **7218** and **7220** for different control signal apertures given a 200 MHZ clock. More specifically, the frequency spectrum **7218** is an example spectrum for signal **7133** given the 200 MHZ clock with the aperture T_A=500 psec (where 500 psec is π radians at the 5th harmonic of 1 GHz). Similarly, the frequency spectrum **7220** is an example spectrum for signal **7133** given a 200 MHZ clock that is a square wave (so T_A=5000 psec). The spectrum **7218** includes multiple harmonics **7218***a–i*, and the frequency spectrum **7220** includes multiple harmonics **7220***a–e*. [It is noted that spectrum **7220** includes only the odd harmonics as predicted by Fourier analysis for a square wave.] At 1 Ghz (which is the 5th harmonic), the signal amplitude of the two frequency spectrums **7218***e* and **7220***c* are approximately equal. However, at 200 MHZ, the frequency spectrum **7218***a* has a much lower amplitude than the frequency spectrum **7220***a*, and therefore the frequency spectrum **7218** is more efficient than the frequency spectrum **7220**, assuming the desired harmonic is the 5th harmonic. In other words, assuming 1 GHz is the desired harmonic, the frequency spectrum **7218** wastes less energy at the 200 MHZ fundamental than does the frequency spectrum **7218**.

3.1.3 Balanced Modulator Having a Shunt Configuration

FIG. **79**A illustrates a universal transmitter **7900** that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration. (In contrast, the balanced modulator **7104** can be described as having a series configuration based on the orientation of the UFT modules.) Transmitter **7900** includes a balanced modulator **7901**, the control signal generator **7142**, the optional bandpass filter **7106**, and the optional amplifier **7108**. The transmitter **7900** up-converts a baseband signal **7902** to produce an output signal **7936** that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator **7901** receives the baseband signal **7902** and shunts the baseband signal to ground in a differential and balanced fashion to generate a harmonically rich signal **7934**. The harmonically rich signal **7934** includes multiple harmonic images, where each image contains the baseband information in the baseband signal **7902**. In other words, each harmonic image includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7902**. The optional bandpass filter **7106** may be included to select a harmonic of interest (or a subset of harmonics) in the signal **7934** for transmission. The optional amplifier **7108** may be included to amplify the selected harmonic prior to transmission, resulting in the output signal **7936**.

The balanced modulator **7901** includes the following components: a buffer/inverter **7904**; optional impedances **7910**, **7912**; UFT modules **7916** and **7922** having controlled switches **7918** and **7924**, respectively; blocking capacitors **7928** and **7930**; and a terminal **7920** that is tied to ground. As stated above, the balanced modulator **7901** differentially shunts the baseband signal **7902** to ground, resulting in a harmonically rich signal **7934**. More specifically, the UFT modules **7916** and **7922** alternately shunts the baseband signal to terminal **7920** according to control signals **7123** and **7127**, respectively. Terminal **7920** is tied to ground and prevents any DC offset voltages from developing between the UFT modules **7916** and **7922**. As described above, a DC offset voltage can lead to undesired carrier insertion. The operation of the balanced modulator **7901** is described in greater detail according to the flowchart **8600** (FIG. **86**) as follows.

In step **8402**, the buffer/inverter **7904** receives the input baseband signal **7902** and generates I signal **7906** and inverted I signal **7908**. I signal **7906** is substantially similar to the baseband signal **7902**, and the inverted I signal **7908** is an inverted version of signal **7902**. As such, the buffer/inverter **7904** converts the (single-ended) baseband signal **7902** into differential signals **7906** and **7908** that are sampled by the UFT modules. Buffer/inverter **7904** can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step **8604**, the control signal generator **7142** generates control signals **7123** and **7127** from the master clock signal **7145**. Examples of the master clock signal **7145**, control signal **7123**, and control signal **7127** are shown in FIGS. **72**A–C, respectively. As illustrated, both control signals **7123** and **7127** have the same period T_S as a master clock signal **7145**, but have a pulse width (or aperture) of TA. Control signal **7123** triggers on the rising pulse edge of the master clock signal **7145**, and control signal **7127** triggers on the falling pulse edge of the master clock signal **7145**.

Therefore, control signals **7123** and **7127** are shifted in time by 180 degrees relative to each other. A specific embodiment of the control signal generator **7142** is illustrated in FIG. **71**A, and was discussed in detail above.

In step **8606**, the UFT module **7916** shunts the signal **7906** to ground according to the control signal **7123**, to generate a harmonically rich signal **7914**. More specifically, the switch **7918** closes and shorts the signal **7906** to ground (at terminal **7920**) during the aperture width TA of the control signal **7123**, to generate the harmonically rich signal **7914**. FIG. **79**B illustrates an exemplary frequency spectrum for the harmonically rich signal **7918** having harmonic images **7950***a–n*. The images **7950** repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image **7950** contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7902**. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGS. **3–6**. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, and incorporated herein by reference.

The relative amplitude of the frequency images **7950** are generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic **7950** can be increased (or decreased) by adjusting the pulse width T_A of the control signal **7123**. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics, as described by equations 1–4 above. Additionally, the relative amplitude of a particular harmonic **7950** can also be adjusted by adding/tuning an optional impedance **7910**. Impedance **7910** operates as a filter that emphasizes a particular harmonic in the harmonically rich signal **7914**.

In step **8608**, the UFT module **7922** shunts the inverted signal **7908** to ground according to the control signal **7127**, to generate a harmonically rich signal **7926**. More specifically, the switch **7924** closes during the pulse widths T_A and shorts the inverted I signal **7908** to ground (at terminal **7920**), to generate the harmonically rich signal **7926**. At any given time, only one of input signals **7906** or **7908** is shorted to ground because the pulses in the control signals **7123** and **7127** are phase shifted with respect to each other, as shown in FIGS. **72**B and **72**C.

The harmonically rich signal **7926** includes multiple frequency images of baseband signal **7902** that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal **7914**. However, the images in the signal **7926** are phase-shifted compared to those in signal **7914** because of the inversion of the signal **7908** compared to the signal **7906**, and because of the relative phase shift between the control signals **7123** and **7127**. The optional impedance **7912** can be included to emphasis a particular harmonic of interest, and is similar to the impedance **7910** above.

In step **8610**, the node **7932** sums the harmonically rich signals **7914** and **7926** to generate the harmonically rich signal **7934**. The capacitors **7928** and **7930** operate as blocking capacitors that substantially pass the respective harmonically rich signals **7914** and **7926** to the node **7932**. (The capacitor values may be chosen to substantially block baseband frequency components as well.) FIG. **79**C illustrates an exemplary frequency spectrum for the harmonically rich signal **7934** that has multiple images **7952***a–n* that repeat at harmonics of the sampling frequency $1/T_S$. Each image **7952** includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal **7902**. The optional filter **7106** can be used to select the harmonic image of interest for transmission. This is represented by a passband **7956** that selects the harmonic image **7932***c* for transmission.

An advantage of the modulator **7901** is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules **7912** and **7914**. DC offset is minimized because the UFT modules **7916** and **7922** are both connected to ground at terminal **7920**. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal **7934**. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

3.1.4 Balanced Modulator FET Configuration

As described above, the balanced modulators **7104** and **7901** utilize two balanced UFT modules to sample the input baseband signals to generate harmonically rich signals that contain the up-converted baseband information. More specifically, the UFT modules include controlled switches that sample the baseband signal in a balanced and differential fashion. FIGS. **71**D and **79**D illustrate embodiments of the controlled switch in the UFT module.

FIG. **71**D illustrates an example transmitter **7162**, according to an embodiment of the present invention. Transmitter **7162** comprises modulator **7104** (FIG. **71**B) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches **7148** and **7128** are embodied as FET **7158** and FET **7160**, respectively. The FET **7158** and **7160** are oriented so that their gates are controlled by the control signals **7123** and **7127**, so that the control signals control the FET conductance. For the FET **7158**, the combined baseband signal **7120** is received at the source of the FET **7158** and is sampled according to the control signal **7123** to produce the harmonically rich signal **7130** at the drain of the FET **7158**. Likewise, the combined baseband signal **7122** is received at the source of the FET **7160** and is sampled according to the control signal **7127** to produce the harmonically rich signal **7134** at the drain of FET **7160**. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs. In other words, the combined baseband signal can be received at the drain of the FETs, and the harmonically rich signals can be taken from the source of the FETs, as will be understood by those skilled in the relevant arts.

FIG. **79**D illustrates an embodiment of the modulator **7900** (FIG. **79**A) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches **7918** and **7924** are embodied as FET **7936** and FET **7938**, respectively. The FETs **7936** and **7938** are oriented so that their gates are controlled by the control signals **7123** and **7127**, respectively, so that the control signals determine FET conductance. For the FET **7936**, the baseband signal **7906** is received at the source of the FET **7936** and shunted to ground according to the control signal **7123**, to produce the harmonically rich signal **7914**. Likewise, the baseband signal **7908** is received at the source of

the FET **7938** and is shunted to grounding according to the control signal **7127**, to produce the harmonically rich signal **7926**. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs, as will be understood by those skilled in the relevant arts.

3.1.5 Universal Transmitter Configured for Carrier Insertion

As discussed above, the transmitters **7102** and **7900** have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the output signal **7140**. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, the present invention can be configured to provide the necessary carrier insertion by implementing a DC offset between the two sampling UFT modules.

FIG. **73**A illustrates a transmitter **7302** that up-converts a baseband signal **7306** to an output signal **7322** having carrier insertion. As is shown, the transmitter **7302** is similar to the transmitter **7102** (FIG. **71**A) with the exception that the up-converter/modulator **7304** is configured to accept two DC references voltages. In contrast, modulator **7104** was configured to accept only one DC reference voltage. More specifically, the modulator **7304** includes a terminal **7309** to accept a DC reference voltage **7308**, and a terminal **7313** to accept a DC reference voltage **7314**. Vr **7308** appears at the UFT module **7124** though summer amplifier **7118** and the inductor **7310**. Vr **7314** appears at UFT module **7128** through the summer amplifier **7119** and the inductor **7316**. Capacitors **7312** and **7318** operate as blocking capacitors. If Vr **7308** is different from Vr **7314** then a DC offset voltage will be exist between UFT module **7124** and UFT module **7128**, which will be up-converted at the carrier frequency in the harmonically rich signal **7320**. More specifically, each harmonic image in the harmonically rich signal **7320** will include a carrier signal as depicted in FIG. **73**B.

FIG. **73**B illustrates an exemplary frequency spectrum for the harmonically rich signal **7320** that has multiple harmonic images **7324***a–n*. In addition to carrying the baseband information in the sidebands, each harmonic image **7324** also includes a carrier signal **7326** that exists at respective harmonic of the sampling frequency $1/T_S$. The amplitude of the carrier signal increases with increasing DC offset voltage. Therefore, as the difference between Vr **7308** and Vr **7314** widens, the amplitude of each carrier signal **7326** increases. Likewise, as the difference between Vr **7308** and Vr **7314** shrinks, the amplitude of each carrier signal **7326** shrinks. As with transmitter **7302**, the optional bandpass filter **7106** can be included to select a desired harmonic image for transmission. This is represented by passband **7328** in FIG. **73**B.

3.2 Universal Transmitter In I/Q Configuration:

As described above, the balanced modulators **7104** and **7901** up-convert a baseband signal to a harmonically rich signal having multiple harmonic images of the baseband information. By combining two balanced modulators, I/Q configurations can be formed for up-converting I and Q baseband signals. In doing so, either the (series type) balanced modulator **7104** or the (shunt type) balanced modulator can be utilized. I/Q modulators having both series and shunt configurations are described below.

3.2.1 IQ Transmitter Using Series-Type Balanced Modulator

FIG. **74** illustrates an I/Q transmitter **7420** with an in-phase (I) and quadrature (O) configuration according to embodiments of the invention. The transmitter **7420** includes an I/Q balanced modulator **7410**, an optional filter **7414**, and an optional amplifier **7416**. The transmitter **7420** is useful for transmitting complex I Q waveforms and does so in a balanced manner to control DC offset and carrier insertion. In doing so, the modulator **7410** receives an I baseband signal **7402** and a Q baseband signal **7404** and up-converts these signals to generate a combined harmonically rich signal **7412**. The harmonically rich signal **7412** includes multiple harmonics images, where each image contains the baseband information in the I signal **7402** and the Q signal **7404**. The optional bandpass filter **7414** may be included to select a harmonic of interest (or subset of harmonics) from the signal **7412** for transmission. The optional amplifier **7416** may be included to amplify the selected harmonic prior to transmission, to generate the I/Q output signal **7418**.

As stated above, the balanced I/Q modulator **7410** up-converts the I baseband signal **7402** and the Q baseband signal **7404** in a balanced manner to generate the combined harmonically rich signal **7412** that carriers the I and Q baseband information. To do so, in an embodiment, the modulator **7410** utilizes two balanced modulators **7104** from FIG. **71**A, a signal combiner **7408**, and a DC terminal **7407**. The operation of the balanced modulator **7410** and other circuits in the transmitter is described according to the flowchart **8700** in FIG. **87**, as follows. It is again noted that the ordering of steps in flowcharts is flexible, and not limited to the particular embodiments discussed herein.

In step **8702**, the I/Q modulator **7410** receives the I baseband signal **7402** and the Q baseband signal **7404**.

In step **8704**, the I balanced modulator **7104***a* samples the I baseband signal **7402** in a differential fashion using the control signals **7123** and **7127** to generate a harmonically rich signal **7411***a*. The harmonically rich signal **7411***a* contains multiple harmonic images of the I baseband information, similar to the harmonically rich signal **7130** in FIG. **711**B.

In step **8706**, the balanced modulator **7104***b* samples the Q baseband signal **7404** in a differential fashion using control signals **7123** and **7127** to generate harmonically rich signal **7411***b*, where the harmonically rich signal **7411***b* contains multiple harmonic images of the Q baseband signal **7404**. The operation of the balanced modulator **7104** and the generation of harmonically rich signals was fully described above and illustrated in FIGS. **71**A–C, to which the reader is referred for further details.

In step **8708**, the DC terminal **7407** receives a DC voltage **7406** that is distributed to both modulators **7104***a* and **7104***b*. The DC voltage **7406** is distributed to both the input and output of both UFT modules **7124** and **7128** in each modulator **7104**. This minimizes (or prevents) DC offset voltages from developing between the four UFT modules, and thereby minimizes or prevents any carrier insertion during the sampling steps **8704** and **8706**.

In step **8710**, the 90 degree signal combiner **7408** combines the harmonically rich signals **7411***a* and **7411***b* to generate I/Q harmonically rich signal **7412**. This is further illustrated in FIGS. **75**A–C. FIG. **75**A depicts an exemplary frequency spectrum for the harmonically rich signal **7411***a* having harmonic images **7502***a–n*. The images **7502** repeat at harmonics of the sampling frequency $1/T_S$, where each image **7502** contains the necessary amplitude and frequency

information to reconstruct the I baseband signal **7402**. Likewise, FIG. **75**B depicts an exemplary frequency spectrum for the harmonically rich signal **7411***b* having harmonic images **7504***a–n*. The harmonic images **7504***a–n* also repeat at harmonics of the sampling frequency $1/T_S$, where each image **7504** contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal **7404**. FIG. **75**C illustrates an exemplary frequency spectrum for the combined harmonically rich signal **7412** having images **7506**. Each image **7506** carries the I baseband information and the Q baseband information from the corresponding images **7502** and **7504**, respectively, without substantially increasing the frequency bandwidth occupied by each harmonic **7506**. This can occur because the signal combiner **7408** phase shifts the Q signal **7411***b* by 90 degrees relative to the I signal **7411***a*. The result is that the images **7502***a–n* and **7504***a–n* effectively share the signal bandwidth do to their orthogonal relationship. For example, the images **7502***a* and **7504***a* effectively share the frequency spectrum that is represented by the image **7506***a*.

In step **8712**, the optional filter **7414** can be included to select a harmonic of interest, as represented by the passband **7508** selecting the image **7506***c* in FIG. **75***c*.

In step **8714**, the optional amplifier **7416** can be included to amplify the harmonic (or harmonics) of interest prior to transmission.

In step **8716**, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. **76**A illustrates a transmitter **7608** that is a second embodiment for an I Q transmitter having a balanced configuration. Transmitter **7608** is similar to the transmitter **7420** except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays **7604***a* and **7604***b* delay the control signals **7123** and **7127** for the Q channel modulator **7104***b* by 90 degrees relative the control signals for the I channel modulator **7104***a*. As a result, the Q modulator **7104***b* samples the Q baseband signal **7404** with 90 degree delay relative to the sampling of the I baseband signal **7402** by the I channel modulator **7104***a*. Therefore, the Q harmonically rich signal **7411***b* is phase shifted by 90 degrees relative to the I harmonically rich signal. Since the phase shift is achieved using the control signals, an in-phase signal combiner **7606** combines the harmonically rich signals **7411***a* and **7411***b*, to generate the harmonically rich signal **7412**. It is noted that other embodiments may employ phase shifts other than 90 degrees.

FIG. **76**B illustrates a transmitter **7618** that is similar to transmitter **7608** in FIG. **76**A. The difference being that the transmitter **7618** has a modulator **7620** that utilizes a summing node **7622** to sum the signals **7411***a* and **7411***b* instead of the in-phase signal combiner **7606** that is used in modulator **7602** of transmitter **7608**.

3.2.2. I/Q Transmitter Using Shunt-Type Balanced Modulator

FIG. **80** illustrates an I/Q transmitter **8000** that is another I/Q transmitter embodiment according to the present invention. The transmitter **8000** includes an I/Q balanced modulator **8001**, an optional filter **8012**, and an optional amplifier **8014**. During operation, the modulator **8001** up-converts an I baseband signal **8002** and a Q baseband signal **8004** to generate a combined harmonically rich signal **8011**. The harmonically rich signal **8011** includes multiple harmonics images, where each image contains the baseband information in the I signal **8002** and the Q signal **8004**. The optional bandpass filter **8012** may be included to select a harmonic of interest (or subset of harmonics) from the harmonically rich signal **8011** for transmission. The optional amplifier **8014** may be included to amplify the selected harmonic prior to transmission, to generate the I/Q output signal **8016**.

The I/Q modulator **8001** includes two balanced modulators **7901** from FIG. **79**A, and a 90 degree signal combiner **8010** as shown. The operation of the I/Q modulator **8001** is described in reference to the flowchart **8800** (FIG. **88**), as follows. The order of the steps in flowchart **8800** is not limiting.

In step **8802**, the balanced modulator **8001** receives the I baseband signal **8002** and the Q baseband signal **8004**.

In step **8804**, the balanced modulator **7901***a* differentially shunts the I baseband signal **8002** to ground according the control signals **7123** and **7127**, to generate a harmonically rich signal **8006**. More specifically, the UFT modules **7916***a* and **7922***a* alternately shunt the I baseband signal and an inverted version of the I baseband signal to ground according to the control signals **7123** and **7127**, respectively. The operation of the balanced modulator **7901** and the generation of harmonically rich signals was fully described above and is illustrated in FIGS. **79**A–C, to which the reader is referred for further details. As such, the harmonically rich signal **8006** contains multiple harmonic images of the I baseband information as described above.

In step **8806**, the balanced modulator **7901***b* differentially shunts the Q baseband signal **8004** to ground according to control signals **7123** and **7127**, to generate harmonically rich signal **8008**. More specifically, the UFT modules **7916***b* and **7922***b* alternately shunt the Q baseband signal and an inverted version of the Q baseband signal to ground, according to the control signals **7123** and **7127**, respectively. As such, the harmonically rich signal **8008** contains multiple harmonic images that contain the Q baseband information.

In step **8808**, the 90 degree signal combiner **8010** combines the harmonically rich signals **8006** and **8008** to generate I/Q harmonically rich signal **8011**. This is further illustrated in FIGS. **81**A–C. FIG. **81**A depicts an exemplary frequency spectrum for the harmonically rich signal **8006** having harmonic images **8102***a–n*. The harmonic images **8102** repeat at harmonics of the sampling frequency $1/T_S$, where each image **8102** contains the necessary amplitude, frequency, and phase information to reconstruct the I baseband signal **8002**. Likewise, FIG. **81**B depicts an exemplary frequency spectrum for the harmonically rich signal **8008** having harmonic images **8104***a–n*. The harmonic images **8104***a–n* also repeat at harmonics of the sampling frequency $1/T_S$, where each image **8104** contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal **8004**. FIG. **81**C illustrates an exemplary frequency spectrum for the I/Q harmonically rich signal **8011** having images **8106***a–n*. Each image **8106** carries the I baseband information and the Q baseband information from the corresponding images **8102** and **8104**, respectively, without substantially increasing the frequency bandwidth occupied by each image **8106**. This can occur because the signal combiner **8010** phase shifts the Q signal **8008** by 90 degrees relative to the I signal **8006**.

In step **8810**, the optional filter **8012** may be included to select a harmonic of interest, as represented by the passband **8108** selecting the image **8106***c* in FIG. **81**C.

In step **8812**, the optional amplifier **8014** can be included to amplify the selected harmonic image **8106** prior to transmission.

In step **8814**, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. **82** illustrates a transmitter **8200** that is another embodiment for an I Q transmitter having a balanced configuration. Transmitter **8200** is similar to the transmitter **8000** except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays **8204***a* and **8204***b* delay the control signals **7123** and **7127** for the Q channel modulator **7901***b* by 90 degrees relative the control signals for the I channel modulator **7901***a*. As a result, the Q modulator **7901***b* samples the Q baseband signal **8004** with a 90 degree delay relative to the sampling of the I baseband signal **8002** by the I channel modulator **7901***a*. Therefore, the Q harmonically rich signal **8008** is phase shifted by 90 degrees relative to the I harmonically rich signal **8006**. Since the phase shift is achieved using the control signals, an in-phase signal combiner **8206** combines the harmonically rich signals **8006** and **8008**, to generate the harmonically rich signal **8011**.

FIG. **83** illustrates a transmitter **8300** that is similar to transmitter **8200** in FIG. **82**. The difference being that the transmitter **8300** has a balanced modulator **8302** that utilizes a summing node **8304** to sum the I harmonically rich signal **8006** and the Q harmonically rich signal **8008** instead of the in-phase signal combiner **8206** that is used in the modulator **8202** of transmitter **8200**. The 90 degree phase shift between the I and Q channels is implemented by delaying the Q clock signals using 90 degree delays **8204**, as shown.

3.2.3 I/Q Transmitters Configured for Carrier Insertion

The transmitters **7420** (FIG. **74**) and **7608** (FIG. **76**A) have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the I/Q output signal **7418**. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, FIG. **77** illustrates a transmitter **7702** to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules.

Transmitter **7702** is similar to the transmitter **7420** with the exception that a modulator **7704** in transmitter **7702** is configured to accept two DC reference voltages so that the I channel modulator **7104***a* can be biased separately from the Q channel modulator **7104***b*. More specifically, modulator **7704** includes a terminal **7706** to accept a DC voltage reference **7707**, and a terminal **7708** to accept a DC voltage reference **7709**. Voltage **7707** biases the UFT modules **7124***a* and **7128***a* in the I channel modulator **7104***a*. Likewise, voltage **7709** biases the UFT modules **7124***b* and **7128***b* in the Q channel modulator **7104***b*. When voltage **7707** is different from voltage **7709**, then a DC offset will appear between the I channel modulator **7104***a* and the Q channel modulator **7104***b*, which results in carrier insertion in the I/Q harmonically rich signal **7412**. The relative amplitude of the carrier frequency energy increases in proportion to the amount of DC offset.

FIG. **78** illustrates a transmitter **7802** that is a second embodiment of an I/Q transmitter having two DC terminals to cause DC offset, and therefore carrier insertion. Transmitter **7802** is similar to transmitter **7702** except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals, similar to that done in transmitter **7608**. More specifically, delays **7804***a* and **7804***b* phase shift the control signals **7123** and **7127** for the Q channel modulator **7104***b* relative to those of the I channel modulator **7104***a*. As a result, the Q modulator **7104***b* samples the Q baseband signal **7404** with 90 degree delay relative to the sampling of the I baseband signal **7402** by the I channel modulator **7104***a*. Therefore, the Q harmonically rich signal **7411***b* is phase shifted by 90 degrees relative to the I harmonically rich signal, which is then combined by the in-phase combiner **7806**.

4. Enhanced Signal Reception

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. **21**, transmitter **2104** accepts a modulating baseband signal **2102** and generates (transmitted) redundant spectrums **2106***a–n*, which are sent over communications medium **2108**. Receiver **2112** recovers a demodulated baseband signal **2114** from (received) redundant spectrums **2110***a–n*. Demodulated baseband signal **2114** is representative of the modulating baseband signal **2102**, where the level of similarity between the modulating baseband signal **2114** and the modulating baseband signal **2102** is application dependent.

Modulating baseband signal **2102** is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal **2202** is illustrated in FIG. **22**A, and has an associated modulating baseband spectrum **2204** and image spectrum **2203** that are illustrated in FIG. **22**B. Modulating baseband signal **2202** is illustrated as an analog signal in FIG. **22***a*, but could also be a digital signal, or combination thereof. Modulating baseband signal **2202** could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum **2106***a–n* contains the necessary information to substantially reconstruct the modulating baseband signal **2102**. In other words, each redundant spectrum **2106***a–n* contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal **2102**.

FIG. **22**C illustrates example transmitted redundant spectrums **2206***b–d*. Transmitted redundant spectrums **2206***b–d* are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums **2206***b–d* are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. **22**D illustrates an alternate embodiment, where redundant spectrums **2208***c,d* are centered on unmodulated oscillating signal **2209** at f_1 (Hz). Oscillating signal **2209** may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break **2205** in the frequency axis of FIGS. **22**C and **22**D.

Received redundant spectrums **2110***a–n* are substantially similar to transmitted redundant spectrums **2106***a–n*, except for the changes introduced by the communications medium **2108**. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. **22**E illustrates example received redundant spectrums **2210***b–d*. Received redundant spectrums **2210***b–d* are substantially similar to transmitted redundant spectrums **2206***b–d*, except that redundant spectrum **2210***c* includes an undesired jamming signal spectrum **2211** in order to illustrate some advantages of the present invention. Jamming signal spectrum **2211** is a

frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum **2211**, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal **2114** is extracted from one or more of received redundant spectrums **2210***b–d*. FIG. **22**F illustrates example demodulated baseband signal **2212** that is, in this example, substantially similar to modulating baseband signal **2202** (FIG. **22**A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal **2202** can be accomplished by receiver **2112** in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum **2211**) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter **2104** will now be explored in greater detail. FIG. **23**A illustrates transmitter **2301**, which is one embodiment of transmitter **2104** that generates redundant spectrums configured similar to redundant spectrums **2206***b–d*. Transmitter **2301** includes generator **2303**, optional spectrum processing module **2304**, and optional medium interface module **2320**. Generator **2303** includes: first oscillator **2302**, second oscillator **2309**, first stage modulator **2306**, and second stage modulator **2310**.

Transmitter **2301** operates as follows. First oscillator **2302** and second oscillator **2309** generate a first oscillating signal **2305** and second oscillating signal **2312**, respectively. First stage modulator **2306** modulates first oscillating signal **2305** with modulating baseband signal **2202**, resulting in modulated signal **2308**. First stage modulator **2306** may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator **2310** modulates modulated signal **2308** with second oscillating signal **2312**, resulting in multiple redundant spectrums **2206***a–n* shown in FIG. **23**B. Second stage modulator **2310** is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum **2206***a–n* contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal **2202**.

Redundant spectrums **2206***a–n* are substantially centered around f_1, which is the characteristic frequency of first oscillating signal **2305**. Also, each redundant spectrum **2206***a–n* (except for **2206***c*) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal **2312**. Thus, each redundant spectrum **2206***a–n* is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator **2309**. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums **2206***a–n*.

In one embodiment, the number of redundant spectrums **2206***a–n* generated by transmitter **2301** is arbitrary and may be unlimited as indicated by the "a–n" designation for redundant spectrums **2206***a–n*. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter **2301** will include an optional spectrum processing module **2304** to process the redundant spectrums **2206***a–n* prior to transmission over communications medium **2108**.

In one embodiment, spectrum processing module **2304** includes a filter with a passband **2207** (FIG. **23**C) to select redundant spectrums **2206***b–d* for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband **2207**. In one embodiment, spectrum processing module **2304** also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium **2108**. Finally, medium interface module **2320** transmits redundant spectrums over the communications medium **2108**. In one embodiment, communications medium **2108** is an over-the-air link and medium interface module **2320** is an antenna. Other embodiments for communications medium **2108** and medium interface module **2320** will be understood based on the teachings contained herein.

FIG. **23**D illustrates transmitter **2321**, which is one embodiment of transmitter **2104** that generates redundant spectrums configured similar to redundant spectrums **2208***c–d* and unmodulated spectrum **2209**. Transmitter **2321** includes generator **2311**, spectrum processing module **2304**, and (optional) medium interface module **2320**. Generator **2311** includes: first oscillator **2302**, second oscillator **2309**, first stage modulator **2306**, and second stage modulator **2310**.

As shown in FIG. **23**D, many of the components in transmitter **2321** are similar to those in transmitter **2301**. However, in this embodiment, modulating baseband signal **2202** modulates second oscillating signal **2312**. Transmitter **2321** operates as follows. First stage modulator **2306** modulates second oscillating signal **2312** with modulating baseband signal **2202**, resulting in modulated signal **2322**. As described earlier, first stage modulator **2306** can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator **2310** modulates first oscillating signal **2304** with modulated signal **2322**, resulting in redundant spectrums **2208***a–n*, as shown in FIG. **23**E. Second stage modulator **2310** is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums **2208***a–n* are centered on unmodulated spectrum **2209** (at f, Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums **2208***a–n* generated by generator **2311** is arbitrary and unlimited, similar to spectrums **2206***a–n* discussed above. Therefore, optional spectrum processing module **2304** may also include a filter with passband **2325** to select, for example, spectrums **2208***c,d* for transmission over communications medium **2108**. In addition, optional spectrum processing module **2304** may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum **2209**. Alterna-

tively, unmodulated spectrum **2209** may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module **2320** transmits redundant spectrums **2208***c,d* over communications medium **2108**.

Receiver **2112** will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. **24**A illustrates receiver **2430**, which is one embodiment of receiver **2112**. Receiver **2430** includes optional medium interface module **2402**, down-converter **2404**, spectrum isolation module **2408**, and data extraction module **2414**. Spectrum isolation module **2408** includes filters **2410***a–c*. Data extraction module **2414** includes demodulators **2416***a–c*, error check modules **2420***a–c*, and arbitration module **2424**. Receiver **2430** will be discussed in relation to the signal diagrams in FIGS. **24**B–**24**J.

In one embodiment, optional medium interface module **2402** receives redundant spectrums **2210***b–d* (FIG. **22**E, and FIG. **24**B). Each redundant spectrum **2210***b–d* includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum **2210***c* also contains jamming signal **2211**, which may interfere with the recovery of a baseband signal from spectrum **2210***c*. Down-converter **2404** down-converts received redundant spectrums **2210***b–d* to lower intermediate frequencies, resulting in redundant spectrums **2406***a–c* (FIG. **24**C). Jamming signal **2211** is also down-converted to jamming signal **2407**, as it is contained within redundant spectrum **2406***b*. Spectrum isolation module **2408** includes filters **2410***a–c* that isolate redundant spectrums **2406***a–c* from each other (FIGS. **24**D–**24**F, respectively). Demodulators **2416***a–c* independently demodulate spectrums **2406***a–c*, resulting in demodulated baseband signals **2418***a–c*, respectively (FIGS. **24**G-**241**). Error check modules **2420***a–c* analyze demodulate baseband signal **2418***a–c* to detect any errors. In one embodiment, each error check module **2420***a–c* sets an error flag **2422***a–c* whenever an error is detected in a demodulated baseband signal. Arbitration module **2424** accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. **24**J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. **24**G–I, arbitration module **2424** will select either demodulated baseband signal **2418***a* or **2418***c*, because error check module **2420***b* will set the error flag **2422***b* that is associated with demodulated baseband signal **2418***b*.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in U.S. Pat. No. 6,061,555 "Method and System for Ensuring Reception of a Communications Signal," filed Oct. 21, 1998, incorporated herein by reference in its entirety.

5. Unified Down-Conversion and Filtering

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. **17** is a conceptual block diagram of a UDF module **1702** according to an embodiment of the present invention. The UDF module **1702** performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module **1702** is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module **1702** effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals **1704** received by the UDF module **1702** are at radio frequencies. The UDF module **1702** effectively operates to input filter these RF input signals **1704**. Specifically, in these embodiments, the UDF module **1702** effectively performs input, channel select filtering of the RF input signal **1704**. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module **1702** effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module **1702** includes a frequency translator **1708**. The frequency translator **1708** conceptually represents that portion of the UDF module **1702** that performs frequency translation (down conversion).

The UDF module **1702** also conceptually includes an apparent input filter **1706** (also sometimes called an input filtering emulator). Conceptually, the apparent input filter **1706** represents that portion of the UDF module **1702** that performs input filtering.

In practice, the input filtering operation performed by the UDF module **1702** is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter **1706** is herein referred to as an "apparent" input filter **1706**.

The UDF module **1702** of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module **1702**. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module **1702** can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Q_S, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module **1702** can be electrically adjusted, either statically or dynamically.

Also, the UDF module **1702** can be designed to amplify input signals.

Further, the UDF module **1702** can be implemented without large resistors, capacitors, or inductors. Also, the UDF module **1702** does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module **1702** is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module **1702** are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module **1702** performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. **19** illustrates an example implementation of the unified down-converting and filtering (UDF) module **1922**. The UDF module **1922** performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. **19**, the frequency selectivity operation performed by the UDF module **1922** comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO=\alpha_1 z^{-1} VI-\beta_1 z^{-1} VO-\beta_0 z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module **1922** includes a down-convert and delay module **1924**, first and second delay modules **1928** and **1930**, first and second scaling modules **1932** and **1934**, an output sample and hold module **1936**, and an (optional) output smoothing module **1938**. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. **19**, the output smoothing module **1938** is optional.

As further described below, in the example of FIG. **19**, the down-convert and delay module **1924** and the first and second delay modules **1928** and **1930** include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2. ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2, and opens on the next corresponding falling edge of ϕ_1 or ϕ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. **19**, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module **1924** is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module **1922** has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module **1922** is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module **1922** is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module **1922** shall now be described with reference to a Table **1802** (FIG. **18**) that indicates example values at nodes in the UDF module **1922** at a number of consecutive time increments. It is assumed in Table **1802** that the UDF module **1922** begins operating at time t−1. As indicated below, the UDF module **1922** reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time t−1, a switch **1950** in the down-convert and delay module **1924** closes. This allows a capacitor **1952** to charge to the current value of an input signal, VI_{t-1}, such that node **1902** is at VI_{t-1}. This is indicated by cell **1804** in FIG. **18**. In effect, the combination of the switch **1950** and the capacitor **1952** in the down-convert and delay module **1924** operates to translate the

frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor **1952** represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module **1924** performs frequency down-conversion is further described elsewhere in this application, and is additionally described in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998, which is herein incorporated by reference in its entirety.

Also at the rising edge of ϕ_1 at time t−1, a switch **1958** in the first delay module **1928** closes, allowing a capacitor **1960** to charge to VO_{t-1}, such that node **1906** is at VO_{t-1}. This is indicated by cell **1806** in Table **1802**. (In practice, VO_{t-1}, is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time t−1, a switch **1966** in the second delay module **1930** closes, allowing a capacitor **1968** to charge to a value stored in a capacitor **1964**. At this time, however, the value in capacitor **1964** is undefined, so the value in capacitor **1968** is undefined. This is indicated by cell **1807** in table **1802**.

At the rising edge of ϕ_2 at time t−1, a switch **1954** in the down-convert and delay module **1924** closes, allowing a capacitor **1956** to charge to the level of the capacitor **1952**. Accordingly, the capacitor **1956** charges to VI_{t-1}, such that node **1904** is at VI_{t-1}. This is indicated by cell **1810** in Table **1802**.

The UDF module **1922** may optionally include a unity gain module **1990**A between capacitors **1952** and **1956**. The unity gain module **1990**A operates as a current source to enable capacitor **1956** to charge without draining the charge from capacitor **1952**. For a similar reason, the UDF module **1922** may include other unity gain modules **1990**B–**1990**G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules **1990**A–**1990**G are optional. The structure and operation of the unity gain modules **1990** will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time t−1, a switch **1962** in the first delay module **1928** closes, allowing a capacitor **1964** to charge to the level of the capacitor **1960**. Accordingly, the capacitor **1964** charges to VO_{t-1}, such that node **1908** is at VO_{t-1}. This is indicated by cell **1814** in Table **1802**.

Also at the rising edge of ϕ_2 at time t−1, a switch **1970** in the second delay module **1930** closes, allowing a capacitor **1972** to charge to a value stored in a capacitor **1968**. At this time, however, the value in capacitor **1968** is undefined, so the value in capacitor **1972** is undefined. This is indicated by cell **1815** in table **1802**.

At time t, at the rising edge of ϕ_1, the switch **1950** in the down-convert and delay module **1924** closes. This allows the capacitor **1952** to charge to VI_t, such that node **1902** is at VI_t. This is indicated in cell **1816** of Table **1802**.

Also at the rising edge of ϕ_1 at time t, the switch **1958** in the first delay module **1928** closes, thereby allowing the capacitor **1960** to charge to VO_t. Accordingly, node **1906** is at VO_t. This is indicated in cell **1820** in Table **1802**.

Further at the rising edge of ϕ_1 at time t, the switch **1966** in the second delay module **1930** closes, allowing a capacitor **1968** to charge to the level of the capacitor **1964**. Therefore, the capacitor **1968** charges to VO_{t-1}, such that node **1910** is at VO_{t-1}. This is indicated by cell **1824** in Table **1802**.

At the rising edge of ϕ_2 at time t, the switch **1954** in the down-convert and delay module **1924** closes, allowing the capacitor **1956** to charge to the level of the capacitor **1952**. Accordingly, the capacitor **1956** charges to VI_t, such that node **1904** is at VI_t. This is indicated by cell **1828** in Table **1802**.

Also at the rising edge of ϕ_2 at time t, the switch **1962** in the first delay module **1928** closes, allowing the capacitor **1964** to charge to the level in the capacitor **1960**. Therefore, the capacitor **1964** charges to VO_t, such that node **1908** is at VO_t. This is indicated by cell **1832** in Table **1802**.

Further at the rising edge of ϕ_2 at time t, the switch **1970** in the second delay module **1930** closes, allowing the capacitor **1972** in the second delay module **1930** to charge to the level of the capacitor **1968** in the second delay module **1930**. Therefore, the capacitor **1972** charges to VO_{t-1}, such that node **1912** is at VO_{t-1}. This is indicated in cell **1836** of FIG. **18**.

At time t+1, at the rising edge of ϕ_1, the switch **1950** in the down-convert and delay module **1924** closes, allowing the capacitor **1952** to charge to VI_{t+1}. Therefore, node **1902** is at VI_{t+1}, as indicated by cell **1838** of Table **1802**.

Also at the rising edge of ϕ_1 at time t+1, the switch **1958** in the first delay module **1928** closes, allowing the capacitor **1960** to charge to VO_{t+1}. Accordingly, node **1906** is at VO_{t+1}, as indicated by cell **1842** in Table **1802**.

Further at the rising edge of ϕ_1 at time t+1, the switch **1966** in the second delay module **1930** closes, allowing the capacitor **1968** to charge to the level of the capacitor **1964**. Accordingly, the capacitor **1968** charges to VO_t, as indicated by cell **1846** of Table **1802**.

In the example of FIG. **19**, the first scaling module **1932** scales the value at node **1908** (i.e., the output of the first delay module **1928**) by a scaling factor of −0.1. Accordingly, the value present at node **1914** at time t+1 is $-0.1*VO_t$. Similarly, the second scaling module **1934** scales the value present at node **1912** (i.e., the output of the second scaling module **1930**) by a scaling factor of −0.8. Accordingly, the value present at node **1916** is $-0.8*VO_{t-1}$ at time t+1.

At time t+1, the values at the inputs of the summer **1926** are: VI_t at node **1904**, $-0.1*VO_t$ at node **1914**, and $-0.8*VO_{t-1}$ at node **1916** (in the example of FIG. **19**, the values at nodes **1914** and **1916** are summed by a second summer **1925**, and this sum is presented to the summer **1926**). Accordingly, at time t+1, the summer generates a signal equal to $VI_t-0.1*VO_t-0.8*VO_{t-1}$.

At the rising edge of ϕ_1 at time t+1, a switch **1991** in the output sample and hold module **1936** closes, thereby allowing a capacitor **1992** to charge to VO_{t+1}. Accordingly, the capacitor **1992** charges to VO_{t+1}, which is equal to the sum generated by the adder **1926**. As just noted, this value is equal to: $VI_t-0.1*VO_t-0.8*VO_{t-1}$. This is indicated in cell **1850** of Table **1802**. This value is presented to the optional output smoothing module **1938**, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in U.S. Pat. No. 6,049,706 "Integrated Frequency Translation And Selectivity," filed Oct. 21, 1998, incorporated herein by reference in its entirety.

6. Example Application Embodiments of the Invention

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in

which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. **1**C, for example, where an example UFT module **115** is used in a down-conversion module **114**. In this capacity, the UFT module **115** frequency down-converts an input signal to an output signal. This is also shown in FIG. **7**, for example, where an example UFT module **706** is part of a down-conversion module **704**, which is part of a receiver **702**.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. **1**D, for example, where an example UFT module **117** is used in a frequency up-conversion module **116**. In this capacity, the UFT module **117** frequency up-converts an input signal to an output signal. This is also shown in FIG. **8**, for example, where an example UFT module **806** is part of up-conversion module **804**, which is part of a transmitter **802**.

The present invention can be used in environments having one or more transmitters **902** and one or more receivers **906**, as illustrated in FIG. **9**. In such environments, one or more of the transmitters **902** may be implemented using a UFT module, as shown for example in FIG. **8**. Also, one or more of the receivers **906** may be implemented using a UFT module, as shown for example in FIG. **7**.

The invention can be used to implement a transceiver. An example transceiver **1002** is illustrated in FIG. **10**. The transceiver **1002** includes a transmitter **1004** and a receiver **1008**. Either the transmitter **1004** or the receiver **1008** can be implemented using a UFT module. Alternatively, the transmitter **1004** can be implemented using a UFT module **1006**, and the receiver **1008** can be implemented using a UFT module **1010**. This embodiment is shown in FIG. **10**.

Another transceiver embodiment according to the invention is shown in FIG. **11**. In this transceiver **1102**, the transmitter **1104** and the receiver **1108** are implemented using a single UFT module **1106**. In other words, the transmitter **1104** and the receiver **1108** share a UFT module **1106**.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter **1202**, and an ESR module (receive) in a receiver **1210**. An example ESR embodiment configured in this manner is illustrated in FIG. **12**.

The ESR module (transmit) **1204** includes a frequency up-conversion module **1206**. Some embodiments of this frequency up-conversion module **1206** may be implemented using a UFT module, such as that shown in FIG. **1**D.

The ESR module (receive) **1212** includes a frequency down-conversion module **1214**. Some embodiments of this frequency down-conversion module **1214** may be implemented using a UFT module, such as that shown in FIG. **1**C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module **1302** is illustrated in FIG. **13**. The unified down-conversion and filtering module **1302** includes a frequency down-conversion module **1304** and a filtering module **1306**. According to the invention, the frequency down-conversion module **1304** and the filtering module **1306** are implemented using a UFT module **1308**, as indicated in FIG. **13**.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. **15**A–**15**F. FIGS. **15**A–**15**C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. **15**D indicates that a unified down-conversion and filtering module **1524** according to the invention can be utilized as a filter **1522** (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module **1524** is minimized). FIG. **15**E indicates that a unified down-conversion and filtering module **1528** according to the invention can be utilized as a down-converter **1526** (i.e., where the filter in the unified down-conversion and filtering module **1528** passes substantially all frequencies). FIG. **15**F illustrates that the unified down-conversion and filtering module **1532** can be used as an amplifier. It is noted that one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. **14**.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. **16**. In the example of FIG. **16**, one or more of the UDF modules **1610**, **1612**, **1614** operates to down-convert a received signal. The UDF modules **1610**, **1612**, **1614** also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules **1610**, **1612**, **1614** are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. **10** illustrates a transceiver **1002** that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter **1004** with a receiver **1008**.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. **16** illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

6.1 Data Communication

The invention is directed to data communication among data processing devices. For example, and without limitation, the invention is directed to computer networks such as, for example, local area networks (LANs), wide area networks (WANs), including wireless LANs (WLANs) and wireless WANs, modulator/demodulators (modems), including wireless modems, short range networks, such as Bluetooth, etc., and combinations thereof.

FIG. **25** illustrates an example environment **2502** wherein computers **2504**, **2512**, and **2526** communicate with one another via a computer network **2534**. In the example of FIG. **25**, computer **2504** is communicating with the network **2534** via a wired link, whereas computers **2512** and **2526** are communicating with the network **2534** via wireless links.

In the teachings contained herein, for illustrative purposes, a link may be designated as being a wired link or a wireless link. Such designations are for example purposes only, and are not limiting. A link designated as being wireless may alternatively be wired. Similarly, a link designated as being wired may alternatively be wireless. This is applicable throughout the entire application.

The computers **2504**, **2512** and **2526** each include an interface **2506**, **2514**, and **2528**, respectively, for communicating with the network **2534**. The interfaces **2506**, **2514**, and **2528** include transmitters **2508**, **2516**, and **2530** respectively. Also, the interfaces **2506**, **2514** and **2528** include receivers **2510**, **2518**, and **2532** respectively. In embodiments of the invention, the transmitters **2508**, **2516** and **2530** are implemented using UFT modules for performing frequency up-conversion operations (see, for example, FIG. **8**). In embodiments, the receivers **2510**, **2518** and **2532** are implemented using UFT modules for performing frequency down-conversion operations (see, for example, FIG. **7**).

As noted above, the computers **2512** and **2526** interact with the network **2534** via wireless links. In embodiments of the invention, the interfaces **2514**, **2528** in computers **2512**, **2526** represent modulator/demodulators (modems).

In embodiments, the network **2534** includes an interface or modem **2520** for communicating with the modems **2514**, **2528** in the computers **2512**, **2526**. In embodiments, the interface **2520** includes a transmitter **2522**, and a receiver **2524**. Either or both of the transmitter **2522**, and the receiver **2524** are implemented using UFT modules for performing frequency translation operations (see, for example, FIGS. **7** and **8**).

In alternative embodiments, one or more of the interfaces **2506**, **2514**, **2520**, and **2528** are implemented using transceivers that employ one or more UFT modules for performing frequency translation operations (see, for example, FIGS. **10** and **11**).

FIG. **26** illustrates another example data communication embodiment **2602**. Each of a plurality of computers **2604**, **2612**, **2614** and **2616** includes an interface, such as an interface **2606** shown in the computer **2604**. It should be understood that the other computers **2612**, **2614**, **2616** also include an interface such as an interface **2606**. The computers **2604**, **2612**, **2614** and **2616** communicate with each other via interfaces **2606** and wireless or wired links, thereby collectively representing a data communication network.

The interfaces **2606** may represent any computer interface or port, such as but not limited to a high speed internal interface, a wireless serial port, a wireless PS2 port, a wireless USB port, PCMCIA port, etc.

The interface **2606** includes a transmitter **2608** and a receiver **2610**. In embodiments of the invention, either or both of the transmitter **2608** and the receiver **2610** are implemented using UFT modules for frequency up-conversion and down-conversion (see, for example, FIGS. **7** and **8**). Alternatively, the interfaces **2806** can be implemented using a transceiver having one or more UFT modules for performing frequency translation operations (see, for example, FIGS. **10** and **11**).

FIGS. **33**–**38** illustrate other scenarios envisioned and encompassed by the invention. FIG. **33** illustrates a data processing environment **3302** wherein a wired network, such as an Ethernet network **3304**, is linked to another network, such as a WLAN **3306**, via a wireless link **3308**. The wireless link **3308** is established via interfaces **3310**, **3312** which are preferably implemented using universal frequency translation modules.

The invention includes multiple networks linked together. The invention also envisions wireless networks conforming to any known or custom standard or specification. This is shown in FIG. **34**, for example, where any combination of WLANs conforming to any WLAN standard or configuration, such as IEEE 802.11 (described in further detail elsewhere herein), any cellular telephone standard or specification, any WAN standard, any short range wireless standard, any type of radio links, any custom standard or specification, etc., can be implemented using the universal frequency translation technology described herein. Also, any combination of these networks may be coupled together. It is noted that the invention is not limited to the embodiment shown in FIG. **34**.

The invention supports WLANs and/or other communication networks (and combinations thereof) that are located in one or multiple buildings, as shown in FIGS. **35** and **36**. The invention also supports WLANs and/or other communication networks (and combinations thereof) that are located in an area including and external to one or more buildings, as shown in FIG. **37**. In fact, the invention is directed to networks that cover any defined geographical area, as shown in FIG. **38**. In the embodiments described above, wireless links are preferably established using interfaces as described herein.

6.1.1. Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.

The present invention is now described as implemented in an interface, such as but not limited to a wireless modem, which can be utilized to implement a wireless local area network (WLAN) or wireless wide area network (WWAN), for example. In an embodiment, the present invention is implemented in a WLAN to support IEEE WLAN Standard 802.11, but this embodiment is mentioned for illustrative purposes only. The invention is not limited to this standard or the WLAN embodiment and described herein.

Conventional wireless modems are described in, for example, U.S. Pat. No. 5,764,693, titled, "Wireless Radio Modem with Minimal Inter-Device RF Interference," incorporated herein by reference in its entirety. The present invention replaces a substantial portion of conventional wireless modems with one or more universal frequency translators (UFTs). The resultant improved wireless modem consumes less power than conventional wireless modems and is easier and less expensive to design and build. A wireless modem in accordance with the present invention can be implemented in a PC-MCIA card or within a main housing of a computer, or on one or more chips, in any data processing or communication device (desk top, handheld, etc.) for example. The invention is not limited to these examples.

FIG. **27** illustrates an example block diagram of a device **2710**, which can be wirelessly coupled to a LAN, as illustrated for example in FIGS. **25** and **26**. The device **2710** includes an interface **2714** and an antenna **2712**. The interface **2714** includes a transmitter module **2716** that receives information from a digital signal processor (DSP) **2720**, and modulates and up-converts the information for transmission from the antenna **2712**. The interface **2714** also includes a receiver module **2718** that receives modulated carrier signals via the antenna **2712**. The receiver module **2718** down-converts and demodulates the modulated carrier signals to baseband information, and provides the baseband information to the DSP **2720**. The DSP **2720** can include a central processing unit (CPU) and other components of the device **2710**. Conventionally, the interface **2714** is implemented with heterodyne components. The device can be any data processing or communication device, or other device where communication with external devices is desired.

FIG. **28** illustrates an example interface **2810** implemented with heterodyne components. The interface **2810** includes a transmitter module **2812** and a receiver module **2824**. The receiver module **2824** includes an RF section **2830**, one or more IF sections **2828**, a demodulator section **2826**, an optional analog to digital (A/D) converter **2834**, and a frequency generator/synthesizer **2832**. The transmitter module **2812** includes an optional digital to analog (D/A) converter **2822**, a modulator section **2818**, one or more IF sections **2816**, an RF section **2814**, and a frequency generator/synthesizer **2820**. Operation of the interface **2810** will be apparent to one skilled in the relevant art(s), based on the description herein.

FIG. **29** illustrates an example in-phase/quadrature-phase (I/Q) interface **2910** implemented with heterodyne components. I/Q implementations allow two channels of information to be communicated on a carrier signal and thus can be utilized to increase data transmission.

The interface **2910** includes a transmitter module **2912** and a receiver module **2934**. The receiver module **2934** includes an RF section **2936**, one or more IF sections **2938**, an I/Q demodulator section **2940**, an optional A/D converter **2944**, and a frequency generator/synthesizer **2942**. The I/Q demodulator section **2940** includes a signal splitter **2946**, mixers **2948**, and a phase shifter **2950**. The signal splitter **2946** provides a received signal to the mixers **2948**. The phase shifter **2950** operates the mixers **2948** ninety degrees out of phase with one another to generate I and Q information channels **2952** and **2954**, respectively, which are provided to a DSP **2956** through the optional A/D converter **2944**.

The transmitter module **2912** includes an optional D/A converter **2922**, an I/Q modulator section **2918**, one or more IF sections **2916**, an RF section **2914**, and a frequency generator/synthesizer **2920**. The I/Q modulator section **2918** includes mixers **2924**, a phase shifter **2926**, and a signal combiner **2928**. The phase shifter **2926** operates the mixers **2924** ninety degrees out of phase with one another to generate I and Q modulated information signals **2930** and **2932**, respectively, which are combined by the signal combiner **2928**. The IF section(s) **2916** and RF section **2914** up-convert the combined I and Q modulated information signals **2930** and **2932** to RF for transmission by the antenna, in a manner well known in the relevant art(s).

Heterodyne implementations, such as those illustrated in FIGS. **28** and **29**, are expensive and difficult to design, manufacture and tune. In accordance with the present invention, therefore, the interface **2714** (FIG. **27**) is preferably implemented with one or more universal frequency translation (UFT) modules, such as the UFT module **102** (FIG. **1**A or other embodiments described herein, or equivalents thereof). Thus previously described benefits of the present invention are obtained in wireless modems, WLANs, or even wired devices, etc.

FIG. **30** illustrates an example block diagram embodiment of the interface **2714** that is associated with a computer or any other data processing or communication device. In FIG. **30**, the receiver module **2718** includes a universal frequency down-converter (UFD) module **3014** and an optional analog to digital (A/D) converter **3016**, which converts an analog output from the UFD **3014** to a digital format for the DSP **2720**. The transmitter module **2716** includes an optional modulator **3012** and a universal frequency up-converter (UFU) module **3010**. The optional modulator **3012** can be a variety of types of modulators, including conventional modulators. Alternatively, the UFU module **3010** includes modulator functionality. The example implementation of FIG. **30** operates substantially as described above and in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998, and U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998.

FIG. **31** illustrates an example implementation of the interface **2714** illustrated in FIG. **30**, wherein the receiver UFD **3014** includes a UFT module **3112**, and the transmitter UFU **3010** includes a universal frequency translation (UFT) module **3110**. This example implementation operates substantially as described above and in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998, and U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998.

FIG. **32** illustrates an example I/Q implementation of the interface module **2710**. Other I/Q implementations are also contemplated and are within the scope of the present invention.

In the example of FIG. **32**, the receiver UFD module **3014** includes a signal divider **3228** that provides a received I/Q modulated carrier signal **3230** between a third UFT module **3224** and a fourth UFT module **3226**. A phase shifter **3232**, illustrated here as a 90 degree phase shifter, controls the third and fourth UFT modules **3224** and **3226** to operate 90 degrees out of phase with one another. As a result, the third and fourth UFT modules **3224** and **3226** down-convert and demodulate the received I/Q modulated carrier signal **3230**, and output I and Q channels **3234** and **3236**, respectively, which are provided to the DSP **2720** through the optional A/D converter **3016**.

In the example of FIG. **32**, the transmitter UFU module **3010** includes first and second UFT modules **3212** and **3214** and a phase shifter **3210**, which is illustrated here as a 90

degree phase shifter. The phase shifter **3210** receives a lower frequency modulated carrier signal **3238** from the modulator **3012**. The phase shifter **3210** controls the first and second UFT modules **3212** and **3214** to operate 90 degrees out of phase with one another. The first and second UFT modules **3212** and **3214** up-convert the lower frequency modulated carrier signal **3238**, which are output as higher frequency modulated I and Q carrier channels **3218** and **3220**, respectively. A signal combiner **3216** combines the higher frequency modulated I and Q carrier channels **3218** and **3220** into a single higher frequency modulated I/Q carrier signal **3222** for transmitting by the antenna **2712**.

The example implementations of the interfaces described above, and variations thereof, can also be used to implement network interfaces, such as the network interface **2520** illustrated in FIG. **25**.

More generally, the invention is directed to WLAN client devices and WLAN infrastructure devices. "WLAN Client Devices" refers to, for example, any data processing and/or communication devices in which wired or wireless communication functionality is desired, such as but not limited to computers, personal data assistants (PDAs), automatic identification data collection devices (such as bar code scanners/readers, electronic article surveillance readers, and radio frequency identification readers), telephones, network devices, etc., and combinations thereof. "WLAN Infrastructure Devices" refers to, for example, Access Points and other devices used to provide the ability for WLAN Client Devices (as well as potentially other devices) to connect to wired and/or wireless networks and/or to provide the network functionality of a WLAN. "WLAN" refers to, for example, a Wireless Local Area Network that is implemented according to and that operates within WLAN standards and/or specifications, such as but not limited to IEEE 802.11, IEEE 802.11 a, IEEE 802.11b, HomeRF, Proxim Range LAN, Proxim Range LAN2, Symbol Spectrum 1, Symbol Spectrum 24 as it existed prior to adoption of IEEE 802.11, HiperLAN1, or HiperLAN2. WLAN client devices and/or WLAN infrastructure devices may operate in a multimode capacity. For example, a device may include WLAN and WAN functionality. Another device may include WLAN and short range communication (such as but not limited to Blue Tooth) functionality. Another device may include WLAN and WAN and short range communication functionality. It is noted that the above definitions and examples are provided for illustrative purposes, and are not limiting. Equivalents to that described above will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.1.2 Example Modifications

The RF modem applications, WLAN applications, etc., described herein, can be modified by incorporating one or more of the enhanced signal reception (ESR) techniques described herein. Use of ESR embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The RF modem applications, WLAN applications, etc., described herein can be enhanced by incorporating one or more of the unified down-conversion and filtering (UDF) techniques described herein. Use of UDF embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.2. Other Example Applications

The application embodiments described above are provided for purposes of illustration. These applications and embodiments are not intended to limit the invention. Alternate and additional applications and embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, such alternate and additional applications and embodiments include combinations of those described above. Such combinations will be apparent to persons skilled in the relevant art(s) based on the herein teachings.

6.3. Example WLAN Implementation Embodiments

6.3.1. Architecture

FIG. **39** is a block diagram of a WLAN interface **3902** (also referred to as a WLAN modem herein) according to an embodiment of the invention. The WLAN interface/modem **3902** includes an antenna **3903**, a low noise amplifier or power amplifier (LNA/PA) **3904**, a receiver **3906**, a transmitter **3910**, a control signal generator **3908**, a demodulator/modulator facilitation module **3912**, and a media access controller (MAC) interface **3914**. The MAC interface **3914** couples the WLAN interface/modem **3902** to a computer **3916** or other data processing or communication device. The computer **3916** preferably includes a MAC **3918**.

The WLAN interface/modem **3902** represents a transmit and receive application that utilizes the universal frequency translation technology described herein. It also represents a zero IF (or direct-to-data) WLAN architecture.

The WLAN interface/modem **3902** also represents a vector modulator and a vector demodulator using the universal frequency translation (UFT) technology described herein. Use of the UFT technology enhances the flexibility of the WLAN application (i.e., makes it universal).

In the embodiment shown in FIG. **39**, the WLAN interface/modem **3902** is compliant with WLAN standard IEEE 802.11. However, the invention is not limited to this standard. The invention is applicable to any communication standard or specification, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein. Any modifications to the invention to operate with other standards or specifications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. **39**, the WLAN interface/modem **3902** provides half duplex communication. However, the invention is not limited to this communication mode. The invention is applicable and directed to other communication modes, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. **39**, the modulation/demodulation performed by the WLAN interface/modem **3902** is preferably direct sequence spread spectrum QPSK (quadrature phase shift keying) with differential encoding. However, the invention is not limited to this modulation/demodulation mode. The invention is applicable and directed to other modulation and demodulation modes, such as but not limited to those described herein, as well as frequency hopping according to IEEE 802.11, OFDM (orthogonal frequency division multiplexing), as well as others. These modulation/demodulation modes will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

The operation of the WLAN interface/modem **3902** when receiving shall now be described.

Signals **3922** received by the antenna **3903** are amplified by the LNA/PA **3904**. The amplified signals **3924** are down-converted and demodulated by the receiver **3906**. The receiver **3906** outputs I signal **3926** and Q signal **3928**.

FIG. **40** illustrates an example receiver **3906** according to an embodiment of the invention. It is noted that the receiver **3906** shown in FIG. **40** represents a vector modulator. In an embodiment, the "receiving" function performed by the WLAN interface/modem **3902** can be considered to be all processing performed by the WLAN interface/modem **3902** from the LNA/PA **3904** to generation of baseband information.

Signal **3924** is split by a 90 degree splitter **4001** to produce an I signal **4006**A and Q signal **4006**B that are preferably 90 degrees apart in phase. I and Q signals **4006**A, **4006**B are down-converted by UFD (universal frequency down-conversion) modules **4002**A, **4002**B. The UDF modules **4002**A, **4002**B output down-converted I and Q signals **3926**, **3928**. The UFD modules **4002**A, **4002**B each includes at least one UFT (universal frequency translation) module **4004**A. UFD and UFT modules are described above.

The demodulator/modulator facilitation module **3912** receives the I and Q signals **3926**, **3928**. The demodulator/modulator facilitation module **3912** optionally amplifies and filters the I and Q signals **3926**, **3928**. The demodulator/modulator facilitation module **3912** also optionally performs automatic gain control (AGC) functions. The AGC function is coupled with the universal frequency translation technology described herein. The demodulator/modulator facilitation module **3912** outputs processed I and Q signals **3930**, **3932**.

The MAC interface **3914** receives the processed I and Q signals **3930**, **3932**. The MAC interface **3914** preferably includes a baseband processor. The MAC interface **3914** preferably performs functions such as combining the I and Q signals **3930**, **3932**, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface **3914** and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The MAC interface **3914** outputs the baseband information signal, which is received and processed by the computer **3916** in an implementation and application specific manner.

In the example embodiment of FIG. **39**, the demodulation function is distributed among the receiver **3906**, the demodulator/modulator facilitation module **3912**, and a baseband processor contained in the MAC interface **3914**. The functions collectively performed by these components include, but are not limited to, de-spreading the information, differentially decoding the information, tracking the carrier phase, de-scrambling, recreating the data clock, and combining the I and Q signals. The invention is not limited to this arrangement. These demodulation-type functions can be centralized in a single component, or distributed in other ways.

The operation of the WLAN interface/modem **3902** when transmitting shall now be described.

A baseband information signal **3936** is received by the MAC interface **3914** from the computer **3916**. The MAC interface **3914** preferably performs functions such as splitting the baseband information signal to form I and Q signals **3930**, **3932**, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface **3914** and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The demodulator/modulator facilitation module **3912** filters and amplifies the I and Q signals **3930**, **3932**. The demodulator/modulator facilitation module **3912** outputs processed I and Q signals **3942**, **3944**. Preferably, at least some filtering and/or amplifying components in the demodulator/modulator facilitation module **3912** are used for both the transmit and receive paths.

The transmitter **3910** up-converts the processed I and Q signals **3942**, **3944**, and combines the up-converted I and Q signals. This up-converted/combined signal is amplified by the LNA/PA **3904**, and then transmitted via the antenna **3903**.

FIG. **41** illustrates an example transmitter **3910** according to an embodiment of the invention. The device in FIG. **41** can also be called a vector modulator. The "transmit" function performed by the WLAN interface/modem **3902** can be considered to be all processing performed by the WLAN interface/modem **3902** from receipt of baseband information through the LNA/PA **3904**.

I and Q signals **3942**, **3944** are received by UFU (universal frequency up-conversion) modules **4102**A, **4102**B. The UFU modules **4102**A, **4102**B each includes at least one UFT module **4104**A, **4104**B. The UFU modules **4102**A, **4102**B up-convert I and Q signals **3942**, **3944**. The UFU modules **4102**A, **4102**B output up-converted I and Q signals **4106**, **4108**. The 90 degree combiner **4110** effectively phase shifts either the I signal **4106** or the Q signal **4108** by 90 degrees, and then combines the phase shifted signal with the unshifted signal to generate a combined, up-converted I/Q signal **3946**.

In the example embodiment of FIG. **39**, the modulation function is distributed among the transmitter **3910**, the demodulator/modulator facilitation module **3912**, and a baseband processor contained in the MAC interface **3914**. The functions collectively performed by these components include, but are not limited to, differentially encoding data, splitting the baseband information signal into I and Q signals, scrambling data, and data spreading. The invention is not limited to this arrangement. These modulation-type functions can be centralized in a single component, or distributed in other ways.

The components in the WLAN interface/modem **3902** are preferably controlled by the MAC interface **3914** in operation with the MAC **3918** in the computer **3916**. This is represented by the distributed control arrow **3940** in FIG. **39**. Such control includes setting the frequency, data rate, whether receiving or transmitting, and other communication characteristics/modes that will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

FIG. **42** illustrates an example implementation of the WLAN interface/modem **3902**. It is noted that in this implementation example, the MAC interface **3914** is located on a different board.

FIG. **62** is an example motherboard corresponding to FIG. **42**. FIG. **63** is an example bill-of-materials (BOM) list for the motherboard of FIG. **62**. This and other implementations are provided herein for example purposes only. Other implementations will be apparent to persons skilled in the relevant art(s), and the invention is directed to such other implementations.

FIG. **102** illustrates an alternate example PCMCIA test bed assembly for a WLAN interface/modem **3902** according to an embodiment of the invention. In this embodiment, the baseband processor **10202** is separate from the MAC interface **3914**.

In some applications, it is desired to separate the receive path and the transmit path. FIG. **43** illustrates an example receive implementation, and FIG. **44** illustrates an example transmit implementation.

6.3.2. Receiver

An example implementation of the receiver **3906** (vector demodulator) is shown in FIG. **53**. An example BOM list for the receiver **3906** of FIG. **53** is shown in FIG. **54**. It is noted that the invention is not limited to this example.

6.3.3. Transmitter

An example implementation of the transmitter **3910** (vector modulator) is shown in FIGS. **57**–**60**. The data conditioning interfaces **5802** in FIG. **58** effectively pre-process the I and Q signals **3942**, **3944** before being received by the UFU modules **4102**. An example BOM list for the transmitter **3910** of FIGS. **57**–**60** is shown in FIGS. **61**A and **61**B. It is noted that the invention is not limited to this example.

6.3.4. Demodulator/Modulator Facilitation Module

An example demodulator/modulator facilitation module **3912** is shown in FIGS. **47** and **48**. A corresponding BOM list is shown in FIGS. **49**A–C.

An alternate example demodulator/modulator facilitation module **3912** is shown in FIGS. **50** and **51**. A corresponding BOM list is shown in FIGS. **52**A and **52**B. It is noted that the invention is not limited to this example.

6.3.5. MAC Interface

An example MAC interface **3914** is shown in FIG. **45**. A corresponding BOM list is shown in FIGS. **46**A–C. It is noted that the invention is not limited to this example.

6.3.6. Control Signal Generator—Synthesizer

In an embodiment, the control signal generator **3908** is preferably implemented using a synthesizer. An example synthesizer is shown in FIG. **55**. A corresponding BOM list is shown in FIGS. **56**A and **56**B. It is noted that the invention is not limited to this example.

6.3.7. LNA/PA

An example LNA/PA **3904** is shown in FIGS. **64** and **65**. A corresponding BOM list is shown in FIG. **66**. It is noted that the invention is not limited to this example.

6.3.8. Test Results

Test results relating to the operation of the WLAN interface/modem **3902** are shown in FIGS. **67**–**70**, **90**–**94**, and **151**–**169**. FIGS. **95**–**100** relate to IIP2 and IIP3, and FIG. **101** relates to power consumption. It is noted that the invention is not limited to this example.

6.4 IEEE Standard 802.11 Background

Embodiments of the present invention shall now be described in greater detail. It is noted that these embodiments are described herein for illustrative purposes only. The invention is not limited to these embodiments. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

IEEE Std 802.11-1997 defines a medium access control (MAC) sublayer, MAC management protocols and services, and three physical (PHY) layers. The three PHY layers are an infrared (1R) baseband PHY, a frequency hopping spread spectrum (FHSS) radio in the 2.4 GHz band, and a direct sequence spread spectrum (DSSS) radio in the 2.4 GHz band. All three physical layers describe both 1 and 2 Mbps operation. The universal frequency translation techniques of the present invention are applicable to these physical layers.

Two further PHY layers are IEEE Std 802.11a and IEEE Std 802.11b. IEEE Std 802.11a is an orthogonal frequency domain multiplexing (OFDM) radio in the UNII bands, delivering up to 54 Mbps data rates. The second, IEEE Std 802.11b, is an extension to the DSSS PHY in the 2.4 GHz band, delivering up to 11 Mbps data rates. The present invention is also applicable to these physical layers.

The IEEE 802.11 standard describes a WLAN that delivers services similar to those found in wired networks, including high throughput, highly reliable data delivery, and continuous network connections. In addition, IEEE 802.11 describes a WLAN that allows transparent mobility and built-in power saving operations to the network user. The subsections that follow describe the architecture of the IEEE 802.11 network, concepts related to supporting the architecture, and applications of universal frequency translation in the IEEE 802.11 network architecture.

Further details on designing, configuring, and operating WLANs and WLAN stations according to IEEE Standard 802.11 are provided in a number of publicly available documents, such as Bob O'Hara & Al Petrick, "IEEE 802.11 Handbook: A Designer's Companion" (1999) (hereinafter IEEE 802.11 Handbook), which is incorporated herein by reference in its entirety.

6.4.1 IEEE 802.11 Architecture

An IEEE 802.11 WLAN provides a network where most decision making is distributed to mobile stations. This provides several advantages, including being tolerant of faults in WLAN equipment and eliminating bottlenecks that may be present in a centralized architecture. The IEEE 802.11 WLAN architecture is very flexible, supporting small, transient networks and large semipermanent or permanent networks. Deep power-saving modes of operation are built into the architecture, along with protocols to prolong the battery life of mobile equipment without losing network connectivity. These advantages of the IEEE 802.11 WLAN architecture may be enhanced by the incorporation of universal frequency translation technology of the present invention. An IEEE 802.11 architecture environment may comprise several components. These may include: the station, the access point (AP), the wireless medium, the basic service set, the distribution system (DS), and the Extended Service Set. The architecture may also include station services and distribution services.

The IEEE 802.11 WLAN architecture also embeds a level of indirection that has not been present in previous LANs. This level of indirection, transparent to protocol users of the IEEE 802.11 WLAN, allows a mobile station to roam throughout a WLAN while appearing to be stationary to protocols above the MAC that have no concept of mobility. This ability allows all of the existing network protocols to run over a WLAN without any special considerations.

6.4.1.1 The Station

The station connects to the wireless medium. The station includes a MAC and a PHY. In embodiments, the station may be referred to as the network adapter or network interface card (NIC), as known to persons skilled in the relevant art(s) from the teachings herein.

The station may be mobile, portable, or stationary. Every station supports station services. These services include authentication, de-authentication, privacy, and delivery of the data (MAC service data unit or MSDU in the standard). Station services are further described elsewhere herein. Embodiments of WLAN stations incorporating universal frequency translation technology of the present invention are presented further below.

6.4.1.2 The Basic Service Set

A basic service set (BSS) is a set of stations that communicate with one another. When all stations in a BSS are mobile stations, and there is no connection to a wired network, the BSS may be referred to as an independent BSS (IBSS). An IBSS is an entire network. Only those stations communicating with each other in the IBSS are part of the LAN. An IBSS may be a short-lived network, with a small number of stations, that is created for a particular purpose.

Mobile stations within an IBSS communicate directly with one another. Not every mobile station within an IBSS

may be able to communicate with every other mobile station, but they are all part of the same IBSS. There is no relay function in an IBSS. Thus, if one mobile station must communicate with another, they must be in direct communication range. FIG. **124** illustrates an IBSS **12400** with mobile stations that must be in direct communication range to communicate with each other.

When a BSS includes an access point (AP), the BSS is no longer independent. It may then be referred to as an infrastructure BSS, or simply a BSS. An AP is a station that also provides distribution services. Distribution services are further described elsewhere herein.

In an infrastructure BSS, all mobile stations communicate with the AP. The AP provides both a connection to a wired LAN, if one exists, and a local relay function for the BSS. For example, if one mobile station in a BSS must communicate with another mobile station within the BSS, the communication is sent first to the AP, and then from the AP to the other mobile station. Hence, communications that both originate and end in the same BSS may consume twice the bandwidth as direct communications from one mobile station to another. FIG. **101**A illustrates an IBSS **10100** with mobile stations that communicate through an AP **10102**. A benefit provided by an AP is the buffering of traffic for a mobile station while that station is operating in a very low power state. Protocols and mechanisms supporting power saving by mobile stations are further described elsewhere herein. An AP may incorporate universal frequency translation technology to provide for the AP's relay communication function. FIG. **101**B illustrates an AP **10102** that includes a universal frequency translation module **10204**, according to an embodiment of the present invention. The embodiments presented herein for receiving and transmitting WLAN signals by WLAN stations are applicable to APs.

6.4.1.3 Extended Service Set (ESS)

A benefit provided by a WLAN is the mobility it provides to its users. This mobility is not confined to a single BSS. IEEE 802.11 extends the range of mobility to any arbitrary range through an extended service set (ESS). An ESS is a set of two or more infrastructure BSSs. In an ESS, APs communicate among themselves to forward traffic from one BSS to another, and to facilitate the movement of mobile stations from one BSS to another. The APs perform this communication via an abstract medium called the distribution system (DS). The DS is a backbone of the WLAN and may be constructed of either wired or wireless networks. The DS is a thin layer in each AP that determines whether communications received from the BSS are to be relayed back to a destination in the BSS, forwarded on the DS to another AP, or sent into the wired network infrastructure to a destination not in the ESS. Communications received by an AP from the DS are transmitted to the BSS to be received by the particular destination mobile station. To network equipment outside of the ESS, the ESS and all of its mobile stations appears to be a single MAC-layer network where all stations are physically stationary. Thus, the ESS hides the mobility of the mobile stations from everything outside the ESS. The IEEE 802.11 architecture provides this level of indirection, allowing existing network protocols that have no concept of mobility to operate correctly with a WLAN where mobility exists. FIG. **125** illustrates an exemplary ESS **12500**.

6.4.1.4 Distribution System

The distribution system (DS) allows an AP to communicate with another AP. The APs may exchange frames for stations in their BSSs, forward frames to follow mobile stations from one BSS to another, and exchange frames with wired networks, if any. As set forth by IEEE 802.11, the DS is not necessarily a network. The standard does not place any restrictions on how the DS is implemented, only on the services it must provide. Thus, the DS may be a wired network, for example, such as IEEE 802.3, or it may be an application specific box that interconnects the AP, and provides the required distribution services.

6.4.1.5 IEEE 802.11 Services

There are nine services defined by the IEEE 802.11 architecture. These services may be divided into two groups: station services and distribution services. Station services comprise authentication, de-authentication, privacy, and delivery of the data. Distribution services comprise association, disassociation, re-association, distribution, and integration.

6.4.1.5.1 Station Services

Four station services—authentication, de-authentication, privacy, and data delivery-provide a IEEE 802.11 WLAN with functions similar to those expected of a wired network. The physical network cable connection of a wired network is similar to the authentication and de-authentication services, where use of the network is limited to authorized users. The authentication service is used to prove the identity of one station to another. Without this proof of identity, the station is not allowed to use the WLAN for data delivery. The de-authentication service is used to eliminate a previously authorized user from any further use of the network. Thus, once a station is de-authenticated (for example, when an employee resigns) that station can no longer access the services of the IEEE 802.11 WLAN.

The privacy service of IEEE 802.11 is designed to provide an equivalent level of protection for data traversing the WLAN as is provided by a wired network that exists in an office building with restricted physical access to the network plant. This service protects the data only as it traverses the wireless medium. It is not designed to provide complete protection of data between applications running over a mixed network environment that happens to include an IEEE 802.11 WLAN.

Finally, the data delivery service of an IEEE 802.11 WLAN is similar to that provided by all other IEEE 802.11 LANs. The data delivery service provides reliable delivery of data frames from a MAC in a first station to a MAC in one or more further stations, with minimal duplication and minimal reordering.

6.4.1.5.2 Distribution Services

Five distribution services—association, re-association, disassociation, distribution, and integration—provide services necessary to allow mobile stations to roam freely within an ESS, and to allow an IEEE 802.11 WLAN to connect with a wired LAN infrastructure. The distribution services comprise a thin layer above the MAC and below the logical link control (LLC) sublayer. The distribution services may be invoked to determine how to forward frames within an IEEE 802.11 WLAN, and to determine how to deliver frames from a IEEE 802.11 WLAN to network destinations outside of the WLAN.

The association service is used to make a logical connection between a mobile station and an AP. This logical connection allows for the DS to know where and how to deliver data to the mobile station. The logical connection allows the AP to accept data frames from the mobile station and to allocate resources to support the mobile station. Typically, the association service is invoked once, when the mobile station enters the WLAN for the first time, such as after the application of power, or when rediscovering the WLAN after being out of touch for a time.

The re-association service is similar to the association service, with a difference that it includes information about the AP with which a mobile station has been previously associated. A mobile station may use the re-association service repeatedly as it moves throughout an ESS. For instance, the mobile station may lose contact with an AP with which it is associated, and may need to become associated with a new AP. Through the re-association service, a mobile station provides information to an AP to which it will become associated. This information allows the AP to contact the AP previously associated with the mobile station. The previously associated AP may be contacted to obtain frames that may be waiting there for delivery to the mobile station, as well as other information that may be relevant.

The disassociation service may be used to force a mobile station to disassociate. An AP may inform one or more mobile stations that the AP can no longer provide the logical connection to the WLAN. This may be due to the available resources in the AP being exceeded, the AP shutting down, or other reasons. When the mobile station becomes disassociated, it may begin a new association by invoking the association service.

A mobile station may also use the disassociation service. When a mobile station is aware that it will no longer require the services of an AP, it may invoke the disassociation service to notify the AP that the logical connection to the WLAN is not required. For example, this may occur when the mobile station is being shut down, or when the IEEE 802.11 adapter card is being ejected. Once the mobile station is disassociated, an AP may recover any resources dedicated to the mobile station for other uses.

When determining how to deliver the frames it receives, an AP uses the distribution service. When a mobile station sends a frame to an AP for delivery to another station, the AP invokes the distribution service to determine where to send the frame. It must be determined if the frame should be sent back into its own BSS for delivery to a mobile station associated with the AP, if the frame should be sent into the DS for delivery to another mobile station associated with a different AP, or if the frame should be sent to a network destination outside the IEEE 802.11 WLAN. The distribution service determines whether the frame is sent to another AP or to a portal.

The integration service couples the IEEE 802.11 WLAN to other LANs, including possibly one or more wired LANs, or other IEEE 802.11 WLANs. A portal performs the integration service. The portal is an abstract architectural concept and may physically reside as a thin layer in some or all APs, or may be a separate network component entirely. The integration service translates IEEE 802.11 frames into frames that may traverse another network. The integration service also translates frames from other network types to frames that may be delivered by an IEEE 802.11 WLAN.

6.4.1.5.3 Service Interaction

The IEEE 802.11 standard states that each station must maintain two variables that are dependent on the authentication/de-authentication services and the association/re-association/disassociation services. The two variables are authentication state and association state. While the standard describes these variables as being enumerated types, they are typically available internal to an implementation, and may be implemented as Boolean truth-values. The variables may be used in a simple state machine that determines the order in which certain services may be invoked and when a station may begin using the data delivery service. The variables must exist in enough instances to allow the station to maintain a unique copy for each station with which it communicates. A station may be authenticated with many different stations simultaneously. However, a station may be associated with only one other station at a time.

FIG. **126** illustrates a state diagram **12600** showing the relationship between state variables and services. A station begins operation in a first state, state **12602**, where both authentication state and association state are false, indicating that the station is neither authenticated nor associated. In state **12602**, a station may use a very limited number of frame types, which are more fully described below. The allowable frame types provide the capability for a station in state **12602** to find an IEEE 802.11 WLAN, an ESS, and its APs, to complete the required frame handshake protocols, and to implement the authentication service. If a station is not successful in becoming authenticated, it will remain in state **12602**. If a station becomes authenticated, authentication state is set to true, and the station will make a transition to a state **12604**. This transition is shown in FIG. **126** as transition **12608**.

If a station is part of an IBSS, it may implement the data service in state **12602**. This is because neither authentication nor association are used in an IBSS, leaving no mechanism for a station in an IBSS to leave state **12602**.

In the second state, state **12604**, the station has been authenticated. This is indicated by the authentication state being true. In state **12604**, however, the station has not yet associated. In state **12604**, additional frame types are allowed, beyond those allowed in state **12602**. The additional frame types provide the capability for a station in state **12604** to implement the association, re-association, and disassociation services. If a station is not successful in becoming associated, it will remain in state **12604**, unless it receives a de-authentication notification. If it receives a de-authentication notification, it will return to state **12602** via a transition **12610**, and authentication state will be made false. If a station becomes associated, setting association state to true, it will travel along a transition **12612** to a state **12606**.

In the third state, state **12606**, the station has been both authenticated and associated, indicated by both authentication state and association state being true. In this state, all frame types are allowed and the station may use the data delivery service. A station will remain in state **12606** until receiving either a disassociation notification or a de-authentication notification, or until it re-associates with another station. If a station receives a disassociation notification, it will travel along a transition **12614** to state **12604** and set association state to false. If a station receives a de-authentication notification, it will travel along a transition **12616** to state **12602** and set both authentication state and association states to false.

A station must react to frames it receives in each of the states, even those frames that are disallowed for a particular state. A station will send a de-authentication notification to any station with which it is not authenticated if it receives frames that are not allowed in state **12602**. A station will send a disassociation notification to any station with which it is authenticated, but not associated, if it receives frames not allowed in state **12604**. These notifications will force the station that sent the disallowed frames to make a transition to the proper state, allowing it to proceed properly toward state **12606**.

A station may make many transitions between states of state diagram **12600** shown in FIG. **126** as it roams through an ESS. Because a station may be authenticated with many stations at once, it may be in state **12604** with relation to

those stations. However, a station may be in state **12606** with relation to a different station. When a station re-associates with another station, the station with which it was previously associated must be moved back to state **12604**, setting the value of associated state for that station to false.

FIG. **127** illustrates a station **12702** moving between APs. As the station **12702** finds a first AP, AP **12704**, it will authenticate and associate (a). As station **12702** moves, it may pre-authenticate with a second AP, AP **12706** (b). When the station **12702** determines that its association with AP **12704** is no longer desirable, it may re-associate with AP **12706** (c). The re-association with AP **12706** causes AP **12706** to notify AP **12704** of the new location of station **12702**, terminating the previous association of station **12702** with AP **12704** (d). At some point, AP **12706** may be taken out of service. If this occurs, AP **12706** disassociates the stations that were associated with it (e). This would require station **12702** to find another access point, AP **12708**, and to authenticate and associate, in order to continue using the wireless LAN (f).

The architecture and services of IEEE 802.11 allow a WLAN to appear similar to wired LANs. The architecture divides the functionality of the WLAN into non-overlapping functional blocks. The services described by IEEE 802.11 provide the user of IEEE 802.11 with the functionality of a wired LAN and the additional benefits of mobility.

6.5 Medium Access Control Overview

The IEEE 802.11 medium access control (MAC) supplies the functionality required to provide a reliable delivery mechanism for user data over potentially noisy, unreliable wireless media. The MAC does this while also providing advanced LAN services, equal to or beyond those of wired LANs.

6.5.1 MAC Functionality

A first function of the MAC is to provide a reliable data delivery service to users of the MAC. Through a frame exchange protocol at the MAC level, the IEEE 802.11 MAC improves on the reliability of data delivery over wireless media, as compared to earlier WLANs.

A second function of the IEEE 802.11 MAC is to control access to the shared wireless medium. It performs this function through two different access mechanisms: the basic access mechanism, known as the distributed coordination function, and a centrally controlled access mechanism, known as the point coordination function.

A third function of the IEEE 802.11 MAC is to protect the data that it delivers. Because a WLAN generally is not limited to a particular physical area, the IEEE 802.11 MAC provides a privacy service, called Wired Equivalent Privacy (WEP), which encrypts the data sent over the wireless medium. The level of encryption chosen may approximate the level of protection that data may have on a wired LAN that does not allow a physical connection to LAN wiring without authorization.

6.5.2 MAC Frame Exchange Protocol

Because the media used by the IEEE 802.11 WLAN are often very noisy and unreliable, the IEEE 802.11 MAC implements a frame exchange protocol to allow the source of a frame to determine when the frame has been successfully received at the destination. This frame exchange protocol adds some overhead beyond that of other MAC protocols, like IEEE 802.3, because it is not sufficient to simply transmit a frame and expect that the destination has received it correctly on wireless media. In addition, every station in a WLAN cannot necessarily communicate directly with every other station in the WLAN. This leads to a situation known as the hidden node problem. The MAC frame exchange protocol is also designed to address this problem of WLANs. The frame exchange protocol requires the participation of all stations in the WLAN. For this reason, every station decodes and reacts to information in the MAC header of every frame it receives.

6.5.2.1 Handling the Media

The minimal MAC frame exchange protocol consists of two frames: a frame sent from the source to the destination, and an acknowledgment from the destination that the frame was received correctly. The frame and its acknowledgment are an atomic unit of the MAC protocol. As such, they cannot be interrupted by the transmission from any other station.

The destination may not send an acknowledgment because of errors in the original frame, or because the acknowledgment itself was corrupted. If the source does not receive the acknowledgment, the source will attempt to transmit the frame again, according to the rules of the basic access mechanism described below. This retransmission of frames by the source effectively reduces the inherent error rate of the medium, with the cost of additional bandwidth consumption. Without this mechanism for retransmission, the users of the MAC, i.e., higher layer protocols, would be left to determine that their packets had been lost through higher layer timeouts or other means. Since higher layer timeouts are often measured in seconds, it is much more efficient to deal with this issue at the MAC layer.

6.5.2.2 The Hidden Node Problem

A WLAN may suffer from a problem that does not occur on a wired LAN. The problem is one of "hidden nodes." This is a result of the fact that every WLAN station cannot be expected to communicate directly with every other WLAN station. The following example illustrates this problem.

In this example, there are three stations, A, B, and C, arranged as shown in FIG. **67**. Station A can communicate only with station B. Station B can communicate with stations A and C. Station C can communicate only with station B. If a simple "transmit and hope" protocol were to be used when station A was sending a frame to station B, the frame could be corrupted by a transmission begun by station C. Station C would be completely unaware of the ongoing transmission from station A to station B.

The IEEE 802.11 MAC frame exchange protocol addresses this problem by adding two additional frames to the minimal frame exchange protocol described so far. The two frames are a request to send frame and a clear to send frame. The source sends a request to send to the destination. The destination returns a clear to send to the source. Each of these frames contain information that allows other stations receiving them to be notified of the upcoming frame transmission and to delay any transmissions of their own. The request to send and clear to send frames serve to announce to all stations in the neighborhood of both the source and destination the impending transmission from the source to the destination. When the source receives the clear to send from the destination, the real frame that the source wants delivered to the destination is sent. If that frame is correctly received at the destination, the destination will return an acknowledgment, completing the frame exchange protocol. Depending on the configuration of a station and its determination of local conditions, a station may choose when to use the request to send and clear to send frames. See FIG. **68**.

The four frames in this exchange are also an atomic unit of the MAC protocol. They cannot be interrupted by the transmissions of other stations. If this frame exchange fails at any point, the state of the exchange and the information carried in each of the frames allows the stations that have

received these frames to recover and regain control of the medium in a minimal amount of time. A station in the neighborhood of the source station receiving the request to send frame will delay any transmissions of its own until it receives the frame announced by the request to send. If the announced frame is not detected, the station may use the medium. Similarly, a station in the neighborhood of the destination station receiving the clear to send frame will delay any transmissions of its own until it receives the acknowledgment frame. If the acknowledgment frame is not detected, the station may use the medium.

In the source station, a failure of the frame exchange protocol causes the frame to be retransmitted. This is treated as a collision, and the rules for scheduling the retransmission are described in the section on the basic access mechanism, below. To prevent the MAC from being monopolized attempting to deliver a single frame, there are retry counters and timers to limit the lifetime of a frame.

While this four-way frame exchange protocol is a required function of the MAC, it may be disabled by an attribute in the management information base (MIB). The value of the dot11RTSThreshold attribute defines the length of a frame that is required to be preceded by the request to send and clear to send frames. All frames of a length greater than the threshold will be sent with the four-way frame exchange. Frames of a length less than or equal to the threshold will not be preceded by the request to send and clear to send. This allows a network designer to tune the operation of the IEEE 802.11 WLAN for the particular environment in which it is deployed. In an environment with low demand for bandwidth or where the stations are concentrated in an area where all are able to receive the transmissions of every station, the threshold may be set so that the request to send and clear to send are never used. As long as stations are not contending with each other, the request to send and clear to send frames will most often be consuming bandwidth for no measurable gain. This is the default setting for the threshold. In an environment where there is a significant demand for the bandwidth available in the WLAN or where the stations are distributed such that some may not hear the transmission of others, the threshold may be set lower, causing long frames to use the request to send and clear to send frame exchange. The value to which the threshold should be set is arrived at by comparing the bandwidth lost to the additional overhead of the protocol to the bandwidth lost from transmissions being corrupted by hidden nodes. A typical value for the threshold is 128. However, the value chosen is dependent on the data rate and should be calculated for the particular data rate in use. It is rarely necessary to change the value of dot11RTSThreshold from the default value in an AP. By definition, an AP is heard by all stations in its BSS and will never be a hidden node. The only situation that may warrant changing the value for the RTS threshold in an AP is when APs are co-located and sharing a channel.

Timing intervals are described in the following subsection. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on MAC frame exchange protocol.

6.5.2.3 Timing Intervals

The decision by a station that the medium in not carrying a transmission when the station is listening before beginning its own transmission is based on timing intervals. The IEEE 802.11 MAC recognizes five timing intervals. There are two basic intervals determined by the PHY: the short interframe space (SIFS) and the slot time. Three additional intervals are built from the two basic intervals: the priority interframe space (PIFS), the distributed interframe space (DIFS), and the extended interframe space (EIFS). The SIFS is the shortest interval, followed by the slot time, which is slightly longer. The PIFS is equal to SIFS plus one slot time. The DIFS is equal to the SIFS plus two slot times. The EIFS is much larger than any of the other intervals. It is used when a frame that contains errors is received by the MAC, allowing the possibility from the MAC frame exchanges to complete correctly before another transmission is allowed. Through these five timing intervals, both the distributed coordination function (DCF) and point coordination function (PCF) are implemented.

6.5.3 Frame Formats

The IEEE 802.11 MAC accepts MSDUs from higher layers in the protocol stack for the purpose of reliably sending those MSDUs to the equivalent layer of the protocol stack in another station. To accomplish this task, the MAC adds information to the MSDU in the form of headers and trailers to create a MAC protocol data unit (MPDU). The MPDU is then passed to the physical layer to be sent over the wireless medium to the other stations. In addition, the MAC may fragment MSDUs into several frames, increasing the probability of each individual frame being delivered successfully. A discussion of fragmentation follows the description of frame formats in this chapter.

The header and trailer information, combined with the information received as the MSDU, is referred to as the MAC frame. This frame contains, among other things, addressing information, IEEE 802.11-specific protocol information, information for setting the NAV, and a frame check sequence for verifying the integrity of the frame. Further details of the frame format are presented in the following sections.

6.5.3.1 General Frame Format

The general IEEE 802.11 frame format is shown in FIG. **69**. This frame format is quite a bit more complex than that for most other LAN protocols. The frame begins with a MAC header. The start of the header is the frame control field. A field that contains the duration information for the NAV or a short identifier follows it. Three addressing fields follow that field. The next field contains frame sequence information. The final field of the MAC header is the fourth address field. It may appear that the MAC header is very long. However, not all of these fields are used in all frames.

Following the MAC header is the frame body. The frame body contains the MSDU from the higher layer protocols. The final field in the MAC frame is the frame check sequence.

Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on each of the general frame format fields, and their use in particular frame types.

6.5.4 Control Frame Subtypes

There are six control frame subtypes: request to send (RTS), clear to send (CTS), acknowledge (ACK), power save poll (PS-Poll), contention-free end (CF-End), and contention-free end plus ACK (CF-End+ACK). A description of these frames follows.

6.5.4.1 Request to Send

The request to send (RTS) frame is 20 bytes in length. It comprises the frame control field, the duration/ID field, two address fields and the frame check sequence field. The purpose of this frame is to transmit the duration information to those stations in the neighborhood of the transmitter, in order that the stations receiving the RTS frame will update their NAV to prevent transmissions from colliding with the data or management frame that is expected to follow. The

RTS is also the first frame in a four-way frame exchange handshake between the transmitter and the receiver. See FIG. **70**.

The RA identifies the individual MAC that is the immediate intended recipient of the frame. In an RTS frame, the RA is always an individual address. The TA identifies the source of the transmission. It is used by the station addressed by the RA to form the clear to send (CTS) frame that is the response to the RTS. The duration information conveyed by this frame is a measure of the amount of time required to complete the four-way frame exchange. The value of the duration is the length of time to transmit a CTS, the data or management frame, the acknowledge (ACK) frame, and the two SIFS intervals between the CTS and the data or management frame and between the data or management frame and the ACK. The duration is measured in microseconds. Fractional microseconds are always rounded up to the next larger integer value.

6.5.4.2 Clear to Send

The clear to send (CTS) frame is 14 bytes in length. It comprises the frame control field, the duration/ID field, one address field, and the frame check sequence field. The purpose of this frame is to transmit the duration information to those stations in the neighborhood of the station intended to receive the expected data or management frame, in order that the stations receiving the CTS frame will update their NAV to prevent transmissions from colliding with the data or management frame that is expected to follow. The CTS is the second frame in a four-way frame exchange handshake between the transmitter and the receiver. See FIG. **90**.

The RA identifies the individual MAC address of the station to which the CTS is sent. In the CTS frame, the RA is always an individual address.

The RA value is taken directly from the TA of the preceding RTS frame. The duration information conveyed by this frame is a measure of the time required to complete the four-way frame exchange handshake. The value of the duration is the length of time to send the subsequent data or management frame, the acknowledge frame, and one SIFS interval. The duration value is calculated by subtracting the length of time to transmit a CTS and one SIFS interval from the duration that was received in the WFS frame. The duration is measured in microseconds. Fractional microseconds are always rounded up to the next larger integer value.

6.5.4.3 Acknowledge

The acknowledge (ACK) frame is 14 bytes in length. It comprises the frame control field, the duration/ID field, one address field and the frame check sequence field. The purpose of this frame is two-fold. First, the ACK frame transmits an acknowledgment to the sender of the immediately previous data, management, or PS-Poll frame that the frame was received correctly. This informs the sender of the frame of the frame's receipt and eliminates the requirement for retransmission by the sender. Second, the ACK frame is used to transmit the duration information for a fragment burst to those stations in the neighborhood of the station intended to receive the fragments. In this case, it performs exactly as the CTS frame. The ACK frame is the fourth frame in the four-way frame exchange handshake between transmitter and receiver. See FIG. **91**.

The RA identifies the individual MAC address of the station to which the ACK is sent. In the ACK frame, the RA is always an individual address. The RA value is taken directly from the address **2** field of the immediately preceding data, management, or PS-Poll frame.

The value of the duration information is zero, if the ACK is an acknowledgment of a PS-Poll frame or is an acknowledgment of a management or data frame where the more fragments subfield of the frame control field is zero. The value of the duration information is the time to transmit the subsequent data or management frame, an ACK frame, and two SIFS intervals, if the acknowledgment is of a data or management frame where the more fragments subfield of the frame control field is one. In the latter case, the duration may be calculated by subtracting the length of time to transmit the ACK frame and one SIFS interval from the duration value received in the immediately preceding data or management frame. The duration value is measured in microseconds. Fractional microseconds are always rounded up to the next integer value.

6.5.4.4 Power Save Poll

The power save poll (PS-Poll) frame is 20 bytes in length. It comprises the frame control field, the duration/ID field, two address fields, and the frame check sequence field. The purpose of this frame is to request that an AP deliver a frame that has been buffered for a mobile station while it was in a power saving mode.

The BSSID identifies the AP to which this frame is directed. This BSSID should be the same BSSID as that to which the sending station has previously associated. The BSSID in the PS-Poll frame is always an individual address. The TA is the MAC address of the mobile station that is sending the PS-Poll frame. The duration/ID value is the AID value that was given to the mobile station upon association with the BSS. Even though this frame does not include any explicit duration information, every mobile station receiving a PS-Poll frame will update its NAV with a value which is the length of time to transmit an ACK frame and a single SIFS interval. This action allows the ACK frame that follows the PS-Poll to be sent by the AP with a very small probability. that it will collide with frames from mobile stations.

For the AP response to this frame, refer to Chapter 4 of the IEEE 802.11 Handbook.

6.5.4.5 CF-End and CF-End+ACK

The CF-End and CF-End+ACK frames are 20 bytes in length. Each frame comprises the frame control field, the duration/ID field, two address fields, and the frame check sequence field. The purpose of these frames is to conclude a CFP and to release stations from the restriction imposed during a CFP, preventing competition for access to the medium. Additionally, the CF-End+ACK frame is used to acknowledge the last transmission received by the PC. This frame is sent by the PC as the last frame in the CFP.

The RA is the broadcast group address, as this frame is intended to be received by every station in the BSS. The BSSID is the MAC address of the AP, where the PC resides. The duration value is zero, ensuring that the NAVs of all stations receiving this frame will be reset to zero.

6.5.5 Data Frame Subtypes

There are eight data frame subtypes in two groups. The first group is simple data, data with contention-free acknowledgment (CF-ACK), data with CF-Poll, and data with CF-ACK and CF-Poll. The second group is null function, CF-ACK, CF-Poll, and CF-ACK+CF-Poll. The first group of data frames carry a nonzero number of data bytes. The second group of data frames carry no data bytes at all.

The data frame is variable in length. The minimum length of the data frame is 29 bytes. The maximum length of the frame is 2346 bytes. The data frame carries the MSDU requested to be delivered by the upper layer protocols. It comprises the frame control field, the duration/ID field, up to four address fields, the sequence control field, the frame body field and the frame check sequence field. See FIG. **92**

for a data frame. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on the data frame.

6.5.6 Management Frame Subtypes

IEEE 802.11 is different from many of the other IEEE 802 standards because it includes very extensive management capabilities defined at the MAC level. One of the four MAC frame types is dedicated to management frames. There are 11 distinct management frame types. All management frames include: frame control, duration, address **1**, **2**, and **3**, sequence control, framebody and frame check sequence (FCS) fields.

The frame body of a management frame carries information in both fixed fields and in variable length information elements that are dependent on subtype. The information element is a flexible data structure that contains an information element identifier, a length, and the content of the information element. Information elements occur in the frame body in order of increasing identifiers. This arrangement and the data structure itself allow for the flexible extension of the management frames to include new functionality without affecting older implementations. This can be done because older implementations will be able to understand the older elements and will ignore elements with new identifiers. Because the length of the element is part of the data structure, an older implementation can skip over newer elements without needing to understand the content of the element. See FIG. **93** for an information element. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on the fixed fields and information elements.

6.5.7 Components of the Management Frame Body

The components of the management frame body comprise fixed fields and variable length information elements. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on these fixed fields and information elements.

6.5.8 MAC Management

IEEE 802.11 is the first LAN standard by the IEEE 802 committee that includes significant management capabilities. This is because an IEEE 802.11 WLAN must deal with an environment that is measurably more complex than those of the wired LAN standards of IEEE 802. A major challenge for the IEEE 802.11 WLAN is that the medium is not a wire. This leads to many difficulties that IEEE 802.11 must overcome in order to offer the same reliable service expected of an IEEE 802 LAN.

Because the media over which the IEEE 802.11 WLAN operate are not wires, the media are shared by other users that have no concept of data communication or sharing the media. An example of this type of user is the common microwave oven. The microwave oven operates in the 2.4 GHz ISM band because one excitation frequency of the water molecule lies in this band. Another user in this same band is the radio frequency ID (RFID) tag. RFID tags are usually small, cheap, unpowered devices that receive their power from a microwave beam and then return a unique identifier. RFID tags are used to track retail inventory, identify rail cars, and many other uses. An unfortunate consequence of these devices sharing the band with WLANs is that some of this microwave energy leaks from the oven and is purposely broadcast for RFID tags, thus, interfering with the operation of the WLAN.

There are also other WLANs than IEEE 802.11 that share the media. This would be somewhat equivalent to attempting to run IEEE 802.3, IEEE 802.5, IEEE 802.12, and fiber distributed data interference (FDDI) on the same twisted pair cable, simultaneously. These other WLAN users of the media are often uncoordinated with IEEE 802.11 and, in most cases, do not provide for any mechanism to share the media at all. Finally, there are other IEEE 802.11 WLANs sharing the media.

These other users of the media result in a first challenge for the IEEE 802.11 WLAN, an intermittent connection to the media and other stations of the IEEE 802.11 WLAN. Much of the management specified in IEEE 802.11 is to deal with the intermittent nature of the media.

A second challenge to be dealt with by an IEEE 802.11 WLAN is that anyone can "connect" to the WLAN, simply by erecting the proper antenna. This leads to the need to identify the stations connecting to the WLAN, in order to allow only authorized stations to use the WLAN, and to the need to protect the information sent over the WLAN from improper interception.

A third challenge to be dealt with by an IEEE 802.11 WLAN is mobility. Once the wires are removed from a LAN, the natural thing to do is to pick up the equipment connected to the LAN and move it around, taking it from an office to a conference room or to another building. Thus, IEEE 802.11 equipment is not always in the same place from one moment to the next. Even if the equipment were to remain in a fixed location, the nature of the wireless media may make it appear as if the equipment has moved. Dealing with mobility while making all of the expected LAN services available is a problem to be solved by MAC management.

One final challenge to be dealt with by an IEEE 802.11 WLAN is power management. A consequence of doing away with wired media and enabling the equipment to be mobile is that much of the equipment will be run on batteries. Conserving the energy stored in the batteries to allow the equipment to operate for as long as possible must be built into the WLAN protocol and controlled by MAC management.

6.5.8.1 Tools Available to Meet the Challenges

The IEEE 802.11 standard defines a number of MAC management capabilities that are designed to meet the challenges of operating a reliable WLAN. These tools are: authentication, association, address filtering, privacy, power management, and synchronization. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on each of these tools.

6.5.9 MAC Management Information Base

The IEEE 802.11 management information base (MIB) is an SMNPv2 managed object that contains a number of configuration controls, option selectors, counters, and status indicators that allow an external management agent to determine the status and configuration of an IEEE 802.11 station, as well as to probe its performance and tune its operation. The MIB in a station comprises two major sections, one for the MAC and one for the PHY. The PHY section is subdivided into pieces that are specific to each PHY layer. In the MIB definition, there is also a compliance section that describes the required portions of the MIB and those parts that are optional. All of the attributes are arranged in tables, coordinating the attributes that are related to a single function.

The MAC MIB comprises two sections: the station management attributes and the MAC attributes. The station management attributes are associated with the configuration of options in the MAC and the operation of MAC management. The MAC attributes are associated with the operation of the MAC and its performance.

6.5.9.1 Station Management Attributes

The station management attributes configure and control the operation of the options of the IEEE 802.11 MAC, as

well as assist in the management of the station. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on these attributes.

6.5.9.2 MAC Attributes

The MAC attributes tune the performance of the MAC protocol, monitor the performance of the MAC, identify the multicast addresses that the MAC will receive, and provide identification of the MAC implementation. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on these attributes.

6.6 Physical Layer (PHY)

Embodiments of the PHY are provided in the following sections for receiving, transmitting, modulating, and/or demodulating WLAN signals, according to the present invention. These embodiments are applicable to WLAN stations, APs, and further WLAN related communications components. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.6.1 PHY Functionality

At the bottom of the OSI stack is the PHY. FIG. **128**A illustrates an OSI model 12800 including the PHY layer **12802**. The PHY **12802** is an interface between the MAC **12804** and wireless media. The PHY **12802** transmits and receives data frames over the shared wireless media. The PHY **12802** provides three levels of functionality. First, the PHY layer **12802** provides a frame exchange between the MAC **12804** and PHY **12802** under the control of a physical layer convergence procedure (PLCP) sublayer **12806**. Second, the PHY **12802** uses signal carrier and spread spectrum modulation to transmit data frames over the media under the control of a physical medium dependent (PMD) sublayer **12808**. Third, the PHY **12802** provides a carrier sense indication back to the MAC **12804** to verify activity on the media.

The PHY layers are unique in terms of modulation type, coexist with the other PHYs, and operate with the MAC described above. The specifications for IEEE 802.11 were selected to meet the radio frequency (RF) emissions guidelines specified by the Federal Communications Commission (FCC), European Telecommunications Standards Institute (ETSI), and Ministry of Telecommunications (MKK). The following sections provide an overview of the specifications for each type of PHY layer.

6.6.1.1 PMD Incorporating Universal Frequency Translation Technology

In the PHY layers of embodiments of the present invention, the PMD sublayer **12808** incorporates universal frequency translation technology to provide for frequency translation of transmitted and received WLAN communication signals. Universal frequency translation technology may be incorporated in transmitters, receivers, and transceivers in PMD sublayer **12808**. As shown in FIG. **128**B, PMD sublayer **12808** comprises one or more UFT modules **12810** in an embodiment. UFT module **12810** may be configured to provide for signal frequency up-conversion or down-conversion. One or more UFT modules **12810** may provide for carrier signal modulation with an information signal, and/or de-modulation, according a variety of modulation schemes. These modulation schemes include but are not limited to amplitude modulation (AM), frequency modulation (FM), or phase modulation (PM), including ASK, FSK, GFSK (Gaussian frequency shift keying), PSK, and DBPSK (differential binary phase shift keying), and combinations thereof. PMD sublayer **12808** may comprise one or more UFT modules for frequency translation of one or more signals. For example, two or more UFT modules may be configured to provide for, or assist in, I/Q modulation or demodulation of signals according to a variety of I/Q modulation schemes, including quadrature amplitude modulation (QAM), differential quadrature phase shift keying (DQPSK), quadrature phase shift keying (QPSK), complementary code keying (CCK), and packet binary convolutional coding (PBCC) modulation schemes. Systems and methods for handling these modulation schemes are further described herein. The UFT module of the present invention may be configured to accommodate further modulation schemes described elsewhere herein or otherwise known to persons skilled in the relevant art(s).

As shown in FIG. **128**C, PMD sublayer **12808** may include one or more UFU modules **12812**. UFU module **12812** comprises at least one UFT module **12810**. Numerous embodiments for frequency up-converting and/or modulating signals via UFU module **12812** in PMD sublayer **12808** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

As shown in FIG. **128**C, PMD sublayer **12808** may include one or more UFD modules **12814**. UFD module **12814** comprises at least one UFT module **12816**. Numerous embodiments for frequency down-converting and/or demodulating signals via UFD module **12814** in PMD sublayer **12808** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

As shown in FIG. **128**D, PMD sublayer **12808** includes one or more UFU modules **12812** and one or more UFD modules **12814**, which share one or more UFT modules **12812**. UFU module **12812** and UFD module **12814** may share UFT module **12812**, and/or share other components. Numerous embodiments for frequency up-converting signals and down-converting signals via UFU module **12812** and UFD module **12814** when sharing components will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

Frequency translation via universal frequency translation technology is described in further detail below, in regards to a variety of IEEE Std. 802.11 PHY layers.

6.6.2 Direct Sequence Spread Spectrum (DSSS) PHY

A DSSS PHY is one of the three PHY layers supported in the standard. The DSSS PHY uses the 2.4 GHz frequency band as the RF transmission media. Data transmission over the media is controlled by the DSSS PMD sublayer as directed by the DSSS PLCP sublayer. The DSSS PMD receives binary bits of information from the PLCP protocol data unit (PPDU) and transforms them into RF signals for the wireless media by using carrier modulation and DSSS techniques. FIG. **129**A illustrates an exemplary DSSS PMD transmitter **12900**. FIG. **129**B illustrates an exemplary DSSS PMD receiver **12902**. The DSSS PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and de-modulation, as described in subsequent sub-sections.

6.6.2.1 DSSS PLCP Sublayer

A PLCP protocol data unit (PPDU) is unique to the DSSS PHY layer. FIG. **130** illustrates a PPDU frame **13002**. PPDU frame **13002** includes a PLCP preamble **13004**, PLCP header **13006**, and MAC protocol data unit (MPDU) **13008**. The receiver **12902** uses the PLCP preamble **13004** to acquire the incoming signal and synchronize the demodu-

lator. The PLCP header **13006** includes information about the MPDU **13008** from the sending DSSS PHY. The PLCP preamble **13004** and PLCP header **13006** are typically transmitted at 1 Mbps, and the MPDU **13008** can be sent at 1 Mbps or 2 Mbps. The segments of the PPDU frame **13002** illustrated in FIG. **130** are described below:

SYNC: This field is 128 bits (symbols) in length and contains a string of 1's which are scrambled prior to transmission. The receiver uses this field to acquire the incoming signal and synchronize the receiver's carrier tracking and timing prior to receiving the start of frame delimiter (SFD).

Start of frame delimiter (SFD): This field contains information marking the start of a PPDU frame. The SFD specified is common for all IEEE 802.11 DSSS radios and uses the following hexadecimal word: F3A0hex.

Signal: The signal field defines which type of modulation must be used to receive the incoming MPDU. The binary value in this field is equal to the data rate multiplied by 100 kbit/s. In the June 1997 version of IEEE 802.11, two rates are supported: OAh for 1 Mbps DBPSK, and 14hex for 2 Mbps DQPSK.

Service: The service field is reserved for future use. The default value is 00h.

Length: The length field is an unsigned 16-bit integer that indicates the number of microseconds necessary to transmit the MPDU. The MAC layer uses this field to determine the end of a PPDU frame.

CRC: The CRC field contains the results of a calculated frame check sequence from the sending station. The calculation is performed prior to data scrambling. The CCITT CRC-16 error detection algorithm is used to protect the signal, service and length fields. The CRC-16 algorithm is represented by the following polynomial: $G(x)=x^{16}+x^{12}+x^5+1$. The receiver performs the calculation on the incoming signal, service, and length fields and compares the results against the transmitted value. If an error is detected, the receiver's MAC makes the decision whether incoming PPDU should be terminated.

Embedded at the end of the MPDU portion of the PPDU is a field called FCS. This field contains a 32-bit CRC, which protects the information in the PLCP service data unit (PSDU). The DSSS PHY does not determine whether errors are present in the MPDU. The MAC makes that determination in a manner similar to the method used by the PHY layer.

6.6.2.2 Data Scrambling

Information bits transmitted by the DSSS PMD may be scrambled using a self-synchronizing 7-bit polynomial. The scrambling polynomial for the DSSS PHY may be: $G(z)=z^{-7}+z^{-4}+1$. Scrambling is used to randomize the data in the SYNC field of the PLCP and data patterns which contain long strings of binary 1s or 0s. The receiver can descramble the information bits without prior knowledge from the sending station.

6.6.2.3 DSSS Modulation

In the June 1997 version of IEEE 802.11, the DSSS PMD uses differential phase shift keying (DPSK) as the modulation to transmit the PPDU. Two types of DPSK are specified. The DSSS PMD transmits the PLCP preamble and PLCP header at 1 Mbps using differential binary phase shift keying (DBPSK). The MPDU is sent at either 1 Mbps DBPSK or 2 Mbps differential quadrature phase shift keying (DQPSK), depending upon the content in the signal field of the PLCP header.

DPSK is a modulation technique which uses a balanced in-phase/quadrature (I/Q) modulator to generate a RF carrier. The RF carrier is phase modulated with symbols mapped from the binary bits in the PPDU. The symbols contain PPDU information. At the receiving station, data recovery for DPSK is based on the phase differences between two consecutive symbols from the sending station. DPSK is non-coherent, meaning that a clock reference is not needed to recover the data. For 1 Mbps DBPSK, 1 and 0 binary bits in the PPDU constitute phase shifts of 180 degrees and the signal information is contained on the I-phase arm, as shown in constellation pattern **13102** of FIG. **131**. For 2 Mbps DQPSK, two binary bits are combined from the PPDU, generating the following I/Q symbol pairs (00, 01, 11, 10). The phase shifts occur at 90 degrees for DQPSK, as shown in constellation pattern **13104** in FIG. **131**. DQPSK is substantially similar to transmitting two 1 Mbps DBPSK signals, one on the I-phase, the other on the Q-phase. DBPSK is more tolerant to intersymbol interference caused by noise and multipath over the media; therefore DBPSK is generally used for the PLCP preamble.

For IEEE 802.11-compliant DSSS products, the rotation of DBPSK and DQPSK modulated symbols spinning about the I/Q constellation is counterclockwise. This is noteworthy because it is common to develop DSSS WLAN products that rotate in the opposite direction. This rotation is illustrated in FIG. **131**.

6.6.2.4 Barker Spreading Method

The DSSS PHY layer is one of the two 2.4 GHz RF PHY layers to choose from in the IEEE 802.11 standard. Direct Sequence is the spreading method used. An 11-bit Barker word may be used as the spreading sequence. Every station in an IEEE 802.11 network uses the same 11-bit sequence. A Barker word sequence is classified as a short sequence, and is known to have very good correlation properties.

Barker word (11-bits)+1, −1, +1, +1, −1, +1, +1, +1, −1, −1, −1

In a transmitter, the 11-bit Barker word may be applied to a modulo-2 adder (XOR function) together with each of the information bits in the (scrambled) PPDU, as shown in FIG. **132**A. The PPDU is clocked at the information rate, for example, 1 Mbps, and the 11-Barker word is clocked at 11 Mbps (the chipping clock rate). The XOR function combines the signals by performing a modulo-2 addition on each PPDU bit with each Barker word bit (sometimes referred to as a chip). The output of the modulo-2 adder is a signal with a data rate that is 10×higher than the information rate. The result in the frequency domain is a signal that is spread over a wider bandwidth than the information signal, at a reduced RF power level. FIG. **132**B illustrates an exemplary transmitter baseband signal before spreading **13202**. FIG. **132**C illustrates an exemplary transmitter baseband signal after spreading. At the receiver, the DSSS signal is convolved with the 11-bit Barker word and correlated. The correlation operation recovers the PPDU information bits at the transmitted information rate, and the undesired interfering in-band signals are spread out-of-band. FIG. **132**D illustrates an exemplary receiver baseband signal before correlation. FIG. **132**E illustrates an exemplary receiver baseband signal after correlation. The spreading and despreading of narrowband to a wideband signal is commonly referred to as processing gain, and is measured in decibels (0). Processing gain is the ratio of the DSSS signal rate to the PPDU information rate. The FCC and MKK specify the minimum requirement for processing gain as 10 dB in North America and Japan.

The Barker word used in IEEE 802.11 is different from the spreading codes used in code division multiple access (CDMA) and global positioning system (GPS). CDMA and

GPS use orthogonal spreading codes, which allow multiple users to operate on the same channel frequency. CDMA codes can have longer sequences and have richer correlation properties.

6.6.2.5 DSSS Operating Channels and Transmit Power Requirements

Each DSSS PHY channel occupies 22 MHZ of bandwidth, and the spectral shape of the channel represents a filtered SinX/X function, as shown in FIG. **133**. The DS channel transmit mask in IEEE 802.11 specifies that spectral products be filtered to −30 dBr from the center frequency and all other products be filtered to −50 dBr. This allows for three non-interfering channels spaced 25 MHZ apart in the 2.4 GHz frequency band. For example, the channel arrangement for North America is illustrated in FIG. **134**. With this channel arrangement, a user can configure multiple DSSS networks to operate simultaneously in the same area.

In IEEE 802.11 fourteen center frequency channels are defined for operation across the 2.4 GHz frequency band (see Table 1). In North America, twelve channels are allowed, ranging from 2.412 GHz to 2.462 GHz. In most of Europe, thirteen channels are allowed, ranging from 2.412 GHz to 2.472 GHz. In Japan, one channel frequency is reserved at 2.483 Ghz.

TABLE 1

Channel Number	Frequency GHz	North America	Europe	Spain	France	Japan-MKK
1	2.412	X	X			
2	2.417	X	X			
3	2.422	X	X			
4	2.427	X	X			
5	2.432	X	X			
6	2.437	X	X			
7	2.442	X	X			
8	2.447	X	X			
9	2.452	X	X			
10	2.457	X	X	X	X	
11	2.462	X	X	X	X	
12	2.467		X		X	
13	2.472		X		X	
14	2.483					X

In addition to frequency and bandwidth allocations, transmit power is a key parameter that is regulated worldwide. The maximum allowable radiated emissions for the DSSS PHY varies from region to region, as illustrated in Table 2. The transmit power is directly related to the range that a particular IEEE 802.11 DSSS PHY implementation can achieve. 100 mW is the nominal RF transmit power level for many of the IEEE 802.11 DSSS PHY wireless products on the market today.

TABLE 2

1000 mW	North America
100 mW	Europe
10 mW/MHZ	Japan

6.6.20.6 DSSS PMD Incorporating Universal Frequency Translation Technology

In embodiments, the DSSS PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the DSSS PMD may comprise one or more UFT modules, such as UFT module **128310** of FIG. **128**B, that provide for these functions. Furthermore, the DSSS PMD may comprise one or more UFU modules such as UFU module **12812** of FIG. **128**C, and/or one or more UFD modules such as UFD module **12814** of FIG. **128**C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The DSSS PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to DBPSK and DQPSK modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for DSSS PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the DSSS PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.6.2.6.1 Transmit DSSS PMD Incorporating Universal Frequency Translation

As shown in FIG. **129**A, transmit DSSS PMD **12900** comprises a scrambler **12904**, a spreader **12906**, a transmit mask filter **12908**, a DPSK modulation transmitter **12910**, and an antenna **12912**. The structure and operation of transmit DSSS PMD **12900** will be further described as follows, and is further described elsewhere herein.

Scrambler **12904** receives a PPDU signal **12914**. In embodiments, PPDU signal **12914** comprises one or more whole PPDU frames and/or portions of PPDU frames. For example, in DSSS PMD embodiments transmitting according to DBPSK modulation, PPDU signal **12914** may comprise a PLCP preamble, a PLCP header, and/or an MPDU. In DSSS PMD embodiments transmitting according to DQPSK modulation, PPDU signal **12914** may comprise an MPDU. In alternate embodiments, the DSSS PMD PLCP preamble, PLCP header, and MPDU may be modulated according to any of the modulation schemes described herein.

Scrambler **12904** scrambles the PPDU signal **12914**, and outputs a scrambled PPDU signal **12916**. The design and use of a scrambler **12904** is well known to those skilled in the relevant art(s). A suitable scrambler **12904** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Spreader **12906** receives scrambled PPDU signal **12916**. Spreader **12906** spreads the frequency spectrum of scrambled PPDU signal **12916**, and outputs spread signal **12920**. Spreader **12906** as shown in FIG. **129**A is implemented as a modulo −2 adder, but other implementations are within the scope of the present invention. The design and use of a spreader **12906** is well known to those skilled in the relevant art(s). A suitable spreader **12906** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmit mask filter **12908** receives spread signal **12920**. Transmit mask filter **12908** filters spread signal **12920**, and outputs filtered signal **12922**. The design and use of a transmit mask filter **12908** is well known to those skilled in the relevant art(s). A suitable transmit mask filter **12908** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

DPSK modulation transmitter **12910** receives filtered signal **12922**. DPSK modulation transmitter **12910** modulates an oscillating signal with filtered signal **12922** accord-

ing to DBPSK modulation or DQPSK modulation, and frequency up-converts filtered signal **12922**. DPSK modulation transmitter **12910** outputs transmitted modulated signal **12924**, which is transmitted by antenna **12912**.

The transmit DSSS PMD **12900** of FIG. **129**A may incorporate universal frequency translation technology to provide for modulation and frequency up-conversion of WLAN station signals. FIG. **129**C illustrates an exemplary embodiment of the DPSK modulation transmitter **12910** of FIG. **129**A. Transmitter **12910** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitter **12910** of FIG. **129**C comprises at least one UFT module **12810**. UFT module **12810** provides for modulation and frequency up-conversion of WLAN station signals to be transmitted. As described above, transmit DSSS PMD **12900** transmits the PLCP preamble and PLCP header at 1 Mbps using DBPSK, and the MPDU is sent at either 1 Mbps DBPSK or at 2 Mbps DQPSK, depending on the content in the signal field of the PLCP header. Numerous embodiments for transmitter **12910** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for transmitter **12910** incorporating UFT module **12810** are further described below and elsewhere herein.

6.6.2.6.1.1 UFU Module Transmitter Embodiments for DBPSK Modulation

FIG. **129**D illustrates in greater detail an exemplary embodiment of transmitter **12910** of FIG. **129**A. Transmitter **12910** comprises a DBPSK modulator **12946**, a UFU module **12812**, and an optional amplifier **12948**.

DBPSK modulator **12946** of transmitter **12910** receives a filtered signal **12922**. DBPSK modulator **12946** modulates filtered signal **12922**, according to differential binary phase shift keying (DBPSK) modulation. For example, DBPSK modulator **12946** may DBPSK modulate an oscillating signal using filtered signal **12922**. DBPSK modulation is well known to persons skilled in the relevant art(s). DBPSK modulator **12946** outputs modulated signal **12950**. The design and use of a DBPSK modulator **12946** is well known to those skilled in the relevant art(s). A suitable DBPSK modulator **12946** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Modulated signal **12950** is received by UFU module **12812**. UFU module **12812** includes at least one UFT module **12810**. UFU module **12812** frequency up-converts modulated signal **12950**, and outputs UFU module output signal **12952**. Various structures and methods for operation of UFU module **12812** are described more fully elsewhere herein. The following subsection provides a structural and operational description of an embodiment of UFU module **12812**.

When present, optional amplifier **12948** amplifies UFU module output signal **12952**, outputting transmitted modulated signal **12924**. Transmitted modulated signal **12924** comprises a DBPSK modulated signal.

Phase modulation techniques and other modulation techniques are more fully described in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, the full disclosure of which is incorporated herein by reference in its entirety.

6.6.2.6.1.1 Detailed UFU Module Embodiment

FIG. **129**E illustrates a more detailed exemplary circuit diagram of an embodiment of UFU module **12812**. UFU module **12812** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

UFU module **12812** comprises a pulse-shaping circuit **12954**, a first reference potential **12956**, a filter **12958**, a second reference potential **12960**, a resistor **12962**, and a UFT module **12810**.

In FIG. **129**E, pulse shaping circuit **12954** receives modulated signal **12950**. Pulse shaping circuit **12954** outputs control signal **12964**, which is preferably comprised of a string of pulses. Control signal **12964** controls UFT module **12810**, which preferably comprises a switch. Various embodiments for UFT module **12810** are described above. One terminal of UFT module **12810** is coupled to a first reference potential **12960**. The second terminal of UFT module **12810** is coupled through resistor **12962** to a second reference potential **12956**. In a PM or PSK modulation embodiment, second reference potential **12956** is preferably a constant voltage level.

The output of UFT module **12810** is a harmonically rich signal **12966**. Harmonically rich signal **12966** has a fundamental frequency and phase substantially proportional to control signal **12964**, and an amplitude substantially proportional to the amplitude of second reference potential **12956**. Each of the harmonics of harmonically rich signal **12966** also have phase proportional to control signal **12964**, and in a PM or PSK embodiment are thus considered to be PM or PSK modulated.

Harmonically rich signal **12966** is received by filter **12958**. Filter **12958** preferably has a high Q. Filter **12958** preferably selects the harmonic of harmonically rich signal **12966** that is at the approximate frequency desired for transmission. Filter **12958** removes the undesired frequencies that exist as harmonic components of harmonically rich signal **12966**. Filter **12958** outputs UFU module output signal **12952**.

Further details pertaining to UFU module **12812** are provided in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, which is incorporated herein by reference in its entirety.

6.6.2.6.1.2 DBPSK Balanced Modulator Transmitter Embodiments

Balanced modulator transmitter configurations are presented in Section 3.1. These transmitter configurations may be applied in transmitter **12910** to modulate and frequency up-convert WLAN station signals according to DBPSK modulation techniques. The balanced modulator transmitter configurations presented above and applicable to transmitter **12910** include transmitter **7102** of FIG. **71**A, transmitter **7162** of FIG. **71**D, transmitter **7302** of FIG. **73**A, and transmitter **7900** of FIG. **79**A. Refer to Section 3.1 above for detailed description of these transmitters. Further details pertaining to balanced modulator transmitters are provided in co-pending U.S. patent application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. **129**F illustrates balanced modulator embodiments for transmitter **12910**, according to the present invention. Transmitter **12910** comprises a DBPSK modulator **1295 68** and a transmitter **7102**, **7162**, **7302**, **7900**. The design and

use of a DBPSK modulator **12968** is well known to those skilled in the relevant art(s). A suitable DBPSK modulator **12968** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "offthe shelf."

DBPSK modulator **12968** receives filtered signal **12922**. DBPSK modulator **12968** produces an oscillating signal modulated with filtered signal **12922** according to DBPSK modulation. DBPSK modulator **12968** outputs DBPSK modulated signal **12970**.

Transmitter **7102**, **7162**, **7302**, **7900** receives DBPSK modulated signal **12970**. DBPSK modulated signal **12970** of FIG. **129**F corresponds to baseband signal **7110** of FIGS. **71**A and **71**D, baseband signal **7306** of FIG. **73**A, and baseband signal **7902** of FIG. **79**A. Transmitter **7102**, **7162**, **7302**, **7900** may be one of transmitter **7102** of FIG. **71**A, transmitter **7162** of FIG. **71**D, transmitter **7302** of FIG. **73**A, and transmitter **7900** of FIG. **79**A, and other balanced modulator transmitter of the present invention described herein. The one of transmitters **7102**, **7162**, **7302**, **7900** selected for a particular implementation of transmitter **12910** will depend on the particular application. Transmitter **7102**, **7162**, **7302**, **7900** frequency up-converts DBPSK modulated signal **12970**, and outputs transmitted modulated signal **12924**. Transmitted modulated signal **12924** of FIG. **129**F corresponds to output signal **7140** of FIGS. **71**A and **71**D, output signal **7322** of FIG. **73**A, and output signal **7936** of FIG. **79**A. Transmitted modulated signal **12924** comprises a DBPSK modulated information signal.

6.6.2.6.1.3 DQPSK Modulation Mode Transmitter Embodiments

Quadrature Phase-Shift Keying (QPSK) is a well known I/Q modulation technique for modulating digital signals using four phase states to code two digital bits per phase shift. An in-phase signal ("I") is modulated such that its phase varies as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its phase varies as a function of the other information signal. The two modulated signals are combined to form an "QPSK" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously.

Embodiments are provided below for implementing QPSK transmitters and receivers that may be implemented in WLAN stations, according to embodiment of the present invention. For example, the QPSK transmitters described below may be implemented in transmit DSSS PMD sublayer **12900** to transmit DQPSK modulated WLAN signals. These transmitter embodiments are described herein for purposes of illustration, and not limitation. Alternate transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

In FIG. **129**G, a QPSK modulation mode embodiment is presented. In this embodiment, two information signals are accepted. An in-phase signal ("I") is modulated such that its phase varies as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its phase varies as a function of the other information signal. The two modulated signals are combined to form an "I/Q" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously. Other uses for this type of modulation would be apparent to persons skilled in the relevant art(s).

FIG. **129**G illustrates an exemplary block diagram of a transmitter **12910** operating in an I/Q modulation mode. Transmitter **12910** comprises a signal separator **12972** and a QPSK modulation transmitter **12978**.

Signal separator **12972** separates filtered signal **12922** into two signals: first information signal **12974** and second information signal **12976**. When filtered signal **12922** is a bused signal, signal separator **12972** may merely be a location on the bus where filtered signal **12922** is separated into separate buses or data signals, for instance. Signal separator **12972** may alternatively comprise logic and memory for receiving and storing filtered signal **12922**, and logically dividing it into the two signals. A suitable signal separator **12972** may be designed and implemented in software, firmware, hardware, and any combination thereof.

QPSK modulation transmitter **12978** comprises at least one UFT module **12810**. QPSK modulation transmitter **12978** provides QPSK modulation to first information signal **12974** and second information signal **12976**, outputting transmitted modulated signal **12924**. Numerous embodiments for QPSK modulation transmitter **12978** will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Various embodiments for QPSK modulation transmitter **12978** are provided in the following subsections.

6.6.2.6.1.3.1 QPSK Modulation Transmitter Using Two UFU Modules

FIG. **129**H illustrates a more detailed circuit block diagram for QPSK modulation transmitter **12978**. QPSK modulation transmitter **12978** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

QPSK modulation transmitter **12978** comprises a first UFU module **12982**, a second UFU module **12984**, an oscillator **12988**, a phase shifter **12990**, a summer **12992**, a first UFT module **12986**, a second UFT module **12973**, a first DBPSK modulator **12909**, a second DBPSK modulator **12980**, and a filter **12994**.

Oscillator **12988** generates an "I"-oscillating signal **12996**.

A first information signal **12974** is input to first DBPSK modulator **12909**. The "I"-oscillating signal **12996** is modulated by first information signal **12974** in the first DBPSK modulator **12909**, thereby producing an "I"-modulated signal **12901**.

First UFU module **12982** inputs "I"-modulated signal **12901**, and generates a harmonically rich "I" signal **12903** with a continuous and periodic wave form.

The phase of "I"-oscillating signal **12996** is shifted by phase shifter **12990** to create "Q"-oscillating signal **12998**. Phase shifter **12990** preferably shifts the phase of "I"-oscillating signal **12996** by 90 degrees.

A second information signal **12976** is input to second DBPSK modulator **12980**. "Q"-oscillating signal **12998** is modulated by second information signal **12976** in second DBPSK modulator **12980**, thereby producing a "Q" modulated signal. The design and use of a first and second DBPSK modulator **12909** and **12980** is well known to those skilled in the relevant art(s). A suitable first and second DBPSK modulator **12909** and **12980** may be designed and imple-

mented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf."

Second UFU module **12984** inputs "Q" modulated signal **12975**, and generates a harmonically rich "Q" signal **12905**, with a continuous and periodic waveform.

Harmonically rich "I" signal **12903** and harmonically rich "Q" signal **12905** are preferably rectangular waves, such as square waves or pulses (although the invention is not limited to this embodiment), and are comprised of pluralities of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveforms. These sinusoidal waves are referred to as the harmonics of the underlying waveforms, and a Fourier analysis will determine the amplitude of each harmonic.

Harmonically rich "I" signal **12903** and harmonically rich "Q" signal **12905** are combined by summer **12992** to create harmonically rich "I/Q" signal **12907**. Summers are well known to persons skilled in the relevant art(s).

Filter **12994** filters out the undesired harmonic frequencies, and outputs an transmitted modulated signal **12924** at the desired harmonic frequency or frequencies.

It will be apparent to persons skilled in the relevant art(s) that an alternative embodiment exists wherein the harmonically rich "I" signal **12903** and the harmonically rich "Q" signal **12905** may be filtered before they are summed, and further, another alternative embodiment exists wherein "I"-modulated signal **12901** and "Q"-modulated signal **12975** may be summed to create a QPSK-modulated signal before being routed to a switch module. Other QPSK modulation embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention. Further details pertaining to an I/Q modulation mode transmitter are provided in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, which is incorporated herein by reference in its entirety.

6.6.2.6.1.3.2 QPSK Modulation Transmitter Using Balanced Modulator

I/Q balanced modulator transmitter configurations are presented in Section 3.2. These transmitter configurations may be applied in transmitter **12910** to modulate and frequency up-convert WLAN station signals according to DQPSK modulation techniques. The I/Q balanced modulator transmitter configurations presented above and applicable to transmitter **12910** include I/Q transmitter **7420** of FIG. **74**, I/Q transmitter **7608** of FIG. **76**A, I/Q transmitter **7618** of FIG. **76**B, I/Q transmitter **7702** of FIG. **77**, I/Q transmitter **7802** of FIG. **78**, I/Q transmitter **8000** of FIG. **80**, I/Q transmitter **8200** of FIG. **82**, and I/Q transmitter **8300** of FIG. **83**. Refer to Section 3.2 above for detailed description of these transmitters. Further details pertaining to I/Q balanced modulator transmitters are provided in co-pending U.S. patent application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. **1291** illustrates I/Q balanced modulator embodiments for QPSK modulation transmitter **12978**, according to the present invention. QPSK modulation transmitter **12978** comprises a first DBPSK modulator **12911**, a second DBPSK modulator **12913**, a pulse generator **7144**, and an I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300**. Further I/Q balanced modulator embodiments for QPSK modulation transmitter **12978** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

First DBPSK modulator **12911** receives I phase information signal **12974**. First DBPSK modulator **12911** produces an oscillating signal modulated with I phase information signal **12976** according to DBPSK modulation. First DBPSK modulator **12911** outputs first DBPSK modulated signal **12977**.

Second DBPSK modulator **12913** receives Q phase information signal **12976**. Second DBPSK modulator **12913** produces an oscillating signal modulated with Q phase information signal **12976** according to DBPSK modulation. Second DBPSK modulator **12913** outputs second DBPSK modulated signal **12979**. The design and use of a first and second DBPSK modulator **12911** and **12913** is well known to those skilled in the relevant art(s). Suitable first and second DBPSK modulators **12911** and **12913** may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf."

Pulse generator **7144** generates control signals **7123** and **7127** as described elsewhere herein. I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** receives first DBPSK modulated signal **12977**, second DBPSK modulated signal **12979**, and control signals **7123** and **7127**. First DBPSK modulated signal **12977** of FIG. **129**I corresponds to I baseband signal **7402** of FIGS. **74**, **76**A, **76**B, **77**, and **78**, and I baseband signal **8002** of FIGS. **80**, **82**, and **83**. I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** may be one of I/Q transmitter **7420** of FIG. **74**, I/Q transmitter **7608** of FIG. **76**A, I/Q transmitter **7618** of FIG. **76**B, I/Q transmitter **7702** of FIG. **77**, I/Q transmitter **7802** of FIG. **78**, I/Q transmitter **8000** of FIG. **80**, I/Q transmitter **8200** of FIG. **82**, and I/Q transmitter **8300** of FIG. **83**, and other I/Q balanced modulator transmitter of the present invention described herein. The one of I/Q transmitters **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** selected for a particular implementation of transmitter **12910** will depend on the particular application. I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** combines and frequency up-converts first and second DBPSK modulated signals **12977** and **12979**, and outputs transmitted modulated signal **12924**. Transmitted modulated signal **12924** of FIG. **129**I corresponds to output signal **7148** of FIGS. **74**, **76**A, **76**B, **77**, and **78**, and output signal **8016** of FIGS. **80**, **82**, and **83**. Transmitted modulated signal **12924** comprises a DQPSK modulated information signal.

6.6.2.6.2 Receiver DSSS PMD Incorporating Universal Frequency Translation

As shown in FIG. **129**B, receiver DSSS PMD **12902** comprises an antenna **12926**, a de-spread correlator **12928**, a DPSK modulation receiver **12930**, a de-scrambler **12932**, a timing clock recovery module **12934**. The structure and operation of receiver DSSS PMD **12902** will be further described as follows, and is further described elsewhere herein.

Antenna **12926** receives a transmitted modulated signal **12924**. Transmitted modulated signal **12924** comprises an RF carrier signal modulated with an information signal according to DBPSK and/or DQPSK modulation techniques.

De-spread correlator **12928** receives transmitted modulated signal **12924** from antenna **12926**, and receives an 11-bit Barker word. De-spread correlator **12928** convolves the received signal with the 11-bit Barker word and correlates it, and outputs a de-spread signal **12938**. The design and use of a conventional de-spread correlator **12928** is well known to those skilled in the relevant art(s). A suitable conventional de-spread correlator **12928** may be designed

and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

DPSK modulation receiver **12930** receives de-spread signal **12938**. DPSK modulation receiver **12930** demodulates and down-converts de-spread signal **12938**, and outputs demodulated signal **12940**.

De-scrambler **12932** receives demodulated signal **12940**. De-scrambler **12932** de-scrambles demodulated signal **12940**, and outputs PPDU signal **12942**. PPDU signal **12942** comprises one or more PPDU frames and/or PPDU frame portions, such as a PLCP preamble, PLCP header, and MPDU. The design and use of a de-scrambler **12932** is well known to those skilled in the relevant art(s). A suitable de-scrambler **12932** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Timing clock recovery module **12924** is coupled to de-spread correlator **12928** and/or DBPSK/DQPSK de-modulator **12930**. Timing clock recovery module **12924** may be used to recover clocking/timing information from the received signal. Timing clock recovery module **12924** may output a data clock signal **12944**, and may pass clocking/timing information back to de-spread correlator **12928** and/or DPSK modulation receiver **12930**. The design and use of a timing clock recovery module **12924** is well known to those skilled in the relevant art(s). A suitable scrambler **12924** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Alternate embodiments for receiver DSSS PMD **12902** will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the positions of DPSK modulation receiver **12930** and de-spread correlator **12928** may be reversed. FIG. **129**L illustrates a receiver DSSS PMD **12915** wherein DPSK modulation receiver **12930** receives transmitted modulated signal **12924**, demodulates and down-converts transmitted modulated signal **12924**, and outputs a demodulated signal that is received by de-spread correlator **12928**. De-spread correlator **12928** convolves the received demodulated signal with the 11-bit Barker word and correlates it, and outputs a de-spread signal to de-scrambler **12932**. The invention is intended and adapted to include such alternate embodiments.

The receiver DSSS PMD **12902** of FIG. **129**B may incorporate universal frequency translation technology to provide for demodulation and frequency down-conversion of received WLAN station signals. FIG. **129**J illustrates an exemplary embodiment of the DPSK modulation receiver **12930** of FIG. **129**B. Receiver **12930** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver **12930** of FIG. **129**J comprises at least one UFT module **12810**. UFT module **12810** provides for demodulation and frequency down-conversion of received WLAN station signals. As described above, receiver DSSS PMD **12902** demodulates the DBPSK-modulated PLCP preamble and PLCP header, and demodulates the DBPSK- or DQPSK-modulated MPDU. Numerous embodiments for receiver **12930** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for receiver **12930** incorporating UFT module **12810** are further described below and elsewhere herein.

In a further embodiment, de-spread correlator **12928** comprises a UFT module. The UFT module may be used to convolve the received signal with the 11-bit Barker word, by coding a control signal received by the UFT module with the 11-bit Barker word. FIG. **129**K illustrates a further embodiment of the present invention, where de-spread correlator **12928** and receiver **12930** share a UFT module **12810**, to unify convolution of the received signal and down-conversion/demodulation of the received signal. Alternate embodiments for receiver DSSS PMD **12902** will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.6.2.6.2.1 UFD Module Receiver Embodiments for DBPSK Demodulation

FIG. **129**M illustrates an embodiment of the DPSK modulation receiver **12930** of FIG. **129**B. DPSK modulation receiver **12930** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

DPSK modulation receiver **12930** comprises a UFD module **12814**, an optional amplifier **12917**, and an optional filter **12919**. UFD module **12814** comprises at least one UFT module **12810**.

UFD module **12814** inputs de-spread signal **12938**. De-spread signal **12938** comprises an oscillating signal modulated by an information signal according to DBPSK modulation techniques. UFD module **12814** frequency down-converts and demodulates de-spread signal **12938** to UFD module output signal **12921**.

UFD module output signal **12921** is optionally amplified by optional amplifier **12917** and optionally filtered by optional filter **12919**, and a down-converted baseband signal **2516** results. The amplifying and filtering functions may instead be provided for in optional signal conditioning module **2504**, when present.

Received signals of a variety of modulation types may be down-converted directly to a baseband signal by DPSK modulation receiver **12930** of FIG. **129**B. These modulation types include, but are not limited to phase modulation (PM), phase shift keying (PSK) including DBPSK, amplitude modulation (AM), amplitude shift keying (ASK), and combinations thereof.

In embodiments, UFD module **12814** frequency down-converts de-spread signal **12938** to a baseband signal. In alternative embodiments, UFD module **12814** down-converts de-spread signal **12938** to an intermediate frequency.

FIG. **129**N illustrates an alternative embodiment of DPSK modulation receiver **12930** comprising a UFD module **12814** that down-converts de-spread signal **12938** to an intermediate frequency. DPSK modulation receiver **12930** of FIG. **129**N comprises an intermediate frequency (IF) down-converter **12923**. IF down-converter **12923** may comprise a UFD module and/or a UFT module, or may comprise a conventional down-converter. In this embodiment, UFD module output signal **12921** is output by UFD module **12814** at an intermediate frequency. This is an offset frequency, not at baseband. IF down-converter **12923** inputs UFD module output signal **12921**, and frequency down-converts it to baseband signal **12925**.

Baseband signal **12925** is optionally amplified by optional amplifier **12917** and optionally filtered by optional filter **12919**, and a demodulated signal **12940** results.

DPSK modulation receiver **12930** may further comprise a third stage 1F down-converter, and subsequent IF down-converters, as would be required or preferred by some applications. It will be apparent to persons skilled in the relevant art(s) how to design and configure such further IF down-converters from the teachings contained herein. Such implementations are within the scope of the present invention.

6.6.2.6.2.1.1 Detailed UFD Module Block Diagram

FIG. **129**O illustrates an embodiment of UFD module **12814** in greater detail. This embodiment is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

UFD module **12814** comprises a storage device **12931**, an oscillator **12927**, a pulse-shaping circuit **2806**, a reference potential **2808**, and a UFT module **12810**. As described above, many embodiments exist for UFD module **12814**. For instance, in embodiments, oscillator **12927**, or both oscillator **12927** and pulse-shaping circuit **12929**, may be external to UFD module **12814**.

Oscillator **12927** outputs oscillating signal **12935**, which is input by pulse-shaping circuit **12929**. The output of pulse-shaping circuit **12929** is a control signal **12937**, which preferably comprises a string of pulses. Pulse-shaping circuit **12929** controls the pulse width of control signal **12937**.

In an embodiment where de-spread correlator **12928** comprises a UFT module, the string of pulses of the corresponding control signal are coded according to the 11 bit-Barker word.

In embodiments, UFT module **12810** comprises a switch. Other embodiments for UFT module **12810** are within the scope of the present invention, such as those described above. One terminal of UFT module **12810** is coupled to a de-spread signal **12938**, and a second terminal of UFT module **12810** is coupled to a first terminal of storage device **12931**. A second terminal of storage device **12931** is coupled to a reference potential **2808** such as a ground, or some other potential. In a preferred embodiment, storage device **12931** is a capacitor. In an embodiment, the switch contained within UFT module **12810** opens and closes as a function of control signal **12937**. As a result of the opening and closing of this switch, a down-converted signal, referred to as UFD module output signal **12921**, results. Additional details pertaining to UFD module **12814** are contained in U.S. Pat. No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed Oct. 21, 1998, which is incorporated herein by reference in its entirety.

6.6.2.6.2.2 DBPSK Single Channel Receiver Embodiments

Single channel balanced receiver configurations are presented in Section 2.2.3. These receiver configurations may be applied in receiver **12930** to demodulate and frequency down-convert WLAN station signals according to DBPSK demodulation techniques. The single channel balanced receiver configurations presented above and applicable to receiver **12930** include receiver **11900** of FIG. **119**. Refer to Section 2.2 above for detailed description of these receivers. Further details pertaining to balanced modulator receivers are provided in co-pending U.S. patent application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. **129**P illustrates a single channel balanced demodulator embodiment for receiver **12930**, according to the present invention. Receiver **12930** comprises a single channel receiver **11900**. Further single channel balanced demodulator embodiments for receiver **12930** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Receiver **11900** receives de-spread signal **12938**. De-spread signal **12938** of FIG. **129**P corresponds to input RF signal **11906** of FIG. **119**. Receiver **11900** frequency down-converts and demodulates de-spread signal **12938**, and outputs demodulated signal **12940**. Demodulated signal **12940** of FIG. **129**P corresponds to baseband output signal **11908** of FIG. **119**. Demodulated signal **12940** comprises an information signal.

6.6.2.6.2.3 DQPSK Modulation Mode Receiver Embodiments

FIG. **129**Q illustrates an exemplary DQPSK modulation mode embodiment of a DPSK modulation receiver **12930**, according to the present invention. This DQPSK modulation mode embodiment is described herein for purposes of illustration, and not limitation. Alternate DQPSK modulation mode embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver **12930** comprises a QPSK modulation receiver **12939**. QPSK modulation receiver **12939** down-converts and demodulates an input signal that is modulated according to QPSK modulation techniques. QPSK modulation receiver **12939** down-converts and demodulates a received input signal to two baseband information signals. QPSK modulation receiver **12939** comprises at least one UFT module **12810**. QPSK modulation receiver **12939** provides for QPSK demodulation to de-spread signal **12938**, outputting demodulated signal **12940**. Numerous embodiments for QPSK modulation receiver **12939** will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Various embodiments for QPSK modulation receiver **12939** are provided in the following subsections.

6.6.2.6.2.3.1 QPSK Modulation Receiver Using Two UFD Modules

FIG. **129**R illustrates a more detailed circuit block diagram for QPSK modulation receiver **12939**. QPSK modulation receiver **12939** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver **12930** comprises an oscillator **12949**, a first UFD module **12941**, a second UFD module **12943**, a first UFT module **12945**, a second UFT module **12947**, a phase shifter **12951**, a first optional amplifier **12953**, a first filter **12955**, a second optional amplifier **12957**, and a second filter **12959**.

Oscillator **12949** provides an oscillating signal used by both first UFD module **12941** and second UFD module

12943 via the phase shifter 12951. Oscillator 12949 generates an "I" oscillating signal 12961.

"I" oscillating signal 12961 is input to first UFD module 12941. First UFD module 12941 comprises at least one UFT module 12945. In an embodiment, first UFD module 12941 is structured similarly to UFD module 12814 of FIG. 129O, with oscillator 12949 substituting for oscillator 12927, and "I" oscillating signal 12961 substituting for oscillating signal 12935. First UFD module 12941 frequency down-converts and demodulates de-spread signal 12938 to down-converted "I" signal 12965 according to "I" oscillating signal 12961. Down-converted "I" signal 12965 may be an information signal with two possible states or voltage levels (QPSK). In further embodiments, down-converted "I" signal 12965 may be an information signal with more than two possible states or voltage levels (QAM).

Phase shifter 12951 receives "I" oscillating signal 12961, and outputs "Q" oscillating signal 12963, which is a replica of "I" oscillating signal 12961 shifted preferably by 90°.

Second UFD module 12943 inputs "Q" oscillating signal 12963. Second UFD module 12943 comprises at least one UFT module 12947. In an embodiment, second UFD module 12943 is structured similarly to UFD module 12814 of FIG. 1290 with "Q" oscillating signal 12963 substituting for oscillating signal 12935. Second UFD module 12943 frequency down-converts and demodulates de-spread signal 12938 to down-converted "Q" signal 12967 according to "Q" oscillating signal 12963. Down-converted "Q" signal 12967 may be an information signal with two possible states or voltage levels (QPSK). In further embodiments, down-converted "Q" signal 12967 may be an information signal with more than two possible states or voltage levels (QAM).

Down-converted "I" signal 12965 is optionally amplified by first optional amplifier 12953 and optionally filtered by first optional filter 12955, and a first information output signal 12969 is output.

Down-converted "Q" signal 12967 is optionally amplified by second optional amplifier 12957 and optionally filtered by second optional filter 12959, and a second information output signal 12971 is output.

In the embodiment depicted in FIG. 129R, first information output signal 12969 and second information output signal 12971 comprise demodulated signal 12940 of FIG. 129Q.

Alternate configurations for QPSK modulation receiver 12939 will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter 12951 is coupled between de-spread signal 12938 and UFD module 12943, instead of the configuration described above. This and other such QPSK modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

6.6.2.6.2.3.2 QPSK Modulation Receiver Using Balanced Demodulator

I/Q balanced demodulator receiver configurations are presented in Section 2.2. These receiver configurations may be applied in receiver 12930 to demodulate and frequency down-convert WLAN station signals according to DQPSK demodulation techniques. The I/Q balanced demodulator receiver configurations presented above and applicable to receiver 12930 includes I/Q modulation receiver 10300 of FIG. 103. Refer to Section 2.2 above for detailed description of this receiver. Further details pertaining to I/Q balanced demodulator receivers are provided in co-pending U.S. patent application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. 129S illustrates I/Q balanced demodulator embodiments for QPSK modulation receiver 12939, according to the present invention. QPSK modulation receiver 12939 comprises a control signal generator 12981 and an I/Q modulation receiver 10300 of FIG. 103. Further I/Q balanced demodulator embodiments for QPSK modulation receiver 12939 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Control signal generator 12981 generates control signals 10390, 10392, 10394 and 10396 as described elsewhere herein. Control signal generator 12981 may comprise a variety of control signal/pulse generator configurations as described elsewhere herein, including control signal generator 10400 of FIG. 104.

I/Q modulation receiver 10300 receives de-spread signal 12938 and control signals 10390, 10392, 10394 and 10396. De-spread signal 12938 corresponds to I/Q modulated RF input signal 10382 of FIG. 103. I/Q modulation receiver 10300 demodulates and frequency down-converts de-spread signal 12938, and outputs I baseband output signal 10384 and Q baseband output signal 10386, which form demodulated signal 12940. Demodulated signal 12940 comprises I baseband output signal 10384 and Q baseband output signal 10386.

6.6.3 Frequency Hopping Spread Spectrum (FHSS) PHY

As with the DSSS PHY, the FHSS PHY is one of the three PHY layers supported in the standard and uses the 2.4 GHz spectrum as the transmission media. Data transmission over the media is controlled by the FHSS PMD sublayer as directed by the FHSS PLCP sublayer. The FHSS PMD takes the binary bits of information from the whitened PSDU and transforms them into RF signals for the wireless media by using carrier modulation and FHSS techniques. FIGS. 135A and 135B illustrate block diagrams showing basic elements of the FHSS PMD transmitter and receiver, respectively. Details of each are expanded upon in the subsequent section. The FHSS PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and demodulation, as described in subsequent sub-sections.

6.6.3.1 FHSS PLCP Sublayer

The PLCP preamble 13602, PLCP header 13604, and PLCP service data unit (PSDU) 13606 make up the PLCP protocol data unit (PPDU) 13600, as shown in FIG. 136. The PLCP preamble 13602 and PLCP header 13604 are unique to the FHSS PHY. The PLCP preamble 13602 is used to acquire the incoming signal and synchronize the receiver's demodulator. The PLCP header 13604 contains information about PSDU 13600 from the sending FHSS PHY. The PLCP preamble 13602 and PLCP header 13604 are transmitted at 1 Mbps (the basic rate).

SYNC: This field contains a string of alternating 0s and 1s, and is used by the receiver to synchronize the receiver's packet timing and correct for frequency offsets.

SFD: This field contains information marking the start of a PSDU frame. A common SFD is specified for all IEEE 802.11 FHSS radios using the following bit pattern: 00001100101111101. The left most bit is transmitted first.

PLW: This field specifies the length of the PSDU in octets and is used by the MAC to detect the end of a PPDU frame.

PLCP signaling field (PSF): The PSF identifies the data rate of the whitened PSDU 13606, ranging from 1 Mbps to 4.5 Mbps in increments of 0.5 Mbps. Refer to Table 3 for the PSF bits corresponding to various data rates. The PLCP preamble 13602 and header 13604 are transmitted at the basic rate, 1 Mbps. The optional data rate for the whitened PSDU 13606 is 2 Mbps.

TABLE 3

Bits 1–3	Data Rates - Mbps
000	1.0
001	1.5
010	2.0
011	2.5
100	3.0
101	3.5
110	4.0
111	4.5

Header check error: This field contains the results of a calculated frame check sequence from the sending station. The calculation is performed prior to data whitening. The CCITT CRC-16 error detection algorithm is used to protect the PSF and PLW fields. The CRC-16 algorithm is represented by the following polynomial: $G(x)=x^{16}+x^{12}+x^5+1$. The receiver performs the calculation on the incoming PSF and PLW fields, and compares the results against the transmitted field. If an error is detected, the receiver's MAC determines if the incoming PPDU **13600** should be terminated.

Embedded at the end of the PSDU portion of the PPDU **13606** is a field called FCS. This field contains a 32-bit CRC, which protects the information in the PSDU. The FHSS PHY does not determine if errors are present in the PSDU. The MAC makes that determination, similar to the method used by the PHY.

6.6.3.2 PSDU Data Whitening

Data whitening is applied to the PSDU before transmission to minimize DC bias on the data if long strings of Is or 0s are contained in the PSDU. The PHY stuffs a special symbol every 4 octets of the PSDU in a PPDU frame. A 127-bit sequence generator using the polynomial $S(x)=x^7+x^4+1$ and a 32/33 bias-suppression encoding algorithm are used to randomize and whiten the data.

6.6.3.3 FHSS Modulation

In the June 1997 version of IEEE 802.11, the FHSS PMD uses two-level Gaussian frequency shift key (GFSK) modulation to transmit the PSDU **13606** at the basic rate of 1 Mbps. The PLCP preamble **13602** and PLCP header **13604** are transmitted at 1 Mbps. However, four-level GFSK is an optional modulation method defined in the standard that enables the whitened PSDU **13606** to be transmitted at a higher rate. The value contained in the PSF field of the PLCP header **13604** is used to determine the data rate of the PSDU **13606**.

GFSK is a modulation technique used by the FHSS PMD, which deviates (shifts) the frequency either side of the carrier hop frequency depending on whether the binary symbol from the PSDU is a 1 or 0. A bandwidth bit period (Bt)=0.5 is used. The changes in the frequency represent symbols containing PSDU information. For two-level GFSK, a binary 1 represents the upper deviation frequency from the hopped carrier, and a binary 0 represents the lower deviation frequency. The deviation frequency shall be greater than 110 KHz for IEEE 802.11 FHSS radios. The carrier frequency deviation is given by:

Binary **1**=F_c+f_d Carrier hopped frequency plus the upper deviated frequency

Binary **0**=F_c-f_d Carrier hopped frequency minus the lower deviated frequency

Four-level GFSK is similar to two-level GFSK, and is used to achieve a data rate of 2 Mbps in the same occupied frequency bandwidth. The modulator combines two binary bits from the whitened PSDU **13606** and encodes them into symbol pairs (10, 11, 01, 00). The symbol pairs generate four frequency deviations from the hopped carrier frequency, two upper and two lower. The symbol pairs are transmitted at 1 Mbps, and for each bit sent, the resulting data rate is 2 Mbps.

6.6.3.4 FHSS Channel Hopping

A set of hop sequences is defined in IEEE 802.11 for use in the 2.4 GHz frequency band. Hop channels are evenly spaced across the band over a span of 83.5 MHZ. During the development of the IEEE 802.11, the hop sequences listed in the standard were pre-approved for operation in North America, Europe, and Japan. The required number of hop channels is dependent upon the geographic location. In North America and Europe (excluding Spain and France) the number of hop channels is 79. The number of hop channels for Spain is 23 and for France is 35. In Japan, the required number of hop channels is 23. The hopped center channels are spaced uniformly across the 2.4 GHz frequency band occupying a bandwidth of 1 MHZ. In North America and Europe (excluding Spain and France) the hopped channels operate from 2.402 GHz to 2.480 GHz. For Japan, the hopped channels operate from 2.473 GHz to 2.495 GHz. In Spain, the hopped channels operate from 2.447 GHz to 2.473 GHz. For France, the hopped channels operate from 2.448 GHz to 2.482 GHz. Channel **2** is the first hopped channel located at a center frequency of 2.402 GHz, and channel **95** is the last hopped frequency channel in the 2.4 GHz band centered at 2.495 GHz.

Channel hopping is controlled by the FHSS PMD. The FHSS PMD transmits the whitened PSDU **13606** by hopping from channel to channel in a pseudorandom fashion using one of the hopping sequences. The hop rate is set by the regulatory bodies in the country of operation. In the US, FHSS radios must hop a minimum of 2.5 hops per second for a minimum hop distance of 6 MHZ. This is in accordance with the rules specified by the FCC rules under Part **15**.

The hopping sequences for IEEE 802.11 are grouped in hopping sets for worldwide operation: Set 1, Set 2, and Set 3. The sequences are selected when a FHSS BSS is configured for a WLAN. The hopping sets are designed to minimize interference between neighboring FHSS radios in a set. The following hop sets are valid IEEE 802.11 hopping sequence numbers.

Operation in North America and most of Europe:
- Set 1: (0, 3, 6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 57, 60, 63, 66, 69, 72, 75)
- Set 2: (1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52, 55, 58, 61, 64, 67, 70, 73, 76)
- Set 3: (2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53, 56, 59, 62, 65, 68, 72, 74, 77)

Operation in Spain:
- Set 1: (0, 3, 6, 9, 12, 15, 18, 21, 24)
- Set 2: (1, 4, 7, 10, 13, 16, 19, 22, 25)
- Set 3: (2, 5, 8, 11, 14, 17, 20, 23, 26)

Operation in France:
- Set 1: (0, 3, 6, 9, 12, 15, 18, 21, 24, 27, 30)
- Set 2: (1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31)
- Set 3: (2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32)

Operation in Japan:
- Set 1: (6, 9, 12, 15)
- Set 2: (7, 10, 13, 16)
- Set 3: (8, 11, 14, 17)

6.6.3.5 FHSS PMD Incorporating Universal Frequency Translation

In embodiments, the FHSS PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the FHSS PMD may

comprise one or more UFT modules, such as UFT module **12810** of FIG. **128**B, that provide for these functions. Furthermore, the FHSS PMD may comprise one or more UFU modules such as UFU module **12812** of FIG. **128**C, and/or one or more UFD modules such as UFD module **12814** of FIG. **128**C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The FHSS PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to 2-level and 4-level GFSK modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for FHSS PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the FHSS PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.6.3.5.1 Transmit FHSS PMD Incorporating Universal Frequency Translation

As shown in FIG. **129**A, transmit FHSS PMD **13500** comprises a data whitener **13504**, a symbol mapping module **13506**, a transmit Gaussian shaping filter **13508**, a GFSK modulation transmitter **13510**, and an antenna **13512**. The structure and operation of transmit FHSS PMD **13500** will be further described as follows, and is further described elsewhere herein.

Data whitener **13504** receives a PSDU signal **13514**. In embodiments, PSDU signal **13514** may comprise one or more PSDU frames to be modulated according to 2-level or 4-level GFSK modulation. In alternate embodiments, transmit FHSS PMD **13500** may receive a signal comprising the PLCP preamble and/or PLCP header, which may be modulated according to 2-level GFSK modulation. Alternatively, the FHSS PMD PSDU frame, PLCP preamble, and PLCP header may be modulated according to any of the modulation schemes described herein.

Data whitener **13504** whitens the PSDU signal **13514**, and outputs a whitened PSDU signal **13516**. Data whitener **13504** is present in 1 Mbps embodiments when necessary. The design and use of a data whitener **13504** is well known to those skilled in the relevant art(s). A suitable data whitener **13504** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Symbol mapping module **13506** receives optionally whitened PSDU signal **13516**. Symbol mapping module **13506** symbol maps whitened PSDU signal **13516**, and outputs mapped signal **13518**. The design and use of a symbol mapping module **13506** is well known to those skilled in the relevant art(s). A suitable symbol mapping module **13506** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmit Gaussian shaping filter **13508** receives mapped signal **13518**. Transmit Gaussian shaping filter **13508** filters mapped signal **13518**, and outputs filtered signal **13520**. The design and use of a transmit Gaussian shaping filter **13508** is well known to those skilled in the relevant art(s). A suitable transmit Gaussian shaping filter **13508** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

GFSK modulation transmitter **13510** receives filtered signal **13520**. GFSK modulation transmitter **13510** modulates an oscillating signal with filtered signal **13520** according to 2-level or 4-level GFSK, and frequency up-converts filtered signal **13520**. GFSK modulation transmitter **13510** outputs transmitted modulated signal **13522**, which is transmitted by antenna **13512**.

The transmit FHSS PMD of FIG. **135**A may incorporate universal frequency translation technology to provide for modulation and frequency up-conversion of WLAN station signals. FIG. **135**C illustrates an exemplary embodiment of the GFSK modulation transmitter **13510** of FIG. **135**A. Transmitter **13510** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitter **13510** of FIG. **135**C comprises at least one UFT module **12810**. UFT module **12810** provides for modulation and frequency up-conversion of WLAN station signals to be transmitted. As described above, transmit FHSS PMD **13500** transmits the PLCP preamble and PLCP header at 1 Mbps using 2-level GFSK, and the PSDU is sent at either 1 Mbps 2-level GFSK or at 2 Mbps 4-level GFSK, depending on the content in the PSF field of the PLCP header. Numerous embodiments for transmitter **13510** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for transmitter **13510** incorporating UFT module **12810** are further described below and elsewhere herein.

6.6.3.5.1.1 UFU Module Transmitter Embodiments for GFSK Modulation

FIG. **135**D illustrates in greater detail an exemplary embodiment of transmitter **13510** of FIG. **135**A. Transmitter **13510** comprises a GFSK modulator **13538**, a UFU module **12812**, and an optional amplifier **13540**.

GFSK modulator **13538** of transmitter **13510** receives a filtered signal **13520**. GFSK modulator **13538** modulates filtered signal **13520**, according to Gaussian frequency shift keying (GFSK) modulation. For example, GFSK modulator **13538** may frequency modulate an oscillating signal using filtered signal **13520**. GFSK modulator **13538** outputs modulated signal **13542**. The design and use of a GFSK modulator **13538** is well known to those skilled in the relevant art(s). A suitable GFSK modulator **13538** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Modulated signal **13542** is received by UFU module **12812**. UFU module **12812** includes at least one UFT module **12810**. UFU module **12812** frequency up-converts modulated signal **13542**, and outputs UFU module output signal **13544**. Various structures and methods for operation of UFU module **12812** are described more fully elsewhere herein. For example, Section 6.6.2.6.1.1.1 provides an exemplary structural and operational description of an embodiment of UFU module **12812** in FIG. **129**E, where in the present GFSK embodiment, modulated signal **13542** is input to pulse shaping circuit **12954**. Hence, each of the harmonics of harmonically rich signal **12966** have frequency

proportional to control signal **12964**, and in a GFSK embodiment are thus considered to be GFSK modulated.

When present, optional amplifier **13540** amplifies UFU module output signal **13544**, outputting transmitted modulated signal **13522**. Transmitted modulated signal **13522** comprises a GFSK modulated signal.

Further embodiments for up-converting FSK modulated signals are described in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, the full disclosure of which is incorporated herein by reference in its entirety.

6.6.3.5.1.2 GFSK Balanced Modulator Transmitter Embodiments

Balanced modulator transmitter configurations are presented in Section 3.1. These transmitter configurations may be applied in transmitter **13510** of FIG. **135**A to modulate and frequency up-convert WLAN station signals according to GFSK modulation techniques. The balanced modulator transmitter configurations presented above and applicable to transmitter **13510** include transmitter **7102** of FIG. **71**A, transmitter **7162** of FIG. **71**D, transmitter **7302** of FIG. **73**A, and transmitter **7900** of FIG. **79**A. Refer to Section 3.1 above for detailed description of these transmitters. Further details pertaining to balanced modulator transmitters are provided in co-pending U.S. patent application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. **135**E illustrates balanced modulator embodiments for transmitter **13510**, according to the present invention. Transmitter **13510** comprises a GFSK modulator **13546** and a transmitter **7102**, **7162**, **7302**, **7900**. Further balanced modulator embodiments for transmitter **13510** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

GFSK modulator **13546** receives filtered signal **13520**. GFSK modulator **13546** produces an oscillating signal modulated with filtered signal **13520** according to GFSK modulation. GFSK modulator **13546** outputs GFSK modulated signal **13548**. The design and use of a GFSK modulator **13546** is well known to those skilled in the relevant art(s). A suitable GFSK modulator **13546** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmitter **7102**, **7162**, **7302**, **7900** receives GFSK modulated signal **13548**. GFSK modulated signal **13548** of FIG. **135**E corresponds to baseband signal **7110** of FIGS. **71**A and **71**D, baseband signal **7306** of FIG. **73**A, and baseband signal **7902** of FIG. **79**A. Transmitter **7102**, **7162**, **7302**, **7900** may be one of transmitter **7102** of FIG. **71**A, transmitter **7162** of FIG. **71**D, transmitter **7302** of FIG. **73**A, and transmitter **7900** of FIG. **79**A, and other balanced modulator transmitter of the present invention described herein. The one of transmitters **7102**, **7162**, **7302**, **7900** selected for a particular implementation of transmitter **13510** will depend on the particular application. Transmitter **7102**, **7162**, **7302**, **7900** frequency up-converts GFSK modulated signal **13548**, and outputs transmitted modulated signal **13522**. Transmitted modulated signal **13522** of FIG. **135**E corresponds to output signal **7140** of FIGS. **71**A and **71**D, output signal **7322** of FIG. **73**A, and output signal **7936** of FIG. **79**A. Transmitted modulated signal **13522** comprises a GFSK modulated information signal.

6.6.3.5.2 Receiver FHSS PMD Incorporating Universal Frequency Translation

As shown in FIG. **135**B, receiver FHSS PMD **13502** comprises an antenna **13530**, a GFSK modulation receiver **13524**, a data de-whitener **13526**, a hop timing recovery module **13528**. The structure and operation of receiver FHSS PMD **13502** will be further described as follows, and is further described elsewhere herein.

Antenna **13530** receives a transmitted modulated signal **13522**. Transmitted modulated signal **13522** comprises an RF carrier signal modulated with an information signal according to 2-level or 4-level GFSK modulation techniques.

GFSK modulation receiver **13524** receives transmitted modulated signal **13522** from antenna **13530**. GFSK modulation receiver **13524** demodulates and down-converts transmitted modulated signal **13522**, and outputs demodulated signal **13532**. Demodulated signal **13532** comprises one or more PPDU frames and/or PPDU frame portions, such as a PLCP preamble, PLCP header, and PSDU.

Data de-whitener **13526** receives demodulated signal **13532**. Data de-whitener **13526** de-whitens demodulated signal **13532**, and outputs PSDU signal **13534**. PSDU signal **13534** comprises one or more PSDU frames. Data de-whitener **13526** is present in 2-level GFSK embodiments when necessary. The design and use of a data de-whitener **13526** is well known to those skilled in the relevant art(s). A suitable data de-whitener **13526** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Hop timing recovery module **13528** is coupled to GFSK modulation receiver **13524**. Hop timing recovery module **13528** may be used to recover hop timing/clocking information from the received signal. Hop timing recovery module **13528** may output a data clock signal **13536**, and may pass hop timing/clocking information back to GFSK modulation receiver **13524**. The design and use of a hop timing recovery module **13528** is well known to those skilled in the relevant art(s). A suitable hop timing recovery module **13528** may be designed and implemented in software, firmware, hardware, and any combination thereof.

Alternate embodiments for receiver FHSS PMD **13502** will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The receiver FHSS PMD **13502** of FIG. **135**B may incorporate universal frequency translation technology to provide for demodulation and frequency down-conversion of received WLAN station signals. FIG. **135**F illustrates an exemplary embodiment of the GFSK modulation receiver **13524**. Receiver **13524** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver **13524** of FIG. **135**F comprises at least one UFT module **12810**. UFT module **12810** provides for demodulation and frequency down-conversion of received WLAN station signals. As described above, receiver FHSS PMD **13502** demodulates the 2-level GFSK-modulated PLCP preamble and PLCP header, and demodulates the 2-level or 4-level GFSK-modulated PSDU. Numerous embodiments for receiver **13524** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the

scope of the invention. Embodiments for receiver **13524** incorporating UFT module **12810** are further described below and elsewhere herein.

6.6.3.5.2.1 UFD Module Receiver Embodiments for GFSK Demodulation

Various embodiments for receiver **13524** exist, where receiver **13524** comprises one or more UFD modules, and are described elsewhere herein. For instance, receiver **13524** may comprise a UFD module **12814**, as shown in FIGS. **128**C and **128**D. These embodiments are adaptable to demodulation of GFSK modulated signals such as transmitted modulated signal **13522**.

For example, Section 6.6.2.6.2.1 provides exemplary structural and operational description of embodiments comprising a UFD module **12814** for signal down-conversion and demodulation. The configurations shown in FIGS. **129**M and **129**N for receiver **12930** are adaptable to receiver **13524** for down-conversion of GFSK modulated WLAN signals. Receiver **135242** may be configured as shown for receiver **12930** in FIGS. **129**M and **129**N to down-convert and demodulate transmitted modulated signal **13522**. As described above, transmitted modulated signal **13522** is modulated according to GFSK.

In the demodulator configurations of FIGS. **129**M and **129**N, transmitted modulated signal **13522** is input to UFD module **12814**. UFD module **12814** frequency down-converts and demodulates transmitted modulated signal **13522** to UFD module output signal **12921**. In the embodiment shown in FIG. **129**M, UFD module **12814** frequency down-converts transmitted modulated signal **13522** to a baseband signal. In the embodiment shown in FIG. **129**N, UFD module **12814** down-converts transmitted modulated signal **13522** to an intermediate frequency. Demodulated signal **12940** of FIGS. **129**M and **129**N corresponds to demodulated signal **13532** of FIG. **135**B. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Various structures and methods for operation of UFD module **12814** are described more fully elsewhere herein. For example, Section 6.6.2.6.2.1.1 provides an exemplary structural and operational description of an embodiment of UFD module **12814**, shown in FIG. **1290**, where in a GFSK embodiment, transmitted modulated signal **13522** is input to UFT module **12810**.

6.6.3.5.2.2 GFSK Single Channel Receiver Embodiments

Single channel balanced receiver configurations are presented in Section 2.2.3. These receiver configurations may be applied in receiver **13524** to demodulate and frequency down-convert WLAN station signals according to GFSK demodulation techniques. The single channel balanced receiver configurations presented above and applicable to receiver **13524** include receiver **11900** of FIG. **119**. Refer to Section 2.2 above for detailed description of these receivers. Further details pertaining to balanced modulator receivers are provided in co-pending U.S. patent application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. **135**G illustrates a single channel balanced demodulator embodiment for receiver **13524**, according to the present invention. Receiver **13524** comprises a single channel receiver **11900**. Further single channel balanced demodulator embodiments for receiver **13524** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Receiver **11900** receives transmitted modulated signal **13522**. Transmitted modulated signal **13522** of FIG. **135**G corresponds to input RF signal **11906** of FIG. **119**. Receiver **11900** frequency down-converts and demodulates transmitted modulated signal **13522**, and outputs demodulated signal **13532**. Demodulated signal **13532** of FIG. **135**G corresponds to baseband output signal **11908** of FIG. **119**. Demodulated signal **13532** comprises an information signal.

6.6.4 Infrared (IR) PHY

As stated previously, the infrared (IR) PHY is one of the three PHY layers supported in the IEEE 802.11 standard. The IR PHY differs from DSSS and FHSS in using near-visible light as the transmission media. IR communication relies on light energy, which may be reflected by objects and travels by line-of-sight. IR PHY operation is generally restricted to indoor environments. The IR PHY signal typically does not pass through walls, as can the DSSS and FHSS radio signals. Data transmission over the media is controlled by the IR PMD sublayer as directed by the IR PLCP sublayer. The IR PMD takes the binary bits of information from the PSDU and transforms them into light energy emissions for the wireless media by using carrier modulation. FIG. **137** illustrates a block diagram of an exemplary IR PMD sublayer **13700**. IR PMD sublayer **13700** comprises a transmitter **13702** and a receiver **13704**. Further details of each are provided in subsequent subsections.

6.6.4.1 IR PLCP Sublayer

A PLCP preamble **13802**, PLCP header **13804**, and PSDU **13806** make up a PPDU **13600**, as shown in FIG. **138**. The PLCP preamble **13802** and PLCP header **13804** are unique to the IR PHY. The PLCP preamble **13802** is used to acquire the incoming signal and synchronize the receiver prior to the arrival of the PSDU **13806**. The PLCP header **13804** contains information about the PSDU **13806** from the sending IR PHY. The PLCP preamble **13802** and PLCP header **13804** are transmitted at 1 Mbps, and the PSDU **13806** can be sent at 1 Mbps or 2 Mbps.

SYNC: This field contains a sequence of alternating pulse presence and absence in consecutive time slots. The SYNC field is used by the IR PHY to perform signal acquisition and clock recovery. The standard specifies 57 time slots as the minimum and 73 time slots as the maximum.

SFD: This field contains information that marks the start of a PPDU frame. A common SFD is specified for all IEEE 802.11 IR implementations. The SFD is represented by the following bit pattern: 1001

Data rate: This field defines the data rate at which the PPDU **13600** is transmitted. There are two rates to choose from: 000 corresponding to 1 Mbps (the basic rate), and 001 corresponding to 2 Mbps (the enhanced access rate). The PLCP preamble **13802** and PLCP header **13804** are sent at the basic rate 1 Mbps.

DC level: This field contains information that allows the IR PHY to stabilize the DC level after receiving the preamble and data rate fields. The supported data rates use the following bit patterns:

1 Mbps: 00000000100000000000000000100000000

2 Mbps: 00100010001000100010001000100010

Length: This field contains an unsigned 16-bit integer that indicates the number of microseconds to transmit the PSDU **13806**. The MAC layer may use this field to detect the end of a frame.

Frame check sequence: This field contains the calculated 16-bit CRC result from the sending station. The CCITT CRC-16 error detection algorithm is used to protect the length field. The CRC-**16** algorithm is represented by the following polynomial: $G(x)=x^{16}+x^{12}+x^5+1$. The receiver performs the calculation on the incoming Length field and compares the results against the transmitted field. If an error is detected, the receiver's MAC determines whether the incoming PSDU **13806** should be terminated.

Embedded at the end of the PSDU **13806** of the PPDU **13600** is a field called FCS. This field contains a 32-bit CRC, which is used to protect the information in the PSDU **13806**. The IR PHY does not determine whether errors are present in the PSDU **13806**. The MAC makes this determination in a manner similar to that used by the PHY layer.

6.6.4.2 IR PHY Modulation Method

The IR PHY transmits binary data at 1 and 2 Mbps using a modulation scheme known as pulse position modulation (PPM). PPM is used in IR systems to reduce the optical power required to be provided by the LED infrared source. The specific data rate is dependent upon the type of PPM. The modulation for 1 Mbps operation is 16-PPM. The modulation for 2 Mbps is 4-PPM. PPM keeps the amplitude and pulse width constant, and varies the position of the pulse in time. Each pulse position represents a different symbol in time.

For 16-PPM, each group of data bits of the PSDU is mapped to one of the 16-PPM symbols for 1 Mbps operation. Notice in Table 4 a "1" bit in the 16-PPM symbol represents data bit position. The order of bit transmission is left to right. The data bits are arranged (gray coded) to reduce the possibility of multiple bit errors due to intersymbol interference in the media.

TABLE 4

Data Bits	16-PPM Symbols
0000	0000000000000001
0001	0000000000000010
0011	0000000000000100
0010	0000000000001000
0110	0000000000010000
0111	0000000000100000
0101	0000000001000000
0100	0000000010000000
1100	0000000100000000
1101	0000001000000000
1111	0000010000000000
1110	0000100000000000
1010	0001000000000000
1011	0010000000000000
1001	0100000000000000
1000	1000000000000000

For 4-PPM, two data bits are paired in the PSDU to form a 4-bit symbol map as shown in Table 5. The order of bit transmission is left to right.

TABLE 5

Data Bits	4-PPM Symbol
00	0001
01	0010
11	0100
10	1000

6.6.5 Geographic Regulatory Bodies

WLAN IEEE 802.11-compliant DSSS and FHSS radios operating in the 2.4 GHz frequency band must comply with local geographical regulatory domains before operating in this spectrum. These products are subject to certification. The technical requirements in the IEEE 802.11 standard were developed to comply with the regulatory agencies of North America, Europe, and Japan. The regulatory agencies in these regions set emission requirements for WLANs to minimize the amount of interference a radio can generate or receive from another in the same proximity. The regulatory requirements do not affect the interoperability of IEEE 802.11-compliant products. It is the responsibility of product developers to investigate and comply with the regulatory agencies. In some situations, additional certifications are necessary for regions within Europe, or outside of Japan or North America. Listed below are agencies defined by IEEE 802.11.

6.6.5.1 North America

Approval Standards: Industry Canada

Documents: GL36

Approval Authorities: Federal Communications Commission, (FCC)

USA Documents: CFR 47, Part 15 Sections 15.205, 15.209, 15.247

Approval Authority: Industry Canada, FCC (USA)

6.6.5.2 Spain

Approval Standards: Supplemento Del Numero 164 Del Boletin Oficial

Del Estado (Published 10, July 91, Revised 25 June 93)

Documents: ETS 300–328, ETS 300–339

Approval Authority: Cuadro Nacional De Atribucion De Frecuesias

6.6.5.3 Europe

Approval Standards: European Telecommunications Standards Institute

Documents: ETS 300–328, ETS 300–339

Approval Authority: National Type Approval Authorities

6.7 Physical Layer Extensions to IEEE 802.11

In October 1997, the IEEE 802 Executive Committee approved two projects for higher rate physical layer (PHY) extensions to the IEEE 802.11 standard. The first extension, IEEE 802.11a, defines requirements for a PHY operating in the 5.0 GHz U-NII frequency, with data rates ranging from 6 Mbps to 54 Mbps. The second extension, IEEE 802.11b, defines a set of PHY specifications operating in the 2.4 GHz ISM frequency band at rates up to 11 Mbps. Both PHY extensions are defined to operate with the existing MAC. The following sections provide further detail of the two extensions.

6.7.1 IEEE 802.11a —The OFDM Physical Layer

The IEEE 802.11a PHY is one of the physical layer (PHY) extensions of IEEE 802.11 and is referred to as the orthogonal frequency division multiplexing (OFDM) PHY. The OFDM PHY provides the capability to transmit PSDU frames at multiple data rates up to 54 Mbps for WLAN networks where transmission of multimedia content is a consideration. The OFDM PHY defined for IEEE 802.11a is similar to the OFDM PHY specification of ETSI-HIPERLAN (High Performance Radio Local Area Network) II. The OFDM PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and demodulation, as described in subsequent sub-sections.

In the OSI structure, the PHY's PLCP sublayer and PMD sublayer are unique to the OFDM PHY. The following sections provide further detail of the PLCP header, data rates, and modulations defined in IEEE 802.11a.

6.7.1.1 OFDM PLCP Sublayer

The PPDU **13900** is unique to the OFDM PHY. The PPDU **13900** consists of a PLCP preamble **13902**, a signal field **13904**, and a data field **13906**, as shown in FIG. **139**. The receiver uses the PLCP preamble **13902** to acquire the incoming OFDM signal and synchronize the demodulator. The PLCP header **13908** contains information about the PSDU **13910** from the sending OFDM PHY. The PLCP preamble **13902** and the signal field **13904** are transmitted at 6 Mbps, binary phase shift keying (BPSK)-OFDM modulated using convolutional encoding rate R=½.

PLCP preamble: This field is used to acquire the incoming signal, and to train and synchronize the receiver. The PLCP preamble **13902** consists of twelve symbols, including ten short symbols and two long symbols. The short symbols are used to train the receiver's AGC, and to obtain a coarse estimate of the carrier frequency and the channel. The long symbols are used to fine-tune the frequency and channel estimates. Twelve subcarriers are used for the short symbols and **53** for the long symbols. The training of an OFDM is accomplished in **16** μs. The PLCP preamble **13902** is BPSK-OFDM modulated at 6 Mbps.

Signal: The signal **13904** is a 24-bit field, which includes information about the rate and length of the PSDU **13910**. The signal field **13904** is convolutional encoded rate ½, BPSK-OFDM modulated. Four bits (R**1**–R**4**) are used to encode the rate, eleven bits are defined for the length, one bit is reserved, one bit is a parity bit, and six bits form a "0" tail. The rate bits (R**1**–R**4**) are defined in Table **6**. The mandatory data rates for IEEE 802.11a-compliant systems are 6 Mbps, 12 Mbps, and 24 Mbps.

TABLE 6

Rate	Modulation	Coding Rate	Signal bits (R1–R4)
6 Mbps	BPSK	R = ½	1101
9 Mbps	BPSK	R = ¾	1111
12 Mbps	QPSK	R = ½	0101
18 Mbps	QPSK	R = ¾	0111
24 Mbps	16QAM	R = ½	1001
36 Mbps (optional)	16QAM	R = ¾	1011
48 Mbps (optional)	64QAM	R = ⅔	0001
54 Mbps (optional)	64QAM	R = ¾	0011

Length: The length field includes an unsigned 12-bit integer that indicates the number of octets in the PSDU **13910**.

Data: The data field contains the service field, the PSDU **13910**, tails bits **13912**, and pad bits **13914**. A total of six tail bits containing 0s are appended to the PPDU **13900** to ensure that the convolutional encoder is brought back to a zero state. The equation for determining the number of bits in the data field **13906**, the number of tail bits **13912**, the number of OFDM symbols, and the number pad bits **13914** is defined in IEEE 802.11a. The data portion of the packet is transmitted at the data rate indicated in the signal field **13904**.

6.7.1.2 Data Scrambler

Bits transmitted by the OFDM PMD in the data portion are scrambled using a frame-synchronous 127-bit sequence generator. The scrambling is used to randomize the service, PSDU **13910**, pad bit **13914**, and data patterns, which may contain long strings of binary 1s or 0s. The tail bits **13912** are not scrambled. The scrambling polynomial for the OFDM PHY is: $S(x)=x^{-7}+x^{-4}+1$. The initial state of the scrambler is randomly chosen. Prior to scrambling the PPDU frame **13900**, the seven least significant bits of the service field are reset to 0 in order to estimate the initial state of the scrambler in the receiver.

6.7.1.3 Convolutional Encoding

All information contained in the service field, PSDU **13910**, tail field **13912**, and pad field **13914** are encoded using a convolutional encoding rate R=½, ⅔, or ¾ corresponding to the desired data rate. Convolutional encoding is generated using the following polynomials; $g_0=133_8$ *and* $g_1=171_8$ of rate R=½. Puncture codes are used for the higher data rates. Industry standard algorithms, such as the Viterbi algorithm, are recommended for decoding.

6.7.1.4 OFDM Modulation

In July 1998, the IEEE 802.11 Working Group adopted OFDM modulation as the basis for IEEE 802.11a. This OFDM method is similar to the modulation technique adopted in Europe by the ETSI-HIPERLAN II 5 GHz radio PHY specification. The basic principal of operation first divides a high-speed binary signal to be transmitted into a number of lower data rate subcarriers. There are 48 data subcarriers and 4 carrier pilot subcarriers for a total of 52 nonzero subcarriers defined in IEEE 802.11a. Each lower data rate bit stream is used to modulate a separate subcarrier from one of the channels in the 5 GHz band. Intersymbol interference is generally not a concern for a lower speed carrier. However, the subchannels may be subjected to frequency selective fading. Therefore, bit interleaving and convolutional encoding is used to improve the bit error rate performance. The scheme uses integer multiples of the first subcarrier, which are orthogonal to each other. This technique is known as orthogonal frequency division multiplexing (OFDM). Prior to transmission, the PPDU is encoded using a convolutional coded rate R=½, and the bits are reordered and bit interleaved for the desired data rate. Each bit is then mapped into a complex number according to the modulation type, and subdivided into 48 data subcarriers and 4 pilot subcarriers. The subcarriers are combined using an inverse fast Fourier transform (FFT) and transmitted. At the receiver, the carrier is converted back to a multi-carrier lower data rate form using an FFT. The lower data rate subcarriers are combined to form the high rate PPDU. Exemplary block diagrams of an IEEE 802.11a OFDM PMD transmitter and receiver are illustrated in FIGS. **140**A and **140**B, respectively.

6.7.1.5 OFDM PMD Incorporating Universal Frequency Translation Technology

In embodiments, the OFDM PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the OFDM PMD may comprise one or more UFT modules, such as UFT module **12810** of FIG. **128**B, that provide for these functions. Furthermore, the OFDM PMD may comprise one or more UFU modules such as UFU module **12812** of FIG. **128**C, and/or one or more UFD modules such as UFD module **12814** of FIG. **128**C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The OFDM PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to BPSK, QPSK, 16-QAM, and 64-QAM modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for OFDM PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled

in the relevant art(s) based on the teachings contained herein. For example, the OFDM PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.7.1.5.1 Transmit OFDM PMD Incorporating Universal Frequency Translation

As shown in FIG. **129**A, transmit OFDM PMD **14000** comprises a convolutional encoder **14004**, a bit interleaving and mapping module **14006**, an inverse FFT module **14008**, a symbol shaping module **14002**, a PSK/QAM modulation transmitter **14012**, and an antenna **14024**. The structure and operation of transmit OFDM PMD **14000** will be further described as follows, and is further described elsewhere herein.

Convolutional encoder **14004** receives a PPDU signal **14014**. In embodiments, PPDU signal **14014** may comprise one or more PPDU frames, and/or PPDU frame portions, to be modulated according to PSK or QAM modulation schemes. For instance, PPDU signal **14014** may comprise the PLCP preamble and/or signal field, which may be modulated according to BPSK modulation. Furthermore, PPDU signal **14014** may comprise one or more data fields, which may be modulated according to BPSK, QPSK, 16-QAM, and 64-QAM. Alternatively, the OFDM PMD PLCP preamble, signal field, and data fields may be modulated according to any of the modulation schemes described herein.

Convolutional encoder **14004** encodes the PPDU signal **14014**, and outputs an encoded PPDU signal **14016**. The design and use of a convolutional encoder **14004** is well known to those skilled in the relevant art(s). A suitable convolutional encoder **14004** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Bit interleaving and mapping module **14006** receives encoded PPDU signal **14016**. Bit interleaving and mapping module **14006** maps encoded PPDU signal **14016**, and outputs mapped signal **14018**. The design and use of a bit interleaving and mapping module **14006** is well known to those skilled in the relevant art(s). A bit interleaving and mapping module **14006** may be designed and implemented in software, firmware, hardware, and any combination thereof.

Inverse FFT module **14008** receives mapped signal **14018**. Inverse FFT module **14008** performs an inverse FFT upon mapped signal **14018**, and outputs IFFT signal **14020**. The design and use of an inverse FFT module **14008** is well known to those skilled in the relevant art(s). A suitable inverse FFT module **14008** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf"

Symbol shaping module **14010** receives IFFT signal **14020**. Symbol shaping module shapes IFFT signal **14020**, and outputs shaped signal **14022**. The design and use of a symbol shaping module **14010** is well known to those skilled in the relevant art(s). A suitable symbol shaping module **14010** may be designed and implemented in software, firmware, hardware, and any combination thereof.

PSK/QAM modulation transmitter **14012** receives shaped signal **14022**. PSK/QAM modulation transmitter **14012** modulates one or more oscillating signals with shaped signal **14022** according to BPSK, QPSK, or QAM modulation techniques, and frequency up-converts shaped signal **14022**. PSK/QAM modulation transmitter **14012** outputs transmitted modulated signal **14026**, which is transmitted by antenna **14024**.

The transmit OFDM PMD of FIG. **140**A may incorporate universal frequency translation technology to provide for modulation and frequency up-conversion of WLAN station signals. For example, OFDM PMD **14000** may use universal frequency translation technology to modulate signals according to BPSK, QPSK, and QAM modulation techniques. FIG. **140**C illustrates an exemplary embodiment of the PSK/QAM modulation transmitter **14012** of FIG. **140**A. Transmitter **14012** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitter **14012** of FIG. **140**C comprises at least one UFT module **12810**. UFT module **12810** provides for modulation and frequency up-conversion of WLAN station signals to be transmitted. As described above, transmit OFDM PMD **14000** transmits the PLCP preamble and signal field at 6 Mbps using BPSK, and the data fields are sent at the rates and modulation schemes shown in Table 6 above, depending on the content in the signal field. Numerous embodiments for transmitter **14012** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for transmitter **14012** incorporating UFT module **12810** are further described below and elsewhere herein.

6.7.1.5.1.1 UFU Module Transmitter Embodiments for BPSK Modulation

FIG. **140**D illustrates in greater detail an exemplary embodiment of transmitter **14012** of FIG. **140**A. Transmitter **14012** comprises a PSK modulator **14001**, a UFU module **12812**, and an optional amplifier **14003**.

PSK modulator **14001** of transmitter **14012** receives a shaped signal **14022**. PSK modulator **14001** modulates shaped signal **14022**, according to binary phase shift keying (BPSK) modulation. For example, PSK modulator **14001** may frequency modulate an oscillating signal using filtered signal **14022**. PSK modulators are well known to persons skilled in the relevant art(s). PSK modulator **14001** outputs modulated signal **14005**. The design and use of a PSK modulator **14001** is well known to those skilled in the relevant art(s). A suitable PSK modulator **14001** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Modulated signal **14005** is received by UFU module **12812**. UFU module **12812** includes at least one UFT module **12810**. UFU module **12812** frequency up-converts modulated signal **14005**, and outputs UFU module output signal **14007**. Various structures and methods for operation of UFU module **12812** are described more fully elsewhere herein. For example, Section 6.6.2.6.1.1.1 provides an exemplary structural and operational description of an embodiment of UFU module **12812** in FIG. **129**E, where in the present PSK embodiment, modulated signal **14005** is input to pulse shaping circuit **12954**. Hence, each of the harmonics of harmonically rich signal **12966** have frequency proportional to control signal **12964**, and in a PSK embodiment are thus considered to be PSK modulated.

When present, optional amplifier **14003** amplifies UFU module output signal **14007**, outputting transmitted modu-

lated signal **14026**. Transmitted modulated signal **14026** comprises a BPSK modulated signal.

Further embodiments for up-converting PSK modulated signals are described in U.S. Pat. No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed Oct. 21, 1998, the full disclosure of which is incorporated herein by reference in its entirety.

6.7.1.5.1.2 BPSK Balanced Modulator Transmitter Embodiments

Balanced modulator transmitter configurations are presented in Section 3.1. These transmitter configurations may be applied in transmitter **14012** of FIG. **140**A to modulate and frequency up-convert WLAN station signals according to PSK modulation techniques. The balanced modulator transmitter configurations presented above and applicable to transmitter **14012** include transmitter **7102** of FIG. **71**A, transmitter **7162** of FIG. **71**D, transmitter **7302** of FIG. **73**A, and transmitter **7900** of FIG. **79**A. Refer to Section 3.1 above for detailed description of these transmitters. Further details pertaining to balanced modulator transmitters are provided in co-pending U.S. patent application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. **140**E illustrates balanced modulator embodiments for transmitter **14012**, according to the present invention. Transmitter **14012** comprises a PSK modulator **14009** and a transmitter **7102**, **7162**, **7302**, **7900**. Further balanced modulator embodiments for transmitter **14012** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

PSK modulator **14009** receives shaped signal **14022**. PSK modulator **14009** produces an oscillating signal modulated with shaped signal **14022** according to PSK modulation. PSK modulator **14009** outputs PSK modulated signal **14011**. The design and use of a PSK modulator **14009** is well known to those skilled in the relevant art(s). A suitable PSK modulator **14009** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmitter **7102**, **7162**, **7302**, **7900** receives PSK modulated signal **14011**. PSK modulated signal **14011** of FIG. **140**E corresponds to baseband signal **7110** of FIGS. **71**A and **71**D, baseband signal **7306** of FIG. **73**A, and baseband signal **7902** of FIG. **79**A. Transmitter **7102**, **7162**, **7302**, **7900** may be one of transmitter **7102** of FIG. **71**A, transmitter **7162** of FIG. **71**D, transmitter **7302** of FIG. **73**A, and transmitter **7900** of FIG. **79**A, and other balanced modulator transmitter of the present invention described herein. The one of transmitters **7102**, **7162**, **7302**, **7900** selected for a particular implementation of transmitter **14012** will depend on the particular application. Transmitter **7102**, **7162**, **7302**, **7900** frequency up-converts PSK modulated signal **14011**, and outputs transmitted modulated signal **14026**. Transmitted modulated signal **14026** of FIG. **140**E corresponds to output signal **7140** of FIGS. **71**A and **71**D, output signal **7322** of FIG. **73**A, and output signal **7936** of FIG. **79**A. Transmitted modulated signal **14026** comprises a BPSK modulated information signal.

6.7.1.5.1.3 QPSK/QAM Modulation Mode Transmitter Embodiments

Embodiments are provided below for implementing QPSK and QAM modulation transmitters and receivers that may be implemented in WLAN stations, according to embodiment of the present invention. For example, the QPSK and QAM modulation transmitters described below may be implemented in transmit OFDM PMD sublayer **14000** to transmit QPSK and QAM modulated WLAN signals. These transmitter embodiments are described herein for purposes of illustration, and not limitation. Alternate transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.1.5.1.3.1 QPSK Modulation Mode Transmitter Embodiments

FIGS. **129**G–**129**I illustrate exemplary DQPSK modulation transmitter configurations related to transmitter **12910** of FIG. **129**A, according to embodiments of the invention. The DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I are adaptable to providing for QPSK modulation in transmitter **14012** of FIG. **140**A, according to further embodiments of the present invention. For instance, referring to FIG. **129**G, in a QPSK modulation embodiment, DQPSK modulation transmitter **12978** may be adapted to a QPSK modulation transmitter. As a result, transmitted modulated signal **12924** is a QPSK modulated signal. Referring to FIG. **129**H, in a QPSK modulation embodiment, first and second DBPSK modulators **12909** and **12980** may be adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals **12901** and **12975** are BPSK modulated signals. Referring to FIG. **129**I, in a QPSK modulation embodiment, first and second DBPSK modulators **12911** and **12913** are adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals **12977** and **12979** are BPSK modulated signals.

Hence, the DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I may be referred to for exemplary QPSK modulation embodiments of transmitter **14012**. Refer to Section 6.6.2.6.1.3 for further description of the structure and operation of the DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I. Alternate QPSK modulation transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.1.5.1.3.2 QAM Modulation Mode Transmitter Embodiments

Quadrature Amplitude Modulation (QAM) is a well known technique for modulating digital signals using both amplitude and phase coding. Multiple signals may be transmitted using quadrature carriers. An in-phase signal ("I") is modulated such that its amplitude varies discretely as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its amplitude varies discretely as a function of the other information signal. The two modulated signals are combined to form an "QAM" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously. For determining the number of possible discrete levels, M-QAM utilizes a signal structure where each data signal may take on the square-root of M different possible levels. In 64-QAM, each information signal is modulated with the carrier signal in 3 bit segments. Hence, 6 bits are transmitted per symbol. In

16-QAM, each information signal is modulated with the carrier signal in 2 bit segments. Hence, 4 bits are transmitted per symbol.

Embodiments are provided below for implementing QAM transmitters and receivers that may be implemented in IEEE Std. 802.11 WLAN implementations, according to embodiments of the present invention.

FIG. **140**F illustrates an exemplary block diagram of a transmitter **14012** operating in a QAM modulation mode, according to an embodiment of the present invention. Transmitter **14012** of FIG. **140**F comprises a signal separator **14048** and a QAM transmitter **14050**.

Signal separator **14048** receives shaped signal **14022** and outputs I information signal **14052** and Q information signal **14054**. When shaped signal **14022** is a bused signal, signal separator **14048** may merely be a location on the bus where shaped signal **14022** is diverges into separate buses or data signals, for instance. Signal separator **14048** may alternatively comprise logic and memory for receiving and storing shaped signal **14022**, and logically dividing it into the two signals. A suitable signal separator **14048** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf" QAM transmitter **14050** receives I information signal **14052** and Q information signal **14054**. QAM transmitter **14050** provides QAM modulation to I information signal **14052** and Q information signal **14054**, outputting transmitted modulated signal **14026**. Methods and structures related to QAM transmitter **14012**, including methods and structures related to QAM transmitter **14050**, are described in more detail in the following sections.

QAM transmitter **14050** comprises at least one UFT module **12810**. Numerous embodiments for QAM transmitter **14050** will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. In embodiments, UFT module **12810** frequency up-converts an input signal to an RF signal. Methods and structures related to UFT module **12810** are described more fully in the following sections.

6.7.1.5.1.3.2.1 QAM Modulation Transmitter Using Two UFU Modules

FIG. **140**G illustrates a more detailed circuit block diagram for QAM transmitter **14050**. QAM transmitter **14050** up-converts and modulates an input signal according to QAM modulation techniques. QAM transmitter **14050** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

QAM transmitter **14050** comprises a first digital-to-analog (D/A) converter **14019**, a second D/A converter **14021**, a first UFU module **14056**, a second UFU module **14058**, an oscillator **14060**, a phase shifter **14062**, a summer **14064**, and a filter **14066**.

First D/A converter **14019** receives I phase information signal **14052**. First D/A converter **14019** outputs an I phase n-level signal **14023** with an amplitude that varies according to the value of I phase information signal **14052**. For example, in a 64-QAM embodiment, n is equal to 8. I phase information signal **14052** is a digital signal that first D/A converter **14019** converts to an analog signal, in 3 bit segments. Each 3 bit segment of I phase information signal **14052** is converted to an analog signal with 8 possible discrete levels, such as ±a, +3a, +5a, and +7a, wherein "a" is equal to any applicable voltage value, such as 0.5 V. Other voltage values are within the scope of the present invention. In a 16-QAM embodiment, n is equal to 4. I phase information signal **14052** is converted to I phase n-level signal **14023** in 2 bit segments. Each 2 bit segment of I phase information signal **14052** is converted to an analog signal with 4 possible discrete levels. Other m-QAM types are within the scope of the present invention.

Second D/A converter **14021** receives Q phase information signal **14054**. Second D/A converter **14021** outputs an Q phase n-level signal **14025** with an amplitude that varies according to the value of Q phase information signal **14054**. For example, in a 64-QAM embodiment, n is equal to 8. Q phase information signal **14054** is a digital signal that second D/A converter **14021** converts to an analog signal, in 3 bit segments. Each 3 bit segment of Q phase information signal **14054** is converted to an analog signal with 8 possible discrete levels, such as ±a, ±3a, ±5a, and ±7a, wherein "a" is equal to any applicable voltage value, such as 0.5 V. Other voltage values are within the scope of the present invention. In a 16-QAM embodiment, n is equal to 4. Q phase information signal **14054** is converted to Q phase n-level signal **14025** in 2 bit segments. Each 2 bit segment of Q information signal **14054** is converted to an analog signal with 4 possible discrete levels. Other m-QAM types are within the scope of the present invention.

The design and use of first and second D/A converters **14019** and **14021** are well known to those skilled in the relevant art(s). Suitable first and second D/A converters **14019** and **14021** may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf." First and second D/A converters **14019** and **14021** may not be required if I phase information signal **14052** and Q phase information signal **14054** are already n-level signals due to operation of a prior stage of PSK/QAM modulation transmitter **14012**.

Oscillator **14060** generates an "I"-oscillating signal **14084**.

I phase n-level signal **14023** is input to first UFU module **14056**. First UFU module **14056** comprises a first UFT module **14068**, a first resistor **14067**, and a first voltage reference **14080**. I phase n-level signal **14023** is preferably a first data signal with multiple discrete voltage values. The "I"-oscillating signal **14084** is modulated by I phase n-level signal **14023** in first UFU module **14056**, thereby producing an "I"-modulated signal **14088**. First UFT module **14068** comprises a first switch **14072**. As first switch **14072** opens and closes, it gates I phase n-level signal **14023**. The result of the gating is a harmonically rich "I" signal **14088** having a fundamental frequency substantially proportional to "I"-oscillating signal **14084** and an amplitude substantially proportional to the amplitude of I phase n-level signal **14023**. Each of the harmonics of the harmonically rich "I" signal also have amplitudes proportional to the I phase n-level signal **14023**, and are thus considered to be amplitude modulated.

The phase of "I"-oscillating signal **14084** is shifted by phase shifter **14062** to create "Q"-oscillating signal **14086**. Phase shifter **14062** preferably shifts the phase of "I"-oscillating signal **14084** by 90 degrees.

Q phase n-level signal **14025** is input to second UFU module **14058**. Second UFU module **14058** comprises a second UFT module **14070**, a second resistor **14078**, and a second voltage reference **14082**. Q phase n-level signal **14025** is preferably a second data signal with multiple discrete voltage values similar to those of I phase n-level signal **14023**. "Q"-oscillating signal **14086** is modulated by

Q phase n-level signal **14025** in second UFU module **14056**, thereby producing an "Q"-modulated signal **14090**. Second UFT module **14070** comprises a second switch **14074**. As second switch **14074** opens and closes, it gates Q phase n-level signal **14025**. The result of the gating is a harmonically rich "Q" signal **14090** having a fundamental frequency substantially proportional to "Q"-oscillating signal **14086** and an amplitude substantially proportional to the amplitude of Q phase n-level signal **14025**. Each of the harmonics of the harmonically rich "Q" signal also have amplitudes proportional to the Q phase n-level signal **14025**, and are thus considered to be amplitude modulated.

Harmonically rich "I" signal **14088** and harmonically rich "Q" signal **14090** are preferably rectangular waves, such as square waves or pulses (although the invention is not limited to this embodiment), and are comprised of pluralities of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveforms. These sinusoidal waves are referred to as the harmonics of the underlying waveforms, and a Fourier analysis will determine the amplitude of each harmonic.

Harmonically rich "I" signal **14088** and harmonically rich "Q" signal **14090** are combined by summer **14064** to create harmonically rich "QAM" signal **14092**. Summers are well known to persons skilled in the relevant art(s).

Filter **14066** filters out the undesired harmonic frequencies, and outputs a transmitted modulated signal **14026** at the desired harmonic frequency or frequencies.

It will be apparent to persons skilled in the relevant art(s) that an alternative embodiment exists wherein the harmonically rich "I" signal **14088** and the harmonically rich "Q" signal **14090** may be filtered before they are summed. Other "QAM"-modulation embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

6.7.1.5.1.3.2.2 QAM Modulation Transmitter Using Balanced Modulator

I/Q balanced modulator transmitter configurations are presented in Section 3.2. These transmitter configurations may be applied in transmitter **14012** to modulate and frequency up-convert WLAN station signals according to QAM modulation techniques. The I/Q balanced modulator transmitter configurations presented above and applicable to transmitter **14012** include I/Q transmitter **7420** of FIG. **74**, I/Q transmitter **7608** of FIG. **76**A, I/Q transmitter **7618** of FIG. **76**B, I/Q transmitter **7702** of FIG. **77**, I/Q transmitter **7802** of FIG. **78**, I/Q transmitter **8000** of FIG. **80**, I/Q transmitter **8200** of FIG. **82**, and I/Q transmitter **8300** of FIG. **83**. Refer to Section 3.2 above for detailed description of these transmitters. Further details pertaining to I/Q balanced modulator transmitters are provided in co-pending U.S. patent application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. **140**H illustrates I/Q balanced modulator embodiments for QAM modulation transmitter **14050**, according to the present invention. QAM modulation transmitter **14050** comprises a first amplitude modulator **14094**, a second amplitude modulator **14096**, a pulse generator **7144**, and an I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300**. Further I/Q balanced modulator embodiments for QAM modulation transmitter **14050** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

For instance, QAM transmitter **14050** may comprise D/A converters such as first and second D/A converters **14019** and **14021** shown in FIG. **140**G to convert I phase information signal **14052** and Q phase information signal **14054** to n-level signals, if required.

First amplitude modulator **14094** receives I phase information signal **14052**. First amplitude modulator **14094** produces a signal amplitude modulated with I phase information signal **14052**. First amplitude modulator **14094** outputs first amplitude modulated signal **14013**.

Second amplitude modulator **14096** receives Q phase information signal **14054**. Second amplitude modulator **14015** produces a signal amplitude modulated with Q phase information signal **14054**. Second amplitude modulator **14096** outputs second amplitude modulated signal **14015**. The design and use of a first and second amplitude modulator **14094** and **14096** is well known to those skilled in the relevant art(s). Suitable first and second amplitude modulators **14094** and **14096** may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf."

Pulse generator **7144** generates control signals **7123** and **7127** as described elsewhere herein.

I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** receives first amplitude modulated signal **14013**, second amplitude modulated signal **14015**, and control signals **7123** and **7127**. First amplitude modulated signal **14013** of FIG. **140**H corresponds to I baseband signal **7402** of FIGS. **74**, **76**A, **76**B, **77**, and **78**, and I baseband signal **8002** of FIGS. **80**, **82**, and **83**. I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** may be one of I/Q transmitter **7420** of FIG. **74**, I/Q transmitter **7608** of FIG. **76**A, I/Q transmitter **7618** of FIG. **76**B, I/Q transmitter **7702** of FIG. **77**, I/Q transmitter **7802** of FIG. **78**, I/Q transmitter **8000** of FIG. **80**, I/Q transmitter **8200** of FIG. **82**, and I/Q transmitter **8300** of FIG. **83**, and other I/Q balanced modulator transmitter of the present invention described herein. The one of I/Q transmitters **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** selected for a particular implementation of transmitter **14012** will depend on the particular application. I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** combines and frequency up-converts first and second amplitude modulated signals **14013** and **14015**, and outputs transmitted modulated signal **14026**. Transmitted modulated signal **14026** of FIG. **140**H corresponds to output signal **7148** of FIGS. **74**, **76**A, **76**B, **77**, and **78**, and output signal **8016** of FIGS. **80**, **82**, and **83**. Transmitted modulated signal **14026** comprises a QAM modulated information signal.

6.7.1.5.2 Receiver OFDM PMD Incorporating Universal Frequency Translation

As shown in FIG. **140**B, receiver OFDM PM **14002** comprises an antenna **14038**, a PSK/QAM modulation receiver **14028**, a FFT module **14030**, a bit de-interleaving and de-mapping module **14032**, a convolutional code decoder **14034**, and an AFC and clock recovery module **14036**. The structure and operation of receiver OFDM PMD **14002** will be further described as follows, and is further described elsewhere herein.

Antenna **14038** receives a transmitted modulated signal **14026**. Transmitted modulated signal **14026** comprises an RF carrier signal modulated with an information signal according to QAM modulation techniques.

PSK/QAM modulation receiver **14028** receives transmitted modulated signal **14026**. PSK/QAM modulation receiver **14028** demodulates and down-converts transmitted modulated signal **14026**, and outputs demodulated signal **14040**.

FFT module **14030** receives demodulated signal **14040**. FFT module **14030** performs an FFT on demodulated signal **14040**, and outputs FFT output signal **14042**. The design and use of a FFT module **14030** is well known to those skilled in the relevant art(s). A FFT module **14030** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Bit de-interleaving and de-mapping module **14032** receives FFT output signal **14042**. Bit de-interleaving and de-mapping module **14032** de-interleaves and de-maps FFT output signal **14042**, and outputs de-mapped signal **14044**. The design and use of a bit de-interleaving and de-mapping module **14032** is well known to those skilled in the relevant art(s). A suitable bit de-interleaving and de-mapping module **14032** may be designed and implemented in software, firmware, hardware, and any combination thereof.

Convolutional code decoder **14034** receives de-mapped signal **14044**. Convolutional code decoder **14034** decodes de-mapped signal **14044**, and outputs PPDU signal **14046**. PPDU signal **14034** comprises one or more PPDU frames and/or PPDU frame portions, such as a PLCP preamble, signal field, and data field. The design and use of a convolutional code decoder **14034** is well known to those skilled in the relevant art(s). A suitable convolutional code decoder **14034** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

AFC and clock recovery module **14036** is coupled to PSK/QAM de-modulator **14028**. AFC and clock recovery module **14036** may be used to recover clocking/timing information from the received signal. AFC and clock recovery module **14036** may output a data clock signal, and may pass clocking/timing information back to PSK/QAM de-modulator **14028**. The design and use of an AFC and clock recovery module **14036** is well known to those skilled in the relevant art(s). A suitable AFC and clock recovery module **14036** may be designed and implemented in software, firmware, hardware, and any combination thereof.

Alternate embodiments for receiver OFDM PMD **14002** will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The receiver OFDM PMD **14002** of FIG. **140**B may incorporate universal frequency translation technology to provide for demodulation and frequency down-conversion of received WLAN station signals. FIG. **1401** illustrates an exemplary embodiment of the PSK/QAM modulation receiver **14028** of FIG. **140**B. Receiver **14028** is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver **14028** of FIG. **1401** comprises at least one UFT module **12810**. UFT module **12810** provides for demodulation and frequency down-conversion of received WLAN station signals. As described above, receiver OFDM PMD **14002** demodulates the BPSK-modulated PLCP preamble and signal field, and demodulates the BPSK-, QPSK-, 16-QAM-, or 64-QAM-modulated data field. Numerous embodiments for receiver **14028** will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for receiver **14028** incorporating UFT module **12810** are further described below and elsewhere herein.

6.7.1.5.2.1 UFD Module Receiver Embodiments for BPSK Demodulation

Various embodiments for receiver **14028** exist, where receiver **14028** comprises one or more UFD modules, and are described elsewhere herein. For instance, receiver **14028** may comprise a UFD module **12814**, as shown in FIGS. **128**C and **128**D. These embodiments are adaptable to demodulation of BPSK modulated signals such as transmitted modulated signal **14026**.

For example, Section 6.6.2.6.2.1 provides exemplary structural and operational description of embodiments comprising a UFD module **12814** for signal down-conversion and demodulation. The configurations shown in FIGS. **129**M and **129**N for receiver **12930** are adaptable to receiver **14028** for down-conversion of BPSK modulated WLAN signals. Receiver **14028** may be configured as shown for receiver **12930** in FIGS. **129**M and **129**N to down-convert and demodulate transmitted modulated signal **14040**. As described above, transmitted modulated signal **14040** is modulated according to BPSK.

In the demodulator configurations of FIGS. **129**M and **129**N, transmitted modulated signal **14040** is input to UFD module **12814**. UFD module **12814** frequency down-converts and demodulates transmitted modulated signal **14040** to UFD module output signal **12921**. In the embodiment shown in FIG. **129**M, UFD module **12814** frequency down-converts transmitted modulated signal **14040** to a baseband signal. In the embodiment shown in FIG. **129**N, UFD module **12814** down-converts transmitted modulated signal **14040** to an intermediate frequency. Demodulated signal **12940** of FIGS. **129**M and **129**N corresponds to demodulated signal **14040** of FIG. **140**B. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Various structures and methods for operation of UFD module **12814** are described more fully elsewhere herein. For example, Section 6.6.2.6.2.1.1 provides an exemplary structural and operational description of an embodiment of UFD module **12814**, shown in FIG. **1290**, where in a BPSK embodiment, transmitted modulated signal **14040** is input to UFT module **12810**.

6.7.1.5.2.2 BPSK Single Channel Receiver Embodiments

Single channel balanced receiver configurations are presented in Section 2.2.3. These receiver configurations may be applied in receiver **14028** to demodulate and frequency down-convert WLAN station signals according to BPSK demodulation techniques. The single channel balanced receiver configurations presented above and applicable to receiver **14028** include receiver **11900** of FIG. **119**. Refer to Section 2.2 above for detailed description of these receivers. Further details pertaining to balanced modulator receivers are provided in co-pending U.S. patent application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. **140**J illustrates a single channel balanced demodulator embodiment for receiver **14028**, according to the present invention. Receiver **14028** comprises a single channel receiver **11900**. Further single channel balanced demodulator embodiments for receiver **14028** will be appar-

ent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Receiver **11900** receives transmitted modulated signal **14026**. Transmitted modulated signal **14026** of FIG. **140**J corresponds to input RF signal **11906** of FIG. **119**. Receiver **11900** frequency down-converts and demodulates transmitted modulated signal **14026**, and outputs demodulated signal **14040**. Demodulated signal **14040** of FIG. **140**J corresponds to baseband output signal **11908** of FIG. **119**. Demodulated signal **14040** comprises an information signal.

6.7.1.5.2.3 QPS/QAM Modulation Mode Receiver Embodiments

FIG. **140**K illustrates an exemplary QPSK and QAM modulation mode embodiment of receiver **14028**, according to the present invention. This QPSK/QAM modulation mode receiver embodiment is described herein for purposes of illustration, and not limitation. Alternate QPSK and QAM modulation mode receiver embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver **14028** comprises a QPSK/QAM modulation receiver **14098**. QPSK/QAM modulation receiver **14098** down-converts and demodulates an input signal that is modulated according to QPSK or QAM modulation techniques. QPSK/QAM modulation receiver **14098** down-converts and demodulates a received input signal to two baseband information signals. QPSK/QAM modulation receiver **14098** comprises at least one UFT module **12810**. QPSK/QAM modulation receiver **14098** provides for QPSK and QAM demodulation to transmitted modulated signal **14026**, outputting demodulated signal **14040**. Numerous embodiments for QPSK/QAM modulation receiver **14098** will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Various embodiments for QPSK/QAM modulation receiver **14098** are provided in the following subsections.

6.7.1.5.2.3.1 QPSK/QAM Modulation Receiver Using Two UFD Modules

QPSK modulation receiver **12939** shown in FIG. **129**R is adaptable to down-converting and demodulating QPSK and QAM modulated signals. Accordingly, the configuration of QPSK modulation receiver **12939** may be applied to QPSK/QAM modulation receiver **14098**. The structure and operation of QPSK modulation receiver **12939** is further described as follows, as applied to a QPSK and QAM modulation environment of QPSK/QAM modulation receiver **14098**.

Receiver **12930** comprises an oscillator **12949**, a first UFD module **12941**, a second UFD module **12943**, a first UFT module **12945**, a second UFT module **12947**, a phase shifter **12951**, a first optional amplifier **12953**, a first filter **12955**, a second optional amplifier **12957**, and a second filter **12959**.

De-spread signal **12938** of FIG. **129**R corresponds to transmitted modulated signal **14026** of FIG. **140**K. As described above, transmitted modulated signal **14026** may comprise a QPSK or QAM modulated signal. Transmitted modulated signal **14026** is received by first UFD module **12941** and second UFD module **12943**.

Oscillator **12949** provides an oscillating signal used by both first UFD module **12941** and second UFD module **12943** via the phase shifter **12951**. Oscillator **12949** generates an "I" oscillating signal **12961**.

"I" oscillating signal **12961** is input to first UFD module **12941**. First UFD module **12941** comprises at least one UFT module **12945**. In an embodiment, first UFD module **12941** is structured similarly to UFD module **12814** of FIG. **129**O, with oscillator **12949** substituting for oscillator **12927**, and "I" oscillating signal **12961** substituting for oscillating signal **12935**. First UFD module **12941** frequency down-converts and demodulates de-spread signal **12938** to down-converted "I" signal **12965** according to "I" oscillating signal **12961**. In a QPSK modulation embodiment, down-converted "I" signal **12965** may be an information signal with two possible states or voltage levels. In a QAM modulation embodiment, down-converted "I" signal **12965** may be an information signal with more than two possible states or voltage levels. For instance, in 16-QAM, down-converted "I" signal **12965** may have 4 states or levels, and in 64-QAM, may have 8 states or levels.

Phase shifter **12951** receives "I" oscillating signal **12961**, and outputs "Q" oscillating signal **12963**, which is a replica of "I" oscillating signal **12961** shifted preferably by 90°.

Second UFD module **12943** inputs "Q" oscillating signal **12963**. Second UFD module **12943** comprises at least one UFT module **12947**. In an embodiment, second UFD module **12943** is structured similarly to UFD module **12814** of FIG. **1290** with "Q" oscillating signal **12963** substituting for oscillating signal **12935**. Second UFD module **12943** frequency down-converts and demodulates de-spread signal **12938** to down-converted "Q" signal **12967** according to "Q" oscillating signal **12963**. In a QPSK modulation embodiment, down-converted "Q" signal **12967** may be an information signal with two possible states or voltage levels. In a QAM modulation embodiment, down-converted "Q" signal **12967** may be an information signal with more than two possible states or voltage levels. For instance, in 16-QAM, down-converted "Q" signal **12967** may have 4 states or levels, and in 64-QAM, may have 8 states or levels.

Down-converted "I" signal **12965** is optionally amplified by first optional amplifier **12953** and optionally filtered by first optional filter **12955**, and a first information output signal **12969** is output.

Down-converted "Q" signal **12967** is optionally amplified by second optional amplifier **12957** and optionally filtered by second optional filter **12959**, and a second information output signal **12971** is output.

In an embodiment of QPSK/QAM modulation receiver **14098**, first information output signal **12969** and second information output signal **12971** depicted in FIG. **129**R comprise demodulated signal **14040** of FIG. **140**K.

Alternate configurations for QPSK/QAM modulation receiver **14028** will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter **12951** is coupled between transmitted modulated signal **14026** (de-spread signal **12938** of FIG. **129**R) and UFD module **12943**, instead of the configuration described above. This and other such QPSK/QAM modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

6.7.1.5.2.3.2 QPSK/QAM Modulation Receiver Using Balanced Demodulator

I/Q balanced demodulator receiver configurations are presented in Section 2.2. These receiver configurations may be applied in demodulator **14098** to demodulate and frequency down-convert WLAN station signals according to

QPSK and QAM demodulation techniques. The I/Q balanced demodulator receiver configurations presented above and applicable to receiver **14028** include I/Q modulation receiver **10300** of FIG. **103**. Refer to Section 2.2 above for detailed description of this receiver. Further details pertaining to I/Q balanced demodulator receivers are provided in co-pending U.S. patent application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Ser. No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. **140**L illustrates I/Q balanced demodulator embodiments for QPSK/QAM modulation receiver **14098** of FIG. **104**K, according to the present invention. QPSK/QAM modulation receiver **14098** comprises a control signal generator **14017** and an I/Q modulation receiver **10300** of FIG. **103**. Further I/Q balanced demodulator embodiments for QPSK/QAM modulation receiver **14098** will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Control signal generator **14017** generates control signals **10390**, **10392**, **10394** and **10396** as described elsewhere herein. Control signal generator **14017** may comprise a variety of control signal/pulse generator configurations as described elsewhere herein, including control signal generator **10400** of FIG. **104**.

I/Q modulation receiver **10300** receives transmitted modulated signal **14026** and control signals **10390**, **10392**, **10394** and **10396**. Transmitted modulated signal **14026** corresponds to I/Q modulated RF input signal **10382** of FIG. **103**. I/Q modulation receiver **10300** demodulates and frequency down-converts transmitted modulated signal **14026**, and outputs I baseband output signal **10384** and Q baseband output signal **10386**, which form demodulated signal **14040**. Demodulated signal **14040** comprises I baseband output signal **10384** and Q baseband output signal **10386**.

6.7.1.6 OFDM Operating Channels and Transmit Power Requirements

The 5 GHz U-NII frequency band is segmented into three 100 MHZ bands for operation in the United States. The lower band ranges from 5.15–5.25 GHz, the middle band ranges from 5.25–5.35 GHz and the upper band ranges from 5.725–5.825 GHz. The lower and middle bands accommodate 8 channels in a total bandwidth of 200 MHZ and the upper band accommodates 4 channels in a 100 MHZ bandwidth. The frequency channels center frequencies are spaced 20 MHZ apart. The outermost channels of the lower and middle bands are centered 30 MHZ from the outer edges. In the upper band, the outermost channel centers are 20 MHZ from the outer edges. The channel frequencies and numbering defined in IEEE 802.11a start at 5 GHz, and each channel is spaced 5 GHz apart. A set of channel frequencies for each of the U-NII bands is defined in Table 7.

TABLE 7

Regulatory Domain	Frequency Band	Channel Number	Center Frequencies
USA	U-NII lower band	36	5.180 GHz
	5.15–5.25 GHz	40	5.220 GHz
		44	5.220 GHz
		48	5.240 GHz
USA	U-NII middle band	52	5.260 GHz
	5.25–5.35 GHz	56	5.280 GHz
		60	5.300 GHz
		64	5.320 GHz
USA	U-NII upper band	149	5.745 GHz
	5.725–5.825 GHz	153	5.765 GHz
		157	5.785 GHz
		161	5.805 GHz

In addition to frequency and channel allocations, transmit power is a key parameter regulated in the 5 GHz U-NII frequency band. Three transmit RF power levels are specified: 40 mW, 200 mW and 800 mW, as illustrated in Table 8. The upper band defines RF transmit power levels suitable for bridging applications. The lower band specifies a transmit power level suitable for short-range indoor home and small office environments.

TABLE 8

Frequency Band	Maximum Transmit Power with 6 dBi Antenna Gain
5.150–5.250 GHz	40 mW (2.5 mW/MHZ)
5.250–5.350 GHz	200 mW (12.5 mW/MHZ)
5.725–5.825 GHz	800 mW (50 mW/MHZ)

6.7.1.7 Geographic Regulatory Bodies

WLAN IEEE 802.11 a-compliant OFDM radios operating in the 5 GHz UNII frequency band must comply with the local geographical regulatory domains regarding this spectrum. Such products may be subject to certification. For example, regulatory agencies may set emission standards for WLANs in order to minimize the amount of interference a radio may generate or may receive from a nearby radio. The regulatory requirements do not affect the interoperability of IEEE 802.11a compliant products. In the United States, the FCC has responsibility for the allocation of 5 GHz U-UNII bands.

6.7.1.7.1 North America

Geographic Area: USA

Approval Standards: Federal Communications Commission (FCC) Documents: CFR47, Part **15**; Sections 15.205, 15.209, and subpart E;

Sections 15.401–15.407

Approval Authorities: Federal Communications Commission (FCC)

6.7.1.8 Globalization of Spectrum at 5 GHz

IEEE 802.11, ETSI's HIPERLAN II, and Japan's Mobile Multimedia Access Communication Promotion Council (MMAC-PC) have pursued available spectrum allocations in the 5 GHz band. In Europe, the 5.15–5.35 GHz frequency band is reserved for HIPERLAN II devices. ETSI-HIPERLAN II and IEEE 802.11 may potentially share the lower 5 GHz band, drawing on the extreme similarity of the PHY layers of both projects. In Japan, the Wireless Ethernet Working Group of the MMAC-PC recommends using the 802.11a standard at the time the 5.15–5.25 GHz band becomes available in Japan.

6.7.2 IEEE 802.11b-2.4 High Rate DSSS PHY

The IEEE 802.11b PHY extension of IEEE 802.11 is referred to as high rate direct sequence spread spectrum (HR/DSSS). The HR/DSSS PHY provides two functions: First, the HR/DSSS extends the PSDU data rates to 5.5

Mbps and 11 Mbps using an enhanced modulation technique. Second, the HR/DSSS PHY provides a rate shift mechanism, which allows 11 Mbps networks to fall back to 1 and 2 Mbps and interoperate with the legacy IEEE 802.112.4 GHz RF PHY layers. The OSI structure and operation of the PHY's PLCP sublayer and PMD sublayer for HR/DSSS is similar to the existing IEEE 802.11 DSSS PHY described herein. The following sections give an overview of the PLCP header, data rates, and modulations defined in IEEE 802.11b. The HR/DSSS PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and de-modulation, as described in subsequent sub-sections.

6.7.2.1 HR/DSSS PHY PLCP Sublayer

A PPDU frame consists of the PLCP preamble, PLCP header, and the PSDU. As with IEEE 802.11 DSSS, the PMD uses the PLCP preamble to acquire the incoming signal and synchronize the receiver's demodulator. The HR/DSSS PHY defines two PLCP preambles, long and short. FIG. **141**A illustrates a PPDU with a long PLCP preamble **14102**. FIG. **141**B illustrates a PPDU with a short preamble **14104**. The long preamble **14102** uses the same PLCP preamble and header as used by the IEEE 802.11 DSSS PHY, and sends the information at 1 Mbps using DBPSK and Barker word direct sequence spreading. The PSDU is transmitted at 1, 2, 5.5, and 11 Mbps as determined by the content in the signal field. The long preamble **14102** is backwards compatible with existing IEEE 802.11 DSSS PHY and defined to interoperate with existing IEEE 802.11 wireless networks operating at 1 and 2 Mbps.

The short preamble **14104** uses a 56-bit SYNC field to acquire the incoming signal, and transmits the preamble at 1 Mbps using DBPSK modulation and Barker word spreading. The PLCP header transmits at 2 Mbps using DQPSK and Barker word spreading (see FIG. **141**). In this case, the PSDU is transmitted at 2, 5.5, or 11 Mbps as determined by the content in the signal field. The short preamble **14104** is an option in IEEE 802.11b and is useful for those networks where throughput efficiency and interoperability with existing IEEE 802.11 DSSS radios in not necessary. Because the short preamble radio may only interoperate with itself, a short preamble radio must support the long preamble **14102** to be IEEE 802.11b compliant.

SYNC: The receiver uses this field to acquire the incoming signal and synchronize the receiver's carrier tracking and timing prior to receiving the start of frame delimiter (SFD). The long preamble SYNC field is 128 bits in length, and contains a string of scrambled 1s. The scrambler seed bit pattern used to initialize the scrambler for the long preamble is 01101100. The short preamble SYNC field is 56 bits in length, and contains a string of scrambled 0s. The scrambler seed bit pattern used to initialize the scrambler for short preamble operation is 00011010. The short preamble SYNC field may be used for networks where minimizing overhead and maximizing PSDU throughput is a consideration.

SFD: This field contains information marking the start of a PPDU frame. The SFD specified is common for all IEEE 802.11 DSSS and IEEE 802.11b long preamble radios. The following hexadecimal word is used: F3A0hex transmitted LSB first. For short preamble radios, the following hexadecimal word is used: 05CFhex transmitted LSB first.

Signal: The signal field defines which type of modulation must be used to receive the incoming PSDU. The binary value in this field is equal to the data rate multiplied by 100 kbit/s. The Mbps data rate is used for long and short preamble implementations. The bit patterns in this field and the respective data rates are shown in Table 9.

TABLE 9

Signal Field	Data Rate
00001010	1 Mbps (long preamble only)
00010100	2 Mbps
00111110	5.5 Mbps
01101110	11 Mbps

Service: The service field uses 3 bits of the reserved 8 bits for IEEE 802.11b. Data bit (b**2**) determines whether the transmit frequency and symbol clocks use the same local oscillator. Data bit (b**3**) indicates whether complimentary code keying (CCK) or packet binary convolutional coding (PBCC) is used and data bit (b**7**) is a bit extension used in conjunction with the length field to calculate the duration of the PSDU in microseconds. This field is used for the long and short preamble frames.

Length: The length field is an unsigned 16-bit integer that indicates the number of microseconds necessary to transmit the PSDU. For any data rate over 8 Mbps, bit-**7** of the service field is used with the length field to determine the time in microseconds from the number of octets contained in the length field. A calculation is defined in IEEE 802.11b for determining the length in microseconds for CCK and PBCC as applied to both preambles. The MAC layer uses this field to determine the end of a PPDU frame.

CRC: The CRC field contains the results of a calculated frame check sequence from the sending station. The calculation is performed prior to data scrambling for the long and short preamble. A CCITT CRC-16 error detection algorithm is used to protect the signal, service, and length fields. The CRC-16 algorithm is represented by the following polynomial: $G(x)=x^{16}+x^{12}+x^{5}+1$. The receiver performs the calculation on the incoming Signal, Service and Length fields, and compares the results against the transmitted value. If an error is detected, the receiver's MAC makes the decision whether incoming PSDU should be terminated.

6.7.2.2 High Rate Data Scrambling

All information bits transmitted by the DSSS PMD are scrambled using a self-synchronizing 7-bit polynomial. The scrambling polynomial for the DSSS PHY is: $G(z)=z^{-7}+z^{-4}+1$. Scrambling is used to randomize the long and short preamble data in the SYNC field of the PLCP and for data patterns which contain long strings of binary 1s or 0s. The receiver can descramble the information bits without prior knowledge from the sending station. The scrambler initialization bit patterns are represented as (00011010) for the short preamble and (01101100) for the long preamble.

6.7.2.3 IEEE 802.11 High Rate Operating Channels

The HR/DSSS PHY uses the same frequency channels as defined for the IEEE 802.11 direct sequence PHY. The channel center frequencies are spaced 25 MHZ apart to allow multiple WLAN systems to operate simultaneously in the same area without interfering with each other. An example of a typical channel arrangement for non-interfering channels for North America is illustrated in FIG. **142**. In Europe, the channels 1 (2.412 GHz), 7 (2.442 GHz), and 13 (2.472 GHz) are used to form three non-interfering networks.

6.7.2.4 IEEE 802.11 DSSS High Rate Modulation and Data Rates

There are four modulation formats and data rates defined in IEEE 802.11b. The data rates include the basic rate, the extended rate, and enhanced rate. The basic rate is defined

as 1 Mbps modulated with DBPSK, and the extended rate is defined as 2 Mbps DQPSK modulated. The 1'-bit Barker word is used as the spreading format for the basic and extended rate as described for the DSSS PHY herein. The enhanced rate is defined to operate at 5.5 Mbps and 11 Mbps using CCK modulation and packet binary convolutional coding (PBCC). PBCC is an option in the standard for networks requiring enhanced performance. Frequency agility is further option defined in IEEE 802.11b. As with the 1 and 2 Mbps DSSS PHY, this option enables existing IEEE 802.11 FHSS 1 Mbps networks to be interoperable with 11 Mbps CCK high rate networks. The PBCC and frequency agility option are further described below.

6.7.2.4.1 Complementary Code Keying (CCK) Modulation

In July of 1998, the IEEE 802.11 Working Group adopted CCK as the basis for the high rate extension to deliver PSDU frames at speeds of 5.5 Mbps and 11 Mbps. CCK was adopted because it provides for interoperability with existing IEEE 802.111 and 2 Mbps systems by maintaining the same bandwidth and incorporating the existing DSSS PHY PLCP preamble and header.

CCK is a variation on M-ary orthogonal keying modulation and is based on an in-phase (I) and quadrature (O) architecture using complex symbols. CCK allows for multichannel operation in the 2.4 GHz band by using the existing 1 and 2 Mbps DSSS channelization scheme. CCK uses 8 complex chips in each spreading code word. Each chip can assume one of four phases (QPSK). CCK uses 64 base spreading code words out of a possible set of 65536 (i.e., $65536\text{-}4^3$). Base spreading codes were chosen with beneficial autocorrelation and crosscorrelation properties. The CCK modulator chooses one of M unique for transmission of the scrambled PSDU. CCK uses one vector from a set of 64 complex quadrature phase shift keying (QPSK) vectors for the symbol and thereby modulates 6 bits (one of 64) on each spreading code symbol. An exemplary block diagram for a CCK modulator is shown in FIG. **143**. Each spreading code is 8 complex chips in length. CCK uses a complex set of Walsh/Hadamard functions known as complementary codes. Refer to IEEE 802.11b for the equation used to derive the set of code words. There are four phase terms in the CCK equation. One of the terms modulates all of the chips, and is used for the QPSK rotation of entire code vector. The others modulate every odd chip, every odd pair of chips and every odd quad of chips. To minimize DC offsets, the 4th and 7th terms in the equation are rotated by 180 degrees with a cover sequence. As with the IEEE 802.11 DSSS PHY, the phase rotation for CCK is counterclockwise. To insure that the modulation has the same bandwidth as the legacy IEEE 802.11 DSSS PHY, the chipping rate is kept at 11 Mbps while the symbol rate is increased to 1.375 Mbps. The spreading rate remains constant while the data rate changes, and the CCK spectrum is the same as the legacy IEEE 802.11 waveform.

For 5.5 Mbps transmission, the scrambled binary bits of the PSDU are grouped into 4-bit nibbles, where two of the bits select the spreading function while the remaining two bits QPSK modulate the symbol, as illustrated in FIG. **144**A. The spreading sequence DQPSK modulates the carrier by driving the I and Q modulators. For 11 Mbps operation, the incoming scrambled PSDU binary bits are grouped into 2 and 6 bits, as illustrated in FIG. **144**B. The 6 bits are used to select (one of 64) complex vectors of 8 chips in length for the symbol and the other 2 bits DQPSK modulate the entire symbol. The transmit waveform is the same, and the chipping rate is maintained at 11 Mbps.

6.7.2.4.2 DSSS Packet Binary Convolutional Coding

Packet binary convolutional coding (PBCC) is an optional coding scheme defined in IEEE 802.11b. The coding option uses a 64-state binary convolutional code (BCC), rate R=½ code, and a cover sequence. An exemplary PBCC modulator is illustrated in FIG. **145**A. The HR/DSSS PMD uses PBCC to transmit the PPDU. To ensure that the PPDU frame is properly decoded at the receiver, the memory of the BCC encoder **14502** is cleared at the beginning and at the end of a frame. A cover sequence is used to map the QPSK symbols. The cover sequence is initialized with a 16-bit pattern (0011001110001011) to produce a 256-bit cover sequence, which selects the QPSK symbols. Binary phase shift keying (BPSK) is used for 5.5 Mbps, and QPSK for 11 Mbps. For QPSK, each pair of output bits from the BCC is used to generate one symbol. For BPSK, each pair of bits produces two symbols. The result is one bit per symbol for QPSK and ±2 bit per symbol for BPSK. Refer to IEEE 802.11b for the equation used for the cover sequence generator **14504**.

6.7.2.4.3 Frequency Hopped Spread Spectrum (FHSS) Interoperability

A channel agility option is defined in IEEE 802.11b which allows IEEE 802.11 FHSS 1 and 2 Mbps networks to interoperate with HR/DSSS 11 Mbps WLANs. Both non-overlapping and overlapping high rate channels are supported. The non-overlapping channels allow WLAN systems to operate simultaneously in the same area without interfering with each other. In North America, channels 1, 6, and 11 are specified for non-overlapping networks, and in Europe (excluding France and Spain) channels 1, 7, and 13 are specified as such. Two sets of hopping sequences are defined for worldwide operation. For more details on the hop patterns, refer to IEEE 802.11b.

6.7.2.5 HR/DSSS PMD Incorporating Universal Frequency Translation Technology

In embodiments, the HR/DSSS PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the HR/DSSS PMD may comprise one or more UFT modules, such as UFT module **12810** of FIG. **128**B, that provide for these functions. Furthermore, the HR/DSSS PMD may comprise one or more UFU modules such as UFU module **12812** of FIG. **128**C, and/or one or more UFD modules such as UFD module **12814** of FIG. **128**C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The HR/DSSS PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to DBPSK, DQPSK, CCK, and PBCC modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for HR/DSSS PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the HR/DSSS PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.7.2.5.1 Transmit HR/DSSS PMD Incorporating Universal Frequency Translation

FIG. **143**A illustrates a transmit HR/DSSS PMD **14300**, according to an embodiment of the present invention. Transmit HR/DSSS PMD **14300** of the present invention comprises at least one UFT module **12810** for frequency translation/modulation/demodulation of WLAN station signals.

As described above, the transmit HR/DSSS PMD **14300** transmits WLAN signals according to DBPSK, DQPSK, CCK, and PBCC modulation schemes. For instance, in the case of a long preamble, transmit HR/DSSS PMD **14300** transmits the PLCP preamble and PLCP header at 1 Mbps according to DBPSK, and the PSDU is sent at either 1 Mbps DBPSK, 2 Mbps DQPSK, or 5.5 or 11 Mbps CCK or PBCC, depending on the content in the signal field and service field. In the case of a short preamble, transmit HR/DSSS PMD **14300** transmits the PLCP preamble at 1 Mbps using DBPSK, the PLCP header at 2 Mbps using DQPSK, and the PSDU is sent at either 2, 5.5, or 11 Mbps, depending on the content in the signal field.

Transmission of WLAN signals according to DBPSK and DQPSK modulation schemes are described in detail in Section 6.6.2.6.1 above in reference to transmit DSSS PMD **12900**. The structure and operation of transmit DSSS PMD **12900** is applicable to transmit HR/DSSS PMD **14300**, and is hence considered incorporated in transmit HR/DSSS PMD **14300**. Refer to Section 6.6.2.6.1 above for detailed description of transmission of DBPSK and DQPSK modulated signals by transmit HR/DSSS PMD **14300**. The transmission of CCK and PBCC modulated signal is described below.

6.7.2.5.1.1 Transmitter Embodiments for CCK Modulation

As shown in FIG. **143**B, transmit HR/DSSS PMD **14300** comprises a CCK modulator **14324**, according to embodiments of the present invention. CCK modulator **14324** modulates WLAN station signals according to CCK modulation techniques. CCK modulator **14324** comprises a scrambler **14302**, a data multiplexer **14304**, a complex code selector module **14306**, and a DQPSK modulation transmitter **14308**. The structure and operation of transmit HR/DSSS PMD **14300** in a CCK modulation mode will be described as follows, and is further described elsewhere herein.

Scrambler **14302** receives a PSDU signal **14310**. In embodiments, PSDU signal **14310** may comprise one or more PPDU frames, and/or PPDU frame portions, such as the PSDU, to be modulated according to CCK modulation. Alternatively, the HR/DSSS PMD PSDU may be modulated according to any of the modulation schemes described herein.

Scrambler **14302** scrambles the PSDU signal **14310**, and outputs a scrambled PSDU signal **14312**. The design and use of a scrambler **14302** is well known to those skilled in the relevant art(s). A suitable scrambler **14302** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Data multiplexor **14304** receives scrambled PSDU signal **14312**. Data multiplexor **14304** multiplexes scrambled PSDU signal **14312**, and outputs first multiplexed output signal **14314** and second multiplexed output signal **14316**. In a 5.5 Mbps embodiment, first multiplexed output signal **14314** is 2 bits wide. In an 11 Mbps embodiment, first multiplexed signal **14314** is 6 bits wide. Second multiplexed output signal **14316** is 2 bits wide. The design and use of a data multiplexor **14304** is well known to those skilled in the relevant art(s). A suitable data multiplexor **14304** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Complex code selector module **14306** receives first multiplexed output signal **14314**. Complex code selector module **14306** selects a spreading code using first multiplexed output signal **14314**. In a 5.5 Mbps embodiment, the spreading code is selected from 4 possible code words. In an 11 Mbps embodiment, the spreading code is selected from 64 possible code words. Complex code selector module **14306** outputs spreading code **14318**. The design and use of a complex code selector module **14306** is well known to those skilled in the relevant art(s). A suitable complex code selector module **14306** may be designed and implemented in software, firmware, hardware, and any combination thereof.

DQPSK modulation transmitter **14308** receives second multiplexed signal **14316** and spreading code **14318**. DQPSK modulation transmitter **14308** modulates spreading code **14318** with second multiplexed signal **14316** according to the technique of DQPSK modulation.

In an embodiment, DQPSK modulator operates similarly to modulator **12978** of FIG. **129**I, and comprises a transmitter such as I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300**, which combines and frequency up-converts these signals to a transmitted modulated signal. The resulting transmitted modulated signal may be transmitted by an antenna. Also refer to the DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I for further configurations for providing DQPSK modulation in transmitter **14308** of FIG. **143**B.

In an alternate embodiment, DQPSK modulation transmitter **14308** outputs I data **14320** and Q data **14320**, as shown in FIG. **1291**, which are input to a transmitter such as I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300**. I/Q transmitter **7402**, **7608**, **7618**, **7702**, **7802**, **8000**, **8200**, **8300** combines and frequency up-converts these signals to a transmitted modulated signal, which may be transmitted by an antenna. Alternate embodiments for CCK modulator **14324** (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.2.5.1.2 Transmitter Embodiments for PBCC Modulation

As shown in FIG. **145**A, transmit HR/DSSS PMD **14300** comprises a PBCC modulator **14500**, according to embodiments of the present invention. PBCC modulator **14500** modulates WLAN station signals according to PBCC modulation techniques. PBCC modulator **14500** comprises a binary convolutional code encoder **14502**, a cover code sequence generator **14504**, a scrambler **14506**, a QPSK cover code map module **14508**, and a QPSK modulation transmitter **14510**. The structure and operation of transmit HR/DSSS PMD **14300** in a PBCC modulation mode will be described as follows, and is further described elsewhere herein.

Scrambler **14506** receives PPDU signal **14512**. In embodiments, PPDU signal **14512** may comprise one or more PPDU frames, and/or PPDU frame portions, such as the PSDU, the PLCP preamble, and the PLCP header, to be modulated according to PBCC modulation. Alternatively, the HR/DSSS PMD PPDU may be modulated according to any of the modulation schemes described herein.

Scrambler **14506** scrambles PPDU signal **14512**, and outputs scrambled PPDU signal **14512**. The design and use

of a scrambler **14506** is well known to those skilled in the relevant art(s). A suitable scrambler **14506** may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Binary convolutional code encoder **14502** receives scrambled PPDU signal **14512**. Binary convolutional code encoder **14502** encodes scrambled PPDU signal **14512**, and outputs encoded signal **14512**. The design and use of a binary convolutional code encoder **14502** is well known to those skilled in the relevant art(s). A suitable binary convolutional code encoder **14502** may be designed and implemented in software, firmware, hardware, and any combination thereof.

Cover code sequence generator **14504** receives 16-bit cover code seed **14520**. Cover code sequence generator **14504** generates cover code sequence **14518**. The design and use of a cover code sequence generator **14504** is well known to those skilled in the relevant art(s). A suitable cover code sequence generator **14504** may be designed and implemented in software, firmware, hardware, and any combination thereof QPSK cover code map module **14508** receives encoded signal **14512** and cover code sequence **14518**. QPSK cover code map module **14508** maps encoded signal **14512** via cover sequence **14518**, and outputs mapped I signal **14522** and mapped Q signal **14524**. A suitable QPSK cover code map module **14508** may be designed and implemented in software, firmware, hardware, and any combination thereof, as would be understood by persons skilled in the relevant art(s) from the teachings herein.

QPSK modulation transmitter **14510** receives mapped I signal **14522** and mapped Q signal **14524**. QPSK modulation transmitter **14510** modulates mapped I signal **14522** and mapped Q signal **14524** according to QPSK modulation, and outputs modulated output signal **14526**. FIGS. **129**G–**129**I illustrate exemplary DQPSK modulation transmitter configurations related to transmitter **12910** of FIG. **129**A, according to embodiments of the invention. The DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I are adaptable to providing for QPSK modulation in transmitter **14510** of FIG. **145**A, according to further embodiments of the present invention. For instance, referring to FIG. **129**G, in a QPSK modulation embodiment, DQPSK modulation transmitter **12978** may be adapted to a QPSK modulation transmitter. As a result, transmitted modulated signal **12924** is a QPSK modulated signal. Referring to FIG. **129**H, in a QPSK modulation embodiment, first and second DBPSK modulators **12909** and **12980** may be adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals **12901** and **12975** are BPSK modulated signals. Referring to FIG. **1291**, in a QPSK modulation embodiment, first and second DBPSK modulators **12911** and **12913** are adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals **12977** and **12979** are BPSK modulated signals.

Hence, the DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I may be referred to for exemplary QPSK modulation embodiments of QPSK modulation transmitter **14510**. Refer to Section 6.6.2.6.1.3 for further description of the structure and operation of the DQPSK modulation transmitter configurations of FIGS. **129**G–**129**I. Alternate QPSK modulation transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.2.5.2 Receiver HR/DSSS PMD Incorporating Universal Frequency Translation

FIG. **145**B illustrates a receiver HR/DSSS PMD **14528**, according to an embodiment of the present invention. Receiver HR/DSSS PMD **14528** of the present invention comprises at least one UFT module **12810** for frequency translation/modulation/demodulation of WLAN station signals.

As described above, receiver HR/DSSS PMD **14528** receives and demodulates WLAN signals modulated according to DBPSK, DQPSK, CCK, and PBCC modulation schemes. For example, receiver HR/DSSS PMD **14528** of the present invention demodulates the DBPSK-modulated PLCP preamble, the DBPSK- or DQPSK-modulated PLCP header, and demodulates the DBPSK-, DQPSK-, CCK-, or PBCC-modulated PSDU.

Receivers for receiving WLAN signals modulated according to DBPSK and DQPSK modulation schemes are described in detail in Section 6.6.2.6.2 above in reference to receiver DSSS PMD **12902**. The structure and operation of receiver DSSS PMD **12902** is applicable to receiver HR/DSSS PMD **14528**, and is hence considered incorporated in receiver HR/DSSS PMD **14528**. Refer to Section 6.6.2.6.2 above for detailed description of the reception of DBPSK and DQPSK modulated signals by receiver HR/DSSS PMD **14528**.

As shown in FIG. **145**C, receiver HR/DSSS PMD **14528** comprises a CCK demodulator **14530**, according to embodiments of the present invention. CCK demodulator **14530** comprises at least one UFT module **12810**. CCK demodulator **14530** demodulates CCK modulated WLAN station signals. As described above, CCK modulated WLAN station signals are generated in part by techniques including DQPSK/QPSK modulation. In embodiments, CCK demodulator **14530** incorporates the structure and operation of QPSK modulation receiver **12939** described above in Section 6.6.2.6.2 in regards to demodulation of DQPSK modulated signals. In further embodiments, CCK demodulator **14530** incorporates the structure and operation of QPSK/QAM modulation receiver **14098** described above in Section 6.7.1.5.2 in regards to demodulation of QPSK modulated signals. Refer to Sections 6.6.2.6.2 and 6.7.1.5.2 above for detailed description of the reception of DQPSK and QPSK modulated signals by receiver HR/DSSS PMD **14528**.

As shown in FIG. **145**D, receiver HR/DSSS PMD **14528** comprises a PBCC demodulator **14532**, according to embodiments of the present invention. PBCC demodulator **14532** comprises at least one UFT module **12810**. PBCC demodulator **14532** demodulates PBCC modulated WLAN station signals. As described above, PBCC modulated WLAN station signals are generated in part by techniques including DQPSK/QPSK modulation. In embodiments, PBCC demodulator **14532** incorporates the structure and operation of QPSK modulation receiver **12939** described above in Section 6.6.2.6.2 in regards to demodulation of DQPSK modulated signals. In further embodiments, PBCC demodulator **14532** incorporates the structure and operation of QPSK/QAM modulation receiver **14098** described above in Section 6.7.1.5.2 in regards to demodulation of QPSK modulated signals. Refer to Sections 6.6.2.6.2 and 6.7.1.5.2 above for detailed description of the reception of DQPSK and QPSK modulated signals by receiver HR/DSSS PMD **14528**.

Alternate embodiments for receiver HR/DSSS PMD **14528** will be apparent to persons skilled in the relevant

art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.8 System Design Considerations for IEEE 802.11 WLANs

The IEEE 802.11 WLAN standard provides a number of physical layer options in terms of data rates, modulation types, and spreading spectrum techniques. Selecting the correct physical layer and MAC technologies for an application requires careful planning and detailed systems analysis for developing the optimal WLAN implementation. The following sections focus on a few key considerations when implementing a compliant IEEE 802.11 interoperable WLAN system.

6.8.1 The Medium

A difference between a "wired" and a RF WLAN is the radio communications link. While a radio communications link provides the freedom to move without the constraints of wires, the wired media has the luxury of a controlled propagation media. Wireless RF media may be difficult to control because the dynamics of the propagated signals over the media are constantly changing. IEEE 802.11 WLANs may suffer from this difficulty because the 2.4 GHz bands are shared with unlicensed users. Radio system designers need to have a thorough understanding of the RF medium to properly design 2.4 GHz and 5 GHz IEEE 802.11 WLAN systems, especially for networks operating at data rates greater than 2 Mbps. The RF communication media for home, enterprise, and manufacturing environments may be different. Multipath and path loss are issues to consider when designing an IEEE 802.11 WLAN system.

6.8.2 Multipath

Multipath is a performance concern for indoor IEEE 802.11 WLAN systems. Multipath may occur when the direct path **9402** of a transmitted signal is combined with paths **9404** and **9406** of a reflected signal, resulting in a corrupted signal at the receiver **9408**, as shown in FIG. **94**. The delay of a reflected signal is measured in nanoseconds (nsec), and is commonly known as delay spread. Delay spread is the parameter used to signify multipath. The amount of delay spread varies for indoor, home, office, and manufacturing environments, as shown in Table 10. Surfaces of furniture, elevator shafts, walls, factory machinery, metal constructed buildings, and other objects may contribute to the amount of delay spread in a given environment.

TABLE 10

Environment	Delay Spread
Home	<50 nsec
Office	~100 nsec
Manufacturing floor	200–300 nsec

The channel impulse response is a way to illustrate the amount of multipath dispersion. For example, the amount of delay spread in an office environment may be approximately 100 nsec, as shown in FIG. **95**. Typically, energy reflected by wall surfaces causes the impulse response to have energy on the leading edge before the peak. The leading energy is called the precursor energy. The amount of precursor energy differs from one environment to the next. The processing required to correct for the precursor energy is more complex than is required for the trailing edge energy. The symbol period on the x-axis of the graph in FIG. **95** is equal to the length of the 8 chip CCK code word. The 11 chip barker code is only 3 chips longer.

RAKE processing and equalization are two methods used to process and resolve delay spread. A RAKE receiver is a well-known architecture used to remove delay spreads on the order of 100 nsec. The RAKE is structured as a bank of correlators (fingers) with weighed delays, and a combiner. Equalization is an alternate architecture that may be used to correct delay spreads greater than 100 nsec. Multipath causes the signals from the previous symbol to interfere with the signals of the next. This is known as intersymbol interference (ISI). As with ISI, interchip interference (ICI) results when the signals of the previous chip interfere with the signals of the next chip. ISI and ICI are issues for higher data rate systems because the symbol and chip periods are shorter. This is the case for IEEE 802.11a and IEEE 802.11b. Equalization may correct for ISI and ICI. An equalizer is a multi-tapped delay line, which subtracts a delayed and attenuated signal from the actual received signal. However, for environments where delay spreads are greater than 200 nsec, more complex signal processing may be necessary. RAKE processing combined with ISI and ICI equalization is commonly implemented to resolve multipath dispersions of this magnitude.

6.8.3 Multipath Channel Model

In an environment where performance measurements of the same radio are used, in the same location, the results may not agree. This may be due to the changing position of people in the room and slight changes in the environment, which can produce significant changes in the signal power at the radio receiver. A consistent channel model is required to allow comparison of different WLAN systems and to provide consistent results. The IEEE 802.11 Working Group adopted the following channel model as the baseline for predicting multipath for modulations used in IEEE 802.11a (5 GHz) and IEEE 802.11b (2.4 GHz). This model is useful for software simulations predicting performance results for a given implementation. The channel impulse response illustrated in FIG. **96** is composed of complex samples with random uniformly distributed phase and Rayleigh distributed magnitude with average power decaying exponentially.

The mathematical model for the channel is provided as follows:

$$h_k = N\left(0, \frac{1}{2}\sigma_k^2\right) + jN\left(0, \frac{1}{2}\sigma_k^2\right)$$

$$\sigma_k^2 = \sigma_0^2 e^{-kT_s/T_{RMS}}$$

$$\sigma_0^2 = 1 - e^{-T_s/T_{RMS}}$$

Where

$$N\left(0, \frac{1}{2}\sigma_k^2\right)$$

is a zero mean Gaussian random variable with variance

$$\frac{1}{2}\sigma_k^2$$

produced by generating an N(0, 1) and multiplying it by

$$\sigma_k / \sqrt{2}\text{, and } \sigma_0^2 = 1 - e^{-T_s/T_{RMS}}$$

is chosen so that the condition

$$\sigma_k^2 = 1$$

I is satisfied to ensure same average received power.

Let T_S be the sampling period, and let T_{RMS} be the delay spread of the channel. The performance assessment shall be no longer than the smaller of 1/(signal bandwidth) or $T_{RMS}/2$. The number of samples to be taken in the impulse response should ensure sufficient decay of the impulse response tail, e.g. $k_{max}=10\times T_{RMS}/T_S$.

6.8.4 Path Loss in a WLAN System

Another key consideration is the issue of operating range relative to path loss. This consideration plays an important role in determining the size of overlapping WLAN cells and distribution of APs. Path loss calculations are equally important for determining a radio's receiver sensitivity, transmitting power level, and signal to noise ratio (SNR) requirements. As a radio transmits signals to other receivers in a given area, the signal is attenuated as a square of the distance (D). The distance D is the radius of a WLAN cell **9700**, as shown in FIG. **97**. FIG. **98** illustrates a graph and equations related to path loss. The wavelength (lambda) is the ratio between the speed of light and the signal frequency. As the receiver moves away from the transmitter, the receiver's signal power decays until it reaches the receiver's noise floor, at which time the bit error rate becomes unacceptable. For indoor applications beyond 20 feet, propagation losses increase at about 30 dB per 100 feet. This may occur because of a combination of attenuation by walls, ceilings, and furniture. Each wall constructed with sheet rock and wood typically attenuates the signal by 6 dB, while walls constructed with cement block attenuate the signal by 4 dB. However, additional losses may occur depending on the fading characteristics of the operating environment, which is further described in the following section. The same path loss principles apply for all frequency bands. However, as the operating frequency increases from 2.4 GHz to 5 GHz, for example, an additional path loss of 5–10 dB occurs. This results in a smaller cell radius, and may require additional overlapping cells and APs to guarantee operation in the same area as a system operating at 2.4 GHz.

6.8.5 Multipath Fading

Another key consideration is the path loss due to multipath fading. Multipath fading occurs when the reflected signal paths refract off people, furniture, windows, and walls, and scatter the transmitted signal. For example, moving the receiver away from the transmitter by a small distance, even just a few inches, may produce an additional loss of signal power on the order of 20 dB or more. Multipath fading is viewed as two separate factors, and is described as probability distribution functions. The first factor is a characteristic known as log normal fading. These are coefficient products which result when the signal reflects off surfaces and propagates to the receiver. As the signal coefficient products propagate to the receiver, they are summed together with the direct path where they may cancel each other, possibly causing significant attention of the transmitted signal. This is the second factor, known as Rayleigh fading. As previously discussed herein, RAKE architectures and equalization may be used to correct for these effects.

6.8.6 Es/No vs BER Performance

System performance tradeoffs are often made in the decision process when selecting a modulation type and data rate. System tradeoffs in terms of receiver sensitivity, range, and transmit power become very important for developing low cost implementations, especially for higher rate 2.4 GHz IEEE 802.11b systems. FIG. **99** illustrates a graph providing a comparison of the theoretical Es/No vs Bit Error Rate (BER) curves for uncoded QPSK, PBCC 5.5–11 Mbps, CCK 5.5–11 Mbps, and Barker 1 and 2 Mbps. The theoretical curves include additive white Gaussian (AWG) noise in the channel. These curves are provided as a guide to assess the performance for a complete system implementing CCK and PBCC. However, to obtain a better understanding of the overall systems performance, other factors such as multipath, signal fading, carrier phase noise, noise figure, and other implementation losses should be considered in the link budget as part of the systems analysis.

6.8.7 Data Rate vs Aggregate Throughput

The IEEE 802.11 standard defines data rate in terms of symbol rate, or available bit rate. The PPDU data is modulated and transmitted over the RF or IR medium at this rate. This rate is often confused with the aggregate data throughput. The aggregate data rate takes into account overhead associated with protocol frame structure, collisions, and implementation processing delays. The implementation processing delays are associated with frames processed by mobile stations and APs. Simulations may be run in software to estimate the aggregate throughput of the protocol and benchmarked against compliant IEEE 802.11 WLAN systems. However, calculating the aggregate throughput can be complex because there are a number of detailed variables to consider. The protocol overhead includes parameters such as RTS, CTS, ACK frames, (SIF, DIFs, PIFs) interframe space timing, beacon periods and random back-off periods, estimated collisions, PPDU frame size, and RF propagation delays. An useful estimate of the average aggregate throughput of an IEEE 802.11 wireless network is 75% of the data rate for DCF operation, and 85% of the data rate for PCF operation.

6.8.8 WLAN Installation and Site Survey

Many installations begin with a site survey. A site survey may serve a number of purposes. First, the survey may be used to determine the maximum operating range between an AP (fixed location) and mobile stations for a specified transmit RF power level. Second, a survey may help to identify holes in coverage due to multipath, interference sources, and neighboring existing WLAN installations. Third, a survey may be used in cell planning of overlapping BSAs, and for layout of APs, to provide them with hardwired access to existing wired Ethernet LAN infrastructures.

Many equipment manufactures have tests built into their products to conduct such surveys. PC laptops having IEEE 802.11 WLAN adaptor cards, with embedded software tools, are commonly used. In some cases, a spectrum analyzer with special directional antennas may be used to measure path loss through walls and other obstructions, and to pinpoint and identify interference sources. Some of the tests include bit error rate (BER) and packet error rate (PER), and link quality measurements as a function of range. Typically, the tests are recorded using a pair of WLAN adaptors; the first WLAN adaptor is set up in a fixed location, and the second WLAN adaptor is set up as a mobile station. Each environment is different, and the number of APs required for a given installation generally depends upon the presence of holes in the coverage area due to multipath, and signal attenuation through walls, ceilings, and floors. However, on average, for indoor operation, the maximum operating distance between a mobile station and an AP operating at a 2.4 GHz frequency, transmitting at an RF transmit power of +20 dBm (100 mW) at data rates of 1 and 2 Mbps, is approximately 400 feet, and is approximately 100 feet at 11 Mbps.

6.8.9 Interference in the 2.4 GHz Frequency Band

A microwave oven used in household and commercial kitchens is frequently the main interference source in the 2.4 GHz unlicensed frequency band. The magnetron tubes used in microwave ovens radiate a continuous-wave-like (CW-

like) interference that sweeps over tens of megahertz (MHZ) of the 2.4–2.483 GHz band during the positive half cycle of ac line voltage. A microwave oven's EIRP has a maximum generally ranging between 16 and 33 dBm. The power cycle frequency is 50 Hz 20 msec or 60 Hz 16 msec, depending upon the geographical location. In North America, the ac line frequency is 60 Hz, and a microwave oven's magnetron pulses on for 8 msec and off for 8 msec. The maximum packet length defined in the IEEE 802.11 protocol was designed to operate between the 8 msec pulses of microwave energy.

Other sources of interference include neighboring in-band radios. Two types of interference are considered here: The first type is co-channel interference, which is induced by radios from adjacent cells that are on the same channel frequency. Proper cell planning of the channel frequency and hopping patterns, and careful layout of the APs can minimize this interference. The second type of interference is due to systems such as neighboring DSSS and FHSS WLAN networks. Three mechanisms are built into the standard to assist in minimizing the amount of interference. The first mechanism is the clear channel assessment, where the MAC layer protocol provides a method of collision avoidance. The second mechanism is processing gain, which provides some protection from FHSS radios, whose spectrum appears as narrowband interferers. The third mechanism is hop patterns. There is sufficient frequency spacing between pseudo-random hops to minimize the interference due to neighboring DSSS channels. To some degree, legacy 2.4 GHz IEEE 802.11—compliant FHSS and DSSS systems and IEEE 802.11b high-rate WLAN systems may coexist. However, careful cell planning will assist in minimizing the amount of interference a system will experience, especially at the outer fringe of the cell.

6.8.10 Antenna Diversity

Historically antenna diversity has been an effective low-cost alternative solution used to combat and mitigate the effects of multipath and delay spread in WLAN radio receivers. It is relatively easy to implement in the mobile stations and APs, and does not require the signal processing hardware used in other diversity techniques. The objective of antenna diversity is to space the antennas apart from each other to minimize the effects of the uncorrelated multipath at the receiver. By spacing the antennas far apart, the receiver may select and demodulate the larger of the two signals. For 2.4 GHz IEEE 802.11 implementations, the bit length of the preamble sync fields was selected based on these criteria. The antennas are typically spaced anywhere from 0.251 to several lambdas (wavelengths) apart. The amount of separation depends upon the amount of delay-spread tolerance required for the system to operate in a given operating environment. Adding antenna diversity may improve the packet error rate (PER) performance of a wireless link by 2 to 1, as well as improve the availability of the link. There are a number of 2.4 GHz antennas available with different configurations. Patch antennas are commonly used in the mobile client PCMCIA implementations, due at least in part to cost and size constraints. On the other hand, omni-directional antennas may be used at the AP because they provide reasonably optimal antenna coverage. Although antenna diversity is an option in the standard, at a minimum, antenna diversity should always be considered at the AP, as shown in FIG. **100**. This form of diversity will assist in minimizing the risk of packet loss due to multipath and interference, and help to ensure reasonably optimal throughput performance in a system.

7. Appendix

The attached Appendix contained in FIGS. **146** to **212**, which forms part of this patent application, includes schematics of an integrated circuit implementation example of the present invention. This example embodiment is provided solely for illustrative purposes, and is not limiting. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings herein.

8. Conclusions

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, various WLAN components have been described herein as being implemented using various UFT, UFU, and/or UFD, etc., embodiments. These embodiments have been described for illustrative purposes only, and are not limiting. Such WLAN components can alternatively be implements using other frequency translation embodiments described herein, and/or using equivalents thereof, as will be apparent to persons skilled in the relevant arts based on the teachings contained herein.

Thus, while various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, wherein said frequency down-conversion module comprises a switch module and a storage element, wherein a first node of said switch module is coupled to a first node of said storage element, wherein said storage element comprises a capacitor, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer.

2. The WLAN device of claim **1**, wherein said first frequency down-conversion module receives said input RF signal, wherein said first frequency down-conversion module down-converts said input RF signal according to a first control signal and outputs a first down-converted signal;

wherein said receiver further comprises:

a second frequency down-conversion module that receives said input RF signal, wherein said second

frequency down-conversion module down-converts said input RF signal according to a second control signal and outputs a second down-converted signal; and

an adder module that adds said second down-converted signal and said first down-converted signal and outputs a down-converted demodulated signal.

3. The WLAN device of claim 2, wherein said first control signal comprises a first control pulse and said second control signal comprises a second control pulse, wherein said second control pulse is delayed relative to said first control pulse by 0.5+n cycles of said input RF signal, wherein n may be any integer greater than or equal to 1.

4. The WLAN device of claim 3, wherein said first frequency down-conversion module under-samples said input RF signal according to said first control signal, and said second frequency down-conversion module under-samples said input RF signal according to said second control signal.

5. The WLAN device of claim 2, wherein said second frequency down-conversion modules comprises a second switch module and a second storage element, wherein a first node of said second switch module is coupled to a node of said second storage element.

6. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a first frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said first frequency down-conversion module receives said input RF signal, wherein said first frequency down-conversion module down-converts said input RF signal according to a first control signal and outputs a first down-converted signal,

wherein said receiver further comprises:

a second frequency down-conversion module that receives said input RF signal, wherein said second frequency down-conversion module down-converts said input RF signal according to a second control signal and outputs a second down-converted signal; and

an adder module that adds said second down-converted signal and said first down-converted signal and outputs a down-converted demodulated signal,

wherein said first and said second frequency down-conversion modules each comprise a switch module and a storage element, wherein a first node of said each switch module is coupled to a node of the corresponding said each storage element,

wherein said each storage element comprises a capacitor, wherein said each capacitor corresponding to said first and said second frequency down-conversion modules reduces a DC offset voltage in said first down-converted signal to produce a first reduced DC offset voltage and said second down-converted signal to produce a second reduced DC offset voltage, wherein said first and said second DC offset voltages are at least due to charge injection effects in said first and said second frequency down-conversion modules, respectively.

7. The WLAN device of claim 2, wherein said adder module comprises a differential amplifier.

8. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a first frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said first frequency down-conversion module receives said input RF signal, wherein said first frequency down-conversion module down-converts said input RF signal according to a first control signal and outputs a first down-converted signal;

wherein said receiver further comprises:

a second frequency down-conversion module that receives said input RF signal, wherein said second frequency down-conversion module down-converts said input RF signal according to a second control signal and outputs a second down-converted signal;

a first adder module that adds said second down-converted signal and said first down-converted signal and outputs an I-phase demodulated signal;

a third frequency down-conversion module that receives said input RF signal, wherein said third UFD frequency down-conversion module down-converts said input RF signal according to a third control signal and outputs a third down-converted signal;

a fourth frequency down-conversion module that receives said input RF signal, wherein said fourth frequency down-conversion module down-converts said input RF signal according to a fourth control signal and outputs a fourth down-converted signal; and

a second adder module that adds said fourth down-converted signal and said third down-converted signal and outputs a Q-phase demodulated signal.

9. The WLAN device of claim 8, wherein said first adder and said second adder each comprise a differential amplifier.

10. The WLAN device of claim 8, further comprising a low-noise amplifier that amplifies said input RF signal.

11. The WLAN device of claim 8, wherein a control signal pulse of said second control signal occurs 1.5 cycles of a frequency of said input RF signal after the occurrence of a control signal pulse of said first control signal;

wherein a control signal pulse of said fourth control signal occurs 1.5 cycles of said frequency of said input RF signal after the occurrence of a control signal pulse of said third control signal; and

wherein said third control signal pulse occurs 0.75 cycles of said frequency of said input RF signal after the occurrence of said first control signal pulse.

12. The WLAN device of claim 11, wherein a re-radiated signal comprises attenuated components of said control signal pulses of said first, second, third, and fourth control signals to form a cumulative frequency, wherein a ratio of said cumulative frequency of said re-radiated signal to said frequency of said input RF signal is substantially equal to 4:3.

13. The WLAN device of claim 8, wherein said first control signal comprises a first control signal pulse, said second control signal comprises a second control signal pulse, said third control signal comprises a third control signal pulse, and said fourth control signal comprises a fourth control signal pulse;

wherein a potentially re-radiated signal comprises attenuated components of said first, second, third, and fourth control signal pulses to form a cumulative frequency; and

wherein said cumulative frequency of said potentially re-radiated signal is chosen to be greater than a frequency of said input RF signal.

14. The WLAN device of claim 8, wherein a first DC offset voltage in said first down-converted signal due to said first frequency down-conversion module and a second DC offset voltage in said second down-converted signal due to said second frequency down-conversion module substantially cancel from said I-phase demodulated signal in said first adder; and

wherein a third DC offset voltage in said third down-converted signal due to said third frequency down-conversion module and a fourth DC offset voltage in said fourth down-converted signal due to said fourth frequency down-conversion module substantially cancel from said Q-phase demodulated signal in said second adder.

15. The WLAN device of claim 8, wherein said first frequency down-conversion module under-samples said input RF signal according to said first control signal, said second frequency down-conversion module under-samples said input RF signal according to said second control signal, said third frequency down-conversion module under-samples said input RF signal according to said third control signal, and said fourth frequency down-conversion module under-samples said input RF signal according to said fourth control signal.

16. The WLAN device of claim 8, wherein said first, said second, said third, and said fourth frequency down-conversion modules each comprise a switch and a storage element, wherein a first node of said each switch is coupled to a node of the corresponding said each storage element.

17. The WLAN device of claim 16, wherein said each storage element comprises a capacitor.

18. The WLAN device of claim 17, wherein said each capacitor corresponding to said first, said second, said third, and said fourth frequency down-conversion modules reduces a DC offset voltage in said first down-converted signal, said second down-converted signal, said third down-converted signal, and said fourth down-converted signal at least due to charge injection effects in said first, said second, said third, and said fourth frequency down-conversion modules, respectively.

19. The WLAN device of claim 8, further comprising a control signal generator that outputs said first, said second, said third, and said fourth control signal.

20. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said transmitter receives an information signal, wherein said information signal comprises an I baseband signal and a Q baseband signal, wherein said transmitter comprises:

(1) a first modulator that receives said I baseband signal and outputs a modulated I phase signal;

(2) a second modulator that receives said Q baseband signal and outputs a modulated Q phase signal;

(3) first differential sampling means for sampling said modulated I phase signal according to a first control signal and a second control signal, to generate an I harmonically rich signal, wherein said second control signal is phase shifted relative to said first control signal;

(4) second differential sampling means for sampling said modulated Q phase signal according to said first control signal and said second control signal, to generate a Q harmonically rich signal;

(5) means for combining said I harmonically rich signal and said Q harmonically rich signal, to generate an I/Q harmonically rich signal, said I/Q harmonically rich signal having multiple harmonic images that contain amplitude and frequency information for reconstruction of the I and Q phase signals;

wherein said first and second control signals have a period of T_S so that said harmonic images repeat at multiples of $1/T_S$;

wherein said first and second control signal comprise pulses that operate to improve energy transfer to a desired harmonic image in said corresponding I and Q harmonically rich signals; and

wherein said output RF signal comprises said I/Q harmonically rich signal.

21. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal, and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said transmitter receives an information signal, wherein said transmitter comprises:

a modulator that receives said information signal and outputs a modulated signal;

a buffer/inverter, for receiving said modulated signal and generating an inverted modulated signal;

a first controlled switch, coupled to an output of said buffer/inverter, said first controlled switch shunting said modulated signal to ground according to a first control signal, and resulting in a first harmonically rich signal;

a second controlled switch coupled to a second output of said buffer/inverter, said second controlled switch shunting said inverted modulated signal to ground according to a second control signal, and resulting in a second harmonically rich signal;

a combiner, coupled to an output of said first controlled switch and an output of said second controlled switch, said combiner combining said first harmonically rich signal and said second harmonically rich signal, resulting in a third harmonically rich signal;

wherein said first control signal and said second control signal comprise pulses that operate to improve energy transfer to a desired harmonic in said third harmonically rich signal;

wherein said first control signal and said second control signal are phase shifted with respect to each other; and

wherein said output RF signal comprises said third harmonically rich signal.

22. The WLAN device of claim **21**, wherein:

said first controlled switch comprises a first field effect transistor (FET), a gate of said first FET coupled to said first control signal, a source of said first FET receiving said modulated signal and outputting said first harmonically rich signal, and a drain of said first FET coupled to ground; and

said second controlled switch comprises a second field effect transistor (FET), a gate of said second FET coupled to said second control signal, a source of said second FET receiving said inverted modulated signal and outputting said second harmonically rich signal, and a drain of said second FET coupled to ground.

23. The WLAN device of claim **22**, wherein said first FET and said second FET alternately shunt said modulated signal and said inverted modulated signal to ground, respectively, according to said first control signal and said second control signal, to generate said harmonically rich signals.

24. The WLAN device of claim **1**, wherein said physical layer comprises a direct sequence spread spectrum (DSSS) physical layer, wherein said input RF signal comprises a differential binary phase shift keying modulated signal or a differential quadrature phase shift keying modulated signal.

25. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a direct sequence spread spectrum (DSSS) physical layer, wherein said input RF signal comprises a differential binary phase shift keying modulated signal or a differential quadrature phase shift keying modulated signal,

wherein said receiver comprises a differential phase shift keying modulation receiver, wherein said differential phase shift keying modulation receiver receives said input RF signal and outputs a down-converted demodulated signal, and wherein said physical medium dependent sublayer further comprises:

a de-spread correlator that receives said down-converted demodulated signal and receives an 11-bit Barker word, wherein said de-spread correlator outputs a de-spread signal; and

a de-scrambler that receives said de-spread signal and outputs at least a portion of at least one PPDU frame.

26. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal, and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a direct sequence spread spectrum (DSSS) physical layer, wherein said input RF signal comprises a differential binary phase shift keying modulated signal or a differential quadrature phase shift keying modulated signal,

wherein said receiver comprises a differential phase shift keying modulation receiver, and wherein said physical medium dependent sublayer further comprises:

a de-spread correlator that receives said input RF signal and receives an 11-bit Barker word, wherein said de-spread correlator outputs a de-spread signal; and

a de-scrambler;

wherein said differential phase shift keying modulation receiver receives said de-spread signal and outputs a down-converted demodulated signal; and

wherein said de-scrambler receives said down-converted demodulated signal and outputs at least a portion of at least one PPDU frame.

27. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence pro-

cedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a direct sequence spread spectrum (DSSS) physical layer, wherein said input RF signal comprises a differential binary phase shift keying modulated signal or a differential quadrature phase shift keying modulated signal,

wherein said receiver comprises a combined differential phase shift keying (DPSK) modulation receiver and de-spread correlator, wherein said combined DPSK modulation receiver and de-spreader correlator receives said input RF signal and receives an 11-bit Barker word, wherein said combined DPSK modulation receiver and de-spread correlator outputs a demodulated/de-spread signal, wherein said physical medium dependent sublayer further comprises:

a de-scrambler that receives said demodulated/de-spread signal and outputs at least a portion of at least one PPDU frame.

28. The WLAN device of claim **1**, wherein said physical layer comprises a direct sequence spread spectrum (DSSS) physical layer, wherein said output RF signal comprises a differential binary phase shift keying modulated signal or a differential quadrature phase shift keying modulated signal.

29. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a direct sequence spread spectrum (DSSS) physical layer, wherein said output RF signal comprises a differential binary phase shift keying modulated signal or a differential quadrature phase shift keying modulated signal,

wherein said transmitter comprises a differential phase shift keying modulation transmitter, and wherein said physical medium dependent sublayer further comprises:

a scrambler that receives at least a portion of at least one PPDU frame and outputs a scrambled at least one PPDU frame portion;

a modulo-2 adder that receives said scrambled at least one PPDU frame portion, wherein said modulo-2 adder receives an 11-bit Barker word, and wherein said scrambler outputs a spread signal; and

a transmit mask filter that receives said spread signal and outputs a filtered signal; and

wherein said differential phase shift keying modulation transmitter receives said filtered signal, wherein said differential phase shift keying modulation transmitter transmits said output RF signal.

30. The WLAN device of claim **1**, wherein said physical layer comprises a frequency hopping spread spectrum physical layer, wherein said input RF signal comprises a 2-level or 4-level Gaussian frequency shift keying modulated signal.

31. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a frequency hopping spread spectrum physical layer, wherein said input RF signal comprises a 2-level or 4-level Gaussian frequency shift keying modulated signal,

wherein said receiver comprises a Gaussian frequency shift keying modulation receiver, wherein said Gaussian frequency shift keying modulation receiver receives said input RF signal, wherein said Gaussian frequency shift keying modulation receiver outputs a demodulated signal, wherein said physical medium dependent sublayer further comprises:

a data de-whitener that receives said demodulated signal and outputs at least a portion of at least one PPDU frame.

32. The WLAN device of claim **1**, wherein said physical layer comprises a frequency hopping spread spectrum physical layer, wherein said output RF signal comprises a 2-level or 4-level Gaussian frequency shift keying modulated signal.

33. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a frequency hopping spread spectrum physical layer, wherein said output RF signal comprises a 2-level or 4-level Gaussian frequency shift keying modulated signal,

wherein said transmitter comprises a Gaussian frequency shift keying modulation transmitter, wherein said physical medium dependent sublayer further comprises:

a data whitener that receives at least a portion of at least one PPDU frame and outputs a whitened at least one PPDU frame portion; and

a transmit Gaussian shaping filter that receives said at least one whitened at least one PPDU frame portion and outputs a filtered signal;

wherein said Gaussian frequency shift keying modulation transmitter receives said filtered signal, wherein said Gaussian frequency shift keying modulation transmitter transmits said output RF signal.

34. The WLAN device of claim **33**, wherein said physical medium dependent sublayer further comprises:

a symbol mapping module that maps said whitened at least one PPDU frame portion.

35. The WLAN device of claim **34**, wherein said physical layer comprises an orthogonal frequency division multiplexing physical layer, wherein said input RF signal comprises a binary phase shift keying modulated signal, a quadrature phase shift keying modulated signal, a 16-QAM modulated signal, or a 64-QAM modulated signal.

36. A wireless local area network (WLAN) device, comprising:

a medium access control layer, and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal, and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said receiver comprises a phase shift keying/quadrature amplitude modulation (PSK/QAM) receiver, wherein said PSK/QAM modulation receiver receives said RF input signal and outputs a demodulated signal, wherein said physical medium dependent sublayer further comprises:

a fast Fourier transform (FFT) module that receives said demodulated signal and outputs a FFT module output signal;

a bit de-interleaving and de-mapping module that receives said FFT module output signal and outputs an encoded at least one data frame; and

a convolutional code decoder that receives said encoded at least one data frame and outputs at least a portion of at least one PPDU frame.

37. The WLAN device of claim **36**, wherein said physical medium dependent sublayer further comprises:

a symbol shaping module that shapes said encoded signal.

38. The WLAN device of claim **1**, wherein said physical layer comprises an orthogonal frequency division multiplexing physical layer, wherein said output RF signal comprises a binary phase shift keying modulated signal, a quadrature phase shift keying modulated signal, a 16-QAM modulated signal, or a 64-QAM modulated signal.

39. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises an orthogonal frequency division multiplexing physical layer, wherein said output RF signal comprises a binary phase shift keying modulated signal, a quadrature phase shift keying modulated signal, a 16-QAM modulated signal, or a 64-QAM modulated signal,

wherein said transmitter comprises a phase shift keying/quadrature amplitude modulation (PSK/QAM) transmitter, wherein said physical medium dependent sublayer further comprises:

a convolutional encoder that receives at least a portion of at least a PPDU frame and outputs an encoded at least one PPDU frame portion;

a bit interleaving and mapping module that receives said encoded at least one PPDU frame portion and outputs at least one bit interleaved and mapped signal; and

an inverse fast Fourier transform (IFFT) module that receives said at least one bit interleaved and mapped signal and outputs an IFFT module output signal; and

wherein said PSK/QAM modulation transmitter receives said IFFT module output signal and transmits said output RF signal.

40. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a high rate direct sequence spread spectrum physical layer, wherein said transmitter comprises a phase shift keying (PSK) modulation transmitter, wherein said output RF signal comprises a packet binary convolutional coding modulated signal, wherein said physical medium dependent sublayer further comprises:

a scrambler that receives at least a portion of at least one PPDU frame and outputs a scrambled at least one PPDU frame portion;

a binary convolutional code encoder that receives said scrambled at least one PPDU frame portion and outputs an encoded signal;

a cover code sequence generator that receives a 16-bit cover code seed and outputs a cover sequence; and

a PSK cover code map module that receives said cover sequence and said encoded signal, and outputs a mapped signal; and

wherein said PSK modulation transmitter receives said mapped signal, wherein said PSK modulation transmitter transmits said output RF signal.

41. A wireless local area network (WLAN) device, comprising:

a medium access control layer; and

a physical layer coupled to said medium access control layer, comprising:

a physical medium dependent sublayer, wherein said physical medium dependent sublayer comprises:

a receiver that receives an input radio frequency (RF) signal, wherein said receiver comprises a frequency down-conversion module, and

a transmitter that transmits an output RF signal; and

a physical layer convergence procedure sublayer coupled to said physical medium dependent sublayer, wherein said physical layer convergence procedure sublayer controls frame exchange between said medium access control layer and said physical layer,

wherein said physical layer comprises a high rate direct sequence spread spectrum physical layer, wherein said transmitter comprises a differential quadrature phase shift keying (DQPSK) modulation transmitter, wherein said output RF signal comprises a complementary code keying modulated signal, wherein said physical medium dependent sublayer further comprises:

a scrambler that receives at least one data frame and outputs a scrambled at least one data frame;

a data multiplexer that receives said scrambled at least one data frame, wherein said data multiplexer outputs a first multiplexed data portion and a second multiplexed data portion; and

a complex code selector module that receives said first multiplexed data portion and outputs a selected code; and

wherein said DQPSK modulation transmitter receives said selected code and said second multiplexed data portion, wherein said DQPSK modulation transmitter transmits said output RF signal.

42. The WLAN device of claim **1**, wherein said medium access control layer and said physical layer are comprised by a network adaptor or a network interface card.

43. The WLAN device of claim **1**, wherein said transmitter comprises a frequency up-conversion module, wherein said frequency up-conversion module comprises a second switch module.

44. The WLAN device of claim **43**, wherein said second switch module is configured to amplitude modulate, frequency modulate, or phase modulate a carrier signal with an information signal.

45. The WLAN device of claim **44**, wherein said transmitter further comprises a third switch module, wherein said third and second switch modules are configured to modulate and up-convert information signals to in-phase and quadrature-phase channels.

46. The WLAN device of claim **45**, wherein said information signals are modulated and up-converted according to quadrature amplitude modulation, differential quadrature phase shift keying, quadrature phase shift keying, complementary code keying, or packet binary convolutional coding modulation schemes.

47. The WLAN device of claim **1**, wherein said input RF signal is an amplitude modulated, frequency modulated, or phase modulated signal, wherein said switch module is configured to demodulate said input RF signal to an information signal.

48. The WLAN device of claim **47**, wherein said receiver further comprises a second switch module, wherein said first and second switch modules are configured to down-convert and demodulate in-phase and quadrature-phase components of a received signal.

49. The WLAN device of claim **48**, wherein said received signal comprises a quadrature amplitude modulated, differential quadrature phase shift keying modulated, quadrature phase shift keying modulated, complementary code keying, or packet binary convolutional coding modulated signal.

50. The WLAN device of claim **1**, wherein said frequency down-conversion module is tuned for at least one frequency substantially equal to one of or between 2.402 Giga Hertz and 2.495 Giga Hertz.

51. The WLAN device of claim **1**, wherein the device is an access point, computer, personal data assistant (PDA), automatic identification data collection device, telephone, network device, or combination thereof.

52. The WLAN device of claim **20**, wherein said first modulator and said second modulator amplitude modulate, frequency modulate, or phase modulate a carrier signal frequency with said I baseband signal and said Q baseband signal, respectively.

53. The WLAN device of claim **20**, wherein said first modulator and said second modulator each comprise a digital-to-analog (D/A) converter.

54. The WLAN device of claim **21**, wherein said modulator amplitude modulates, frequency modulates, or phase modulates a carrier signal frequency with said information signal.

55. The WLAN device of claim **21**, wherein said modulator comprises a digital-to-analog (D/A) converter.

56. The WLAN device of claim **1**, wherein a second node of said switch module is coupled to a reference potential.

57. The WLAN device of claim **1**, wherein a second node of said storage element is coupled to a reference potential.

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