IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

ICPILLAR LLC,	§	
	§	
Plaintiff,	§	
	§	Case No. 1:23-CV-00282-ADA
v.	§	
	§	Jury Trial Requested
ARM LIMITED and ARM, INC.,	§	
	§	
	§	
Defendants.	§	

DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to the current Standing Order Governing Proceedings (OGP) 4-3 – Patent Cases ("OGP") and the Court's Scheduling Order (Dkt. 31), Defendants Arm Limited and Arm, Inc. (collectively, "Arm") respectfully submit these Preliminary Invalidity Contentions.

The Asserted Claims, as reflected in Plaintiff ICPillar LLC's ("ICPillar") Preliminary Infringement Contentions, are claims 1, 5, 6, 8, and 14 of U.S. Patent No. 8,924,899 (the "'899 Patent") and claims 1, 5, 6, 8, 9, 15, and 16 of U.S. Patent No. 9,367,657 (the "'657 Patent"). The '899 Patent and the '657 Patent are referred to collectively as the "Asserted Patents."

I. PRELIMINARY STATEMENT

These Preliminary Invalidity Contentions are preliminary in nature and do not address claim construction or noninfringement. Arm reserves all rights with respect to such issues, including its position that the Asserted Claims of the Asserted Patents should be construed in a particular manner and/or are not infringed. These Preliminary Invalidity Contentions are based on Arm's current knowledge, understanding, and belief of the Asserted Patents and prior art, of ICPillar's infringement theories (as disclosed in the Preliminary Infringement Contentions), and of the facts and other information available as of the date of service. Arm's investigation,

discovery, and analysis of information related to this action is ongoing. Additional discovery and/or orders of the Court may require Arm to amend or supplement these Preliminary Invalidity Contentions, and Arm expressly reserves the right to do so as the case proceeds. These contentions represent Arm's good-faith effort to provide a comprehensive identification of prior art relevant to this case, but Arm reserves the right to modify or supplement its prior art list and Preliminary Invalidity Contentions at a later time with, or based upon, pertinent information that may be subsequently discovered.

A. Identification of and Citation to Prior Art

The identification of any patent or patent publication in these Preliminary Invalidity Contentions shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world. The identification of any specifications published by any standard-setting organization shall be deemed to include any earlier or later version of the specifications with the same or similar disclosures. Moreover, the citation to any specifications published by standard-setting organizations shall be deemed to include any product that implements such specifications and that would qualify as prior art for purposes of 35 U.S.C. §§ 102 and 103.

Arm's claim charts cite to particular teachings and disclosures of the prior art as applied to features of the Asserted Claims. Persons of ordinary skill in the art may, however, view an item of prior art in the context of other publications, literature, products, and understanding. As such, the cited portions are only exemplary, and Arm reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses particular a claim limitation. Arm further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish bases for

combinations of certain cited references that render the Asserted Claims obvious. Further, for any combination, Arm reserves the right to rely additionally on information generally known to those skilled in the art or on common sense.

The prior art references discussed in the accompanying claim charts may disclose the elements of the Asserted Claims explicitly or inherently, or they may be relied upon to show the state of the art in the relevant time frame. The suggested obviousness combinations are provided in the alternative to Arm's anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

Where Arm identifies a particular figure in a prior art reference, that identification is intended to encompass the caption and description of the figure and any text relating to the figure, and not merely the figure itself. Similarly, where an identified portion of text refers to a figure or other material, that identification is intended to encompass the referenced figure or other material as well.

B. No Waiver

Nothing in these Preliminary Invalidity Contentions is intended, nor should be construed, as a waiver of any claim construction argument, noninfringement position, or argument under 35 U.S.C. §§ 101 or 112. Arm's statements in these Preliminary Invalidity Contentions (including in the accompanying claim charts) reflect Arm's present understanding of the purported scope of the Asserted Claims as alleged by ICPillar in its Preliminary Infringement Contentions, as best those contentions can be understood in light of their present deficiencies. For the avoidance of doubt, these contentions are not intended to present or argue in favor of any construction of the Asserted Claims, and Arm expressly reserves the right to present constructions that differ from any construction that may be alleged to underlie these contentions. The Court established separate

deadlines for the parties' proposed claim constructions, and Arm will disclose its proposed constructions accordingly.

Moreover, these Preliminary Invalidity Contentions do not constitute an acquiescence to ICPillar's interpretation of any Asserted Claims to the extent they depart from the plain meaning of the Asserted Claims and from the proper scope of the claims as may be subsequently construed by the Court. Arm disagrees with ICPillar's apparent positions as to the purported scope of the Asserted Claims to the extent they seek to expand the scope of the Asserted Claims beyond their proper construction.

The Asserted Claims have not yet been construed by the Court in this case and, thus, Arm has not yet had the opportunity to compare the Asserted Claims of the Asserted Patents (as construed by the Court) with the prior art. Arm reserves the right to amend, supplement, or materially modify its Preliminary Invalidity Contentions after the claims of the Asserted Patents have been construed by the Court in this case. Arm also reserves the right to amend, supplement, or materially modify their Preliminary Invalidity Contentions in response to any claim construction positions that ICPillar may take. Arm also reserves the right to assert that a claim is indefinite, not enabled, or fails to meet the written description requirement of 35 U.S.C. § 112 based on any claim construction position ICPillar may take in this case or based on any claim construction the Court may adopt in this case.

C. No Admission

Nothing disclosed in these Preliminary Invalidity Contentions is an admission or acknowledgement that any product accused of infringement by ICPillar in its Preliminary Infringement Contentions (the "Accused Products"), or any of Arm's other products or services, infringes any of the Asserted Claims.

Arm further notes that ICPillar appears to rely upon overly broad constructions of the Asserted Claims. At the same time, ICPillar's Preliminary Infringement Contentions are in most places too general and vague to discern ICPillar's infringement theories and how exactly ICPillar contends each Accused Product meets or practices each element of the Asserted Claims.

For example, ICPillar's Preliminary Infringement Contentions fail to clearly identify the aspects or features of the Accused Products that ICPillar contends meet the elements of the Asserted Claims. As a result, Arm has been hindered in its ability to prepare these Preliminary Invalidity Contentions. In addition, ICPillar's Preliminary Infringement Contentions, in many cases, fail to put Arm on notice of ICPillar's interpretation of the Asserted Claims, further hindering Arm's ability to identify relevant prior art.

In its Preliminary Infringement Contentions, ICPillar has not identified any doctrine of equivalents theories. Arm has relied on ICPillar's representation that it has no doctrine of equivalents theories in preparing these Preliminary Invalidity Contentions, and any attempt by ICPillar to present an untimely doctrine of equivalents argument would be severely prejudicial to Arm. To the extent that ICPillar is later permitted by the Court to amend its contentions to cure the current deficiencies or to pursue any currently undisclosed doctrine of equivalents theories, Arm expressly reserves the right to supplement or amend these Preliminary Invalidity Contentions to account for such amendments.

To the extent that any of the prior art references disclose the same functionality or feature of any of the Accused Products, Arm reserves the right to argue that said feature or functionality does not practice any element of any of the Asserted Claims, and to argue, in the alternative, that if such a feature or functionality is found to practice any element of any of the Asserted Claims,

then the prior art reference demonstrates that the element is not novel, is obvious, and/or is otherwise not patentable.

Attached to these Preliminary Invalidity Contentions are representative claim charts that demonstrate how the Asserted Claims of the Asserted Patents are invalid in view of certain prior art. The references cited in the attached claim charts may disclose the limitations of the Asserted Claims expressly and/or inherently. The suggested obviousness combinations may be presented in conjunction with or in the alternative to Arm's contentions regarding anticipation. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

D. Reservation of Rights

Prior art not included in this disclosure may become relevant later in this case. Arm is currently unaware of the extent, if any, to which ICPillar will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Arm. Arm reserves the right to identify other references that would have made the addition of the allegedly missing limitation to the disclosed device or method obvious or show that the allegedly missing limitation would have been known or readily apparent to one of ordinary skill in the art at the time of the invention in light of the disclosure of the prior art at issue.

Arm also reserves the right to amend its Preliminary Invalidity Contentions with any additional, potential prior art known by ICPillar, but not yet disclosed to Arm.

Arm additionally reserves the right to challenge any contention that an Asserted Claim is entitled to a priority date earlier than the filing date of the patent application that matured into the respective Asserted Patent. Arm further reserves the right to seek discovery regarding any alleged

conception and reduction to practice dates, as appropriate, and to demonstrate earlier invention by other parties under 35 U.S.C. § 102(a)(2).

Arm further reserves the right to take discovery on the issues of improper inventorship under 35 U.S.C. § 115(a), public use and/or the on-sale bar under 35 U.S.C. § 102(a), and/or applicants' failure to comply with 35 U.S.C. § 112. Arm accordingly reserves all rights to further supplement or amend these Preliminary Invalidity Contentions if and when further information is discovered or becomes available, including to add contentions that any and all parent applications to the Asserted Patents are prior art to, and therefore invalidating of, one or more of the Asserted Claims, and/or that the Asserted Claims are invalid under the doctrine of obviousness-type double patenting in light of same.

Arm provides these Preliminary Invalidity Contentions only for the Asserted Claims but reserves the right to seek invalidation of all claims in each of the Asserted Patents.

E. Ongoing Investigation

Arm's investigation of ICPillar's claims is ongoing, and Arm expressly reserves the right to amend its disclosures and document production to account for evidence uncovered as its investigation continues. Such amendments include identifying and relying on additional prior art references that may result from Arm's further search and analysis. Arm reserves the right to supplement these contentions in light of any additional prior art of which ICPillar is aware and has yet to disclose to Arm in discovery. Arm anticipates issuing subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed in these Preliminary Invalidity Contentions and/or additional prior art. These third parties include, but are not limited to, the authors, employers of authors, inventors, assignees, or former or current employees of assignees, of the references or systems/products identified in these

Preliminary Invalidity Contentions. Arm reserves the right to supplement these Preliminary Invalidity Contentions in light of any newly discovered information produced by such third parties.

II. STATE OF THE ART

This section is intended to set forth a summary of Arm's current understanding of the state of the art for the general subject matter of the Asserted Patents. Arm expressly reserves the right to rely on each of the prior art references disclosed below and in Exhibits 899-A, 899-B, 657-A, and 657-B as it relates to demonstrating the relevant state of the art. Arm also reserves the right to rely on the discussions of the state of the art and prior art for the Asserted Patents and their respective file histories in explaining the state of the art and the ways that each respective prior art reference corresponds with the Asserted Claims. Arm further expressly reserves the right to supplement its summary of the state of the art, including for example, with information from any of the authors, named inventors, or assignees of any of the prior art references, by personnel familiar with systems/products based on any of the prior art, or by technical experts retained on behalf of any party.

A. Core Concepts Underlying The Asserted Claims Were Well Known

By the priority date(s) of the Asserted Patents, many, if not all, of the core concepts underlying the Asserted Claims were well-known to persons of ordinary skill in the art. Examples of these well-known concepts are included below, but Arm expressly reserves the right to identify and/or rely upon other well-known concepts disclosed in the prior art.

i. Automated Circuit Design Was Well Known

By the time of the alleged invention of the Asserted Patents, the concept of automated circuit design, including automated design of integrated circuits (ICs), was well known to those of ordinary skill in the art. In fact:

> By the mid-1970's as computers had developed to the point where bit-mapped graphics could be rendered in real-time, and as integrated circuit densities increased into the thousands of devices per chip, automated graphical layout programs began to appear that permitted the designer to directly 'draw' the circuit artwork on a computer monitor using interactive graphical tools.

U.S. 9,275,185 (McIlrath) at 1:50-56. According to McIlrath, examples of these programs are described in, among other places, *An Interactive Graphics System for the Design of Integrated Circuits* by B. Infante et al. and *ICARUS: An Interactive Integrated Circuit Layout Program* by D.G. Fairbairn et al., both presented at the 15th Conference on Design Automation in June 1978.

As computer performance improved, so too did these CAD tools. In the 1980s, GUI-based design tools were available that allowed a user to input specifications and automatically generate a system controller, select necessary integrated circuit hardware cells, and produce data and control paths for operation of the integrated circuit. An example of such a system was described in a patent assigned to International Chip Corporation. *See generally* U.S. 4,922,432 (Kobayashi).

By the 1990s, CAD tools allowed not only the design and development of ICs, but automated synthesis and optimization processes:

> Several types of computer-aided design (CAD) tools are available to design and fabricate integrated circuits (IC). Such computer-aided or automated IC design tools can include modules or programs addressing both the synthesis and optimization processes.

U.S. 6,862,563 (Hakewill) at 1:28-32. The well-known use of CAD tools to design circuits and semiconductor devices was also described by Synopsys, Inc. in a series of patents to Hakewill. *See, e.g.*, U.S. 8,386,972 (Hakewill 972) at 1:20-44; U.S. Patent No. 9,171,114 (Hakewill 114) at 1:20-44.

As another example, the use of hardware description language in designing and synthesizing integrated circuits was well known. *See, e.g.*, U.S. 7,275,233 (McElvain) at Abstract,

1:12-16, 1:20-51; U.S. 7,454,732 (McElvain 732) at Abstract, 1:19-23, 1:27-40, 13:36-14:6. More generally, the use of CAD tools to design integrated circuits was well known. *See, e.g.*, U.S. 6,564,363 (Dahl) at Abstract, 1:30-62, 2:30-36, 5:10-36; U.S. 8,527,934 (Ginetti) at 1:32-33, 1:46-52, 3:7-25, 5:18-22. In fact, the use of electronic design automation (EDA) and CAD tools was well known throughout the industry, such as for designing and developing Application Specific Integrated Circuits (ASICs), Field-Programmable Gate Arrays (FPGAs), and Programmable Logic Devices (PLDs). *See, e.g.*, U.S. 9,171,114 (Hakewill 114) at 5:60-67, 19:16-31 (describing the use of CAD tools to design various integrated circuits, including ASICs and FPGAs); U.S. Patent Application Publication No. 2007/0200596 (Lee), ¶¶ 40-41 (describing use of "industry-standard EDA tools" and known "CAD tools" for circuit design, including design of PLDs).

It was also well known that automated IC design tools could have libraries of features, functionalities, and other descriptions that could be accessed during the design or synthesis processes. *See, e.g.*, U.S. 9,268,578 (Cummings) at 6:17-64, 7:39-8:2.

In fact, even the Asserted Patents recognize that automated circuit design was known prior to the alleged invention and specifically reference computer-aided design tools available from multiple companies, including Synopsys, Cadence, and Magma. *See, e.g.*, '899 Patent at 13:1-17.

These tools are also disclosed in, among other places, the passages cited for claim element 1[c] in each chart in Exhibit 899-A.

ii. Computer-Based ASIC Design Tools Were Well Known

By the time of the alleged invention of the Asserted Patents, the use of computer-based ASIC (or "application-specific integrated circuit") design tools was well known. For example, as described by inventors from Altera Corporation, "ASIC design tools are available from Synopsys of Mountain View, Calif. and Avant! of Fremont, Calif." *See* U.S. 6,976,239 (Allen) at 2:32-36.

These tools are also disclosed in, among other places, the passages cited for claim 8 in each chart in Exhibit 657-A.

iii. Automated Simulation and Debugging of Circuit Designs Was Well Known

By the time of the alleged invention of the Asserted Patents, the concept of automated and/or software-based simulation and debugging of circuit designs, including integrated circuit designs, was well known to those of ordinary skill in the art. For example, ARC International disclosed in a patent to Hakewill et al. that software tools could be used to generate descriptive models of a complete processor to enhance the simulation and synthesis processes. *See, e.g.*, U.S. 6,862,563 (Hakewill) at 2:40-63, 3:4-29, 8:10-27, 10:22-34.

In general, the use of computers to simulate and debug integrated circuit designs was well known. *See, e.g.*, U.S. 7,366,652 (Wang) at 1:16-20, 1:22-42, 1:45-2:4, 3:26-48, 4:16-32; U.S. 8,943,452 (Hsu) at Abstract, 1:19-24, 2:33-44, 3:37-56; U.S. 9,195,784 (Tseng 784) at Abstract, 1:24-43, 2:11-28, 11:34-55. This includes, among other things, real-time simulation, design-checking, and debugging of integrated circuit designs. *See, e.g.*, U.S. 8,807,948 (Luo) at Abstract, 1:6-10, 1:14-40, 2:24-55, 3:16-35, 4:23-39. The need to simulate both hardware and software aspects of integrated circuits, including SoCs, was likewise known and recognized in the industry. *See, e.g.*, U.S. Patent Application Publication No. 2002/0059054 (Bade), ¶¶ 3, 12, 16-17, 21, 85, 91-94, 96-97, 99-100, 103-104, 109.

This functionality is also disclosed in, among other places, the passages cited for claim 14 in each chart in Exhibit 899-A.

iv. Automated Generation of Software to Control an Integrated Circuit Was Well Known

By the time of the alleged invention of the Asserted Patents, the concept of automated generation of software to control an integrated circuit was well known to those of ordinary skill in the art. For example, ARC International disclosed in a patent to Hakewill et al. the use of a suite of CAD tools to design and configure both the hardware and software for an integrated circuit. *See, e.g.*, U.S. 5,197,016 (Sugimoto) at 3:58-4:9, 7:1-31; U.S. 5,870,588 (Rompaey) at Figs. 2, 6, 7, 9, 18, 6:45-53, 27:4-28:12, 12:35-44, 17:49-18:46; U.S. 6,862,563 (Hakewill) at 6:12-30, 10:21-33; U.S. Patent Application Publication No. 2008/0222581 (Banerjee) at Figs. 2, 5, ¶¶ 32-39, 55-87. It was also well known in the industry to automatically generate code to control both software simulations and hardware emulations of circuits during the design process. *See, e.g.*, U.S. 6,477,683 (Killian) at Abstract, 6:32-37, 7:22-43, 9:56-10:5, 17:42-47, 17:48-56, 18:1-9, 25:64-26:29, 27:47-28:8, 28:16-39, 41:44-50, 42:41-43, 43:13-19, Fig. 7; U.S. 9,195,784 (Tseng 784) at 11:35-56, 22:36-56.

Moreover, to the extent that ICPillar asserts that "outputting" software as recited by claims can be performed by an entirely separate program that is not integrated with the hardware design program (or that the software can be generated or output by a program that can generically create software for the processor within the designed product), such software development tools were well-known since at least the 1980's. One example is the Arm Development Suite referenced below and which was later named as the RealView Development Suite. If ICPillar amends its Preliminary Infringement Contentions to explicitly acknowledge and assert such a theory, Arm will present additional art showing the pervasive nature of such software development tools.

This functionality is also disclosed in, among other places, the passages cited for claim element 1[d] in each chart in Exhibit 899-A.

v. Use of Hierarchical Menus and Data Structures in Computer-Based Circuit Design Tools Was Well Known

By the time of the alleged invention of the Asserted Patents, the concept of using hierarchical menus, through files, libraries, interactive user interfaces, and other data structures in a computer-based circuit design tool was well known to those of ordinary skill in the art. For example, Altera disclosed in a patent to Allen et al. the use of various wizards that can be used to configure processor cores and peripheral components. *See, e.g.*, U.S. 6,976,239 (Allen) at 8:63-9:10, 10:42-49, Figs. 3A-3U. The same patent also discloses a hierarchical data structure for logic generation processes. *See id.* at Fig. 4. Similarly, ARC disclosed in a patent to Hakewill the use of a menu-driven computer program that is used to automatically build a VHDL simulator and synthesis files. *See, e.g.*, U.S. 6,862,563 (Hakewill) at 3:30-51, 6:44-54, 9:1-19, Fig. 2A.

Moreover, menu-driven selection tools were specified for various known systems using operating systems such as Windows and forms of Unix. *See, e.g.*, U.S. 4,922,432 (Kobayashi) at 5:59-67, 11:29-12:35; U.S. 5,197,016 (Sugimoto) at 4:20-36; U.S. 5,870,588 (Rompaey) at 6:19-34, 11:21-37, 14:49-17:7, Figs. 3, 4, 14; U.S. 2008/0222581(Banerjee) at Fig. 3, ¶¶ 9, 33, 45, 55, 56, 58, 89; *see generally* CoWare System. This includes hierarchal data structures within menu-driven selection tools. *See, e.g.*, U.S. Patent Application Publication No. 2003/0229482 (Cook) at Figs. 32-33.

The substitution of one form of input (such as a menu) for another form of input (such as using input files) is merely a design choice that reflects the substitution of functionally equivalent operations. The inventors of the Asserted Patents did not invent using menus to specify parameters for usage by a computer program.

This functionality is also disclosed in, among other places, the passages cited for claim element 1[a] in each chart in Exhibit 899-A.

B. Prior Art Solutions

In addition to the exemplary combinations of prior art separately identified for the Asserted Patents in Sections IV.B.iii.b and V.B.iii.b, respectively, multiple individuals and companies developed solutions for the purported problems identified by the Asserted Patents prior to the date of the alleged invention(s), including Altera, ARC International, Arm Limited, Cadence Design Systems, IMEC, Magma Design Automation, PACT XPP, Quickturn Design Systems, Synopsys, Tensilica, Texas Instruments, and more. To the extent that ICPillar alleges that the prior art publications and systems do not disclose each and every limitation of the Asserted Claims of the Asserted Patents, it would have been obvious to a person of ordinary skill in the art to modify the prior art solutions in light of the other prior art references identified in these Preliminary Invalidity Contentions, including in Exhibits 899-A, 899-B, 657-A, and 657-B, because they are closely related teachings of the same or related companies, individuals, or, on information and belief, describe aspects of the same prior art system or technology.

For example, Altera engineers and inventors disclosed numerous concepts in this technical field and it would have been obvious to one of ordinary skill in the art to combine such concepts into one prior art Altera solution. By way of example, it would have been obvious to combine or modify U.S. 6,110,223 (Southgate 223), U.S. 6,161,211 (Southgate), U.S. 6,401,230 (Ahanessians), U.S. 6,976,239 (Allen), and/or U.S. 7,272,546 (Brown). Each of the applications that matured into these patents were assigned to Altera and were filed around the same time. Altera was a leader in the development and manufacture of programmable logic devices, including field-programmable gate arrays and other integrated circuit devices, and would have been well-known to a person of ordinary skill in the art. As such, a person of ordinary skill in the art would have

been motivated to combine aspects from one or more of these references alone or in combination with other disclosures from developers and researchers working in the same or similar areas.

As another example, ARC International engineers and inventors disclosed numerous concepts in this technical field and it would have been obvious to one of ordinary skill in the art to combine such concepts into one prior art ARC solution. By way of example, it would have been obvious to combine or modify U.S. 6,862,563 (Hakewill), U.S. 7,475,000 (Cook), and/or U.S. 7,493,470 (Cumplido). Each of the applications that matured into these patents were assigned to ARC and were filed around the same time. ARC was a leader in the design and development of embedded processors, such as the Argonaut RISC core, as well as various computer-based processor configuration and design tools that included GUIs with drag-and-drop components that allowed the addition of custom instructions, integration of customer IP, generation of simulation scripts for system verification, and more. ARC and its products and services would have been well-known to a person of ordinary skill in the art. As such, a person of ordinary skill in the art would have been motivated to combine aspects from one or more of these references alone or in combination with other disclosures from developers and researchers working in the same or similar areas.

As another example, Cadence engineers and inventors disclosed numerous concepts in this technical field and it would have been obvious to one of ordinary skill in the art to combine such concepts into one prior art Cadence solution. By way of example, it would have been obvious to combine or modify U.S. 6,578,174 (Zizzo), U.S. 6,851,094 (Robertson), U.S. 7,392,255 (Sholtis), and/or U.S. 9,195,784 (Tseng 784). Each of the applications that matured into these patents were assigned to Cadence and were filed around the same time. Cadence was (and remains) a leader in software, hardware, and silicon structures for designing integrated circuits, systems on chips,

printed circuit boards, and more, and a person of ordinary skill in the art would have been familiar with Cadence and its innovations. As such, a person of ordinary skill in the art would have been motivated to combine aspects from one or more of these references alone or in combination with other disclosures from developers and researchers working in the same or similar areas.

As another example, Synopsys engineers and inventors disclosed numerous concepts in this technical field and it would have been obvious to one of ordinary skill in the art to combine such concepts into one prior art Synopsys solution. By way of example, it would have been obvious to combine or modify U.S. 7,353,489 (Dowling), U.S. 7,454,732 (McElvain), U.S. 7,873,930 (Vujkovic), U.S. 8,386,972 (Hakewill 972), U.S. 9,171,114 (Hakewill 114), and/or U.S. 10,296,690 (Vujkovic). Synopsys was (and remains) a leader in electronic design automation, including tools and services for semiconductor design, logic synthesis, simulation, and debugging, and a person of ordinary skill in the art would have been familiar with Synopsys and its innovations. As such, a person of ordinary skill in the art would have been motivated to combine aspects from one or more of these references alone or in combination with other disclosures from developers and researchers working in the same or similar areas.

i. Example Kobayashi Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Kobayashi does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Kobayashi and/or combine the teachings of Kobayashi with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below

are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

As noted in the Kobayashi and Sugimoto charts, Sugimoto is a related application that expressly incorporates by reference the Kobayashi disclosure. Thus, to the extent that Sugimoto is not considered part of Kobayashi's disclosure, this relationship and incorporation by reference provides an express motivation to combine. Furthermore Kobayashi expressly references the Fletcher textbook discussed herein and uses it as a basis for one of the Kobayashi examples. This is an express motivation to combine Kobayashi with Fletcher.

Furthermore, Rompaey cites to Kobayashi and Sugimoto on its face as a reference cited in the prosecution of Rompaey. Such citation is evidence that a POSITA would be motivated to combine Kobayashi with Rompaey with a reasonable expectation of success.

Also, a person of ordinary skill in the art would be motivated to combine Kobayashi with U.S. 5,949,993 (Fritz), U.S. 7,171,632 (Masuda), U.S. 7,353,489 (Dowling), Socrates, RealView, SoC Designer, AMBA Designer and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Kobayashi describes "a computer-aided design system and method for designing an application specific integrated circuit which enables a user to define functional architecture independent specifications for the integrated circuit and which translates the functional architecture independent specifications into the detailed information needed for directly producing the integrated circuit." Kobayashi at Abstract. That is precisely what each of these other references do. A person having ordinary skill in the art would have been motivated to modify the teachings of Kobayashi to implement the details of these other reference taught by these references because

it would allow for advances such as the normal improvements in computer technologies (capabilities such as more detailed GUIs, additional components to be used for designs, etc.) that arose in the 25 years between Kobayashi's disclosure and the priority date of the asserted patents. In addition, a person of ordinary skill in the art would be motivated to combine Kobayashi with these references because (a) Kobayashi and these references disclose complementary computer-aided circuit design tools; (b) these references are assigned to, or owned by, leaders in computer system design industry to which a person of ordinary skill in the art would look when seeking to improve existing computer-aided circuit design tools, and (c) these references are analogous art and in the same field of endeavor as each other. Moreover, a POSITA would have had a reasonable expectation of success in incorporating these references' teachings with those of Kobayashi because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine Kobayashi with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

ii. Example Sugimoto Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Sugimoto does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Sugimoto and/or combine the teachings of Sugimoto with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below

are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

As noted in the Kobayashi and Sugimoto charts, Sugimoto is a related application that expressly incorporates by reference the Kobayashi disclosure. Thus, to the extent that Kobayashi is not considered part of Sugimoto's disclosure, this relationship and incorporation by reference provides an express motivation to combine. Furthermore Kobayashi expressly references the Fletcher textbook discussed herein and uses it as a basis for one of the Kobayashi examples. This is an express motivation to combine Sugimoto with Fletcher.

Furthermore, Rompaey cites to Kobayashi and Sugimoto on its face as a reference cited in the prosecution of Rompaey. Such citation is evidence that a POSITA would be motivated to combine Sugimoto with Rompaey with a reasonable expectation of success.

A person of ordinary skill in the art would be motivated to combine Sugimoto with Rompaey, Van Rompaey, Venkest, SoC Designer, Socrates, AMBA Designer, and/or Realview for many reasons. For example, Sugimoto describes "[a] computer-aided system and method…for designing an application specific integrated circuit (ASIC) whose intended function is implemented both by a hardware subsystem including hardware elements on the integrated circuit and by a software subsystem including a general purpose microprocessor also on the integrated circuit." Sugimoto at Abstract. Sugimoto further describes using user interfaces to select components from categorized hierarchal databases to design a system with hardware design and associated software to control the system. A person having ordinary skill in the art would have been motivated to modify Sugimoto to implement the additional features taught by these

references because it would allow for advances such as the normal improvements in computer technologies (capabilities such as more detailed GUIs, additional components to be used for designs, etc.) that arose in the 24 years between Sugimoto's disclosure and the priority date of the asserted patents that include such well-known features as simulation which was known to be a standard part of the design process by 2013. In addition, a person of ordinary skill in the art would be motivated to combine Sugimoto with these references because (a) Sugimoto and these references disclose complementary computer-aided circuit design tools; (b) these references are assigned to, or owned by leaders in the semiconductor / device design industry to which a person of ordinary skill in the art would look when seeking to improve existing computer-aided circuit design tools, and (c) both patents are analogous art and in the same field of endeavor as each other. Moreover, a POSITA would have had a reasonable expectation of success in incorporating these references' teachings with those of Sugimoto because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine Sugimoto with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

iii. Example Rompaey Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Rompaey does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Rompaey and/or combine the teachings of Rompaey with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious.

Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

Rompaey cites to Kobayashi and Sugimoto on its face as a reference cited in the prosecution of Rompaey. Such citation is evidence that a POSITA would be motivated to combine Sugimoto with Rompaey with a reasonable expectation of success.

In addition, as noted in the Kobayashi and Sugimoto charts, Sugimoto is a related application that expressly incorporates by reference the Kobayashi disclosure. Thus, to the extent that Kobayashi is not considered part of Sugimoto's disclosure, this relationship and incorporation by reference provides an express motivation to combine. Furthermore Kobayashi expressly references the Fletcher textbook discussed herein and uses it as a basis for one of the Kobayashi examples. This is an express motivation to combine Rompaey with Kobayashi, Sugimoto, and/or Fletcher.

In addition, a POSITA would be motivated to combine Rompaey with Van Rompaey and/or Verkest with a reasonable expectation of success because all three references have similar disclosures, with similar examples, using the same CoWare system and have overlapping authors/inventors that published the references (or filed the patent) contemporaneously. Van Rompaey and Venkest are also cited on the face of Rompaey.

Furthermore, a person of ordinary skill in the art would be motivated to combine Rompaey with SoC Designer, AMBA Designer, Socrates, and/or RealView for many reasons. For example, Rompaey describes "[a] hardware and software co-design environment and design methodology

based on a data-model that allows one to specify, simulate, and synthesize heterogeneous hardware and software architectures from a heterogeneous specification." Rompaey at Abstract. Rompaey further describes using a GUI to select components from categorized hierarchal databases to design a system with hardware design and associated software to control the system, simulating the system and then outputting the hardware and software. This is precisely what is taught by those other systems. A person having ordinary skill in the art would have been motivated to modify Rompaey to implement the additional details of these references because it would allow for advances such as the normal improvements in computer technologies (capabilities such as more detailed GUIs, additional components to be used for designs, etc.) that arose in the 17 years between Rompaey and the priority date of the asserted patents. In addition, a person of ordinary skill in the art would be motivated to combine Rompaey with these references because (a) Rompaey and these references disclose complementary computer-aided circuit design tools; (b) these references are all assigned to, or sold by, industry leaders to which a person of ordinary skill in the art would look when seeking to improve existing computer-aided circuit design tools, and (c) both patents are analogous art and in the same field of endeavor as each other. Moreover, a POSITA would have had a reasonable expectation of success in incorporating the teachings of these references with those of Rompaey because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine Rompaey with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

iv. Example Killian Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Killian does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Killian and/or combine the teachings of Killian with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Killian with U.S. 8,103,987 (Banerjee 987) for many reasons. For example, Killian describes a process in which "the system circuitry is synthesized, placed and routed on circuit boards, and the layout and timing are re-optimized." Killian at 2:14-22. To the extent such is not expressly or inherently disclosed, a person having ordinary skill in the art would have been motivated to modify the computer-aided circuit design tool of Killian to implement the details of displaying the circuit layout in a graphical user interface, such as that taught by Banerjee 987. *See, e.g.*, Banerjee 987 at Fig. 3. In addition, a person of ordinary skill in the art would be motivated to combine Killian with Banerjee 987 because (a) Killian and Banerjee 987 disclose complementary computer-aided circuit design tools; (b) Killian and Banerjee 987 are closely related technologies, as reflected in their identical international class (G06F 17/50) and the fact that Killian is expressly referenced on the face of

Banerjee 987; (c) Banerjee 987 is assigned to MIPS Technologies, a leading fabless semiconductor design company that is widely known for, among other things, developing the MIPS architecture and a series of RISC CPUs; (d) Killian already discloses a GUI-based computer-aided circuit design tool (e.g., "Xtensa Processor Generator") into which the graphical circuit layout feature of Banerjee 987 would fit like a puzzle piece; and (e) both patents are analogous art and in the same field of endeavor, as they both relate to systems and methods for designing and configuring processors and integrated circuits. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating Banerjee 987's teachings with those of Killian. For similar reasons, a person of ordinary skill in the art would be motivated to combine Killian with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

A person of ordinary skill in the art would be motivated to combine Killian with U.S. 6,161,211 (Southgate), U.S. 7,366,652 (Wang), and/or U.S. Patent No. 8.036,874 (Igarashi) for many reasons. For example, Killian explains that if the process of customizing circuits "could be automated and made reliable, then the ability of a system designer to create application solutions would be significantly enhanced." Killian at 1:55-60. It was well known that one way to enhance the reliability of circuit designs was to simulate the designs before incurring the expense of fabricating a prototype (or the final product). *See, e.g.*, Igarashi at 1:20-2:48. A person of ordinary skill in the art therefore would be motivated to combine Killian and references disclosing techniques for simulating circuit designs, such as Southgate, Wang, and/or Igarashi. In addition, a person of ordinary skill in the art would be motivated to combine Killian with Southgate, Wang, and/or Igarashi because (a) Southgate, Wang, and Igarashi are each assigned to well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in the shared international classifications among Killian, Southgate, and Igarashi; and (c) Killian already

discloses a GUI-based computer-aided circuit design tool into which the simulation functionalities of Southgate, Igarashi, and/or Wang would fit like a puzzle piece. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of Southgate, Igarashi, and/or Wang with those of Killian. For similar reasons, a person of ordinary skill in the art would be motivated to combine Killian with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

v. Example Hakewill Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Hakewill does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Hakewill and/or combine the teachings of Hakewill with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Hakewill with U.S. 5,949,993 (Fritz), U.S. 7,171,632 (Masuda), U.S. 7,353,489 (Dowling), and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Hakewill explains that it "provides a method for managing the configuration, design parameters, and functionality of an integrated circuit design in which custom instructions and other elements may be arbitrarily controlled by the designer." Hakewill at

1:21-26. To expand or enhance the custom instructions available for controlling a custom integrated circuit, a person of ordinary skill in the art therefore would be motivated to combine Hakewill and other references disclosing techniques for generating software to control a custom integrated circuit, such as Fritz, Masuda, Dowling, and/or Sandy. In addition, a person of ordinary skill in the art would be motivated to combine Hakewill with Fritz, Masuda, Dowling, and/or Sandy because (a) Masuda, Dowling, Sandy are each assigned to well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) Hakewill already discloses generation of software for a custom integrated circuit, which easily could be supplemented with the capabilities of Fritz, Dowling, Masuda, and/or Sandy. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of Fritz, Dowling, Masuda, and/or Sandy with those of Hakewill. For similar reasons, a person of ordinary skill in the art would be motivated to combine Hakewill with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

A person of ordinary skill in the art would be motivated to combine Hakewill with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Hakewill explains that its "synthesis engine may create a specific physical layout of the design that meets the performance criteria of the overall design process." Hakewill at 8:21-24. Hakewill further explains that the disclosed innovation is intended to allow the creation of a custom circuit design "with few or no errors and in a much shorter time period than would be otherwise possible with manual design techniques such as hand layouts." Hakewill at 1:40-45. A person of ordinary skill in the art would understand that hand layouts are graphical representations of layouts or schematics, and that implementing such layouts or schematics in a

CAD tool would further Hakewill's goals. A person of ordinary skill in the art therefore would be motivated to combine Hakewill and other references disclosing techniques for generating layouts or schematics, such as McElvain 732, Banerjee 987, and/or Sandy. In addition, a person of ordinary skill in the art would be motivated to combine Hakewill with McElvain 732, Banerjee 987, and/or Sandy because (a) McElvain 732, Banerjee 987, and Sandy are each assigned to well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) Hakewill already discloses generating a layout or schematic in a CAD tool, which easily could be supplemented with the capabilities of McElvain 732, Banerjee 987, and/or Sandy. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of McElvain 732, Banerjee 987, and/or Sandy with those of Hakewill. For similar reasons, a person of ordinary skill in the art would be motivated to combine Hakewill with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

vi. Example Bade Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Bade does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Bade and/or combine the teachings of Bade with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations

should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Bade with U.S. Patent No. 7,171,632 (Masuda), 7,353,489 (Dowling), and/or 7,454,732 (McElvain 732) for many reasons. For example, Bade explains that the circuit design process includes "a requirement definition phase 102." Bade, ¶ 8. A person of ordinary skill in the art would understand that part of the requirement definition phase involves identifying characteristics of the target device. A person of ordinary skill in the art therefore would be motivated to combine Bade and other references disclosing computer-aided design tools that design circuits based, at least in part, on characteristics of the target device, such as Masuda, Dowling, and/or McElvain 732. In addition, a person of ordinary skill in the art would be motivated to combine Bade with Masuda, Dowling, and/or McElvain 732 because (a) each are assigned to well-known leaders in the industry and, in fact, Bade, Dowling, and McElvain 732 are each assigned to Synopsys; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50)[1]; and (c) Bade already discloses the process of defining design requirements in a CAD tool, which easily could be supplemented with the capabilities of Masuda, Dowling, and/or McElvain 732. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of Masuda, Dowling, and/or McElvain 732 with those of Bade. For similar reasons, a person of ordinary skill in the art would be motivated to combine Bade with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

[1] Bade ultimately issued as U.S. 7,613,599, which bears international classification G06F 17/50.

vii. Example Allen Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Allen does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Allen and/or combine the teachings of Allen with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Allen with U.S. 6,578,174 (Zizzo), U.S. 8,103,987 (Banerjee 987), and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Allen describes implementing a customized chip, including association of peripheral components through busses or other interconnections. *See* Allen at 3:13-56. A person having ordinary skill in the art would have been motivated to modify Allen to more readily implement standardized IP libraries or otherwise make use of predefined circuit components to improve the efficiency and reliability of designs, such as those disclosed by Zizzo, Banerjee 987, and/or Sandy. In addition, a person of ordinary skill in the art would be motivated to combine Allen with Zizzo, Banerjee 987, and/or Sandy because (a) each are assigned to well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) Allen already discloses the process of selecting

components and/or features for a customized chip, which easily could be supplemented with the capabilities of Zizzo, Banerjee 987, and/or Sandy. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of Zizzo, Banerjee 987, and/or Sandy with those of Allen. For similar reasons, a person of ordinary skill in the art would be motivated to combine Allen with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

viii. Example Brown Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Brown does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Brown and/or combine the teachings of Brown with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Brown with U.S. 7,275,233 (McElvain 732), U.S. 8,103,987 (Banerjee 987), and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Brown describes a custom circuit design process involving design entry, synthesis, place and route, and verification. *See, e.g.*, Brown at Fig. 3. To the extent such is not expressly or inherently disclosed, a person having ordinary skill in the art would have been

motivated to modify the custom circuit design process of Brown to generate a graphical layout or schematic of the circuit design, such as that taught by McElvain 732, Banerjee 987, and/or Sandy. In addition, a person of ordinary skill in the art would be motivated to combine Brown with McElvain 732, Banerjee 987, and/or Sandy because (a) each of the references disclose complementary computer-aided circuit design tools; (b) all of the references disclose closely related technologies, as reflected in their identical international class (G06F 17/50); (c) McElvain 732, Banerjee 987, and Sandy are each assigned to well-known leaders in the industry; and (d) Brown already discloses a GUI-based computer-aided circuit design tool (Quartus) into which the graphical circuit layout feature of McElvain 732, Banerjee 987, and/or Sandy would fit like a puzzle piece. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of McElvain 732, Banerjee 987, and/or Sandy with those of Brown. For similar reasons, a person of ordinary skill in the art would be motivated to combine Brown with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

ix. Example Cook Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Cook does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Cook and/or combine the teachings of Cook with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior

art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Cook with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Cook explains that the disclosed innovation is intended to allow the creation of a custom circuit design "with few or no errors and in a much shorter time period than would be otherwise possible with manual design techniques such as hand layouts." Cook at 1:49-54. A person of ordinary skill in the art would understand that hand layouts are graphical representations of layouts or schematics, and that implementing such layouts or schematics in a CAD tool would further Cook's goals. A person of ordinary skill in the art therefore would be motivated to combine Cook and other references disclosing techniques for generating layouts or schematics, such as McElvain 732, Banerjee 987, and/or Sandy. In addition, a person of ordinary skill in the art would be motivated to combine Cook with McElvain 732, Banerjee 987, and/or Sandy because (a) McElvain 732, Banerjee 987, and Sandy are each assigned to well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) Cook already discloses a GUI for designing a custom circuit, which easily could be supplemented with the capabilities of McElvain 732, Banerjee 987, and/or Sandy. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of McElvain 732, Banerjee 987, and/or Sandy with those of Cook. For similar reasons, a person of ordinary skill in the art would be motivated to combine Cook with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

x. Example Banerjee Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Banerjee does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Banerjee and/or combine the teachings of Banerjee with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Banerjee with Rompaey, Van Rompaey, Verkest, SoC Designer, Socrates, AMBA Designer, and / or RealView for many reasons. For example, Banerjee teaches a GUI based system for system designers to select components from libraries of categorized hierarchal components including processors, buses, memories and input/output devices, generated hardware and software based on those selections, simulate the generated system, and output hardware designs in commonly known formats such as RTL, Verilog, VHDL, HDL, and netlists. These actions are exactly what is performed in each of these references. A person having ordinary skill in the art would have been motivated to modify Banerjee to implement the details of these references because it would allow for additional capabilities and functionalities known to be beneficial by system designers. In addition, a person of ordinary skill in the art would be motivated to combine Banerjee with these

additional references because (a) Banerjee and these additional references disclose complementary computer-aided circuit design tools; (b) all of these references are assigned to, or sold by, leaders in the electronic device / computer system industry to which a person of ordinary skill in the art would look when seeking to improve existing computer-aided circuit design tools, and (c) both patents are analogous art and in the same field of endeavor as each other. Moreover, a POSITA would have had a reasonable expectation of success in incorporating these additional references' teachings with those of Banerjee because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine Banerjee with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

xi. Example Vorbach Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Vorbach does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Vorbach and/or combine the teachings of Vorbach with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Vorbach with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), and/or U.S. 8,316,341 (Sandy) for many reasons. For example, Vorbach explains that "parameterization may be performed interactively by a programmer, in particular by interaction with a place-and-route too." Vorbach at 5:50-54. To the extent such is not expressly or inherently disclosed, a person of ordinary skill in the art would understand that displaying the circuit design as a physical layout or schematic in a CAD tool would further Vorbach's goals. A person of ordinary skill in the art therefore would be motivated to combine Vorbach and other references disclosing techniques for generating layouts or schematics, such as McElvain 732, Banerjee 987, and/or Sandy. In addition, a person of ordinary skill in the art would be motivated to combine Vorbach with McElvain 732, Banerjee 987, and/or Sandy because (a) McElvain 732, Banerjee 987, and Sandy are each assigned to well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) the graphical circuit layout feature of McElvain 732, Banerjee 987, and/or Sandy would fit into the Vorbach system like a puzzle piece. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of McElvain 732, Banerjee 987, and/or Sandy with those of Vorbach. For similar reasons, a person of ordinary skill in the art would be motivated to combine Vorbach with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

xii. Example Quartus Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Quartus does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Prior Art Socrates and/or combine the teachings of

Quartus with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Quartus with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), SoC Designer, Rompaey, Van Rompaey / CoWare, Verkest / CoWare, AMBA Designer, RealView, and/or U.S. 8,316,341 (Sandy) for many reasons. For example, the documents identified in the Exhibit A charts related to Quartus explain the need to be able to design hardware/software systems with reusable components to control devices. To the extent such is not expressly or inherently disclosed, a person of ordinary skill in the art would understand that displaying the circuit design as a physical layout or schematic in a CAD tool would further the goals of Quartus. A person of ordinary skill in the art therefore would be motivated to combine Quartus and other references disclosing additional techniques for generating layouts or schematics, such as these references. In addition, a person of ordinary skill in the art would be motivated to combine Quartus with McElvain 732, Banerjee 987, and/or Sandy because (a) these references are each assigned to, or sold by, well-known leaders in the industry; (b) the patented references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) the graphical circuit layout feature of McElvain 732, Banerjee 987, SoC Designer (including its incorporated AMBA Designer and RealView) and/or Sandy would fit into the Quartus system like a puzzle piece. Moreover, a person

of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of these references with those of Quartus because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine Quartus with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

xiii. Example Socrates Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges Socrates does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify Prior Art Socrates and/or combine the teachings of Socrates with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine Socrates with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), SoC Designer, Rompaey, Van Rompaey / CoWare, Verkest / CoWare, AMBA Designer, RealView, and/or U.S. 8,316,341 (Sandy) for many reasons. For example, the documents related to Socrates as charted explain the need to be able to design hardware/software systems with reusable components to control devices.

To the extent such is not expressly or inherently disclosed, a person of ordinary skill in the art would understand that displaying the circuit design as a physical layout or schematic in a CAD tool would further Socrates's goals. A person of ordinary skill in the art therefore would be motivated to combine Socrates and other references disclosing additional techniques for generating layouts or schematics, such as these references. In addition, a person of ordinary skill in the art would be motivated to combine Socrates with McElvain 732, Banerjee 987, and/or Sandy because (a) these references are each assigned to, or sold by, well-known leaders in the industry; (b) the patented references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) the graphical circuit layout feature of McElvain 732, Banerjee 987, SoC Designer (including its incorporated AMBA Designer and RealView) and/or Sandy would fit into the Socrates system like a puzzle piece. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of these references with those of Socrates because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine Socrates with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings

xiv. Example Soc Designer Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges SoC Designer does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify SoC Designer and/or combine the teachings of SoC Designer with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a

manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B.These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

Furthermore, as discussed in the SoC Designer charts, SoC Designer expressly uses and references AMBA Designer and RealView. This express use and cross-reference constitutes an express motivation to combine, to the extent that the AMBA Designer and RealView are not considered to be part of SoC Designer.

A person of ordinary skill in the art would be motivated to combine SoC Designer with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), AMBA Designer, RealView Socrates, Rompaey, Van Rompaey, Verkest, and/or U.S. 8,316,341 (Sandy) for many reasons. For example, SoC Designer explains that tit is a tool for designing SoC (system on chips) with processors, memory, buses, and input/output components and then designing the related software. To the extent such is not expressly or inherently disclosed, a person of ordinary skill in the art would understand that displaying the circuit design as a physical layout or schematic in a CAD tool would further SoC Designer's goals. A person of ordinary skill in the art therefore would be motivated to combine SoC Designer and other references disclosing techniques for generating layouts or schematics, such as these references. In addition, a person of ordinary skill in the art would be motivated to combine SoC Designer with these references because (a) these references are each assigned to, or sold by, well-known leaders in the industry; (b) the patented references are directed to closely related technologies, as reflected in their identical international class (G06F

17/50); and (c) the graphical circuit layout feature of M these references would fit into the SoC Designer system like a puzzle piece. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of these references because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine SoC Designer with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings

xv. Example AMBA Designer Solutions

In addition to the example combinations provided above, to the extent that ICPillar alleges AMBA Designer does not disclose any particular limitation of the Asserted Claims of the Asserted Patents, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the alleged invention date, to modify AMBA Designer and/or combine the teachings of AMBA Designer with the other prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B in a manner that would have rendered the Asserted Claims of the Asserted Patents invalid as obvious. Arm provides some examples of such combinations below. The exemplary combinations below are non-exhaustive, and Arm reserves the right to rely on additional combinations as may be apparent from the prior art references in Exhibits 899-A, 899-B, 657-A, and 657-B. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right.

A person of ordinary skill in the art would be motivated to combine AMBA Designer with U.S. 7,454,732 (McElvain 732), U.S. 8,103,987 (Banerjee 987), SoC Designer, Socrates, RealView Rompaey, Van Rompaey, Verkest, and/or U.S. 8,316,341 (Sandy) for many reasons. For example, AMBA Designer is a tool devoted to designing hardware systems, including their

associated buses using a GUI that interacts with libraries of components. To the extent such is not expressly or inherently disclosed, a person of ordinary skill in the art would understand that displaying the circuit design as a physical layout or schematic in a CAD tool would further AMBA Designer's goals. A person of ordinary skill in the art therefore would be motivated to combine AMBA Designer and other references disclosing techniques for generating layouts or schematics, such as these references. In addition, a person of ordinary skill in the art would be motivated to combine AMBA Designer with these references because (a) these references are each assigned to, or sold by, well-known leaders in the industry; (b) these references are directed to closely related technologies, as reflected in their identical international class (G06F 17/50); and (c) the graphical circuit layout feature of these references would fit into the AMBA Designer system like a puzzle piece. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in incorporating the teachings of these references with those of AMBA Designer because they all relate to computer aided design systems implemented in similar software programs running on similar workstations under similar operating systems to accomplish similar functionalities and goals. For similar reasons, a person of ordinary skill in the art would be motivated to combine AMBA Designer with other references in Exhibits 899-A, 899-B, 657-A, and 657-B with similar teachings.

C. The Asserted Claims Recite Well-Known Concepts That Would Have Been Obvious To Implement

As noted above and elsewhere in these Preliminary Invalidity Contentions, the Asserted Claims of the Asserted Patents represent nothing more than an arrangement of well-known concepts and features and add nothing to the state of the art at the time of the alleged invention(s). For each of the concepts represented by the Asserted Claims, it would have been obvious to add to the teachings of any number of known systems and references, including to any of the primary

references in Exhibits 899-A and 657-A to the extent that such reference is alleged to be missing such concept or feature.

i. It would have been obvious to modify any primary reference for receiving categorized input, output, display, and/or control characteristics provided by a user, including through a GUI

To the extent ICPillar contends that any reference charted in Exhibits 899-A or 657-A does not disclose receiving categorized input, output, display, and/or control characteristics provided by a user, through a GUI or otherwise, it would have been obvious to combine such a well-known feature with any of the references charted in Exhibits 899-A, 899-B, 657-A, and 657-B. A person having ordinary skill in the art would have been motivated to implement this capability in a computer-based integrated circuit design tool. For example, before the priority date of the Asserted Patents, "[s]everal types of computer-aided design (CAD) tools [were] available to design and fabricate integrated circuits (IC). Such computer-aided or automated IC design tools [could] include modules or programs addressing both the synthesis and optimization processes." U.S. 6,862,563 (Hakewill) at 1:28-32. "The synthesis process generally begins with the designer compiling a set of IC specifications based on the desired functionality of the target device." *Id.* at 1:66-2:1. Yet it was known that improvements were needed, such as "an improved method and apparatus for implementing control algorithms (such as LTI algorithms) which meets the simultaneous goal of a significantly reduced instruction set and cycle count associated with controller operations, while also optimizing other design criteria such as gate count and power consumption. Such improved method and apparatus would allow the controller designer to select the control functionality or algorithm best adapted for the application(s) at hand, and then easily tailor a cycle-, silicon-, and power-efficient processor solution which is optimized for that particular control algorithm." U.S. 7,493,470 (Cumplido) at 4:15-26. It was likewise recognized

that there was a need for "managing the configuration, design parameters, and functionality of an integrated circuit design in which the instruction set can be interactively varied by the user." U.S. 8,386,972 (Hakewill 972) at 2:37-41. Little or no complexity would have been involved in including this functionality, as it was recognized as commonplace and was the natural progression of circuit design in the computer-enabled world.

Indeed, numerous well-known companies in the industry offered computer-aided design tools with graphical user interfaces that allowed a user to input device characteristics as part of the design and development of integrated circuits.

For example, Tensilica offered the Xtensa Processor Generator tool, as described in, among other places, U.S. 6,477,683 (Killian):

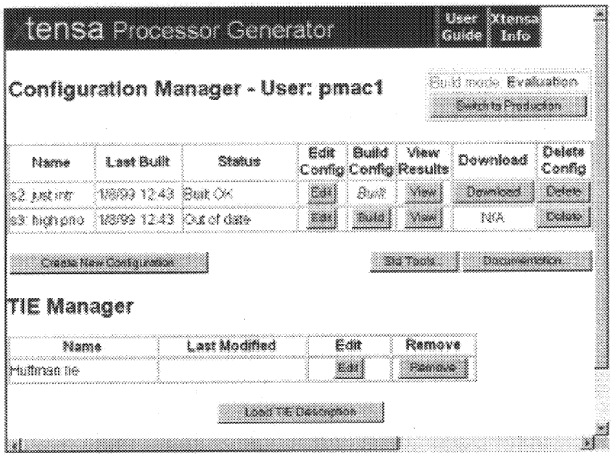


FIGURE 3 86

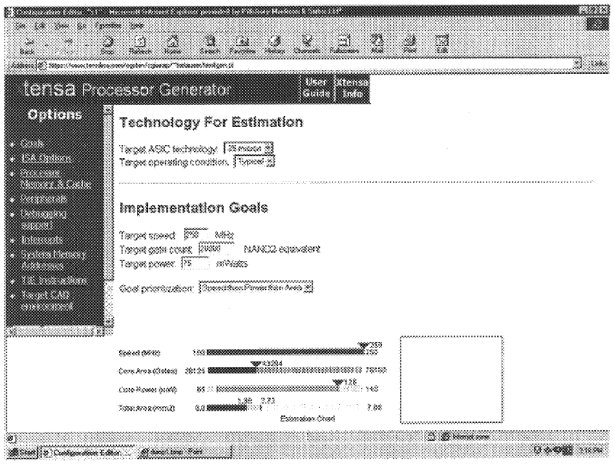
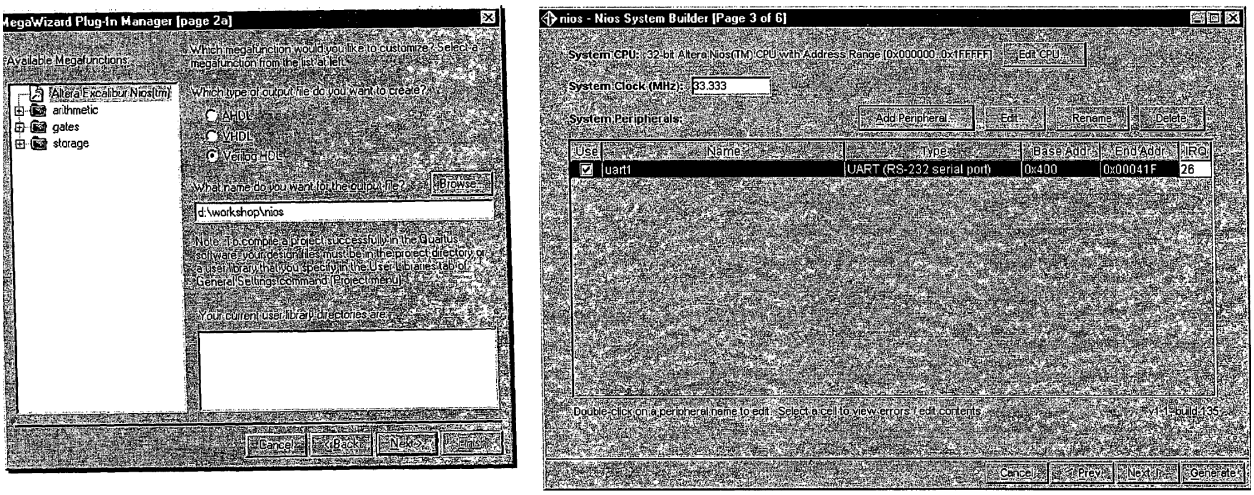


FIGURE 4 88

As another example, Altera offered the Quartus Development Tool, as described in, among other places, U.S. 6,976,239 (Allen):



As another example, MIPS offered a computer-based design tool, as described in, among other places, U.S. 8,103,987 (Banerjee):

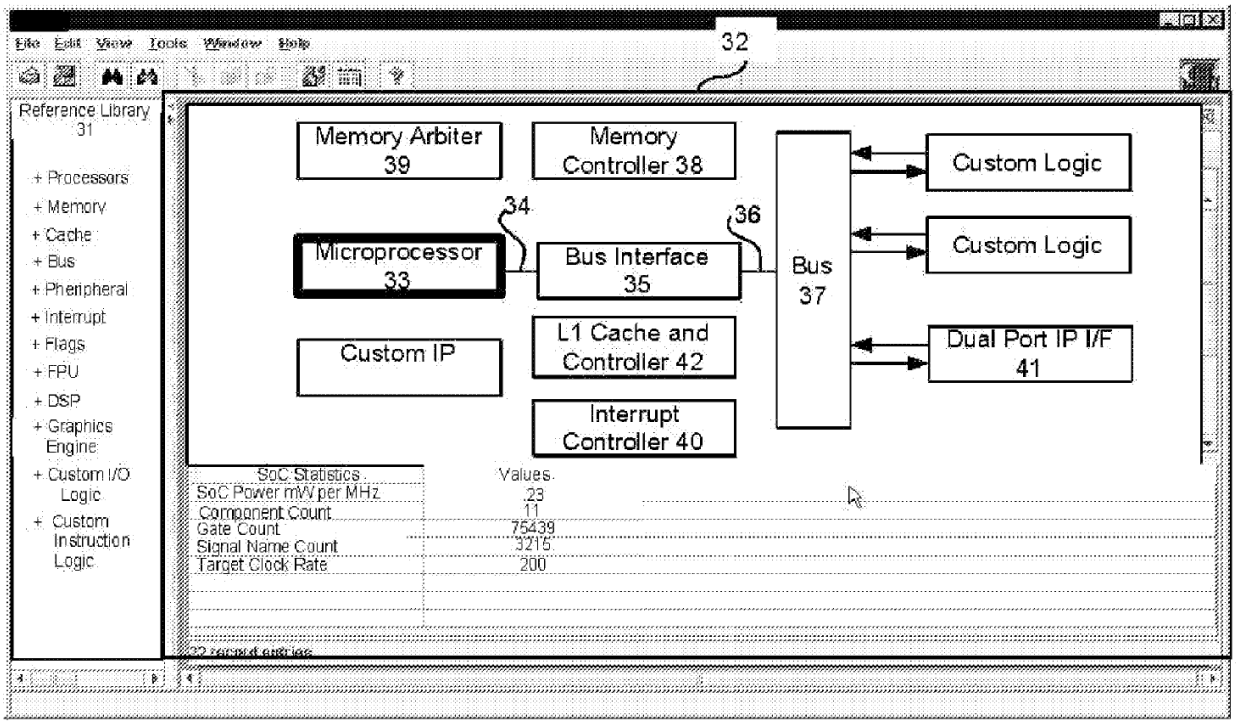


Figure 3

As another example, Mentor Graphics offered a computer-based design tool, as described in, among other places, U.S. Patent Application Publication No. 2006/0095882 (Mankin):

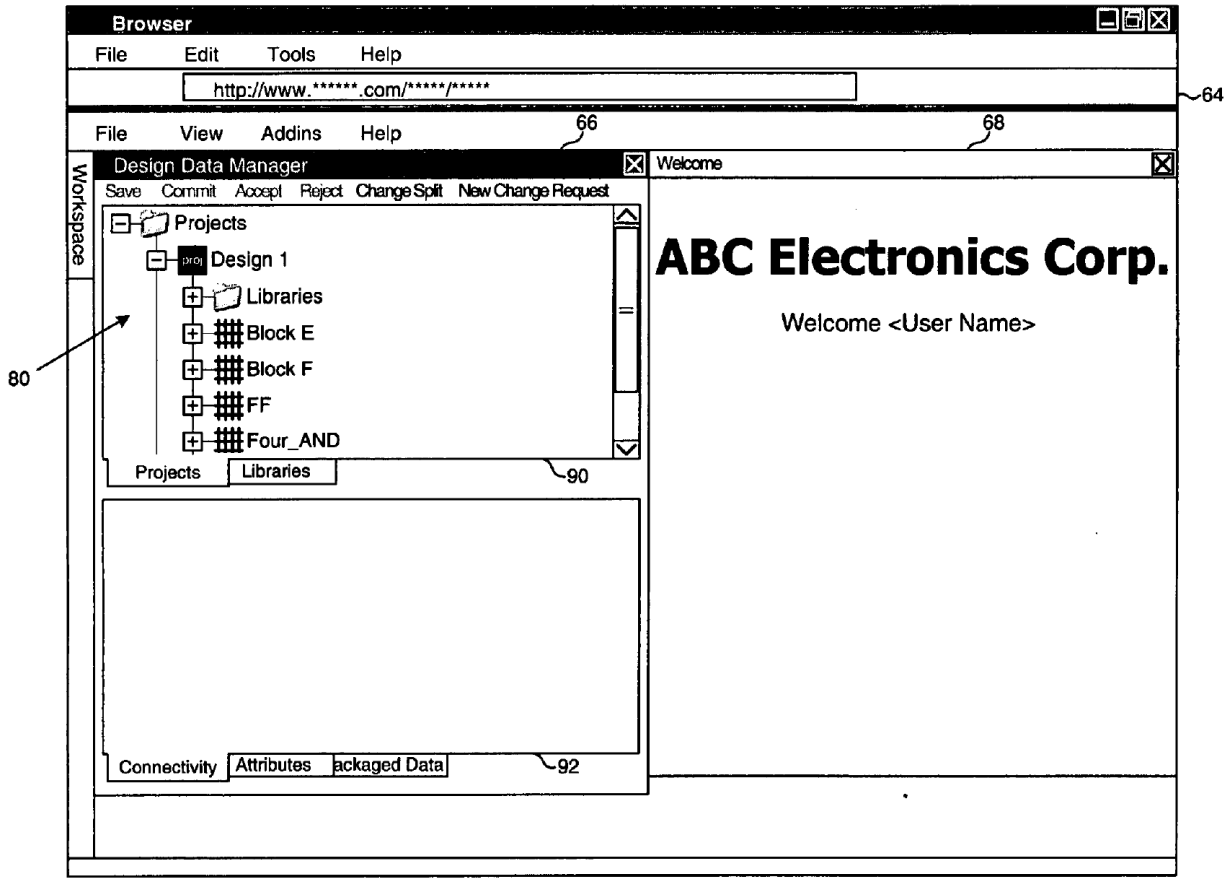


FIG. 8A

Further examples of the GUI's that allow for system design by selecting components and their characteristics / parameters from categorized, hierarchal databases of predetermined elements such as processors, buses, memories, interfaces, UARTs, and other circuits are shown throughout the documents and working systems describing Quartus, Socrates, AMBA Designer, SoC Designer, and RealView. These are shown, for example, in claim element 1[a] of the associated charts for the '899 Patent.

ii. It would have been obvious to modify any primary reference for outputting a hardware integrated circuit design based on input and output characteristics provided by a user

To the extent ICPillar contends that any reference charted in Exhibits 899-A or 657-A does not disclose outputting a hardware integrated circuit design based on input and output

characteristic provided by a user, it would have been obvious to combine such a well-known feature with any of the references charted in Exhibits 899-A, 899-B, 657-A, and 657-B. A person having ordinary skill in the art would have been motivated to implement this capability in a computer-based integrated circuit design tool. For example, before the priority date of the Asserted Patents, "[s]everal types of computer-aided design (CAD) tools [were] available to design and fabricate integrated circuits (IC). Such computer-aided or automated IC design tools [could] include modules or programs addressing both the synthesis and optimization processes." U.S. 6,862,563 (Hakewill) at 1:28-32. "The synthesis process generally begins with the designer compiling a set of IC specifications based on the desired functionality of the target device." *Id.* at 1:66-2:1. Even though "designers often employ computer aided design techniques" for "the design of circuits on integrated circuits," it was recognized that "[i]t is desirable to provide improved automated circuit design techniques, including techniques which include improved routing and optimization techniques." U.S. 7,873,930 (Vujkovic) at 1:17-18, 2:57-60. Little or no complexity would have been involved in including this functionality, as it was recognized as commonplace and was the natural progression of circuit design in the computer-enabled world.

Further examples of the GUI's that allow for analysis and outputting the hardware designs in known formats such as RTL, Verilog, HDL, VHDL, and netlist are shown throughout the documents and working systems describing Quartus, Socrates, AMBA Designer, SoC Designer, and RealView, as well as in Banerjee, Rompaey, Van Rompaey, and Verkest. These are shown, for example, in claim element 1[a] of the associated charts for the '899 Patent.

iii. It would have been obvious to modify any primary reference for outputting software commands to be executed by an integrated circuit design based on input and output characteristics provided by a user

To the extent ICPillar contends that any reference charted in Exhibits 899-A or 657-A does not disclose outputting software commands to be executed by an integrated circuit design based on input and output characteristics provided by a user, it would have been obvious to combine such a well-known feature with any of the references charted in Exhibits 899-A, 899-B, 657-A, and 657-B. A person having ordinary skill in the art would have been motivated to implement this capability in a computer-based integrated circuit design tool. For example, before the priority date of the Asserted Patents, it was recognized that "there is a need for a design tool which will enable the designer not only to create high level block diagrams, but to actually use these diagrams in the software environment as a design entry point, and moreover to use the diagrams in conjunction with existing design tools to implement gate level designs." U.S. 6,110,223 (Southgate 223) at 2:58-63. Similarly, it was known that "an improved method (and associated apparatus) [was] needed for managing the configuration, design parameters, and functionality of an integrated circuit design in which the instruction set can be interactively varied by the user." U.S. 6,862,563 (Hakewill) at 2:40-44. It was likewise recognized that "although prior art techniques provide for limited processor configurability, they fail to provide for the generation of software development tools tailored for use with the configured processor." U.S. 6,477,683 (Killian) at 6:25-29. As Rompaey recognized "automated synthesis of hardware/hardware and hardware/software interfaces, including the generation of the software drivers in programmable processors is possible. This is an essential part of hardware/software co-design" such that the hardware "and the software I/O device driver is generated automatically." Rompaey at 10:41-43, 25:36-37. Similarly, Banerjee's development tool include "modules" responsible for generating and outputting the

related application and driver software specific to the hardware. *See, e.g.*, Banerjee at ¶¶ 30, 67, 72-75, 81. Similarly, Socrates combined the elements of hardware design with sub-components like Bitwise that output the software specifically for the designed hardware. These are all disclosed, for example, in claim element 1[d] in the associated charts for the '899 Patent. Little or no complexity would have been involved in including this functionality, as it was recognized as a necessary aspect of computer-aided integrated circuit design and development.

Moreover, as noted above, if ICPillar asserts that the software can be generated and output by a tool that is separate from the hardware design tool, it would be obvious to combine any of the hardware design tools with such a software design tool. Indeed, that is how hardware / software have been designed since at least the 1980's. One example of such a software design tool is the Arm Development Suite (renamed RealView Development Suite) discussed herein.

iv. It would have been obvious to modify any primary reference for providing an integrated circuit design as a schematic and/or layout

To the extent ICPillar contends that any reference charted in Exhibits 899-A or 657-A does not disclose providing an integrated circuit design as a schematic and/or layout, it would have been obvious to combine such a well-known feature with any of the references charted in Exhibits 899-A, 899-B, 657-A, and 657-B. A person having ordinary skill in the art would have been motivated to implement providing an integrated circuit design as a schematic and/or layout. For example, before the priority date of the Asserted Patents, numerous commercially-available computer-aided circuit design tools that incorporated this functionality were available. Examples of such tools include the Design Data Manager from Mentor Graphics (*see, e.g.*, U.S. Patent Application Publication No. 2006/0095882 (Mankin) at Fig. 8C) and Virtual Silicon from Synopsys (*see, e.g.*, U.S. Patent Application Publication No. 2002/0059054 (Bade) at Fig. 29). A tool with similar functionality was also disclosed in a patent assigned to MIPS. *See* U.S. 8,103,987 (Banerjee) at

Fig. 3. Indeed, largely every charted reference disclosed well-known hardware formats for integrated circuit design such as Verilog, RTL, HDL, VHDL, or netlists. *See generally* claim element 1[c] in Exhibit 899-A and 899-B. A person of ordinary skill in the art would have been motivated to incorporate this functionality into a computer-aided circuit design tool because it would facilitate more efficient design and development of target devices. Little or no complexity would have been involved in including these features and functionalities, as they would have fit together like pieces of a puzzle.

Moreover, the Asserted Patents do not specify any particular details of such "software schematic" or "layout" as recited in certain claims. The Asserted Patents do not identify any formats of these terms. The Asserted Patents do not mention or recite such well-known standards as Verilog, RTL, VHDL, or netlists (the Asserted Patents do include the term "HDL" but characterize it as a "communications type" and not a format of a software schematic or layout). Thus, to the extent that the Asserted Patents provide sufficient support under Section 112 (including to accuse these well-known standard formats in connection with hardware design), the Asserted Patents are necessarily relying upon the knowledge of a POSITA to understand such formats. That same knowledge would be applied by a POSITA in understanding the prior art and its disclosures.

v. It would have been obvious to modify any primary reference for simulating the functionality of the hardware integrated circuit

To the extent ICPillar contends that any reference charted in Exhibits 899-A or 657-A does not disclose simulating the functionality of the hardware integrated circuit, it would have been obvious to combine such a well-known feature with any of the references charted in Exhibits 899-A, 899-B, 657-A, and 657-B. A person having ordinary skill in the art would have been motivated to implement simulating the functionality of the hardware integrated circuit. For example, before

the priority date of the Asserted Patents, it was recognized that many "prior art systems are incapable of automatically assembling a HDL model of the complete processor and simulating its operation." U.S. 8,386,972 (Hakewill 972) at 2:32-36. It was also recognized that doing so "can greatly increase the efficiency and effectiveness of the design process." *Id.* These very same benefits are also recognized in other patents. *See, e.g.*, U.S. 7,475,000 (Cook) at 2:61-65. In fact, by 2007, it was well recognized that IC designers "often employ computer aided design techniques" and that "[s]tandard languages known as Hardware Description Languages (HDLs) have been developed to describe circuits to aid in the design and simulation of complex circuits." U.S. 7,873,930 (Vujkovic) at 1:17-21. It was also common for IC designers to employ electronic design automation, "a computer-based tool configured in various workstations to provide designers with automated or semi-automated tools for designing and verifying user's customer circuit designs," including "creating, analyzing, and editing any electronic design for the purpose of simulation, emulation, prototyping, execution, or computing." U.S. 9,195,784 (Tseng 784) at 1:31-37. "The value of software simulating a circuit design followed by hardware emulation is recognized in various industries that use and benefit from EDA technology." *Id.* at 1:44-46. The CoWare references (as discussed above including the Van Rompaey paper, the Verkest paper, and Rompaey) all detailed simulation of the designed products as part of the development process. Similarly, the Banerjee / CoWare, Socrates, AMBA Designer, SoC Designer, and RealView prior art systems and documents also detailed simulation of the designed products as part of the development process. The fact that simulation was a well-known step in the design process would be a motivation to combine a simulation of the designed hardware with any of the disclosed references. As such, a person of ordinary skill in the art would be motivated to incorporate this

functionality in a computer-aided design tool for a variety of reasons, including reducing errors, increasing efficiency, and improving the effectiveness of the IC design process.

D. Additional Reasons To Combine

In addition to the information contained elsewhere in these Preliminary Invalidity Contentions, including in Exhibits 899-A, 899-B, 657-A, and 657-B, Arm identifies additional motivations and reasons to combine the various references as it pertains to the Asserted Patents. Arm notes that in *KSR Int'l Co. v. Teleflex Inc.*, the Supreme Court held that "[i]n determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." 550 U.S. 398, 419 (2007).

KSR further illustrated several ways in which the subject matter of a patent claim may be shown to be obvious. For instance, "[o]ne of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id.* at 420. The Supreme Court held that it was error to "look only to the problem the patentee was trying to solve." *Id.* Rather, "[t]he question is not whether the combination was obvious to the patentee but whether the combination was obvious to a person with ordinary skill in the art. Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id.* Further, "[c]ommon sense teaches … that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* Further, a showing that a combination of elements was "obvious to try" may show that it was obvious under § 103. *Id.* at 421. For instance, the

Supreme Court held that "predictable solutions" using a combination of "known options" may render the subject matter of a patent claim obvious:

> When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense.

Id., 550 U.S. at 421.

The ways in which the subject matter of a patent claim may be shown to be obvious, identified in *KSR*, are merely illustrative. The main thrust of *KSR* was that "[r]igid preventative rules that deny factfinders recourse to common sense"—such as the overturned "teaching, suggestion, or motivation" test—are neither necessary under our case law nor consistent with it." *Id.*, 550 U.S. at 421-22 (citing with approval, e.g., *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F. 3d 1356, 1367 (2006) ("Our suggestion test is in actuality quite flexible and not only permits, but requires, consideration of common knowledge and common sense"); *Alza Corp. v. Mylan Labs., Inc.*, 464 F. 3d 1286, 1291 (2006) ("There is flexibility in our obviousness jurisprudence because a motivation may be found implicitly in the prior art. We do not have a rigid test that requires an actual teaching to combine ...")).

Although Arm notes that there is no longer a rigid requirement regarding motivation to combine under *KSR*, Arm provides the following examples of the motivations to combine prior art relevant to the invalidity of the Asserted Patents. Multiple teachings, suggestions, and/or reasons to modify any of the references and/or to combine any two or more of the references in Exhibits 899-A, 899-B, 657-A, and 657-B come from many sources, including the prior art (both specific references and as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obvious to

try, the nature of the problem faced, and/or knowledge possessed by one of ordinary skill. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one.

The combination of prior art references identified in these contentions would have been obvious because the combination represents the known potential options with a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry, and the desire to improve features and performance, would motivate the addition of features to systems as they become available, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results.

Moreover, in addition to the information contained elsewhere in these contentions, and in particular in Exhibits 899-A, 899-B, 657-A, and 657-B, Arm has identified additional motivations and reasons to combine the various references cited herein. In particular, multiple teachings, suggestions, and/or reasons to modify any of the references and/or to combine any two or more of the references in Exhibits 899-A, 899-B, 657-A, and 657-B come from many sources, including the prior art (both specific references and as a whole), common knowledge, common sense, predictability, expectations, industry trends, design incentives or need, market demand or pressure, market forces, obvious to try, the nature of the problem faced, and/or knowledge possessed by one

of ordinary skill. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of prior art references identified in these contentions would have been obvious because the claimed combinations represent the known potential options with a reasonable expectation of success.

Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry, and the desire to improve features and performance, would motivate the addition of features to systems as they become available, become less expensive, become more commonly used, provide better performance, reduce costs, size, or weight, or predictably achieve other clearly desirable results.

To the extent that ICPillar contends that Kobayashi (Exhibits 899-A1 and 657-A1) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Kobayashi or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Kobayashi with references in the same or similar field as Kobayashi would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable

expectation of success. For example, Kobayashi discusses multiple ways in which a designer can specify design requirements, such as with flowcharts or logic circuit schematics. *See, e.g.*, U.S. 4,922,432 at 4:5-15. Kobayashi likewise describes the ability of CAD tools to accept design specifications at varying levels of abstraction, such as at the algorithm level, the flowchart (or functional) level, or at the structural (or logic) level. *See, e.g.*, *id.* at 1:13-44, 3:49-4:34. Kobayashi goes on to explain that its "elements or modules are in the form of software programs," but that "persons skilled in the appropriate art will recognize that these elements can easily be embodied in other forms, such as in hardware." *Id.* at 4:50-55.

To the extent that ICPillar contends that Sugimoto (Exhibits 899-A2 and 657-A2) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Sugimoto or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Sugimoto with references in the same or similar field as Sugimoto would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Sugimoto acknowledges that the functional specifications of a desired integrated circuit can be defined in a variety of manners, such as in text form or in a flowchart format, irrespective of any particular architecture or design style. *See* U.S. 5,197,016 (Sugimoto) at 3:9-20. Sugimoto goes on to acknowledge that designers might wish to specify other design constraints, such as annual volume, speed, size, pin count, packaging type, power consumption, and thermal stability. *See id.* at 3:21-29. Sugimoto likewise acknowledges that there

are various options for both the computer system on which the design tool is operated and the graphical user interface with which the designer interfaces. *See id.* at 4:20-43. Sugimoto further acknowledges that "modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention." *Id.* at 16:36-42.

To the extent that ICPillar contends that Rompaey (Exhibits 899-A3 and 657-A3) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Rompaey or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Rompaey with references in the same or similar field as Rompaey would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Rompaey itself describes a computer aided design tools that has numerous options for specifying a desired component. For example, it discloses that "hardware subsystems comprise any one or more of processor cores, off-the-shelf components, customer components, ASICs, processors, and boards." U.S. 5,870,588 (Rompaey) at 6:49-53. As another example, it discloses that a specification can be "a heterogeneous specification comprising a plurality of behavioral and structural languages." *Id.* at 6:54-56. It further recognizes that "other embodiments of the present invention may be obvious to the person skilled in the art." *Id.* at 28:40-43.

To the extent that ICPillar contends that Killian (Exhibits 899-A4 and 657-A4) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the

Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Killian or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Killian with references in the same or similar field as Killian would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Killian itself describes a variety of options with respect to the level of processor configurability that may be desired depending on the designer's requirements. *See* Killian at 3:50-4:14. Killian goes on to describe various commercially-available configurable processors that can satisfy differing designer requirements. *See* Killian at 4:15-5:24. Killian also acknowledges various options for accepting user input describing the designer's goals. *See, e.g.*, Killian at 18:18-21 ("In addition to taking a configuration specification 100 as an input from the designer, it is also possible to accept goals and have the build system 50 determine the configuration automatically."). Killian likewise acknowledges that various algorithms are possible for optimizing a user's desired configuration settings. *See* Killian at 18:47-19:24. Killian further acknowledges that "[m]odifications and variations of the preferred embodiment will be readily apparent to those skilled in the art" and that "[s]uch variations are within the scope of the present invention." Killian at 45:17-20.

To the extent that ICPillar contends that Hakewill (Exhibits 899-A5 and 657-A5) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Hakewill or to combine its teachings with other prior art references, including the prior

art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Hakewill with references in the same or similar field as Hakewill would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Hakewill itself describes a variety of commercially-available computer-aided design tools for designing and fabricating integrated circuits, including modules or programs addressing both the synthesis and optimization processes. *See* Hakewill at 1:28-32. Hakewill explains that there are a variety of ways in which a designer can input desired criteria, including "in the form of an interactive software prompt, or alternatively…using command line parameters, by accessing a pre-built configuration file, or a concurrently running application or other computer program resident on the designer's system or another system linked thereto." Hakewill at 7:64-8:2. Hakewill further explains that "[m]any other methods of input are also possible, all of which are considered to be within the scope of the invention." Hakewill at 8:2-4. Hakewill also specifically explains that, with respect to Figures 2-30, "various substitutions, alterations, permutations, additions, and deletions may be made to the disclosed method," including for example that "individual steps within each of the routines may be modified as required by the particular application." Hakewill at 19:9-17.

To the extent that ICPillar contends that Bade (Exhibits 899-A6 and 657-A6) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Bade or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims

obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Bade with references in the same or similar field as Bade would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Bade itself acknowledges the interchangeability of certain features and technologies in these fields, such as the ability to "model hardware elements and processes as blocks, processes, or symbols." Bade, ¶ 100. Bade further acknowledges that "various modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present invention." Bade, ¶ 225.

To the extent that ICPillar contends that Allen (Exhibits 899-A7 and 657-A7) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Allen or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Allen with references in the same or similar field as Allen would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Allen itself acknowledges the interchangeability of certain features, explaining that the description "is not intended to limit the invention" and instead "it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention." U.S. 6,976,239 (Allen) at 5:8-14. Allen further identifies several

examples of alternative systems, such as ASIC design tools from Synopsys and Avant!, PLC design tools from Triscend, and other CAD tools such as the ARChitect platform. *See id.* at 2:2-3:7. All goes on to explain that characteristics of a desired design can be input a variety of ways, including through a graphical user interface, or through a text interface, a program reading a data file, or a schematic. *See id.* at 6:29-46, 8:41-49, 9:62-65. Allen also explains that the circuit design can be output in a variety of formats. *See id.* at 7:23-25 ("Various synthesized netlist formats will be appreciated by one of skill in the art."); *id.* at 7:37-40 ("As will be appreciated by one of skill in the art, a variety of synthesis, place and route, and programmable logic configuration tools can be used to implement various techniques of the present invention."); *id.* at 7:53-57.

To the extent that ICPillar contends that Brown (Exhibits 899-A8 and 657-A8) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Brown or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Brown with references in the same or similar field as Brown would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Brown itself acknowledges the interchangeability of certain features, such as how the graphical user interface works with various busses that may be required in a given design. *See* U.S. 7,272,546 (Brown) at 10:16-26. Brown also acknowledges that the "actual implementation may or may not contain separately identifiable hardware or software for the various functional blocks" and that the "choice of implementation depends on various factors,

such as particular design and performance specifications for a given implementation." *Id.* at 14:27-35. Brown further explains that "modifications and alternative embodiments of the invention in addition to those described here will be apparent to persons of ordinary skill in the art." *Id.* at 14:37-40.

To the extent that ICPillar contends that Cook (Exhibits 899-A9 and 657-A9) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Cook or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Cook with references in the same or similar field as Cook would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Cook itself acknowledges that "the IC device of the present invention" could be designed to include "any commonly available peripheral such as serial communications devices, parallel ports, timers, counters, high current drivers, analog to digital (A/D) converters, digital to analog converters (D/A), interrupt processors, LCD drivers, memories and other similar devices." U.S. 7,475,000 (Cook) at 39:1-7. Cook also explains that, while the described CAD tools can have an IP library, a user may wish to create their own components or modify existing ones. *See id.* at 28:60-29:6. Cook further explains that "while certain aspects of the invention have been described in terms of a specific sequence of steps of a method, these descriptions are only illustrative of the broader methods of the invention, and may be modified as required by the particular application." *Id.* at 39:20-24.

To the extent that ICPillar contends that Banerjee (Exhibit 899-A10) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Banerjee or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Banerjee with references in the same or similar field as Banerjee would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Banerjee describes a "parameter description module" that "guides the developer in defining the performance requirements for the functional blocks." U.S. Patent Application Publication No. 2008/0222581 (Banerjee), ¶ 34. It goes on to explain that "[o]ne skilled in the art will appreciate that other operating parameters can be readily included in module 22." *Id.* Banerjee further explains that a designer can chose whether or not to simulate a design before synthesis. *Id.*, ¶ 90. Banerjee also explains that "those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiments as a basis for designing or modifying other structures for carrying out the same purposes." *Id.*, ¶ 130.

To the extent that ICPillar contends that Vorbach (Exhibits 899-A11 and 657-A11) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Vorbach or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that

combining Vorbach with references in the same or similar field as Vorbach would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success. For example, Vorbach explains that "selection of the type of modules to be implemented may occur in various ways; the following possibilities being mentioned only by way of example, it being obvious that it is possible and preferred in a practically preferred embodiment of the present invention not to fall back exclusively on a single one of the possibilities." U.S. 8,250,503 (Vorbach) at 6:45-50; *see generally id.* at 6:45-7:58. Vorbach further explains that "parameterization may be performed interactively by a programmer" or "[a]lternatively, heuristic methods are possible as well." *Id.* at 5:50-62. Vorbach also explains that its disclosure is to be read "individually and in combination" with various identified patent applications and other patent-related materials. *See, e.g.*, *id.* at 16:47-56.

To the extent that ICPillar contends that Quartus (Exhibits 899-A12 and 657-A12) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Quartus or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Quartus with references in the same or similar field as Quartus would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

To the extent that ICPillar contends that Socrates (Exhibits 899-A13 and 657-A13) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Socrates or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Socrates with references in the same or similar field as Socrates would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

To the extent that ICPillar contends that RealView (Exhibits 899-A14 and 657-A14) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify RealView or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining RealView with references in the same or similar field as RealView would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

To the extent that ICPillar contends that Soc Designer (Exhibits 899-A15 and 657-A15) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in

the art to modify Soc Designer or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Soc Designer with references in the same or similar field as Soc Designer would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

To the extent that ICPillar contends that AMBA Designer (Exhibits 899-A16 and 657-A16) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify AMBA Designer or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining AMBA Designer with references in the same or similar field as AMBA Designer would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

To the extent that ICPillar contends that Van Rompaey / CoWare (Exhibits 899-A17 and 657-A17) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Van Rompaey / CoWare or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the

art would recognize that combining Van Rompaey / CoWare with references in the same or similar field as Van Rompaey / CoWare would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

To the extent that ICPillar contends that Verkest / CoWare (Exhibits 899-A18 and 657-A18) does not expressly or inherently disclose a particular element or limitation of an Asserted Claim of the Asserted Patents, it nevertheless would have been obvious to a person of ordinary skill in the art to modify Verkest / CoWare or to combine its teachings with other prior art references, including the prior art references in these Preliminary Invalidity Contentions, in a manner that renders such claims obvious and invalid. In particular, a person of ordinary skill in the art would recognize that combining Verkest / CoWare with references in the same or similar field as Verkest / CoWare would be a simple exercise of combining well-known prior art elements according to known methods and techniques to improve similar apparatuses, methods, and systems to yield predictable results with a reasonable expectation of success.

E. Additional Prior Art Relevant To The State Of The Art

In addition to the references identified elsewhere in these Preliminary Invalidity Contentions, including those charted in Exhibits 899-A, 899-B, 657-A, and 657-B, each of the references listed below is relevant to the Asserted Patents, including as it relates to the state of the art.

Prior Art References
U.S. 6,914,551
U.S. 7,526,739
U.S. 7,813,822
U.S. 7,991,606
U.S. 8,032,857
U.S. 8,245,163
U.S. 8,266,560

Prior Art References
U.S. 8,271,773
U.S. 8,326,962
U.S. 8,555,032
U.S. 8,650,516
U.S. Appl. No. 2001/0039190
U.S. Appl. No. 2002/0108006
U.S. Appl. No. 2005/0160195
U.S. Appl. No. 2005/0216870
U.S. Appl. No. 2009/0113037
U.S. Appl. No. 2010/0217967
U.S. Appl. No. 2011/0145777
U.S. Appl. No. 2011/0260752
U.S. Appl. No. 2012/0019371
U.S. Appl. No. 2012/0317574
U.S. Appl. No. 2013/0057583

Each of the concepts discussed above, as well as many others, were widely known by the alleged priority dates of the Asserted Patents. Accordingly, the Asserted Patents are nothing more than a recitation of knowledge that was well-known in the industry, and are, at best, a recitation of well-known features and functionalities that took no more than ordinary skill in the relevant field to arrange in a known manner using conventional techniques.

III. IDENTIFICATION OF PRIOR ART

In addition to the prior art identified on the face of the Asserted Patents and in their respective prosecution histories, Arm intends to rely upon the prior art identified below. Arm identifies each item of prior art based upon information that is currently available and reserves the right to amend and/or supplement the prior art identified above and/or identify further prior art as it becomes known.

Arms identification of patents and publications as prior art here and in the attached invalidity charts under 35 U.S.C. §§ 102 and/or 103 is intended to include the patents and publications themselves, as well as the use, sale, and/or offer for sale of any products, devices, or systems described in the prior art. Although Arm's investigation continues, information available

to date indicates that such products, devices, and systems were known or used in the United States before the alleged prior date of the claimed subject matter of the Asserted Patents and/or were previously invented by another who did not abandon, suppress, or conceal the invention. On information and belief, these prior art products, devices, and systems and their associated references anticipate and/or render obvious each of the Asserted Claims. Arm further intends to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, for example, the prosecution histories of the Asserted Patents and in any related patents, patent applications, and/or reexaminations, any deposition testimony of the named inventor of the Asserted Patents, and the papers and evidence submitted by Plaintiff in conjunction with this litigation.

Arm expressly reserves the right to rely upon additional evidence of invalidity obtained from third parties in the future. In addition, Arm reserves the right to assert invalidity on additional bases under 35 U.S.C. § 102 to the extent that further investigation and discovery yield information forming the basis for such claims.

A. Prior Art Patents and Patent Applications

Arm contends that the following patents and patent applications anticipate and/or render obvious, alone or in combination with each other or other references, one or more of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103.

Reference	Filing Date	Publication / Issue Date
U.S. 4,922,432 (“Kobayashi”)	January 13, 1988	May 1, 1990
U.S. 5,197,016 (“Sugimoto”)	July 14, 1989	March 23, 1993
U.S. 5,870,588 (“Rompaey”)	October 23, 1996	February 9, 1999
U.S. 5,896,521 (“Shakleford”)	October 2, 1996	April 20, 1999
U.S. 5,949,993 (“Fritz”)	October 31, 1997	September 7, 1999
U.S. 6,110,223 (“Southgate 223”)	October 27, 1997	August 29, 2000
U.S. 6,161,211 (“Southgate”)	October 27, 1997	December 12, 2000
U.S. 6,401,230 (“Ahanessians”)	February 1, 1999	June 4, 2002
U.S. 6,477,683 (“Killian”)	February 5, 1999	November 5, 2002

Reference	Filing Date	Publication / Issue Date
U.S. 6,477,697 (“Killian 697”)	February 5, 1999	November 5, 2023
U.S. 6,564,363 (“Dahl”)	July 18, 2001	May 13, 2003
U.S. 6,578,174 (“Zizzo”)	June 8, 2001	June 10, 2003
U.S. 6,851,094 (“Robertson”)	February 28, 2000	February 1, 2005
U.S. 6,682,563 (“Hakewill”)	October 14, 1999	March 1, 2005
U.S. 6,976,239 (“Allen”)	June 12, 2001	December 13, 2005
U.S. 7,171,632 (“Masuda”)	May 24, 2004	January 30, 2007
U.S. 7,240,303 (“Schubert”)	June 6, 2003	July 3, 2007
U.S. 7,272,546 (“Brown”)	March 20, 2003	September 18, 2007
U.S. 7,275,233 (“McElvain”)	March 4, 2003	September 25, 2007
U.S. 7,284,225 (“Ballagh”)	May 20, 2004	October 16, 2007
U.S. 7,353,489 (“Dowling”)	May 28, 2004	April 1, 2008
U.S. 7,366,652 (“Wang”)	September 19, 2005	April 29, 2008
U.S. 7,392,255 (“Sholtis”)	July 31, 2003	June 24, 2008
U.S. 7,475,000 (“Cook”)	April 25, 2003	January 6, 2009
U.S. 7,454,732 (“McElvain 732”)	October 18, 2005	November 18, 2008
U.S. 7,493,470 (“Cumplido”)	December 6, 2002	February 17, 2009
U.S. 7,512,728 (“Tseng”)	November 29, 2004	March 31, 2009
U.S. 7,873,930 (“Vujkovic”)	March 22, 2007	January 18, 2011
U.S. 8,036,874 (“Igarashi”)	June 20, 2008	October 11, 2011
U.S. 8,103,987 (“Banarjee 987”)	March 9, 2007	January 24, 2012
U.S. 8,250,503 (“Vorbach”)	January 17, 2007	August 21, 2012
U.S. 8,316,341 (“Sandy”)	September 17, 2009	November 20, 2012
U.S. 8,386,972 (“Hakewill 972”)	December 16, 2009	February 26, 2013
U.S. 8,386,980 (“Murray 890”)	November 18, 2010	February 26, 2013
U.S. 8,527,934 (“Ginetti”)	September 9, 2010	September 3, 2013
U.S. 8,807,948 (“Luo”)	September 29, 2011	August 19, 2014
U.S. 8,943,452 (“Hsu”)	June 13, 2011	January 27, 2015
U.S. 9,088,491 (“Vaidya”)	March 7, 2012	July 21, 2015
U.S. 9,171,114 (“Hakewill 114”)	January 30, 2013	October 27, 2015
U.S. 9,195,784 (“Tseng 784”)	April 1, 2011	November 24, 2015
U.S. 9,268,578 (“Cummings”)	November 7, 2011	February 23, 2016
U.S. 9,275,185 (“McIlrath”)	January 23, 2014	March 1, 2016
U.S. 9,591,496 (“Cummings 496”)	January 12, 2016	March 7, 2017
U.S. 10,296,690 (“Vujkovic 690”)	December 8, 2015	May 21, 2019
U.S. 10,867,333 (“Banerjee 333”)	August 12, 2019	December 15, 2020
U.S. 2002/0059054 (“Bade”)	June 1, 2001	May 16, 2002
U.S. 2003/0204830 (“Brawn”)	April 4, 2003	October 30, 2003
U.S. 2003/0229482 (“Cook 482”)	April 25, 2003	December 11, 2003
U.S. 2004/0268283 (“Perry”)	June 24, 2003	December 30, 2004
U.S. 2005/0076315 (“Wen”)	October 3, 2003	April 7, 2005
U.S. 2005/0262462 (“Janakiraman”)	May 20, 2004	November 24, 2005
U.S. 2006/0075382 (“Shaburov”)	October 5, 2004	April 6, 2006
U.S. 2006/0095882 (“Mankin”)	September 8, 2004	May 4, 2006

Reference	Filing Date	Publication / Issue Date
U.S. 2006/0155968 ("Inuo")	June 21, 2004	July 13, 2006
U.S. 2007/0200596 ("Lee")	February 24, 2006	August 30, 2007
U.S. 2008/0222581 ("Banerjee")	March 9, 2007	September 11, 2008
U.S. 2009/0113037 ("Pouchak")	October 24, 2007	April 30, 2009
U.S. 2009/0187756 ("Nollet")	December 10, 2008	July 23, 2009
U.S. 2010/0169857 ("Campi")	December 28, 2009	July 1, 2010

B. Prior Art Publications

Arm contends that the following printed publications anticipate and/or render obvious, alone or in combination with each other or other references, one or more of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Moreover, as noted before, these prior art documents demonstrate the functionality of the systems discussed below (and listed in the associated charts) and constitute prior art publications that are asserted as document prior art in addition to the system prior art.

Reference	Publication Date
An Engineering Approach to Digital Design, William Fletcher, Prentice Hall[2]	1980
K. Van Rompaey, D. Verkest, I. Bolsens and H. De Man, "CoWare-a design environment for heterogeneous hardware/software systems," Proceedings EURO-DAC '96. European Design Automation Conference with EURO-VHDL '96 and Exhibition, Geneva, Switzerland, 1996, pp. 252-257, doi: 10.1109/EURDAC.1996.558213.	1996
CoWare—A design environment for heterogeneous hardware/software systems, Verkest, D., Van Rompaey, K., Bolsens, I. et al. Des Autom Embed Syst 1, 357–386 (1996). https://doi.org/10.1007/BF00209910	1996
Decentralized, Modular Real-Time Control for Machining Applications, J. Yook et al.	September 25, 1997
Open Architecture Control Systems, Y. Koren et al.	1998

[2] This textbook is 765 pages in length and is protected by copyright. Defendants have this book available for inspection upon reasonable notice by ICPillar.

C. Prior Art Systems

In addition to any prior art systems that correspond to the references in the tables above, Arm contends that the following prior art systems that were in public use, on sale, or otherwise available to the public before the priority date of the Asserted Patents anticipate and/or render obvious, alone or in combination with each other or other references, one or more of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Arm notes that it has not yet obtained third-party discovery, such as non-public information about these prior art systems. As such, Arm reserves the right to seek third-party discovery relating to prior art systems and to supplement these Preliminary Invalidity Contentions based upon information obtained through such discovery.

System	Date	Entities / Persons Involved
Quartus	No later than Mar. 20, 2003	Altera Corporation
ARChitect System	No later than June 11, 2002	ARC International
Development Tool Suite	No later than Dec. 1, 2003	ARC International
AMBA Designer	No later than 2006	Arm Limited
SEmulator System	No later than Apr. 1, 2011	Cadence Design Systems
CoWare	No later than 1996	IMEC (Interuniversitair Microelektronica Centrum)[3]
System Realizer	No later than Jan. 27, 1998	Quickturn
coreTools	No later than 2008	Synopsys
xTensa Processor Generator	No later than Feb. 5, 1999	Tensilica
Prior Art Socrates	No later than 2006	DuoLog
RealView Development Suite	No later than 2001	Arm Limited
SoC Designer	No later than 2007	Arm Limited (pre-2008); Carbon (post-2008)

Brief summaries of these prior art systems, based on information presently available to Arm, are provided below.

For each of the charted prior art systems, the documents and materials cited in the associated exhibits can be combined to demonstrate the functionality of the invalidating system.

[3] On information and belief, IMEC is a research center in Leuven, Belgium that is now part of Synopsys, with facilities in San Jose, California.

Those documents and materials may also be combined for obviousness and/or anticipation purposes as document prior art (as opposed to the system) to create a combination (either obviousness or inherent anticipation).

i. Altera Quartus

The Altera Quartus design software was a comprehensive environment for designing and developing integrated circuits, including systems-on-a-programmable-chip (SOPC) and other programmable logic devices. The Quartus design software is described in, among other places, U.S. 7,272,546 (Brown), a patent assigned to Altera. The Quartus design software was one example of the many well-known computer-aided circuit design tools available in the industry. *See, e.g.*, U.S. 6,976,239 (Allen) at 7:33-37 ("According to various embodiments, the place and route tool 113 and the programmable logic configuration stage 119 are provided in the Quartus Development Tool, available from Altera Corporation of San Jose, Calif.").

ii. ARC Development Tool Suite Platforms

ARC offered a full suite of computer-aided circuit design tools under the Development Tool Suite. The ARC Development Tool Suite was a powerful collection of tools to facilitate software and hardware development as well as co-simulation. The Development Tools Suite included at least the ARChitect, MetaDeveloper, Cycle Accurate Simulator, MetaSim, and ARCangel tools and capabilities. The ARChitect processor configurator was a Java-based design tool that allowed SoC designers to configure and extend and ARC processor through a graphical user interface with drag-and-drop components and point-and-click options that resided on the user's desktop. It also allowed users to add customer instructions, allowing further optimization of the processor for the end application. ARC's design tools are described in various publications and patents. *See generally* U.S. 6,862,563 (Hakewill).

These design tools are an example of some of the many well-known computer-aided circuit design tools available in the industry. *See, e.g.*, U.S. 6,976,239 (Allen) at 2:62-66 ("A processor core based on hardwired logic is less flexible than a processor core based on undifferentiated programmable logic. ARC Cores of Elstree, United Kingdom provides a graphical user interface in its ARChitect tool to configure processor cores in programmable chips."); *see also* U.S. Patent Application Publication No. 2003/0229482 (Cook), ¶ 12 (discussing the ARChitect system).

iii. AMBA Designer

AMBA Designer was a tool that allowed users to specify the parameters / characteristics of a designed device that included different forms of the AMBA bus fabric along with various predetermined models such as processor models for ARM cores including the ARM11 family of cores. After selecting the characteristics / parameters, the user could generate RTL outputs reflecting the hardware design. The user could also run simulations on the design. AMBA Designer included a GUI interface allowing for selection from a categorized hierarchal database of predetermined components.

Once the hardware was designed and output, the user used software tools such as the RealTime Development Suite to generate and output the software for the designed system / device.

AMBA Designer was a software tool suite that ran on Windows and Unix workstations that included processors. It was stored on non-transitory media such as CDs and hard drives for execution. The NIC-400 materials cited in the AMBA Designer exhibit are a specific example of the usage of the AMBA Designer. AMBA Designer was part of the SoC Designer as well.

iv. Cadence SEmulator System

This system allowed for computer-aided circuit modeling and simulation, including software simulation, simulation through hardware acceleration, in-circuit emulation, and post-

simulation analysis. The SEmulator system, through automatic component type analysis, could model a user's custom circuit design in software and hardware, such that the entire user circuit design was modeled in software, while evaluation components (i.e., register components, combinational components) were modeled in hardware. The SEmulator system is described in, among other places, U.S. 7,512,728 (Tseng) and U.S. 9,195,784 (Tseng 784), both patents assigned to Cadence.

v. IMEC CoWare

This system is described, at least in part, in U.S. 5,870,588 (Rompaey), which is charted against the Asserted Patents in Exhibits 899-A and 657-A with respect to the product matching the patent. It is also cited in the Van Rompaey / CoWare and Verkest / CoWare publications cited above and charted separately. This functionality has been integrated into Synopsys products since at least 2010. *See* https://news.synopsys.com/index.php?s=20295&item=123132; *see also* https://news.synopsys.com/index.php?s=20295&item=123141. Synopsys subsequently combined CoWare into its Virtualizer product. *See* https://www.embedded.com/synopsys-gathers-virtio-vast-and-coware-into-virtualizer/. The CoWare System originated in the IMEC (Interuniversitair Microelektronica Centrum) research center in Leuven, Belgium. CoWare is now based in San Jose, California.

The CoWare prior art system is described, alone and in combination, in Exhibit 899-A3 (Rompaey), Exhibit 899-A17 (Van Rompaey / CoWare), Exhibit 899-A18 (Verkest / CoWare), Exhibit 657-A3 (Rompaey), Exhibit 657-A17 (Van Rompaey / CoWare), and Exhibit 657-A18 (Verkest / CoWare).

vi. Quickturn System Realizer

This system enabled real-time, system-level design verification through in-circuit emulation. This in turn allowed rapid prototyping of ASIC/ICs directly from all standard EDA netlist formats. The Quickturn System Realizer was one example of the many well-known computer-aided circuit design tools available in the industry. *See, e.g.*, U.S. 7,240,303 (Schubert) at 4:5-9 ("An example of such a hardware emulation system is System Realizer from Quickturn Systems, in San Jose, Calif.").

vii. Synopsys coreTools

Synopsys offered a full suite of computer-aided circuit design tools, packaged in the coreTools platform. This platform included at least coreBuilder, coreAssembler, and coreConsultant. The coreBuilder tool was a robust packaging tool that allowed designers to capture the knowledge and design intent of IP and provide graphical or command based configuration menus for the IP. The coreAssembler tool was an open IP assembly tool that automatically generated the interconnect and configured RTL, as well as documented the block and system configuration details and design testbench. The coreConsultant tool was a utility package for configuring, implementing and validating individual IP blocks packaged with coreBuilder. Synopsys coreTools, including coreBuilder and coreKit, are described in, among other places, U.S. 7,353,489 (Dowling), a patent assigned to Synopsys.

viii. xTensa Processor Generator

This system allowed was a computer-aided configuration editor that allowed a user to interact with the tool via a graphical user interface. Among other instruction sets, the Xtensa Instruction Set Architecture could be implemented within the xTensa Processor Generator as core instructions and instructions that are available via the selection of configurable options. The

xTensa Processor Generator platform is described in, among other places, U.S. 6,477,683 (Killian), a patent assigned to Tensilica.

ix. Prior Art Socrates

Prior Art Socrates was a tool that allowed users to specify the parameters / characteristics of a designed device that included different forms of the AMBA bus fabric along with various predetermined models such as processor models for various processors including various ARM cores including the ARM11 family of cores. After selecting the characteristics / parameters, the user could generate RTL outputs reflecting the hardware design. The user could also run simulations on the design. Prior Art Socrates included a GUI interface allowing for selection from a categorized hierarchal database of predetermined components.

The user could also generate and output software based on the selected parameters and characteristics of the device including through the use of the Socrates Bitwise subcomponent. Once the hardware was designed and output, the user used software tools such as the Socrates Bitwise component to generate and output the software for the designed system / device.

Prior Art Socrates was a software tool suite that ran on Windows and Unix workstations that included processors. It was stored on non-transitory media such as CDs and hard drives for execution. Socrates was on sale at least as of 2006 and continued through the effective filing date of the Asserted Patents and is therefore prior art to those patents under post-AIA section 102.

Prior Art Socrates was created and sold by DuoLog. In 2014, Arm purchased DuoLog. Moreover, Arm itself licensed the Prior Art Socrates system no later than October 10, 2012. *See* Agreement For Software Tools Licensing Between ARM Ltd. And Duolog Technologies Ltd, LES-EDN-20004, Duolog Agreement No. DLG-2012817-01, 10 October 2012.

ICPillar's infringement contentions cite to Socrates functionality.:

> Arm Socrates User Guide (Version 1.5) at 1-11 ("Socrates IP Tooling platform is an environment for exploring, configuring, and building Arm IP ready for integration into a *System on Chip* (SoC).") (Italics in original); *id*. at 4-33 (showing "Cortex- A35 sample configure and build script")

ICPillar Infringement Contentions, Exhibit A at p. 1; *see also id.* at n.1.

> Arm Socrates User Guide (Version 1.5) at 7 ("Socrates enables you to browse, configure, (with configuration space validation),and build Arm IP, including Arm Interconnect IP. The generated RTL and IP-XACT can then be integrated into Arm-based systems … Socrates provides several types of technical information for each supported Arm IP, and a standardized way to configure and build IP.");*id.* at 1-14 (defining "IP Catalog" as "A hierarchical list of all the supported Arm IP products and versions. You can filter the list by group, name, protocol, or valid associations.")

Id. at p. 2.

To the extent that ICPillar's Infringement Contentions recite infringement, the Prior Art Socrates also discloses the claim elements for the same reason and therefore invalidates the claims under ICPillar's interpretation of the claims.

Arm's invalidating prior art includes materials that were distributed with Release 12.1 of Prior Art Socrates in a release dated August 3, 2012,[4] as well as materials distributed with Release 1.5.2 of the Socrates Weaver sub-product from a release dated December 13, 2012.[5]

x. RealView Development Suite (RVDS)

RVDS was originally named Arm Development Suite and was first sold no later than 2001 and was continued to be sold through the effective filing date of the Asserted Patents. *See* document DUI0056C. As detailed in the related exhibit, RVDS is used to generate and output software to control devices based on the selected characteristics / parameters for the hardware of

[4] Arm has located the software corresponding to this version of Prior Art Socrates and will make it available for inspection upon reasonable notice from ICPillar.

[5] Arm has located the software corresponding to this version of the Socrates Weaver sub-product and will make it available for inspection upon reasonable notice from ICPillar.

those devices, at least under ICPillar's infringement theory. Arm's invalidating prior art includes materials that were distributed with Release 4.1 of RVDS in a release dated May 31, 2011.[6]

In its Infringement Contentions, ICPillar cited to, and accused, the Arm Development Guide as allegedly providing infringement of one or more elements.

> Arm uses the Accused Design Tools to compile and output software commands for the integrated circuit, which controls the electronic device in accordance with the selected input and output characteristics. Arm Development Studio Getting Started Guide (Version 2021.2) at 184 (CMSIS packs offer you a quick and easy way to create, build and debug embedded software applications for Arm Cortex-A5/A7/A9 based processors."); Arm Development Studio: Introducing the Pack Manager (video) ("The pack manager allows you to install ready-made packs of software that you can integrate into your own application code and we can now build our project to give us a resulting executable file.").

ICPillar Infringement Contentions, Exhibit A at p. 6. RVDS is the precursor product to Arm Development Studio and provides whatever functionality that ICPillar asserts corresponds to the claim elements for which it is cited and therefore invalidates the claims under ICPillar's interpretation of the claims.

As delivered in 2012, for example, RVDS included an extensive set of documents describing its functionality as shown in the associated exhibit and the documents cited therein. To the extent that ICPillar is allowed to amend its Infringement Contentions to state more details, RVDS documents will disclose such details and rendered the claims invalid.

For example, RVDS uses the hardware models, such as models of various ARM processors and other hardware components including the ARM11 and Cortex families to generate software output based on the characteristics / parameters of those hardware components. The generation and output of such executable software is shown in, for example, the many Compiler Toolchain documents that were delivered as part of the RVDS. It is also shown in the documents describing

[6] Arm has located the software corresponding to this version of the RVDS system and will make it available for inspection upon reasonable notice from ICPillar.

debugging which allowed for recompilation and output of the software as part of the development process.

RVDS could be, and was, used to develop and output software for devices for which the hardware was created for other systems described herein including at least AMBA Designer, Prior Art Socrates, SoC Designer, and Synopsis and Cadence products. Thus, RVDS can be combined with any of the other systems and document references that show the development and output of hardware because RVDS's purpose is to design, debut, and output software.

xi. SoC Designer

SoC Designer was acquired by Arm from AXYS Design in 2004 under the product name of "MaxSim." In 2008, Arm sold SoC Designer to Carbon Design Systems who developed it until 2015 when Arm re-acquired it. SoC Designer was sold continuously throughout this entire period. Arm's invalidating prior art materials include the materials (e.g., manuals, etc.) included in Release 7.1 of SoC Designer dated from June 2008, in addition to other materials.[7]

SoC Designer integrated numerous other Arm design tools into a single environment. Specifically, as noted in the exhibits charted SoC Designer, it integrated by AMBA Designer and RealView which are both separately charted. SoC Designer allowed the user to design systems by selecting components and their associated characteristics / parameters using a GUI from libraries of predetermined components in categorized and hierarchal databases. These components included various Arm processors. The components that could be specified also related to input, output, control and display parameters including specifically components that interacted with mouse, keyboards, and LCD displays.

[7] Arm has located the software corresponding to this version of SoC Designer and will make it available for inspection upon reasonable notice from ICPillar.

In addition, SoC Designer allowed the use of AMBA Designer to create, for example, the bus fabrics between the components designed with the other portions of SoC Designer. The user would then invoke the RVDS, including the RealView Debugger, to create and output the associated software. The output of the hardware from SoC Designer was in numerous forms including Verilog, RTL, HDL, VHDL.

Effectively, SoC Designer shows the entire integrated suite of products that ICPillar's Infringement Contentions now accuse – all in a product sold long prior to the effective filing date of the Asserted Patents.

D. Admitted Prior Art

Arm contends that the admitted prior art, as set forth in the Asserted Patents and their prosecution histories, is relevant to, among other things, the state of the art at the time of the alleged inventions in the Asserted Patents and anticipates or renders obvious (alone or in combination with each other or with other references) one or more of the Asserted Claims. Arm therefore reserves the right to rely upon the admitted prior art, including but not limited to the following exemplary admissions from the Asserted Patents:

- "For some time now, technology has advanced to the point where developers and manufacturers have had the ability to provide remote control over their products. A very simple example is a television and its remote controller. A remote controller uses a wireless signal, usually infrared, to send user provided control instructions to a television set. The television set then executes those instructions, such as turning off the television or changing the channel." '899 Patent at 1:6-13.

- "With the wide proliferation of the devices connected to the internet, developers have had the ability to develop software and controllers to control devices connected to the internet. One example is a personal computer with remote desktop software. This software enables a personal computer (with the correct software) to control another personal computer which is connected to the internet and running the remote desktop software. Another example is a mechanical device which is fitted with integrated circuits (ICs) that can be controlled by smartphones such as AR.Drone, Sphero and iHelicopter." '899 Patent at 1:21-31.

- "Developers have designed and built micro control units (MCUs) integrated with remote communication devices and programmed them to receive instructions both locally and remotely." '899 Patent at 1:35-39.

- "Historically, we have accepted that information and its movement through the internet have been viewed as unrestricted through the establishment of communication, messaging and interaction standards such as TCP, SMTP, and HTTP and we have viewed access to the same as commonplace due to the ubiquity of the web browser. These standards and related technologies not only assure access to information but are largely taken for granted as being available anywhere and through anything at any time." '899 Patent at 2:39-48.

- "FIG. 2 illustrates one embodiment [of] such a hierarchal database. In this illustration, the hierarchal database contains data directed to particular aspects of a device. For example, such hierarchal databases are used by the United States Patent and Trademark Office as classification aids for classifying inventions into one or more fields of technology." '899 Patent at 8:45-50.

- "As one skill in the art will immediately understand, any device, such as a blender, can be defined by defining its control type, display type, input type, and output type." '899 Patent at 9:15-18.

- "Fabless design of ICs and MCUs is well known in the art. In general, the term fabless design is applied to [a] process where the design of the IC is accomplished separately from the manufacture of the device itself, rather than past methods which relied upon vertical integration of design and manufacture." '899 Patent at 9:65-10:3.

- "It will be apparent to those skilled in the art that in many ways, the FDK of the various embodiments described herein may function similarly to a so called software development kit or an IDE. A software development kit has similar functionality, that is, a software development kit is typically a set of software development tools that allows for the creation of applications for a certain software package, software framework, hardware platform, computer system, video game console, operating system, or similar development platform." '899 Patent at 10:15-23.

- "According to one embodiment, Control Management System 103 may be a unitary server or may be a distributed server spanning multiple computers or multiple data centers. The term server may refer to various types of servers, such as, for example and without limitation, a web server, news server, mail server, message server, advertising server, file server, application server, exchange server, database server, proxy server, and the like." '899 Patent at 11:16-23.

- "At step 2001, system 2000 may provide a developer a fabless integrated circuit (IC) development kit. The FDK may be software which, when executed on a computer system, allows for a developers to input interface attributes of a device which a developer intends to enable a user to remotely control the device. The FDK may provide a software representations of a complete IC design. In one embodiment, the

> software representation may be a schematic and/or layout. The user may have the ability to edit the software representation of the IC or the software representation may be locked and only allow for testing. The software representation may also provide simulation and debugging capabilities through proprietary software and/or design automation software. Design automation software may include but, is not limited to, computer aided design software developed by Synopsis, Inc.; Cadence Design Systems, Inc.; Magma Design Automation, Inc.; and the like." '899 Patent at 13:1-17.

Arm also reserves the right to rely upon the admitted prior art described in the prosecution histories of the Asserted Patents. For example, and without limitation, the applicant admitted that U.S. Patent Application Publication No. 2009/0113037 to Pouchak "teaches a software system that can be used to develop software operating commands on a computer" and "to use that computer to simulate how the software will operate when applied to control an HVAC system." Response to April 11, 2014 Office Action (Aug. 11, 2014) at 7. The applicant further admitted that Pouchak discloses "simulations of a collection of hardware components, the virtual nature of which are then used to test the software 'blocks' and 'modules' to determine if the software works." *Id.*

IV. THE '899 PATENT IS INVALID

A. Identification of Prior Art

Arm contends that the prior art references described and charted in Exhibits 899-A and 899-B anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '899 Patent.

B. Bases for Invalidity

ICPillar asserts claims 1, 5, 6, 8, and 14 of the '899 Patent against Arm. These claims are invalid because the '899 Patent fails to meet one or more of the requirements for patentability. The individual bases for invalidity are provided below and in Exhibits 899-A and 899-B. Each of the prior art references, the underlying work, and/or the underlying apparatus or method qualifies as invalidating prior art under one or more sections of 35 U.S.C. §§ 102 and/or 103.

In an effort to focus the issues, Arm has cited exemplary portions of identified references, even where a reference may contain additional disclosures or support for a particular claim element. Each and every disclosure of the same limitation in the same reference is not necessarily identified. In addition, persons of ordinary skill in the art generally read a prior art reference as a whole and in the context of other publications and literature and in the context of their own knowledge and experience as persons of ordinary skill in the art. Thus, to understand and interpret any specific statement or disclosure within a prior art reference, such persons would rely on other information within the reference, along with other publications and their general scientific knowledge and experience in the field.

Each prior art reference identified in these Preliminary Invalidity Contentions therefore should be understood in the context of the reference itself, in conjunction with anything incorporated by reference or described as relevant technology by the reference, any documents that are referred to for further understanding by the reference, any system embodying the subject matter of the reference, and any testimony by those with knowledge of the subject matter of the reference, such as the named authors and inventors. Arm may rely upon uncited portions of the prior art references and on other publications and expert testimony to provide context, and as aids to understanding and interpreting the portions that are cited. Arm also may rely on uncited portions of the prior art references, other disclosed publications, and the testimony of experts to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

i. The Priority Date for the ’899 Patent

ICPillar’s Preliminary Infringement Contentions allege that the Asserted Claims of the ’899 Patent are entitled to a priority date of May 23, 2013. To the extent that ICPillar alleges that

any prior art relied upon in these Preliminary Invalidity Contentions does not qualify as prior art, Arm reserves the right to rebut those allegations (e.g., by demonstrating an earlier critical date for the challenged prior art and/or a later priority date for the Asserted Patent and/or Asserted Claim).

ii. The ’899 Patent Is Anticipated By The Prior Art

Some or all of the Asserted Claims of the ’899 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of the prior art references identified in the claim charts attached as Exhibit 899-A, which identify specific examples of where each limitation of the Asserted Claims is found in the respective prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

Arm identifies the following references as anticipating one or more of the Asserted Claims of the ’899 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate one or more of the claims of the ’899 Patent. Further, Arm contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following table.

Exhibit	Prior Art	Priority Date
899-A1	U.S. 4,922,432 (“Kobayashi”)	January 13, 1988
899-A2	U.S. 5,197,016 (“Sugimoto”)	January 13, 1988
899-A3	U.S. 5,870,588 (“Rompaey”)	October 23, 1995
899-A4	U.S. 6,477,683 (“Killian”)	February 5, 1999
899-A5	U.S. 6,862,563 (“Hakewill”)	October 14, 1998
899-A6	U.S. 2002/0059054 (“Bade”)	June 2, 2000
899-A7	U.S. 6,976,239 (“Allen”)	June 12, 2001
899-A8	U.S. 7,272,546 (“Brown”)	January 21, 2003
899-A9	U.S. 2003/0229482 (“Cook”)	April 25, 2003
899-A10	U.S. 2008/0222581 (“Banerjee”)	March 9, 2007
899-A11	U.S. 8,250,503 (“Vorbach”)	December 2, 2008

Exhibit	Prior Art	Priority Date
899-A12	Quartus Platform	No later than 2003
899-A13	Prior Art Socrates	No later than 2006
899-A14	RealView Development Suite	No later than 2001
899-A15	SoC Designer (including its incorporated AMBA Designer and RealView as taught in A14, and A16)	No later than 2007
899-A16	AMBA Designer	No later than 2006
899-A17	Van Rompaey / CoWare	1996
899-A18	Verkest / CoWare	1996

For the avoidance of doubt, Arm reserves the right to identify additional bases for qualification of the above references as prior art in the event that it is determined that the '899 Patent is not entitled to the priority date claimed by ICPillar.

To the extent any prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '899 Patent, Arm reserves the right to argue that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Arm has not specifically denoted that the prior art is to be combined with the knowledge of a person of ordinary skill in the art.

iii. The '899 Patent Is Obvious In View Of The Prior Art

To the extent the ICPillar argues that any limitation of the asserted claims of the '899 Patent are not explicitly disclosed by prior art identified above and in Exhibit 899-A, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

a. The Claims Are Obvious Over The Primary References In View Of One Or More Secondary References

To the extent the foregoing references are found not to anticipate the asserted claims of the ’899 Patent, the foregoing references render the asserted claims obvious, either alone or in combination with one or more of the other references identified above. A person of ordinary skill in the art would have been motivated to combine the various references cited herein so as to disclose each and every limitation of the asserted claims of the ’899 Patent.

Prior art references rendering the asserted claims of the ’899 Patent obvious, either alone or in combination with other references in Exhibits 899-A, are provided in the table below and in Exhibit 899-B. The prior art identified in Exhibit 899-A renders one or more asserted claims of the ’899 Patent obvious when read in combination with one or more of the other references charted in Exhibit 899-A, when read in combination with any of the prior art identified in Exhibit 899-B, and/or when read in view of the state of the art and knowledge of those skilled in the art at the relevant time.

Reference	Priority / Filing Date
U.S. 5,896,521 (“Shakleford”)	October 2, 1996
U.S. 5,949,993 (“Fritz”)	October 31, 1997
U.S. 6,110,223 (“Southgate 223”)	October 27, 1997
U.S. 6,161,211 (“Southgate”)	October 27, 1997
U.S. 6,401,230 (“Ahanessians”)	February 1, 1999
U.S. 6,477,697 (“Killian 697”)	February 5, 1999
U.S. 6,564,363 (“Dahl”)	July 18, 2001
U.S. 6,578,174 (“Zizzo”)	June 8, 2001
U.S. 6,851,094 (“Robertson”)	February 28, 2000
U.S. 7,171,632 (“Masuda”)	May 24, 2004
U.S. 7,240,303 (“Schubert”)	June 6, 2003
U.S. 7,275,233 (“McElvain”)	March 4, 2003
U.S. 7,284,225 (“Ballagh”)	May 20, 2004
U.S. 7,353,489 (“Dowling”)	May 28, 2004
U.S. 7,366,652 (“Wang”)	September 19, 2005
U.S. 7,392,255 (“Sholtis”)	July 31, 2003
U.S. 7,475,000 (“Cook”)	April 25, 2003
U.S. 7,454,732 (“McElvain 732”)	October 18, 2005

Reference	Priority / Filing Date
U.S. 7,493,470 ("Cumplido")	December 6, 2002
U.S. 7,512,728 ("Tseng")	November 29, 2004
U.S. 7,873,930 ("Vujkovic")	March 22, 2007
U.S. 8,036,874 ("Igarashi")	June 20, 2008
U.S. 8,103,987 ("Banarjee 987")	March 9, 2007
U.S. 8,316,341 ("Sandy")	September 17, 2009
U.S. 8,386,972 ("Hakewill 972")	December 16, 2009
U.S. 8,386,980 ("Murray 890")	November 18, 2010
U.S. 8,527,934 ("Ginetti")	September 9, 2010
U.S. 8,807,948 ("Luo")	September 29, 2011
U.S. 8,943,452 ("Hsu")	June 13, 2011
U.S. 9,088,491 ("Vaidya")	March 7, 2012
U.S. 9,171,114 ("Hakewill 114")	January 30, 2013
U.S. 9,195,784 ("Tseng 784")	April 1, 2011
U.S. 9,268,578 ("Cummings")	November 7, 2011
U.S. 9,275,185 ("McIlrath")	January 23, 2014
U.S. 9,591,496 ("Cummings 496")	January 12, 2016
U.S. 10,296,690 ("Vujkovic 690")	December 8, 2015
U.S. 10,867,333 ("Banerjee 333")	August 12, 2019
U.S. 2003/0204830 ("Brawn")	April 4, 2003
U.S. 2004/0268283 ("Perry")	June 24, 2003
U.S. 2005/0076315 ("Wen")	October 3, 2003
U.S. 2005/0262462 ("Janakiraman")	May 20, 2004
U.S. 2006/0075382 ("Shaburov")	October 5, 2004
U.S. 2006/0095882 ("Mankin")	September 8, 2004
U.S. 2006/0155968 ("Inuo")	June 21, 2004
U.S. 2007/0200596 ("Lee")	February 24, 2006
U.S. 2009/0113037 ("Pouchak")	October 24, 2007
U.S. 2009/0187756 ("Nollet")	December 10, 2008
U.S. 2010/0169857 ("Campi")	December 28, 2009

To the extent that ICPillar argues that any asserted claim of the '899 Patent is not disclosed or rendered obvious by any reference identified in Exhibit 899-A, the asserted claims nevertheless would have been obvious in light of one or more other reference identified in Exhibit 899-A and/or one or more references identified and charted in Exhibit 899-B and in view of the knowledge, experience, and understanding of persons of ordinary skill in the art.

Each and every reference identified is also relevant to the state of the art at the time of the alleged invention. Any of the references disclosed above may be combined with one another to

render obvious (and therefore invalid) each of the claims asserted by ICPillar from the ’899 Patent. Arm may rely upon a subset of the references identified above or all of the references identified above, including all references in Exhibits 899-A and 899-B, for purposes of obviousness depending on the Court’s claim constructions, positions taken by ICPillar during this litigation, and further investigation and discovery.

b. Exemplary Combinations Of The Prior Art

The table below provides an identification of exemplary combination of prior art references that, based on Arm’s present understanding of ICPillar’s Preliminary Infringement Contentions and apparent reading of the claims, render obvious one or more of the asserted claims of the ’899 Patent. The combinations of Exhibit 899-A and 899-B references identified below are non-exhaustive, and additional examples are apparent from other combinations of Exhibit 899-A references. Arm expressly notes that, although certain references charted in Exhibit A are listed in the left or right column below, Arm does not thereby imply any restriction as to which Exhibit A reference is primary and which Exhibit A reference is secondary in such a combination. Arm reserves the right to rely on either identified reference in the identified combinations as a primary and/or secondary reference.

Exemplary Combinations of Prior Art – ’899 Patent

Reference	Combination References
U.S. 4,922,432 (“Kobayashi”) (Exhibit 899-A1)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey, Verkest / CoWare, Vorbach, Wang, and/or Zizzo

Reference	Combination References
U.S. 5,197,016 (“Sugimoto”) (Exhibit 899-A2)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Van Rompaey, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 5,870,588 (“Rompaey”) (Exhibit 899-A3)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 6,477,683 (“Killian”) (Exhibit 899-A4)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 6,862,563 (“Hakewill”) (Exhibit 899-A5)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 2002/0059054 (“Bade”) (Exhibit 899-A6)	Ahanessians, Allen, AMBA Designer, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo

Reference	Combination References
U.S. 6,976,239 ("Allen") (Exhibit 899-A7)	Ahanessians, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 7,272,546 ("Brown") (Exhibit 899-A8)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 2003/0229482 ("Cook") (Exhibit 899-A9)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 2008/0222581 ("Banerjee") (Exhibit 899-A10)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 8,250,503 ("Vorbach") (Exhibit 899-A11)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Wang, and/or Zizzo

Reference	Combination References
Quartus Platform (Exhibit 899-A12)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
Prior Art Socrates (Exhibit 899-A13)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
RealView Development Suite (Exhibit 899-A14)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
SoC Designer (Exhibit 899-A15)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
AMBA Designer (Exhibit 899-A16)	Ahanessians, Allen, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo

Reference	Combination References
Van Rompaey / CoWare (Exhibit 899-A17)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
Verkest / CoWare (Exhibit 899-A18)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Vorbach, Wang, and/or Zizzo

It would have been obvious to make the combinations identified above for reasons that are readily apparent to one of ordinary skill in the art, as well as for the reasons explained in detail in the sections that follow and in Exhibit 899-B.

C. Other Grounds For Invalidity

Pursuant to the OGP and the Court's Scheduling Order, Arm identifies the following additional grounds for invalidity of the Asserted Claims of the '899 Patent. Arm reserves the right to supplement these disclosures based upon further investigation and discovery.

i. Invalidity Of The '899 Patent Based On 35 U.S.C. § 112(a) (Enablement and Written Description)

Based upon Arm's present understanding of the scope of the Asserted Claims of the '899 Patent, as informed by ICPillar's Preliminary Infringement Contentions (to the extent such positions can be understood), the following claim terms, phrases, or limitations render the applicable claims invalid because of a lack of enablement or sufficient written description:

- "outputting by the processor of a hardware integrated circuit design" (Claim 1);

- "[outputting by the processor / output] software programming commands" (Claims 1, 8);
- "the logic executed by the one or more processors operable to design a hardware integrated circuit" (Claim 8); and
- "simulate the hardware integrated circuit's functionality" (Claim 14).

These claim terms, phrases, and limitations, as apparently construed by ICPillar, fail to satisfy the enablement and/or written description requirements of 35 U.S.C. § 112. This is at least because the specification of the '899 Patent demonstrates that the patentee neither conceived of nor demonstrated possession of all that ICPillar now contends the claims cover. In addition, based on Arm's present understanding of ICPillar's Preliminary Infringement Contentions, each of the claims of the '899 Patent in which these claim terms, phrases, and limitations appear is invalid because the specification fails to provide sufficient disclosure to enable a person of ordinary skill in the art to which to which the alleged invention pertains, or with which it is most nearly connected, to implement the alleged invention without undue experimentation.

ii. Invalidity Of The '899 Patent Based On 35 U.S.C. § 112(b) (Indefiniteness)

Based upon Arm's present understanding of the scope of the Asserted Claims of the '899 Patent, as informed by ICPillar's Preliminary Infringement Contentions (to the extent such positions can be understood), the following claim terms, phrases, or limitations render the applicable claims invalid as indefinite:

- "the logic executed by the one or more processors operable to design a hardware integrated circuit" (Claim 8); and
- "output software programming commands to [sic] executed by the hardware integrated circuit for controlling the device…using a communication protocol compatible with the device through the communication bus of the hardware integrated circuit" (Claim 8).

This claimed phrase is indefinite because a person of ordinary skill in the art at the time of the alleged invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and the prosecution history, particularly given ICPillar's apparent constructions of the claims.

iii. Additional Grounds For Invalidity Of The '899 Patent

In addition to the preceding grounds for invalidity, Arm reserves the right to assert that the '899 Patent is invalid under 35 U.S.C. §§ 102 and/or 115 in the event that Arm obtains evidence that the named inventor of the '899 Patent did not invent (either alone or in conjunction with other parties) the subject matter claimed in the '899 Patent. Should Arm obtain such evidence, it will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived, and/or the circumstances surrounding the making of the invention before the patent application. Arm reserves the right to supplement these disclosures based on further investigation and discovery.

V. THE '657 PATENT IS INVALID

A. Identification of Prior Art

Arm contends that the prior art references described and charted in Exhibits 657-A and 657-B anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '657 Patent.

B. Bases for Invalidity

ICPillar asserts claims 1, 5, 6, 8, 9, 15, and 16 of the '657 Patent against Arm. These claims are invalid because the '657 Patent fails to meet one or more of the requirements for patentability. The individual bases for invalidity are provided below and in Exhibits 657-A and 657-B. Each of the prior art references, the underlying work, and/or the underlying apparatus or method qualifies as invalidating prior art under one or more sections of 35 U.S.C. §§ 102 and/or 103.

In an effort to focus the issues, Arm has cited exemplary portions of identified references, even where a reference may contain additional disclosures or support for a particular claim element. Each and every disclosure of the same limitation in the same reference is not necessarily identified. In addition, persons of ordinary skill in the art generally read a prior art reference as a whole and in the context of other publications and literature and in the context of their own knowledge and experience as persons of ordinary skill in the art. Thus, to understand and interpret any specific statement or disclosure within a prior art reference, such persons would rely on other information within the reference, along with other publications and their general scientific knowledge and experience in the field.

Each prior art reference identified in these Preliminary Invalidity Contentions therefore should be understood in the context of the reference itself, in conjunction with anything incorporated by reference or described as relevant technology by the reference, any documents that are referred to for further understanding by the reference, any system embodying the subject matter of the reference, and any testimony by those with knowledge of the subject matter of the reference, such as the named authors and inventors. Arm may rely upon uncited portions of the prior art references and on other publications and expert testimony to provide context, and as aids to understanding and interpreting the portions that are cited. Arm also may rely on uncited portions of the prior art references, other disclosed publications, and the testimony of experts to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

i. The Priority Date for the ’657 Patent

ICPillar’s Preliminary Infringement Contentions allege that the Asserted Claims of the ’657 Patent are entitled to a priority date of May 23, 2013. To the extent that ICPillar alleges that

any prior art relied upon in these Preliminary Invalidity Contentions does not qualify as prior art, Arm reserves the right to rebut those allegations (e.g., by demonstrating an earlier critical date for the challenged prior art and/or a later priority date for the Asserted Patent and/or Asserted Claim).

ii. The ’657 Patent Is Anticipated By The Prior Art

Some or all of the Asserted Claims of the ’657 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of the prior art references identified in the claim charts attached as Exhibit 657-A, which identify specific examples of where each limitation of the Asserted Claims is found in the respective prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

Arm identifies the following references as anticipating one or more of the Asserted Claims of the ’657 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate one or more of the claims of the ’ 657 Patent. Further, Arm contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following table.

Exhibit	Prior Art	Priority Date
657-A1	U.S. 4,922,432 (“Kobayashi”)	January 13, 1988
657-A2	U.S. 5,197,016 (“Sugimoto”)	January 13, 1988
657-A3	U.S. 5,870,588 (“Rompaey”)	October 23, 1995
657-A4	U.S. 6,477,683 (“Killian”)	February 5, 1999
657-A5	U.S. 6,862,563 (“Hakewill”)	October 14, 1998
657-A6	U.S. 2002/0059054 (“Bade”)	June 2, 2000
657-A7	U.S. 6,976,239 (“Allen”)	June 12, 2001
657-A8	U.S. 7,272,546 (“Brown”)	January 21, 2003
657-A9	U.S. 2003/0229482 (“Cook”)	April 25, 2003
657-A10	U.S. 2008/0222581 (“Banerjee”)	March 9, 2007
657-A11	U.S. 8,250,503 (“Vorbach”)	December 2, 2008

Exhibit	Prior Art	Priority Date
657-A12	Quartus Platform	No later than 2003
657-A13	Prior Art Socrates	No later than 2006
657-A14	RealView Development Suite	No later than 2001
657-A15	SoC Designer (including its incorporated AMBA Designer and RealView as taught in A14, and A16)	No later than 2007
657-A16	AMBA Designer	No later than 2006
657-A17	K. Van Rompaey, D. Verkest, I. Bolsens and H. De Man, "CoWare-a design environment for heterogeneous hardware/software systems," Proceedings EURO-DAC '96. European Design Automation Conference with EURO-VHDL '96 and Exhibition, Geneva, Switzerland, 1996, pp. 252-257, doi: 10.1109/EURDAC.1996.558213.	1996
657-A18	CoWare—A design environment for heterogeneous hardware/software systems, Verkest, D., Van Rompaey, K., Bolsens, I. et al. Des Autom Embed Syst 1, 357–386 (1996).	1996

For the avoidance of doubt, Arm reserves the right to identify additional bases for qualification of the above references as prior art in the event that it is determined that the ' 657 Patent is not entitled to the priority date claimed by ICPillar.

To the extent any prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '657 Patent, Arm reserves the right to argue that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Arm has not specifically denoted that the prior art is to be combined with the knowledge of a person of ordinary skill in the art.

iii. The '657 Patent Is Obvious In View Of The Prior Art

To the extent the ICPillar argues that any limitation of the asserted claims of the '657 Patent are not explicitly disclosed by prior art identified above and in Exhibit 657-A, any purported

differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

a. The Claims Are Obvious Over The Primary References In View Of One Or More Secondary References

To the extent the foregoing references are found not to anticipate the asserted claims of the ’657 Patent, the foregoing references render the asserted claims obvious, either alone or in combination with one or more of the other references identified above. A person of ordinary skill in the art would have been motivated to combine the various references cited herein so as to disclose each and every limitation of the asserted claims of the ’657 Patent.

Prior art references rendering the asserted claims of the ’657 Patent obvious, either alone or in combination with other references in Exhibits 657-A, are provided in the table below and in Exhibit 657-B. The prior art identified in Exhibit 657-A renders one or more asserted claims of the ’657 Patent obvious when read in combination with one or more of the other references charted in Exhibit 657-A, when read in combination with any of the prior art identified in Exhibit 657-B, and/or when read in view of the state of the art and knowledge of those skilled in the art at the relevant time.

Reference	Priority / Filing Date
U.S. 5,896,521 (“Shakleford”)	October 2, 1996
U.S. 5,949,993 (“Fritz”)	October 31, 1997
U.S. 6,110,223 (“Southgate 223”)	October 27, 1997
U.S. 6,161,211 (“Southgate”)	October 27, 1997
U.S. 6,401,230 (“Ahanessians”)	February 1, 1999
U.S. 6,477,697 (“Killian 697”)	February 5, 1999
U.S. 6,564,363 (“Dahl”)	July 18, 2001
U.S. 6,578,174 (“Zizzo”)	June 8, 2001
U.S. 6,851,094 (“Robertson”)	February 28, 2000
U.S. 7,171,632 (“Masuda”)	May 24, 2004

Reference	Priority / Filing Date
U.S. 7,240,303 (“Schubert”)	June 6, 2003
U.S. 7,275,233 (“McElvain”)	March 4, 2003
U.S. 7,284,225 (“Ballagh”)	May 20, 2004
U.S. 7,353,489 (“Dowling”)	May 28, 2004
U.S. 7,366,652 (“Wang”)	September 19, 2005
U.S. 7,392,255 (“Sholtis”)	July 31, 2003
U.S. 7,475,000 (“Cook”)	April 25, 2003
U.S. 7,454,732 (“McElvain 732”)	October 18, 2005
U.S. 7,493,470 (“Cumplido”)	December 6, 2002
U.S. 7,512,728 (“Tseng”)	November 29, 2004
U.S. 7,873,930 (“Vujkovic”)	March 22, 2007
U.S. 8,036,874 (“Igarashi”)	June 20, 2008
U.S. 8,103,987 (“Banarjee 987”)	March 9, 2007
U.S. 8,316,341 (“Sandy”)	September 17, 2009
U.S. 8,386,972 (“Hakewill 972”)	December 16, 2009
U.S. 8,386,980 (“Murray 890”)	November 18, 2010
U.S. 8,527,934 (“Ginetti”)	September 9, 2010
U.S. 8,807,948 (“Luo”)	September 29, 2011
U.S. 8,943,452 (“Hsu”)	June 13, 2011
U.S. 9,088,491 (“Vaidya”)	March 7, 2012
U.S. 9,171,114 (“Hakewill 114”)	January 30, 2013
U.S. 9,195,784 (“Tseng 784”)	April 1, 2011
U.S. 9,268,578 (“Cummings”)	November 7, 2011
U.S. 9,275,185 (“McIlrath”)	January 23, 2014
U.S. 9,591,496 (“Cummings 496”)	January 12, 2016
U.S. 10,296,690 (“Vujkovic 690”)	December 8, 2015
U.S. 10,867,333 (“Banerjee 333”)	August 12, 2019
U.S. 2003/0204830 (“Brawn”)	April 4, 2003
U.S. 2004/0268283 (“Perry”)	June 24, 2003
U.S. 2005/0076315 (“Wen”)	October 3, 2003
U.S. 2005/0262462 (“Janakiraman”)	May 20, 2004
U.S. 2006/0075382 (“Shaburov”)	October 5, 2004
U.S. 2006/0095882 (“Mankin”)	September 8, 2004
U.S. 2006/0155968 (“Inuo”)	June 21, 2004
U.S. 2007/0200596 (“Lee”)	February 24, 2006
U.S. 2009/0113037 (“Pouchak”)	October 24, 2007
U.S. 2009/0187756 (“Nollet”)	December 10, 2008
U.S. 2010/0169857 (“Campi”)	December 28, 2009

To the extent that ICPillar argues that any asserted claim of the ’657 Patent is not disclosed or rendered obvious by any reference identified in Exhibit 657-A, the asserted claims nevertheless would have been obvious in light of one or more other reference identified in Exhibit 657-A and/or

one or more references identified and charted in Exhibit 657-B and in view of the knowledge, experience, and understanding of persons of ordinary skill in the art.

Each and every reference identified is also relevant to the state of the art at the time of the alleged invention. Any of the references disclosed above may be combined with one another to render obvious (and therefore invalid) each of the claims asserted by ICPillar from the ’657 Patent. Arm may rely upon a subset of the references identified above or all of the references identified above, including all references in Exhibits 657-A and 657-B, for purposes of obviousness depending on the Court’s claim constructions, positions taken by ICPillar during this litigation, and further investigation and discovery.

b. Exemplary Combinations Of The Prior Art

The table below provides an identification of exemplary combination of prior art references that, based on Arm’s present understanding of ICPillar’s Preliminary Infringement Contentions and apparent reading of the claims, render obvious one or more of the asserted claims of the ’657 Patent. The combinations of Exhibit 657-A and 657-B references identified below are non-exhaustive, and additional examples are apparent from other combinations of Exhibit 657-A references. Arm expressly notes that, although certain references charted in Exhibit A are listed in the left or right column below, Arm does not thereby imply any restriction as to which Exhibit A reference is primary and which Exhibit A reference is secondary in such a combination. Arm reserves the right to rely on either identified reference in the identified combinations as a primary and/or secondary reference.

<u>Exemplary Combinations of Prior Art – ’657 Patent</u>

Reference	Combination References
U.S. 4,922,432 ("Kobayashi") (Exhibit 657-A1)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 5,197,016 ("Sugimoto") (Exhibit 657-A2)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 5,870,588 ("Rompaey") (Exhibit 657-A3)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 6,477,683 ("Killian") (Exhibit 657-A4)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 6,862,563 ("Hakewill") (Exhibit 657-A5)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo

Reference	Combination References
U.S. 2002/0059054 ("Bade") (Exhibit 657-A6)	Ahanessians, Allen, AMBA Designer, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 6,976,239 ("Allen") (Exhibit 657-A7)	Ahanessians, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 7,272,546 ("Brown") (Exhibit 657-A8)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 2003/0229482 ("Cook") (Exhibit 657-A9)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
U.S. 2008/0222581 ("Banerjee") (Exhibit 657-A10)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo

Reference	Combination References
U.S. 8,250,503 ("Vorbach") (Exhibit 657-A11)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Wang, and/or Zizzo
Quartus Platform (Exhibit 657-A12)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
Prior Art Socrates (Exhibit 657-A13)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
RealView Development Suite (Exhibit 657-A14)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
SoC Designer (including its incorporated AMBA Designer and RealView as taught in A14, and A16) (Exhibit 657-A15)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo

Reference	Combination References
AMBA Designer (Exhibit 657-A16)	Ahanessians, Allen, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
K. Van Rompaey, D. Verkest, I. Bolsens and H. De Man, "CoWare-a design environment for heterogeneous hardware/software systems," (Exhibit 657-A17)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Verkest / CoWare, Vorbach, Wang, and/or Zizzo
CoWare—A design environment for heterogeneous hardware/software systems, (Exhibit 657-A18)	Ahanessians, Allen, AMBA Designer, Bade, Banerjee, Banerjee 987, Brown, Cook, Dowling, Fritz, Hakewill, Igarashi, Killian, Killian 697, Kobayashi, Masuda, McElvain, McElvain 732, Quartus, RealView, Rompaey, Sandy, Schubert, Shackleford, SoC Designer, Socrates, Southgate, Southgate 223, Sugimoto, Van Rompaey / CoWare, Vorbach, Wang, and/or Zizzo

It would have been obvious to make the combinations identified above for reasons that are readily apparent to one of ordinary skill in the art, as well as for the reasons explained in detail in the sections that follow and in Exhibit 657-B.

C. Other Grounds For Invalidity

Pursuant to the OGP and the Court's Scheduling Order, Arm identifies the following additional grounds for invalidity of the Asserted Claims of the '657 Patent. Arm reserves the right to supplement these disclosures based upon further investigation and discovery.

i. Invalidity Of The '657 Patent Based On 35 U.S.C. § 112(a) (Enablement and Written Description)

Based upon Arm's present understanding of the scope of the Asserted Claims of the '657 Patent, as informed by ICPillar's Preliminary Infringement Contentions (to the extent such

positions can be understood), the following claim terms, phrases, or limitations render the applicable claims invalid because of a lack of enablement or sufficient written description:

- "a processor…to design a hardware integrated circuit and associated operating software" (Claim 1);
- "outputting by the processor a hardware integrated circuit design based on the selection of input and output characteristics of the electronic device" (Claim 1);
- "outputting by the processor software programming commands…for controlling the electronic device in accordance with the selection of categorized input and output characteristics" (Claim 1);
- "one or more processors operable to design a hardware integrated circuit design based on the selected…parameter values" (Claim 9); and
- "simulate the hardware integrated circuit's functionality" (Claim 15).

These claim terms, phrases, and limitations, as apparently construed by ICPillar, fail to satisfy the enablement and/or written description requirements of 35 U.S.C. § 112. This is at least because the specification of the '657 Patent demonstrates that the patentee neither conceived of nor demonstrated possession of all that ICPillar now contends the claims cover. In addition, based on Arm's present understanding of ICPillar's Preliminary Infringement Contentions, each of the claims of the '657 Patent in which these claim terms, phrases, and limitations appear is invalid because the specification fails to provide sufficient disclosure to enable a person of ordinary skill in the art to which to which the alleged invention pertains, or with which it is most nearly connected, to implement the alleged invention without undue experimentation.

ii. Invalidity Of The '657 Patent Based On 35 U.S.C. § 112(b) (Indefiniteness)

Based upon Arm's present understanding of the scope of the Asserted Claims of the '657 Patent, as informed by ICPillar's Preliminary Infringement Contentions (to the extent such positions can be understood), the following claim terms, phrases, or limitations render the applicable claims invalid as indefinite:

- "control type parameter" (Claims 1, 5, 9, 16);
- "display type parameter" (Claims 1, 5, 9, 16);
- "outputting by the processor software programming commands to be executed by the hardware integrated circuit…through the communication bus of the hardware integrated circuit using a communication protocol compatible with the electronic device and the hardware integrated circuit" (Claim 1); and
- "output software programming commands to be executed by the hardware integrated circuit…using a communication protocol compatible with the device and the hardware integrated circuit through the communication bus of the hardware integrated circuit" (Claim 9).

These claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given ICPillar's apparent constructions of the claims, any person of ordinary skill in the art at the time of the alleged invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and the prosecution history.

iii. Additional Grounds For Invalidity Of The '657 Patent

In addition to the preceding grounds for invalidity, Arm reserves the right to assert that the '657 Patent is invalid under 35 U.S.C. §§ 102 and/or 115 in the event that Arm obtains evidence that the named inventor of the '657 Patent did not invent (either alone or in conjunction with other parties) the subject matter claimed in the '657 Patent. Should Arm obtain such evidence, it will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived, and/or the circumstances surrounding the making of the invention before the patent application. Arm reserves the right to supplement these disclosures based on further investigation and discovery.

VI. INVALIDITY CONTENTIONS UNDER 35 U.S.C. § 101

Arm also contends that the Asserted Claims of the Asserted Patents are invalid under 35 U.S.C § 101 because they are not directed to patent-eligible subject matter. Whether an invention

is eligible for patent protection under 35 U.S.C. § 101 is a "threshold test." *See Bilski v. Kappos*, 561 U.S. 593, 602 (2010). Under this "threshold test," the court "must first determine whether the claims at issue are directed to a patent-ineligible concept," such as an abstract idea. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l,* 573 U.S. 208, 218 (2014). If so, the court must then "consider the elements of each claim both individually and 'as an ordered combination' to determine whether the additional elements 'transform the nature of the claim' into a patent-eligible application." *Id.* (quoting *Mayo Collaborative Servs. v. Prometheus Labs., Inc.,* 566 U.S. 66, 79 (2012)).

In *Alice,* the Supreme Court set forth a two-part test to analyze patent eligibility: (1) determine whether the claims are directed to an abstract idea or other patent-ineligible concept; and (2) if so, determine whether the claim amounts to "significantly more" than the abstract idea. If the claim does not recite "significantly more" than the abstract idea, it is invalid. *Id.* at 217-18.

The first step of the *Alice* test requires the Court to ask whether the claim is "directed to a patent-ineligible concept," such as an abstract idea. *Id.* at 217. An idea is abstract if it has "no particular concrete or tangible form." *Ultramercial, Inc. v. Hulu, LLC,* 772 F.3d 709, 715 (Fed. Cir. 2014). A telling and common feature of an abstract idea is that its elements are the equivalent of human work that can be performed without a computer. A method that "can be performed in the human mind, or by a human using a pen and paper" "is merely an abstract idea and is not patent-eligible under § 101." *CyberSource Corp. v. Retail Decisions, Inc.,* 654 F.3d 1366, 1372-73 (Fed. Cir. 2011); *see also Gottschalk v. Benson,* 409 U.S. 63, 67 (1972) (method that "can be done mentally" was an abstract idea). Furthermore, the fact that a computer can expedite a mental process does not turn an abstract idea into something patent-eligible. *See Bancorp Servs., LLC v. Sun Life Assurance Co. of Canada (U.S.),* 687 F.3d 1266, 1279 (Fed. Cir. 2012) ("Using a computer to accelerate an ineligible mental process does not make that process patent-eligible.").

For example, result-focused claims having no particular concrete or tangible form are directed to an abstract idea. *See Innovation Scis., LLC v. Amazon.com, Inc.*, 778 Fed. App'x 859, 862 (Fed. Cir. 2019) (finding a claim for "securely processing a credit card transaction with a payment server" was "directed to [an] abstract idea" because it was result-focused and had "no particular concrete or tangible form"); *VoIP-Pal.com, Inc. v. Apple Inc.*, 411 F. Supp. 3d 926, 952 (N.D. Cal. 2019) (finding ineligible a claim directed to routing communications because it "is worded in such broad, functional terms, so as to describe a desired result…without explaining *how* that result is achieved").

If the answer to the first question is yes, then the second step of the *Alice* framework requires the Court to determine whether there are "additional elements [that] 'transform the nature of the claim' into a patent-eligible application." *Alice,* 573 U.S. at 217 (quoting *Mayo,* 566 U.S. at 78). The second step entails a search for an "inventive concept" "that is sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the [ineligible concept] itself." *Id.* (alteration in original) (citation omitted). "Simply appending conventional steps, specified at a high level of generality, [is] not enough to supply an inventive concept" needed to make this transformation. *Id.* at 222 (citation omitted). Further, "[t]he introduction of a computer into the claims does not alter the analysis." *Id.* Neither "[s]tating an abstract idea while adding the words 'apply it with a computer,'" nor "limiting the use of an abstract idea 'to a particular technological environment,'" is enough for patent eligibility. *Id.* at 223 (citations omitted). Moreover, the Federal Circuit has held that the "machine-or-transformation test" "can provide a 'useful clue' in the second step of the *Alice* framework." *Ultramercial,* 772 F.3d at 716.

Where the additional elements are "'well-understood, routine, conventional activit[ies]' previously known to the industry," the claim is not saved and remains ineligible. *Alice,* 573 U.S.

225 (quoting *Mayo,* 566 U.S. at 73). Moreover, "[s]oftware may be patent eligible, but when a claim is not directed towards a process, the subject matter must exist in tangible form." *Allvoice Devs. US, LLC v. Microsoft Corp.*, 612 Fed. App'x 1009, 1018 (Fed. Cir. May 22, 2015). "Except for process claims, the eligible subject matter must exist in some physical or tangible form." *Id.* at 1017 (citing *Digitech Image Techs., LLC v. Elecs. For Imaging, Inc.*, 758 F.3d 1344, 1348 (Fed. Cir. 2014)). Where the claim elements are all software elements that do not expressly require hardware elements, the claim lacks subject matter eligibility. *Id.*

"In considering patent eligibility under § 101, one must focus on the claims." *Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1334 (Fed. Cir. 2012). "This is because a claim may 'preempt' only that which the claims encompass, not what is disclosed but left unclaimed." *Id.* As such, disclosures in the specification do not save an otherwise ineligible claim. *Id.*

A. The '899 Patent

Asserted Claims 1, 5, 6, 8, and 14 of the '899 Patent are invalid under 35 U.S.C. § 101 as directed to patent ineligible subject matter because they are directed to an abstract idea and do not contain an inventive concept that amounts to substantially more than a claim directed to the abstract idea itself.

Specifically, these result-focused claims are directed to the abstract idea of providing a circuit design and corresponding software based on received parameters. This amounts to no more than an activity that can be (and has been) performed by humans using a pen and paper for decades, merely applied with a computer.

The following claim elements are well-understood, routine, and conventional, as demonstrated by the prior art identified above and charted in Exhibits 899-A and 899-B. By way

of example only, the following table includes citations to exemplary prior art demonstrating that the corresponding claim elements are well-understood, routine, and convention in the industry.

Claim Element	**Exemplary Prior Art**
"memory" *(e.g., Claims 1, 8)*	*See* claim 8[b] in Exhibit 899-A charts. *See e.g.*, Shackleford, Fig. 3; Southgate 223, Figs. 8-9; Ahanessians, Fig. 9; McElvain, Fig. 2.
"processor(s)" *(e.g., Claims 1, 8)*	*See* claim 8[a] in Exhibit 899-A charts. *See also, e.g.*, Shackleford, Fig. 3; Southgate 223, Figs. 8-9; Ahanessians, Fig. 9; McElvain, Fig. 2.
"electronic device" / "device" *(e.g., Claims 1, 8)*	*See* claims 1[a]-1[d].
"schematic, layout, or both" *(e.g., Claim 6)*	*See* claim 6 in Exhibit 899-A charts. *See also, e.g.*, Shackleford at Fig. 35, 1:64-67; Southgate at Fig. 1; Ahanessians at Fig. 1:52-62, 7:7-26; Zizzo at 11:66-12:25.
"logic encoded in one or more non-transitory computer-readable media" *(e.g., Claim 8)*	*See* claim 8[b] in Exhibit 899-A charts. *See also, e.g.*, Shackleford, Fig. 3; Southgate 223, Figs. 8-9; Ahanessians, Fig. 9; McElvain, Fig. 2.
"communication bus" *(e.g., Claim 8)*	*See* claims 8[d] and 8[e] in Exhibit 899-A charts.
"simulate the hardware integrated circuit's functionality" *(e.g., Claim 14)*	*See* claim 14 in Exhibit 899-A charts. *See also, e.g.*, Shackleford at 3:52-56, 7:35-41; Fritz at 3:49-63, 4:8-24; Southgate at Abstract, Figs. 1, 3, 4, 3:57-4:10, 6:30-54, 7:10-28, 7:43-59; Ahanessians at 1:52-62; Zizzo at Fig. 5, 14:58-15:27, 15:59-67; Masuda at 9:13-35; Schubert at Figs. 1A-8, 15-23, 26-28, 31-33B, 38, 42, 12:24-32, 13:8-45, 15:34-48; Dowling at Fig. 1A, 4:10-27.

B. The ’657 Patent

Asserted Claims 1, 5, 6, 8, 9, 15, and 16 of the ’657 Patent are invalid under 35 U.S.C. § 101 as directed to patent ineligible subject matter because they are directed to an abstract idea and do not contain an inventive concept that amounts to substantially more than a claim directed to the abstract idea itself.

Specifically, these result-focused claims are directed to the abstract idea of providing a circuit design and corresponding software based on received parameters. This amounts to no more than an activity that can be (and has been) performed by humans using a pen and paper for decades, merely applied with a computer.

The following claim elements are well-understood, routine, and conventional, as demonstrated by the prior art identified above and charted in Exhibits 657-A and 657-B. By way of example only, the following table includes citations to exemplary prior art demonstrating that the corresponding claim elements are well-understood, routine, and convention in the industry.

Claim Element	**Exemplary Prior Art**
“electronic device” *(e.g., Claims 1, 9)*	*See* claims 1[a]-1[d] in Exhibit 657-A charts.
“hierarchal classification database” *(e.g., Claims 1, 16)*	*See* claims 1[a]-1[d] in Exhibit 657-A charts.
“memory” *(e.g., Claims 1, 9)*	*See* claims 1[e] and 9[c] in Exhibit 657-A charts. *See also, e.g.*, Shackleford, Fig. 3; Southgate 223, Figs. 8-9; Ahanessians, Fig. 9; McElvain, Fig. 2.
“processor” *(e.g., Claims 1, 9, 15)*	*See* claim 9[a] in Exhibit 657-A charts. *See also, e.g.*, Shackleford, Fig. 3; Southgate 223, Figs. 8-9; Ahanessians, Fig. 9; McElvain, Fig. 2.

Claim Element	Exemplary Prior Art
"hardware integrated circuit design" *(e.g., Claims 1, 5, 6, 9, 15)*	*See* claim 1[g] in Exhibit 657-A charts. *See also, e.g.*, Shackleford at 1:64-67, 2:36-42, 3:40-51, 4:1-7; Southgate at 6:55-7:9, 7:60-8:5; Ahanessians at 8:60-9:6; Killian 697 at Fig. 1, 3:42-58; Zizzo at Fig. 9, 11:66-12:25; Masuda at 2:54-3:12; Dowling at Fig. 2, 4:10-27.
"software programming commands" *(e.g., Claims 1, 9)*	*See* claim 1[h] in Exhibit 657-A charts. *See also, e.g.*, Shackleford at 2:48-67, 3:40-51, 7:14-34, 16:48-59; Fritz at Figs. 2, 4, 14, 2:59-67, 11:18-64; Killian 697 at Fig. 1, 3:42-58; Zizzo at Fig. 9; Masuda at 2:54-3:12; Dowling at 5:23-52.
"communication bus" *(e.g., Claims 1, 9)*	*See* claims 1[g] and 1[h] in Exhibit 657-A charts.
"schematic, layout, or both" *(e.g., Claim 6)*	*See* claim 6 in Exhibit 657-A charts. *See also, e.g.*, Shackleford at Fig. 35, 1:64-67; Southgate at Fig. 1; Ahanessians at Fig. 1:52-62, 7:7-26; Zizzo at 11:66-12:25.
"fabless development kit" *(e.g., Claim 8)*	*See* claim 8 in Exhibit 657-A charts.
"simulate the hardware integrated circuit's functionality" *(e.g., Claim 15)*	*See* claim 15 in Exhibit 657-A charts. *See also, e.g.*, Shackleford at 3:52-56, 7:35-41; Fritz at 3:49-63, 4:8-24; Southgate at Abstract, Figs. 1, 3, 4, 3:57-4:10, 6:30-54, 7:10-28, 7:43-59; Ahanessians at 1:52-62; Zizzo at Fig. 5, 14:58-15:27, 15:59-67; Masuda at 9:13-35; Schubert at Figs. 1A-8, 15-23, 26-28, 31-33B, 38, 42, 12:24-32, 13:8-45, 15:34-48; Dowling at Fig. 1A, 4:10-27.

VII. ACCOMPANYING DOCUMENT PRODUCTION

Based on its investigations to date and its understanding of ICPillar's Preliminary Infringement Contentions, Arm is concurrently producing copies of the prior art cited in these Preliminary Invalidity Contentions, labeled ARM_ICPILLAR_PRIOR_ART_0000001 –

ARM_ICPILLAR_PRIOR_ART_0028866 as well as documents sufficient to show the operation of the accused products, to the extent understood by Arm, labeled ARM_ICPILLAR_0000001 – ARM_ICPILLAR_0031206.

Arm notes that this case is in its early stages and its investigation is ongoing. Arm therefore reserves the right to identify and produce additional documents pursuant to the Court's Local Rules, the OGP, the Scheduling Order, and any other applicable Orders of the Court.

Dated: November 7, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing document was served upon all counsel of record via email on November 7, 2023.

/s/ Matthew W. Cornelia
Matthew W. Cornelia