

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ARM LIMITED,
Petitioner,

v.

ICPILLAR LLC,
Patent Owner.

IPR2024-00566
Patent 9,367,657 B2

Before DONNA M. PRAISS, BRIAN J. McNAMARA, and
CHRISTOPHER M. KAISER, *Administrative Patent Judges*.

PRAISS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Arm Limited (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1, 5, 6, 8, 9, 15, and 16 of U.S. Patent No. 9,367,657 B2 (Ex. 1001, “the ’657 patent”). Paper 2 (“Pet.”). ICPillar LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

Pursuant to Board authorization (Paper 7 (“Order”)), Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 9 (“Prelim. Reply”)), and Patent Owner filed a Preliminary Sur-reply (Paper 10 (“Prelim. Sur-Reply”)).

To institute *inter partes* review, we must determine that the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For the reasons discussed below, after considering the parties’ submissions and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’657 patent, and we determine *inter partes* review of all claims and all grounds asserted in the Petition.¹

A. Related Proceedings

The parties identify the following related court proceeding: *ICPillar LLC v. ARM Ltd., et al.*, Case No. 1:23-cv-00282 (W.D. Tex.) (“the parallel District Court litigation”). Pet. 93; Paper 4, 1 (Patent Owner’s Mandatory Notices).

¹ *Guidance on the Impact of SAS on AIA Trial Proceedings* (Apr. 26, 2018), <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>; *see also SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

B. Real Parties-in-Interest

The parties identify themselves as the real parties in interest. Pet. 92; Paper 4, 1.

C. The '657 Patent

The '657 patent is titled “System and Method for Universal Control of Electronic Devices” and issued on June 14, 2016. Ex. 1001, code (45), (54). The '657 patent is directed to “providing universal and integrated control to constructs and devices which may be controlled by micro control units (MCU) or other controlling hardware.” *Id.* at 3:45–48. The '657 patent is also directed to “delivering true universal automation and control of any device or construct that can be imagined within an automation and control ecosystem.” *Id.* at 3:50–52. The '657 patent’s Figure 5, reproduced below, discloses an Integrated Device Control System.

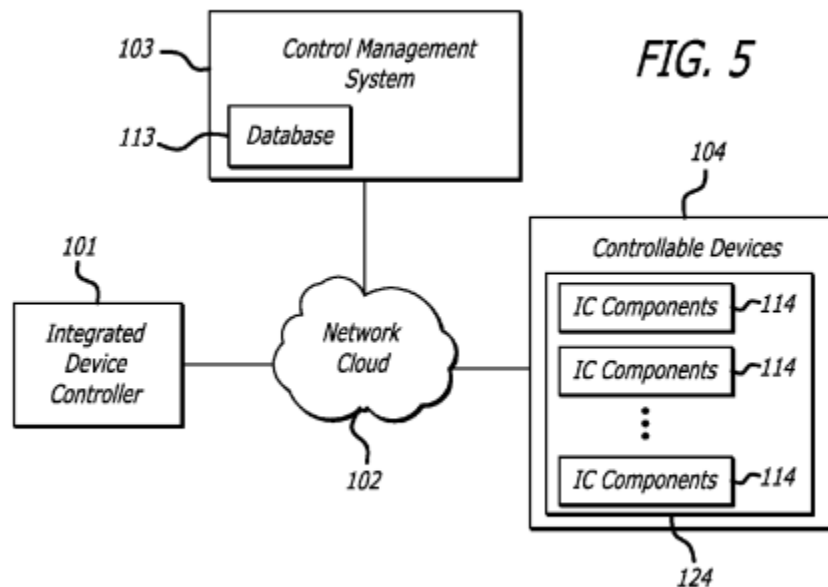


Figure 5 above shows an Integrated Device Control System with a Network Cloud 102 over which Integrated Device Controllers 101, Control

Management System 103, and/or Controllable Devices 104 may interact with each other. *Id.* at 10:51–64.

D. Illustrative Claims

Petitioner challenges claims 1, 5, 6, 8, 9, 15, and 16 of the '657 patent. Claims 1 and 9 are independent. Claim 1 is illustrative and reproduced below:

1[pre] A method for designing an integrated circuit which controls a device when the integrated circuit is integrated into the device comprising:

1[a] selecting a value for a control type parameter associated with an electronic device from a hierarchal classification database;

selecting a value for a display type parameter associated with the electronic device from the hierarchal classification database;

selecting a value for an input type parameter for the electronic device from the hierarchal classification database;

selecting a value for an output type parameter for the electronic device from the hierarchal classification database;

receiving the selected values for the control type, display type, input type and output type parameters into a memory of a processor programmed by software commands to design a hardware integrated circuit and associated operating software for controlling the hardware integrated circuit to control the electronic device;

1[b] analyzing by the processor the selected values for the control type, display type, input type and output type parameters of the electronic device;

1[c] outputting by the processor a hardware integrated circuit design based on the selection of input and output characteristics of the electronic device, the hardware integrated circuit including a communication bus for communicating with the electronic device; and

1[d] outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device through the communication bus of the hardware integrated circuit using a communication protocol compatible with the electronic device and the hardware integrated circuit.

Ex. 1001, 18:49–19:17 (numbering added as broken down in the Petition).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability.

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1, 5, 6, 8, 9, 15, 16	103	Banerjee ²
2	1, 5, 6, 8, 9, 15, 16	103	Rompaey, ³ CoWare I ⁴

In support of its unpatentability arguments, Petitioner relies on the declaration of Dr. Henry Houh (Ex. 1003).

II. ANALYSIS

A. Legal Standards

In *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under 35 U.S.C. § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior

² U.S. Patent Publication No. 2008/0222581 A1, published Sept. 11, 2008 (Ex. 1005).

³ U.S. Patent No. 5,870,588, issued Feb. 9, 1999 (Ex. 1004).

⁴ Verkest, D., et al., *CoWare – A design environment for heterogeneous hardware/software systems*, Des Autom Embed Syst 1, 357–386 (1996) (Ex. 1006).

art,” (3) the “differences between the prior art and the claims at issue,” and (4) if in evidence, “secondary considerations” of non-obviousness, such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *Id.* at 17–18. “While the sequence of these questions might be reordered in any particular case,” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the U.S. Court of Appeals for the Federal Circuit has repeatedly emphasized that “it is error to reach a conclusion of obviousness until all those factors are considered,” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016). Because Patent Owner does not address objective evidence of non-obviousness, we focus solely on the first three *Graham* factors.

B. Level of Ordinary Skill in the Art

Petitioner contends that one of ordinary skill in the art would be “familiar with automated circuit design” and “possess[] this knowledge through training and work experience, including having a Bachelor’s or Master’s Degree in computer science, electrical engineering, or a related field, with at least three years of practical experience.” Pet. 9.

At this stage of the proceeding, Patent Owner does not challenge the Petitioner’s definition of a person of ordinary skill in the art. *See* Prelim. Resp., generally.

On this record, we adopt Petitioner’s assessment of the level of ordinary skill in the art as it is consistent with the ’657 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b) (2022). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

No express construction of any claim term beyond its plain and ordinary meaning was asserted in the Petition or Preliminary Response. Pet. 8; Prelim. Resp., generally. The Board invited additional briefing on the proper claim construction of the term “outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device” after Petitioner requested additional briefing on how this term is met by the prior art references. Order 2–4.

According to Petitioner, the term should be broadly construed to encompass “internal outputs from ‘compilers’ that are then used by other portions of the design” and “any form of software or mechanics of

‘providing’ software.” Prelim. Reply 2–3.⁵ Petitioner contends that the term must be construed broadly to encompass the embodiment shown in the ’657 patent’s Figure 4 illustrating output 71 of compiler 67, which is an internal input to ASIC Design 69 described as “a circuit design such as a layout or a schematic that can be sent out to a manufacturer for fabrication.” *Id.* at 1–2 (quoting Ex. 1001, 10:3–5)⁶ (emphasis omitted). Petitioner directs us to the disclosure that Figure 4’s output 71 (ASIC Programming) “may be software to be programmed and/or stored in a fabricated ASIC.” *Id.* at 2 (quoting Ex. 1001, 10:5–6)⁷ (emphasis omitted). Petitioner contends that the ’657 patent defines “software” broadly. *Id.* The portion of the ’657 patent disclosure that Petitioner indirectly cites states “[h]erein, reference to software may encompass one or more applications, byte code, one or more computer programs, one or more executable, one or more instructions, logic, machine code, one or more scripts, or source code, and vice versa where appropriate.” Ex. 1001, 17:17–21.

Patent Owner asserts that Petitioner’s proffered claim construction is incorrect because the language of the claim itself “does not suggest ‘internal’ software for use by the design tool, nor that the second recited ‘output[]’ could be part of the first.” Prelim. Sur-Reply 2. According to Patent Owner,

⁵ Petitioner’s Preliminary Reply cites to U.S. Patent 8,924,899 (“the ’899 patent”), to which the ’657 patent claims the benefit of priority. Prelim. Reply 1; Ex. 1001, code (63). The ’899 patent, however, is not an exhibit in this proceeding. Papers filed in this proceeding should refer to the exhibits filed in this proceeding.

⁶ Petitioner’s citation to Exhibit 1001, column 9, lines 59–61 for the quote is incorrect for this proceeding because it does not refer to the ’657 patent.

⁷ Petitioner’s citation to Exhibit 1001, column 9, lines 61–62 for the quote is incorrect for this proceeding because it does not refer to the ’657 patent.

viewed in context, the '657 patent defines “software” broadly for “an exemplary computer system, not of the invention’s outputs.” *Id.* Patent Owner asserts this definition describes the software types that a computer could execute, not a definition of “software programming commands” recited in claim 1[d]. *Id.* Regarding the '657's Figure 4, Patent Owner asserts that Petitioner has not shown that Programming 71 must be an internal output for internal use because both Design 69 and Programming 71 are shown as outputs, not inputs, of the compiler. *Id.* at 4. Regarding the term “layout,” Patent Owner asserts this is merely a description of physical hardware for fabrication and that “[i]t is impossible for ‘software programming commands’ to be ‘stored in “layouts.”” *Id.* at 3 (citing Ex. 2001 ¶¶ 32, 76, 90).

For purposes of this Decision, we construe the term “outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device” as referring to software programming commands that are capable of controlling an electronic device, that are output by a processor, and that are not merely a circuit design for fabrication. We emphasize that this construction is preliminary and based on the current record; to the extent the parties wish to argue for a different construction or to further clarify this construction, we encourage them to present arguments and supporting evidence at trial.

For the purposes of this Decision, we need not expressly construe any additional claim terms.⁸ *See Nidec Motor Corp. v. Zhongshan Broad Ocean*

⁸ If either party intends to further argue claim construction at trial, including what is the plain and ordinary meaning of a term, they should do so in a clearly designated section of their briefing so as to expressly identify such

Motor Co. Matal, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Discretionary Denial under 35 U.S.C. § 314(a)

Patent Owner argues the Board should exercise its discretion under 35 U.S.C. § 314(a) and deny institution in light of the parallel District Court litigation involving the ’657 patent. Prelim. Resp. 44–65.

Institution of *inter partes* review is at the Director’s discretion, which has been delegated to the Board under her guidance. *See* 35 U.S.C. § 314(a); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [USPTO] is permitted, but never compelled, to institute an IPR proceeding.”); 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”).

In assessing whether to exercise such discretion, the Board weighs six non-exclusive factors, known as the *Fintiv* factors. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). The six *Fintiv* factors that the Board considers as part of this balanced assessment when determining whether to use its discretion to deny institution are:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

arguments. *See, e.g.*, 37 C.F.R. § 42.104(b)(3) (content of petition); *see also* Patent Trial and Appeal Board Consolidated Trial Practice Guide, 84 Fed. Reg. 64,280, at 46, 48–45 (Nov. 2019) (available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>). Claim construction arguments should not be relegated to patentability arguments on the facts.

2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv, Paper 11, 5–6. Recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to more than one factor,” the Board “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* at 6.

On June 21, 2022, the Director of the USPTO issued several clarifications concerning the application of the *Fintiv* factors. *See Interim Procedure For Discretionary Denials In AIA Post-Grant Proceedings With Parallel District Court Litigation*, issued June 21, 2022 (“Guidance Memo”).⁹ The Guidance Memo clarifies “the PTAB’s current application of *Fintiv* to discretionary institution where there is parallel litigation.” *Id.* at 2. The Guidance Memo instructs us not to “discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” *Id.* at 3 (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A)). The Guidance Memo

⁹ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

explains that such a *Sotera* stipulation “mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB . . . and allows the PTAB to review grounds that the parallel district court litigation will not resolve.” *Id.* at 7–8. When such a stipulation is offered after the Board’s decision on whether to institute review, however, it is too late to gain the benefit of the rule articulated in the Guidance Memo. *NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13, 4 (PTAB Sept. 7, 2022) (precedential).

Here, Petitioner “stipulates ‘not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.’” Prelim. Reply 10 (quoting Ex. 1020, 1). Petitioner offered this stipulation prior to a decision on whether to institute review, so it is timely under *NXP*. Accordingly, pursuant to the Guidance Memo, we do not exercise discretion under *Fintiv* to deny institution.

E. Ground 1: Obviousness over Banerjee

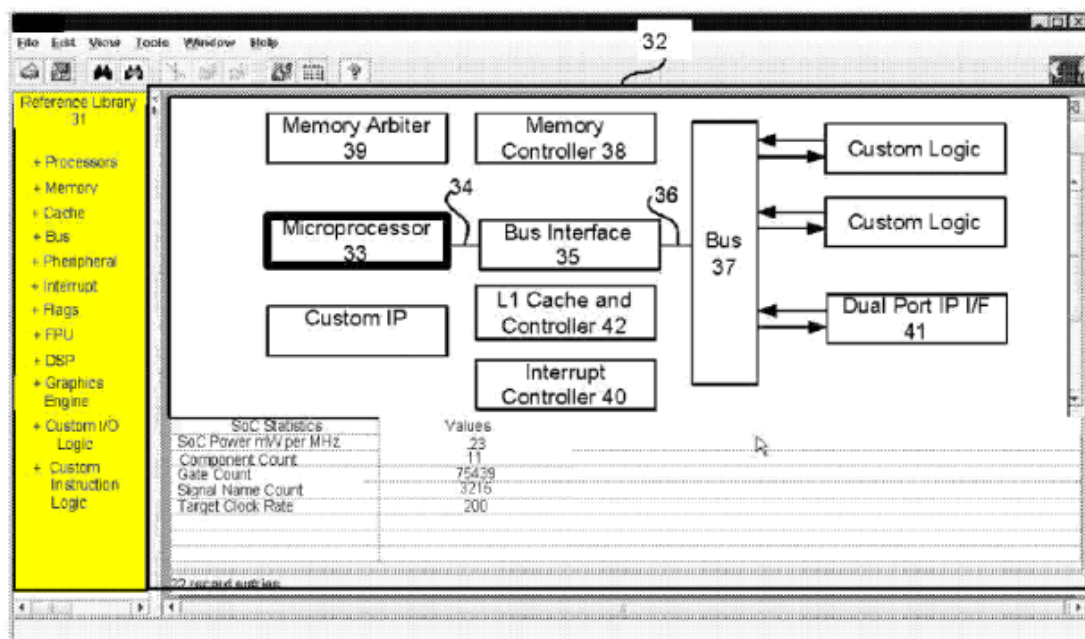
Petitioner argues that claims 1, 5, 6, 8, 9, 15, and 16 would have been obvious over Banerjee. Pet. 14–53; Reply 3–7. Patent Owner disagrees. Prelim. Resp. 2–25; Prelim. Sur-Reply 1–9. Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on this asserted obviousness ground with respect to at least claim 1.

1. Overview of Banerjee (Ex. 1005)

Banerjee is a U.S. patent application titled “Remote Interface for Managing the Design and Configuration of an Integrated Circuit Semiconductor Design.” Ex. 1005, code (54). Banerjee relates to “a mechanism for facilitating the design process of an IC [(Integrated Circuit)]

comprising a system on a chip (SoC).” *Id.* ¶ 1. Banerjee discloses “the automated description of hardware components, such as a processor core, and software components, such as application and operating software, as well as the integration of the hardware and software components.” *Id.* ¶ 8.

Petitioner’s annotated version of Banerjee Figure 3 is reproduced below.



Pet. 15 (citing Ex. 1005, Fig. 3). Figure 3, as annotated by Petitioner and reproduced above, depicts “a graphical user interface (GUI) associated with module 21 of the computer program 15.” Ex. 1005 ¶ 47. Banerjee discloses that “[c]omponents are identified in the reference area 31 and when selected are instantiated in the work palette 32.” *Id.* The “reference area 31 may provide the designer of a SoC with a plurality of configurable or configured processor cores so that the designer can implement a wide range of functions ranging from conventional DSP functions to media-processing functions while employing a consistent set of development tools.” *Id.* ¶ 48.

2. *Analysis of Claim 1*

a) *Disputed Limitation 1[d]*

Claim 1 recites

outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device through the communication bus of the hardware integrated circuit using a communication protocol compatible with the electronic device and the hardware integrated circuit.

Ex. 1001, 19:9–16.

Petitioner contends that Banerjee teaches or suggests this limitation. Pet. 44–47; Prelim. Reply 1–7. Specifically, Petitioner first directs us to a disclosure in Banerjee of the “output[of] the software based on the selections identified in 1[a],” including “(1) the operating system; (2) application software; (3) application specific instruction extensions; and (4) ‘middleware’ (such as I/O device driver software).” Pet. 44–45 (citing Ex. 1003 ¶¶ 472–480; Ex. 1005 ¶¶ 38–39, 45–46, 56, 67, 78, 84). Petitioner also argues that Banerjee teaches generating and outputting operating system software that is stored within the designed device. *Id.* at 45–47 (citing Ex. 1003 ¶¶ 472–480; Ex. 1005 ¶¶ 72–83, Fig. 5).

Patent Owner argues that “Banerjee’s tool outputs only a hardware description file. It does not output software programming commands to be executed by the IC, to control the electronic device into which it is integrated.” Prelim. Resp. 13–14; *see* Prelim. Resp. 14–25 (developing argument further). In particular, Patent Owner argues that “[w]hat the Petition points to in Banerjee in reference to this limitation are internal analyses in Banerjee’s tool during the hardware design process. These

intermediate analyses do not produce any output from the tool and certainly not executable software commands.” *Id.* at 14 (citing Ex. 2001 ¶ 44).

On the present record, we determine that Petitioner has shown sufficiently that Banerjee teaches outputting software intended to be installed on the designed integrated circuit that is capable of controlling the device into which the designed integrated circuit is installed. At paragraphs 72–83, Banerjee discloses the operation of its operating system optimization module. Ex. 1005 ¶¶ 38, 72–83. In particular, Banerjee teaches that the operating system optimization module can “compile a symmetric multiprocessing operating system” and that “the optimized operating system is compiled into a reduced footprint operating system that is instantiated in the device.” *Id.* ¶¶ 82–83. Because Banerjee teaches both compiling an operating system and instantiating that operating system in the designed device, the present record shows sufficiently that Banerjee teaches outputting software to run on the designed device.

Patent Owner’s declarant, Joseph C. McAlexander III, P.E., disagrees with this interpretation, testifying that Banerjee’s paragraph 83 teaches only “compil[ing] the characteristics of the typical or ‘baseline’ ‘operating system configuration’ . . . in order to analyze its expected ‘footprint’ on the IC and how it is expected to be instantiated on the device.” Ex. 2001 ¶ 65. But the idea that Banerjee is concerned only with analyzing how the operating system is expected to be instantiated appears to contradict Banerjee’s teaching that the “reduced footprint operating system . . . is instantiated in the device,” which suggests actual, not merely expected, instantiation in the device. On the present record, beyond stating that “Banerjee only outputs a hardware description file,” Mr. McAlexander does not explain why Banerjee

should be interpreted in this alternate fashion. *Id.* ¶ 66 (citing Ex. 1005 ¶¶ 44, 69, 84). There is no explanation of why the cited paragraphs of Banerjee should be interpreted to limit Banerjee's disclosure (which, as discussed above, includes a teaching that the operating system is compiled and instantiated in the designed device) to merely outputting a hardware description file. *Id.*

Accordingly, on the present record, Petitioner has shown sufficiently that Banerjee teaches or suggests limitation 1[d].

b) Undisputed Limitations of Claim 1

Claim 1 also recites

1[pre] A method for designing an integrated circuit which controls a device when the integrated circuit is integrated into the device comprising:

1[a] selecting a value for a control type parameter associated with an electronic device from a hierarchal classification database;

selecting a value for a display type parameter associated with the electronic device from the hierarchal classification database;

selecting a value for an input type parameter for the electronic device from the hierarchal classification database;

selecting a value for an output type parameter for the electronic device from the hierarchal classification database;

receiving the selected values for the control type, display type, input type and output type parameters into a memory of a processor programmed by software commands to design a hardware integrated circuit and associated operating software for controlling the hardware integrated circuit to control the electronic device;

1[b] analyzing by the processor the selected values for the control type, display type, input type and output type parameters of the electronic device; [and]

1[c] outputting by the processor a hardware integrated circuit design based on the selection of input and output characteristics of the electronic device, the hardware integrated circuit including a communication bus for communicating with the electronic device.

Ex. 1001, 18:49–19:8. Petitioner argues that these additional limitations would have been obvious over Banerjee. *See* Pet. 18–44.

After reviewing Petitioner’s arguments and information regarding the limitations identified immediately above, including the Houh Declaration, which are not addressed by Patent Owner at this stage (*see* Prelim. Resp.; Prelim. Sur-Reply), we are persuaded that Petitioner sufficiently demonstrates, for purposes of this Decision, that the preamble of claim 1 and limitations 1[a], 1[b], and 1[c] would have been obvious to a person having ordinary skill in the art in light of Banerjee.

c) Conclusion Regarding Claim 1

Based on the current record, we determine that there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 1 is unpatentable as obvious in view of Banerjee. Accordingly, we institute *inter partes* review with respect to all grounds asserted in the Petition.

3. Claims 5, 6, 8, 9, 15, and 16

Because Petitioner demonstrates a reasonable likelihood of success in proving that at least one claim of the ’657 patent is unpatentable, we institute on all grounds and all claims raised in the Petition. *See* 37 C.F.R.

§ 42.108(a). Therefore, at this stage of the proceeding, it is not necessary for us to provide an assessment of every challenge raised by Petitioner,

especially, as in this case, when Patent Owner does not separately argue those claims. Those challenges, in our view, are best left for trial after full development of the record.

F. Ground 2: Obviousness over Rompaey and CoWare I

Petitioner argues that claims 1, 5, 6, 8, 9, 15, and 16 are obvious over Rompaey and CoWare I. Pet. 54–88; Reply 7–10. Patent Owner disagrees. Prelim. Resp. 25–44; Prelim. Sur-Reply 1–9.

1. Overview of Rompaey (Ex. 1004)

Rompaey is a U.S. patent titled “Design Environment and a Design Method for Hardware/Software Co-Design.” Ex. 1004, code (54). Rompaey describes a “hardware and software co-design environment and design methodology based on a data-model that allows one to specify, simulate, and synthesize heterogeneous hardware and software architectures from a heterogeneous specification.” *Id.*, Abstract. The environment allows for “interactive synthesis of hardware and software interfaces,” by defining “primitive objects to represent a specification of an essentially digital system.” *Id.* Defining the primitive objects “describ[es] the specification of the system in one or more processes, each process representing a functional aspect of the system.” *Id.*

2. Overview of CoWare I (Ex. 1006)

CoWare I is a research paper titled “CoWare – A design environment for heterogeneous hardware/software systems.” Ex. 1006, Title. CoWare I describes a “heterogenous system design environment based on co-specification, co-simulation and co-synthesis.” *Id.*, Abstract. CoWare I describes “[m]odularity in the specification is provided by means of processes,” and that a “single *process* can have multiple host language

encapsulations describing different implementations for the same component, or for the same component represented at different abstraction levels.” *Id.* at 3.

3. *Analysis of Claim 1*

a) *Disputed Limitation 1[d]*

Claim 1 recites

outputting by the processor software programming commands to be executed by the hardware integrated circuit for controlling the electronic device in accordance with the selection of categorized input and output characteristics of the electronic device through the communication bus of the hardware integrated circuit using a communication protocol compatible with the electronic device and the hardware integrated circuit.

Ex. 1001, 19:9–16.

Petitioner contends that Rompaey teaches or suggests this limitation. Pet. 82–84; Prelim. Reply 7–10. Specifically, Petitioner first directs us to a disclosure in Rompaey of “the hardware output and the associated ‘applic. Software’ and ‘IO device drivers’ to interface with the display, keyboard, and program controls.” Pet. 83 (citing Ex. 1003 ¶¶ 295–296; Ex. 1004, codes (54), (57), 6:45–53, 8:4–38, 25:29–26:49, Figs. 2, 6, 7, 9, 18). Petitioner also argues that “Rompaey describes the output of ‘I/O device driver’ software” because “[t]he I/O device driver processes are merged with the original software application code’ controlling the device.” *Id.* (citing Ex. 1003 ¶ 296; Ex. 1004, 12:35–43, 17:59–64, 18:31–46, 19:10–28, 26:38–49, 27:61–64).

Patent Owner argues that the portions of Rompaey to which Petitioner directs us “make it perfectly clear to artisans that when Rompaey refers to the ‘software’ on the chip to be designed, it is referring to such ‘software’ in

the context of what is ‘in’ a ‘model.’” Prelim. Resp. 34 (quoting Ex. 2001 ¶ 85).

There is evidence to support the contentions of both Petitioner and Patent Owner. On the present record, it appears that Petitioner is correct that there are steps of Rompaey’s method that output software, and the evidence introduced by Patent Owner supports (but does not, on the present record, mandate) a finding that the software being output is not intended to be used to control the device into which the integrated circuit being designed will be installed. Much of the evidence supporting each side is testimonial and has not yet been tested by cross-examination. Accordingly, the issue of whether Rompaey teaches or suggests limitation 1[d] is best resolved at trial.

b) Undisputed Limitations of Claim 1

Claim 1 also recites

1[pre] A method for designing an integrated circuit which controls a device when the integrated circuit is integrated into the device comprising:

1[a] selecting a value for a control type parameter associated with an electronic device from a hierarchal classification database;

selecting a value for a display type parameter associated with the electronic device from the hierarchal classification database;

selecting a value for an input type parameter for the electronic device from the hierarchal classification database;

selecting a value for an output type parameter for the electronic device from the hierarchal classification database;

receiving the selected values for the control type, display type, input type and output type parameters into a memory of a processor programmed by software commands to

design a hardware integrated circuit and associated operating software for controlling the hardware integrated circuit to control the electronic device;

1[b] analyzing by the processor the selected values for the control type, display type, input type and output type parameters of the electronic device; [and]

1[c] outputting by the processor a hardware integrated circuit design based on the selection of input and output characteristics of the electronic device, the hardware integrated circuit including a communication bus for communicating with the electronic device.

Ex. 1001, 18:49–19:8. Petitioner argues that these additional limitations would have been obvious over Rompaey and CoWare I. *See* Pet. 54–82.

After reviewing Petitioner’s arguments and evidence regarding the limitations identified immediately above, including the Houh Declaration, which are not addressed by Patent Owner at this stage (*see* Prelim. Resp.; Prelim. Sur-Reply), we are persuaded that Petitioner sufficiently demonstrates, for purposes of this Decision, that the preamble of claim 1 and limitations 1[a], 1[b], and 1[c] would have been obvious to a person having ordinary skill in the art in light of the combination of Rompaey and CoWare I.

c) Conclusion Regarding Claim 1

Based on the current record, we do not reach a conclusion as to whether there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 1 is unpatentable as obvious in view of Rompaey and CoWare I. As discussed above, however, we institute review on all grounds asserted in the Petition.

4. *Claims 5, 6, 8, 9, 15, and 16*

Because Petitioner demonstrates a reasonable likelihood of success in proving that at least one claim of the '657 patent is unpatentable, we institute on all grounds and all claims raised in the Petition. *See* 37 C.F.R.

§ 42.108(a). Therefore, at this stage of the proceeding, it is not necessary for us to provide an assessment of every challenge raised by Petitioner, especially, as in this case, when Patent Owner does not separately argue those claims. Those challenges, in our view, are best left for trial after full development of the record.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the '657 patent, and we institute *inter partes* review on all challenged claims and on all grounds presented.

Our factual findings, conclusions of law, and determinations at this stage of the proceeding are preliminary, and based on the evidentiary record developed thus far. This is not a final decision as to the patentability of claims for which *inter partes* review is instituted. Our final decision will be based on the record as fully developed during trial.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1, 5, 6, 8, 9, 15, and 16 of the '657 patent on the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this decision.

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