DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as "MARC") code and contain information such as a physical description of the material, metadata from the material's publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item's MARC record indicates the date of an item's public availability.

5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book's physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library's collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I have reviewed Exhibit MTK-1004, "A 32-bit PowerPC System-on-a-Chip with Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling" by Kevin J. Nowka, et. al as published in *IEEE Journal of Solid-State Circuits*, November 2002.

7. Attached hereto as Appendix NOWKA01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix NOWKA01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the November 2002 edition of *IEEE Journal of Solid-State Circuits* containing "A 32-bit PowerPC System-on-a-Chip with Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling." In comparing Exhibit MTK-1004 to Appendix NOWKA01, it is my determination that Exhibit MTK-1004 is a true and correct copy of "A 32-bit PowerPC System-on-a-Chip with Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling" by Kevin J.

Nowka et. al as published in *IEEE Journal of Solid-State Circuits* November 2002.

8. The 008 field of the MARC record in Appendix NOWKA01 indicates the date of record creation. The 008 field of Appendix NOWKA01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975 and held the journal in perpetuity until 2008. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* November 2002 and therefore "A 32-bit PowerPC System-on-a-Chip with Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling" was made available to the public shortly after its initial release in November 2002.

9. I have reviewed Exhibit MTK-1016, "Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design" by Tadahiro Kuroda, et. al as published in *IEEE Journal of Solid-State Circuits*, March 1998.

10. Attached hereto as Appendix KURODA01 is a true and correct copy of the MARC record for *IEEE Journal of Solid-State Circuits* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix

KURODA01 accurately describes the title, author, publisher, and ISSN number of *IEEE Journal of Solid-State Circuits.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the March 1998 edition of *IEEE Journal of Solid-State Circuits* containing "Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design." In comparing Exhibit MTK-1016 to Appendix KURODA01, it is my determination that Exhibit MTK-1016 is a true and correct copy of "Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design" by Tadahiro Kuroda, et. al as published in *IEEE Journal of Solid-State Circuits* March 1998.

11. The 008 field of the MARC record in Appendix KURODA01 indicates the date of record creation. The 008 field of Appendix KURODA01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of September 1, 1975 and held the journal in perpetuity until 2008. Considering this information, it is my determination that *IEEE Journal of Solid-State Circuits* March 1998 and therefore "Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design" was made available to the public shortly after its initial release in March 1998.

12. I have reviewed Exhibit MTK-1017, *Dynamic Power Management: Design Techniques and CAD Tools* by Luca Benini and Giovanni de Micheli.

13. Attached hereto as Appendix BENINI01 is a true and correct copy of the MARC record for *Dynamic Power Management: Design Techniques and CAD Tools* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix BENINI01 accurately describes the title, author, publisher, and ISBN number of *Dynamic Power Management: Design Techniques and CAD Tools.* In comparing Exhibit MTK-1017 to Appendix BENINI01, it is my determination that Exhibit MTK-1017 is a true and correct copy of *Dynamic Power Management: Design Techniques and CAD Tools* by Luca Benini and Giovanni de Micheli.

14. The 008 field of the MARC record in Appendix BENINI01 indicates the date of record creation. The 008 field of Appendix BENINI01 indicates Penn State University library first acquired this book as of February 18, 1998. Considering this information, it is my determination that *Dynamic Power Management: Design Techniques and CAD Tools* was made available to the public shortly after its initial acquisition as of February 18, 1998.

15. I have reviewed Exhibit MTK-1018, "A Survey of Design Techniques for System-Level Dynamic Power Management" by Luca Benini, et. al as published in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, June 2000.

16. Attached hereto as Appendix BENINI02 is a true and correct copy of the MARC record for *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix BENINI02 accurately describes the title, author, publisher, and ISSN number of *IEEE Transactions on Very Large Scale Integration (VLSI) Systems.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the June 2000 edition of *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* containing "A Survey of Design Techniques for System-Level Dynamic Power Management." In comparing Exhibit MTK-1018 to Appendix BENINI02, it is my determination that Exhibit MTK-1018 is a true and correct copy of "A Survey of Design Techniques for System-Level Dynamic Power Management" by Luca Benini, et. al as published in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* June 2000.

17. The 008 field of the MARC record in Appendix BENINI02 indicates the date of record creation. The 008 field of Appendix BENINI02 indicates the Carnegie Library of Pittsburgh first acquired this journal as of July 7, 1992 and held the journal in perpetuity until 2009. Considering this information, it is my determination that *IEEE Transactions on Very Large Scale Integration Systems* June 2000 and therefore "A Survey of Design Techniques for System-Level Dynamic Power Management" was made available to the public shortly after its initial release in June 2000.

18. I have reviewed Exhibit MTK-1019, "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" by David Lackey, et. al as published in *IEEE/ACM International Conference on Computer-Aided Design*, December 2002.

19. Attached hereto as IEEE01 is a screen capture of a webpage entitled "Managing power and performance for system-on-chip designs using Voltage Islands". I secure these screen captures myself from https://ieeexplore.ieee.org/document/1167534. This page is found on the Institute of Electrical and Electronics Engineers' website and describes "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" by David Lackey, et. al as found in Exhibit MTK-1019.

Appendix IEEE01's description of the Lackey paper indicates this paper was published in the proceedings for IEEE/ACM International Conference on Computer Aided Design 2002. According to Appendix IEEE01, this conference took place from November 10 – 14, 2002 and was added to the IEEE Xplore database as of January 29, 2003.

20. Attached hereto as Appendix LACKEY01 is a true and correct copy of the MARC record for *IEEE/ACM International Conference on Computer-Aided Design* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix LACKEY01 accurately describes the title, author, publisher, and ISSN number of *IEEE/ACM International Conference on Computer-Aided Design.* The 'Availability' field of this record visible on page 3 indicates this collection includes the December 2002 edition of *IEEE/ACM International Conference on Computer-Aided Design* containing "Managing Power and Performance for System-on-Chip Designs using Voltage Islands." In comparing Exhibit MTK-1019 to Appendix LACKEY01, it is my determination that Exhibit MTK-1019 is a true and correct copy of "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" by David Lackey, et. al as published in

IEEE/ACM International Conference on Computer-Aided Design December 2002.

21. The 008 field of the MARC record in Appendix LACKEY01 indicates the date of record creation. The 008 field of Appendix LACKEY01 indicates the Penn State University library first acquired this journal as of March 2, 2001 and held the journal in perpetuity until 2004. Considering this information, it is my determination that *IEEE/ACM International Conference on Computer-Aided Design* December 2002 and therefore "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" was made available to the public shortly after its initial release in December 2002.

22. I have reviewed Exhibit MTK-1020, "Policy Optimization for Dynamic Power Management" by Luca Benini, et. al as published in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, June 1999.

23. Attached hereto as Appendix BENINI03 is a true and correct copy of the MARC record for *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog.

The MARC record contained within Appendix BENINI03 accurately describes the title, author, publisher, and ISSN number of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. The 'Lib Has' field of this record visible on page 2 indicates this collection includes the June 1999 edition of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* containing "Policy Optimization for Dynamic Power Management." In comparing Exhibit MTK-1020 to Appendix BENINI03, it is my determination that Exhibit MTK-1020 is a true and correct copy of "Policy Optimization for Dynamic Power Management" by Luca Benini, et. al as published in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* June 1999.

24. The 008 field of the MARC record in Appendix BENINI03 indicates the date of record creation. The 008 field of Appendix BENINI03 indicates the Carnegie Library of Pittsburgh first acquired this journal as of August 18, 1981 and held the journal in perpetuity until 2009. Considering this information, it is my determination that *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* June 1999 and therefore "Policy Optimization for Dynamic Power Management" was made available to the public shortly after its initial release in June 1999.

25. I have reviewed Exhibit MTK-1021, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling" by Greg Semeraro, et. al as published in *Proceedings of the Eight International Symposium on High-Performance Computer Architecture (HPCA 02)*.

26. Attached hereto as Appendix SEMERARO01 is a true and correct copy of the MARC record for *Proceedings of the Eight International Symposium on High-Performance Computer Architecture (HPCA 02)* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix SEMERARO01 accurately describes the title, author, publisher, and ISBN number of *Proceedings of the Eight International Symposium on High-Performance Computer Architecture (HPCA 02)*. In comparing Exhibit MTK-1021 to Appendix SEMERARO01, it is my determination that Exhibit MTK-1021 is a true and correct copy of "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling" by Greg Semeraro, et. al as published in *Proceedings of the Eight International Symposium on High-Performance Computer Architecture (HPCA 02)*.

27. The 008 field of the MARC record in Appendix SEMERARO01 indicates the date of record creation. The 008 field of Appendix SEMERARO01 indicates the Penn State University library first acquired these proceedings as of June 12, 2002. Considering this information, it is my determination that *Proceedings of the Eight International Symposium on High-Performance Computer Architecture (HPCA 02)* and therefore "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling" was made available to the public shortly after its initial acquisition as of June 12, 2002.

28. I have reviewed Exhibit MTK-1022, "Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems" by Santanu Dutta, et. al as published in *IEEE Design & Test of Computers*, September/October 2001.

29. Attached hereto as Appendix DUTTA01 is a true and correct copy of the MARC record for *IEEE Design & Test of Computers* as held by the Carnegie Library of Pittsburgh. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DUTTA01 accurately describes the title, author, publisher, and ISSN number of *IEEE Design & Test of Computers.* The 'Lib Has' field of this record visible on page 2 indicates this collection includes the

September/October 2001 edition of *IEEE Design & Test of Computers* containing "Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems." In comparing Exhibit MTK-1022 to Appendix DUTTA01, it is my determination that Exhibit MTK-1022 is a true and correct copy of "Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems" by Santanu Dutta, et. al as published in *IEEE Design & Test of Computers* September/October 2001.

30. The 008 field of the MARC record in Appendix DUTTA01 indicates the date of record creation. The 008 field of Appendix DUTTA01 indicates the Carnegie Library of Pittsburgh first acquired this journal as of October 17, 1983 and held the journal in perpetuity until 2009. Considering this information, it is my determination that *IEEE Design & Test of Computers* September/October 2001 and therefore "Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems" was made available to the public shortly after its initial release in September/October 2001.

31. I am familiar with the Internet Archive, a digital library formally certified by the State of California as a public library. Among other services that the Internet Archive makes available to the general public is the Wayback Machine, an online archive. The Internet Archive's Wayback Machine

service archives webpages as of a certain capture date to track changes in the web over time. The Internet Archive has been in operation as a nonprofit library since 1996 and has hosted the Wayback Machine service since its inception in 2001. During my time as a librarian, I frequently used the Internet Archive's Wayback Machine for research and instruction purposes. This includes teaching instructional classes on using the Wayback Machine to library patrons and using the Wayback Machine to research reference inquiries that require hard-to-find online resources. I consider the Internet Archive's recordskeeping to be as rigorous and detailed as other formal library recordskeeping practices such as MARC records, OCLC records and Dublin Core.

32. I have reviewed Exhibit MTK-1023, a paper entitled "The CoreConnect Bus Architecture" by IBM Corporation.

33. Attached hereto as Appendix IBM01 is a screen capture of the Internet Archive Wayback Machine entry forhttp://www-01.ibm.com/chips/techlib/techlib.nsf/productfamilies/CoreConnect_Bus_Architecture. I secured these screen captures myself from http://www-01.ibm.com/chips/techlib/techlib.nsf/productfamilies/CoreConnect_Bus_Architecture. Exhibit MTK-1004, also known as "A 32-bit PowerPC System-

on-a-Chip with Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling" by Nowka, et. al, contains a citation of "The CoreConnect Bus Architecture" referencing this webpage as www.chips.ibm.com/techlib/techlib.nsf/productfamilies/CoreConnect_Bus_Architecture/. Appendix IBM01 is the result of the Internet Archive results for www.chips.ibm.com/techlib/techlib.nsf/productfamilies/CoreConnect_Bus_Architecture/.

34. Appendix IBM01 contains a page from a historical version of the IBM website describing various technical documents, including "The CoreConnect Bus Architecture". Clicking on the link to "The CoreConnect Bus Architecture" leads to a page offering the document for download. Appendix IBM01 also dates their copy of "The CoreConnect Bus Architecture" with the note "09/01/99". Considering Appendix IBM01 indicates http://www-01.ibm.com/chips/techlib/techlib.nsf/productfamilies/CoreConnect_Bus_Architecture was first preserved by the Internet Archive as of September 16, 2007, it is also my determination that http://www-01.ibm.com/chips/techlib/techlib.nsf/productfamilies/CoreConnect_Bus_Arc

hitecture was first available to the public by the Internet Archive as of September 17, 2007 and likely earlier by IBM itself.

35. Attached hereto as Appendix IBM02 is a screen capture of the Internet Archive Wayback Machine entry for http://www.chips.ibm.com/products/coreconnect/docs/crcon_wp.pdf. I secured these screen captures myself from https://web.archive.org/web/20000816221308/http://www.chips.ibm.com/products/coreconnect/docs/crcon_wp.pdf.

36. Appendix IBM02 contains a PDF copy of "The CoreConnect Bus Architecture" by IBM Corporation. In comparing Appendix IBM02 to Exhibit MTK-1023, it is my determination that Exhibit MTK-1023 is a true and correct copy of "The CoreConnect Bus Architecture". Considering Appendix IBM02 indicates "The CoreConnect Bus Architecture" was first preserved by the Internet Archive as of August 16, 2000, it is also my determination that "The CoreConnect Bus Architecture" was first available to the public by the Internet Archive as of August 16, 2000 if not earlier by IBM itself.

37. I have reviewed Exhibit MTK-1024, *The Computer Engineering Handbook* by Vojin G. Oklobdzija.

38. Attached hereto as Appendix OKLOBDZIJA01 is a true and correct copy of the MARC record for *The Computer Engineering Handbook* as held by the Carnegie Mellon University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix OKLOBDZIJA01 accurately describes the title, author, publisher, and ISBN number of *The Computer Engineering Handbook.* In comparing Exhibit MTK-1024 to Appendix OKLOBDZIJA01, it is my determination that Exhibit MTK-1024 is a true and correct copy of *The Computer Engineering Handbook* by Vojin G. Oklobdzija.

39. The 008 field of the MARC record in Appendix OKLOBDZIJA01 indicates the date of record creation. The 008 field of Appendix OKLOBDZIJA01 indicates Carnegie Mellon University library first acquired this book as of September 20, 2001. Considering this information, it is my determination that *The Computer Engineering Handbook* was made available to the public shortly after its initial acquisition as of September 20, 2001.

40. I have reviewed Exhibit MTK-1025, *Computer Systems: Concepts and Design* by Glenn A. Gibson.

41. Attached hereto as Appendix GIBSON01 is a true and correct copy of the MARC record for *Computer Systems: Concepts and Design* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix GIBSON01 accurately describes the title, author, publisher, and ISBN number of *Computer Systems: Concepts and Design.* In comparing Exhibit MTK-1025 to Appendix GIBSON01, it is my determination that Exhibit MTK-1025 is a true and correct copy of *Computer Systems: Concepts and Design* by Glenn A. Gibson.

42. The 008 field of the MARC record in Appendix GIBSON01 indicates the date of record creation. The 008 field of Appendix GIBSON01 indicates Penn State University library first acquired this book as of February 15, 1991. Considering this information, it is my determination that *Computer Systems: Concepts and Design* was made available to the public shortly after its initial acquisition as of February 15, 1991.

43. I have reviewed Exhibit MTK-1026, *Multimedia Information Networking* by Nalin K. Sharda.

44. Attached hereto as Appendix SHARDA01 is a true and correct copy of the MARC record for *Multimedia Information Networking* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix SHARDA01 accurately describes the title, author, publisher, and ISBN number of *Multimedia Information Networking.* In comparing Exhibit MTK-1026 to Appendix SHARDA01, it is my determination that Exhibit MTK-1026 is a true and correct copy of *Multimedia Information Networking* by Nalin K. Sharda.

45. The 008 field of the MARC record in Appendix SHARDA01 indicates the date of record creation. The 008 field of Appendix SHARDA01 indicates Penn State University library first acquired this book as of November 27, 2000. Considering this information, it is my determination that *Multimedia Information Networking* was made available to the public shortly after its initial acquisition in November 27, 2000.

46. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

47. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 3/1/2024



June Ann Munford

APPENDIX CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter
- Treasurer, 2012

Library Of Michigan
- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014
- New Directors Conference Panel Member

Southwest Michigan Library Cooperative
- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Civil Action No. 4:21-cv-149-ALM)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (IPR2022-00818)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Erise I.P.

- Apple
  - v. Ericsson Inc. (IPR2022-00715)
  - v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)
  - v. INVT (Case No. 20-1881)
  - v. Navblazer LLC (IPR2020-01253)
  - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
  - v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
  - v. Telefonaktiebolaget LM Ericsson (IPR2022-00275)
- Fanduel
  - v. CGT (Case No. 19-1393)
- Garmin
  - v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)
- Netscout
  - v. Longhorn HD LLC (Case No. 2:20-cv-00349)
  - v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)
- Sony Interactive Entertainment LLC
  - v. Bot M8 LLC (IPR2020-01288)
  - v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)
- Unified Patents

v. GE Video Compression (Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple

  v. AliveCor (3:21-cv-03958)

  v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)

  v. Koss Corporation (IPR2021-00305)

  v. Masimo (IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)

  v. Neonode (Case No. 21-cv-08872-EMC)

  v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- Dell

  v. Neo Wireless (IPR2022-00616)

- Dish Network

  v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

  v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

  v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

  v. SPG Dry Cooling (IPR2021-00688)

- Genetec

  v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

v. Bell Northern Research LLC (IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- Metaswitch

  v. Sonus Networks (IPR2018-01719)

- Microsoft

  v. Throughputer Inc (IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

  v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

  v. EagleView Technologies (IPR2022-01009)

- Neuroderm Ltd.

  v. Abbvie, Inc (Case No. PGR2022-00040)

- Realtek Semiconductor

v. Future Link (IPR2021-01182)

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- Intel Corporation

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- Twitter Inc

  v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)

- TCL Industries

  v. Koninklijke Philips NV (IPR2021-00495, IPR2021-00496 and IPR2021-00497)

Pillsbury Winthrop Shaw Pittman

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v. Costco (Case No. 4:21-cv-149)
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- Wolfspeed

  v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

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- Cadence Design Systems Inc.

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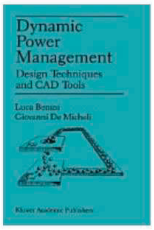
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Managing power and performance for system-on-chip designs using Voltage Islands

Publisher: IEEE Cite This PDF

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» Voltage Island Scenarios and Examples
» System-level Power Management Approaches
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Abstract:
This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption. Effective use of Voltage Islands for meeting SoC power and performance requirements, while meeting Time to Market (TAT) demands, requires novel approaches throughout the design flow as well as special circuit components and chip powering structures. This paper outlines methods being used today to design Voltage Islands in a rapid-TAT product development environment, and discusses the need for industry EDA advances to create an industry-wide Voltage Island design capability.

Published in: IEEE/ACM International Conference on Computer Aided Design, 2002. ICCAD 2002.

Date of Conference: 10-14 November 2002

DOI: 10.1109/ICCAD.2002.1167534

Publisher: IEEE

Date Added to IEEE *Xplore*: 29 January 2003

Conference Location: San Jose, CA, USA

Print ISBN:0-7803-7607-2

Print ISSN: 1092-3152

Background
The total power consumed by conventional CMOS circuitry is composed of two sources. The first is active power, this power represents the power consumed by the intended work of the circuit to switch states and thus execute logic functions. Active power is primarily composed of the power associated with the charging or discharging of the capacitance of the switching nodes [1]. The magnitude of this power is given by equation 1.

$$P_{active} = C^{*}Vdd2^{*}F \quad (1)$$

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As silicon technology scales, the frequency of operation increase by 30% each. Assuming perfect scaling, these increases are exactly

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Proceedings. 1999 International Symposium on Low Power Electronics and Design (Cat. No.99TH8477)
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A 32-bit PowerPC system-on-a-chip with support for dynamic voltage scaling and dynamic frequency scaling
IEEE Journal of Solid-State Circuits
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offset by a corresponding 30% decrease in Vdd, and the power per unit area remains constant. However, frequency of operation has increased at a faster rate than the scaling of the silicon process technology [2], [3]. This has led to an increase in power

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362	0		a| Nov. 5/9, 2000-
500			a| Published: Boulder, CO : MP Associates, Inc., 2001-
500			a| Latest issue consulted: Nov. 7/11, 2004.
530			a| Also issued online, and on CD-ROM, 2006-
550			a| Sponsored by: IEEE Circuits & Systems Society, IEEE Computer Society DATC, Association for Computing Machinery/SIGDA; in cooperation with: The Institute of Electrical and Electronics Engineers, Inc.
650		0	a| Computer-aided design v| Congresses.
650		0	a| Integrated circuits x| Computer-aided design v| Congresses.
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710	2		a| Institute of Electrical and Electronics Engineers.
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776	1		a| IEEE/ACM International Conference on Computer-Aided Design. s| ICCAD (Online) w| (OCoLC)57665602
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037			b| IEEE, 345 E. 47th St., New York, NY 10017
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866		0	8| 0 a| 2001-2004


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ICCAD / IEEE/ACM International Conference on Computer-Aided Design

Conference Author:	IEEE/ACM International Conference on Computer-Aided Design
Additional Titles:	ICCAD -- IEEE/ACM Int. Conf. Comput. Aided Des, Proceedings of the ... IEEE/ACM International Conference on Computer-Aided Design, Proceedings of the ... International Conference on Computer-Aided Design 2001-, IEEE/ACM digest of technical papers, and Digest of technical papers
Published:	New York, NY : IEEE, [2000-]
Copyright Date:	©2000-
Physical Description:	volumes : illustrations ; 28 cm
Additional Creators:	Institute of Electrical and Electronics Engineers, IEEE Circuits and Systems Society, IEEE Computer Society. Design Automation Technical Committee, and ACM Special Interest Group on Design Automation

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Dates of Publication and/or Sequential Designation:
Nov. 5/9, 2000-

Subject(s):
Computer-aided design—Congresses
Integrated circuits—Computer-aided design—Congresses
Electronic circuit design—Congresses

ISSN:
1933-7760

Publication Frequency:
Annual

Note:
Published: Boulder, CO : MP Associates, Inc., 2001-
Latest issue consulted: Nov. 7/11, 2004.

Other Forms:
Also issued online, and on CD-ROM, 2006-

Issuing Body:

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245 00 IEEE transactions on computer-aided design of integrated
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246 10 Transactions on computer-aided design of integrated
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246 23 IEEE transactions on computer aided design of integrated
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260    New York, NY :|bInstitute of Electrical and Electronics
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300    volumes :|billustrations ;|c28 cm
310    Monthly,|bJan. 1988-
321    Quarterly
321    Bimonthly,|b-Nov. 1987
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510 1  Physics abstracts. Science abstracts. Series A|x0036-8091
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510 2  International aerospace abstracts|x0020-5842|b1983-
515    Vol. designation CAD drops with v. 7, no. 1 (Jan. 1988).
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710 2  IEEE Circuits and Systems Society.
710 2  Institute of Electrical and Electronics Engineers.
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901    |cSer
935    ADN-7153
936    July 1982
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22.01.2024

Title	**IEEE transactions on computer-aided design of integrated circuits and systems : a publication of the IEEE Circuits and Systems Society.**
Publisher	New York, NY : Institute of Electrical and Electronics Engineers, ©1982-
Description	volumes : illustrations ; 28 cm
Frequency	Monthly, Jan. 1988- Quarterly Bimonthly, -Nov. 1987
Pub Date	Vol. CAD-1, no. 1 (Jan. 1982)-
Location	CLP Main (Oakland) Second Floor - Magazines
Lib Has	Volume 3 (1984) to Volume 28, no. 2 (2009).

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Note	Vol. designation CAD drops with v. 7, no. 1 (Jan. 1988).
Subject	Integrated circuits -- Design and construction -- Data processing -- Periodicals. *Show similar items*
Addt'l Author	IEEE Circuits and Systems Society. Institute of Electrical and Electronics Engineers.
Key Title	IEEE trans. comput.-aided des. integr. circuits syst. IEEE transactions on computer-aided design of integrated circuits and systems
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260			a| Los Alamitos : b| IEEE Computer Society Press c| Jan. 2002	
300			a| 323 p. b| ill c| 28.000 x 020.000 cm.	
506			a| License restrictions may limit access.	
520	8		a| Annotation b| The keynote speaker at the February 2002 conference discussed "the software industry: ten lessons for long life." Subsequent papers (27 in all) are arranged in sections on energy and thermal management, speculative multithreading, potpourri, memory-aware scheduling, latency tolerance and caches, speculation and prediction, multiprocessor systems, and pipelining and microarchitecture. A panel discussion addresses the question: "What will have the greatest impact in 2010: the processor, the memory, or the interconnect?" Indexing is by author only. Annotation copyrighted by Book News Inc., Portland, OR.	
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856	4	0	u| http://SK8ES4MC2L.search.serialssolutions.com/?sid=sersol&SS_jc=TC0000451541&title=8th%20International%20Symposium%20on%20High%20Performance%20Computer%20Architecture%3A%20Proceedings%202002%3A%20Cambridge%2C%20MA	
955			a| Books In Print, (c) 2011 R.R. Bowker LLC	
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8th International Symposium on High Performance Computer Architecture [electronic resource]: Proceedings 2002: Cambridge, MA

Corporate Author: IEEE Computer Society, Technical Committee on Computer Architecture Staff

Published: Los Alamitos : IEEE Computer Society Press Jan. 2002

Physical Description: 323 p. ill 28.000 x 020.000 cm.

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serialssolutions.com

Restrictions on Access:

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Summary:

Annotation The keynote speaker at the February 2002 conference discussed "the software industry: ten lessons for long life." Subsequent papers (27 in all) are arranged in sections on energy and thermal management, speculative multithreading, potpourri, memory-aware scheduling, latency tolerance and caches, speculation and prediction, multiprocessor systems, and pipelining and microarchitecture. A panel discussion addresses the question: "What will have the greatest impact in 2010: the processor, the memory, or the interconnect?" Indexing is by author only. Annotation copyrighted by Book News Inc., Portland, OR.

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ISBN:

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310    Quarterly,|bMar. 1991-
321    Quarterly,|bFeb. 1984-
321    Bimonthly,|b<Oct. 1987>-Dec. 1990
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362 0  Vol. 1, no. 1 (Feb. 1984)-
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510 2  Electronics and communications abstracts journal
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510 2  International aerospace abstracts|x0020-5842|b1984-
510 2  ISMEC bulletin|x0306-0039
510 2  Pollution abstracts with indexes|x0032-3624
510 2  Safety science abstracts journal|x0160-1342
515    Vol. 1, no. 1 also called premiere issue.
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Title	**IEEE design & test of computers / IEEE Computer Society [and] the Institute of Electrical and Electronics Engineers, Inc.**
Publisher	Los Alamitos, CA : IEEE Computer Society, ©1984-
Frequency	Quarterly, Mar. 1991- Quarterly, Feb. 1984- Bimonthly, <Oct. 1987>-Dec. 1990
Pub Date	Vol. 1, no. 1 (Feb. 1984)-
Location	CLP Main (Oakland) Second Floor - Magazines
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Indexed In:	Index to IEEE publications 0099-1368 Electronics and communications abstracts journal (Riverdale) 0361-3313 International aerospace abstracts 0020-5842 1984- ISMEC bulletin 0306-0039 Pollution abstracts with indexes 0032-3624 Safety science abstracts journal 0160-1342
Note	Vol. 1, no. 1 also called premiere issue. Available also on microfilm and microfiche from the Institute of Electrical and Electronics Engineers.
Subject	Computer engineering -- Periodicals. Electronic digital computers -- Testing -- Periodicals. *Show similar items*
Addt'l Author	IEEE Computer Society. Institute of Electrical and Electronics Engineers.
Key Title	IEEE des. test comput. IEEE design & test of computers
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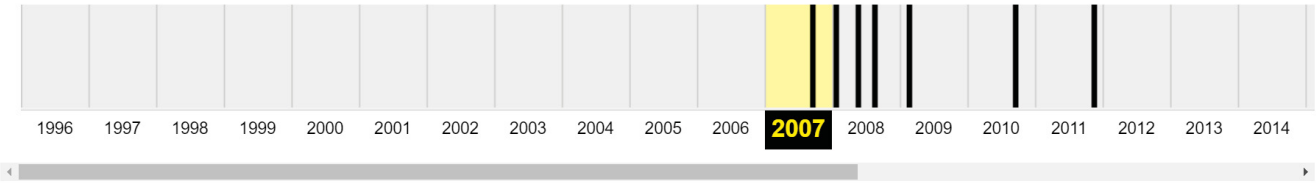
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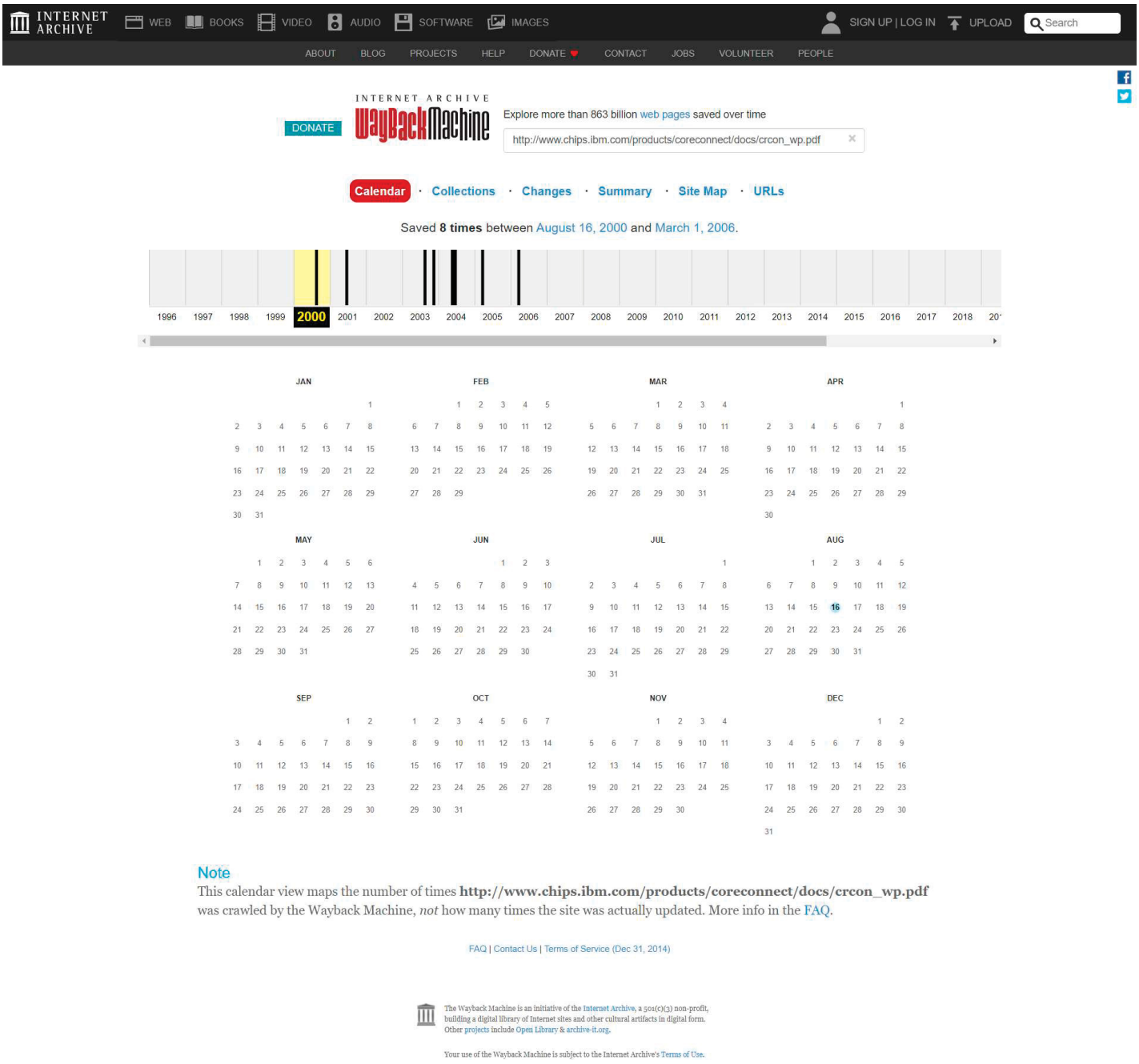
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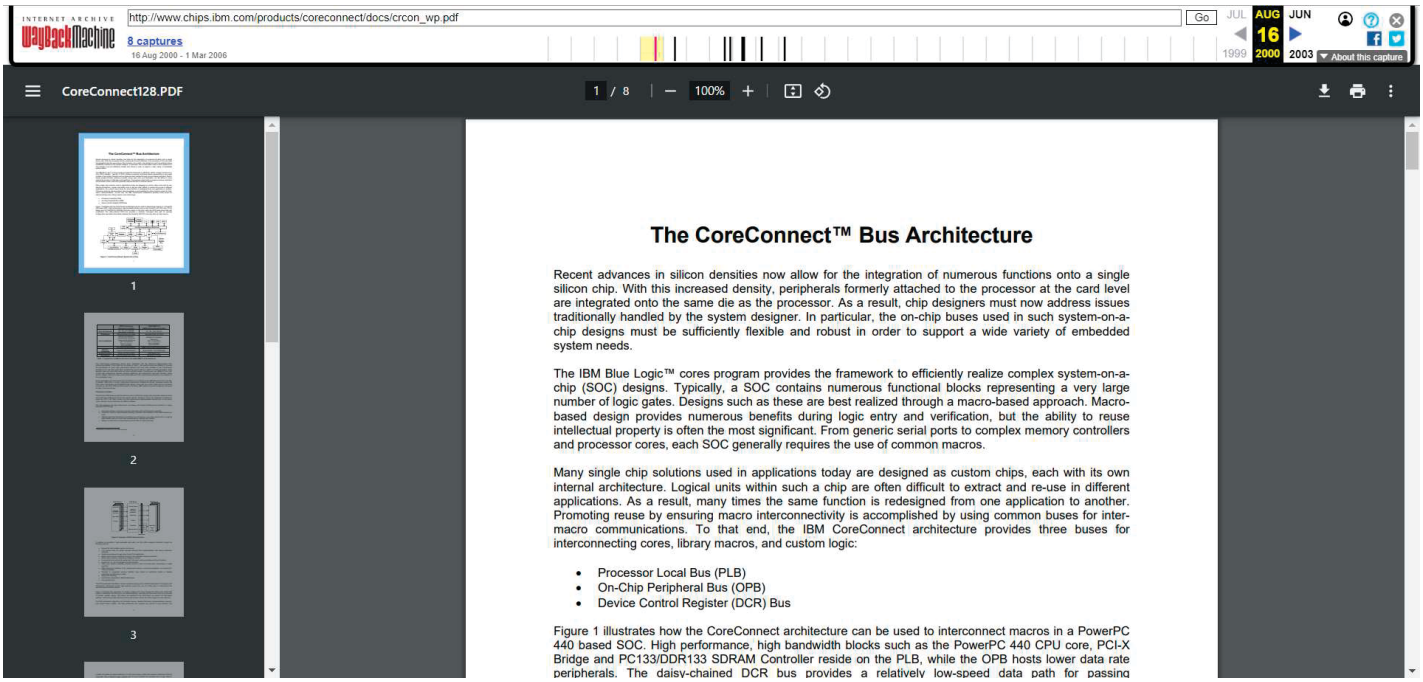
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The CoreConnect™ Bus Architecture

Recent advances in silicon densities now allow for the integration of numerous functions onto a single silicon chip. With this increased density, peripherals formerly attached to the processor at the card level are integrated onto the same die as the processor. As a result, chip designers must now address issues traditionally handled by the system designer. In particular, the on-chip buses used in such system-on-a-chip designs must be sufficiently flexible and robust in order to support a wide variety of embedded system needs.

The IBM Blue Logic™ cores program provides the framework to efficiently realize complex system-on-a-chip (SOC) designs. Typically, a SOC contains numerous functional blocks representing a very large number of logic gates. Designs such as these are best realized through a macro-based approach. Macro-based design provides numerous benefits during logic entry and verification, but the ability to reuse intellectual property is often the most significant. From generic serial ports to complex memory controllers and processor cores, each SOC generally requires the use of common macros.

Many single chip solutions used in applications today are designed as custom chips, each with its own internal architecture. Logical units within such a chip are often difficult to extract and re-use in different applications. As a result, many times the same function is redesigned from one application to another. Promoting reuse by ensuring macro interconnectivity is accomplished by using common buses for inter-macro communications. To that end, the IBM CoreConnect architecture provides three buses for interconnecting cores, library macros, and custom logic:

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register (DCR) Bus

Figure 1 illustrates how the CoreConnect architecture can be used to interconnect macros in a PowerPC 440 based SOC. High performance, high bandwidth blocks such as the PowerPC 440 CPU core, PCI-X Bridge and PC133/DDR133 SDRAM Controller reside on the PLB, while the OPB hosts lower data rate peripherals. The daisy-chained DCR bus provides a relatively low-speed data path for passing

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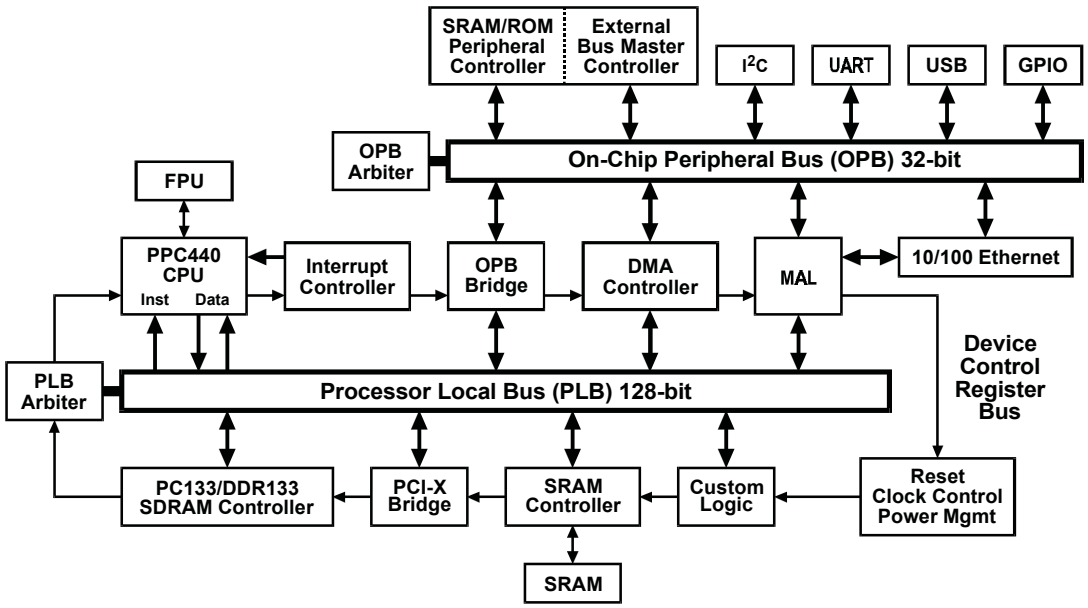


Figure 1: CoreConnect Based System-On-a-Chip.

	IBM CoreConnect Processor Local Bus	ARM AMBA 2.0 AMBA High-performance Bus
Bus Architecture	32-, 64-, and 128-bits Extendable to 256-bits	32-, 64-, and 128-bits
Data Buses	Separate Read and Write	Separate Read and Write
Key Capabilities	Multiple Bus Masters 4 Deep Read Pipelining 2 Deep Write Pipelining Split Transactions Burst Transfers Line Transfers	Multiple Bus Masters Pipelining Split Transactions Burst Transfers Line Transfers
	On-Chip Peripheral Bus	**AMBA Advanced Peripheral Bus**
Masters Supported	Supports Multiple Masters	Single Master: The APB Bridge
Bridge Function	Master on PLB or OPB	APB Master Only
Data Buses	Separate Read and Write	Separate or 3-state

Table 1: Comparison of IBM CoreConnect and ARM AMBA 2.0 Architectures.

The CoreConnect architecture shares many similarities with the Advanced Microcontroller Bus Architecture (AMBA™) from ARM Ltd. As shown in Table 1, the recently announced AMBA 2.0[1] includes the specification of many high performance features that have been available in the CoreConnect architecture for over three years. Both architectures support data bus widths of 32-bits and higher, utilize separate read and write data paths and allow multiple masters. CoreConnect and AMBA 2.0 now both provide high performance features including pipelining, split transactions and burst transfers. Many custom designs utilizing the high performance features of the CoreConnect architecture are available in the marketplace today.

Open specifications for the CoreConnect architecture are available on the IBM Microelectronics web site. In addition, IBM offers a no-fee, royalty-free CoreConnect architectural license. Licensees receive the PLB arbiter, OPB arbiter and PLB/OPB bridge designs along with bus model toolkits and bus functional compilers for the PLB, OPB and DCR buses. In the future, IBM intends to include compliance test suites for each of the three buses.

Processor Local Bus

The PLB and OPB buses provide the primary means of data flow among macro elements. Because these two buses have different structures and control signals, individual macros are designed to interface to either the PLB or the OPB. Usually the PLB interconnects high-bandwidth devices such as processor cores, external memory interfaces and DMA controllers.

The PLB addresses the high performance, low latency and design flexibility issues needed in a highly integrated SOC through:

- Decoupled address, read data, and write data buses with split transaction capability
- Concurrent read and write transfers yielding a maximum bus utilization of two data transfers per clock
- Address pipelining that reduces bus latency by overlapping a new write request with an ongoing write transfer and up to three read requests with an ongoing read transfer.
- Ability to overlap the bus request/grant protocol with an ongoing transfer

[1] ARM AMBA data obtained from the ARM web pages.

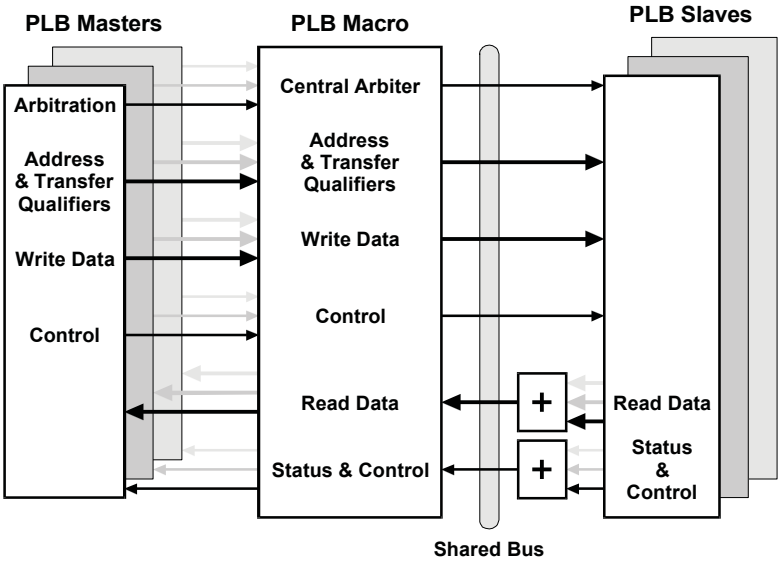


Figure 2: Example of PLB Interconnection.

In addition to providing a high bandwidth data path, the PLB offers designers flexibility through the following features:

- Support for both multiple masters and slaves
- Four priority levels for master requests allowing PLB implementations with various arbitration schemes
- Deadlock avoidance through slave forced PLB rearbitration
- Master driven atomic operations through a bus arbitration locking mechanism
- Byte-enable capability, supporting unaligned transfers
- A sequential burst protocol allowing byte, half-word, word and double-word burst transfers
- Support for 16-, 32- and 64-byte line data transfers
- Read word address capability, allowing slaves to return line data either sequentially or target word first
- DMA support for buffered, fly-by, peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfers
- Guarded or unguarded memory transfers allow slaves to individually enable or disable prefetching of instructions or data
- Slave error reporting
- Architecture extendable to 256-bit data buses
- Fully synchronous

The PLB specification describes a system architecture along with a detailed description of the signals and transactions. PLB-based custom logic systems require the use of a PLB macro to interconnect the various master and slave macros.

Figure 2 illustrates the connection of multiple masters and slaves through the PLB macro. Each PLB master is attached to the PLB macro via separate address, read data and write data buses and a plurality of transfer qualifier signals. PLB slaves are attached to the PLB macro via shared, but decoupled, address, read data and write data buses along with transfer control and status signals for each data bus.

The PLB architecture supports up to 16 master devices. Specific PLB macro implementations, however, may support fewer masters. The PLB architecture also supports any number of slave devices. The

number of masters and slaves attached to a PLB macro directly affects the maximum attainable PLB bus clock rate. This is because larger systems tend to have increased bus wireload and a longer delay in arbitrating among multiple masters and slaves.

The PLB macro consists of a bus arbitration control unit and the control logic required to manage the address and data flow through the PLB. The separate address and data buses from the masters allow simultaneous transfer requests. The PLB macro arbitrates among these requests and directs the address, data and control signals from the granted master to the slave bus. The slave response is then routed from the slave bus back to the appropriate master.

PLB Bus Transactions

PLB transactions consist of multiphase address and data tenures. Depending on the level of bus activity and capabilities of the PLB slaves, these tenures may be one or more PLB bus cycles in duration. In addition, address pipelining and separate read and write data buses yield increased bus throughput by way of concurrent tenures. Address tenures have three phases: request, transfer and address acknowledge. A PLB transaction begins when a master drives its address and transfer qualifier signals and requests ownership of the bus during the request phase of the address tenure. Once the PLB arbiter grants bus ownership the master's address and transfer qualifiers are presented to the slave devices during the transfer phase. The address cycle terminates when a slave latches the master's address and transfer qualifiers during the address acknowledge phase.

Figure 3 illustrates two deep read and write address pipelining along with concurrent read and write data tenures. Master A and Master B represent the state of each master's address and transfer qualifiers. The PLB arbitrates between these requests and passes the selected master's request to the PLB slave address bus. The trace labeled Address Phase shows the state of the PLB slave address bus during each PLB clock.

As shown in Figure 3, the PLB specification supports implementations where these three phases can require only a single PLB clock cycle. This occurs when the requesting master is immediately granted access to the slave bus and the slave acknowledges the address in the same cycle. If a master issues a request that cannot be immediately forwarded to the slave bus, the request phase lasts one or more cycles.

Each data beat in the data tenure has two phases: transfer and acknowledge. During the transfer phase the master drives the write data bus for a write transfer or samples the read data bus for a read transfer. As shown in Figure 3, the first (or only) data beat of a write transfer coincides with the address transfer

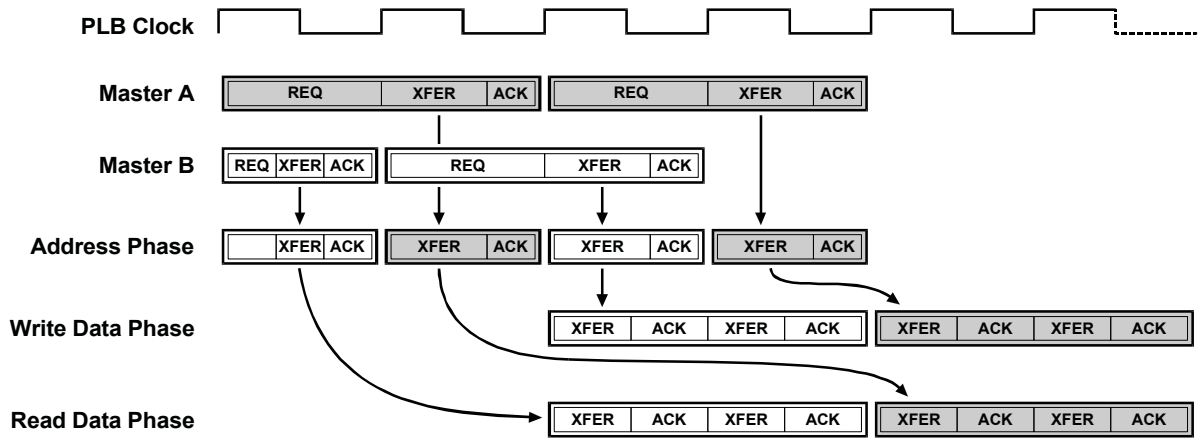


Figure 3: PLB Transfer Protocol Example.

phase. Data acknowledge cycles are required during the data acknowledge phase for each data beat in a data cycle. In the case of a single-beat transfer, the data acknowledge signals also indicate the end of the data transfer. For line or burst transfers, the data acknowledge signals apply to each individual beat and indicate the end of the data cycle only after the final beat. The highest data throughput occurs when data is transferred between master and slave in a single PLB clock cycle. In this case the data transfer and data acknowledge phases are coincident. During multi-cycle accesses there is a wait-state either before or between the data transfer and data acknowledge phases.

The PLB address, read data, and write data buses are decoupled from one another, allowing for address cycles to be overlapped with read or write data cycles, and for read data cycles to be overlapped with write data cycles. The PLB split bus transaction capability allows the address and data buses to have different masters at the same time. Additionally, a second master may request ownership of the PLB, via address pipelining, in parallel with the data cycle of another master's bus transfer. This is shown in Figure 3. Overlapped read and write data transfers and split-bus transactions allow the PLB to operate at a very high bandwidth by fully utilizing the read and write data buses.

Allowing PLB devices to move data using long burst transfers can further enhance bus throughput. However, to control the maximum latency in a particular application, master latency timers are required. All masters able to issue burst operations must contain a latency timer that increments at the PLB clock rate and a latency count register. The latency count register is an example of a configuration register that is accessed via the DCR bus. During a burst operation, the latency timer begins counting after an address acknowledge is received from a slave. When the latency timer exceeds the value programmed into the latency count register, the master can either immediately terminate its burst, continue until another master requests the bus or continue until another master requests the bus with a higher priority.

PLB Cross-Bar Switch

In some PLB-based systems multiple masters may cause the aggregate data bandwidth to exceed that which can be satisfied with a single PLB. With such a system it may be possible to place the high data rate masters and their target slaves on separate PLB buses. An example is a multiprocessor system using separate memory controllers. A macro known as the PLB Cross-Bar Switch (CBS) can be utilized to allow communication between masters on one PLB and slaves on the other. As shown in Figure 4, the CBS is placed between the PLB arbiters and their slave buses. When a master begins a transaction, the CBS uses the associated address to select the appropriate slave bus. The CBS supports simultaneous data transfers on both PLB buses along with a prioritization scheme to handle multiple requests to a common slave port. In addition, a high priority request can interrupt a lower priority transaction.

On-Chip Peripheral Bus

The On-Chip Peripheral Bus (OPB) is a secondary bus architected to alleviate system performance bottlenecks by reducing capacitive loading on the PLB. Peripherals suitable for attachment to the OPB include serial ports, parallel ports, UARTs, GPIO, timers and other low-bandwidth devices. As part of the

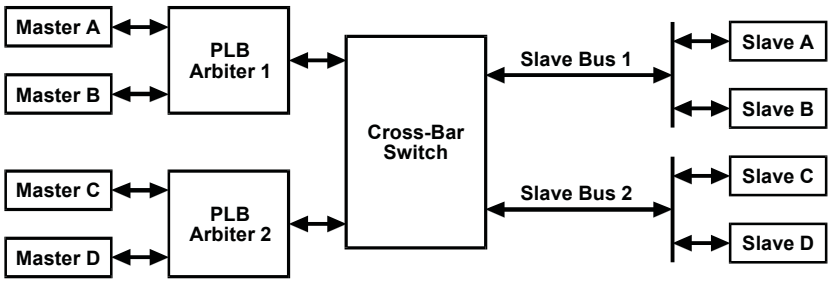


Figure 4: PLB Crossbar Switch.

IBM Blue Logic cores program, all OPB core peripherals directly attach to OPB. This common design point accelerates the design cycle time by allowing system designers to easily integrate complex peripherals into an ASIC.

The OPB provides the following features:

- A fully synchronous protocol with separate 32-bit address and data buses
- Dynamic bus sizing to support byte, half-word and word transfers
- Byte and half-word duplication for byte and half-word transfers
- A sequential address (burst) protocol
- Support for multiple OPB bus masters
- Bus parking for reduced-latency transfers

OPB Bridge

PLB masters gain access to the peripherals on the OPB bus through the OPB bridge macro. The OPB bridge acts as a slave device on the PLB and a master on the OPB. It supports word (32-bit), half-word (16-bit) and byte read and write transfers on the 32-bit OPB data bus, bursts and has the capability to perform target word first line read accesses. The OPB bridge performs dynamic bus sizing, allowing devices with different data widths to efficiently communicate. When the OPB bridge master performs an operation wider than the selected OPB slave the bridge splits the operation into two or more smaller transfers.

OPB Implementation

The OPB supports multiple masters and slaves by implementing the address and data buses as a distributed multiplexer. This type of structure is suitable for the less data intensive OPB bus and allows adding peripherals to a custom core logic design without changing the I/O on either the OPB arbiter or existing peripherals. Figure 5 shows one method of structuring the OPB address and data buses. Observe that both masters and slaves provide enable control signals for their outbound buses. By requiring that each macro provide this signal, the associated bus combining logic can be strategically

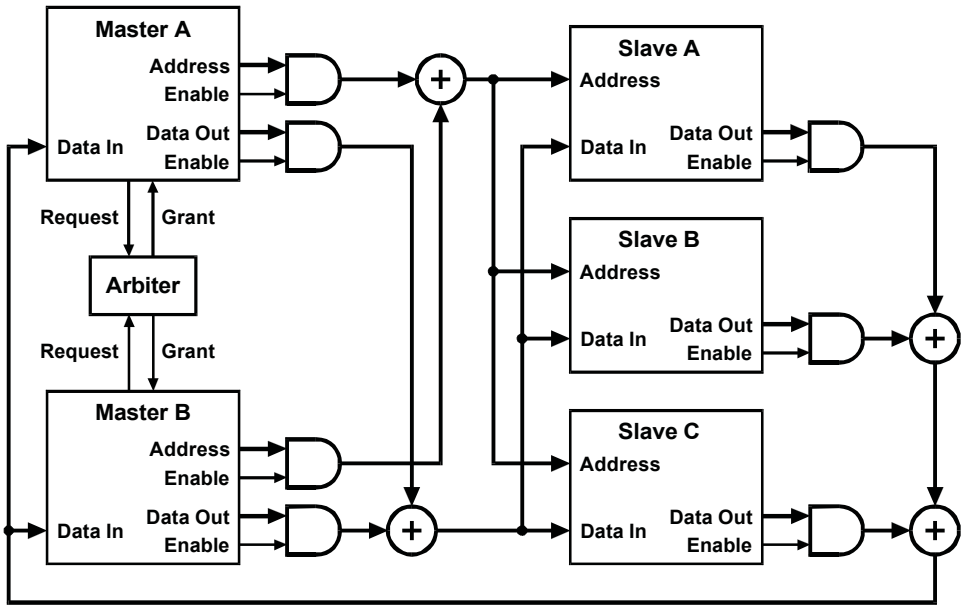


Figure 5: OPB Physical Implementation.

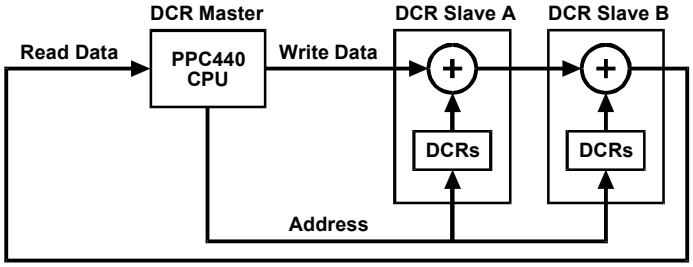


Figure 6: DCR Bus Structure.

placed throughout the chip. As shown in the figure, either of the masters is capable of providing an address to the slaves, whereas both masters and slaves are capable of driving and receiving the distributed data bus.

DCR Bus

Lower performance status and configuration registers are typically read and written through the Device Control Register (DCR) Bus. The DCR provides a maximum throughput of one read or write transfer every two cycles and is a fully synchronous bus typically implemented as a distributed multiplexer. Figure 6 illustrates the address and data flow between a processor core master and the DCR slaves. Observe that the relatively slow DCR bus utilizes a ring-type data bus. This provides the required connectivity while minimizing silicon usage.

Design Toolkits

Design toolkits are available for each of the on-chip buses. These toolkits contain master, slave and arbiter Bus Functional Models (BFM). Also provided is a Bus Functional Compiler used to translate testcases written in a bus functional language into simulator commands executable by the master and slave models.

These toolkits aid in unit and subsystem simulation of macros designed for attachment to any of the three on-chip buses. The toolkits are available in VHDL and Verilog such that they can be used in any simulation environment. The Bus Functional Language (BFL) command definition is unique for each bus and allows the user to execute and respond to all allowable transactions on the particular bus. BFL is processed by the bus functional compiler into command sequences executable by a BFM running on an event driven simulator such as VerilogXL, MTI or VSS.

Each bus toolkit provides a bus monitor that automatically performs architectural protocol checking on all masters and slaves attached to the bus. These checks verify that the masters and slaves under test adhere to the defined bus protocol and help to ensure compatibility when the macros are interconnected in a system environment. In addition to protocol checking, the master and slave models also perform read and write data checking. For example, when a master is programmed to perform a read transfer, the model checks the read data with the expected data as programmed in the BFL.

The toolkits also support concurrently executing multiple master models. A model intercommunication scheme is provided to allow transaction synchronization between the masters. One use of this feature is creating bus contention testcases often necessary to verify a macro.

Summary

The open standard CoreConnect bus provides the primary means of communication between macros in an IBM Blue Logic design. Designers realize several advantages in creating and using compliant macros. First, IBM is continually expanding its extensive library of Blue Logic off-the-shelf core macros. These logic blocks are easily integrated into a customer's SOC solution. Additionally, customers benefit by being able to reuse their own macros in multiple products. Finally, these common interfaces allow for easy integration, providing valuable time savings when implementing complex designs.

Design toolkits are available for the CoreConnect bus and include functional models, monitors, and a bus functional language to drive the models. These toolkits provide an excellent validation environment for engineers designing macros to attach to the PLB, OPB and DCR buses.

Further information on CoreConnect licensing, IBM Blue Logic, available cores, macros, and design toolkits is available on the WWW at:

http://www.chips.ibm.com/products/coreconnect

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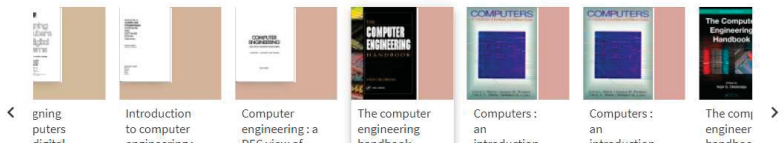
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Creator	Oklobdzija, Vojin G. >
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MESH subjects	Computers >
Contents	Fabrication and technology -- Computer systems and architecture -- Design techniques -- Design for low power -- Embedded applications -- Signal processing -- Communications and networks -- Input/output -- Operating system -- New directions in computing -- Testing and design for testability.
Related titles	Available in other form: Online version: Computer engineering handbook. Boca Raton : CRC Press, ©2002 >
Series	Electrical engineering handbook series >
	Electrical engineering handbook series. >
Publisher	Boca Raton : CRC Press
Creation Date	©2002
Format	1 volume (various pagings) : illustrations ; 26 cm.
Bibliography Note	Includes bibliographical references and index.
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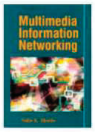
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