

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Hoberman et al.
U.S. Patent No.: 7,051,306 Attorney Docket No.: 44508-0023IP1
Issue Date: May 23, 2006
Appl. Serial No.: 10/840,893
Filing Date: May 7, 2004
Title: MANAGING POWER ON INTEGRATED CIRCUITS
 USING POWER ISLANDS

Mail Stop Patent Board

Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,051,306 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

TABLE OF CONTENTS

I.	REQUIREMENTS FOR IPR	1
	A. Grounds for Standing	1
	B. Challenge and Relief Requested.....	1
II.	THE '306 PATENT	2
	A. Brief Description	2
	B. Summary of the Prosecution History	4
	C. Level of Ordinary Skill in the Art	5
	D. Claim Construction.....	5
III.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	6
	A. GROUND 1A—Claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51 are obvious over Nowka	6
	1. Overview of Nowka	6
	2. Claim 1	9
	3. Claim 2	17
	4. Claim 3	18
	5. Claim 4	19
	6. Claim 5	20
	7. Claim 6	20
	8. Claim 7	20
	9. Claim 8	21
	10.Claim 10	21
	11.Claim 11	22
	12.Claim 12	22
	13.Claim 14	22
	14.Claim 15	23
	15.Claim 16	24
	16.Claim 17	26
	17.Claim 18	26
	18.Claim 19	26

19.Claim 20	27
20.Claim 21	27
21.Claim 22	27
22.Claim 23	27
23.Claim 25	27
24.Claim 26	27
25.Claim 27	27
26.Claim 29	27
27.Claim 30	27
28.Claim 31	27
29.Claim 32	29
30.Claim 33	30
31.Claim 34	30
32.Claim 36	31
33.Claim 37	31
34.Claim 38	33
35.Claim 39	33
36.Claim 40	34
37.Claim 41	34
38.Claim 42	34
39.Claim 43	34
40.Claim 44	34
41.Claim 46	34
42.Claim 47	34
43.Claim 48	34
44.Claim 50	34
45.Claim 51	34
B. GROUND 1B—Claims 9, 13, 24, 28, 45, and 49 are obvious over Nowka and Borkar	35
1. Overview of Borkar.....	35
2. Nowka-Borkar Combination.....	38

3. Claim 9	41
4. Claim 13	43
5. Claim 24	46
6. Claim 28	46
7. Claim 45	46
8. Claim 49	46
C. GROUND 1C—Claim 35 is obvious over Nowka and Boerstler.....	46
1. Overview of Boerstler	46
2. Nowka-Boerstler Combination	47
3. Claim 35	48
D. GROUNDS 2A—Claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47 are obvious over Nicol.....	50
1. Overview of Nicol	50
2. Claim 1	52
3. Claim 2	60
4. Claim 3	62
5. Claim 4	64
6. Claim 5	65
7. Claim 7	65
8. Claim 8	66
9. Claim 9	66
10.Claim 11	66
11.Claim 16	67
12.Claim 17	67
13.Claim 18	68
14.Claim 19	68
15.Claim 20	68
16.Claim 22	68
17.Claim 23	68
18.Claim 24	68
19.Claim 26	68

20.Claim 31	68
21.Claim 32	69
22.Claim 33	69
23.Claim 36	70
24.Claim 37	71
25.Claim 38	72
26.Claim 39	72
27.Claim 40	72
28.Claim 41	72
29.Claim 42	72
30.Claim 43	72
31.Claim 44	72
32.Claim 45	72
33.Claim 47	72
E. GROUND 2B—Claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51 are obvious over Nicol and Nowka.....	73
1. Overview of Nowka	73
2. Nicol-Nowka Combination	73
3. Claim 6	75
4. Claim 10	75
5. Claim 12	76
6. Claim 14	77
7. Claim 15	78
8. Claim 21	79
9. Claim 25	79
10.Claim 27	79
11.Claim 29	79
12.Claim 30	79
13.Claim 34	79
14.Claim 46	80
15.Claim 48	80

16.Claim 50	80
17.Claim 51	81
F. GROUND 2C—Claims 13, 28, and 49 are obvious over Nicol and Borkar	81
1. Overview of Borkar.....	81
2. Nicol-Borkar Combination.....	81
3. Claim 13	83
4. Claim 28	86
5. Claim 49	86
G. GROUND 2D—Claim 35 is obvious over Nicol and Naffziger.....	86
1. Overview of Naffziger.....	86
2. Nicol-Naffziger Combination	88
3. Claim 35	90
IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION....	92
A. Discretionary denial under §325(d) is not warranted.....	92
B. Discretionary Denial under Section 314(a) Is Not Warranted.....	93
C. The <i>Fintiv</i> Factors Weigh Against Exercising Discretion To Deny Institution.....	94
V. CONCLUSION.....	95
VI. PAYMENT OF FEES	95
VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1).....	95
A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)	95
B. Related Matters Under 37 C.F.R. § 42.8(b)(2).....	95
C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)	97
D. Service Information	97

LIST OF EXHIBITS

- MTK-1001 U.S. Patent No. 7,051,306 to Hoberman et al. (“the ’306 patent”)
- MTK-1002 Excerpts from the Prosecution History of the ’306 patent
- MTK-1003 Declaration of Tajana Rosing, Ph.D.
- MTK-1004 “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling” by Nowka, et al. (“Nowka”)
- MTK-1005 Declaration of June Ann Munford
- MTK-1006 U.S. Patent No. 6,484,265 to Borkar et al. (“Borkar”)
- MTK-1007 U.S. Patent No. 6,353,369 to Boerstler (“Boerstler”)
- MTK-1008 U.S. Patent No. 6,141,762 to Nicol, et al. (“Nicol”)
- MTK-1009 Complaint for Patent Infringement Against MediaTek, Inc. in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023)
- MTK-1010 Affidavit of Service On MediaTek USA, Inc. in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (March 30, 2023)
- MTK-1011 Claim Construction Order in *Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)
- MTK-1012 Claim Construction Order in *Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.*, Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)
- MTK-1013 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherine K. Vidal (USPTO June 21, 2022)

- MTK-1014 Stipulation
- MTK-1015 U.S. Patent No. 8,086,884 to Naffziger et al. (“Naffziger”)
- MTK-1016 “Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design” by Kuroda et al. (“Kuroda”)
- MTK-1017 “Dynamic Power Management: Design Techniques and CAD Tools” by Benini & De Micheli (“Dynamic Power Management”)
- MTK-1018 “A Survey of Design Techniques for System-Level Dynamic Power Management” by Benini, et al. (“Benini Survey”)
- MTK-1019 “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey, et al. (“Lackey”)
- MTK-1020 “Policy Optimization for Dynamic Power Management” by Benini et al., (“Benini Policy Optimization”)
- MTK-1021 “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”)
- MTK-1022 “Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems” by Dutta et al. (“Dutta”)
- MTK-1023 “The CoreConnect™ Bus Architecture” by IBM (“CoreConnect White Paper”)
- MTK-1024 “The Computer Engineering Handbook” edited by Oklobdzija (“Computer Engineering Handbook”), excerpts
- MTK-1025 “Computer Systems: Concepts and Design” by Gibson (“Gibson”), excerpts
- MTK-1026 Multimedia Information Networking” by Sharda (“Sharda”), excerpts

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:
1[a]	determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;
1[b]	determining at least one of actions to change a power consumption level of the one of the power islands to the target power level; and
1[c]	performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.
Claim 2	
2	The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit
Claim 3	
3	The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 4	
4	The method of claim 1 wherein the power islands comprise power sub-islands.
Claim 5	
5	The method of claim 1 wherein the power islands comprises multiple clock domains.
Claim 6	
6	The method of claim 1 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 7	
7	The method of claim 1 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

Claim 8	
8	The method of claim 7 wherein the first voltage comprises a source voltage.
Claim 9	
9	The method of claim 7 wherein the first voltage comprises a threshold voltage.
Claim 10	
10	The method of claim 1 wherein another one of the actions comprises powering on the one of the power islands.
Claim 11	
11	The method of claim 1 wherein another one of the actions comprises powering off the one of the power islands.
Claim 12	
12	The method of claim 1 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 13	
13	The method of claim 1 further comprising: monitoring the power consumption level of the one of the power islands; determining whether a threshold level was crossed based on the power consumption level; and performing another one of the actions based on the crossing of the threshold level.
Claim 14	
14	The method of claim 1 further comprising saving a state of components within the one of the power islands.
Claim 15	
15	The method of claim 1 further comprising restoring a state of components within the one of the power islands.

Claim 16	
16[p]	A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:
16[a]	power control circuitry configured to control power for one of the power islands; and
16[b]	a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.
Claim 17	
17	The system of claim 16 wherein the power islands are delineated based on geographic factors of the integrated circuit.
Claim 18	
18	The system of claim 16 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 19	
19	The system of claim 16 wherein the power islands comprise power sub-islands.
Claim 20	
20	The system of claim 16 wherein the power islands comprise multiple clock domains.
Claim 21	
21	The system of claim 16 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 22	
22	The system of claim 16 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

Claim 23	
23	The system of claim 22 wherein the first voltage comprises a source voltage.
Claim 24	
24	The system of claim 22 wherein the first voltage comprises a threshold voltage.
Claim 25	
25	The system of claim 16 wherein another one of the actions comprises powering on the one of the power islands.
Claim 26	
26	The system of claim 16 wherein another one of the actions comprises powering off the one of the power islands.
Claim 27	
27	The system of claim 16 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 28	
28	The system of claim 16 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.
Claim 29	
29	The system of claim 16 wherein the power manager is configured to save a state of components within the one of the power islands.
Claim 30	
30	The system of claim 16 wherein the power manager is configured to restore a state of components within the one of the power islands.
Claim 31	
31	The system of claim 16 further comprising a bus coupled to the power manager and the power islands.

Claim 32	
32	The system of claim 16 wherein the power manager comprises a master manager configured to control power of the integrated circuit.
Claim 33	
33	The system of claim 16 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.
Claim 34	
34	The system of claim 16 wherein the power control circuitry includes clock multiplexing circuitry.
Claim 35	
35	The system of claim 16 wherein the power control circuitry includes voltage multiplexing circuitry.
Claim 36	
36	The system of claim 16 wherein the power control circuitry includes level shifting circuitry.
Claim 37	
37[p]	A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:
37[a]	power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands; and
37[b]	a software storage medium operational to store the power management software.

Claim 38	
38	The software product of claim 37 wherein the power islands are delineated based on geographic factors of the integrated circuit.
Claim 39	
39	The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 40	
40	The software product of claim 37 wherein the power islands comprise power sub-islands.
Claim 41	
41	The software product of claim 37 wherein the power islands comprise multiple clock domains.
Claim 42	
42	The software product of claim 37 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 43	
43	The software product of claim 37 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.
Claim 44	
44	The software product of claim 43 wherein the first voltage comprises a source voltage.
Claim 45	
45	The software product of claim 43 wherein the first voltage comprises a threshold voltage.
Claim 46	
46	The software product of claim 37 wherein another one of the actions comprises powering on the one of the power islands.
Claim 47	
47	The software product of claim 37 wherein another one of the actions comprises powering off the one of the power islands.

Claim 48	
48	The software product of claim 37 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 49	
49	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.
Claim 50	
50	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.
Claim 51	
51	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.

MediaTek, Inc. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-51 (“Challenged Claims”) of U.S. Patent No. 7,051,306 (“the ’306 patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’306 patent is available for IPR. Petitioner is not barred or estopped from requesting this review of the Challenged Claims. The present Petition is filed within one year of service of a complaint against Petitioner in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023). MTK-1010.

B. Challenge and Relief Requested

Petitioner requests IPR and cancellation of the Challenged Claims on the grounds below. Dr. Tajana Rosing provides complementary explanations in her Declaration (MTK-1003) cited throughout this petition.

Ground	Claims	Basis	References
1A	1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51	§103	Nowka
1B	9, 13, 24, 28, 45, 49	§103	Nowka and Borkar
1C	35	§103	Nowka and Boerstler
2A	1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47	§103	Nicol
2B	6, 10, 12, 14-15, 21, 25,	§103	Nicol and Nowka

Ground	Claims	Basis	References
	27, 29-30, 34, 46, 48, 50-51		
2C	13, 28, 49	§103	Nicol and Borkar
2D	35	§103	Nicol and Naffziger

Each reference pre-dates the '306 patent's earliest possible priority date (May 7, 2003; "Critical Date") and qualifies as prior art.¹

Reference	Date	Prior Art Under
Nowka	11/2002 (published)	§102(a)
Nicol	10/31/2000 (published)	§102(b)
Borkar	11/2002 (published)	§102(e)
Boerstler	03/05/2002 (published)	§102(b)
Naffziger	12/16/2002 (filed)	§102(e)

II. THE '306 PATENT

A. Brief Description

The '306 patent relates to managing power on an integrated circuit ("IC") using power islands. MTK-1001, Abstract, 2:21-24. The '306 patent explains that reducing power consumption in integrated circuits is a design goal increasing in importance as ICs become more complex and power consuming. MTK-1001, 1:19-26, 2:1-9. One alleged problem in the existing art, according to the '306 patent, is "that power consumption is not efficiently utilized." MTK-1001, 1:58-

¹ Petitioner does not concede that the '306 patent is entitled to the Critical Date.

59. “For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency.” MTK-1001, 1:59-63.

The ’306 patent explains that while “[s]ome prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption.... [T]he voltages in the power island and the frequencies of the multiple clocks are static. The voltages and frequencies do not dynamically change based on the needs and operation of the integrated circuit.” MTK-1001, 2:10-16.

The ’306 patent proposes a method and apparatus for allegedly managing the power consumption of an integrated circuit (“IC”) using power islands whose power consumption is independently controlled. MTK-1001, Abstract, 2:21-24. A power island is “any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:51-54.

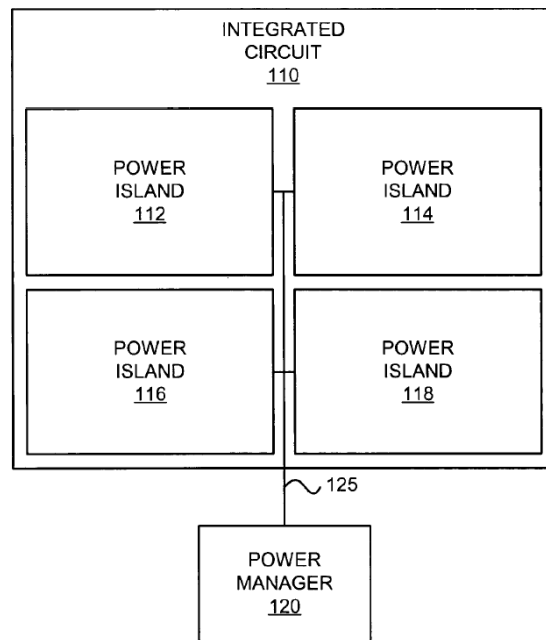


FIG. 1
MTK-1001, Fig. 1.

The system has a “power manager” that determines a target power level for one of the power islands and then determines an action to change the power consumption for one of the islands to the target power level. MTK-1001, Abstract, 2:24-30. The action to change the power consumption can be selecting a clock frequency or modifying a voltage for one of the power islands, among other actions. MTK-1001, 2:32-38, 4:45-55, 5:34-36.

B. Summary of the Prosecution History

U.S. Application 10/840,893, which resulted in the '306 patent, was filed May 7, 2004. The '306 patent claims priority to provisional application 60/468,742, filed May 7, 2003. MTK-1002, 174. The Patent Office issued one non-final rejection and one final rejection during prosecution. MTK-1002, 127-

135 (Feb. 24, 2005 Non-Final Rejection), 73-83 (Aug. 3, 2005 Final Rejection).

The Office never considered Nowka, Nicol, Borkar, Naffziger, or Boerstler. These references render the challenged claims obvious, as discussed below.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. MTK-1003, ¶21.

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for purposes of addressing the Grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Petitioner notes for the Board that there have been prior litigations involving the ’306 Patent, two of which had a claim construction order before voluntary dismissal, attached as MTK-1011 and MTK-1012. Petitioner submits that the Board does not need to address any of the prior

constructions to resolve the patentability disputes before the PTAB, and that none of the constructions impact the invalidity analysis in this Petition.

Petitioner reserves the right to respond to any constructions offered/adopted by Patent Owner/Board. Furthermore, Petitioner does not concede that each challenged claim satisfies all statutory requirements and does not waive any arguments concerning grounds that can only be raised in district court.

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A—Claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51 are obvious over Nowka

1. Overview of Nowka

Nowka describes a system-on-a-chip (“SOC”) that is capable of dynamic voltage and frequency scaling “to adapt to the dynamically changing performance demands and power consumption constraints” of the system. MTK-1004, Abstract; MTK-1003, ¶46. Nowka’s SOC consists of a high performance 32-bit processor core, also referred to as the “CPU core,” an integrated LCD display controller, I/O interfaces, a dedicated speech accelerator, an instruction decompression engine, a DES accelerator core, a low-voltage phase-locked-loop (PLL) core, a real-time-clock core, a clock power-management core, and a sleep-management core. MTK-1004, 1442. Some of these components are shown in the structural diagram in Figure 1 and die photograph in Figure 2.

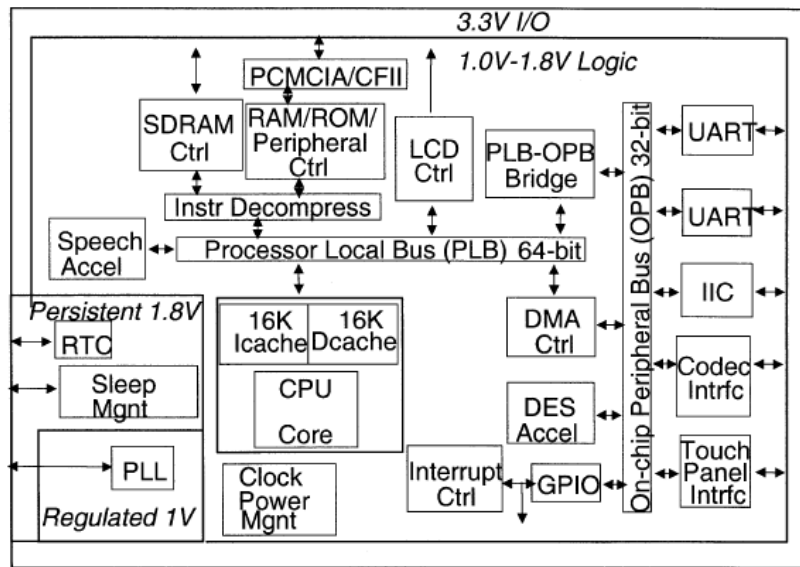
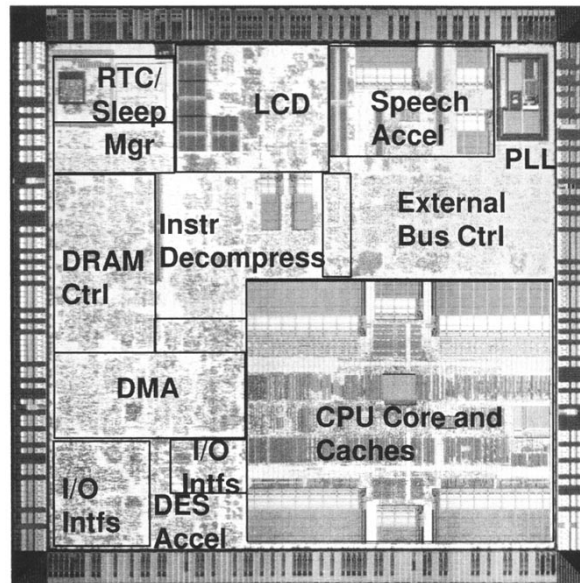


Fig. 1. PowerPC SOC structure.

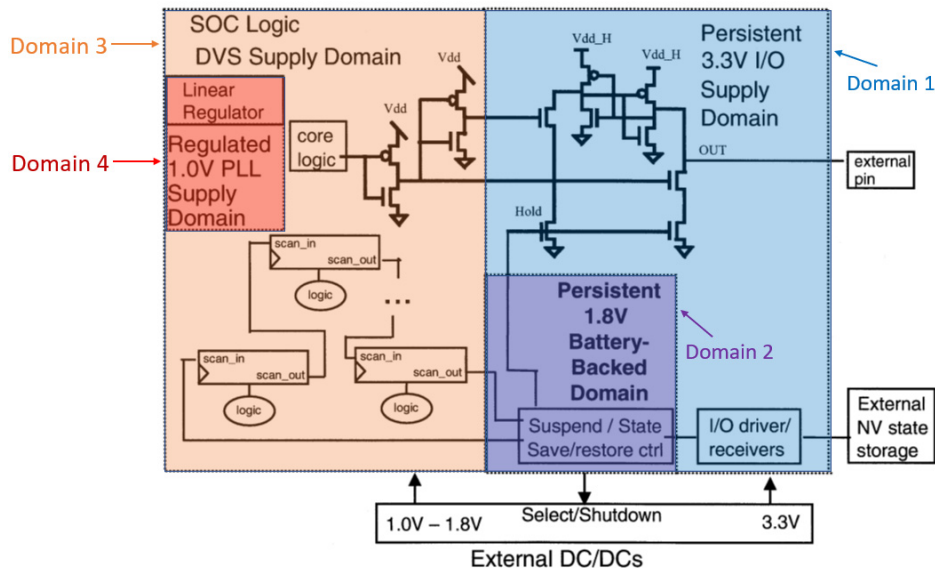
MTK-1004, Fig. 1.



MTK-1004, Fig. 2.

Nowka's SOC is divided into four power domains to enable dynamic voltage and frequency scaling. These domains—two persistent voltage domains, one

dynamically voltage-scaled and frequency-scaled logic domain, and one internally derived domain—are shown in annotated Figure 3 below. The I/O drivers and receivers are in the persistent 3.3V domain (domain 1 below); the real-time clock and the logic controlling the voltage of the cores is in the persistent 1.8V domain (domain 2 below); the logic supply for the processor core, caches, SOC cores and accelerators in the 1-1.8V variable domain (domain 3 below); and the PLL is in the constant 1V domain (domain 4 below). MTK-1004, 1444; MTK-1003, ¶48. The operating frequency of the variable voltage domain (domain 3) can also be altered for additional active power reduction. MTK-1004, 1444 (“When the performance demands of the application decrease, the system software can lower the operating frequency.”); MTK-1003, ¶¶48-49.



MTK-1004, Fig. 3²

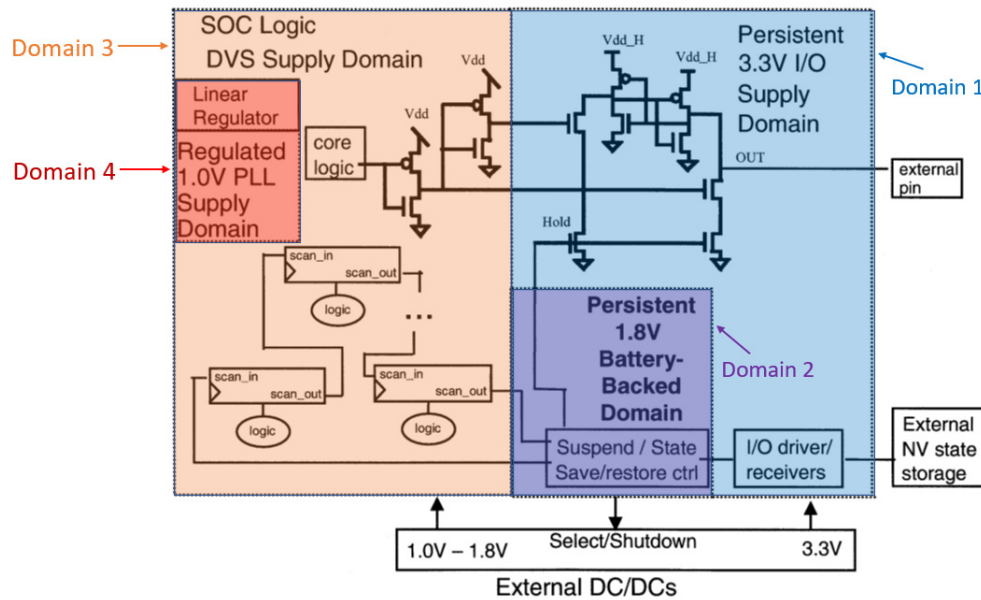
2. Claim 1

(a) 1[p]

To the extent the preamble is limiting,³ Nowka discloses a method of managing power on an IC including a plurality of power islands. Nowka explains that its SOC design is “optimized for energy efficiency” by controlling voltage and frequency. MTK-1004, 1446; MTK-1003, ¶50. Nowka discloses multiple power domains on the IC, namely the four domains supplied different voltages, depicted in Figure 3. MTK-1004, 1444. A POSITA would have understood and found obvious that the four domains are power islands as defined by the ’306 Patent because each domain is a “section, delineation, partition, or division” on the SOC where “power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:51-54; MTK-1003, ¶51.

² All annotations to the figures have been added unless otherwise noted herein.

³ Petitioner reserves the right to argue in counterpart litigation that the preamble is not limiting.



MTK-1004, Fig. 3.

(b) 1[a]

Nowka discloses and renders obvious determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands. Nowka discloses that its SOC allows for “performance demands of the application to be met” (needs and operation of the integrated circuit) while “minimizing the dynamic power consumption” (determining a target power level). MTK-1004, 1446; MTK-1003, ¶52. Nowka discloses a number of actions to reduce the power level “when resource demands are low” (needs and operation of the integrated circuit) such as “dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating,” and standby modes. MTK-1004, 1442, 1446; MTK-1003, ¶¶53-60.

For example, in Section III.C, Nowka discusses the power results of voltage scaling while running Dhrystone2.1 benchmark (Figure 5) and MPEG-4 decoding on the SOC (Figure 6). MTK-1004, 1444. Both examples demonstrate that the target power level of a power island (target supply voltage of logic domain) is shifted in response to needs and operation of the integrated circuit (varying requirements of the application being run, or different requirements from different applications). MTK-1003, ¶54.

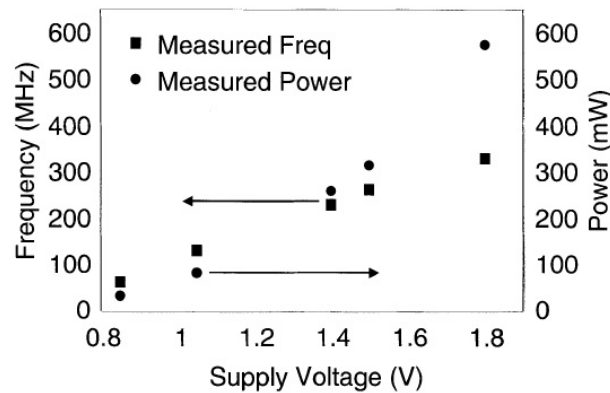


Fig. 5. Dhrystone2.1 voltage scaling measurements.

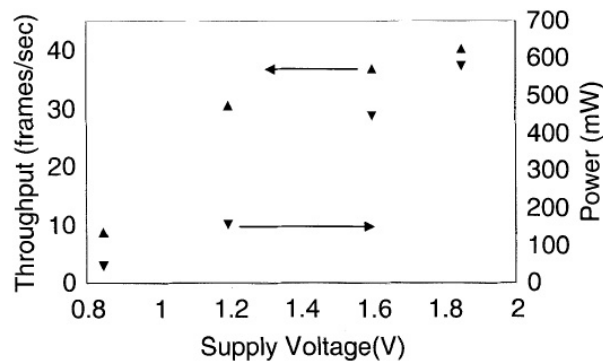


Fig. 6. MPEG-4 decode voltage scaling measurements.

MTK-1004, Figs. 5, 6.

As another example, Figure 8 shows the corresponding decrease and increase and power consumption in response to frequency and voltage changes, which a POSITA would have understood to be executed “in anticipation of [] performance demands” (needs and operation of the integrated circuit). MTK-1004, 1444, Fig. 8; MTK-1003, ¶55.

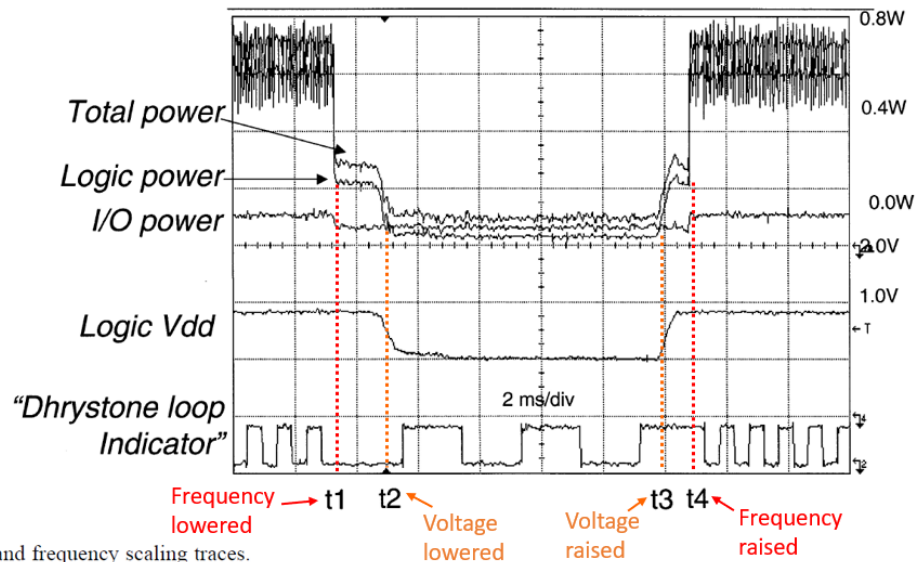


Fig. 8. Dynamic voltage and frequency scaling traces.

MTK-1004, Fig. 8.

Additionally, Nowka discloses clock gating inactive registers and cores, as well as putting the system in various standby modes, which changes the power state of the logic domain, when certain registers and units, or the entire logic domain, does not need to be active. MTK-1004, 1445-46; MTK-1003, ¶¶59-60.

A POSITA would have found it obvious that each of these actions involves determining a target power level because these actions were well-understood in the art as mechanisms for adjusting power level. MTK-1003, ¶¶56-60. For instance, Nowka's disclosure regarding determining a target power level mirrors the approach of the '306 patent, which describes setting the target for certain *parameters* such as frequency or voltage as the example of "determining a target power level." MTK-1001, 7:38-50, Fig. 5; MTK-1003, ¶¶57-58, 61. To the extent that Nowka doesn't disclose determining a target power level based on needs and

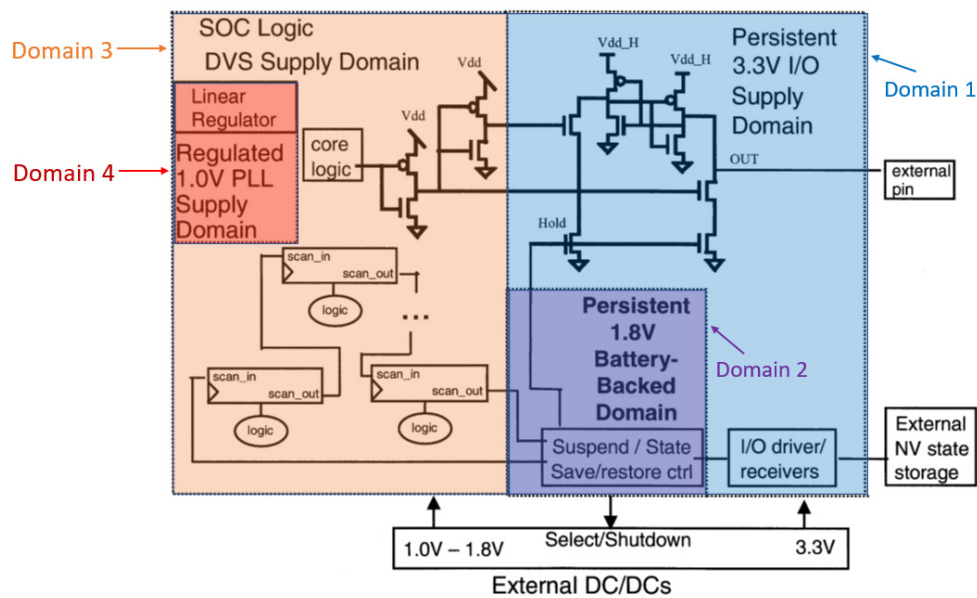
operation of the integrated circuit, it would have been obvious to a POSITA that the system was making such a determination. MTK-1003, ¶¶56-61.

On “based on needs and operation of the integrated circuit,” Petitioner notes that in prior litigations involving the ’306 patent, the parties in those litigations agreed to a construction of “based on future operational needs and current operating status of the integrated circuit.” MTK-1011, 48, MTK-1012, 9. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶62. The ’306 Patent does not provide further explanation of this phrase, nor a particular balancing of “needs” and “operation” that is required. Rather, it provides examples of determining parameters such as required frequency, supply voltage, or threshold voltage, given a particular application. MTK-1001, 7:38-50, 8:56-62 (discussing setting a “required frequency” for an IP unit in response to an application request). As explained above, Nowka’s disclosures mirror the approach of the ’306 Patent. MTK-1003, ¶¶61-62.

Additionally, while there is no briefing regarding the prior-agreed upon construction in *Freescale* (MTK-1011) and *Conversant* (MTK-1012), Petitioner submits that Nowka’s disclosure, in light of a POSITA’s knowledge, also satisfies this construction. For example, Nowka’s discussion that it changes frequency and voltage “*in anticipation* of lower performance demands” shows that its power

management is responsive to future operational needs, while its disclosure that “anticipating an increase in demand, the logic supply is raised to 1.8 V *without interrupting execution*” shows that it is also responsive to the current operational status of the integrated circuit. MTK-1004, 1444; MTK-1003, ¶63.

Further, Nowka discloses that power consumption is independently controlled within each of the power islands. Nowka’s power domains receive distinct power supplies, which can be controlled independently (for example, the logic domain can receive variable supply while the persistent domains 1 and 2 do not change in power). MTK-1004, 1442; MTK-1003, ¶64.



MTK-1004, Fig. 3.

(c) 1[b]

Nowka discloses determining an action to change the power consumption

level of one of the power islands to the target power level. As discussed for element 1[a], Nowka discloses a number of actions such as changing frequency, changing voltage, clock gating, and standby modes, to change the power consumption level of the logic domain to a target power level. MTK-1003, ¶¶65-68. It would have been obvious to a POSITA, in light of Nowka's disclosure of various actions, that Nowka's system makes a determination on which action to take. MTK-1004, 1442 ("[T]he supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation."), 1446 ("The on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to the control the standby power."); MTK-1003, ¶69.

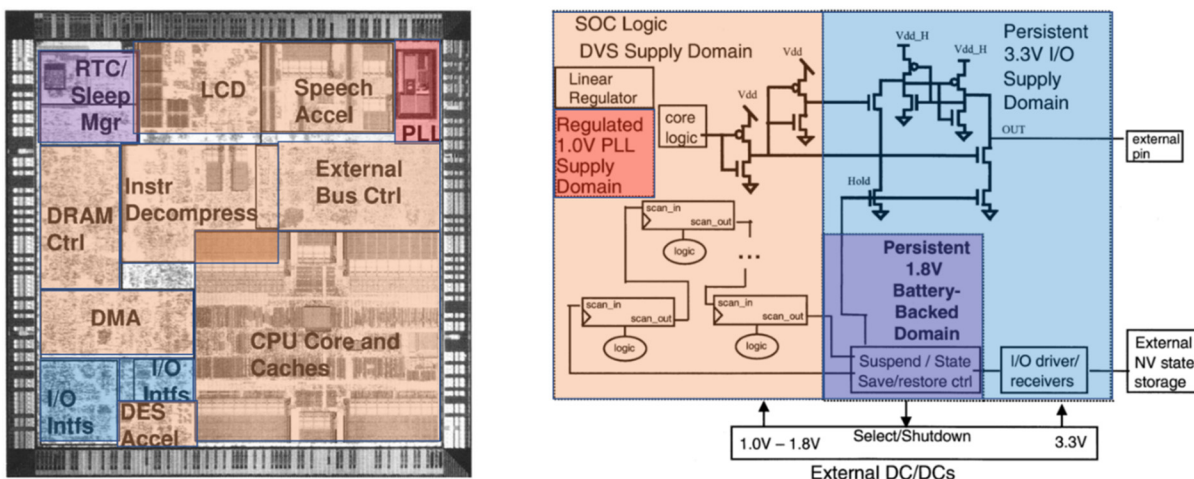
(d) 1[c]

Nowka discloses performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands. As discussed for 1[b], Nowka discloses performing an action such as changing frequency, changing voltage, clock gating, or standby mode to change the power consumption level of the logic domain to the target power level. MTK-1004, 1444 Section III.C (voltage scaling), 1444 Section V (frequency and voltage scaling), 1445 (clock gating), 1446 (standby modes); MTK-1003, ¶70. As

changing a frequency level is “selecting a frequency” for the logic domain, Nowka satisfies this element.

3. Claim 2

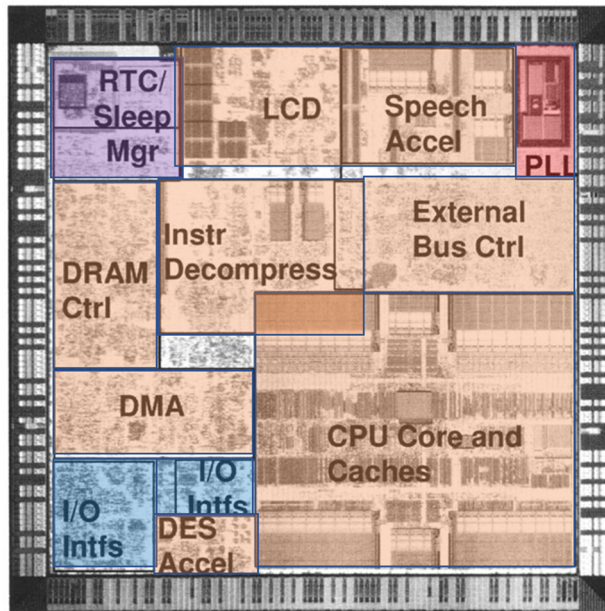
Nowka discloses and renders obvious that the power islands are delineated based on geographic factors of the integrated circuit. Annotated Figures 2 and 3 below show that the components in Nowka’s four power domains are located near other components in the same power domain. MTK-1004, Figs. 2-3; MTK-1003, ¶¶71. To the extent that Nowka does not explicitly disclose this claim, a POSITA would have understood and found it obvious from Nowka’s disclosure and basic circuit design principles that power islands would be delineated based on geographic factors (e.g., physical proximity) to minimize signal deterioration and power dissipation, for better routing of power supply and signals, and optimization of performance and power. MTK-1003, ¶¶72.



MTK-1004, Figs. 2, 3.

4. Claim 3

Nowka discloses and renders obvious that the power islands are delineated based on functional circuitry of the integrated circuit. As shown in the annotated Figure 2, Nowka's power domains are defined by the functional circuitry of the constituent components. MTK-1003, ¶73. For example, the I/O drivers and receivers are in the persistent 3.3V supply domain because of their function, which is to interface between the SoC and external components. MTK-1004, 1442. Additionally, components that dynamically respond to program needs are grouped together in the variable-supply logic domain. MTK-1004, 1442. "The real-time clock and the logic associated with controlling the voltage of the cores" receives a persistent 1.8-V supply because these functional circuits need to retain power even when other parts of the SOC are off. MTK-1004, 1442. The PLL, which generates the clock signal to control operation of the SoC, receives an internally derived voltage supply which allows it to maintain a constant, well-regulated voltage. MTK-1004, 1442. To the extent that Nowka does not explicitly disclose this claim, a POSITA would have found this limitation obvious from these disclosures because as explained, different functional circuitry requires different power characteristics. MTK-1003, ¶73.



MTK-1004, Fig. 2.

5. Claim 4

Nowka discloses that the power islands comprise power sub-islands. Nowka discloses that “active power of the SOC can be further reduced through modification of the clock frequency within the individual cores.” MTK-1004, 1445. A POSITA would have understood and found obvious that the individual cores are power sub-islands in which power is independently controlled. MTK-1003, ¶74. Nowka also discloses that “[d]ynamic power is saved in this design by gating off inactive latches and units. Approximately 80% of the processor registers and 50% of the SOC core registers are functionally clock gated when they are not accessed.” MTK-1004, 1445. A POSITA would have understood and found obvious from this disclosure that the latches, registers, and units are also power

sub-islands. MTK-1004, 1445; MTK-1003, ¶75.

6. Claim 5

Nowka discloses that the power islands comprise multiple clock domains. The individual cores in the logic domain “receive clocks whose frequency is derived from the processor clock through clock dividers. The clock dividers are controlled by register values. The hazard-free clock dividers *allow the clocks to the cores to be modified dynamically and individually.*” MTK-104, 1445. A POSITA would therefore have understood and found obvious that the individual cores are multiple clock domains within a power island. MTK-1003, ¶76.

7. Claim 6

Nowka discloses selecting a clock for one of the power islands. Nowka discloses that a different clock can be selected “when the performance demands of the application decrease:” “[t]he output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock as the processor clock source to allow for extremely low frequency operation.” MTK-1004, 1444; MTK-1003, ¶77.

8. Claim 7

Nowka discloses modifying a first voltage for one of the power islands. The Nowka system employs “dynamic voltage scaling (DVS)” as a means to match “the performance and power consumption of this device to the application...DVS systems adjust the supply voltage dynamically to meet the performance demands

while minimizing power consumption.” MTK-1004, 1442; MTK-1003, ¶78. As discussed above, the supply voltage for the logic domain “can be varied between 1 and 1.8V.” MTK-1004, 1442; MTK-1003, ¶¶78-80.

9. Claim 8

Nowka discloses and renders obvious that the first voltage comprises a source voltage. Nowka discloses “[p]rocessor energy efficiency can be improved by scaling the supply voltage. DVS systems adjust the supply voltage dynamically to meet the performance demands while minimizing power consumption.” MTK-1004, 1442; MTK-1003, ¶81. The ’306 patent describes a “dynamic voltage source” labeled Vdd, that can be modified for one of the power islands. MTK-1001, 4:51-53. A POSITA would have understood that a supply voltage and source voltage are the same because they both provide the voltage required to operate the power island. MTK-1003, ¶81.

10. Claim 10

Nowka discloses that one of the actions of claim 1 comprises powering on one of the power islands. Nowka discloses “hibernation” and “cryo” modes where “the logic supply to the processor, caches and the SOC core is disconnected.” MTK-1004, 1446. When exiting hibernation or cryo mode, the SOC “restores the [logic] supply” to power on the power island and restore functionality. MTK-1004, 1446; MTK-1003, ¶82. Accordingly, a POSITA would have understood that

process of coming out of Hibernation or Cryo mode is powering on the power island for normal operation of the system. MTK-1003, ¶82.

11. Claim 11

Nowka discloses that one of the actions of claim 1 comprises powering off one of the power islands. Nowka discloses “hibernation mode” and “cryo mode” where “the logic supply to the processor, caches and the SOC core is disconnected.” MTK-1004, 1446; MTK-1003, ¶83. A POSITA would have understood that disconnecting the supply voltage to the logic domain is powering off the power island because the voltage to the power island is removed, turning the power island off. MTK-1003, ¶83.

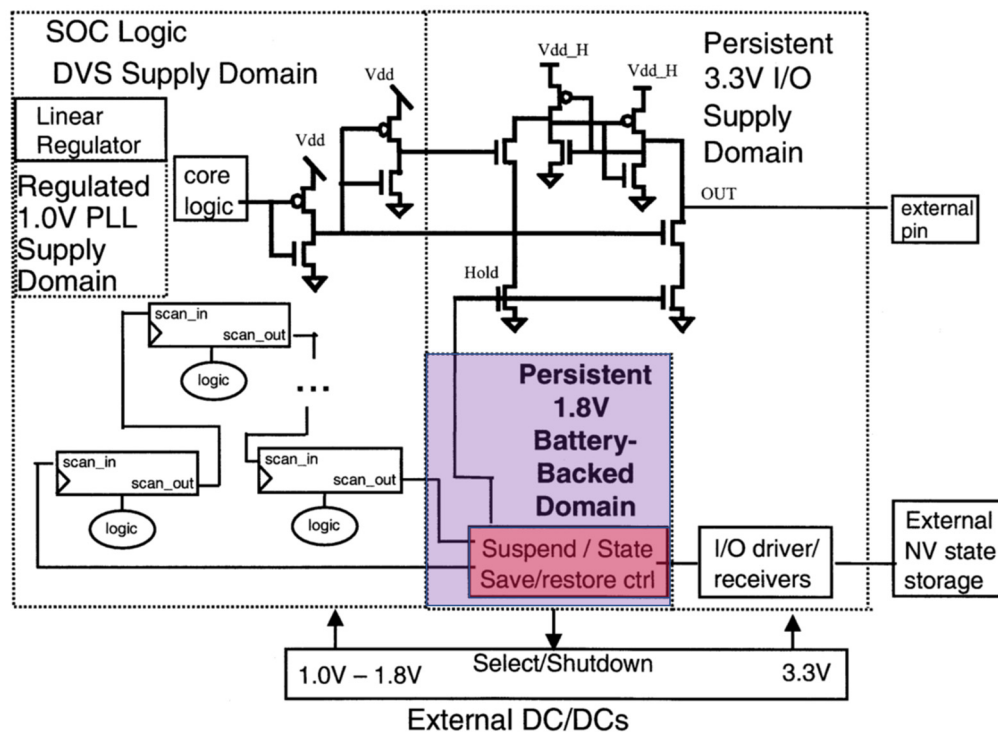
12. Claim 12

Nowka discloses that one of the actions comprises changing a power island to a sleep mode. Nowka discloses “sleep and hibernation modes” to “minimize standby power consumption,” similar to the ’306 patent’s disclosure of “low power modes such as sleep, nap, and full power down.” MTK-1004, 1442, 1446; MTK-1001, 7:26-27; MTK-1003, ¶84. Nowka discloses “low power modes” such as hibernate and cryo modes, in which the logic supply voltage, is disconnected to reduce standby power consumption. MTK-1004, 1446; MTK-1003, ¶84.

13. Claim 14

Nowka discloses saving a state of components within one of the power

islands. Nowka discloses that in “Cryo mode,” “the state of latches and register arrays in the processor core and SOC cores *is transferred to nonvolatile storage* prior to disconnecting the logic supply.” MTK-1004, 1446; MTK-1003, ¶85. Therefore, Nowka discloses saving the state of the latches and register arrays, which are components in the logic domain. MTK-1003, ¶85. Figure 3 shows a block labeled “Save/restore ctrl” (highlighted in red) within the variable voltage power domain, which a POSITA would have understood to facilitate the saving a state of components. MTK-1003, ¶85.



MTK-1004, Fig. 3.

14. Claim 15

Nowka discloses restoring a state of components within one of the power

islands. After entering “Cryo mode,” the suspend controller “waits for a wakeup event at which time it restores the supply, *restores the state* and restart the clocks” for components in the variable voltage power domain. MTK-1004, 1446; MTK-1003, ¶86.

15. Claim 16

(a) 16[p]

Supra Ground 1A, element 1[p]. MTK-1003, ¶87. Nowka further discloses a “system for an integrated circuit” because it is a system-on-a-chip, which a POSITA would have recognized as a “system for an integrated circuit.” MTK-1004, 1441, 1446, Figs. 1-2; MTK-1003, ¶88.

(b) 16[a]

Nowka discloses power control circuitry configured to control power for one of the PEs. The DC/DC converter controls the supply voltage of the logic domain, and the PLL controls the clock frequency of the logic domain. MTK-1004, Abstract, 1442-1444, Figs. 1, 3, 7; MTK-1003, ¶89.

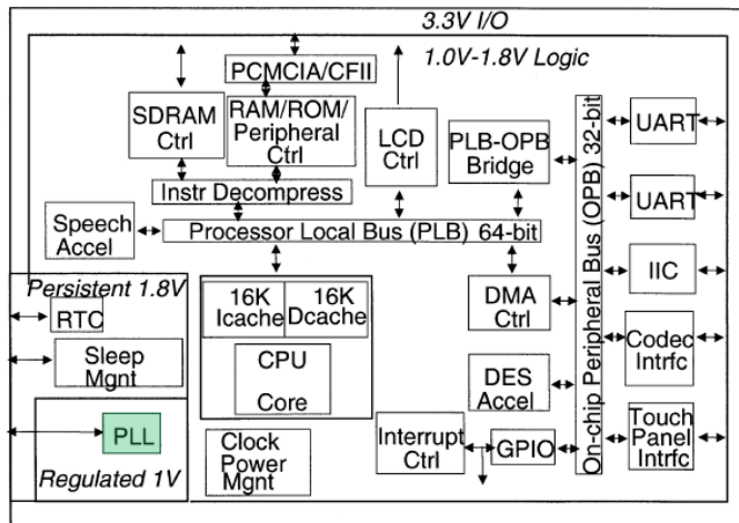
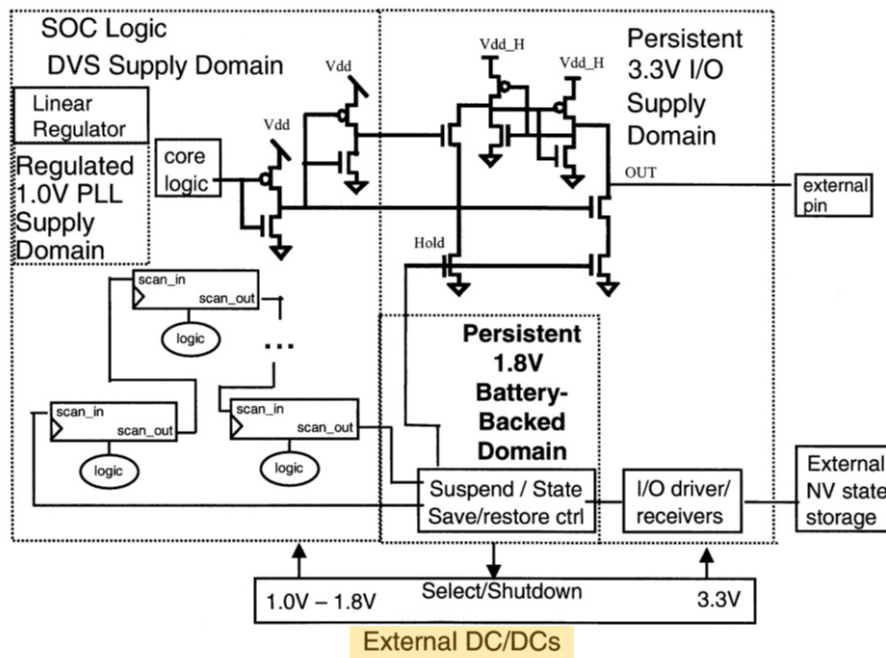


Fig. 1. PowerPC SOC structure.

MTK-1004, Fig. 1.



MTK-1004, Fig. 3.

(c) 16[b]

Supra Ground 1A, elements 1[a]-[c]. MTK-1003, ¶90. Nowka further discloses a “power manager” comprised of an “on-chip supervisor” and “system

software.” MTK-1004, 1442; MTK-1003, ¶91. The “on-chip supervisor controls the external DC/DC converter, which provides the logic supply” and “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” MTK-1004, 1442. In addition, Nowka discloses that the power supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to the control the standby power,” and during freeze mode, “the supervisor software first sets a low operating frequency and then lowers the supply.” MTK-1004, 1446; MRK-1003, ¶92. Nowka’s “power manager” also includes the PLL (which controls the frequency) and the external DC/DC (which controls the supply voltage), which work with the supervisor to execute frequency and voltage scaling, MTK-1004, 1444, and clock dividers which enable “unit and register level functional clock gating.” MTK-1004, 1445; MTK-1003, ¶93.

16. Claim 17

Supra Ground 1A, claim 2. MTK-1003, ¶94.

17. Claim 18

Supra Ground 1A, claim 3. MTK-1003, ¶95.

18. Claim 19

Supra Ground 1A, claim 4. MTK-1003, ¶96.

19. Claim 20

Supra Ground 1A, claim 5. MTK-1003, ¶97.

20. Claim 21

Supra Ground 1A, claim 6. MTK-1003, ¶98.

21. Claim 22

Supra Ground 1A, claim 7. MTK-1003, ¶99.

22. Claim 23

Supra Ground 1A, claim 8. MTK-1003, ¶100.

23. Claim 25

Supra Ground 1A, claim 10. MTK-1003, ¶101.

24. Claim 26

Supra Ground 1A, claim 11. MTK-1003, ¶102.

25. Claim 27

Supra Ground 1A, claim 12. MTK-1003, ¶103.

26. Claim 29

Supra Ground 1A, claim 14. MTK-1003, ¶104.

27. Claim 30

Supra Ground 1A, claim 15. MTK-1003, ¶105.

28. Claim 31

Nowka discloses and renders obvious a bus coupled to the power manager and the power islands. Nowka shows a “processor local bus” and “on-chip

peripheral bus” that connects its various function units in Figure 1. MTK-1003, ¶106.

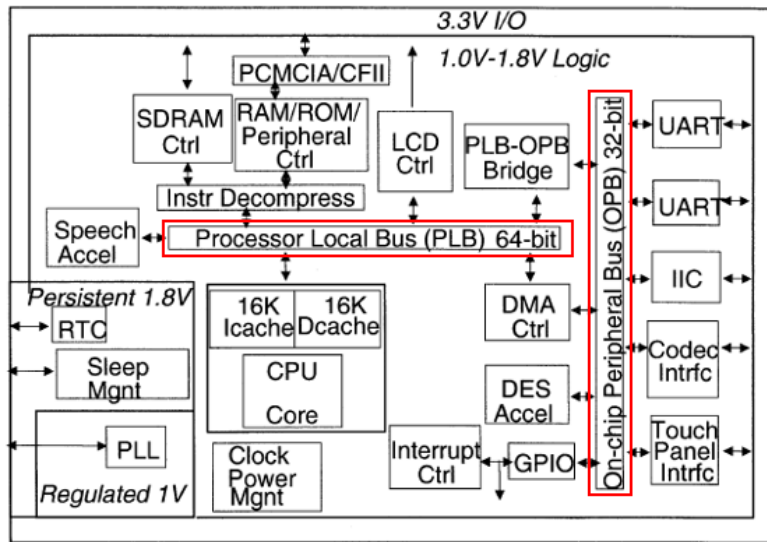


Fig. 1. PowerPC SOC structure.

MTK-1004, Fig. 1.

Nowka also discloses that “the SOC uses IBM’s Core-Connect [1] technology to integrate a rich set of memory and I/O devices.” MTK-1004, 1441. The “Core-Connect technology allows integration of semicustom synthesized cores and custom hard-cores in an SOC.” MTK-1004, 1445; MTK-1003, ¶107. Figure 1 in the CoreConnect Bus Architecture White Paper shows various buses connecting the power manager (“Reset Clock Control Power Mgmt”) to the other SOC components. Accordingly, a POSITA would have understood that the Nowka has a bus coupled to the power manager and the power islands. MTK-1003, ¶107.

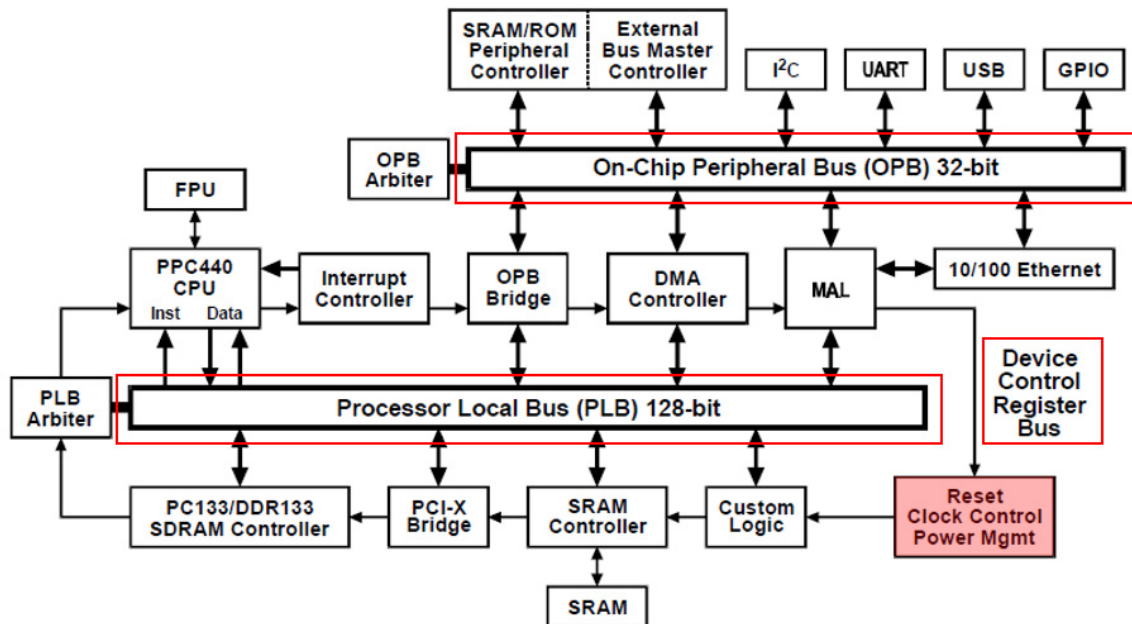


Figure 1: CoreConnect Based System-On-a-Chip.

MTK-1023, Fig. 1.

29. Claim 32

Nowka discloses and renders obvious that the power manager comprises a master manager configured to control power of the integrated circuit. Nowka discloses an “on-chip supervisor” that “requests changes to the logic supply and requests shutdown of the logic supply during hibernation,” MTK-1004, 1442, and “manages the clocks, internal state and external power supply to control the standby power.” MTK-1004, 1446; MTK-1003, ¶108. A POSITA would have recognized the on-chip supervisor acts as a master power manager because it oversees the global power behavior of the system. MTK-1001, 5:47-48; MTK-1003, ¶108.

30. Claim 33

Nowka discloses that the power manager comprises a slave manager configured to control power of one of the power islands. First, the PLL (which controls the frequency) and the external DC/DC converters (which control the supply voltage) constitute a “slave manager” because they control the power of the logic domain. MTK-1004, 1442, 1444, MTK-1003, ¶109. Second, Nowka discloses “clock dividers controlled by register values” that “allow[s] the clocks to the cores to be modified dynamically and individually.” MTK-1004, 1445. A POSITA would have understood the clock dividers and the relevant registers as additional “slave manager.” MTK-1003, ¶110.

31. Claim 34

Nowka discloses that the power control circuitry includes clock multiplexing circuitry. Nowka discloses an “output multiplexor” that “allows for clock freezing for sleep and hibernation modes. The output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock.” MTK-1004, 1444, Fig. 7; MTK-1003, ¶111.

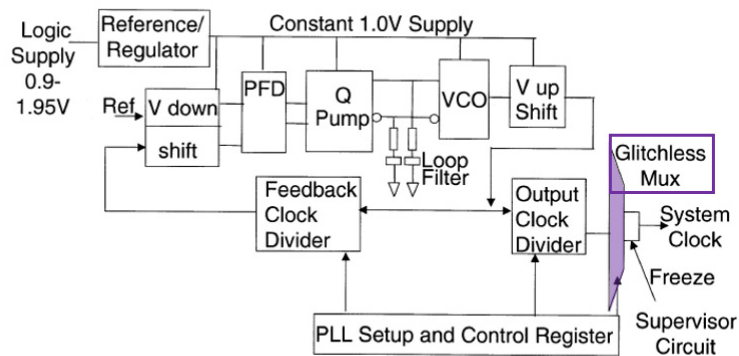


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

MTK-1004, Fig. 7.

32. Claim 36

Nowka discloses that the power control circuitry includes level shifting circuitry. Nowka discloses that “signals passing from the logic domain to the persistent domain are latched by *level shifters* at the interface.” MTK-1004, 1443; MTK-1003, ¶112. Further, “the PLL integrates *level shifting* into the reference clock, feedback clock and output clock paths.” MTK-1004, 1444; MTK-1003, ¶112.

33. Claim 37

(a) 37[p]

Supra Ground 1A, element 1[p]. MTK-1003, ¶113. Nowka also discloses “a software product” because it discloses “system software” that requests changes to the logic supply and requests shutdown of the logic supply during hibernation,” MTK-1004, 1442, “can lower the operating frequency,” MTK-1004, 1444, exert “control over the PLL and external DC/DC,” MTK-1004, 1444, modifies “both the

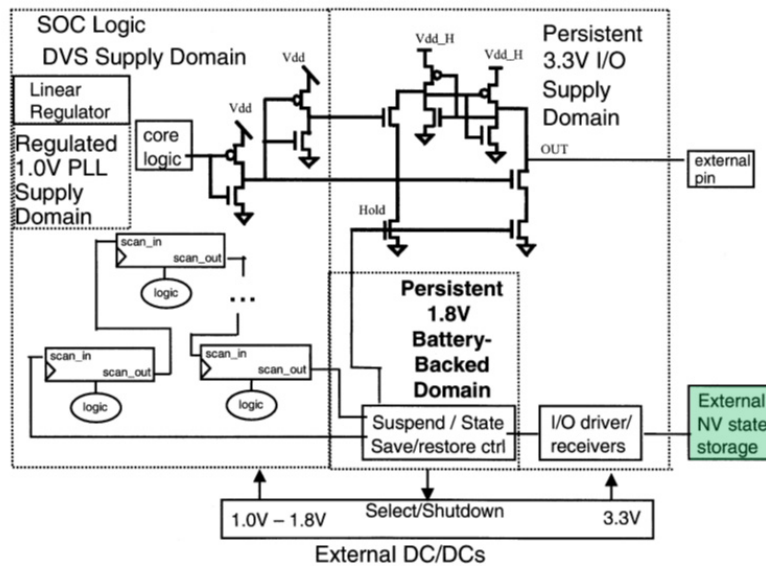
voltage and the frequency of the processor...thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption,” MTK-1004, 1446, and cause the processor to “enter both a low-leakage sleep state and a state-preserving deep-sleep state to minimize standby power consumption.” MTK-1004, 1446; MTK-1003, ¶113.

(b) 37[a]

Supra Ground 1A, elements 1[a]-[c]. MTK-1003, ¶114. Nowka also discloses “a power management software” because a POSITA would have understood and found obvious that Nowka’s software executes power management functions. MTK-1004, 1442, 1444, 1446; MTK-1003, ¶115.

(c) 37[b]

It would have been obvious to a POSITA that Nowka’s software product would be stored in a software storage medium, namely the external volatile state storage off-chip, as such a setup was common, and also contemplated in the ’306 Patent. MTK-1004, 1441-1443, 1446; MTK-1001, 4:58-59, Fig. 2; MTK-1003, ¶116.



MTK-1004, Fig. 3.

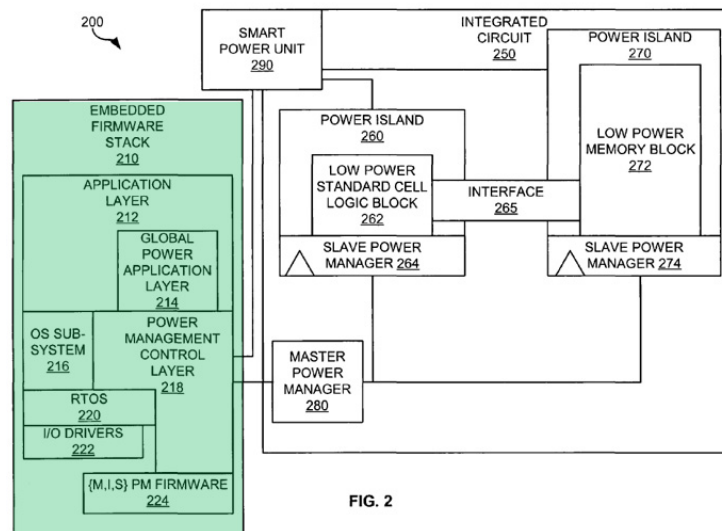


FIG. 2

MTK-1001, Fig. 2.

34. Claim 38

Supra Ground 1A, claim 2. MTK-1003, ¶117.

35. Claim 39

Supra Ground 1A, claim 3. MTK-1003, ¶118.

36. Claim 40

Supra Ground 1A, claim 4. MTK-1003, ¶119.

37. Claim 41

Supra Ground 1A, claim 5. MTK-1003, ¶120.

38. Claim 42

Supra Ground 1A, claim 6. MTK-1003, ¶121.

39. Claim 43

Supra Ground 1A, claim 7. MTK-1003, ¶122.

40. Claim 44

Supra Ground 1A, claim 8. MTK-1003, ¶123.

41. Claim 46

Supra Ground 1A, claim 10. MTK-1003, ¶124.

42. Claim 47

Supra Ground 1A, claim 11. MTK-1003, ¶125.

43. Claim 48

Supra Ground 1A, claim 12. MTK-1003, ¶126.

44. Claim 50

Supra Ground 1A, claim 14. MTK-1003, ¶127.

45. Claim 51

Supra Ground 1A, claim 15. MTK-1003, ¶128.

B. GROUND 1B—Claims 9, 13, 24, 28, 45, and 49 are obvious over Nowka and Borkar

1. Overview of Borkar

Borkar relates to software control and control circuitry that control parameters such as performance, power consumption, and temperature in a processor. MTK-1006, Abstract. Borkar discloses controlling various circuit parameters, such as performance, power consumption, and temperature in integrated circuits. MTK-1006, 2:2-3. Borkar discusses controlling these parameters by changing the clock frequency, supply voltage, and threshold voltage (via body bias signals). MTK-1006, 2:49-54, Figs. 1-3, 5, 7, 9; MTK-1003, ¶131. Borkar discloses some embodiments that are a single-processor system (Figs. 1-4) and some embodiments with multiple “domains” (Figs. 5, 7). MTK-1003, ¶132. Borkar’s “domains” shown in Figures 5 and 7, also called “functional unit blocks,” are groups of transistors, which can be controlled independently of each other. MTK-1006, 9:48-59, 10:34-36; MTK-1003, ¶132.

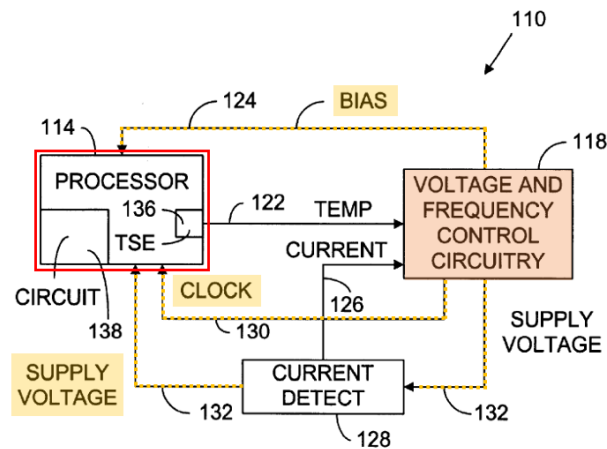


FIG. 1

MTK-1006, Fig. 1 (single-processor embodiment).

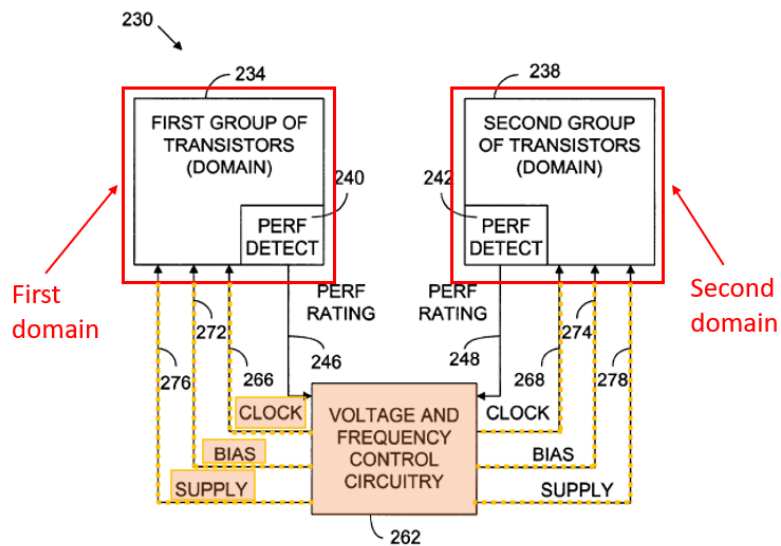


FIG. 5

MTK-1006, Fig. 5 (multiple-domain embodiment).

Borkar explains that the goal in an integrated circuit may be “keeping power consumption below a particular level” or “obtaining the highest performance while not exceeding a particular power consumption level.” MTK-1006, 12:10-15. “A

simple but imprecise way [to not exceed power consumption levels] is to not allow the supply voltage, threshold voltages, or frequency, to pass certain levels. A more precise way is to detect current being consumed.” MTK-1006, 13:4-8. For example, Figures 1 and 7 show current detection circuitry which detects current being consumed and provides that information to the voltage and frequency control circuitry. MTK-1006, 4:58-60, 7:39-42, 13:8-11; *see also* MTK-1006, Figs. 2, 4; MTK-1003, ¶133. The control circuitry can then determine the power being consumed. MTK-1006, 4:64-67, 6:64-67, 13:7-8; MTK-1003, ¶133.

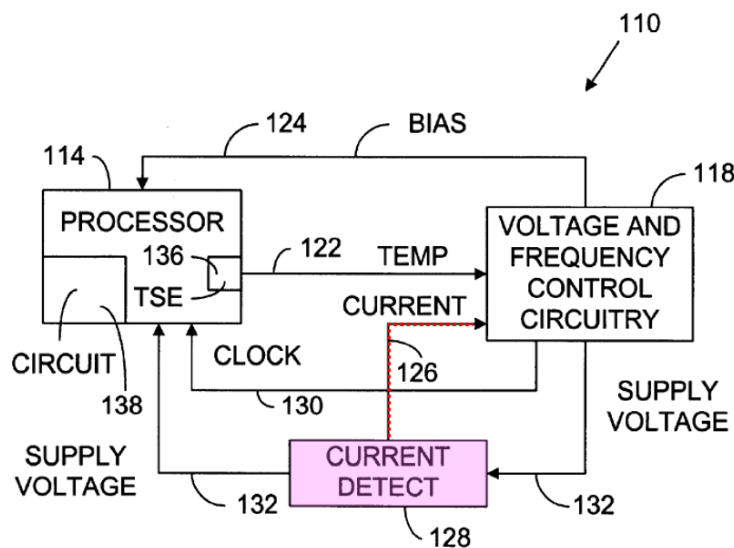


FIG. 1

MTK-1006, Fig. 1.

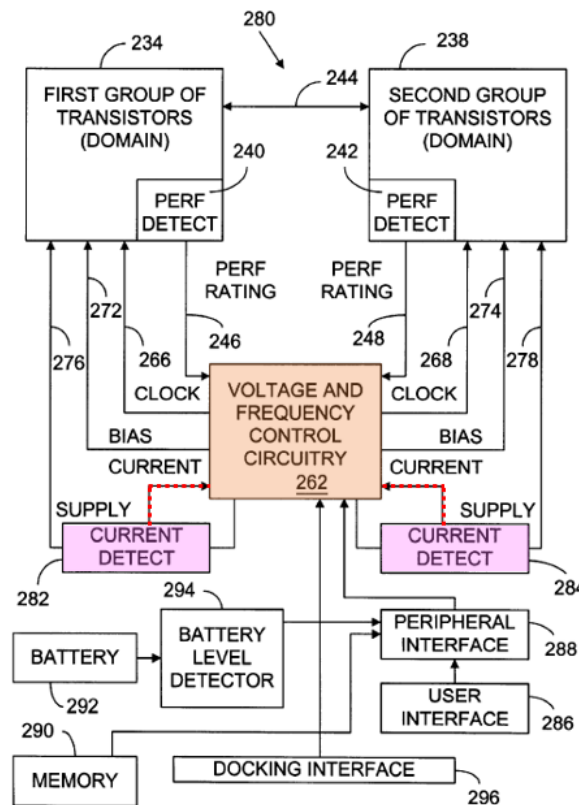


FIG. 7

MTK-1006, Fig. 7.

2. Nowka-Borkar Combination

A POSITA would have been motivated to modify Nowka's SOC to incorporate the teachings of Borkar with reasonable expectation of success. Nowka and Borkar are in the same field of endeavor: power management on an integrated circuit. MTK-1004, 1441 ("A PowerPC system-on-a-chip processor...adapt[s] to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications[.]"); MTK-1006, 2:49-57 ("The invention involves changing body bias signals applied to transistors in an integrated circuit in response to changing conditions to at least

partially control a parameter of the integrated circuit... A parameter of the integrated circuit is a characteristic of the integrated circuit which can vary during performance including temperature, power consumption, and performance.”); MTK-1003, ¶135.

Further, Nowka and Borkar address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1004, 1441 (“While [devices’] peak performance demands tend to be significant, they are also highly power constrained.”), MTK-1006, 1:20-21 (“The performance, power consumption, and temperature [of an integrated circuit] are typically related.”), 5:45-46 (“The user may specify certain power conditions or a power versus performance tradeoff.”); MTK-1003, ¶136. Both Nowka and Borkar teach the known solution of using distinct units on an integrated circuit whose power can be independently controlled. MTK-1004, 1442 (“To support DVS in this SOC, the power distribution has been divided into four distinct domains as shown in Fig. 3), Fig. 3; MTK-1006, 10:34-39 (“The first and second groups of transistors may be different function unit blocks (FUBS) on the same chip...”); MTK-1003, ¶137. Both Nowka and Borkar also suggest the identified, predictable solution of dynamically changing variables such as frequency and voltage according to certain needs and operation of the integrated circuit. MTK-1004, 1442 (“The primary means of matching the performance and power consumption of this device to the

application is through the use of dynamic voltage scaling (DVS).”); MTK-1006, 6:48-53 (““The process of selecting the body bias, supply voltage, and/or clock settings in control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and current) and other signals indicating preference[.]”); MTK-1003, ¶138.

Because Nowka and Borkar provide similar solutions to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references when selecting a method for Nowka’s dynamic power management mechanism. MTK-1003, ¶138. For example, Nowka does not explicitly disclose comparing the power consumption to a threshold and performing an action based on the crossing of the threshold level. A POSITA would have been motivated to look to Borkar’s threshold-comparing technique because, for example, Nowka teaches that “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” MTK-1004, 1441; MTK-1003, ¶139. Nowka also does not explicitly disclose changing a threshold voltage to control the power consumption. However, Nowka explains that “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency.” MTK-1004, 1446. Thus, a POSITA

would have been motivated to look to Borkar's threshold voltage-tuning solution to alleviate static power in Nowka's SOC. MTK-1003, ¶140.

3. Claim 9

The Nowka-Borkar combination renders obvious modifying a voltage, where that voltage is a threshold voltage. Borkar explains how threshold voltage interacts with performance and power consumption, and how controlling threshold voltage can alleviate leakage power. "The switching speed is increased with a lower threshold voltage and increased with a higher threshold voltage. The leakage power consumption is higher with a smaller threshold voltage and lower with a higher threshold voltage." MTK-1006, 3:50-55; MTK-1003, ¶141. A POSITA would have understood that modifying the threshold voltage of the transistors in a power island would have been useful for controlling the power consumption of the transistors in that power island. MTK-1003, ¶141.

Borkar discloses modifying threshold voltage of transistors in response to temperature or power conditions in the integrated circuit. For example:

In some embodiments, if the temperature TACTUAL of processor 114 as represented in the temperature signal on conductor(s) 122 exceeds an upper temperature limit THIGH, control circuitry 118 changes the *body bias*, supply voltage, and/or clock signal settings to decreases temperature. For example, the supply voltage and clock frequency may be decreased, and/or body bias signals changed *so that the threshold voltage is raised*. In some

embodiments, if TACTUAL drops below a lower temperature limit TLOW, control circuitry 118 may increase the supply voltage, increase the clock frequency, and/or the change the bias voltages *so that the threshold voltage is lowered*.

MTK-1006, 4:21-32. In this example, threshold voltage is raised or lowered in response to certain temperature conditions, which indicate needs and operation of the integrated circuit (temperature too high or too low). MTK-1003, ¶141.

Borkar also explains that “when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to *raise the threshold voltages* of some or all of the transistors. This will reduce the power consumption to maintain the battery.”

MTK-1006, 5:25-30. Once again, threshold voltages are changed to change the power consumption based on needs and operation of the system (battery power is low). *See also* MTK-1006, 6:15-24 (discussing using threshold voltage to balance performance and power consumption); MTK-1003, ¶142.

Nowka teaches that “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems.” MTK-1004, 1446. A POSITA would have been motivated to implement Borkar’s threshold voltage-tuning mechanism in Nowka because a POSITA would have known that modifying

threshold voltage helps reduce static power consumption. MTK-1003, ¶143. For example, Borkar explains that “[t]he leakage power consumption is higher with a smaller threshold voltage and lower with a higher threshold voltage” and that “leakage power can still be reduced by increasing the threshold voltages,” and such concepts were well-understood in the art. MTK-1006, 3:53-55, 6:23-24; MTK-1003, ¶143. A POSITA would have needed only routine electrical and computer engineering principles to implement changing threshold voltages. MTK-1003, ¶143.

4. Claim 13

The Nowka-Borkar combination renders obvious monitoring the power consumption level of a power island, determining whether a threshold level was crossed based on the power consumption level, and performing another action based on the crossing of the threshold level. Nowka discloses that “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” MTK-1004, 1441. A POSITA would have understood that Nowka recommends implementing a power consumption threshold and would have naturally looked to a reference like Borkar which discloses such a mechanism. MTK-1003, ¶¶144-145.

Borkar discloses numerous embodiments (depicted in Figures 1-2, 4, 7) that explicitly show “current detection circuitry” which provide current signals to

“voltage and frequency control circuitry.” Figure 7 of Borkar shows current detection circuitry 282 and 284, which provide current signals to control circuitry 262. MTK-1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7 (Figs. 1, 7 shown below). Because current multiplied by supply voltage is power consumption, Borkar’s system is able to monitor power consumption by monitoring current signal. MTK-1006, 4:64-67, 13:7-8. By calculating the power consumption in this way, the system can monitor the power consumption and take appropriate actions, such as changing body bias, supply voltage, and clock frequencies, to prevent power consumption from crossing a certain level. MTK-1006, 6:1-7, 13:4-7; MTK-1003, ¶146.

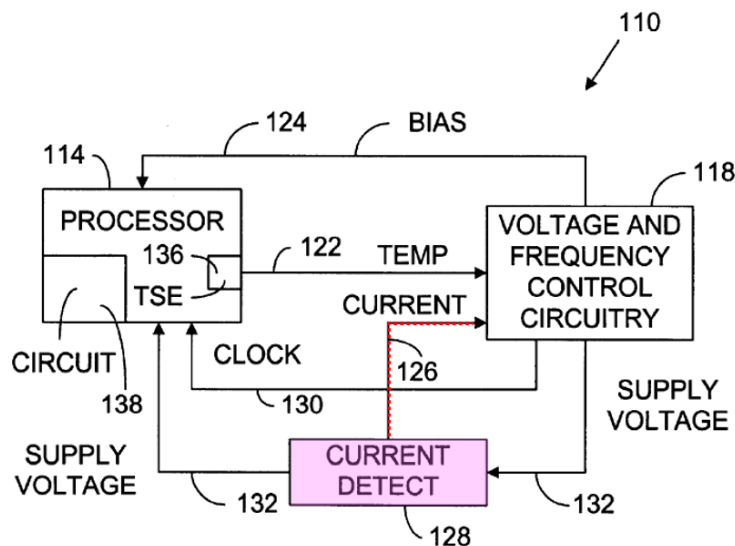


FIG. 1
MTK-1006, Fig. 1.

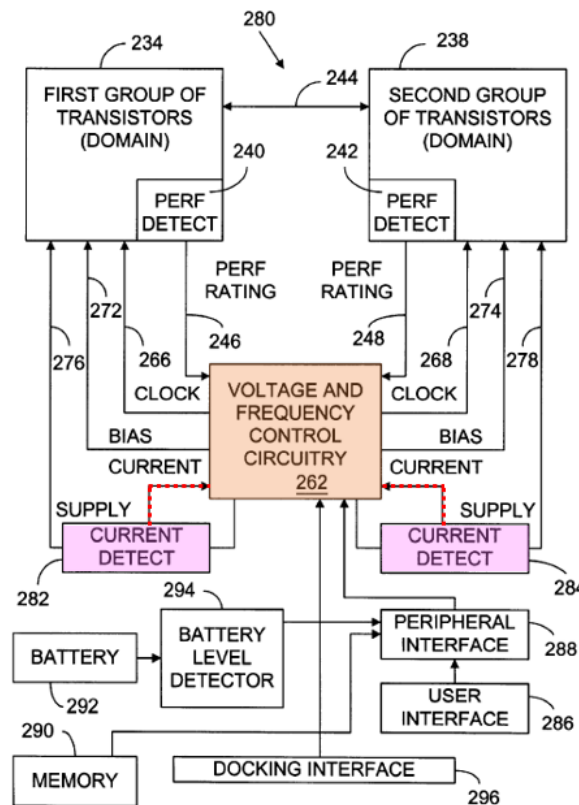


FIG. 7

MTK-1006, Fig. 7.

A POSITA would have been motivated to combine Borkar's power consumption monitoring with Nowka's voltage and frequency scaling to achieve more precise and predictable power consumption control because Nowka teaches that "during active computation [the system's] required performance tends to vary widely and quickly as a function of the workload" and "during peak activity the power consumption of the processor core is best kept at or below 500 mW." MTK-1004, 1441; MTK-1003, ¶147. A POSITA would have needed only routine electrical and computer engineering principles to implement Borkar's monitoring

and threshold-comparing mechanism in Nowka's SOC, as demonstrated by Borkar's implementation in a system directly analogous to Nowka's SOC. MTK-1006, 2:49-52 ("The invention involves changing body bias signals applied to transistors in an integrated circuit in response to changing conditions to at least partially control a parameter of the integrated circuit."); MTK-1003, ¶148. Such a combination would predictably result in improved performance and longevity. MTK-1003, ¶148.

5. Claim 24

Supra Ground 1B, claim 9. MTK-1003, ¶149.

6. Claim 28

Supra Ground 1B, claim 13. MTK-1003, ¶150.

7. Claim 45

Supra Ground 1B, claim 9. MTK-1003, ¶151.

8. Claim 49

Supra Ground 1B, claim 13. MTK-1003, ¶152.

C. GROUND 1C—Claim 35 is obvious over Nowka and Boerstler

1. Overview of Boerstler

Boerstler relates to controlling the timing of signals in integrated circuits by using a voltage controlled oscillator. MTK-1007, Abstract. Boerstler teaches that a voltage multiplexer can be used as part of a voltage controlled oscillator ("VCO"), which is "important for applications such as processor clock generation

and distribution, wired and wireless communication, system synchronization and frequency synthesis.” MTK-1007, 1:24-27. The VCO of Boerstler, shown in Fig. 4 below, is implemented using a control voltage multiplexer, an interleaved ring oscillator, and true/complement generator.

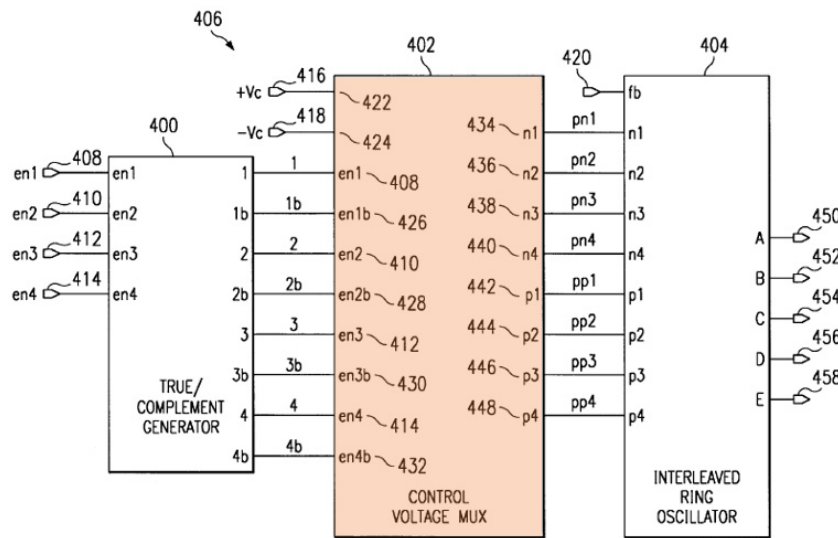


FIG. 4

MTK-1007, Fig. 4.

2. Nowka-Boerstler Combination

A POSITA would have been motivated to modify Nowka’s SOC to incorporate the teachings of Boerstler with reasonable expectation of success. First, Nowka and Boerstler resulted from work performed at the same company, IBM. MTK-1004, 1446 (“This chip represents the joint development of IBM’s Austin Research Laboratory, IBM’s Microelectronics Division [], as well as IBEM’s Tokyo Research Laboratory and IBM’s T.J. Watson Research

Laboratory.”); MTK-1007, (73) (showing IBM as assignee). Second, Nowka and Boerstler are in the same field of endeavor and involve similar concepts, such as clock generation and distribution in integrated circuits. MTK-1004, 1444 (“the clock generation subsystem is key to supporting a voltage scalable design.”); MTK-1007, 1:23-27 (“A high frequency voltage controlled oscillator (VCO) is extremely important for applications such as processor clock generation and distribution, wired and wireless communication, system synchronization and frequency synthesis.”); MTK-1003, ¶157. Thus, Boerstler is pertinent art in the same field as Nowka, and it would have been obvious to implement the teachings of Boerstler in Nowka’s SOC. MTK-1003, ¶157.

In fact, the solution offered by Boerstler for voltage multiplexing was directly cited in Nowka. Nowka cites Boerstler as a reference that describes the VCO architecture used in Nowka’s power management integrated circuit. MTK-1004, 1447 (reference 11). Because Nowka and Boerstler provide similar solutions to a similar problem within the same field of endeavor, and because Boerstler is explicitly cited in Nowka, a POSITA would have naturally looked at, and been motivated to combine, the two references when implementing Nowka’s power control circuitry. MTK-1003, ¶159.

3. Claim 35

The Nowka-Boerstler combination renders obvious a power control system

that includes voltage multiplexing circuitry. Nowka discloses a VCO integrated into the phase locked loop (PLL), as shown in Figure 7. MTK-1004, Fig. 7; MTK-1003, ¶160. The VCO is described as an “interleaved five-stage ring oscillator” that is taken from reference 11 of the paper, which is Boerstler. MTK-1004, 1444, 1447; MTK-1003, ¶161.

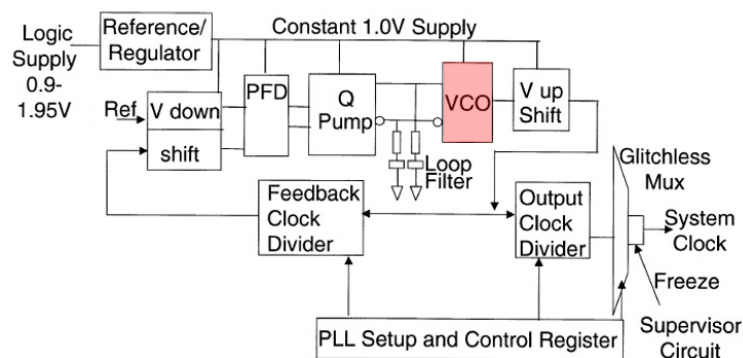


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

MTK-1004, Fig. 7.

Boerstler’s voltage controlled oscillator (VCO) is comprised of a control voltage multiplexor that can be used to change the voltage level of a control voltage. MTK-1007, 5:50-55, Fig. 4; MTK-1003, ¶162. As explained by Boerstler, the control voltage multiplexer “is used to select control elements that are to be enabled within interleaved ring oscillator 404,” MTK-1007, 5:65-6:1, and “the analog control voltage is channeled to the appropriate control elements by the analog multiplexer.” MTK-1007, 7:2-4; MTK-1003, ¶163.

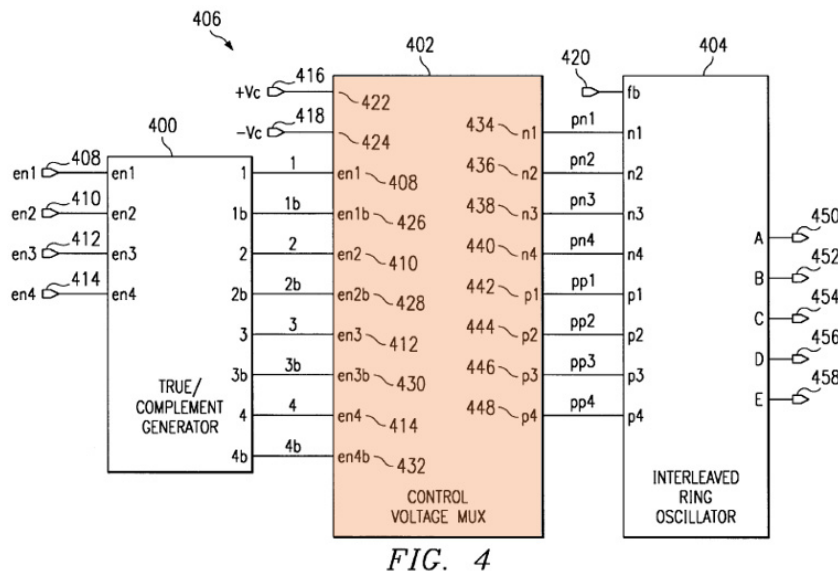


FIG. 4

MTK-1007, Fig. 4.

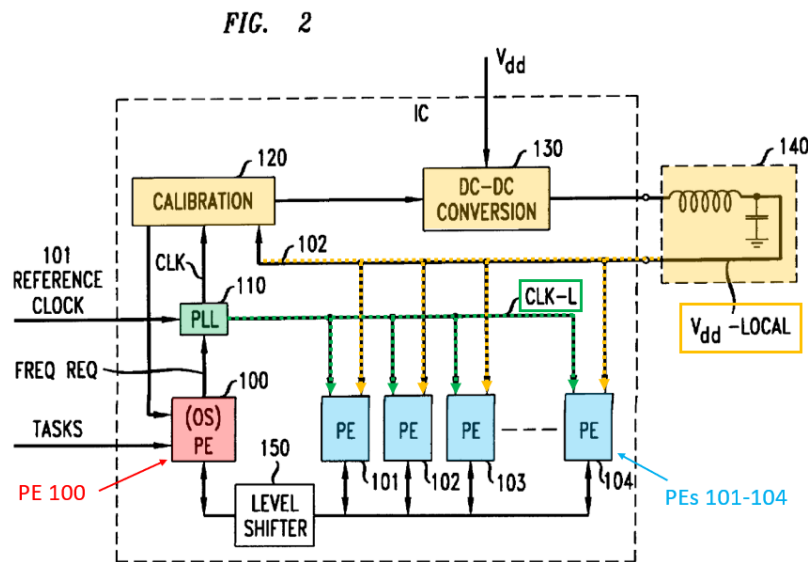
A POSITA would have been motivated to combine Boerstler's voltage multiplexing circuitry with Nowka, with reasonable expectation of success because Nowka explicitly cites to Boerstler's VCO, and such technology was commonly implemented in power control circuitry at the time. MTK-1003, ¶164.

D. GROUNDS 2A—Claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47 are obvious over Nicol

1. Overview of Nicol

Nicol discloses a dynamic load-balancing mechanism in a multiprocessor chip which divides tasks among multiple processors, and then adjusts the frequency and voltage of those processors to minimize power consumption. MTK-1008, Abstract. In the embodiment shown in Figure 2, an application “is subdivided into N concurrent task streams” and “mapped to N PEs under control of

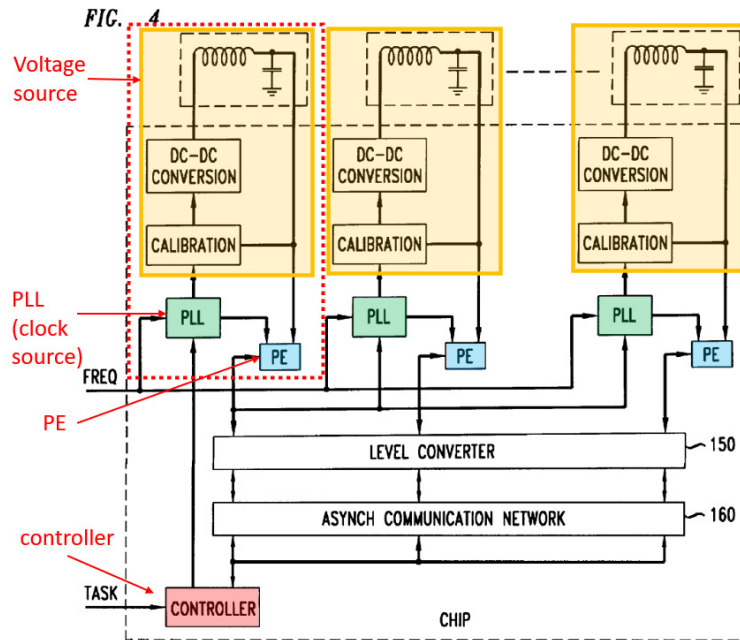
real-time operating system executed on PE 100.” MTK-1008, 3:10-13, 3:22-23; MTK-1003, ¶167. As a result of the division, each PE can be “lightly loaded,” which “allows the clock frequency of the PEs to be reduced,” which in turns “allows reducing the necessary supply voltage.” MTK-1008, 3:24-30; MTK-1003, ¶¶168-169.



MTK-1008, Fig. 2.

Nicol also explains that there are “tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage.” MTK-1008, 5:60-65; MTK-1003, ¶170. To address this limitation, Figure 4 shows each PE with its own associated clock source and voltage source to allow “the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” MTK-1008,

5:66-6:3, Fig. 4; MTK-1003, ¶¶170-171.



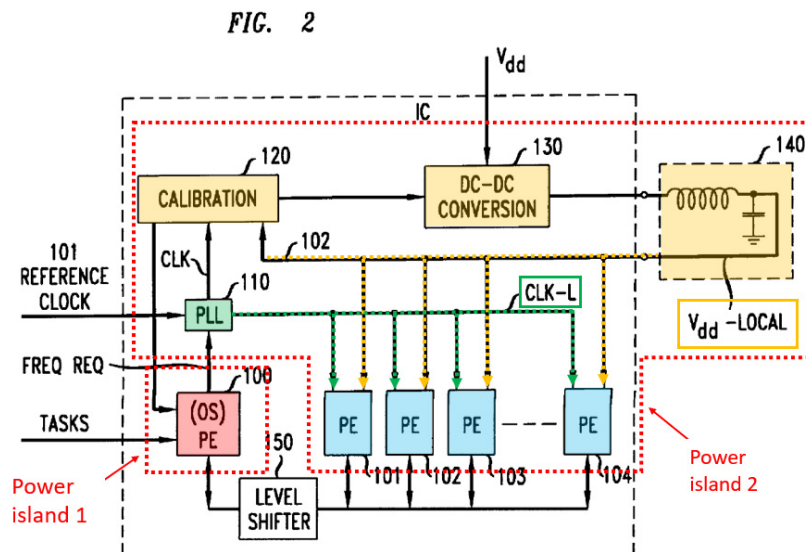
MTK-1008, Fig. 4.

2. Claim 1

(a) 1[p]

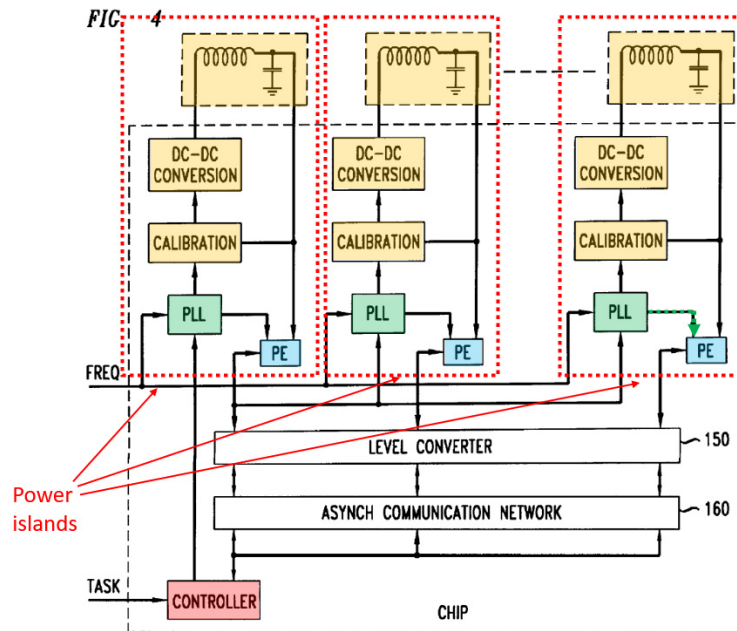
To the extent the preamble is limiting, Nicol discloses a method for managing power on an IC including a plurality of power islands. Specifically, Nicol discloses improving performance of multi-processor chips by dynamically controlling the processing load of chips and controlling the frequencies and operating voltages of those chips to minimize overall power consumption. MTK-1008, Abstract, 2:18-22, 3:21-42; MTK-1003, ¶172. Nicol's integrated circuit contains a plurality of power islands. The '306 patent defines "power island" as "any section, delineation, partition, or division of the integrated circuit [] where

power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:51-54. In the embodiment shown in Figure 2, the PE 100 and PEs 101-104 form two different power islands as they are sections, delineations, partitions, or divisions of the integrated circuit, are powered independently and receive separate clock sources. MTK-1008, 4:35 (“The V-local supply voltage is also applied to all of the PEs (excluding perhaps the operating system PE 100).”); MTK-1003, ¶173.



MTK-1008, Fig. 2.

In the embodiment shown in Figure 4, each PE (along with its respective control circuitry) is a power island because each is a section, delineation, partition, or division, has its independent voltage and clock source, allowing for independent power control. MTK-1008, 5:66-6:2, Fig. 4; MTK-1003, ¶174.

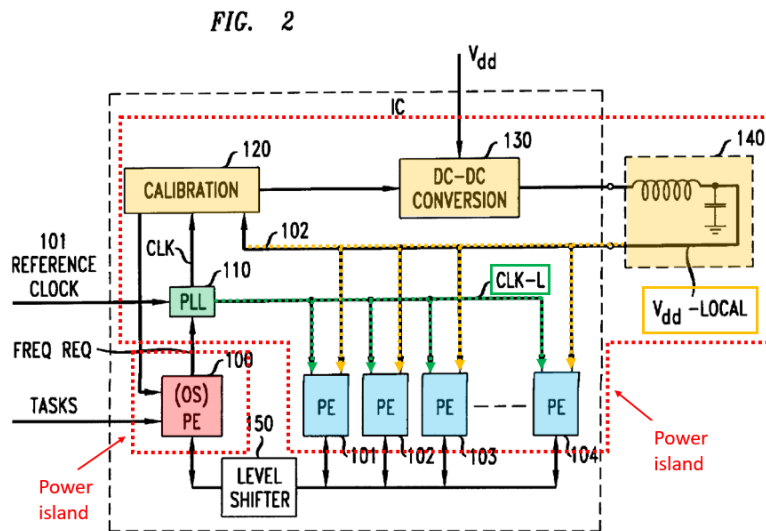


MTK-1008, Fig. 4.

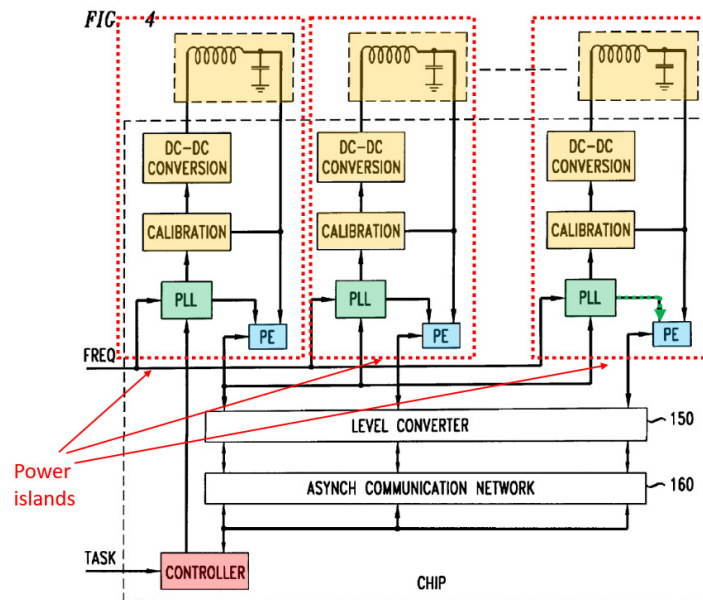
(b) 1[a]

Nicol discloses and renders obvious determining a target power level for a power island based on the needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands. First, Nicol discloses power islands, as discussed for element 1[pre] and shown in the annotations in Figures 2 and 4 below. MTK-1003, ¶¶172-175. Nicol also provides that power consumption is independently controlled within each power island. MTK-1008, 3:24-31, 5:42-45 (“Of course, Vdd-local can only be reduced so far before the circuits start to fail, at which the operating system employs gated clocking techniques to “shut down” PEs that are not needed.”), 5:66-6:2; MTK-1003, ¶176. The ability for independent control is most explicit in the embodiment

depicted in Figure 4, where “[a] separate power supply for each PE in a chip [allows] the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” MTK-1008, 5:66-6:2, Fig. 4; MTK-1003, ¶177.



MTK-1008, Fig. 2.



MTK-1008, Fig. 4.

Nicol renders obvious determining a target power level for one of the power islands based on needs and operation of the integrated circuit. The determination of the target power level of a PE takes place in the controlling operating system – either the real time operating system (RTOS) in PE 100 in the Figure 2 embodiment or the operating system in the “controller” in the Figure 4 embodiment. For the Figure 2 embodiment, Nicol explains that “the operating system of PE 100” “divide[s] the collection of tasks as evenly as possible (in terms of needed processing time)” and “adjust[s] the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time.” MTK-1008, 3:66-4:6; MTK-1003, ¶177. In the Figure 2 system, the target power level is set “to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE’s.” MTK-

1008, 3:19-21. In other words, the goal (or “needs and operation”) in the Figure 2 embodiment is to load the PEs as evenly as possible so that the task in its entirety can be completed as fast as possible. MTK-1008, 3:47-49, 3:61-65; MTK-1003, ¶178. Nicol’s target power level, then, is the lowest frequency that is needed to complete the task in the required time. MTK-1008, 3:22-4:5, 5:23-29, cl. 1 (“...determining a lowest frequency at which or above which the sub-circuit must operate in order to complete execution of the assigned task within the allotted time...”); MTK-1003, ¶178. In addition, Nicol sets the corresponding lowest needed supply voltage, which is another example of determining a target power level. MTK-1008, 4:5-16 (discussing setting the minimum supply voltage needed for the determined operating frequency); MTK-1003, ¶179.

In the context of the Figure 4 embodiment, Nicol explains that, in a computer system, “[i]t is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called. When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is, *lower clock frequency* can be employed in connection with the fast memory and the hard drive, with *a corresponding lower supply voltage*, resulting in an *overall power saving* in both the memory’s operation and in the operation of the hard drive.” MTK-1008, 6:39-56; MTK-1003, ¶180. Thus, Nicol discloses and renders obvious

that based on needs and operation of the system (the memory in the fast memory can be discarded such that lower operating speed is needed for the fast memory and the hard drive), there is a determination of the target power level (lowest frequency and voltage required for that lower performance). MTK-1003, ¶180.

A POSITA would have found it obvious from these examples that Nicol is “determining a target power level based on needs and operation of the integrated circuit” because frequency is directly proportional to power and voltage is quadratically related to power. MTK-1008, 1:26-29, 3:28-31; MTK-1003, ¶181. For example, this approach mirrors the disclosure in the ’306 Patent. MTK-1001, 7:38-50, Fig. 5; MTK-1003, ¶¶181-182. Further, Nicol renders obvious “based on needs and operation of the integrated circuit” either under the plain and ordinary meaning of this limitation, MTK-1003, ¶183, or the prior-agreed upon claim construction. First, Nicol’s disclosure mirrors the ’306 Patent’s disclosure on this limitation, which is summarized in Ground 1A, element 1[a]. MTK-1003, ¶¶183-184. Further, Nicol’s discussion that its system can “*anticipate* that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called” such that “lower clock frequency can be employed in connection with the fast memory and the hard drive,” MTK-1008, 6:39-56, shows that it responds to “future operational needs,” while Nicol’s ability to set the lowest corresponding frequency and voltage needed for its operation responds to “current

operational status” of the integrated circuit. MTK-1008, Abstract, 2:22-27, 4:54-5:2 5:66-6:2, cl. 1; MTK-1003, ¶184.

(c) 1[b]

Nicol discloses and renders obvious determining at least one of actions to change a power consumption level of one of the power islands to the target power level. As discussed for 1[a], Nicol discloses setting the target frequency and/or supply voltage for a power island either to complete a given task by the required time using the lowest frequency possible, *e.g.*, MTK-1008, 3:66-4:6, or to otherwise optimize overall power savings given the operating needs of the system, *e.g.*, MTK-1008, 6:39-56. Nicol discloses determining an action to change the power consumption level to the target power level, namely changing the frequency and/or supply voltage of the power islands, as “power consumption of a CMOS circuit increases linearly with operating frequency and quadratically with supply voltage.” MTK-1008, 1:27-36, 3:22-42; MTK-1003, ¶185. For example, in the context of Figure 2, Nicol discloses that after the “operating system of PE 100” “divide[] the collection of tasks as evenly as possible (in terms of needed processing time),” it “adjust[] the clock frequency to insure that the most heavily loaded PE carries out its adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is thus determined, a minimum supply voltage can be determined.”

MTK-1008, 3:66-4:6; MTK-1003, ¶186. Nicol provides further examples, including exemplary frequency and voltage levels and the timing of these actions. MTK-1008, 3:31-42, 4:54-5:2, Fig. 3; MTK-1003, ¶¶186-187. As discussed previously, Nicol similarly discloses examples of setting a lower frequency and lower supply voltage to match the needs of the system in an embodiment where it is desirable for different components to operate at different speeds (such as in Figure 4). MTK-1008, 6:39-56; MTK-1003, ¶188.

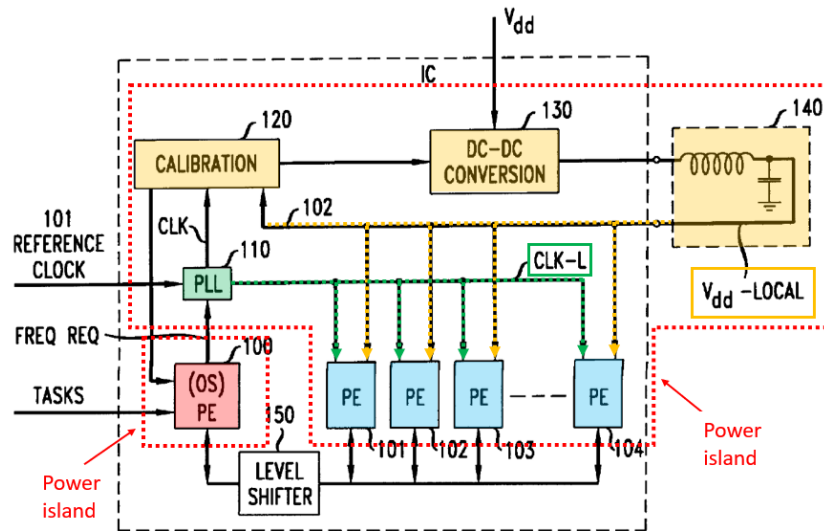
(d) 1[c]

Nicol discloses changing the frequency to change the power consumption level of a PE to the target power level determined based on the required task. As discussed for 1[b], incorporated herein, Nicol discloses changing frequency and/or supply voltage for power islands depending on the load placed on the Pes, which in turn is calculated based on needs and operation of the integrated circuit. MTK-1008, 3:21-4:10, 4:54-66, cl. 2 (“... a frequency at which or above which the sub-circuit operates is set to said determined frequency.”); MTK-1003, ¶189.

3. Claim 2

Nicol renders obvious wherein the power islands are delineated based on geographic factors of the integrated circuit. For example, Figure 4 shows that each PE has its own associated power supply and clock supply, and a POSITA would have understood from basic circuit design principles that each PE would have to be

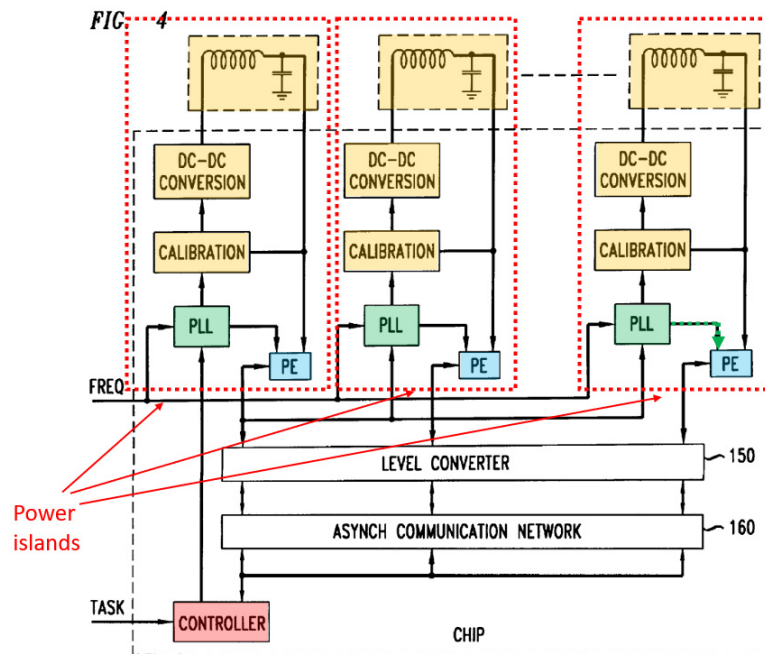
FIG. 2



MTK-1008, Fig. 2.

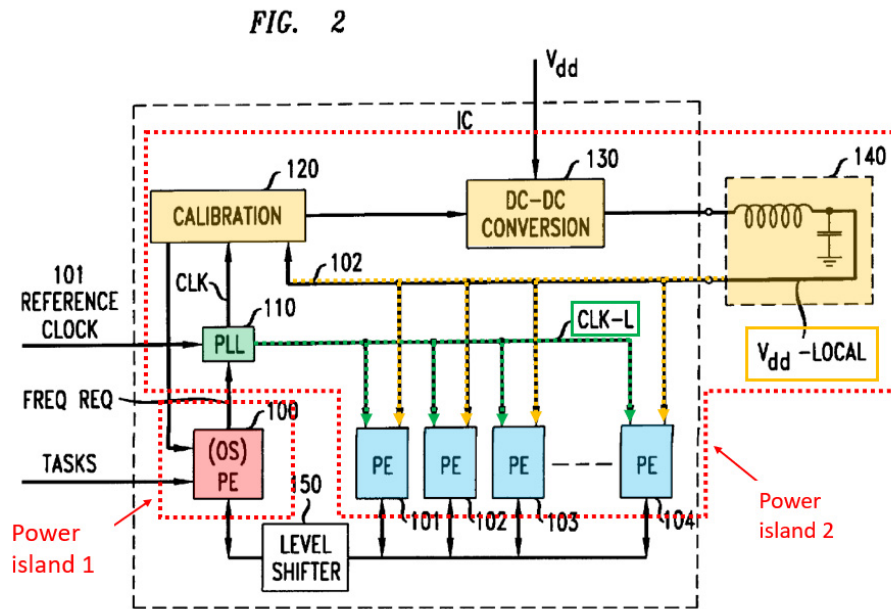
4. Claim 3

Nicol renders obvious wherein the power islands are delineated based on functional circuitry of the integrated circuit. First, a POSITA would have understood and found obvious that the power islands in the Figure 4 embodiment, which are the PEs, are delineated based on functional circuitry because each PE is capable of executing different functions. MTK-1008, 2:53-56, 3:66-4:5, 5:23-29; MTK-1003, ¶¶192-193. Such ability to allocate different tasks to the PEs motivates the provision of individual power and clock source. MTK-1003, ¶¶192-193.



MTK-1008, Fig. 4.

A POSITA would have further understood and found obvious that the power islands in the Figure 2 embodiment are delineated based on functional circuitry because the power islands are separated based on PE 100's function of hosting the real-time operating system which allocates tasks among the other PEs. MTK-1008, 2:53-56, 3:66-4:5, 4:35-37; MTK-1003, ¶194.



MTK-1008, Fig. 2.

5. Claim 4

Nicol discloses and renders obvious wherein the power islands further comprise further power sub-islands. The '306 Patent explains that power sub-islands are units within power islands “to provide further specificity in controlling power in the integrated circuit[.]” MTK-1001, 3:63-66. First, a POSITA would have recognized that each PE within the power island in the Figure 2 embodiment would be a power sub-island capable of being power controlled. MTK-1008, 2:52-53; MTK-1003, ¶195.

Second, a POSITA would have recognized that each PE (power island in the Figure 4 embodiment) themselves comprise sub-units whose power can be further controlled. For example, one PE could be a CPU, which a POSITA would have

understood to comprise sub-units such as cores or latches that can be turned on and off individually, or otherwise controlled via clock or power gating. MTK-1003, ¶196. A POSITA would have been motivated to implement power sub-islands based on Nicol's teaching on power management at different levels of abstraction, as well as general knowledge in the art to implement power management at various levels of abstraction. MTK-1008, 6:66-7:3; MTK-1003, ¶197.

6. Claim 5

Nicol renders obvious wherein the power islands comprise multiple clock domains. A POSITA would have understood and found obvious that each PE in Nicol comprises multiple sub-units, each of which can be clock gated, thereby creating multiple clock domains in each PE. MTK-1003, ¶198.

7. Claim 7

Nicol discloses modifying a voltage for a PE. Nicol explains that “reduced load permits lowering the clock frequency to 100 MHz and *lowering the supply voltage* to 2.1V.” MTK-1008, 4:54-66. In the Figure 2 embodiment, Vdd-local, which powers power island 2 (consisting of PEs 101-104) is changed. MTK-1008, 3:31-42, 4:5-16, 4:54-5:22, 5:35-41, 5:44-49, cl. 1; MTK-1003, ¶199. In the Figure 4 embodiment, “[a] separate power supply for each PE in a chip” allows for independently programming the “corresponding lowest supply voltage” for each PE. MTK-1008, 5:66-6:2, Fig. 4; MTK-1003, ¶200.

8. Claim 8

Nicol discloses modifying a source voltage. A POSITA would have understood that Vdd-local in Figure 2 and the voltages supplied to each PE in Figure 4 are “source voltages” because they supply the power that allows the PEs to operate. MTK-1008, 3:28-31, 3:31-42, 4:5-16, 5:66-6:2, cl. 1; MTK-1003, ¶201.

9. Claim 9

Nicol renders obvious modifying a threshold voltage for one of the power islands. Nicol explicitly describes varying the threshold voltage as a known on-chip voltage scaling technique. MTK-1008, 1:65-2:10. Nicol references the paper by Kuroda et al., “Variable Supply-Voltage Scheme for Low Power High-Speed COMS Digital Design,” (“Kuroda”) which demonstrates that tuning threshold voltages as supply voltage is lowered helps minimize speed degradation. *Id.*; MTK-1003, ¶202. This discussion in Nicol shows that changing a threshold voltage was a known technique that was routinely applied to improve performance in chips, and it would have been obvious to a POSITA to including to control the power consumption level. MTK-1003, ¶¶202-203.

10. Claim 11

Nicol discloses powering off one of the power islands. *See* MTK-1008, claim 36 (“The apparatus of claim 32 further comprising means within said

controller for turning supply power off to at least one of said N processing elements.”); MTK-1003, ¶204.

11. Claim 16

(a) 16[p]

Supra Ground 2A, element 1[p]. MTK-1003, ¶205. Nicol further discloses a “system” because it discloses the circuit which carries out the power management mechanism. MTK-1008, 2:50-58, 5:66-6:12, Figs. 2, 4, cl. 17; MTK-1003, ¶205.

(b) 16[a]

Nicol discloses power control circuitry configured to control power for one of the PEs. The voltage conversion circuitry and the PLL associated with each power island in the Figure 2 and 4 embodiments are “power control circuitry” because they control the power of the power island via controlling voltage and frequency, respectively. MTK-1008, 4:17-37, Figs. 2, 4; MTK-1003, ¶¶206-207.

(c) 16[b]

Supra Ground 2A, elements 1[a]-[c]. MTK-1003, ¶208. Nicol further discloses a power manager (PE 100 in Figure 2 or “controller”/PE 200 in Figure 4) as discussed for element 1[a]. MTK-1003, ¶209-210.

12. Claim 17

Supra Ground 2A, claim 2. MTK-1003, ¶211.

13. Claim 18

Supra Ground 2A, claim 3. MTK-1003, ¶212.

14. Claim 19

Supra Ground 2A, claim 4. MTK-1003, ¶213.

15. Claim 20

Supra Ground 2A, claim 5. MTK-1003, ¶214.

16. Claim 22

Supra Ground 2A, claim 7. MTK-1003, ¶215.

17. Claim 23

Supra Ground 2A, claim 8. MTK-1003, ¶216.

18. Claim 24

Supra Ground 2B, claim 9. MTK-1003, ¶217.

19. Claim 26

Supra Ground 2A, claim 11. MTK-1003, ¶218.

20. Claim 31

Nicol discloses a bus (“line”) coupled to the power manager and the power islands. *See* MTK-1008, 4:17-53; MTK-1003, ¶219. To the extent that Nicol does not expressly disclose a bus, it would have been obvious to a POSITA that the PEs and the controlling circuitry on the SOC would be connected by a bus because busses were a commonly used technology at the time of the invention. MTK-1003, ¶219. This is further supported by the presence of a “level shifter” or “level

converter” in Figures 2 and 4, and “asynchronous communication network” in Figure 4, which would allow for uniform frequency and voltage signals across the bus network. MTK-1008, 6:18-33, MTK-1003, ¶220.

21. Claim 32

Nicol discloses wherein the power manager comprises a master manager configured to control power of the integrated circuit. The '306 Patent explains that the master manager is “any circuitry configured to control the ‘global’ power behavior of the entire integrated circuit” and communicates with the slave power managers, which controls power within the power islands. MTK-1001, 5:47-53, Fig. 2. The “controller” in Nicol (PE 100 in the embodiment shown in Figure 2, “controller” in the embodiment shown in Figure 4) is a master manager, because it communicates with the plurality of individual power islands (PEs) to manage the power consumption of the integrated circuit as a whole. MTK-1008, 2:53-56, 3:10-21, 3:66-4:10, 5:23-28, 6:6-13 (discussing “controller” or “PE 200” that assigns tasks among the PEs and calculates required frequency and/or voltage); MTK-1003, ¶221.

22. Claim 33

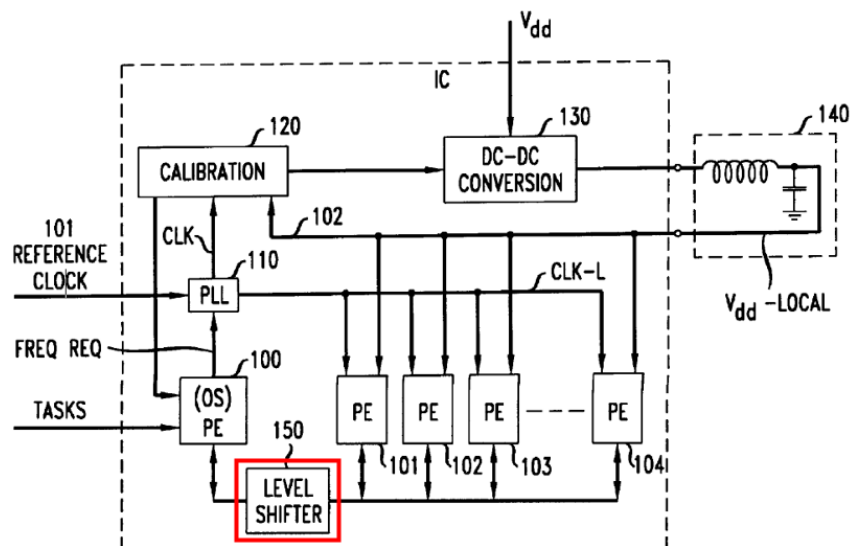
Nicol discloses wherein the power manager comprises a slave manager configured to control power of one of the power islands. In contrast to the master manager, which controls power of the whole integrated circuit, a slave manager

specifically controls the power of a power island. MTK-1001, 5:47-53, Figs. 2, 4, 12. In each embodiment, the PLL and voltage circuitry is a slave manager which controls the power of the PE. MTK-1008, 2:50-53, 6:3-6; MTK-1003, ¶222.

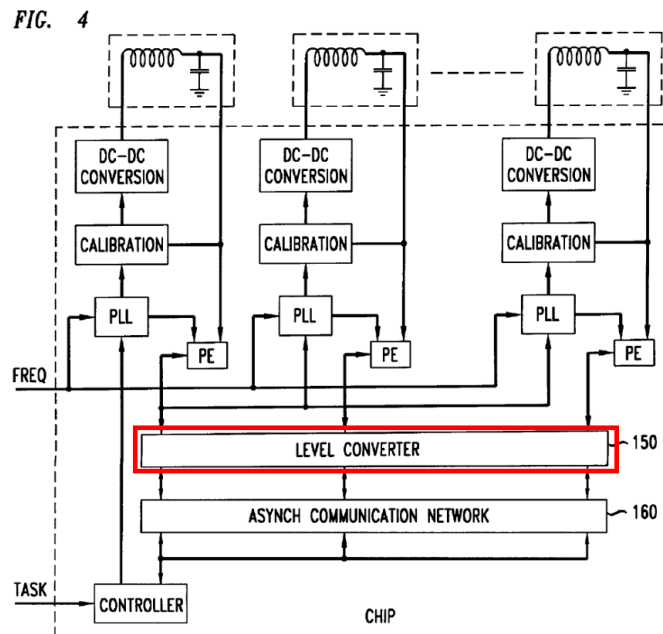
23. Claim 36

Nicol discloses level shifting circuitry. MTK-1008, 5:49-52 (“This is accomplished with level converter 150, which is quite conventional...”), 6:29-32, 7:9-11, Figs. 2, 4; MTK-1003, ¶223-224.

FIG. 2



MTK-1008, Fig. 2.



MTK-1008, Fig. 4.

24. Claim 37

(a) 37[p]

Supra Ground 2A, element 1[p]. MTK-1003, ¶225. Further, Nicol’s power management is executed on an operating system, which a POSITA would have understood to be a “software product.” MTK-1008, 2:53-56, 3:10-21, 3:66-4:16, 4:38-53, 5:23-29, 5:66-6:13; MTK-1003, ¶225.

(b) 37[a]

Supra Ground 2A, elements 1[a]-[c]. MTK-1003, ¶226. Nicol discloses an operating system, which a POSITA would have understood to be “power management software.” MTK-1008, 2:53-54, 4:11-13; MTK-1003, ¶226.

(c) 37[b]

Nicol discloses that its software product is stored in a software storage

medium. Nicol's operating system resides in PE 100 (Fig. 2) or the controller or PE 200 (Fig. 4). MTK-1008, 2:53-56, 3:10-21, 3:66-4:5, 6:6-13; MTK-1003, ¶227.

25. Claim 38

Supra Ground 2A, claim 2. MTK-1003, ¶228.

26. Claim 39

Supra Ground 2A, claim 3. MTK-1003, ¶229.

27. Claim 40

Supra Ground 2A, claim 4. MTK-1003, ¶230.

28. Claim 41

Supra Ground 2A, claim 5. MTK-1003, ¶231.

29. Claim 42

Supra Ground 2A, claim 6. MTK-1003, ¶232.

30. Claim 43

Supra Ground 2A, claim 7. MTK-1003, ¶233.

31. Claim 44

Supra Ground 2A, claim 8. MTK-1003, ¶234.

32. Claim 45

Supra Ground 2A, claim 9. MTK-1003, ¶235.

33. Claim 47

Supra Ground 2A, claim 11. MTK-1003, ¶236.

E. GROUND 2B—Claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51 are obvious over Nicol and Nowka

1. Overview of Nowka

Supra Ground 1A, Overview of Nowka. MTK-1003, ¶238.

2. Nicol-Nowka Combination

A POSITA would have been motivated to modify Nicol with the teachings of Nowka with a reasonable expectation of success. Nicol and Nowka are in the same field of endeavor: power management on an integrated circuit. MTK-1008, 2:18-22 (“Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips...as to minimize overall power consumption.”); MTK-1004, 1441 (“A PowerPC system-on-a-chip processor...adapt[s] to the dynamically changing performance demands and power consumption constraints[.]”); MTK-1003, ¶240. Further, Nicol and Nowka address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1005, 1:24-30 (describing the direct relationship between performance and power consumption), MTK-1004, 1441 (“While [devices’] peak performance demands tend to be significant, they are also highly power constrained.”); MTK-1003, ¶240. Both teach dynamically varying certain parameters like frequency and voltage to control the power consumption. MTK-1008, 2:11-14, 3:24-27; MTK-1004, 1442 (“DVS systems *adjust the supply voltage dynamically* to meet the performance demands while minimizing power

consumption.”), 1444 (“*Adjustment to the output clock frequency* can be done on-the-fly by modifying the output clock divider through a write to a control register.”); MTK-1003, ¶241.

Because Nicol and Nowka provide similar solutions to a similar problem within the same field of endeavor, and Nowka provides a physical implementation of the power-management scheme of Nicol, a POSITA would have naturally looked at, and been motivated to combine, the two references when selecting a method for Nicol’s voltage-changing solution. For example, Nicol does not explicitly disclose standby modes. A POSITA would have been motivated to incorporate Nowka’s standby modes in Nicol because such modes were known to eliminate unnecessary standby power. MTK-1008, 3:4-7 (“[T]ypically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption.”); MTK-1004, 1446 (“Several modes of standby operation are employed to achieve a range of standby power levels.”); MTK-1003, ¶242.

Similarly, a POSITA would have been motivated to incorporate Nowka’s PLL circuitry in Nicol’s PLL to improve the resolution of the varying frequency, and to allow for glitchless frequency switching, clock freezing for hibernation modes, and selecting alternative clock sources for extremely low-frequency operation. MTK-1008, 4:17-22 (“[T]he programmable-frequency clock is

generated using an appropriately multiplied input reference clock (line 101) via a phase lock loop frequency synthesizer circuit 110 which has a high resolution, e.g., can be altered in increments of 5 MHz.”), MTK-1004, 1444; MTK-1003, ¶243.

3. Claim 6

The Nicol-Nowka combination renders obvious selecting a clock. Nowka discloses that the “output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock as the processor clock source to allow for extremely low frequency operation.” MTK-1004, 1444; MTK-1003, ¶244. A POSITA would have been motivated to implement such a clock-selecting technique in Nicol to enhance the ability to quickly switch between clock frequencies for a given PE or power island, and to allow for alternative clock sources for extremely low-frequency operation. MTK-1003, ¶245. This modification is simply the application of a known technique (clock selection) to improve a similar device (Nicol’s PLL) in the same way (to provide means for selecting various frequencies). MTK-1003, ¶245.

4. Claim 10

The Nicol-Nowka combination renders obvious powering on a power island. Nowka discloses “hibernation” and “cyro” modes where “the logic supply to the processor, caches and the SOC core is disconnected.” MTK-1004, 1446; *see also* MTK-1004, 1442 (“the supervisor requests shutdown of the logic supply during

hibernation”); MTK-1003, ¶246. When exiting hibernation or cryo mode, the SOC “restores the [logic] supply” to power on the power island and restore functionality. MTK-1004, 1446; MTK-1003, ¶246. Accordingly, a POSITA would have understood that coming out of Hibernation or Cryo mode entails powering on the power island for normal operation of the system. MTK-1003, ¶246.

A POSITA would have been motivated to incorporate Nowka’s standby modes into Nicol, and with it, powering on a power island, to minimize unnecessary power consumption. MTK-1008, 2:8-10, 3:4-7; MTK-1003, ¶247. Further, Nicol discloses controlling operating voltages with “significantly greater than on/off granularity,” demonstrating that turning a component on and off was well-known and widely implemented in the art. MTK-1008, Abstract, 2:18-31; MTK-1003, ¶247.

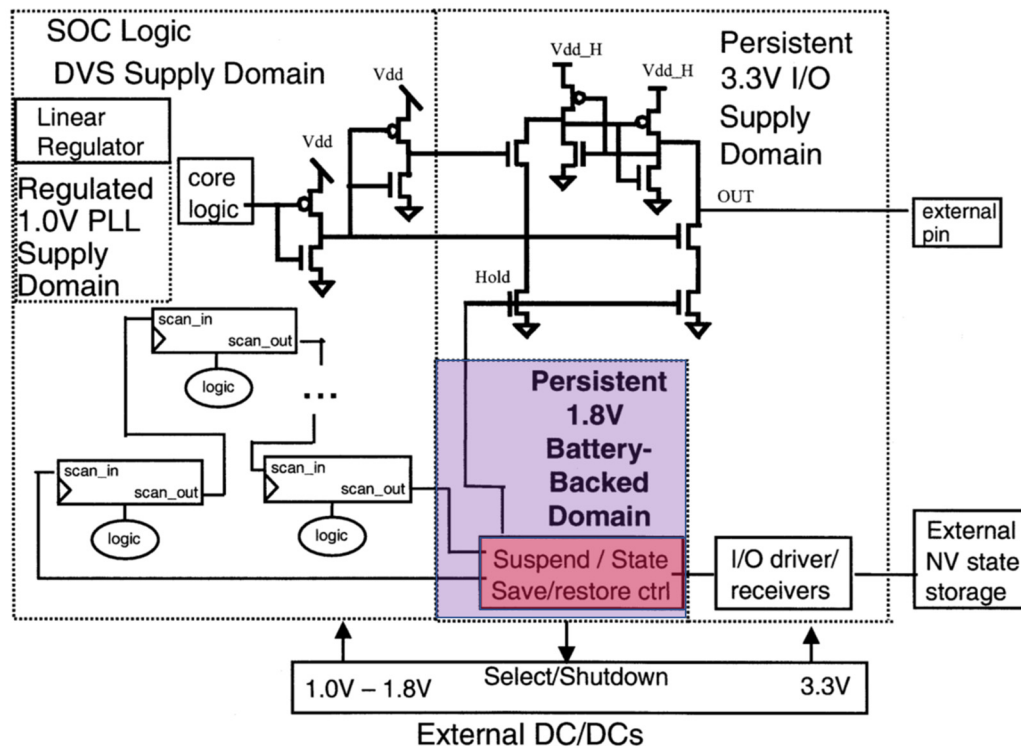
5. Claim 12

The Nicol-Nowka combination renders obvious changing one of the power islands to a sleep mode. Nowka discloses “sleep and hibernation modes” to “minimize standby power consumption,” similar to the ’306 Patent’s “low power modes such as sleep, nap, and full power down.” MTK-1004, 1442, 1446; MTK-1001, 7:26-27; MTK-1003, ¶248. A POSITA would have been motivated to incorporate Nowka’s standby modes in Nicol to “reduce the average power

consumption” while PEs or groups of PEs (power islands in Nicol) are on standby, or not needed. MTK-1008, 3:4-7; MTK-1003, ¶249. Such modes were a well-known solution in the art, and incorporation into Nicol would have been no more than a combination of familiar elements according to known methods to yield predictable results (minimize leakage current and unnecessary power consumption). MTK-1003, ¶250.

6. Claim 14

The Nicol-Nowka combination renders obvious saving a state of components within one of the power islands. Nowka discloses that in “Cryo mode,” “[t]he suspend controller stops the clocks, freezes the I/O drivers, *scans the register state* out through the IIC interface to nonvolatile storage, removes logic power[.]” MTK-1004, 1446; MTK-1003, ¶251. Therefore, Nowka discloses saving the state of the latches and register arrays, which are components in the logic domain. MTK-1003, ¶251. Figure 3 shows a block labeled “Save/restore ctrl” (highlighted in red) within the variable voltage power domain, which a POSITA would have understood to facilitate the saving a state of components. MTK-1003, ¶251.



MTK-1004, Fig. 3.

A POSITA would have been motivated to incorporate Nowka's state-saving mechanism in Nicol because such a solution allows for efficient restoration of the component state after the power island (PE or group of PEs) have been in standby mode. MTK-1003, ¶252.

7. Claim 15

The Nicol-Nowka combination renders obvious restoring a state of components within one of the power islands. After entering "Cryo mode," the suspend controller "waits for a wakeup event at which time it restores the supply, *restores the state* and restart the clocks" for components in the variable voltage power domain. MTK-1004, 1446; MTK-1003, ¶253.

In incorporating Nowka into Nicol, a POSITA would have been motivated to allow the system to restore a state of systems (*i.e.*, of the PE or group of PEs that was placed in standby mode). MTK-1003, ¶254. Such a technique was known to improve wake-up time and hence energy efficiency and performance. MTK-1003, ¶254.

8. Claim 21

Supra Ground 2B, claim 6. MTK-1003, ¶255.

9. Claim 25

Supra Ground 2B, claim 10. MTK-1003, ¶256.

10. Claim 27

Supra Ground 2B, claim 12. MTK-1003, ¶257.

11. Claim 29

Supra Ground 2B, claim 14. MTK-1003, ¶258.

12. Claim 30

Supra Ground 2B, claim 15. MTK-1003, ¶259.

13. Claim 34

The Nicol-Nowka combination renders obvious clock multiplexing circuitry. Nowka discloses an “output multiplexor” in its PLL that “allows for clock freezing for sleep and hibernation modes. The output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock.” MTK-1004, 1444; MTK-1003, ¶260.

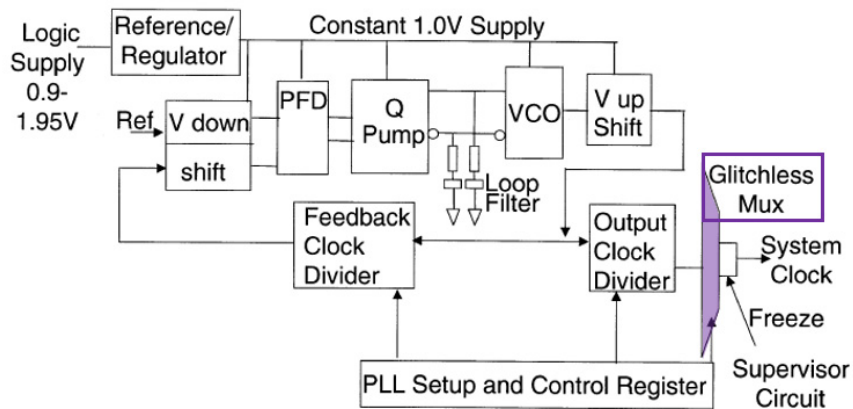


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

MTK-1004, Fig. 7.

In incorporating Nowka into Nicol, a POSITA would have found it obvious to incorporate clock multiplexing circuitry into Nicol's PLL to allow for seamless selection of frequency in Nicol's dynamic frequency scaling, as well as to allow for selecting from alternative clock sources. MTK-1008, 4:17-27, Figs. 2, 4; MTK-1003, ¶261. Multiplexing was conventional and well-known in the art, and this circuitry would have required only the application of routine engineering skills and design principles to implement. MTK-1003, ¶261.

14. Claim 46

Supra Ground 2B, claim 10. MTK-1003, ¶262.

15. Claim 48

Supra Ground 2B, claim 12. MTK-1003, ¶263.

16. Claim 50

Supra Ground 2B, claim 14. MTK-1003, ¶264.

17. Claim 51

Supra Ground 2B, claim 15. MTK-1003, ¶265.

F. GROUND 2C—Claims 13, 28, and 49 are obvious over Nicol and Borkar

1. Overview of Borkar

Supra Ground 1B, Overview of Borkar. MTK-1003, ¶267.

2. Nicol-Borkar Combination

A POSITA would have been motivated to modify Nicol’s integrated circuit to incorporate the teachings of Borkar with reasonable expectation of success.

Nicol and Borkar are in the same field of endeavor: power management on an integrated circuit. Nicol relates to “electronic circuits and, more particularly to power consumption within electronic circuits.” MTK-1008, Abstract, 1:6-7

Similarly, Borkar describes “control circuitry [that] controls a setting of a body bias signal...to at least partially control a parameter of the processor.... Examples of the parameters include performance, power consumption, and temperature.”

MTK-1006, 1:60-2:3.

Further, Nicol and Borkar address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1008, 2:65-3:9 (discussing how power consumption and performance should match the load in order to optimize power savings), MTK-1006, 1:20-21 (“The performance, power consumption, and temperature [of an integrated circuit] are typically

related.”), 5:45-46 (“The user may specify certain power conditions or a power versus performance tradeoff.”); MTK-1003, ¶270. Both Nicol and Borkar also suggest the solution of dynamically controlling variables such as frequency and voltage in response to changing needs and operations. MTK-1008, 4:64-66 (“The reduced load permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V.”), 5:66-6:2; MTK-1006, 5:25-29 (“In some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors.”), 2:52-54; MTK-1003, ¶271.

The similarities across Nicol and Borkar’s disclosures would have led a POSITA to incorporate Borkar’s teachings in Nicol’s dynamic power management. For example, Nicol discusses the need to adjust to temperature variations “to achieve high performance at varying operating temperatures and process corners,” and existing systems that “use[] an on-chip temperature sensor and associated processing circuitry” to respond to variations in temperature. MTK-1008, 1:41-48; *see also* MTK-1008, 1:65-67 (“Researchers have been also experimenting with on-chip voltage scaling techniques to counter process and temperature variations.”). A POSITA would have understood that the discussion of temperature variation is closely related to the need to monitor power consumption because, as Borkar

teaches, “performance, power consumption, and temperature are typically related.” MTK-1006, 1:19-20. MTK-1003, ¶272. A POSITA would have understood that Borkar’s power consumption monitoring mechanism would provide an additional check on the adverse effects of high power consumption (which causes high temperature) on performance that Nicol discusses. MTK-1003, ¶272.

3. Claim 13

The Nicol-Borkar combination renders obvious monitoring the power consumption level, determining whether a threshold level was crossed based on the power consumption level, and performing another action based on the crossing of the threshold level. Borkar discloses numerous embodiments (depicted in Figures 1-2, 4, 7) that explicitly show “current detection circuitry” which provide current signals to “voltage and frequency control circuitry.” MTK-1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7 (Figs. 1, 7 shown below); MTK-1003, ¶273. Control circuitry “may *consider the current signal (which when multiplied by the supply voltage indicates the active power consumption)* in deciding how to control the settings.” MTK-1006, 4:64-67. Borkar explains that “detect[ing] current being consumed” is a precise way of tracking power consumption levels. MTK-1006, 13:6-7; MTK-1003, ¶274. Because current multiplied by supply voltage is power consumption, Borkar’s system is able to monitor power consumption by monitoring current signal. MTK-1006, 4:64-67, 13:7-8. By calculating the power

consumption in this way, the system can monitor the power consumption and take appropriate actions, such as changing body bias, supply voltage, and clock frequencies, to prevent power consumption from crossing a certain level. MTK-1006, 6:1-7, 13:4-7; MTK-1003, ¶274.

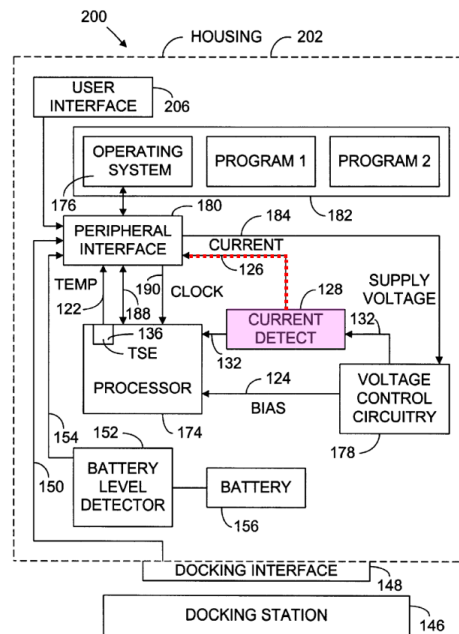


FIG. 4

MTK-1006, Fig. 4.

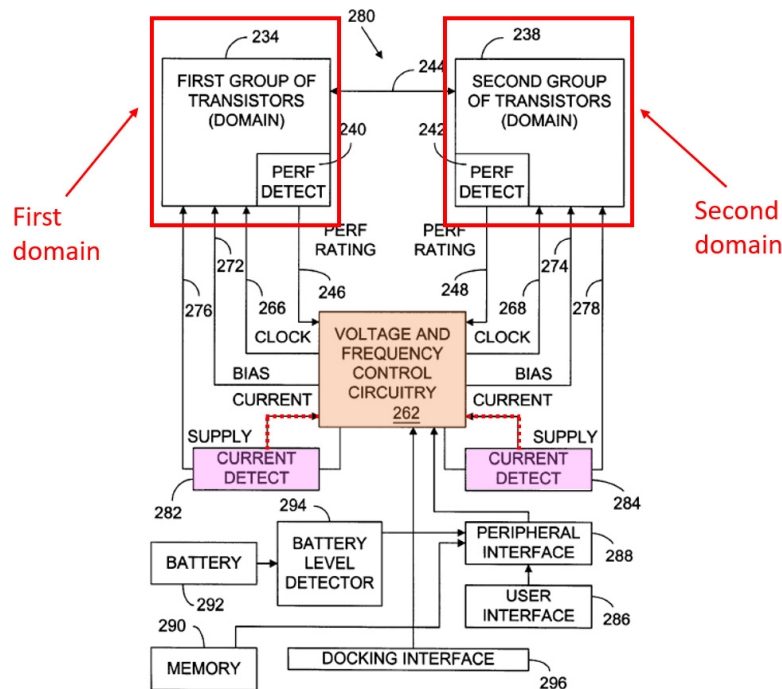


FIG. 7

MTK-1006, Fig. 7.

A POSITA would have been motivated to implement Borkar's power consumption monitoring in Nicol to achieve more precise and predictable power consumption control. Whereas Nicol changes operating parameters based primarily on the most efficient division of the application at hand, incorporating power monitoring from Borkar would allow Nicol's system to further respond to excessive power consumption levels, similar to Nicol's disclosure that "the operating system can reduce the supply voltage even further by tracking temperature and process variations." MTK-1008, 4:11-13; MTK-1003, ¶275. A POSITA would have needed only routine electrical and computer engineering principles to implement Borkar's monitoring and threshold-comparing mechanism

in Nicol, as demonstrated by Borkar's implementation in a system directly analogous to Nicol's IC. MTK-1006, 2:49-52 ("The invention involves changing body bias signals applied to transistors in an integrated circuit in response to changing conditions to at least partially control a parameter of the integrated circuit."); MTK-1003, ¶276.

4. Claim 28

Supra Ground 2C, claim 13. MTK-1003, ¶277.

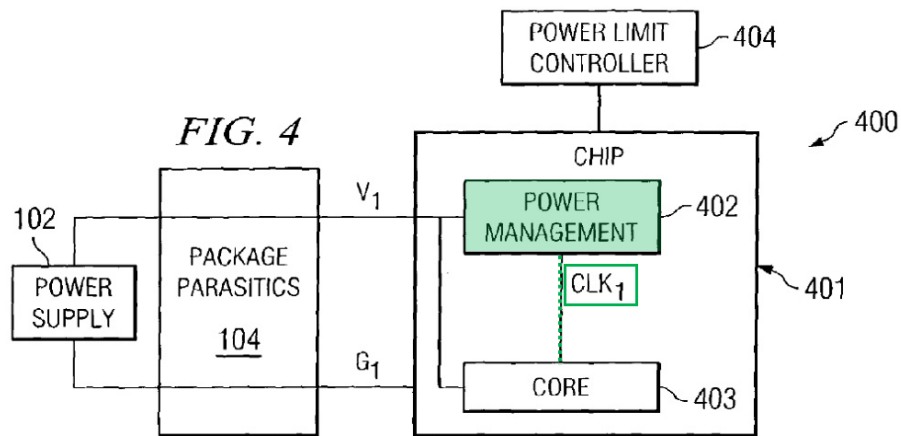
5. Claim 49

Supra Ground 2C, claim 13. MTK-1003, ¶278.

G. GROUND 2D—Claim 35 is obvious over Nicol and Naffziger

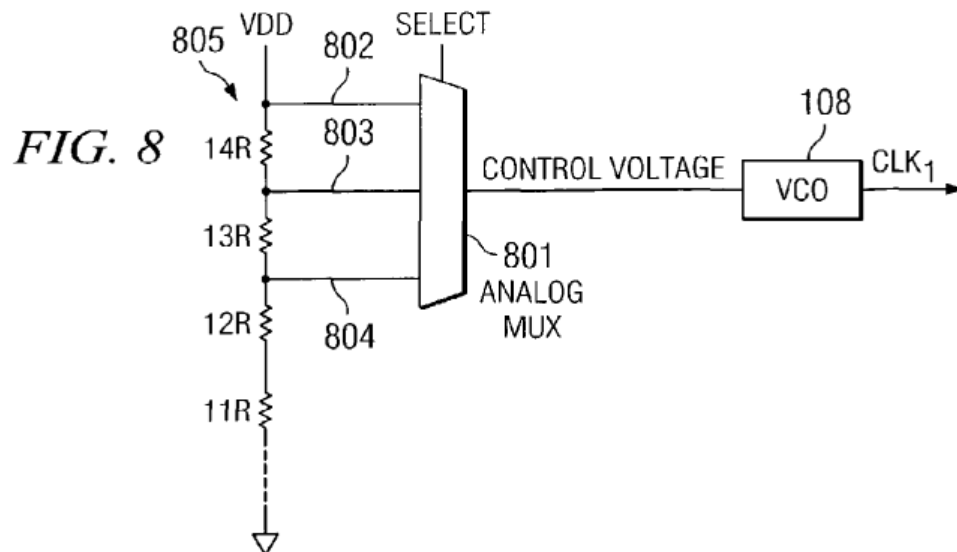
1. Overview of Naffziger

Naffziger relates to an integrated circuit with a dynamically variable power limit. MTK-1015, Abstract. Naffziger's system is "capable of having its power limit dynamically varied to any of a plurality of different values. Preferably, the chip is implemented in a manner that enables any of a plurality of different measured power limits to be dynamically set for the chip." MTK-1015, 5:32-36. Naffziger includes a "power management" logic for self-regulating power consumption. MTK-1015, 11:50-51. The power management logic comprises a voltage controlled frequency oscillator that generates a clock signal for the core chip circuitry. MTK-1015, 11:52-61.



MTK-1015, Fig. 4.

Naffziger's power management logic includes a voltage multiplexor in conjunction with a resistor divider to produce multiple voltages, which in turn allows variable clock frequency output from the VCO. MTK-1015, 19:30-64; MTK-1003, ¶280. Figure 8 shows an example of resistor divider combined with a multiplexor to enable selecting from different control voltage levels.



MTK-1007, Fig. 8.

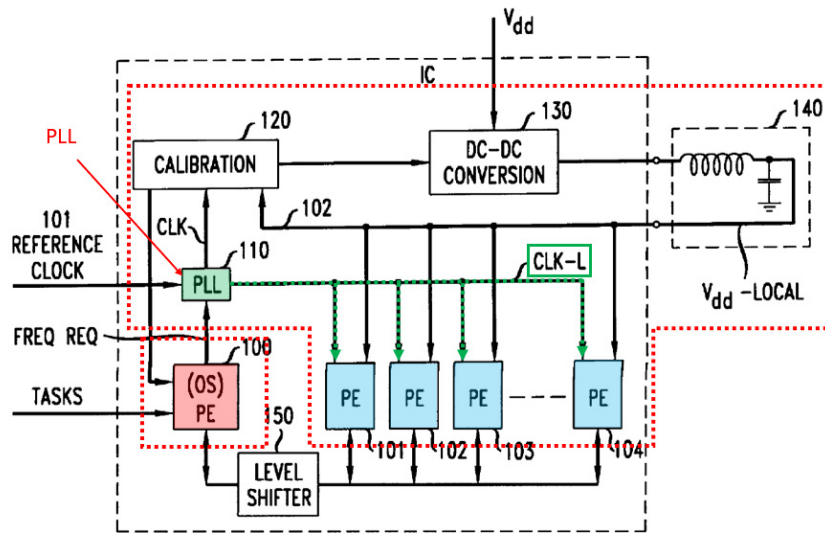
2. Nicol-Naffziger Combination

A POSITA would have been motivated to modify Nicol's integrated circuit to incorporate the teachings of Naffziger with reasonable expectation of success. Nicol and Naffziger are in the same field of endeavor: power management on an integrated circuit. MTK-1008, 2:18-22 ("Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips...as to minimize overall power consumption."); MTK-1015, 1:19-20 ("This invention relates in general to management of power consumption by an integrated circuit[.]"); MTK-1003, ¶283.

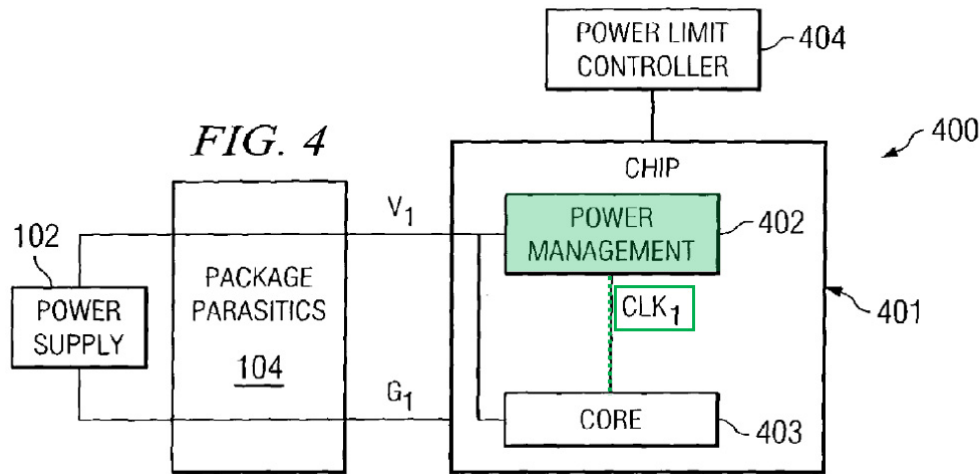
Further, Nicol and Naffziger address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1008, 2:65-3:9 (discussing how power consumption and performance should match the load in order to optimize power savings), 3:4-6; MTK-1015, 1:33-39 ("...chip designers are faced with the difficult task of designing chips that achieve the desired performance (e.g., fast processing speed), while managing the power consumption of the chips."), 6:15-20; MTK-1003, ¶284. Both Nicol and Naffziger address that problem with the identified, predictable solution of dynamically controlling the power in real-time in response to changing needs and operations. MTK-1008, 2:18-22 ("Improved performance of multi-processor chips is achieved

by dynamically controlling the processing load of chips”); MTK-1015, 4:10-19 (“The integrated circuit...dynamically set[s] the clock signal to a determined frequency value for managing power of the integrated circuit to comply with the dynamically set power limit value.”), Fig. 3; MTK-1003, ¶285. Both Nicol and Naffziger teach changing variables such as frequency and voltage to change the power level. MTK-1008, 1:26-28 (“The power consumption of a CMOS circuit increases linearly with operating frequency and quadratically with supply voltage.”), 2:11-14, 3:24-27; MTK-1015, 1:56-60 (“By reducing the chip’s operating point to a lower voltage and lower frequency, the chip’s power consumption will be reduced to some degree below that consumed at the higher operating point (recall $P=C*V^2*F$).”), 6:49-51 (“For example, the chip’s **voltage** and **frequency** are preferably dynamically varied to provide optimum performance within a set power limit[.]”); MTK-1003, ¶286. To this end, Naffziger shows a “power management” block which outputs a clock to the core. MTK-1015, 11:50-53. A POSITA would have recognized that this “power management” block is performing the same function as the PLL in Nicol, which outputs a clock frequency to the PEs. However, Naffziger provides more detail on the circuitry in the power management block, so a POSITA would have naturally combined the teachings of Naffziger, which discloses similar power management mechanisms as Nicol, in Nicol with reasonable expectation of success. MTK-1003, ¶¶286-287.

FIG. 2



MTK-1008, Fig. 2.

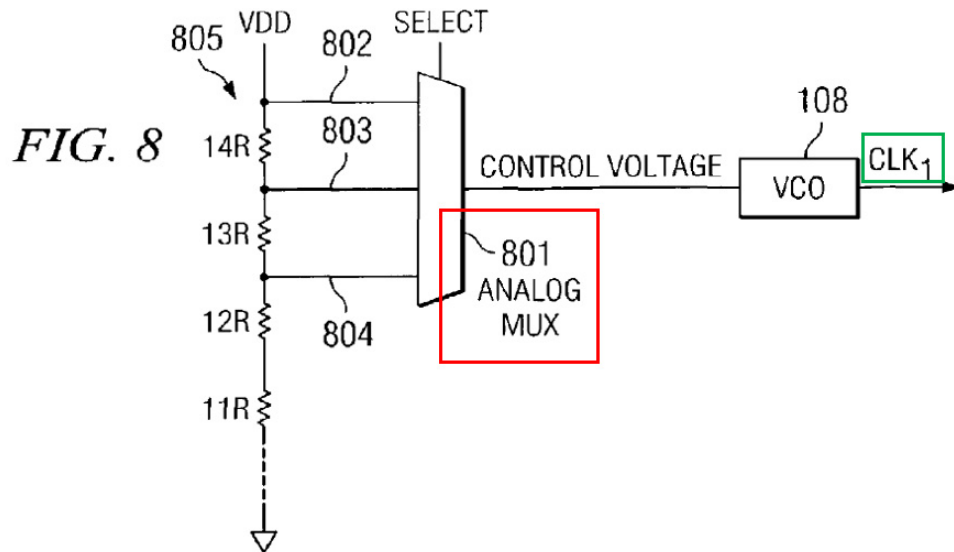


MTK-1015, Fig. 4.

3. Claim 35

The Nicol-Naffziger combination renders obvious voltage multiplexing circuitry. Naffziger discloses a voltage multiplexor that allows choosing between various voltage levels for its VCO. MTK-1015, 19:43-62, Fig. 8; MTK-1003,

¶288. Changing the control voltage for the VCO in turn changes the frequency of clock signal CLK₁.



MTK-1007, Fig. 8.

A POSITA would have been motivated to integrate Naffziger's multiplexer in Nicol to provide an efficient method for adaptively changing the voltage input to the VCO, which in turn allows for varying the clock signal frequency. Such a modification would have been a straightforward implementation of a known technique (PLL with a VCO, which incorporates voltage multiplexing) to implement the frequency-switching ability in Nicol's system. MTK-1003 ¶289.

IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION

A. Discretionary denial under §325(d) is not warranted

Advanced Bionics and the *Becton* factors strongly favor institution.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential); *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph).

Advanced Bionics Part 1—The references relied upon here were not cited by the examiner during prosecution, and are not listed on the face of the '306 Patent. *See generally* MTK-1001, MTK-1002. Thus, there is no indication that the examiner substantively considered the references raised in this Petition, and therefore, the Petition's art and arguments cannot be said to be the same as, or substantially similar to, art and arguments previously presented to the Office in connection with the '306 Patent. *Id.* Accordingly, neither condition of the first prong of the *Advanced Bionics* framework is met.

Becton factors [a], [b], and [d] further counsel in favor of institution. None of Nowka, Nicol, Borkar, Boerstler, or Naffziger were addressed during prosecution (factor [a]), nor are they cumulative of other art relied on or considered by the examiner (factor [b]). *Id.* There are also no overlapping arguments (factor

[d]) between the prosecution record and the Grounds above. Thus, *Becton* factors [a], [b], and [d] favor Petitioner.

Advanced Bionics Part 2—The Board need not reach the second prong to resolve against discretionary denial under Section 325(d), since the first prong is not satisfied. *See Oticon Med. AB et. al. v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019) (precedential) (no discretionary denial under Section 325(d) because of “new, noncumulative prior art asserted in the Petition”). Nonetheless, each of *Becton* factors [c], [e], and [f] favors Petitioner. None of Nowka, Nicol, Borkar, Boerstler, or Naffziger was cited during prosecution, and thus did not form the basis of any rejection (factor [c]). As for factors [e] and [f], by not considering Nowka, Nicol, Borkar, Boerstler, or Naffziger, or combinations based on them, the Office erred in its evaluation of the prior art, thus warranting reconsideration. *Advanced Bionics*, Paper 6, 10. The Grounds above demonstrate why further consideration is warranted.

B. Discretionary Denial under Section 314(a) Is Not Warranted

Given this is the first ever petition to be filed against the '306 Patent, the *General Plastic* factors do not apply. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 (PTAB Sept. 6, 2017) (precedential)

C. The *Fintiv* Factors Weigh Against Exercising Discretion To Deny Institution

The PTAB considers a set of non-exclusive factors (the *Fintiv* factors) in determining whether to institute an IPR proceeding where there is parallel district court litigation. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020). On June 21, 2022, Director Vidal issued “binding agency guidance” entitled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation.” MTK-1013 (hereinafter the “Interim Guidance”). This Interim Guidance presents “several clarifications... to the PTAB’s... application of *Fintiv* to discretionary institution where there is parallel litigation.” *Id.*, 2.

One clarification provided by the Interim Guidance specifies the effect of particular types of stipulations presented by petitioners on the Board’s application of the *Fintiv* framework. *Id.*, 3, 7-8. In particular, the Interim Guidance unequivocally states that “***the PTAB will not discretionarily deny institution*** of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” *Id.*, 7 (emphasis added) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020)). In the present case, Petitioner presents a

stipulation not to pursue in the parallel district court proceeding the same grounds as in the present Petition or any grounds that could have reasonably been raised in the present Petition. *See* MTK-1014. Accordingly, based on the Interim Guidance, institution of the present Petition ***should not*** be discretionarily denied in view of the parallel district court proceeding. *See* MTK-1013, 7.

V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

MediaTek Inc. is petitioner and real party-in-interest. MediaTek USA Inc. is an additional real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers or reexamination certificates regarding the '306 Patent. MOSAID—the alleged Patent Owner—filed a complaint asserting the '306 Patent against Petitioner on March 28, 2023 in the U.S. District Court for the Eastern District of Texas (Civil Action No. 2:23-CV-

00129-JRG). The '306 Patent was asserted in five district court infringement actions (*Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case. No. 6:11-cv-00173 (Apr. 8, 2011, E.D. Tex.); *Conversant Intellectual Property Management Inc. v. STMicroelectronics, Inc.*, Case No. 6:12-cv-00848 (Nov. 5, 2012) (E.D. Tex.); *MOSAID Technologies Inc. v. Xilinx, Inc.*, Case. No. 6:12-cv-00847 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. NXP Semiconductors USA, Inc.*, Case. No. 6:12-cv-00844 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. ST-Ericsson, Inc.*, Case. No. 6:12-cv-00845 (Nov. 5, 2012, E.D. Tex.)) and subject to one declaratory judgment action (*ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 3:11-cv-03869 (Aug. 5, 2011, N.D. Cal.), transferred to *ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 6:12-cv-00008 (Jan. 9, 2012, E.D. Tex), which were all voluntarily dismissed based on settlement.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
Timothy W. Riffe, Reg. No. 43,881 Fish & Richardson P.C. 60 South Sixth Street Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR44508-0023IP1@fr.com	Joseph Colaianni, Reg. No. 39,948 Linhong Zhang, Reg. No. 64,749 Jared M. Hartzman, Reg. No. 70,255 Tim Rawson, Reg. No. 70,316 60 South Sixth Street Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 IPR44508-0023IP1@fr.com

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR44508-0023IP1@fr.com.

Respectfully submitted,

Dated: March 6, 2024

/Timothy W. Riffe/

Timothy W. Riffe, Reg. No. 43,881
Fish & Richardson P.C.
60 South Sixth Street
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2024-00598)

Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,779 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: March 6, 2024

/Timothy W. Riffe/

Timothy W. Riffe, Reg. No. 43,881

Fish & Richardson P.C.

60 South Sixth Street

Minneapolis, MN 55402

T: 202-783-5070

F: 877-769-7945

Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on March 6, 2024, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
55 Old Bedford Rd., Suite 200
LINCOLN, MA 01773
(978) 341-0036

/Crena Pacheco/
Crena Pacheco
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
pacheco@fr.com