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Paper 12
Date: September 26, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

IPR2024-00598
Patent 7,051,306 B2

Before KEN B. BARRETT, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges.*

ROESEL, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

MediaTek Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 1–51 of U.S. Patent No. 7,051,306 B2 (Ex. 1001, "the '306 Patent"). MOSAID Technologies, Inc. ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). For the reasons discussed below, we determine that the reasonable likelihood standard is met, and we institute *inter partes* review.

II. BACKGROUND

A. Related Matter

The parties identify the following district court action involving the '306 Patent: *MOSAID Technologies Inc. v. MediaTek, Inc.*, No. 2:23-cv-00129-JRG (E.D. Tex.) (hereinafter, "the related litigation"). Pet. 95–96; Paper 8, 1 (Patent Owner's updated mandatory notices).

A. The '306 Patent (Ex. 1001)

The '306 Patent is titled "Managing Power on Integrated Circuits Using Power Islands" and was issued based on a regular application filed May 7, 2004 and a provisional application filed May 7, 2003. Ex. 1001, codes (22), (54), (60). According to the '306 Patent, "[o]ne design goal for integrated circuits is to reduce power consumption." *Id.* at 1:19–20.

The ’306 Patent states, “[s]ome prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption,” but “[o]ne problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static” and “do not dynamically change based on the needs and operation of the integrated circuit.” *Id.* at 2:10–16.

Figure 2 of the ’306 Patent is reproduced below.

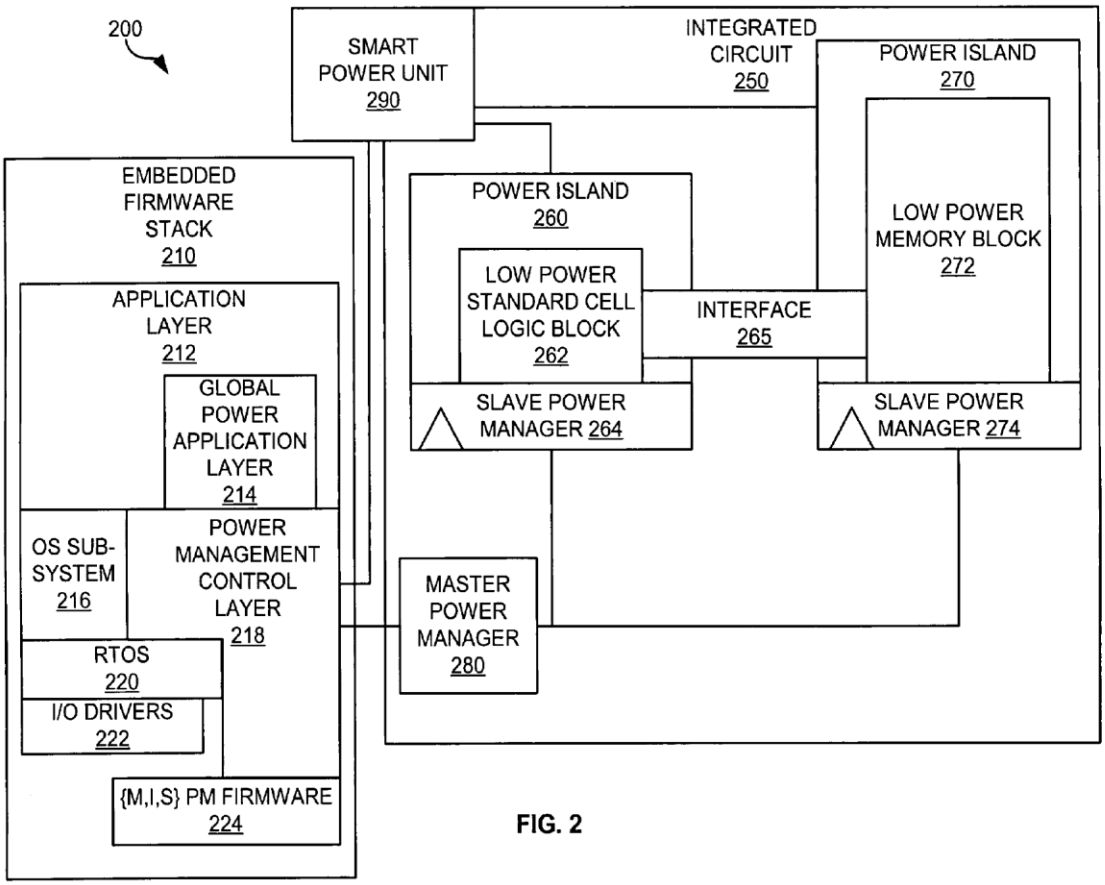

FIG. 2

Figure 2 shows a system for managing power in integrated circuit 250. Ex. 1001, 2:53–55, 4:56–58. The system includes embedded firmware stack 210, which runs on a central processing unit (CPU) and includes application layer 212 and power management control layer (PMCL) 218. *Id.* at 4:58–65. Integrated circuit 250 includes power islands 260 and 270,

master power manager (MPM) 280, and smart power unit (SPU) 290. *Id.* at 5:1–2, 5:36–40, Fig. 2; *see also id.* at 4:33–37 (explaining acronyms). Power island 260 includes slave power manager (SPM) 264, and power island 270 includes SPM 274. *Id.* at 5:2–7.

According to the ’306 Patent, the integrated circuit may be a system-on-a-chip that includes “multiple IP units, which are blocks of circuitry performing specific functions.” *Id.* at 2:3–6, 3:42–44. The ’306 Patent explains that “power islands may be delineated based on geographic factors or functional circuitry” and a power island is “any section, delineation, partition, or division of the integrated circuit” within which “power consumption is controlled.” Ex. 1001, 2:32–33, 3:51–59.

Figure 5 of the ’306 Patent is reproduced below.

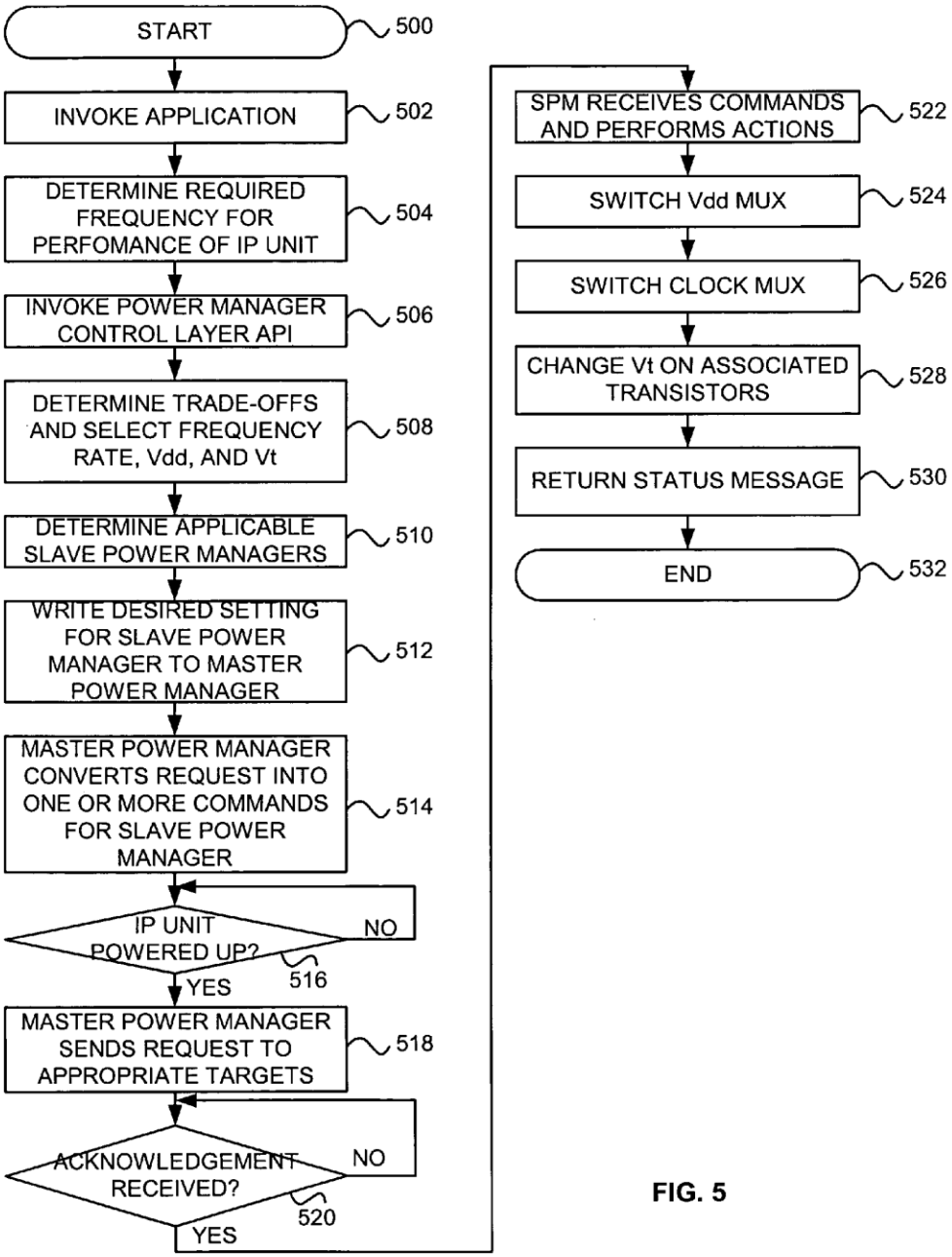

FIG. 5

Figure 5 is a flowchart from an application request to an SPM action. Ex.1001, 2:61–63, 7:39–41. In step 502, an application is invoked, such as playing a movie. *Id.* at 7:41–42. In step 504, the application determines the required frequency for performance of an IP unit, for example, a specified frequency for an IP unit for an MPEG decoder. *Id.* at 7:42–46. In step 506, the application invokes PMCL 218 application program interface (API) call.

Id. at 7:51–52; *see also* 5:11–14 (explaining acronym). In step 508, PMCL 218 determines possible trade-offs available for the IP unit and selects a frequency rate, Vdd, and Vt that best meets the given requirements and, in step 510, determines the applicable SPMs 264 and 274. *Id.* at 7:62–66.[1] In step 512, PMCL 218 writes the selected settings for SPMs 264 and 274 to MPM 280, which converts the settings into commands (step 514) and sends them to SPMs 264 and 274 (step 518). *Id.* at 8:4–18, Fig. 5. In steps 522 to 528, SPM 264 performs the commanded actions by, e.g., switching a Vdd mux, switching a clock mux, or changing the Vt on the associated transistors. *Id.* at 8:23–29, Fig. 5.

Figure 8 of the ’306 Patent is a flowchart from an application request to an SPU action. Ex. 1001, 3:1–3, 8:56–58. Steps 802 to 810 are similar to steps 502 to 510 of Figure 5. *Compare id.* at 7:41–66, Fig. 5 (steps 502 to 510), *with id.* at 8:56–9:8, Fig. 8 (steps 802 to 810).

B. Illustrative Claim

Petitioner challenges all 51 claims of the ’306 Patent, of which claims 1, 16, and 37 are independent. Claim 1 is reproduced below:

> 1. A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:
>
> [1a] determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;
>
> [1b] determining at least one of actions to change a power consumption level of the one of the power islands to the target power level; and

[1] “Vdd” refers to “dynamic voltage source” (Ex. 1001, 4:51–55), and “Vt” refers to threshold voltage (*id.* at 7:1–3).

> [1c] performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

Ex. 1001, 13:33–47 (bracketed designations added to correspond with Petitioner's identification of claim elements). Claims 16 and 37 are directed to a system and software product, respectively, and contain recitations similar to claim 1. *Id.* at 14:19–34, 15:21–38.

C. Asserted Challenges and Evidence

Petitioner raises the following challenges to patentability.

Claim(s) Challenged	35 U.S.C. §[2]	References/Basis
1–8, 10–12, 14–23, 25–27, 29–34, 36–44, 46–48, 50, 51	103	Nowka[3]
9, 13, 24, 28, 45, 49	103	Nowka, Borkar[4]
35	103	Nowka, Boerstler[5]

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112–29, amended §§ 102 and 103 of Title 35, effective March 16, 2013. Because the filing date of the '306 Patent is before this date, we refer to the pre-AIA versions of §§ 102 and 103. Ex. 1001, code (22).

[3] Ex. 1004, *A 32-bit Power PC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling*, IEEE J. of Solid-State Circuits, Vol. 37, No. 11, November 2002 ("Nowka"). Petitioner contends that Nowka is prior art under § 102(a). Pet. 2.

[4] Ex. 1006, US 6,484,265 B2, issued November 19, 2002 ("Borkar"). Petitioner contends that Borkar is prior art under § 102(e). Pet. 2.

[5] Ex. 1007, US 6,353,369 B1, issued March 5, 2002 ("Boerstler"). Petitioner contends that Boerstler is prior art under § 102(b). Pet. 2.

Claim(s) Challenged	35 U.S.C. §[2]	References/Basis
1–5, 7–9, 11, 16–20, 22–24, 26, 31–33, 36–45, 47	103	Nicol[6]
6, 10, 12, 14, 15, 21, 25, 27, 29, 30, 34, 46, 48, 50, 51	103	Nicol, Nowka
13, 28, 49	103	Nicol, Borkar
35	103	Nicol, Naffziger[7]

Pet. 1–2. Petitioner submits the Declaration of Tajana Rosing, Ph.D. Ex. 1003.

III. ANALYSIS

A. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

[6] Ex. 1008, US 6,141,762, issued October 31, 2000 ("Nicol"). Petitioner contends that Nicol is prior art under § 102(b). Pet. 2.

[7] Ex. 1015, US 8,086,884 B2, filed December 16, 2002 and issued December 11, 2011 ("Naffziger"). Petitioner contends that Naffziger is prior art under § 102(e). Pet. 2.

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")). Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements," but "must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

At this stage of the proceeding, there is no dispute about the level of ordinary skill in the art. Based on the testimony of Petitioner's declarant, we determine that a person of ordinary skill in the art ("POSITA") would have had a bachelor of science degree in electrical engineering, computer

engineering, computer science, or a related field, and two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. Ex. 1003 ¶ 21. We find that the level of ordinary skill in the art, as articulated above, is consistent with the level of technical understanding and competence reflected in the ’306 Patent Specification and the asserted prior art references.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Below we address the meaning of the phrase, “based on needs and operation of the integrated circuit.” There are no other claim construction disputes at this stage of the proceeding.

"based on needs and operation of the integrated circuit"

The phrase "based on needs and operation of the integrated circuit" appears identically in independent claims 1, 16, and 37. Ex. 1001, 13:37–38, 14:26–27, 15:26–27.

Petitioner contends that no construction is necessary "because the plain and ordinary meaning suffices." Pet. 14. Petitioner acknowledges that, in prior district court litigations involving the '306 Patent, the parties agreed to the construction, "based on future operational needs and current operating status of the integrated circuit." *Id.* (citing Exs. 1011, 1012).[8] When analyzing the prior art, Petitioner applies each of these constructions. *See, e.g.*, Pet. 10–14 (plain and ordinary meaning); Pet. 14–15 (construction agreed to in prior district court litigations).

After the filing of the Petition and before the filing of the Preliminary Response, the parties filed a joint claim construction statement in the related litigation agreeing that, "based on needs and operation of the integrated circuit" in claims 1, 16, and 37 of the '306 Patent should be construed as "based on future operational needs and current operating status of the integrated circuit." Ex. 2004, 2; Prelim. Resp. 3–4. The agreed construction is reproduced in Appendix A of the district court's claim construction order. Ex. 2005, 8, 26 (filed after the Preliminary Response). Patent Owner argues that the Board should apply this construction. Prelim. Resp. 2–10.

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[8] Exhibit 1011 is an April 29, 2013, claim construction order in *Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, No. 6:11-cv-00173 (E.D. Tex.). Ex. 1012 is a January 9, 2015, claim construction order in *Conversant Intellectual Property Management Inc. v. Xilinx, Inc.*, No. 6:12-cv-00847 (E.D. Tex.). Petitioner informs us that these prior litigations were voluntarily dismissed based on settlement. Pet. 5, 96.

After considering the parties' arguments and evidence, we do not adopt Patent Owner's proposed construction. We see no support in the '306 Patent for limiting "needs and operation," as recited in the claims, to "future operational needs and current operating status," as in Patent Owner's proposed construction.

Our analysis begins with the claims themselves. Claim 1 recites "determining a target power level for one of the power islands based on needs and operation of the integrated circuit." Ex. 1001, 13:36–38. Claims 16 and 37 contain similar language. *Id.* at 14:25–27, 15:25–27. We see no support in the claim language for limiting "needs and operation" to "future operational needs and current operating status," as in Patent Owner's proposed construction.

We next turn to the Specification, where the phrase, "needs and operation of the integrated circuit" appears twice. First, when describing prior integrated circuits, the '306 Patent states that "[t]he voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit." Ex. 1001, 2:14–16. Second, when describing an embodiment, the '306 Patent discloses, "The power manager . . . can dynamically change the power consumption of the power islands . . . based on the needs and operation of the integrated circuit . . . . The target power level is a desired, calculated, or specified power consumption of the power islands." *Id.* at 4:28–33. We see no support in these passages for limiting "needs and operation" to "future operational needs and current operating status," as in Patent Owner's proposed construction.

The parties and Dr. Rosing direct us to the '306 Patent's descriptions of Figures 5 and 8 as support for their respective claim construction arguments. Pet. 13–14 (citing Ex. 1001, 7:38–50, 8:56–62, Fig. 5); Prelim.

Resp. 8 (citing Ex. 1001, 7:61–65, 9:4–7); Ex. 1003 ¶ 58 (citing Ex. 1001, 5:31–36, 7:41–48, 7:62–66, 8:56–9:26, Figs. 5, 8). Petitioner contends that "determining a target power level," as recited in the claim, corresponds, for example, to the '306 Patent's description of "setting the target for certain parameters such as frequency or voltage." Pet. 13 (emphasis omitted). According to Petitioner, the '306 Patent does not explain the meaning of the phrase, "based on needs and operation of the integrated circuit," but "provides examples of determining parameters such as required frequency, supply voltage, or threshold voltage, given a particular application." Pet. 14 (citing 7:38–50, 8:56–62).

We agree with Petitioner that the '306 Patent's description of Figures 5 and 8, steps 504 and 804, appears to provide exemplary support for claim 1's recitation of "determining a target power level for one of the power islands based on needs and operation of the integrated circuit" and the corresponding recitations in claims 16 and 37. Ex. 1001, 13:36–38, 14:25–27, 15:25–27. Referring to these steps, the '306 Patent discloses that an application, such as a movie player, determines the required frequency for performance of an IP unit, for example, a specified frequency for an IP unit for an MPEG decoder. *Id.* at 7:41–46, 8:58–62.

Patent Owner does not disagree that the '306 Patent's description of determining a required frequency to run an application is an example of determining a target power level. Prelim. Resp. 8. Instead, Patent Owner tries to show intrinsic record support for its proposed construction by juxtaposing the '306 Patent's descriptions of Figures 5 and 8 (Ex. 1001, 7:61–65, 9:4–7) with the description of Figure 11 (*id.* at 11:34–36). Prelim. Resp. 8. Patent Owner argues that Figures 5 and 8 show consideration of "future operational needs," that Figure 11 shows consideration of "current

operating status," and the Figures collectively "indicat[e] that the determination of a target power level is based upon both what is occurring in the future and how the current power level management might impact that, as well as consideration of current operational status." Prelim. Resp. 8–9. We disagree. Figures 5 and 8 are flowcharts illustrating how target power levels are adjusted based on an application request. Ex. 1001, 2:61–63, 3:1–3, 7:39–8:33, 8:56–9:26. Figure 11, on the other hand, is a flowchart for generating a "hot spot" report based on a current operating parameter (i.e., temperature) and adjusting a target power level based on the report. *Id.* at 3:11–15, 11:31–12:10. According to the '306 Patent, temperature is a proxy for power consumption level, and the IPM monitors the temperature of a power island, checks if it exceeds a threshold, and if so, lowers the frequency. *Id.* at 6:44–50, 11:31-59, Fig. 11. We do not see a connection between the flowcharts of Figures 5 and 8 and the flowchart of Figure 11 sufficient to support Patent Owner's argument. In our view based on the current record, the '306 Patent describes a method for determining a target power level based on *either* the future operational needs *or* the current operating status of the integrated circuit and does not require considering *both* future needs and current status, as argued by Patent Owner.

Moreover, even if the '306 Patent's "exemplary embodiments" did discuss consideration of both "future operational needs" and "current operating status," as Patent Owner argues (Prelim. Resp. 8)—they do not—that would *not* justify importing the limitations "future" and "current" of "exemplary embodiments" into the claim. *Cadence Pharm. Inc. v. Exela PharmSci Inc.*, 780 F.3d 1364, 1369 (Fed. Cir. 2015) (even if "all of the embodiments discussed in the patent" included a specific limitation, it would not be "proper to import from the patent's written description limitations that

are not found in the claims themselves."). Patent Owner points to nothing in the intrinsic evidence that would support a departure from the plain and ordinary meaning of the claims and we decline to depart from that plain and ordinary meaning. *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) ("Absent lexicography or disavowal, we do not depart from the plain meaning of the claims.").

Lastly, we turn to the extrinsic evidence. Exhibits 1011, 1012, 2004, and 2005 show that Patent Owner's proposed construction was agreed to by the parties in three district court litigations. Contrary to Patent Owner's argument (Prelim. Resp. 3–4), the evidence before us does not show that a district court has construed the term, "based on needs and operation of the integrated circuit." Although Patent Owner's proposed construction is recorded as an agreed-upon construction in three district court claim construction orders (Exs. 1011, 1012, 2005), there is no evidence that any court has construed the limitation and arrived at that construction. Furthermore, the two earlier litigations were settled and voluntarily dismissed (*see* Pet. 96), and there is no evidence the agreed-upon construction has been applied in any validity or infringement determination. Exhibits 1011, 1012, 2004, and 2005 provide no reasoning or citations to intrinsic evidence in support of Patent Owner's proposed construction. *See* Pet. 14 (asserting there is no briefing regarding the agreed-upon construction in Exhibits 1011 and 1012). Under these circumstances, we give little weight to the extrinsic evidence showing the construction agreed to by the parties in district court.

For all of the foregoing reasons, we do not adopt Patent Owner's proposed construction for the phrase, "based on needs and operation of the

integrated circuit" and instead apply the plain and ordinary meaning, which does not distinguish between future needs and current operating status.

Our claim construction determination is not final, and the parties are invited to address claim construction in their post-institution briefs to the extent permitted under the Board's rules and precedent.

D. Petitioner's Nowka-led Challenges

Petitioner contends that claims 1–51 are unpatentable as obvious based on Nowka alone or in combination with Borkar or Boerstler. Pet. 6–50. Patent Owner opposes. Prelim. Resp. 10–21, 28–34, 37–38. We begin with an overview of Nowka.

1. Nowka (Ex. 1004)

Nowka is journal article titled, "A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling." Ex. 1004, 1441.[9] Nowka describes a system-on-a-chip (SOC) processor that uses "dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications," such as "Web pads, advanced PDAs, cell phones and small form factor PCs." *Id.* (Abstract, Introduction).

Under the heading, "System Overview," Nowka asserts that the SOC "makes use of active power reduction techniques to dynamically match the power consumption with the requirements of the application." Ex. 1004, 1442 (lefthand column). According to Nowka, "The active power consumption is reduced when resource[] demands are low through the use of

[9] We refer to the original page numbers of Nowka, not those added by Petitioner.

dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating." *Id.*

Under the heading, "Dynamic Voltage Scaling," Nowka states, "The primary means of matching the performance and power consumption of this device to the application is through the use of dynamic voltage scaling (DVS)," which "adjust[s] the supply voltage dynamically to meet the performance demands while minimizing power consumption." Ex. 1004, 1442 (righthand column).

Under the subheading, "Dynamic Voltage Scaling Architecture," Nowka discloses, "To support DVS in this SOC, the power distribution has been divided into four distinct domains," consisting of "two persistent voltage domains, one dynamically voltage-scaled logic domain and one internally derived domain." Ex. 1004, 1442 (righthand column). The four domains are shown in Figure 3, which identifies an "SOC Logic DVS Supply Domain," a "Regulated 1.0V PLL Supply Domain," a "Persistent 3.3V I/O Supply Domain," and a "Persistent 1.8V Battery-Backed Domain." *Id.* at 1443, Fig. 3.

Nowka discusses Figures 5 and 6 under the subheading, "Measured DVS Results." Ex. 1004, 1444 (lefthand column). Figure 5 shows voltage scaling measurements when "the SOC was running the Dhrystone2.1 benchmark under Linux." *Id.* Referring to Figure 5, Nowka reports that, by lowering the supply voltage from a nominal value to 0.85 V, the power consumption was reduced from 570 MW at 333 MHz to 33 mW at 66 MHz, representing "a frequency range of 5:1 with a power range of 17:1." *Id.*; *see also id.* at 1443 (lefthand column; discussing logic supply's "nominal 1.8-V value"). Figure 6 shows voltage scaling measurements when the "device was performing MPEG-4 decoding under Linux." *Id.* at 1444 (lefthand

column). Referring to Figure 6, Nowka states that the "throughput of the MPEG-4 decode[r] is varied over a range of 4:1 with a logic supply power consumption range of about 13:1." *Id.*

Under the heading, "Scalable Clocking Subsystem," Nowka discloses that "on-the-fly frequency modification techniques can be used to provide dynamic frequency scaling for additional active power reduction." Ex. 1004, 1444 (righthand column). According to Nowka, "When the performance demands of the application decrease, the system software can lower the operating frequency." *Id.* Nowka discloses that, "[u]nder software control, the frequency of the core can be varied from the maximum frequency down to 1/64th of the maximum." *Id.*

Nowka discusses Figure 8 under the heading, "Dynamic Voltage and Frequency Scaling Measurements." Ex. 1004, 1444 (righthand column). Figure 8 shows voltage versus time traces for the total SOC power, the SOC logic power, the SOC I/O power, and the SOC logic supply voltage (Vdd). *Id.* at 1444–45 (righthand column, Fig. 8). Figure 8 also includes a "Dhrystone Loop Indicator" trace that "toggles when a fixed number of Dhrystone loops have been executed." *Id.* Figure 8 shows how power is affected by changes in frequency[10] and logic supply voltage under control of the clock and power management software. *Id.*

Under the heading, "Active Power Management," Nowka states that dynamic voltage scaling and dynamic frequency scaling are used to reduce the power consumption of the processor and control power consumption "on

[10] According to Nowka, the clock and power management adjusts the frequency by modifying the output clock divider of the phase locked loop (PLL). Ex. 1004, 1444 (righthand column under the heading "Scalable Clocking Subsystem").

a very fine time scale." Ex. 1004, 1445 (lefthand column). According to Nowka, "Through voltage and frequency scaling and clock gating, the performance/watt of this design can be varied by more than a factor of four." *Id.* (righthand column).

Under the heading "Standby Power Management," Nowka discloses that "[s]everal modes of standby operation are employed to achieve a range of standby power levels." Ex. 1004, 1446 (lefthand column). According to Nowka, "The on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power." *Id.*

By way of summary, Nowka states, "Under software control, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption." Ex. 1004, 1446 (righthand column). According to Nowka, "[b]y applying these techniques," high frequencies and low power consumption can be achieved, "thereby dynamically adapting to the changing needs for performance and power demanded by the applications." *Id.*

2. Independent Claims 1, 16, and 37

As discussed above, claims 1, 16, and 37 contain similar recitations. Although we refer explicitly to claim 1, our analysis applies equally to claims 16 and 37.

a) Claim 1 Preamble

The claim 1 preamble recites, "A method of managing power on an integrated circuit including a plurality of power islands."
Ex. 1001, 13:33–34.

Petitioner contends that Nowka discloses the claim 1 preamble. Pet. 9–10. According to Petitioner, "Nowka discloses a method of managing power on an [integrated circuit] IC including a plurality of power islands," where the power islands correspond to Nowka's four domains that are supplied with different voltages. *Id.* (citing Ex. 1003 ¶¶ 50, 51; Ex. 1004, 1444, 1446, Fig. 3).

Patent Owner does not dispute Petitioner's contentions for the claim 1 preamble.

We find that Petitioner's contentions for the claim 1 preamble are sufficiently supported by the cited evidence and adequate for purposes of institution.

b) Claim Element [1a]

Claim element [1a] recites "determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands." Ex. 1001, 13:36–39.

Petitioner contends that Nowka discloses and renders obvious claim element [1a]. Pet. 10–15. According to Petitioner, "Nowka discloses that its SOC allows for 'performance demands of the application to be met' (needs and operation of the integrated circuit) while 'minimizing the dynamic power consumption' (determining a target power level)." Pet. 10 (citing Ex. 1003 ¶ 52; Ex. 1004, 1446). Petitioner contends that "Nowka discloses that power consumption is independently controlled within each of the power islands," asserting that "Nowka's power domains receive distinct power supplies, which can be controlled independently." Pet. 15 (citing Ex. 1003 ¶ 64; Ex. 1004, 1442).

Petitioner identifies three examples of "determining a target power level" in Nowka. Pet. 11–13. First, Petitioner contends that Nowka's Figures 5 and 6 "demonstrate that the target power level of a power island (target supply voltage of logic domain) is shifted in response to needs and operation of the integrated circuit (varying requirements of the application being run, or different requirements from different applications)." Pet. 11 (citing Ex. 1003 ¶ 54; Ex. 1004, 1444, Figs. 5, 6). Second, Petitioner contends that Nowka's "Figure 8 shows the corresponding decrease and increase and power consumption in response to frequency and voltage changes, which a POSITA would have understood to be executed 'in anticipation of [] performance demands' (needs and operation of the integrated circuit)." Pet. 12 (brackets in original; citing Ex. 1003 ¶ 55; Ex. 1004, 1444, Fig. 8). Third, Petitioner contends that "Nowka discloses clock gating inactive registers and cores, as well as putting the system in various standby modes, which changes the power state of the logic domain, when certain registers and units, or the entire logic domain, does not need to be active." Pet. 13 (citing Ex. 1003 ¶¶ 59, 60; Ex. 1004, 1445–46). Petitioner contends that the actions disclosed in these three examples "were well-understood in the art as mechanisms for adjusting power level" and "mirror[] the approach of the '306 patent, which describes setting the target for certain parameters such as frequency or voltage as the example of 'determining a target power level.'" *Id.* (citing Ex. 1001, 7:38–50, Fig. 5; Ex. 1003 ¶¶ 56–61).

Petitioner contends that Nowka teaches the claim limitation, "based on needs and operation of the integrated circuit," under both its plain and ordinary meaning and Patent Owner's proposed construction, i.e., "based on future operational needs and current operating status." Pet. 14–15 (citing

Exs. 1011, 1012). Petitioner contends that "Nowka's discussion that it changes frequency and voltage '[i]n anticipation of lower performance demands' shows that its power management is responsive to future operational needs, while its disclosure that 'anticipating an increase in demand, the logic supply is raised to 1.8 V without interrupting execution' shows that it is also responsive to the current operational status of the integrated circuit." *Id.* (citing Ex. 1003 ¶ 63; Ex. 1004, 1444).

Patent Owner disputes Petitioner's contentions for the portion of claim element [1a] that recites "determining a target power level for one of the power islands based on needs and operation of the integrated circuit." Prelim. Resp. 10–21, 28–34.

We find that Petitioner's contentions for claim element [1a], as summarized above, are sufficiently supported by the cited evidence and adequate for purposes of institution.

Patent Owner argues that Petitioner collapses three separately recited elements—[1a], [1b], and [1c]—into a single inquiry and "does not offer reasoning or evidence to connect the cited disclosure of . . . [Nowka] to the requirements of the claims." Prelim. Resp. 10–12, 14, 20. On the present record, we disagree. Petitioner's use of parentheticals shows with sufficient particularity where and how Petitioner contends the limitations of claim element [1a] are disclosed or suggested by Nowka. *See, e.g.*, Pet. 10 (quotes from Nowka followed by claim language in parentheses).

Patent Owner argues it is unclear whether Petitioner's contentions are based on obviousness or inherency. Prelim. Resp. 12–13, 15. On the present record, we disagree. Obviousness and inherency are not mutually exclusive legal standards. *Paul Hartmann AG v. Attends Healthcare Prod., Inc.*, No. 2022-1724, 2024 WL 911880, at *3 (Fed. Cir. Mar. 4, 2024)

("[I]nherency may supply a missing claim limitation in an obviousness analysis," but "the use of inherency . . . must be carefully circumscribed in the context of obviousness." (quoting *PAR Pharm., Inc. v. TWI Pharm., Inc.*, 773 F.3d 1186, 1194–95 (Fed. Cir. 2014)). We find that Petitioner's contentions are sufficiently clear for purposes of institution, regardless of whether they invoke inherency in addition to obviousness. *See, e.g.*, Pet. 13 ("A POSITA would have found it obvious that each of these actions involves determining a target power level . . . ."); Pet. 13–14 ("To the extent that Nowka doesn't disclose determining a target power level based on needs and operation of the integrated circuit, it would have been obvious to a POSITA that the system was making such a determination.").

Patent Owner asserts that Petitioner's obviousness argument is conclusory and does not identify what is lacking in Nowka, what modifications would need to be made, or why a POSITA would have been motivated and able to make such modifications. Prelim. Resp. 15. On the present record, we disagree. We find that Petitioner's contentions for claim element [1a], as summarized above, are sufficiently detailed for purposes of institution.

Patent Owner argues that Petitioner fails to show that Nowka discloses claim element [1a] under Patent Owner's proposed construction, i.e., "based upon the future operational needs and current operating status of the integrated circuit." Prelim. Resp. 16–21. We disagree for two reasons. First, we do not adopt Patent Owner's proposed construction for the reasons discussed in Section III.C. above. Second, the Petition addresses Patent Owner's proposed construction, and we find that Petitioner's contention is sufficiently supported by the cited evidence and adequate for purposes of institution. Pet. 14–15 (citing Ex. 1003 ¶ 63; Ex. 1004, 1444).

c) Claim Element [1b]

Claim element [1b] recites "determining at least one of actions to change a power consumption level of the one of the power islands to the target power level." Ex. 1001, 13:40–42.

Petitioner contends that Nowka discloses claim element [1b]. Pet. 15–16. Cross-referencing its contentions for claim element [1a], Petitioner asserts, "Nowka discloses a number of actions such as changing frequency, changing voltage, clock gating, and standby modes, to change the power consumption level of the logic domain to a target power level." Pet. 16 (citing Ex. 1003 ¶¶ 65–68). According to Petitioner, it "would have been obvious to a POSITA, in light of Nowka's disclosure of various actions, that Nowka's system makes a determination on which action to take. *Id.* (citing Ex. 1004, 1442).

Patent Owner disputes Petitioner's contention for claim element [1b], relying on the same arguments Patent Owner presents for claim element [1a]. Prelim. Resp. 37–38.

We find that Petitioner's contentions for claim element [1b] are sufficiently supported by the cited evidence and adequate for purposes of institution for the reasons discussed above with reference to element [1a].

d) Claim Element [1c]

Claim element [1c] recites "performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands." Ex. 1001, 13:43–47.

Petitioner contends that Nowka discloses claim element [1c]. Pet. 16–17. Cross-referencing its contentions for claim element [1b],

Petitioner asserts, "Nowka discloses performing an action such as changing frequency, changing voltage, clock gating, or standby mode to change the power consumption level of the logic domain to the target power level. Pet. 16 (citing Ex. 1003, ¶ 70; Ex. 1004, 1444 Section III.C (voltage scaling), 1444 Section V (frequency and voltage scaling), 1445 (clock gating), 1446 (standby modes).) According to Petitioner, "changing a frequency level is 'selecting a frequency' for the logic domain." Pet. 17.

Patent Owner does not dispute Petitioner's contentions for claim element [1c].

We find that Petitioner's contentions for claim element [1c] are sufficiently supported by the cited evidence and adequate for purposes of institution.

e) Conclusion for Claims 1, 16, and 37

For the reasons discussed above, we determine that Petitioner shows a reasonable likelihood of prevailing on its challenge to independent claims 1, 16, and 37 based on Nowka.

3. Dependent Claims 2–15, 17–36, and 38–51

Claims 2–15 depend from claim 1; claims 17–36 depend from claim 16; and claims 38–51 depend from claim 37. Petitioner challenges the dependent claims based on Nowka alone or Nowka in combination with Borkar or Boerstler. Pet. 17–50. At this stage, Patent Owner does not present arguments for the dependent claims separate from its arguments for the independent claims, stating "the Board does not need to address [Petitioner's multiple-reference obviousness grounds] in its institution decision." Prelim. Resp. 38. In view of our determination that Petitioner shows a reasonable likelihood of prevailing on its challenge to the

independent claims and in the absence of any separate argument by Patent Owner addressing the dependent claims, we decline at this stage to provide an explicit analysis of Petitioner's challenge to the dependent claims.

E. Petitioner's Nicol-led Challenges

Petitioner contends that claims 1–51 are unpatentable as obvious based on Nicol alone or in combination with Nowka, Borkar, or Naffziger. Pet. 50–91. Patent Owner opposes. Prelim. Resp. 1–2, 21–28, 34–38.

In view of our determination that Petitioner shows a reasonable likelihood of prevailing on its challenge to the independent claims based on Nowka, we decline at this stage to provide an explicit analysis of Petitioner's Nicol-led challenges.

IV. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–51 of the '306 Patent is instituted commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial.

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