UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,224,563 B2
APPLICATION NO. : 10/651360
DATED : May 29, 2007
INVENTOR(S) : Samuel D. Naffziger

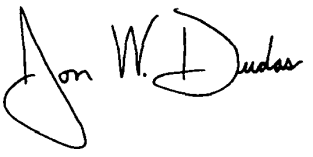
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 2, line 44, delete "bums" and insert -- burns --, therefor.

In column 7, line 65, in Claim 12, delete "circuits" and insert -- circuit --, therefor.

Signed and Sealed this

Twelfth Day of August, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	3547236
Application Number:	10651360
International Application Number:	
Confirmation Number:	8560
Title of Invention:	METHOD AND DEVICE FOR CIRCUIT CONTROL
First Named Inventor/Applicant Name:	Samuel D. Naffziger
Customer Number:	22879
Filer:	Kevin M. Hart/Marci Santillanes
Filer Authorized By:	Kevin M. Hart
Attorney Docket Number:	200208753-2
Receipt Date:	01-JUL-2008
Filing Date:	29-AUG-2003
Time Stamp:	09:34:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	200208753.pdf	462217 f898292aaa720a8e428141818b2bae720d2b86e0	no	3
Warnings:					
Information:					

Total Files Size (in bytes):	462217

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: U.S. Patent No. 7,224,563

USPTO CONFIRMATION CODE: 8560

APPLICATION NO.: 10/651,360

FILED: Aug. 29, 2003

EXAMINER: Stephen W. Jackson

GROUP ART UNIT: 2836

FOR: METHOD AND DEVICE FOR CIRCUIT CONTROL

ATTORNEY DOCKET NUMBER: 200208753-2

37 CFR 1.322 & 37 CFR 1.323 REQUEST FOR CERTIFICATE OF CORRECTION

HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS

Sir:

The following is a request for a certificate of correction in Serial Number 10/651,360, now Patent Number 7,224,563.

A certificate of correction under 35 USC 254 is respectfully requested in the above-identified patent.

☒ All errors were the fault of the USPTO, no fee required. In the event that a further fee is required, please charge the amount to Deposit Account No. 082025.

☐ All errors were the fault of the applicant and, accordingly, please charge **$100.00** to our Deposit Account No. 082025. In the event that a further fee is required, please charge the amount to the same Deposit Account.

☐ The errors were the fault of both the applicant and USPTO and, accordingly, please charge **$100.00** to our Deposit Account No. 082025. In the event that a further fee is required, please charge the amount to the same Deposit Account.

The exact locations where the errors appear in the patent and patent application are as follows:

In column 2, line 44, delete "bums" and insert - - burns - -, therefor.
(Specification filed on Aug. 29, 2003, page 3, line 11)

In column 7, line 65, in Claim 12, delete "circuits" and insert - - circuit - -, therefor.
(Amendment to claims filed on Nov. 13, 2006, page 3, in Claim 12, line 5)

The requested corrections are attached on Form PTO 1050.

Respectfully Submitted

6/30/2008
DATE

Name: Steven L. Webb
Registration No.: 44,395

Attorney/Agent of Record

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,224,563

APPLICATION NO. : 10/651,360

ISSUE DATE : May 29, 2007

INVENTOR(S) : Samuel D. Naffziger

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 2, line 44, delete "bums" and insert - - burns - -, therefor.

In column 7, line 65, in Claim 12, delete "circuits" and insert - - circuit - -, therefor.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

This collection of information is required by 37 CFR 1.322, and 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Attention Certificate of Corrections Branch, Commissioner for Patent, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,360	05/29/2007	7224563	200208753-2	8560

22879 7590 05/09/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 655 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Samuel D. Naffziger, Fort Collins, CO;

USPTO APR 23 2007 PATENT & TRADEMARK OFFICE

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22879 7590 02/22/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Laura M. Clark	(Depositor's name)
	(Signature)
4/23/2007	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,360	08/29/2003	Samuel D. Naffziger	200208753-2	8560

TITLE OF INVENTION: METHOD AND DEVICE FOR CIRCUIT CONTROL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	05/22/2007

04/23/2007 TBESHAH2 00000067 08202S 10651360

EXAMINER	ART UNIT	CLASS-SUBCLASS
JACKSON, STEPHEN W	2836	361-115000

01 FC:1501 1400.00 DA
02 FC:1504 300.00 DA

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Hewlett-Packard Development Company, L.P. Houston, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-2025 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 4/23/2007

Typed or printed name William P. O'Meara Registration No. 29,962

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PAGE 1/2 * RCVD AT 4/23/2007 11:08:33 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2732885 * CSID:9708987247 * DURATION (mm-ss):00-58

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22879 7590 02/22/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
JACKSON, STEPHEN W	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/22/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,360	08/29/2003	Samuel D. Naffziger	200208753-2	8560

TITLE OF INVENTION: METHOD AND DEVICE FOR CIRCUIT CONTROL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	05/22/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

nd send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where urther correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for otifications.

SPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 02/22/2007

T PACKARD COMPANY
72400, 3404 E. HARMONY ROAD
TUAL PROPERTY ADMINISTRATION
LLINS, CO 80527-2400

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
0	08/29/2003	Samuel D. Naffziger	200208753-2	8560

TION: METHOD AND DEVICE FOR CIRCUIT CONTROL

	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
l	NO	$1400	$300	$0	$1700	05/22/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SON, STEPHEN W	2836	361-115000

spondence address or indication of "Fee Address" (37

orrespondence address (or Change of Correspondence TO/SB/122) attached.

ss" indication (or "Fee Address" Indication form v 03-02 or more recent) attached. **Use of a Customer uired.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

ME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

E: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for et forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

ppropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

fee(s) are submitted:

Fee (No small entity discount permitted)

der - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

ty Status (from status indicated above)

claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in y the records of the United States Patent and Trademark Office.

nature _____ Date _____

d name _____ Registration No. _____

nformation is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) nfidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and npleted application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete ggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. dria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, ia 22313-1450.

ork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,360	08/29/2003	Samuel D. Naffziger	200208753-2	8560

22879 7590 02/22/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
JACKSON, STEPHEN W	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/22/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 655 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 655 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/651,360	NAFFZIGER, SAMUEL D.	
	Examiner	Art Unit	
	Stephen W. Jackson	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment of 11-13-06*.

2. ☒ The allowed claim(s) is/are *1-35*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Stephen W Jackson 2-20-07

STEPHEN W. JACKSON
PRIMARY EXAMINER

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/651,360	NAFFZIGER, SAMUEL D.	
	Examiner	Art Unit	
	Stephen W. Jackson	2836	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
361	115	361	90						
INTERNATIONAL CLASSIFICATION									
H 0 2 H	7/00								
	/								
	/								
	/								
	/								

N/A
(Assistant Examiner) (Date)

T. Bell 2-07
(Legal Instruments Examiner) (Date)

Stephen W Jackson 2-20-07
STEPHEN W. JACKSON
PRIMARY EXAMINER
(Primary Examiner) (Date)

Total Claims Allowed: 35

O.G. Print Claim(s)	O.G. Print Fig.
35	2

☒ **Claims renumbered in the same order as presented by applicant** ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/651,360	NAFFZIGER, SAMUEL D.
	Examiner	Art Unit
	Stephen W. Jackson	2836

SEARCHED			
Class	Subclass	Date	Examiner
361	115	2/20/2007	SWJ
361	90	2/20/2007	SWJ

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
USPTO East text search	8/8/2006	SWJ

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Alexandria, Virginia 22313-1450
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Bib Data Sheet

CONFIRMATION NO. 8560

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/651,360	08/29/2003 RULE	361	2836	200208753-2

APPLICANTS
Samuel D. Naffziger, Fort Collins, CO;

**** CONTINUING DATA ***************************
This appln claims benefit of 60/480,056 06/20/2003

**** FOREIGN APPLICATIONS ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 11/22/2003

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☑ no	CO	4	34	3
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature / Initials				

ADDRESS
22879

TITLE
Method and device for circuit control

FILING FEE RECEIVED		
1252	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

OIPE IAP89
NOV 13 2006
PATENT & TRADEMARK OFFICE

11-14-06

IFW

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

Inventor(s): Samuel D. Naffziger

Application No.: 10/651,360

Filing Date: August 29, 2003

Confirmation No.: *8560*

Examiner: S. W. Jackson

Group Art Unit: 2836

Title: METHOD AND DEVICE FOR CIRCUIT CONTROL

Mail Stop **Amendment**
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- [x] Response/Amendment
- [x] New fee as calculated below
- [ ] No additional fee
- [ ] Other _____ Fee$
- [ ] Petition to extend time to respond
- [ ] Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	35	MINUS	34	= 1	X $50	$ 50
INDEP. CLAIMS	4	MINUS	3	= 1	X $200	$ 200
☐	FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM				+ $360	$ 0
EXTENSION FEE	☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 250

Charge $ 250 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail No. EV568266362US in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

Date of Deposit: November 13, 2006

Typed Name: Linda L. Gibson

Signature: Linda L. Gibson

Respectfully submitted,
Samuel D. Naffziger

By _____
David H. Tannenbaum
Attorney/Agent for Applicant(s)

Reg No. : 24,745

Date : November 13, 2006

Telephone : 214.855.8185

Rev 10/06a (TransAmd)

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

OIPE
NOV 13 2006
IAP89
PATENT & TRADEMARK OFFICE

Docket No.: 200208753-2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Samuel D. Naffziger

Application No.: 10/651,360 | Confirmation No.: 8560

Filed: August 29, 2003 | Art Unit: 2836

For: METHOD AND DEVICE FOR CIRCUIT CONTROL | Examiner: S. W. Jackson

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated August 15, 2006 (hereinafter "Current Action"), please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

11/15/2006 MBELETE1 00000085 082025 10651360

01 FC:1201 200.00 DA
02 FC:1202 50.00 DA

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of circuit control, comprising:
sensing a delivered voltage to a portion of an integrated circuit;
determining an appropriate frequency for the portion of the integrated circuit; and
providing the appropriate frequency to ~~the~~ said portion of said integrated circuit.

2. (Previously Amended) The method of claim 1 wherein said sensing, determining, and providing are continuously repeated during the integrated circuit's operation.

3. (Original) The method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

4. (Original) The method of claim 1 further comprising:
applying the delivered voltage to constituent devices of a voltage sensor.

5. (Original) The method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.

6. (Original) The method of claim 4 further comprising:
further determining a switching speed of the constituent devices at the delivered voltage.

7. (Original) The method of claim 6 further comprising:
using the switching speed to determine the appropriate frequency.

8. (Currently Amended) The method of claim 4 further comprising:
exposing the voltage sensor and the portion of the integrated circuit to the same physical conditions.

9. (Previously Amended) The method of claim 8 wherein the physical conditions include temperature.

10. (Original) The method of claim 1 further comprising:
calculating a value for the delivered voltage.

11. (Original) The method of claim 10 further comprising:

using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.

12. (Currently Amended) A device for electronic circuit control comprising:

means for sensing a delivered voltage to [[a]] one portion of an integrated circuit;

means for determining an appropriate frequency for the portion of the integrated circuit; and

means of providing the appropriate frequency to the portion of the integrated circuit, independent of frequencies provided to other portions of said integrated circuit.

13. (Original) The device of claim 12 further comprising:

means for determining the maximum possible frequency for the portion of the integrated circuit at the delivered voltage.

14. (Original) The device of claim 12 wherein said sensing means further comprises:

means for testing a switching speed of at least one test device at the delivered voltage.

15. (Previously Amended) The device of claim 14 wherein the at least one test device is similar to a circuit device comprising the portion of the integrated circuit.

16. (Previously Amended) The device of claim 14 further comprising:

means for using the switching speed as the appropriate frequency.

17. (Previously Amended) The device of claim 14 wherein the at least one test device and the circuit device are exposed to similar physical conditions.

18. (Previously Amended) The device of claim 17 wherein the physical conditions include temperature.

19. (Original) The device of claim 12 further comprising:

means for calculating a value for the delivered voltage.

20. (Original) The device of claim 19 wherein said calculating means includes analog-to-digital converter.

21. (Original) The device of claim 19 further comprising:

means for associating the value of the delivered voltage with a value for the appropriate frequency.

22. (Original) The device of claim 21 wherein said associating means includes a tabulation of possible values for the delivered voltage associated with a set of values for the appropriate frequency.

23. (Original) A system for circuit control comprising:

at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit;

at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit; and

at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.

24. (Original) The system of claim 23 wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

25. (Original) The system of claim 23 further comprising:

at least one test device to which the delivered voltage is applied.

26. (Previously Amended) The system of claim 25 at least one test device logic block to determine a switching speed of the at least one test device at the applied voltage.

27. (Original) The system of claim 26 wherein the switching speed is used to determine the appropriate voltage.

28. (Original) The system of claim 25 wherein the at least one test device is similar to a device that comprises the portion of the integrated circuit.

29. (Original) The system of claim 25 wherein the at least one test device and the portion of the integrated circuit are exposed to similar physical conditions.

30. (Original) The system of claim 29 wherein the physical conditions include temperature.

31. (Original) The system of claim 23 further comprising:

a converter to convert the delivered voltage to a value.

32. (Original) The system of claim 31 wherein the converter is an analog-to-digital converter.

33. (Original) The system of claim 23 further comprising:

a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.

34. (Previously Amended) The system of claim 33 wherein said table is a computer readable database.

35. (New) A system for circuit control comprising:

a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit;

a plurality of logic blocks arranged to determine an appropriate frequency for each said portion from said delivered voltages; and

a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.

REMARKS

I. Introduction

The Current Action:

Rejects claims 1-32 under the non-statutory doctrine of double patenting; and

Rejects claims 1-32 under 35 U.S.C. §102(b)

This Response:

Amends claims 1 and 12;

Adds claim 35; and

Traverses all rejections.

The Applicant has amended claim 1 and 12 to more clearly describe the claimed subject matter. Claim 35 has been added. No new matter has been added. Claims 1-35 are pending in the present application.

II. Arguments

A. The Rejection For Obviousness-Type Double Patenting

The Current Action has rejected claims 1-32 as obvious in light of Fetzer et al., U.S. Patent No. 6,927,605 (hereinafter *Fetzer*), and contends that the present application is impermissible obvious-type double patenting. However, as M.P.E.P. § 804 states, the analysis of obvious-type double patenting is the same as the analysis required for obviousness under 35 U.S.C. § 103(a). Thus, the Examiner must at least make a *prima facie* showing that claims 1-32 are obvious in light of *Fetzer*. Specifically, "any obvious-type double patenting should make clear: A) the differences between the inventions defined by the conflicting claims – a claim in the patent compared to a claim in the application; and B) the reasons why a person of ordinary skill in the art would conclude that the invention defined in the claims at issue would have been an obvious variation of the invention defined in a claim in the patent." M.P.E.P. §804B(1). The Applicant respectfully points out that, contrary to the contention of the Current Action, claims 1-32 of the present application contain substantially different limitations than those of *Fetzer*. The Current Action's unsupported statement that these substantial differences are "minor design variations" falls far short of that which is required

for making a *prima facie* rejection of obviousness. Therefore, the Applicant respectfully asks the Examiner to withdraw the obviousness-type double patenting rejection of claims 1-32.

B. The Rejections Under 35 U.S.C. § 102(b)

The Current Action also rejects claims 1-32 as anticipated by Tam et al., U.S. Patent No. 6,762,629 (hereinafter *Tam*) or Huard et al., U.S. Patent No. 6,885,233 (hereinafter *Huard*). However, the Applicant respectfully points out that *Tam* was published on July 13, 2004 and *Huard* was published on August 9, 2005. Since the present application was filed on August 29, 2003, neither *Tam* nor *Huard* are prior art under 35 U.S.C. § 102(b). Therefore, the Applicant respectfully submits that no rejection under 35 U.S.C. § 102(b) currently exists for claims 1-35, and the Applicant respectfully asks the Examiner to pass this application to issue.

III. Conclusion

In view of the above, Applicant believes the pending application is in condition for allowance.

Applicant believes that a fee in the amount of **$250.00** is due with this response, and that this amount is covered in the accompanying Fee Transmittal; however, please charge any underpayment or overpayment to Deposit Account No. 08-2025, under Order No. 200208753-2 from which the undersigned is authorized to draw.

Respectfully submitted,

By _____
David H. Tannenbaum
Registration No.: 24,745
Date: November 13, 2006

(214) 855-8185

Dated: November 13, 2006

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/651,360	08/29/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/13/2006	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 35	Minus	** 34	= 1	X $ =		OR	X $50=	50
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $ =		OR	X $200=	200
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	250

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
Deborah Nash

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,360	08/29/2003	Samuel D. Naffziger	200208753-2	8560

22879 7590 08/15/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
JACKSON, STEPHEN W	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,360	NAFFZIGER, SAMUEL D.	
	Examiner	Art Unit	
	Stephen W. Jackson	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-3-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Tam et al (6,762,629) or Huard et al (6,885,233).

Tam teaches a method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes. A clock frequency of a clock signal generator is adjusted in response to an evaluation of sampled values of the supply voltage.

The title of the Huard patent is "Altering Operating Frequency and Voltage Set Point of a Circuit in Response to the Operating Temperature and Instantaneous Operating Voltage of the Circuit".

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-32 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,927,605. Although the conflicting claims are not identical, they are not patentably distinct from each other because the above mentioned patent includes means for dynamically varying the frequency of a clock signal in response to observed (sensed) changes in the variable operating voltage. Differences between the two sets of claims are minor design variations well within the abilities of persons of ordinary skill in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Jackson whose telephone number is 571-272-2051. The examiner can normally be reached on 6:30am-3:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SWJackson

August 8, 2006

Stephen W Jackson 8-8-06

STEPHEN W. JACKSON
PRIMARY EXAMINER

OIPE JC46 OCT 0 3 2003 PATENT & TRADEMARK OFFICE

PATENT APPLICATION
Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200208753-2	10/651,360	

APPLICANT: Samuel D. Naffziger

FILING DATE: Aug. 29, 2003 | GROUP:

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	60/480,056		Naffziger	
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check If Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER: S. Jackson | DATE CONSIDERED: 8-8-06

Rev 10/03 (PTO1449)

Notice of References Cited	Application/Control No. 10/651,360	Applicant(s)/Patent Under Reexamination NAFFZIGER, SAMUEL D.	
	Examiner Stephen W. Jackson	Art Unit 2836	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,927,605	08-2005	Fetzer et al.	327/101
*	B	US-6,885,233	04-2005	Huard et al.	327/513
*	C	US-6,762,629	07-2004	Tam et al.	327/114
*	D	US-7,071,768	07-2006	Abe et al.	327/540
	E	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/651,360	NAFFZIGER, SAMUEL D.	
	Examiner	Art Unit	
	Stephen W. Jackson	2836	

SEARCHED			
Class	Subclass	Date	Examiner
361	115	8/8/2006	SWJ
361	103	8/8/2006	SWJ
361	90	8/8/2006	SWJ

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
USPTO East search for prior art	8/8/2006	SWJ

Index of Claims



Application/Control No.	Applicant(s)/Patent under Reexamination
10/651,360	NAFFZIGER, SAMUEL D.
Examiner	**Art Unit**
Stephen W. Jackson	2836

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	27544	clock adj frequency	USPAT	OR	OFF	2006/08/08 12:13
L2	20	1 same voltage adj (sensor sensing monitor$3)	USPAT	OR	OFF	2006/08/08 12:13
L3	20	1 same (voltage adj (sensor sensing monitor$3))	USPAT	OR	OFF	2006/08/08 12:13

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	27544	clock adj frequency	USPAT	OR	OFF	2006/08/08 12:13
L2	20	1 same voltage adj (sensor sensing monitor$3)	USPAT	OR	OFF	2006/08/08 12:13
L3	20	1 same (voltage adj (sensor sensing monitor$3))	USPAT	OR	OFF	2006/08/08 12:13

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Hewlett-Packard Company
Legal Department
3404 East Harmony Road
Mail Stop 79
Fort Collins, Colorado 80528-9599

To	Company	Telephone	Fax
USPTO	USPTO		571-273-8300
From	**Subject**	**Number of Pages: 25**	**Date**
Shannan M. Sullivan Legal Administrator	**Status Inquiries**		**11/15/05**

Attached please find twenty-four (24) Status Inquiries for the following Application Numbers:

App. No.	HP PDNO
10/680472	200304426-2
10/679725	200208731-1
10/679786	200208730-1
10/678263	10992268-3
10/677705	10016293-1
10/676859	200209135-1
10/670933	200208344-1
10/670934	200208330-1
10/670033	200300848-1
10/669074	200205496-1
10/662383	10992435-3
10/659901	200310430-1
10/652098	200308564-1
10/651360	200208753-2
10/652123	200300350-1
10/647607	100111259-1
10/647769	100111257-1
10/647596	100111234-1
10/647595	100111227-1
10/694108	200300193-1
10/379246	200206055-1
10/690194	200206304-1
10/689410	200300486-1
10/393192	200210138-1

Thank you.

Shannan Sullivan
Legal Administrator
Hewlett-Packard Company
(970) 898-0665 Phone; (970) 898-7247 Fax

2 of 25 pgs rec'd CFC

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PAGE 1/25 * RCVD AT 11/15/2005 2:12:50 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/30 * DNIS:2738300 * CSID:9708987247 * DURATION (mm-ss):05-16

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

Inventor(s): Samuel D. Naffziger

Application No.: 10/651360

Filing Date: Aug 29, 2003

Confirmation No.: 8560

Examiner: Unknown

Group Art Unit:

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NOV 15 2005

Title: Method And Device For Circuit Control

Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

STATUS INQUIRY

More than 26 months have passed since:

☒ NEW APPLICATIONS
The filing of this application on Aug 29, 2003. No communication has been received from the Patent and Trademark Office indicating action on this application.

☐ AMENDED APPLICATIONS
The filing of a response on _____. No communication has been received from the Patent and Trademark Office.

☐ APPEALED APPLICATION
The Appeal Brief was filed on _____.

☐ An Examiner's Answer was mailed on _____.

☐ A Reply Brief to the Examiner's Answer was submitted on _____.

☐ ALLOWED APPLICATIONS
The mailing of FORM POL-85 and/or Examiner's Amendment on _____.

Kindly advise the undersigned of the present status of this application.

☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450

Date of Deposit:

OR

☒ I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300.

Date of facsimile: 11/15/05

Typed Name: Shannan Sullivan

Signature: Shannan Sullivan

Respectfully submitted,

By _____

Attorney/Agent for Applicant(s)

William P. O'Meara

Reg No.: 29982

Date: Nov 14, 2005

Telephone: 970 898 7917

Rev 10/05 (Status)

10/651,360

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 200208753-2

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	34	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	34 minus 20=	* 14
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	252
X42=		OR	X84=	0
+140=		OR	+280=	0
TOTAL		OR	TOTAL	1002

PIE Amdt A

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 34	Minus	** 34	= —
Independent	* 3	Minus	*** 3	= —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=	—	OR	X$18=	—
X42=	—	OR	X84=	—
+140=	—	OR	+280=	—
TOTAL ADDIT. FEE	—	OR	TOTAL ADDIT. FEE	—

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

OIPE
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PATENT & TRADEMARK OFFICE

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Docket No.: 200208753-2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Samuel D. Naffziger

Application No.: 10/651,360 Art Unit: N/A

Filed: August 29, 2003 Examiner: Not Yet Assigned

For: METHOD AND DEVICE FOR CIRCUIT CONTROL

FIRST PRELIMINARY AMENDMENT

MS Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 7 of this paper.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

10-6-3



PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Samuel D. Naffziger

Confirmati n N .:

Application No.: 10/651,360

Examiner:

Filing Date: Aug. 29, 2003

Group Art Unit:

Title: METHOD AND DEVICE FOR CIRCUIT CONTROL

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

(X) Response/Amendment ( ) Petition to extend time to respond
( ) New fee as calculated below (X) Supplemental Declaration
(X) No additional fee (Address envelope to "Mail Stop Non-Fee Amendment")
(X) Other: Information Disclosure Statement with PTO1449 (fee $_____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	34	MINUS	34	= 0	X $18	$ 0
INDEP. CLAIMS	3	MINUS	3	= 0	X $86	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $290	$ 0
EXTENSION FEE	1ST MONTH $110.00 [ ]	2ND MONTH $420.00 [ ]	3RD MONTH $950.00 [ ]	4TH MONTH $1480.00 [ ]		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EV256035774US

Date of Deposit Oct. 3, 2003

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By _____

Typed Name: John Pallivathukal

Respectfully submitted,

Samuel D. Naffziger

By Michael J. Fogarty, III

Michael J. Fogarty, III

Attorney/Agent for Applicant(s)
Reg. No. **42,541**

Date: **Oct. 3, 2003**

Telephone No.: **(214) 855-8172**

Rev 10/03 (TnAmdExp)

- Attach as First Page to Transmitted Papers -

AMENDMENTS TO THE SPECIFICATION

Please add the following heading and paragraph prior to paragraph **[0001]**, page 1 of the specification.

CROSS-REFERENCE TO RELATED APPLICATIONS

[0000] This application claims priority to U.S. Provisional Patent Application No. 60/480,056, filed June 20, 2003, entitled "A SYSTEM FOR RAPID ADAPTATION OF CLOCK FREQUENCY TO VOLTAGE TRANSIENTS."

AMENDMENTS TO THE CLAIMS

1. (Original) A method of circuit control, comprising:
sensing a delivered voltage to a portion of an integrated circuit;
determining an appropriate frequency for the portion of the integrated circuit; and
providing the appropriate frequency to the integrated circuit.

2. (Currently Amended) The method of claim 1 wherein said sensing, determining[[;]], and providing are continuously repeated during the integrated circuit's operation.

3. (Original) The method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

4. (Original) The method of claim 1 further comprising:
applying the delivered voltage to constituent devices of a voltage sensor.

5. (Original) The method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.

6. (Original) The method of claim 4 further comprising:
further determining a switching speed of the constituent devices at the delivered voltage.

7. (Original) The method of claim 6 further comprising:
using the switching speed to determine the appropriate frequency.

8. (Currently Amended) The method of claim 4 further comprising:
exposing the voltage sensor and the portion [[to]]of the integrated circuit to the same physical conditions.

9. (Currently Amended) The method of claim 8 wherein the physical conditions include temperature.

10. (Original) The method of claim 1 further comprising:
calculating a value for the delivered voltage.

11. (Original) The method of claim 10 further comprising:

using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.

12. (Original) A device for electronic circuit control comprising:

means for sensing a delivered voltage to a portion of an integrated circuit;

means for determining an appropriate frequency for the portion of the integrated circuit; and

means of providing the appropriate frequency to the portion of the integrated circuit.

13. (Original) The device of claim 12 further comprising:

means for determining the maximum possible frequency for the portion of the integrated circuit at the delivered voltage.

14. (Original) The device of claim 12 wherein said sensing means further comprises:

means for testing a switching speed of at least one test device at the delivered voltage.

15. (Currently Amended) The device of claim [[12]]14 wherein the at least one test device is similar to a circuit device comprising[[:]] the portion of the integrated circuit.

16. (Currently Amended) The device of claim 14 further comprising:

means for using the switching speed as the appropriate frequency.

17. (Currently Amended) The device of claim 14 wherein the at least one test device and the circuit device are exposed to similar physical conditions.

18. (Currently Amended) The device of claim 17 wherein the physical conditions include temperature.

19. (Original) The device of claim 12 further comprising:

means for calculating a value for the delivered voltage.

20. (Original) The device of claim 19 wherein said calculating means includes analog-to-digital converter.

21. (Original) The device of claim 19 further comprising:

means for associating the value of the delivered voltage with a value for the appropriate frequency.

22. (Original) The device of claim 21 wherein said associating means includes a tabulation of possible values for the delivered voltage associated with a set of values for the appropriate frequency.

23. (Original) A system for circuit control comprising:

at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit;

at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit; and

at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.

24. (Original) The system of claim 23 wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

25. (Original) The system of claim 23 further comprising:

at least one test device to which the delivered voltage is applied.

26. (Currently Amended) The system of claim 25 at least one test device logic block to determine a switching speed of the at least one test device at the applied voltage.

27. (Original) The system of claim 26 wherein the switching speed is used to determine the appropriate voltage.

28. (Original) The system of claim 25 wherein the at least one test device is similar to a device that comprises the portion of the integrated circuit.

29. (Original) The system of claim 25 wherein the at least one test device and the portion of the integrated circuit are exposed to similar physical conditions.

30. (Original) The system of claim 29 wherein the physical conditions include temperature.

31. (Original) The system of claim 23 further comprising:

a converter to convert the delivered voltage to a value.

32. (Original) The system of claim 31 wherein the converter is an analog-to-digital converter.

33. (Original) The system of claim 23 further comprising:

a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.

34. (Currently Amended) The system of claim 33 wherein said table is a computer readable database.

REMARKS

The specification has been amended to include a reference to U.S. Provisional Patent Application No. 60/480,056, filed June 20, 2003, entitled "A SYSTEM FOR RAPID ADAPTATION OF CLOCK FREQUENCY TO VOLTAGE TRANSIENTS," to which the present application claims priority. A Supplemental Declaration showing reference to this priority is being filed concurrently with this Preliminary Amendment.

Claims 2, 8, 9, 15 – 18, 26, and 34 have been amended to correct typographical errors. No new matter has been added.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 06-2380, under Order No. 200208753-2 from which the undersigned is authorized to draw.

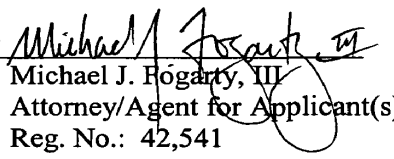
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV256035774US, in an envelope addressed to: MS Non-Fee Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Date of Deposit: October 3, 2003

Typed Name: John Pallivathukal

Signature: 

Respectfully submitted,

By 
Michael J. Fogarty, III
Attorney/Agent for Applicant(s)
Reg. No.: 42,541

Date: October 3, 2003

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P. O. Box 272400
Fort Collins, Colorado 80527-2400



PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

SUPPLEMENTAL DECLARATION

As a below named inventor, I hereby declare that:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND DEVICE FOR CIRCUIT CONTROL

Application No. **10/651,360**, filed in the United States Patent and Trademark Office on **Aug. 29, 2003**, and included in

(X) the attached amendment.
( ) the amendment(s) filed on or about _____

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understood the contents of the above identified specification, including the claims, as amended by any amendment(s) referred to above and that I have disclosed the best mode for carrying out the invention as of the effective filing date of this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, CFR 1.56. If this is a continuation-in-part application, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior (priority) application and the National or PCT international filing date of this continuation-in-part application.

(X) In compliance with this duty there is attached an Information Disclosure Statement. (37 CFR 1.97).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of inventor: Samuel D. Naffziger **Citizenship:** United States

Residence: 3749 Ashmount Drive, Fort Collins, Colorado 80525

Post Office Address: Same as residence.

Samuel D Naffziger 10-2-03

Inventor's Signature **Date**

Full Name of # 2 joint inventor: _____ **Citizenship:** _____

Residence: _____

Post Office Address: _____

_____ _____

Inventor's Signature **Date**

HEWLETT-PACKARD COMPANY
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Fort Collins, Colorado 80527-2400



PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Samuel D. Naffziger

Confirmation N .:

Application No.: 10/651,360

Examiner:

Filing Date: Aug. 29, 2003

Group Art Unit:

Title: METHOD AND DEVICE FOR CIRCUIT CONTROL

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97 (c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

( ) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: _____
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( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number _____ on _____
Number of pages:

Typed Name: **J hn Pallivathukal**

Signature: _____

Respectfully submitted,

Samuel D. Naffziger

By _____
Michael J. F garty, III
Attorney/Agent for Applicant(s)
Reg. No. **42,541**

Date: **Oct. 3, 2003**

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Rev 10/03 (IDSCERT)

OIPE JC46 OCT 0 3 2003 PATENT & TRADEMARK OFFICE

PATENT APPLICATION
Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200208753-2	**10/651,360**	

APPLICANT: **Samuel D. Naffziger**

FILING DATE	GROUP
Aug. 29, 2003	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	60/480,056		Naffziger	
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER	DATE CONSIDERED

Rev 10/03 (PTO1449)

HEWLETT-PACKARD COMPANY
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Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter



Mail Stop Patent Application
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Samuel D. Naffziger**

TITLE: **METHOD AND DEVICE FOR CIRCUIT CONTROL**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 4 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( ) (Other)_____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	34 — 20	14	X $18	$ 252
INDEPENDENT CLAIMS	3 — 3	0	X $84	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$280	$ 0
BASIC FEE: Design ($330.00); Utility ($750.00)				$ 750
TOTAL FILING FEE				$ 1,002
OTHER FEES				$
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 1,002

Charge $ 1,002 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EV256035108US

Date of Deposit August 29, 2003

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By _____

Typed Name: **John Pallivathukal**

Respectfully submitted,

Samuel D. Naffziger

By _____

Michael J. Fogarty, III

Attorney/Agent for Applicant(s)
Reg. No. **42,541**

Date: **August 29, 2003**

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Rev 05/03 (TransNew)

- Attach as First Page to Transmitted Papers -

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

METHOD AND DEVICE FOR CIRCUIT CONTROL

Inventor:

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Fort Collins, Colorado 80525
Citizenship: United States

METHOD AND DEVICE FOR CIRCUIT CONTROL

BACKGROUND

[0001] Because of trends in process technology, scaling, and the frequency of operations for VLSI devices, power consumption has become a dominant issue in integrated circuit design. Managing power consumption is thus a high priority in the design objectives of these devices.

[0002] It is broadly recognized in the implementation of power management systems for VLSI devices that the most efficient means of power management is to simultaneously change 1) the voltage delivered to an integrated circuit, and 2) the frequency of that integrated circuit's operation. Because voltage is a primary determinant of switching speed for transistors of an integrated circuit, a designer will typically specify the maximum frequency at which a part can operate for a given voltage. Thus, for an example micro-processor, a power supply may generate a fixed voltage of 2 volts to a device and the device may be specified as operating at 2 GigaHertz (GHz). However, the design of the device has to be such that the voltage seen at the integrated circuit is never below the level that enables the full 2 GHz operation. If the voltage on the integrated circuit falls below that level, there could be a timing failure and some of the components would be unable to switch fast enough to make the 2 GHz cycle times.

[0003] But power supplies vary and electrical parasitics between the power supply and the actual transistors of an integrated circuit effect power transmission. Thus the voltage actually delivered to an integrated circuit is not a completely fixed value, but rather ripples and varies with time. On average these ripples may have a total magnitude of approximately + or - 10% of the total voltage. If the intent is to deliver 2 volts to the integrated circuit, the actual delivered voltage may vary between 1.8 volts and 2.2 volts. Since the voltage in large part determines the switching speed of components, designers have to make sure that (in the current example) the device in use can still operate at 2 GHz even if the delivered voltage is 1.8 volts. This is a technique known as guardbanding. Without this guardbanding, the integrated circuit could fail when the voltage drops.

[0004] For power consumption, two relationships become important when the voltage varies. One is the relationship of the device speed to voltage; a relationship that is approximately linear. If the voltage applied to a transistor is lowered by 10%, the switching speed of that transistor is reduced by approximately 10%. A first order approximation can be shown as:

$$F \propto v \tag{1}$$

[0005] The second relationship is between power and frequency. Power (the total wattage dissipated by an integrated circuit) is equal to the switching capacitance of a device (a relatively fixed value for a given design, labeled C), multiplied by the voltage across the device squared (labeled V), and multiplied by the frequency at which the device is switching (plus a leakage term which may be disregarded here). This relationship is thus:

$$P=CxV^2xF \tag{2}$$

[0006] Using the previous example, if the capacitance on a component is switching once per cycle, then the capacitance is switching at a rate of 2 GHz, (or once every 500 picoseconds). Equation 2 show that a reduction in voltage would result in a square law reduction in power. For example, when voltage (V) drops 10%, becomes .9xV, the square law reduction causes the power (P) to be .9x.9xP, or .81xP (a 19% reduction).

[0007] As equation 1 indicates, frequency is directly proportional to voltage. Thus when combined with equation 2, a reduction in frequency will lead to an additional voltage factor in power reduction. This results in power being reduced by approximately V^3. Using the previous example, a 10% drop in V would result in a .9x.9x.9xP (.72xP or 28%) reduction in power for a 10% reduction in voltage. This relationship is well known, and has been exploited for power management particularly in mobile devices such as laptops.

[0008] Many power-management solutions use software to minimize the excess computing power of microprocessors and other like devices. Based upon an expected load, the software determines how fast the processor must operate; for example, the software may note that a densely coded application may require more speed than a simple one. Once the software determines the speed required by the demand, it can reduce the speed to only that which is required. The result is a reduction in the power consumption for the device over time.

[0009] However, these methods lead to inefficiencies in voltage management. For example, these methods require that a software program predict the computing demands an integrated circuit may see and then change the voltage and frequency accordingly. This results in lag times associated with prediction inaccuracies. Further, the intention of these systems is to minimize the total energy consumed over time for the processor. Portable units, such as laptops, can then maximize the battery life with these algorithms. For a server type processor, minimizing total energy usage over a period of time is not the goal. Maximum computing power is the goal. Within a given power envelope, a server system should maximize the performance that is available on demand for a customer. Ideally, the full performance capability should be available at any time to a customer. Even in server systems, however, there are significant motivations for keeping the power down. For example, as a chip burns power it generates heat that is difficult to draw away from a small silicon die. Further, it is more expensive to run a large number of processors at higher power, and it is difficult to provide that power in tight spaces. Thus, for a server, a system that only tries to minimize power when the compute needs are high does not suffice; the compute needs are always high. Likewise, a system that simply provides maximum computing power is insufficient for most systems. Thus, there exists a need for a method that actively optimizes the power consumed while maintaining the system's ability to deliver the highest performance without having to rely on software predictions that are often inaccurate.

[0010] An additional shortcoming of currently available solutions is the time lag between the recognition that an opportunity to reduce power (or the recognition of the need to increase power due to high compute needs) and the operation that effects that change. After recognition, a command to vary voltage must be sent out to a voltage regulator which generates the voltage used by the processor. It then takes a number of microseconds (10s to 100s of microseconds, typically) for the voltage regulator to perform that task. It is not until that voltage transition is completed that the frequency can actually be raised on the processor itself, because a processor running at a frequency higher than the voltage supports can result in a timing failure. Thus, there is a time lag waiting for the voltage to slew before the frequency can be raised. Similarly, in order to lower the voltage (to reduce the power consumption) the frequency must be lowered first to avoid a timing failure caused by a voltage too low for a given frequency. A

system that understood exactly how fast the integrated circuit could operate for a given voltage, combined with a system that could operate the chip at a frequency matched to that voltage, would result in a significant efficiency gains. Instead of anticipating a voltage reduction and lowering frequency in advance, such a system could lower voltage and frequency together. Such a system could also avoid the guardbanding necessary when a designer is required to anticipate the varying operating conditions of a device. If, using the above example, the voltage varies by + or – 10%, a designer must ensure that the device will work at its quoted frequency if only 90% of the expected voltage is provided. Thus, there exists a need for a system that could set the frequency to an observed voltage and constantly vary the frequency to match the voltage actually delivered.

[0011] In order to further improve efficiencies, many power-management systems shut off parts of an integrated circuit that are not in use. For example, the floating point computation unit in a microprocessor is a high performance unit that is needed for technical code. For many applications (word processing, transaction processing, and other general integer applications) the floating point computation is unnecessary. A typical power-savings method might shut the clock down to the floating point unit so that it is not using power. But as units on an integrated circuit are powered up and down, the processor can experience large, sudden changes in power consumption. This poses a challenge to the power delivery system, because there is always some resistance and some inductance between the components and the power supply. Further, a sudden spike in power to dormant areas can result in a voltage drop to already powered sections that can cause operational and timing problems. Thus, there exists a need for a system that can adapt very rapidly to changes in voltage induced by sudden changes in power consumption.

SUMMARY

[0012] One disclosed embodiment of the invention is directed to circuit control that comprises sensing a delivered voltage to a portion of an integrated circuit, determining an appropriate frequency for the portion of the integrated circuit, and providing the appropriate frequency to the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which

[0014] FIGURE 1 is a flow chart of an embodiment of the present invention;

[0015] FIGURE 2 is a circuit layout according to an embodiment of the present invention;

[0016] FIGURE 3 is a graph illustrating some advantages of certain embodiments of the present invention;

[0017] FIGURE 4 is a flow chart of an embodiment of the present invention;

[0018] FIGURE 5 is a circuit layout according to an embodiment of the present invention;

[0019] FIGURE 6 is a flow chart of an embodiment of the present invention;

[0020] FIGURE 7 is a chart of timing relationships; and

[0021] FIGURE 8 is a circuit floor plan in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0022] Voltage sensors, such as those described in Patent Application No: Attorney Docket No. 200208752-1 (P747US-10304067, not yet filed) hereby incorporated by reference, can provide a means of detecting the voltage actually delivered to an integrated circuit. Often, the power consumption of different points on a integrated circuit will vary, resulting in a drop in voltage in one part of a integrated circuit that are not seen elsewhere. It may be advantageous to have a number of voltage sensors distributed across an entire die. Circuitry arranged to provide a determined frequency, such as a fast response frequency synthesizer as described in Patent

Application No.: Attorney Docket No. 200208731-1 (P749US-10304071, not yet filed) hereby incorporated by reference, can provide the ability to quickly adjust a clock frequency that drives a particular section of an integrated circuit. A frequency determining means is used to determine what frequency is appropriate for the integrated circuit (or a portion thereof) at the voltage delivered.

[0023] FIGURE 1 depicts a flow chart 100 describing the basic stages of certain embodiments of the present invention. In stage 101, the voltage that is actually delivered to an integrated circuit in sensed. As described above, the voltage delivered by a power supply can vary over time. As the voltage varies, the frequency of the clock used to operate the integrated circuit may have to be changed in order to avoid timing failures. Stage 102 illustrates that the basic method determines an appropriate frequency to provide to the integrated circuit. Typically, this frequency is derived directly from the delivered voltage. Lastly, the basic method provides to the integrated circuit the frequency determined to by appropriate in stage 103.

[0024] FIGURE 2 depicts an example component layout of one embodiment of the present invention. System 200 is capable of addressing all of the above described problems in the art for the management of integrated circuit 201. Power supply 202 supplies a voltage to system 200. As described above, this voltage is likely to vary. Voltage sensor 203 senses the voltage that is delivered to integrated circuit 201. In the depicted embodiment, voltage sensor 203 provides information regarding the delivered voltage to logic block 204. Logic block 204, in the depicted embodiment, determines the frequency that is appropriate for integrated circuit 201 and provides this information to frequency synthesizer 205. Frequency synthesizer 205 alters the system clock 206 signal to correspond with the determined appropriate frequency. Those of ordinary skill in the art will appreciate that system 200 is an example arrangement, and that the embodiments of the present invention are not limited to the arrangement depicted.

[0025] FIGURE 3 illustrates some advantages of the above embodiments. Graphic relationship 300 show a comparison between the delivered voltage 301, the frequency 302 provided by an embodiment of the present invention, the average frequency 303 provided by an embodiment of the present invention, and the frequency 304 allowed by prior art methods.

[0026] As described above, the delivered voltage 301 will likely vary, as seen by voltage deviation 305. Prior art solutions required that the provided frequency 304 be low enough to still be viable even at the minimum voltage 306. Some embodiments of the present invention are able to continuously sense the delivered voltage 301 and provide a frequency 302 that tracks the delivered voltage 301. Thus the average frequency 303, provided by these embodiments of the present invention is significantly higher than the frequency 304 allowed by prior art solutions.

[0027] The embodiments of the present invention are not limited to one manner of voltage to frequency conversion. In one embodiment of the present invention, the voltage sensors measure the effect of the voltage on circuit speed. FIGURE 4 is an example flow chart for an embodiment of this type. Method 400 illustrates, generally, how such an embodiment can use switching speed. The delivered voltage is sensed in stage 401. In such an embodiment, the delivered voltage would then be applied 402 to test devices (such as transistors) that may be part of the voltage sensor. The voltage sensor then determines 403 if the test devices are able to cycle at the currently provided clock frequency. If not, the frequency synthesizer instructs 404 to slow the provided frequency in order to compensate. If the test devices can cycle at the currently provided frequency, the depicted method determines 405 if the test devices are capable of cycling at a rate faster than the provided frequency. If so, the frequency synthesizer is instructed 406 to raise the frequency accordingly. If not, the currently provided frequency is unchanged.

[0028] In one embodiment using this method, the voltage sensor contains a plurality of VLSI transistors that are implemented as gates. These transistors are specifically chosen to be of a length and propagation time delay that will represent the limits of the VLSI circuit on which the embodiment has been implemented. Thus, when the delay through the sensor transistors equals the cycle time of the instantaneous frequency on the integrated circuit, the integrated circuit is operating efficiently. If the voltage drops, the transistors in the voltage sensor will slow down (take longer to propagate than the cycle time). This indicates that the cycle time is too short and that frequency should be reduced in order to avoid a timing failure. Conversely, if the voltage rises, the propagation of the sensor transistors is faster than one clock cycle, and frequency can be safely increased.

[0029] FIGURE 5 depicts an example voltage sensor that could be used with the above embodiments. Sensor 500 is connected to the power line supplying power from power source 501 to integrated circuit 502. Test devices 503 comprise sensor 500. These devices may be implemented as gates, simple transistors, or other components. Information regarding switching speed of these components is then transferred to a logic block.

[0030] Other embodiments of the present invention may use an analog to digital converter to actually measure the value of the delivered voltage. This measured number can then be used by indexing a table. FIGURE 6 shows an example flow chart depicting a method that may be implemented by certain embodiments of the present invention. The delivered voltage is applied 601 to a voltage sensor. This voltage is converted 602 to a numeric value, by a analog-to-digital converter for example. Then the embodiment may access 603 a table or database that associates voltage values with appropriate frequencies, and transmit 604 the frequency associated with the delivered voltage to a frequency synthesizer. The synthesizer can then adjust 605 the clock frequency to match. For example, if the delivered voltage is measured as 1.4 volts, an embodiment could index a table that showed 1.4 volts could sustain 1.9 GHz. 1.9 GHz is then sent to the frequency synthesizer as the new frequency. During the next clock cycle, the process could repeat. If 1.42 volts is measured in the next cycle, the table could be indexed again, the appropriate frequency re-determined, and the new frequency (for example, 1.93 GHz) sent to the synthesizer.

[0031] Temperature effects can also cause devices to run faster or slower than the designer anticipated value. In a hot environment, devices tend to slow down. Embodiments such as those describe by FIGURE 6 may require guardbanding to account for inaccuracies in a table or database brought about by temperature. However, embodiments such as those described by FIGURE 4 can have transistors in the sensor to determine how fast an integrated circuit can run at a given voltage that experience the same physical conditions, such as temperature, the integrated circuit as a whole is experiencing. Because the detector transistors will slow as the temperature rises in the same manner as the devices in the integrated circuit, no additional correction is needed.

[0032] FIGURE 7 is a timing diagram of the activities in the response loop. It shows a voltage drop 701 and how the regional voltage detectors slow down 702 in response to that drop 701. It further shows where that slow down is detected 703, how that information gets communicated back to the frequency synthesizer 704, and how the frequency synthesizers change the frequency that is seen subsequently at the components of the integrated circuit 705. Of course, the change in frequency is only useful when it is actually seen by the components on the integrated circuit that use the clock. With sudden changes in power consumption, steep voltage drops are seen. The faster the frequency changes in response to the voltage, the more efficient the system becomes. Ideally, frequency will remain very close to the maximum supported by the voltage. Some embodiments of the present invention incorporate voltage sensors that compare cycle time and synthesizers to supply the appropriate frequency. As a result, a system is provided where frequency follows along behind voltage, allowing the voltage to change freely based upon the power needs.

[0033] Many embodiments will find it advantageous to distribute multiple voltage sensors in several regions of an integrated circuit. Those of ordinary skill in the art will appreciate that the embodiments of the present invention are not limited to a single implementation of the arrangements depicted above. Some embodiments may have multiple voltage detectors, distributed as regional voltage detectors, as well as multiple frequency synthesizers. FIGURE 8 shows where the regional voltage detectors are and where the frequency synthesizers are located in one embodiment. Regional voltage sensors 801 are distributed across VLSI (Very Large Scale Integration) integrated circuit 800. These sensors 801 are able to sense the delivered voltage to a portion of VLS integrated circuit 800, and by means of frequency synthesizers 802, alter the frequency to different positions of the integrated circuit.

[0034] The frequency synthesizers 802 in some embodiments of the present invention can have the ability to "talk" to each other. If one frequency synthesizer 802 senses a voltage drop, i.e. the regional voltage detectors indicate a need to slow down, the frequency synthesizer associated with those detectors slow down immediately. This regional slow down can then be communicated to the other frequency synthesizer allowing them to follow. Remote ones, however, may slow down one or more cycles later. But because it takes a non-zero amount of time for voltage disturbances to propagate across the integrated circuit, the delay in slow down

is inconsequential from an operational prospective. Thus, the clock frequency on a integrated circuit may not be universal, as it would be in a preemptive system, the frequency may have a time and location variance. Aspects of some embodiments may account for this. If one region of the integrated circuit sees a change in frequency that another region has not yet experienced, phase error may occur between the two. However, such errors are well known in the art of VLSI design, and one of ordinary skill in the art could easily adapt a specific VLSI design to compensate for such skew without undue experimentation.

[0035] Certain embodiments of the present invention utilize the concept of average frequency. As voltage is varying, these embodiments of the present invention push the frequency very close to maximum for the voltage. As a result, the frequency varies with respect to location and with respect to time. Thus, the performance of the integrated circuit (usually well correlated with operating frequency) is sustained at an average frequency substantially higher than the minimum frequency that is the maximum at which a prior art integrated circuit can safely operate. The difference between these two values and the benefit gained is illustrated in FIGURE 3.

CLAIMS

What is claimed is:

1. A method of circuit control, comprising:
sensing a delivered voltage to a portion of an integrated circuit;
determining an appropriate frequency for the portion of the integrated circuit; and
providing the appropriate frequency to the integrated circuit.

2. The method of claim 1 wherein said sensing, determining; and providing are continuously repeated during the integrated circuit's operation.

3. The method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

4. The method of claim 1 further comprising:
applying the delivered voltage to constituent devices of a voltage sensor.

5. The method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.

6. The method of claim 4 further comprising:
further determining a switching speed of the constituent devices at the delivered voltage.

7. The method of claim 6 further comprising:
using the switching speed to determine the appropriate frequency.

8. The method of 4 further comprising:
exposing the voltage sensor and the portion to the integrated circuit to the same physical conditions.

9. The method of 8 wherein the physical conditions include temperature.

10. The method of claim 1 further comprising:
calculating a value for the delivered voltage.

11. The method of claim 10 further comprising:

using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.

12. A device for electronic circuit control comprising:

means for sensing a delivered voltage to a portion of an integrated circuit;

means for determining an appropriate frequency for the portion of the integrated circuit; and

means of providing the appropriate frequency to the portion of the integrated circuit.

13. The device of claim 12 further comprising:

means for determining the maximum possible frequency for the portion of the integrated circuit at the delivered voltage.

14. The device of claim 12 wherein said sensing means further comprises:

means for testing a switching speed of at least one test device at the delivered voltage.

15. The device of claim 12 wherein the at least one test device is similar to a circuit device comprising:

the portion of the integrated circuit.

16. The device of 14 further comprising:

means for using the switching speed as the appropriate frequency.

17. The device of 14 wherein the at least one test device and the circuit device are exposed to similar physical conditions.

18. The device of 17 wherein the physical conditions include temperature.

19. The device of claim 12 further comprising:

means for calculating a value for the delivered voltage.

20. The device of claim 19 wherein said calculating means includes analog-to-digital converter.

21. The device of claim 19 further comprising:

means for associating the value of the delivered voltage with a value for the appropriate frequency.

22. The device of claim 21 wherein said associating means includes a tabulation of possible values for the delivered voltage associated with a set of values for the appropriate frequency.

23. A system for circuit control comprising:

at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit;

at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit; and

at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.

24. The system of claim 23 wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

25. The system of claim 23 further comprising:

at least one test device to which the delivered voltage is applied.

26. The system of 25 at least one test device logic block to determine a switching speed of the at least one test device at the applied voltage.

27. The system of claim 26 wherein the switching speed is used to determine the appropriate voltage.

28. The system of claim 25 wherein the at least one test device is similar to a device that comprises the portion of the integrated circuit.

29. The system of claim 25 wherein the at least one test device and the portion of the integrated circuit are exposed to similar physical conditions.

30. The system of claim 29 wherein the physical conditions include temperature.

31. The system of claim 23 further comprising:

a converter to convert the delivered voltage to a value.

32. The system of claim 31 wherein the converter is an analog-to-digital converter.

33. The system of claim 23 further comprising:

a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.

34. The system of 33 wherein said table is a computer readable database.

ABSTRACT

One disclosed embodiment of the invention is directed to circuit control that comprises sensing a delivered voltage to a portion of an integrated circuit, determining an appropriate frequency for the portion of the integrated circuit, and providing the appropriate frequency to the integrated circuit.

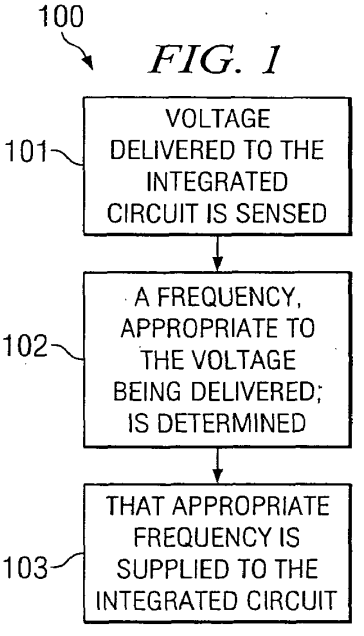


FIG. 1

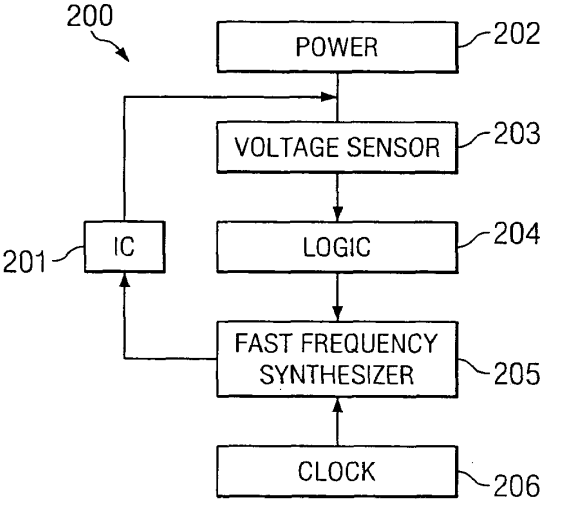


FIG. 2

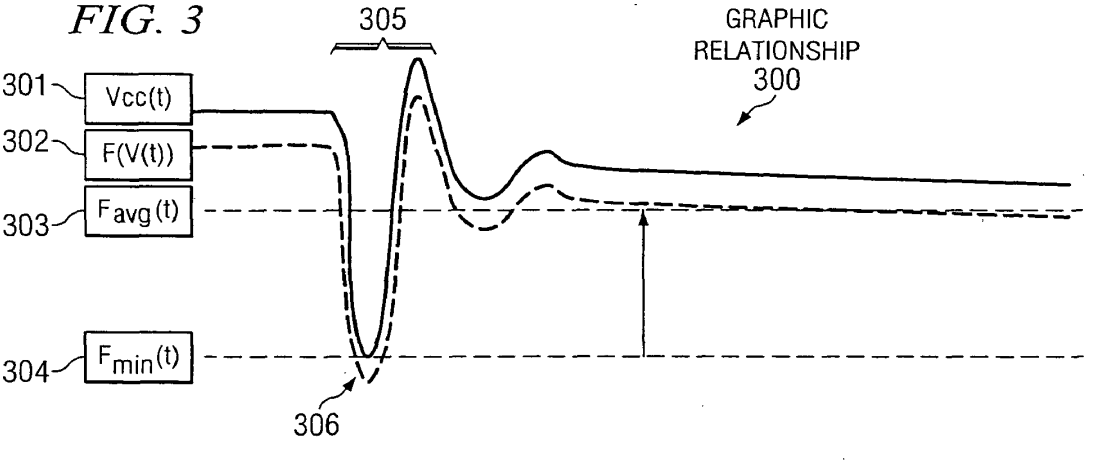


FIG. 3

FIG. 4

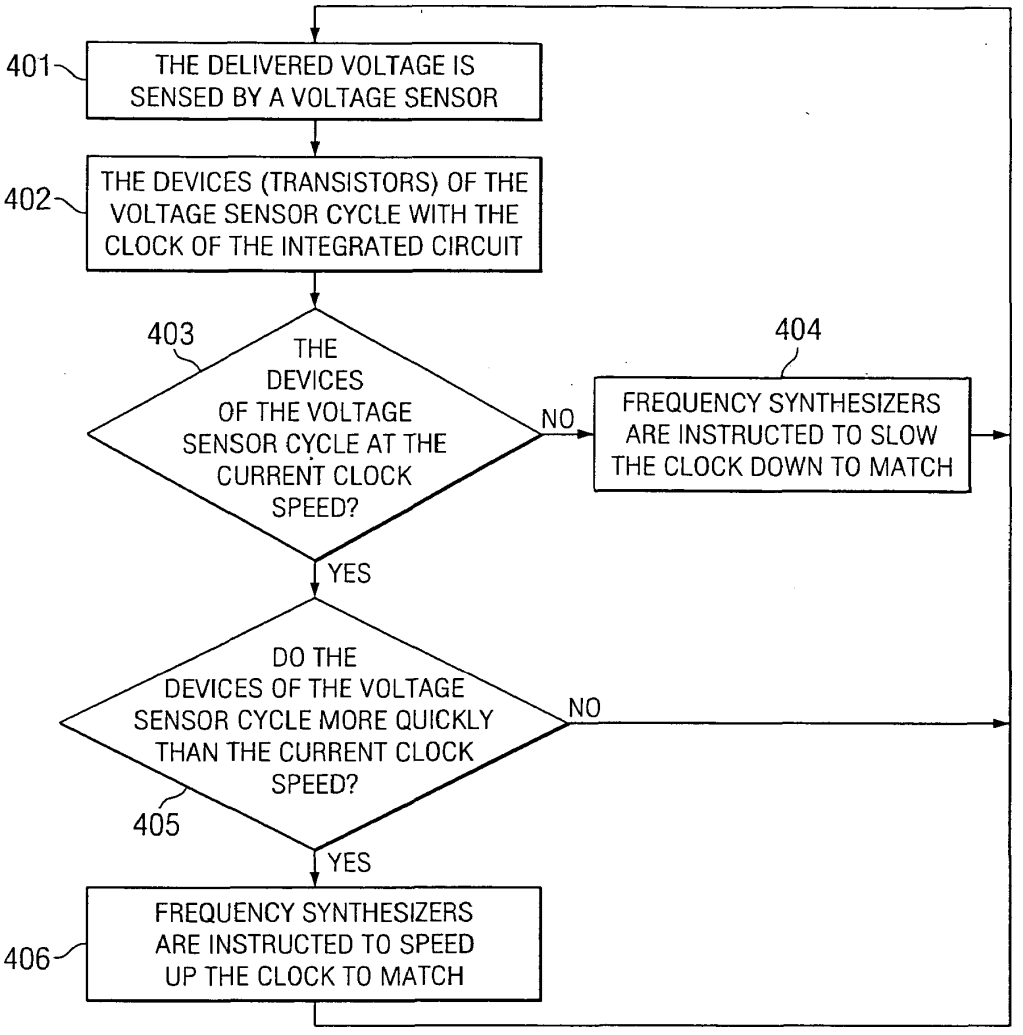

401
THE DELIVERED VOLTAGE IS SENSED BY A VOLTAGE SENSOR
402
THE DEVICES (TRANSISTORS) OF THE VOLTAGE SENSOR CYCLE WITH THE CLOCK OF THE INTEGRATED CIRCUIT
403
THE DEVICES OF THE VOLTAGE SENSOR CYCLE AT THE CURRENT CLOCK SPEED?
NO
404
FREQUENCY SYNTHESIZERS ARE INSTRUCTED TO SLOW THE CLOCK DOWN TO MATCH
YES
DO THE DEVICES OF THE VOLTAGE SENSOR CYCLE MORE QUICKLY THAN THE CURRENT CLOCK SPEED?
NO
405
YES
406
FREQUENCY SYNTHESIZERS ARE INSTRUCTED TO SPEED UP THE CLOCK TO MATCH

FIG. 5

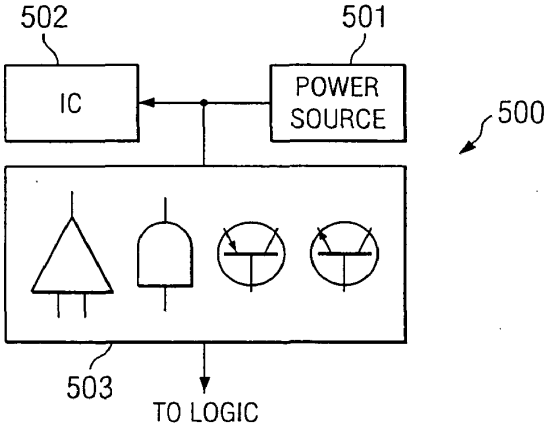

502
501
IC
POWER SOURCE
500
503
TO LOGIC

FIG. 6

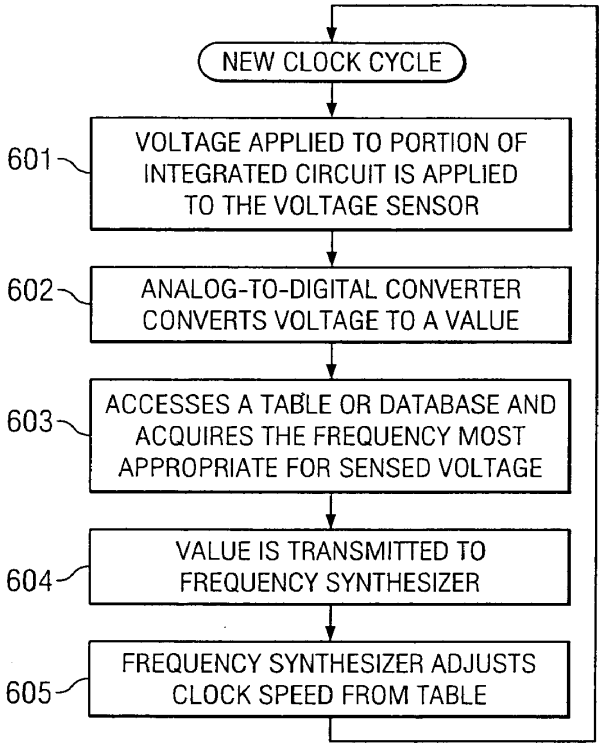
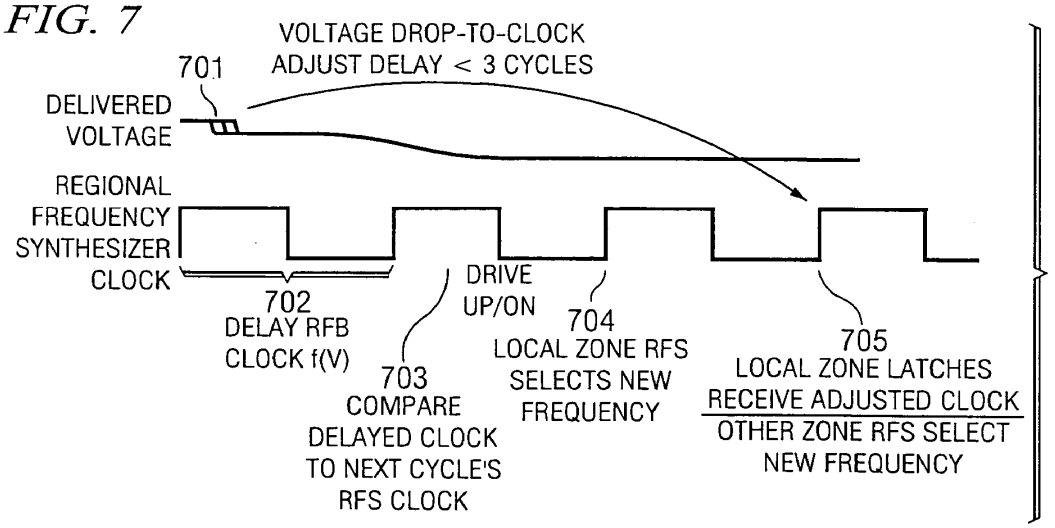

NEW CLOCK CYCLE
601
VOLTAGE APPLIED TO PORTION OF INTEGRATED CIRCUIT IS APPLIED TO THE VOLTAGE SENSOR
602
ANALOG-TO-DIGITAL CONVERTER CONVERTS VOLTAGE TO A VALUE
603
ACCESSES A TABLE OR DATABASE AND ACQUIRES THE FREQUENCY MOST APPROPRIATE FOR SENSED VOLTAGE
604
VALUE IS TRANSMITTED TO FREQUENCY SYNTHESIZER
605
FREQUENCY SYNTHESIZER ADJUSTS CLOCK SPEED FROM TABLE

FIG. 7


VOLTAGE DROP-TO-CLOCK ADJUST DELAY < 3 CYCLES
701
DELIVERED VOLTAGE
REGIONAL FREQUENCY SYNTHESIZER CLOCK
702
DELAY RFB CLOCK f(V)
703
COMPARE DELAYED CLOCK TO NEXT CYCLE'S RFS CLOCK
DRIVE UP/ON
704
LOCAL ZONE RFS SELECTS NEW FREQUENCY
705
LOCAL ZONE LATCHES RECEIVE ADJUSTED CLOCK
OTHER ZONE RFS SELECT NEW FREQUENCY

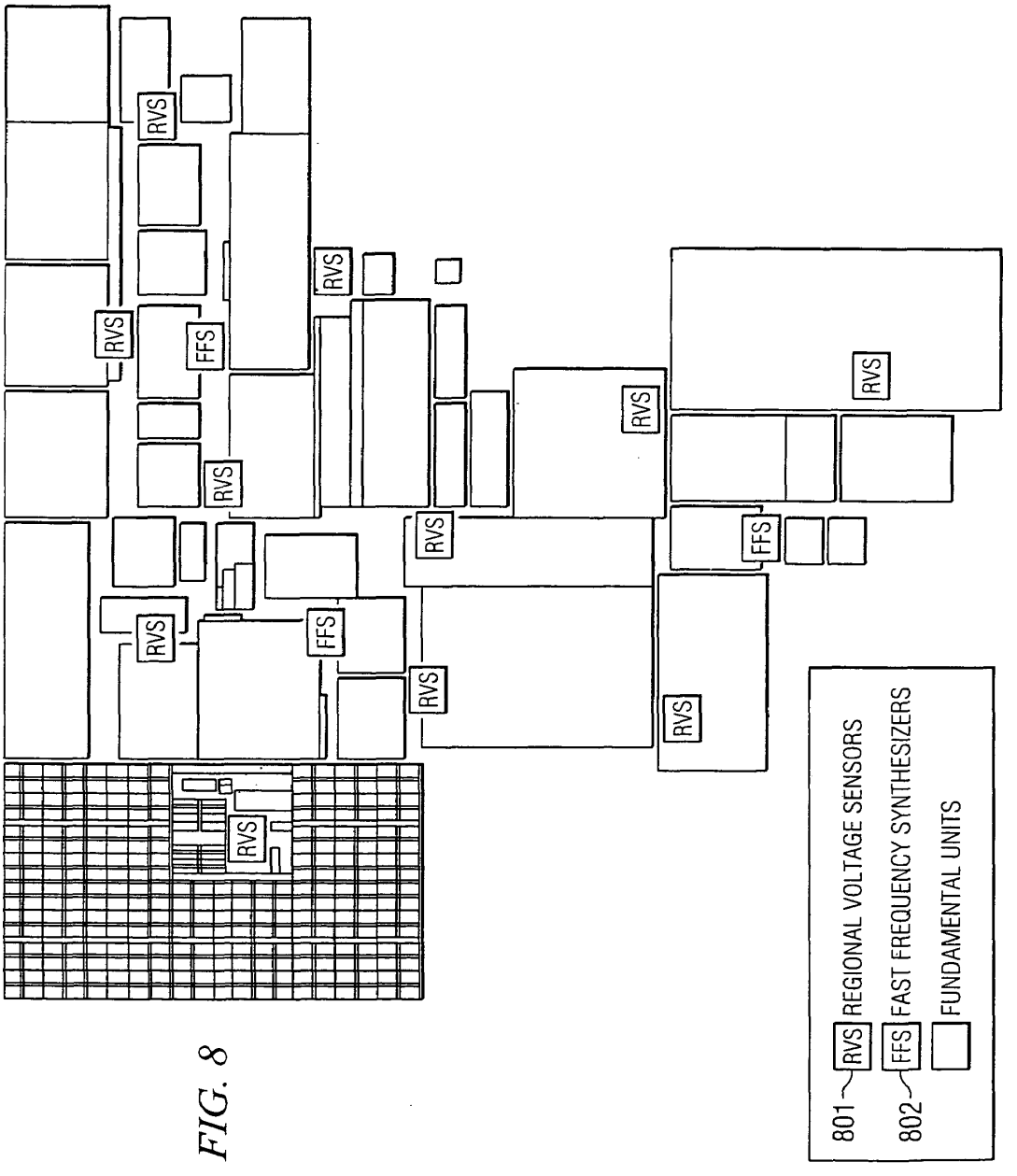

RVS
FFS
801
802
REGIONAL VOLTAGE SENSORS
FAST FREQUENCY SYNTHESIZERS
FUNDAMENTAL UNITS

FIG. 8

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 200208753-2

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND DEVICE FOR CIRCUIT CONTROL

the specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Customer Number 022879

Place Customer Number Bar Code Label here

Send Correspondence to:	**Direct Telephone Calls To:**
HEWLETT-PACKARD COMPANY **Intellectual Property Administration** **P.O. Box 272400** **Fort Collins, Colorado 80527-2400**	**William P. O'Meara** **970-898-7917**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Samuel D. Naffziger **Citizenship:** United States

Residence: 3749 Ashmount Drive, Fort Collins, Colorado 80525

Post Office Address: sam as residenc

Samuel D Naffziger
Inventor's Signature

8-28-03
Date

Rev 05/03 (DecPwr) (Use Page Two For Additional Inventor(s) Signature(s))

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 200208753-2

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	34	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	34 minus 20=	* 14
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	252
X42=		OR	X84=	0
+140=		OR	+280=	0
TOTAL		OR	TOTAL	1002

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

09/03/2003 STEUBEL1 00000007 082025 10651360

01 FC:1001 750.00 DA
02 FC:1202 252.00 DA

PTO-1556
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