
DESIGN FOR AT-SPEED TEST, DIAGNOSIS AND MEASUREMENT

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SM Scan Mode.

SOC System on a Chip. Devices created by using VDSM technology. With SOC's, the vast availability of gates is used to integrate analog circuitry, blocks of logic, memories, and processors on a single chip.

source Used to refer to the test stimuli generator. A source can be either on chip (BIST) or off chip (external ATE). Usually connected to an embedded core via a TAM.

SRAM Static RAM. A type of semiconductor memory in which a pair of flip-flops is cross-coupled to hold a binary state as long as power is applied.

structural test A test process based on a pattern set that has a known defect or fault coverage. This testing is used for manufacturing. Structural testing involves strategies to verify the individual elements of the design: logic gates, transistors, and interconnects.

subblock A subdivision within a *design block*. Sample subblocks are *cores*, memories, and UDL.

SVF Serial Vector Format. A board-level test pattern format used with IEEE 1149.1 board test software. SVF was jointly developed by ASSET InterTech and Teradyne.

synchronous testpoints Testpoints that require one or more clocks to reset them.

system chip A system integrated on a chip. Included are one or more cores with UDL integrated by the core user or system integrator.

TAP Abbreviation for the five-pin, IEEE 1149.1 Test Access Port.

The IEEE 1149.1 TAP defines a chip-level test structure that is used to implement a simplified board and system-level test strategy. External test processors control and communicate with various test features built into a design through the TAP. The TAP is used to initialize BIST operations, start BIST, monitor status, and output results.

The five pins of the TAP are TDI, TDO, TCK, TMS, and TRST.

TCK Dedicated Test Clock. This mandatory terminal of the TAP is driven by the clock that controls the synchronous operation of the TAP.

TDI Test Data-In. Serial test data shifted in with a default value of 1. A mandatory terminal of the TAP.

TDO Test Data-Out. Serial test data shifted out with a default value of Z. This mandatory terminal of the TAP is only active during a shift operation.

TDR Test Data Register.

terminal Connections at the input and output of a core. The term *node* is sometimes used but *terminal* is the preferred term.

test access mechanism (TAM) Logic that provides data transport between sources of test stimuli and embedded cores and between embedded cores and test response evaluators or sinks. The core integrator adds TAM features to deliver data to the core wrappers or cores. The TAM delivers test data between cores and various pins of the chip. The TAM also delivers dynamic controls the cores or wrappers.

testbenches Output from the Verify tools that initializes and executes tests then returns test completion values. (DONE flags, pass/fail signals). These testbenches also provide diagnostic information useful for debugging. These testbenches provide input to simulation tools.