

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Naffziger
U.S. Patent No.: 7,224,563 Attorney Docket No.: 44508-0023IP2
Issue Date: May 29, 2007
Appl. Serial No.: 10/651,360
Filing Date: August 29, 2003
Title: METHOD AND DEVICE FOR CIRCUIT CONTROL

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,224,563 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

MTK-1001	U.S. Patent No. 7,224,563 to Naffziger (“the ’563 patent”)
MTK-1002	Excerpts from the Prosecution History of the ’563 patent
MTK-1003	Declaration of Paul Min, Ph.D.
MTK-1004	U.S. Patent No. 6,762,629 to Tam et al. (“Tam”)
MTK-1005	U.S. Patent No. 6,885,233 to Huard et al. (“Huard”)
MTK-1006	U.S. Patent No. 6,853,259 to Norman et al. (“Norman ’259”)
MTK-1007	U.S. Patent Pub. No. 2003/0034851 to Norman et al. (“Norman ’851”)
MTK-1008	U.S. Patent No. 6,509,788 to Naffziger et al. (“Naffziger ’788”)
MTK-1009	Excerpts from Microsoft Computer Dictionary, Fifth Edition, Microsoft Press (2002)
MTK-1010	Excerpts from Modern Dictionary of Electronic, Seventh Edition Revised and Updated, Rudolf F. Graf (1999)
MTK-1011	Excerpts from Design For At-Speed Test, Diagnosis and Measurement, Kluwer Academic Publishers (2000)
MTK-1012	Excerpts from The Computer Engineering Handbook, CRC Press LLC (2002)
MTK-1013	U.S. Patent No. 5,428,790 to Harper et al. (“Harper”)
MTK-1014	U.S. Patent No. 6,489,834 to Naffziger et al. (“Naffziger ’834”)
MTK-1015	Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherine K. Vidal (USPTO June 21, 2022)

MTK-1016	Stipulation
MTK-1017	Syllabus to ESE 232 Introduction to Electronic Circuits
MTK-1018	Excerpts from Microelectronic Circuits, Fourth Edition, Sedra et al., Oxford University Press (1998)
MTK-1019	Affidavit of Service On MediaTek USA, Inc. in <i>Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.</i> , Case No. 2:23-cv-00129 (March 30, 2023)
MTK-1020	Declaration of June Ann Munford

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A method of circuit control, comprising:
1[a]	sensing a delivered voltage to a portion of an integrated circuit;
1[b]	determining an appropriate frequency for the portion of the integrated circuit; and
1[c]	providing the appropriate frequency to said portion of said integrated circuit.
Claim 2	
2	The method of claim 1 wherein said sensing, determining, and providing are continuously repeated during the integrated circuit's operation.
Claim 3	
3	The method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.
Claim 4	
4	The method of claim 1 further comprising: applying the delivered voltage to constituent devices of a voltage sensor.
Claim 5	
5	The method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.
Claim 6	
6	The method of claim 4 further comprising: further determining a switching speed of the constituent devices at the delivered voltage.

Claim 7	
7	The method of claim 6 further comprising: using the switching speed to determine the appropriate frequency.
Claim 8	
8	The method of claim 4 further comprising: exposing the voltage sensor and the portion of the integrated circuit to the same physical conditions.
Claim 9	
9	The method of claim 8 wherein the physical conditions include temperature.
Claim 10	
10	The method of claim 1 further comprising: calculating a value for the delivered voltage.
Claim 11	
11	The method of claim 10 further comprising: using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.
Claim 23	
23[p]	A system for circuit control comprising:
23[a]	at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit;
23[b]	at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit; and
23[c]	at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.

Claim 24	
24	The system of claim 23, wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.
Claim 31	
31	The system of claim 23 further comprising: a converter to convert the delivered voltage to a value.
Claim 32	
32	The system of claim 31 wherein the converter is an analog-to-digital converter.
Claim 33	
33	The system of claim 23 further comprising: a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.
Claim 34	
34	The system of claim 33 wherein said table is a computer readable database.
Claim 35	
35[p]	A system for circuit control comprising:
35[a]	a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit;
35[b]	a plurality of logic blocks arranged to determine an appropriate frequency for each said portion from said delivered voltages; and
35[c]	a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.

MediaTek Inc. (“Petitioner” or “MediaTek”) petitions for *Inter Partes* Review (“IPR”) of claims 1-11, 23-24, and 31-35 (“Challenged Claims”) of U.S. Patent No. 7,224,563 (“the ’563 patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’563 patent is available for IPR. Petitioner is not barred or estopped from requesting this review of the Challenged Claims. The present Petition is filed within one year of service of a complaint against Petitioner in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023).

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds below. Dr. Paul Min provides supporting explanations in his Declaration (MTK-1003, ¶¶1-236) cited throughout this petition.

Ground	Claims	Basis	References
1	1-10, 23-24, 31, 32, 35	§103	Tam
2	1-11, 23-24, 31-35	§103	Tam and Huard
3	1-11, 23-24, 31-35	§103	Norman ’259 and Norman ’851
4	1, 3, 10, 23, 24, 31, 32, 35	§103	Naffziger ’788

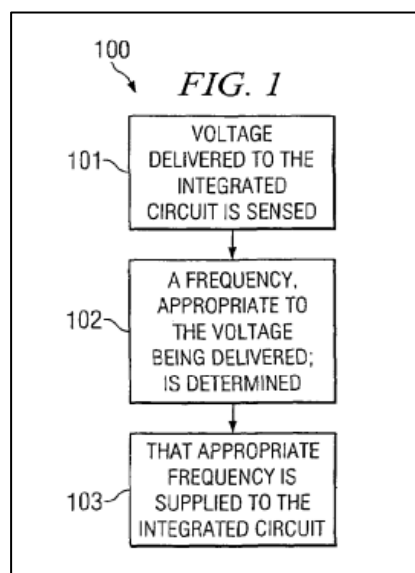
Each reference pre-dates the ’563 patent’s earliest possible priority date (June 20, 2003; “Critical Date”) and qualifies as prior art.

Reference	Date	Prior Art Under
Tam	7/26/2002 (filed)	§102(e)
Huard	5/2/2002 (filed)	§102(e)
Norman '259	8/15/2001 (filed)	§102(e)
Norman '851	2/20/2003 (published)	§102(a)/(e)
Naffziger '788	1/21/2003 (issued)	§102(a)

II. THE '563 PATENT

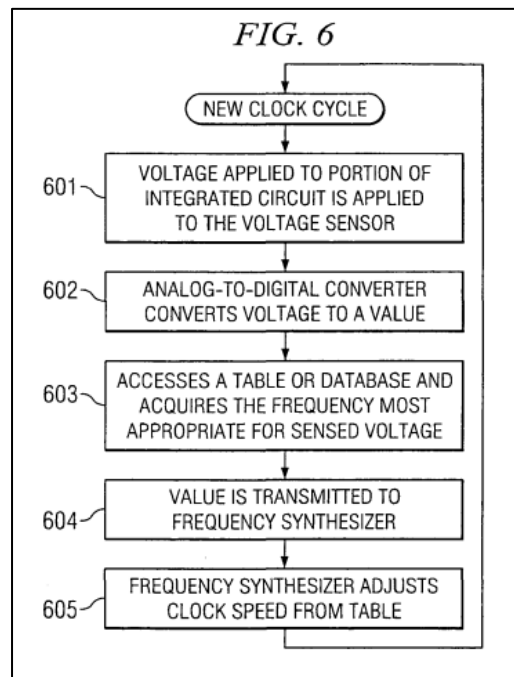
A. Brief Description

The '563 patent discloses a method and device for circuit control that broadly comprises: (1) sensing a delivered voltage to a portion of an integrated circuit; (2) determining an appropriate frequency for the portion of the integrated circuit based on that sensed voltage; and (3) providing the appropriate frequency to the portion of the integrated circuit. MTK-1001, Abstract, 3:46-50, 4:22-24, 4:25-37, 4:43-52, claims 1, 23, and 35; MTK-1003, ¶39.



MTK-1001, FIG. 1

According to the '563 patent, “[v]oltage sensors ... provide a means of detecting the voltage actually delivered to an integrated circuit,” and “[i]t may be advantageous,” though not necessary, “to have a number of voltage sensors distributed across an entire die.” MTK-1001, 4:9-17; MTK-1003, ¶40. “A frequency determining means is used to determine what [clock] frequency is appropriate for the integrated circuit (or a portion thereof) at the voltage delivered.” MTK-1001, 4:22-24. “Typically, this frequency is derived directly from the delivered voltage.” MTK-1001, 4:34-35. One way of doing this is to use “an analog to digital converter to ... measure the value of the delivered voltage,” MTK-1001, 5:49-51, “access ... a table or database that associates voltage values with appropriate frequencies,” and transmit the frequency associated with the delivered voltage “to a frequency synthesizer” to “adjust ... the clock frequency,” *id.* at 5:57-62; *see also id.* at claims 10-11 at 31-34.



MTK-1001, FIG. 6

B. Summary of the Prosecution History

U.S. Application No. 10/651,360, which resulted in the '563 patent, was filed August 29, 2003, claiming priority to U.S. Provisional Patent Application No. 60/480,056, filed June 20, 2003. MTK-1002, 41, 50; MTK-1003, ¶¶41-48.

On October 3, 2003, the Applicant amended the specification "to include reference to U.S. Provisional Patent Application No. 60/480,056" and amended claims 2, 8, 9, 15-18, 26, and 34 "to correct typographical errors." MTK-1002, 46.

In a Non-Final Office Action dated August 8, 2006, all then-pending claims (i.e., claims 1-32) were rejected "under 35 U.S.C. 102(b) as being anticipated by Tam et al (6,762,629) or Huard et al (6,885,233)" and "on the ground of

nonstatutory obviousness-type double patenting [“OTDP”] ... over claims 1-6 of U.S. Patent No. 6,927,605.” MTK-1002, 25-29.

On November 13, 2006, the Applicant responded to the August 8, 2006 Office Action. MTK-1002, 16-23. With respect to the 102(b) rejections, the Applicant did not dispute that both Tam and Huard expressly teach the method and device for circuit control embodied in then-pending claims 1-32; rather, the Applicant argued only that, due to their respective dates of publication, “neither *Tam* nor *Huard* are prior art under 35 U.S.C. § 102(b).” MTK-1002, 23. With respect to the OTDP rejection, the Applicant argued that the Examiner had failed to show “that which is required for making a *prima facie* rejection of obviousness.” MTK-1002, 22-23. The Applicant also “amended claim 1 and 12 to more clearly describe the claimed subject matter,” e.g., by clarifying that the “appropriate frequency for the portion of the integrated circuit” is provided to “said portion of said integrated circuit,” *id.* at 18, and added claim 35. MTK-1002, 22; MTK-1003, ¶46.

On February 22, 2007, in response to Applicant’s remarks, claims 1-35 were allowed, MTK-1002, 9-15, and the ’563 patent issued on May 29, 2007, *id.* at 7.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science degree in electrical engineering, computer engineering,

computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. MTK-1003, ¶24.

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. For purposes of this proceeding only, Petitioner submits that no claim term requires a formal construction for purposes of addressing the Grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Petitioner reserves the right to respond to any constructions offered/adopted by Patent Owner/Board. Petitioner does not concede that each challenged claim satisfies all statutory requirements and does not waive any arguments concerning grounds that can only be raised in district court.

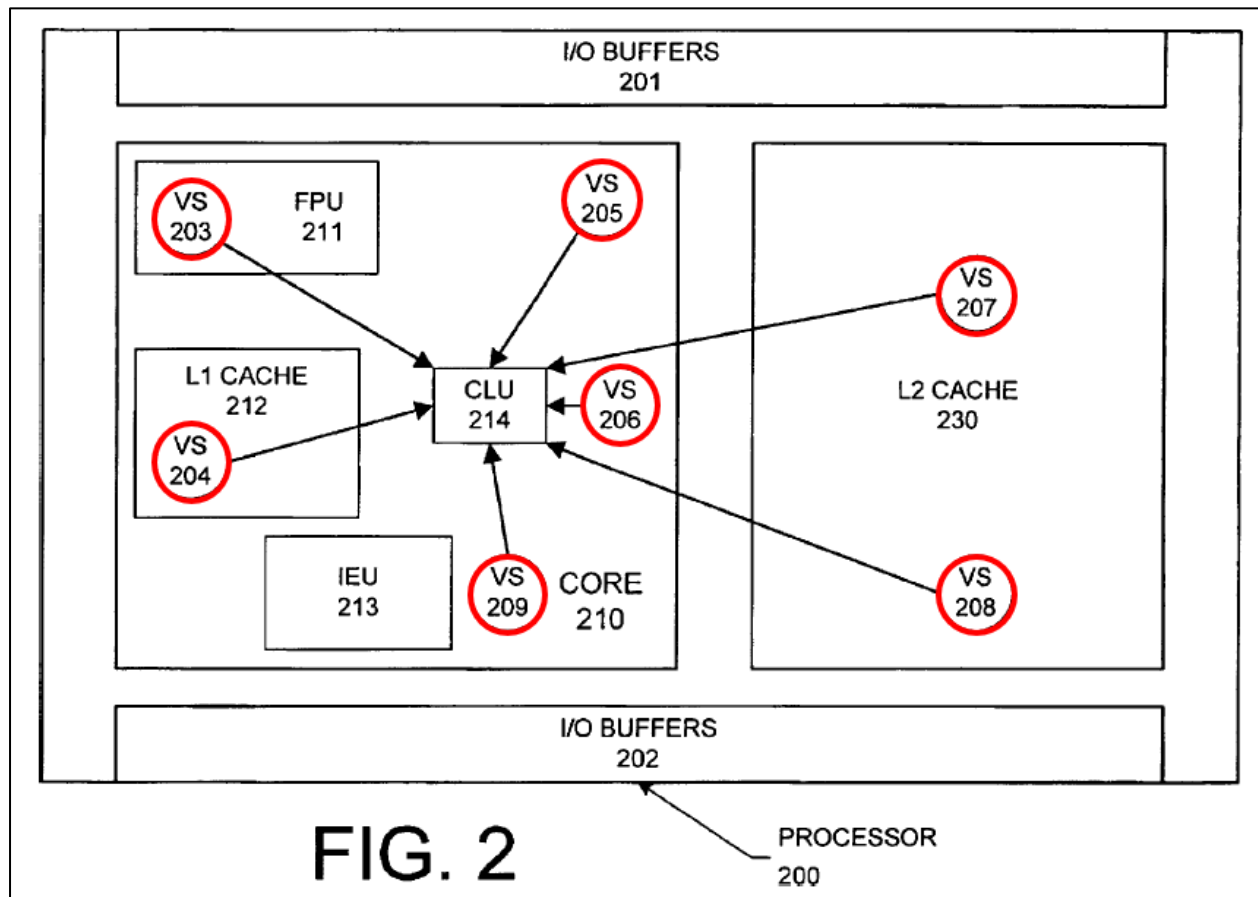
III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1—Claims 1-10, 23-24, 31, 32, and 35 are obvious over Tam

1. Overview of Tam

Tam relates to “[a] method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes.” MTK-1004, Abstract; MTK-1003, ¶52. Specifically, Tam discloses “voltage sensors” that “can be

strategically placed at various” portions of an integrated circuit to sense delivered “VCC supply voltages” and “get an accurate and useful view of the power environment.” MTK-1004, 5:46-53 (e.g., “high voltage circuitry, critical circuits, power bussing, and high speed logic”), 5:62-65.



MTK-1004, FIG. 2¹

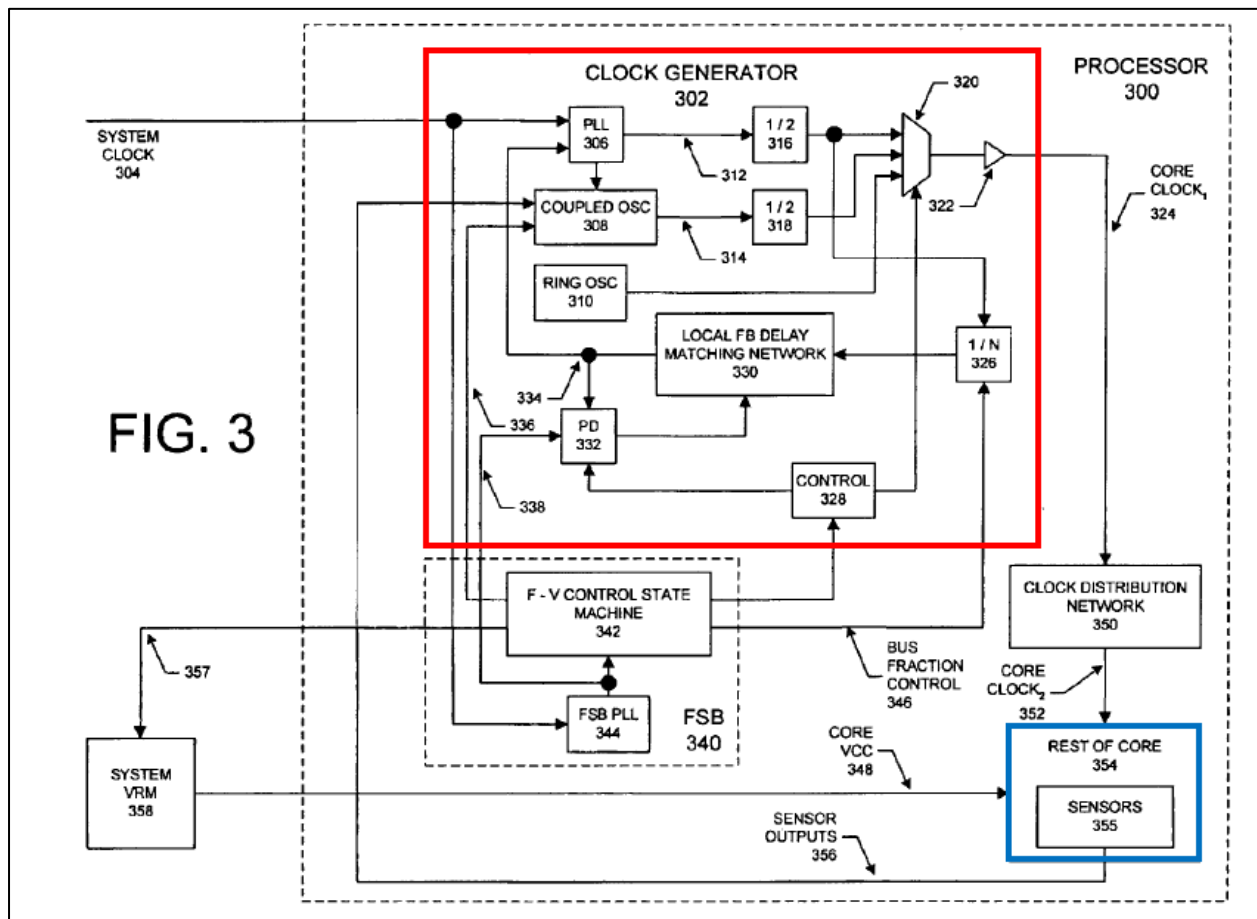
For example, in the embodiment illustrated in FIG. 2, above, “a network of voltage sensors [203, 204, 205, 206, 209] are distributed in the [processor] core,”

¹ Annotations and color added unless otherwise noted.

i.e., a portion of the integrated circuit. MTK-1004, 5:62-63; MTK-1003, ¶¶52-54.

“These sensors,” shown in red above, “are to detect the local VCC voltage levels and to communicate that information back to the clock generator[.]” MTK-1004, 6:7-9. “Logic in the clock generator 214 monitors the voltage statuses and can dynamically adapt and adjust the clock frequency based on the sensed information.” *Id.* at 6:9-12. “[W]hen a droop is detected, the clock is slowed down to accommodate the reduced voltage level. Similarly, when the voltage recovery is detected, the clock frequency can be increased to enhance performance.” *Id.* at 3:47-50; *id.* at 6:19-23. By “dynamically adjusting the clock frequency based on sensed on-die voltage changes,” Tam’s circuit “control technique” “provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.” *Id.* at 3:44-4:5.

Tam’s FIG. 3, like FIG. 2, is “a block diagram of a processor architecture having a mechanism for dynamically adjusting a clock frequency in order to adapt to varying supply voltages.” MTK-1004, 6:33-36.



MTK-1004, FIG. 3

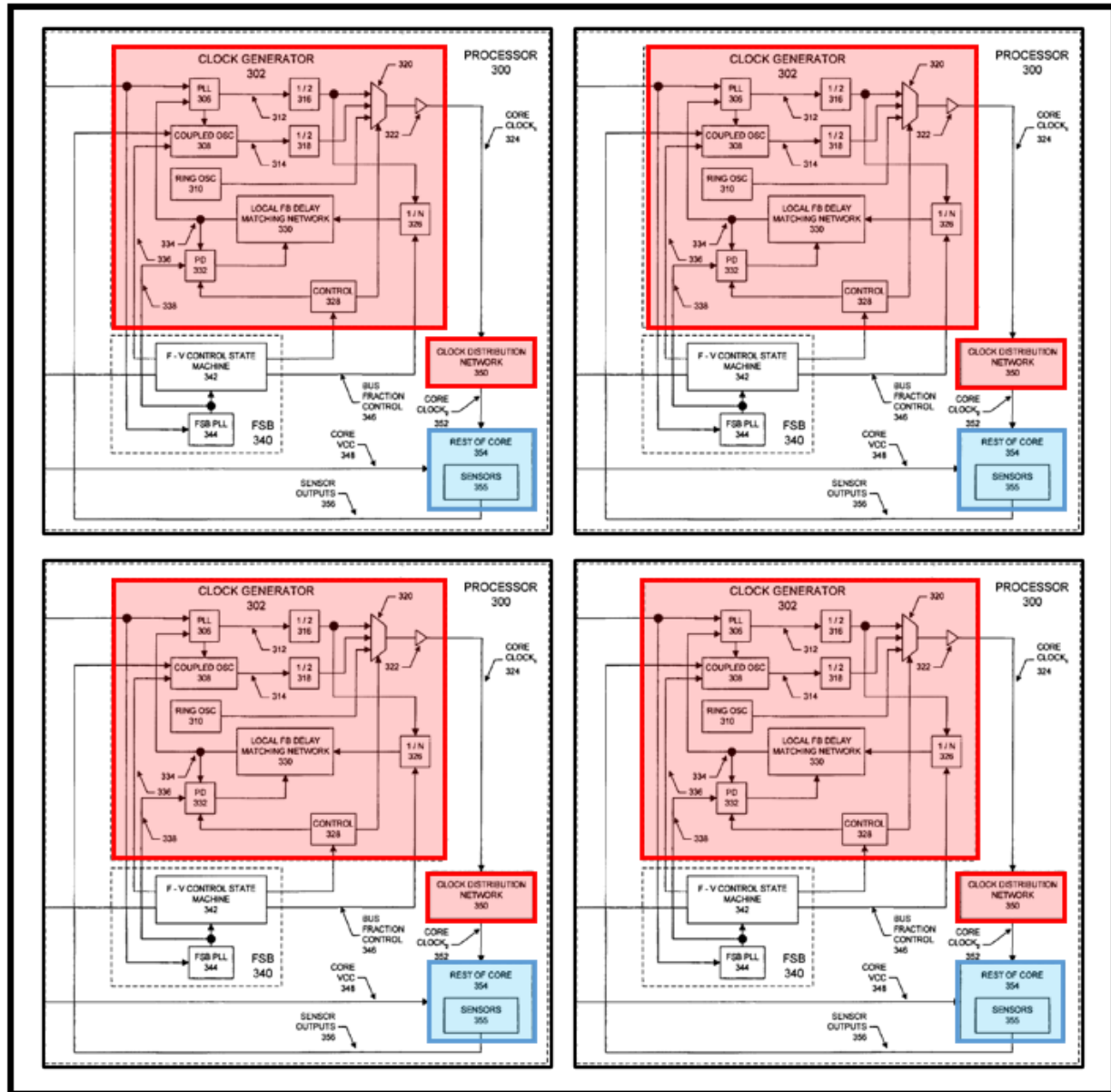
“The clock generator 302,” shown in red, “is a VCC adaptive dynamically variable frequency clock system capable of varying the frequency of its clock output” to the processor core, shown in blue, “in response to voltage sensors 355,” *id.* at 6:38-44, which are “distributed around the processor die,” *id.* at 7:39-41, as in FIG. 2.

MTK-1003, ¶55²; *see also id.* at ¶56 (discussing clock generator of FIG. 4).

Tam's teachings are applicable to both single-processor and multiprocessor systems. MTK-1004, 13:12-18; MTK-1003, ¶57. "In a multiprocessor system," Tam's "method can be performed concurrently in each processor," wherein "[e]ach processor can contain an adaptive variable frequency clock system," including a clock generator and a clock distribution network, shown in red below, that can (1) adjust "its own frequency and voltage settings independent of the other processors in the system," and (2) provide an updated clock frequency to each processors' core, shown in blue below, in response to voltage variations sensed by voltage sensors located within the cores. MTK-1004, 13:12-18; MTK-1003, ¶57.

² FIGS. 2 and 3 of Tam are not limited to specific embodiments; rather both generally depict a "block diagram of a processor ... in accordance with the present invention." MTK-1004, 5:46-48; *id.* at 6:33-36 (same); MTK-1003, ¶53. "[L]ike references" in FIGS. 2-3 "indicate similar elements." MTK-1004, 1:64-66.

Multiprocessor Circuit

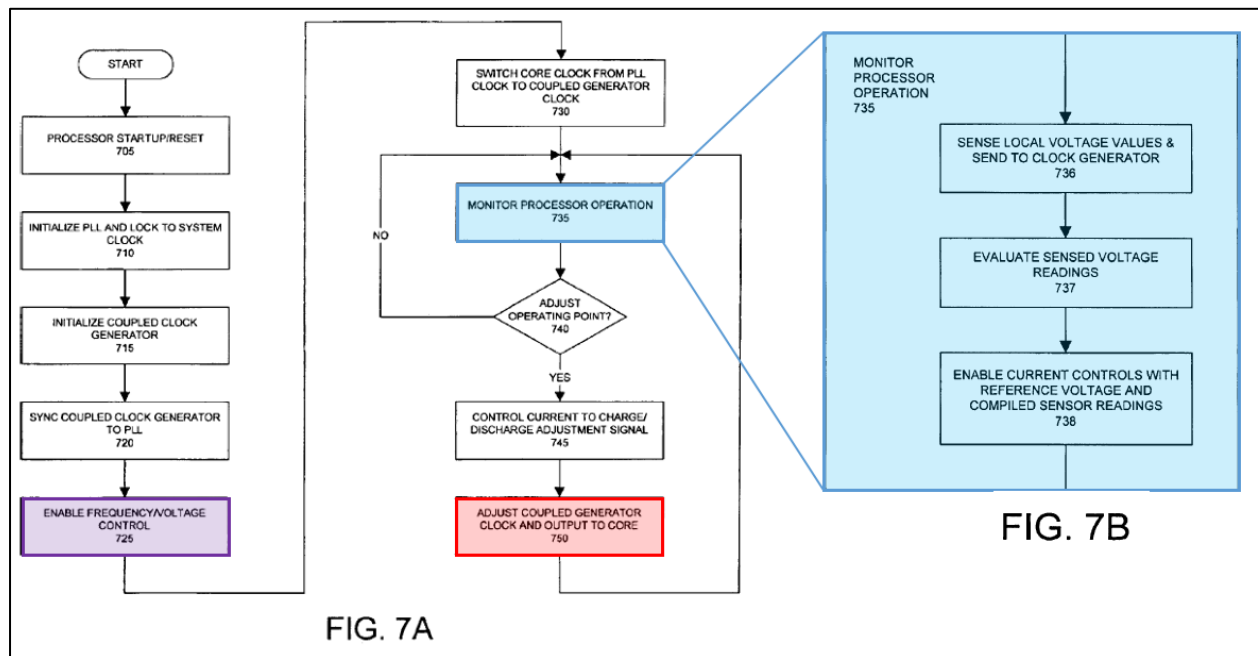


MTK-1003, ¶57 (Tam's FIG. 3 processor in potential multiprocessor system)

2. Claim 1

(a) Element 1[p]

To the extent the preamble is limiting,³ Tam discloses a method of circuit control. *Infra* 1[a]-1[c]; MTK-1004, Abstract, 2:30-40, 3:67-4:5, claim 8 (claiming method); MTK-1003, ¶58. Specifically, Tam discloses a circuit “control technique,” i.e., method, that “implements on-die voltage sensing” to “detect voltage fluctuations and reduce the operating frequency as needed to match the detected VCC voltage decrease.” MTK-1004, 3:67-4:5. One embodiment of this method is depicted in FIGS. 7A-B:



MTK-1004, FIGS. 7A-B

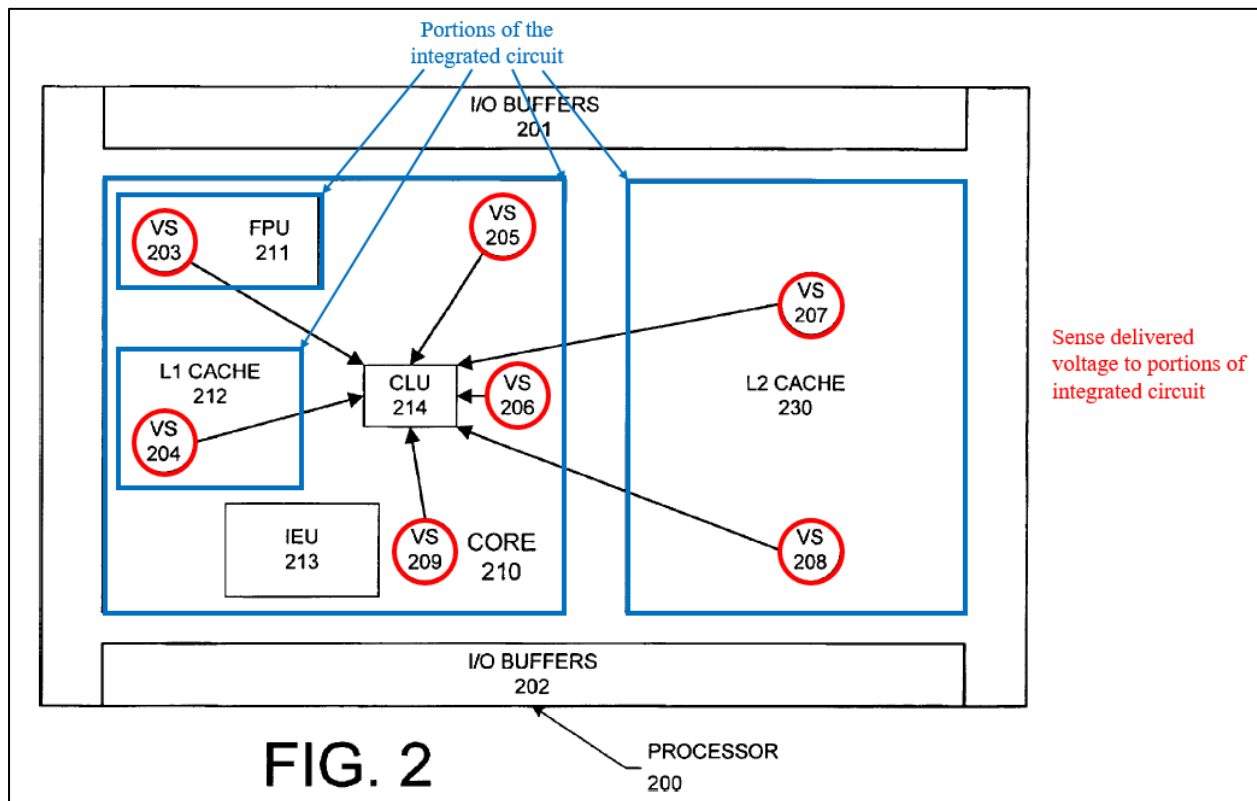
Among the steps described in Tam, “[t]he frequency/voltage control logic is

³ Petitioner reserves the right to argue in counterpart litigation that the preamble is not limiting.

enabled at block 725” (purple). MTK-1004, 12:24-25. Thereafter, “the processor operation is monitored” at block 735 (blue), where the monitoring includes “sens[ing] the local voltage values and send[ing] the data to the clock generator,” “evaluat[ing] the sensed voltage readings,” and enabling “[t]he current control blocks that can shift the adjustment signal.” MTK-1004, 12:33-47. Finally, “[a]t block 750” (red) “the new frequency setting takes effect,” and the “clock signal is adjusted and is outputted to the processor core.” MTK-1004, 13:6-9.

(b) Element 1[a]

Tam discloses sensing a delivered voltage to a portion of an integrated circuit. MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 11:24-28, 12:14-11, 12:30-64, FIGS. 1-7B, claims 1-30; MTK-1003, ¶¶59-61. Specifically, Tam discloses a circuit “control technique” that includes “on-die voltage sensing” using “sensors [that] can detect voltage fluctuations[.]” MTK-1004, 3:67-4:5; *id.* at 3:44-46. Tam expressly teaches that its “on-die voltage sensors ... can be strategically placed at various locations” on an integrated circuit, i.e., portions of an integrated circuit, “such as high voltage circuitry, critical circuits, power bussing, and high speed logic, for example.” MTK-1004, 5:46-53; *id.* at 7:40-41, 8:31-36 (“These sensors are to detect the voltage of the supply available to the surrounding circuitry[.]”), 14:43, Abstract, FIG. 7B.



MTK-1004, FIG. 2

While Tam teaches that “the number of sensors can vary” and that the “sensors are designer/application specific,” MTK-1004, 5:65-6:1, a POSITA would have recognized that each of Tam’s “on-die voltage sensors” is sensing a delivered voltage to a portion of an integrated circuit, whether it be the “FPU,” “L1 Cache,” processor “core,” or “L2 Cache.” MTK-1003, ¶61; MTK-1004, FIG. 2, 6:3-7. Moreover, a POSITA would have found it obvious to utilize a plurality of voltage sensors, as in Tam, to “determine how the supply voltage is distributed across the processor,” MTK-1004, 12:38-39, because doing so provides “an accurate and useful view of the power environment,” *id.* at 5:62-65. MTK-1003, ¶61.

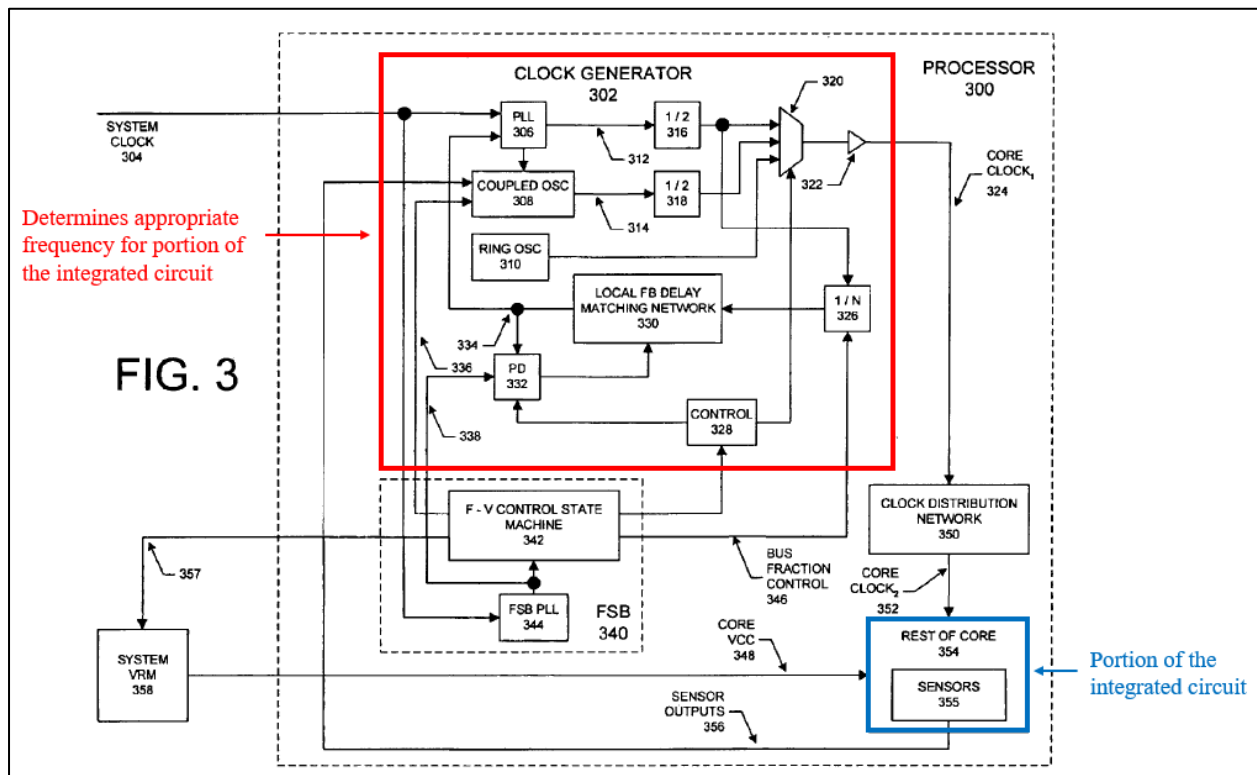
(c) Element 1[b]

Tam discloses determining an appropriate frequency for the portion of the integrated circuit. MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 12:4-11, 12:30-64, FIGS. 1-7B, claims 1-30; MTK-1003, ¶¶62-64. Specifically, Tam teaches “[a] method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes.” MTK-1004, Abstract; *id.* at 2:30-40. For example, after receiving data from voltage sensors associated with a portion of the integrated circuit, such as the processor core,⁴ “the dynamic frequency adjustment circuit” can “evaluate the supply voltage conditions and dynamically adapt the clock oscillator output,” i.e., the clock signal/frequency, “*appropriately*.”⁵ MTK-1004, 8:37-40; *id.* at 6:33-45 (“The clock generator” “is a VCC adaptive dynamically variable frequency clock system capable of varying the frequency of its clock output in response to voltage sensors[.]”); 7:34-35; MTK-1003, ¶62. The exemplary embodiment shown in FIG. 3 below depicts the clock generator 302 determining and providing an “appropriate frequency,” e.g., “CORE CLOCK,” to the processor core 354, representing a portion of the integrated circuit, via a clock

⁴ “[V]oltage sensors ... are distributed in the core.” MTK-1004, 5:62-63.

⁵ Emphasis added throughout unless otherwise noted.

distribution network 350. MTK-1004, FIG. 3; MTK-1003, ¶63.



MTK-1004, FIG. 3

“[W]hen a droop is detected” by a voltage sensor located at a portion of the integrated circuit, “the clock is slowed down to accommodate the reduced voltage level... [W]hen the voltage recovery is detected, the clock frequency can be increased to enhance performance.” MTK-1004, 3:44-50; *id.* at 6:19-23, FIG. 4.

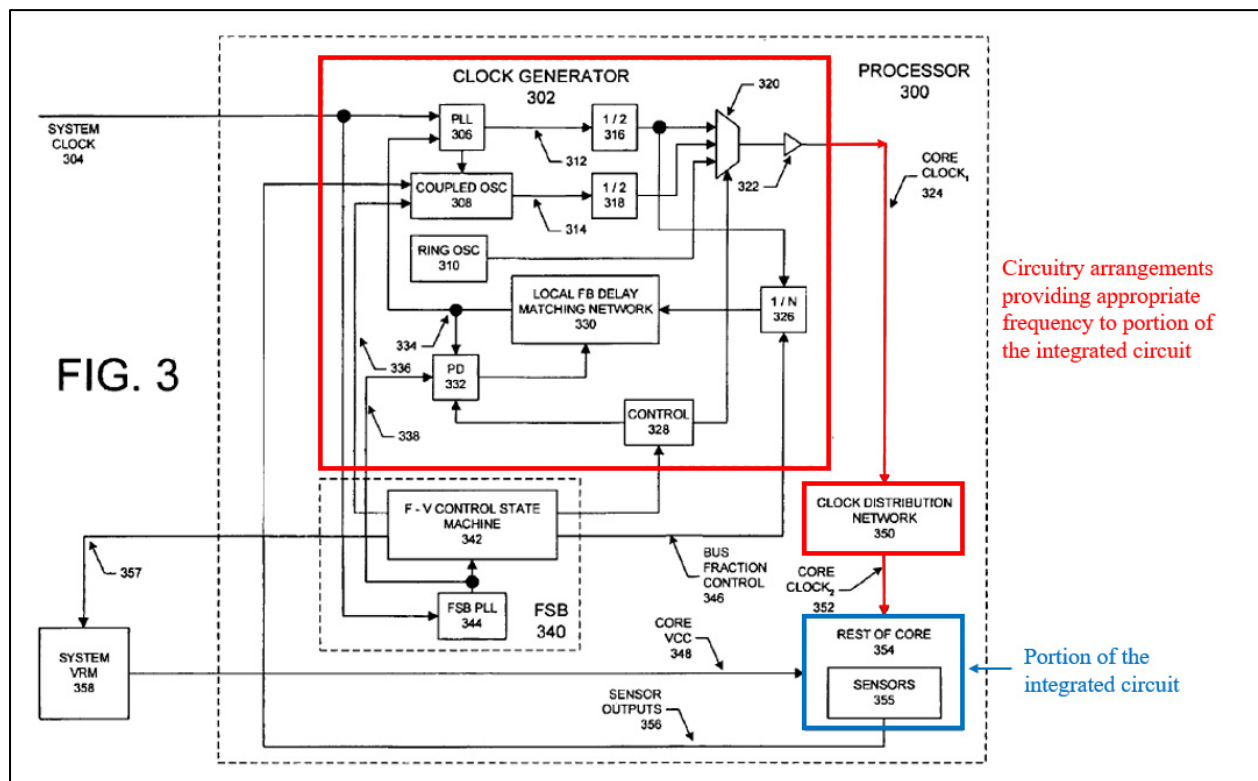
To the extent it is determined that Tam does not disclose determining an appropriate frequency for a specific portion of the integrated circuit, it would have been obvious to a POSITA to determine an appropriate frequency for a portion of the integrated circuit. MTK-1003, ¶64. For example, it would have been obvious

to a POSITA that “a local sensor in a high activity area such as the FPU [located in the processor core] can better indicate the existence of a critical low voltage condition in that circuitry and inform the clock generator of a need to lower the operating frequency” for that portion of the integrated circuit. MTK-1004, 6:12-16; MTK-1003, ¶64. A POSITA would have recognized that doing so would “provide[] an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.” MTK-1004, 3:51-54. A POSITA would have also understood, based on Tam’s disclosures, that this allows the integrated circuit to “avoid performance errors, “maintain consistent power draw,” and “continue to operate despite non-optimal voltage conditions at certain locations on the die.” MTK-1004, 7:45-50; MTK-1003, ¶64.

(d) Element 1[c]

Tam discloses providing the appropriate frequency to said portion of said integrated circuit. *Supra* 1[b]; MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 12:4-11, 12:30-64, FIGS. 1-7B, claims 1-30; MTK-1003, ¶65. For example, Tam teaches that “[c]lock generator 302 is to provide an internal processor clock signal,” i.e., a clock frequency, to “the processor core 354,” i.e., said portion of said integrated circuit, “via a clock distribution network 350.” MTK-1004, 6:41-44; MTK-1003, ¶65.

It would have been obvious to a POSITA that Tam's clock frequency, which is dynamically adjusted by the clock generator in response to voltage variations at a portion of the integrated circuit and is thus an "appropriate frequency for the portion of the integrated circuit," is provided to that portion of the circuit via the clock distribution network, as depicted in FIG. 3 below. MTK-1003, ¶65.



MTK-1004, FIG. 3

3. Claim 2

Tam discloses continuously repeating claim 1's sensing, determining, and providing method steps during the integrated circuit's operation. *Supra* 1[a]-1[c]; MTK-1004, 11:24-28, 12:50-13:11; MTK-1003, ¶66. Specifically, Tam discloses,

in one embodiment, that after sensing a delivered voltage, determining an appropriate frequency, and providing that frequency, MTK-1004, 12:4-13:9, the “frequency adjustment mechanism continues to monitor the processor and evaluates the sensors for further changes,” MTK-1004, 13:9-11. In a second embodiment, such “sensor outputs are sampled every 50 or 100 clock pulses,” and in a third embodiment, “the output” is “sampled *continuously*[.]” MTK-1004, 11:24-28. It would have been obvious to a POSITA to continue to monitor the processor and evaluate the sensors for further changes by continuously sampling the sensor outputs, and a POSITA would have been motivated to do so, so that the frequency is able to “gradually follow the voltage changes” without having to make “large adjustments to catch up with big voltage steps.” MTK-1004, 11:46-51; MTK-1003, ¶66. A POSITA would have also understood, based on Tam, that how often the sensor outputs are sampled is merely a design choice “depending on the particular implementation and the desired response speed.” MTK-1004, 11:26-28; MTK-1003, ¶66.

4. **Claim 3**

It would have been obvious to a POSITA, as evidenced by both Tam and applicant admitted prior art (“AAPA”), to have the appropriate frequency be the maximum frequency possible for the portion of the integrated circuit at the delivered voltage. MTK-1003, ¶¶67-69; *see also id.* at ¶¶35-38.

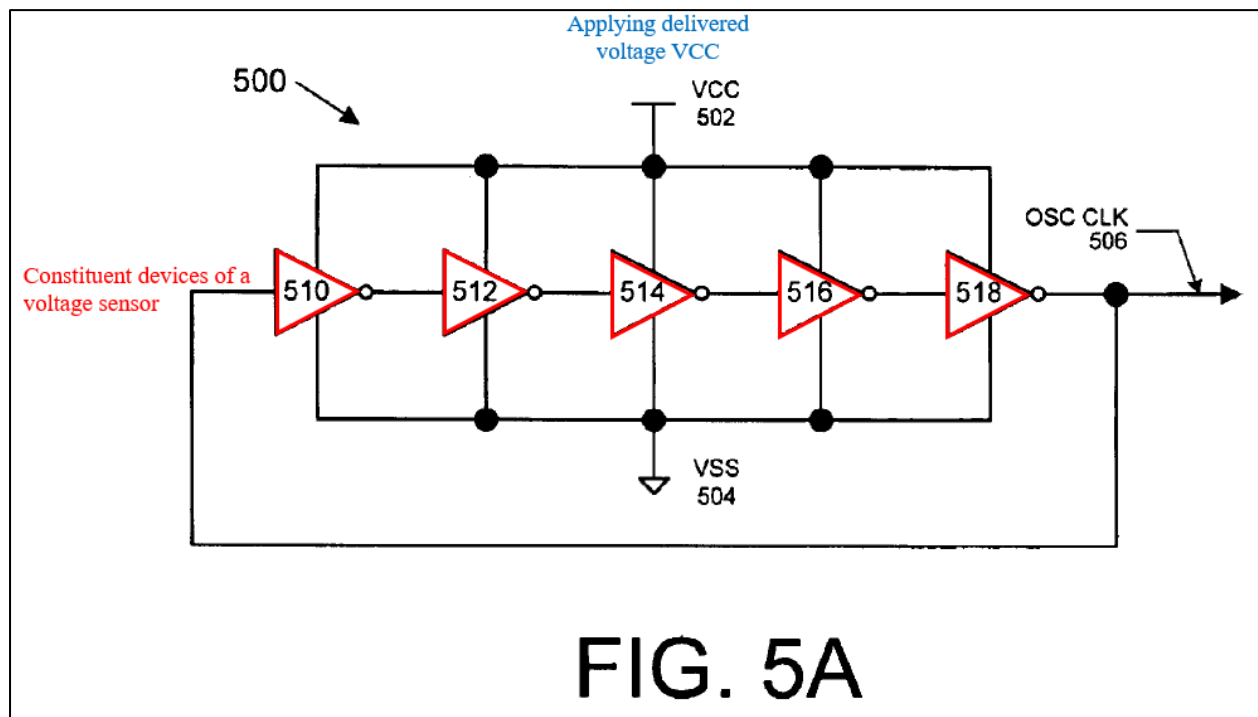
Tam specifically notes that “[a] high clock frequency is one of the principal performance drivers for a high performance microprocessor design.” MTK-1004, 1:27-29, *id.* at 1:29-30 (“One common method for achieving higher performance is to increase the processor operating frequency.”). Thus, a POSITA would have understood that utilizing the maximum frequency supported by the delivered voltage would be highly beneficial to a system’s performance. MTK-1003, ¶68; *see also* MTK-1004, 3:51-54 (“Thus a mechanism in accordance with the present invention provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.”), 11:46-47 (“this embodiment tracks the frequency with the voltage in a tight manner”), 11:66-12:2 (“determine the highest frequency ... possible to prevent circuit failure”).

Tam’s disclosure is commensurate with AAPA from the ’563 patent. MTK-1003, ¶69. For example, the ’563 patent admits that, as of the time of the alleged invention, “a designer will typically specify the maximum frequency at which a part can operate for a given voltage.” MTK-1001, 1:24-27. A designer would have typically done this because—as disclosed in Tam—having the frequency remain close to the maximum frequency supported by the voltage increases system efficiency. MTK-1001, 6:28-31; MTK-1003, ¶69.

5. Claim 4

It would have been obvious to a POSITA, based on Tam, to apply the

delivered voltage to constituent devices of a voltage sensor. *Supra* 1[a]-1[c]; MTK-1003, ¶70. For example, “FIG. 5A” is an “embodiment of a ring oscillator 500,” which “can function as a voltage sensor” and comprises “five inverters [510,] 512, 514, 516, 518,” i.e., constituent devices of a voltage sensor. MTK-1004, 9:22-37; MTK-1003, ¶70.



MTK-1004, FIG. 5A

The inverters are “connected together in series as a closed loop” and “are coupled to ... a supply voltage VCC,” i.e., a delivered supply voltage.” MTK-1004, 9:24-26. A POSITA would have therefore understood that the delivered voltage VCC is being applied to constituent devices of voltage sensor 500. MTK-1003, ¶70.

According to Tam, “[t]he ring oscillator 500 provides an analog clock signal

OSC CLK 506 ... to the clock generator where its oscillation frequency embodies the local VCC.” MTK-1004, 9:27-33. By doing so, the “ring oscillator 500 can function as a voltage sensor” because “OSC CLK 506 reflects the VCC supply voltage in and around the ring oscillator location,” i.e., a portion of the integrated circuit. MTK-1004, 9:33-37; MTK-1003, ¶70.

6. Claim 5

It would have been obvious to a POSITA that Tam contemplated having the constituent devices be similar to devices comprising the portion of the integrated circuit. *Supra* 1[a]-1[c] and claim 4; MTK-1003, ¶71. For example, it would have been obvious to a POSITA that such constituent devices would be similar to the devices comprising the portion of the integrated circuit if they have similar timing elements, including “length and propagation time delay[s],” as the underlying circuit. *See* MTK-1001, 5:26-31; MTK-1003, ¶71. A POSITA would have recognized that, like the ’563 patent, Tam discloses that a voltage sensor, e.g., ring oscillator 500, can incorporate “‘known’ timing critical circuit elements” to “provide a more accurate reflection of the circuit delay behavior of the respective circuit blocks,” i.e., the respective portion of the integrated circuit. MTK-1004, 9:56-62; MTK-1003, ¶71. Accordingly, it would have been obvious to a POSITA that Tam discloses utilizing constituent devices of a voltage sensor that have similar timing elements as—and are thus similar to—devices comprising the

portion of the integrated circuit. MTK-1003, ¶71.

7. **Claim 6**

It would have been obvious to a POSITA, given their knowledge at the time of the alleged invention, to apply a delivered voltage to constituent devices of a voltage sensor, *supra* claim 4, and determine the switching speed of the constituent devices at the delivered voltage. MTK-1003, ¶¶72-75; MTK-1004, 10:45-11:12, FIGS. 1-7B.

As an initial matter, a POSITA would have recognized that, like the transistors of the '563 patent, Tam's inverters depicted in FIG. 5A comprise constituent devices of a voltage sensor, e.g., ring oscillator 500. *Supra* claim 5; MTK-1003, ¶73; MTK-1004, FIG. 5A. Moreover, the background section of the '563 patent—which constitutes AAPA—makes clear that a POSITA would have understood that “*voltage is a primary determinate of switching speed*” for such constituent devices, MTK-1001, 1:24-25, and that “*the voltage in large part determines the switching speed*” of such devices, *id.* at 1:44-45; MTK-1013, 8:50-58. Additionally, according to the '563 patent, a POSITA would have understood that the “relationship of the device speed to voltage ... is approximately linear,” MTK-1001, 1:50-55, and that the relationship between power, voltage, frequency, and switching speed was “well known, and has been exploited for power management particularly in mobile devices,” *id.* at 2:1-17; *id.* at 1:59-67; MTK-

1003, ¶74.

According to the '563 patent, a “voltage sensor” can “measure the effect of the voltage on circuit speed” by applying the delivered voltage to the constituent devices and determining if the constituent devices remain “able to cycle at the currently provided clock frequency” at that voltage. MTK-1001, 5:6-25. Like the '563 patent, Tam discloses a voltage sensor, e.g., ring oscillator 500, that applies the delivered voltage to constituent devices, e.g., inverters 510-518, and a clock generator that adjusts the clock frequency accordingly. *See* MTK-1004, FIGS. 3-5A, 9:22-67. It would have thus been obvious to a POSITA that Tam’s voltage sensor 500 would measure the effect of the voltage on circuit speed by determining whether constituent devices 510-518 are able to cycle at the current clock frequency and, if not, adjust the clock frequency accordingly. MTK-1003, ¶¶36-38, 75 (discussing MTK-1001, 5:6-25); MTK-1004, FIG. 5A.

8. **Claim 7**

It would have been obvious to a POSITA, given their knowledge at the time of the alleged invention, to use the switching speed of the constituent devices, i.e., inverters 510-518 shown in FIG. 5A, to determine the appropriate frequency. *Supra* claims 4 and 6; MTK-1003, ¶76. Specifically, it would have been obvious to a POSITA that, with knowledge of the constituent devices’ power consumption, delivered voltage, and switching speed, the system could determine an updated

“appropriate” frequency using well-known mathematical relationships. MTK-1003, ¶¶36-38, 76; MTK-1001, 1:59-67 (“ $P = CxV^2xF$ ”).

9. Claim 8

It would have been obvious to a POSITA to expose the voltage sensor and portion of the integrated circuit from Tam to the same physical conditions. *Supra* 1[a]-1[c] and claim 4; MTK-1003, ¶77. Specifically, Tam discloses exposing the voltage sensors to “the local VCC supply voltages” in one embodiment, and using others sensors to monitor “current, power, temperature, and/or processing load” in another embodiment. MTK-1004, 12:34-37. It would have been obvious to a POSITA that by exposing the voltage sensors and certain portions of the integrated circuit to the same physical conditions, including the same VCC supply voltage, current, power, temperature, and/or processing load, one could accurately track those conditions at specific portions of the integrated circuit. MTK-1003, ¶77; MTK-1004, 6:12-18, 8:30-36. A POSITA would have further understood that doing so would be beneficial as it would provide “an accurate and useful view of the power environment.” MTK-1004, 5:62-65; MTK-1003, ¶77.

10. Claim 9

Supra claim 8. MTK-1003, ¶78.

11. Claim 10

Tam discloses calculating a value for the delivered voltage. MTK-1004,

9:42-55, claims 29-30; MTK-1003, ¶¶79-81. The '563 patent notes that “an analog to digital converter” (an “A/D converter”) may be used “to actually measure [i.e., calculate] the value of the delivered voltage.” MTK-1001, 5:49-51; *id.* at 5:55-57. Like the '563 patent, Tam discloses using an A/D converter to calculate a value for the delivered voltage. MTK-1004, 9:42-55, claims 29-30. Specifically, Tam teaches that different “types of voltage sensors are available and can be implemented in accordance with the present invention,” including a “voltage sensor” comprising “an analog to digital converter.” MTK-1004, 9:42-46. According to Tam, that A/D converter “takes the local voltage as one input” and “can communicate the numerical value of the local voltage,” i.e., the value for the delivered voltage, “over a digital bus as a binary set of bits of 8 or 16 bits back to the clock generator block.” MTK-1004, 9:44-50.

One of Tam’s embodiments also includes an A/D converter that “receive[s] a first voltage reading” from a “voltage sensor” and converts that “voltage reading from an analog value to an [sic] coded numerical value.” MTK-1004, claim 29; *see also id.* at claim 30. Thus, a POSITA would have understood that Tam teaches calculating a value for the delivered voltage using an A/D converter to convert local voltage readings from analog values to digital values, which is similar to several embodiments of the '563 patent. MTK-1003, ¶¶80-81.

12. Claim 23

(a) Element 23[p]

Tam teaches a system for circuit control. MTK-1003, ¶82; *see also* 1[p]-1[c], *supra*.

(b) Element 23[a]

Supra 1[p] and 1[a]. MTK-1003, ¶83.

(c) Element 23[b]

Supra 1[p] and 1[b]. MTK-1003, ¶¶84-85.

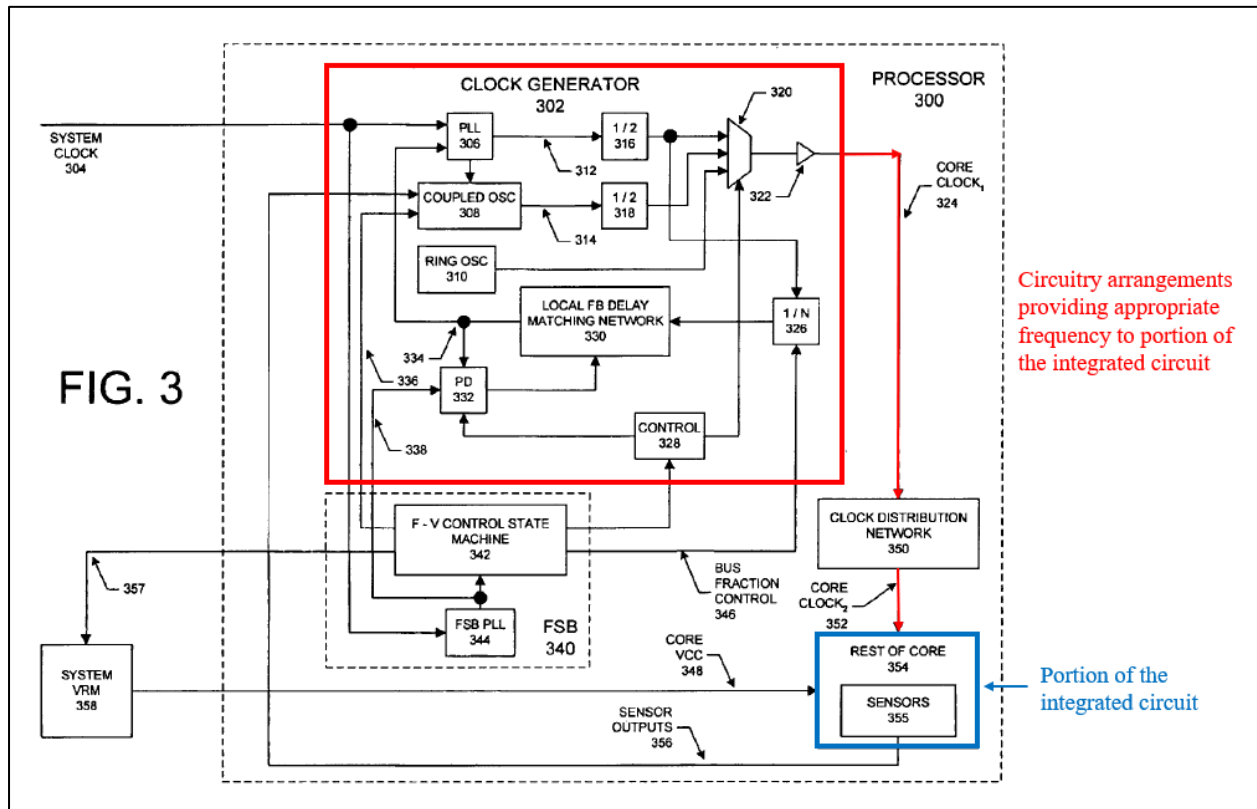
Tam specifically discloses at least one logic block, within its clock generator, to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit. *E.g.*, MTK-1004, 6:9-12 (“**Logic** in the clock generator 214 monitors the voltage statuses and can dynamically adapt and adjust the clock frequency based on the sensed information.”), 9:16-21 (“the clock control **logic** can adjust the processor clock frequency ... when supply voltages vary”), 12:24-29 (“The frequency/voltage control **logic** ... can shift the processor operating point by adjusting the processor core frequency[.]”), 12:34-36 (“The frequency/voltage control **logic** and clock circuitry analyze inputs from sensors that track the local VCC supply voltages.”), FIGS. 1-7B; MTK-1003, ¶¶84-85.

(d) Element 23[c]

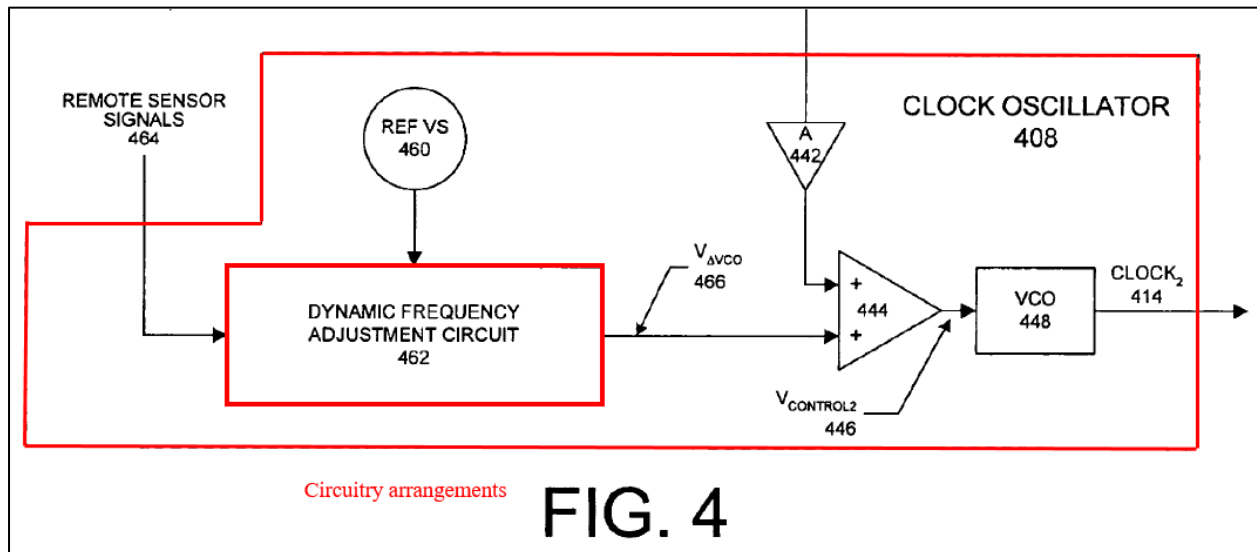
Supra 1[p], 1[b], and 1[c]. MTK-1003, ¶¶86-88.

Tam specifically discloses at least one circuitry arrangement (including the

clock generator and/or clock distribution network) to provide the appropriate frequency to the portion of the integrated circuit. *E.g.*, MTK-1004, 6:41-44 (“***Clock generator*** is to provide an internal processor clock signal CORE CLOCK₁ 324 to the rest of the processor core 354 via a ***clock distribution network*** 350.”), 7:43-47 (“Upon receipt of the voltage information, the ***clock circuitry*** can evaluate the data and respond accordingly.”), 8:37-40 (“Upon receipt of the sensor data, the dynamic frequency adjustment ***circuit*** 462 can evaluate the supply voltage conditions and dynamically adapt the clock oscillator output 414 appropriately.”), 10:15-16 (“The frequency adjustment ***circuit*** 600 provides an ability to tune the core clock frequency[.]”), 12:34-36 (“The frequency/voltage control logic and ***clock circuitry*** analyze inputs from sensors that track the local VCC supply voltages.”), claim 1 (“a clock generator coupled to said a [frequency] adjustment ***circuit***”), FIGS. 1, 3, 4, and 6A; MTK-1003, ¶¶87-88. Indeed, as depicted in FIGS. 3-4 below, Tam’s clock generator 302 (which includes the dynamic frequency adjustment circuit 462 within the coupled oscillator 308/clock oscillator 408) provides an updated clock frequency, i.e., the appropriate frequency, to clock distribution network 350, which in turn provides it to a portion of the integrated circuit, e.g., processor core 354:



MTK-1004, FIG. 3



MTK-1004, FIG. 4

13. **Claim 24**

Supra claim 3. MTK-1003, ¶89.

14. **Claim 31**

Supra claim 10. MTK-1003, ¶90.

15. **Claim 32**

Supra claim 10. MTK-1003, ¶90.

16. **Claim 35**

(a) Element 35[p]

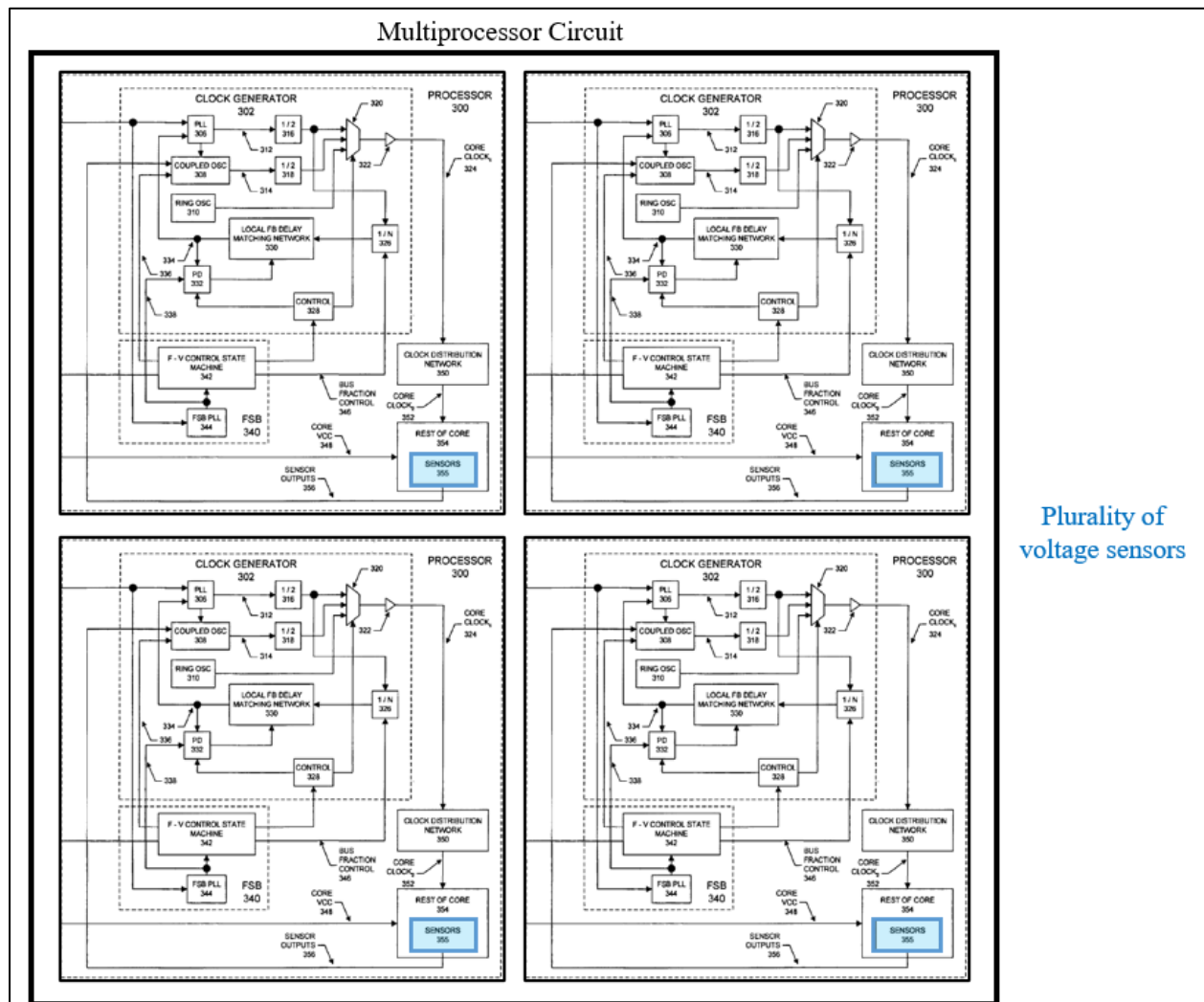
Tam teaches a system for circuit control. MTK-1003, ¶91; *see also* 1[p]-1[c] and 23[p]-23[c], *supra*.

(b) Element 35[a]

Supra 1[p] and 1[a]. MTK-1003, ¶¶92-94.

Tam teaches that its circuit control system can be utilized in a multiprocessor environment. *See* MTK-1003, ¶93; MTK-1004, 4:39-42 (“embodiments can [be] included in a multiprocessor system”). It would have thus been obvious to a POSITA to apply Tam’s teaching to a number of known multiprocessor (or multi-core) integrated circuits, including very large-scale integration (i.e., VLSI) devices, multi-chip modules (i.e., MCMs), and multiprocessor systems on a chip (MPSoCs). *E.g.*, MTK-1001, 1:19-23 (VLSI); MTK-1004, 5:36-39; MTK-1003, ¶93; MTK-1009, 488; MTK-1010, 460, 833; MTK-1011, 223; MTK-1012, 22-4; MTK-1020, ¶¶6-17.

A POSITA would have understood, based on Tam, that each processor in such a multiprocessor system would include “on-die voltage sensors and [an] adaptively variable clock generator[.]” MTK-1004, 5:46-48; *see also id.* at 13:12-18 (“In a multiprocessor system, the method can be performed concurrently in each processor.”); MTK-1003, ¶94. Further, it would have been obvious to a POSITA that voltage sensors in each of the processors’ cores would sense a delivered voltage to a different portion of the integrated circuit. *Id.*



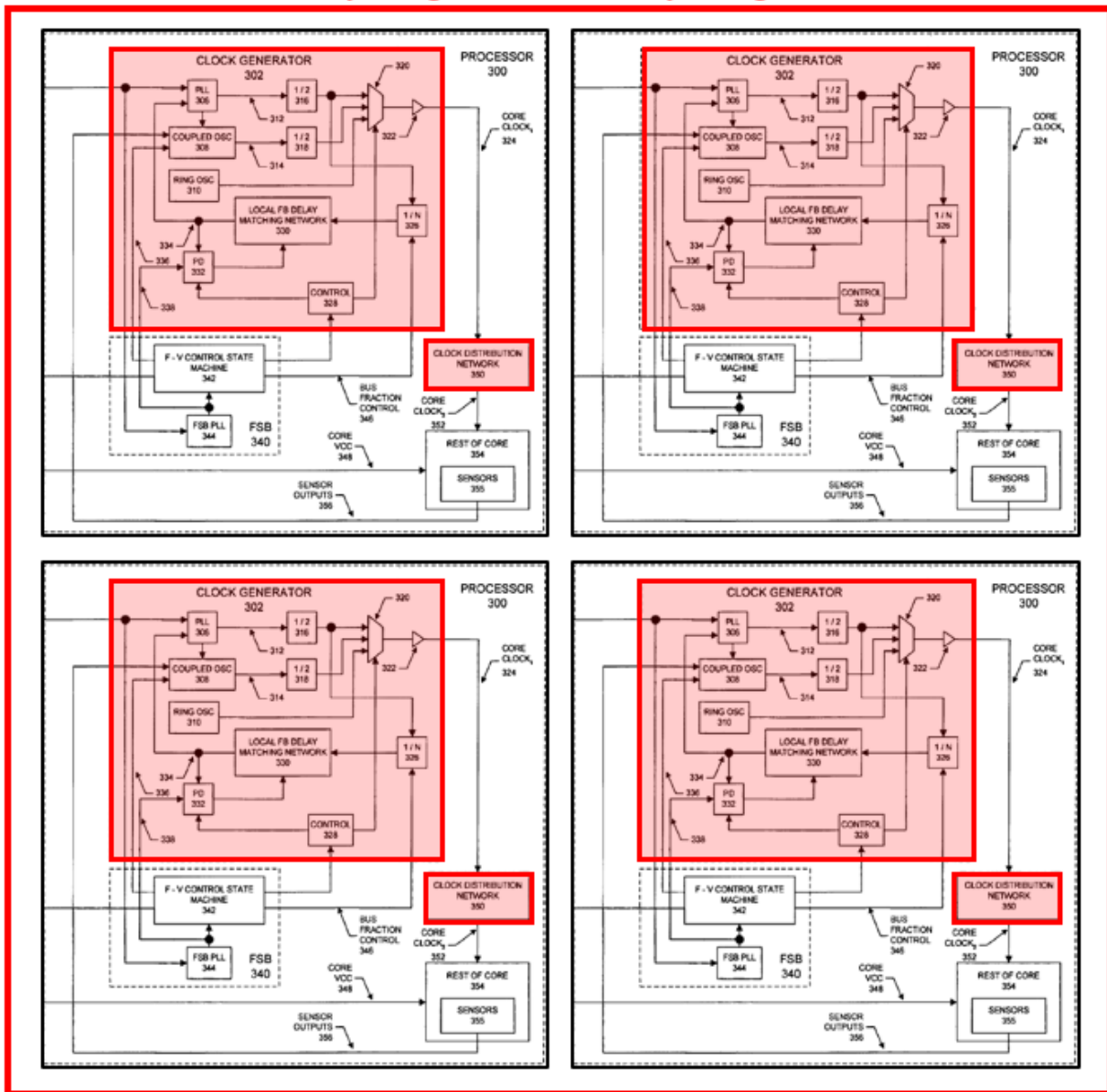
MTK-1003, ¶94 (Tam's FIG. 3 processor in potential multiprocessor system)

(c) Element 35[b]

Supra 1[p], 1[b], 23[b], 35[a]. MTK-1003, ¶¶95-96.

It would have been obvious to a POSITA that, in a multiprocessor system, such as the one depicted above with respect to claim element 35[a], logic in each of the processors' clock generators, i.e., the plurality of logic blocks arranged to determine an appropriate frequency, would have determined new clock frequencies for the processors' cores, i.e., portions of the integrated circuit, from the voltages delivered to each such core and sensed by that cores' voltage sensors. *See* 1[b], 23[b], 35[a] *supra*; MTK-1003, ¶96; MTK-1004, 13:12-18.

Plurality of logic blocks / circuitry arrangements



MTK-1003, ¶96 (Tam's FIG. 3 processor in potential multiprocessor system)

(d) Element 35[c]

Supra 1[p], 1[b], 1[c], 23[b], 23[c], 35[a], 35[b]. MTK-1003, ¶¶97-98.

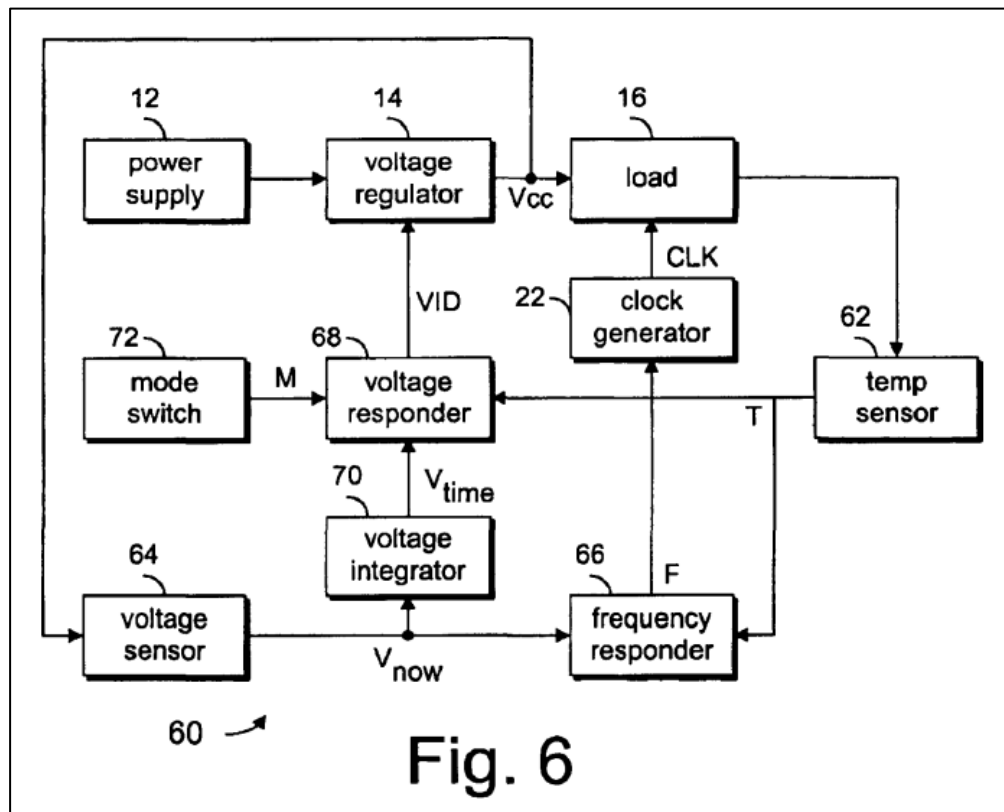
It would have been obvious to a POSITA that, in a multiprocessor system, each processor would include Tam's clock generator/clock distribution network

(i.e., a plurality of circuitry arrangements) for providing each processor core (i.e., portions of the integrated circuit) its associated appropriate frequency. MTK-1003, ¶98; MTK-1004, 13:12-18 (“each processor can” “adjust[] its own frequency”).

B. GROUND 2—Claims 1-11, 23-24, and 31-35 are obvious over Tam and Huard

1. Overview of Huard

Huard relates “to controlling operating conditions such as clock frequency ... as a function of the ... instantaneous voltage of the circuit.” MTK-1005, 1:20-24; MTK-1003, ¶¶100-102. Huard discusses an exemplary embodiment via reference to FIG. 6. *See* MTK-1005, 3:38-4:25; MTK-1003, ¶100.



MTK-1005, FIG. 6

According to Huard, “[a] power supply 12 provides electrical power to a voltage regulator 14, which provides a voltage supply V_{cc} to a load circuit 16,” e.g., a portion of an integrated circuit. MTK-1005, 3:39-43. In FIG. 6, “[a] voltage sensor 64 is coupled to measure the V_{cc} voltage provided to the load circuit, and to provide a present voltage signal V_{now} indicating the instantaneous present voltage.” *Id.* at 3:51-54. “A frequency responder 66 is coupled to receive ... V_{now} and ... provides a frequency control signal F ,” “in response” to V_{now} , to the clock generator to control the frequency of the clock signal CLK .” *Id.* at 3:56-60. The new frequency, CLK , is provided from the clock generator back to the load circuit. FIG. 6; MTK-1003, ¶¶101-102. According to Huard, this system is applicable when “operating a wide variety of synchronous load circuits,” i.e., multiple portions of a larger integrated circuit. MTK-1005, 5:1-7; MTK-1003, ¶102.

2. Tam-Huard Combination

A POSITA would have been motivated to combine Tam and Huard. MTK-1003, ¶¶103-108. At the time of the alleged invention, Tam and Huard were commonly owned by Intel and were in the same field of endeavor. *Id.*; MTK-1004, 1:8-12 (“[T]he present invention relates to a method and apparatus for a V_{CC} adaptive dynamically variable frequency clock system[.]”); MTK-1005,

1:20-24 (“This invention relates generally to controlling operating conditions such as clock frequency ... as a function of the operating temperature and instantaneous voltage of the circuit.”). Moreover, Tam and Huard both address a known problem (combating voltage droop), having a finite number of identified predictable solutions, in the same way. MTK-1003, ¶104 (citing MTK-1004, 2:35-39 (noting invention can be applied to avoid “voltage droop transients”); MTK-1005, 4:39-42 (noting advantage of invention is ability to address “voltage droop”)).

As discussed above, both Tam and Huard disclose a method and apparatus for: (1) sensing a delivered voltage to a portion of an integrated circuit (e.g., the “processor core” for Tam and the “load circuit” for Huard) using voltage sensors; (2) determining an appropriate frequency for that portion of the integrated circuit based on the sensed voltage using a frequency adjustment/responder circuit; and (3) providing that appropriate frequency to the portion of the integrated circuit via a clock generator/distribution network. *See* Sections III.A.1 and III.B.1, *supra*; MTK-1003, ¶105. Moreover, both Tam and Huard teach that adjusting frequency for a portion of an integrated circuit in response to instantaneous voltage changes or droops (as measured by local voltage sensors) would be beneficial to system performance. *See* MTK-1004, 3:44-4:5 (By “dynamically adjusting the clock frequency based on sensed on-die voltage changes,” Tam’s circuit “control technique” “provides an ability to tailor a clock frequency based on realistic supply

voltage levels and to alter the overall performance intelligently.”), 7:45-50 (such a method/system could “avoid performance errors, “maintain consistent power draw,” and “continue to operate despite non-optimal voltage conditions at certain locations on the die”); MTK-1005, 4:50-58 (“the invention will ... enabl[e] the majority of the systems, in which the power supply or voltage regulator are performing well, to operate at a higher performance level”); MTK-1003, ¶105.

To “evaluate the supply voltage conditions and dynamically adapt the clock oscillator output [] appropriately,” Tam discloses using a “dynamic frequency adjustment circuit,” which receives “sensor data” from “voltage sensors ... distributed over the integrated circuit.” MTK-1004, 8:24-40; *see also id.* at 5:2-5, 9:16-18, 12:24-28, 12:50-53; MTK-1003, ¶106. However, a POSITA would have understood that *how* Tam’s “dynamic frequency adjustment circuit” selects an appropriate frequency corresponding to a sensed voltage is merely a design choice with a finite number of known solutions. MTK-1003, ¶106.

A POSITA would have further understood that Huard discloses one such solution for selecting an appropriate frequency, in response to a sensed voltage, in the form of a “lookup table[] stored in read-only memory.” MTK-1005, 4:31-33; MTK-1003, ¶107. Specifically, Huard discloses a “frequency responder,” which a POSITA would have understood corresponds to Tam’s “dynamic frequency adjustment circuit,” that uses “the detected supply voltage as [an] address[] into the

lookup table” to “select[] a maximum frequency permitted by ... the detected supply voltage,” i.e., an appropriate frequency for the sensed voltage. MTK-1005, claims 36-37; MTK-1003, ¶107.

Because Tam and Huard provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references—especially considering their common ownership—when selecting a method for Tam’s “dynamic frequency adjustment circuit” to determine the appropriate frequency for a given voltage. MTK-1003, ¶108. Thus, it would have been obvious to a POSITA to use Huard’s lookup table in Tam’s “dynamic frequency adjustment circuit” to determine the appropriate frequency for the voltage delivered to a portion of the integrated circuit. MTK-1003, ¶108. A POSITA would have understood that utilizing a lookup table, as in Huard, in the “dynamic frequency adjustment circuit” of Tam to select the maximum frequency permitted by the sensed voltage would have been a mere design choice that was both obvious to try and would have yielded predictable results. *Id.* A POSITA would have further had a reasonable expectation of success in such a combination. *Id.*

3. Claim 1

(a) Element 1[p]

Supra Ground 1, 1[p]. MTK-1003, ¶109; MTK-1005, 5:8-15, claim 36.

(b) Element 1[a]

Supra Ground 1, 1[a]. MTK-1003, ¶110. Like Tam, Huard discloses sensing a delivered voltage to a portion of an integrated circuit. MTK-1005, Abstract, 1:20-24, 2:10-23, 3:38-65 (“A voltage sensor 64 is coupled to measure the Vcc voltage provided to the load circuit, and to provide a present voltage signal Vnow indicating the instantaneous present voltage.”), 4:26-38, 4:39-49, FIG. 6, claims 4, 7-8, 12, 15-25, 32, 36. Thus, it would have been obvious to a POSITA that Tam-Huard discloses this limitation. MTK-1003, ¶110.

(c) Element 1[b]

Supra Ground 1, 1[b]. MTK-1003, ¶111.

To the extent it is determined that Tam does not explicitly disclose determining an appropriate frequency for a specific portion of the integrated circuit, Huard discloses determining an appropriate frequency for the portion of the integrated circuit, e.g., a load circuit. MTK-1005, Abstract, 1:20-24, 2:10-23, 3:38-65 (“A frequency responder 66 is coupled to receive the outputs ... of the voltage sensor and ... in response to them, provides a frequency control signal F to the clock generator to control the frequency of the clock signal CLK.”), 4:13-25, 4:39-49, FIG. 6, claims 7-8, 12, 15-25, 32, 36. Thus, it would have been obvious to a POSITA to use the dynamic frequency adjustment circuit of Tam to determine an appropriate frequency for a specific portion of the integrated circuit (as done by

Huard's frequency responder), in a Tam-Huard combination. MTK-1003, ¶111.

(d) Element 1[c]

Supra Ground 1, 1[b]-[c]. MTK-1003, ¶112. Like Tam, Huard discloses providing the appropriate frequency to said portion of said integrated circuit. MTK-1005, Abstract, 1:20-24, 2:10-23, 3:38-65, 4:13-25, 4:39-49, FIG. 6, claims 7-8, 12, 15 (“a clock generator coupled to provide to the load circuit a clock signal”), 16-25, 32, 36. Thus, it would have been obvious to a POSITA that Tam-Huard discloses this limitation. MTK-1003, ¶112.

4. Claim 2

Supra Ground 1, claim 2. MTK-1003, ¶113.

5. Claim 3

Supra Ground 1, claim 3; MTK-1003, ¶¶114-115.

Moreover, to the extent Tam does not explicitly disclose having the appropriate frequency be the maximum frequency possible, Tam-Huard discloses having the appropriate frequency be the maximum frequency possible for the portion of the integrated circuit at the delivered voltage. MTK-1003, ¶115. Specifically, Tam-Huard discloses a method comprising, “detecting the supply voltage” of a portion of the integrated circuit and “setting the clock frequency as a function of ... the detected supply voltage,” where the frequency is the “*maximum frequency permitted by [] the detected supply voltage[.]*” MTK-1005, claim 36.

6. **Claim 4**

Supra Ground 1, claim 4. MTK-1003, ¶116.

7. **Claim 5**

Supra Ground 1, claim 5. MTK-1003, ¶117.

8. **Claim 6**

Supra Ground 1, claim 6. MTK-1003, ¶118.

9. **Claim 7**

Supra Ground 1, claim 7. MTK-1003, ¶119.

10. **Claim 8**

Supra Ground 1, claim 8. MTK-1003, ¶120.

11. **Claim 9**

Supra Ground 1, claim 9. MTK-1003, ¶121. Like Tam, Huard discloses exposing the voltage sensor and portion of the integrated circuit to the same physical conditions, where those conditions include temperature. *Id.*; MTK-1005, Title, Abstract, 1:20-24, 3:8-30, 3:49-55 (noting combined voltage/temperature sensor can detect voltage and temperature at load circuit), 3:56-65, FIGS. 5-6, claims 1-3. A POSITA would have understood that doing so is important to prevent “data corruption or catastrophic failure.” MTK-1005, 3:26-30; MTK-1003, ¶121. Thus, it would have been obvious to a POSITA that Tam-Huard discloses wherein the physical conditions include temperature. MTK-1003, ¶121.

12. **Claim 10**

Supra Ground 1, claim 10. MTK-1003, ¶122. Like Tam, Huard teaches that its voltage sensor can include an analog-to-digital converter for calculating a value for the delivered voltage. MTK-1005, 4:26-38 (“In one embodiment, the voltage sensor and the temperature sensor can include analog-to-digital (A/D) converters, which output multi-bit binary signals V_{now} and T , respectively.”). Thus, it would have been obvious to a POSITA that Tam-Huard discloses utilizing voltage sensors that comprise analog-to-digital converters to calculate values for the delivered voltages to specific portions of an integrated circuit (e.g., the processor core). MTK-1003, ¶122.

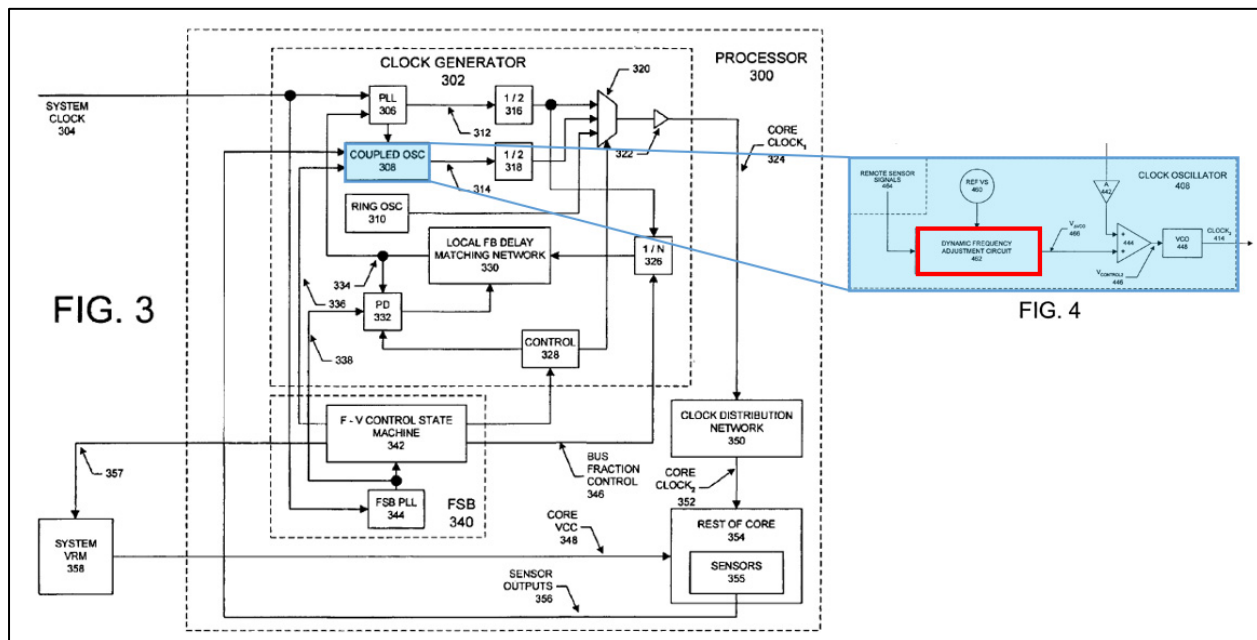
13. Claim 11

Tam-Huard teaches using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency. *See* MTK-1003, ¶¶123-126; MTK-1005, 3:8-20, 4:26-38, claims 1, 3, 4, 15, 22, 23, 36, and 37.

For example, Huard discloses “[a] frequency responder” that receives “a present voltage signal V_{now} indicating the instantaneous present voltage” and, “in response ... provides a frequency control signal ... to the clock generator to control the frequency of the clock signal[.]” MTK-1005, 3:51-60. According to Huard, “the frequency responder can be implemented as [a] lookup table[] stored in read-only memory,” i.e., a computer readable database. MTK-1005, 4:31-33. Huard

teaches that the frequency responder uses the lookup table, i.e., a tabulation of a set of values, to determine the appropriate frequency for an associated supply voltage. *See* MTK-1005, claim 15 (“a frequency responder coupled to provide a frequency control signal as a function of ... the present operating voltage signal”), claim 22 (“the frequency responder comprises a lookup table”), claim 23 (“the frequency responder’s lookup table is addressed by ... the present voltage signal”), claim 36 (“selecting a maximum frequency permitted by ... the detected supply voltage ... by looking up the maximum frequency in a lookup table”), claim 37 (“using ... the detected supply voltage as [an] address[] into the lookup table”); MTK-1003, ¶¶124-125.

A POSITA would have recognized that Huard’s “frequency responder” directly corresponds to Tam’s “dynamic frequency adjustment circuit,” which similarly receives “sensor data” from “voltage sensors ... distributed over the integrated circuit,” “evaluate[s] the supply voltage conditions and dynamically adapt[s] the clock oscillator output [] appropriately.” MTK-1004, 8:24-40; MTK-1003, ¶126. Thus, it would have been obvious to a POSITA to use Huard’s lookup table, i.e., “a tabulation of a set of values,” in Tam-Huard’s “dynamic frequency adjustment circuit” to determine the appropriate frequency for the voltage delivered to a portion of the integrated circuit. MTK-1003, ¶126.



MTK-1004, FIGS. 3-4

14. **Claim 23**

(a) **Element 23[p]**

Supra Ground 1, 1[p], 23[p]; Ground 2, 1[p]. MTK-1003, ¶127.

(b) **Element 23[a]**

Supra Ground 1, 1[p]-1[a], 23[a]; Ground 2, 1[p]-1[a]. MTK-1003, ¶128.

(c) **Element 23[b]**

Supra Ground 1, 1[p], 1[b], 23[b]; Ground 2, 1[p], 1[b]. MTK-1003, ¶129.

(d) **Element 23[c]**

Supra Ground 1, 1[p], 1[c], 23[c]; Ground 2, 1[p], 1[c]. MTK-1003, ¶130.

15. **Claim 24**

Supra Ground 1, claim 3; Ground 2, claim 3. MTK-1003, ¶131.

16. **Claim 31**

Supra Ground 1, claims 10 and 31; Ground 2, claim 10. MTK-1003, ¶132.

17. **Claim 32**

Supra Ground 1, claims 10 and 32; Ground 2, claim 10. MTK-1003, ¶132.

18. **Claim 33**

Supra Ground 2, claim 11. MTK-1003, ¶133.

19. **Claim 34**

Supra Ground 2, claim 11. MTK-1003, ¶134.

20. **Claim 35**

(a) Element 35[p]

Supra Ground 1, 1[p]-1[c], 23[p]-23[c], 35[p]; Ground 2, 1[p]-1[c], 23[p]-23[c]. MTK-1003, ¶135.

(b) Element 35[a]

Supra Ground 1, 1[p], 1[a], 35[a]; Ground 2, 1[p], 1[a]. MTK-1003, ¶136.

(c) Element 35[b]

Supra Ground 1, 1[p], 1[b], 23[b], 35[a], 35[b]; Ground 2, 1[p], 1[b], 23[b]. MTK-1003, ¶137.

(d) Element 35[c]

Supra Ground 1, 1[p], 1[b], 1[c], 23[b], 23[c], 35[a], 35[b], 35[c]; Ground 2, 1[p], 1[b], 1[c], 23[b], 23[c]. MTK-1003, ¶138.

C. GROUND 3—Claims 1-11, 23-24, and 31-35 are obvious over Norman '259 and Norman '851 (“the Norman Combination”)

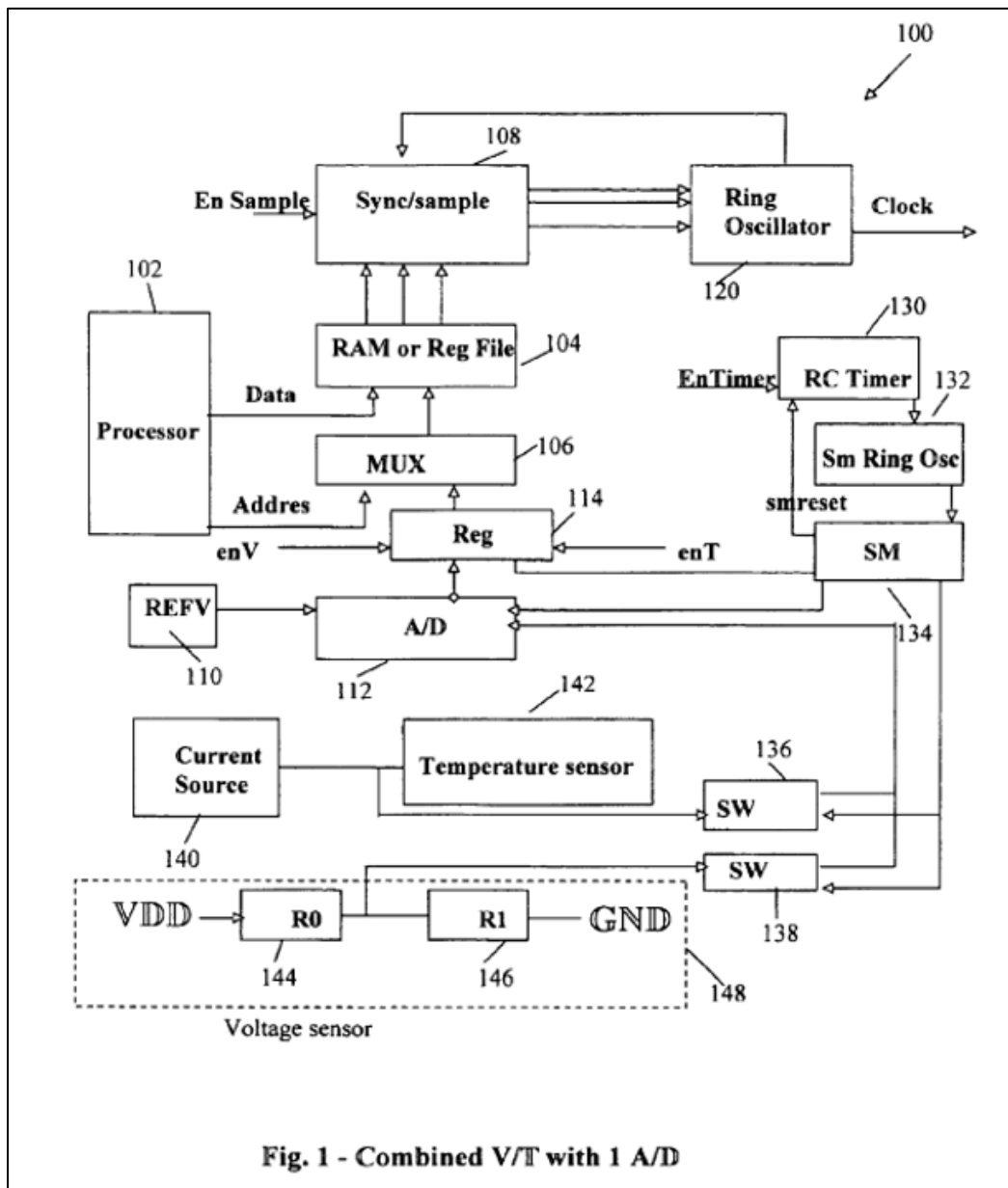
1. Overview of Norman '259

Norman '259 relates to “[a]n apparatus” and “method” that “compensates for voltage and temperature variations on an integrated circuit.” MTK-1006, Abstract; *id.* at 2:58-62; MTK-1003, ¶140. Specifically, Norman '259 discloses “dynamically adjusting for temperature and voltage variations on an integrated circuit” by “periodically sensing the voltage and temperature values[] and dynamically making adjustments in clock frequency based on the voltage and temperature values.” MTK-1006, 2:58-62; MTK-1003, ¶141. To do this, Norman '259 discloses utilizing:

A voltage sensor having a digital voltage output; a register coupled to the voltage sensor having a digital temperature output; a register coupled to the voltage sensor and the temperature sensor, the register adapted to concatenate the digital voltage output and the temperature output into an address output; and a memory device having an address input coupled to the address output of the register, the memory device being adapted to store one or more corrective vectors.

MTK-1006, 2:28-37. According to Norman '259, “[t]he memory device can generate an adjustment vector,” e.g., an adjustment for a new operating frequency, “based on the current voltage and temperature,” “wherein the adjustment vector is applied to the ring oscillator” and “selects the ring frequency; lengthening or shortening the ring delay to maintain the desired operating point.” *Id.* at 2:46-51.

Norman '259 discusses the invention in view of the exemplary auto-calibration system of FIG. 1:



MTK-1006, FIG. 1

According to Norman '259, “[t]o adjust for” changes in temperature and voltage “and keep the system running at the ideal frequency, the temperature and voltage of the system needs to be monitored.” MTK-1006, 4:1-7. After sensing voltage and temperature values using voltage sensor 148 and temperature sensor 142, *id.* at

4:7-36, those values are applied to the ADC 112, and the “output of the ADC 112 is registered and applied to the multiplexor 106,” which is driven by an address from the processor 102.” MTK-1006, 4:15-20. “The output of the multiplexor 106 is applied to the memory 104 as the address input” and, “[a]t initialization, the processor 102 writes adjustment values into the RAM or Register File 104,” and the “output of the RAM 104 ... acts as the adjustment vector that is applied to the ring oscillator 120” to “select[] the ring frequency.” MTK-1006, 4:20-29; *id.* at claim 7; *see also* MTK-1003, ¶142.

2. Overview of Norman ’851

Norman ’851 relates to a “self-calibrating integrated circuit” that “includes a processor having at least one analog function used with the processor; one or more sensors adapted to sense one or more environmental parameters of the at least one analog function; and a solid state memory being configured to store the one or more environmental parameters of the at least one analog function.” MTK-1007, Abstract; MTK-1003, ¶143. According to Norman ’851, “[t]o capture information that allows the processor 12 to automatically calibrate the IC 10 so that the on-chip clock oscillator 42 is precise and accurate in spite of process, temperature or power supply variations, various sensors 46-48 are placed at predetermined locations in the IC 10 to sense environmental variations.” MTK-1007, [0019]; MTK-1003, ¶143. Norman ’851 teaches that “[e]nvironmental parameters of the IC include

temperature, supply voltage and other external parameters which effect the performance of the IC 10.” MTK-1007, [0024]. According to Norman ’851, by using various “voltage sensors,” *id.* at [0026], the system can “detect the supply voltage that the system is presently operating at and adjust for variations in the supply voltage,” *id.* at [0024]; MTK-1003, ¶144. Indeed, Norman ’851 expressly claims certain embodiments of an integrated circuit that include “one or more sensors adapted to sense one or more environmental parameters” and “an oscillator ... having a frequency varied by one or more environmental parameters,” MTK-1007, claim 18, wherein those “environmental parameters include[] temperature or supply voltage,” *id.* at claim 19. *See also* MTK-1003, ¶145.

3. The Norman Combination

A POSITA would have been motivated to combine Norman ’259 with Norman ’851. MTK-1003, ¶¶146-150. Norman ’259 and Norman ’851 share the same inventors (i.e., Norman and Schmidt), were commonly owned by Gallitzin Alleghany LLC when filed, and are in the same field of endeavor. MTK-1003, ¶147. Moreover, Norman ’851 incorporates the contents of Norman ’259’s application by reference. *Compare* MTK-1007, [0024], *with* MTK-1006, Title; MTK-1003, ¶148.

Additionally, Norman ’259 and Norman ’851 both address a known problem (compensating for voltage and temperature variations), having a finite number of

identified predictable solutions, in the same way. MTK-1003, ¶149. As discussed above, both references utilize voltage and temperature sensors for sensing instantaneous voltage and temperature fluctuations in an integrated circuit, and a ring oscillator for adjusting clock frequency based on those supply voltage and temperature variations. *See, e.g.*, MTK-1006, Abstract, 2:28-37, 2:46-51, 2:58-62, 3:10-25, 3:67-4:1, 4:4-5:10, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0004], [0006]-[0007], [0009], [0019], [0024]-[0027], claims 1-3 and 18-19, FIGS. 1-2; MTK-1003, ¶149. Norman '259 discloses, in detail, a device that corrects for temperature and voltage variations, while Norman '851 discloses utilizing the device of Norman '259 in a system including multiple “sub-systems” and “voltage sensors.” *See* MTK-1007, [0024], [0026], [0030].

Because Norman '259 and Norman '851 provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references—especially considering their common inventorship, common ownership, and incorporations by reference—when using Norman '259's dynamic frequency adjustment method to self-calibrate a system having multiple voltage sensors and sub-systems as in Norman '851. MTK-1003, ¶150.

4. Claim 1

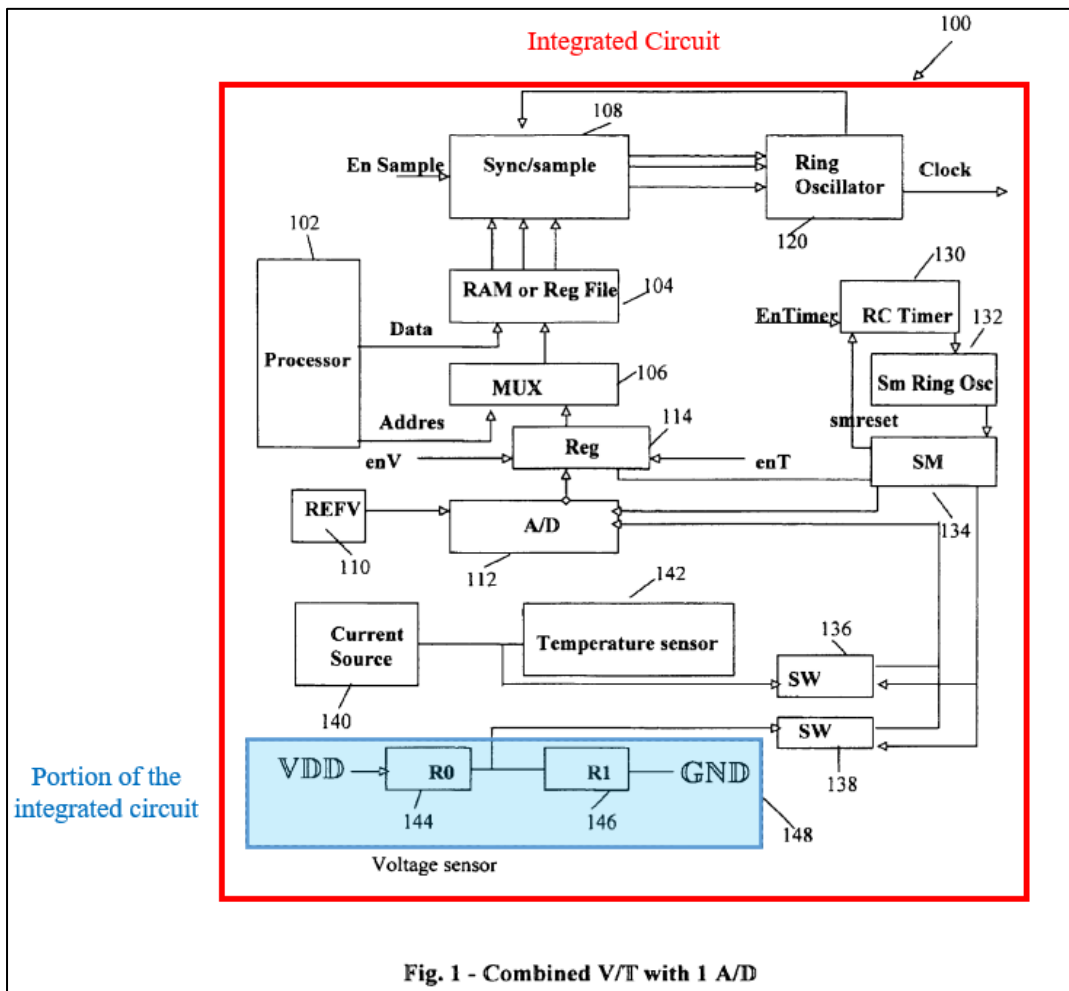
(a) Element 1[p]

To the extent the preamble is limiting, the Norman Combination discloses a method of circuit control as set forth below. *Infra* Ground 3, 1[a]-1[c]; MTK-1006, 2:12-24, 2:58-62, claim 11; MTK-1007, Title; MTK-1003, ¶151. Specifically, the Norman Combination discloses “a method for dynamically adjusting for ... voltage variations on an integrated circuit” that involves “periodically sensing the voltage ... values” and “making adjustments in clock frequency based on the voltage ... values.” MTK-1006, 2:58-62; *id.* at claim 11 (“A method for dynamically adjusting for ... voltage variations on an integrated circuit...”); MTK-1007, [0001] (“The present invention relates [to] systems and method for self-calibrating semiconductor devices.”), [0025] (“An exemplary processor of calibrating and correcting the IC 10 is shown in the flow chart 200 of FIG. 2.”), FIG. 2.

(b) Element 1[a]

The Norman Combination discloses sensing a delivered voltage to a portion of an integrated circuit. MTK-1006, Abstract, 2:28-37, 2:58-62, 3:10-25, 4:4-7, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0006], [0007], [0009], [0019], [0023]-[0027], claims 1, 3, and 18-19, FIGS. 1-2; MTK-1003, ¶¶152-155. As discussed above, Norman ’851 states that details of “the device that corrects ... voltage variations are discussed in” the application that led to Norman ’259, which Norman ’851 “incorporate[s] by reference.” MTK-1007, [0024]. Norman ’259, in

turn, discloses “a method for dynamically adjusting for ... voltage variations on an integrated circuit” that includes “periodically sensing the voltage” values using a voltage sensor. MTK-1006, 2:58-62; *id.* at 2:28-30 (an apparatus for “compensat[ing] for voltage ... variations on an integrated circuit includes: a voltage sensor”), FIG. 1 (depicting voltage sensor 148 located at a portion of integrated circuit 100); MTK-1003, ¶153. It would have been obvious to a POSITA that such a voltage sensor would sense a voltage delivered to a portion of the integrated circuit, e.g., the portion of the integrated circuit or sub-system where the voltage sensor is located. MTK-1003, ¶154.



MTK-1006, FIG. 1

For example, it would have been obvious to a POSITA, based on Norman '851, to include voltage sensors, such as those disclosed in Norman '259, at various “predetermined locations in the IC [integrated circuit],” i.e., portions of the integrated circuit, “to sense environmental variations,” such as variations in “supply voltage,” at those locations. MTK-1007, [0019], [0023]-[0024], [0026] (“the voltage sensors are monitored”); MTK-1003, ¶155.

(c) Element 1[b]

The Norman Combination discloses determining an appropriate frequency for the portion of the integrated circuit. MTK-1006, Abstract, 2:28-37, 2:46-51, 2:58-62, 3:10-25, 3:67-4:1, 4:4-7, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0004], [0006]-[0007], [0009], [0019], [0024]-[0027], claims 1-3 and 18-19, FIGS. 1-2; MTK-1003, ¶¶156-158. Specifically, the Norman Combination discloses “keep[ing] the system running at the ideal frequency,” i.e., the appropriate frequency, by monitoring “the voltage of the system,” MTK-1006, 4:4-7, and “dynamically making adjustments in clock frequency based on the voltage,” *id.* at 2:58-62. *See also id.* at 2:46-51 (“The adjustment vector selects,” i.e., determines, “the ring frequency” “based on the current voltage and temperature[.]”), 3:10-25 (“These adjustments are accomplished by sensing the voltage ... values and dynamically making adjustments in clock frequency.”); MTK-1007, [0024] (“[T]he system can also detect the supply voltage that the system is presently operating at and adjust for variations in the supply voltage... If the operating voltage is not at a nominal value, the controller adjusts the ring oscillator delay path to compensate for the voltage differential.”); MTK-1003, ¶157.

The Norman Combination determines the ideal, i.e., appropriate, frequency for the portion of the integrated circuit by:

[C]ombining the voltage and temperature values into a digital word. The method can store the temperature value in a first register; the voltage value in a second register; and merge the first and second

registers to represent a concatenated address. The concatenated address can be applied to the address of a memory to retrieve a corrective value from a corrective table.

MTK-1006, 2:63-3:3; MTK-1003, ¶158. The Norman Combination discloses that, “[t]he table should produce a desired center frequency[.]” MTK-1006, 4:64-5:1.

Thus, it would have been obvious to a POSITA that the Norman Combination discloses sensing the instantaneous voltage and temperature values at a portion of the integrated circuit (using voltage and temperatures sensors), digitizing and concatenating those values, and then using the concatenated value as an address in a lookup table, i.e., a tabulation of a set of values, to determine the ideal, i.e., appropriate, frequency, associated with the delivered voltage. MTK-1003, ¶158.

(d) Element 1[c]

It would have been obvious to a POSITA that the Norman Combination’s “ring oscillator” provides the appropriate frequency to said portion of said integrated circuit. *Supra* 1[b]; MTK-1003, ¶¶159-161; MTK-1006, 3:60-65 (“The ring oscillator 120 generates a system clock and a control signal that is *provided* ...”).

First, it would have been obvious to a POSITA that the Norman Combination teaches utilizing multiple “voltage sensors,” MTK-1007, [0026], like those described in Norman ’259 and incorporated into Norman ’851 by reference, which can be “placed at predetermined locations in the IC [] to sense

environmental variations,” *id.* at [0019], including variations in “supply voltage,” *id.* at [0024]. MTK-1003, ¶¶160-161. Second, it would have been obvious to a POSITA that each “voltage sensor” would be placed at a different portion of the integrated circuit. MTK-1003, ¶161. Third, it would have been obvious to a POSITA that the Norman Combination’s dynamic frequency adjustment mechanism could be applied to individual sub-systems located in the integrated circuit. *Id.*; MTK-1007, [0030] (“This process of calibration and correction can be conducted for each sub-system of the IC.”). Finally, it would have been obvious to a POSITA that correcting the sub-system, i.e., a portion of the integrated circuit, involves providing that sub-system with an appropriate frequency, which is determined based on the instantaneous voltage and temperatures readings for that sub-system. MTK-1003, ¶¶160-161; MTK-1006, 4:54-5:1 (“Process variations can be dialed out based on the correction table vector loaded,” where “[t]he table ... produce[s] a desired frequency[.]”), 6:67-7:3 (noting a ring oscillator “provides a plurality of clock signal signals, each of which can be used to clock a portion of the chip to prevent clock degradation due to too much load on the chip”).

5. Claim 2

The Norman Combination discloses continuously repeating claim 1’s sensing, determining, and providing method steps during the integrated circuit’s operation. *Supra* Ground 3, 1[a]-1[c]; MTK-1006, 2:58-62, claim 11; MTK-1007,

[0009], [0028]-[0029]; MTK-1003, ¶162. For example, the Norman Combination discloses “periodically sensing the voltage ... values[] and dynamically making adjustments in clock frequency based on the voltage ... values.” MTK-1006, 2:58-62; *see also id.* at claim 11 (“periodically sensing the voltage”); MTK-1007, [0028] (“The data is continually collected.”).

6. Claim 3

It would have been obvious to a POSITA, as evidenced by both the Norman Combination and AAPA, to have the appropriate frequency be the maximum frequency possible for the portion of the integrated circuit at the delivered voltage. MTK-1003, ¶¶163-164.

The Norman Combination discloses selecting a “frequency that operates as close to the desired frequency when operating at nominal temperature and voltage,” MTK-1006, 4:64-5:1, while noting that “by dynamically monitoring environmental parameters [such as voltage supply] and adjusting the operation and clock signal frequency” accordingly, “[t]he system optimizes operating performance,” MTK-1007, [0009]. *See also* MTK-1003, ¶164.

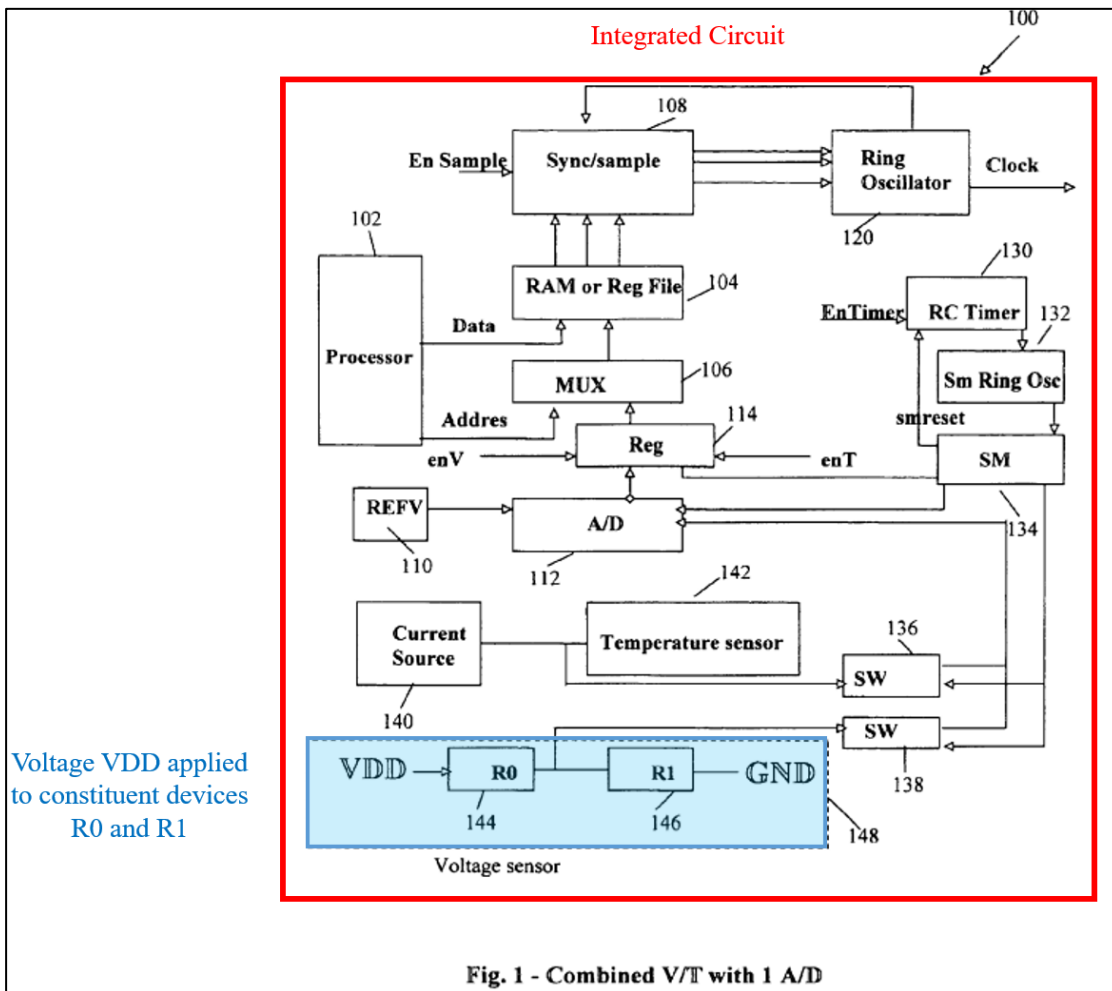
The Norman Combination’s disclosure is commensurate with AAPA from the ’563 patent. MTK-1003, ¶164. For example, the ’563 patent admits that, as of the time of the alleged invention, “a designer will typically specify the maximum frequency at which a part can operate for a given voltage.” MTK-1001, 1:24-27.

A designer would have typically done this because, by having the frequency remain close to the maximum frequency supported by the voltage, system efficiency is increased. MTK-1001, 6:28-31; MTK-1003, ¶164.

Thus, it would have been obvious to a POSITA, as evidenced by the Norman Combination and AAPA, that utilizing the maximum frequency supported by the delivered voltage would be highly beneficial to a system's performance. MTK-1003, ¶164.

7. Claim 4

It would have been obvious to a POSITA that the Norman Combination applies the delivered voltage to constituent devices of a voltage sensor. *Supra* Ground 3, 1[a]-1[c]; MTK-1003, ¶¶165-166. For example, the Norman Combination expressly discloses applying “[t]he system voltage ... to a voltage divider,” i.e., voltage sensor 148, “formed by resistors 144 and 146,” i.e., constituent devices of the voltage sensor, MTK-1006, 4:33-36, FIG. 1, which are connected “in series,” *id.* at 3:50-52. MTK-1003, ¶166.



MTK-1006, FIG. 1

8. Claim 5

It would have been obvious to a POSITA that the Norman Combination contemplated having the constituent devices be similar to devices comprising the portion of the integrated circuit. *Supra* Ground 3, 1[a]-1[c] and claim 4; MTK-1003, ¶¶167-168. For example, it would have been obvious to a POSITA that such constituent devices would be similar to the devices comprising the portion of the integrated circuit if they have, e.g., similar timing elements, including “length and

propagation time delay[s],” as the underlying circuit. *See* MTK-1001, 5:26-31; MTK-1003, ¶168. It would have further been obvious to a POSITA to have the Norman Combination’s constituent devices, e.g., resistors 144 and 146, be similar to the devices comprising the portion of the integrated circuit, such as by having similar timing elements as the underlying circuits, to provide a more accurate reflection of the circuit delay behavior of that portion of the integrated circuit. MTK-1003, ¶168.

9. Claim 6

It would have been obvious to a POSITA, given their knowledge at the time of the alleged invention, to apply a delivered voltage to constituent devices of a voltage sensor, *supra* claim 4, and determine the switching speed of the constituent devices at the delivered voltage. MTK-1003, ¶¶169-172; Ground 1, claim 6, *supra*.

Like the ’563 patent, the Norman Combination discloses a voltage sensor that applies the delivered voltage to constituent devices, e.g., resistors 144 and 146, and a circuitry arrangement that adjusts the clock frequency accordingly. *See* MTK-1006, 3:50-52, 4:33-38, FIG. 1. It would have thus been obvious to a POSITA that the Norman Combination’s voltage sensor 148 would measure the effect of the voltage on circuit speed by determining whether constituent devices 144 and 146 are able to cycle at the current clock frequency. MTK-1003, ¶¶170-

172 (discussing MTK-1001, 5:6-25).

10. **Claim 7**

It would have been obvious to a POSITA, given their knowledge at the time of the invention, to use the switching speed to determine the appropriate frequency. MTK-1003, ¶173; Ground 1, claim 7 and Ground 3, claims 4 and 6, *supra*.

11. **Claim 8**

It would have been obvious to a POSITA to expose the Norman Combination's voltage sensor and portion of the integrated circuit to the same physical conditions. *Supra* Ground 3, 1[a]-1[c] and claim 4; MTK-1003, ¶¶174-176. A POSITA would have understood, based on the Norman Combination, that one could "combine[] voltage and temperature detectors," MTK-1006, 3:34-35, and that such "detectors" or "sensors" could be placed "at key locations across the chip" to "minimize[] wide variations in clock signal frequency over operating parameter variables such as voltage and temperature," MTK-1007, [0009]. *See* MTK-1003, ¶175. It would have been obvious to a POSITA that by exposing the voltage/temperature sensors and certain portions of the integrated circuit to the same physical conditions, including the same voltages and temperatures, one could accurately track those conditions at specific portions of the integrated circuit. MTK-1003, ¶176. It would have been obvious to a POSITA that doing so would be beneficial as it would provide an accurate and useful view of the power

environment. MTK-1003, ¶176 (citing MTK-1004, 5:62-65, 12:33-39).

12. **Claim 9**

Supra Ground 3, claim 8. MTK-1003, ¶177.

13. **Claim 10**

The Norman Combination discloses calculating a value for the delivered voltage. MTK-1006, Abstract, 2:28-37, 3:41-45, claim 1; MTK-1007, [0007]-[0008], [0032]; MTK-1003, ¶¶178-179. The '563 patent notes that “an analog to digital converter” (an “A/D converter”) may be used “to actually measure [i.e., calculate] the value of the delivered voltage.” MTK-1001, 5:49-51; *id.* at 5:55-57. Like the '563 patent, the Norman Combination discloses using an A/D converter to calculate a value for the delivered voltage. MTK-1003, ¶178. Specifically, the Norman Combination discloses “chang[ing] the input” to an A/D converter “[a]s the voltage changes.” MTK-1006, 4:33-38.

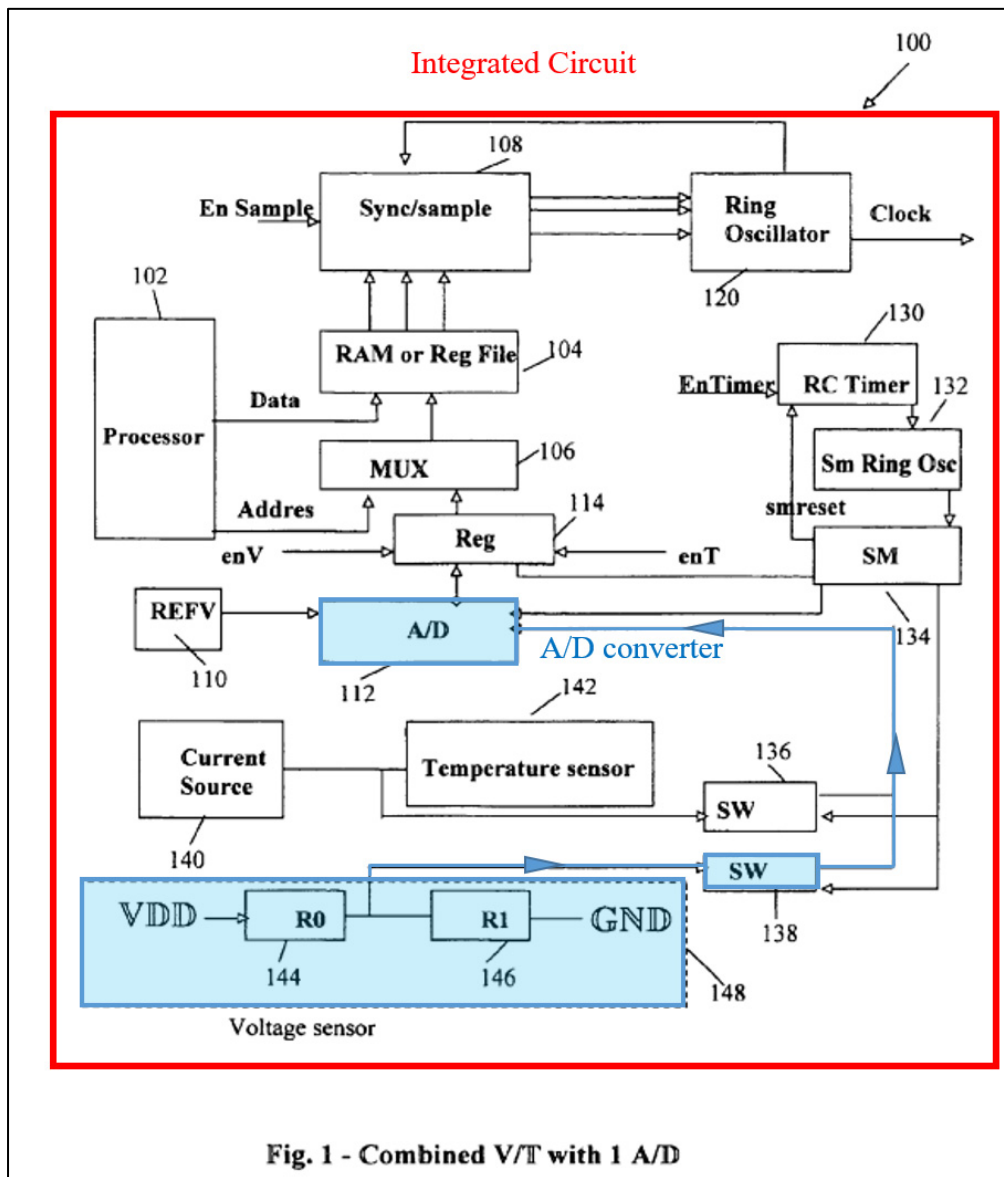


Fig. 1 - Combined V/T with 1 A/D

MTK-1006, FIG. 1

A POSITA would have understood that voltage values applied to the A/D converter would be translated to a digital value. MTK-1003, ¶179; MTK-1006, 4:15-17 (“This voltage ... value applied is translated to a digital value[.]”); MTK-1007, [0022].

14. **Claim 11**

Supra Ground 3, 1[b]. MTK-1003, ¶¶158, 180-182; MTK-1006, 2:63-3:10 (“The concatenated address can be applied to the address of a memory to retrieve a corrective value from a corrective table.”), 4:64-5:1 (“The table should produce a desired center frequency that operates as close as possible to the desired frequency when operating at nominal temperature and voltage.”), claim 16 (“retrieve a corrective value from a corrective table”), claim 17.

15. **Claim 23**

(a) Element 23[p]

The Norman Combination teaches a system for circuit control as set forth below. MTK-1003, ¶183; *see also* Ground 3, 1[p]-1[c], *supra*.

(b) Element 23[a]

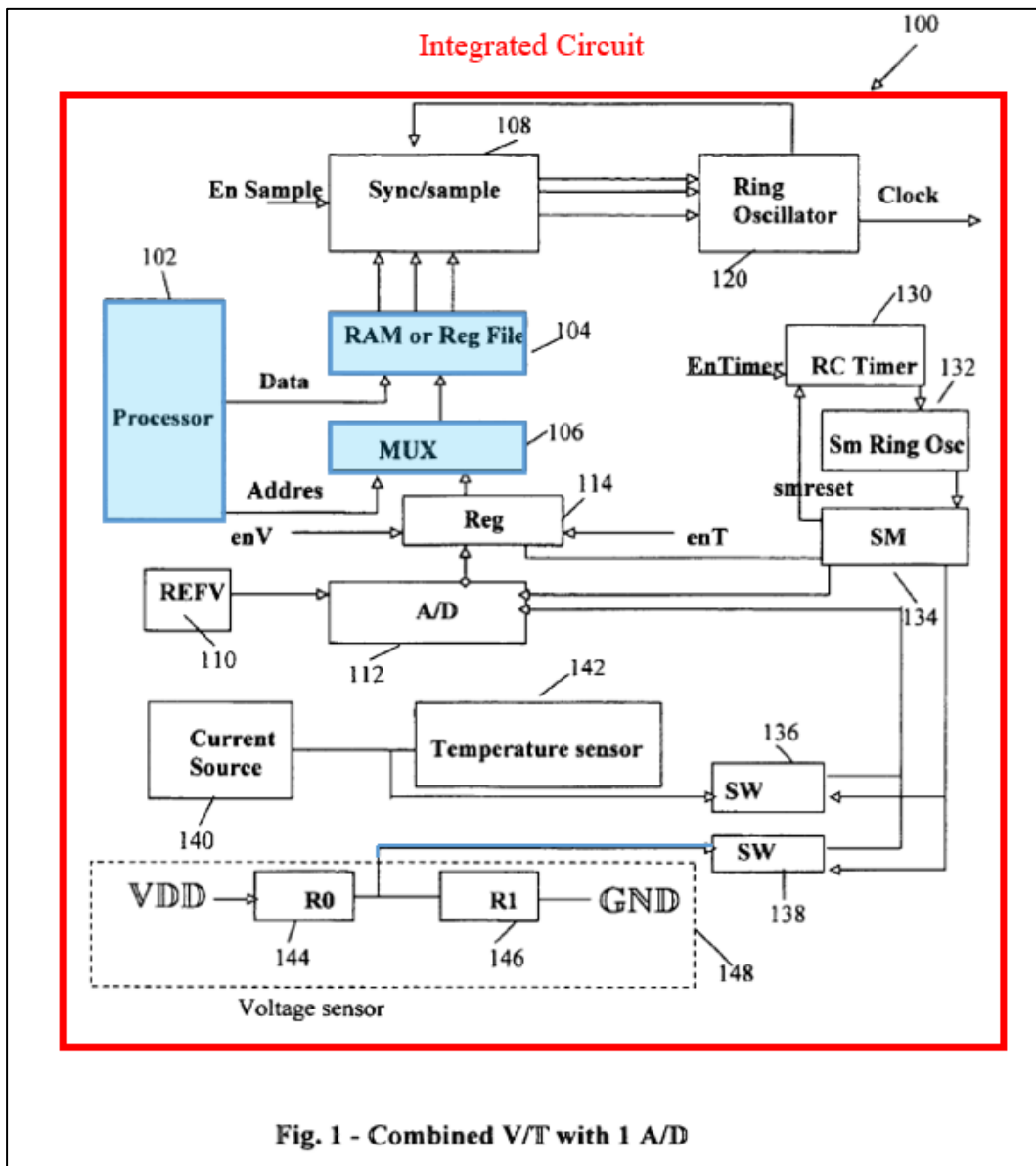
Supra Ground 3, 1[p] and 1[a]. MTK-1003, ¶¶184-185.

(c) Element 23[b]

Supra Ground 3, 1[p] and 1[b]. MTK-1003, ¶¶186-188.

The Norman Combination specifically discloses at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit. *Id.* For example, the Norman Combination discloses that, after sensing voltage and temperature values, those values are applied to the ADC 112, and the “output of the ADC 112 is registered and applied to the multiplexor 106,” which is driven by an address from the processor 102.” MTK-1006, 4:15-20.

“The output of the multiplexor 106 is applied to the memory 104 as the address input” and, “[a]t initialization, the processor 102 writes adjustment values into the RAM or Register File 104,” and the “output of the RAM 104 ... acts as the adjustment vector that is applied to the ring oscillator 120” to “select[] the ring frequency.” MTK-1006, 4:20-29. In other words, the Norman Combination’s multiplexor provides the RAM with an address input, its processor provides the RAM with adjustment values, and then the RAM uses the address input and adjustment values to determine the appropriate frequency for the portion of the integrated circuit using a lookup table. MTK-1003, ¶¶187-188; MTK-1006, 2:63-3:3, 4:64-5:1, claim 7. Thus, a POSITA would have understood that at least the Norman Combination’s processor 102, multiplexor 106, and RAM or Register File 104 comprise, or consist of, logic blocks for determining the appropriate frequency for a portion of the integrated circuit. MTK-1003, ¶188.



MTK-1006, FIG. 1

(d) Element 23[c]

Supra Ground 3, 1[p], 1[b], and 1[c]. MTK-1003, ¶¶189-191.

The Norman Combination specifically discloses at least one circuitry arrangement (including the sync/sample module 108 and the ring oscillator 120) to

provide the appropriate frequency (i.e., “clock”) to the portion of the integrated circuit. *Id.* For example, the Norman Combination discloses that “[t]he output of the memory or register file 104 drives a sync/sample module 108, which in turn drives a ring oscillator 102” that “generates a system clock[.]” MTK1006, 3:60-65. According to the Norman Combination, “[w]hen a calibration sequence occurs the output of the memory [i.e., the corrective vector for the frequency] may change in value or remain the same. Whenever this sequence occurs the Sync/Sample has the job of determining if there is a new value or the same value exists... If there is a new vector the state machine will be activated[.]” MTK-1006, 6:10-18. “When the new vector is loaded the output will then drive the input to the ring oscillator[.]” *Id.* at 6:30-32. According to the Norman Combination, the ring oscillator “provides a plurality of clock signal signals, each of which can be used to clock a portion of the chip,” i.e., a portion of the integrated circuit, “to prevent clock degradation due to too much load on the chip.” MTK-1006, 6:67-7:3; MTK-1003, ¶191. Thus, a POSITA would have understood that at least the Norman Combination’s sync/sample module and ring oscillator comprise, or consist of, circuitry arrangements for providing the appropriate frequency to the portion of the integrated circuit. MTK-1003, ¶191.

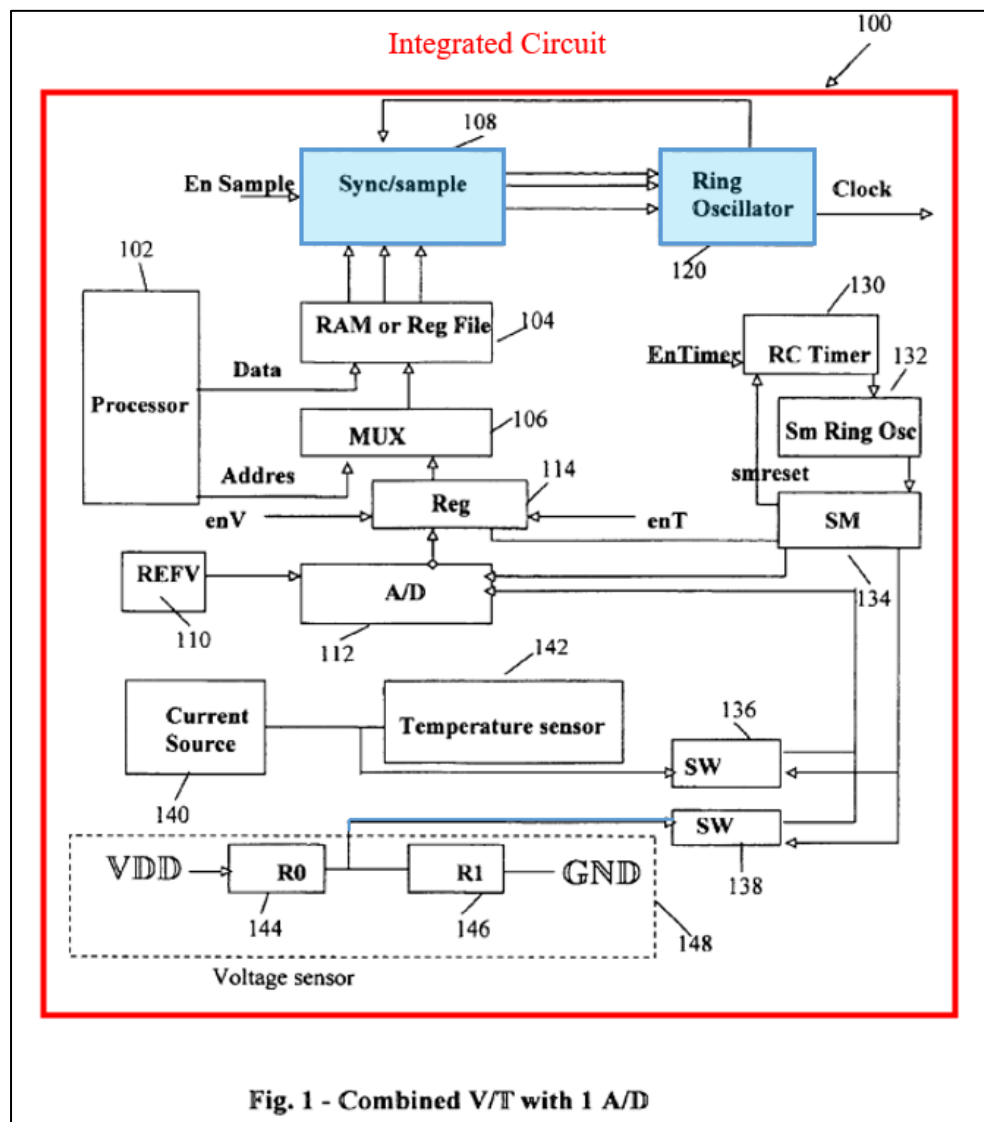


Fig. 1 - Combined V/T with 1 A/D

MTK-1006, FIG. 1

16. Claim 24

Supra Ground 3, claim 3. MTK-1003, ¶192.

17. Claim 31

Supra Ground 3, claim 10. MTK-1003, ¶193.

18. Claim 32

Supra Ground 3, claim 10. MTK-1003, ¶193.

19. **Claim 33**

Supra Ground 3, claim 11. MTK-1003, ¶194.

20. **Claim 34**

Supra Ground 3, claim 11. MTK-1003, ¶195.

21. **Claim 35**

(a) Element 35[p]

The Norman Combination teaches a system for circuit control as set forth below. MTK-1003, ¶196; *see also* Ground 3, 1[p]-1[c] and 23[p]-23[c], *supra*.

(b) Element 35[a]

Supra Ground 3, 1[p] and 1[a]. MTK-1003, ¶¶197-198.

(c) Element 35[b]

Supra Ground 3, 1[p], 1[b], 23[b]. MTK-1003, ¶¶199-202, 203-206.

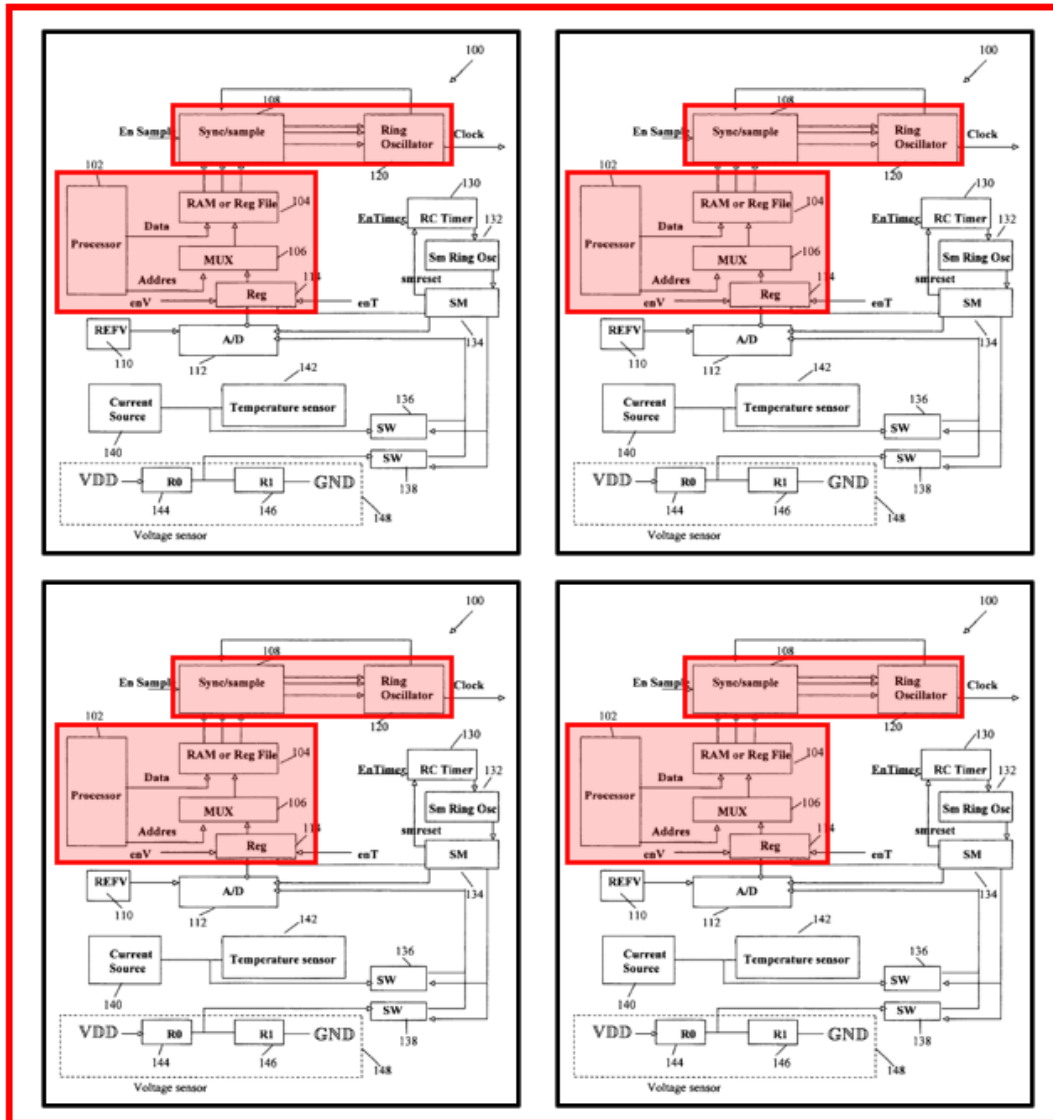
As addressed above, the Norman Combination (1) discloses employing multiple voltage sensors, Ground 3, 1[a], *supra*, (2) teaches that its ring oscillator “provides a plurality of clock signal signals, each of which can be used to clock a portion of the chip,” i.e., a portion of the integrated circuit, MTK-1006, 6:67-7:3, and (3) that its frequency adjustment mechanism could be applied to individual sub-systems located in the integrated circuit, MTK-1007, [0030] (“This process of calibration and correction can be conducted for each sub-system of the IC.”).

MTK-1003, ¶200

Moreover, it would have been obvious to a POSITA that the Norman

Combination's dynamic frequency adjustment mechanism could be employed in multiprocessor (or multi-core) integrated circuits, including very large-scale integration (i.e., VLSI) devices, multi-chip modules (i.e., MCMs), and multiprocessor systems on a chip (MPSoCs), wherein each processor or core includes a plurality of logic blocks for determining a frequency for a portion of the integrated circuit, and a plurality of circuitry arrangements for providing those frequencies to the portions of the integrated circuit. MTK-1003, ¶¶201-202; MTK-1007, [0033] ("the invention is ... is capable of numerous rearrangements, modifications, and substitutions").

Plurality of logic blocks / circuitry arrangements



MTK-1003, ¶202 (MTK-1006, FIG. 3 in potential multi-chip module)

(d) Element 35[c]

Supra Ground 3, 1[p], 1[b], 1[c], 23[b], 23[c], and 35[b]. MTK-1003,

¶¶199-202, 203-206.

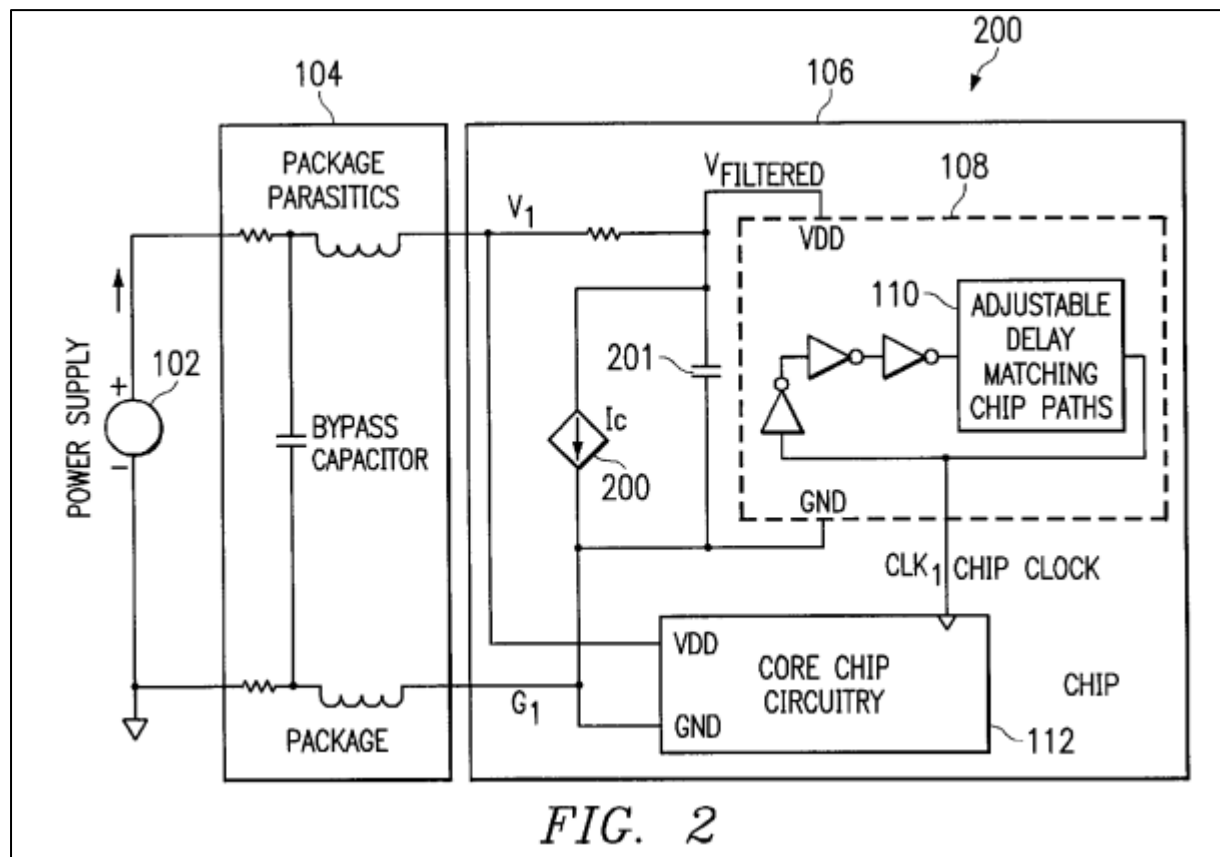
D. GROUND 4—Claims 1, 3, 10, 23, 24, 31, 32, and 35 are obvious over Naffziger '788

1. Overview of Naffziger '788

Naffziger '788 shares an inventor with the '563 patent, but is unrelated to the '563 patent and issued approximately five months before its earliest possible priority date. *Compare* MTK-1001 ("Jun. 20, 2003"), *with* MTK-1008 ("Jan. 21, 2003"). Naffziger '788 relates "to a system and method that utilize an on-chip voltage controlled oscillator to dynamically generate an appropriate clock frequency for the chip based on the voltage being drawn by the chip." MTK-1008, 1:16-21; MTK-1003, ¶208. Specifically, Naffziger '788 "is directed to a system and method which utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip," i.e., portions of the integrated circuit. MTK-1008, 4:9-12; *see also id.* at 1:25 ("[i]ntegrated circuits" are "chips").

According to Naffziger '788, "the voltage controlled oscillator of a most preferred embodiment is controlled by the same voltage as the core of the chip (e.g., the microprocessor), and therefore upon a voltage droop occurring in the core circuitry of the chip, the voltage droop is also received by the oscillator, resulting in the oscillator decreasing its output frequency." *Id.* at 4:31-39. In one "alternative embodiment, a sensor (e.g., a thermal or voltage sensor) is utilized." *Id.* at 4:47-48. "[I]n this alternative embodiment," which is depicted in FIG. 2, "sensor(s), such as a voltage sensor ..., may be utilized to monitor the voltage level drawn by core circuitry 112," i.e., a portion of the integrated circuit, "and may

communicate such voltage level to control circuitry 200.” *Id.* at 7:9-16. “In turn, control circuitry 200 may control the voltage input to oscillator 108, thereby dynamically controlling the output frequency of oscillator 108 (i.e., the frequency of CLK₁),” i.e., an appropriate frequency, which is thereafter provided to core circuitry 112, “to manage the chip’s power consumption.” *Id.* at 7:16-20.



MTK-1008, FIG. 2

See also MTK-1003, ¶209.

Like the '563 patent, Naffziger '788 claims embodiments that: (1) sense a delivered voltage to a portion of an integrated circuit; (2) determine an appropriate

frequency for the portion of the integrated circuit; and (3) provide the appropriate frequency to the portion of the integrated circuit. *E.g.*, MTK-1008, claims 1, 15, and 24; MTK-1003, ¶210.

2. Claim 1

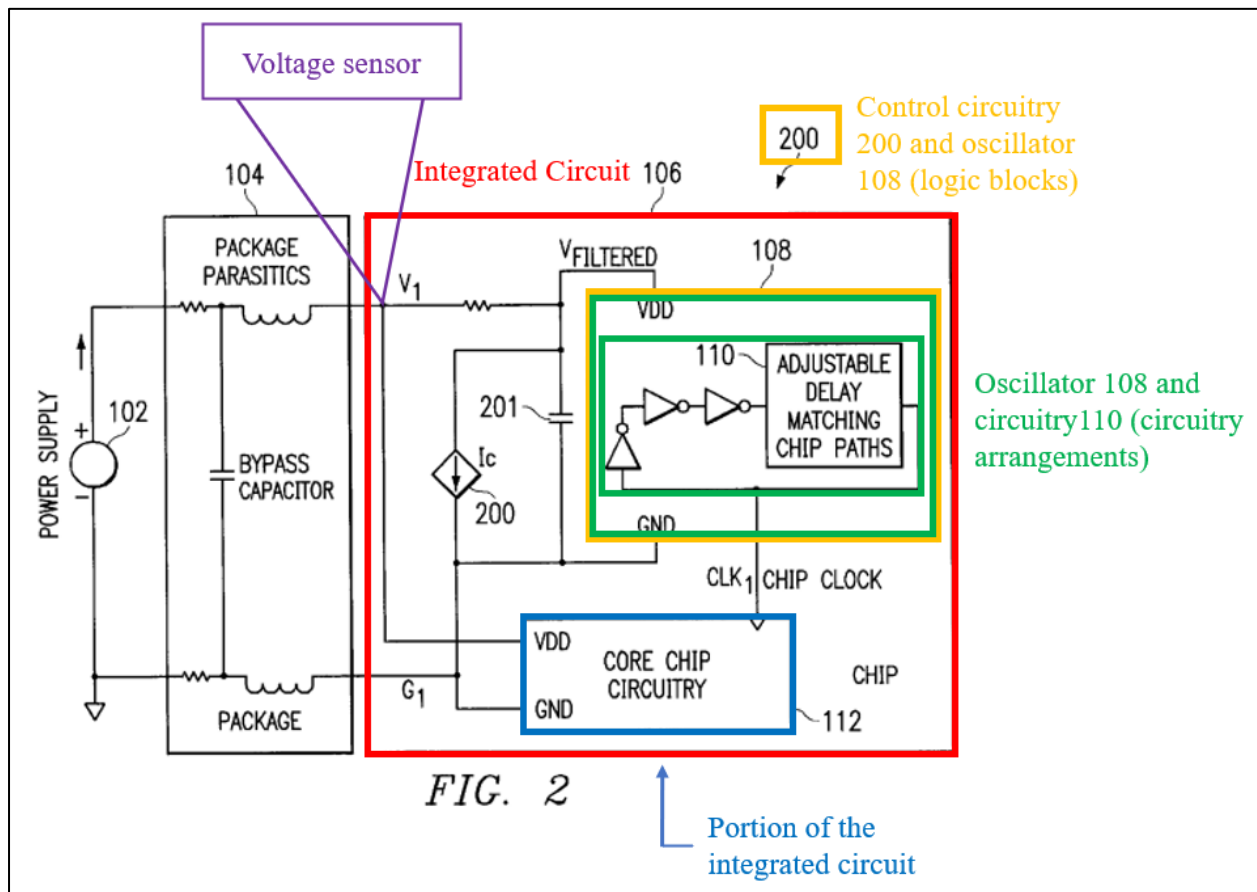
(a) Element 1[p]

To the extent the preamble is limiting, Naffziger '788 discloses a method of circuit control. *Infra* Ground 4, 1[a]-1[c]; MTK-1003, ¶¶211-212. Specifically, Naffziger '788 discloses a “method” which “utilize[s] an on-chip oscillator to provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit, “based on the voltage supplied to such oscillator to effectively manage the chip’s power consumption.” MTK-1008, Abstract; *id.* at 1:16-21, 3:62-4:3, 4:9-5:10, claim 1 (“A method ... comprising: [1] supplying voltage to said integrated circuit; [2] utilizing an oscillator included on said integrated circuit to generate a clock signal to be utilized by said integrated circuit; and [3] dynamically adjusting the clock signal’s frequency in response to changes in voltage supplied to said integrated circuit[.]”).

(b) Element 1[a]

Naffziger '788 discloses sensing a delivered voltage to a portion of an integrated circuit. MTK-1008, Abstract, 1:16-21, 3:62-4:3, 4:9-5:10, 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3; MTK-1003, ¶¶213-214.

Specifically, Naffziger '788 discloses one embodiment that utilizes “sensor(s), such as a voltage sensor,” “to monitor [i.e., sense] the voltage level drawn by core circuitry 112,” i.e., a portion of the integrated circuit. MTK-1008, 7:13-16; *id.* at 7:28-30 (“circuitry (e.g., sensors) may be included for monitoring the value of voltage V_1 ”); MTK-1003, ¶213. Though the “circuitry,” i.e., voltage sensors, “that monitors the value of the voltage V_1 input to chip 106” is “not shown” in any figures, MTK-1008, 7:35-36, it would have been obvious to a POSITA to include the voltage sensor(s) (purple) in chip 106 (red) of at least the embodiment shown in FIG. 2, to sense the delivered voltage V_1 being delivered to core chip circuitry 112 (blue), representing a portion of the integrated circuit. MTK-1003, ¶214.



MTK-1008, FIG. 2

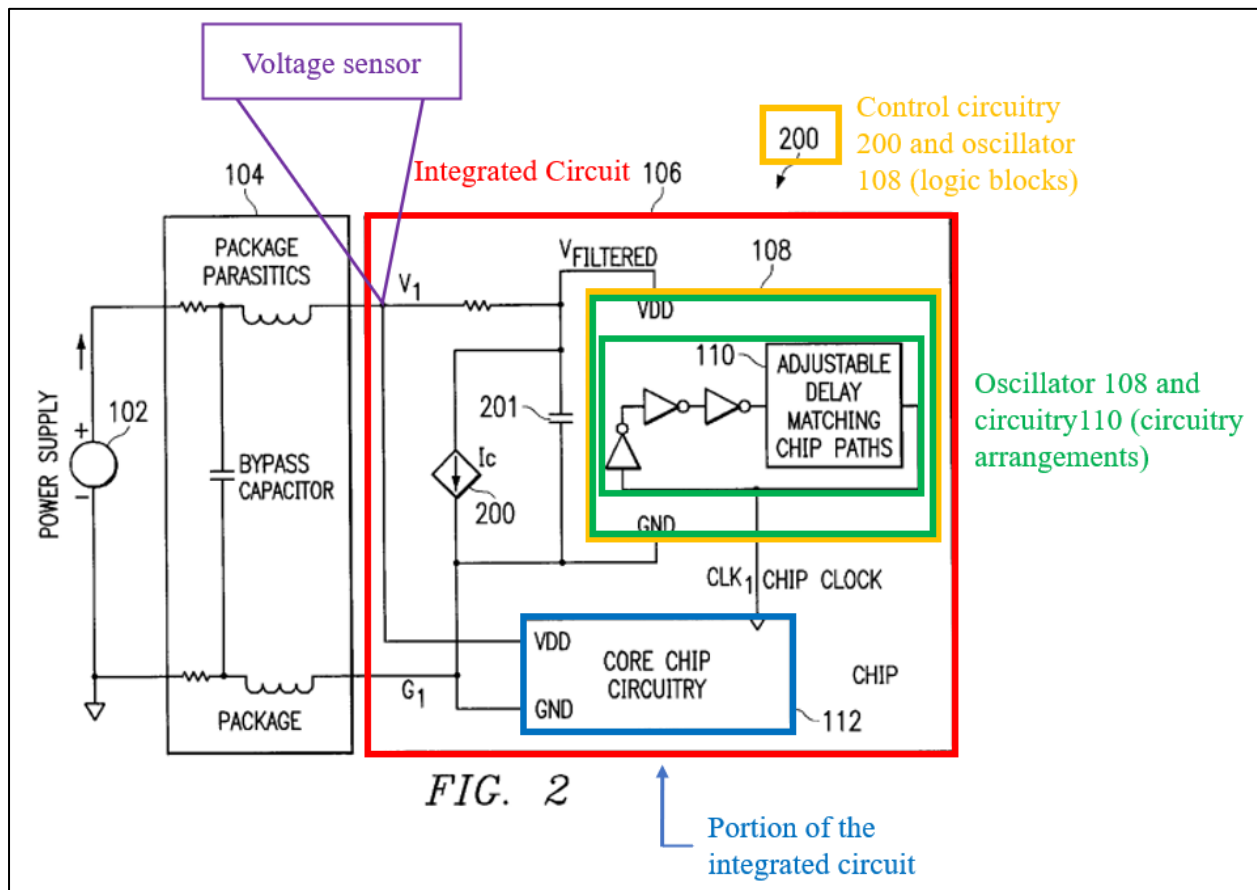
(c) Element 1[b]

Naffziger '788 discloses determining an appropriate frequency for the portion of the integrated circuit. MTK-1008, Abstract (disclosing method for determining “*appropriate clock frequency for components of the chip*”), 1:16-21, 3:62-4:3, 4:9-5:10, 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3; MTK-1003, ¶¶215-217. Specifically, Naffziger '788 discloses utilizing “an on-chip oscillator” that “can dynamically adjust ... clock frequency,” and “provide the appropriate clock frequency for components of the chip,” i.e., portions of the

integrated circuit. MTK-1008, 4:9-17; MTK-1003, ¶216. According to Naffziger '788:

[S]ensor(s), such as a voltage sensor ..., may be utilized to monitor the voltage level drawn by core circuitry 112, and may communicate such voltage level to control circuitry 200. In turn, control circuitry 200 may control the voltage input to oscillator 108, thereby dynamically controlling the output frequency of oscillator 108 (i.e., the frequency of CLK) to manage the chip's power consumption.

MTK-1008, 7:9-20; *id.* at 4:47-56; MTK-1003, ¶217. Thus, it would have been obvious to a POSITA to: (1) monitor a voltage delivered to a component of the chip, i.e., a portion of the integrated circuit, such as core chip circuitry 112, using one or more voltage sensors; (2) determine the “appropriate frequency” for the component using oscillator 108 and control circuitry 200, i.e., logic blocks; and (3) provide the appropriate frequency, e.g., CLK₁, to the component using clock oscillator 108 and circuitry 110, i.e., circuitry arrangements. MTK-1003, ¶217.



MTK-1008, FIG. 2

(d) Element 1[c]

Supra Ground 4, 1[b]. MTK-1003, ¶218.

3. Claim 3

Naffziger '788 discloses having the appropriate frequency be the maximum frequency possible for the portion of the integrated circuit at the delivered voltage. MTK-1003, ¶219. Specifically, Naffziger '788 discloses an embodiment that “allows for operation at the highest processing speed (*or fastest clock frequency*) that is possible,” i.e., maximum frequency possible, “while remaining within a

desired power consumption.” MTK-1008, 8:61-64. For example, according to Naffziger ’788, “the chip’s clock frequency supplied by on-chip oscillator 108 can dynamically adjust such that it is consistently at the *fastest frequency possible* to remain within the desired power consumption.” *Id.* at 8:64-67.

4. Claim 10

It would have been obvious to a POSITA to calculate a value for the delivered voltage. MTK-1003, ¶¶220-221. For example, Naffziger ’788 incorporates the disclosure of U.S. patent application Ser. No. 09/811,243, filed Mar. 16, 2001, by reference. MTK-1008, 1:8-13. That application issued as U.S. Patent No. 6,489,834 to Naffziger et al. (“Naffziger ’834”) on December 3, 2002. MTK-1014. Naffziger ’834, in turn, discloses a “voltage comparator,” i.e., a voltage sensor, comprising “an analog to digital converter.” MTK-1014, 4:46-48, 5:15-17, 7:26-34, 7:56-58 (“an A/D converter may be utilized to convert the analog voltage signal to a digital signal”). Because Naffziger ’788 incorporates Naffziger ’834’s discussion of A/D converters by reference, it would have been obvious to a POSITA that Naffziger ’788’s voltage sensor could be an A/D converter that is used to calculate a digital value for the delivered voltage. MTK-1003, ¶221; *see also* MTK-1001, 5:49-51, 5:55-57.

5. Claim 23

(a) Element 23[p]

Naffziger '788 teaches a system for circuit control. MTK-1003, ¶222; *see also* Ground 4, 1[p]-1[c], *supra*.

(b) Element 23[a]

Supra Ground 4, 1[p] and 1[a]. MTK-1003, ¶223.

(c) Element 23[b]

Supra Ground 4, 1[p] and 1[b]. MTK-1003, ¶224.

(d) Element 23[c]

Supra Ground 4, 1[p], 1[b], and 1[c]. MTK-1003, ¶225.

6. Claim 24

Supra Ground 4, claim 3. MTK-1003, ¶226.

7. Claim 31

Supra Ground 4, claim 10. MTK-1003, ¶227.

8. Claim 32

Supra Ground 4, claim 10. MTK-1003, ¶227.

9. Claim 35

(a) Element 35[p]

Naffziger '788 teaches a system for circuit control. MTK-1003, ¶228; *see also* Ground 4, 1[p]-1[c] and 23[p]-23[c], *supra*.

(b) Element 35[a]

Supra Ground 4, 1[p] and 1[a]. MTK-1003, ¶¶229-230; *see also* MTK-1008, 7:13-14 (“sensor(s), such as a voltage sensor), 7:29 (“sensors”).

It would have been obvious to a POSITA, based on Naffziger '788, to utilize a plurality of voltage sensors for sensing delivered voltages to different portions of an integrated circuit. MTK-1003, ¶230; MTK-1008, 7:13-14, 7:29. For example, it would have been obvious to a POSITA to utilize Naffziger '788's one or more voltage sensors to "monitor the voltage level drawn," MTK-1008, 7:13-15, by different "components of the chip," *id.* at 4:9-12, i.e., different portions of an integrated circuit. MTK-1003, ¶230.

(c) Element 35[b]

Supra Ground 4, 1[p], 1[b], 23[b]. MTK-1003, ¶¶231-232.

It would have been obvious to a POSITA, based on Naffziger '788, to include a plurality of logic blocks arranged to determine an appropriate frequency for each said portion from said delivered voltages. MTK-1003, ¶232. For example, it would have been obvious to a POSITA that Naffziger '788's oscillator 108 and control circuitry 200 comprise a plurality of logic blocks. *Id.* Indeed, Naffziger '788 discloses that control circuitry 200 could be "implemented on chip 106 with software [or firmware] executing thereon for managing the chip's power consumption." MTK-1008, 7:20-23. A POSITA would have understood that the control circuitry 200 "may control the voltage input to oscillator 108, thereby dynamically controlling the output frequency of oscillator 108" to the various components of the chip, i.e., portions of the integrated circuit. MTK-1008, 7:16-

20; MTK-1003, ¶232.

(d) Element 35[c]

Supra Ground 4, 1[p], 1[b], 1[c], 23[b], 23[c], and 35[b]. MTK-1003, ¶¶233-234.

It would have been obvious to a POSITA, based on Naffziger '788, to include a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency. MTK-1003, ¶234. For example, Naffziger '788 discloses that “circuitry 110, which is well known to those of ordinary skill in the art, is included in oscillator 108 to adjust the frequency of CLK based on the value of voltage V_1 .” MTK-1008, 6:24-27. Naffziger '788 discloses that “[s]uch circuitry 110 may include any switched capacitive or resistive elements,” i.e., circuitry arrangements, “that effect the loop delay of ring oscillator 108,” and that such circuitry “are generally well known in the art[.]” *Id.* at 6:27-31. It would have been obvious to a POSITA that oscillator 108 and circuitry 110 comprise a plurality of circuitry arrangements that are used to provide each component of the chip, i.e., each portion of the integrated circuit, its associated appropriate frequency. MTK-1003, ¶234; MTK-1008, Abstract (“utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip”), 4:9-12 (same), FIGS. 1-2.

IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION

A. Discretionary denial under §325(d) is not warranted

Advanced Bionics and the *Becton* factors strongly favor institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (“*Advanced Bionics*”) (precedential); *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15 2017) (“*Becton*”) (precedential).

1. Tam and Huard

While both Tam and Huard were considered by the Examiner during prosecution, and served as a basis for rejection, MTK-1002, 27, the Examiner materially erred in his evaluation of the asserted prior art. *Becton* factors (e) and (f), considered under prong two of the *Advanced Bionics* framework, strongly favor institution. *Becton, Dickinson* at 17-18.

First, the Examiner considered only anticipation under 35 U.S.C. § 102(b), MTK-1002, 27, despite both Tam and Huard indisputably qualifying as prior art to the '563 patent under 35 U.S.C. § 102(e). Because both references qualify as prior art under § **102(e)**, Applicant's sole argument that “neither *Tam* nor *Huard* are prior art under 35 U.S.C. § **102(b)**,” MTK-1002, 23, should not have been dispositive. This is especially true where, as here, the Applicant did not even

attempt to dispute the Examiner's finding that both Tam and Huard expressly teach the method and device for circuit control embodied in the Challenged Claims. *See* MTK-1002, 23. Indeed, as demonstrated in this Petition, and with reference to Dr. Min's testimony, both Tam and Huard disclose, among other things: (1) sensing a delivered voltage to a portion of an integrated circuit, (2) determining an appropriate frequency for the portion of the integrated circuit, and (3) providing the appropriate frequency to the portion of the integrated circuit. Sections III.A-B, *supra*. Thus, by failing to recognize that Tam and Huard still qualify as prior art under 102(e), "the Office erred in a manner material to the patentability of all of the challenged claims." *Apple Inc. v. Immervision, Inc.*, No. IPR2023-00471, 2023 WL 5166410, at *13 (P.T.A.B. July 11, 2023). Had the Office recognized that Tam and Huard qualify as 102(e) prior art, the Office would not have reached its erroneous finding of patentability of the Challenged Claims. MTK-1003, ¶44.

Second, by focusing solely on anticipation, the Examiner failed to consider whether Tam or Huard, either individually or in combination, render obvious the Challenged Claims under 35 U.S.C. § 103. As demonstrated in this Petition with reference to Dr. Min's testimony, the Examiner's failure to consider the obviousness of the Challenged Claims over the Tam and Huard references constitutes material error, warranting reconsideration. *Advanced Bionics*, Paper 6, 10. For at least this additional reason, Petitioner respectfully submits that

discretionary denial is unwarranted, and that the Board should instead institute IPR based on the instant Petition's grounds.

2. Norman '259, Norman '851, and Naffziger '788

Advanced Bionics Part 1—The examiner never issued a rejection over the Norman '259, Norman '851, or Naffziger '788 references during the '563 patent's prosecution. *See generally* MTK-1002. Moreover, these references were not cited by the examiner during prosecution, and are not listed on the face of the '563 patent. *See generally* MTK-1001; MTK-1002. Thus, there is no indication that the examiner substantively considered these references.

Additionally, because the applicant never provided arguments relating to the claimed technology in response to **any** rejections during prosecution of the '563 patent, the Petition's art and arguments cannot be said to be the same as, or substantially similar to, art and arguments previously presented to the Office in connection with the '563 patent. *See generally* MTK-1002. Accordingly, neither condition of the first prong of the *Advanced Bionics* framework is met.

Becton factors [a], [b], and [d] further counsel in favor of institution. None of Norman '259, Norman '851, and Naffziger '788 were addressed during prosecution (factor [a]), nor are they cumulative of other art relied on or considered by the examiner (factor [b]). *Id.* There are also no overlapping arguments (factor [d]) between the prosecution record and Grounds 3 and 4 above. Thus, *Becton*,

Dickinson factors [a], [b], and [d] favor Petitioner.

Advanced Bionics Part 2—The Board need not reach the second prong to resolve against discretionary denial under Section 325(d), since the first prong is not satisfied. *See Oticon Medical AB et. al. v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019) (precedential) (no discretionary denial under §325(d) because of “new, noncumulative prior art asserted in the Petition”). Nonetheless, each of *Becton*, *Dickinson* factors [c], [e], and [f] favors Petitioner. None of Norman ’259, Norman ’851, and Naffziger ’788 was cited during prosecution, and thus did not form the basis of any rejection (factor [c]). As for factors [e] and [f], by not considering Norman ’259, Norman ’851, Naffziger ’788, or combinations based on them, the Office erred in its evaluation of the prior art, thus warranting reconsideration. *Advanced Bionics*, Paper 6, 10. Grounds 3 and 4 demonstrate why further consideration is warranted in view of these references.

B. Discretionary denial under §314(a) is not warranted

1. The *General Plastic* Factors Weigh Against Exercising Discretion To Deny Institution

In *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357-01361, Paper 19 at 9-10 (Sept. 6, 2017) (PTAB Precedential), the Board identified seven factors that inform application of discretionary institution denials under 35 U.S.C. §314(a). Given this is the first ever petition to be filed

against the '563 Patent, the *General Plastic* factors do not apply. *See Acronis, Inc., v. Realtime Data LLC*, IPR2018-00706, Paper 11, 15-16 (Oct. 1, 2018).

2. **The *Fintiv* Factors Weigh Against Exercising Discretion To Deny Institution**

The PTAB considers a set of non-exclusive factors (the *Fintiv* factors) in determining whether to institute an IPR proceeding where there is parallel district court litigation. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020). On June 21, 2022, Director Vidal issued “binding agency guidance” entitled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation.” MTK-1015 (hereinafter the “Interim Guidance”). This Interim Guidance presents “several clarifications... to the PTAB’s... application of *Fintiv* to discretionary institution where there is parallel litigation.” *Id.*, 2.

One clarification provided by the Interim Guidance specifies the effect of particular types of stipulations presented by petitioners on the Board’s application of the *Fintiv* framework. *Id.*, 3, 7-8. In particular, the Interim Guidance unequivocally states that “***the PTAB will not discretionarily deny institution*** of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” *Id.*,

7 (emphasis added) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020)). In the present case, Petitioner presents a stipulation not to pursue in the parallel district court proceeding the same grounds as in the present Petition or any grounds that could have reasonably been raised in the present Petition. *See* MTK-1016. Accordingly, based on the Interim Guidance, institution of the present Petition ***should not*** be discretionarily denied in view of the parallel district court proceeding. *See* MTK-1015, 7.

V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

MediaTek Inc. is petitioner and real party-in-interest. MediaTek USA Inc. is an additional real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

MOSAID Technologies Inc. (“MOSAID”)—the alleged Patent Owner—filed a complaint asserting the ’563 patent against MediaTek on March, 28, 2023 in

the U.S. District Court for the Eastern District of Texas (Case No. 2:23-cv-00129).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR44508-0023IP2@fr.com.

Respectfully submitted,

Dated: March 5, 2024

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CERTIFICATION UNDER 37 C.F.R. §42.24

Under the provisions of 37 C.F.R. §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,956 words, which is less than the 14,000 allowed under 37 C.F.R. §42.24.

Dated: March 5, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on March 5, 2024, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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