

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Naffziger
U.S. Patent No.: 7,224,563 Attorney Docket No.: 44508-0023IP2
Issue Date: May 29, 2007
Appl. Serial No.: 10/651,360
Filing Date: August 29, 2003
Title: METHOD AND DEVICE FOR CIRCUIT CONTROL

DECLARATION OF PAUL MIN, Ph.D.

I, Paul Min, Ph.D., of St. Louis, Missouri, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of MediaTek Inc. (“Petitioner” or “MediaTek”). I understand that MediaTek is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 7,224,563 (“the ’563 patent”) (MTK-1001).

2. I have been asked to provide my independent analysis of the ’563 patent in light of the prior art publications cited below.

3. I am not currently an employee of MediaTek. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’563 patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’563 patent.

II. QUALIFICATIONS

4. A summary of my background and qualifications as a technical expert for this case is provided below. A complete listing of my qualifications and background are detailed in my curriculum vitae (“CV”), which is attached hereto as Appendix A. Among other things, my CV includes a list of my issued patents and publications. My curriculum vitae also includes information about my expert witness experience, with case numbers where available.

5. I received a B.S. degree in Electrical Engineering in 1982, an M.S. degree in Electrical Engineering in 1984, and a Ph.D. degree in Electrical Engineering in 1987 from the University of Michigan in Ann Arbor. I received several academic honors, including my B.S. degree with honors, a best graduate student award and a best teaching assistant award during my M.S. study, and a best paper award from a major international conference for reporting results from my Ph.D. thesis.

6. After receiving my Ph.D., I worked at Bellcore in New Jersey from August 1987 until August 1990. At Bellcore, I was a member of the team responsible for evolving the public switched telephone network (PSTN) into a multi-services voice and data network that incorporated packet switches, optical technologies, and wireless technologies.

7. In September 1990, I joined the faculty at Washington University in St. Louis. In July 1996, I was promoted to an Associate Professor of Electrical Engineering with tenure. I am currently a Senior Professor of Electrical and Systems Engineering at Washington University in St. Louis. I have served as the Chair of the Graduate Curriculum (2000-2002) and the Chair of the Undergraduate Curriculum (2011-2014) for the Electrical and Systems Engineering department.

8. At Washington University, I have conducted research in communication, computing, and related electronic hardware and software. I have received several grants from the U.S. Federal Agencies, including the National Science Foundation and the Defense Advanced Research Project Agency, the Air Force Office of Scientific Research, and numerous contracts from companies and organizations around the world.

9. As a faculty member at Washington University, I taught a number of courses in electronics, communication, and computing at both the undergraduate and graduate levels. For example, I have taught courses including electronic circuits, communication theory, data networks, transmission and multiplexing, and signaling and control of communication networks. I have supervised numerous graduate students, many of whom received a doctoral degree under my guidance.

10. In addition to my responsibilities as a university faculty member, I founded two companies. In May 1997, I founded MinMax Technologies, Inc., a

fabless semiconductor company that developed switch fabric integrated circuit chips for the Internet. In March 1999, I founded Erlang Technology, Inc., a fabless semiconductor company that focused on the design and development of integrated circuit chips and software for the Internet. One of Erlang's products received a best product of the year award in 2004 from a major trade journal for the electronics industry. In these companies, I have designed a number of circuits and software applications for the Internet and wireless communication networks. Specifically related to the technology at issue in the '563, many of the integrated circuit chips my companies developed were notoriously power-hungry (as many specialized communication chips do), requiring us to incorporate various power control mechanisms to assure the proper functioning of these chips.

11. Outside my own start-up companies, I have also served in various technology and business advisor roles for other companies and organizations around the world. I was the main technical author for one of two winning proposals to the Korean government for CDMA wireless service licenses (1996). I was responsible for designing a commercial scale IS-95 CDMA cellular network, which I understand to be one of the earliest such networks deployed in the world. I worked with numerous engineers and scientists around the world to implement this commercial-scale cellular network before IS-95 CDMA was widely accepted and deployed. This provided me with extensive insight into various components of CDMA technology,

which extensively use various transmission and switching technologies. I have also been involved in a semiconductor company that specializes in semiconductor memories such as flash EEPROMs as a board member and as a technical advisor (2007-2011).

12. I am a member of and have been actively involved in a number of professional organizations. For example, I have served as the Chair of the Saint Louis Section of the IEEE with more than 3,000 members (2014), and a member of the Eta Kappa Nu Honor Society for electrical engineers. I have also been an Ambassador of the McDonnell International Scholars Academy (2007-2013).

13. I am a named inventor on eleven U.S. patents. I have extensively published technical papers in international conferences and journals, technical memoranda and reports, and given a number of seminars and invited talks. I have organized several international conferences and served as an international journal editor.

14. I have also served as an expert in certain legal proceedings. A list of cases in which I have testified at trial, hearing, or by deposition is provided in my *curriculum vitae* (Appendix A). Over the past several years, I have been retained by patent owners as well as patent challengers in various IPR proceedings.

III. LEGAL PRINCIPLES

15. In forming my analysis and conclusions expressed in this declaration, I have applied the legal principles described in the following paragraphs, which were provided to me by counsel for the Petitioner.

A. Anticipation

16. It is my understanding that invalidation by “anticipation” exists only if a single alleged prior art reference discloses each and every limitation of the claim at issue, either expressly or inherently. In other words, every limitation of the claim must appear in a single prior art reference for the reference to anticipate that claim. I also understand that all elements of the claim must be disclosed in the reference as they are arranged in the claim. I also understand that to be considered anticipatory, the prior art reference must be enabling and must describe the patentee’s claimed invention sufficiently to have placed it in the possession of a person of ordinary skill in the field of invention. Under the principles of inherency, I understand that if the prior art necessarily functions in accordance with or includes the claimed limitations, it anticipates.

17. I have been informed that a claim is invalid if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant’s invention. I further have been informed that a claim is invalid if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the

patent application (critical date). I have also been informed that a claim is invalid if an invention described by that claim was described in a U.S. patent granted on an application for a patent (or in a published application for a U.S. patent) that was filed by another in the U.S. before the date of invention for such a claim.

18. I understand that a dependent claim contains all of the limitations of the independent claim from which it depends. Thus, to establish anticipation, every limitation set forth in a dependent claim as well as the independent claim from which it depends must be found in an anticipatory reference.

B. Obviousness

19. I have been informed that a patent claim is invalid as “obvious” in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention (“POSITA”), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. I understand that a patent cannot be properly granted for subject matter that would have been obvious to a POSITA at the time of the alleged invention, and that a patent claim directed to such obvious subject matter

is invalid under 35 U.S.C. § 103. It is also my current understanding that in assessing the obviousness of claimed subject matter one should evaluate obviousness over the prior art from the perspective of a POSITA at the time the invention was made (and not from the perspective of either a layman or a genius in that art).

20. While I do not know the exact date that the alleged invention claimed in the '563 patent was made, I do know that the '563 patent was filed on August 29, 2003 (MTK-1001, Cover Page) and claims priority to a provisional application filed on June 20, 2003. For purposes of my analysis here, I have applied a date of June 20, 2003 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than June 20, 2003 (especially given the earlier publication or filing dates of the cited prior art references).

21. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and this reason may be

explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

22. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

23. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). Because I do not know at what date the alleged invention was

made, I have used the date of June 20, 2003 for reasons explained in ¶20 above. However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the late 1990s to early 2000s.

IV. PERSON OF ORDINARY SKILL IN THE ART

24. Based on my knowledge and experience in the field and my review of the '563 patent and its file history, and my first-hand knowledge of undergraduate electrical engineering curricula at the time of the '563 patent's alleged priority date of June 2003, I believe a person of ordinary skill in the art ("POSITA") at the time of the earliest possible priority date of the '563 patent would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

V. MATERIALS CONSIDERED

25. My analyses set forth in this declaration are based on my experience in the field of high performance circuit design, in particular power management of such

circuitries. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experience, I understand and know of the capabilities of persons of ordinary skill in this field during the late 1990s to early 2000s and specifically during the time before the earliest possible priority date (June 20, 2003) for the '563 patent, and I taught classes as part of the Electrical Engineering curricula, personally designed and implemented a number of circuitries that required active power management, and worked closely with many persons of such skill level in the field during that time frame.

26. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the earlier possible priority date for the '563 patent; my own knowledge and experiences gained from my work experience in the field of high performance circuit design generally; my experience in teaching and advising others in such subjects; and my experience in working with others involved in the field of high performance circuit design or similar fields. In addition, I have analyzed the following publications and materials:

- U.S. Patent No. 7,224,563 to Naffziger (“the '563 patent”) (MTK-1001) and its accompanying prosecution history (MTK-1002);
- U.S. Patent No. 6,762,629 to Tam et al. (“Tam”) (MTK-1004);

- U.S. Patent No. 6,885,233 to Huard et al. (“Huard”) (MTK-1005);
- U.S. Patent No. 6,853,259 to Norman et al. (“Norman ’259”) (MTK-1006);
- U.S. Patent Pub. No. 2003/0034851 to Norman et al. (“Norman ’851”) (MTK-1007);
- U.S. Patent No. 6,509,788 to Naffziger et al. (“Naffziger ’788”) (MTK-1008);
- Excerpts from Microsoft Computer Dictionary, Fifth Edition, Microsoft Press (2002) (MTK-1009);
- Excerpts from Modern Dictionary of Electronic, Seventh Edition Revised and Updated, Rudolf F. Graf (1999) (MTK-1010);
- Excerpts from Design For At-Speed Test, Diagnosis and Measurement, Kluwer Academic Publishers (2000) (MTK-1011);
- Excerpts from The Computer Engineering Handbook, CRC Press LLC (2002) (MTK-1012);
- U.S. Patent No. 5,428,790 to Harper et al. (“Harper”) (MTK-1013);
- U.S. Patent No. 6,489,834 to Naffziger et al. (“Naffziger ’834”) (MTK-1014);
- Syllabus to ESE 232 Introduction to Electronic Circuits (MTK-1017);
- Excerpts from Microelectronic Circuits, Fourth Edition, Sedra et al., Oxford University Press (1998) (MTK-1018); and
- Declaration of June Ann Munford (MTK-1020).

27. Although for the sake of brevity this Declaration refers to selected portions of the cited references, it should be understood that one of ordinary skill in the art would have viewed the references cited herein in their entirety, and in combination with other references cited herein or cited within the references themselves. The references used in this Declaration, therefore, should be viewed as being incorporated herein in their entirety.

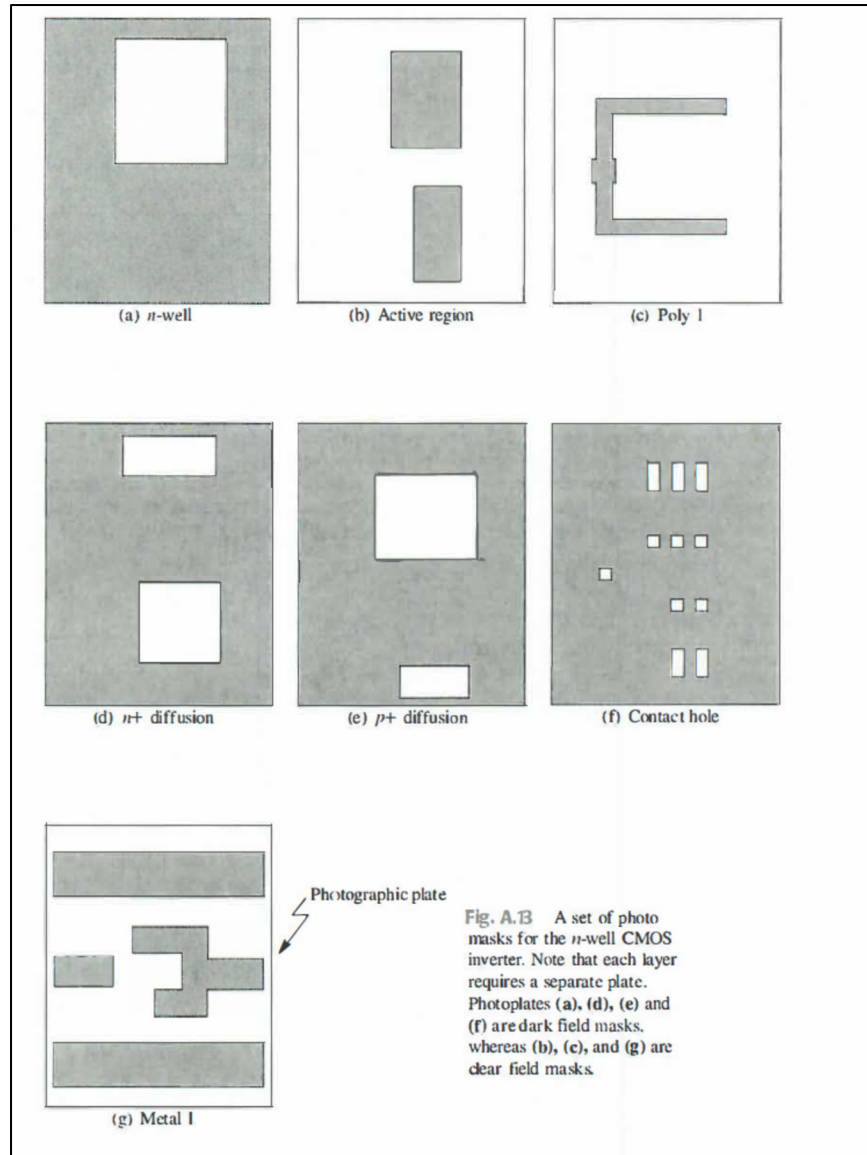
VI. BACKGROUND INFORMATION

A. Background of the Technology

28. In order to aid the understanding of the opinions I provide in the declaration, I now provide a brief background of the technology at issue. In doing so, I will refer to a popular undergraduate textbook entitled “Microelectronic Circuits,” Fourth Edition by Adel S. Sedra and Kenneth C. Smith 1998 (“Sedra”) (MTK-1018); MTK-1020, ¶¶18-20 (“*Microelectronic Circuits* was made available to the public shortly after its initial acquisition” by the “Penn State University library” on “August 19, 1997.”). Personally, I have taught an undergraduate course at Washington University in St. Louis referred to as ESE 232 Introduction to Electronic Circuits using various editions of Sedra as the main textbook. In what follows, I will quote various excerpts from the fourth edition of Sedra, which is the latest edition of Sedra prior to the alleged time of invention for the ’563 patent (i.e., the 2003 time frame).

29. At around the time of the alleged priority date for the '563 patent, a vast majority of the Very Large Scale Integration (VLSI) circuits were based on the Complementary Metal-Oxide-Semiconductor (CMOS) technology. MTK-1018 at A-4 (“Since the early 1980s, CMOS (complementary MOS) technology has almost completely dominated the SLSI scene.”).

30. Appendix A of Sedra illustrates a high-level overview of the VLSI processes. *Id.* at A-4 to A-13. In particular, after placing various components on the VLSI circuits, certain areas of the circuitry can be grouped together as part of the layout process as shown in the figure below.



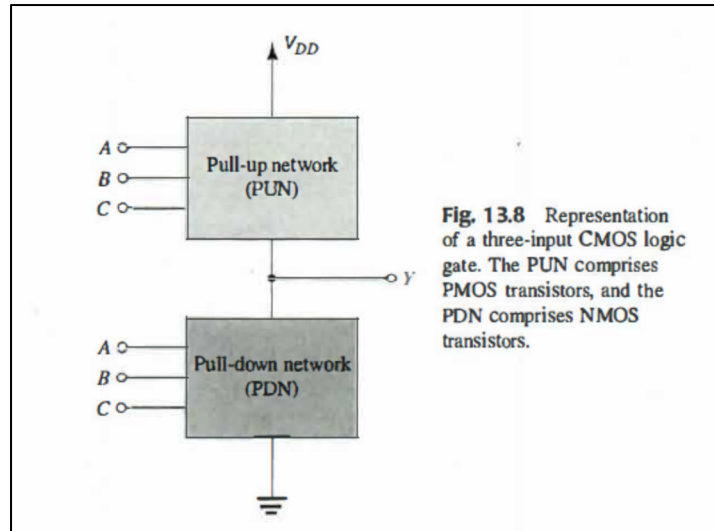
MTK-1018 at A-13

31. One particular portion of the VLSI area is noted as the active region (Fig. A-13 (b) above), where the active components (such as the transistors and diodes) are placed to implement the functions designed to be performed by the circuitry. As shown in the figure above, there are multiple distinct and separate active regions in a circuitry. For example, for a central processing unit (CPU), one

active region may correspond to the Arithmetic Logic Unit (ALU), another active region may be a Static Random Access Memory (SRAM), yet another may be interface module, and so on. While these active regions together implement the overall required functions of the CPU, by in large, they operate independently with different levels of requirements such as the clock speed and power consumption level.

32. Many types of Application Specific Integrated Circuits (ASICs) have extremely high levels of complexity and performance requirements. For example, switch fabric chips, like those I personally designed over the past 30+ years, required a very high number of input/output pins (in excess of thousand), a high power consumption level (tens of watts), and a very high clock frequency (multiple gigabits per second). In addition, the resulting chip designs required a large surface dimension (multiple square inches), comprising many distinct active regions. For these types of chips, it is necessary to manage the power consumption tightly, optimizing the power consumption levels separately for each different active region.

33. The following figure shows a high-level construct of the basic structure of CMOS logic-gate.



MTK-1018 at 1059

34. Sedra states:

A CMOS logic circuit is in effect an extension, or a generalization, of the CMOS inverter: The inverter consists of an NMOS pull-down transistor, and a PMOS pull-up transistor, operated by the input voltage in a complementary fashion. The CMOS logic gate consists of two networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull-up network (PUN) constructed of PMOS transistors (see Fig. 13.8).

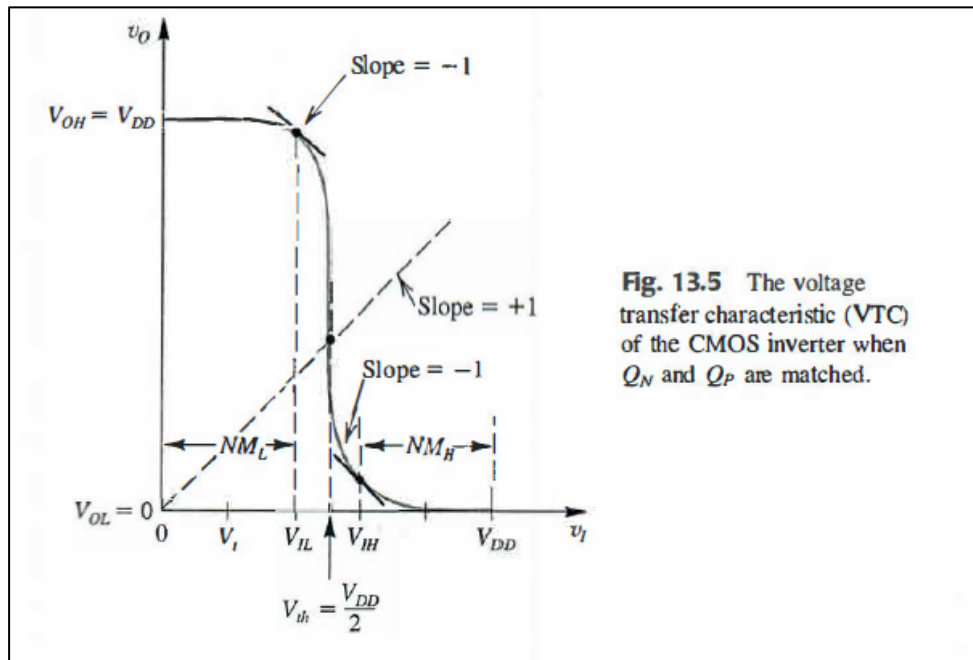
MTK-1018 at 1058. Sedra further states:

[F]or the three-input gate represented in Fig. 13.8, the PDN will conduct for all input combinations that require a low output ($Y = 0$) and will then pull the output node down to ground, causing a zero voltage to appear at the output, $v_y = 0$. Simultaneously, the PUN will be off, and no direct dc path will exist between V_{DD} and ground. On the other hand, all input combinations that call for a high output ($Y = 1$) will cause the PUN to conduct, and the PUN will then pull the output node up to V_{DD} , establishing an output

voltage $v_y = V_{DD}$. Simultaneously, the PDN will be cut off, and again, no dc current path between V_{DD} and ground will exist in the circuit.

Id. at 1058-59. In other words, at both at the low output state, i.e., $Y = 0$ and the high output state $Y = 1$, either the PUN or the PDN is turned off and there is no dc path between V_{DD} and ground exists in the circuit. As both the PDN and the PUN must conduct at the same time for the current to flow, there is no dc current flowing between V_{DD} and ground at both at the low output state, i.e., $Y = 0$ and the high output state $Y = 1$.

35. The following is a figure from Sedra showing the voltage transfer characteristics of a CMOS inverter:



MTK-1018 at 1051

The PMOS transistor (noted as Q_P in the figure above) corresponds to the PDN in Fig. 13.8 of Sedra and the NMOS transistor (noted as Q_N in the figure above) corresponds to the PDN in Fig. 13.8 of Sedra. v_O in the figure above corresponds to Y in Fig. 13.8 of Sedra. In this way, V_{OH} (output high) corresponds to $Y = 1$ and V_{OL} corresponds to $Y = 0$. As explained above, at $Y = 1$ and $Y = 0$, there is no current path through the PUN and the PDN. In order for the current to pass through the PUN and the PDN, both the PUN and the PDN must be on at the same time, which happens during the transition period from/to $Y = 1$ to/from $Y = 0$. The transition period correspond to the portion of the graph shown in the above figure when $v_I = V_{OL}$ and $v_I = V_{OL}$ along the horizontal axis when v_O transitions from/to V_{OH} to/from V_{OL} along the vertical axis. In digital design, this transition period is referred to as the switching time. Since the CMOS gates only consume power during the transition period, the power consumed by the CMOS gates are mostly dynamic in nature. MTK-1018 at 1056 (“The negligible static power dissipation of CMOS has been a significant factor in motivating its replacing NMOS as the technology of choice in implementing high-density VLSI circuits.”).

36. Sedra explains that: “The dynamic power dissipated in the CMOS inverter is given by Eq. (13.4), which we repeat here as $P_D = fCV_{DD}^2$ (13.20) where f is the frequency at which the gate is switched.” *Id.* Setting aside the various capacitance, C , associated with the CMOS gate, the power consumed by a CMOS

gate is proportional to the switching frequency f and to the square of the supplied voltage V_{DD} . Since digital circuits including the CMOS gates are clocked, the switching frequency f is related to the clocking frequency of the circuit. This is the reason why the management of the power is performed by changing the clock frequency and the supplied power level.

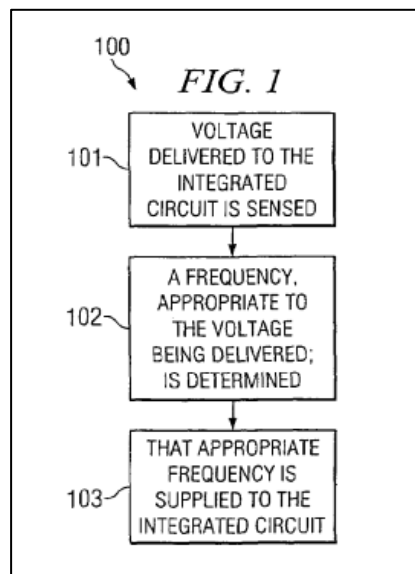
37. In addition to the level of power consumption based on the clock frequency and the voltage as explained by equation $P_D = fCV_{DD}^2$, there is yet another relationship between the clock frequency and the voltage, which is imp.

38. As Fig. 13.5 of Sedra shown above, the transition of output v_O from the high state (noted in the figure as V_{OH}) to the low state (noted in the figure as V_{OL}) or vice versa, is not instantaneous. This is shown that from/to $v_O = V_{OH}$ to/from $v_O = V_{OL}$ is not straight vertical line – rather there is a region between $v_I = V_{IL}$ and $v_I = V_{IH}$ along the input values, where the output voltage v_O transitions along a curve. This is because as the input v_I changes to cause the transition of the output v_O between V_{OL} and V_{OH} , due to certain unavoidable amount of capacitance and resistance in the circuitry, the output v_O cannot change instantly. This means that the difference between V_{OH} and V_{OL} , which is equal to the amount of the output voltage between the high output state and the low output state, impacts how fast the circuit can operate. As Fig. 13.5 of Sedra also shows, $V_{OH} = V_{DD}$, where V_{DD} is the supply voltage to the circuit. In other words, the supply voltage to the circuit, V_{DD} , affects

the frequency at which the CMOS gates can operate, i.e., f , the clock frequency of the circuit.

B. Overview of the '563 Patent

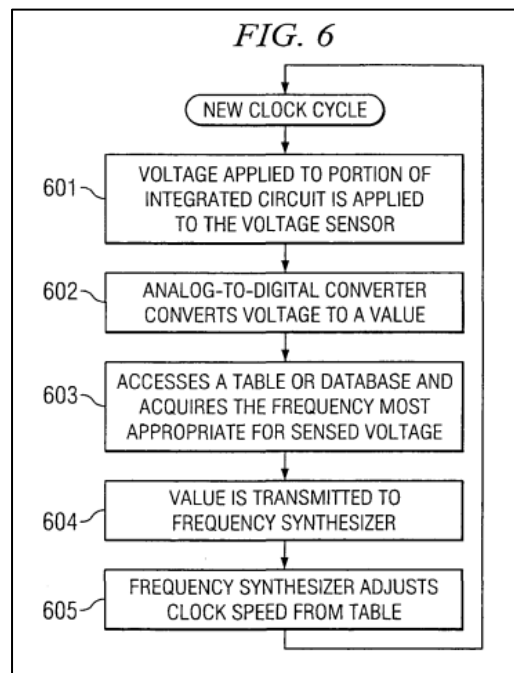
39. The '563 patent discloses a method and device for circuit control that comprises: (1) sensing a delivered voltage to a portion of an integrated circuit; (2) determining an appropriate frequency for the portion of the integrated circuit based on that sensed voltage; and (3) providing the appropriate frequency to the portion of the integrated circuit. MTK-1001, Abstract, 3:46-50, 4:22-24, 4:25-37, 4:43-52, claims 1, 23, and 35.



MTK-1001, FIG. 1

40. According to the '563 patent, “[v]oltage sensors ... provide a means of detecting the voltage actually delivered to an integrated circuit,” and “[i]t may be advantageous,” though not necessary, “to have a number of voltage sensors

distributed across an entire die.” MTK-1001, 4:9-17. “A frequency determining means is used to determine what [clock] frequency is appropriate for the integrated circuit (or a portion thereof) at the voltage delivered.” MTK-1001, 4:22-24. “Typically, this frequency is derived directly from the delivered voltage.” MTK-1001, 4:34-35. As illustrated in FIG. 6 below, the ’563 patent teaches that one way of doing this is to use “an analog to digital converter to ... measure the value of the delivered voltage,” MTK-1001, 5:49-51, “access ... a table or database that associates voltage values with appropriate frequencies,” and transmit the frequency associated with the delivered voltage “to a frequency synthesizer” to “adjust ... the clock frequency” accordingly, *id.* at 5:57-62; *see also id.* at claims 10-11 at 31-34.



MTK-1001, FIG. 6

C. Prosecution History of the ’563 Patent

41. On August 29, 2003, the Applicant filed U.S. Patent Application No. 10/651,360, which led to the issuance of the '563 patent and claimed priority to U.S. Provisional Patent Application No. 60/480,056, filed on June 20, 2003. MTK-1002, 41, 50.

42. On October 3, 2003, the Applicant amended the specification “to include reference to U.S. Provisional Patent Application No. 60/480,056” and amended claims 2, 8, 9, 15-18, 26, and 34 “to correct typographical errors.” MTK-1002, 46.

43. On August 8, 2006, the Examiner issued a Non-Final Office Action rejecting all of the then-pending claims (i.e., claims 1-32) “under 35 U.S.C. 102(b) as being anticipated by Tam et al (6,762,629) or Huard et al (6,885,233)” and “on the ground of nonstatutory obviousness-type double patenting ... over claims 1-6 of U.S. Patent No. 6,927,605.” MTK-1002, 25-29. With respect to the rejection under 35 U.S.C. 102, the Examiner stated:

Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Tam et al (6,762,629) or Huard et al (6,885,233).

Tam teaches a method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes. A clock frequency of a clock signal generator is adjusted in response to an evaluation of sampled values of the supply voltage.

The title of the Huard patent is “Altering Operating Frequency and Voltage Set Point of a Circuit in Response to the Operating Temperature and Instantaneous Operating Voltage of the Circuit.”

Id. at 27. With respect to the rejection for obviousness-type double patenting, the Examiner further stated:

Claims 1-32 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,927,605. Although the conflicting claims are not identical, they are not patentably distinct from each other because the above mentioned patent includes means for dynamically varying the frequency of a clock signal in response to observed (sensed) changes in the variable operating voltage. Differences between the two sets of claims are minor design variations were within the abilities of persons of ordinary skill in the art.

Id. at 28.

44. On November 13, 2006, the Applicant responded to the August 8, 2006 Office Action. MTK-1002, 16-23. With respect to the 102(b) rejections, the Applicant did not dispute that both Tam and Huard teach the method and device for circuit control embodied in then-pending claims 1-32. MTK-1002, 23. Instead, the Applicant argued only that, due to their respective dates of publication, “neither *Tam* nor *Huard* are prior art under 35 U.S.C. § 102(b)”:

The Current Action also rejects claims 1-32 as anticipated by Tam et., U.S. Patent No. 6,762,629 (hereinafter *Tam*)

or Huard et al., U.S. Patent No. 6,885,233 (hereinafter *Huard*). However, the Applicant respectfully points out that Tam was published on July 13, 2004 and Huard was published on August 9, 2005. Since the present application was filed on August 29, 2003, neither *Tam* nor *Huard* are prior art under 35 U.S.C. § 102(b). Therefore, the Applicant respectfully submits that no rejection under 35 U.S.C. § 102(b) currently exists for claims 1-35, and the Applicant respectfully asks the Examiner to pass this application to issue.

Id. Though I am not an attorney, and thus offer no opinion as to whether Tam and Huard qualify as prior art under 35 U.S.C. § 102(b), I have been informed that both Tam and Huard nonetheless qualify as prior art under 35 U.S.C. § 102(e). I understand, however, that the Examiner failed to analyze whether Tam and Huard anticipated then-pending claims 1-32 under 35 U.S.C. § 102(e). *See generally* MTK-1002. In my opinion, had the Examiner recognized that Tam and Huard remained prior art under 35 U.S.C. § 102(e) (even if the two references were not prior art under 35 U.S.C. § 102(b)), the Examiner would not have allowed the claims to issue for the reasons expressed in Sections VIII.A-B below.

45. With respect to the obviousness-type double patenting rejection, the Applicant argued that the August 8, 2006 Non-Final Office Action's rejection for obviousness-type double patenting fell "short of that which is required for making a *prima facie* rejection of obviousness":

The Current Action has rejected claims 1-32 as obvious in light of Fetzer et al., U.S. Patent No. 6,927,605 (hereinafter *Fetzer*), and contends that the present application is impermissible obvious-type double patenting. However, as M.P.E.P. § 804 states, the analysis of obvious-type double patenting is the same as the analysis required for obviousness under 35 U.S.C. § 103(a). Thus, the Examiner must at least make a *prima facie* showing that claims 1-32 are obvious in light of *Fetzer*. Specifically, “any obvious-type double patenting should make clear: A) the differences between the inventions defined by the conflicting aims — a claim in the patent compared to a claim in the application; and B) the reasons why a person of ordinary skill in the art would conclude that the invention defined in the claims at issue would have been an obvious variation of the invention defined in a claim in the patent.” M.P.E.P. §804B(1). The Applicant respectfully points out that, contrary to the contention of the Current Action, claims 1-32 of the present application contain substantially different limitations than those of *Fetzer*. The Current Action’s unsupported statement that these substantial differences are “minor design variations” falls far short of that which is required for making a *prima facie* rejection of obviousness. Therefore, the Applicant respectfully asks the Examiner to withdraw the obviousness-type double patenting rejection of claims 1-32.

Id. at 22-23 (italics in original). The Applicant’s argument against obviousness-type double patenting was longer, and more substantive, than its argument against the Examiner’s rejection under 35 U.S.C. § 102(b). *See id.*

46. Finally, in its November 13, 2006 response to the August 8, 2006 Non-Final Office Action, the Applicant also “amended claim 1 and 12 to more clearly describe the claimed subject matter,” and added claim 35. MTK-1002, 22. I reproduce the amendments to claims 1 and 12 below for ease of reference:

1. (Currently Amended) A method of circuit control, comprising:
sensing a delivered voltage to a portion of an integrated circuit;
determining an appropriate frequency for the portion of the integrated circuit; and
providing the appropriate frequency to the said portion of said integrated circuit.

Id. at 18.

12. (Currently Amended) A device for electronic circuit control comprising:
means for sensing a delivered voltage to [[a]] one portion of an integrated circuit;
means for determining an appropriate frequency for the portion of the integrated circuit; and
means of providing the appropriate frequency to the portion of the integrated circuit, independent of frequencies provided to other portions of said integrated circuit.

Id. at 19. With respect to claim 1, the Applicant merely clarified that the “appropriate frequency for the portion of the integrated circuit” is provided to “said portion of said integrated circuit.” *Id.* at 18. I understand that claim 12 is not being challenged in this IPR proceeding and thus I will refrain from characterizing it at this point in time.

47. On February 22, 2007, in response to Applicant’s November 13, 2006 remarks, claims 1-35 were allowed. *Id.* at 9-15.

48. On May 29, 2007, the '563 patent issued. *Id.* at 7.

D. Interpretations of the '563 Patent Claims at Issue

49. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to what is referred to as the “*Phillips*” standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. I further understand that the words of the claims should be given their plain meaning unless that meaning is inconsistent with the patent specification or the patent’s history of examination before the Patent Office. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the invention (not today). Without further information on what date the invention as claimed was made, I have used the earliest possible priority date of the '563 patent as the point in time for claim interpretation purposes. That date was June 20, 2003.

VII. OVERVIEW OF CONCLUSIONS FORMED

50. I have reviewed the Petition for IPR of the '563 patent, and agree with the analysis contained therein. In summary, it is my opinion that each and every limitation of each and every challenged claim would have been at least obvious to one of ordinary skill in the art at the time of the alleged invention in view of the prior art cited in the Petition and further explained in this declaration. To summarize my conclusions below:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-10, 23-24, 31-32, and 35 of the '563 patent are rendered obvious by Tam alone.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-11, 23-24, and 31-35 of the '563 patent are rendered obvious by Tam in view of Huard.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-11, 23-24, and 31-35 of the '563 patent are rendered obvious by Norman '259 in view of Norman '851.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1, 3, 10, 23, 24, 31, 32, and 35 of the '563 patent are rendered obvious by Naffziger '788 alone.

VIII. ANALYSIS OF THE PRIOR ART

A. Analysis of Tam with respect to Claims 1-10, 23-24, 31, 32, and 35

51. For the reasons articulated in detail below, and based on my review of the '563 patent and the Tam reference, I am confident that a POSITA would have readily understood that Tam renders obvious all elements of claims 1-10, 23-24, 31-32, and 35.

1. Overview of Tam

52. Tam relates to “[a] method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes”:

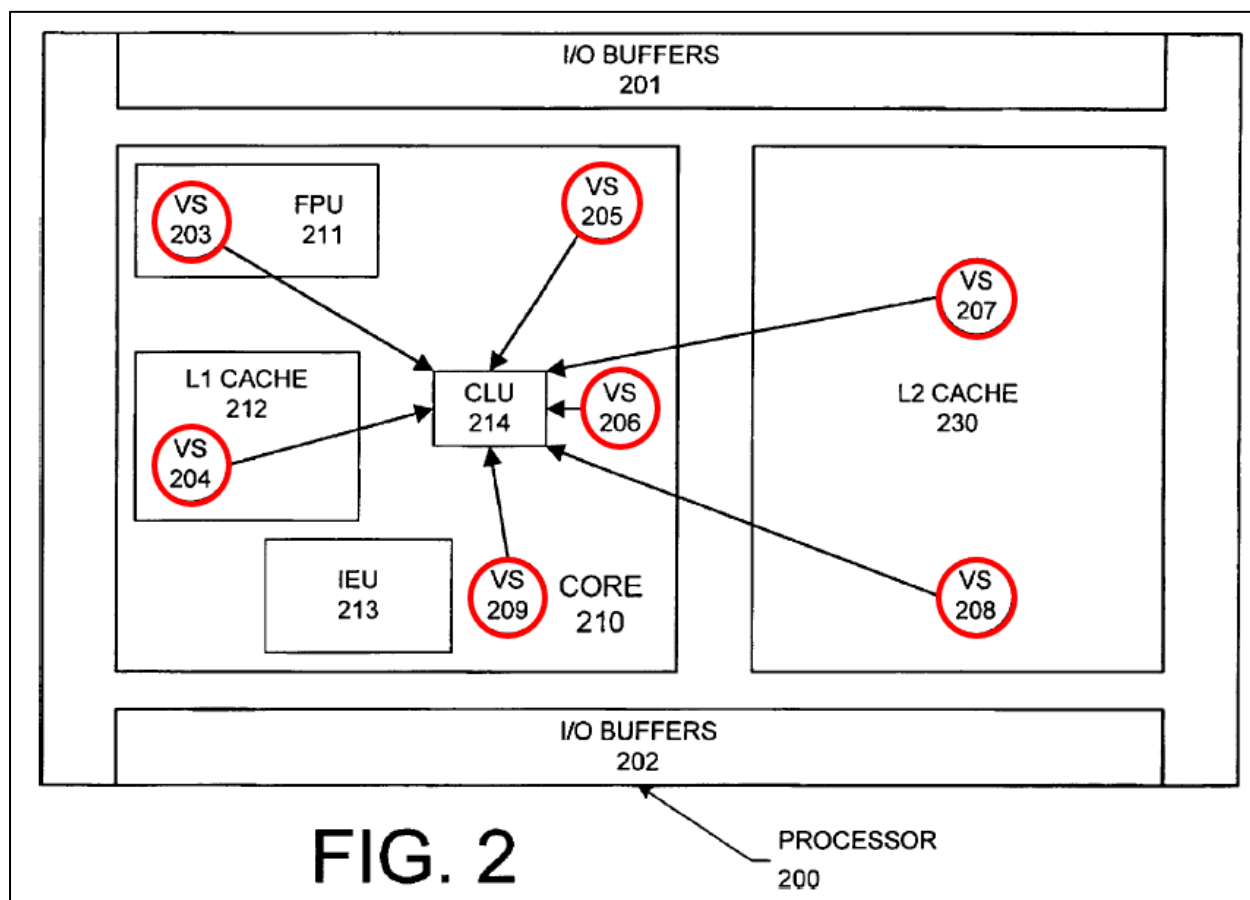
A method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes. The method of one embodiment includes sampling a supply voltage at a plurality of locations. The values of said supply voltage are communicated to a clock generator. A clock frequency of a clock signal generated from the clock generator is adjusted in response to an evaluation of the sampled values of the supply voltage.

MTK-1004, Abstract. Specifically, Tam discloses “voltage sensors” that “can be strategically placed at various” portions of an integrated circuit, to sense delivered “VCC supply voltages” and “get an accurate and useful view of the power environment.” MTK-1004, 5:46-53 (e.g., “high voltage circuitry, critical circuits, power bussing, and high speed logic”), 5:62-65 (“For this embodiment, a network of voltage sensors 202, 204, 205, 206, 207, 208, 209, are distributed in the core 210 and L2 cache 230 to get an accurate and useful view of the power environment.”).

53. FIGS. 2 and 3 of Tam generally depict a “block diagram of a processor ... in accordance with the present invention.” MTK-1004, 5:46-48 (“FIG. 2 is a block diagram of a processor that includes on-die voltage sensors and adaptively variable clock generator in accordance with the present invention.”); *id.* at 6:33-36 (“FIG. 3 is a block diagram of a processor architecture having a mechanism for

dynamically adjusting a clock frequency in order to adapt to varying supply voltages in accordance with the present invention.”). Because Tam notes that “like references” (including in FIGS. 2-3), such as “processor,” “core,” “sensors,” clock generator, etc., “indicate similar elements” across the figures, neither FIG. 2 nor FIG. 3 appears to be limited to any specific embodiment. *Id.* at 1:64-66.

54. In the processor illustrated in FIG. 2 below, which “includes on-die voltage sensors and [an] adaptively variable clock generator,” “a network of voltage sensors [203, 204, 205, 206, 209] are distributed in the [processor] core,” i.e., a portion of the integrated circuit. MTK-1004, 2:5-7, 5:62-63.



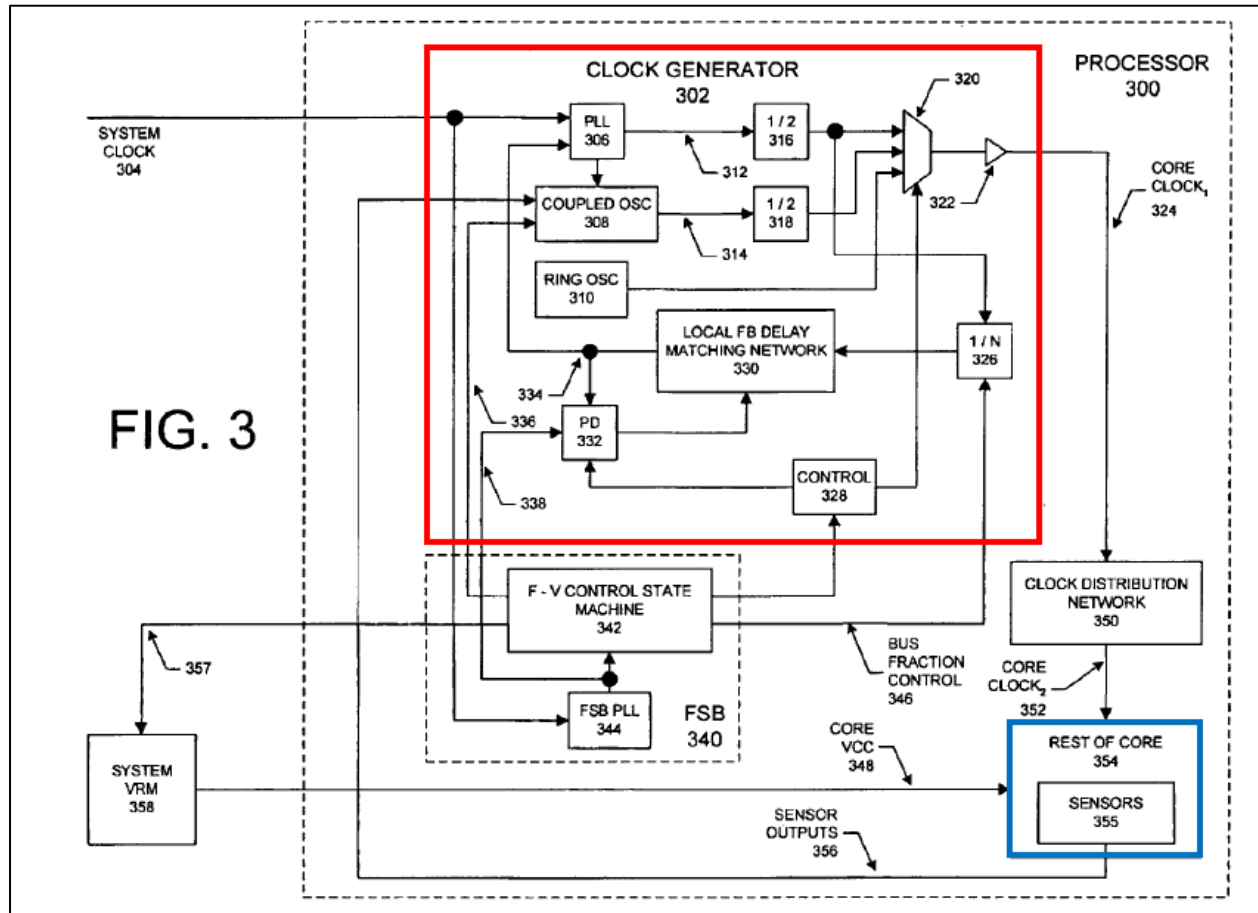
MTK-1004, FIG. 2¹

“These sensors,” which are circled in red above, “are to detect the local VCC voltage levels and to communicate that information back to the clock generator[.]” MTK-1004, 6:7-9. “Logic in the clock generator 214 monitors the voltage statuses and can dynamically adapt and adjust the clock frequency based on the sensed information.” *Id.* at 6:9-12. “[W]hen a droop is detected, the clock is slowed down to accommodate the reduced voltage level. Similarly, when the voltage recovery is detected, the clock frequency can be increased to enhance performance.” *Id.* at 3:47-50; *id.* at 6:19-23 (“Thus if VCC droop transients arises, the clock generator can detect the voltage decrease based on data from the on-die voltage sensors and react by reducing the operating frequency in order to avoid any circuit timing failures or computation errors.”). By “dynamically adjusting the clock frequency based on sensed on-die voltage changes,” the “control technique” “provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.” *Id.* at 3:44-4:5.

55. In the block diagram of a processor illustrated in FIG. 3 below, “[t]he clock generator 302,” shown in red, “is a VCC adaptive dynamically variable frequency clock system capable of varying the frequency of its clock output” to the

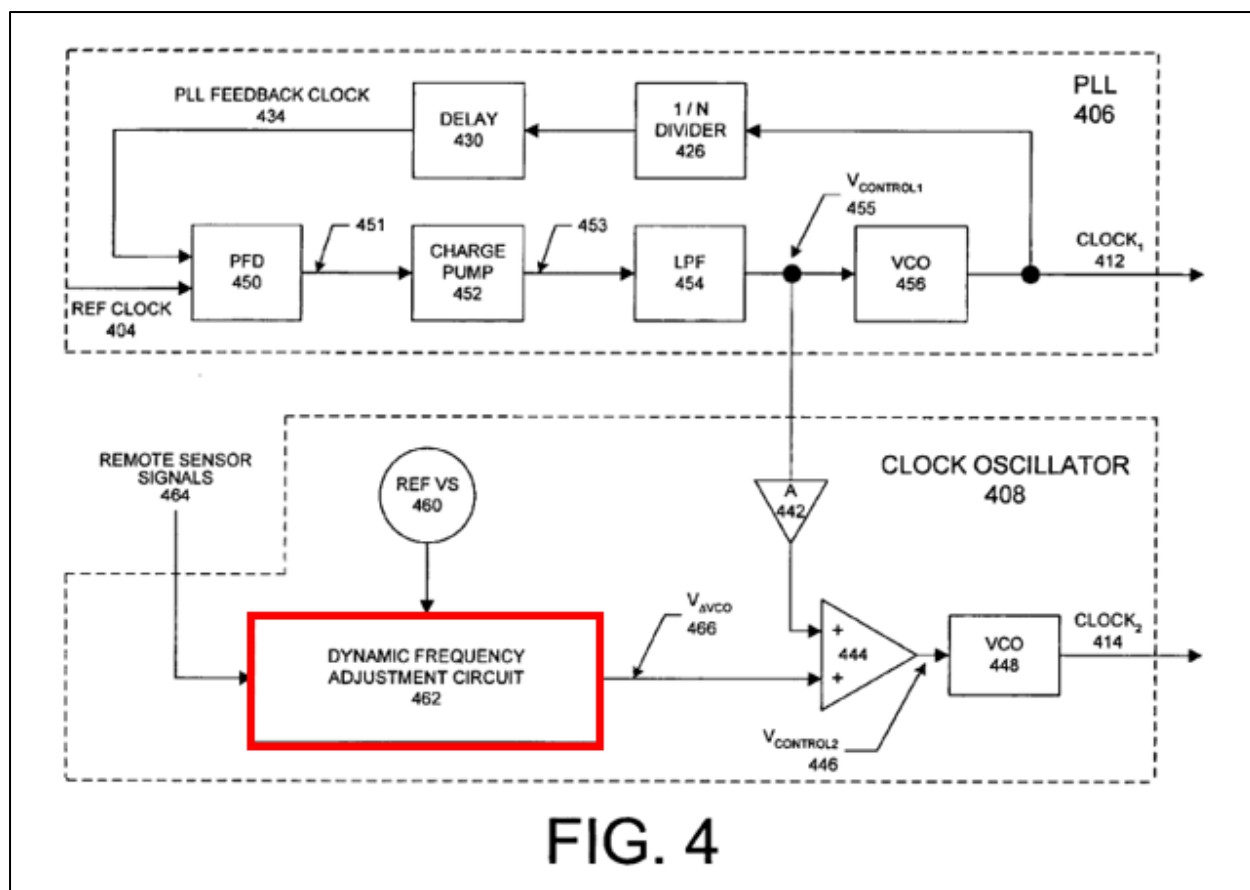
¹ Annotations and color added unless otherwise noted.

processor core, shown in blue, “in response to voltage sensors 355,” *id.* at 6:38-44, which are “distributed around the processor die,” *id.* at 7:39-41, as in FIG. 2.



MTK-1004, FIG. 3

56. Next, FIG. 4 depicts “a block diagram of a clock generator structure,” such as the clock generator 302 shown in FIG. 3 above, “incorporating a dynamic frequency adjustment feature of one embodiment,” which I have shown in red below MTK-1004, 2:12-14:



MTK-1004, FIG. 4

A POSITA would understand that the “PLL” 406 and “clock oscillator” 408 depicted in FIG. 4 correspond to the “PLL” 306 and “coupled OSC” 308 depicted in FIG. 3, respectively. See MTK-1004, 1:65-66 (“like references indicate similar elements”), 6:46-49 (“The clock generator 302 comprises a phase locked loop (PLL) clock generator 306, coupled oscillator clock generator 308, a ring oscillator 310, and a local feedback delay matching network 330.”). For example, FIG. 3 includes a “coupled oscillator” 308, and Tam expressly discloses that the clock oscillator 408 shown in FIG. 4 is a “coupled oscillator structure.” *Id.* at 7:56.

Thus, a POSITA would have understood that the coupled oscillator 308, which is part of the clock generator 302 shown in FIG. 3, includes a “dynamic frequency adjustment circuit,” as shown in red in FIG. 4 above, to “allow for the dynamic adjustment of the core frequency in order to reduce the effects of voltage droop transients.” *Id.* at 7:34-36; *id.* at 8:37-40 (“Upon receipt of the sensor data, the dynamic frequency adjustment circuit 462 can evaluate the supply voltage conditions and dynamically adapt the clock oscillator output 414 appropriately.”).

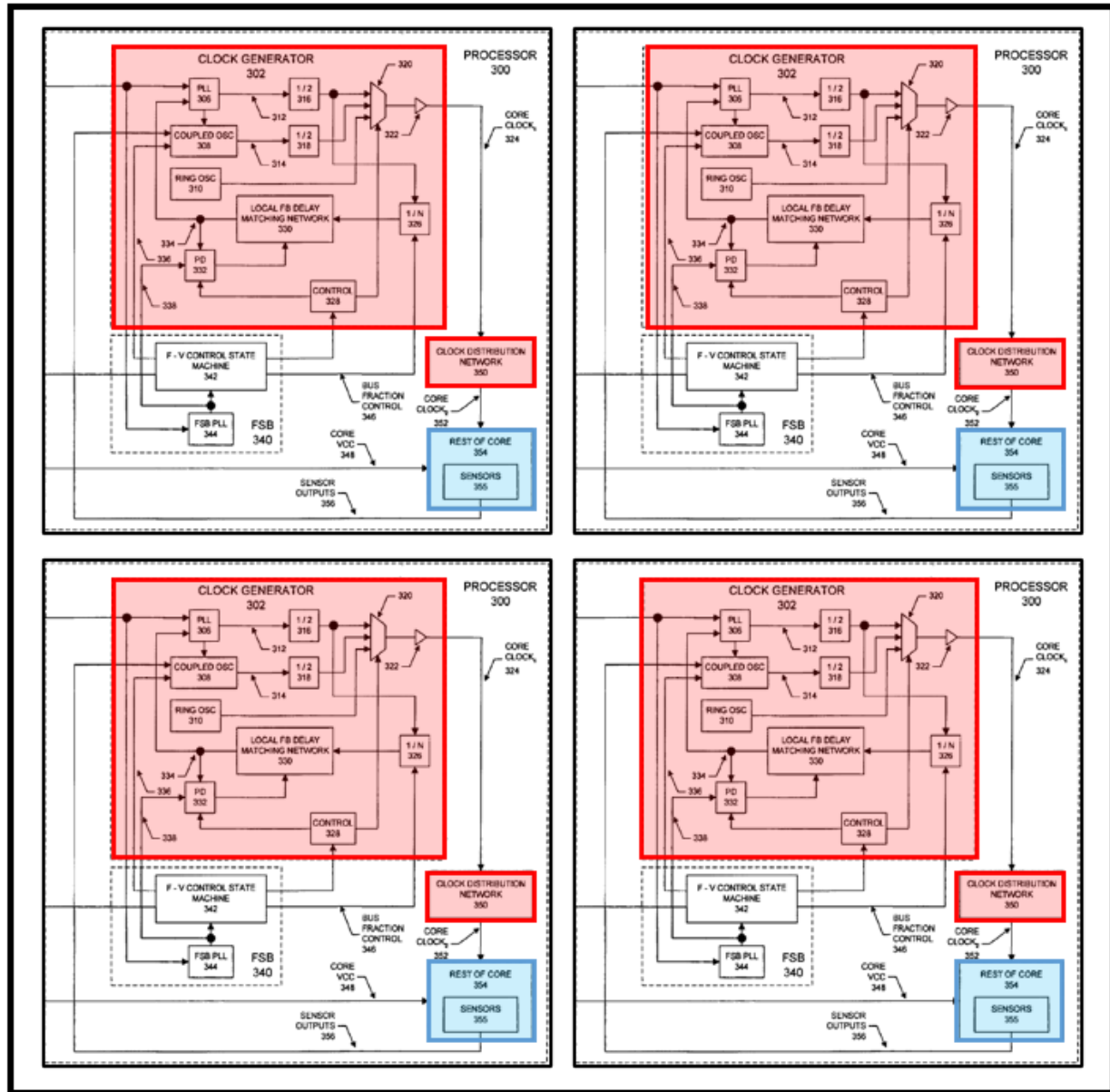
57. Though the figures depict single processor systems, Tam’s teachings are applicable to both single-processor and multiprocessor systems:

The examples above have been described in the context of a single processor. In a multiprocessor system, the method can be performed concurrently in each processor. Each processor can contain an adaptive variable frequency clock system. For example, each processor can be adjusting its own frequency and voltage settings independent of the other processors in the system.

MTK-1004, 13:12-18. Indeed, Tam expressly teaches that, “[i]n a multiprocessor system,” its circuit control “method can be performed concurrently in each processor,” wherein “[e]ach processor can contain an adaptive variable frequency clock system,” including a clock generator and a clock distribution network, shown in red below, that can (1) adjust “its own frequency and voltage settings independent of the other processors in the system,” and (2) provide an updated

clock frequency to each processors' core, shown in blue below, in response to voltage variations sensed by voltage sensors located within the cores. *Id.*

Multiprocessor Circuit

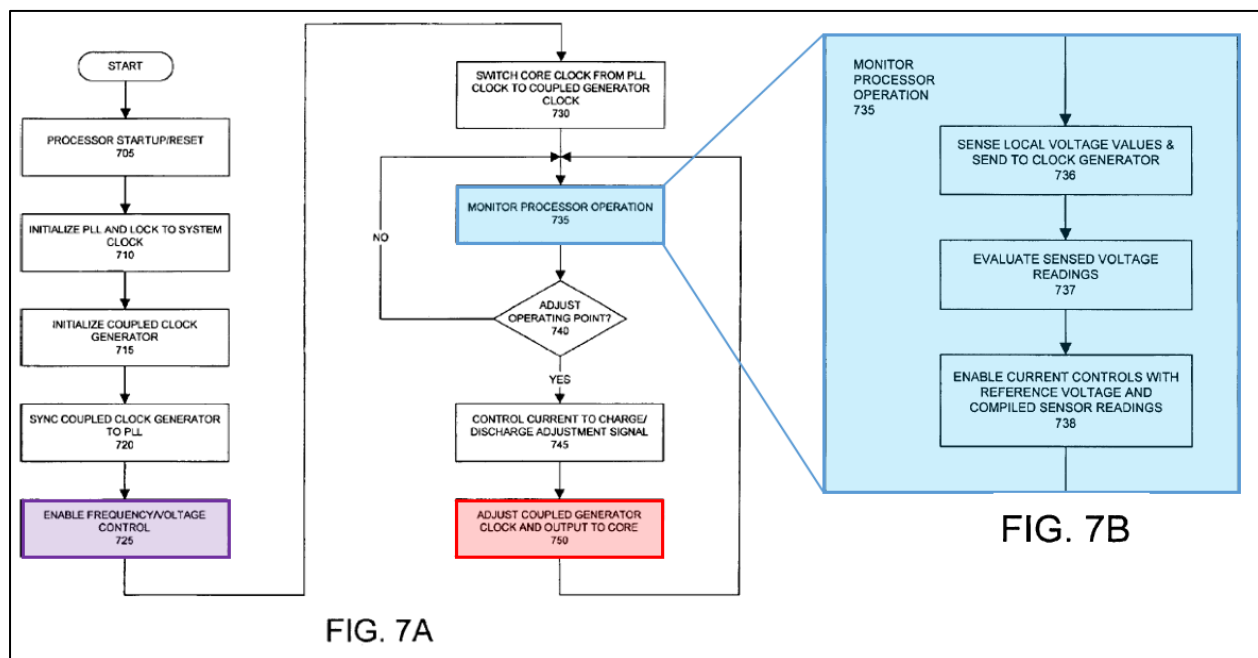


MTK-1004, FIG. 3 (annotated to show processor in multiprocessor system)

2. Claim 1

(a) Element 1[p]

58. The preamble of claim 1 recites: “[a] method of circuit control.” Tam provides the preamble of claim 1. *Infra* 1[a]-1[c]; MTK-1004, Abstract (“A method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes.”), 2:30-40 (same), 3:67-4:5, claim 8 (“A method...”), 12:4-7. Indeed, Tam discloses a circuit “control technique” that “implements on-die voltage sensing” to “detect voltage fluctuations and reduce the operating frequency as needed to match the detected VCC voltage decrease.” MTK-1004, 3:67-4:5. An embodiment of this circuit control method is depicted in FIGS. 7A-B² below:



MTK-1004, FIGS. 7A-B

² According to Tam, “FIGS. 7A-B are flow charts showing one embodiment of a method in accordance with the present invention for dynamically varying clock frequencies in response to voltage variations.” MTK-1004, 12:4-7.

At step 725 (shown in purple above), “[t]he frequency/voltage control logic is enabled. MTK-1004, 12:24-25. At step 735 (shown in blue above), “the processor operation is monitored,” where the monitoring includes “sens[ing] the local voltage values and send[ing] the data to the clock generator,” “evaluat[ing] the sensed voltage readings,” and enabling “[t]he current control blocks that can shift the adjustment signal.” MTK-1004, 12:33-47. Finally, at step 750 (shown in red above), “the new frequency setting takes effect,” and the “clock signal is adjusted and is outputted to the processor core.” MTK-1004, 13:6-9.

(b) Element 1[a]

59. Claim element 1[a] recites: “sensing a delivered voltage to a portion of an integrated circuit.” Tam provides claim element 1[a]. MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 11:24-28, 12:14-11, 12:30-64, FIGS. 1-7B, claims 1-30. For example, Tam discloses a circuit “control technique” that includes “on-die voltage sensing” using “sensors [that] can detect voltage fluctuations[.]” MTK-1004, 3:67-4:5; *id.* at 3:44-46 (“Embodiments of the present invention adapt the clock signal to voltage droops and fluctuations by dynamically adjusting the clock frequency based on sensed on-die voltage changes.”).

60. Tam expressly teaches that its “on-die voltage sensors ... can be strategically placed at various locations” on an integrated circuit, i.e., various

portions of an integrated circuit, to detect/sense the available supply voltages for those portions of the integrated circuit:

FIG. 2 is a block diagram of a processor that includes on-die voltage sensors and adaptively variable clock generator in accordance with the present invention. Embodiments of the present invention incorporate one voltage sensors to monitor the on-die VCC supply voltages. **These sensors can be strategically placed at various locations** such as high voltage circuitry, critical circuits, power bussing, and high speed logic, for example.

MTK-1004, 5:46-53.³

For this embodiment, **a network of voltage sensors 202, 204, 205, 206, 207, 208, 209, are distributed in the core 210 and L2 cache 230** to get an accurate and useful view of the power environment. In other embodiments, the number of sensors can vary widely depending on the particular implementation. Similarly, the placement of these sensors are designer/application specific. In FIG. 2, the sensor 206 closest to the clock generator is a reference sensor to detect a baseline VCC voltage level. **Two sensors 207, 208, are located in the L2 cache 230. Other sensors 203, 204, 209, are located with or around the FPU 211, L1 cache 212, and IEU 213, respectively, to sense the supply voltages in those regions.** These sensors 203, 204, 205, 206, 207, 208, 209, are to detect the local VCC voltage levels and to communicate that information back to the clock generator 214. Logic in the clock generator 214 monitors the voltage statuses and can dynamically adapt and adjust the clock frequency based on the sensed information. For example, **a local sensor in**

³ Emphasis added throughout unless otherwise noted.

a high activity area such as the FPU can better indicate the existence of a critical low voltage condition in that circuitry and inform the clock generator of a need to lower the operating frequency.

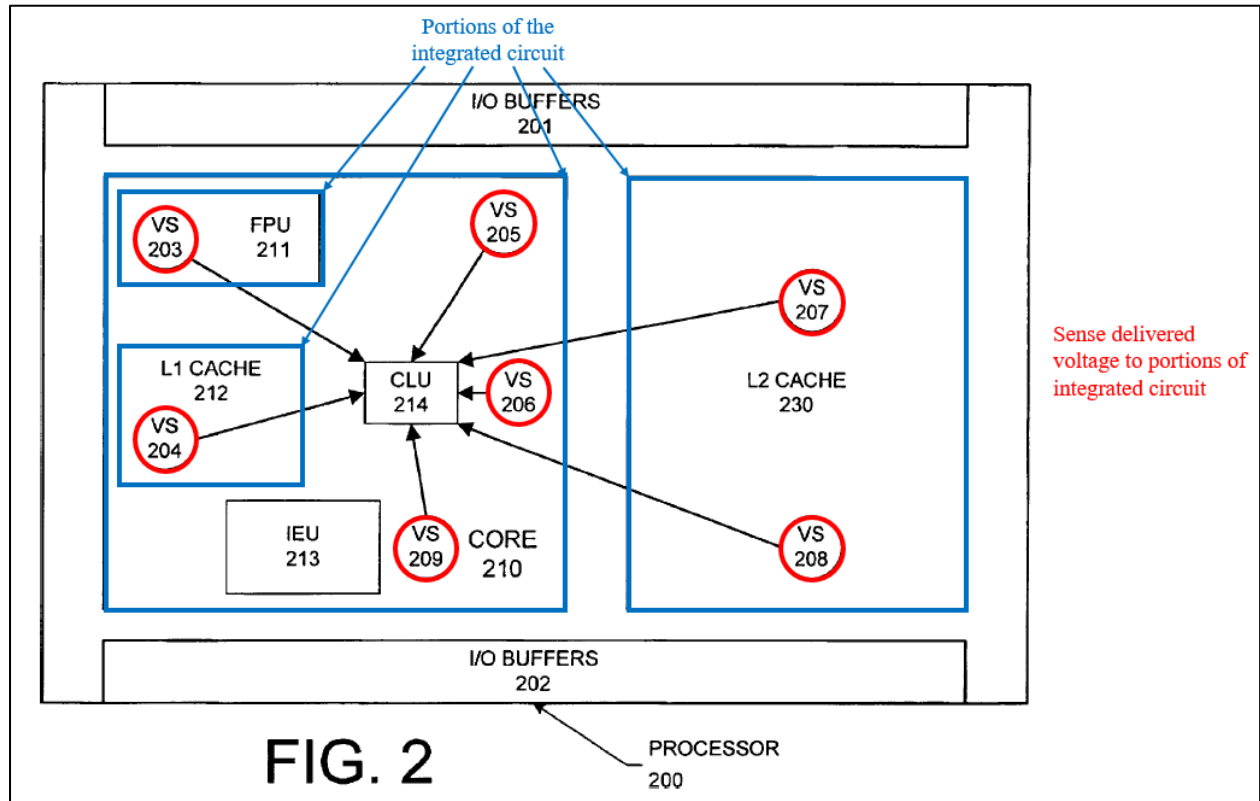
Id. at 5:62-6:16.

The clock generation system of the present embodiment uses **voltage sensors 355 distributed around the processor die**. The sensors communicate voltage information to the clock generator 302. Upon receipt of the voltage information, the clock circuitry 302 can evaluate the data and respond accordingly. If any of the sensors indicated that any voltage droops or transients exist, the clock signal can be adjusted to avoid performance errors and to maintain consistent power draw. Thus the processor core 354 can continue to operate despite non-optimal voltage conditions at certain locations on the die.

Id. at 7:39-50.

The **local reference voltage sensor 460 is to sense supply voltages in the circuitry in and around the clock generator 408**. Because the local voltage sensor 460 is proximate to the clock generator 408 in this embodiment, its output is used as the reference value of the VCC supply voltage. Similarly, **a number of voltage sensors are distributed over the integrated circuit to provide supply voltage readings from other circuit locations**. These sensors are to detect the voltage of the supply available to the surrounding circuitry and to communicate the voltage values to the clock generator 408.

Id. at 8:27-36; *see also id.* at 14:43 (“sampling a supply voltage at a plurality of locations”), Abstract, FIG. 7B. Such voltage sensors are depicted in FIG. 2 below:



MTK-1004, FIG. 2

61. While Tam teaches that “the number of sensors can vary” and that the “sensors are designer/application specific,” MTK-1004, 5:65-6:1 (“the number of sensors can vary widely depending on the particular implementation”), a POSITA would have recognized that each of Tam’s “on-die voltage sensors” is sensing a delivered voltage to a portion of an integrated circuit, whether it be the “FPU,” “L1 Cache,” processor “core,” or “L2 Cache.” *See* MTK-1004, FIG. 2, 6:3-9. In my opinion, a POSITA would have found it obvious to utilize a plurality of voltage

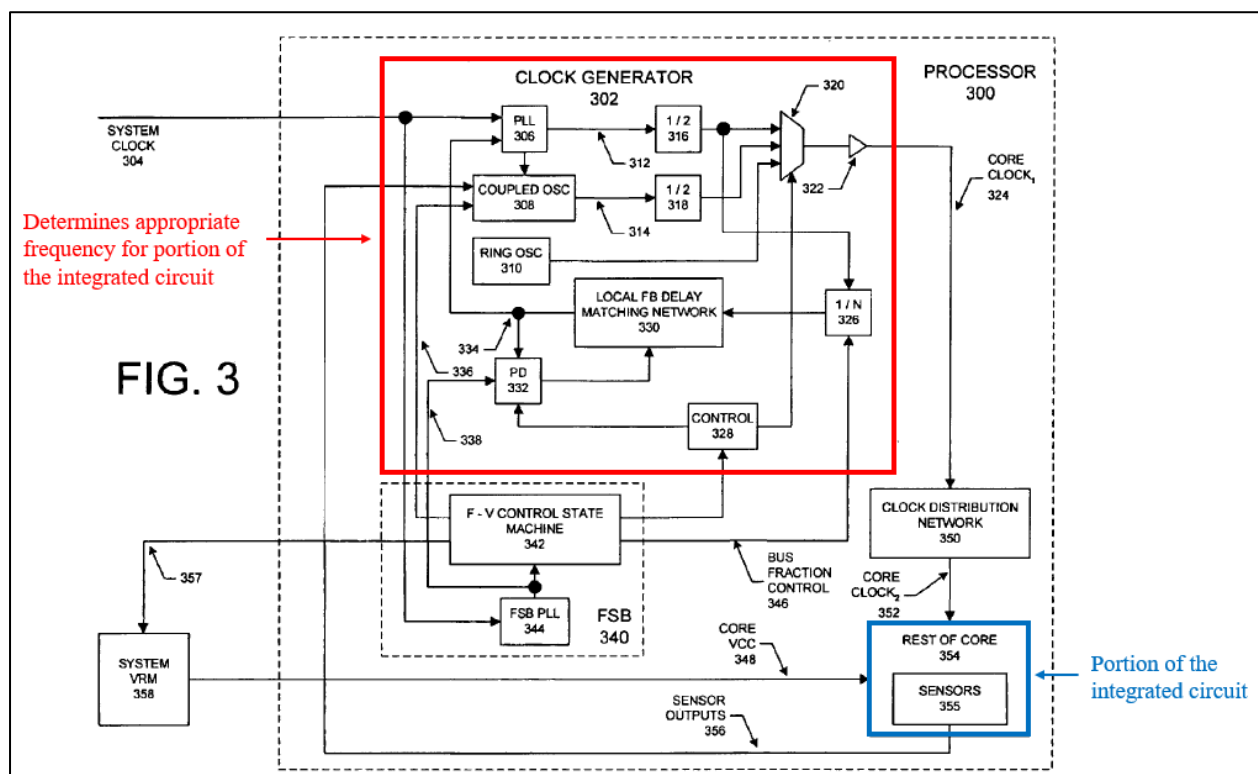
sensors, as in Tam, to “determine how the supply voltage is distributed across the processor,” *id.* at 12:38-39, because, as noted by Tam, doing so provides “an accurate and useful view of the power environment,” *id.* at 5:62-65.

(c) Element 1[b]

62. Claim element 1[b] recites: “determining an appropriate frequency for the portion of the integrated circuit.” Tam provides claim element 1[b]. MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 12:4-11, 12:30-64, FIGS. 1-7B, claims 1-30. Specifically, Tam teaches “[a] method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes.” MTK-1004, Abstract; *id.* at 2:30-40 (“A method and apparatus for a VCC adaptive dynamically variable frequency clock system is disclosed.”). After receiving data from voltage sensors associated with a portion of the integrated circuit, such as a processor core where multiple voltage sensors may be distributed, *id.* at 5:62-63 (“a network of voltage sensors . . . are distributed in the core”), Tam discloses that “the dynamic frequency adjustment circuit” located within the clock generator can “evaluate the supply voltage conditions and dynamically adapt the clock oscillator output,” i.e., the clock signal/frequency, “**appropriately.**” MTK-1004, 8:37-40; *id.* at 6:33-45 (“The clock generator” “is a VCC adaptive dynamically variable frequency clock system capable of varying the frequency of its clock output in response to voltage sensors[.]”); 7:34-

35 (“[T]he present invention can allow for the dynamic adjustment of the core frequency[.]”). A POSITA would have understood that dynamically varying a clock frequency, as in Tam, necessarily involves determining a new clock frequency.

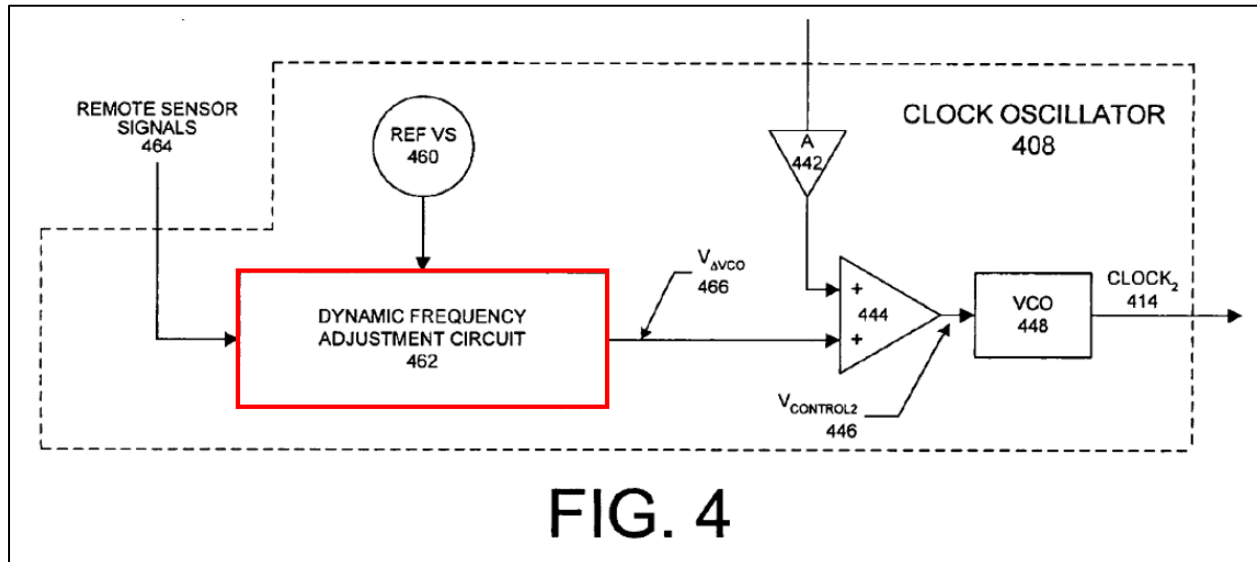
63. Tam FIG. 3 (below) depicts the clock generator 302 determining and providing an “appropriate frequency,” “CORE CLOCK,” to the processor core 354, representing a portion of the integrated circuit, via a clock distribution network 350:



MTK-1004, FIG. 3

As previously discussed, in my opinion, a POSITA would have understood that the clock generator 302’s coupled oscillator 308, which is shown in FIG. 3 above, includes a “dynamic frequency adjustment circuit,” as shown in red in FIG. 4

below, to “allow for the dynamic adjustment of the core frequency in order to reduce the effects of voltage droop transients.” *Id.* at 7:34-36.



MTK-1004, FIG. 4

Specifically, the dynamic frequency adjustment circuit, located within the clock generator’s coupled oscillator structure, determines the appropriate frequency after evaluating the current supply voltage conditions. *Id.* at 8:37-40. “[W]hen a [voltage] droop is detected” by a voltage sensor located at a portion of the integrated circuit, e.g., within the processor core, “the clock is slowed down to accommodate the reduced voltage level... [W]hen the voltage recovery is detected, the clock frequency can be increased to enhance performance.” MTK-1004, 3:44-50; *see also id.* at 6:19-23 (“Thus if VCC droop transients arises, the clock generator can detect the voltage decrease based on data from the on-die voltage

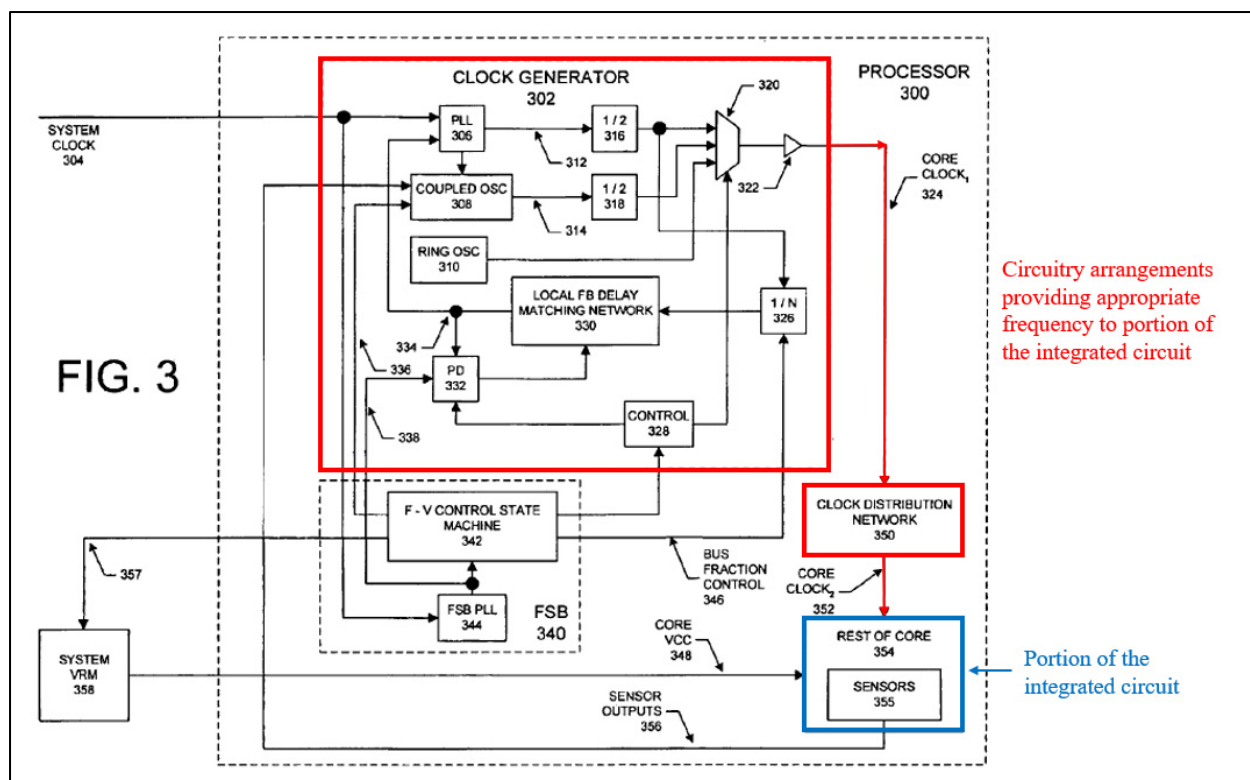
sensors and react by reducing the operating frequency in order to avoid any circuit timing failures or computation errors.”).

64. To the extent it is determined that Tam does not disclose determining an appropriate frequency for a specific portion of the integrated circuit, it is my opinion that it would have nevertheless been obvious to a POSITA to determine an appropriate frequency for a portion of the integrated circuit. For example, it would have been obvious to a POSITA, based on Tam, that “a local sensor in a high activity area such as the FPU [located in the processor core] can better indicate the existence of a critical low voltage condition in that circuitry and inform the clock generator of a need to lower the operating frequency” for that portion of the integrated circuit. MTK-1004, 6:12-16. Indeed, a POSITA would have recognized that doing so would “provide[] an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.” *Id.* at 3:51-54. In my opinion, a POSITA would have also understood, based on Tam’s disclosures, that this allows the integrated circuit to “avoid performance errors, “maintain consistent power draw,” and “continue to operate despite non-optimal voltage conditions at certain locations on the die.” MTK-1004, 7:45-50.

(d) Element 1[c]

65. Claim element 1[c] recites: “providing the appropriate frequency to said portion of said integrated circuit.” Tam provides claim element 1[c] for at least

the reasons discussed in the analysis of claim element 1[b] for Tam above. *See also* MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 12:4-11, 12:30-64, FIGS. 1-7B, claims 1-30. Moreover, Tam expressly teaches that its “[c]lock generator 302 is to **provide** an internal processor clock signal,” i.e., a clock frequency, to “the processor core 354,” i.e., said portion of said integrated circuit, “via a clock distribution network 350.” MTK-1004, 6:41-44. It would have been obvious to a POSITA both that Tam’s clock frequency, which is dynamically adjusted by the clock generator 302 in response to voltage variations at a portion of the integrated circuit, e.g., processor core 354, is an “appropriate frequency for the portion of the integrated circuit,” MTK-1004, 8:37-40, and is provided to that portion of the circuit via the clock distribution network 350, as depicted in FIG. 3 below:



MTK-1004, FIG. 3

3. Claim 2

66. Claim 2 recites: “[t]he method of claim 1 wherein said sensing, determining, and providing are continuously repeated during the integrated circuit’s operation.” Tam provides claim 2. *Supra* 1[a]-1[c]; MTK-1004, 11:24-28, 12:50-13:11. For example, Tam discloses, in one embodiment, that after sensing a delivered voltage, determining an appropriate frequency, and providing that frequency, MTK-1004, 12:4-13:9, the “frequency adjustment mechanism continues to monitor the processor and evaluates the sensors for further changes,” MTK-1004, 13:9-11. In additional embodiments, Tam specifically discloses that such “sensor outputs are sampled every 50 or 100 clock pulses,” or “sampled **continuously**”:

For one embodiment, the sensor outputs are sampled every 50 or 100 clock pulses. In another embodiment, the output can be sampled continuously or less often depending on the particular implementation and the desired response speed.

MTK-1004, 11:24-28. In my opinion, it would have been obvious to a POSITA to have Tam's frequency adjustment mechanism continue to monitor the processor and evaluate the voltage sensors for further changes by continuously sampling the sensor outputs, and a POSITA would have been motivated to do so, based on Tam, so that the frequency is able to "gradually follow the voltage changes" without having to make "large adjustments to catch up with big voltage steps." MTK-1004, 11:46-51. A POSITA would have also understood, based on Tam, that how often the voltage sensor outputs are sampled is simply a design choice "depending on the particular implementation and the desired response speed." *Id.* at 11:26-28.

4. Claim 3

67. Claim 3 recites: "[t]he method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage." Tam provides claim 3. For example, in my opinion, it would have been obvious to a POSITA, as evidenced by both Tam and applicant admitted prior art ("AAPA"), to have the appropriate frequency be the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

68. As an initial matter, Tam correctly discloses that “[a] high clock frequency is one of the principal performance drivers for a high performance microprocessor design.” MTK-1004, 1:27-29, *id.* at 1:29-30 (“One common method for achieving higher performance is to increase the processor operating frequency.”). Thus, in my opinion, a POSITA would have readily understood that utilizing the maximum frequency supported by the delivered voltage would be highly beneficial to a system’s performance. This is supported by Tam’s own disclosures, which suggests tracking the frequency with the voltage in a tight manner to alter performance intelligently and prevent circuit failure. *See, e.g.*, MTK-1004, 3:51-54 (“Thus a mechanism in accordance with the present invention provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.”), 11:46-47 (“this embodiment tracks the frequency with the voltage in a tight manner”), 11:66-12:2 (“determine the highest frequency ... possible to prevent circuit failure”).

69. A POSITA would have also recognized that Tam’s disclosures, including those discussed in the preceding paragraph, are commensurate with AAPA from the ’563 patent. For example, the ’563 patent admits that, as of the time of the alleged invention, “a designer,” i.e., a POSITA, “will typically specify the maximum frequency at which a part can operate for a given voltage.” MTK-1001, 1:24-27. A “designer,” or POSITA, would have typically done this because—as disclosed in

Tam—they would have recognized that having the frequency remain close to the maximum frequency supported by the voltage increases system efficiency. Moreover, as I have explained in the Background of Technology section above, a POSITA would have known that the voltage levels, e.g., V_{OL} and V_{OH} used for the circuitry in Fig. 13.5 of Sedra, place limits as to how fast the clock frequency for the circuitry can be. As I have noted, Sedra is a widely used textbook for the undergraduate curriculum in Electrical Engineering.

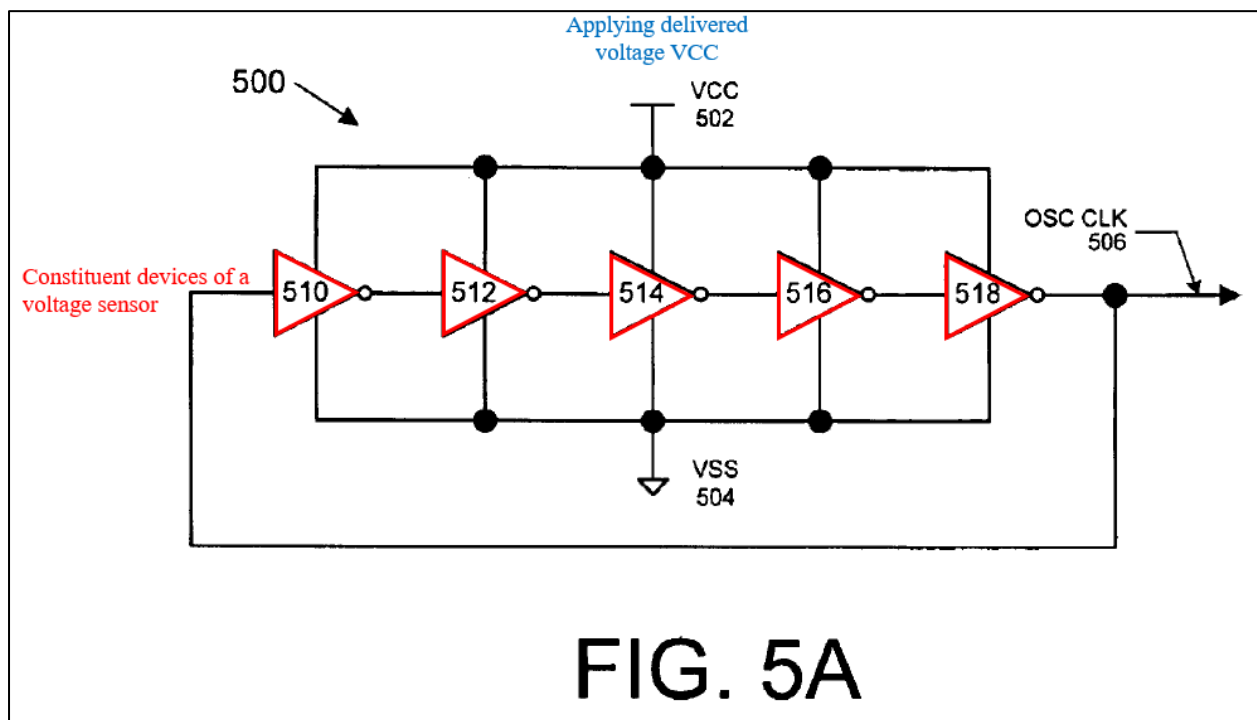
5. Claim 4

70. Claim 4 recites: “[t]he method of claim 1 further comprising: applying the delivered voltage to constituent devices of a voltage sensor.” Tam provides claim 4. *Supra* 1[a]-1[c]. For example, in FIG. 5A, Tam discloses one embodiment of a “voltage sensor” in the form of “ring oscillator 500,” which communicates an analog clock signal OSC CLK 502, reflecting the VCC supply voltage in and around the ring oscillator location, to the clock logic and clock generator:

FIG. 5A is a one embodiment of a ring oscillator 500 for a voltage sensor transducer. The ring oscillator 500 of this embodiment comprises of five inverters 510, 512, 514, 516, 518, connected together in series as a closed loop. These inverters 510, 512, 514, 516, 518, are coupled to a ground potential VSS 504 and a supply voltage VCC 502. The ring oscillator 500 provides an analog clock signal OSC CLK 506. The output frequency of a ring oscillator 500 is a monotonic function of the local power supply voltage, i.e. frequency $\propto$ VCC. The ring oscillator output 506 can be sent back to the clock generator where its

oscillation frequency embodies the local VCC 502. **The ring oscillator 500 can function as a voltage sensor by communicating OSC CLK 506 to the clock logic and clock generator, as OSC CLK 506 reflects the VCC supply voltage in and around the ring oscillator location.**

MTK-1004, 9:22-37. According to Tam, ring oscillator 500, i.e., an embodiment of a voltage sensor, comprises “five inverters [510,] 512, 514, 516, 518,” shown in red below, which a POSITA would recognize are constituent devices of the voltage sensor/ring oscillator 500. *Id.*



MTK-1004, FIG. 5A

According to Tam, the inverters depicted in FIG. 5A above, i.e., the constituent devices of a voltage sensor, are “connected together in series as a closed loop” and

“are coupled to ... a supply voltage VCC,” i.e., a delivered supply voltage.” MTK-1004, 9:24-26. Thus, a POSITA would have understood that the delivered voltage VCC 502 in FIG. 5A is being applied to constituent devices of voltage sensor 500, including inverters 510, 512, 514, 516, and 518.

6. Claim 5

71. Claim 5 recites: “[t]he method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.” Tam provides claim 5. *Supra* 1[a]-1[c] and claim 4. For example, as noted in the ’563 patent, constituent devices of the voltage sensor would be similar to the devices comprising the portion of the integrated circuit if they have similar timing elements, including “length and propagation time delay[s],” as the underlying circuit. *See* MTK-1001, 5:26-31. In my opinion, a POSITA would have recognized that, like the ’563 patent, Tam discloses that a voltage sensor, e.g., the ring oscillator discussed above with respect to claim 4, can incorporate “‘known’ timing critical circuit elements” to “provide a more accurate reflection of the circuit delay behavior of the respective circuit blocks,” i.e., the respective portion of the integrated circuit. MTK-1004, 9:56-62. Accordingly, it would have been obvious to a POSITA that Tam discloses utilizing constituent devices of a voltage sensor that have similar timing elements as—and are thus similar to—devices comprising the portion of the integrated circuit. *Id.* According to Tam, doing so provides a more accurate

reflection of the circuit delay behavior of the devices (e.g., FPU 211, L1 cache 212, IEU 213) comprising the portion of the integrated circuit (e.g., processor core 210).

7. Claim 6

72. Claim 6 recites: “[t]he method of claim 4 further comprising: further determining a switching speed of the constituent devices at the delivered voltage.”

Tam provides claim 6. MTK-1004, 9:22-67, 10:45-11:12, FIGS. 1-7B.

73. First, as previously discussed with respect to claims 4 and 5, a POSITA would have recognized that, like the transistors of the ’563 patent, Tam’s inverters depicted in FIG. 5A comprise constituent devices of a voltage sensor, e.g., ring oscillator 500. MTK-1004, FIG. 5A.

74. Second, the background section of the ’563 patent—which I note constitutes AAPA—acknowledges that a POSITA would have understood that **“voltage is a primary determinate of switching speed”** for such constituent devices, MTK-1001, 1:24-25, and that **“the voltage in large part determines the switching speed”** of such devices, *id.* at 1:44-45; *see also* MTK-1013, 8:50-58 (“higher power being a result of the higher voltage of the system power supply and the higher switching speed resulting from the higher VCO speed”). Additionally, as recognized by the ’563 patent, a POSITA would have understood that the “relationship of the device speed to voltage ... is approximately linear,” MTK-1001, 1:50-55, and that the relationship between power, voltage, frequency, and switching

speed was “well known, and has been exploited for power management particularly in mobile devices,” *id.* at 2:1-17; *see also id.* at 1:59-67.

75. Third, as noted by the '563 patent, a “voltage sensor” can “measure the effect of the voltage on circuit speed” by applying the delivered voltage to the constituent devices and determining if the constituent devices remain “able to cycle at the currently provided clock frequency” at that voltage. MTK-1001, 5:6-25. Indeed, as I have explained in the Background of Technology section above, a POSITA would have known that the voltage levels, e.g., V_{OL} and V_{OH} used for the circuitry in Fig. 13.5 of Sedra, place limits as to how fast the clock frequency for the circuitry can be. As in the '563 patent, Tam discloses a voltage sensor, e.g., ring oscillator 500, that applies the delivered voltage to constituent devices, e.g., inverters 510-518, and a clock generator that adjusts the clock frequency accordingly. *See* MTK-1004, FIGS. 3-5A, 9:22-67. Thus, in my opinion, it would have been obvious to a POSITA that Tam’s voltage sensor 500 would measure the effect of the voltage on circuit speed by determining whether constituent devices 510-518 are able to cycle at the current clock frequency and, if not, adjust the clock frequency accordingly.

8. Claim 7

76. Claim 7 recites: “[t]he method of claim 6 further comprising: using the switching speed to determine the appropriate frequency.” Tam provides claim 7.

Supra claims 4 and 6. For example, in my opinion, it would have been obvious to a POSITA that, with knowledge of the constituent devices' power consumption, delivered voltage, and switching speed, the system could determine an updated "appropriate" frequency using well-known mathematical relationships, such as those disclosed as AAPA within the background portion of the '563 patent. *See, e.g.*, MTK-1001, 1:59-67 (" $P = C \times V^2 \times F$ "). This equation describes the same relationship as Eq. (13.20) of Sedra, which I explained in the Background of Technology section. As I have noted, Sedra is a widely used textbook for the undergraduate curriculum in Electrical Engineering, and one of ordinary skill in the art would have known this equation.

9. Claim 8

77. Claim 8 recites: "[t]he method of claim 4 further comprising: exposing the voltage sensor and the portion of the integrated circuit to the same physical conditions." Tam provides claim 8. For example, Tam discloses the possibility of exposing its voltage sensors to "the local VCC supply voltages," while using others sensors to monitor "current, power, temperature, and/or processing load" in another embodiment. MTK-1004, 12:34-37. In my opinion, it would have been obvious to a POSITA that by exposing the voltage sensors and certain portions of the integrated circuit to the same physical conditions, including the same VCC supply voltage, current, power, temperature, and/or processing load, one could accurately track those

conditions at those specific portions of the integrated circuit. Indeed, Tam discloses that by exposing a voltage sensor to the same physical conditions as the underlying portion of the integrated circuit, the sensor can better indicate the existence of a voltage condition in that specific circuitry:

For example, a local sensor in a high activity area such as the FPU can better indicate the existence of a critical low voltage condition **in that circuitry**[.]

MTK-1004, 6:12-14.

Similarly, a number of voltage sensors are distributed over the integrated circuit to provide supply voltage readings from other circuit locations. These sensors are to detect the voltage of the supply **available to the surrounding circuitry** and to communicate the voltage values to the clock generator 408.

Id. at 8:31-36. A POSITA would have understood that tracking the physical condition of the voltage sensors' surrounding circuitry is important because physical conditions, such as temperature, can impact how fast an integrated circuit can run at a given voltage. Thus, it would have been obvious to a POSITA that exposing voltage sensors and portions of the integrated circuit to the same physical conditions, include voltage, current, power, temperature, and/or processing load, would be beneficial and would provide "an accurate and useful view of the power environment." MTK-1004, 5:62-65, 12:33-39.

10. Claim 9

78. Claim 9 recites: “[t]he method of claim 8 wherein the physical conditions include temperature.” Tam provides claim 9 for at least the reasons discussed directly above with respect to claim 8, which I incorporate herein.

11. Claim 10

79. Claim 10 recites: “[t]he method of claim 1 further comprising: calculating a value for the delivered voltage.” Tam provides claim 10. MTK-1004, 9:42-55, claims 29-30. For example, the ’563 patent notes that “an analog to digital converter” (an “A/D converter”) may be used “to actually measure [i.e., calculate] the value of the delivered voltage.” MTK-1001, 5:49-51; *id.* at 5:55-57 (“This voltage is converted 602 to a numeric value, by a analog-to-digital converter for example.”). A POSITA would have understood that Tam discloses using an A/D converter for just that purpose. MTK-1004, 9:42-55, claims 29-30. Specifically, Tam teaches that different “types of voltage sensors are available and can be implemented in accordance with the present invention,” including a “voltage sensor” comprising “an analog to digital converter.” MTK-1004, 9:42-46. According to Tam, that A/D converter “takes the local voltage as one input” and “can communicate the numerical value of the local voltage,” i.e., the value for the delivered voltage, “over a digital bus as a binary set of bits of 8 or 16 bits back to the clock generator block.” MTK-1004, 9:44-50. In other words, Tam discloses

using an A/D converter to calculate a digital value (as a binary set of bits) from an analog value for the local VCC supply voltage.

80. In fact, Tam expressly claims certain embodiments comprising an A/D converter that “receive[s] a first voltage reading” from a “voltage sensor” and converts that “voltage reading from an analog value to an [sic] coded numerical value”:

a first analog-to-digital (A/D) converter coupled to receive a first voltage reading from said first voltage sensor, said first A/D converter to **convert said first voltage reading from an analog value to an coded numerical value;**

MTK-1004, claim 29.

The apparatus of claim 29 further comprising **a second A/D converter** coupled to receive a second voltage reading from said second voltage sensor, said second A/D converter to **convert said second voltage reading from an analog reference value to an encoded numerical reference value**, and said encoded numerical reference value to be provided to said frequency adjustment circuit as said reference.

Id. at claim 30.

81. Thus, in my opinion, a POSITA would have understood that Tam teaches calculating a value for the delivered voltage using an A/D converter by converting local voltage readings from analog values to digital values. A POSITA

would have also understood that Tam’s disclosure is similar to several embodiments described within the ’563 patent.

12. Claim 23

(a) Element 23[p]

82. The preamble of claim 23 recites: “[a] system for circuit control.” Tam provides the preamble of claim 23 for at least the reasons discussed above with respect to claim elements 1[p] through 1[c], my discussions for which I incorporate herein by reference.

(b) Element 23[a]

83. Claim element 23[a] recites: “at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit.” Tam provides claim element 23[a] for at least the reasons discussed above with respect to claim elements 1[p] and 1[a]. Indeed, Tam expressly discloses the use of voltage sensors for sensing delivered voltages to portions of an integrated circuit. *See, e.g.*, MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 11:24-28, 12:14-11, 12:30-64, FIGS. 1-7B, claims 1-30.

(c) Element 23[b]

84. Claim element 23[b] recites: “at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit.” Tam provides claim element 23[b] for at least the reasons discussed above with respect to claim elements 1[p] and 1[b]. *See also* MTK-1004, Abstract, 2:30-

40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 12:4-11, 12:30-64, FIGS. 1-7B, claims 1-30.

85. Moreover, Tam expressly discloses at least one logic block (e.g., “clock control logic” / “frequency/voltage control logic”), within its clock generator, to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit:

Logic in the clock generator 214 monitors the voltage statuses and **can dynamically adapt and adjust the clock frequency** based on the sensed information.

MTK-1004, 6:9-12.

Subsequently, the **clock control logic can adjust the processor clock frequency** to shift the processor operating point to meet certain power conditions. The operating frequency can be adjusted when supply voltages vary across the die in order to achieve the desired power and performance trade off.

Id. at 9:16-21.

The **frequency/voltage control logic** is enabled at block 725. The frequency/voltage control can shift the processor operating point by **adjusting the processor core frequency** and the processor supply voltage.

Id. at 12:24-29.

The **frequency/voltage control logic** and clock circuitry analyze inputs from sensors that track the local VCC supply voltages.

Id. at 12:34-36; *see also id.* at FIGS. 1-7B.

(d) Element 23[c]

86. Claim element 23[c] recites: “at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.” Tam provides claim element 23[c] for at least the reasons discussed above with respect to claim elements 1[p], 1[b], and 1[c]. *See also* MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 12:4-11, 12:30-64, FIGS. 1-7B, claims 1-30.

87. Moreover, Tam expressly discloses at least one circuitry arrangement (including the clock generator and/or clock distribution network) to provide the appropriate frequency to the portion of the integrated circuit:

Clock generator 302 is to provide an internal processor clock signal CORE CLOCK₁ 324 to the rest of the processor core 354 via a clock distribution network 350.

MTK-1004, 6:41-44.

Upon receipt of the voltage information, **the clock circuitry 302** can evaluate the data and respond accordingly. If any of the sensors indicated that any voltage droops or transients exist, the clock signal can be adjusted to avoid performance errors and to maintain consistent power draw.

Id. at 7:43-47.

Upon receipt of the sensor data, the dynamic frequency adjustment **circuit** 462 can evaluate the supply voltage conditions and dynamically adapt the clock oscillator output 414 appropriately.

Id. at 8:37-40.

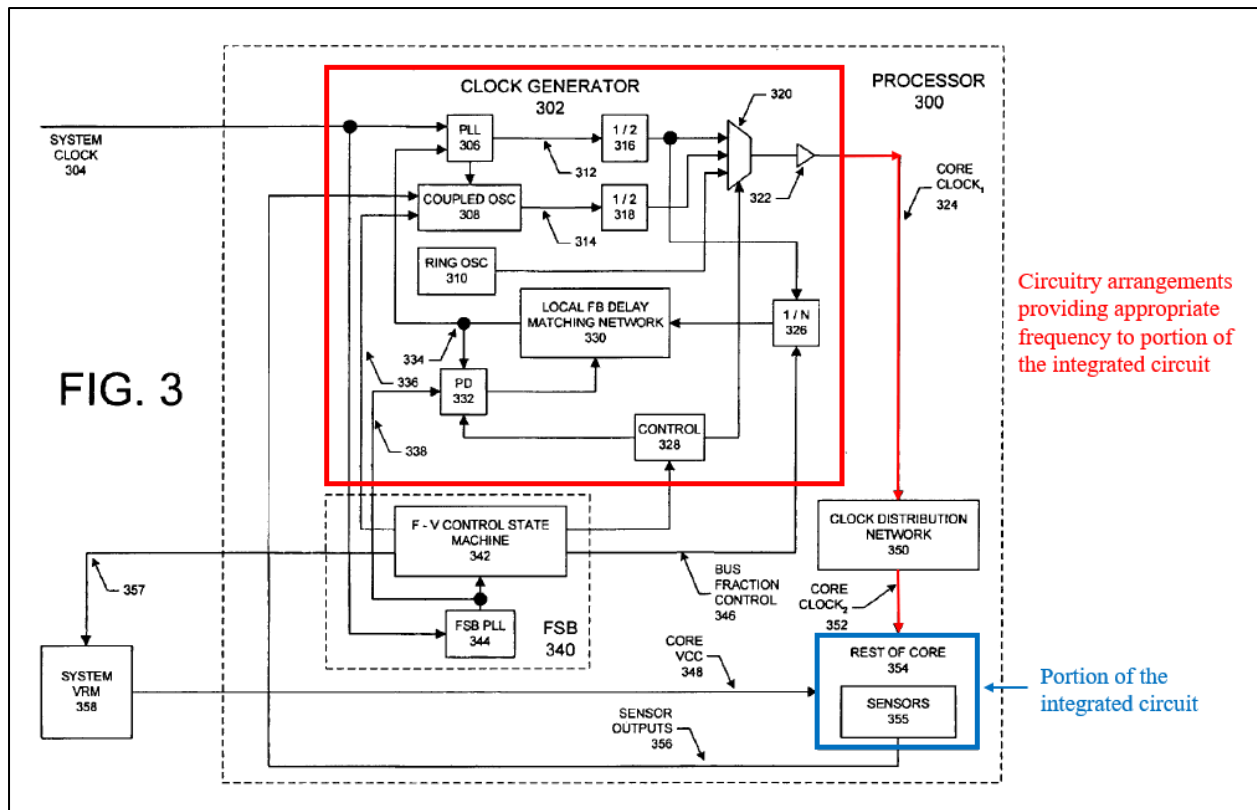
FIG. 6A is a dynamic frequency adjustment **circuit** 600 of one embodiment. The frequency adjustment **circuit** 600 provides an ability to tune the core clock frequency in accordance to outputs from voltage sensors 610, 620, 630, 640.

Id. at 10:14-18.

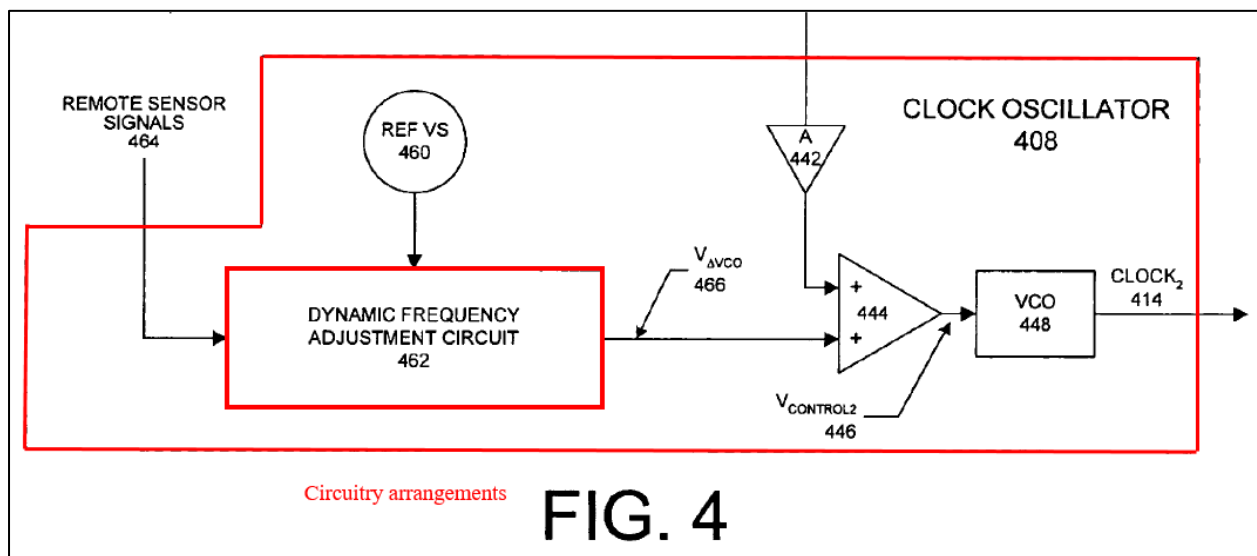
The frequency/voltage control logic and **clock circuitry** analyze inputs from sensors that track the local VCC supply voltages.

Id. at 12:34-36; *see also id.* at claim 1, FIGS. 1, 3, 4, 6A.

88. In fact, as depicted in FIGS. 3-4 below, Tam's clock generator 302 (which includes the dynamic frequency adjustment circuit 462 within the coupled oscillator 308/clock oscillator 408) provides an updated clock frequency, i.e., the appropriate frequency, to clock distribution network 350, which in turn provides it to a portion of the integrated circuit, e.g., processor core 354:



MTK-1004, FIG. 3



MTK-1004, FIG. 4

13. Claim 24

89. Claim 24 recites: “[t]he system of claim 23, wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.” Tam provides claim 24 for at least the reasons discussed above with respect to claim 3, the discussion of which I incorporate herein by reference.

14. Claims 31 and 32

90. Claim 31 recites: “[t]he system of claim 23 further comprising: a converter to convert the delivered voltage to a value.” Claim 32 recites: “[t]he system of claim 31 wherein the converter is an analog-to-digital converter.” Tam provides both claims 31 and 32 for at least the reasons discussed above with respect to claim 10, the discussion of which I incorporate herein by reference.

15. Claim 35

(a) Element 35[p]

91. The preamble of claim 35 recites: “[a] system for circuit control.” Tam provides the preamble of claim 35 for at least the reasons discussed above with respect to claim elements 1[p] through 1[c] and 23[p] through 23[c], the discussions for which I incorporate herein by reference.

(b) Element 35[a]

92. Claim element 35[a] recites: “a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit.” Tam provides claim element 35[a] for at least the reasons discussed above with respect to

claim elements 1[p] and 1[a]. Indeed, Tam expressly discloses the use of a plurality of voltage sensors for sensing delivered voltages to different portions of an integrated circuit. *See, e.g.*, MTK-1004, Abstract, 2:30-40, 3:44-4:5, 4:55-5:5, 5:46-6:32, 6:33-45, 7:34-50, 8:20-65, 9:22-10:26, 10:45-11:12, 11:24-28, 12:14-11, 12:30-64, FIGS. 1-7B, claims 1-30.

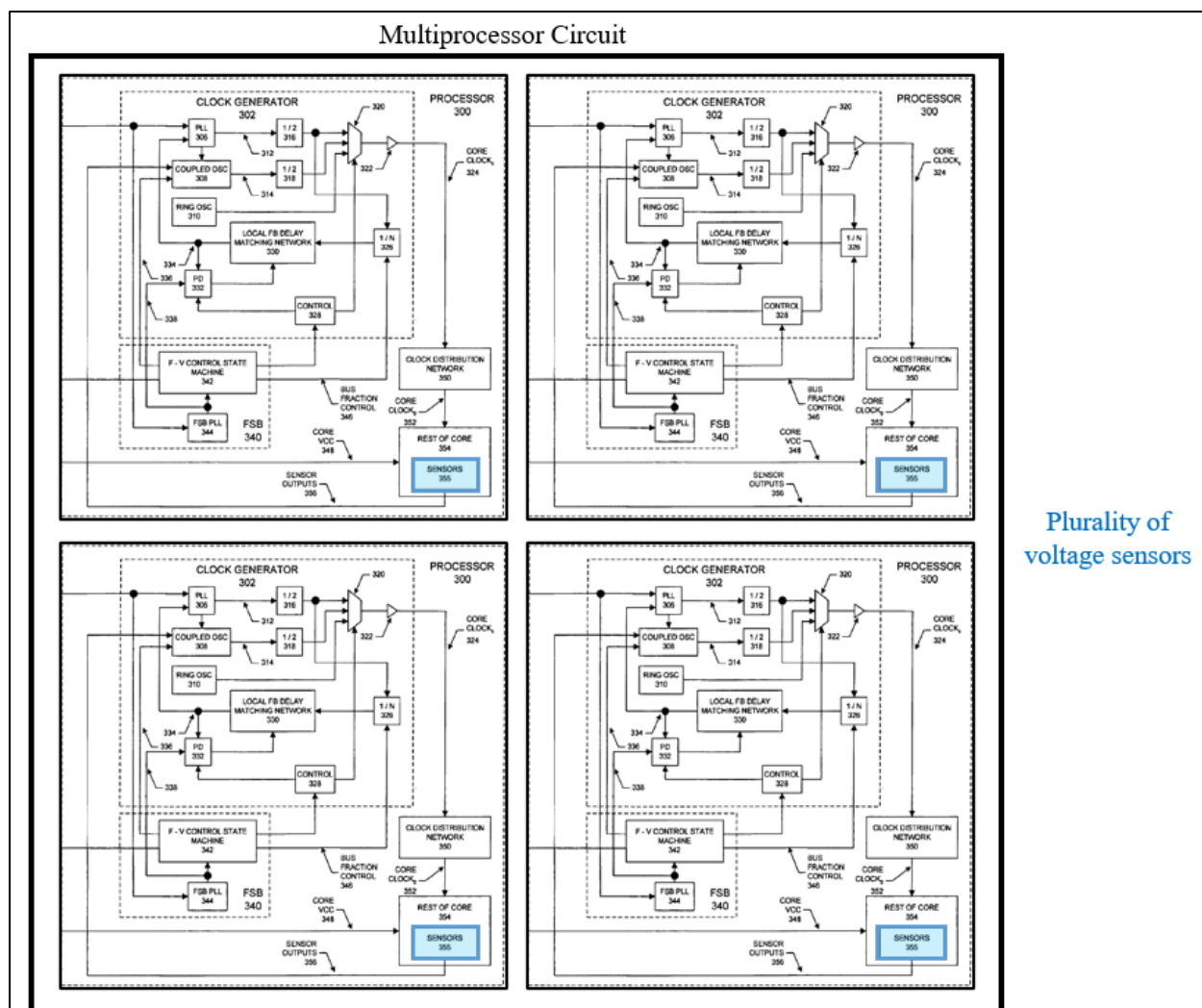
93. Moreover, Tam teaches that its circuit control system can be utilized in a multiprocessor environment. MTK-1004, 4:39-42 (“embodiments can [be] included in a multiprocessor system”). Thus, in my opinion, it would have been obvious to a POSITA to apply Tam’s teaching to a number of known multiprocessor (or multi-core) integrated circuits, including very large-scale integration (i.e., VLSI) devices, multi-chip modules (i.e., MCMs), and multiprocessor systems on a chip (MPSoCs). *E.g.*, MTK-1001, 1:19-23 (VLSI); MTK-1004, 5:36-39; MTK-1009, 488; MTK-1010, 460, 833; MTK-1011, 223; MTK-1012, 22-4; MTK-1020, ¶¶6-17.

94. A POSITA would have further understood that, in such a multiprocessor system, Tam’s circuit control “method can be performed concurrently in each processor” and that “[e]ach processor can contain an adaptive variable frequency clock system”:

The examples above have been described in the context of a single processor. In a multiprocessor system, **the method can be performed concurrently in each processor. Each processor can contain an adaptive variable frequency clock system.** For example, each

processor can be adjusting its own frequency and voltage settings independent of the other processors in the system.

Id. at 13:12-18. A POSITA would have understood that, to perform Tam's circuit control method concurrently across the various processors in a multiprocessor system, each processor would necessary include "on-die voltage sensors and [an] adaptively variable clock generator[.]" MTK-1004, 5:46-48. In my opinion, it would have been obvious to a POSITA that voltage sensors in each of the processors' cores would sense a delivered voltage to those processors' cores, i.e., different portions of the integrated circuit:



MTK-1004, FIG. 3 (Tam's FIG. 3 processor in potential multiprocessor system)

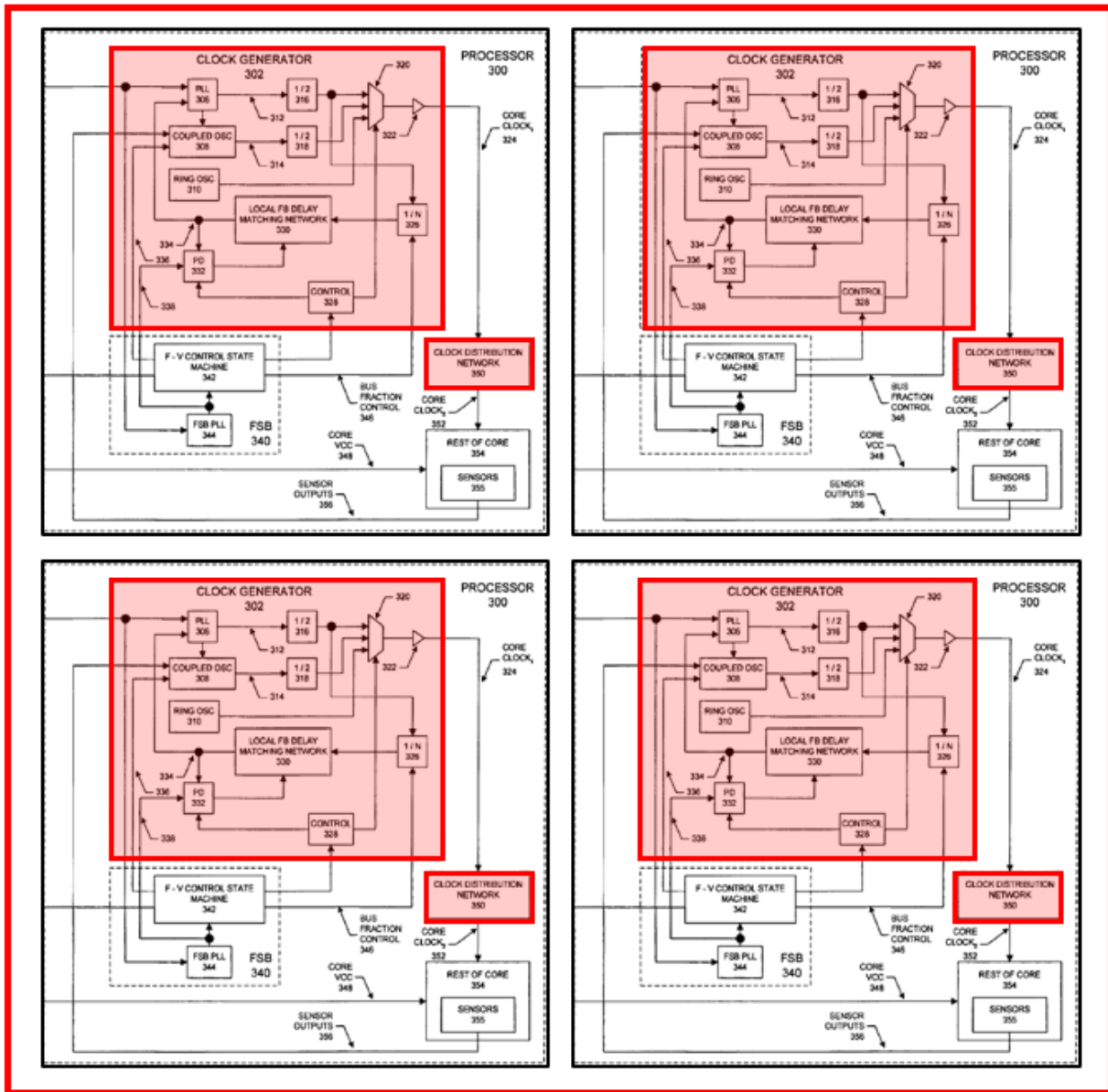
(c) Element 35[b]

95. Claim element 35[b] recites: “a plurality of logic blocks arranged to determine an appropriate frequency for each said portion from said delivered voltages.” Tam provides claim element 35[b] for at least the reasons discussed above with respect to claim elements 1[p], 1[b], 23[b], and 35[a].

96. For example, it would have been obvious to a POSITA that, in a multiprocessor system, such as the one depicted above with respect to claim element

35[a], logic in each of the processors' clock generators (e.g., "clock control logic" / "frequency/voltage control logic"), i.e., the plurality of logic blocks arranged to determine an appropriate frequency, would have determined new clock frequencies for each of the processors' cores, i.e., each said portion of the integrated circuit, from the voltages delivered to each such core and sensed by that cores' voltage sensors. MTK-1004, 13:12-18.

Plurality of logic blocks / circuitry arrangements



MTK-1004, FIG. 3 (Tam's FIG. 3 processor in potential multiprocessor system)

(d) Element 35[c]

97. Claim element 35[c] recites: “a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.” Tam provides claim

element 35[c] for at least the reasons discussed above with respect to claim elements 1[p], 1[b], 1[c], 23[b], 23[c], 35[a], and 35[b].

98. For example, in my opinion, it would have been obvious to a POSITA that, in a multiprocessor system, each processor would include Tam's clock generator/clock distribution network (i.e., a plurality of circuitry arrangements), as shown in red below, for providing each processor core (i.e., portions of the integrated circuit) its associated appropriate frequency. *See* MTK-1004, 13:12-18 ("each processor can" "adjust[] its own frequency").

B. Analysis of Tam in view of Huard with respect to Claims 1-11, 23-24, and 31-35

71

would have readily understood that Tam in view of Huard renders obvious all elements of claims 1-11, 23-24, and 31-35.

1. Overview of Huard

100. Huard relates “to controlling operating conditions such as clock frequency ... as a function of the ... instantaneous voltage of the circuit.” MTK-1005, 1:20-24. Huard discusses an exemplary embodiment via reference to FIG. 6, the discussion of which I reproduce below with relevant excerpts emphasized:

FIG. 6 illustrates one exemplary embodiment of a system 60 according to this invention. A power supply 12 provides electrical power to a voltage regulator 14, which provides a voltage supply Vcc to a load circuit 16. The load circuit can be, for example, a microprocessor, or any other device in which it is appropriate for the invention to be practiced. The voltage regulator may typically be adapted to provide different voltages to different components in the system, but, for ease of illustration, only the Vcc voltage to the load circuit is illustrated here. **A clock generator 22 provides a clock signal CLK to the load circuit.**

A temperature sensor 62 measures the operating temperature of the load circuit and provides a signal T indicating the present temperature. **A voltage sensor 64 is coupled to measure the Vcc voltage provided to the load circuit, and to provide a present voltage signal Vnow indicating the instantaneous present voltage.** In some embodiments, the temperature sensor and the voltage sensor may be constructed as one unified module performing both functions.

A frequency responder 66 is coupled to receive the outputs V_{now} and T of the voltage sensor and the temperature sensor, respectively, and, in response to them, provides a frequency control signal F to the clock generator to control the frequency of the clock signal CLK . As long as the load circuit is cool enough (e.g. below T_{test}), the clock frequency can be raised above F_{limit} . The cooler the circuit is, the faster it can be clocked. At some point, the increased frequency will raise the temperature enough that the frequency must be lowered.

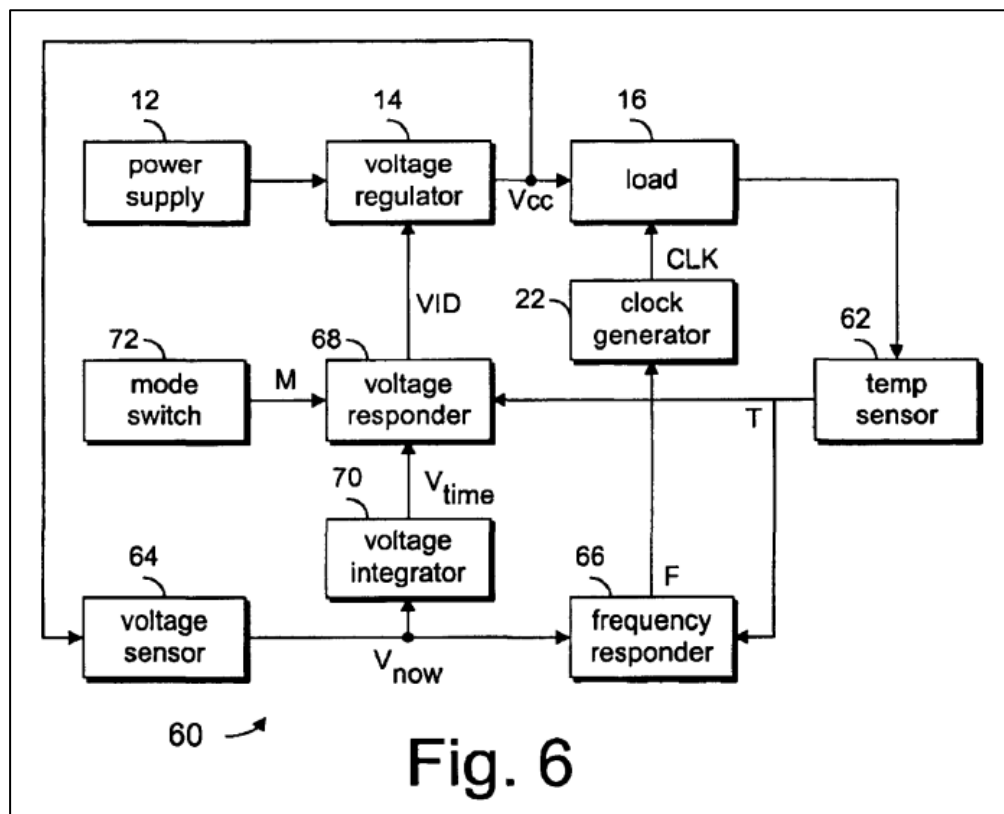
The system also includes a voltage responder 68 which provides a voltage identification signal VID to tell the voltage regulator what V_{cc} voltage it should provide to the load circuit. The voltage responder does this as a function of the temperature signal T from the temperature sensor, and as a function of the instantaneous voltage V_{now} . In some embodiments, it may be found desirable to operate the voltage responder according to a voltage identification V_{time} which has been smoothed over time, rather than according to the instantaneous voltage V_{now} itself; in such cases, a voltage integrator 70 may be included to provide this smoothing function. The smoothing allows the voltage responder to make VID changes that make better sense in the long term, rather than simply responding to a possibly wildly swinging V_{now} value.

An optional mode switch 72 provides a mode signal M to control the voltage responder, such that the system operates in either a high-performance mode or a low-power mode. If the mode switch has selected high-performance mode, the voltage responder will cause the operating voltage V_{cc} to be raised as high as reliability limits will allow, which will in turn enable the frequency

responder to cause the clock signal CLK frequency to be raised.

In the low-power mode, the voltage responder will cause the operating voltage V_{cc} to be lowered as low as possible while still maintaining adequate performance, which will in turn force the frequency responder to lower the frequency, both of which will lower the temperature.

MTK-1005, 3:38-4:25.



MTK-1005, FIG. 6

101. According to Huard, with reference to FIG. 6 above, “[a] power supply 12 provides electrical power to a voltage regulator 14, which provides a voltage supply V_{cc} to a load circuit 16,” e.g., a portion of an integrated circuit. MTK-1005,

3:39-43. “A voltage sensor 64 is coupled to measure the Vcc voltage provided to the load circuit, and to provide a present voltage signal Vnow indicating the instantaneous present voltage.” *Id.* at 3:51-54. “A frequency responder 66 is coupled to receive ... Vnow and ... provides a frequency control signal F,” “in response” to Vnow, to the clock generator to control the frequency of the clock signal CLK.” *Id.* at 3:56-60. The new frequency, CLK, is provided from the clock generator back to the load circuit. FIG. 6.

102. Huard further discloses that “the frequency responder,” which receives a voltage signal indicating the instantaneous present voltage and sends a control signal F to the clock generator to adjust the load circuit’s frequency, can be implemented as [a] lookup table[] stored in read-only memory,” i.e., a computer readable database. MTK-1005, 4:31-33. Specifically, Huard discloses that its frequency responder 66 uses the “detected supply voltage,” i.e., the instantaneous present voltage, for load circuit 16 as an address in the lookup table, to determine the “maximum frequency permitted,” i.e., an appropriate frequency, at that voltage. *See id.* at 3:8-20, 4:26-38, claims 1, 3, 4, 15, 22, 23, 36, and 37. Having determined the appropriate frequency utilizing its lookup table, the frequency responder 66 then

directs the clock generator 22 to provide the appropriate frequency, CLK, back to the load circuit 16, i.e., the portion of the integrated circuit.⁴ *Id.* at 3:56-60, FIG. 6.

2. Combination of Tam and Huard

103. In my opinion, a POSITA would have been motivated to combine Tam and Huard for a number of reasons.

104. At the time of the alleged invention, Tam and Huard were commonly owned by Intel and were in the same field of endeavor. MTK-1004, 1:8-12 (“[T]he present invention relates to a method and apparatus for a VCC adaptive dynamically variable frequency clock system[.]”); MTK-1005, 1:20-24 (“This invention relates generally to controlling operating conditions such as clock frequency ... as a function of the operating temperature and instantaneous voltage of the circuit.”). Indeed, Tam and Huard both address a known problem (combating voltage droop), having a finite number of identified predictable solutions, in the same way. *See* MTK-1004, 2:35-39 (noting invention can be applied to avoid “voltage droop transients”); MTK-1005, 4:39-42 (noting advantage of invention is ability to address “voltage droop”).

105. As noted herein, both Tam and Huard disclose a method and apparatus for: (1) sensing a delivered voltage to a portion of an integrated circuit (e.g., the

⁴ According to Huard, this system is applicable when “operating a wide variety of synchronous load circuits,” i.e., multiple portions of a larger integrated circuit. MTK-1005, 5:1-7.

“processor core” for Tam and the “load circuit” for Huard) using voltage sensors; (2) determining an appropriate frequency for that portion of the integrated circuit based on the sensed voltage using a frequency adjustment/responder circuit; and (3) providing that appropriate frequency to the portion of the integrated circuit via a clock generator/distribution network. Moreover, both Tam and Huard teach that adjusting frequency for a portion of an integrated circuit in response to instantaneous voltage changes or droops (as measured by local voltage sensors) would be beneficial to system performance. *See* MTK-1004, 3:44-4:5 (By “dynamically adjusting the clock frequency based on sensed on-die voltage changes,” Tam’s circuit “control technique” “provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.”), 7:45-50 (such a method/system could “avoid performance errors, “maintain consistent power draw,” and “continue to operate despite non-optimal voltage conditions at certain locations on the die”); MTK-1005, 4:50-58 (“the invention will ... enabl[e] the majority of the systems, in which the power supply or voltage regulator are performing well, to operate at a higher performance level”).

106. As addressed in Section VIII.A above, Tam discloses using a “dynamic frequency adjustment circuit,” which receives “sensor data” from “voltage sensors ... distributed over the integrated circuit,” to “evaluate the supply voltage conditions and dynamically adapt the clock oscillator output [] appropriately.” MTK-1004,

8:24-40; *see also id.* at 5:2-5, 9:16-18, 12:24-28, 12:50-53. However, in my opinion, a POSITA would have understood that how Tam’s “dynamic frequency adjustment circuit” selects an appropriate frequency corresponding to a sensed voltage is merely a design choice with a finite number of known solutions.

107. As discussed in the overview of Huard above, and in more detail below with respect to, e.g., claim 11, a POSITA would have understood that Huard discloses a solution for selecting an appropriate frequency, in response to a sensed voltage, in the form of a “lookup table[] stored in read-only memory.” MTK-1005, 4:31-33. Indeed, Huard discloses a “frequency responder,” which a POSITA would have understood corresponds to Tam’s “dynamic frequency adjustment circuit,” that uses “the detected supply voltage as [an] address[] into the lookup table” to “select[] a maximum frequency permitted by ... the detected supply voltage,” i.e., an appropriate frequency for the sensed voltage. MTK-1005, claims 36-37.

108. In my opinion, because Tam and Huard provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have looked at, and been motivated to combine, Tam and Huard—especially considering their common ownership—when selecting a method for Tam’s “dynamic frequency adjustment circuit” to determine the appropriate frequency for a given voltage. Thus, would have been obvious to a POSITA to use Huard’s lookup table in Tam’s “dynamic frequency adjustment circuit” to determine the appropriate frequency for

the voltage delivered to a portion of the integrated circuit. A POSITA would have understood that utilizing a lookup table, as in Huard, in the “dynamic frequency adjustment circuit” of Tam to select the maximum frequency permitted by the sensed voltage would have been a mere design choice that was both obvious to try and would have yielded predictable results. A POSITA would have further had a reasonable expectation of success in such a combination, as evidenced by, among other things, Huard itself, which uses a lookup table to determine a frequency that is appropriate for the detected voltage.

3. Claim 1

(a) Element 1[p]

109. The preamble of claim 1 recites: “[a] method of circuit control.” The combination of Tam and Huard provides the preamble of claim 1 for at least the reasons discussed above in the analysis of claim element 1[p] with respect to Tam. Moreover, like Tam, Huard similarly discloses a method of circuit control. For example:

36. A method of operating a load circuit which is coupled to receive a supply voltage from a voltage regulator and a clock signal from a clock generator, the clock signal having a clock frequency, wherein the method comprises:

detecting a present operating temperature of the load circuit;

detecting the supply voltage;

setting the clock frequency as a function of the detected present operating temperature and the detected supply voltage;

setting the supply voltage as a function of the detected present operating temperature; and

selecting a maximum frequency permitted by both the detected supply voltage and a reliability characteristic of the load circuit at the detected present operating temperature by looking up the maximum frequency in a lookup table.

MTK-1005, claim 36; *see also id.* at 5:8-15.

(b) Element 1[a]

110. Claim element 1[a] recites: “sensing a delivered voltage to a portion of an integrated circuit.” The combination of Tam and Huard provides claim element 1[a] for at least the reasons discussed above in the analysis of claim element 1[a] with respect to Tam. Moreover, like Tam, Huard similarly discloses sensing a delivered voltage to a portion of an integrated circuit. MTK-1005, Abstract, 1:20-24 (“This invention relates generally to controlling operating conditions such as clock frequency and supply voltage set point of a circuit, and more specifically to doing so as a function of the operating temperature and instantaneous voltage of the circuit.”), 2:10-23, 3:38-65 (“A voltage sensor 64 is coupled to measure the Vcc voltage provided to the load circuit, and to provide a present voltage signal Vnow

indicating the instantaneous present voltage.”), 4:26-38, 4:39-49, FIG. 6, claims 4, 7-8, 12, 15-25, 32, 36.

(c) Element 1[b]

111. Claim element 1[b] recites: “determining an appropriate frequency for the portion of the integrated circuit.” The combination of Tam and Huard provides claim element 1[b] for at least the reasons discussed above in the analysis of claim element 1[b] with respect to Tam. Moreover, like Tam, Huard similarly discloses determining an appropriate frequency for the portion of the integrated circuit, e.g., a load circuit. MTK-1005, Abstract, 1:20-24, 2:10-23, 3:38-65 (“A frequency responder 66 is coupled to receive the outputs ... of the voltage sensor and ... in response to them, provides a frequency control signal F to the clock generator to control the frequency of the clock signal CLK.”), 4:13-25, 4:39-49, FIG. 6, claims 7-8, 12, 15-25, 32, 36. Thus, to the extent it is determined that Tam does not explicitly disclose determining an appropriate frequency for a specific portion of the integrated circuit, it would have been obvious to a POSITA to use the dynamic frequency adjustment circuit of Tam to determine an appropriate frequency for a specific portion of the integrated circuit (as done by Huard’s frequency responder), in the combination of Tam and Huard.

(d) Element 1[c]

112. Claim element 1[c] recites: “providing the appropriate frequency to said portion of said integrated circuit.” The combination of Tam and Huard provides claim element 1[c] for at least the reasons discussed above in the analysis of claim element 1[c] with respect to Tam. Moreover, like Tam, Huard discloses providing the appropriate frequency to said portion of said integrated circuit. MTK-1005, Abstract, 1:20-24, 2:10-23, 3:38-65, 4:13-25, 4:39-49, FIG. 6, claims 7-8, 12, 15 (“a clock generator coupled to provide to the load circuit a clock signal”), 16-25, 32, 36.

4. Claim 2

113. Claim 2 recites: “[t]he method of claim 1 wherein said sensing, determining, and providing are continuously repeated during the integrated circuit’s operation.” The combination of Tam and Huard provides claim 2 for at least the reasons discussed above in the analysis of claim 2 with respect to Tam.

5. Claim 3

114. Claim 3 recites: “[t]he method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.” The combination of Tam and Huard provides claim 3 for at least the reasons discussed above in the analysis of claim 3 with respect to Tam.

115. However, to the extent it is determined that Tam does not explicitly disclose having the appropriate frequency be the maximum frequency possible, the combination of Tam and Huard discloses having the appropriate frequency be the

maximum frequency possible for the portion of the integrated circuit at the delivered voltage. For example, Huard specifically discloses “detecting the supply voltage” of a portion of the integrated circuit and “setting the clock frequency as a function of ... the detected supply voltage,” where the frequency is the “**maximum frequency permitted by [] the detected supply voltage[.]**” MTK-1005, claim 36. Thus, in my opinion, it would have been obvious to a POSITA that the combination of Tam and Huard disclose selecting the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

6. Claim 4

116. Claim 4 recites: “[t]he method of claim 1 further comprising: applying the delivered voltage to constituent devices of a voltage sensor.” The combination of Tam and Huard provides claim 4 for at least the reasons discussed above in the analysis of claim 4 with respect to Tam.

7. Claim 5

117. Claim 5 recites: “[t]he method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.” The combination of Tam and Huard provides claim 5 for at least the reasons discussed above in the analysis of claim 5 with respect to Tam.

8. Claim 6

118. Claim 6 recites: “[t]he method of claim 4 further comprising: further determining a switching speed of the constituent devices at the delivered voltage.”

The combination of Tam and Huard provides claim 6 for at least the reasons discussed above in the analysis of claim 6 with respect to Tam.

9. Claim 7

119. Claim 7 recites: “[t]he method of claim 6 further comprising: using the switching speed to determine the appropriate frequency.” The combination of Tam and Huard provides claim 7 for at least the reasons discussed above in the analysis of claim 7 with respect to Tam.

10. Claim 8

120. Claim 8 recites: “[t]he method of claim 4 further comprising: exposing the voltage sensor and the portion of the integrated circuit to the same physical conditions.” The combination of Tam and Huard provides claim 8 for at least the reasons discussed above in the analysis of claim 8 with respect to Tam.

11. Claim 9

121. Claim 9 recites: “[t]he method of claim 8 wherein the physical conditions include temperature.” The combination of Tam and Huard provides claim 9 for at least the reasons discussed above in the analysis of claim 9 with respect to Tam. Moreover, like Tam, Huard discloses exposing the voltage sensor and portion of the integrated circuit to the same physical conditions, where those conditions include temperature. MTK-1005, Title, Abstract, 1:20-24, 3:8-30, 3:49-55 (disclosing that a combined voltage/temperature sensor can detect voltage and temperature at the load circuit), 3:56-65, FIGS. 5-6, claims 1-3. A POSITA would

have understood that exposing the voltage sensor and portion of the integrated circuit to similar physical conditions, such as temperature, is important, because increased temperatures can result in “data corruption or catastrophic failure.” MTK-1005, 3:26-30. Moreover, a POSITA would have understood that exposing the voltage sensor and portion of the integrated circuit to the same temperature is necessary, because voltage impacts frequency, which in turn impacts temperature. If the temperature at the voltage sensor/portion of the integrated circuit is too high, the frequency will have to be lowered, which could be done by adjusting the supply voltage delivered to the voltage sensor at that specific portion of the integrated circuit. *Id.* at 3:60-65 (“At some point, the increased frequency will raise the temperature enough that the frequency must be lowered.”). Thus, in my opinion, it would have been obvious to a POSITA that the combination of Tam and Huard discloses wherein the physical conditions include temperature.

12. Claim 10

122. Claim 10 recites: “[t]he method of claim 1 further comprising: calculating a value for the delivered voltage.” The combination of Tam and Huard provides claim 10 for at least the reasons discussed above in the analysis of claim 10 with respect to Tam. Moreover, like Tam, Huard teaches that its voltage sensor can include an analog-to-digital converter for calculating a value for the delivered voltage. MTK-1005, 4:26-38 (“In one embodiment, the voltage sensor and the

temperature sensor can include analog-to-digital (A/D) converters, which output multi-bit binary signals V_{now} and T , respectively.”). Thus, in my opinion, it would have been obvious to a POSITA that the combination of Tam and Huard discloses utilizing voltage sensors that comprise analog-to-digital converters to calculate values for the delivered voltages to specific portions of an integrated circuit (e.g., Tam’s processor core).

13. Claim 11

123. Claim 11 recites: “[t]he method of claim 10 further comprising: using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.” The combination of Tam and Huard provides claim 11. *See* MTK-1005, 3:8-20, 4:26-38, claims 1, 3, 4, 15, 22, 23, 36, and 37.

124. First, Huard discloses “[a] frequency responder” that receives “a present voltage signal V_{now} indicating the instantaneous present voltage” and, “in response ... provides a frequency control signal ... to the clock generator to control the frequency of the clock signal”:

A voltage sensor 64 is coupled to measure the V_{cc} voltage provided to the load circuit, and to provide a present voltage signal V_{now} indicating the instantaneous present voltage. In some embodiments, the temperature sensor and the voltage sensor may be constructed as one unified module performing both functions.

A frequency responder 66 is coupled to receive the outputs V_{now} and T of the voltage sensor and the temperature sensor, respectively, and, in response to them, provides a frequency control signal F to the clock generator to control the frequency of the clock signal CLK.

MTK-1005, 3:51-60. According to Huard, “the frequency responder can be implemented as [a] lookup table[] stored in read-only memory,” i.e., a computer readable database. MTK-1005, 4:31-33.

125. Huard discloses multiple claimed embodiments whereby the frequency responder uses the lookup table, which a POSITA would have understood comprises a tabulation of a set of values, to determine the appropriate frequency for an associated supply voltage:

15. An apparatus comprising:

a voltage regulator to provide a supply voltage in response to a voltage identification control signal;

a load circuit coupled to receive the supply voltage;

a temperature sensor coupled to the load circuit to provide a temperature identification signal;

a voltage sensor coupled to provide a present voltage signal indicating a value of the supply voltage;

a frequency responder coupled to provide a frequency control signal as a function of the

temperature identification signal and the present voltage signal;

a clock generator coupled to provide to the load circuit a clock signal whose frequency is indicated by the frequency control signal;

a voltage responder coupled to provide the voltage identification control signal as a function of the temperature identification signal and the present voltage signal.

Id. at claim 15.

22. The apparatus of claim 15 wherein **the frequency responder comprises a lookup table.**

Id. at claim 22.

23. The apparatus of claim 22 wherein **the frequency responder's lookup table is addressed by the temperature identification signal and the present voltage signal.**

Id. at claim 23.

36. A method of operating a load circuit which is coupled to receive a supply voltage from a voltage regulator and a clock signal from a clock generator, the clock signal having a clock frequency, wherein the method comprises:

detecting a present operating temperature of the load circuit;

detecting the supply voltage;

setting the clock frequency as a function of the detected present operating temperature and the detected supply voltage;

setting the supply voltage as a function of the detected present operating temperature; and

selecting a maximum frequency permitted by both the detected supply voltage and a reliability characteristic of the load circuit at the detected present operating temperature by looking up the maximum frequency in a lookup table.

Id. at claim 36.

37. The method of claim 36 further comprising: **using the detected present operating temperature and the detected supply voltage as addresses into the lookup table.**

Id. at claim 37. Specifically, Huard discloses utilizing a lookup table, i.e., a tabulation of set of values, which includes values for the “maximum frequency permitted,” i.e., an appropriate frequency, for the “detected supply voltage,” i.e., the delivered voltage, which is used as an address in the lookup table. *Id.*

126. In my opinion, a POSITA would have recognized that Huard’s “frequency responder” directly corresponds to Tam’s “dynamic frequency adjustment circuit,” which similarly receives “sensor data” from “voltage sensors ... distributed over the integrated circuit,” “evaluate[s] the supply voltage conditions and dynamically adapt[s] the clock oscillator output [] appropriately.” MTK-1004,

FIG. 3

14. Claim 23

(a) Element 23[p]

90

(b) Element 23[a]

128. Claim element 23[a] recites: “at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit.” The combination of Tam and Huard provides claim element 23[a] for at least the reasons discussed above in the analysis of claim elements 1[p]-1[a] and 23[a] with respect to Tam, and in the analysis of claim elements 1[p]-1[a] with respect to the combination of Tam and Huard.

(c) Element 23[b]

129. Claim element 23[b] recites: “at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit.” The combination of Tam and Huard provides claim element 23[b] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], and 23[b] with respect to Tam, and in the analysis of claim elements 1[p] and 1[b] with respect to the combination of Tam and Huard.

(d) Element 23[c]

130. Claim element 23[c] recites: “at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.” The combination of Tam and Huard provides claim element 23[c] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[c], and 23[c] with respect to Tam, and in the analysis of claim elements 1[p] and 1[c] with respect to the combination of Tam and Huard.

15. Claim 24

131. Claim 24 recites: “[t]he system of claim 23, wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.” The combination of Tam and Huard provides claim 24 for at least the reasons discussed above in the analysis of claim 3 with respect to Tam and in the analysis of claim 3 with respect to the combination of Tam and Huard.

16. Claims 31 and 32

132. Claim 31 recites: “[t]he system of claim 23 further comprising: a converter to convert the delivered voltage to a value.” Claim 32 recites: “[t]he system of claim 31 wherein the converter is an analog-to-digital converter.” The combination of Tam and Huard provides claims 31 and 32 for at least the reasons discussed above in the analysis of claim 10 with respect to Tam and in the analysis of claim 10 with respect to the combination of Tam and Huard.

17. Claim 33

133. Claim 33 recites: “[t]he system of claim 23 further comprising: a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.” The combination of Tam and Huard provides claim 33 for at least the reasons discussed above in the analysis of claim 11 with respect to the combination of Tam and Huard.

18. Claim 34

134. Claim 34 recites: “[t]he system of claim 33 wherein said table is a computer readable database.” The combination of Tam and Huard provides claim 34 for at least the reasons discussed above in the analysis of claim 11 with respect to the combination of Tam and Huard.

19. Claim 35

(a) Element 35[p]

135. The preamble of claim 35 recites: “[a] system for circuit control.” The combination of Tam and Huard provides the preamble of claim 35 for at least the reasons discussed above in the analysis of claim elements 1[p]-1[c], 23[p]-23[c], and 35[p] with respect to Tam, and in the analysis of claim elements 1[p]-1[c] and 23[p]-23[c] with respect to the combination of Tam and Huard.

(b) Element 35[a]

136. Claim element 35[a] recites: “a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit.” The combination of Tam and Huard provides claim element 35[a] for at least the reasons discussed above in the analysis of claim elements 1[p]-1[a] and 35[a] with respect to Tam, and in the analysis of claim elements 1[p]-1[a] with respect to the combination of Tam and Huard.

(c) Element 35[b]

137. Claim element 35[b] recites: “a plurality of logic bocks arranged to determine an appropriate frequency for each said portion from said delivered

voltages.” The combination of Tam and Huard provides claim element 35[b] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], 23[b], and 35[a]-35[b] with respect to Tam, and in the analysis of claim elements 1[p], 1[b], and 23[b] with respect to the combination of Tam and Huard.

(d) Element 35[c]

138. Claim element 35[c] recites: “a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.” The combination of Tam and Huard provides claim element 35[c] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], 1[c], 23[b], 23[c], and 35[a]-35[c] with respect to Tam, and in the analysis of claim elements 1[p], 1[b], 1[c], 23[b], and 23[c] with respect to the combination of Tam and Huard.

C. Analysis of Norman ’259 in view of Norman ’851 with respect to Claims 1-11, 23-24, and 31-35

139. For the reasons articulated in detail below, and based on my review of the ’563 patent and the Norman ’259 and Norman ’851 references, I am confident that a POSITA would have readily understood that Norman ’259 in view of Norman ’851 (which I understand the Petition refers to as “the Norman Combination”) renders obvious all elements of claims 1-11, 23-24, and 31-35.

1. Overview of Norman ’259

140. Norman ’259 relates to “[a]n apparatus” and “method” that “compensates for voltage and temperature variations on an integrated circuit”:

An apparatus compensates for voltage and temperature variations on an integrated circuit with: a voltage sensor having a digital voltage output; a temperature sensor having a digital temperature output; a register coupled to the voltage sensor and the temperature sensor, the register adapted to concatenate the digital voltage output and the temperature output into an address output; and a memory device having an address input coupled to the address output of the register, the memory device being adapted to store one or more corrective vectors.

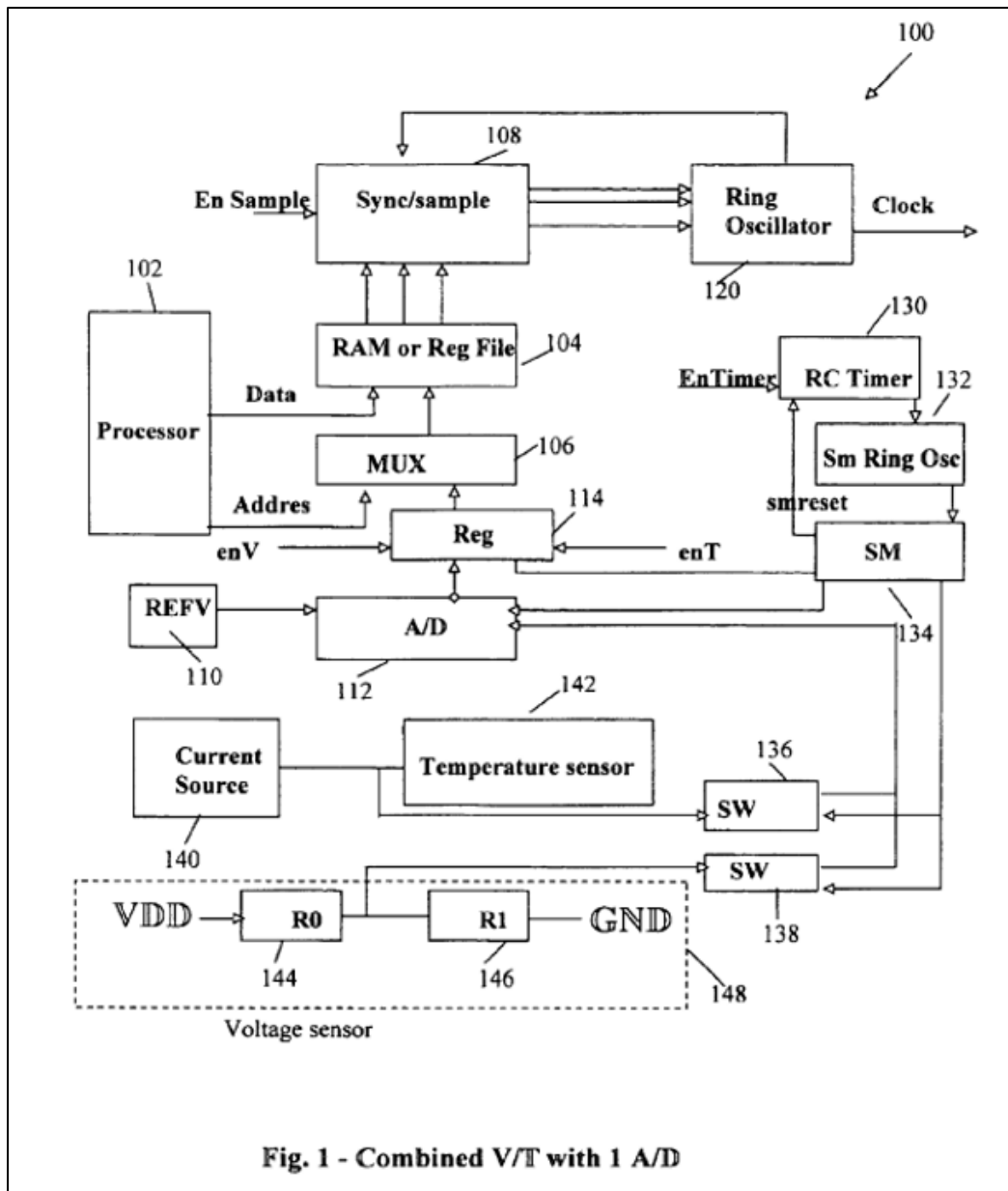
MTK-1006, Abstract; *id.* at 2:58-62 (further disclosing “**a method for dynamically adjusting for temperature and voltage variations on an integrated circuit**”).

141. Norman '259 discloses “dynamically adjusting for temperature and voltage variations on an integrated circuit” by “periodically sensing the voltage and temperature values[] and dynamically making adjustments in clock frequency based on the voltage and temperature values.” *Id.* at 2:58-62. To do this, Norman '259 discloses utilizing:

A voltage sensor having a digital voltage output; a register coupled to the voltage sensor having a digital temperature output; a register coupled to the voltage sensor and the temperature sensor, the register adapted to concatenate the digital voltage output and the temperature output into an address output; and a memory device having an address input coupled to the address output of the register, the memory device being adapted to store one or more corrective vectors.

Id. at 2:28-37. According to Norman '259, “[t]he memory device can generate an adjustment vector,” e.g., an adjustment for a new operating frequency, “based on the current voltage and temperature,” “wherein the adjustment vector is applied to the ring oscillator” and “selects the ring frequency; lengthening or shortening the ring delay to maintain the desired operating point.” *Id.* at 2:46-51.

142. Norman '259 discusses the invention in relation to the exemplary autocalibration system depicted in FIG. 1:



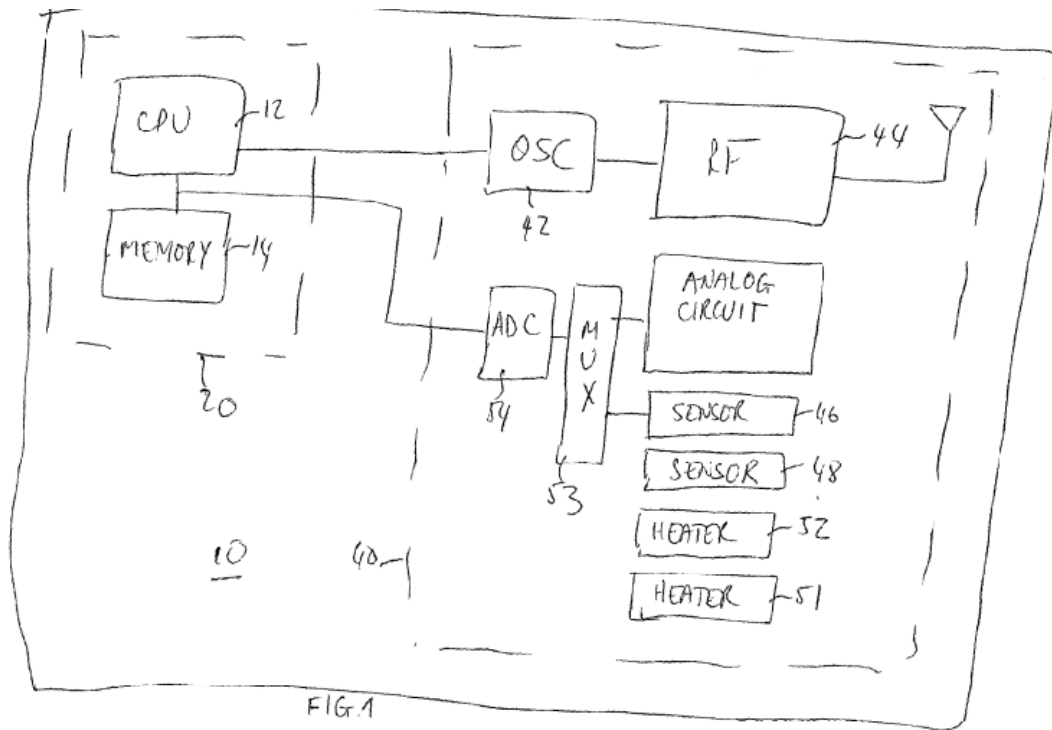
MTK-1006, FIG. 1

Norman '259 teaches that, “[t]o adjust for” changes in temperature and voltage “and keep the system running at the ideal frequency, the temperature and voltage of the system needs to be monitored.” MTK-1006, 4:1-7. After sensing voltage and temperature values using voltage sensor 148 (which comprises constituent

devices 144 and 146) and temperature sensor 142, *id.* at 4:7-36, those values are applied to the ADC [analog-to-digital converter] 112, and the “output of the ADC 112 is registered and applied to the multiplexor 106,” which is driven by an address from the processor 102.” MTK-1006, 4:15-20. “The output of the multiplexor 106 is applied to the memory 104 as the address input” and, “[a]t initialization, the processor 102 writes adjustment values into the RAM or Register File 104,” and the “output of the RAM 104 ... acts as the adjustment vector that is applied to the ring oscillator 120” to “select[] the ring frequency.” MTK-1006, 4:20-29; *id.* at claim 7 (“the memory device generates an adjustment vector based on the current voltage and temperature and wherein the adjustment vector is applied to the ring oscillator”).

2. Overview of Norman '851

143. Norman '851 relates to a “self-calibrating integrated circuit” that “includes a processor having at least one analog function used with the processor; one or more sensors adapted to sense one or more environmental parameters of the at least one analog function; and a solid state memory being configured to store the one or more environmental parameters of the at least one analog function.” MTK-1007, Abstract. Norman '851 discusses the invention in relation to the exemplary system depicted in FIG. 1:



MTK-1007, FIG. 1

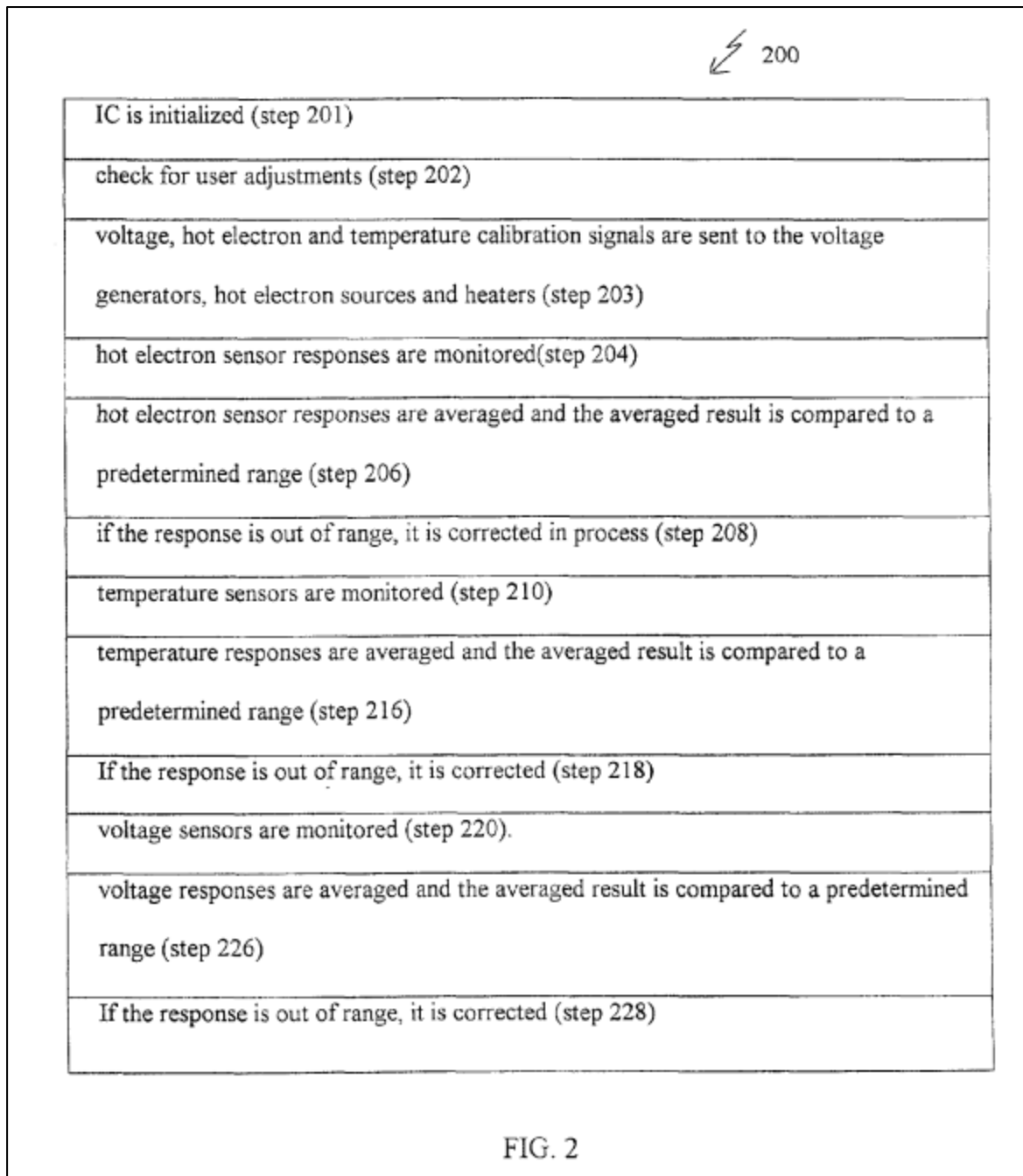
According to Norman '851, “[t]o capture information that allows the processor 12 to automatically calibrate the IC [integrated circuit] 10 so that the on-chip clock oscillator 42 is precise and accurate in spite of process, temperature or power supply variations, various sensors 46-48 are placed at predetermined locations in the IC 10 to sense environmental variations.” MTK-1007, [0019].

“Environmental parameters of the IC include temperature, supply voltage and other external parameters which effect the performance of the IC 10.” *Id.* at [0024].

144. According to Norman '851, by using various “voltage sensors,” *id.* at [0026], the system can “detect the supply voltage that the system is presently operating at and adjust for variations in the supply voltage,” *id.* at [0024]. In fact,

Norman '851 expressly claims certain embodiments of an integrated circuit that include “one or more sensors adapted to sense one or more environmental parameters” and “an oscillator ... having a frequency varied by one or more environmental parameters,” MTK-1007, claim 18, wherein those “environmental parameters include[] temperature or supply voltage,” *id.* at claim 19.

145. Norman '851's self-calibration method is described with reference to FIG. 2, which I have reproduced below:



MTK-1007, FIG. 2

First, the IC 10 is initialized (step 201). The process 200 checks for user adjustments (step 202). If a user wants to adjust the operating frequency of the clock to meet the temperature and voltage conditions of the application, the

process 200 adds the adjustments so that the oscillator moves toward the user specified operating frequency.

Next, in step 203, voltage, hot electron and temperature calibration signals are sent to the voltage generators, hot electron sources and heaters, respectively. These calibration signals are preferably generated by the processor 12 of FIG. 1 so that they have a known level and can be swept over a known test range. In process step 204, the hot electron sensor responses are monitored. In decision step 206, the hot electron sensor responses are averaged and the averaged result is compared to a predetermined range. If the response is out of range, it is corrected in process step 208. The above steps are performed for each sensor type. For example, in step 210, the temperature sensors are monitored. In decision step 216, the temperature responses are averaged and the averaged result is compared to a predetermined range. If the response is out of range, it is corrected in process step 218. **Next, in step 220, the voltage sensors are monitored.**

In decision step 226, the voltage responses are averaged and the averaged result is compared to a predetermined range. If the response is out of range, it is corrected in process step 228. In the above manner, each sensor type is monitored and the environment sensed by the sensor type is adjusted. For example, if the temperature gets hotter (indicating slower silicon and slower ring oscillator) the flash system will move the oscillator settings to the faster settings to compensate for the slow down because of increased temperature or a corresponding decrease in operating voltage.

The data is continually collected. This is done by having the processor 12 instruct the switch 53 to connect to each sensor 46-52 in seriatim and the ADC 54 to digitize the environmental parameters, and the FLASH memory file to store the output of the ADC 54 (step 240). The FLASH memory file can store one sample point for each sensor, or can store historical data for the sensors.

To keep a constant clock frequency, the process 200 moves the oscillator as to the environmental changes. Moreover, the processor 12 can predict the environmental changes based on historical data.

Id. at [0025]-[0029]. According to Norman '851, its “process of calibration and correction,” i.e., calibrating/correcting clock frequency based on voltage and temperature, “can be conducted for each sub-system of the IC 10,” i.e., each portion of the integrated circuit. *Id.* at [0030].

3. Combination of Norman '259 and Norman '851

146. In my opinion, a POSITA would have been motivated to combine Norman '259 with Norman '851.

147. As an initial matter, Norman '259 and Norman '851 share the same inventors (i.e., Norman and Schmidt), were commonly owned by Gallitzin Alleghany LLC when filed, and are in the same field of endeavor (as discussed above in the overview sections for each of these references). Thus, in my opinion, a POSITA attempting to solve the problem addressed by each of the references would have naturally looked to, and been motivated to combine with, the other reference.

148. Second, Norman '851 appears to expressly incorporate the contents of Norman '259's application by reference. For example, as previously discussed, Norman '851 discloses a "self-calibrating integrated circuit" that "includes a processor having at least one analog function used with the processor; one or more sensors adapted to sense one or more environmental parameters of the at least one analog function; and a solid state memory being configured to store the one or more environmental parameters of the at least one analog function." MTK-1007, Abstract. However, Norman '851 discloses that:

Additional details on the device that corrects temperature and voltage variations are discussed in a co-pending patent application entitled "**Ring Oscillator Dynamic Adjustments for Auto-calibration**" and having Ser. No. _____, the content of which is hereby incorporated by reference.

MTK-1007, [0024]. It would have been clear to a POSITA that the application that led to Norman '259 is the referenced "co-pending patent application entitled '**Ring Oscillator Dynamic Adjustments for Auto-Calibration.**'" *Compare* MTK-1007, [0024], *with* MTK-1006, Title ("**Ring Oscillator Dynamic Adjustments for Auto-Calibration**"). Thus, a POSITA would have understood that Norman '851 incorporates the contents of Norman '259 by reference, and that Norman '851—itself—suggests combining Norman '259 with Norman '851.

149. Third, Norman '259 and Norman '851 both address a known problem (compensating for voltage and temperature variations), having a finite number of identified predictable solutions, in the same way. For example, as discussed above, both references utilize voltage and temperature sensors for sensing instantaneous voltage and temperature fluctuations in an integrated circuit, and a ring oscillator for adjusting clock frequency based on those supply voltage and temperature variations. *See, e.g.*, MTK-1006, Abstract, 2:28-37, 2:46-51, 2:58-62, 3:10-25, 3:67-4:1, 4:4-5:10, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0004], [0006]-[0007], [0009], [0019], [0024]-[0027], claims 1-3 and 18-19, FIGS. 1-2. Indeed, Norman '259 discloses a device that corrects for temperature and voltage variations, while Norman '851 discloses utilizing the device of Norman '259 in a system including multiple “sub-systems” and “voltage sensors.” *See* MTK-1007, [0024], [0026], [0030].

150. Finally, because Norman '259 and Norman '851 provide a similar solution to a similar problem within the same field of endeavor, I believe that a POSITA would have naturally looked at, and been motivated to combine, the two references—especially considering their common inventorship, common ownership, and incorporations by reference—when using Norman '259's dynamic frequency adjustment method to self-calibrate a system having multiple voltage sensors and sub-systems as in Norman '851.

4. Claim 1

(a) Element 1[p]

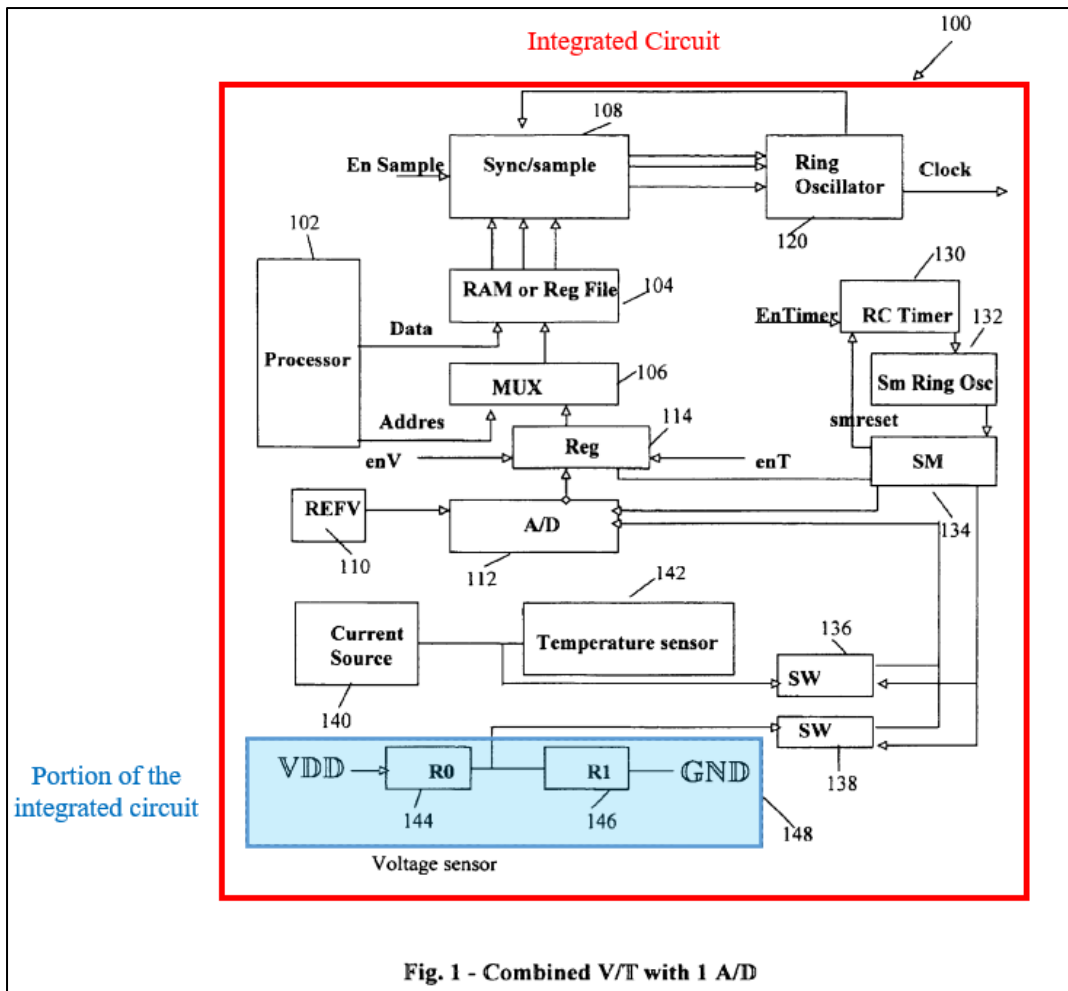
151. The preamble of claim 1 recites: “[a] method of circuit control.” The combination of Norman ’259 and Norman ’851 provides the preamble of claim 1. *See* MTK-1006, 2:12-24, 2:58-62, claim 11; MTK-1007, Title. For example, the combination of Norman ’259 and Norman ’851 discloses “a method for dynamically adjusting for ... voltage variations on an integrated circuit” that involves “periodically sensing the voltage ... values” and “making adjustments in clock frequency based on the voltage ... values.” MTK-1006, 2:58-62; *id.* at claim 11 (“A method for dynamically adjusting for ... voltage variations on an integrated circuit...”); MTK-1007, [0001] (“The present invention relates [to] systems and method for self-calibrating semiconductor devices.”), [0025] (“An exemplary processor of calibrating and correcting the IC 10 is shown in the flow chart 200 of FIG. 2.”), FIG. 2.

(b) Element 1[a]

152. Claim element 1[a] recites: “sensing a delivered voltage to a portion of an integrated circuit.” The combination of Norman ’259 and Norman ’851 provides claim element 1[a]. *See* MTK-1006, Abstract, 2:28-37, 2:58-62, 3:10-25, 4:4-7, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0006], [0007], [0009], [0019], [0023]-[0027], claims 1, 3, and 18-19, FIGS. 1-2.

153. As an initial matter, Norman '851 states that details of “the device that corrects ... voltage variations are discussed in” the application that led to Norman '259, which Norman '851 “incorporate[s] by reference.” MTK-1007, [0024] (incorporating application “entitled ‘Ring Oscillator Dynamic Adjustments for Auto-calibration’ by reference). Norman '259, in turn, discloses “a method for dynamically adjusting for ... voltage variations on an integrated circuit” that includes “periodically sensing the voltage” values using a voltage sensor. MTK-1006, 2:58-62; *id.* at 2:28-30 (an apparatus for “compensat[ing] for voltage ... variations on an integrated circuit includes: a voltage sensor”), FIG. 1 (depicting voltage sensor 148 located at a portion of integrated circuit 100).

154. In my opinion, it would have been obvious to a POSITA that a voltage sensor, like the one depicted in blue in FIG. 1 from Norman '259 below, would sense a voltage delivered to a portion of the integrated circuit, e.g., the portion of the integrated circuit or sub-system where the voltage sensor is located:



MTK-1006, FIG. 1

155. Moreover, in my opinion, it would have been obvious to a POSITA, based on Norman '851, to include voltage sensors, like the one from Norman '259 shown in blue above, at various “predetermined locations in the IC [integrated circuit],” i.e., portions of the integrated circuit, “to sense environmental variations,” such as variations in “supply voltage,” at those locations. MTK-1007, [0019], [0023]-[0024], [0026] (“the voltage sensors are monitored”).

(c) **Element 1[b]**

156. Claim element 1[b] recites: “determining an appropriate frequency for the portion of the integrated circuit.” The combination of Norman ’259 and Norman ’851 provides claim element 1[b]. *See* MTK-1006, Abstract, 2:28-37, 2:46-51, 2:58-62, 3:10-25, 3:60-4:1, 4:4-7, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0004], [0006]-[0007], [0009], [0019], [0024]-[0027], claims 1-3 and 18-19, FIGS. 1-2.

157. For example, Norman ’259 discloses “keep[ing] the system running at the ideal frequency,” i.e., the appropriate frequency, by monitoring “the voltage of the system,” MTK-1006, 4:4-7, and “dynamically making adjustments in clock frequency based on the voltage,” *id.* at 2:58-62. *See also id.* at 2:46-51 (“The adjustment vector selects,” i.e., determines, “the ring frequency” “based on the current voltage and temperature[.]”), 3:10-25 (“These adjustments are accomplished by sensing the voltage ... values and dynamically making adjustments in clock frequency.”). Similarly, Norman ’851, which incorporates Norman ’259, discloses that the system can “detect the supply voltage that the system is presently operating at and adjust for variations in the supply voltage... If the operating voltage is not at a nominal value, the controller adjusts the ring oscillator delay path to compensate for the voltage differential.” MTK-1007, [0024]. Thus, in my opinion, a POSITA would have understood that the combination of Norman ’259 and Norman ’851 discloses monitoring the instantaneous supply voltage for a portion of the integrated

circuit and determining a new clock frequency for that portion of the integrated circuit by dynamically adjusting the clock frequency based on the detected voltage.

158. More specifically, the combination of Norman '259 and Norman '851 discloses that the ideal, i.e., appropriate, frequency for the portion of the integrated circuit is determined by:

[C]ombining the voltage and temperature values into a digital word. The method can store the temperature value in a first register; the voltage value in a second register; and merge the first and second registers to represent a concatenated address. **The concatenated address can be applied to the address of a memory to retrieve a corrective value from a corrective table.**

MTK-1006, 2:63-3:3. “The table should produce a desired center frequency[.]”

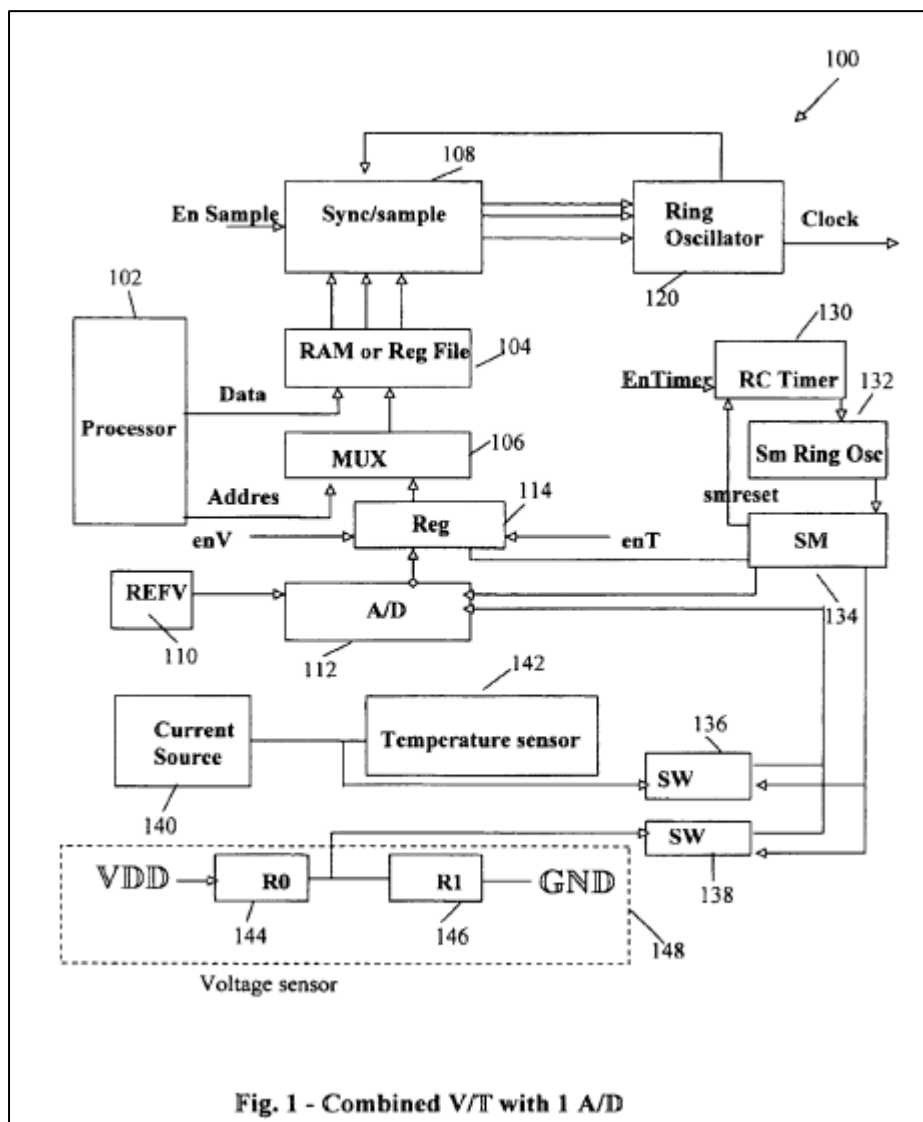
Id. at 4:64-5:1. Thus, it would have been obvious to a POSITA that the Norman Combination discloses sensing the instantaneous voltage and temperature values at a portion of the integrated circuit (using voltage and temperatures sensors), digitizing and concatenating those values, and then using the concatenated value as an address in a lookup table, i.e., a tabulation of a set of values, to determine the ideal, i.e., appropriate, frequency, associated with the delivered voltage.

(d) Element 1[c]

159. Claim element 1[c] recites: “providing the appropriate frequency to said portion of said integrated circuit.” The combination of Norman '259 and Norman '851 provides claim element 1[c] for at least the reasons addressed above

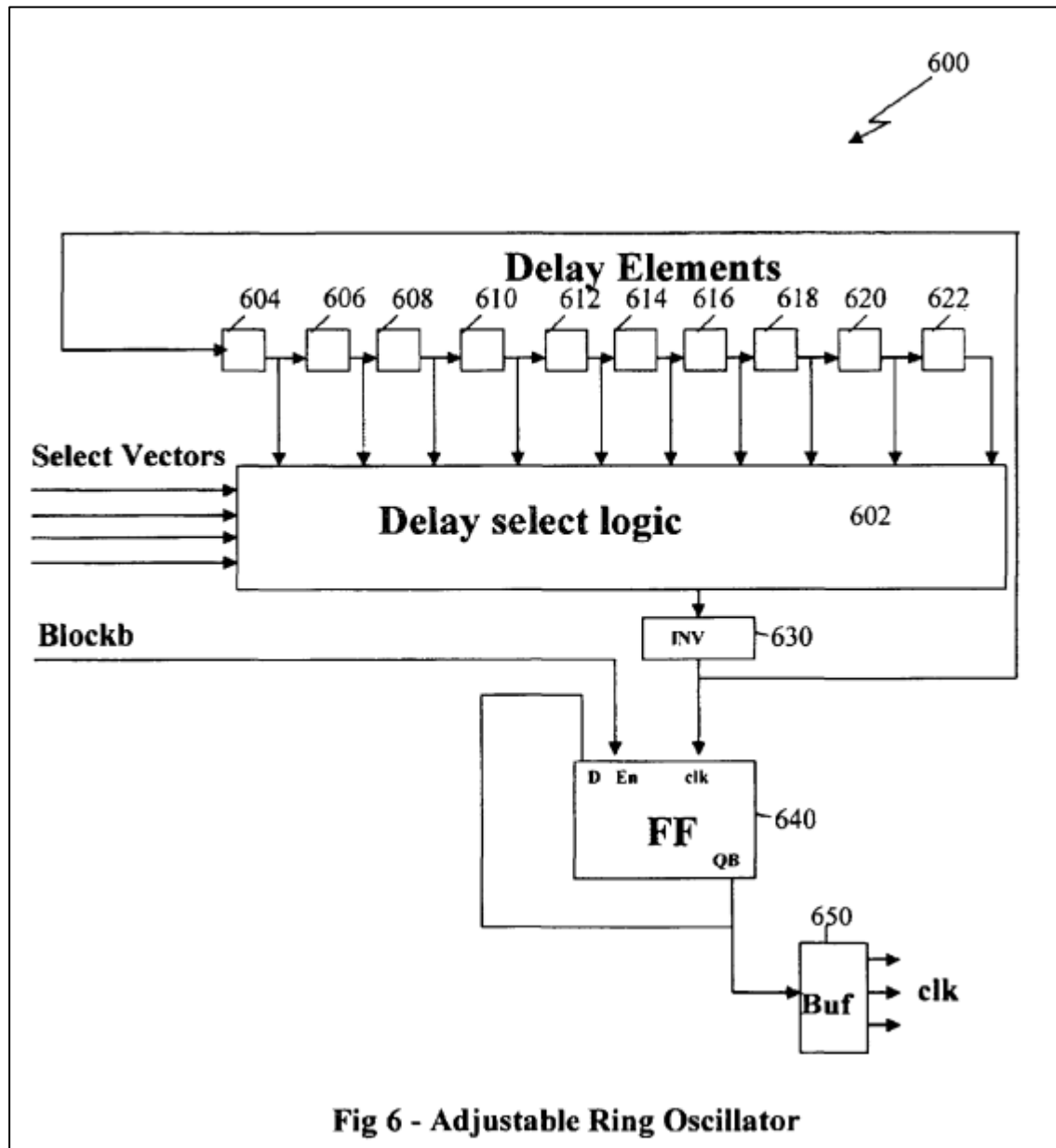
for claim element 1[b]. *See* MTK-1006, Abstract, 2:28-37, 2:46-51, 2:58-62, 3:10-25, 3:60-4:1, 4:4-7, FIG. 1, claims 1 and 11; MTK-1007, Abstract, [0004], [0006]-[0007], [0009], [0019], [0024]-[0027], claims 1-3 and 18-19, FIGS. 1-2.

160. As an initial matter, it would have been obvious to a POSITA that the combination of Norman '259 and Norman '851 teaches providing the newly generated clock frequency, e.g., “clock” coming from ring oscillator 120 in FIG. 1 of Norman '259 below, to the portion of the integrated circuit:



MTK-1006, FIG. 1

For example, an embodiment of ring oscillator 120 from FIG. 1 above is depicted in FIG. 6 of Norman '259:



MTK-1006, FIG. 6

See also id. at 6:58-59 (“FIG. 6 shows one embodiment of an adjustable ring oscillator 600”). According to Norman ’259, “[t]he output of the flip-flop 640 is ... provided to a buffer 650 that **provides a plurality of clock signals,**” e.g., “clk,” **“each of which can be used to clock a portion of the chip,”** which a POSITA would have understood to be a portion of the integrated circuit, “to prevent clock degradation due to too much load on the chip.” *Id.* at 6:66-7:3; *id.* at FIG. 6.

161. Additionally, it would have been obvious to a POSITA that the combination of Norman ’259 and Norman ’851 teaches sensing a voltage and providing an appropriate frequency for that voltage to various portions of the integrated circuit located across various sub-systems of the circuit. First, it would have been obvious to a POSITA that the combination of Norman ’259 and Norman ’851 teaches utilizing multiple “voltage sensors,” MTK-1007, [0026], like those described in Norman ’259 and incorporated into Norman ’851 by reference, which can be “placed at predetermined locations in the IC [] to sense environmental variations,” *id.* at [0019], including variations in “supply voltage,” *id.* at [0024]. A POSITA would have understood that those “predetermined locations in the IC” are different portions of the integrated circuit. Second, it would have been obvious to a POSITA that the combination of Norman ’259 and Norman ’851 discloses that its dynamic frequency adjustment mechanism could be applied to individual sub-systems located in the integrated circuit. *Id.*; MTK-1007, [0030] (“This process of

calibration and correction can be conducted for each sub-system of the IC.”). And third, it would have been obvious to a POSITA that correcting the sub-system, i.e., a portion of the integrated circuit, involves providing that sub-system with an appropriate frequency, which is determined based on the instantaneous voltage and temperatures readings for that sub-system. *See* MTK-1006, 4:54-5:1, 6:67-7:3.

5. Claim 2

162. Claim 2 recites: “[t]he method of claim 1 wherein said sensing, determining, and providing are continuously repeated during the integrated circuit’s operation.” The combination of Norman ’259 and Norman ’851 provides claim 2. *See* claim 1 *supra*; *see also* MTK-1006, 2:58-62, claim 11; MTK-1007, [0009], [0028]-[0029]. Specifically, a POSITA would have understood that the combination of Norman ’259 and Norman ’851 discloses “periodically” or “continually” sensing the voltage to continuously adjust the frequency to “prevent clock degradation,” MTK-1006, 6:66-7:3:

In another aspect, a method for dynamically adjusting for temperature and voltage variations on an integrated circuit includes **periodically sensing the voltage and temperature values; and dynamically making adjustments in clock frequency based on the voltage and temperature values.**

Id. at 2:58-62; *see also id.* at claim 11 (“A method for dynamically adjusting for temperature and voltage variations on an integrated circuit, comprising:

periodically sensing the voltage and temperature values...”); MTK-1007, [0028] (“The data is continually collected.”).

6. Claim 3

163. Claim 3 recites: “[t]he method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.” The combination of Norman ’259 and Norman ’851 provides claim 3. Indeed, it would have been obvious to a POSITA to have the appropriate frequency be the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

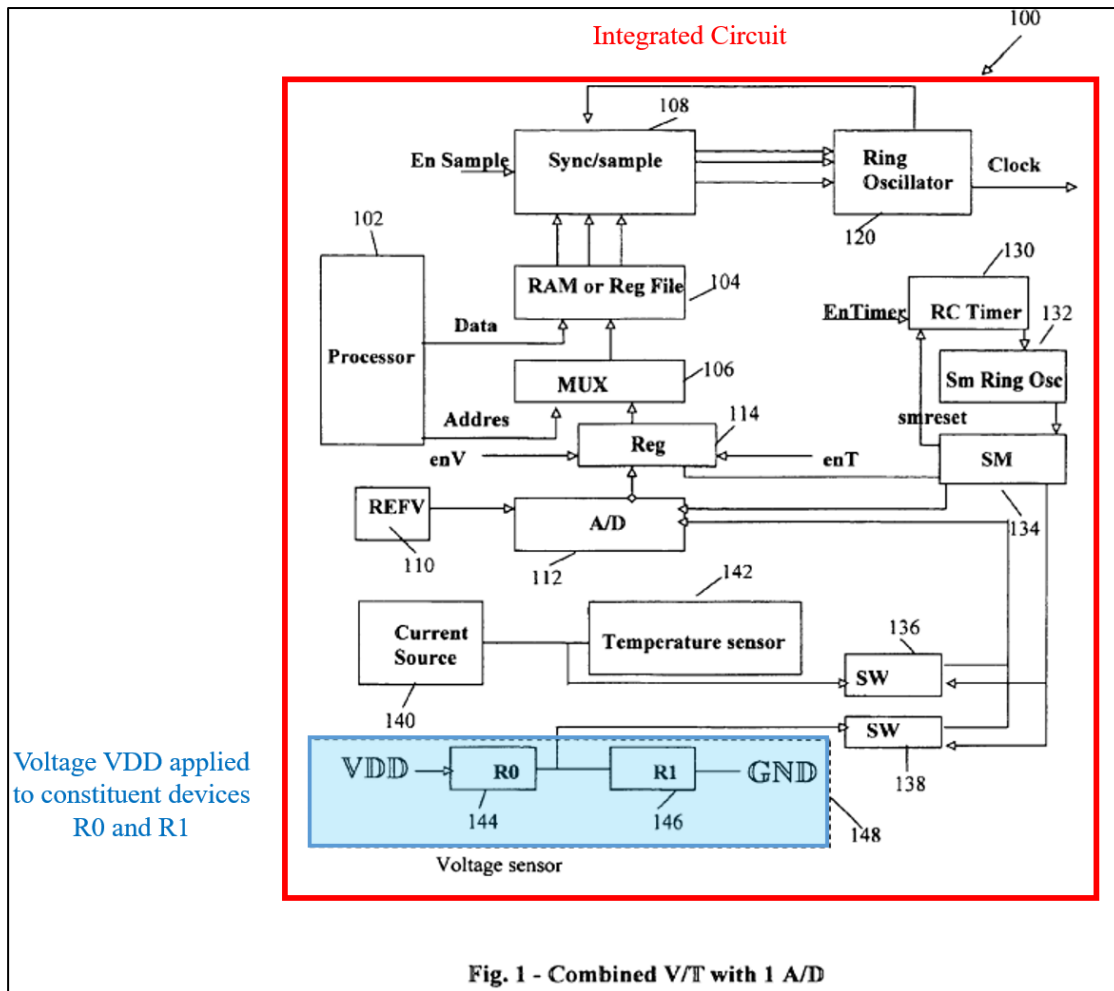
164. For example, the combination of Norman ’259 and Norman ’851 discloses selecting a “frequency that operates ... close to the desired frequency when operating at nominal temperature and voltage,” MTK-1006, 4:64-5:1, while noting that “by dynamically monitoring environmental parameters [such as voltage supply] and adjusting the operation and clock signal frequency” accordingly, “[t]he system optimizes operating performance,” MTK-1007, [0009]. In my opinion, this disclosure is commensurate with AAPA from the ’563 patent, which admits that, as of the time of the alleged invention, “a designer will typically specify the maximum frequency at which a part can operate for a given voltage.” MTK-1001, 1:24-27. As discussed elsewhere in this declaration, a “designer,” or POSITA, would have done this because they would have recognized that having the frequency remain close to

the maximum frequency supported by the voltage increases system efficiency. Thus, it would have been obvious to a POSITA that utilizing the maximum frequency supported by the delivered voltage would be beneficial to a system's performance.

7. **Claim 4**

165. Claim 4 recites: “[t]he method of claim 1 further comprising: applying the delivered voltage to constituent devices of a voltage sensor.” The combination of Norman '259 and Norman '851 provides claim 4.

166. Specifically, the combination of Norman '259 and Norman '851 discloses a “voltage divider having a first resistor 144 and a second resistor 146 in series between voltage and ground.” MTK-1006, 3:50-52; *see also id.* at 4:34-36 (“The system voltage in question can be applied to a voltage divider formed by resistors 144 and 146 that is input to the ADC 112.”). A POSITA would have understood that the referenced “voltage divider” is simply “voltage sensor 148” from FIG. 1 of Norman '259 (in blue below), which comprises resistors 144 and 146 in series between voltage VDD and ground GND:



MTK-1006, FIG. 1

A POSITA would have thus understood that the combination of Norman '259 and Norman '851 discloses applying "[t]he system voltage," i.e., delivered voltage VDD, to "resistors 144 and 146," i.e., constituent devices of voltage sensor 148, *id.* at 4:33-36, FIG. 1, which are connected together "in series," *id.* at 3:50-52.

8. Claim 5

167. Claim 5 recites: “[t]he method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.” The combination of Norman ’259 and Norman ’851 provides claim 5.

168. As noted in the ’563 patent, constituent devices of the voltage sensor would be similar to the devices comprising the portion of the integrated circuit if they have similar timing elements, including “length and propagation time delay[s],” as the underlying circuit. *See* MTK-1001, 5:26-31. In my opinion, it would have been obvious to a POSITA to have resistors 144 and 146 from FIG. 1 of Norman ’259, i.e., constituent devices of voltage sensor 148, be similar to the devices comprising the portion of the integrated circuit such as by having them have similar timing elements as the underlying circuits, to provide a more accurate reflection of the circuit delay behavior of that portion of the integrated circuit.

9. Claim 6

169. Claim 6 recites: “[t]he method of claim 4 further comprising: further determining a switching speed of the constituent devices at the delivered voltage.” The combination of Norman ’259 and Norman ’851 provides claim 6.

170. First, as previously discussed with respect to claims 4 and 5, a POSITA would have recognized that, like the transistors of the ’563 patent, resistors 144 and 146 depicted in FIG. 1 of Norman ’259 comprise constituent devices of a voltage sensor, e.g., voltage sensor 148. MTK-1006, FIG. 1.

171. Second, the background section of the '563 patent—which I note constitutes AAPA—acknowledges that a POSITA would have understood that **“voltage is a primary determinate of switching speed”** for such constituent devices, MTK-1001, 1:24-25, and that **“the voltage in large part determines the switching speed”** of such devices, *id.* at 1:44-45; *see also* MTK-1013, 8:50-58 (“higher power being a result of the higher voltage of the system power supply and the higher switching speed resulting from the higher VCO speed”). Additionally, as recognized by the '563 patent, a POSITA would have understood that the “relationship of the device speed to voltage ... is approximately linear,” MTK-1001, 1:50-55, and that the relationship between power, voltage, frequency, and switching speed was “well known, and has been exploited for power management particularly in mobile devices,” *id.* at 2:1-17; *see also id.* at 1:59-67.

172. Third, as noted by the '563 patent, a “voltage sensor” can “measure the effect of the voltage on circuit speed” by applying the delivered voltage to the constituent devices and determining if the constituent devices remain “able to cycle at the currently provided clock frequency” at that voltage. MTK-1001, 5:6-25. As I have explained in the Background of Technology section above, a POSITA would have known that the voltage levels, e.g., V_{OL} and V_{OH} used for the circuitry in Fig. 13.5 of Sedra, place limits as to how fast the clock frequency for the circuitry can be. In my opinion, it would have thus been obvious to a POSITA that the voltage

sensor 148 from FIG. 1 of Norman '259 would measure the effect of the voltage on circuit speed by determining whether constituent devices 144 and 146 are able to cycle at the current clock frequency and, if not, adjust the clock frequency accordingly.

10. Claim 7

173. Claim 7 recites: “[t]he method of claim 6 further comprising: using the switching speed to determine the appropriate frequency.” The combination of Norman '259 and Norman '851 provides claim 7. *Supra* claims 4 and 6 with respect to the combination of Norman '259 and Norman '851. For example, in my opinion, it would have been obvious to a POSITA that, with knowledge of the constituent devices’ power consumption, delivered voltage, and switching speed, the system could determine an updated “appropriate” frequency using well-known mathematical relationships, such as those disclosed as AAPA within the background portion of the '563 patent. *See, e.g.*, MTK-1001, 1:59-67 (“ $P = CxV^2xF$ ”). This equation describes the same relationship as Eq. (13.20) of Sedra, which I explained in the Background of Technology section. As I have noted, Sedra is a widely used textbook for the undergraduate curriculum in Electrical Engineering, and one of ordinary skill in the art would have known this equation.

11. Claim 8

174. Claim 8 recites: “[t]he method of claim 4 further comprising: exposing the voltage sensor and the portion of the integrated circuit to the same physical conditions.” The combination of Norman ’259 and Norman ’851 provides claim 8.

175. It would have been obvious to a POSITA to expose the voltage sensor and portion of the integrated circuit to the same physical conditions. First, a POSITA would have understood, based on the combination of Norman ’259 and Norman ’851, that one could “combine[] voltage and temperature detectors,” MTK-1006, 3:34-35, and that such “detectors” or “sensors” could be placed “at key locations across the chip” to “minimize[] wide variations in clock signal frequency over operating parameter variables such as voltage and temperature,” MTK-1007, [0009].

176. Second, it would have been obvious to a POSITA that by exposing the voltage sensors and certain portions of the integrated circuit to the same physical conditions, including the same VCC supply voltage, current, power, temperature, and/or processing load, one could accurately track those conditions at those specific portions of the integrated circuit. Moreover, a POSITA would have understood that tracking the physical condition of the voltage sensors’ surrounding circuitry is important because physical conditions, such as temperature, can impact how fast an integrated circuit can run at a given voltage. Thus, it would have been obvious to a POSITA that exposing voltage sensors and portions of the integrated circuit to the same physical conditions, include voltage, current, power, temperature, and/or

processing load, would, as noted in Tam (which is indicative of the knowledge of a POSITA at the time of the alleged invention), be beneficial and provide “an accurate and useful view of the power environment.” MTK-1004, 5:62-65, 12:33-39.

12. Claim 9

177. Claim 9 recites: “[t]he method of claim 8 wherein the physical conditions include temperature.” The combination of Norman ’259 and Norman ’851 provides claim 9 for at least the reasons discussed directly above with respect to claim 8, which I incorporate herein.

13. Claim 10

178. Claim 10 recites: “[t]he method of claim 1 further comprising: calculating a value for the delivered voltage.” The combination of Norman ’259 and Norman ’851 provides claim 10. For example, the ’563 patent notes that “an analog to digital converter” (an “A/D converter”) may be used “to actually measure [i.e., calculate] the value of the delivered voltage.” MTK-1001, 5:49-51; *id.* at 5:55-57 (“This voltage is converted 602 to a numeric value, by a analog-to-digital converter for example.”). A POSITA would have understood that the combination of Norman ’259 and Norman ’851 discloses using an A/D converter for just that purpose:

The circuit of FIG. 1 compensates for changes in voltage as follows. **The system voltage in question can be applied to a voltage divider formed by resistors 144 and 146 that is input to the ADC [analog-to-digital converter]112.** As the voltage changes the input to the

MTK-1006, 4:33-38. This is depicted in FIG. 1 of Norman '259 below:

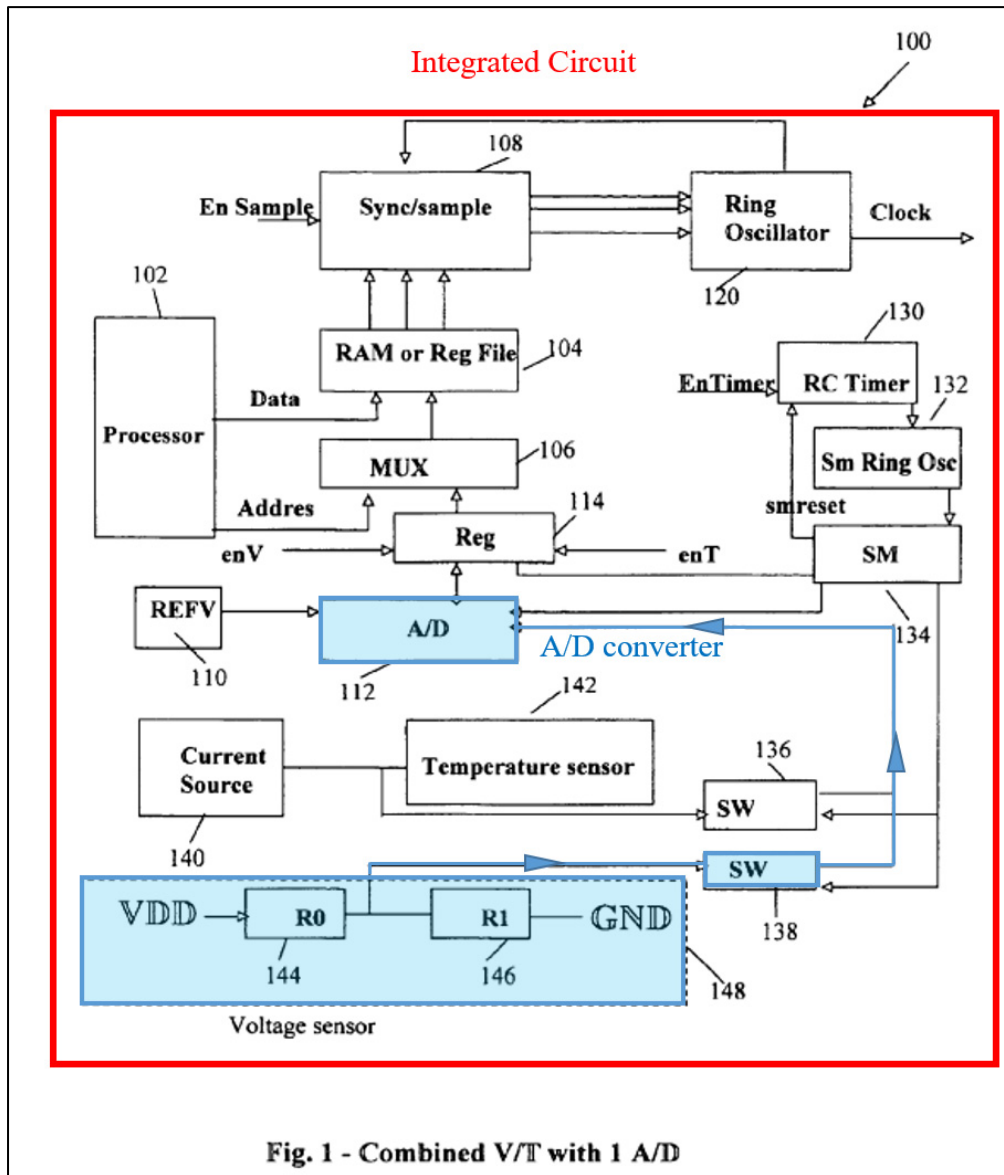


Fig. 1 - Combined V/T with 1 A/D

MTK-1006, FIG. 1

179. In my opinion, a POSITA would have understood that voltage values applied to the A/D converter would be translated to a digital value, and thus that the

A/D converter calculates a value for the delivered voltage. *See, e.g.*, MTK-1006, 4:15-17 (“This voltage ... value applied is translated to a digital value[.]”); MTK-1007, [0022] (“The outputs of the sensors 46-48 are provided to analog switch 53 that in turn is connected to a precision analog to digital converter 54 (ADC). The analog switch 53 is controlled by the processor 12 to select the output of one of the sensors 46-52 to the input of the ADC 54 to digitize autocalibration data. In one implementation, the ADC is a 12 bit ADC. The output of the ADC 54 is provided to the processor 12 to make decisions and the flash memory in the memory array 14 to store the autocalibration data.”).

14. Claim 11

180. Claim 11 recites: “[t]he method of claim 10 further comprising: using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.” The combination of Norman ’259 and Norman ’851 provides claim 11. *See* MTK-1006, 2:63-3:10, 4:64-5:1, claim 16, claim 17.

181. Specifically, the combination of Norman ’259 and Norman ’851 discloses implementations whereby:

The method includes combining the voltage and temperature values into a digital word. The method can store the temperature value in a first register; the voltage value in a second register; and merge the first and second registers to represent a concatenated address. **The**

concatenated address can be applied to the address of a memory to retrieve a corrective value from a corrective table. The corrective table can be generated by characterizing the integrated circuit. The characterization includes varying the voltage and temperature over a predetermined range. The method includes applying a corrective vector to a ring oscillator.

MTK-1006, 2:64-3:8.

To be able to adjust for voltage and temperature change at the same time, the two sensing methods are combined in FIG. 1. The temperature and voltage inputs to the A/D are switched to give an alternate readout of the A/D. When the Temperature is sampled by the A/D its value is stored in a register. Likewise, when the voltage is sampled by the A/D its value is stored in a holding register. **The two register values are combined to represent a concatenated address applied to the look-up table RAM or register File.**

Id. at 4:45-53.

The method of claim 15, further comprising **applying the concatenated address to the address of a memory to retrieve a corrective value from a corrective table.**

Id. at claim 16.

The method of claim 16, further comprising generating the **corrective table** by characterizing the integrated circuit.

Id. at claim 17. The combination of Norman '259 and Norman '851 also discloses that "[t]he table should produce a desired center frequency ..." *Id.* at 4:65-5:1.

182. Thus, a POSITA would have understood that the combination of Norman '259 and Norman '851 discloses: (1) measuring voltage and temperature; (2) merging the voltage and temperature values to represent a concatenated address; and (3) using the concatenated address to retrieve a corrective value from a corrective table, i.e., a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage, wherein the table produces a desired frequency. *Id.* at 2:64-3:8, 4:65-5:1.

15. Claim 23

(a) Element 23[p]

183. The preamble of claim 23 recites: “[a] system for circuit control.” The combination of Norman '259 and Norman '851 provides the preamble of claim 23 for at least the reasons discussed above with respect to claim elements 1[p] through 1[c], my discussions for which I incorporate herein by reference.

(b) Element 23[a]

184. Claim element 23[a] recites: “at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit.” The combination of Norman '259 and Norman '851 provides claim element 23[a] for at least the reasons discussed above with respect to claim element 1[a], my analysis for which I incorporate herein by reference.

185. As discussed above, Norman '851 states that details of “the device that corrects ... voltage variations are discussed in” the application that led to Norman

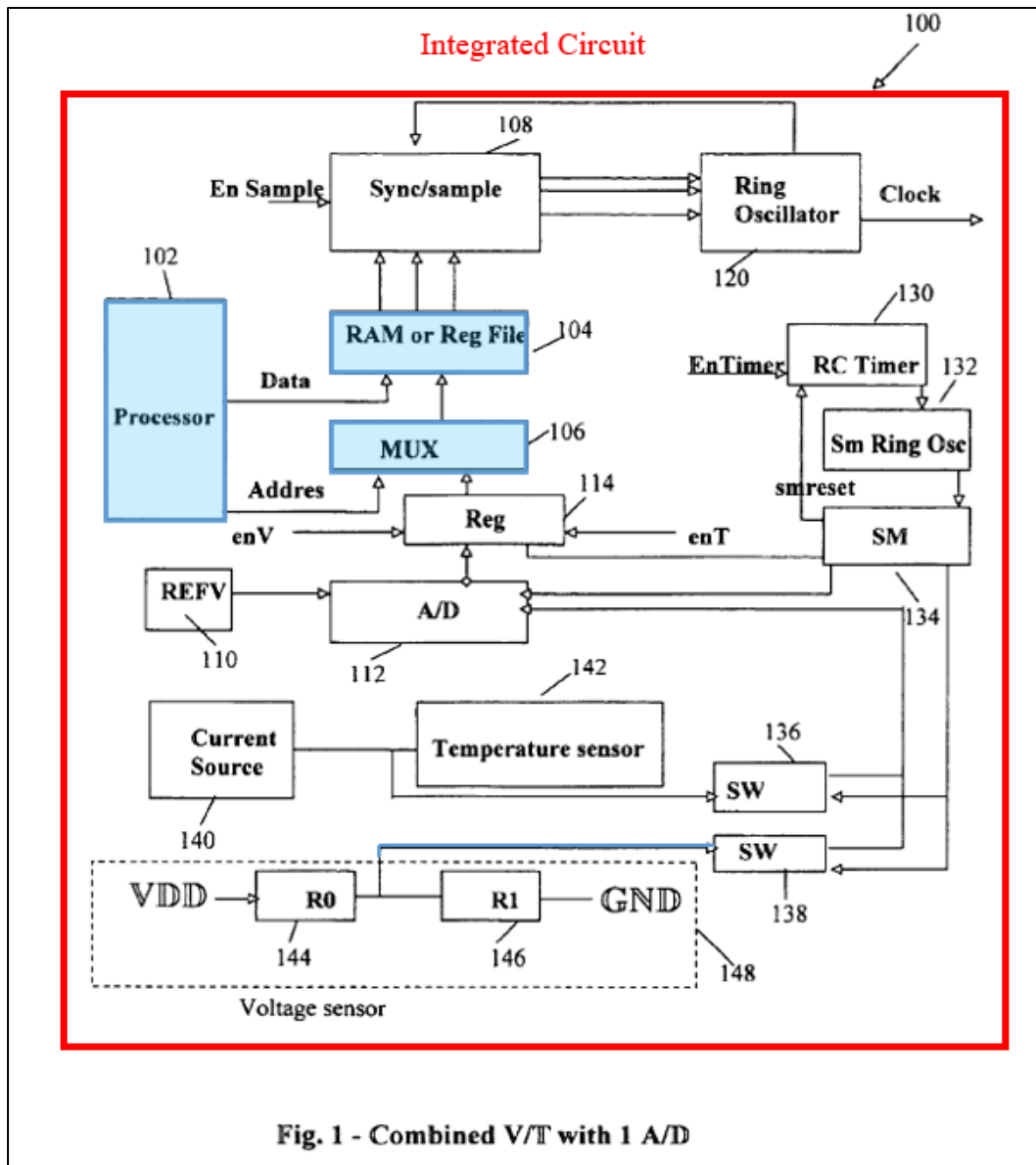
'259, which Norman '851 “incorporate[s] by reference.” MTK-1007, [0024] (incorporating application “entitled ‘Ring Oscillator Dynamic Adjustments for Auto-calibration’ by reference). Norman '259, in turn, discloses “a method for dynamically adjusting for ... voltage variations on an integrated circuit” that includes “periodically sensing the voltage” values using a voltage sensor. MTK-1006, 2:58-62; *id.* at 2:28-30 (an apparatus for “compensat[ing] for voltage ... variations on an integrated circuit includes: a voltage sensor”), FIG. 1 (depicting voltage sensor 148 located at a portion of integrated circuit 100). Moreover, as previously noted, it would have been obvious to a POSITA, based on Norman '851, to include voltage sensors, like Norman '259's, at various “predetermined locations in the IC [integrated circuit],” i.e., portions of the integrated circuit, “to sense environmental variations,” such as variations in “supply voltage,” at those locations. MTK-1007, [0019], [0023]-[0024], [0026] (“the voltage sensors are monitored”).

(c) Element 23[b]

186. Claim element 23[b] recites: “at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit.” The combination of Norman '259 and Norman '851 provides claim element 23[b] for at least the reasons discussed above with respect to claim element 1[b], my analysis for which I incorporate herein by reference.

187. Moreover, combination of Norman '259 and Norman '851 discloses at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit. Specifically, it teaches that after sensing voltage and temperature values, those values are applied to the ADC 112, and the “output of the ADC 112 is registered and applied to the multiplexor 106,” which is driven by an address from the processor 102.” MTK-1006, 4:15-20. “The output of the multiplexor 106 is applied to the memory 104 as the address input” and, “[a]t initialization, the processor 102 writes adjustment values into the RAM or Register File 104,” and the “output of the RAM 104 ... acts as the adjustment vector that is applied to the ring oscillator 120” to “select[] the ring frequency.” MTK-1006, 4:20-29.

188. Based on the foregoing, a POSITA would have understood that the multiplexor provides the RAM with an address input, its processor provides the RAM with adjustment values, and then the RAM uses the address input and adjustment values to determine the appropriate frequency for the portion of the integrated circuit using a lookup table. MTK-1006, 2:63-3:3, 4:64-5:1, claim 7. Thus, in my opinion, a POSITA would have understood that at least the processor 102, multiplexor 106, and RAM or Register File 104 (which are shown in blue in FIG. 1 of Norman '259 below) comprise, or consist of, logic blocks for determining the appropriate frequency for a portion of the integrated circuit.



MTK-1006, FIG. 1

(d) Element 23[c]

189. Claim element 23[c] recites: “at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.” The combination of Norman ’259 and Norman ’851 provides claim element 23[c] for at

least the reasons discussed above with respect to claim elements 1[b], 1[c], and 23[b], the analyses of which are incorporated herein by reference.

190. Moreover, the combination of Norman '259 and Norman '851 discloses at least one circuitry arrangement (including the sync/sample module 108 and the ring oscillator 120 depicted in blue in FIG. 1 of Norman '259 below) to provide the appropriate frequency (i.e., “clock”) to the portion of the integrated circuit:

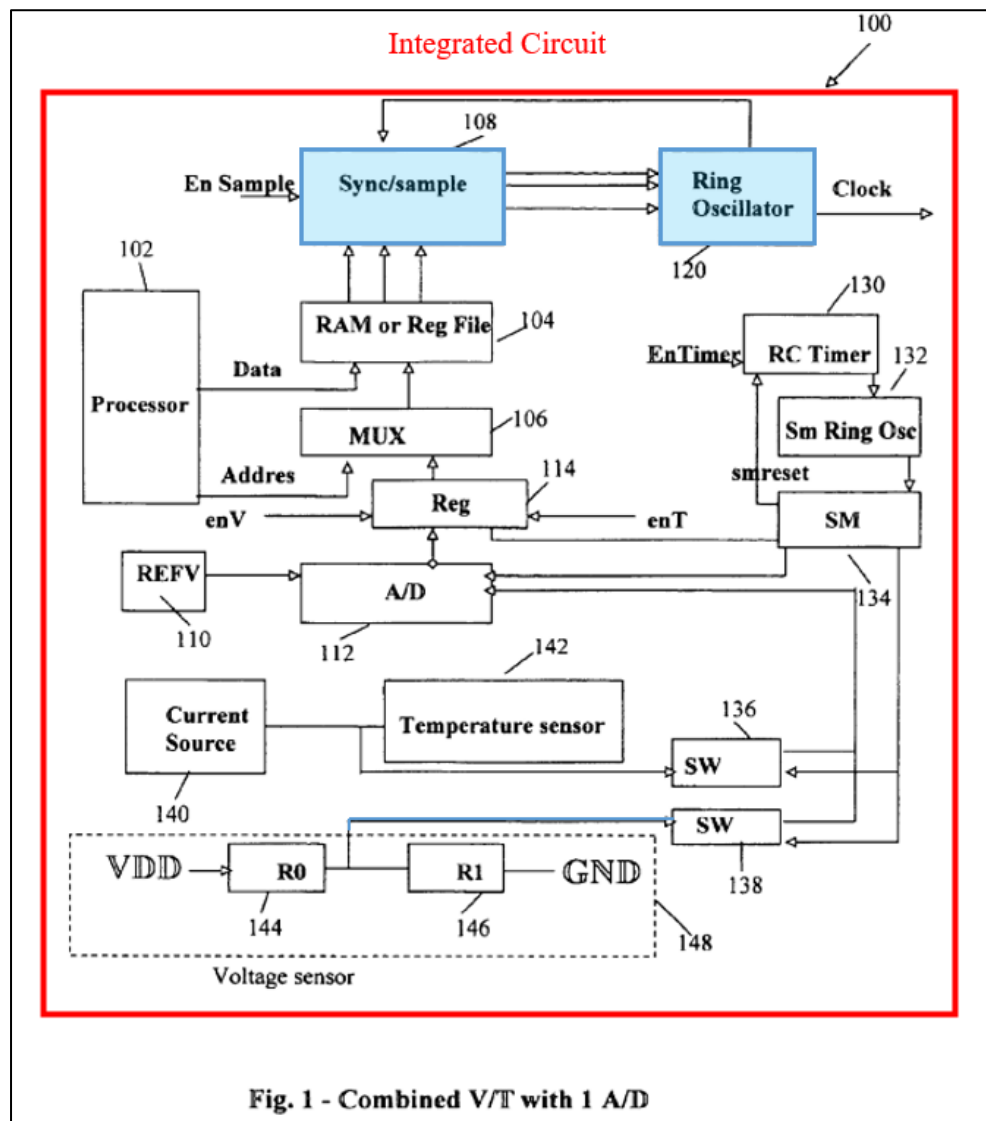


Fig. 1 - Combined V/T with 1 A/D

MTK-1006, FIG. 1. “The output of the memory or register file 104 drives a sync/sample module 108, which in turn drives a ring oscillator 102” that “generates a system clock[.]” MTK1006, 3:60-65. “Whenever a calibration sequence occurs the output of the memory [i.e., the corrective vector for the frequency] may change in value or remain the same. Whenever this sequence occurs the Sync/Sample has the job of determining if there is a new value or the same value exists... If there is a new vector the state machine will be activated[.]” MTK-1006, 6:10-18. “When the new vector is loaded the output will then drive the input to the ring oscillator[.]” *Id.* at 6:30-32.

191. The combination of Norman ’259 and Norman ’851 discloses that the ring oscillator “provides a plurality of clock signal signals, each of which can be used to clock a portion of the chip,” i.e., a portion of the integrated circuit, “to prevent clock degradation due to too much load on the chip.” MTK-1006, 6:67-7:3. Thus, a POSITA would have understood that at least the sync/sample module 108 and ring oscillator 120 comprise, or consist of, circuitry arrangements for providing the appropriate frequency, e.g., “clock,” to the portion of the integrated circuit.

16. Claim 24

192. Claim 24 recites: “[t]he system of claim 23, wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.” The combination of

Norman '259 and Norman '851 provides claim 24 for at least the reasons discussed above with respect to claim 3, the discussion of which I incorporate herein by reference.

17. Claims 31 and 32

193. Claim 31 recites: “[t]he system of claim 23 further comprising: a converter to convert the delivered voltage to a value.” Claim 32 recites: “[t]he system of claim 31 wherein the converter is an analog-to-digital converter.” The combination of Norman '259 and Norman '851 provides claims 31 and 32 for at least the reasons discussed above in the analysis of claim 10 with respect to the combination of Norman '259 and Norman '851.

18. Claim 33

194. Claim 33 recites: “[t]he system of claim 23 further comprising: a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.” The combination of Norman '259 and Norman '851 provides claim 33 for at least the reasons discussed above in the analysis of claim 11 with respect to the combination of Norman '259 and Norman '851.

19. Claim 34

195. Claim 34 recites: “[t]he system of claim 33 wherein said table is a computer readable database.” The combination of Norman '259 and Norman '851 provides claim 34 for at least the reasons discussed above in the analysis of claim 11 with respect to the combination of Norman '259 and Norman '851.

20. Claim 35

(a) Element 35[p]

196. The preamble of claim 35 recites: “[a] system for circuit control.” The combination of Norman ’259 and Norman ’851 provides the preamble of claim 35 for at least the reasons discussed above in the analysis of claim elements 1[p]-1[c] and 23[p]-23[c] with respect to the combination of Norman ’259 and Norman ’851.

(b) Element 35[a]

197. Claim element 35[a] recites: “a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit.” The combination of Norman ’259 and Norman ’851 provides claim element 35[a] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[a], 23[p], and 23[a] with respect to the combination of Norman ’259 and Norman ’851.

198. Specifically, as discussed above, Norman ’851 states that details of “the device that corrects ... voltage variations are discussed in” the application that led to Norman ’259, which Norman ’851 “incorporate[s] by reference.” MTK-1007, [0024] (incorporating application “entitled ‘Ring Oscillator Dynamic Adjustments for Auto-calibration’ by reference). Norman ’259, in turn, discloses “a method for dynamically adjusting for ... voltage variations on an integrated circuit” that includes “periodically sensing the voltage” values using a voltage sensor. MTK-1006, 2:58-62; *id.* at 2:28-30 (an apparatus for “compensat[ing] for voltage ... variations on an integrated circuit includes: a voltage sensor”), FIG. 1 (depicting

voltage sensor 148 located at a portion of integrated circuit 100). Moreover, as previously noted, it would have been obvious to a POSITA, based on Norman '851, to include voltage sensors, like Norman '259's, at various "predetermined locations in the IC [integrated circuit]," i.e., portions of the integrated circuit, "to sense environmental variations," such as variations in "supply voltage," at those locations. MTK-1007, [0019], [0023]-[0024], [0026] ("the voltage sensors are monitored").

(c) Element 35[b]

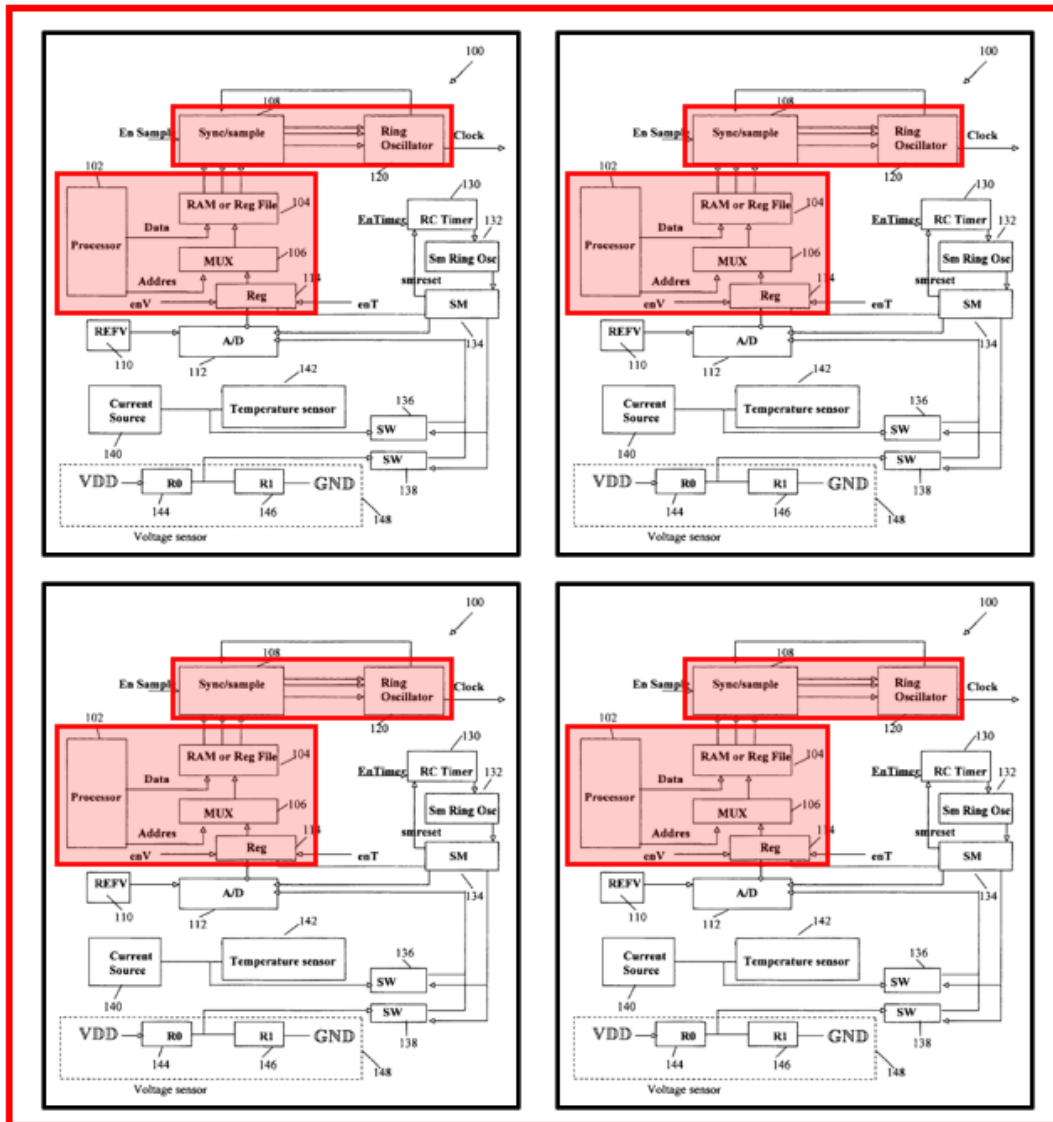
199. Claim element 35[b] recites: "a plurality of logic bocks arranged to determine an appropriate frequency for each said portion from said delivered voltages." The combination of Norman '259 and Norman '851 provides claim element 35[b] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], 23[p], and 23[b] with respect to the combination of Norman '259 and Norman '851.

200. First, as previously noted, the combination of Norman '259 and Norman '851 discloses: (1) employing multiple voltage sensors, (2) that its ring oscillator "provides a plurality of clock signal signals, each of which can be used to clock a portion of the chip," i.e., a portion of the integrated circuit, MTK-1006, 6:67-7:3, and (3) that its frequency adjustment mechanism could be applied to individual sub-systems located in the integrated circuit, MTK-1007, [0030] ("This process of calibration and correction can be conducted for each sub-system of the IC.").

201. Second, in my opinion, it would have been obvious to a POSITA to apply the teachings of the Norman '259 and Norman '851 combination to a number of known multiprocessor (or multi-core) integrated circuits, including very large-scale integration (i.e., VLSI) devices, multi-chip modules (i.e., MCMs), and multiprocessor systems on a chip (MPSoCs). *E.g.*, MTK-1001, 1:19-23 (VLSI); MTK-1009, 488; MTK-1010, 460, 833; MTK-1011, 223; MTK-1012, 22-4; MTK-1020, ¶¶6-17; MTK-1007, [0033] (“the invention is ... is capable of numerous rearrangements, modifications, and substitutions”).

202. Third, it would have been obvious to a POSITA that, in a multichip module, such as the one depicted below, logic on each chip (e.g., processor 102, multiplexor 106, and RAM or Register File 104), i.e., the plurality of logic blocks arranged to determine an appropriate frequency, would have determined new clock frequencies for each of the chips, i.e., each said portion of the integrated circuit, from the voltages delivered to each such chip and sensed by that chips' voltage sensors.

Plurality of logic blocks / circuitry arrangements



MTK-1006, FIG. 3 (potential multi-chip module)

(d) Element 35[c]

203. Claim element 35[c] recites: “a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.” The combination of Norman ’259 and Norman ’851 provides claim element 35[c] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], 1[c], 23[p],

23[b], 23[c], and 35[b] with respect to the combination of Norman '259 and Norman '851.

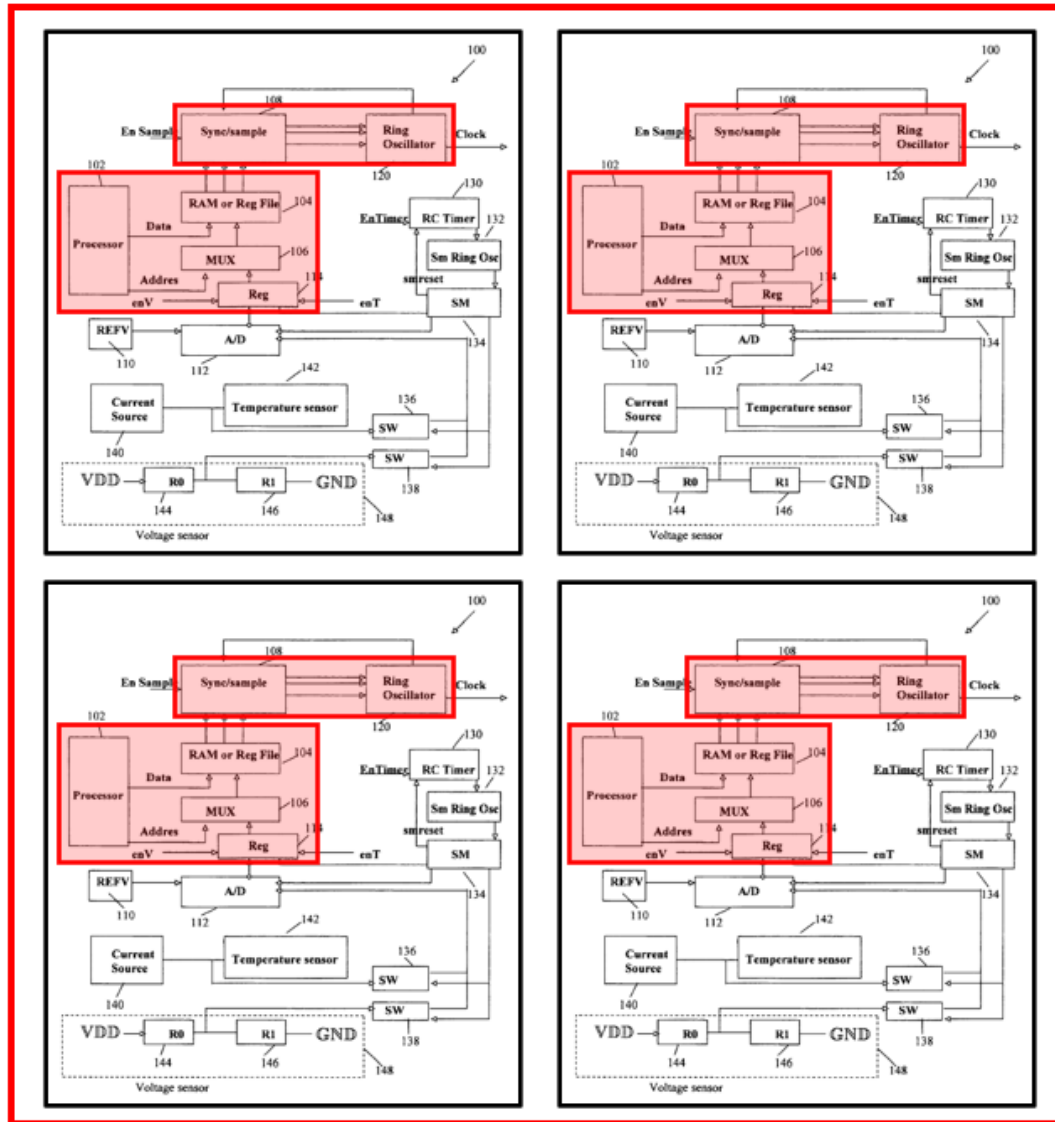
204. First, as previously noted, the combination of Norman '259 and Norman '851 discloses: (1) employing multiple voltage sensors, (2) that its ring oscillator “provides a plurality of clock signal signals, each of which can be used to clock a portion of the chip,” i.e., a portion of the integrated circuit, MTK-1006, 6:67-7:3, and (3) that its frequency adjustment mechanism could be applied to individual sub-systems located in the integrated circuit, MTK-1007, [0030] (“This process of calibration and correction can be conducted for each sub-system of the IC.”).

205. Second, in my opinion, it would have been obvious to a POSITA to apply the teachings of the Norman '259 and Norman '851 combination to a number of known multiprocessor (or multi-core) integrated circuits, including very large-scale integration (i.e., VLSI) devices, multi-chip modules (i.e., MCMs), and multiprocessor systems on a chip (MPSoCs). *E.g.*, MTK-1001, 1:19-23 (VLSI); MTK-1009, 488; MTK-1010, 460, 833; MTK-1011, 223; MTK-1012, 22-4; MTK-1020, ¶¶6-17; MTK-1007, [0033] (“the invention is ... is capable of numerous rearrangements, modifications, and substitutions”).

206. Third, it would have been obvious to a POSITA that, in a multichip module, such as the one depicted below, circuitry arrangements on each chip (e.g., sync/sample module 108 and ring oscillator 120), i.e., the plurality of circuitry

arrangements, would provide each chip in the MCM, i.e., each said portion of the integrated circuit, its associated appropriate frequency.

Plurality of logic blocks / circuitry arrangements



MTK-1006, FIG. 3 (potential multi-chip module)

D. Analysis of Naffziger '788 with respect to Claims 1, 3, 10, 23, 24, 31, 32, and 35

207. For the reasons articulated in detail below, and based on my review of the '563 patent and the Naffziger '788 reference, I am confident that a POSITA would have readily understood that Naffziger '788 renders obvious all elements of claims 1, 3, 10, 23-24, 31-32, and 35.

1. Overview of Naffziger '788

208. Naffziger '788, which shares an inventor with the '563 patent, relates “to a system and method that utilize an on-chip voltage controlled oscillator to dynamically generate an appropriate clock frequency for the chip based on the voltage being drawn by the chip.” MTK-1008, 1:16-21. Specifically, Naffziger '788 “is directed to a system and method which utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit. MTK-1008, 4:9-12; *see also id.* at 1:25 (noting that “[i]ntegrated circuits” are “commonly referred to as ‘chips’”).

209. According to Naffziger '788, “the voltage controlled oscillator of a most preferred embodiment is controlled by the same voltage as the core of the chip (e.g., the microprocessor), and therefore upon a voltage droop occurring in the core circuitry of the chip, the voltage droop is also received by the oscillator, resulting in the oscillator decreasing its output frequency.” *Id.* at 4:31-39. In one “alternative embodiment, a sensor (e.g., a thermal or voltage sensor) is utilized.” *Id.* at 4:47-48. “[I]n this alternative embodiment,” which is depicted in FIG. 2 below, “sensor(s),

FIG. 2 is a block diagram of a power supply system for a chip. The system includes a power supply (102) connected to a package (104). The package (104) contains package parasitics and a bypass capacitor. The package (104) is connected to a chip (106). The chip (106) includes a core chip circuitry (112) and an adjustable delay matching chip paths (110). The chip (106) is connected to a filtered voltage source (V_FILTERED) and a ground (GND). The chip (106) also includes a current source (I_c) and a capacitor (201). The chip (106) is connected to a clock signal (CLK₁) and a ground (GND).

210. Like the '563 patent, Naffziger '788 claims embodiments that: (1) sense a delivered voltage to a portion of an integrated circuit; (2) determine an appropriate

frequency for the portion of the integrated circuit; and (3) provide the appropriate frequency to the portion of the integrated circuit. For example:

1. A method for managing power consumption on an integrated circuit, said method comprising:

supplying voltage to said integrated circuit;

utilizing an oscillator included on said integrated circuit to generate a clock signal to be utilized by said integrated circuit; and

dynamically adjusting the clock signal's frequency in response to changes in voltage supplied to said integrated circuit to manage power consumption of said integrated circuit.

MTK-1008, claim 1.

15. An integrated circuit comprising:

core circuitry; and

oscillator that outputs a clock signal that is utilized for timing purposes by said core circuitry, wherein said clock signal is dynamically adjustable to manage power consumption of said integrated circuit.

Id. at claim 15.

24. A system comprising:

integrated circuit that includes an oscillator and core circuitry;

power supply for supplying voltage to said integrated circuit; and

wherein said oscillator outputs a clock frequency that is utilized by said core circuitry, and wherein said oscillator is operable to dynamically adjust said clock frequency responsive to voltage being consumed by said integrated circuit to manage power consumption of said integrated circuit.

Id. at claim 24. Moreover, Naffziger '788 claims embodiments whereby the frequency is increased or decreased in response to a respective increase or decrease in the voltage supplied to the integrated circuit:

4. The method of claim 1 wherein said dynamically adjusting the clock signal's frequency in response to changes in voltage required by said integrated circuit includes:

decreasing said clock signal's frequency in response to a decrease in said voltage supplied to said integrated circuit.

Id. at claim 4.

6. The method of claim 1 wherein said dynamically adjusting the clock signal's frequency in response to changes in voltage supplied to said integrated circuit includes:

increasing said clock signal's frequency in response to an increase in said voltage supplied to said integrated circuit.

Id. at claim 6.

2. Claim 1

(a) Element 1[p]

211. The preamble of claim 1 recites: “[a] method of circuit control.” Naffziger ’788 provides the preamble of claim 1. For example, Naffziger ’788 discloses a “method” which “utilize[s] an on-chip oscillator to provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit, “based on the voltage supplied to such oscillator to effectively manage the chip’s power consumption”:

A system and method are disclosed which utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip to manage power consumption by the chip. More specifically, in a preferred embodiment of the present invention, **an on-chip oscillator is utilized to provide the clock frequency for the chip's core circuitry, and such oscillator can dynamically adjust such clock frequency to manage the chip's power consumption.** Thus, such on-chip oscillator generates the processor clock instead of the usual synchronous, externally controlled clock generator. **A preferred embodiment of the present invention utilizes a voltage controlled frequency oscillator to control the chip's clock frequency in order to dynamically manage power consumption by the chip. Such oscillator is preferably operable to adjust its output frequency based on the voltage supplied to such oscillator to effectively manage the chip's power consumption.**

MTK-1008, Abstract.

This invention relates in general to **management of power consumption by an integrated circuit**, and in specific to a system and method that utilize an on-chip voltage controlled oscillator to dynamically **generate an appropriate clock frequency for the chip based on the voltage being drawn by the chip.**

Id. at 1:16-21.

FIG. 1 shows a preferred embodiment of the present invention which utilizes an on-chip voltage controlled oscillator to **dynamically adjust the frequency of the chip's clock to manage the power consumption of the chip;**

FIG. 2 shows an alternative embodiment of the present invention which includes **circuitry for controlling the voltage input to the on-chip voltage controlled oscillator to allow for the frequency of the chip's clock output by such oscillator to be controlled in a desired manner[.]**

Id. at 3:62-4:3; *see also id.* at 4:9-5:10, 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3.

212. Naffziger '788 even claims a method embodiment of the invention that comprises: [1] supplying voltage to said integrated circuit; [2] utilizing an oscillator included on said integrated circuit to generate a clock signal to be utilized by said

integrated circuit; and [3] dynamically adjusting the clock signal's frequency in response to changes in voltage supplied to said integrated circuit”:

1. A method for managing power consumption on an integrated circuit, said method comprising:

supplying voltage to said integrated circuit;

utilizing an oscillator included on said integrated circuit to generate a clock signal to be utilized by said integrated circuit; and

dynamically adjusting the clock signal's frequency in response to changes in voltage supplied to said integrated circuit to manage power consumption of said integrated circuit.

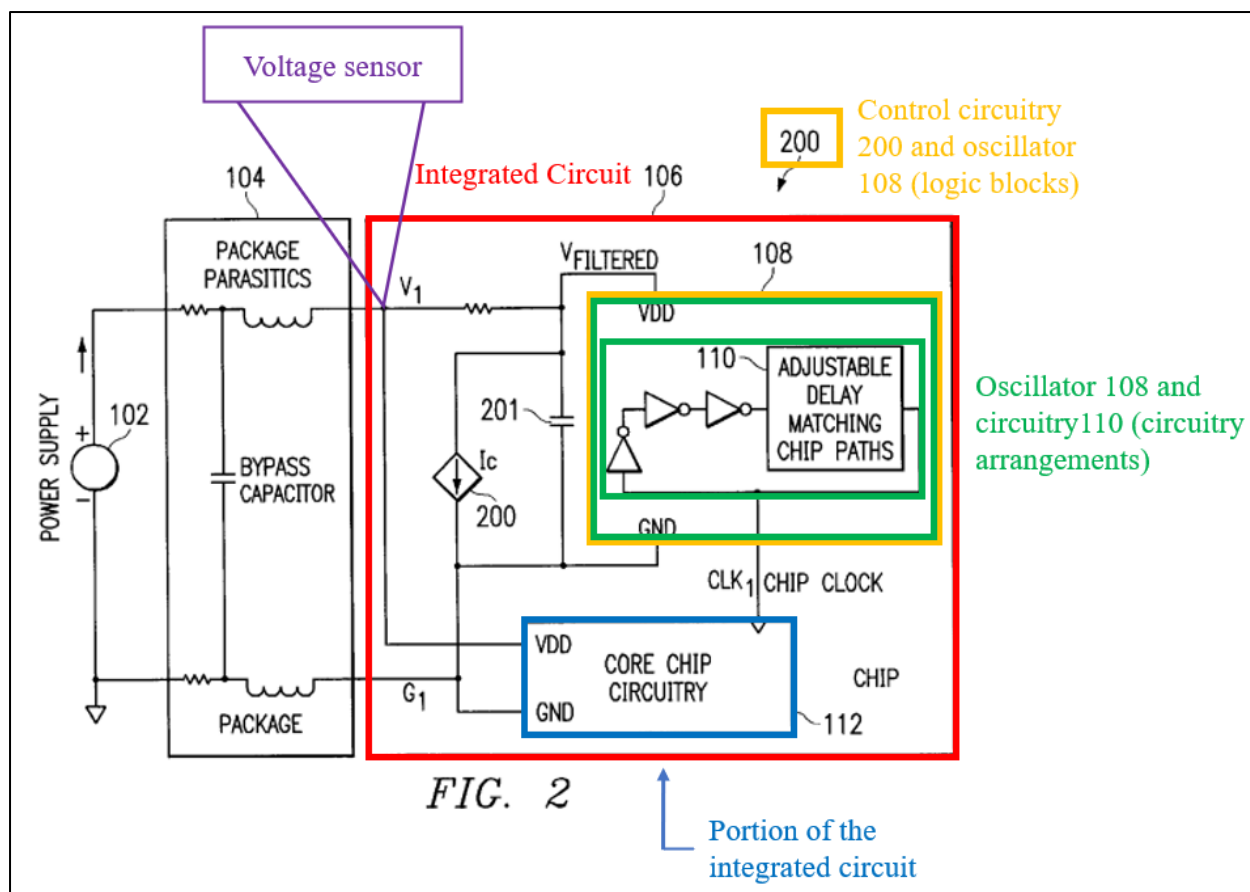
MTK-1008, claim 1. In my opinion, claim 1 of Naffziger '788, alone, renders obvious at least dependent claims 1, 23, and 35 of the '563 patent for the reasons discussed below because it, among other things, teaches sensing a delivered voltage and determining/providing an appropriate frequency for a portion of an integrated circuit in response to changes in the delivered supply voltage. *Id.*

(b) Element 1[a]

213. Claim element 1[a] recites: “sensing a delivered voltage to a portion of an integrated circuit.” Naffziger '788 provides claim element 1[a]. *See* MTK-1008, Abstract, 1:16-21, 3:62-4:3, 4:9-5:10, 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3. For example, Naffziger '788 discloses one embodiment that utilizes

“sensor(s), such as a voltage sensor,” “to monitor [i.e., sense] the voltage level drawn by core circuitry 112,” i.e., a portion of the integrated circuit. MTK-1008, 7:13-16; *id.* at 7:28-30 (“circuitry (e.g., sensors) may be included for monitoring the value of voltage V_1 ”).

214. The “circuitry,” i.e., voltage sensors, “that monitors the value of the voltage V_1 input to chip 106” is “not shown” in any figures. MTK-1008, 7:35-36 (noting that the “circuitry . . . that monitors the value of the voltage V_1 input to chip 106” is “not shown”). However, in my opinion, it would have been obvious to a POSITA to include the voltage sensor(s) (purple) in chip 106 (red) of at least the embodiment shown in FIG. 2 below, to sense the delivered voltage V_1 being delivered to core chip circuitry 112 (blue), which a POSITA would have further understood represents a portion of the integrated circuit:



MTK-1008, FIG. 2

(c) Element 1[b]

215. Claim element 1[b] recites: “determining an appropriate frequency for the portion of the integrated circuit.” Naffziger ’788 provides claim element 1[b]. MTK-1008, Abstract, 1:16-21, 3:62-4:3, 4:9-5:10, 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3.

216. For example, Naffziger ’788 discloses “[a] system and method . . . which utilize an on-chip oscillator” to determine and “provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit:

A system and method are disclosed which utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip to manage power consumption by the chip. More specifically, in a preferred embodiment of the present invention, an on-chip oscillator is utilized to provide the clock frequency for the chip's core circuitry, and such oscillator can dynamically adjust such clock frequency to manage the chip's power consumption. Thus, such on-chip oscillator generates the processor clock instead of the usual synchronous, externally controlled clock generator. A preferred embodiment of the present invention utilizes a voltage controlled frequency oscillator to control the chip's clock frequency in order to dynamically manage power consumption by the chip. Such oscillator is preferably operable to adjust its output frequency based on the voltage supplied to such oscillator to effectively manage the chip's power consumption.

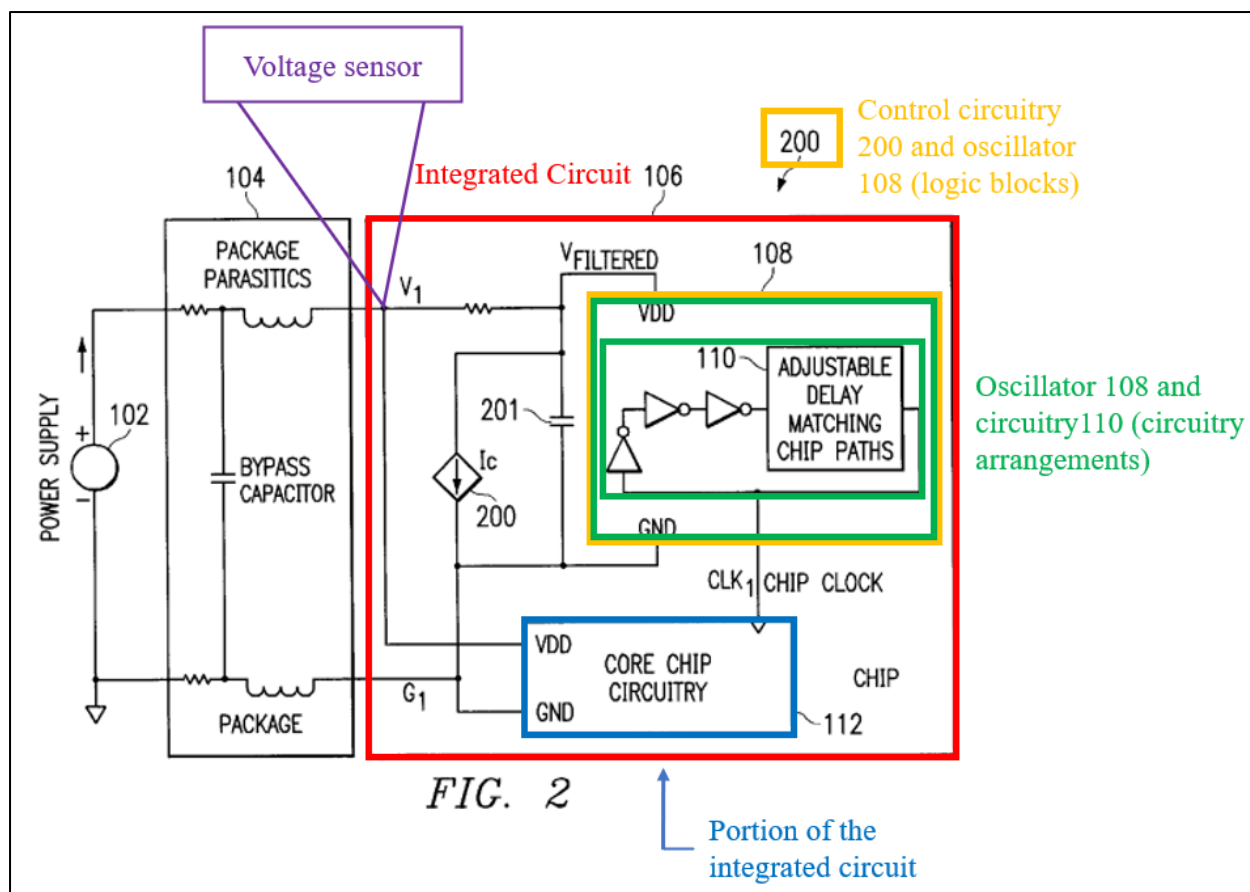
MTK-1008, Abstract. Specifically, Naffziger '788 discloses utilizing “an on-chip oscillator” that “can dynamically adjust ... clock frequency,” i.e., determine the appropriate frequency, and “provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit. MTK-1008, 4:9-17.

217. According to Naffziger '788:

[S]ensor(s), such as a voltage sensor ..., may be utilized to monitor the voltage level drawn by core circuitry 112, and may communicate such voltage level to control circuitry 200. In turn, control circuitry 200 may control the voltage

input to oscillator 108, thereby dynamically controlling the output frequency of oscillator 108 (i.e., the frequency of CLK) to manage the chip's power consumption.

MTK-1008, 7:9-20; *id.* at 4:47-56. Thus, in my opinion, it would have been obvious to a POSITA to: (1) monitor a voltage delivered to a component of the chip, i.e., a portion of the integrated circuit, such as core chip circuitry 112 (in blue below), using one or more voltage sensors (in purple below); (2) determine the “appropriate frequency” for the component using oscillator 108 and control circuitry 200, i.e., logic blocks (in yellow below); and (3) provide the appropriate frequency, e.g., CLK₁, to the component using clock oscillator 108 and circuitry 110, i.e., circuitry arrangements (in green below).



MTK-1008, FIG. 2

(d) Element 1[c]

218. Claim element 1[c] recites: “providing the appropriate frequency to said portion of said integrated circuit.” Naffziger ’788 provides claim element 1[c] for at least the reasons discussed above with respect to claim element 1[b], the analysis of which I incorporate herein by reference. *See also* MTK-1008, Abstract (disclosing a “system and method ... which utilize an on-chip oscillator **to provide the appropriate clock frequency for components of the chip,**” i.e., portions of the integrated circuit), 1:16-21, 3:62-4:3, 4:9-5:10 (“The present invention is

directed to a system and method which utilize an on-chip oscillator **to provide the appropriate clock frequency for components of the chip...**”), 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3.

3. Claim 3

219. Claim 3 recites: “[t]he method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.” Naffziger ’788 provides claim 3. For example, Naffziger ’788 discloses an embodiment that “allows for operation at the highest processing speed (*or fastest clock frequency*) that is possible,” i.e., maximum frequency possible, “while remaining within a desired power consumption.” MTK-1008, 8:61-64. Indeed, according to Naffziger ’788, “the chip’s clock frequency supplied by on-chip oscillator 108 can dynamically adjust such that it is consistently at the *fastest frequency possible* to remain within the desired power consumption” at the delivered voltage. *Id.* at 8:64-67; *id.* at 8:54-58 (“[A] preferred embodiment utilizes on-chip oscillator 108 to dynamically generate clock frequency CLK₁ for the core circuitry 112 of chip 106 responsive to Voltage V₁ in order to manage the power consumption of chip 106.”).

4. Claim 10

220. Claim 10 recites: “[t]he method of claim 1 further comprising: calculating a value for the delivered voltage.” Naffziger ’788 provides claim 10.

For example, the '563 patent notes that “an analog to digital converter” (an “A/D converter”) may be used “to actually measure [i.e., calculate] the value of the delivered voltage.” MTK-1001, 5:49-51; *id.* at 5:55-57 (“This voltage is converted 602 to a numeric value, by a analog-to-digital converter for example.”). It would have been obvious to a POSITA, in view of Naffziger '788, to use an A/D converter to calculate a value for the delivered voltage.

221. For example, Naffziger '788 incorporates the disclosure of U.S. patent application Ser. No. 09/811,243, filed Mar. 16, 2001, by reference. MTK-1008, 1:8-13. That application issued as U.S. Patent No. 6,489,834 to Naffziger et al. (“Naffziger '834”) on December 3, 2002. MTK-1014. Naffziger '834, in turn, discloses a “voltage comparator,” i.e., a voltage sensor, comprising “an analog to digital converter.” MTK-1014, 4:46-48, 5:15-17, 7:26-34, 7:56-58 (“an A/D converter may be utilized to convert the analog voltage signal to a digital signal”). In my opinion, because Naffziger '788 incorporates Naffziger '834's discussion of A/D converters by reference, it would have been obvious to a POSITA that Naffziger '788's voltage sensor could be an A/D converter that is used to calculate a digital value for the delivered voltage.

5. Claim 23

(a) Element 23[p]

222. The preamble of claim 23 recites: “[a] system for circuit control.” Naffziger ’788 provides the preamble of claim 23 for at least the reasons discussed above with respect to claim elements 1[p] through 1[c], my discussions for which I incorporate herein by reference.

(b) Element 23[a]

223. Claim element 23[a] recites: “at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit.” Naffziger ’788 provides claim element 23[a] for at least the reasons discussed above with respect to claim element 1[a], my analysis for which I incorporate herein by reference. For example, as discussed above, Naffziger ’788 discloses an embodiment that utilizes “sensor(s), such as a voltage sensor,” “to monitor [i.e., sense] the voltage level drawn by core circuitry 112,” i.e., a portion of the integrated circuit. MTK-1008, 7:13-16; *id.* at 7:28-30 (“sensors[] may be included for monitoring the value of voltage V_1 ”).

(c) Element 23[b]

224. Claim element 23[b] recites: “at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit.” Naffziger ’788 provides claim element 23[b] for at least the reasons discussed above with respect to claim element 1[b], my analysis for which I incorporate herein by reference. For example, as discussed above, Naffziger ’788 discloses utilizing “an on-chip oscillator” and “control circuitry,” i.e., logic blocks,

that “can dynamically adjust ... clock frequency,” i.e., determine the appropriate frequency, and “provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit. MTK-1008, 4:9-17, FIG. 2.

(d) Element 23[c]

225. Claim element 23[c] recites: “at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.” Naffziger ’788 provides claim element 23[c] for at least the reasons discussed above with respect to claim elements 1[b], 1[c], and 23[b], the analyses of which are incorporated herein by reference. For example, as discussed above, Naffziger ’788 discloses providing the appropriate frequency, e.g., CLK₁, to a component, i.e., a portion of the integrated circuit, using clock oscillator 108 and circuitry 110, i.e., circuitry arrangements. MTK-1008, Abstract (“system and method ... which utilize an on-chip oscillator **to provide the appropriate clock frequency for components of the chip,” i.e., portions of the integrated circuit**), 1:16-21, 3:62-4:3, 4:9-5:10 (“The present invention is directed to a system and method which utilize an on-chip oscillator **to provide the appropriate clock frequency for components of the chip...**”), 5:64-6:44, 6:45-7:45, 8:54-9:15, claims 1-29, FIGS. 1-3.

6. Claim 24

226. Claim 24 recites: “[t]he system of claim 23, wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the

portion of the integrated circuit at the delivered voltage.” Naffziger ’788 provides claim 24 for at least the reasons discussed above in the analysis of claim 3 with respect to Naffziger ’788, the discussion of which I incorporate herein by reference.

7. Claims 31 and 32

227. Claim 31 recites: “[t]he system of claim 23 further comprising: a converter to convert the delivered voltage to a value.” Claim 32 recites: “[t]he system of claim 31 wherein the converter is an analog-to-digital converter.” Naffziger ’788 provides claims 31 and 32 for at least the reasons discussed above in the analysis of claim 10 with respect to Naffziger ’788, the discussion of which I incorporate herein by reference.

8. Claim 35

(a) Element 35[p]

228. The preamble of claim 35 recites: “[a] system for circuit control.” Naffziger ’788 provides the preamble of claim 35 for at least the reasons discussed above in the analysis of claim elements 1[p]-1[c] and 23[p]-23[c] with respect to Naffziger ’788.

(b) Element 35[a]

229. Claim element 35[a] recites: “a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit.” Naffziger ’788 provides claim element 35[a] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[a], 23[p], and 23[a] with respect to Naffziger ’788.

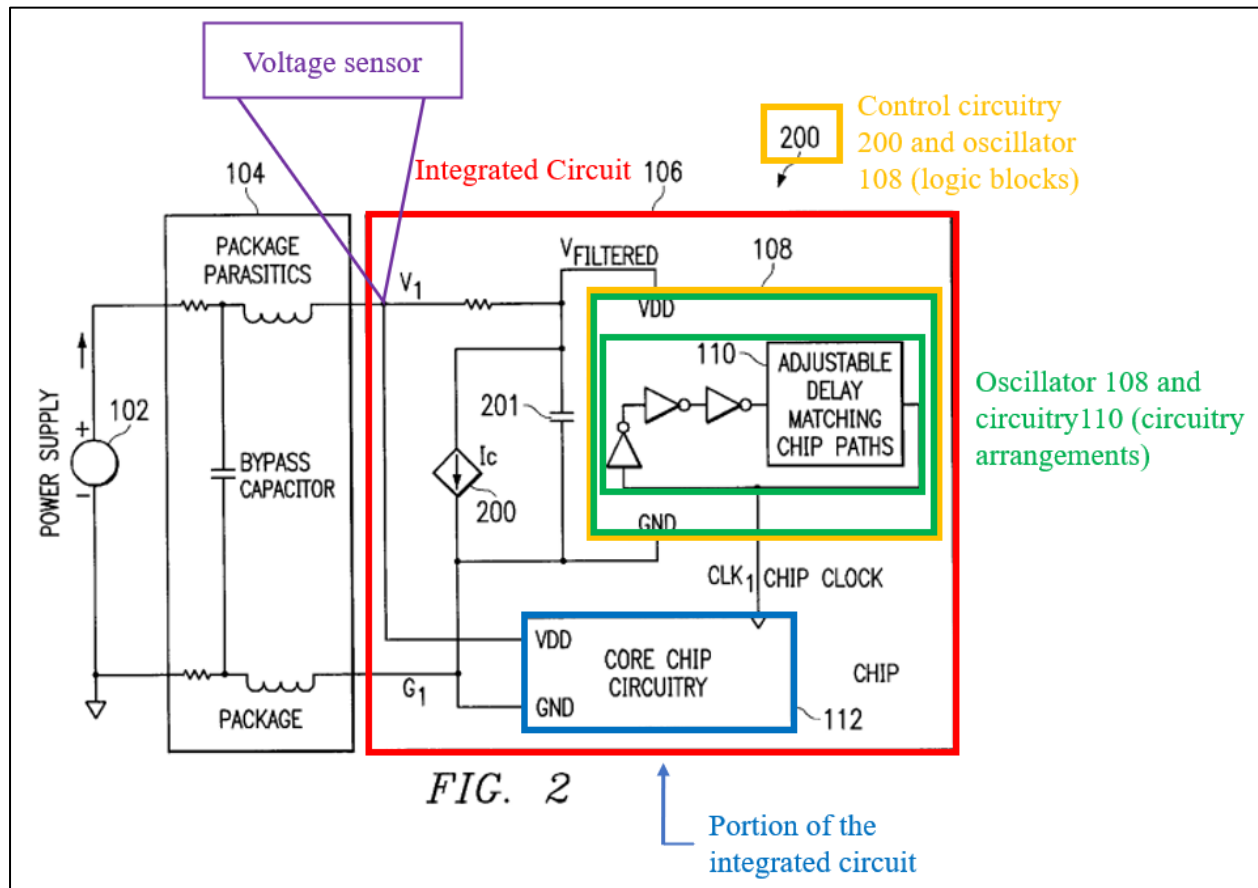
230. For example, Naffziger '788 discloses utilizing a plurality of “sensor(s), such as a voltage sensor,” “to monitor [i.e., sense] the voltage level drawn by core circuitry 112,” i.e., a portion of the integrated circuit. MTK-1008, 7:13-16; *id.* at 7:28-30 (“sensors[] may be included for monitoring the value of voltage V_I”). Moreover, in my opinion, it would have been obvious to a POSITA, based on Naffziger '788, to utilize a plurality of voltage sensors for sensing delivered voltages to different portions of an integrated circuit, which Naffziger '788 refers to as different “components of the chip.” *See* MTK-1008, Abstract; *id.* at 4:9-12 (same). A POSITA would have understood that doing so could help “manage power consumption by the chip.” *Id.* at 4:9-12.

(c) Element 35[b]

231. Claim element 35[b] recites: “a plurality of logic blocks arranged to determine an appropriate frequency for each said portion from said delivered voltages.” Naffziger '788 provides claim element 35[b] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], 23[p], and 23[b] with respect to Naffziger '788.

232. Moreover, in my opinion, it would have been obvious to a POSITA, based on Naffziger '788, to include a plurality of logic blocks arranged to determine an appropriate frequency for each said portion of the integrated circuit (e.g., the various “components of the chip,” MTK-1008, Abstract, 4:9-12) from said delivered

voltages. For example, it would have been obvious to a POSITA that Naffziger '788's oscillator 108 and control circuitry 200 depicted in FIG. 2 below, comprise a plurality of logic blocks.



MTK-1008, FIG. 2

Indeed, Naffziger '788 discloses that control circuitry 200 could be “implemented on chip 106 with software [or firmware] executing thereon for managing the chip’s power consumption.” *Id.* at 7:20-23. A POSITA would have understood that the control circuitry 200 “may control the voltage input to oscillator 108, thereby

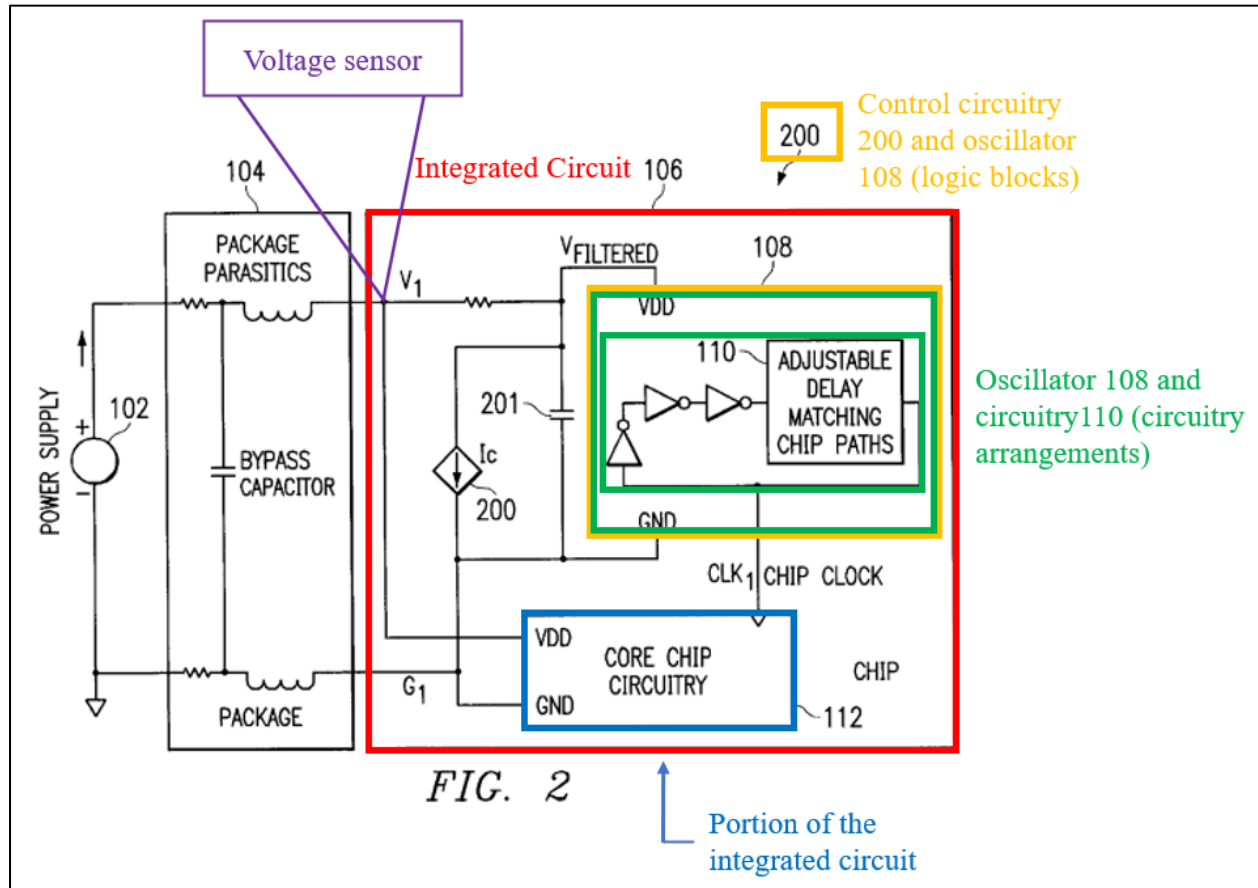
dynamically controlling the output frequency of oscillator 108” to the various components of the chip, i.e., portions of the integrated circuit. *Id.* at 7:16-20.

(d) Element 35[c]

233. Claim element 35[c] recites: “a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.” Naffziger ’788 provides claim element 35[c] for at least the reasons discussed above in the analysis of claim elements 1[p], 1[b], 1[c], 23[b], 23[c], and 35[b] with respect to Naffziger ’788, which I incorporate herein by reference.

234. For example, in my opinion, it would have been obvious to a POSITA, based on Naffziger ’788, to include a plurality of circuitry arrangements to provide each said portion of the integrated circuit (e.g., each of the various “components of the chip,” MTK-1008, Abstract, 4:9-12) its associated appropriate frequency. Indeed, Naffziger ’788 discloses that “circuitry 110, which is well known to those of ordinary skill in the art, is included in oscillator 108 to adjust the frequency of CLK based on the value of voltage V_1 .” MTK-1008, 6:24-27. According to Naffziger ’788, “[s]uch circuitry 110 may include any switched capacitive or resistive elements,” i.e., circuitry arrangements, “that effect the loop delay of ring oscillator 108,” and that such circuitry “are generally well known in the art[.]” *Id.* at 6:27-31. Thus, it would have been obvious to a POSITA, based on Naffziger ’788’s own express disclosures, that oscillator 108 and circuitry 110 (shown in FIG.

2 below) comprise a plurality of circuitry arrangements that are used to provide each component of the chip, i.e., each portion of the integrated circuit, its associated appropriate frequency. See MTK-1008, Abstract, 4:9-12, FIGS. 1-2.



MTK-1008, FIG. 2

IX. ADDITIONAL REMARKS

235. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

236. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: March 5, 2024

By: 

Paul Min, Ph.D.
St. Louis, Missouri

APPENDIX A

Paul S. Min, Ph.D.
Washington University in Saint Louis
(Webpage : <https://engineering.wustl.edu/faculty/Paul-Min.html>)

psm@wustl.edu
+1 (314) 853-6200 (phone)

Campus Box 1223
Academy Building Room 218A
St. Louis, MO 63130

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1987	The University of Michigan	Ph.D. in Electrical Engineering
1984	The University of Michigan	M.S. in Electrical Engineering
1982	The University of Michigan	B.S. in Electrical Engineering

Professional Experience

From: 1990
To: Present
Organization: Washington University, St. Louis

Summary:

2015 - Senior Professor - Department of Electrical Systems Engineering

2011 – 2014 Chair – Undergraduate Curriculum, Department of Electrical and Systems Engineering

2000 – 2002 Chair – Graduate Curriculum, Department of Electrical and Systems Engineering

2002 - 2014 Associate Professor - Department of Electrical and Systems Engineering

1997 - 2008 On leave from full-time duty at Washington University – as Presidents of MinMax Technologies and Erlang Technology.)

1996 - 2002 Associate Professor - Department of Electrical Engineering

1996 Promoted with Tenure

1990 - 1996 Assistant Professor - Department of Electrical Engineering

- Teaching Experience
- “Transmission System and Multiplexing,” Washington University, ESE 571
 - “Electrical Laboratory I,” Washington University, EE 250.
 - “Communication Theory,” Washington University, ESE 471.
 - “Reliability and Quality Control,” Washington University, ESE 405/505
 - “Signaling and Control of Communications Networks,” Washington University, ESE 572.
 - “Introduction to Electronic Circuits,” Washington University, ESE232
 - “Queueing Systems and Discrete Stochastic Processes,” Washington University, EE 536 / CS 567.
 - “Digital Computer,” Washington University, EE 260M / CS 260.
 - “Data Networks,” Washington University, EE 530.
 - “Electrical Circuit Analysis,” Washington University, ESE 230.
 - “Computer/Communications System Analysis I,” Washington University, EE 557/ CS 557.
 - “Computer/Communications System Analysis II,” Washington University, EE558 / CS 558.
 - “Digital Systems Laboratory,” Washington University, EE 455 / CS 455.

From: 1999
To: 2008
Organization: Erlang Technology, Inc., St. Louis, Missouri
Title: Founder and President
Summary: Up to 70 employees, \$40M in total capital raised from 5 VCs and 3 Corporations
Received “Product of Year” Award from Analog Zone Magazine in 2004

From: 1997
To: 1999
Organization: MinMax Technologies, Inc., St. Louis, Missouri
Title: Founder and President
Summary: Fabless semiconductor company, designing high performance switching ASICs

From: September 1987
To: August 1990
Organization: Bellcore, New Jersey
Title: Member of Technical Staff
Summary: Member of New Network Architecture Development Group

From: 1983
To: 1987

Organization: Department of Electrical Engineering, The University of Michigan
Title: Graduate Instructor
Summary: Instructor for senior level Electrical Engineering Laboratory Class. Received a Best “Best Graduate Instructor Award” from the Department of Electrical Engineering

Professional Affiliations, Achievements & Awards

- Technical Program Committee, COMCAS 2021, Tel Aviv, November 2021.
- Technical Program Committee, COMCAS 2019, Tel Aviv, November 2019.
- Technical Program Committee, COMCAS 2017, Tel Aviv, November 2017.
- Technical Program Committee, COMCAS 2015, Tel Aviv, October 2015.
- Past-Chair, Saint Louis Section of the Institute of Electrical and Electronics Engineers (IEEE), 2015.
- Member of Executive Committee, Saint Louis Section of the IEEE, 2010-2015.
- Chair, Saint Louis Section of the IEEE, 2014.
- Technical Program Committee, COMCAS 2013, Tel Aviv, October 2013.
- Vice Chair, Saint Louis Section of the IEEE, 2013
- Treasurer, Saint Louis Section of the IEEE, 2012.
- The Best Paper Award at MOBILITY 2011, October 2011, Barcelona, Spain.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2011.
- Award of Appreciation, Saint Louis Section of the Institute of Electrical and Electronics Engineers, 2011, for contribution to various activities of the Saint Louis Section the Institute of Electrical and Electronics Engineers.
- Secretary, Saint Louis Section of the IEEE, 2010.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2010.
- Wall Street Journal Businessmen of Year, 2003.
- American Men and Women of Science, listed in 1997.
- Member, Eta Kappa Nu (Honor Society for Electrical Engineers), inducted in 1992
- Outstanding Achievement Award, Bellcore, 1990.
- 18th ISATA Award of Technical Excellence, the best paper award at ISATA 1988.
- Rockwell Fellow, Rockwell International, 1985, 1986.
- Outstanding Graduate Student Award, the University of Michigan, 1985.
- Outstanding Teaching Award, the University of Michigan, 1984, 1986.
- Member of Honor's College, the University of Michigan, 1979, 1980.

- Honor's Convocation, the University of Michigan, 1979.
- Outstanding Freshman Award, the University of Michigan, 1979.
- Woodhaven Rotary Club Scholarship, Woodhaven Rotary Club, 1978.
- Second Place Winner, the State of Michigan Mathematics Prize Competition, 1977.
- International Program Committee, *IASTED International Conference on Communications, Internet and Information Technology (CIIT 2005)*, Cambridge, Massachusetts from October 31-November 2, 2005.
- International Program Committee, *IASTED International Conference on Communications 2003*, Scottsdale, Arizona, 2003.
- International Program Committee, *Wireless and Optical Communications 2003*, Banff, Canada, 2003.
- International Program Committee, Session Chair, *Wireless and Optical Communications 2002*, Banff, Canada, 2002.
- Invited participant, *NSF Workshop on Enhancing International Cooperation in CS/CE Research and Education*, Portland, 1997.
- Session Chair, *the 1993 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Member, Board of Editors, *Journal of Network and Systems Management*, 1996-1998.
- Program Committee, *International Symposium on Integrated Network Management*, San Diego, 1997.
- Guest Editor, *Journal of Network and Systems Management, Special Issue on Routing in Broadband Networks*, December 1995 and June 1996.
- Invited participant, *ARPA Workshop on Survivability of Large Scale Systems*, Washington D.C., 1996.
- Special Event Organizer, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Organizing Committee, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Local Arrangements Chair, *IEEE Information Theory Workshop on Information Theory Multiple Access and Queueing*, St. Louis, 1995.
- Chair, *Communications Chapter, St. Louis Section of the IEEE*, 1995.
- Participant, *IEEE Information Theory Workshop on Information Theory, Multiple Access and Queueing*, St. Louis, 1995.
- Participant, *ARPA/AFOSR Non-Linear Optics and Communication Workshop*, Denver, 1994.
- Participant, *CNRI Giga Bit Network Workshop*, Washington D.C., 1993.
- Participant, *IFIP/IEEE International Workshop on Distributed Systems*, New Jersey, 1993.
- Program Committee, *International Conference on Computer Communications and Networks*, San Diego, 1992.
- Session Chair, *ISMM International Conference*, New Orleans, 1990.
- Senior Member, *IEEE*.

- Member, *IEEE Committee on Network Operations and Management*.
- Member, *IEEE Committee on Computer Communications*.
- Registered Specialist, *Hong Kong Research Grant Council*.
- Reviewer, *IEEE Transactions on Communications*.
- Reviewer, *IEEE Transactions on Networking*.
- Reviewer, *IEEE Journal on Selected Areas in Communications*.
- Reviewer, *Journal of Network and Systems Management*.
- Reviewer, *Telecommunication Systems*.
- Reviewer, *Computers and Electrical Engineering*.
- Reviewer, *ETRI Journal*.
- Reviewer, *IEEE Transactions on Automatic Control*.
- Reviewer, *IEEE Communications*.
- Book Reviewer, *Prentice Hall*.
- Book Reviewer, *Morgan Kaufmann Publishers, Inc.*
- Book Reviewer, *Irwin Publishing Co.*

University Activities:

- Undergraduate Studies Committee, School of Engineering and Applied Science (2012 – Present)
- Faculty Advisor for IEEE Student Chapter (2009 – Present)
- Ambassador for McDonnell International Scholar Academy (2007 – 2013)
- Web Development Committee (2006 – 2008)
- University Judicial Board (1998 - 2000)
- Resource Generation Committee (1994 - 1995)
- Top 20 Committee (1992 - 1995)
- Telecommunications Committee, Chair (1991 - 1997)
- Library Planning Committee (1991 - 1992)
- Computer Engineering Committee (1990 - 1996)
- Communications Curriculum Committee (1990 - 1992)
- Resources Committee (1990 - 1992)

Patents

<u>Patent No.</u>	<u>Date</u>	<u>Title</u>
10,623,323	04/14/20	Network Devices and a Method for Signature Pattern Detection
10,284,476	05/07/19	Hierarchical Pattern Matching Devices and Methods

7,110,411	09/19/06	Method of and Apparatus for WFQ Scheduling Using a Plurality of Scheduling Queues to Provide Fairness, High Scalability, and Low Computational Complexity
7,106,738	09/12/06	Method of and Apparatus for High Speed Packet Switching Using Train Packet Queuing and Providing High Scalability
6,859,455	02/22/05	Method of and Apparatus for Building and Using Multi-Dimensional Index Trees for Multi-Dimensional Data Objects
6,614,789	09/02/03	Method of and Apparatus for Matching Strings of Different Lengths
6,359,885	3/19/02	Multi-Channel Packet Switching Apparatus Having Traffic Flow Controlling and Checking Functions
6,128,292	10/03/00	Packet Switching Apparatus with Multi-Channel and Multi-Cast Switching Functions and Packet Switching System Using the Same
5,788,161	12/13/98	Network Designer for Communication Networks
5,526,352	06/11/95	Integrable Low Complexity Multi-Channel Switch
5,440,549	08/08/95	Nonblocking Multi-Channel Switching with Multicasting Capability

Publications

- Yu, Qixiang, Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruders.” Proceedings of the APSIPA 2015 conference. December 16-19, 2015.
- Hung, C.P., and Min, P.S., “Simple Web Application Framework.” Submitted for publication in the IEEE Transactions on Cloud Computing.
- Luo, Z., and Min, P.S., “Parallel Implementation of Energy-Based Target Localization Methods in Wireless Sensor Networks.” Proceeding of the 2014 IEEE SOUTHEASTCON.
- Yu, Q., Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruder.” Proceeding of 2014 International Conference on Smart Computing (SMARTCOMP 2014).
- Luo, Z., and Min, P.S., “Survey of Target Localization Methods in Wireless Sensor Networks,” 19th IEEE International Conference on Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Deriving and Visualizing the Lower Bounds of Information Gain for Prefetch Systems,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Access LUT without CAM - Improved Pearson Hashing for Collision Reduction,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Luo, Z and Min, P.S., “Target Localization in Wireless Sensor Networks for Industrial Control with Selected Sensors.” International Journal of Distributed Sensor Networks, Volume 2013 (2013), Article ID 304631.
- Hung, C.P., and Min, P.S. “Performance Evaluation of Distributed Mobile Application Virtualization Services,” International Journal on Advances in Internet Technology, Vol. 5, no. 3&4, 2012, pp. 65-83.

- Hung, C.P. and Min, P.S., “Performance evaluation of distributed application virtualization services using the UMTS mobility model,” *MOBILITY 2011 The First International Conference on Mobile Services, Resources, and Users*, 23-29 Oct. 2011.
- Hung, C.P. and Min, P.S., “Service Area Optimization For Application Virtualization Using UMTS Mobility Model,” *International Conference on Internet Computing*, pp. 128-134, Las Vegas, July 18-21, 2011.
- Hung, C.P. and Min, P.S., “Application Virtualization Using UMTS Mobility Model,” *ICOMP'11*, September, 2011.
- Hung, C.P. and Min, P.S., “Infrastructure Arrangement for Application Virtualization Service,” the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 78-85, Rio de Janeiro, December 2010.
- Hung, C.P. and Min, P.S., “Probabilistic Approach to Network-Based Virtual Computing,” the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 117-124, Rio de Janeiro, December 2010.
- Shiravi, A. and Min, P. S., “On the Latency Bound of Proportional Nested-DRR with Credit Adjusting,” *2007 Workshop on High Performance Switching and Routing HPSR 2007*, July 2007.
- Shiravi, A. and Min, P. S., “LOOFA-PB: A Modified LOOFA Scheduler for Variable-Length Packet Switching,” *2007 IEEE International Conference on Communications (ICC 2007)*, Glasgow, June 2007.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Congestion Prediction of Self-Similar Network through Parameter Estimation,” *Proceedings of 2006 IEEE/IFIP Network Operations & Management Symposium*, April 2006, Vancouver.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Traffic Dispatching Algorithm in Three-Stage Switch,” *Proceedings of 5th International Conference on Networking*, April 2006, Mauritius.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Proportional Nested Deficit Round Robin with Credit Adjusting,” *Proceedings of 2nd Int'l Conf. on Quality of Service in Heterogeneous Wired/Wireless Networks (QShine 2005)*, Orlando, August 2005.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Proportional Nested Deficit Round Robin: Improving the Latency of Packet Scheduler with an $O(1)$ Complexity,” *Proceedings of International Workshop on Advanced Architectures and Algorithms for Internet Delivery and Applications (AAA-IDEA 2005)*, Orlando, June 2005
- Kim, Y. G., Shiravi, A., and Min, P. S., “Prediction-Based Routing through Least Cost Delay Constraint,” *Proceedings of IEEE IPDPS 2004*, Santa Fe, April 2004.
- Kim, Y. G. and Min, P. S., “On the Prediction of Average Queuing Delay with Self-Similar Traffic,” *Proceedings of IEEE GLOBECOM 2003*, San Francisco, December 2003.
- Hu, C., Saidi, H., Yan, P. Y., and Min, P.S., “A Protocol Independent Policier And Shaper Using Virtual Scheduling Algorithm,” *Proceedings of ICCAS 2002*.

- Hu, C., Saidi, H., and Min, P.S., “DB_WFQ: An Efficient Fair Queueing Using Binary Counter,” *Proceeding of Coins 2002*.
- Yoon, U. and Min, P.S., “Performance Analysis of Radio Link Control Mechanism in W-CDMA System”, IEEE VTC’01 Fall, October 2001, New Jersey
- Akl, B., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., “Multi-Cell CDMA Network Design,” *IEEE Transaction on Vehicular Technology*, Volume 50, No. 3, pp. 711-722, May 2001.
- Yoon, U., Park, S., Min, P.S., “Performance Analysis of Multiple Rejects ARQ at RLC (Radio Link Control) for Packet Data Service in W-CDMA System,” *IEEE Globecom*, November 2000, San Francisco.
- Yoon, U., Park, S., Min, P.S., “Performance Analysis of Multiple Rejects ARQ for RLC (Radio Link Control) in the Third Generation Wireless Communication,” *WCNC*, September 2000, Chicago.
- Yoon, U., Park, S., Min, P.S., “Network Architecture and Wireless Data Service Protocol based on Mobile IP toward the Third Generation Wireless Communication,” *3G Wireless*, June 2000, San Francisco, pp. 211-215
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Multi-Cell CDMA Network Design,” *IEEE International Conference on Communications*, June 2000.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “CDMA Network Design to Meet Non-uniform User Demand,” *International Teletraffic Congress*, March 2000.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “CDMA Network Design,” *IEEE Transactions on Vehicular Technology*.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Cell Placement in a CDMA Network,” *IEEE Wireless Communications and Networking Conference*, September 1999, Volume 2, pp. 903-907.
- R.G. Akl, M.V. Hegde, P.S. Min, “Effects of Call Arrival Rate and Mobility on Network Throughput in Multi-Cell CDMA,” *IEEE International Conference on Communications*, June 1999, Volume 3, pp. 1763-1767.
- Hegde, M.V., Schmid, O.A., Saidi, H., and Min, P.S., “Real-Time Adaptive Bandwidth Allocation for High-Speed ATM Switches,” accepted, *International Conference on Communications*, June 1999.
- Akl, B.G., Hegde, M.V., and Min, P.S., “Effects of Mobility on Network Throughput in Multicell CDMA Networks,” accepted, *International Conference on Communications*, June 1999.
- Akl, B.G., Hegde, M.V., Min, P.S., and Naraghi-Pour, M., “Flexible Allocation of Capacity in Multi-Cell CDMA Networks,” accepted, *Vehicular Technology Conference*, June 1999.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Flexible Allocation of Capacity in Multi-Cell CDMA Networks,” *IEEE Vehicular Technology Conference*, May 1999, Volume 2, pp. 1643-1647.

- Oh, M.S., and Min, P.S., "Reliability Analysis for One-Turn and Deflection Crossbar Architectures and Distributed Fault Recovery Scheme," *Proceedings of GLOBECOM 97*, Phoenix, November 1997.
- Kim, K.B., Yan, P.Y., Kim, K.S., Schmid, O., and Min, P.S., "A Growable ATM Switch with Embedded Multi-Channel Multicasting Property," *Proceedings of GLOBECOM 97*, pp. 222-226, Phoenix, November 1997.
- Kim, K.B., Yan, P.Y., Kim, K.S., Schmid, O., and Min, P.S., "MASCON: A Single IC Solution to ATM Multi-Channel Switching with Embedded Multicasting," *Proceedings of ISS 97*, pp. 451-458, Toronto, September 1997.
- Maunder, A.S., and Min, P.S., "Investigation of Rate Control in Routing Policies for B-ISDN Networks," *Proceedings of the 15th International Teletraffic Congress*, Washington D.C., June 1997.
- Yan, P.Y., Kim, K.B., Kim, K.S., and Min, P.S., "A Large Scale ATM Switch System Using Multi-Channel Switching Paradigm," *Proceedings of ATM Workshop*, Lisbon, Portugal, May 1997.
- Yan, P.Y., Kim, K.S., Min, P.S., and Hegde, M.V., "Multi-Channel Deflection Crossbar (MCDC): A VLSI Optimized Architecture for Multi-Channel ATM Switching," *Proceedings of IEEE INFOCOM 97*, Kobe, Japan, April 1997.
- Maunder, A., Rayes, A., and Min, P.S., "Analysis and Rate Controlling Link: Leaky Bucket with Finite Servers," *Proceedings of the 1997 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Shin, S.W., Min, P.S., and Kim, J.H., "Real Time Traffic Management System at Korean Mobile Telecom," *Proceedings of 19th Annual Pacific Telecommunications Conference*, pp. 113-121, Honolulu, Hawaii, January 1997.
- Min, P.S., Hegde, M.V., Chandra, A., and Maunder, A.S., "Analysis of Banyan Based Copy Networks with Internal Buffering," *Journal of High Speed Networks*, Volume 5, No. 3, pp. 259-275 November 1996.
- Vargas, C., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., "Shadow Prices for Least Loaded Routing and Aggregated Least Busy Alternate Routing," *IEEE Transactions on Networking*, Volume 4, No. 5, pp. 796-807, October 1996.
- Shin, S.W., Kwon, S.M., and Min, P.S., "Capacity Analysis of CDMA with Nonuniform Cell Loading and Sizes," *Proceedings of the 34th Annual Allerton Conference*, October 1996.
- Hegde, M.V., Min, P.S., and Sohraby, K., "Note from Guest Editors," *Journal of Network and Systems Management*, Volume 4, No. 2, pp. 101-102, June 1996.
- Rayes, A. and Min, P.S., "Application of Shadow Price in Capacity Expansion of State Dependent Routing," *Journal of Network Systems Management*, Volume 4, No. 1, pp. 71-93, March 1996.
- Min, P.S., "PCS Revolution in the United States," *Electronics News*, No. 2277, January 22, 1996. Translated and published in Korean.

- Hegde, M.V., Min, P.S., and Sohraby, K., "Guest Editorial," *Journal of Network and Systems Management*, Volume 3, No. 4, pp. 347-349, December 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Nonblocking Copy Networks in Multi-Channel Switching," *IEEE Transactions on Networking*, Volume 3, No. 6, pp. 857-871, December 1995.
- Rayes, A. and Min, P.S., "Capacity Expansion of Least Busy Alternate Routing with Shadow Price," *Proceedings of GLOBECOM 95*, Singapore, November 1995.
- Min, P.S., Hegde, M.V., Chandra, A., and Maunder, A., "Throughput and Delay for Copy Networks with Internal Buffers," *Proceedings of the 33rd Annual Allerton Conference*, October 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Fanout Splitting in Nonblocking Copy Networks with Shared Buffering," *Proceedings of the 33rd Annual Allerton Conference*, October 1995.
- Min, P.S., Hegde, M.V., and Rayes, A., "Estimation of Exogenous Traffic Based on Link Measurements in Circuit-Switched Networks," *IEEE Transactions on Communications*, Volume 43, No. 8, pp. 2381-2390, August 1995.
- Maunder, A., Rayes, A., and Min, P.S., "Analysis of Routing Policies in Broadband Networks." Invited paper. *Canadian Journal of Electrical and Computer Engineering*, Special Issue on Planning and Designing of Broadband Networks, Volume 20, No. 3, pp. 125-136, July 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Architecture and Performance of Nonblocking Copy Networks with Multi-Channel Switching," *Proceedings of APCC 95*, pp. 531-535, Osaka, Japan, June 1995.
- Saidi, H., Min, P.S., and Hegde, M.V., "A New Structural Property of Statistical Data Fork," *IEEE Transactions on Networking*, Volume 3, No. 3, pp. 289-298, June 1995.
- Min, P.S., Saidi, H., and Hegde, M.V., "A Nonblocking Architecture for Broadband Multi-Channel Switching," *IEEE Transactions on Networking*, Volume 3, No. 2, pp. 181-198, April 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Multi-Channel Copy Networks: Architecture, Performance Model, Fairness, and Cell Sequencing," *Proceedings of IEEE INFOCOM 95*, pp. 931-938, Boston, April 1995.
- Min, P.S., Hegde, M.V., and Chandra, A., "Analysis of Packet Movements in Internally Buffered Copy Networks," *Third ORSA Telecommunications Conference*, p. 141, Boca Raton, Florida, March 1995.
- Maunder, A. and Min, P.S., "Routing for Multi-Rate Traffic with Multiple Qualities of Service," *Proceedings of the Third International Conference on Computer Communications and Networks*, pp. 104-108, San Francisco, September 1994.
- Saidi, H. and Min, P.S., "Performance Benefits of Multi-Channel Switching," *Proceedings of the 32nd Annual Allerton Conference*, pp. 583-592, September 1994.
- Min, P.S., "Book Review: 'Telecommunications Network Management into the 21st Century'," *IEEE Communications*, Volume 32, No. 7, pp. 5-8, July 1994.

- Saidi, H., Min, P.S., and Hegde, M.V., "Guaranteed Cell Sequence in Nonblocking Multi-Channel Switching," *Proceedings of IEEE INFOCOM 94*, Toronto, pp. 1420-1427, June 1994.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Shared Buffering in Nonblocking Copy Networks," *Proceedings of the 1994 IEEE International Symposium on Information Theory*, Norway, p. 406, June 1994.
- Min, P.S., Hegde, M.V., and Rayes, A., "Real Time Traffic Estimation in Circuit-Switched Networks," *Proceedings of the 14th International Teletraffic Congress*, France, pp. 1175-1184, June 1994.
- Hegde, M.V., Min, P.S., and Rayes, A., "State Dependent Routing: Traffic Dynamics and Performance Benefits," *Journal of Network and Systems Management*, Volume 2, No. 2, pp. 125-149, June 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Control of Packet Flow in Statistical Data Forks," *Proceedings of the 1994 International Conference on Communications*, New Orleans, pp. 415-419, May 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Nonblocking Multi-Channel Switching in ATM Networks," *Proceedings of the 1994 International Conference on Communications*, New Orleans, pp. 701-705, May 1994.
- Maunder, A. and Min, P.S., "Analysis and Development of Routing Schemes for Multi-Rate, Multi-Point Traffic," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 1041-1046, March 1994.
- Min, P.S., Hegde, M.V., and Chandra A., "Internal Buffering in Banyan-Based Copy Networks," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 209-214, March 1994.
- Rayes, A. and Min, P.S., "Capacity Expansion in State Dependent Routing Schemes," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 237-241, March 1994.
- Vargas, C., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., "Shadow Prices for State Dependent Routing," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 243-248, March 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Non-Blocking Multi-Channel Switching." Invited paper. *Proceedings of the 31st Annual Allerton Conference*, pp. 335-344, September 1993.
- Min, P.S., Hegde, M.V., and Rayes, A., "Model Based Estimation of Exogenous Traffic," *Proceedings of the 1993 Conference on Information Sciences and Systems*, Baltimore, pp. 126-131, March 1993.
- Hegde, M.V., Min, P.S., and Rayes, A., "Performance Analysis of State Dependent Routing," *Proceedings of the 1993 Conference on Information Sciences and Systems*, pp. 695-700, Baltimore, March 1993.
- Hegde, M.V. and Min, P.S., "Telephone Networks," Magill Survey of Science Applied Science, Salem Press, pp. 2624-2630, 1992.

- Saidi, H., Min, P.S., and Hegde, M.V., "Assignment of 2^k Trunk Groups in Multi-Channel Switches Using Generalized Binary Addresses," *Proceedings of the 30th Annual Allerton Conference*, pp. 652-661, September 1992.
- Hegde, M.V. and Min, P.S., "Performance Analysis of State Dependent Routing." Invited paper. *Second ORSA Telecommunications Conference*, Boca Raton, Florida, February 1992.
- Rizzoni, R. and Min, P.S., "Detection of Sensor Failures in Automotive Engines," *IEEE Transactions on Vehicular Technology*, Volume 40, No. 2, pp. 487-500, May 1991.
- Min, P.S. and Hegde, M.V., "End-to-End Planning Models for Optimal Evolution of Telecommunications Network," *Proceedings of IEEE INFOCOM 90*, San Francisco, pp. 200-206, June 1990.
- Min, P.S., "Validation of Controller Inputs in Electronically Controlled Engines." Invited paper. *Proceedings of the 1990 American Control Conference*, pp.2887-2890, San Diego, May 1990.
- Min, P.S. and Youn, C., "Generic Equipment Models (GEM) for Consistent Planning of Telecommunications Networks," *Proceedings of the 1990 ISMM International Conference*, New Orleans, pp. 190-194, March 1990.
- Min, P.S., "Robust Application of Beard-Jones Detection Filter," *Advances in Computing and Control*, Springer-Verlag, Volume 130, pp. 162-173, 1989.
- Min, P.S. and Ribbens, W.B., "A Vector Space Solution to Incipient Sensor Failure Detection," *IEEE Transactions on Vehicular Technology*, Volume 38, No.3, pp. 148-158, August 1989.
- Min, P.S., "Robust Application of Beard-Jones Detection Filter," *Proceedings of the 1989 American Control Conference*, Pittsburgh, pp. 859-864, June 1989.
- Rizzoni, G. and Min, P.S., "Real Time Detection Filters for the On-board Diagnosis of Incipient Failures," *Proceedings of the 1989 International Symposium on Allied Technology and Automation*, pp. 1445-1466, Paper No. 89131, Florence, Italy, June 1989.
- Min, P.S., "Diagnosis of On-Board Sensors in Internal Combustion (IC) Engines," *Proceedings of the 1989 American Control Conference*, Pittsburgh, pp. 1065-1070, June 1989.
- Min, P.S., "Detection of Incipient Sensor Failures in Internal Combustion Engines," *Proceedings of the 1988 International Symposium on Allied Technology and Automation*, Paper No. 88038, Florence, Italy, June 1988.

Testimony Provided or Expected to Provide as Expert Witness

Matter: Patent Infringement for Wireless Local Area Networks
Law Firm: Quinn Emanuel Urquhard & Sullivan LLP

Case Name: Certain Audio Players and Components thereof (II). U.S.I.T.C. Inv. No. 337-TA-1330.

Testifying Expert for Google Inc.

Completed in June 2023.

(Expert reports submitted and deposed.)

Matter: Patent Infringement for Wireless Communications

Law Firm: Alston & Bird

Case Name: Atlas Global Technologies LLC v. ASUSTek Computers Inc. USDC WD TX

Civil Action No. 6:21-cv-820

Testifying Expert for ASUSTek

Completed in November 2023

(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications

Law Firm: Perkins Coie

Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)

Testifying Expert for HMD

Completed in December 2023

(Expert report submitted. Deposed.)

Matter: Patent Infringement for Wireless Communications

Law Firm: LAW OFFICES S. J. CHRISTINE YANG

Case Name: Atlas Global Technologies LLC v. ZyXEL Communications Corp. et al., U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00355 Atlas Global Technologies LLC v. D-Link Corp. U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00520

Testifying Expert for ZyXel

Retained in March 2023.

(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications

Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP

Case Name: Bell Northern Research v. MeidaTek Inc.

Testifying Expert for MediaTek Inc.

Retained in August 2023.

Matter: Patent Infringement for Home Security System

Law Firm: Foley and Lardner LLP

Case Name: Alarm.com v. Vivint, Inc., AAA Arbitration Case. No. 01-22-0004-5525 and U.S.D.C. Case No. 2:23-cv-00004-JRG-RSP (E.D. Tex.),

Testifying Expert for Vivint, Inc.

Completed in 2023.

Matter: Patent Infringement for Wireless Communications and Electronics

Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023.

Matter: Patent Infringement for Network Switches
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC v. CouldFlare, Inc. U.S.D.C. WD Tx
Case No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.
Completed in January 2024.
(Expert report submitted and deposited.)

Matter: Patent Infringement for Network Security
Law Firm: Fish and Richardson
Case Name: Finjan LLC v. Palo Alto Networks, Inc. – Case No. 4:14-cv-04908-PJH. USDC
ND CA, Oakland Division.
Testifying Expert for Finjan LLC.
Retained in September 2022.
(Expert report submitted and deposited.)

Matter: Patent Infringement for Network Management
Law Firm: Irell & Manella LLP
Case Name: SNMP Research, Inc. & SNMP Research International, Inc. v. Broadcom Inc.,
Brocade Communications Systems LLC, & Extreme Networks, Inc. U.S.D.C.
E.D. Tennessee at Knoxville Case No. 3:20-CV-451
Testifying Expert for SNMP Research.
Retained in May 2022.

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for MediaTek
Retained in March 2023.

Matter: Patent Infringement for Network Switching
Law Firm: Baker Botts
Case Name: Corrigent Corp. v. Arista Networks, Inc., Case No. 1:22-cv-00497-UNA. USDC
Delaware
Testifying Expert for Arista
Retained in October 2022.

Matter: Patent Infringement for Mobile Devices
Law Firm: Fish and Richardson
Case Name: GComm v. Samsung, U.S.D.C. ED. TX. Case No.:2:22-cv-0078-JRG

Testifying Expert for Samsung
Completed in January 2024.

Matter: Patent Infringement for Wireless Networks
Law Firm: McKool Smith
Case Name: Certain Mobile Telephones, Tablet Computers with Cellular Connectivity, and Smart Watches with Cellular Connectivity, Components Thereof, and Products Containing Same. U.S.I.T.C. Inv. No. 337-TA-1299
Testifying Expert for Ericsson
Completed in July 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Semiconductor Manufacturing
Law Firm: Kramer Levin
Case Name: Oasis Tooling, Inc. v. Siemens Indus. Software, Inc., 1:22-cv-151 (D. Del.), Oasis Tooling, Inc. v. GlobalFoundries U.S. Inc., 1:22-cv-312 (D. Del.)
Testifying Expert for Oasis Tooling
Retained in June 2022.
(Expert reports submitted.)

Matter: Patent Infringement for Optical Networks
Law Firm: Duane Morris
Case Name: NextGen Innovations, LLC v. Infinera Corporation. U.S.D.C. ED. TX (Marshall) Case No. 2:22-cv-00306-JRG-RSP / IPR
Testifying Expert for Infinera
Retained in April 2023.

Matter: Patent Infringement for Wireless Devices
Law Firm: King and Spalding LLP
Case Name: Intellectual Ventures, et. al. v. General Motors Company and General Company Motors, LLC, Case No. 6:21-CV-1088 pending in the Western District of Texas, Waco Division
Testifying Expert for General Motors
Completed in January 2023.
(Expert report submitted.)

Matter: Patent Infringement for Wireless Devices
Law Firm: Sterne Kessler
Case Name: Neo Wireless LLC v. Volkswagen Group of America, Inc. and Volkswagen Group of America Chattanooga Operations, LLC and related matters
Testifying Expert for Volkswagen
Completed in September 2023.
(Expert report submitted and deposed. IPR declarations submitted)

Matter: Patent Infringement for Wireless Networks
Law Firm: Covington & Burling LLP

Case Name: XR Communications, LLC v. D-Link Systems, Inc., No. 8:17-cv-00596
(Consolidated) (C.D. Cal.)
Testifying Expert for Hewlett Packard Enterprise
Completed
(Expert report submitted and deposed.)

Matter: Patent Infringement for USB Charging System
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Fundamental Innovation Systems International LLC v. TCT Mobile (US), TCT
Mobile (US) Holdings, Inc., et al. U.S.D.C. Delaware No. 20-552-RGA-CJB
Testifying Expert for TCL
Completed in June 2022.
(Expert report submitted and deposed.)

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Alston & Bird
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Nokia
Retained in May 2022.
(Expert report submitted.)

Matter: Patent Infringement for Network Management System
Law Firm: Morgan, Lewis & Bockius, LLP
Case Name: Certain Routers, Access Points, Controllers, Network Management Devices,
Other Networking Products, and Hardware and Software Components Thereof,
U.S.I.T.C. Inv. No. 337-TA-1227
Testifying Expert for Hewlett Packard, Netgear, and CommScope
Completed in August 2021.
(Expert report submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Security Systems
Law Firm: Forley and Lardner LLP
Case Name: Certain Residential Premises Security Monitoring and Automation Control
Panels, and Components Thereof (ITC Inv. No. 337-TA-1273) and ADT LLC et
al v. Vivint, Inc., Case No. 6:21-cv-00687 (W.D. Tex.)
Testifying Expert for Vivint, Inc.
Completed in April 2022.
(Expert report submitted, deposed, and testified during trial.)

Matter: Inter Parte Reexamination for Internet Communications
Law Firm: Perkins Coie
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Twitter
Retained in June 2020.
(Expert report submitted.)

- Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd. v. Heathco LLC, U.S.D.C. Delaware No. 20-224-LPS
Testifying Expert for Vaxcel
Retained in February 2021.
(Expert report submitted and deposed.)
- Matter: Patent Infringement for Network Communication System
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC, v. ClouFlare, Inc. U.S.D.C. WDTX, Civil Action No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.,
Completed in January 2024.
- Matter: Patent Infringement for Mobile Wireless Device
Law Firm: Pearl Cohen
Case Name: In the Matter Of Certain UMTS And LTE Cellular Communications Modules And Products Containing The Same, U.S.I.T.C. Inv. No. 337-TA-1240
Testifying Expert for Telit Wireless Communication, Quectel, and Thales
Completed in March 2023.
(Expert reports submitted and deposed.)
- Matter: Transactional Taxes for Internet Application
Law Firm: Ryan Rapp & Underwood, PLC
Case Name: ADP, LLC v. Arizona Department of Revenue (TX2018-000246),
Testifying Expert for ADP, LLC.
Completed in June 2020.
(Expert report submitted.)
- Matter: Trade Secret Misappropriation in Digital Electronics
Law Firm: Goodwin Proctor LLP
Case Name: Guzik Technical Enterprises versus Keysight Technologies, Inc. Superior Court of the State of California for the County of Santa Clara, Case No.: 19CV355879
Testifying Expert for Keysight Technologies, Inc.
Retained in August 2020.
- Matter: Patent Infringement for Fiber Optic Devices
Law Firm: Cooley
Case Name: Certain High-Density Fiber Optic Equipment and Components Thereof, U.S.I.T.C. Inv. No. 337-TA-1194
Testifying Expert for AFL Communications, Panduit, FS.Com, Wirewerk, and Siemon
Completed in October 2020.
(Expert reports submitted, deposed, and testified during trial.)
- Matter: Patent Infringement for Optical Transport Networks

Law Firm: Venerble
Case Name: Huawei Technologies Co. Ltd v Verizon Communications, Inc., et. al., 2:20-cv-0030
Testifying Expert for Verizon.
Retained in March 2020.
(IPR declarations submitted.)

Matter: Patent Infringement for Lighting System
Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd., v. Jasco Products Company, LLC., (Case No. USDC Western District of Oklahoma, 5:19-CV-00154-JD
Testifying Expert for Vaxcel.
Retained in August 2020.

Matter: Patent Infringement for Wireless Communication
Law Firm: McDermott Will & Emery
Case Name: Bell Northern Research LLC v. ZTE. (Case No. 3:18-cv-01786 - S.D. Cal)
Testifying Expert for ZTE.
Retained in July 2019.
(IPR declarations submitted.)

Matter: Patent Infringement for Wireless Communication
Law Firm: Jones Day
Case Name: Bell Northern Research LLC v. Kyocera Corp. (Case No. 3:18-cv-1785 - S.D. Cal)
Testifying Expert for Kyocera.
Completed in May 2019.
(Claim construction declaration submitted, and deposed.)

Matter: Patent Infringement for Electronic Payment Systems
Law Firm: Paul Hastings
Case Name: ID Tech Corp. v. Samsung Electronics Co., Ltd., et al. (Case No. No. 8:17-cv-1748-DOC-JDE (C.D. Cal))
Testifying Expert for Samsung.
Retained in January 2019.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Internet Switching
Law Firm: Maynard Cooper
Case Name: Parity Networks, LLC v. Juniper Networks, Inc., Case No. 6:17-CV-00495-RWS-KNM (U.S.D.C.E.D. Tx.)
Testifying Expert for Juniper.
Retained in April 2018.
(IPR declarations submitted.)

Matter: Patent Infringement for Internet Switching

Law Firm: Morgan Lewis
Case Name: Parity Networks, LLC v. Hewlett Packard Enterprise Company, Case No. 6:17-CV-00682 (U.S.D.C.E.D. Tx.)
Testifying Expert for Hewlett Packard Enterprise Company.
Retained in September 2018.
(IPR declarations submitted.)

Matter: Inter Parte Rexamination for Covered Business Method
Law Firm: Reed Smith LLP
Case Name: NASDAQ v. Miami International
Expert for Miami International.
Retained in February 2018.
(Expert declarations submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Qualcomm v. Apple, Case No. 3:17-cv-00108-GPC-MDD (U.S.D.C.S.D. Cal.)
Testifying Expert for Qualcomm.
Completed in April 2019.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Communication Devices
Law Firm: Venable
Case Name: Sycamore IP Holdings LLC v. Verizon Communications Inc, Case No. 2:16-cv-591-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Verizon and Level 3.
Completed in September 2017.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Alston Bird
Case Name: Huawei Technologies Co. Ltd. V. Nokia Solutions and Networks, Case No. 2:16-cv-0056-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Nokia.
Completed in December 2017.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Huawei Technologies Co. Ltd. V. Samsung Electronics C. Ltd, Case No. 3:16-cv-02787 (U.S.D.C. N.D. Cal)
Testifying Expert for Samsung.
Completed in March 2019.
(Expert reports submitted, and deposited.)

Matter: Arbitration for Licensing
Law Firm: Alston Bird
Case Name: Nokia v. LG Electronics, International Chamber of Commerce Arb. No. 21326
Testifying Expert for Nokia.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Ropes and Gray
Case Name: Godo Kaisha IP Bridge 1 v. TCL Communication Technology Holdings, Case No. 15-634-SLR-SRF (U.S.D.C.S.D. Delaware.)
Testifying Expert for IP Bridge.
Completed in October 2018.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Paul Hastings
Case Name: Odyssey Wireless, Inc., v. Samsung Electronics Co., Ltd., et al, Case No. 3:15-cv-1738-H-RBB (U.S.D.C.S.D. Cal.)
Testifying Expert for Samsung.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Greenberg Traurig
Case Name: Mobile Telecommunications Technologies LLC v. Amazon.com, Inc., 2:13-cv-883-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Amazon.
Completed in April 2015.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Mayer Brown
Case Name: Mobile Telecommunications Technologies LLC v. LG Electronics Mobilecomm U.S.A., Inc., 2:13-cv-947-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for LG Electronics Mobilecomm.
Completed in February 2016.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Semiconductor Devices
Law Firm: Mayer Brown
Case Name: Inter Parte Reexamination for U.S. Patent Nos. 6,895,520 and 6,899,332
Expert for LG Electronics.
Completed in February 2016.
(Expert declaration submitted, and deposited.)

- Matter: Patent Infringement in Vehicular Electronics
Law Firm: Gardner, Linn, Burkhardt & Flory, L.L.P
Case Name: *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:12-cv-00654 (Western District of Michigan), and relating to the action styled *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:13-cv-00324 (Western District of Michigan).
Testifying Expert for Magna Electronics
Completed in February 2016.
(Expert reports submitted, and deposited.)
- Matter: Patent Infringement in Electronic Circuits
Law Firm: Ropes and Gray
Case Name: Certain Devices Containing Non-Volatile Memory and Products Containing the Same (USITC Inv. Nos. 337-TA-922)
Testifying Expert for Spansion Inc.
Completed in February 2015.
(Expert reports submitted.)
- Matter: Trade Secret Misappropriation in Software Method for Cable Television Advertisement
Law Firm: Brownstein Hyatt Farber Schreck
Case Name: Cross MediaWorks v. EMT Holdings, USDC Southern District of New York, Case No. 1:14-cv-00561-VSB
Testifying Expert for Cross MediaWorks.
Completed in April 2015.
(Testified during injunction hearing.)
- Matter: Patent Infringement in Vehicular Electronics
Law Firm: Steptoe and Johnson
Case Name: Certain Vision-Based river Assistance System Cameras and Components Thereof (USITC Inv. Nos. 337-TA-899 and 907)
Testifying Expert for Magna Electronics
Completed in February 2015.
(Expert reports submitted, deposited, and testified during trial.)
- Matter: Patent Infringement for Vehicular System
Law Firm: Susman Godfrey
Case Name: Eagle Harbor Holdings, LLC, and Mediustech, LLC, v. Ford Motor Company, 3:11-cv-05503-BHS (U.S.D.C. Western District of Washington at Tacoma)
Testifying Expert for Mediustech.
Completed in March 2015.
(Expert reports submitted, deposited, and testified during trial.)
- Matter: Patent Infringement for Communication Networks
Law Firm: Davis Polk & Wardwell LLP

Case Name: Sprint Communications Company L.P., v. Comcast Cable Communications, LLC, Comcast IP Phone, LLC, and Comcast Phone of Kansas, LLC. 2:11-cv-02684-KHV-DJW (U.S.D.C. Kansas)
Testifying Expert for Comcast.
Retained in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Networks
Law Firm: Quinn Emanuel
Case Name: France Telecom S.A. v. Marvell Semiconductor, Inc., 12-Civ-4986 (S.D.N.Y.)
Testifying Expert for Marvell.
Completed in September 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Wireless Image Distribution
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent No. 8,437,797
Expert for Google Inc.
Completed in November 2014.
(Expert declaration submitted.)

Matter: Nonvolatile Semiconductor Memories
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent Nos. 8,301,833 and 8,516,187
Expert for SanDisk.
Completed in May 2014.
(Expert declaration submitted.)

Matter: Communication Protocols for Wireless Device
Law Firm: Dorsey & Whitney, LLP
Case Name: Certain Point-To-Point Network Communication Devices and Products Containing Same (USITC Inv. No. 337-TA-892)
Testifying Expert for Toshiba
Completed in May 2014.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Ropes and Gray
Case Name: In the Matter of Certain Wireless Devices With 3G and/or 4G Capabilities and Components Thereof (USITC Inv. No. 337-TA-868) InterDigital Comms., Inc. v. Huawei Techs. Co., Ltd., No. 13-00008 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. ZTE Corp., No. 13-00009 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Nokia Corp., No. 1:13-cv-00010 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Samsung Elec. Co., Ltd., No. 13-00011 (D. Del., filed January 2, 2013)
Testifying Expert for Joint Defense Group.

Completed in February 2014.
(Expert reports submitted, deposed, and testified during trials.)

Matter: Patent Infringement for Mobile Communication
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.
Case Name: Certain Digital Media Devices, Including Televisions, Blu-Ray Disc Players, Home Theater Systems, Tablets and Mobile Phones, Components Thereof and Associated Software (USITC Inv. No. 337-TA-882)
Testifying Expert for LG Electronics, Inc.
Completed in February 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Vinson & Elkins LLP
Case Name: Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Telefonaktiebolaget LM Ericsson and Ericsson, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23569), Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Alcatel-Lucent USA, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23568-Altonaga/Simonton)
Testifying Expert for Wi-LAN.
Completed in May 2015.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Data Storage
Law Firm: Ropes and Gray, Weil Gotshal
Case Name: Summit Data Systems, LLC v. EMC Corporation., et al. 1:10-cv-00749-GMS (U.S.D.C. Delaware)
Testifying Expert for EMC Corporation and Netapp, Inc.
Completed in December 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Ashurst Australia
Case Name: Samsung v. Apple, Australian Federal Court Proceeding No. NSD 1243 of 2011
Testifying Expert for Samsung Electronics.
Completed in December 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Apple Inc. v. Samsung Electronics Co., Ltd., et al., 4:11-cv-01846-LHK (N.D. Cal.) and Samsung Electronics Co., Ltd., et al. v. Apple Inc., 4:11-cv-02079 (N.D. Cal.)
Testifying Expert for Samsung Electronics.
Completed in July 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Quinn Emanuel
Case Name: Certain Electronic Devices, Including Wireless Communication Devices, Portable Music And Data Processing Devices, And Tablet Computer, U.S.I.T.C. Inv. No. 337-TA-794
Testifying Expert for Samsung Electronics.
Completed in June 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Portable Storage Device
Law Firm: White and Case
Case Name: CERTAIN UNIVERSAL SERIAL BUS (“USB”) PORTABLE STORAGE DEVICES, INCLUDING USB FLASH DRIVES AND COMPONENTS THEREOF, US International Trade Commission Investigation No. 337-TA-788
Testifying Expert Witness for Trek
Completed in May 2012.
(Expert reports submitted, and deposed.)

Matter: Copyright Infringement for Petroleum Processing Software
Law Firm: Osha Liang LLP
Case Name: Aspen Technology, Inc. v. Tekin A. Kunt and M3 Technology, Inc., Case Number: H-10-1127, US District Court, Texas, Houston Division.
Testifying Expert for M3 Technology, Inc.
Completed in May 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Trade Secret Misappropriation for DC-DC converter
Law Firm: Covington & Burling, Haynes Boone
Case Name: Certain DC—DC Controllers and Products Containing Same, US International Trade Commission Investigation No. 337-TA-698
Testifying Expert for UPI.
Completed in March 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Parallel Processor
Law Firm: Orrick, Herrington, & Sutcliffe. Kirkland and Ellis.
Case Name: BIAx Corporation v. Nvidia and Sony Civil Action No. 09-cv-01257-PAB-MEH
Testifying Expert for Nvidia and Sony
Completed in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Duffy, Sweeney, and Scott. Foley Lardner.
Case Name: Ronald Katz Technology Licensing v. Citizens Financial Group 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for Citizens Financial Group.

Completed in 2011.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Storage Area Network
Law Firm: DLA Piper
Case Name: Network Appliance, Inc., v. Sun Microsystems, Inc., Case Number: C-07-06053
EDL, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Sun Microsystems, Inc.
Completed in 2010.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flat Panel Display Controller
Law Firm: Jones Day
Case Name: Certain Video Displays, Components Thereof, and Products Containing Same, US
International Trade Commission Investigation No. 337-TA-687
Testifying Expert for Vizio, Inc.
Completed in 2010.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Foley Lardner
Case Name: Ronald Katz Technology Licensing v. US Bank 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for US Bank
Completed in May 2009.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for USB to VGA Converter
Law Firm: Wang Hartmann, Gibbs, & Cauley, P.C.
Case Name: Displaylink Corporation v. Magic Control Technology Corporation, Case No.
5:07-CV-01998-RMW, US District Court, Northern District of California, San
Francisco Division.
Testifying Expert for Magic Control Technology Corporation
Completed in 2009.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flash Memory
Law Firm: Jones Day and Wilson Sansini
Case Name: Certain Flash Memory Controllers, Drives, Memory Card, and Media Players and
Products Containing Same. US International Trade Commission Investigation
No. 337-TA-619
Testifying Expert for SanDisk Corporation.
Completed in 2008.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Semiconductor Packaging
Law Firm: Jones Day

Case Name: Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing the Same. US International Trade Commission Investigation No. 337-TA-605

Testifying Expert for Freescale Semiconductor

Completed in 2008.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Automatic Switching System

Law Firms: Jones Day, and Heller Ehrman, LLP.

Case Name: ATEN International Co., Ltd and ATEN Technology, Inc. v. Belkin Corporation, Belkin Logistics, Inc. and Emine Technology Co., Ltd. US International Trade Commission Investigation No. Ltd 337-TA-589

Testifying Expert for Belkin Corporation, Belkin Logistics, Inc., and Emine Technology Co., Ltd.

Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Dual Mode Communication

Law Firm: Wilmer Cutler Pickering Hale and Dorr, LLP

Case Name: Broadcom Corporation v. Qualcomm Incorporated SACV05-467-JVS (RNBx)

Testifying Expert Witness for Broadcom Corporation

Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)