

THE ART OF ELECTRONICS

SECOND EDITION

MOSAID Technologies Inc.
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Technologies Inc.
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CAMBRIDGE

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accurately calibrated 10dB steps; a vernier is provided for variable gain. IC₂ is an inverting amplifier; it allows offsetting the output over a range of ± 10 volts, accurately calibrated via R_{14} , by injecting current into the summing junction. $C_2 - C_4$ set the high-frequency rolloff, since it is often a nuisance to have excessive bandwidth (and noise). IC₅ is a power booster for driving low-impedance loads or cables; it can provide ± 150 mA output current.

Some interesting details: A $10\text{M}\Omega$ in-

put resistor is small enough, since the bias current of the 411 is 25pA (0.3mV error with open input). R_2 , in combination with D_1 and D_2 , limits the input voltage at the op-amp to the range V_- to $V_+ + 0.7$. D_3 is used to generate a clamp voltage at $V_- + 0.7$, since the input common mode range extends only to V_- (exceeding V_- causes the output to reverse phase). With the protection components shown, the input can go to ± 150 volts without damage.

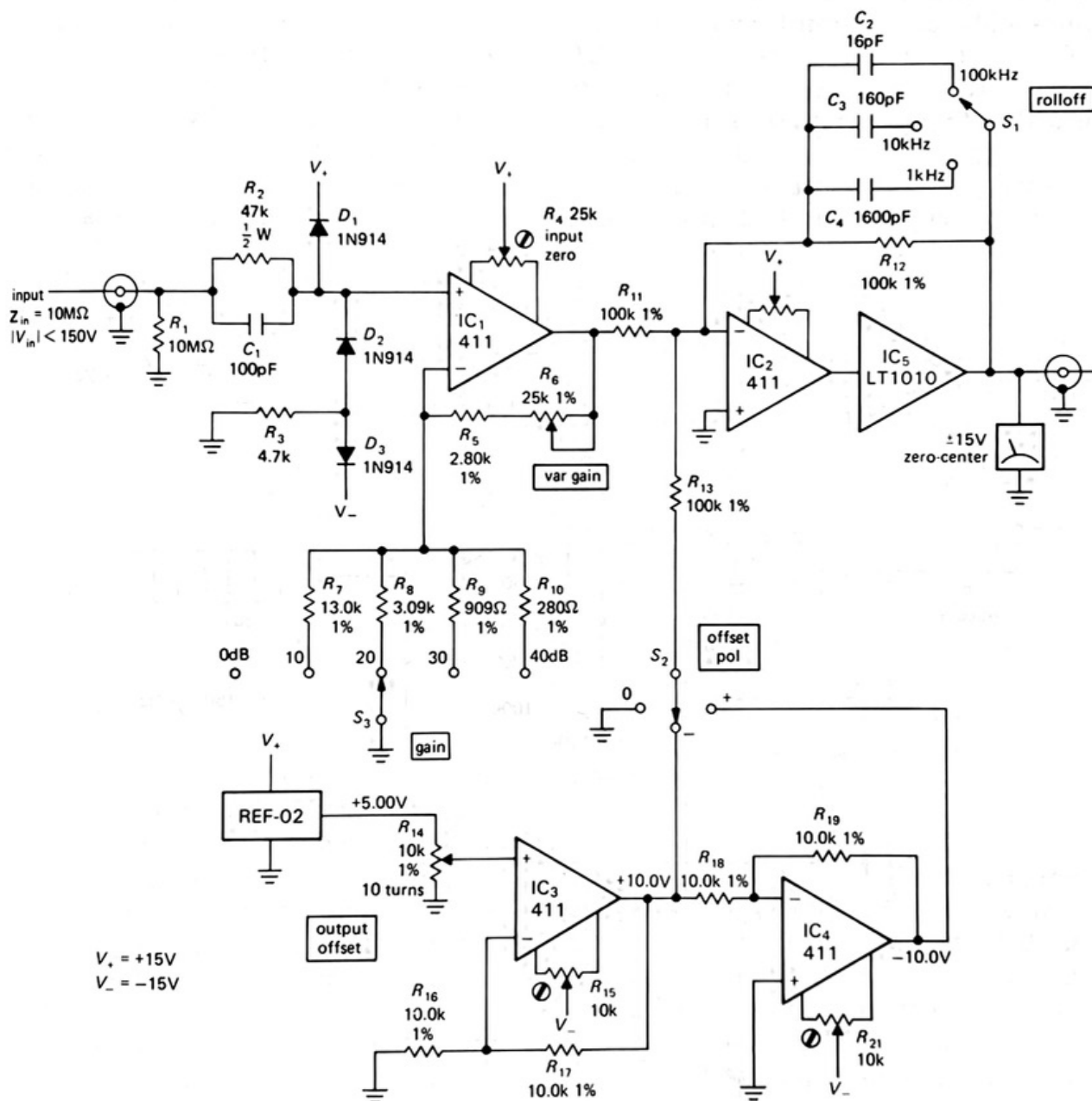


Figure 4.74. Laboratory dc amplifier with output offset.

EXERCISE 4.12

Check that the gain is as advertised. How does the variable offset circuitry work?

4.29 Voltage-controlled oscillator

Figure 4.75 shows a clever circuit, borrowed from the application notes of several manufacturers. IC₁ is an integrator, rigged up so that the capacitor current ($V_{in}/200k$) changes sign, but not magnitude, when Q_1 conducts. IC₂ is connected as a Schmitt trigger, with thresholds at one-third and two-thirds of V_+ . Q_1 is an n -channel MOSFET, used here as a switch; it is simpler to use than bipolar transistors in this sort of application, but an alternative circuit using n pn transistors is shown in addition. In either case, the bottom side of R_4 is pulled to ground when the output

is HIGH and open-circuited when the output is LOW.

An unusual feature of this circuit is its operation from a single positive supply. The 3160 (internally compensated version of the 3130) has FETs as output transistors, guaranteeing a full swing between V_+ and ground at the output; this ensures that the thresholds of the Schmitt don't drift, as they would with an op-amp of conventional output-stage design, with its ill-defined limits of output swing. In this case this means that the frequency and amplitude of the triangle wave will be stable. Note that the frequency depends on the ratio V_{in}/V_+ ; this means that if V_{in} is generated from V_+ by a resistive divider (made from some sort of resistive transducer, say), the output frequency won't vary with V_+ , only with changes in resistance.

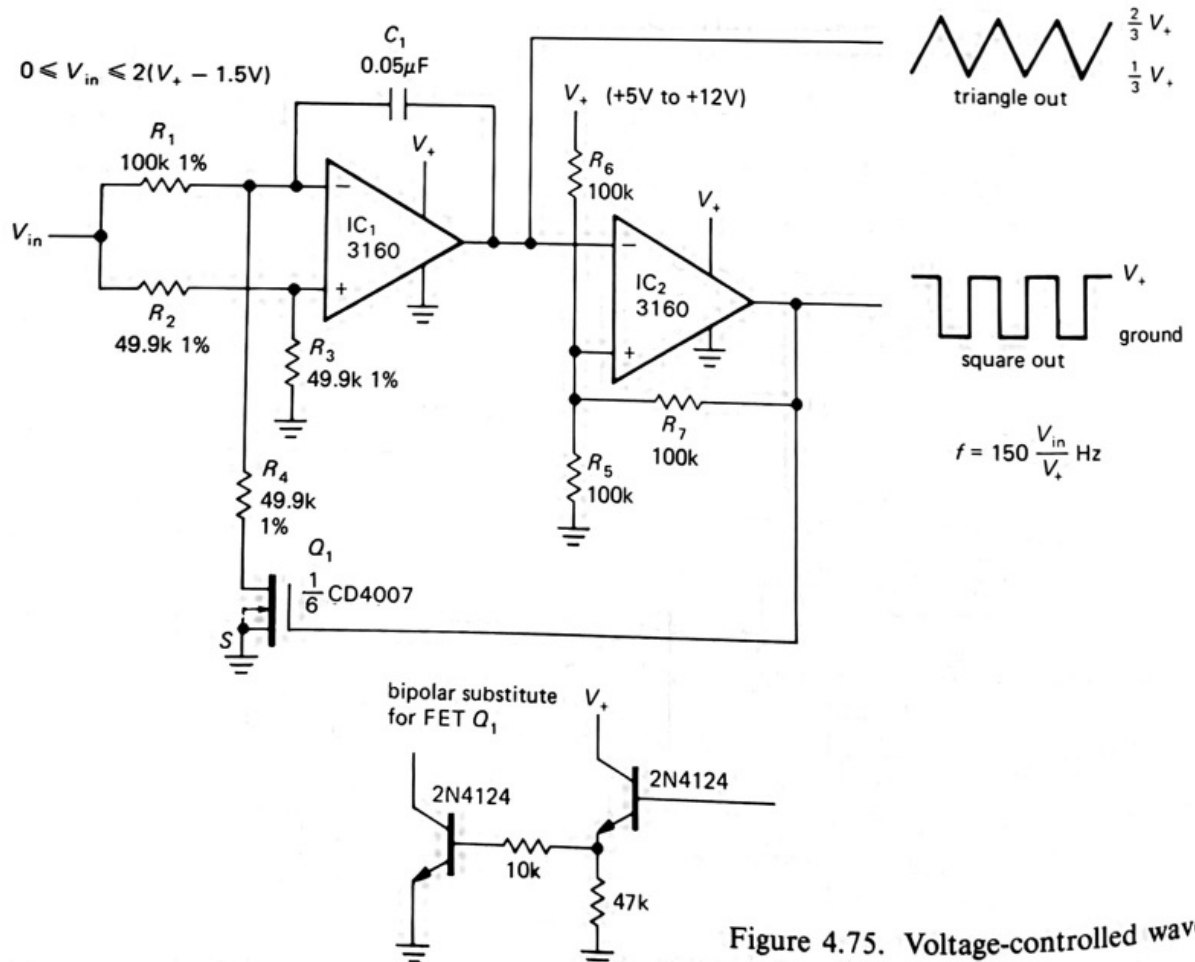


Figure 4.75. Voltage-controlled waveform generator.

EXERCISE 4.13

Show that the output frequency is given by $f(\text{Hz}) = 150V_{in}/V_+$. Along the way, verify that the Schmitt thresholds and integrator currents are as advertised.

4.30 JFET linear switch with R_{ON} compensation

In Chapter 3 we considered MOSFET linear switches in some detail. It is also possible to use JFETs as linear switches. However, you have to be more careful about gate signals so that gate conduction doesn't occur. Figure 4.76 shows a typical arrangement. The gate is held well below ground to keep the JFET pinched off. This means that if the input signals go negative, the gate must be held at least V_P below the most negative input swing. To bring the FET into conduction, the control input is brought more positive than the most positive input excursion. The diode is then reverse-biased, and the gate rides at source voltage via the 1M resistor.

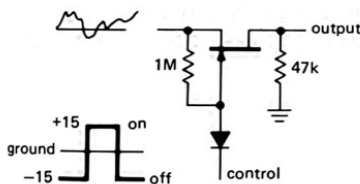
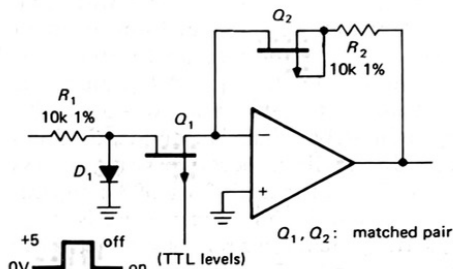


Figure 4.76

The awkwardness of this circuit probably accounts for much of the popularity of MOSFETs in linear switch applications. However, it is possible to devise an elegant JFET linear switch circuit if you use an op-amp, since you can tie the JFET source to the virtual ground at the summing junction of an inverting amplifier. Then you simply bring the gate to ground potential to turn the JFET on. This arrangement has the added advantage of providing a method of canceling precisely the errors caused by

finite R_{ON} and its nonlinearity. Figure 4.77 shows the circuit.

Figure 4.77. JFET-switched amplifier with R_{ON} cancellation.

There are two noteworthy features of this circuit: (a) When Q_1 is ON (gate grounded), the overall circuit is an inverter with identical impedances in the input and feedback circuits. That results in the cancellation of any effects of finite or nonlinear R_{ON} , assuming the FETs are matched in R_{ON} . (b) Because of the low pinch-off voltage of JFETs, the circuit will work well with a control signal of zero to +5 volts, which is what you get with standard digital logic circuits (see Chapters 8 and 9). The inverting configuration, with Q_1 's source connected to a virtual ground (the summing junction), simplifies circuit operation, since there are no signal swings on Q_1 's source in the ON state; D_1 prevents FET turn-on for positive input swings when Q_1 is OFF, and it has no effect when the switch is closed.

There are p -channel JFETs with low pinch-off voltages available in useful configurations at low prices. For example, the IH5009–IH5024 family includes devices with four input FETs and one cancellation FET in a single DIP package, with R_{ON} of 100 ohms and a price less than two dollars. Add an op-amp and a few resistors and you've got a 4-input multiplexer. Note that the same R_{ON} cancellation trick can be used with MOSFET switches.

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