

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK INC.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

IPR2024-00599
Patent 7,224,563 B2

Before KEN B. BARRETT, JOHN F. HORVATH, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

MediaTek Inc. (“Petitioner”)¹ filed a Petition requesting *inter partes* review of U.S. Patent No. 7,224,563 B2 (“the ’563 patent,” Ex. 1001). Paper 2 (“Pet.”). The Petition challenges the patentability of claims 1–11, 23, 24, and 31–35 of the ’563 patent. MOSAID Technologies Inc. (“Patent Owner”)² filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the ’563 patent. Accordingly, we institute an *inter partes* review as to all the challenged claims of the ’563 patent on all the grounds of unpatentability set forth in the Petition.

B. *Related Proceedings*

Both parties identify, as a matter involving or related to the ’563 patent, *MOSAID Technologies Inc. v. MediaTek, Inc., et al*, No. 2:23-cv-00129 (E.D. Tex.). Pet. 88–89; Paper 4, 1.

¹ Petitioner identifies MediaTek Inc. and MediaTek USA Inc. as real parties in interest. Pet. 88.

² Patent Owner identifies MOSAID Technologies Inc. as the real party in interest. Paper 4, 1.

C. The '563 Patent

The '563 patent is titled “Method and Device for Circuit Control.”

Ex. 1001, code (54). According to the Abstract of the '563 patent,

One disclosed embodiment of the invention is directed to circuit control that comprises sensing a delivered voltage to a portion of an integrated circuit, determining an appropriate frequency for the portion of the integrated circuit, and providing the appropriate frequency to the integrated circuit.

Id. at code (57).

The Background section of the Specification explains that “[i]t is broadly recognized in the implementation of power management systems for VLSI [(Very Large Scale Integration)] devices that the most efficient means of power management is to simultaneously change 1) the voltage delivered to an integrated circuit, and 2) the frequency of that integrated circuit's operation.” *Id.* at 1:19–23, 6:47–48. “Because voltage is a primary determinant of switching speed for transistors of an integrated circuit, a designer will typically specify the maximum frequency at which a part can operate for a given voltage.” *Id.* at 1:24–27.

The Specification further explains that “power supplies vary and electrical parasitics between the power supply and the actual transistors of an integrated circuit effect power transmission, [and, t]hus the voltage actually delivered to an integrated circuit is not a completely fixed value, but rather ripples and varies with time.” *Id.* at 1:36–40. “[A] processor running at a frequency higher than the voltage supports can result in a timing failure.” *Id.* at 3:1–2. According to the '563 patent, “[t]hus, there exists a need for a system that could set the frequency to an observed voltage and constantly vary the frequency to match the voltage actually delivered.” *Id.* at 3:20–22.

Figure 3 of the '563 patent is reproduced below.

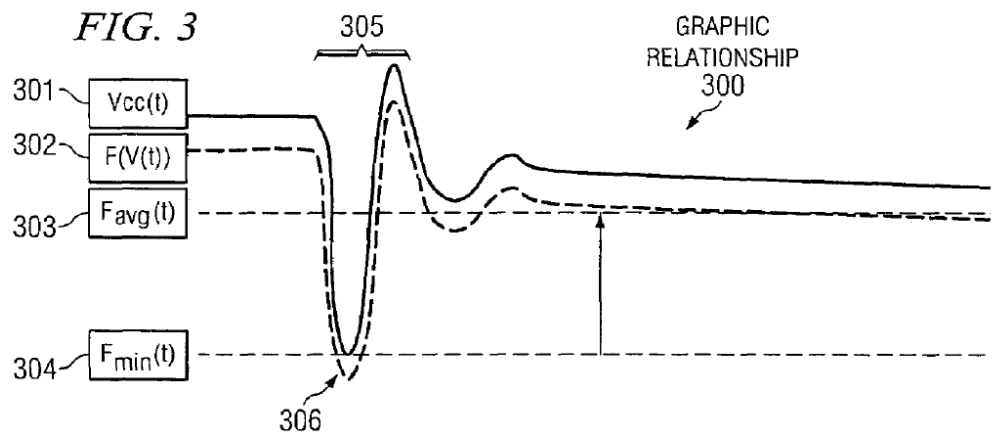


Figure 3, according to the Specification, “is a graph illustrating some advantages of certain embodiments of the [’563 patent].” *Id.* at 3:62–63.

The Specification states that:

[T]he delivered voltage 301 will likely vary, as seen by voltage deviation 305. Prior art solutions required that the provided frequency 304 be low enough to still be viable even at the minimum voltage 306. Some embodiments of the present invention are able to continuously sense the delivered voltage 301 and provide a frequency 302 that tracks the delivered voltage 301. Thus the average frequency 303, provided by these embodiments of the present invention is significantly higher than the frequency 304 allowed by prior art solutions.

Id. at 4:63–5:5. “Ideally, frequency will remain very close to the maximum supported by the voltage.” *Id.* at 6:29–30.

“Some embodiments may have multiple voltage detectors, distributed as regional voltage detectors, as well as multiple frequency synthesizers.”

Id. at 6:42–44. “Regional voltage sensors 801 are distributed across VLSI (Very Large Scale Integration) integrated circuit 800.” *Id.* at 6:46–48.

“These sensors 801 are able to sense the delivered voltage to a portion of VLS integrated circuit 800, and by means of frequency synthesizers 802,

alter the frequency to different positions of the integrated circuit.” *Id.* at 6:48–52.

The value of the delivered voltage may be measured and “[t]his voltage is converted . . . to a numeric value, by a[n] analog-to-digital converter for example.” *Id.* at 5:49–57. “Then the embodiment may access . . . a table or database that associates voltage values with appropriate frequencies, and transmit . . . the frequency associated with the delivered voltage to a frequency synthesizer” and “[t]he synthesizer can then adjust . . . the clock frequency to match.” *Id.* at 5:57–62.

D. Illustrative Claims

Of the challenged claims of the ’563 patent, claims 1, 23, and 35 are independent claims. Claims 1 and 35, reproduced below with bracketed annotations inserted, are illustrative.

1. [1Pre] A method of circuit control, comprising:
[1a] sensing a delivered voltage to a portion of an integrated circuit;
[1b] determining an appropriate frequency for the portion of the integrated circuit; and
[1c] providing the appropriate frequency to said portion of said integrated circuit.

35. [35pre] A system for circuit control comprising:
[35a] a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit;
[35b] a plurality of logic blocks arranged to determine an appropriate frequency for each said portion from said delivered voltages; and
[35c] a plurality of circuitry arrangements to provide each said portion its associated appropriate frequency.

Ex. 1001, 7:21–27, 9:1–10:4.³

E. Evidence

Petitioner relies on the following references:

Name	Reference	Exhibit No.
Tam	US 6,762,629 B2, issued July 13, 2004	1004
Huard	US 6,885,233 B2, issued April 26, 2005	1005
Norman ’259	US 6,853,259 B2, issued Feb. 8, 2005	1006
Norman ’851	US 2003/0034851 A1, published Feb. 20, 2003	1007
Naffziger ’788	US 6,509,788 B2, issued Jan. 21, 2003	1008

Petitioner also relies on the declaration of Paul Min, Ph.D. (Ex. 1003) in support of its arguments, and Patent Owner relies on the declaration of William Henry Mangione-Smith, Ph.D (Ex. 2001) in support of its arguments. The parties also rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. § ⁴	Reference(s)/Basis
1–10, 23, 24, 31, 32, 35	103(a)	Tam
1–11, 23, 24, 31–35	103(a)	Tam, Huard
1–11, 23, 24, 31–35	103(a)	Norman ’259, Norman ’851
1, 3, 10, 23, 24, 31, 32, 35	103(a)	Naffziger ’788

³ Independent claim 35 contains line breaks within certain limitations. *See* Ex. 1001, 9:3–4, 9:6–10:1, 10:3–4. We reproduce the claim with those line breaks omitted.

⁴ The application that issued as the ’563 patent was filed before the effective date of the Leahy Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), and we apply the pre-AIA version of 35 U.S.C. § 103.

II. DISCRETIONARY DENIAL UNDER 35 U.S.C. § 314(a)

Patent Owner asserts that we should discretionarily deny institution under 35 U.S.C. §314(a), arguing that “the Petition here presents excessive grounds of questionable merit.” Prelim. Resp. 62 (citing *Chevron Oronite Co. v. Infineum USA L.P.*, IPR2018-00923, Paper 9 at 10–11 (Nov. 7, 2018) (informative); *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 at 41–43 (Jan. 24, 2019) (informative); *see also* Prelim. Resp. 63 (Patent Owner arguing that “[c]ompounding this problem is the Petition’s improper incorporation by reference of large sections of the Min Declaration and the nearly verbatim language shared between the two.”).

In *Chevron Oronite* and *Deeper*, the petitioners had demonstrated a likelihood of prevailing only as to two claims out of several challenged, and the Board determined that instituting a trial would not be an efficient use of the Board’s time and resources. *See Chevron Oronite*, IPR2018-00923, Paper 9 at 10–11 (“Petitioner demonstrates, at most, a reasonable likelihood of prevailing with respect to two dependent claims out of a total of twenty challenged claims.”); *Deeper, UAB*, IPR2018-01310, Paper 7 at 43 (“On this record, and based on the particular facts of this proceeding, instituting a trial with respect to all twenty-three claims and on all four grounds based on evidence and arguments directed to only two claims and one ground would not be an efficient use of the Board’s time and resources.”). In contrast, we, for the reasons discussed below, determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to all of the challenged claims. We decline to exercise discretion to deny institution under § 314(a) for the reasons argued by Patent Owner.

III. ANALYSIS OF PETITIONER'S CHALLENGES

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) if present, any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quoting *Custom Accessories, Inc. v. Jeffrey–Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)).

Petitioner contends:

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.

Pet. 5–6 (citing Ex. 1003 ¶ 24).

Patent Owner asserts, without citation:

[F]or the purposes of this proceeding, a POSITA would have at least [a] bachelors of science degree in electrical engineering or computer engineering and at least two years of clock network design and/or power management design for processors or large system-on-chip (“SoC”) integrated circuits (“ICs”).

Prelim. Resp. 4–5.

Both parties contend that the ordinary artisan would have had two years of experience, with Patent Owner’s proposal in that regard being somewhat more specific than Petitioner’s. However, we do not see any meaningful distinction between the parties’ definitions of the person of ordinary skill in the art. For purposes of this decision, we apply Petitioner’s definition, which is consistent with the level of ordinary skill reflected in the prior art references of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (recognizing that the prior art itself may reflect an appropriate level of skill in the art). We note, however, that were we to apply Patent Owner’s definition, the outcome of this decision would be the same.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 37 C.F.R. § 42.100(b). In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). “[W]hile extrinsic evidence can shed useful light on the relevant art, . . . it is less significant than the intrinsic record in determining the legally operative meaning of claim language.” *Phillips*, 415 F.3d at 1317 (internal quotation marks omitted).

Petitioner states that, “[f]or purposes of this proceeding only, Petitioner submits that no claim term requires a formal construction for purposes of addressing the Grounds in this Petition,” and impliedly contends that all claim terms have their ordinary and customary meaning. Pet. 6.

Appropriate Frequency

Independent method claim 1, for example, recites “sensing a delivered voltage to a portion of an integrated circuit; determining an *appropriate frequency* for the portion . . . ; and providing the *appropriate frequency* to said portion” Ex. 1001, 7:22–27 (emphasis added).

Patent Owner asserts that “appropriate frequency” means “a frequency adapted to be at or below a maximum frequency possible at the delivered

voltage.” Prelim. Resp. 5. This is the construction that was proposed by Patent Owner in the parallel litigation and the construction adopted by the District Court after the Preliminary Response was filed. Ex. 2009, 8–16.

In this forum, Patent Owner goes further after advocating for the construction that has since been adopted by the District Court. Specifically, Patent Owner argues:

In other words, a POSITA reading the ’563 Patent would understand an “appropriate frequency” to be one that is adjusted in response to fluctuations in a voltage delivered to a portion of the integrated circuit in order to support higher average frequencies while still avoiding timing failures in that portion of the integrated circuit. Ex. 2001, ¶¶23–29. This is the focus of the specification, which describes the appropriate frequency as being a frequency derived from the delivered voltage that varies as the voltage varies in order to provide more optimal power consumption. *See, e.g.*, MTK-1001, Fig. 3, 1:14–58, 2:9–10, 4:29–35, 4:56–5:5, 5:34–40, 6:4–9, 6:28–31, 7:9–19, claim 3; Ex. 2001, ¶¶24–25. Stated another way, dealing with voltage fluctuation rapidly enough to prevent malfunctions while still using the highest possible operating frequency at all times is the reason d’etre of the patent.

Prelim. Resp. 5–6. Additionally, Patent Owner, in arguing against the challenge based on Tam, impliedly argues that an “appropriate frequency” is limited to the optimal frequency. *See id.* at 17–18 (“[B]ecause Tam’s frequency is for the entire integrated circuit and provides a sub-optimal frequency to any part of the chip not at the same voltage as the sensor driving the frequency change in Tam, it is not determining an ‘appropriate frequency’ as required.”); *see id.* at 17 (Patent Owner attempting to distinguish Tam by repeating the sentence in the block quote above pertaining to an “appropriate frequency” being “one that is adjusted in response to fluctuations in a voltage.”).

To the extent that Patent Owner argues for a construction narrowing the meaning of “appropriate frequency” beyond that adopted by the District Court, we decline to adopt a narrower construction at this time.

We also note that some of the concepts mentioned by Patent Owner are not consistent with the language of the District Court’s construction or, for example, method claim 1.⁵ For example, the reference to fluctuations in voltage implies multiple voltage readings; however, the method of claim 1 calls for the step of “sensing a delivered voltage,” which need only be performed once. *See* Ex. 1001, 7:22–23; *see also id.* at 7:28–30 (dependent claim 2 further limiting claim 1 by requiring the “sensing . . . [to be] continuously repeated during the integrated circuit’s operation.”).

Also, Patent Owner’s and the District Court’s construction contains the phrase, “at or below a maximum frequency possible.” Limiting the “appropriate frequency” to the optimal or to the “highest possible” frequency seemingly would be at odds with this broad range of possible frequencies. *See* Ex. 1001, 7:31–33 (dependent claim 3 further limiting the “appropriate frequency” of claim 1 to “a maximum frequency possible for the portion of the integrated circuit at the delivered voltage”). The District Court’s claim construction order states that “Defendants cite testimony of Plaintiff’s expert that the scope of ‘appropriate frequency’ encompasses everything from the maximum possible frequency all the way down to a frequency at which the circuit ceases to operate.” Ex. 2009, 14. That testimony, if applicable to the District Court’s construction (and it appears that it is), suggests that the claims encompass the presumably non-optimal

⁵ The District Court’s Order indicates that its construction is for system claims 23, 24, and 33. Ex. 2009, 8.

situation where the circuit no longer operates. *See also* Prelim. Resp. 7 (Patent Owner implying that the prior art “safe” approach—where “[t]he chosen frequency was sufficiently low that the circuit would not malfunction even in the worst-case of any expected voltage drop”—is not optimal.).

On this record and for purposes of this decision, we apply the District Court’s construction, namely that “appropriate frequency” means “a frequency adapted to be at or below a maximum frequency possible at the delivered voltage.” The parties may discuss the meaning of “appropriate frequency” in further briefing authorized in the Scheduling Order.

D. The Alleged Obviousness of Claims 1–10, 23, 24, 31, 32, and 35 Over Tam (Ground 1)

Petitioner alleges that claims 1–10, 23, 24, 31, 32, and 35 of the ’563 patent would have been obvious over Tam. *See* Pet. 6–18 (addressing claim 1). Patent Owner argues that Tam does not disclose determining an appropriate frequency for or providing an appropriate frequency to a portion of an integrated circuit, and that it would not have been obvious to modify Tam to meet those limitations. Prelim. Resp. 14.

1. Tam (Ex. 1004)

Tam is titled “VCC Adaptive Dynamically Variable Frequency Clock System for High Performance Low Power Microprocessors.” Ex. 1004, code (54). Tam “relates to a method and apparatus for a VCC adaptive dynamically variable frequency clock system for microprocessors.” Ex. 1004, 1:10–12. Tam explains that “[f]requency/voltage adjustment methods can be used to alter the circuit performance.” *Id.* at 1:49–50. Techniques taught in Tam “can easily be applied to other types of circuits or semiconductor devices that can benefit from power savings and avoiding voltage droop transients.” *Id.* at 2:36–40. Tam describes “the clock control

technique[, which] implements on-die voltage sensing and adjusts the clock frequency accordingly.” *Id.* at 4:1–3. According to Tam:

Embodiments of the present invention adapt the clock signal to voltage droops and fluctuations by dynamically adjusting the clock frequency based on sensed on-die voltage changes. For instance, when a droop is detected, the clock is slowed down to accommodate the reduced voltage level. Similarly, when the voltage recovery is detected, the clock frequency can be increased to enhance performance. Thus, a mechanism in accordance with the present invention provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.

Id. at 3:44–54.

Figure 2 is reproduced below.

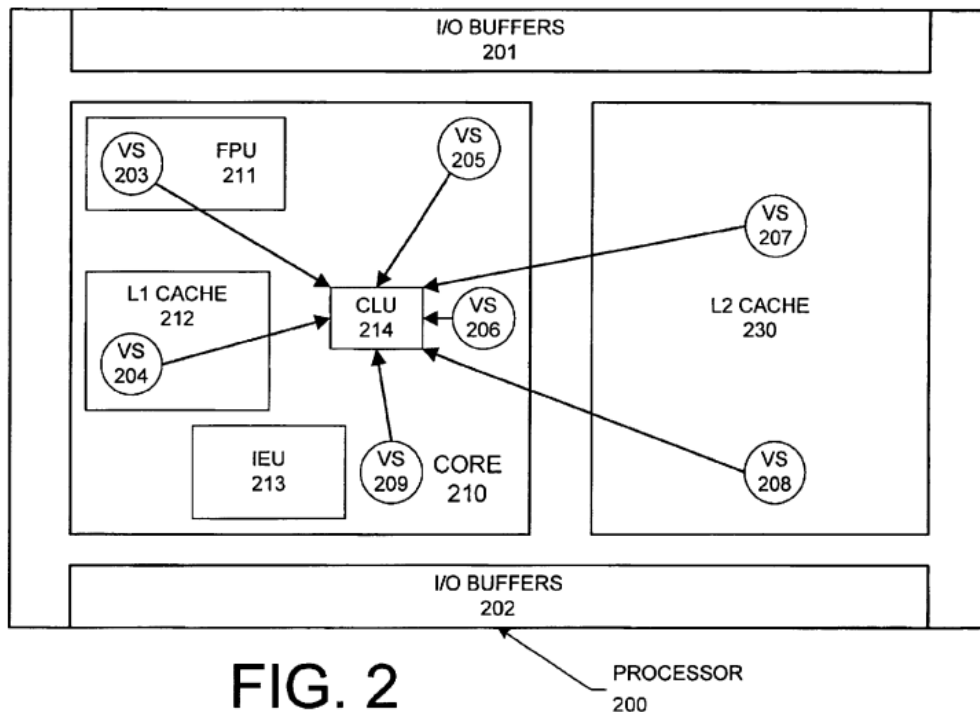


Figure 2 illustrates “a block diagram of a processor that includes on-die voltage sensors and adaptively variable clock generator.” *Id.* at 2:5–6. As can be seen in the figure, there are multiple voltage sensors (VS) located at various locations of processor 200. *See id.* at 5:50–53 (“These [voltage]

sensors can be strategically placed at various locations such as high voltage circuitry, critical circuits, power bussing, and high speed logic, for example.”). As also can be seen in Figure 2, there is a core or core block 210 that “includes a floating point unit FPU 211, level 1 L1 cache memory 212, an integer execution unit IEU 213, and a clock generation unit CLU 214.” *Id.* at 5:57–60. Tam discloses:

[T]he sensor 206 closest to the clock generator is a reference sensor to detect a baseline VCC voltage level. Two sensors 207, 208, are located in the L2 cache 230. Other sensors 203, 204, 209, are located with or around the FPU 211, L1 cache 212, and IEU 213, respectively, to sense the supply voltages in those regions. These sensors 203, 204, 205, 206, 207, 208, 209, are to detect the local VCC voltage levels and to communicate that information back to the clock generator 214. Logic in the clock generator 214 monitors the voltage statuses and can dynamically adapt and adjust the clock frequency based on the sensed information. For example, a local sensor in a high activity area such as the FPU can better indicate the existence of a critical low voltage condition in that circuitry and inform the clock generator of a need to lower the operating frequency. But when the FPU is inactive, another different sensor may read low and another circuit may be the controlling factor.

Id. at 6:1–18.

Figure 3 is reproduced below.

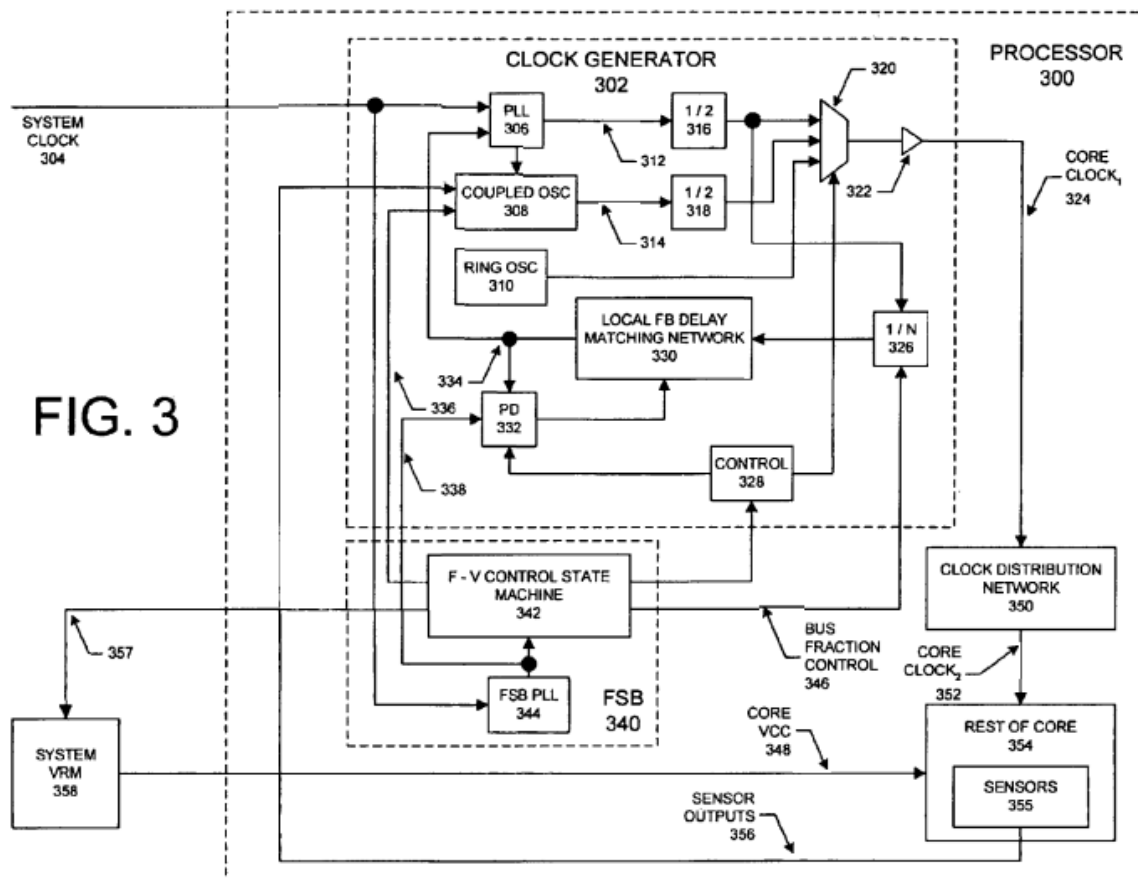


Figure 3 “is a block diagram of a processor architecture having a mechanism for dynamically adjusting a clock frequency in order to adapt to varying supply voltages.” *Id.* at 6:33–36.

The clock generator is a VCC adaptive dynamically variable frequency clock system capable of varying the frequency of its clock output in response to voltage sensors 355. Clock generator is to provide an internal processor clock signal CORE CLOCK₁ 324 to the rest of the processor core 354 via a clock distribution network 350.

Id. at 6:38–44.

According to Tam, “[t]he configuration of the PLL 306 in the clock generator 302 enables the microprocessor core frequency to be significantly higher, N times greater in this case, than the system frequency. The coupled

oscillator circuit 308 is capable of providing a clock signal of varying frequencies.” *Id.* at 6:56–61.

Tam’s technique “can allow for the dynamic adjustment of the core frequency in order to reduce the effects of voltage droop transients.” *Id.* at 7:34–36. Tam explains that:

Embodiments of the present invention can allow for the dynamic adjustment of the core frequency in order to reduce the effects of voltage droop transients. Droops may occur during periods of high activity at specific areas of a die. Power supply variations can also arise from abnormal dI/dt spikes as well as resistive drops in routing. The clock generation system of the present embodiment uses voltage sensors 355 distributed around the processor die. The sensors communicate voltage information to the clock generator 302. Upon receipt of the voltage information, the clock circuitry can evaluate the data and respond accordingly. If any of the sensors indicated that any voltage droops or transients exist, the clock signal can be adjusted to avoid performance errors and to maintain consistent power draw. Thus the processor core 354 can continue to operate despite non-optimal voltage conditions at certain locations on the die.

Id. at 7:34–50.

Tam states:

The examples . . . have been described in the context of a single processor. In a multiprocessor system, the method can be performed concurrently in each processor. Each processor can contain an adaptive variable frequency clock system. For example, each processor can be adjusting its own frequency and voltage settings independent of the other processors in the system. However, the overall system software may have the capability to control all of the processor either through a hardware pin or software inputs.

Id. at 13:12–20.

2. *The Alleged Obviousness of Independent Claim 1 Over Tam*

For reasons discussed below, Petitioner has shown a reasonable likelihood that it would prevail in establishing unpatentability of independent claim 1 as obvious over Tam.

a. *[IPre] A method of circuit control, comprising:*

Petitioner contends that, “to the extent the preamble is limiting, Tam discloses a method for circuit control.” Pet. 12 (footnote omitted) (citing Ex. 1004, code (57) (Abstract), 2:30–40, 3:67–4:5, 14:42–49 (claim 8 directed to a method); Ex. 1003 ¶ 58). In particular, Petitioner asserts “Tam discloses a circuit ‘control technique,’ i.e., method, that ‘implements on-die voltage sensing’ to ‘detect voltage fluctuations and reduce the operating frequency as needed to match the detected VCC voltage decrease.’” *Id.* (citing Ex. 1004, 3:67–4:5, Figs. 7A, 7B). Patent Owner does not raise any arguments regarding these contentions. *See* Prelim. Resp. 14–22, 55–56. We determine that Petitioner has shown sufficiently for purposes of institution that Tam teaches the preamble.

b. *[1a] sensing a delivered voltage to a portion of an integrated circuit;*

Petitioner contends that Tam discloses sensing a delivered voltage to a portion of an integrated circuit. Pet. 13. Petitioner contends that “Tam expressly teaches that its ‘on-die voltage sensors . . . can be strategically placed at various locations’ on an integrated circuit, i.e., portions of an integrated circuit[.]” *Id.* (citing Ex. 1004, 5:46–53, 7:40–41, 14:43, Abstract, Fig. 7B); *see* Ex. 1004, 8:31–36 (“[A] number of voltage sensors are distributed over the integrated circuit to provide supply voltage readings from other circuit locations. These sensors are to detect the voltage of the supply available to the surrounding circuitry and to communicate the voltage

values to the clock generator 408.”). Petitioner further contends that “a POSITA would have recognized that each of Tam’s ‘on-die voltage sensors’ is sensing a delivered voltage to a portion of an integrated circuit, whether it be the ‘FPU,’ ‘L1 Cache,’ processor ‘core,’ or ‘L2 Cache.’” Pet. 14 (quoting Ex. 1003 ¶ 61; citing Ex. 1004, 6:3–7, Fig. 2); *see also* Ex. 1004, 6:3–9 (“[S]ensors . . . are located with or around the FPU 211, L1 cache 212, and IEU 213, respectively, to sense the supply voltages in those regions. These sensors . . . are to detect the local VCC voltage levels . . .”).

Patent Owner does not raise any arguments regarding these contentions. *See* Prelim. Resp. 14–22, 55–56. We determine that Petitioner has shown sufficiently for purposes of institution that Tam teaches the “sensing” limitation 1a.

c. [1b] determining an appropriate frequency for the portion of the integrated circuit; and

Petitioner contends Tam discloses determining an appropriate frequency for the portion of the integrated circuit. Pet 15. Petitioner contends that “Tam teaches ‘[a] method and an apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes.’” *Id.* (citing Ex. 1004, Abstract, 2:30–40) (alteration in original). According to Petitioner, Tam teaches that “after receiving data from voltage sensors associated with a portion of the integrated circuit, such as the processor core, ‘the dynamic frequency adjustment circuit’ can ‘evaluate the supply voltage conditions and dynamically adapt the clock oscillator output,’ i.e., the clock signal/frequency, ‘*appropriately.*’” *Id.* (quoting Ex. 1004, 8:37–40; citing Ex. 1004, 6:33–45, 7:34–35; Ex. 1003 ¶ 62) (footnotes omitted). Petitioner asserts that Tam discloses voltage sensors in the core, and that clock generator 302 provides the appropriate frequency “to the processor core 354,

representing a portion of the integrated circuit.” *Id.* at 15–16 (citing Ex. 1004, Fig. 3; Ex. 1003 ¶ 63); *see also id.* at 15 n.4 (citing Ex. 1004, 5:62–63 (describing Tam’s Figure 2 and stating that “a network of voltage sensors 202 [sic, 203], 204, 205, 206, 207, 208, 209, are distributed in the core 210 and L2 cache 230 to get an accurate and useful view of the power environment.”)). Petitioner further contends that:

“[W]hen a droop is detected” by a voltage sensor located at a portion of the integrated circuit, “the clock is slowed down to accommodate the reduced voltage level. . . . [W]hen the voltage recovery is detected, the clock frequency can be increased to enhance performance.”

Id. at 16 (citing Ex. 1004, 3:44–50, 6:19–23, FIG. 4) (alterations in original).

In the alternative, Petitioner contends that, “[t]o the extent it is determined that Tam does not disclose determining an appropriate frequency for a specific portion of the integrated circuit, it would have been obvious to a POSITA to determine an appropriate frequency for a portion of the integrated circuit.” Pet. 16 (citing Ex. 1003 ¶ 64). According to Petitioner:

For example, it would have been obvious to a POSITA that “a local sensor in a high activity area such as the FPU [located in the processor core] can better indicate the existence of a critical low voltage condition in that circuitry and inform the clock generator of a need to lower the operating frequency” for that portion of the integrated circuit. MTK-1004, 6:12–16; MTK-1003, ¶64. A POSITA would have recognized that doing so would “provide[] an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently.” MTK-1004, 3:51–54. A POSITA would have also understood, based on Tam’s disclosures, that this allows the integrated circuit to “avoid performance errors,” “maintain consistent power draw,” and “continue to operate despite non-optimal voltage conditions at certain locations on the die.” MTK-1004, 7:45-50; MTK-1003, ¶64.

Id. at 16–17 (alterations in original).

Patent Owner argues that “[t]he Petition fails to show that Tam discloses element 1[b] at least because (1) the Petition points to a different structure of Tam to meet element 1[a] than is proposed to meet element 1[b].” Prelim. Resp. 14–15 (brackets in original). Patent Owner asserts that “the claim . . . requires the same structure satisfy both elements.” *Id.* at 15. Patent Owner argues that, for element 1a, “the Petition relies upon Figure 2’s FPU 211, L1 cache 212, L2 cache 230, and core 210 as a portion of an integrated circuit,” but, for element 1b, “the Petition switches to a different embodiment depicted in Fig. 3 and points to ‘rest of core’ 354 as the required portion of the integrated circuit.” *Id.* at 15–16 (citing Pet. 13–17).

We do not agree with Patent Owner’s argument. Petitioner, quoting Tam, contends: “FIGS. 2 and 3 of Tam are not limited to specific embodiments; rather both generally depict a ‘block diagram of a processor . . . in accordance with the present invention’” and “[L]ike references’ in FIGS. 2–3 ‘indicate similar elements.’” Pet. 10 n.2 (citing Ex. 1004, 1:64–66, 5:46–48, 6:33–36; Ex. 1003 ¶ 53) (alterations in original). Patent Owner, on the other hand, does not direct us to any description in Tam of those figures representing two different and independent embodiments, as opposed to descriptions at different levels of detail of the same overall technique. *See* Prelim. Resp. 15–16.

Figure 2 depicts core 210 having therein certain components (e.g., FPU 211) along with their corresponding voltage sensors (e.g., the FPU’s VS203) and including clock generation unit CLU 214. *See* Ex. 1004, 5:57–65, Fig. 2. Figure 3 focuses more on the components of clock generator 302, depicting “rest of core 354” as a box having therein another box labeled

“sensors 355,” with those being “voltage sensors 355 distributed around the processor die.” *See id.*, 7:39–41, Fig. 3. Petitioner, for limitation 1b, maps “portion” to at least processor core 354 of Figure 3 and, in conjunction with that, refers to the “voltage sensors . . . distributed in the core,” namely the voltage sensors depicted in Figure 2 and which were mapped to the “portion” for limitation 1b. *See* Pet. 14 (annotated Figure 2), 15, 15 n.4 (citing Ex. 1004, 5:62–63); *see also id.* at 16–17 (citing Ex. 1004, 6:12–16) (referring to, for limitation 1b, a local voltage sensor in the area of the FPU 211 of Figure 2, which was used in the analysis of limitation 1a).

At this stage and on this present record, we determine that Petitioner has adequately shown that Tam teaches the “sensing” of limitation 1a and the “determining” of limitation 1b involving the same “portion” of the integrated circuit.

Patent Owner also argues Tam “does not disclose determining an appropriate frequency,” and “only discloses determining a frequency or clock speed for the entire integrated circuit and not a portion thereof.” Prelim. Resp. 17. Specifically, Patent Owner argues that, “because Tam’s frequency is for the entire integrated circuit and provides a sub-optimal frequency to any *part of the chip* not *at the same voltage as the sensor driving the frequency change* in Tam, it is not determining an ‘appropriate frequency’ as required.” *Id.* at 17–18 (citing Ex. 2001 ¶ 44; Ex. 1004, 7:48–50) (emphasis added). Patent Owner similarly argues that, “as Tam recognizes, the frequency adjustment for the entire chip *based on one area of voltage droop* will still result in ‘non-optimal voltage conditions at certain locations in the die.’” *Id.* at 17 (citing Ex. 1004, 7:48–50; Ex. 2001 ¶¶ 41, 44) (emphasis added)).

We do not agree with Patent Owner’s argument as, on this record, it does not appear to be commensurate in scope with the language of independent claim 1. Patent Owner impliedly agrees that, in Tam, an “optimum” frequency will be determined for a portion of the integrated circuit chip based on a sensor near that portion—in Patent Owner’s words, the “part of the chip . . . at . . . the sensor driving the frequency change” and the “one area of voltage droop.” *Id.* at 17–18. Patent Owner’s arguments are focused on the appropriateness of the frequency for other portions of the chip. *Id.* Independent claim 1 is directed to only one “portion,” and Patent Owner does not identify a limitation directed to any portion other than the one recited.

Patent Owner additionally argues that “[t]he Petition’s arguments that a POSITA would find these elements [“determining” 1b and “providing” 1c] obvious in view of Tam are conclusory, at best, and fail for a lack of evidence.” Prelim. Resp. 20 (citing Pet. 16, 18); *see id.* at 20–22 (argument under the heading, “Tam does not render any missing element obvious”); *see also id.* at 54–56, 60 (arguing that portions of Dr. Min’s declaration are conclusory and are improperly incorporated by reference into the Petition). Patent Owner argues that “the Min Declaration[] should be given little to no weight because it is nearly verbatim to the Petition and adds no additional analysis or evidence.” *Id.* at 20 (citing Pet. 16–18; Ex. 1003, ¶¶ 64–65). We understand Patent Owner to argue that Petitioner has failed to explain why it would have been obvious to modify Tam to determine an appropriate frequency for and provide that frequency to all portions of the integrated circuit. *See, e.g., id.* at 21 (referring to “the non-optimal conditions that result on the processor by providing a frequency that is not optimal for

certain locations on the processor.”). For the reasons discussed in the previous paragraph, Patent Owner’s arguments against Petitioner’s challenge are based on an incorrect interpretation of the claim. Patent Owner does not identify adequately any specific alleged flaw in Petitioner’s contention that Tam teaches all of the limitations that would require us, at this stage of the proceeding, to determine whether a proposition is too conclusory or is adequately supported by Dr. Min’s declaration. For example, Patent Owner argues that, “in Ground 1 for element 1[b], the Petition relies on the Min Declaration to supply limitations missing from the prior art, including ‘the portion of the integrated circuit.’” *Id.* at 55–56 (brackets in original). However, for the reasons discussed above, we determine that Petitioner has adequately addressed how the *claimed* “portion” is taught by Tam.

We determine that Petitioner has shown sufficiently for purposes of institution that Tam teaches the “determining” limitation 1b.

d. [1c] providing the appropriate frequency to said portion of said integrated circuit.

Petitioner contends Tam discloses providing the appropriate frequency to said portion of said integrated circuit. Pet. 17. Petitioner asserts that, as an example, “Tam teaches that ‘[c]lock generator 302 is to provide an internal processor clock signal,’ i.e., a clock frequency, to ‘the processor core 354,’ i.e., said portion of said integrated circuit, ‘via a clock distribution network 350.’” *Id.* (alternation in original) (citing Ex. 1004, 6:41–44; Ex. 1003 ¶ 65). Petitioner further contends that:

It would have been obvious to a POSITA that Tam’s clock frequency, which is dynamically adjusted by the clock generator in response to voltage variations at a portion of the integrated circuit and is thus an “appropriate frequency for the portion of the integrated circuit,” is provided to that portion of

the circuit via the clock distribution network, as depicted in [the annotated version of Figure 3].

Id. at 18 (citing Ex. 1004, Fig 3; Ex. 1003 ¶ 65). Petitioner, via an annotated version of Tam’s Figure 3, indicates its contention that clock generator 302 provides an “appropriate frequency” to the “rest of core 354,” mapped as a “portion” of the integrated circuit. *See id.*; *see also id.* at 17 (citing, *inter alia*, Ex. 1004, 5:46–6:32 (description of Tam’s Figure 2)).

Patent Owner makes the same or similar arguments for limitation 1c as it did for limitation 1b. Prelim. Resp. 18–22, 56; *see, e.g., id.* at 19 (arguing that Tam does not determine an “appropriate frequency” because “Tam teaches that its changes to the overall clock speed/frequency for the entire chip based on localized voltage values will result in non-optimal conditions within locations of the chip, including a sub-optimal frequency to any part of the chip not at the same voltage as the sensor driving the frequency change.”). We have addressed those arguments above.

We determine that Petitioner has shown sufficiently for purposes of institution that Tam teaches the “providing” limitation 1c.

e. Conclusion as to Independent Claim 1

Having considered the parties’ arguments and evidence, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claim 1 as obvious over Tam.

3. Independent Claim 23

Independent claim 23 recites a system comprising components to perform the same or similar method steps recited in claim 1. *See* Ex. 1001, 8:31–38. Specifically, claim 23 recites a voltage sensor, a logic block, and a circuitry arrangement. *Id.*

Petitioner’s challenge to independent claim 23 relies, in large part, on its contentions regarding independent claim 1. *See* Pet. 26–29. Petitioner also contends that Tam discloses a logic block within its clock generator and a “circuitry arrangement (including the clock generator and/or clock distribution network).” *Id.* at 27–29 (citing, *inter alia*, Ex. 1003 ¶¶ 84–88).

Patent Owner makes the same or similar arguments for claim 23 as it did for claim 1. Prelim. Resp. 22–25, 60. We have addressed those arguments above.

Having considered the parties’ arguments and evidence, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claim 23 as obvious over Tam.

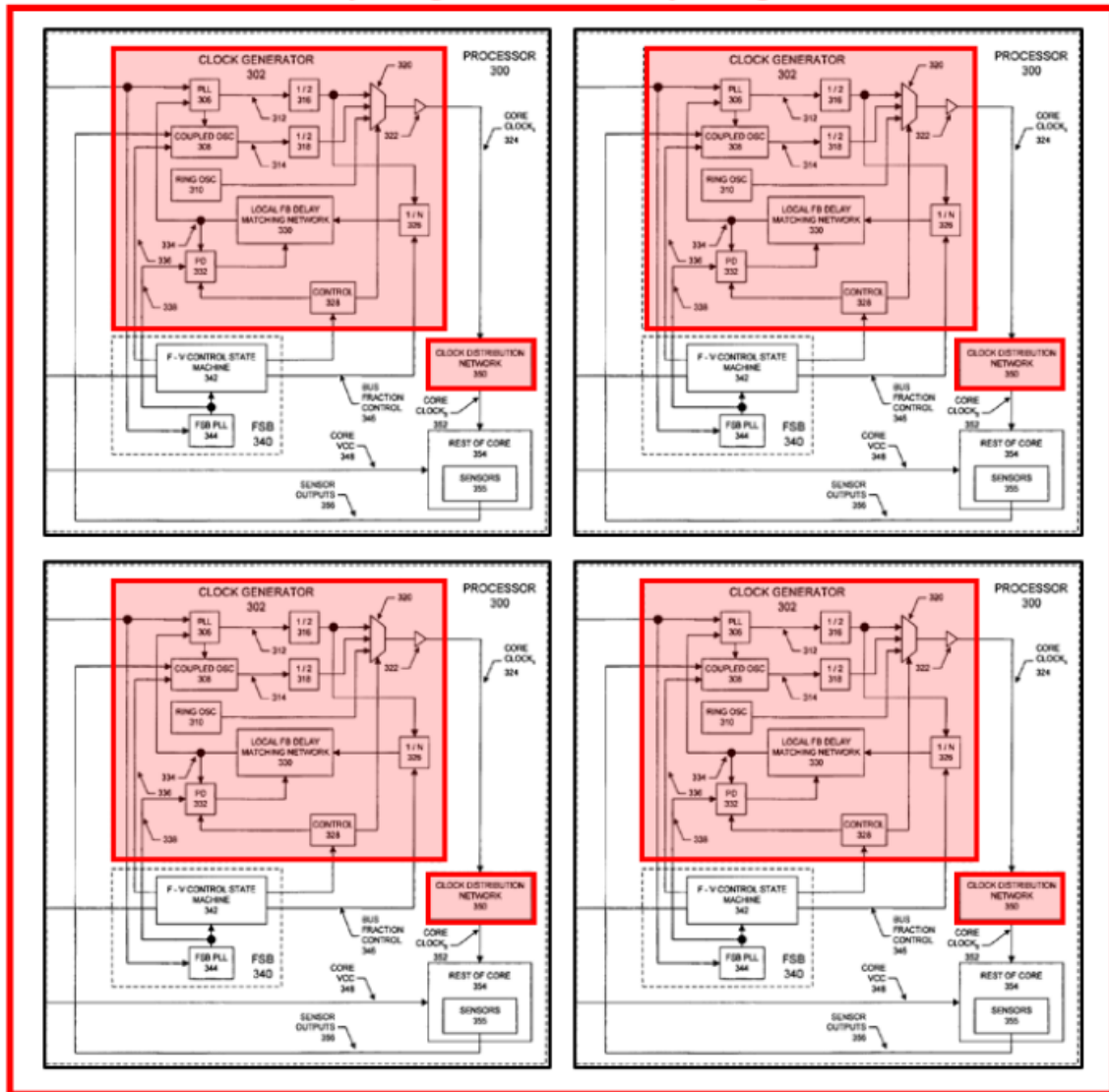
4. *Independent Claim 35*

Independent claim 35 recites “a plurality of voltage sensors arranged to sense a delivered voltage to different portions of an integrated circuit.” Ex. 1001, 9:2–4 (line break omitted). The claim goes on to recite “a plurality of logic blocks” and “a plurality of circuitry arrangements,” both regarding “each said portion.” *Id.* at 9:5–10:4 (line breaks omitted). The parties appear to agree that claim 35 requires the plurality of components to be on a single integrated circuit. *See, e.g.*, Pet. 30 (contending that it would have been obvious to apply Tam’s teachings to a multiprocessor integrated circuit); Prelim. Resp. 29 (arguing that “Tam does not disclose or teach that a multiprocessor system on chip or a multiprocessor system on a single integrated circuit.”).

Petitioner contends that Tam would have rendered obvious independent claim 35. Pet. 30–34. As discussed further below, Petitioner contends that it would have been obvious to include, on a single integrated circuit, more than one of Tam’s processors. *See id.* Petitioner provides

modified and annotated versions of Tam's Figure 3 to assist in explaining its contentions, and we reproduce one of those below.

Plurality of logic blocks / circuitry arrangements



Pet. 33. Above is Petitioner's depiction of how four of the processors illustrated in Tam's Figure 3 would be configured on a single integrated circuit, and annotated to identify the structures mapped by Petitioner as the plurality of logic blocks and circuitry arrangements.

Patent Owner asserts that Tam, in discussing the applicability of the disclosed technique to a multiprocessor system, "describes that 'the overall

system may have the capability to control all of the processor[s] either through a hardware pin or software inputs.” Prelim. Resp. 29 (quoting Ex. 1004, 13:18–20). Patent Owner argues that “[a] POSITA would understand that this is describing communicating with the processors through external pins of an integrated circuit,” and, “[t]hus, a POSITA would understand that Tam is suggesting connecting multiple processors on separate integrated circuits, rather than combining them onto a single integrated circuit, as otherwise the pins would not need to be used. *Id.* at 29–30 (citing Ex. 2001 ¶ 54). Patent Owner further argues that, “[a]ccordingly, a POSITA would not understand that Tam discloses or teaches multiple copies of Tam combined into a single integrated circuit.” *Id.* at 30 (citing Ex. 2001 ¶ 54); *see id.* at 29 (“Tam does not disclose or teach that [sic] a multiprocessor system on [a] chip or a multiprocessor system on a single integrated circuit.”).

We, however, do not understand Petitioner’s challenge to be based on Tam disclosing the entirety of the claimed subject matter and does not rely solely on Tam for an express teaching to modify its system. Rather, Petitioner first contends that “Tam teaches that its circuit control system can be utilized in a multiprocessor environment.” Pet. 30 (citing Ex. 1003 ¶ 93; Ex. 1004, 4:39–42). In that regard, Tam states: “The present embodiment is described in the context of a single processor desktop or server system, but alternative embodiments can [be] included in a multiprocessor system.” Ex. 1004, 4:39–42; *see also id.* at Ex. 1004, 13:12–14 (“The examples above have been described in the context of a single processor,” and “[i]n a multiprocessor system, the method can be performed concurrently in each processor.”). We understand Petitioner to then contend that it would have

been obvious to apply that teaching to the ordinary artisan's knowledge that there existed, at the pertinent time, integrated circuit chips having multiple processors on a single chip. *See* Pet. 30 (citing what we understand to be exhibits purportedly evidencing "known multiprocessor (or multi-core) integrated circuits.")). Patent Owner agrees that single-chip integrated circuits having multiple processors were known, stating that, "[a]t the time of Tam and the '563 Patent, multiprocessor integrated circuits were in their infancy and were not a default choice." Prelim. Resp. 29 (citing Ex. 2001 ¶ 54). We understand Petitioner's contention to be that a person of ordinary skill in the art would apply Tam's technique to a known multiprocessor integrated circuit chip and, in doing so, would replicate, for example, the processor depicted in Tam's Figure 3, on that single chip. *See* Pet. 30–31. According to Petitioner, this modification would result in the claimed subject matter having a plurality of components on "an integrated circuit" as recited in claim 35.

We determine that Petitioner has addressed all of the limitations of claim 35 and provided reasoning adequate at this stage as to why a person of ordinary skill in the art would have made the proposed modification.

Patent Owner additionally makes the same or similar arguments for claim 35 as it did for claim 1. Prelim. Resp. 26–28, 60. We have addressed those arguments above.

Having considered the parties' arguments and evidence, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claim 35 as obvious over Tam.

5. Dependent Claims 2–10, 24, 31, and 32

The remaining claims in this ground depend from one of the independent claims also challenged in this ground. Petitioner presents

contentions as to how each limitation of those claims is taught or suggested by Tam. Pet. 18–26, 29–30. Patent Owner does not present arguments regarding Petitioner’s contentions beyond those already addressed. *See* Prelim. Resp. 14 (“Because the Petition fails to establish a reasonable likelihood regarding each challenged independent claim, it necessarily follows that it also fails to do so regarding all the challenged dependent claims.”). We have reviewed Petitioner’s arguments and evidence in support of its contentions and determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to dependent claims 2–10, 24, 31, and 32 as being obvious over Tam.

*E. The Alleged Obviousness of Claims 1–11, 23, 24, and 31–35
Over Tam and Huard (Ground 2)*

Petitioner alleges that claims 1–11, 23, 24, and 31–35 of the ’563 patent would have been obvious over Tam and Huard. *See* Pet. 34–40 (addressing claim 1). This ground, unlike Ground 1, challenges dependent claims 11, 33, and 34, which pertain to tables associating delivered voltages with appropriate frequencies. *See, e.g.,* Ex. 1001, 7:54–58 (claim 11).

1. Huard (Ex. 1005)

Huard pertains “generally to controlling operating conditions such as clock frequency and supply voltage set point of a circuit, and more specifically to doing so as a function of the operating temperature and instantaneous voltage of the circuit.” Ex. 1005, 1:20–24. According to Huard:

One scenario in which the invention may be advantageous is in applications in which the load circuit has large, sudden swings in the current it draws (di/dt), which cause voltage droop at the power supply. When the load circuit suddenly increases its current draw, the supply voltage V_{cc}

may sag below the value indicated by VID, and the frequency responder lowers the frequency to keep the load circuit within reliable operating parameters. When the current draw lessens, or when the power supply catches up and provides the requested Vcc, the frequency responder reacts and increases the frequency to improve performance.

Id. at 4:39–48.

2. Discussion

In addressing independent claim 1, Petitioner contends that Huard discloses certain claim features that also are disclosed by Tam. *See* Pet. 39–40. For limitation 1b, Petitioner contends that, “[t]o the extent it is determined that Tam does not explicitly disclose determining an appropriate frequency for a specific portion of the integrated circuit, Huard discloses determining an appropriate frequency for the portion of the integrated circuit, e.g., a load circuit,” and contends that “it would have been obvious to a POSITA to use the dynamic frequency adjustment circuit of Tam to determine an appropriate frequency for a specific portion of the integrated circuit (as done by Huard’s frequency responder), in a Tam-Huard combination.” *Id.* Petitioner relies on its analysis of claim 1 in challenging independent claim 23 in this ground. *See id.* at 44. For the reasons discussed above, we determine that Petitioner has demonstrated a reasonable likelihood in prevailing on its challenge to claims 1 and 23 as obvious over Tam alone. We do not reach, at this time, Petitioner’s alternative challenge to the independent claims based on Tam in combination with Huard.

Method claim 11 depends indirectly from independent claim 1 and recites: “using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.” Ex. 1001, 7:54–58. System claim 33 depends

directly from independent claim 23 and recites a table of possible values for voltages and frequencies. *Id.* at 8:62–65. Claim 34 depends from claim 33 and recites that the table is a computer readable database. *Id.* at 8:66–67.

In discussing dependent claim 11, Petitioner (Pet. 42) points to Huard’s disclosure that, “[i]n one embodiment, the voltage responder and the frequency responder can be implemented as lookup tables stored in read-only memory, for example.” Ex. 1005, 4:31–33. Petitioner contends that this reference to being in memory is a teaching of a computer readable database. *See* Pet. 42. Petitioner further contends that “Huard teaches that the frequency responder uses the lookup table, i.e., a tabulation of a set of values, to determine the appropriate frequency for an associated supply voltage.” *Id.* at 42–43 (citing Ex. 1005, claims 15, 22, 23, 36, 37; Ex. 1003 ¶¶ 124–125). Petitioner additionally contends that a person of ordinary skill in the art would recognize that Huard and Tam share certain similarities of components and methodology. *See id.* at 43 (citing Ex. 1004, 8:24–40; Ex. 1003 ¶ 126). According to Petitioner, “it would have been obvious to a POSITA to use Huard’s lookup table, i.e., ‘a tabulation of a set of values,’ in Tam-Huard’s ‘dynamic frequency adjustment circuit’ to determine the appropriate frequency for the voltage delivered to a portion of the integrated circuit.” *Id.* (citing Ex. 1003 ¶ 126); *see also id.* at 37–38 (contentions regarding motivations to combine the teachings). Petitioner relies on this same analysis for dependent system claims 33 and 34. *See id.* at 45.

Patent Owner does not present specific arguments regarding Petitioner’s contentions for these dependent claims. *See* Prelim. Resp. 31 (“Because the Petition fails to establish a reasonable likelihood regarding

each challenged independent claim, it necessarily follows that it also fails to do so regarding all the challenged dependent claims.”).

We have reviewed Petitioner’s arguments and evidence in support of its contentions and determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to dependent claims 11, 33, and 34 as being obvious over Tam and Huard.

*F. The Alleged Obviousness of Claims 1–11, 23, 24, 31–35
Over Norman ’259 and Norman ’851 (Ground 3), and
The Alleged Obviousness of Claims 1, 3, 10, 23, 24, 31, 32, and 35
Over Naffziger ’788 (Ground 4)*

Petitioner alleges that claims 1–11, 23, 24, and 31–35 of the ’563 patent would have been obvious over Norman ’259 and Norman ’851 (Ground 3), and that claims 1, 3, 10, 23, 24, 31, 32, and 35 of the ’563 patent would have been obvious over Naffziger ’788 (Ground 4). Pet. 45–82.

For the reasons discussed above, we determine that Petitioner has shown a reasonable likelihood of demonstrating the unpatentability of all challenged claims of the ’563 patent. Therefore, we institute an *inter partes* review on all challenged claims on all asserted grounds, and we do not review, at this time, Petitioner’s Grounds 3 and 4. *See SAS Inst. Inc. v. Iancu*, 584 U.S. 357, 362, 370–371 (2018); 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). The parties may address further during trial any disputed issues pertaining to Grounds 3 and 4.

IV. CONCLUSION

Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one of the challenged claims of

the '563 patent. Accordingly, we institute an *inter partes* review on all challenged claims on all asserted grounds. *See SAS Inst. Inc.*, 584 U.S. at 362, 370–371; 37 C.F.R. § 42.108(a). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims.

V. ORDER

For the foregoing reasons, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–11, 23, 24, and 31–35 of the '563 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '563 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2024-00599
Patent 7,224,563 B2

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